INVESTIGATION OF TRANSPORT CHARACTERISTICS OF GALLIUM OXIDE FETS AND CARBON NANOTUBE NETWORK BASED FETS FOR EMERGING APPLICATIONS

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INVESTIGATION OF TRANSPORT CHARACTERISTICS OF GALLIUM OXIDE FETS AND CARBON NANOTUBE NETWORK BASED FETS FOR EMERGING APPLICATIONS

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To my parents

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LIST OF SYMBOLS AND ABBREVIATIONS

2-DEG	2-dimensional electron gas
ALD	Atomic layer deposition
BTE	Boltzmann transport equation
CBL	Current blocking layer
CCD	Charge-coupled device
CMOS	Complementary metal-oxide-semiconductor
CNT	Carbon nanotube
COMET	Coupled ordinates method
CRP	Challenge-response pair
DFT	Density functional theory
EEPROM	Electronically erasable programmable read-only memory
FET	Field-effect transistor
FEA	Finite element analysis
FOM	Figure-of-merit
FVM	Finite volume method

HBT	Heterojunction bipolar transistors
HCAFOM	Huang's chip area manufacturing figure-of-merit
HCS	High conductivity section
HCD	High current device
HEMT	High electron mobility transistors
IoT	Internet of Things
LCS	Low conductivity section
LCD	Low current device
MBE	Molecular-beam epitaxy
MOSFET	Metal-oxide-semiconductor field-effect transistor
MOVPE	Metal-organic vapor phase epitaxy
MESFET	Metal-semiconductor field-effect transistor
MWCNT	Multi-wall carbon nanotubes
mfp	Mean free path
PUF	Physically unclonable function
PAE	Power added efficiency
RF	Radio frequency

RIE	Reactive ion etching
SMRTA	Single-mode relaxation time approximation
SRAM	Static random-access memory
SWCNT	Single-wall carbon nanotubes
TBC	Thermal boundary conductance
TBR	Thermal boundary resistance
TCAD	Technology computer-aided design
TTI	Thermoreflectance thermal imaging
UID	Unintentionally doped
WBG	Wide bandgap
C_{th}	Thermoreflectance coefficient
D	CNt network density
E_c	Breakdown field, Conduction band energy
E_g	Band gap
E_v	Valence band energy
e”	Energy of the phonon mode
e^o	Energy of the phonon mode in equilibrium

F	Driving field
f_{MAX}	Maximum oscillation frequency
f_T	Cutoff frequency
$G_{net,n}$	Electron net generation rates
$G_{net,p}$	Hole net generation rates
I_{ds}	Drain-to-source current
J	Current density
J_n	Electron current density
J_p	Hole current density
Kn	Knudsen number
k	Thermal conductivity
k_B	Boltzmann constant
L_{CNT}	CNT length
L_c	Channel length
L_d	Drain contact length
L_g	Gate length
L_s	Source contact length

L_{gd}	Gate-drain spacing
L_{sd}	Source-drain spacing
m_e	Effective mass of electron
N_A	Concentration of ionized acceptors
N_c	Density of conduction band states
N_D	Concentration of ionized donors
n	Electron charge density
P_n	Thermoelectric power corresponding to electrons
P_p	Thermoelectric power corresponding to holes
P_{total}	Total power dissipated by device
p	Hole charge density
q	Electronic charge
$R_{net,n}$	Electron net recombination rates
$R_{net,p}$	Hole net recombination rates
R_{th}	Thermal resistance
S_{vol}	External volumetric heat source
V_{gs}	Gate-to-source voltage

V_{ds}	Drain-to-source voltage
v	Phonon group velocity
v_s	Saturation velocity
T, T_L	Lattice temperature
T_{peak}	Peak lattice temperature in the device
$\hbar$	Reduced plank constant
α	Temperature dependence coefficient of electrical mobility
β	Electric field dependence exponent in mobility model
ε	Dielectric constant, permittivity
λ	Screening length
μ	Electrical mobility
μ_n	Electron mobility
$\mu_{n,low}$	Low-field electron mobility
μ_p	Hole mobility
ρ	Total charge density
ρ_{th}	Percolation threshold density
ρ_{trap}	Trap charge density

τ_{eff} Effective phonon relaxation time

τ_i i^{th} thermal time constant

Φ Electrostatic potential

Φ_b Schottky barrier height

ψ_i Electrostatic potential at the ith section of a CNT

ω Phonon frequency

SUMMARY

Field effect transistors (FETs) are the building blocks of both analog and digital circuits. Silicon is the most widely used semiconductor, but introduction of novel semi-conducting materials with their unique material properties has opened the avenues for significant improvement in many electronic systems. For example, gallium oxide, with its ultra-wide bandgap, can help achieve higher breakdown voltages and switching efficiency, which make it a promising candidate for next generation of RF and power electronics. Similarly, the carbon nanotubes (CNTs) with their superior electrical, thermal, and mechanical properties can help build low-power, transparent, flexible and wearable electronics. This work aims to study the transport characteristics of gallium oxide FETs and CNT network-based FETs to explore the unique challenges and/or opportunities for future applications.

First, the transport characteristics of a random CNT network-based FET has been investigated using a drift-diffusion model. The unique property of randomness of the networks has been used to develop physically unclonable functions (PUFs). PUFs can enable a hardware based cryptographic technique to prevent unauthorized access of electronics devices. CNT-FETs based PUFs offer new security primitives that can be compatible with the various substrates of the next generation of flexible electronic devices. A new multi-gated CNT-FET design has been proposed, which can further enhance randomness and security of the PUF.

In addition, this work has investigated the electro-thermal transport in β-Ga_2O_3 based FETs using a combination of modeling and metrology techniques. Low thermal

conductivity of β-Ga_2O_3 leads to self-heating in its FETs and heat dissipation poses a significant challenge for viability of these devices. Accurate prediction of the electrical and thermal characteristics of these devices is needed for efficient thermal management and device design. A thermodynamic carrier transport device model and 3-D diffusive transport model have been developed to investigate the transport characteristics of these FETs. Ultrafast thermal imaging of the FETs has been performed using a thermoreflectance system to understand the temperature rise at short time scales at different operating voltages. The device level passive thermal management techniques has also been investigated. Boltzmann Transport Equation (BTE) based model has been used to understand the effect of ballistic-diffusive transport and complex phonon-phonon energy exchange mechanisms on thermal transport characteristics of β-Ga_2O_3 thin films and FETs.

CHAPTER 1. INTRODUCTION

Electronics has revolutionized the modern society. It is omnipresent. Semiconductors have played a major role in development of electronics. Several types of semiconductor devices are basic building blocks of various electronic circuits. Field effect transistors (FETs) are the most common type of semiconductor devices present in both digital and analog circuits. They are used for electronic switching, signal amplification, power control, radio frequency applications, etc.

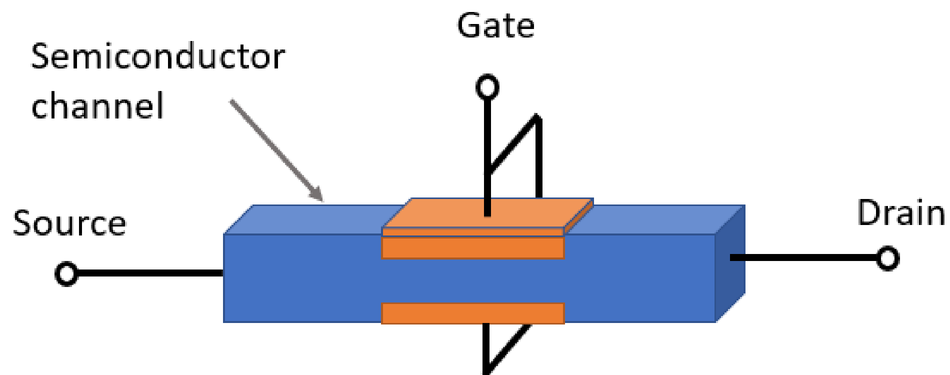


Figure 1.1 A schematic of a Field Effect Transistor (FET).

A schematic of a FET is shown Figure 1.1. FET is a type of transistor in which an electric field is used to control the flow of current in a semiconductor channel. A FET has three terminals—Source, Drain and Gate. Source and Drain electrodes are connected at the two ends of the semiconductor to form a channel for current flow between them. The Gate electrode is placed in the proximity of channel in such a way that, by application of voltage, it can control the current flow. The voltage applied on Gate electrode alters the electric field and density of carriers (electrons and holes) in the channel. In this way, Gate alters

the electric conductivity and current flow of the channel. Silicon is the most widely used semiconductor for channel material in the devices, but the development of novel semi-conducting materials with unique material properties, has opened the avenues for further improvement of the electronic systems. In this work, two such classes of semiconductors are studied because of their unique electrical, thermal and/or mechanical characteristics, which make them suitable for various next generation electronic technologies. First class is 1-D/2-D carbon-based nanomaterials, and second class is wide bandgap materials. In the first class, we focus on carbon nanotubes (CNTs) for their application in low-cost, high-performance, flexible, and wearable electronics. In the second class, we focus on β-Ga_2O_3 for their application in RF and power electronics. In the following sections, we discuss the advantages, challenges and opportunities offered by CNT and β-Ga_2O_3 based devices.

1.1 CNT based Electronics

CNTs are one of the allotropes of carbon. They are long cylindrical tubes of very high aspect ratio and made of carbon atoms arranged in hexagonal structure. CNTs can have a single layer, known as single-wall nanotubes (SWCNTs), or multiple layers, known as multi-wall nanotubes (MWCNTs), of carbon atoms (see Figure 1.2). Diameters of CNTs typically vary from less than a nanometer to several tens-of-nanometers. CNT lengths can vary from less than a nanometer to several centimeters. Due to their unique structure and strength of carbon atom bonds, CNTs can exhibit remarkable mechanical, thermal, optical, and electrical properties. CNTs possess exceptional flexibility and elasticity under large strain and bending. The Young's modulus and tensile strength of CNTs are reported to be around 1 TPa and 100 GPa, respectively [1]. Thermal conductivities of SWCNTs and MWCNTs are measured to be as high as 3500 W/m^2K [2] and 3000 W/m^2K [3],

respectively. The orientation of hexagonal structure of a CNT layer with respect to tube axis, which is known as chirality, render the layer metallic or semiconducting [4]. MWCNTs are usually metallic, whereas SWCNTs can be metallic or semiconducting. Semiconducting SWCNTs can have charge-carrier mobility as high as 100,000 cm^2/Vs [5]. The mechanical, thermal, and electrical properties of semiconducting SWCNTs are extraordinary and significantly better than those of silicon. Thus, semiconducting SWCNTs (hereafter referred to as CNTs) are promising candidate to be used as channel material in transistors and have potential to surpass silicon in performance and utility in several areas of application.

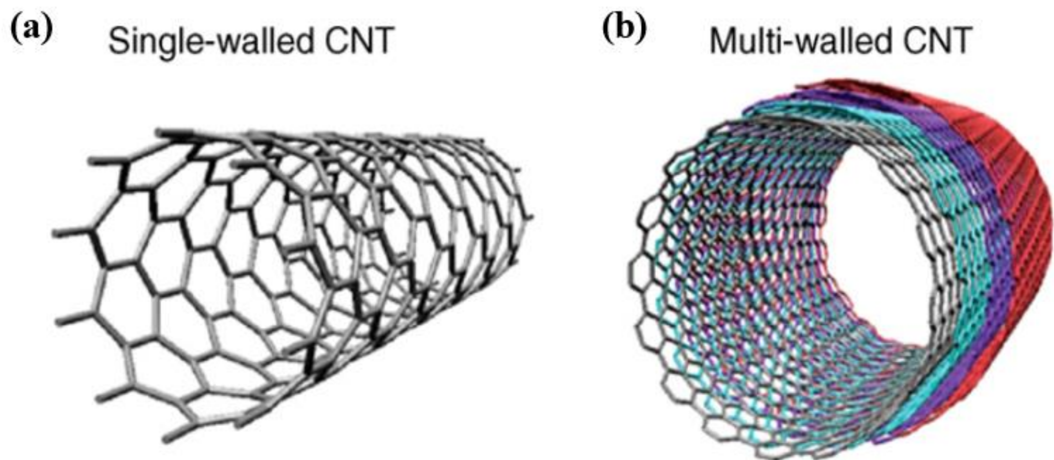


Figure 1.2 Structure of (a) a single-walled carbon nanotube and (b) a multi-walled carbon nanotube. Reprinted from [6]. Copyright (2010), with permission from Elsevier.

In the past, CNTs were only used as a bulk material in batteries, automotive parts, coating, etc. for their mechanical properties. However, in recent years, CNTs have been extensively studied for application in beyond Si based complementary metal-oxide-semiconductor (CMOS) electronics, flexible and transparent devices, RF electronics,

sensors, displays, light-emitting devices, thermal interface material, etc. The usage of CNTs as a channel material in transistors is one of the most exciting areas of application. One major advantage of CNTs over other potential next generation electronics technology is that it is compatible with existing FET architecture. So far, the continued dimensional downscaling has led to tremendous improvements in Si based micro/ nano- electronics. But this approach has reached close to its full potential. Therefore, due to their exceptionally high current carrying densities and mobilities, CNTs are considered as a potential replacement for Si in next generation micro/nano-electronics. First transistor based on a single CNT was demonstrated in 1998 [7]. Since then, normalized current density of 2.41 mA/µm [8] and field effect mobility of 79,000 cm^2/Vs in single CNT transistors have been achieved, which are significantly higher than Si devices [5]. Even though single CNT based devices have shown significant improvement in performance over Si devices, these devices may not be a viable technology at production scale, at least in the near future. This is due to poor device-to-device reproducibility, which can be attributed to inability to control CNT orientation, diameter, spatial locations etc., to synthesize electronically homogeneous CNTs [4, 9].

On the other hand, FETs with thin films of CNT networks are easy to fabricate and have less performance variability compared to individual CNT FETs [4, 9]. CNT films are optically transparent, bendable and can withstand large strains [10]. They are compatible with flexible substrates [11]. These properties make them an attractive candidate for flexible/stretchable and transparent electronics. In fact, various studies have already demonstrated the application of CNT thin films in flexible/stretchable electronic devices, such as integrated circuits [12], sensors [13], displays [14], etc. CNT network based thin

film transistors (TFTs) are believed to be the most viable and realistic application of CNTs in electronics in the near future [4, 9]. TFTs are a key component of macroelectronics, flexible/stretchable and optically transparent systems. They are widely used in display backplanes, flexible integrated circuits, and sensors [15]. Amorphous silicon (a-Si), polycrystalline silicon and organic semiconductors are the most widely used TFT channel materials. a-Si is the most mature TFT channel material, but it suffers from low mobility

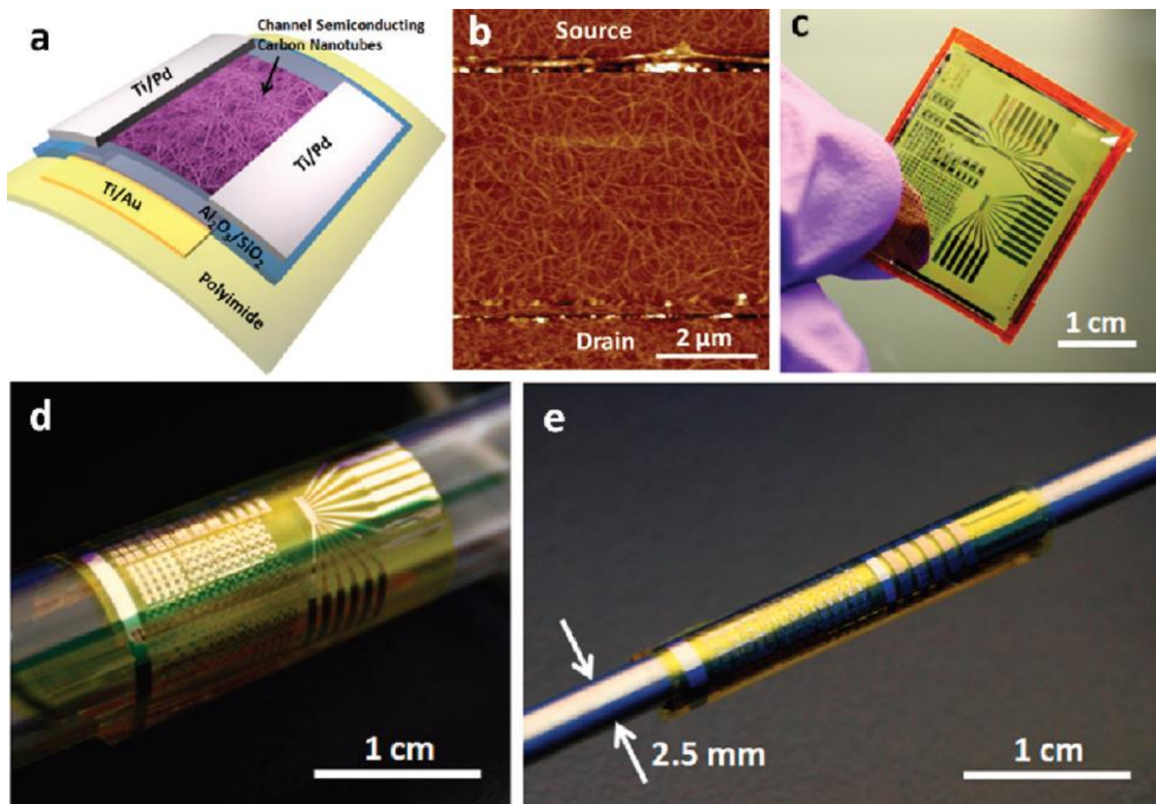


Figure 1.3 Flexible thin-film transistors and integrated circuits using semiconducting carbon nanotube networks. (a) Schematic diagram of a local gated nanotube TFT on a flexible substrate. (b) AFM image showing the channel of the flexible nanotube TFT, which consists of random networks of semiconducting carbon nanotubes. (c) Photograph of a flexible nanotube circuit with a size of ~2.5 × 3 cm^2. (d, e) Photographs showing the extreme bendability of the flexible nanotube circuits, where the samples are being rolled onto a test tube with a diameter of 10 mm (d), and a metal rod with a diameter of 2.5 mm (e). Reprinted with permission from [10]. Copyright (2012) American Chemical Society.

(~ 1 cm^2/Vs) [16, 17]. Both a-Si and polysilicon have poor transparency and flexibility. On the other hand, organic TFTs have excellent flexibility and low-cost fabrication but their device performance is poor (mobility ~ 1 cm^2/Vs) [16]. CNT films have achieved much higher carrier mobilities (~ 100 cm^2/Vs), better flexibility and transparency, and better stability in the air [18-20]. In addition, these films can be deposited at low temperatures, which makes them compatible with low-cost, flexible plastic substrates [12, 19]. Another promising feature of CNT TFTs is that they can be produced in large volumes and at low-cost using printing processes [11]. Inkjet printing has been widely used to produce the CNT TFTs based integrated circuits [21, 22]. Thus, CNT films can overcome all the major challenges in producing low-cost, high-performance flexible and macro electronics. Overall, we can say that, in the short term, CNTs are better suited to be high performance and low-cost replacement of organic semiconductors and a-Si in flexible devices and macroelectronics rather than to be a replacement of Si in micro/nano-electronics.

1.2 Ultra-wide Bandgap Semiconductor: β-Ga_2O_3

Wide bandgap (WBG) semiconductors refer to the semiconductors with a significantly wider bandgap (usually > 3 eV) than the conventional semiconductors such as Si (1.12 eV). The WBG material-based devices can operate at higher voltages, temperatures, and frequencies. These capabilities make the WBG semiconductor devices more efficient, faster, and smaller compared to the Si based counterparts for power and RF electronics applications [23]. The major areas of application of WBG power devices are automotive, transportation, consumer electronics, energy storage and distribution as

illustrated in Figure 1.4 [24]. The RF devices are mainly used in radars, wireless communication, and connectivity systems, etc. [25].

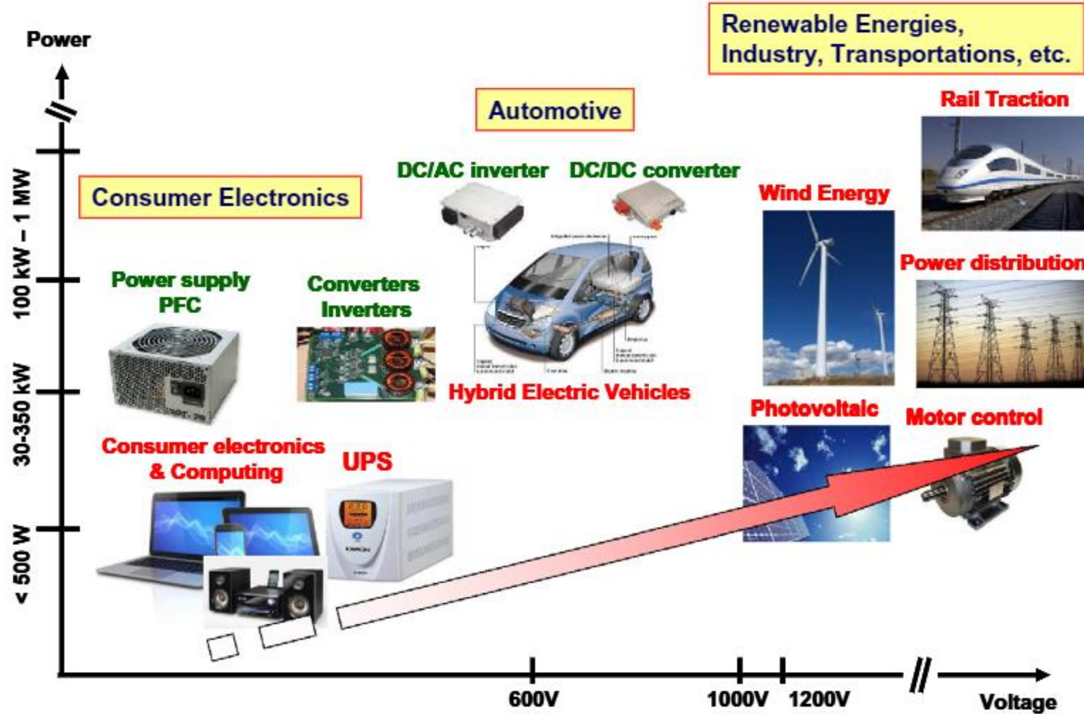


Figure 1.4 Major application areas of WBG power devices in a plot of the power vs voltage operation range. Reprinted from [24]. Copyright (2010), with permission from Elsevier.

The key advantage of WBG materials is that the wider bandgap help achieve the higher critical electric field strength [26]. The dependence of critical electric field strength on bandgap is shown in Figure 1.5 (a). Various figures-of-merit (FOMs), which are used to estimate the relative efficacies of different semiconductors, non-linearly scale with critical field strength [27]. WBG semiconductors such as SiC (Eg ~ 3.25 eV) and GaN (Eg ~ 3.4 eV) have emerged as an alternative to Si based devices. But, recently, β-Ga_2O_3 has shown potential to become an even better alternative due to its ultra-wide bandgap (Eg ~

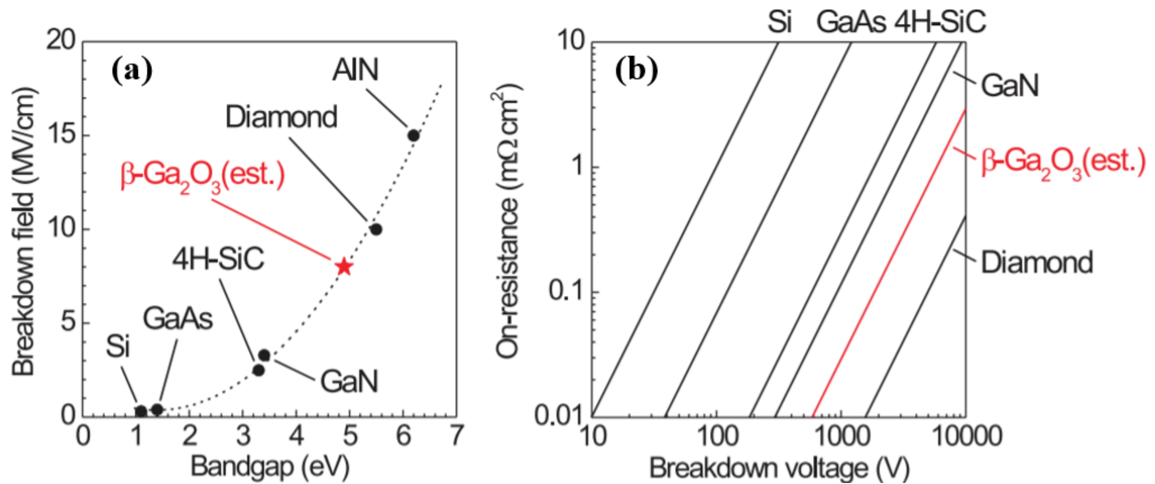


Figure 1.5 (a) Dependence of critical electric field on bandgap and (b) theoretical limits of on-resistance at given breakdown voltages for various materials. Reprinted from [28], with the permission of AIP Publishing.

4.8 eV). The theoretically predicted critical electric field strength of β-Ga_2O_3 is 8 MV/cm, which is significantly higher than that of GaN (3 MV/cm) and SiC (2.5 MV/cm) [27, 28]. Figure 1.5 (b) shows how theoretical limits of on-resistance vary with breakdown voltage for different semiconductors. For a given on-resistance, β-Ga_2O_3 devices can achieve larger breakdown voltage compared to Si, SiC and GaN. Additionally, bulk crystals of GaN and SiC produced using vapor growth techniques whereas large wafers of β-Ga_2O_3 can be produced using melt growth techniques, which give it cost advantage over GaN and SiC [26].

Ga_2O_3 forms several different polymorphs such as the rhombohedral (α), monoclinic (β), defective spinel (γ), cubic (δ), or orthorhombic (ε) structures. β-Ga_2O_3 is the most stable among these polymorphs under normal conditions [26, 29]. It is the only polymorph which remains stable though the entire temperature ranges up to its melting point. So, bulk single crystals of β-Ga_2O_3 can be grown using high temperature processes such as melt growth techniques due to its thermal stability [26]. Its availability and thermal stability make it

the most studied polymorph of Ga_2O_3. The crystal structure of β-Ga_2O_3 is base-centered monoclinic, as shown in Figure 1.6, and the space group is C2/m. Each conventional unit cell has 4 Ga_2O_3 formula units, i.e., total 20 atoms. The lattice constants are, a = 1.22 nm, b = 0.30 nm, c = 0.58 nm. The monoclinic angle (β) is ~ 104º and the other two angles (α = γ) are 90º [30]. In each unit cell, there are two inequivalent gallium atom sites (Ga(I), Ga(II) and three inequivalent oxygen atom sites (O(I), O(II) and O(III)). There are two types of coordination for Ga ions—tetrahedral and octahedral. The Ga(I) ions are located at tetrahedral sites and surrounded by 4 oxygen atoms. The Ga(II) ions are located at octahedral sites and surrounded by 6 oxygen atoms. The O(I) and O(II) ions are surrounded

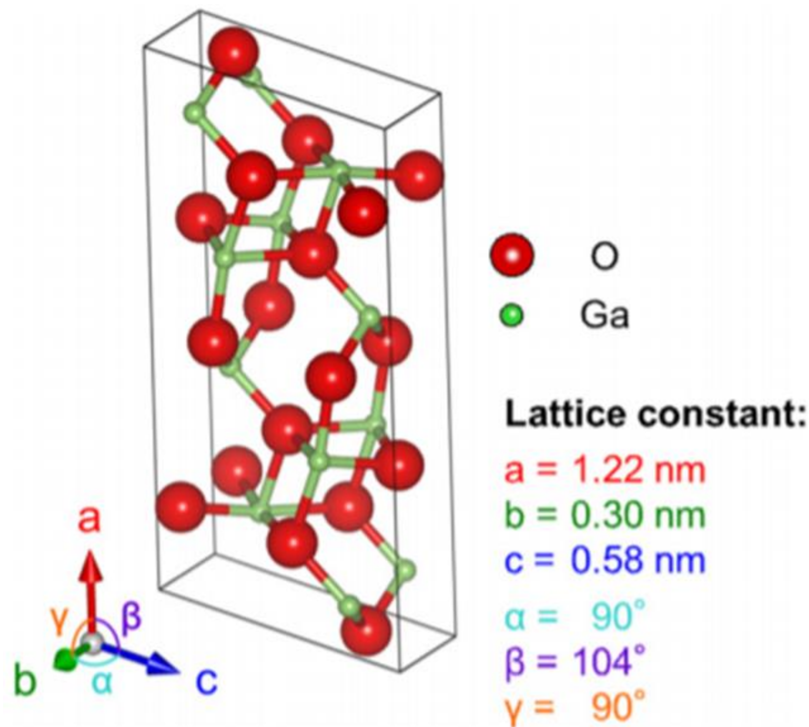


Figure 1.6 β-Ga_2O_3 crystal structure reproduced from [30]. © IOP Publishing. Reproduced with permission. All rights reserved.

by 3 gallium atoms, whereas the O(III) ions are surrounded by four gallium atoms [26, 30, 31]. This has important implication on material properties. Various theoretical and experimental studies have shown anisotropy in material properties of β-Ga_2O_3 [32-35].

Table 1.1 compares the key properties and figure of merits (FOMs) of β-Ga_2O_3 to other widely used semiconductors to highlight its advantages and challenges for different type of applications. FOMs are function of material properties such as critical electric field (Ec), mobility (μ), dielectric constant (ε), saturation velocity (vs), etc. Baliga's FOM and Huang's material FOM estimate dc conduction losses and dynamic switching losses [26, 27]. Higher values of these FOMs for β-Ga_2O_3 compared to Si, SiC and GaN shows its potential for high-power and high-frequency applications. The switching frequency (f) varies as a function of E_c^2 at a specified power loss, thus higher critical field strength is desirable for power conversion in GHz regime. Johnson's FOM is a metric of power-frequency capability for RF applications [26, 27]. The large value of electron saturation velocity (~ 2 x 10^7 cm/s) enable high current density and operating frequencies. Huang's chip area manufacturing FOM (HCAFOM) is a metric of manufacturability and cost of large area substrate availability [26, 27]. HCAFOM of β- Ga_2O_3 is 3 and 6 times larger than that of SiC and GaN, respectively. However, the thermal conductivity of β-Ga_2O_3 is significantly lower than other semiconductors compared in Table 1.1. The high-power density combined with low thermal conductivity leads to self-heating effects and high temperatures in β-Ga_2O_3 based devices. Performance, reliability, and lifetime of the devices are adversely affected by operating at higher temperatures. Therefore, it is important to understand not only the electrical but also thermal characteristics of these devices. We need to address the thermal management issues in addition of electrical issues

to realize the ultimate potential of β-Ga_2O_3. β-Ga_2O_3 based devices have capabilities to dramatically improve efficiency industrial processes, consumer electronics. They can accelerate widespread use of electric vehicles and renewable energy and improve next generation communication systems and radar technology.

Table 1.1 Comparison of important properties and FOM of β-Ga_2O_3 with other widely used semiconductors [26, 27]. The FOM are calculated relative to Si.

	Si	4H-SiC	GaN	*β*-Ga_2O_3
Band gap, E_g (eV)	1.1	3.25	3.4	4.8
Electron mobility, μ ($cm^{-2}V^{-1}s^{-1}$)	1480	1000	1250	300
Breakdown field, E_c (MV/cm)	0.3	2.5	3.3	8
Dielectric constant, ε	11.8	9.7	9	10
Saturation velocity, v_s (10^7 cm/s)	1	2	2.5	1.8–2
Thermal conductivity, k (W/m K)	150	370	230	10–30
Baliga's FOM = $\varepsilon \mu E_c^3$	1	317	846	3214
Johnson's FOM ($E_c^2 v_s^2/4\pi^2$)	1	278	1089	2844
Huang's material FOM ($E_c\mu^{0.5}$)	1	7	10	12
Huang's chip area FOM ($\varepsilon Ec^2\mu 0^{.5}$)	1	48	85	279
Huang's thermal FOM ($k/\varepsilon E_c$)	1	0.36	0.1	0.01

1.3 Outline of the Work

The aim of this work is to study the electric/thermal transport in CNT network-based and β-Ga_2O_3-based FETs to FETs to explore the unique challenges and/or opportunities for applications in next generation electronics.

Chapter 2 includes review of the previous work pertinent to the work done in this thesis and summarizes the significant contributions of the current work. Chapter 3 covers the methodology employed to achieve the objectives of this thesis. A novel design of PUF has been proposed in the chapter 4. This design is based on CNT FETs, which is expected to be low-cost, and compatible with flexible electronics and have significantly higher level of entropy. A 2-D electrothermal model is developed using TCAD Sentaurus and effect of bias conditions on Joule heat generation profile, electric field, current density, and peak temperature is studied in chapter 5. A 3-D diffusive thermal model is developed using Ansys Fluent to accurately predict the temperature distribution in the device in chapter-6. The thermoreflectance imaging is used to validate the diffusive thermal model and measure thermal characteristics such as thermal resistance, thermal time constants, etc. Phonon transport in β-Ga_2O_3 thin films and FETs is investigated using steady-state non-gray Boltzmann Transport Equations (BTE) with single mode relaxation time approximation in chapter 7. Finally, chapter 8 summarizes the work done in this thesis and scope of the future work.

CHAPTER 2. BACKGROUND AND CONTRIBUTIONS OF THE CURRENT WORK

This chapter revisits the relevant past works, which are available in the literature, and how they motivated the work done in this dissertation. First, the importance and need of better security primitive for future electronics is highlighted. Then the idea of CNT FET as a security primitive is proposed and evaluated. Second, recent progress in β-Ga_2O_3 devices for power and RF electronics is discussed. Then, the challenges in realizing full potential of these device and gaps in the literature are highlighted. These challenges and gaps serve as a motivation for the current work done on these devices.

2.1 Application of CNT Network FETs in Hardware Security

In Chapter 1, it was highlighted that CNT thin film FETs can be a low-cost, high-performance, and scalable alternative to a-Si, polysilicon, and organic FETs for application in flexible/stretchable, transparent and/or wearable electronics. In this section, application of CNT thin film transistors in hardware security is proposed and investigated. First, challenges faced by existing cryptography techniques are highlighted. Then, a new cryptographic technique is described. Several instances and designs, known as physically unclonable functions (PUFs), based on this technique are discussed. Finally, the need and advantage of CNT based PUFs, and existing CNT based PUF is discussed.

2.1.1 Challenges in Hardware Security

Usage of electronic devices has increased exponentially in the last few decades and this is expected to further rise due to the rapid growth of Internet of Things (IoT). It has

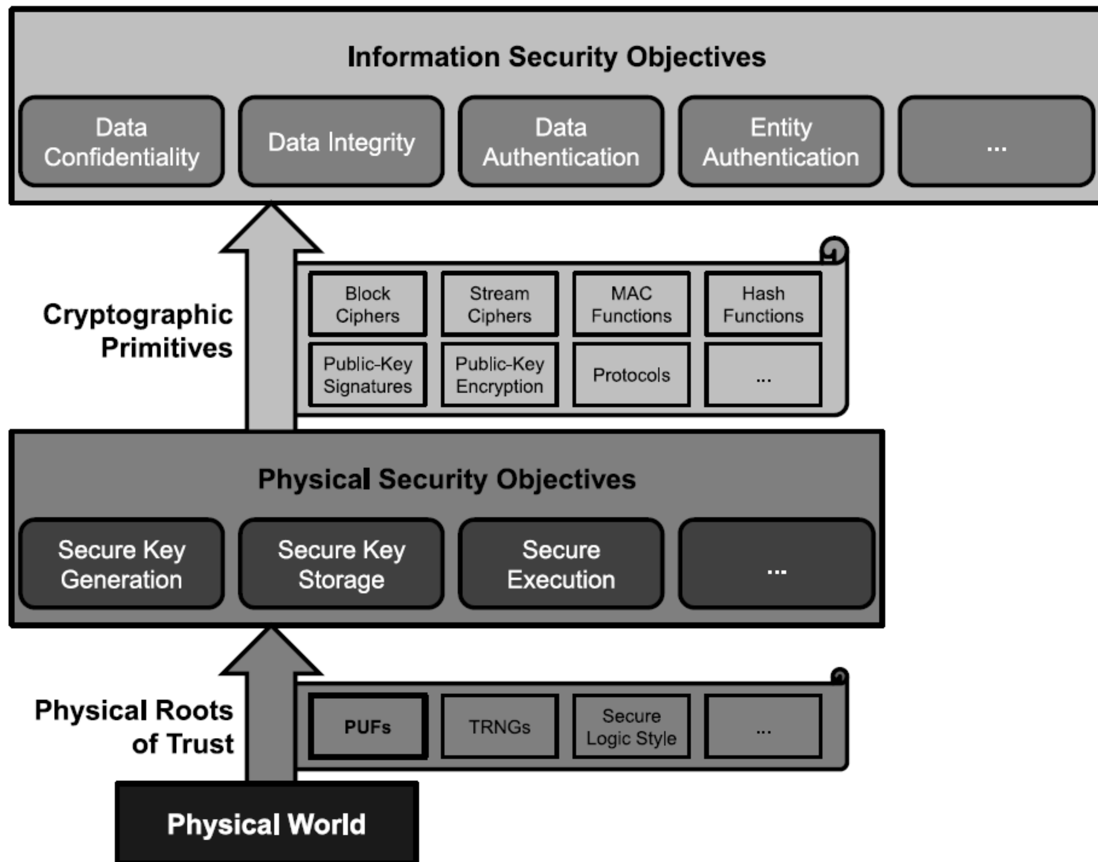


Figure 2.1 A Relation between information security, cryptography, physical security, and physical roots of trust. Reprinted by permission from [36]. © Springer Nature COPYRIGHT (2013). All rights reserved.

made transfer of data and information very fast and simple but increased the risk of privacy and security breach. The field of cryptography deals with the development and analysis of techniques and algorithms to achieve the goal of information and data security. There are several cryptographic techniques to secure data, but most of the cryptographic primitives use 'keys'. Ideally, they should be able to generate random and unique keys as well as securely store, retrieve, and use these keys as an input into an encryption algorithm to encrypt the data without revealing any information about the keys. However, these tasks are not simple. Previous studies have reported that many security systems have poor key

generators, which make them vulnerable [37, 38]. Lenstra et al. [37] analyzed a very large set of public keys and showed that some of those keys did not possess sufficient level of randomness and offered little security. In addition, these keys are usually stored in a non-volatile digital memory, e.g., Electronically Erasable Programmable Read-Only Memory (EEPROM). The keys are stored permanently in the memory even when the device is powered off. Thus, keeping them secure also becomes a challenge as physical, fault and side-channel attacks (e.g., power consumption, execution time) can be used to steal the keys [39-41]. Torrance and James [42] were able to steal security keys and encryption algorithm from a well-secured IC. The security keys were stored in EEPROM. This work highlights that it is possible for a competent and well-equipped adversary to breach the security measures implemented in EEPROM to steal the security keys.

2.1.2 Physically Unclonable Functions (PUFs)

Given the drawbacks of storing the keys in non-volatile digital memory, a radical new approach to key storage is needed. Physically Unclonable Functions (PUFs), physical root-of-trust cryptographic primitives, are a promising new approach to overcome the challenges associated with key storage in the digital memory. Figure 2.1 illustrates how objective of information security is achieved using physical root-of-trust cryptographic primitives such as PUF. The PUF concept is based on the fact that, usually on small length scales, many physical systems cannot be replicated or cloned, even if all the parameters in the fabrication process are constant. Each instance of the physical system is known as PUF instance and as the name suggests, cannot be replicated due to their complex physical properties and inherent randomness associated with small length scales. Usually, this instance-to-instance variation is considered disadvantageous in manufacturing. For

example, in semiconductor industry, chips and devices are designed in such a way that small uncontrollable manufacturing variations does not affect their electronic behavior during operation. However, PUFs turn these instance-to-instance variations into an advantage and utilize them to generate cryptographic primitives.

Each instance of a PUF receives external stimuli (inputs), which are known as challenges. Depending upon the PUF type, a PUF can have only one or multiple challenges [43, 44]. A PUF which can only support one or a few challenges is called Weak PUF, whereas a PUF which can support an extremely large number of challenges is called Strong PUF. After receiving a challenge, a PUF generates a response (output) (see Figure 2.2). A challenge and its corresponding response are usually referred as challenge-response pair (CRP). A PUF acts as a black box and the response of each instance for a given challenge will be unique and unpredictable as the physical phenomenon or parameter rendering the response cannot be controlled to produce only a particular type of response. These different types of responses can be associated with different bit values and multi-level (e.g., binary, ternary) keys can be generated using multiple PUFs together to secure data from the external attacks. Thus, PUF tackles the need of random key generation and storage together.

There are several advantages of PUF over the digital memory based cryptographic techniques. In the conventional digital memory storage approach, keys are permanently stored in digital form. On the other hand, PUF-response is derived only when required and, therefore, available in digital form for a very short span of time [44]. An additional circuit, which is continuously powered on, is added to digital memory to prevent, and detect tampering/stealing of the permanently stored key. It increases cost and design area [44]. In

addition, non-volatile digital memory fabrication is expensive process. It requires additional mask steps during manufacturing, which increases the cost of the device. Since PUFs do not require non-volatile digital memory for key storage, they are cheaper, less power consuming and can also be used in the systems, which do not have non-volatile digital memory. PUFs can also be used in other applications e.g., secure RFID systems [45], IP protection [46], device authentication [47].

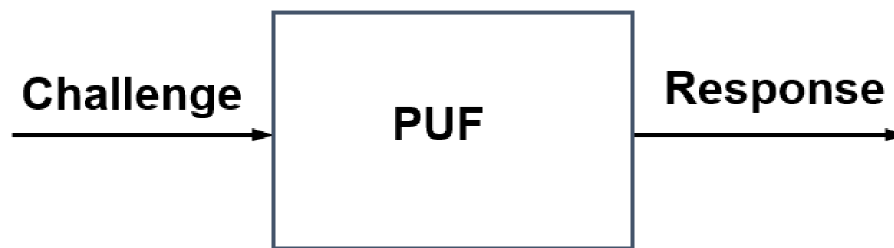


Figure 2.2 A PUF acts as a black box. For a given challenge (input) and it produces a unique and unpredictable response (output).

2.1.3 Existing PUFs

Several PUF designs have been proposed in the past that exploit electronic, optical, magnetic and many other properties of materials. Pappu et el. [48] proposed one of the first PUFs and called it Physical One-way Function. It was an optical PUF based on optical microstructure, which was made up of randomly mixed microscopic refractive particles in a transparent epoxy plate. When a laser beam is passed through this microstructure, the beam scatters multiple times from the refractive particles and generates a random speckle pattern. The location and polarization of the laser is considered the challenge and the speckle pattern is considered the response. The pattern was then converted to binary key using image processing technique known as Gabor transform. Even though optical PUF satisfied various requirements of a PUF such as unclonability, uniqueness, unpredictability

etc. of output, it requires large, complex, and expensive external measurement systems. The reliability of the PUF strongly depends on some very accurate measurements. In addition, it cannot be integrated in resource constrained systems. Since the PUFs are used for security purposes in electronic devices, electronics based PUF design, which can be easily integrated in an IC, are desired.

Several electronic PUFs have been proposed over last two decades. Gassend et al. [49, 50] proposed one of the first Silicon based PUF, which was initially called Physical Random Function but later renamed as Arbiter PUF (APUF). Manufacturing variabilities in gate delays are the source of randomness. There are two identical signal processing paths, but time delays are different on the two paths due to random silicon process variations. Both signals are received by an arbiter circuit, which can determine which of the two signals reached first and generate a binary output accordingly. Like the Optical PUF, the APUF satisfies all the major requirements and properties of a PUF but it has been demonstrated that APUF is susceptible to modeling attacks. To address this, several variations of APUF with a more complex architecture, have been proposed such as XOR-APUF, lightweight PUF and the feed forward APUF. In addition, APUF is susceptible to environmental effects such as temperature, supply voltages, etc. If the delays in two signals is very small, then response will not be stable and additional mechanism for bit-error correction will be needed.

Another type of electronic PUF, known as Ring Oscillator PUF (ROPUF) is also delay based PUF. There are several variations of ROPUF, all are based on the measurement of random variations in oscillation frequencies of digital circuits. Like the APUF, source of unclonable randomness in ROPUF is also the silicon process variations. Gassend et al.

[51] proposed the very first design of ROPUF. ROPUF also uses gate delays and create an oscillator by feeding back the delay output in the line. However, like APUF, ROPUF response can also be affected by the environmental parameters such as temperature, input voltage, etc. Gassend et al. [51] proposed a compensation technique to address this issue and make the response more stable. In addition, it was also susceptible to modeling attacks and several variants were proposed to address the shortcomings of the initial design. Suh & Devadas [47], Maiti & Schaumont [52, 53], Maiti et al [54, 55], and Yin & Qu [56] proposed significant improvement in ROPUF design and post-processing.

Both APUF and ROPUF exploit the random variation in the gate delays. There are also other physical properties, which can be used to design PUFs. There is another prominent category of electronic PUFs, which are based on the settling states of digital memory cells. Static Random-Access Memory (SRAM) is one of the most well-known memory based PUF. The first SRAM PUF was proposed by Guajardo et al. [46] and simultaneously a very similar design was proposed by Holcomb et al. [57]. When a voltage is applied to memory cells, i.e., when memory is powered on, each cell can go any of the two possible logical states— '0' and '1'. However, which state a particular memory cell will store, is random and depends upon manufacturing variability. A positive feedback loop pushes the cell into one of the states and help maintain that state as well. Thus, a random binary key can be generated.

Besides the aforementioned PUFs and their variations, some of the other conventional PUF designs include Magnetic PUF [58], Coating PUF [59], Bitline PUF [60], Glitch PUF [61], Latch PUF [62], Flip-flop PUF [63], Butterfly PUF [64], current-based PUF [65], Nonlinear current mirror based PUF [66], Buskeeper PUF [67], Bitstable

Ring PUF [68], etc. In the past, among all the PUF types, silicon PUFs have attracted the most interest. Because they can be easily integrated into standard digital circuits and deployed as a security primitive faster. Almost all silicon PUFs exploit the random manufacturing variations in physical properties but these variations follow a gaussian distribution [69]. Therefore, most of the variations are clustered around the mean value and the instance-to-instance variations are very small for significant number of PUF instances. The bit generated based on the small mismatches can be easily disturbed by noise or environmental factors such as temperature, supply voltage, etc. and lead to bit-errors. It necessitates the implementation of bit-error correction mechanism and post-processing to reduce the bit-error rate. The additional data-processing increases the silicon area and cost. In addition, for many applications, we may be moving from conventional silicon-based electronics toward nano-materials based flexible, transparent, wearable and faster electronics [12, 70-73]. Nanomaterial-based devices can help reduce power consumption and cost and are compatible with various new substrates used for the next generation of electronic devices. New security primitives, which are compatible with the next generation non-silicon electronics are desired.

CNT is one of the nanomaterials with huge potential for next generation electronics. CNT based PUFs have been proposed and even fabricated in recent years [69, 74]. Hu et al. [69] fabricated devices on lab-scale where CNTs are selectively self-assembled into HfO_2 trenches to create open and closed connections, which are associated with bit values '0' and '1' respectively. They also showed ternary key generation by further differentiating between semi-conducting and metallic CNT closed connections. It was not clear how to control the yield of semi-conducting and metallic CNT connections to maximize the

randomness in ternary keys. Each instance had only one challenge, which also limited randomness and level of security. In addition, these trenches were of nanometer scale and large-scale production may not be reliable and economically viable. This has motivated us to further explore CNT based structures with inherent randomness for novel CNT PUF designs, which are reliable, low-cost, and compatible with flexible, transparent, and wearable electronics.

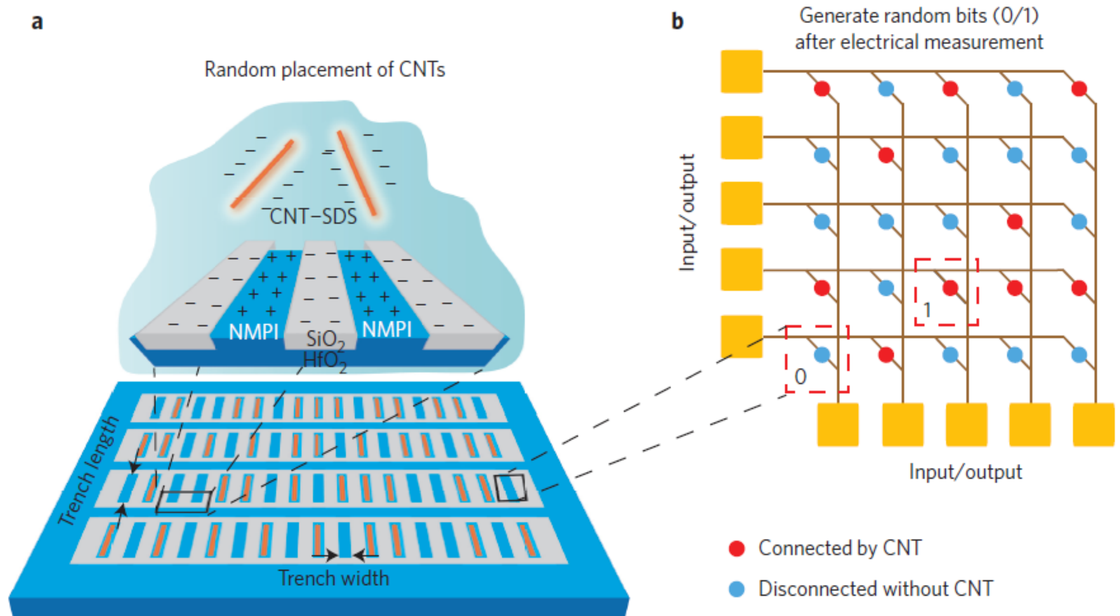


Figure 2.3 Random bits based on a 2D carbon nanotube array. (a) Schematic of chemical self-assembly of the CNTs in the HfO_2 trenches modified by a monolayer. The self-assembly was realized through ion exchange between Na^+ in SDS and I^- in NMPI. The width of the HfO_2 trenches varies from 70 nm to 300 nm. (b) Schematic of a randomly connected 2D CNT array featuring a 5 × 5 crossbar structure. Reprinted by permission from [69]: © Springer Nature COPYRIGHT (2016). All rights reserved.

2.1.4 CNT Network FET as a PUF

Random CNT network based thin film FETs have received significant attention for their applications in logic circuits, e-displays, sensors, flexible and wearable electronics

etc. [9]. There is significant progress made in fabrication, purification, and large-scale controlled integration of ultra-thin films of random CNT networks. Printed CNT networks FETs have also been demonstrated [11]. Printing has potential to significantly reduce the cost and make large scale production viable. However, device-to-device performance variability, which is rooted in the randomness of CNT network, poses a significant challenge. Chen and Kumar [75] fabricated the CNT network FETs and studied the variability in output characteristics as shown in Figure 2.4. On the other hand, the device-to-device variability in electrical characteristics provides a novel opportunity of their application in cryptography. The inherent randomness of CNT network can be exploited to create a novel PUF design. This PUF design can be used as security primitive in low-cost, flexible, transparent, and wearable electronics. It can be used for user authentication, unique device identity generation and unauthorized access prevention in the IoT devices, wearable medical devices, etc.

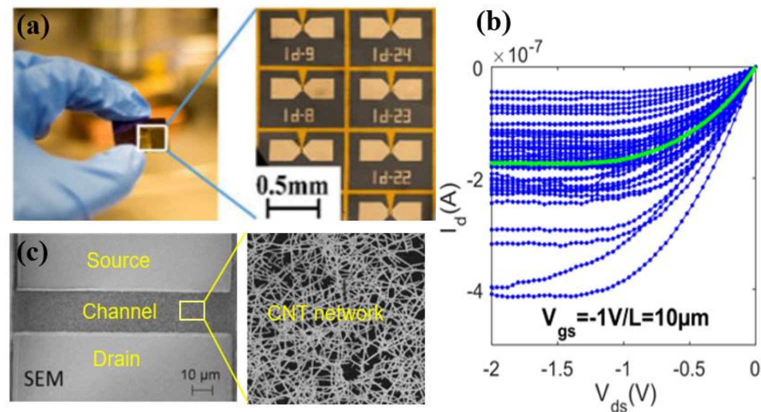


Figure 2.4 (a) Fabricated CNT network FETs (b) Measured output characteristics of various fabricated CNT network FETs of channel length =10 μm, width = 100 μm and CNT network density = 13 per μm^2. The device-to-device variation in I-V characteristics can be attributed to random CNT network channel (c) SEM image of a CNT network FET and random CNT network channel. Reprinted from [75]. Copyright © 2018, IEEE.

2.2 β-Ga_2O_3 for Power and RF Electronics

The material properties of β-Ga_2O_3 were discussed in detail in the chapter 1. The wider bandgap of β-Ga_2O_3 help it achieve significantly higher critical field strength compared to other widely used wide bandgap materials such as GaN and SiC. The significant advantage of β-Ga_2O_3 over GaN and SiC in power and RF electronics are evident through various figures of merit such as Baliga's figure of merit, Johnson's figure of merit etc. [26]. The excellent electrical properties will enable β-Ga_2O_3 devices to operate at higher temperatures and voltages with higher efficiency. It will help make power electronics module more powerful and efficient. High-quality bulk crystals of β-Ga_2O_3 can be produced at low cost using melt growth techniques, which makes it very attractive for large-scale adaptation in many technologies. The aforementioned advantages have significantly increased the interest of scientific community in β-Ga_2O_3.Various β-Ga_2O_3 devices have been developed and significant improvement in the fabrication technology and device characteristics has been achieved. Next, we discuss various important milestones and progress made in β-Ga_2O_3 based FETs so far, and the major challenges and issues, which still need to be addressed to realize the full potential of β-Ga_2O_3 in power and RF electronics.

2.2.1 β-Ga_2O_3 FETs: Progress and Achievements

The first transistor using single crystal β-Ga_2O_3 was demonstrated by Higashiwaki et al. [28] in a metal–semiconductor field-effect transistor (MESFET) structure. A Sn-doped n-type β-Ga_2O_3 buffer layer of thickness 300 nm was grown on a Mg-doped semi-insulating β-Ga_2O_3 (010) substrate fabricated by molecular-beam epitaxy (MBE). The gate

length is 4 μm and spacing between source and drain is 20 μm. Ohmic contacts of Ti (20 nm)/Au (100 nm) at source and drain were formed using reactive ion etching (RIE) treatment, which help in reducing the contact resistance. Schottky contact at gate were formed by Pt(15 nm)/Ti(5 nm)/Au(250 nm) deposition. The cross-sectional and top view of the MESFET are shown in Figure 2.5. The maximum drain current (I_{DS}) was reported to be 26 mA/mm at a gate voltage (V_G) = 2 V and drain voltage (V_D) = 40 V. The breakdown voltage at the off-state was reported to be 257 V at V_G =- 30 V. A voltage higher than breakdown voltage resulted in catastrophic failure in the device as gate electrode burned. The maximum transconductance was reported to be 2.3 mS/mm at (V_D) = 40 V. The on/off I_{DS} ratio was around 10^4 and drain leakage current in off-state was 5 μA/mm. The two main issues with the device are—high contact resistance and low on/off ratio. Still, it was a remarkable first demonstration of potential of β-Ga_2O_3 for power electronics. All the device characteristics of this MESFETs are comparable to or better than those of initial GaN MESFETs. Higashiwaki et al. [76] further developed this depletion mode (D-mode) MESFET into a D-mode MOSFET to further improve the device characteristics.

In recent year, several D-mode FETs have been designed, which demonstrated significant improvement in device characteristics such as maximum drain current, on/off ratio, breakdown voltage, critical field strength, power density, etc. Green et al. [77] developed MOVPE-Grown Sn-Doped β-Ga_2O_3 MOSFETs and achieved breakdown strength of 3.8-MV/cm, which is higher than the theoretical limits of field strength of bulk GaN and SiC. Also, this was highest measured critical field strength in lateral FETs and around half of the theoretical field strength of β-Ga_2O_3. The current on/off ratio as high as

10^{10} has been reported [76, 78, 79]. Wong et al. [80] demonstrated field-plated D-mode MOSFETs with off-state breakdown voltage higher than 750 V. Mun et al. [81] achieved a breakdown voltage of 2.32 kV in β-Ga_2O_3 MOSFETs, which is highest value achieved in lateral β-Ga_2O_3 devices. Moser et al. [82] reported a pulsed current density of 478 mA/mm and power density of 47.8 W/mm in Sn-doped β-Ga_2O_3 MOSFETs grown by MBE. Zhou et al. [79] demonstrated record high 1.5 A/mm drain current by utilizing a highly doped β-Ga_2O_3 nano-membrane as the channel in D-mode β-Ga_2O_3 on insulator FETs with minimal self-heating effects. The current density in these devices was comparable to that in GaN/GaAs based device [83]. Noh et al. [84] achieved power density of 64.7 W/mm in β-Ga_2O_3 Nano-Membrane FETs using high thermal conductivity diamond substrate. β-Ga_2O_3 FETs demonstrated to have stable operation up to at least 300 ºC temperature range [76, 80]. Enhancement mode (E-mode) FETs are highly desirable in power electronics applications as they enable normally off operation. Normally off operation reduces circuit complexity and helps in safe operation in power electronics. Chabak et al. [85] fabricated Sn-doped gallium oxide wrap-gate E-mode fin-array FETs on a semi-insulating Mg-doped (100) β-Ga_2O_3 substrate. These devices achieved a breakdown voltage greater than 600 V at V_G=0. Zhou et al. [79] achieved maximum drain current of 1 A/mm and current on/off ratio of 10^{10} in E-mode β-Ga_2O_3 Nano-Membrane FETs.

So far, most of the FETs demonstrated by researchers are lateral devices. However, for high voltage and high power applications, vertical structures are expected to be more suitable because they can utilize chip area more efficiently and device operation is stable under surface defects [26]. In recent years, two main types of vertical β-Ga_2O_3 transistors have been developed—current aperture vertical MSOFETs and vertical fin-channel

MOSFETs. Wong et al. [86] used a Mg-implanted current blocking layer (CBL) in current aperture vertical transistor design. Further, both D-mode [87] and E-mode [88] MOSFETs were demonstrated with N^{++} CBLs. Hu et al. [89, 90] fabricated first vertical fin-channel MOSFETs. These were single fin, normally off MOSFETs, which could achieve a breakdown voltage of 1.6 kV, drain current density of 10 A/mm^2 and current on/off ratio of 10^9. Li et al. [91] further improved this design, introduced multi-fin design and the record breakdown voltage of 2.66 kV was achieved.

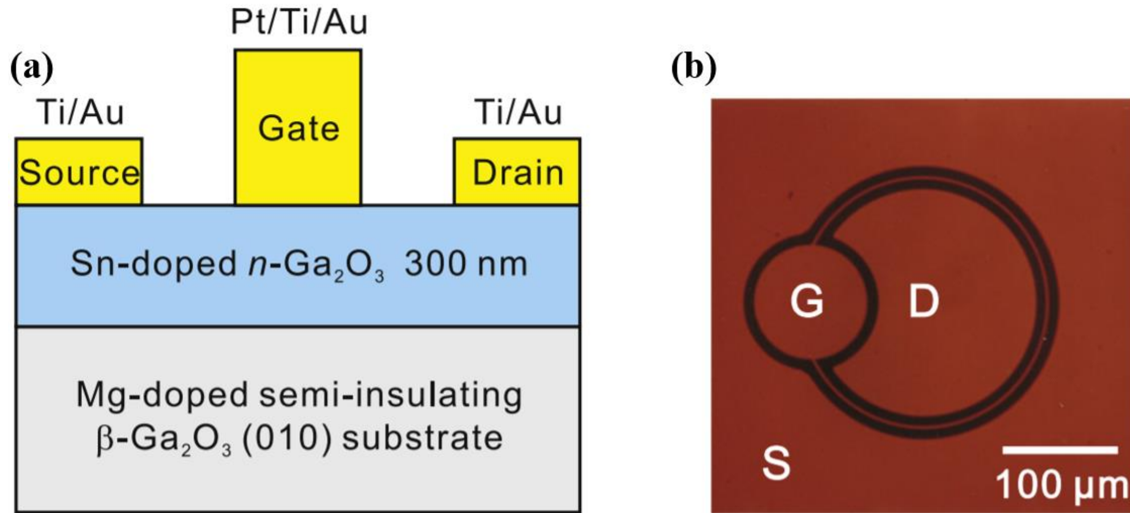


Figure 2.5 (a) Cross-sectional view and (b) top view of the β-Ga_2O_3 MESFET demonstrated in [28] Reprinted from [28] , with the permission of AIP Publishing. Copyright 2012, AIP Publishing LLC.

The high saturation velocity of β-Ga_2O_3 combined with extremely high electric field strength, which is 2.5 times of GaN devices, indicates high potential for RF applications. First ever β-Ga_2O_3 MOSFET for RF operation was demonstrated by Green et al. [92]. A silicon-doped β-Ga_2O_3 was homoepitaxially grown on a semi-insulating β-Ga_2O_3 (100) substrate by metal-organic vapor phase epitaxy (MOVPE). The gate length was 0.7 µm and spacing between source and drain is 3.8 µm. The maximum current density and

transconductance of 150 mA/mm and 21 mS/mm, respectively, were measured during dc operation. The device achieved extrinsic cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of 3.3 and 12.9 GHz, respectively, during small signal RF operation. The large signal measurements at 800 MHz of output power, power gain and power added efficiency (PAE) were reported to be 0.23 W/mm, 5.1 dB and 6.3%, respectively.

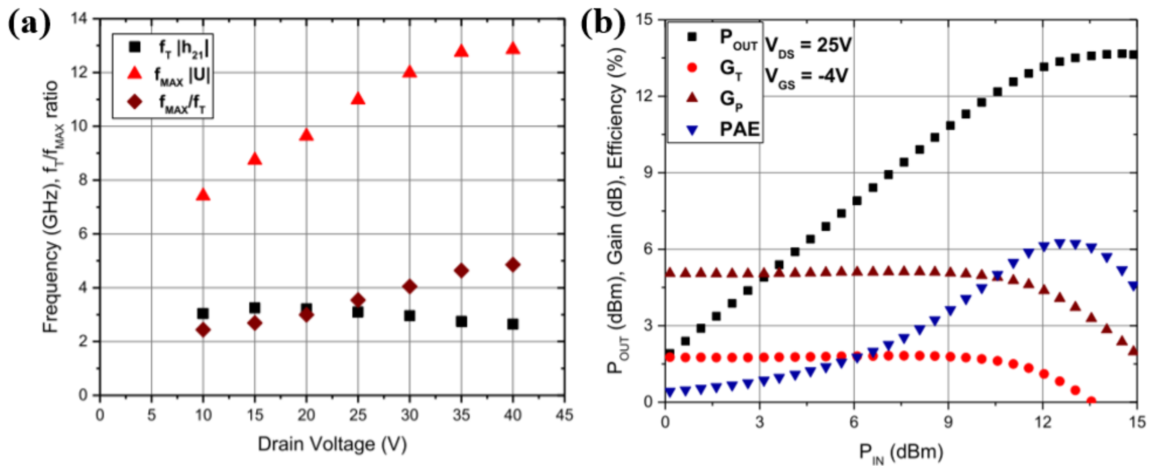


Figure 2.6 (a) Cutoff frequency (f_T) and maximum oscillating frequency (f_{MAX}) as a function of drain bias. Each measurement was taken with the gate contact biased with the gate voltage corresponding to peak transconductance. (b) 800 MHz Class-A power sweep of a 2 × 50 µm β-Ga_2O_3 gate recessed MOSFET. Reprinted with permission from [92]. Copyright © 2017, IEEE.

Chabak et al. [93] demonstrated two MOSFETs—gate recessed MOSFET and thin-channel with T-gate MOSFET, for RF applications. Thin-channel MOSFET achieved a significantly higher f_T =5.1 GHz and f_{max} =17.1 GHz using vertical channel scaling and small gate-length in T-gate design. Recently, Xia et al. [94] demonstrated a delta-doped β-Ga_2O_3 MESFET with 120 nm gate-length and achieved f_T of 27 GHz. There are very limited β-Ga_2O_3 RF devices exist in the literature, but significant progress have been made in a very short span of time by scaling the gate length. Further progress in operating voltage

and frequencies is expected. In future, β-Ga_2O_3 RF devices may be used in the applications where integrated power conversion and RF circuits are required [95].

2.2.2 *β-Ga_2O_3 FETs: Multiscale Electrothermal Modeling and Measurements*

In recent years, several β-Ga_2O_3-based FETs have been developed and a significant improvement in some of the parameters such as breakdown voltage, cut-off frequency, on/off ratio, contact resistance, maximum drain current, etc. have been reported. However, efficient heat removal is still one of the biggest challenges for these devices due to low thermal conductivity. Green et al. [92] have observed temperature induced catastrophic failure. The thermal conductivity of β-Ga_2O_3 depending upon the crystal direction varies between 10 and 29 W/mK at room temperature [32, 33, 96]. It is significantly lower than that of GaN (150 W/mK) and 4H-SiC (370 W/mK). The issue of efficient heat dissipation should become even more critical in the future devices with a further increase in power density. Since, electrical performance of the device is dependent upon the temperature, both electrical and thermal characteristics of these devices should be investigated simultaneously.

2.2.2.1 TCAD Device Modeling

Technology computer-aided design (TCAD) device modeling is an important tool to predict spatial and/or temporal profile of various electrical and thermal quantities of interest such as electric field, potential drops, current density, temperature, carrier density, Joule heat generation, etc. of a device. In TCAD modeling, finite element models are used to solve electrostatics (Poisson's equation), carrier transport, heat transport equations to predict the aforementioned quantities at various device operating conditions. A model

validated against experimental measurements can improve our scientific understanding of the material and device physics. In addition, the model can help in investigating the effect of various device parameters such as doping concentration, dopant type, channel length, gate length, etc. on various physical quantities such as breakdown voltage, switching speed, electric field distribution, peak temperature, etc. and in designing devices with optimum performance. TCAD modeling is widely used in semiconductor industry for cost-reduction and the development of silicon technology. Thus, it is critical to develop TCAD models for β-Ga_2O_3 devices to improve scientific understanding and enable low-cost, fast improvement in device performance without expensive and time-consuming trial-and-error experiments.

So far, only few studies have focused on understanding the electrothermal characteristics of these devices using TCAD modeling. Wong et al. [97] and Russell et al. [98] have performed electro-thermal simulations of β-Ga_2O_3 based MOSFETs using a temperature-dependent mobility model. Wong et al. compared the experimental and computed I-V data at a single gate-to-source voltage (Vgs) = 0 V. They reported channel temperatures of the device at various power dissipations (Vgs= 0 V and $10 \leq$ drain-to-source voltage (Vds) ≤ 35 V) but their correlation with current density and electric field were not investigated. Russell et al. showed that using 4H-SiC instead of semi-insulating β-Ga_2O_3 as substrate may improve electrical and thermal characteristics of the FETs. They have computed I-V characteristics at various bias voltages but did not attempt to validate it against the measurement. Therefore, a TCAD model, which is validated against experiments and over multiple operating conditions across several Vgs and Vds values, is needed for gaining trustworthy insight into the physics and improvement in device design.

2.2.2.2 3-D Diffusive Thermal Model and Coupling with 2-D TCAD Model

Even though TCAD modeling is an effective tool to predict device characteristics, 3-D TCAD modeling is impractical from computational cost and time perspective, and, thus, rarely used. The device size in various dimensions can go up to a few microns and mesh resolution requirement, where gradients of electric field, carrier density, doping, current density, etc. are high, is of sub-nanometer scale. 2-D TCAD modeling have been the preferred approach. 2-D TCAD models, where only a cross-section of the device is simulated, have a significantly smaller number of elements and nodes and the computational cost and time become more practical. 2-D models can predict electrical characteristics with required accuracy as demonstrated and verified in various studies in the literature [99, 100]. However, 2-D model may not provide accurate temperature distribution in the device, especially for the devices with small gate width. A 2-D TCAD model can over-predict the actual temperature because the heat dissipation in third dimension is not considered. Therefore, a 3-D thermal model is needed to predict the temperature distribution in the device. The Joule heat generation profile from TCAD modeling can be provided as an input in the 3-D thermal model. Singh et al. [101] and Chatterjee et al. [102] have predicted peak temperature of β-Ga_2O_3 MOSFETs using numerical simulations. In addition to temperature prediction, 3-D thermal models can be used to study the effectiveness of various device level thermal management techniques.

2.2.2.3 Device-level Thermal Management

The thermal conductivity of Fe-doped β-Ga_2O_3 substrate is not good enough to take full advantage of β-Ga_2O_3 material properties in the devices. Several device-level

thermal management techniques have been developed for GaN devices in the past. These techniques are also applicable for β-Ga_2O_3 devices. [26, 103, 104]. Dumka et al. demonstrated that GaN devices grown on diamond substrate could achieve significant higher power density compared to GaN on silicon substrate devices [103]. Therefore, various studies have investigated integration of β-Ga_2O_3 thin films on high conductivity substrates such as SiC, diamond to address the issue of thermal management and increase power density in β-Ga_2O_3 devices [105-108]. However, thermal boundary conductance (TBC) can introduce significant thermal resistance at the interface. Cheng et al. integrated β-Ga_2O_3 thin films on SiC substrates by the ion-cutting technique and room-temperature surface-activated bonding technique and measured a TBC between 67-100 MW/m^2 K. Nepal et al. [105] demonstrated heteroepitaxial growth of β-Ga_2O_3 films on 4H-SiC substrate via molecular beam epitaxy and measured an improved TBC 140 ± 60 MW/m^2 K at the interface. Cheng et al. also integrated of β-Ga_2O_3 films with diamond by atomic layer deposition (ALD) and van der Waals bonding to show the potential of diamond in improving heat dissipation. Weak van der Waals bonding method introduced significantly lower TBC (17 MW/m^2 K) compared to ALD integration method (TBC ~ 179 MW/m^2 K). Therefore, it is important to account for TBC at the β-Ga_2O_3 and substrate interface while estimating the temperature distribution in the device. Russell et al. [98] studied the effect of introducing SiC substrate but it is not clear if TBC has been included. Another approach to improve the heat dissipation could be the addition of a surface passivation layer of a high thermal conductivity material. Traditionally, passivation layers are used to improve electrical characteristics of the device, make the device surface inert and avoid interaction between the surface and air or other materials in contact [76, 109]. However, the selection

of a high thermal conductivity passivation layer can also help in thermal management by providing additional paths for heat dissipation.

2.2.2.4 Thermo-reflectance Imaging

In addition to electro-thermal simulations, thermal measurements are also crucial to investigate thermal characteristics. Thermal measurements can be used to validate and calibrate thermal models of the devices. There are a few temperature measurement techniques that have already been used in the literature. Simms et al. [110] and Wong et al. [97] have used electrical methods to measure the steady-state temperature of β-Ga_2O_3 based MOSFETs. This technique measures the average temperature over the channel region, thus, tends to underestimate the actual peak temperature [110, 111]. Therefore, thermal simulations will still be needed to estimate the peak temperature of FETs. Raman thermography have also been used recently to measure steady-state peak channel temperature[111]. Raman thermography is a single-point measurement technique and, therefore, unfavorable for temperature mapping. In addition, transient measurements using Raman thermography may be challenging due to its sensitivity to mechanical stress [112]. It may not be suitable for capturing both spatial mapping and transient temperature change across a device simultaneously. Besides, to the best of our knowledge, the transient measurements of β-Ga_2O_3 FETs have not been reported yet. Both steady-state and transient temperature distribution with high temporal and spatial resolution is important for understanding the thermal characteristics of devices relevant to power and RF applications. Thermoreflectance imaging has emerged as a promising alternative, which can provide temperature profile with submicron temporal and spatial resolution [113]. It is a non-invasive and non-contact imaging technique. This technique has successfully been used to

measure spatial and temporal variation in temperature profile of various power and RF devices with sub-micron features such as Gallium Arsenide (GaAs) high electron mobility transistors (HEMTs), GaN HEMTs, GaN heterojunction bipolar transistors (HBTs) [112-115]. Therefore, application of this technique can be easily extended to β-Ga_2O_3 based power and RF devices.

2.2.2.5 Phonon Transport in β-Ga_2O_3 Films and Devices

Another important aspect of accurate thermal modeling and thermal behavior prediction is the size and dimensions of the devices. At smaller length scales, diffusive transport model may not predict the thermal transport accurately [116]. Heat transport in β-Ga_2O_3 is dominated by phonons [32, 96]. Phonons are quantized lattice vibrations [117]. As the dimension of the system approaches the same order as of the phonon mean free path (mfp), ballistic transportation of the phonons also need to be considered. The heat transport is no longer purely diffusive, and Fourier's law may give erroneous results [118]. Therefore, a thermal transport model is needed, which can account for ballistic effects at smaller length scales and recover bulk diffusive behavior at larger length scales. Several types of models and techniques have been developed to study the thermal transport at smaller length scales such as atomistic modeling using molecular dynamics, mesoscale modeling using Boltzmann transport equation (BTE), etc. The semi-classical BTE is applicable when phonon wavelength is significantly smaller than characteristic lengths of the device. The wave nature of the phonons can be ignored and phonons can be treated as semi-classical particles [119, 120]. The semi-classical phonon BTE has been widely used to describe the thermal transport in semiconductor devices [121-123]. This approach can also be used for β-Ga_2O_3 devices.

Phonon BTE is solved in both physical space of the geometry and wave-vector space of the phonons. The complex inter-phonon scattering terms needs to be computed over the entire wave-vector space which make solving it very expensive and time-consuming for microscale geometries. A widely used approximation for the complex full scattering term is single mode relaxation time approximation (SMRTA), which allows implementation of phonon BTE for complex geometries with heat source and different boundary conditions. The main limitation of this approximation is that it cannot account for momentum conserving scattering (Normal processes). However, these processes are only important at significantly lower temperatures than room temperatures. The effect of Normal processes is negligible at room temperature and SMRTA agrees well with experiments. Several studies have employed SMRTA successfully to study heat transport in the semiconductor devices including wide bandgap devices [119, 121, 123, 124]. Several other simplifications are also proposed such gray BTE, semi-gray BTE. Gray and non-gray models incorporate single group velocity and relaxation time [125]. They can account for ballistic effects and boundary scattering. However, they cannot predict temperature accurately because all the polarizations and full phonon dispersion are not considered. Narumanchi et al. [126] compared gray and semi-gray BTE models against non-gray BTE model with full phonon dispersion and showed these models gives erroneous results. Several other studies have solved BTE dispersion and polarization effects are considered [121, 127, 128].

However, solving non-gray BTE model with full phonon dispersion involves for all the phonon modes in each physical cell. It requires solving a large number of equations simultaneously and makes the non-gray BTE modeling computationally expensive. In the conventional solution approach, known as sequential method, a phonon mode is chosen

and solved over entire physical domain before moving to the next phonon mode. However, this method suffers from slow convergence at low Knudsen numbers (Kn = phonon mean free path/characteristic length) because of the increased amount of phonon scattering can tightly couple the discrete equations [119]. Loy et al. [119, 129] developed an alternative method, known as Coupled Ordinates Method (COMET). In the COMET, the process is reversed, and all the phonon modes are solved in a cell before moving to the next cell. For Kn <1, COMET is 233 times faster than sequential method for non-gray BTE [119]. Even though at high Kn, sequential method is faster than COMET, the total simulation time is relatively smaller while using COMET because domain size is smaller compared to the effective mean free path of phonons. So, the improvement in solution time is inconsequential. Therefore, COMET is the better approach to solve the non-gray BTE for β-Ga_2O_3 devices, where most of the phonon modes have mean free paths smaller than the device characteristics lengths.

2.3 Contributions of Current Work

The major contributions and important findings of this work are-

(1) A new application of CNT networks FETs has been proposed in cryptography. The inherent randomness of CNT network is utilized to propose a novel PUF design using multi-gated CNT FETs. The multi-gated design exhibit significantly higher level of randomness and hepta-decimal keys are demonstrated. It is compatible with next generation flexible, wearable, and disposable electronic devices.

(2) A 2-D electrothermal model has been developed for the delta-doped β-Ga_2O_3 based MESFET using Synopsys TCAD Sentaurus. This is one of the first electro-thermal models for β-Ga_2O_3. It is validated against experiments for a wide range of V_{ds} and V_{gs}. We studied the effect of bias condition on Joule heat profile and peak temperature of the device. Our study highlighted that the peak temperature in a delta-doped β-Ga_2O_3 based MESFET is dependent on the bias conditions at a given power.

(3) A 3-D diffusive thermal transport model, which is coupled with 2-D TCAD model, has been developed for accurate prediction of temperature profile in the device. It was determined that the temperature measured at the gate surface by thermoreflectance imaging is less than overall peak temperature, which is located inside the device. Effectiveness of different device-level passive cooling techniques were compared using this model for future device design.

(4) Steady-state thermoreflectance imaging has been performed to measure the spatial variation of temperature on the electrodes of delta-doped β-Ga_2O_3 based MESFET and validate the 3-D thermal model. Transient thermoreflectance imaging and 3-D diffusive thermal modeling were also performed to understand the transient behavior of the device. A compact thermal model was developed to predict the temperature rise and drop during power on and power off states of the device. The thermal time constants of delta-doped β-Ga_2O_3 based MESFET were calculated.

(5) Phonon transport in β-Ga_2O_3 thin films and FETs using non-gray Boltzmann Transport Equations (BTE) is studied. β-Ga_2O_3 thermal conductivity as a

function of film thickness is predicted. It was determined that the distribution of input energy to different phonon modes do not play any major role in the temperature field near hot spot. However, the characteristic length of the domain can play a significant role in thermal transport in the domain. It was demonstrated that the device with a thin (<1 μm) semiconducting β-Ga_2O_3 layer, diffusive transport model may not give accurate temperature distribution in the presence of interface scattering and non-gray BTE model needs to be solved to account for ballistic effects and accurate temperature predictions.

CHAPTER 3. METHODOLOGY

This chapter describes the methods, models and techniques used in this work. Electrical transport in CNT network FETs is investigated using drift-diffusion model. 2-D electrothermal modeling of β-Ga_2O_3 devices is performed using TCAD Sentaurus. A thermodynamic carrier transport device model, which accounts for temperature dependence of various material properties, is employed. A 3-D diffusive thermal transport was developed using Ansys Fluent. The thermal model was validated against the experimental measurements. Steady-state and transient thermal measurements were performed using Microsanj thermo-reflectance measurements. The ballistic effects in thin films of β-Ga_2O_3 and β-Ga_2O_3 FETs were studied using non-gray phonon BTE. The BTE solution was obtained using COMET method.

3.1 Electrical Transport in CNT Network FETs

The carrier transport in CNT network FETs was modeled and compared to experiments in the linear regime by Kumar et al. [130]. Ninad et al. [131] generalized this model to predict characteristics in non-linear regime as well. This model of electrical transport in CNT-FETs was based on modified Poisson's, current continuity, and Drift-Diffusion equations [130-137]. The channel lengths (L_c) of the CNT-FETs studied in this work were larger than CNT lengths (L_{CNT}). All the CNTs in the model are assumed to be semiconducting. The method used to generate random CNT network is also described in [130, 135]. The equations, which were used to predict current and potential distribution in CNT-FETs are given by Equations 3.1, 3.2 and 3.3.

$$\frac{d^2\psi_i}{ds^2} + \frac{\rho_i}{\varepsilon} - \frac{(\psi_i - V_G)}{\lambda^2} + \sum_{j \neq i} \frac{(\psi_j - \psi_i)}{\lambda_{ij}^2} = 0 \tag{3.1}$$

$$\nabla . J_{pi} + \sum_{j \neq i} C_{ij}^p (p_j - p_i) = 0 \tag{3.2}$$

$$\nabla . J_{ni} + \sum_{j \neq i} C_{ij}^n (n_j - n_i) = 0 \tag{3.3}$$

The first equation is a modified version of Poisson's equation. Here, ψ_i represents electrostatic potential along i^{th} section of a CNT, ρ is the total charge density, ε is permittivity of CNT and V_G is gate voltage. The third and fourth terms on the left-hand side of Poisson's equation account for CNT-gate voltage interaction and CNT-CNT interactions respectively, where λ and λ_{ij} are corresponding screening lengths. "s" is the length along CNT. The next two equations are Carrier Continuity equations for hole and electrons. Here, J is current density and p and n are hole and electron charge density respectively. The second terms on the left-hand sides of these equations account for hole or electron charge transfer across CNT-CNT at junctions. The numerical values of various parameters are chosen from the previous studies [135-137], where experimental validation was also performed.

3.2 2-D Electrothermal TCAD Modeling of Delta-doped β-Ga_2O_3 MESFET

A commercial software package TCAD Sentaurus by Synopsys Inc. was used to simulate device characteristics [138]. A flow-chart of device simulation process is shown in Figure 3.1. There are three main tools in this package—Sentaurus Structure Editor,

Sentaurus Device and Sentaurus Visual. The Structure Editor is used to create device geometry, contacts, doping and mesh. This information as well as initial conditions, boundary conditions, model types and parameters are then given as input in the Sentaurus Device, which solves the Poisson's equation, current-continuity and lattice temperature equations and generates the results, which include current density, electric field, temperature profile, etc. These results can be visualized and plotted using the Sentaurus Visual.

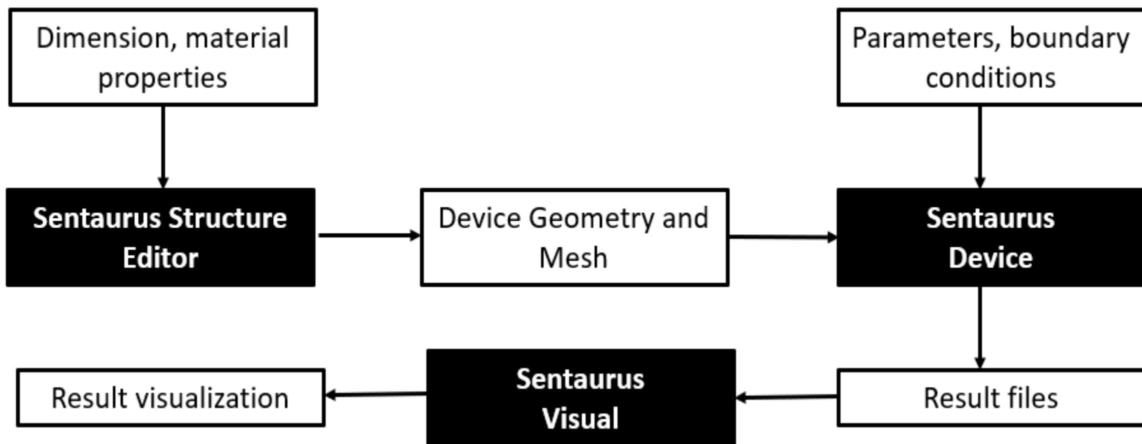


Figure 3.1 A flow-chart of device simulation process. The three tools (Sentaurus Structure Editor, Sentaurus Device and Sentaurus Visual) used for simulations are shown in dark boxes.

The Thermodynamic device model in Sentaurus Device, which accounts for self-heating and suitable for high power devices with long active regions, is used for electrothermal modeling [138]. The various parameters and material properties are chosen from the literature. The following equations were used to obtain electrostatic potential, current densities, and temperature—

$$\nabla.(\epsilon\nabla\varphi) = -q\,(p - n + N_D - N_A) - \rho_{trap} \tag{3.4}$$

$$\nabla.\vec{J}_n = q\,(R_{net,n} - G_{net,n}) + q\frac{\partial n}{\partial t} \tag{3.5}$$

$$-\nabla.\vec{J}_p = q\,(R_{net,p} - G_{net,p}) + q\frac{\partial p}{\partial t} \tag{3.6}$$

$$\vec{J}_n = -nq\mu_n(\nabla\varphi_n + P_n\nabla T) \tag{3.7}$$

$$\vec{J}_p = -pq\mu_p(\nabla\varphi_p + P_p\nabla T) \tag{3.8}$$

$$-\nabla.(k\nabla T) = -\nabla.\left[(P_nT + \varphi_n)\vec{J}_n + (P_pT + \varphi_p)\vec{J}_p\right] - \frac{1}{q}\left(E_c + \frac{3}{2}kT\right)\left(\nabla.\vec{J}_n - qR_{net,n}\right) - \frac{1}{q}\left(-E_v + \frac{3}{2}kT\right)\left(-\nabla.\vec{J}_p - qR_{net,p}\right) \tag{3.9}$$

Here, ϵ is the electrical permittivity, φ is electrostatic potential, q is electronic charge, n and p are the electron and hole densities, N_D and N_A are concentration of ionized donors and acceptors, ρ_{trap} is fixed or trap charge density, $R_{net,n}$ and $R_{net,p}$ are electron and hole net recombination rates, $G_{net,n}$ and $G_{net,p}$ are electron and hole net generation rates, $\vec{J}_n$ and $\vec{J}_p$ are electron and hole current densities, μ_n and μ_p are electron and hole mobility, $\vec{J}_n$ and $\vec{J}_p$ are electron and hole current densities, P_n and P_p are the absolute thermoelectric powers, k is the thermal conductivity, E_c and E_v are the conduction and valence band energies and T is lattice temperature.

3.3 3-D Diffusive Thermal Transport Modeling of Delta-doped β-Ga_2O_3 MESFET

The 2-D electrothermal simulations in TCAD Sentaurus cannot account for heat dissipations in all the three dimensions. The accurate prediction of temperature requires consideration of heat dissipation in all three dimensions. Therefore, we have developed a 3-D model in Ansys Workbench. The CAD models of the device were created in SpaceClaim and SolidWorks. The grid generation was performed using Ansys meshing software. The Ansys Fluent was used to setup the problem and compute the solution. It uses Fourier's law for conduction in solids and energy balance to predict the temperature distribution in the device. The Joule heat profile predicted from the TCAD Sentaurus is used as an input to the model.

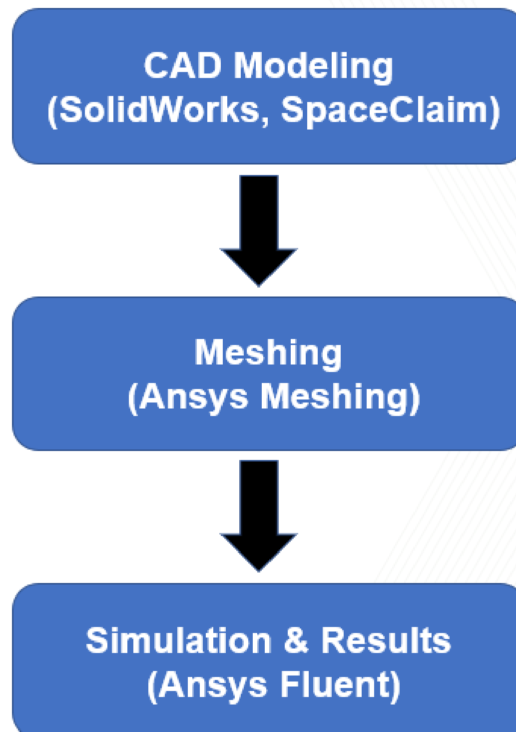


Figure 3.2 A flowchart of 3-D thermal modeling procedure.

3.4 Thermoreflectance Thermal Imaging of Delta-doped β-Ga_2O_3 MESFET

Thermoreflectance thermal imaging (TTI) can provide temperature profile with submicron temporal and spatial resolution [139-141]. Therefore, TTI has been used in this work to conduct high resolution measurements of steady-state and transient temperature variation in β-Ga_2O_3 devices. A schematic diagram of the setup, which includes the CCD detector, illumination source, microscope objective, and the temperature-controlled stage, is shown in Figure 3.3. The Microsanj thermo-reflectance system NT210B with piezoelectric stage, which accounts for thermal expansion during calibration and measurements, is used for TTI. This system uses autofocusing function and charge coupled

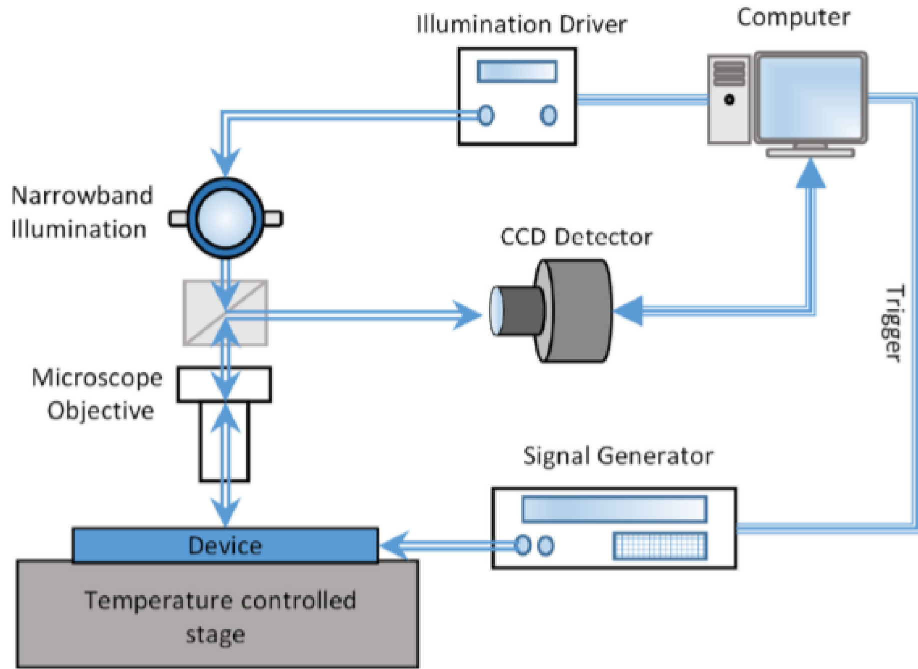


Figure 3.3 A schematic of Microsanj thermoreflectance imaging system that includes the CCD detector, illumination source (LED), microscope objective, and the temperature-controlled piezoelectric stage. Reprinted with permission from [142]. Copyright © 2020, IEEE.

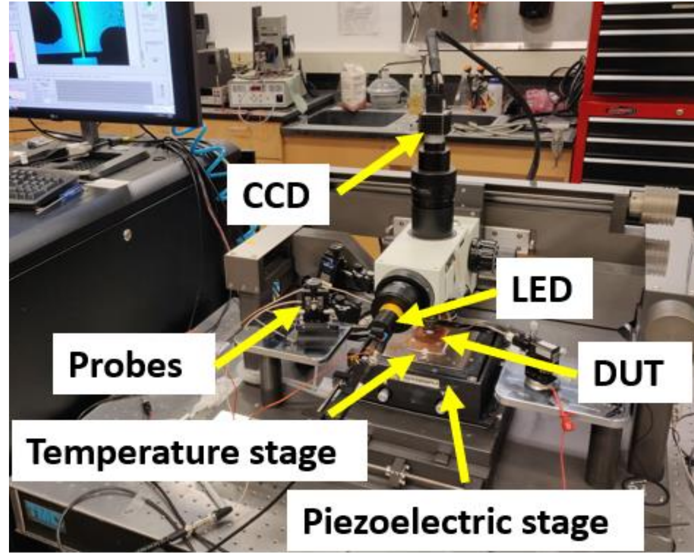


Figure 3.4 A photograph of Microsanj thermoreflectance imaging system depicting different components of the setup.

device (CCD) instead of photodiode detector for the thermal measurements and account for thermal expansion. A photograph depicting different components of the experimental setup is shown in Figure 3.4. It is proven to be an accurate technique for transient measurements, which have been validated against gate resistance thermometry (GRT), Raman thermography, and 3-D FEA modeling [84, 112, 143]. This technique is based on the principle that surface reflectivity of a material is function of temperature. The relative change in the reflectivity$\left(^{\Delta R}/_{R}\right)$ with change in temperature (ΔT) is represented by thermoreflectance coefficient (C_{th}) as shown below—

$$C_{th} = \Delta T/\left(^{\Delta R}/_{R}\right) \tag{3.10}$$

The additional details of the technique is available in [112, 141]. A schematic of timing control during transient measurements is shown in Figure 3.5. During transient

measurements, a constant cycle of device excitation is repeated and temperature measurement at a particular time instant is averaged over several images. Once the measurements is performed at a time instant then LED pulse is shifted to the next desired time instant for measurements. This procedure is repeated until temperature data at all the desired time instants are acquired.

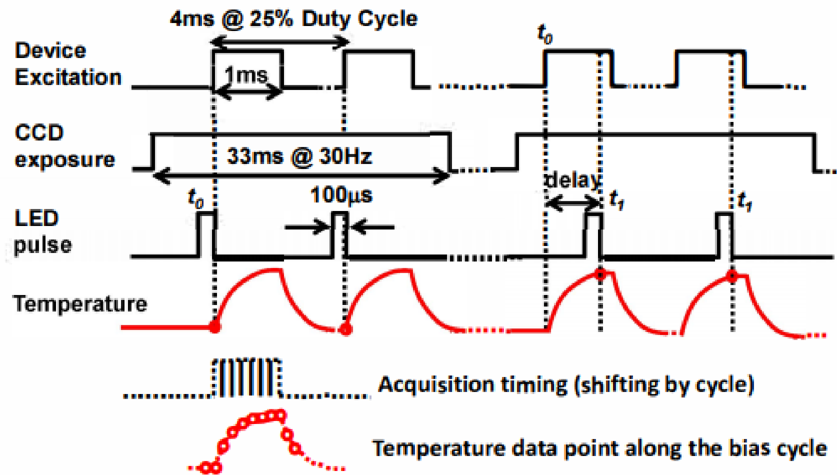


Figure 3.5 A schematic of timing control during transient measure.

3.5 Boltzmann Transport Equations for Phonon Transport Modeling in Thin Films and β-Ga_2O_3 FETs

Non-gray Boltzmann Transport Equations (BTE) is used to study phonon transport in β-Ga_2O_3 thin films for applications relevant to FETs. The steady-state non-gray BTE of a phonon mode with under single-mode relaxation time approximation (SMRTA) [120] is given as-

$$\sum_f e_f^{"} v.\nabla A_f = \frac{e_c^o - e_c^{"}}{\tau_{eff}} \Delta V + S_{vol} \tag{3.11}$$

$$e^o = \hbar\omega N = \frac{\hbar\omega}{exp\left(\frac{\hbar\omega}{K_b T}\right) - 1} \tag{3.12}$$

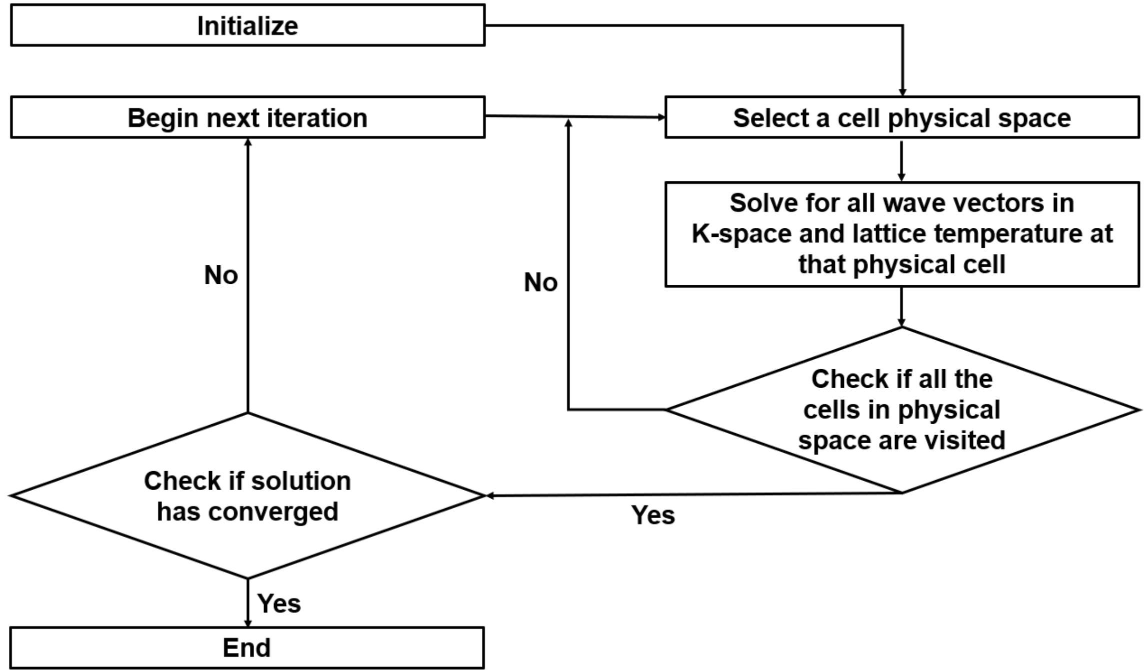


Figure 3.6 Flowchart of COMET algorithm.

Here, subscript c and f denote that value is calculated at centroid and face of a cell, respectively. The e" is the energy of the phonon mode, v is the phonon group velocity, ∇A is the area vector associated with a face in the physical domain, and e^o is the equilibrium energy, τ_{eff} is the effective phonon relaxation time, which accounts for contribution from different mechanisms, ω is the phonon frequency, ΔV represents the volume of a cell in physical space and S_{vol} is the external volumetric heat source, $\hbar$ is reduced Planck's

constant, K_b is Boltzmann constant and N is the equilibrium Bose-Einstein distribution for a phonon mode of frequency ω, and polarization p at temperature T. The parameters such as e'', v and τ_{eff} are different for different phonon modes. Direct coupling of all these BTEs is extremely expensive to solve. RTA is used to simplify the scattering term on the right-hand side of the BTE. In the current study, the BTE will be solved iteratively using Coupled Ordinates Method (COMET). The finite volume method is used for discretization of physical and wave-vector space. Then, all the phonon modes are directly solved together in a cell before moving to the next cell in physical space. This process is repeated until convergence is achieved. This method is parallelized such that physical mesh is divided into sub-meshes, which are solved by different processors to reduce calculation time. The flowchart of COMET algorithm is shown in Figure 3.6. The additional details on the solution of BTE using COMET algorithm are available in [129, 144].

3.6 Closure

The various methods and techniques used in this work are discussed in this chapter. Electrical transport in CNT network FETs is modeled using Poisson's equation, drift-diffusion equation, and current continuity equation. 2-D electrothermal modeling of β-Ga_2O_3 devices is performed using a thermodynamic carrier transport model in TCAD Sentaurus. 3-D diffusive thermal transport modeling is performed using Ansys Fluent. Thermal measurements are performed using Thermoreflectance imaging technique. The phonon BTE is solved using COMET algorithm to study ballistic effect in β-Ga_2O_3 thin films and devices.

CHAPTER 4. MULTI-GATED CARBON NANOTUBE FIELD EFFECT TRANSISTORS BASED PHYSICALLY UNCLONABLE FUNCTIONS AS SECURITY KEYS

In this work, we introduced a random CNT network-based multi-gated FET as PUF, which exploits the randomness of a CNT network in the channel to generate keys. Single-gate transistors with CNT density close to percolation threshold density produced binary keys depending upon whether the CNT network channel was connected or not. We introduced a multi-gate CNT-FET, where the channel was divided into multiple sections and each section could be biased with an independent gate voltage. FETs with four-gates produced three different levels of current including zero current (corresponding to an unconnected CNT network) and generated six different challenge-response pairs in a single instance. Current levels were separate enough to avoid any bit error. We could also control the distribution of different bit-values easily to maximize the randomness by changing the dimensions of the channel and/or its sections. By combining six challenges and three current levels, it was shown that not only ternary-bit keys but base-17 (hepta-decimal) keys could also be produced. Consequently, a significantly higher level of randomness was achieved by our PUF in comparison with existing PUFs, which could generate only binary or ternary keys.

4.1 Assessment of CNT-FETs as PUFs

Since CNT networks are random, each FET should have a unique CNT network distribution. Therefore, the current should be different for different FETs for a given gate

and drain voltage even if all the parameters, e.g., CNT network density, device dimensions and fabrication process are identical. We wanted to engineer these devices in such a way that different current levels can be obtained to facilitate the development of ternary or higher order bits. However, the measurement of current in the fabricated FETs and numerical simulations revealed that the change in current values of different FETs were not large enough [75, 145]. Two disjoint levels (groups) of currents with enough separation were not present. Environmental effects (e.g., humidity) could affect the current in a device and cause the bit error if the separation between current levels corresponding to different bit values is not large enough. To address this challenge, we decreased the CNT network density close to the percolation threshold density. So, the channel of FETs may or may not conduct depending on whether the CNT network channel is connected or not. Percolation threshold density (ρ_{th}) is a critical number of CNTs per unit area below which the probability that a CNT network would conduct is very low. Although the CNT length-dependent empirical equation for ρ_{th} can be used to estimate ρ_{th}, the same equation may not be applicable to the finite length of channels. So, numerical simulation or experimental analysis is necessary. To predict the dimensions and CNT network density required for highest randomness, we used numerical simulations because fabrication is costly and time-consuming. Numerical simulation could guide us in selecting the appropriate dimensions and CNT network density before we fabricate the devices. Numerical simulation approach is described in the Chapter-3. Passivation layer of dielectric may help in minimizing the effect of environmental factors and improve stability of the devices. Passivation layer could also be used to hide CNT network from adversary in bottom-gate CNT-FETs.

4.2 Single-gate CNT-FET as PUF

Using numerical simulations, we studied the effect of change in channel length, channel width and CNT density on device current and the probability of any device having a connected channel (non-zero current) or an unconnected channel (zero current). When the CNT network density is significantly higher than the ρ_{th} and the network is very dense, as shown in Figure 4.1 (a), the probability of having an unconnected device in a random sample-set is negligible and there are very few or no unconnected devices. Even changing the dimensions of the channel does not increase unconnected devices in the sample. Figure 4.1 (b) and (c) present illustrations of CNT-FETs with unconnected and connected channels, respectively. We associated unconnected devices with a bit-value of '0' and connected devices with a bit-value of '1'. The analytical expression for percolation threshold density, $\rho_{\mathrm{th}} = 4.236^2/\pi L_{CNT}^2$, can be used for the estimation of ρ_{th} for large networks [146-148]. We performed simulations for different network densities close to ρ_{th} using approximately 2,500 random network devices for each density. Length of the CNTs (L_{CNT}) was maintained at 1 μm in simulations, which is the same as the average length of CNTs in experiments [75]. The value of ρ_{th} for this average length of CNTs will be 5.7 per μm^2. Our simulations showed that most of the networks were not connected at this density for small channel dimensions (e.g., channel length/width of 3-50 μm), which is typically used for the fabrication of CNT-FETs. We selected a CNT network density (D) = 7 per μm^2, which is very close to the ρ_{th} of 5.7 per μm^2 and could be used to have about 50% unconnected devices by considering the channel dimensions of interest (e.g., channel length/width of 3-20 μm). Once the density was fixed, we aimed to achieve almost equal

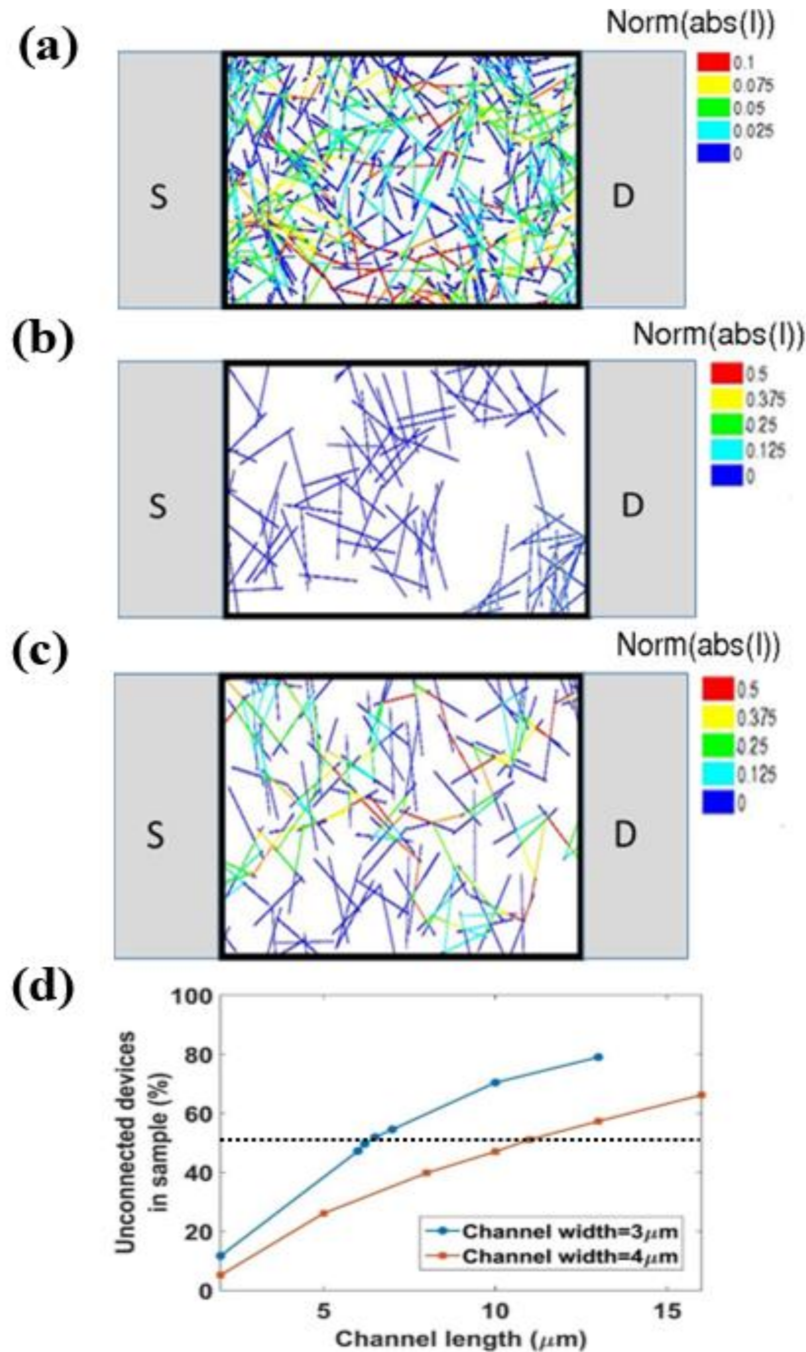


Figure 4.1 Network connectivity in single gate CNT-FETs. (a) A high-density connected network in a CNT-FET. (b) A FET channel with unconnected CNT network (zero current), (c) A low-density FET channel with connected CNT network. Network is generated using same CNT density as in (b). Normalized absolute currents in the channels are also shown for these figures. (d) Percentage of unconnected networks in CNT-FETs with respect to channel length for channel width of 3 μm and 4 μm. Samples are randomly generated with a density of 7 μm^{-2}. Dashed horizontal line corresponds to 50% unconnected devices.

numbers of connected and unconnected devices in any given sample to achieve maximum randomness by varying channel dimensions. Figure 4.1 (d) presents the percentage of unconnected devices as a function of channel length and width at a CNT network density of 7 per μm^2. At this CNT network density (close to ρ_{th}), increasing the length and decreasing the width will increase the percentage of unconnected devices in any given sample. A device with a channel length close to 6.2 μm and width 3 μm or a channel length close to 11 μm and width 4 μm was observed to be suitable for maximum randomness but the former dimensions are more desirable as size of the device is much smaller.

A widely accepted statistical test suit developed by the National Institute of Standards and Technology (NIST) was used to test the quality of random numbers generated by these CNT-FETs. The proposed PUF design passed all the relevant tests. The NIST Statistical Test Suite is a set of algorithmic tests that attempts to identify sequences of binary numbers that do not behave in a truly random manner. The tests calculate a p-value for every sequence of bits. The p-value represents the probability that the given sequence could have been generated by running a truly random number generator once. Each test passes if the p-value is greater than 0.01 as directed in [149].

4.3 Multi-gate CNT-FET as PUF

Next, we introduced a multi-gate CNT-FET design, where the CNT network channel was divided into multiple sections and each section could be biased with a different gate voltage. The conductivity of any of the sections could be independently changed by changing the applied gate voltage in that section. Thus, the path and magnitude of the current in the device could be controlled. The two important advantages of this device

were– (1) we could separate connected devices in two or more groups based on the magnitude of current, and (2) we could create multiple challenges per device. Thus, we could generate n-ary (n>2) keys, which would have more entropy than binary keys for the same key size. Schematic diagrams of a single-gate CNT-FET and a multi-gate CNT-FET are shown in Figure 4.2 (a) and (b), respectively, to highlight the difference in design and operation of the two devices.

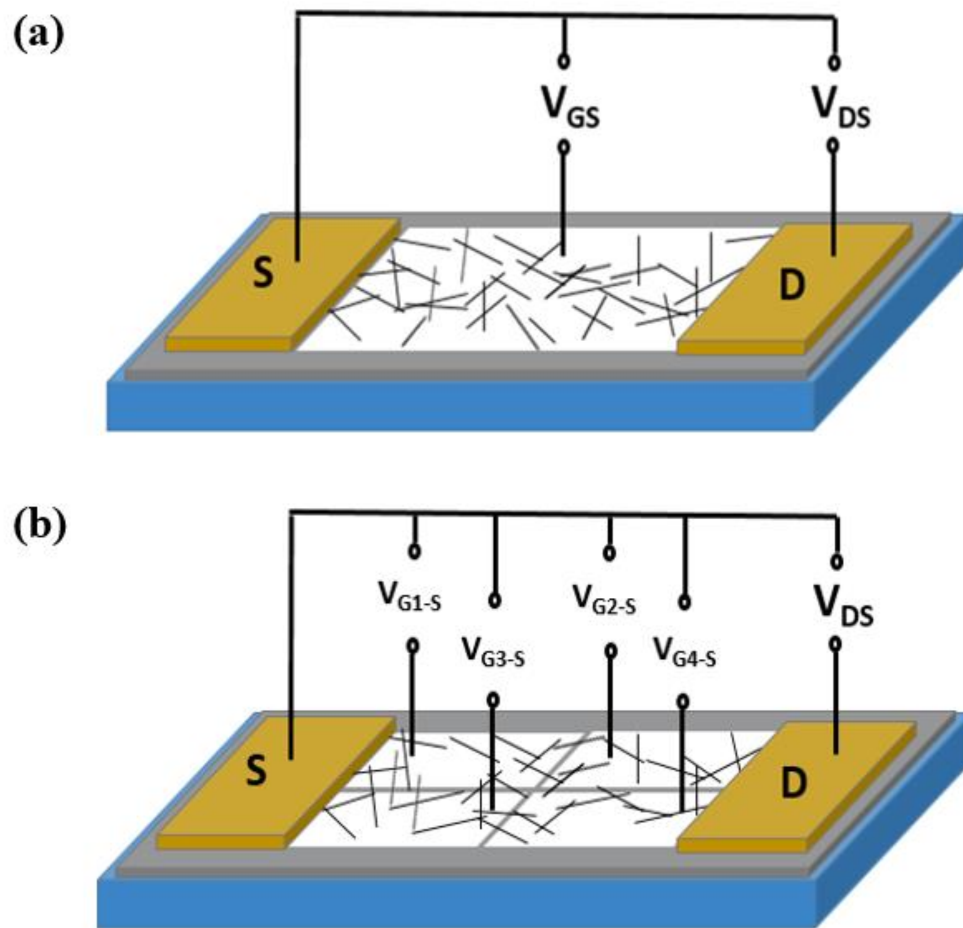
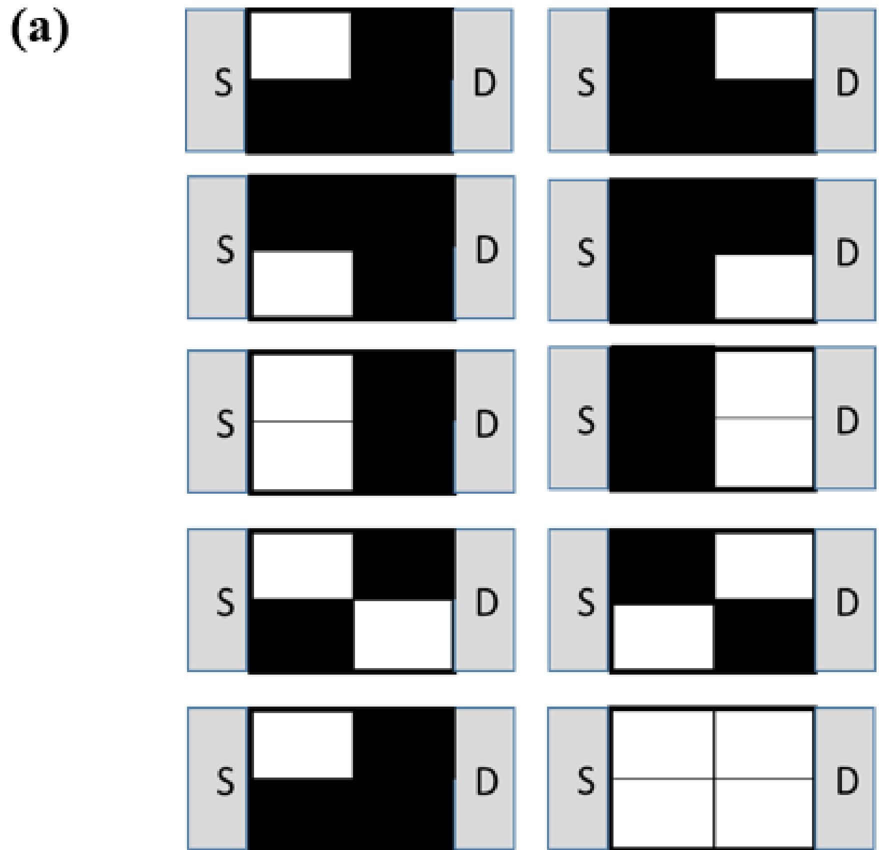


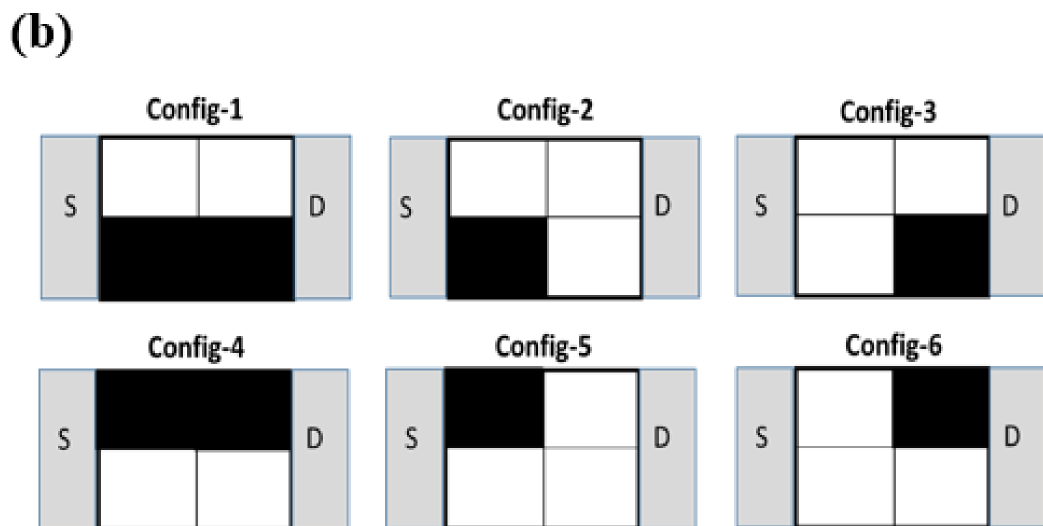
Figure 4.2 Comparison between single gate CNT-FETs and multi-gate CNT-FETs. (a) A schematic diagram of single-gate CNT-FET. (b) A schematic diagram of multi-gate CNT-FET.

Several different multi-gate channel designs can be useful depending upon the application. We are presenting one such design to demonstrate the concept and the advantages of multi-gate CNT-FETs. In this design, we divided the channel into four rectangular sections of the same size, as shown in the Figure 4.2 (b). We created two different types of sections, namely a high conductivity section (HCS) and a low conductivity section (LCS). The ratio of conductivity between the HCS and LCS is chosen to be 10^4. We chose two gate voltages, one corresponding to an ON state and another to an OFF state, such that the current ON/OFF ratio was 10^4, which is as per reported in the literature [75, 136]. Thus, HCS and LCS mimic (correspond to) sections biased with the ON and OFF state gate voltages, respectively.

We simulated around 1600 devices with different random CNT networks. Each device can have 16 (2^4) different combinations (or configurations) of high conductivity and low conductivity sections in the channel. However, we found that 10 out of 16 configurations (shown in Figure 4.3 (a)) could not produce two non-zero levels of current and in only remaining 6 configurations (shown in Figure 4.3 (b)) it was possible to separate the connected, devices into low current devices (LCDs) and high current devices (HCDs) depending on the magnitude of current. As shown in Figure 4.3 (b), we named these configurations Config-1, Config-2, Config-3, Config-4, Config-5 and Config-6. The black sections represent LCSs and white sections represent HCSs. For example, in Config-1, the two black sections in the lower-half are LCSs and the two upper-half white sections are HCSs. Similarly, LCSs and HCSs in other configurations can be identified. We associated unconnected devices with a bit-value of '0', LCDs with a bit-value of '1' and HCDs with

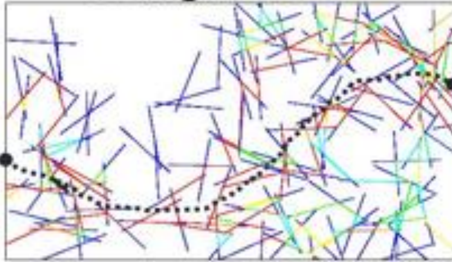
a bit-value of ‘2’. Thus, we generated a ternary key using one of these configurations. Figure 4.3 (c) demonstrates representative networks and normalized current distribution



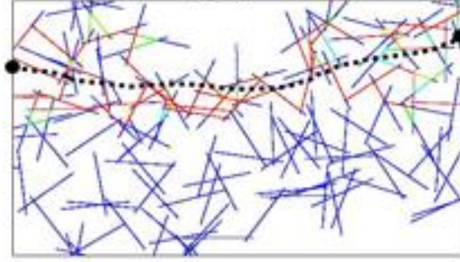


(c)

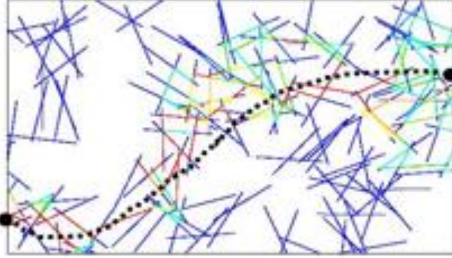
Config-1, bit ‘1’



Config-1, bit ‘2’

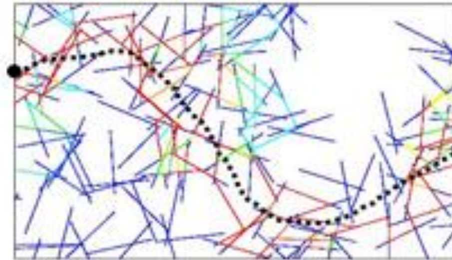


Config-2, bit ‘1’

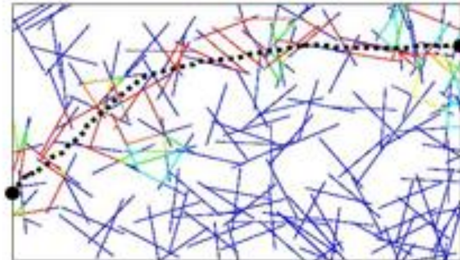


Config-2, bit

Config-3, bit ‘1’

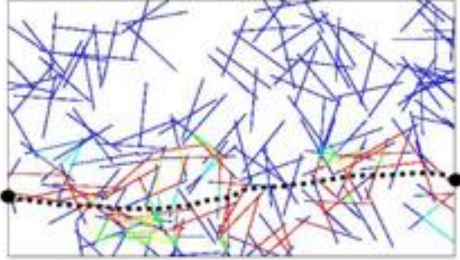


Config-3, bit ‘2’

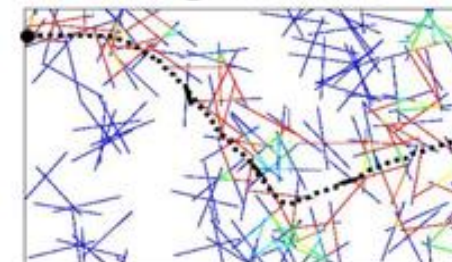


Config-4, bit ‘1’

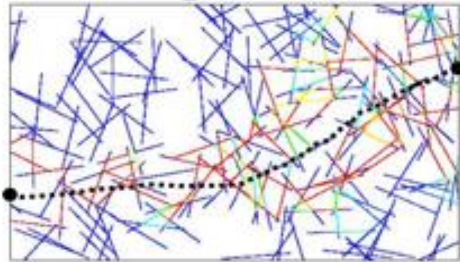
Config-4, bit ‘2’



Config-5, bit ‘1’



Config-5, bit ‘2’



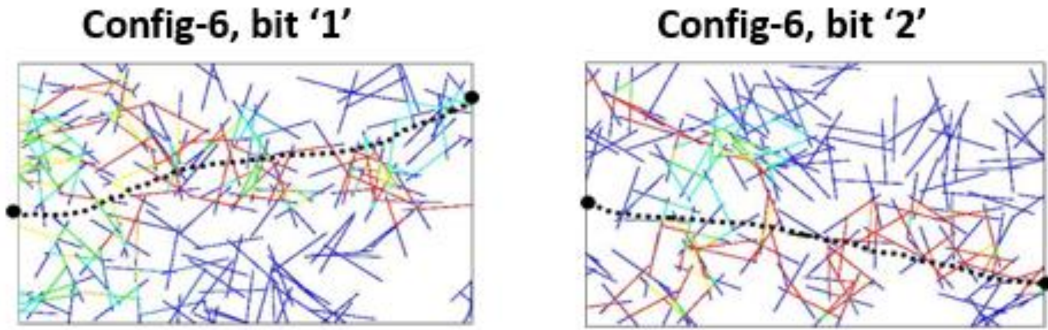


Figure 4.3. Multi-gate CNT-FETs. (a) 10 different configuration which could have only one continuous level of non-zero current and were not useful for ternary keys (b) 6 different configurations with two separate levels of currents and useful in generating ternary bits and creating 6 different challenges per device. HCSs and LCSs of the channel are represented by white and black colors, respectively. Configurations in the top row are named Config-1, Config-2, and Config-3 (from left to right) and in the bottom row are named Config-4, Config-5, and Config-6 (from left to right) respectively. (c) Representative networks and normalized absolute currents for six configurations: from Config-1 to Config-6; bit value '1' (left image) and '2' (right image).

generating bit-values of '1' and '2' in multi-gate devices for Config-1 to Config-6. An HCD is produced by a random network wherein there are one or more connected paths available and at least one connected path is passing only through higher conductivity sections of the channel. An LCD is produced by a random network where there are one or more connected paths available but does not have even a single path passing exclusively through higher conductivity sections of the channel. In that case, current must pass through the low conductivity section and, therefore, current will be much lower in LCDs compared to HCDs. These two disjoint levels of currents are shown in Figure 4.4 (a).

The dimensions of sections and channel were chosen such that the probability of producing any of the three bit values is approximately equal to 1/3. An equal distribution

of all the bit values corresponds to the maximum possible combinations for a key of given length. Since the probability of a bit value also depends on configuration, it was not possible to have equal probabilities of bit values in all the six gate configurations simultaneously. Therefore, we chose the dimensions of the device such that the maximum number of configurations has an equal distribution of bit values. We kept the value of CNT network density at 7 per μm^2, same as in the single-gate devices, and selected channel length and width equal to 6.5 μm and 4 μm, respectively. Each of the four channel sections had length and width equal to 3.25 μm and 2 μm respectively. We achieved an approximately equal probability, i.e., close to 33.3%, for all the three bit values in Config-2, Config-3, Config-5 and Config-6 (four out of six configurations) as shown in Figure 4.4 (b). However, in Config-1 and Config-4, the percentages of bit-values '1' and '2' were close to 45% and 20%, respectively. The increase in bit-value '1' and decrease in bit-value '2' compared to the other four configurations was due to an increase in LCSs compared to the other configurations. For a ternary key with maximum randomness, we can choose one of the four configurations. For example, in a 128-bit ternary key, if all three bit-values are approximately equally distributed, e.g., 42 '0-bit', 43 '1-bit' and 43 '2-bit', then 7.52×10^{58} combinations are possible. However, in a binary key of the same size only 2.40×10^{37} combinations are possible if the bit values are equally distributed. The number of total possible combinations in 128-bit ternary key is 1.18×10^{61} (3^{128}) in comparison to 3.4×10^{38} (2^{128}) of a 128-bit binary key. Thus, ternary keys can significantly increase the possible combinations and randomness level without increasing the size of the key.

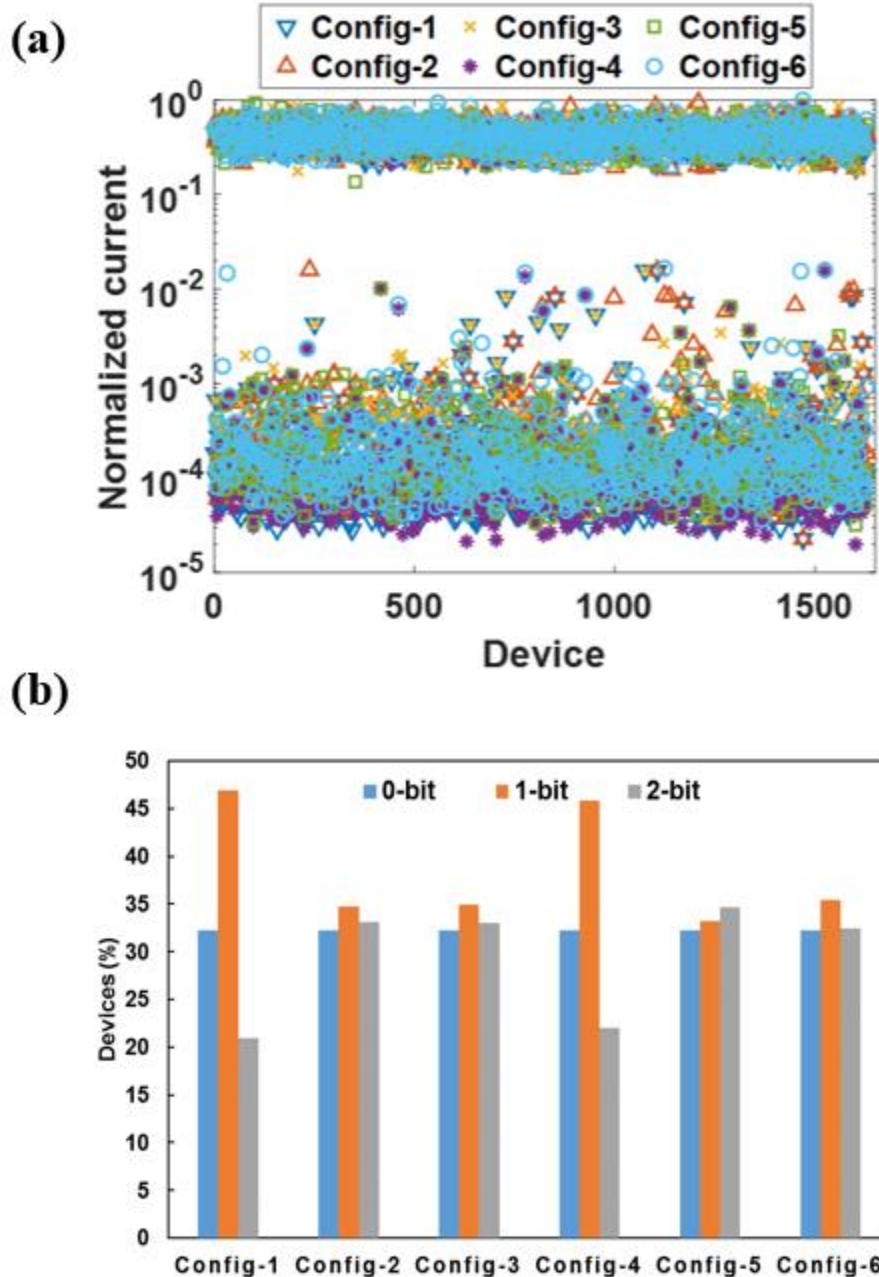


Figure 4.4. Multi-gate CNT-FETs. (a) Two disjoint levels of non-zero currents associated with bit-value '1' and '2' in all six configurations generated by connected devices. Third current level associated with bit-value '0' corresponds to 'zero current' generated by unconnected devices. Zero current devices could not be shown on logarithmic scale. CNT networks are randomly generated in the channel region of FETs and current is obtained from the device simulations (b) Percentage of devices with bit values (0, 1 and 2) produced by different configurations of multi-gate CNT-FETs.

Initially, we used only one configuration at a time and were able to generate only ternary keys. Next, we utilized all the six configurations simultaneously as challenges. We were able to generate base-17 (heptadecimal) keys by increasing the total possible combinations and achieved significantly increased randomness in comparison with single challenge multi-gate PUF. Theoretically, each connected device with ‘n’ different challenges and ‘m’ current levels can produce m^n different types of outputs. Therefore, a device with six different challenges and two non-zero current levels can produce up to 64 (2^6) different types of outputs e.g., 111222,112121,122111 and so on. For all outputs, the first digit from the left corresponds to the output of Config-1 and the second digit in that order corresponds to the associated output for Config-2 and so on. However, only 16 different types of outputs out of the possible 64 are obtained during simulation, because if Config-2 (or Config-5) and/or Config-3 (or Config-6) rendered bit ‘1’ for a network then Config-1 (or Config-4) would also render bit ‘1.’ This can be understood by the overlap of HCSs in different configurations. For example, if in Config-2 there is no conducting path passing exclusively through HCSs, then Config-1, which has both its HCSs overlapped by two out of three HCSs of Config-2 also produces bit ‘1’. Figure 4.5 presents those 16 outputs and their percentage yield in the random sample. Unconnected devices will always have zero current and will, therefore, only produce ‘0’ bit in all the six configurations. Thus, a bit output of ‘000000’ for unconnected devices and 16 different outputs corresponding to the connected devices constitute a total of 17 different outputs in comparison with just 3 outputs, when only one configuration (challenge) was used in multi-gate CNT-FETs. The total number of possible combinations in a 128-bit string is 3.14 x 10^{157} (17^{128}) and the maximum possible combinations if all the states are approximately

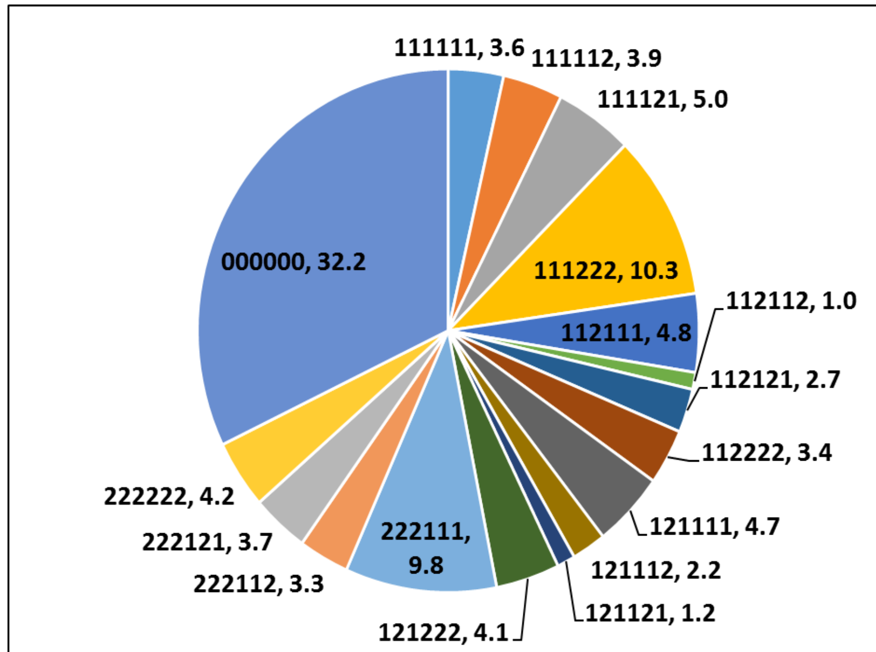


Figure 4.5. Multi-gate CNT-FETs. Percentage yield of different possible composite states produced in around 1600 four-gated CNT-FETs whose networks are randomly sampled. First value represents unique composite output state, and second value represents corresponding yield. Each CNT-FET is tested for six gate configurations shown in Figure 4(a). The digits from left to right in six-bit string (composite output state) correspond to the output states (0, 1 or 2) for gate Config-1 to Config-6.

equally distributed are 3.29 $x10^{144}$. However, in this device design, all the states were not equally distributed, as shown in Figure 4.5. The number of possible combinations corresponding to this distribution is 1.25 $x10^{123}$, which is significantly larger than the number of possible combinations corresponding to a binary or ternary key of the same length. The calculation details of maximum possible combinations are shown in Table 4.1 and described below.

Table 4.1 Occurrence of different output states in multi-gate CNT-FETs.

Output type	Total occurrence	% Total occurrence	Occurrence in 128-bit key	Approx. bit distribution in 128-bit key	Possible combinations
111111	58	3.56	4.56	5	128C5
111112	63	3.86	4.95	5	123C5
111121	82	5.03	6.44	6	118C6
111222	167	10.25	13.12	13	112C13
112111	79	4.85	6.21	6	99C6
112112	17	1.04	1.34	2	93C2
112121	44	2.70	3.46	4	91C4
112222	56	3.43	4.40	4	87C4
121111	76	4.66	5.97	6	83C7
121112	36	2.21	2.83	3	77C74
121121	19	1.16	1.49	2	74C72
121222	67	4.11	5.26	5	72C67
222111	159	9.76	12.49	12	67C12
222112	53	3.25	4.16	4	55C4
222121	60	3.68	4.71	5	51C5
222222	69	4.23	5.42	5	46C5
000000	524	32.16	41.17	41	41C41

For a fixed string length, maximum possible combinations occur when all the bit-values occur equally in the string. Maximum possible combinations in binary, ternary and base-17 (hepta-decimal) keys are calculated on this basis. For a 128-bit binary and ternary key, maximum possible combinations are 128C64 (2.40×10^{37}) and 128C86 * 86C43 (7.52×10^{58}), respectively. Possible combinations in hepta-decimal keys will be maximum when 9 bit-values occur 8-times and 8 bit-values occur 7-times in 128-bit key and maximum possible combinations are 3.29×10^{144} (128C8 * 120C8 * 112C8 * 104C8 * 96C8 * 88C8 * 80C8 * 72C8 * 64C8 * 56C7 * 49C7 * 42C7 * 35C7 * 28C7 * 21C7 * 14C7 * 7C7). Possible combinations in 128-bit hepta-decimal key are $1.25 \mathrm{X} 10^{123}$ (128C5 * 123C5 * 118C6 * 112C13 * 99C6 * 93C2 * 91C4 * 87C4 * 83C6 * 77C3 * 74C2 * 72C5 * 67C12 * 55C4 * 51C5 * 46C5 * 41C41) if bit-values occur as per distribution shown in Figure 4.5. In addition, the entropy generated by these devices can be calculated using the formula:

$$Entropy = -\sum_{i=1}^{N} p_i \log_2(p_i)$$

Here, N is total number of outputs and p_i is the probability of occurrence of the ith output. The entropy generated using single-gate CNT-FETs is 1 bit per device, whereas entropy generated using multi-gate CNT-FETs is 3.47 bits per device for the output distribution shown in Figure 4.5. It implies that we need only ‘n/3.47’ multi-gate devices to generate an n-bit long key, whereas we need ‘n’ single-gate devices to generate an n-bit long key. The maximum entropy of 4.09 bits per device can be achieved using multi-gate CNT-FETs when all the outputs are equally distributed. Channel area of the single-gate device was 18.6 μm^2 and the multi-gate device was 26 μm^2. But the total device area is a sum of channel, source, drain and gate area. The source, and drain area constitute a

significant proportion of the total area and render the increase in channel area of the multi-gate devices compared to single-gate devices insignificant. The gain in entropy is achieved without any consequential increase in the device area.

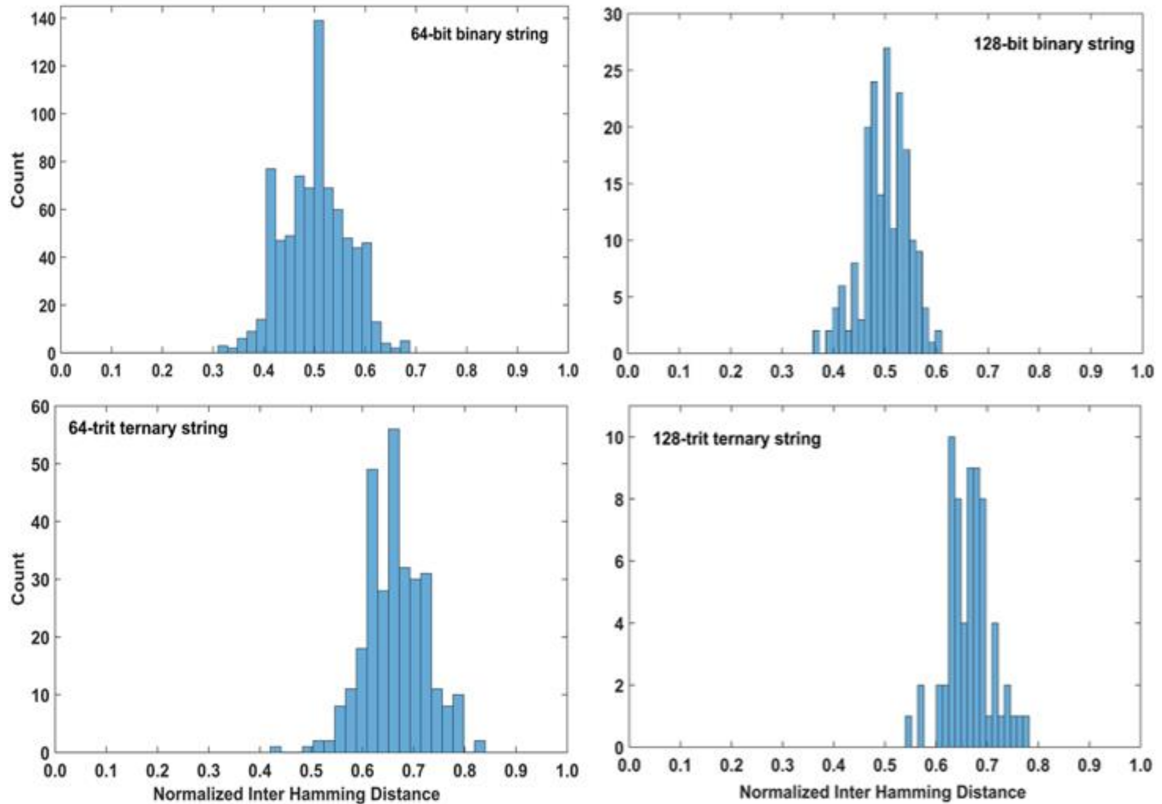


Figure 4.6. Histograms of Normalized Inter Hamming Distance for single-gate and multi-gate devices. (a) 64-bit binary string generated by single-gate devices. (b) 128-bit binary string generated by single-gate devices. (c) 64-bit ternary string generated by multi-gate devices. (d) 128-bit ternary string generated by multi-gate devices.

For purposes of statistical study and demonstrating capability of simulator to generate random network, we also calculated normalized Inter Hamming Distance for binary and ternary strings produced by single-gate and multi-gate devices, respectively. Normalized Inter Hamming Distance is a ratio of the number of positions with different bit values in two different strings of equal length divided by string length. It signifies the

fraction of corresponding bit positions with different bit values in any two keys. For reasonably long keys (e.g., 64-bit, 128-bit), Inter Hamming Distance for binary keys should be close to 0.5, and for ternary keys it should be close to 0.667 indicating optimal unpredictability and inter-device uniqueness. We selected two reasonable key lengths–64-bit and 128-bit–to produce binary and ternary strings from 2560 single-gate and 1600 multi-gate devices, respectively. The following formula is used-

$$Inter\ HD = \frac{2}{k(k-1)} \sum_{i=1}^{k-1} \sum_{j=i+1}^{k} \frac{HD(R_i, R_j)}{l}$$

Here, k is total number of strings, l is string length and R_i and R_j are i^{th} and j^{th} string. For any n-ary (n output states) key to be completely independent, unique and unpredictable, the bit value at any position should not be biased towards or against any particular bit value. All the output states should occur with equal probability. Inter Hamming Distance is fraction of bit positions with different bit values in any two strings. If there is a n-ary string 'A' and we generate another string 'B'. If there is no bias then probability of occurring a different bit value in B than that in A at the corresponding bit position is 1-(1/n). It will lead to 1-(1/n) bit positions in B having different bit values that those in A. Therefore, Inter Hamming Distance between any two strings for complete independence, uniqueness and unpredictability should be 1-(1/2), i.e., 0.5 in case of binary strings and 1-(1/3), i.e., 0.667 in case of ternary strings.

Figure 4.6 presents the distribution of Inter Hamming Distance between strings. For binary strings produced by single-gate devices, Inter Hamming Distances for a 64-bit string are 0.501 with a standard deviation of 0.063. For a 128-bit string it is 0.500 with a standard

deviation of 0.045. This means that 99.73% of the time, any two keys generated by multi-gate devices will have different bit values in at least 31.2% and at most 69% of the bit positions for 64-bit keys and in at least 36.5% and at most 63.5% of the positions for 128-bit keys. For ternary strings produced by multi-gate devices in Config-5, Inter Hamming Distances are 0.665 with a standard deviation of 0.061 for a 64-bit string and 0.666 with a standard deviation of 0.043 for a 128-bit string. This means 99.73% of the time any two keys generated by multi-gate devices will have different bit values in at least 48.2% and at most 84.8% of the bit positions for 64-bit keys and in at least 53.7% and at most 79.5% of the positions for 128-bit keys.

4.4 Closure

We have proposed the design of multi-gate CNT-FET based PUF in this study. An appropriate selection of CNT network channel density and dimensions for the devices enabled us to generate random bit arrays. Single-gate devices with network density close to percolation threshold density produced binary keys. We introduced multi-gate devices, which can have multiple challenges and generate multiple types of outputs. We generated ternary and base-17 (hepta-decimal) keys by using these devices. This study shows that multi-gate CNT-FETs with networks of density close to the percolation threshold density can be promising in producing low-cost and high-quality cryptographic primitives.

CHAPTER 5. ELECTROTHERMAL CHARACTERISTICS OF DELTA-DOPED BETA-GALLIUM OXIDE MESFETS

In this chapter, we have presented details of development of a 2-D electrothermal model of a recently fabricated Si delta-doped β-Ga_2O_3 MESFET [150] using TCAD Sentaurus. Our simulations incorporate temperature and electric field-dependent electron mobility and self-heating effects. We have compared their effects on the I-V characteristics of the FET. Our model shows good agreement with the experiments at a wide range of gate and drain voltages. We have investigated the effect of bias voltages on electric field, current density and its path, volumetric heat generation, and peak temperature in the FET. At a given power dissipation, different bias voltages could lead to different peak temperatures due to a change in the volumetric heat generation profile. Finally, we investigate the effect of the gate-drain spacing, location of delta-doping layer and source-drain length on the FET characteristics, which can provide guidelines for future device design.

5.1 2-D Electrothermal Modeling: Approach

We have developed a 2-D electrothermal model for the delta-doped β-Ga_2O_3 based MESFET using Synopsys TCAD Sentaurus. The cross-sectional view of the device is shown in Figure 5.1. The β-Ga_2O_3 buffer layer in this FET has been fabricated using molecular beam epitaxy (MBE) technique; the fabrication details of FET are available in [150] and briefly described below. A commercially available Fe-doped, semi-insulating, and (010)-oriented β-Ga_2O_3 substrate of thickness 500 μm was used to grow epitaxial structure in (010) crystal direction. It consists of an unintentionally doped (UID) β-Ga_2O_3

buffer layer of thickness 600 nm, a Si delta-doped β-Ga_2O_3 layer and a UID β-Ga_2O_3 cap layer of 38 nm thickness. The delta doped layer has a total charge density of around 1.6 x 10^{13} cm^{-2}. Metal stacks used for Schottky contact at the gate and ohmic contacts at source and drain are Ni/Au (30 nm /100 nm) and Ti/Au (30 nm/ 100 nm), respectively. The source and the drain contacts are 60 μm long, the gate is 2.6 μm long, source-to-gate distance is 1.4 μm and gate-to-drain distance is 2 μm. The channel width (normal to the page) is 100 μm. We measured DC I-V characteristics of the devices using Microtech Summit 11k probe station and Keithley 4200-SCS. The measurements were recorded one second after the application of bias voltages to account for self-heating and to make sure that steady state is reached.

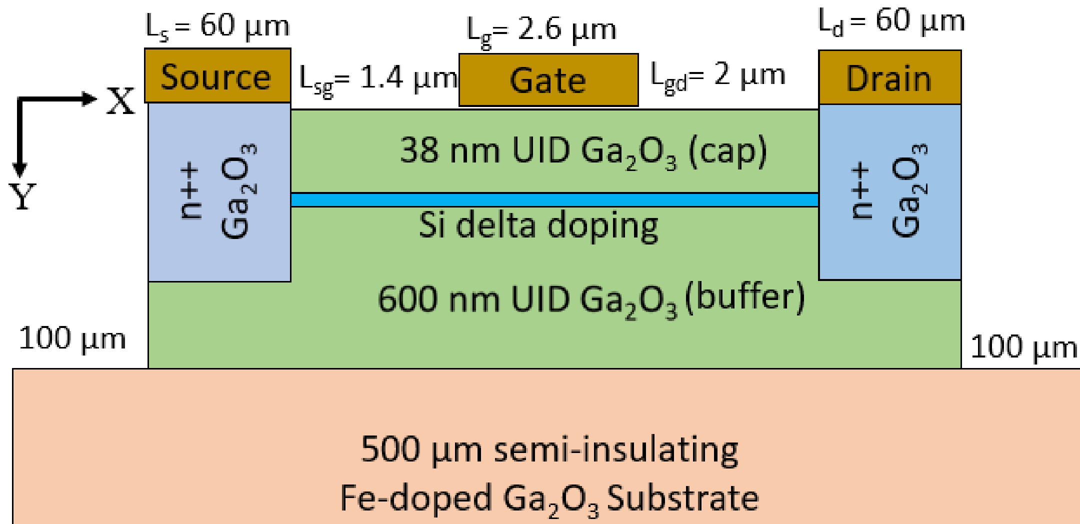


Figure 5.1. A schematic of the MESFET used in the 2-D simulations.

In the 2-D TCAD Sentaurus simulations [151], the substrate is extended by an additional 100 μm on both sides beyond the source and drain pads to allow heat dissipation from the active region as shown in the Figure 5.1. An optimum mesh was generated to

achieve numerical convergence. The grid is of sub-nanometer scale in the active region such as delta-doping layer and of micrometer-scale as we move away from the active region. We use thermodynamic carrier transport model which accounts for self-heating and is suitable for high-power density devices with long active regions. Additional details of this model and other available models can be found in the *Sentaurus Device User Guide* [138]. The bottom of the substrate is set to a constant temperature of 300 K. All other boundaries are considered adiabatic. Temperature and electric field dependence of electron mobility is implemented using Equations (5.1) and (5.2), respectively.

$$\mu_{n,low} = \mu_{n,o}\left(\frac{T_L}{300}\right)^{-\alpha} \tag{5.1}$$

$$\mu_n = \frac{\mu_{n,low}}{\left\{1+\left(\frac{\mu_{n,low}.F}{v_{sat}}\right)^{\beta}\right\}^{1/\beta}} \tag{5.2}$$

Here, $\mu_{n,low}$ is the low-field electron mobility, μ_n is the effective electron mobility considering field dependence, and T_L is the lattice temperature. F is the driving field, which is a function of electric field. We selected default driving field, which is a gradient of quasi-fermi potential. From sensitivity study, it was predicted that electron mobility and I-V characteristics are not significantly affected by variation in v_{sat} and β values. Therefore, temperature dependence of v_{sat} and β is not considered and assumed to be constant. The density of conduction band states (N_c) is considered to be temperature dependent using the relation: $N_c(T_L) = N_{c,300} \times (T_L / 300)^{3/2}$. Here, $N_{c,300} = 3.72 \times 10^{18}$ cm^{-3} is dependent on the effective mass of electron. In addition, other important models such as SRH, Auger,

Table 5.1 Important TCAD Simulation Parameters. [a]The value of the parameter at 300 K.

Symbol	Quantity	Value
α	temperature dependence coefficient	0.5
β	electric field dependence exponent	1
ε	dielectric constant	10
Φ_b	Schottky barrier height	1.4 eV[a]
$\mu_{n,0}$	low-field electron mobility	70[a]
E_g	Ga_2O_3 bandgap	4.8 eV[a]
$k_{x,GaO}$	thermal cond. of Ga_2O_3 in x-dir.	17.1 W/m-K[a]
$k_{y,GaO}$	thermal cond. of Ga_2O_3 in y-dir.	28.9 W/m-K[a]
$k_{x,sub}$	thermal cond. of the Fe-doped Ga_2O_3 substrate in x-dir.	16.6 W/m-K[a]
$k_{y,sub}$	thermal cond. of the Fe-doped Ga_2O_3 substrate in y-dir.	28.8 W/m-K[a]
m_e	effective mass of electron	0.28 m_0

radiative recombination, Fermi-Dirac statistics, bandgap narrowing were considered. The values of important parameters such as dielectric constant [152], Schottky barrier height [153], bandgap [154], effective electron mass [155], saturation velocity [26] etc., are chosen from the literature and summarized in Table 5.1. A net n-type concentration of 3.1 x 10^{16} cm^{-3} is considered in the buffer and the cap layer to account for unintentional doping. This value is in agreement with the experimentally reported values [156]. The thermal conductivity of Ga_2O_3 is an important parameter for accurately predicting the temperature profile in the device. The thermal conductivity of Ga_2O_3 is temperature dependent, and an anisotropic property. We have used temperature and direction-dependent relationships for

the thermal conductivity of Ga_2O_3 and Fe-doped Ga_2O_3 substrate from [96]. The x-axis of the device (see Figure 5.1) is aligned either along crystal direction (102) or perpendicular to (102) in the horizontal plane (~ x-z plane), where z-axis is normal to the page. However, there is insignificant difference in thermal conductivity values along these crystal directions. Therefore, we have used the mean value of thermal conductivity of these two crystal directions for x-axis in 2-D simulations. The y-axis (transverse direction) is aligned with (010) crystal direction, therefore, $k_y=k_{(010)}$.

5.2 2-D Electrothermal Modeling: Validation and Comparison

The experimentally measured and simulated DC I-V characteristics curves are shown in Figure 5.2. We achieved a good agreement between the I-V measurements and the simulations using the thermodynamic model incorporating temperature and electric field dependent electron mobility model. The slight difference in the linear region of I_d-V_{ds} curve at V_{gs} = 2 V could be attributed to the trapping effects as details of all traps are still not known. This difference should not affect the thermal analysis as self-heating is more prominent in the saturation region. We carried out simulations using two additional simplified models– (a) the thermodynamic model with electric field dependence of electron mobility turned off (only temperature-dependent electron mobility considered). The detail of this model is presented in Ref. [151]. (b) The Drift-diffusion model with constant electron mobility and no self-heating (Isothermal simulation at 300 K). The primary difference between the two models is that model (a) solves for the temperature equation, whereas model (b) does not. Model (a) explains well the measurements except it slightly overpredicts the current at higher V_{ds} values, where electric field is high in the device. It was expected because high electric field effect such as electron velocity saturation is

ignored. It leads to overprediction of the electron mobility and thus, overpredicts the current. The model (b) significantly overpredicts the electron mobility as self- heating is

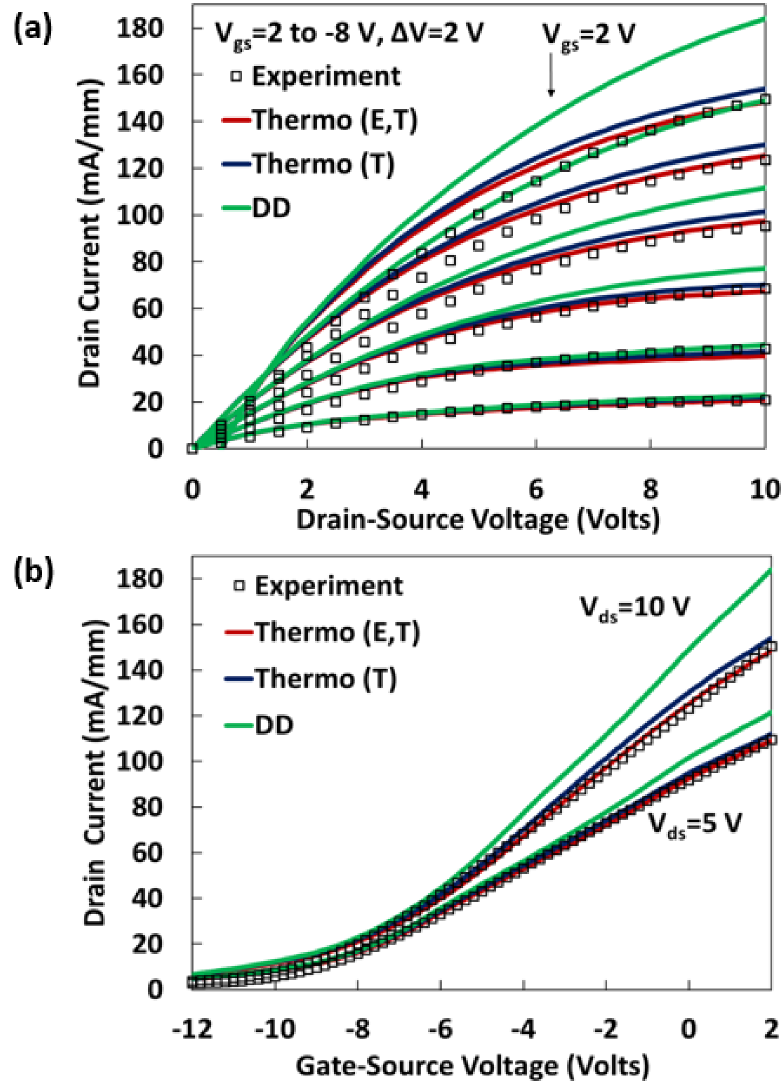


Figure 5.2. Comparison between experimental and simulated DC I-V curves. (a) Output characteristics (b) transfer characteristics. "Thermo (E, T)" and "Thermo (T)" represent simulations using Thermodynamic model incorporating both electric field and temperature dependent electron mobility model and only temperature dependent electron mobility model, respectively. "DD" represents isothermal simulations using Drift-Diffusion model (no self-heating) with constant mobility.

not considered. The overprediction of mobility leads to overprediction of current at high V_{ds} and V_{gs}. At low V_{gs}, power dissipation is small, therefore neglecting self-heating effect does not lead to any error in the simulations. In the rest of the study, we have discussed results obtained from the simulations using the thermodynamic model incorporating temperature and electric field-dependent electron mobility model.

5.3 Effect of Bias Condition on Electrothermal Characteristics

Figure 5.3 shows the change in peak temperature and thermal resistance of the device with respect to V_{ds} and power. The variation in peak temperature with V_{ds} is qualitatively similar to the variation in the power dissipation with V_{ds} (see Figure 5.3 (a)). The curves are non-linear when the device is operating in the linear region and are almost linear in the saturation region. Thermal resistance of the device is defined as ratio of the difference between the peak and ambient (bottom of the substrate ~ 300 K) temperature and the power, i.e., $R_{th} = (T_{peak} - 300)/P_{total}$. Increase in the peak temperature with the power is approximately linear as shown in the Figure 5.3 (b). We observed that peak temperatures are different for different bias voltages even though the power dissipation is same (see inset in Figure 5.3 (b)). Here, peak temperature is smallest for the bias condition with more positive V_{gs}. Choi et al. also observed similar effect of bias voltages on peak temperature in their measurements on AlGaN/GaN HEMTs [157]. The difference in peak temperatures at the same power dissipation but different bias voltages is shown in Figure 5.3 (c). As the power is increased by increasing V_{ds} the difference between peak temperatures of different cases of V_{gs} also increases. Figure 5.3 (d) shows increase in the thermal resistance with increase in the power. We varied the power by varying the V_{ds} for three different V_{gs}, i.e., -6, -2 and 2 V. We could expect the same trend if we plot the variation in thermal resistance

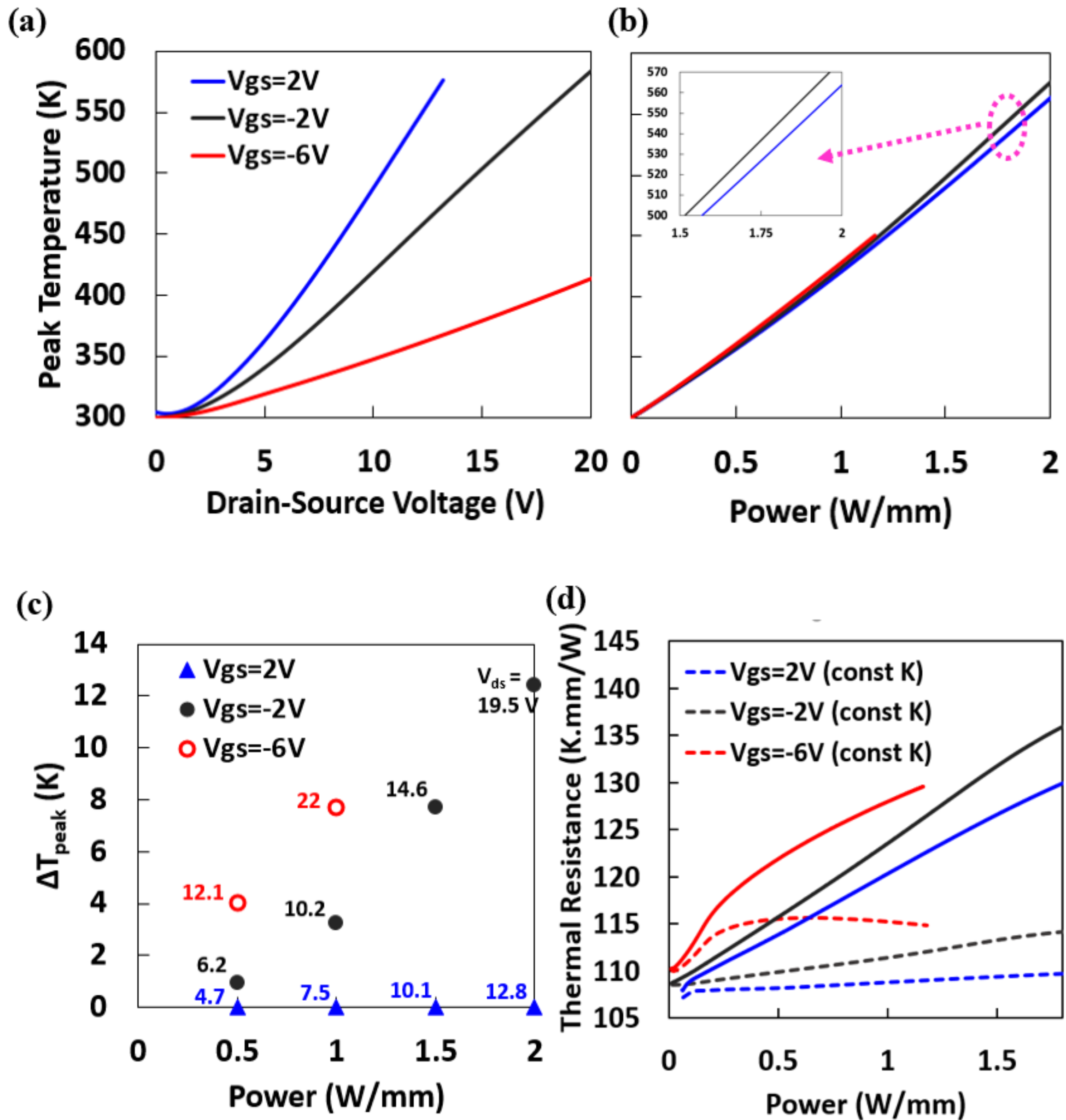


Figure 5.3. Variation in the peak temperature of the device with respect to (a) Vds and (b) power. Inset shows the dependence of the peak temperature on bias voltages (c) Difference in the peak temperatures due to difference in applied bias conditions at a given power. ΔT_{peak} is defined as $T_{peak,Vgs} - T_{peak,Vgs=2V}$ at a given power. The values next to data points represent corresponding Vds. (d) Increase in thermal resistance with peak temperature. Dotted lines assume constant thermal conductivity k, but solid lines considered T dependent conductivity.

with respect to peak temperature because peak temperature is almost linearly dependent on the power dissipation. There are two factors contributing to net increase in thermal resistance with increase in power. First factor is decrease in the thermal conductivity with temperature. The peak and overall temperature of the device will increase with the increase in power. The thermal conductivity of the Ga_2O_3 and Fe-doped Ga_2O_3 substrate decreases with the increase in the temperature and contributes to increase in thermal resistance. The decrease in thermal conductivity with temperature is attributed to enhanced phonon scattering leading to decrease in phonon mean free path [158]. The second factor is change in electron Joule heat generation profile with change in power (at a given V_{gs}). To show that, we performed simulations assuming constant thermal conductivity (not a function of temperature) for Ga_2O_3 and Fe-doped Ga_2O_3 substrate and plotted variation in thermal resistance against power (shown by dotted lines in Figure 5.3 (d)). Since, thermal conductivity is assumed to be constant, this change in thermal resistance with power is entirely due to change in the electron Joule heat generation profile with change in power. However, this change in thermal resistance is minor and most of the change in thermal resistance with power is due to decrease in the thermal conductivity of the Ga_2O_3 and Fe-doped Ga_2O_3 substrate layers with temperature. The trend of thermal resistance versus power is different at different V_{gs} because the variation in electron Joule heat profile with power is different at different V_{gs}. We can also comprehend the trends of the curves obtained from constant conductivity simulations in Figure 5.3 (d) in context of Joule heat profile. At V_{gs} = -6 V, when power increases due to increase in V_{ds}, the 2-DEG channel starts depleting near the gate edge of the drain side and path of the current flow changes. It leads to change in Joule heat profile near gate edge of the drain side. There is an increase

in the thermal resistance with power up to 0.25 W/mm as the Joule heating density is increasing in the buffer near the gate edge of the drain side. The channel is almost fully depleted near gate edge of the drain side at power ~ 0.25 W/mm (~V_{ds} ~ 7V). After 2-DEG channel is fully depleted, there is negligible change in the Joule heat profile with power and, therefore, no significant change in thermal resistance is observed. The minor decrease in the thermal resistance beyond 0.25 W/mm can be attributed to the spreading of Joule heat profile in the buffer. At V_{gs} = -2 V, the depletion of 2-DEG channel with power near the gate edge of the drain side is slower than that at V_{gs} = -6 V and the channel is not fully depleted in the range of power (0 -1.7 W/mm) considered in Fig. 3 (d). At V_{gs} =2 V, no depletion of 2-DEG is observed up to power =1.7 W/mm. Therefore, the thermal resistance is increasing at V_{gs} = ± 2 V and should keep increasing until the full depletion of the 2-DEG channel.

It is evident that peak temperature is strongly dependent upon the power, but to understand how peak temperature is dependent on bias conditions while keeping the power constant, we have compared the electron Joule heat generation profiles of two different bias conditions– (a) Bias-A: V_{ds}=8.3 V and V_{gs}=2 V (b) Bias-B: V_{ds}=25 V and V_{gs}=-6 V, dissipating the same power (=1.16 W/mm) as shown in Figure 5.4 (a) and (b). Figure 5.4 (c) and (d) compare the electron Joule heating profiles of Bias-A and Bias-B along y-axis at x = 164.3 µm (gate edge on drain side and location of peak temperature) and x-axis at y = 38 nm (location of delta-doping layer), respectively. These bias conditions are chosen for a better understanding of the changes in peak temperature and hot spot location when the gate bias is swept from positive to negative values but keeping power constant by increasing V_{ds}. Most of the heat in Bias-A is generated in the delta-doping layer, whereas

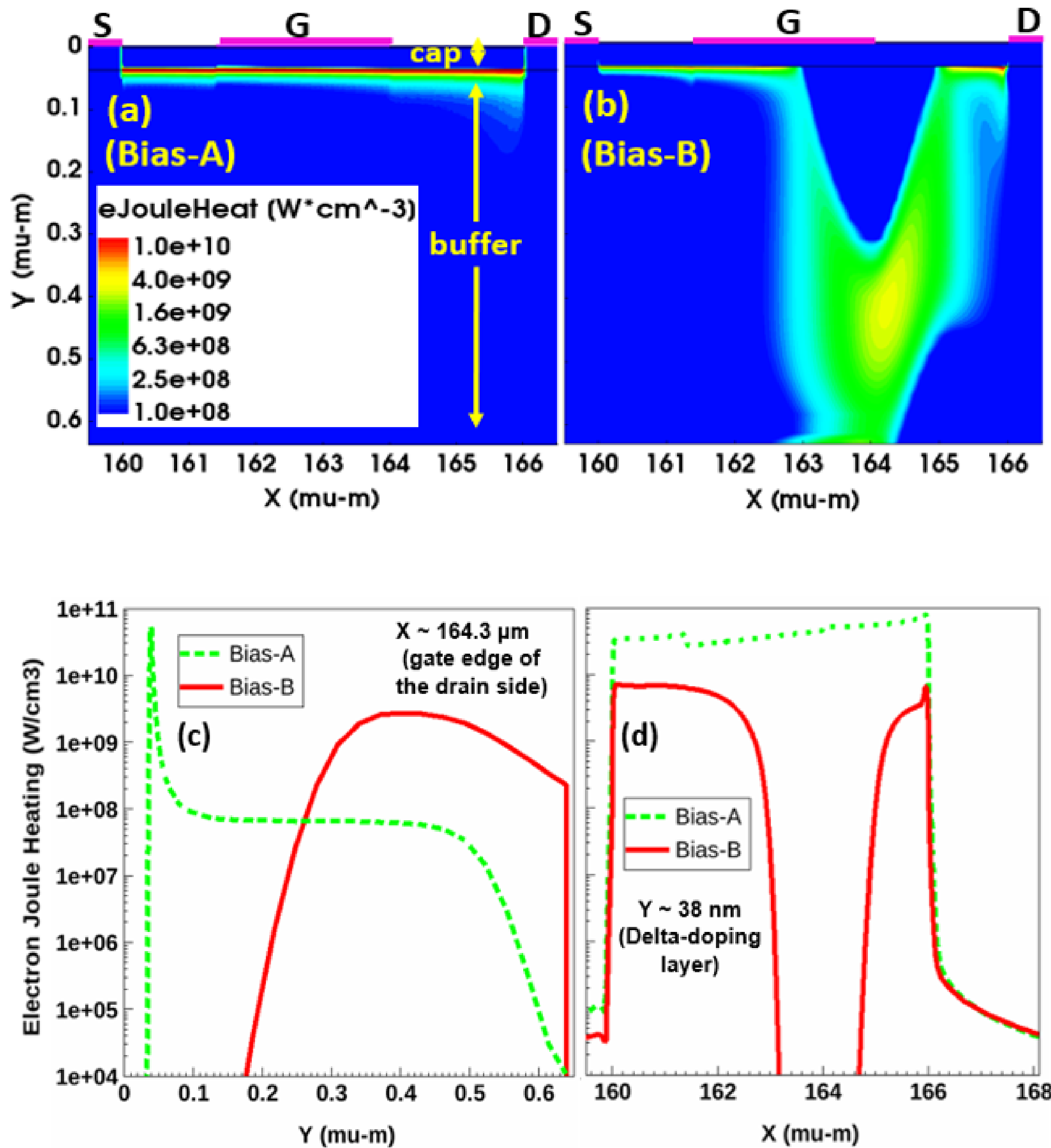


Figure 5.4. Electron Joule heat density profiles in the device when power =1.16 W/mm with (a) Bias-A: V_{ds}=8.3 V and V_{gs}=2 V (b) Bias-B: V_{ds}=25 V and V_{gs}=-6 V. Note that x and y axes have different scaling factor in these contour plots and subsequent contour plots. Variation of electron Joule heating for Bias-A and Bias-B along (c) y-axis at x = 164.3 µm (gate edge on drain side and location of peak temperature) and (d) x-axis at y = 38 nm (delta doping layer location).

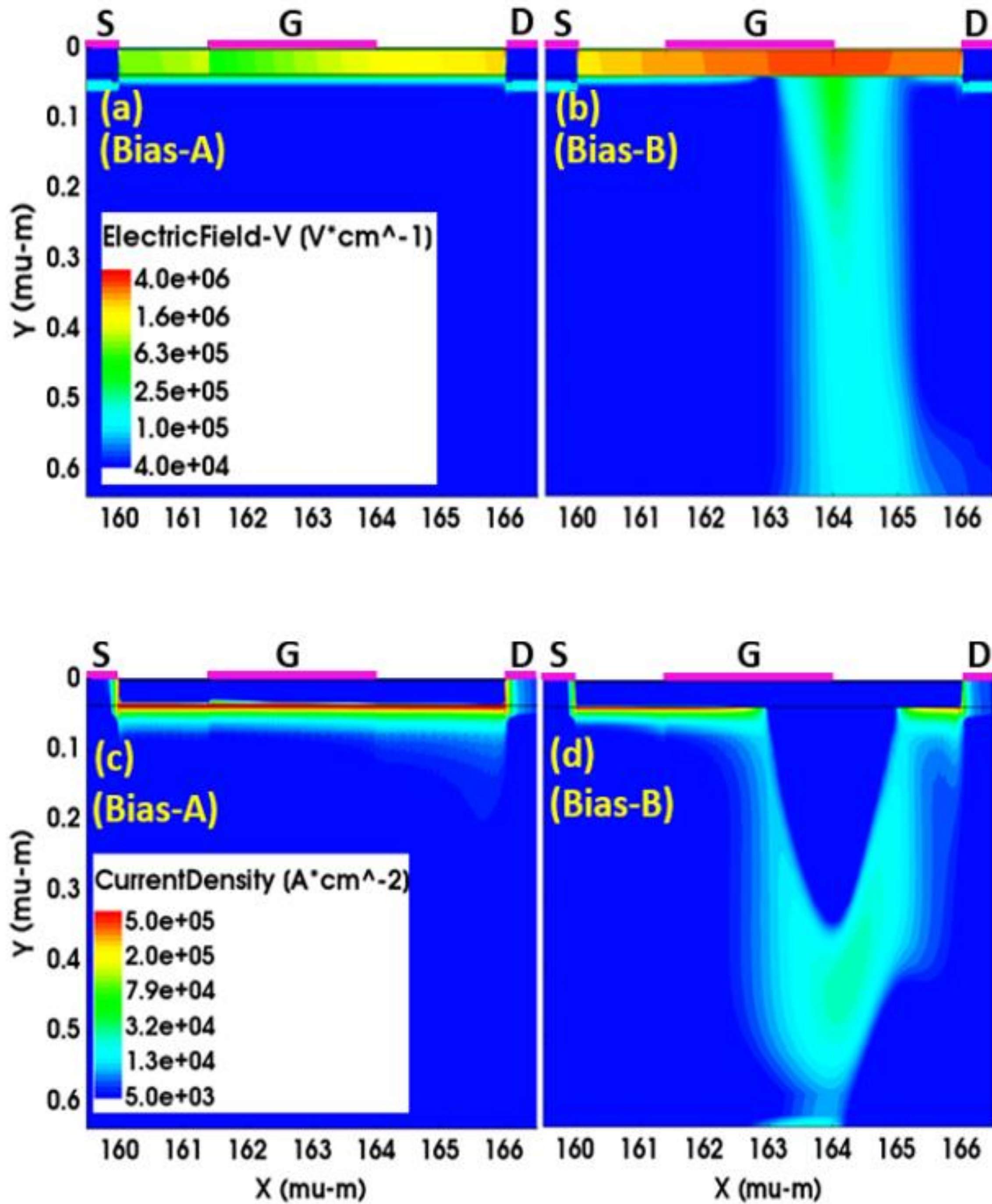


Figure 5.5. Variation in the electric field at (a) Bias-A (V_{ds}=8.3 V and V_{gs}=2 V) (b) Bias-B (V_{ds}=25 V and V_{gs}=-6 V), and current density at (c) Bias-A (d) Bias-B in the device when power is 1.16 W/mm.

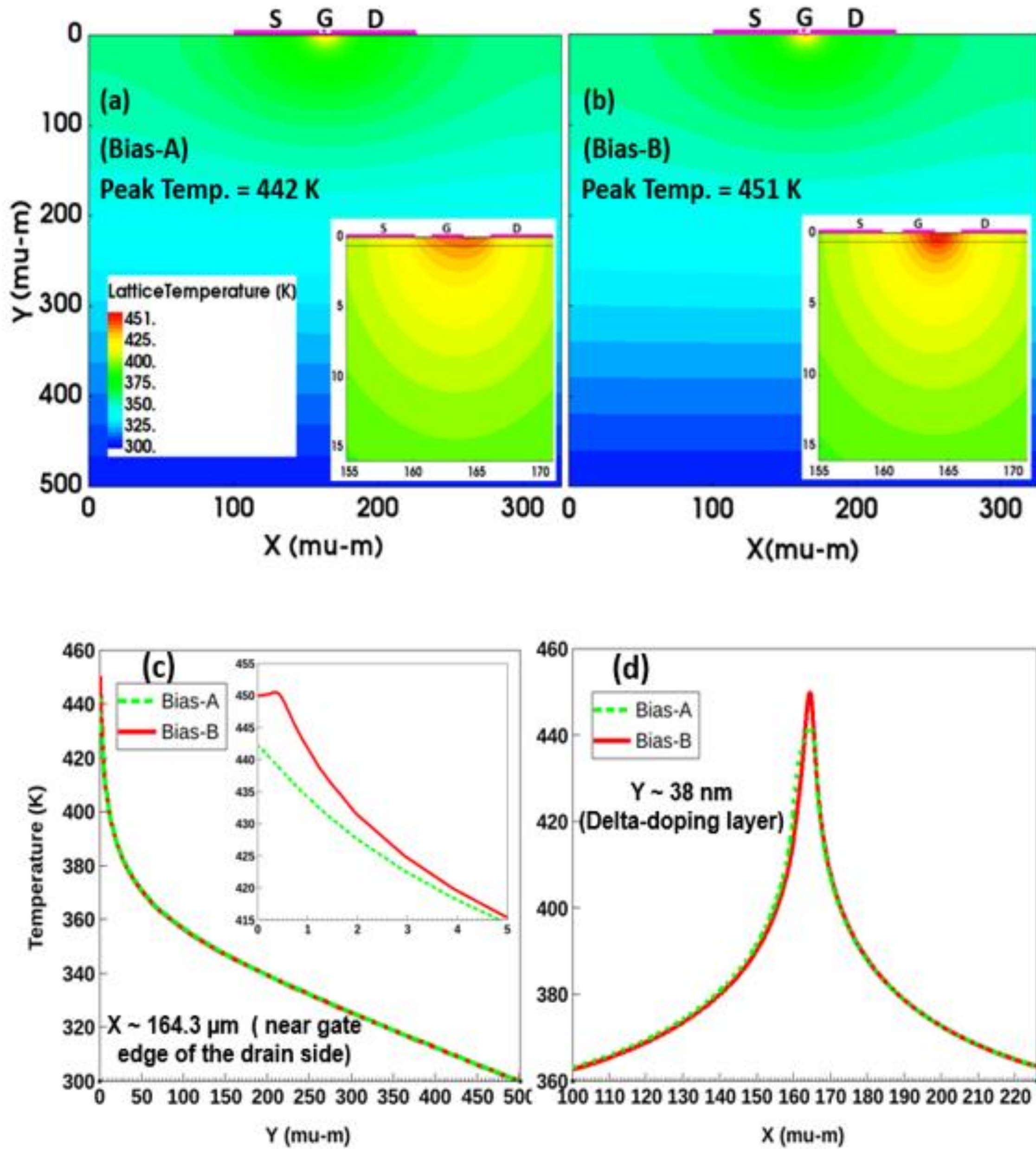


Figure 5.6. Temperature profiles in the device when power =1.16 W/mm at (a) Bias-A (V_{ds}=8.3 V and V_{gs}=2 V) (b) Bias-B (V_{ds}=25 V and V_{gs}= – 6 V). Variation of temperature for Bias-A and Bias-B along (c) y-axis at x = 164.3 μm and (d) x-axis at y = 38 nm.

in Bias-B, most of the heat generation occurs in buffer layer. It is expected, because in the case of Bias-A, a 2-dimensional electron gas (2-DEG) is created where the delta-doping layer is located. However, in the case of Bias-B, a negative gate voltage depletes the 2-

DEG near the gate edge of the drain side and thus, there is a change in the path of the current flow in the device. Current must flow through the buffer layer under the gate edge of the drain side. Since, Joule heating is a scalar product of electric field and current density, we have shown variation of electric field and current density at Bias-A and Bias-B in Figure 5.5. Figure 5.5 (a) and (b) show the electric field profiles at the Bias-A and the Bias-B, respectively, and we observe that electric field is significantly higher in the cap layer than in the buffer layer for both bias conditions. It is most likely a consequence of fixed charges in the 2-DEG, traps at the top surface and applied gate voltage. Figure 5.5 (c) and (d) show the current density profiles at the Bias-A and the Bias-B, respectively and we can observe that the path of current flow changes with change in the applied bias

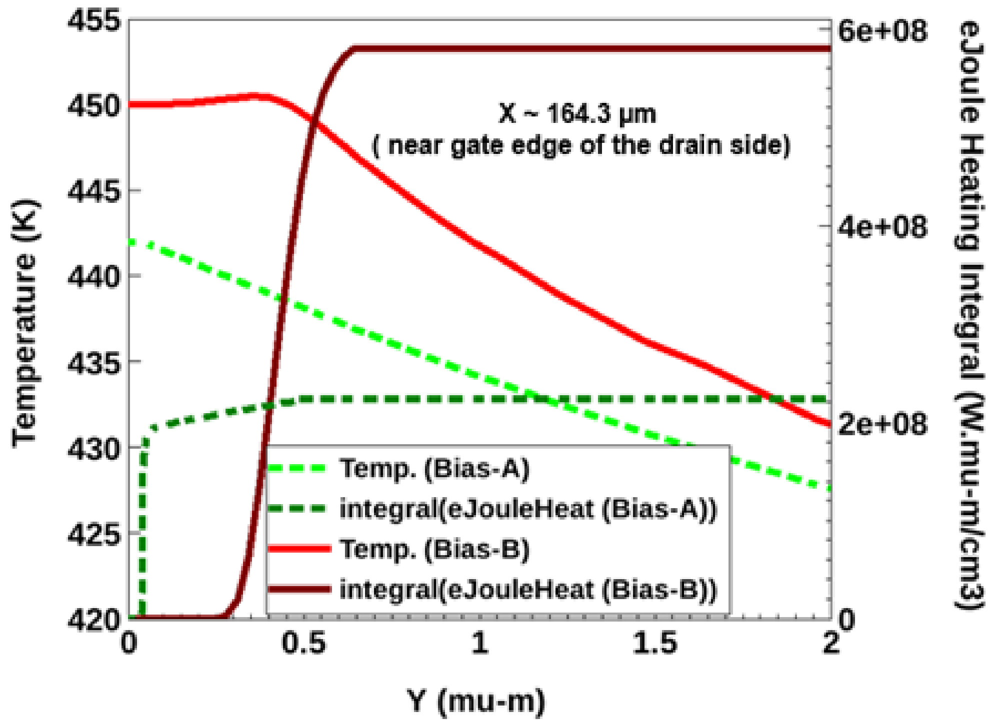


Figure 5.7. Temperature and integral of electron Joule heating along x =164.3 μm at Bias-A and Bias-B with power =1.16 W/mm.

condition. The total heat density profile is qualitatively similar to the total current density profile at the corresponding bias condition. Interestingly, the change in bias conditions does not significantly affect the location of peak temperature in the device. It only affects the magnitude of peak temperature, for example, a difference of about 9 K in peak temperature is observed between Bias-A and Bias-B, but the location of the peak temperature is still near the 2-DEG and the gate edge of the drain side, as shown in Figure 5.6 (a)-(d). This difference in peak temperature could be attributed to the difference in integral of electron Joule heating along the y-direction. We have plotted an integral of electron Joule heating and the temperature near the gate edge of the drain side (at x ~164.3 μm) along y-direction, as shown in Figure 5.7. The integral of electron Joule heating is lower for Bias-A, which leads to a lower peak temperature for Bias-A.

5.4 Effect of Device Structure and Dimensions on Electrothermal Characteristics

The development of Ga_2O_3-based delta-doped MESFETs is still in its early stages. The simulations could guide future design and fabrication by suggesting how the location of doping or miniaturization of device could affect performance. Usually, gate-drain spacing (L_{gd}) is an important parameter to improve the breakdown voltage of the device. Therefore, first, we studied the effect of L_{gd} on some of the important electrical and thermal characteristics of the devices such as on-resistance, saturation current and peak temperature. We varied L_{gd} by keeping source-drain spacing (L_{sd}) and source-gate spacing (L_{sg}) constant (i.e., gate length was changed to accommodate the change in gate-drain spacing). The increase in L_{gd} leads to increase in saturation current, unchanged on-resistance, slight decrease in peak temperature and decrease in threshold voltage (makes

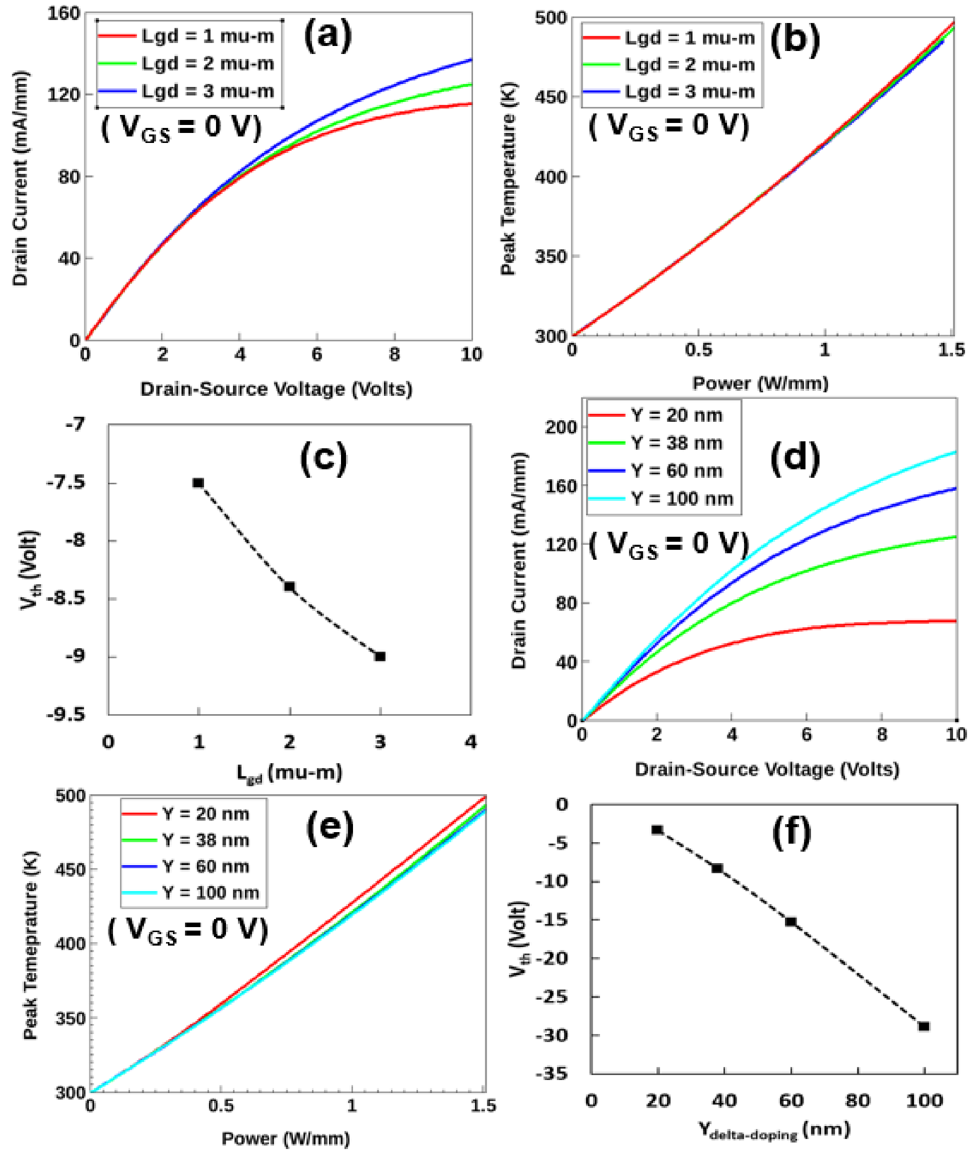


Figure 5.8. Effect of gate-drain spacing and location of delta-doping on the device output characteristics. To study effect of gate-drain spacing, the distance between source and drain is kept 6 μm and gate-drain spacing is varied by varying the length of the gate. The three cases studied have: L_{gd}=1 μm and L_g=3.6 μm, L_{gd}=2 μm and L_g=2.6 μm (actual device), L_{gd}=3 μm and L_g=1.6 μm. (a) Output characteristics at V_{gs}=0 V (b) Peak temperature variation with the power dissipation in the device (c) Change in threshold voltage of the device with respect to L_{gd}. Then, to study the effect of location of delta-doping, the distance between gate and delta-doping layer is set to 20 nm, 38 nm (actual device), 60 nm and 100 nm. Effect of location of delta-doping in the device on (d) Output characteristics at V_{gs}=0 V (e) Peak temperature with the power dissipation, (f) Change in the threshold voltage with the location of delta-doping layer.

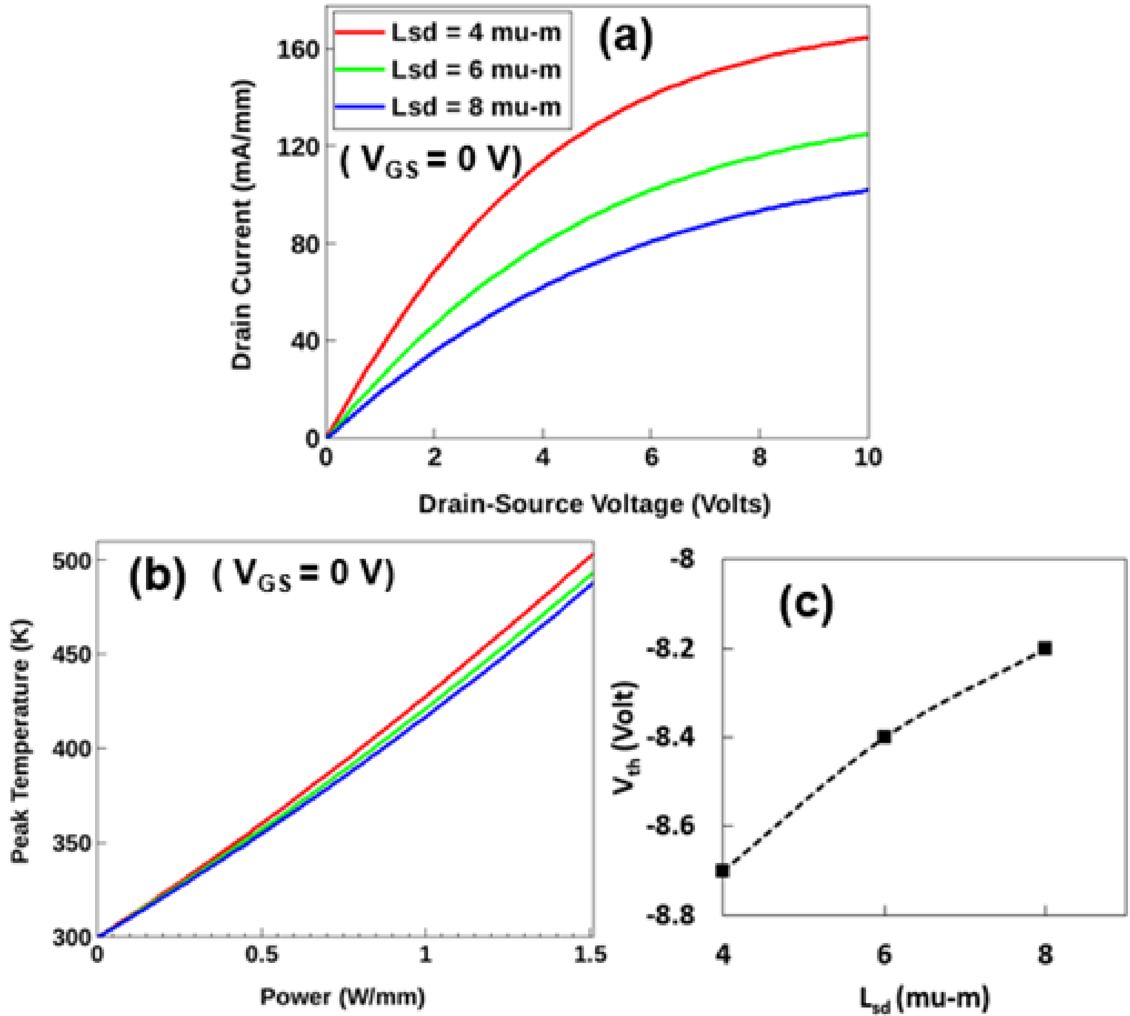


Figure 5.9. Effect of source-to-drain length on the device output characteristics. The distance between source and drain is set to 4 μm (L_{sg}=0.93 μm and L_g=1.74 μm), 6 μm, (actual device), and 8 μm (L_{sg}=1.86 μm and L_g=3.47 μm. (a) Output characteristics at V_{gs}=0 V (b) Peak temperature variation with the power dissipation in the device (c) Change in threshold voltage of the device with the location of delta-doping layer.

turning off the device harder), as shown in Figure 5.8 (a)-(c). Therefore, it is a compromise between higher saturation current and lower threshold voltage. Then, we studied the effect of the location of the delta-doping layer on the device characteristics (see Figure 5.8 (d)-(f)). The increase in distance between gate and delta-doping layer significantly lowers on-resistance and improves saturation current. The improvement in these characteristics is

non-linear with respect to increase in the distance. For a given power, the peak temperature is lowest when delta-doping layer farthest from the gate. However, the drawback of increasing the distance between gate and delta-doping layer is that it significantly decreases the threshold voltage of the device, thus, making it more difficult to turn off the device. Finally, we varied L_{sd} to study its effect on device characteristics (see Figure 5.9). The decrease in the channel length leads to a significant decrease in on-resistance and increase in the saturation current. In addition, threshold voltage does not decrease significantly with the L_{sd}. Peak temperature is affected but it does not increase drastically with decrease in the length at low power. The reduction in the length improves output characteristics without aggravating the heat dissipation problem at low power. However, at high power settings, higher peak temperature in smaller channel devices compared to longer channel devices may also lead to higher leakage current in smaller channel devices. At a given power, the smaller channel devices may require more efficient (or expensive) cooling techniques compared to longer channel length devices to achieve the same peak temperature limit because heat generation density is higher in smaller channel device.

5.5 Closure

We developed a 2-D electro-thermal model, which accounts for self-heating and incorporates an electric field and temperature-dependent mobility model. A good agreement was achieved between the measured and computed I-V characteristics at various bias voltages, which validates the developed model. We studied the effect of bias conditions on electric field, current density, Joule heating profile and peak temperature in the device. Peak temperature strongly depends on the power. However, at a given power dissipation, different bias voltages could lead to different Joule heating profile and thus, to

different peak temperatures. Therefore, the knowledge of Joule heat generation profile is important in predicting accurate peak temperature. We studied the effect of L_{gd}, the location of delta-doping layer and L_{sd} on the device I-V characteristics and peak temperature. The increase in L_{gd} improves saturation current without affecting on-resistance but it decreases threshold voltage and, thus, makes turning off the device difficult. The increase in the distance between delta-doping and gate improves on-resistance and decreases saturation current, but it also makes turning off the device significantly difficult. However, decrease in the L_{sd} can significantly improve on-resistance and saturation current without drastically decreasing the threshold voltage and aggravating the problem of heat dissipation at low power.

CHAPTER 6. ULTRAFAST THERMAL IMAGING, THERMAL MODELING AND THERMAL MANAGEMENT OF BETA-GALLIUM OXIDE MESFETS

In this work, we investigated the thermal characteristics of a recently developed delta-doped β-Ga_2O_3 MESFET using thermoreflectance imaging technique, which enabled temperature measurement with ~ 250 nm spatial and ~ 400 ns temporal resolution. To the best of our knowledge, it was first study on transient measurements of β-Ga_2O_3 FETs. We measured the temperature contours on source, drain and gate pads and estimated peak temperature at different bias conditions. A 3-D diffusive thermal model combined with a device thermodynamic carrier transport model was developed and validated against the thermal measurements. We used this model to predict the temperature profile inside the device and study effectiveness of various device-level thermal management techniques. A compact thermal model was also developed based on experimental measurements and thermal time constants were estimated. The compact model is useful in predicting the temperature rise and drop when the device is turned on and off, respectively.

6.1 Measurements and Modeling Approach

The cross-sectional view of the device used in this study is shown in Figure 6.1 (a). It was fabricated using molecular beam epitaxy (MBE). The detailed description of fabrication process is reported in [150]. An unintentionally doped (UID) (010)-oriented β-Ga_2O_3 buffer layer of thickness 600 nm was grown on 500 μm thick Fe-doped semi-insulating (010) β-Ga_2O_3 substrate. The silicon delta-doped layer of concentration around

1.6×10^{13} cm^{-2} is located between 38 nm UID β-Ga_2O_3 cap and the buffer layer. Thus, it is located 38 nm below the top edge of the device. Schottky barrier at the gate and ohmic contacts at source and drain are formed using Ni/Au (30 nm /100 nm) and Ti/Au (30 nm/ 100 nm) metal stacks, respectively. The lengths of gate contact (L_g), drain contact (L_d), and source contact are 2.85 μm, 60 μm, 60 μm, respectively. The source-gate spacing (L_{sg}) and gate-drain spacing (L_{gd}) are 1.05 μm and 2.4 μm, respectively. The channel width (normal to the page) is 100 μm. The DC I-V characteristics are shown in Figure 6.1 (b). The I-V characteristics of the devices were measured using Microtech Summit 11k probe station and Keithley 4200-SCS. The Microsanj thermoreflectance system NT210B with piezoelectric stage is used for thermoreflectance imaging. The measurement technique and the experimental setup was described in the Chapter-3.

A 2-D electrothermal model, which was developed using thermodynamic carrier transport model in TCAD Sentaurus was used to predict Joule heat profile in the device. First, the simulated I-V curves were verified against the experimental data. Then, the simulated Joule heat profile is given as an input in 3-D diffusive thermal model in Ansys Fluent to accurately predict the temperature distribution in the device [151]. Both the 2-D electrothermal TCAD model and 3-D diffusive thermal model are discussed in detail in Chapter-4. Temperature and direction dependence of the thermal conductivity of Ga_2O_3 and Fe-doped Ga_2O_3 substrate is obtained from [96]. There is insignificant difference in thermal conductivity in the x-z plane. Therefore, we have used the mean value of thermal conductivity of these two crystal directions in the lateral plane. The y-axis is aligned with (010) crystal direction, therefore, $k_y = k_{(010)}$. The bottom of the substrate is set to isothermal

boundary condition at 27 ºC (300 K) and all other boundaries of the domain are assumed to be adiabatic.

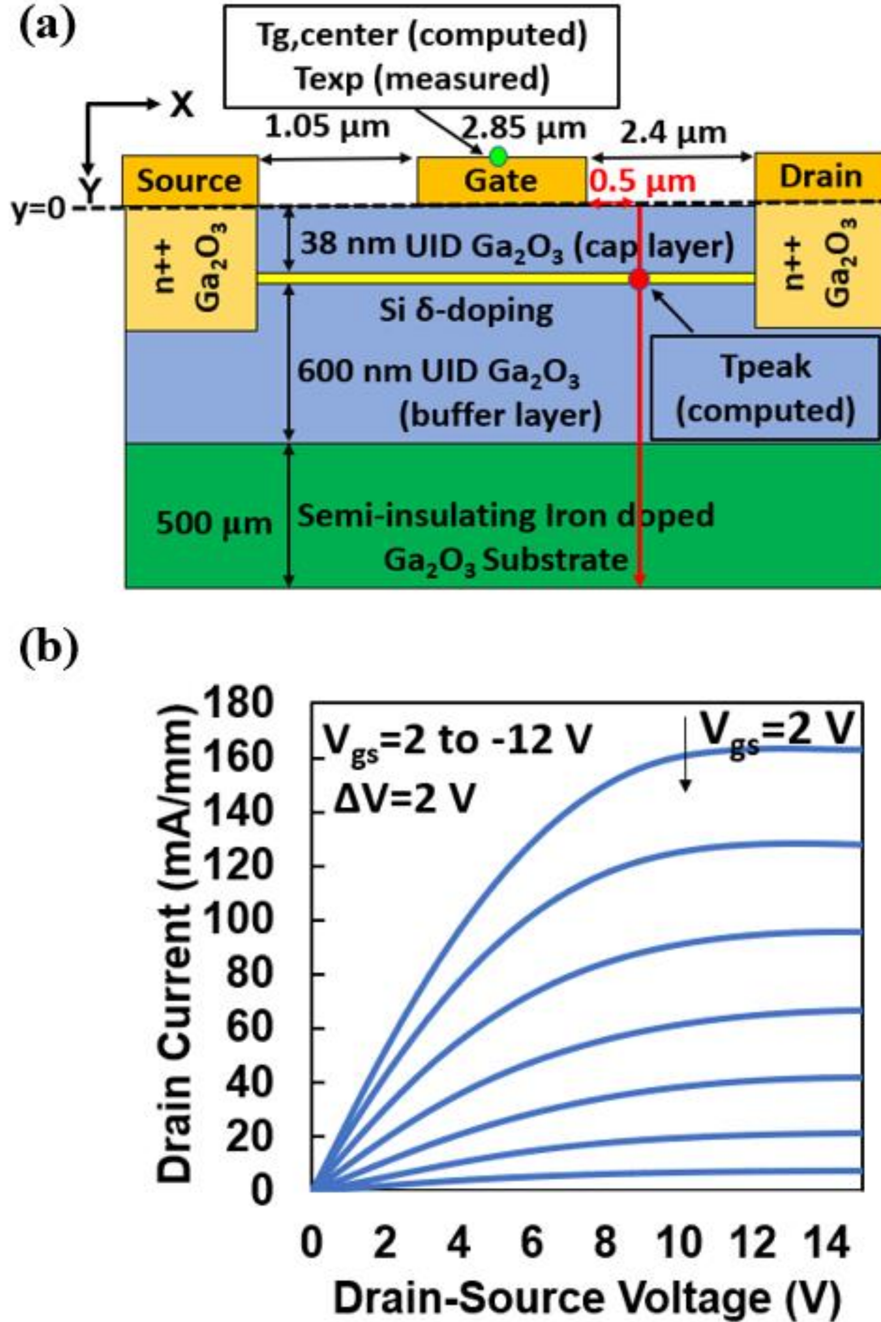


Figure 6.1. (a) A schematic of the β-Ga_2O_3 delta-doped MESFET (not drawn to scale), (b) Measured I-V output characteristics.

6.2 Steady-State Thermoreflectance Imaging and 3-D Diffusive Thermal Modeling

First step in thermal measurements is the estimation of thermoreflectance coefficient (C_{th}), which relates relative change in the reflectivity of a surface to the temperature change of the surface. C_{th} is defined in Chapter-3. A large value of C_{th} is desirable for high signal to noise ratio and the accurate measurements. Since, the top surface of electrode pads is gold, we used 530 nm green LED as light source because the thermoreflectance coefficient of gold for this wavelength is known to be significantly high [27]. A 100x magnification lens was used for calibration and measurements as it can provide up to ~250 nm spatial resolution with high signal to noise ratio. The thermoreflectance coefficient over the electrodes was determined to be $1.80 \times 10^{-4} \pm 1.29 \times 10^{-5}$ by measuring the change in the surface reflectivity with ~ 90 ºC change in temperature of the electrodes. After obtaining the C_{th}, temperature measurements were performed.

The CCD image of the electrodes is shown in Figure 6.2 (a), where source, drain, and gate regions are also marked. Steady-state temperature map of the electrodes at power dissipation of 2.56 W/mm (gate-to-source voltage, V_{gs} = 2 V and drain-to-source voltage ,V_{ds} = 20 V) is shown in Figure 6.2 (b). The temperatures are measured only on the top surface of the electrodes. The temperature at bottom of the substrate (T_{base}) is maintained at 27 ºC. The temperature data on the Ga_2O_3 and edges of the electrodes are excluded due to low intensity of light reflected from these areas, which translated into large uncertainties. The highest temperature on the electrodes is measured in the central region of the gate (see Figure 6.2 (b)). However, from the simulations, we determined that overall peak temperature (also referred as hotspot or Tpeak) of the device is not located on the electrode surfaces but located inside the device. It is estimated to be in the delta-doping layer and ~

0.5 μm away from the gate- edge towards drain as shown in Figure 6.2 (a). Figure 6.3 (a) presents the measured temperature (Texp), computed temperatures at the drain side gate-edge (Tg,max), source side gate-edge (Tg,min), center of the gate (Tg,center), and Tpeak

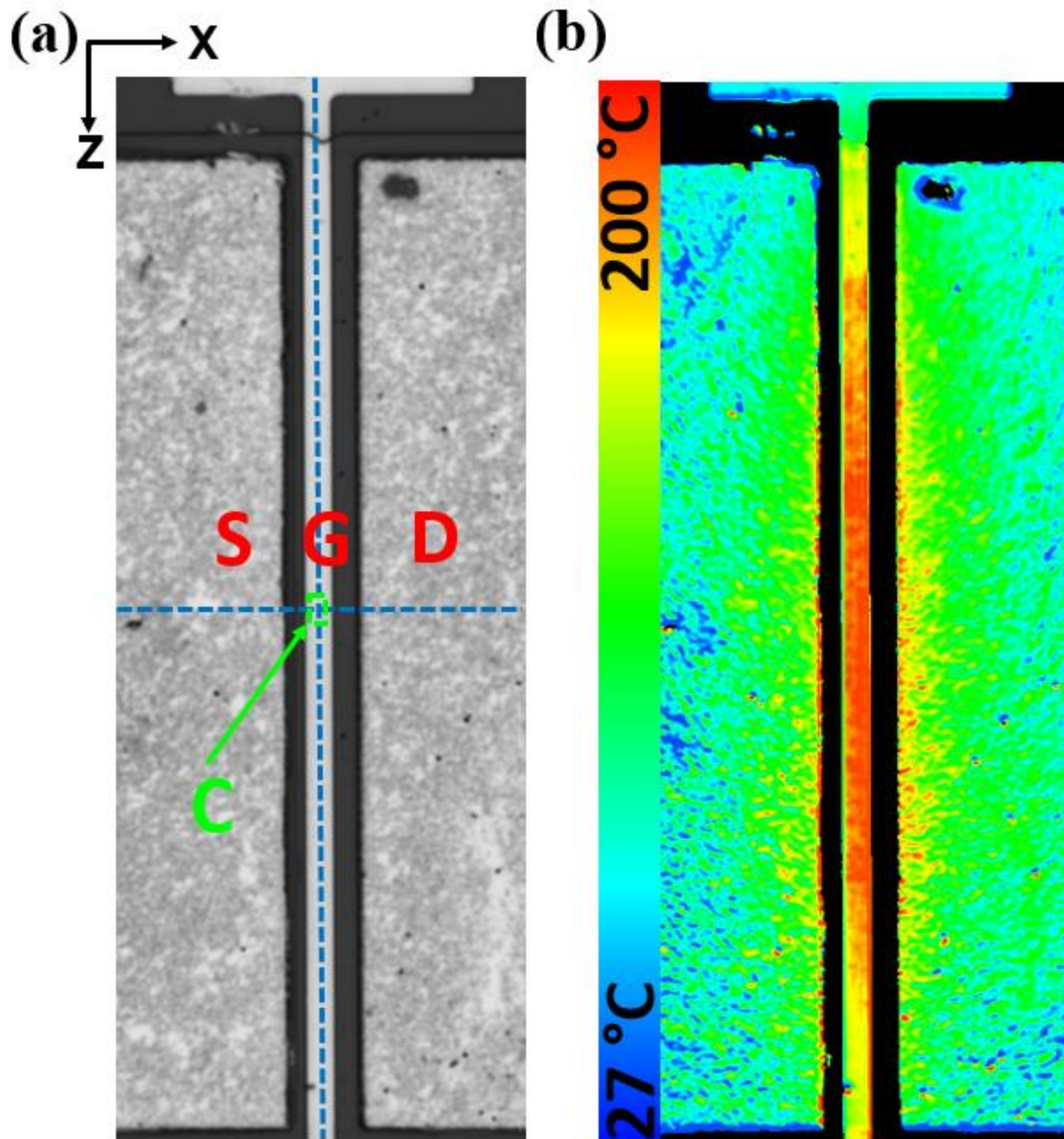


Figure 6.2. (a) A CCD image of the device using 100x objective, (b) Temperature contours of the electrodes at power = 2.56 W/mm obtained from thermoreflectance imaging.

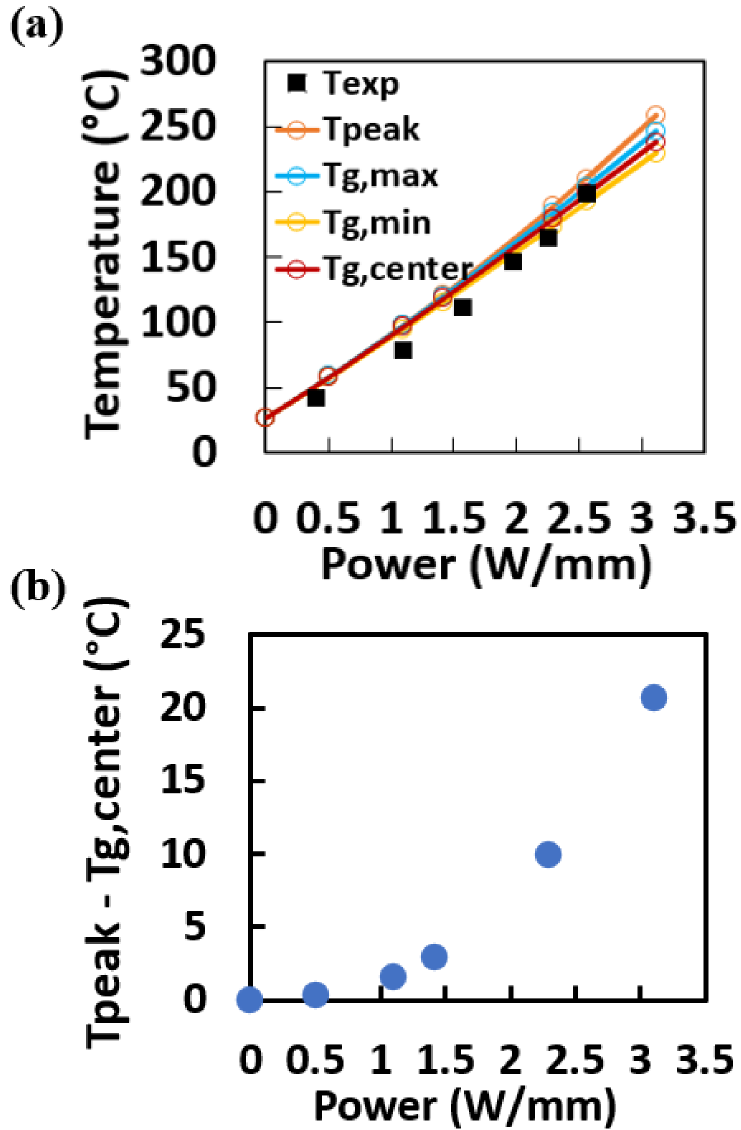


Figure 6.3. (a) Comparison of measured and computed temperatures at the gate-center 'C' in steady-state at various power settings. (b) The difference between computed overall peak temperature (T_{peak}) and computed gate-center temperature ($T_{g,center}$) with power.

as a function of power at Vgs =2V. A small region of interest was chosen at the center of the gate (shown by green rectangle and marked as 'C' in Figure 6.2 (a) and by green circle in Figure 6.1 (a)), avoiding the edges, for measuring Texp as a function of power. A good match is obtained between Texp and Tg,center (computed at the same location) , as shown

in Figure 6.3 (a). The uncertainty bounds (95.4 % confidence interval) in temperature measurement (U_T) are: ± 0.0718 x (Texp - Tbase), e.g., the steady-state Texp is 199 ± 12.3 °C at power = 2.56 W/mm. The difference between Tpeak and Tg,center as a function of power dissipation is shown in Figure 6.3 (b). As expected, the difference is increasing with increase in power dissipation and the non-linearity of the trend can be attributed to temperature dependence of the thermal conductivity.

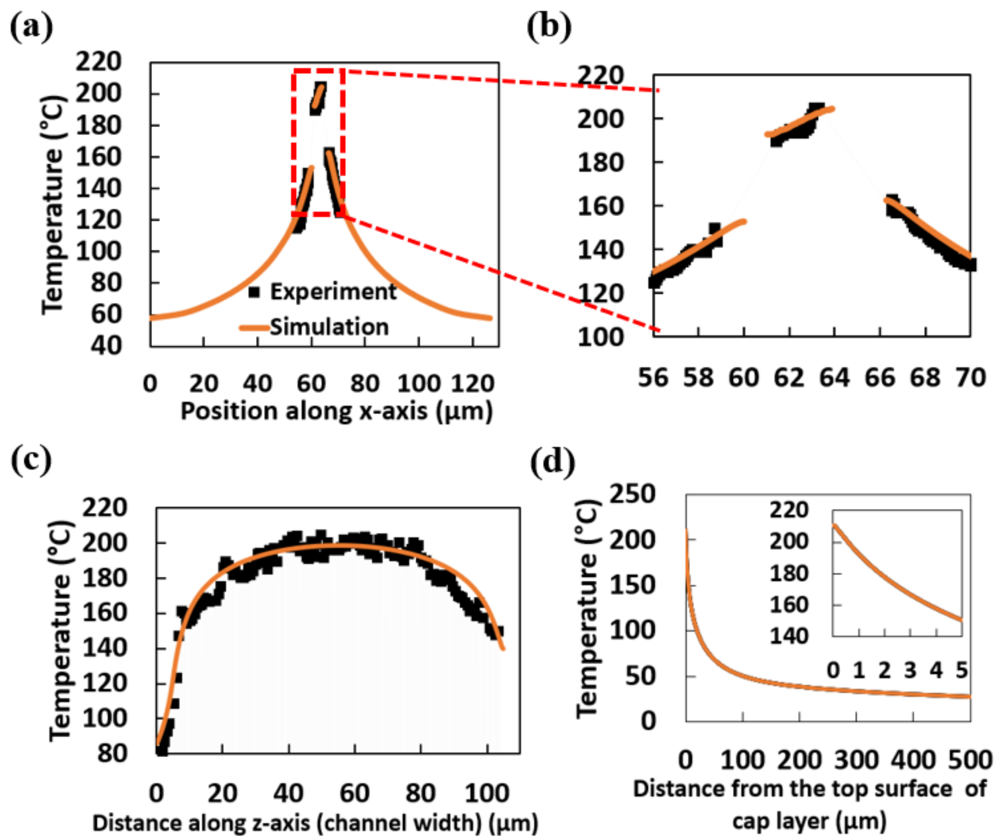


Figure 6.4. Spatial variation in measured and computed temperatures at steady-state at power = 2.56 W/mm. Variation in temperature (a) along the horizontal dotted-line shown in Figure 6.2(a) with (b) a close-up, (c) along the vertical dotted-line and (d) predicted from simulations along y-direction (depth of the device) on the red solid line passing through hotspot as shown in Figure 6.1(a). The dotted lines and gate-center 'C' is marked in Figure 6.2(a). Black markers are measured temperature and solid lines are simulated results.

The measured and computed temperature profiles along the x-axis in the middle of the channel are shown in Figure 6.4 (a). As explained earlier, the measured temperature data on the edges and Ga_2O_3 channel is excluded (see Figure 6.4 (b)). The drain side of gate-edge has the highest temperature among all electrode pads. Figure 6.4 (c) presents the temperature profile along the z-axis at the gate-centerline. There is a sharp drop in the temperature close to the edges of the channel. Figure 6.4 (d) presents the computed temperature profile along the y-axis (depth of the device) on the red solid line passing through hotspot as shown in Figure 6.1 (a). Although the hotspot is located in the delta-doping layer, there is negligible variation in the temperature between top surface of cap layer and hot-spot along y-axis. There is sharp drop in the temperature along y-axis in the buffer layer, as shown in Figure 6.4 (d). The initial non-linearity indicates temperature dependent and anisotropic thermal conductivity and heat spreading effects. Linear profile beyond ~ 100 μm suggests that rest of the substrate could be modeled using a 1-D resistance model.

6.3 Transient Thermoreflectance Imaging and 3-D Diffusive Thermal Modeling

In this section, transient thermoreflectance imaging and 3-D diffusive thermal modeling using Ansys Fluent are performed to understand transient thermal behavior of the device. Figure 6.5 (a) presents the transient measurements for a 500 μs pulse width and 25% duty cycle for three different power and bias settings—Case-A (power = 3.25 W/mm, V_{ds} =20V and V_{gs} = 2 V), Case-B (power = 2.04 W/mm, V_{ds} =13.3 V and V_{gs} = 2 V), Case-C (power = 1.85 W/mm, V_{ds} =20V and V_{gs} = -2 V). The pulse width of the LED for the measurements is ~400 ns, which is also the temporal resolution of these measurements. A good match is obtained between T_{exp} and $T_{g,center}$ for transient thermal measurements at

different power settings. In Figure 6.5 (b), we have compared change in ΔT_{pc} (T_{peak} – $T_{g,center}$) as a function of time for the three cases. As expected, the ΔT_{pc} increases as power increases at V_{gs} =2 V.

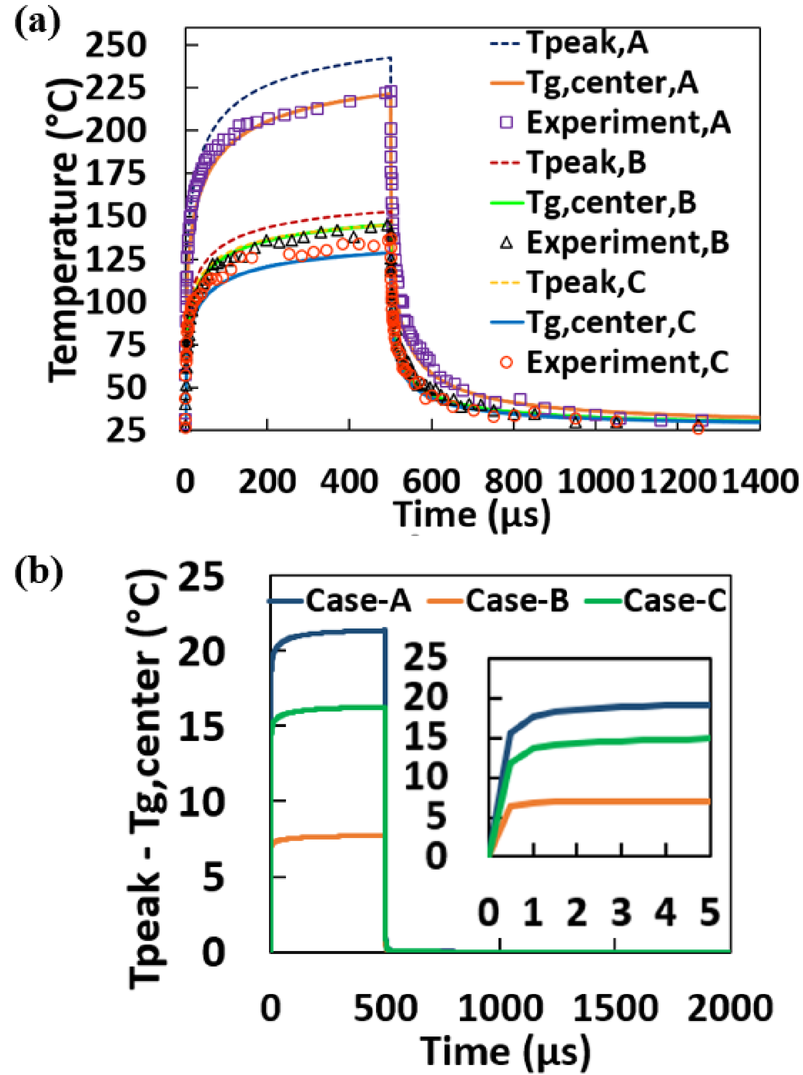


Figure 6.5. Transient thermal measurements at the gate-center 'C', which is marked in Figure 6.2 (a). Measured and computed temperatures for a pulse width of 500 µs and 25% duty cycle (i.e., pulse period is 2 ms) for (a) Case-A: power = 3.25 W/mm (V_{gs} = 2 V; V_{ds}= 20 V), Case-B: power = 2.04 W/mm (V_{gs} = 2 V; V_{ds} = 13.3 V), and Case-C: power = 1.85 W/mm (V_{gs} = -2 V; V_{ds} = 20 V). (b) difference between the computed peak temperature and the computed gate center temperature with time for Case-A, B and C.

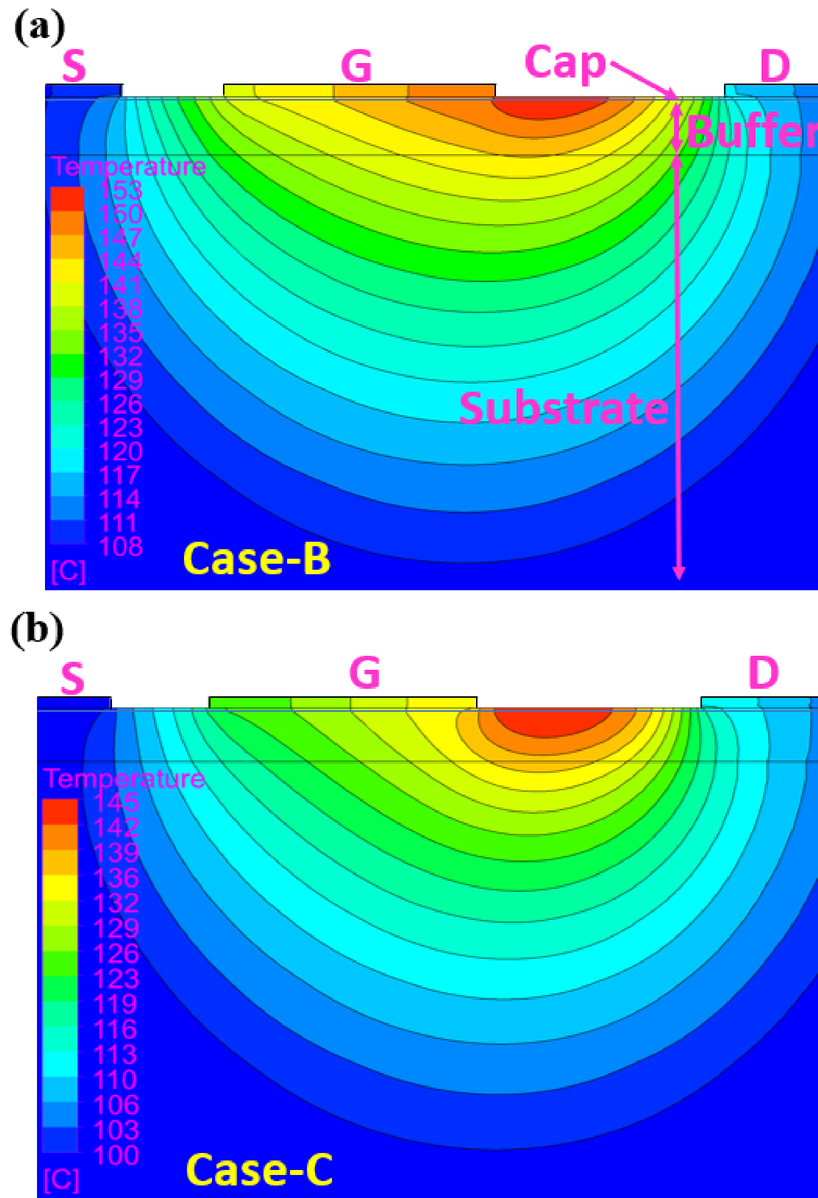


Figure 6.6. Computed temperature profiles for a pulse width of 500 µs and 25% duty cycle (i.e., pulse period is 2 ms) for (a) Case-B: power = 2.04 W/mm (V_{gs} = 2 V; V_{ds} = 13.3 V), and (b) Case-C: power = 1.85 W/mm (V_{gs} = -2 V; V_{ds} = 20 V) at time = 500 µs.

However, Case-C has larger ΔT_{pc} compared to Case-B, even though Case-C has slightly lower power than Case-B. The measurement location (shown in Figure 6.1 (a)) is gate-center, which is same in both the cases. But the hotspot moved away from the gate towards the drain in Case-C. Thus, the hotspot is slightly farther from the measurement

location in Case-C compared to Case-B, as shown in Figure 6.6. Even though power dissipations are comparable, the applied bias conditions in the Case-B and Case-C are different, which leads to different electric field profiles and current flow paths and, in turn, different Joule heat profiles [159]. The Joule heat generation at a location is dot product of electric field current density vectors there. Therefore, the two cases have different Joule heat generation profiles, which leads to different temperature distribution (as shown in Figure 6.6 (a) and (b)) and different ΔT_{pc} in the two cases. This has an important implication as it suggests that the temperature measured at electrodes by thermoreflectance imaging or Raman thermometry may not be necessarily close to peak temperature and dependent on the bias conditions.

6.4 Compact Thermal Modeling

A compact thermal model was developed to predict transient thermal behavior of these devices. The model can be useful when only peak temperature is the quantity of interest and entire temperature distribution is not required. We have calculated the thermal time constants by curve fitting the experimental data using Equations (6.1) and (6.2). Only one or two time constants cannot adequately predict the temperature rise and drop in the device during heating and cooling period. We needed three time constants to describe the temperature rise and another time constant to describe drop in these devices. The equations are-

$$\Delta T_{heat}(t) = (\Delta T_{heat,max}/3) \sum_{i=1}^{3} \left(1 - \exp\left(-{}^{t}/_{\tau_i}\right)\right) \qquad (6.1)$$

$$\Delta T_{cool}(t) = (\Delta T_{cool,max}/3) \sum_{i=1}^{3} \exp\left(-{}^{t}/_{\tau_i}\right) \tag{6.2}$$

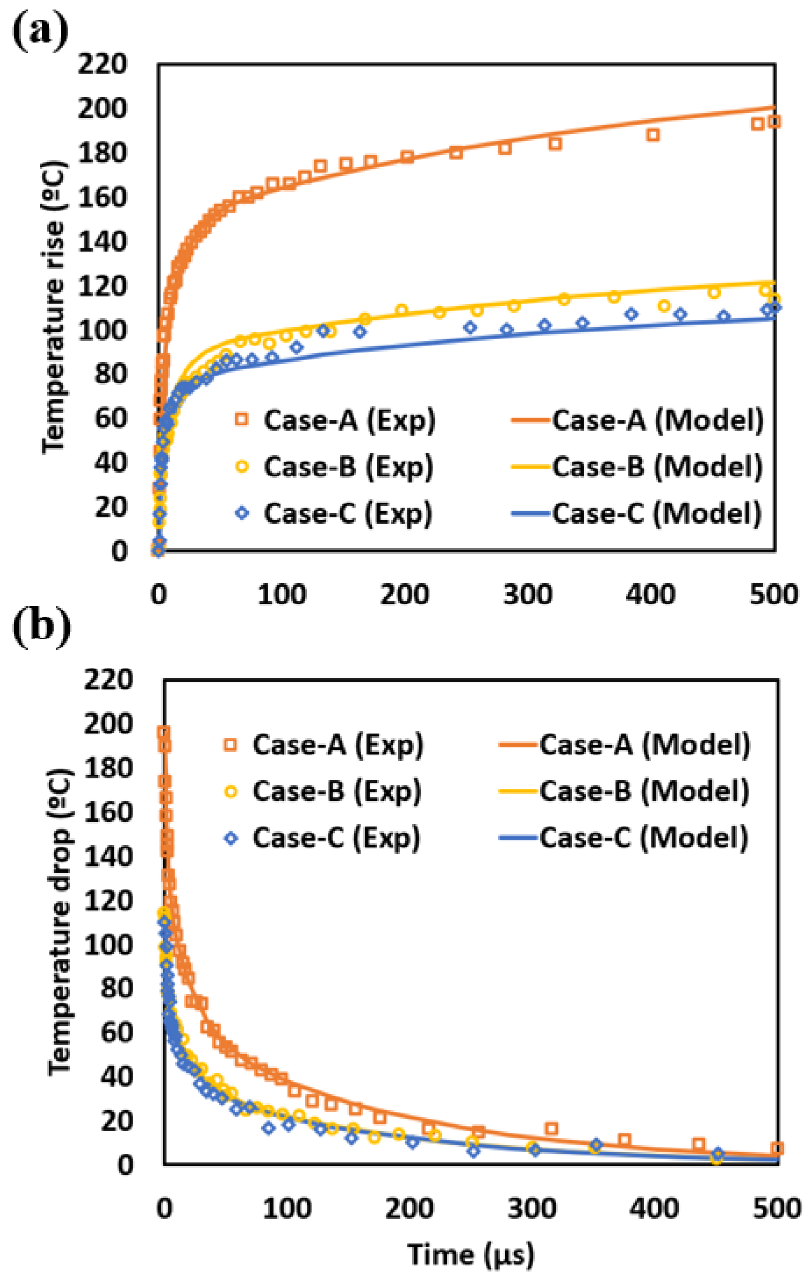


Figure 6.7. Comparison of compact thermal model predictions with the measurements when (a) the device is turned on and temperature rises and (b) the device is turned off and temperature drops for Case-A, Case-B and Case-C.

For Case-A, we calculated τ_1, τ_2 and τ_3 for transient temperature rise to be 2 μs, 15 μs and 400 μs, respectively, and for transient temperature drop to be 2 μs, 20 μs, and 180 μs, respectively. The $\Delta T_{heat,max}$ is the rise in temperature to reach steady-state for the given power at the gate center and computed to be 221.7 ^{o}C from steady-state simulations for Case-A. $\Delta T_{cool,max}$ is the drop in temperature during cooling and measured to be 196 ^{o}C for Case-A. Even though time constants are estimated by fitting for Case-A only, they are also able to predict temperature rise and drop for Case-B and Case-C as shown in Figure 6.7. Therefore, these time constants can predict transient thermal behavior at different power settings and bias conditions. The multiple time constants required for fitting can be attributed to heat spreading in the materials of different thermal diffusivities, which leads to different rate of heat spreading in different directions.

6.5 Device-level Thermal Management

We have investigated two different passive cooling techniques for Ga_2O_3 devices using 3-D thermal model. First, we investigated the effect of various high thermal conductivity substrates, e.g., SiC and diamond. We also accounted for the thermal boundary resistance (TBR) between substrate and Ga_2O_3 buffer layer. The thermal conductivities of the substrates and TBR at the buffer-substrate interfaces are based on the literature and tabulated in Table 6.1. The TBR of Ga_2O_3-AlN interface was not available in the literature, so a value between Ga_2O_3-SiC and Ga_2O_3-diamond TBRs was chosen. Second, we studied the effect of introduction of a passivation layer at the top of device on heat spreading and peak temperature.

Figure 6.8 shows the introduction of passivation layer in the device at the top. Usually, passivation layers are introduced in the devices to improve the electrical characteristics by passivating the charges at the top surface. However, a high thermal conductivity passivation layer can also reduce the device temperature by provide additional paths for heat spreading. AlN has a significantly higher thermal conductivity than other common passivation materials such as Al_2O_3, Si_3N_4, etc. Therefore, we investigated the effects of addition of AlN layer in reducing the peak temperature of the device.

Table 6.1 Thermal conductivities and thermal boundary resistances used in the simulations.

Material	Thermal conductivity (W/mK)	Thermal boundary resistance (m^2K/W)	Reference
SiC	$337*(T/300)^{-2.059}$	-	[160]
AlN	$316*(T/300)^{-1.49}$	-	[161]
Diamond	2169	-	[107]
SiC- Ga_2O_3	-	7.14×10^{-9}	[105]
AlN- Ga_2O_3	-	6.67×10^{-9}	[105, 107]
Diamond- Ga_2O_3	-	5.59×10^{-9}	[107]

Table 6.2 presents the peak temperature of the devices with different thermal management solutions. The peak temperatures shown in Table 6.2 corresponds to Case-A, where total power dissipation was 3.25 W/mm at V_{gs} = 2 V and V_{ds}= 20 V. We can make a few observations regarding the effectiveness of the different thermal management strategies from Table 6.2. The rise in peak temperature for the baseline case, when semi-insulating Ga_2O_3 was used as substrate and no passivation layer was added, is 243 ºC. It was observed that replacing semi-insulating Ga_2O_3 substrate with a high thermal

conductivity substrate such as SiC and diamond, reduces the rise in peak temperature of the device to 34.2 ºC and 21.2 ºC, respectively. The other cooling technique where a layer of AlN was deposited at the top is also an effective strategy. Thickness of the passivation layer has significant effect on temperature rise. We observed that a passivation layer of 10 μm can reduce the rise in the peak temperature from 243 ºC to 54ºC. Thus, both thermal management techniques are effective in significant reduction of the peak temperature and can be implemented in future device structures to address the thermal management issues.

Table 6.2 Comparison of various thermal management techniques.

Thermal management technique	Rise in peak temperature (ºC)
None (Baseline)	243
SiC substrate	34.2
Diamond substrate	21.2
1 μm AlN passivation layer	137.3
10 μm AlN passivation layer	54

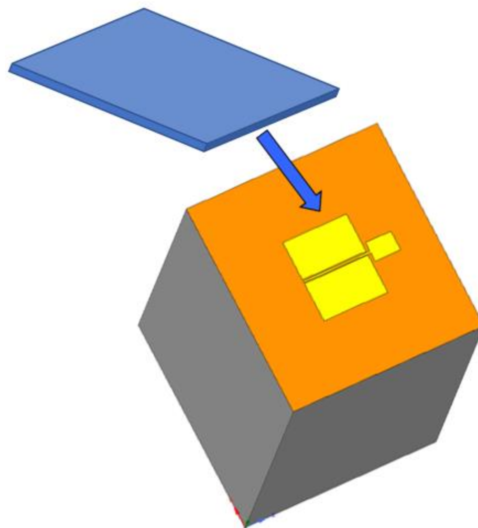


Figure 6.8. Introduction of passivation layer at the top of the device.

6.6 Closure

In summary, thermoreflectance imaging technique has been used to measure steady-state and transient temperature profile of the β-Ga_2O_3 delta-doped MESFET. To the best of our knowledge, the transient measurements of β-Ga_2O_3 FETs were reported for the time. We have developed a 3-D diffusive thermal model for these devices. 3-D steady-state and transient thermal simulations were used to compare with thermal measurements and predict the temperature variation inside the device. The difference in overall peak temperature inside the device and the measured temperature at the gate pad is observed to be dependent on bias conditions even at similar powers. A compact thermal model was developed, and the thermal time constants of the device were estimated to predict the transient thermal behavior of the device. We studied two different cooling techniques for these devices—(1) introduction of a high thermal conductivity substrate and (2) introduction of a passivation layer at the top. Both techniques appears to be effective in reducing device peak temperature.

CHAPTER 7. NON-GRAY THERMAL TRANSPORT IN BETA-GALLIUM OXIDE FILMS AND MESFETS

In this chapter, phonon transport in β-Ga_2O_3 thin films and MESFETs are investigated using non-gray Boltzmann Transport Equations (BTE). The results from this work will help in understanding the mechanism of phonon transport in the β-Ga_2O_3 thin films and MESFETs. First, the effect of film thickness on the β-Ga_2O_3 thermal conductivity is investigated at room temperature. Next, the effect of domain size and the energy transferred to various phonon modes on the temperature distribution in the domain is studied. The difference in the hotspot temperatures predicted using Fourier's law and non-gray BTE are compared for three different domain sizes. The role of distribution of energy transfer to various phonon modes and domain size on the thermal transport and temperature profile is investigated. Finally, thermal transport in β-Ga_2O_3 MESFET integrated with a high thermal conductivity diamond substrate is studied. The ballistic-diffusive thermal transport and its dependence on the β-Ga_2O_3 layer thickness is studied. The error in the temperature prediction using Fourier's law in these devices is calculated for three β-Ga_2O_3 layer thicknesses. The importance of solving non-gray phonon BTE model in β-Ga_2O_3 layer to predict accurate temperature profile in these devices is highlighted.

7.1 Modeling Approach

7.1.1 Non-gray Phonon BTE Simulations

Non-gray Phonon BTE with SMRTA is solved to predict the thermal conductivity along (100) and (010) directions in β-Ga_2O_3 and predict steady-state spatial temperature

distribution in β-Ga_2O_3 MESFETs. In non-gray BTE, all the phonon modes in the wave-vector space and their interactions are considered. Each phonon mode has corresponding relaxation time (τ) , group velocity (v_g) and frequency (ω). On the contrary, gray BTE is solved using a single τ, v_g and ω. Thus, it cannot account for phonon interactions and energy re-distributions. The phonon properties for non-gray BTE such as τ, v_g and ω for β-Ga_2O_3, are obtained from Density Function Theory (DFT) calculations performed in [33]. The steady-state BTE, discretized using finite volume method (FVM) in both physical and wave-vector space, is defined in Chapter-3 by Equations (3.1) and (3.2). The COMET algorithm developed by Loy et al. [119, 129] is used to solve BTE. The algorithm has already been discussed in Chapter-3 and the flow chart is shown in Figure 3.6.

7.1.2 Multiscale Electrothermal Simulations

The size of β-Ga_2O_3 MESFETs can be significantly larger as substrate thickness are typically of the order of a few hundreds of microns. Therefore, it is impractical and computationally very expensive to solve the phonon BTE in the entire MESFET. The Joule heating occurs only in the semiconducting β-Ga_2O_3 layer in the MESFETs. It is known that the complex electron-phonon scattering mechanisms occur near Joule heating zone only. The thermal transport becomes diffusive away from the heat source. Therefore, the BTE needs to be solved only in the semiconducting β-Ga_2O_3 layer, where heat generation occurs. Fourier's law should be applicable away from the heat source in the substrate, where thermal transport is diffusive. The two models are coupled together to predict temperature distribution in the entire device.

7.2 Effect of Film Thickness on Thermal Conductivity

The non-gray phonon BTE is employed to estimate the effect of film thickness on thermal conductivity of β-Ga_2O_3. A schematic of the β-Ga_2O_3 film is shown in Figure 7.1. The thermal conductivity is measured at room temperature. Therefore, 305 K and 295 K are applied at left and right edge of the film. The top and the bottom edge are insulated, where the specular reflection boundary condition is applied to simulate infinite thickness in vertical (y-axis) direction. The thermal conductivity is computed in two crystal direction—(100) and (010). These two directions are perpendicular to each other in the

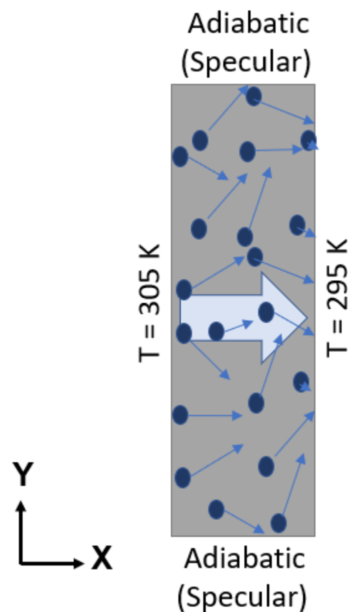


Figure 7.1. A schematic of thin film with the applied boundary conditions.

crystal. The MESFETs studied in the Chapter-5 and 6 are grown along (010) crystal direction and (100) is in transverse plane in these devices. Even though β-Ga_2O_3 has anisotropic thermal conductivity, it can be approximated to be bi-directional because conductivity in all directions in the plane perpendicular to (010) are very close [32].

Therefore, (100) direction is considered to be representative of all these directions. The conductivity in each crystal direction is calculated by aligning that direction along x-axis and the other direction along y-axis in the simulations. In addition, the effect of point defects on the thermal transport in β-Ga_2O_3 has also been investigated. We have considered two different types of β-Ga_2O_3 samples (1) β-Ga_2O_3 with no defects and (2) β-Ga_2O_3 with 2% Ga vacancies. In the latter sample, 2% Ga vacancies in the crystal will introduce additional phonon scattering. The additional scattering has been accounted for in the simulations as described in [33].

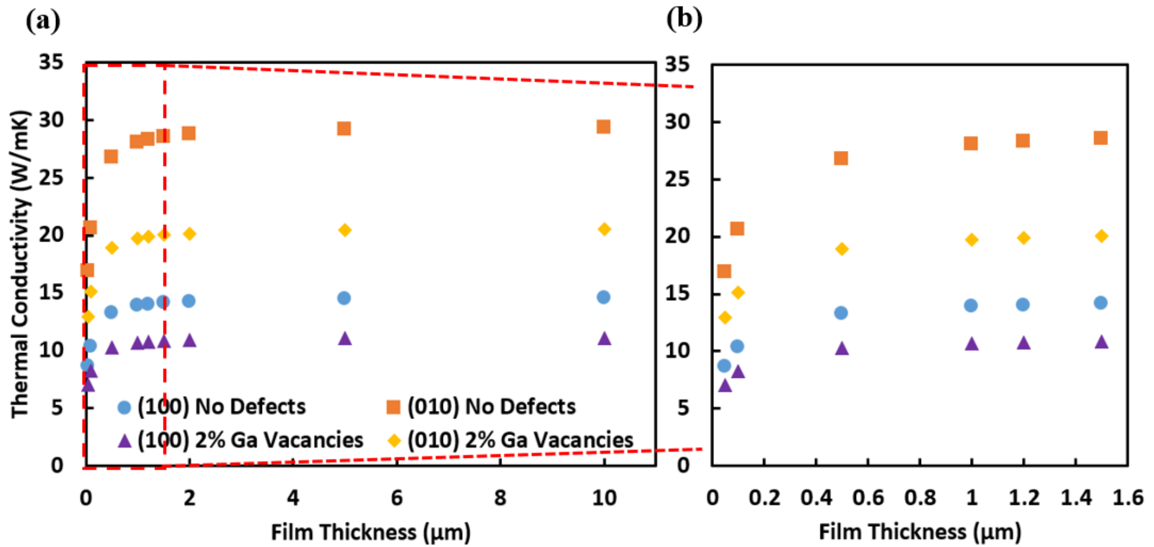


Figure 7.2. (a) Effect of film thickness on the thermal conductivity of *β*-Ga_2O_3 with no defects and *β*-Ga_2O_3 with 2% Ga vacancies along (100) and (010) directions. (b) A close-up view of Figure 7.2 (a) .

Figure 7.2 shows effect of film thickness on thermal conductivity of β-Ga_2O_3 with no defects and β-Ga_2O_3 with 2% Ga vacancies along (100) and (010) directions. It can be observed that thermal conductivity increases as the film thickness increases and asymptotically approaches the bulk conductivity for both the samples and crystal

directions. The thermal conductivity along (010) is much higher than (100) direction for both the samples as shown in Figure 7.2.The thermal conductivity of the β-Ga_2O_3 with no defects is higher than the β-Ga_2O_3 with 2% Ga vacancies along both the directions because the scattering due to Ga vacancies suppresses the thermal conductivity. The bulk thermal conductivity predicted in this study of no defect sample is in good agreement with the experimentally measured bulk values in both the crystal directions as shown in Table 7.1. The measured thermal conductivities are slightly lower than the predictions from the simulations for samples without any defects, which can be attributed to the presence of defects or impurities in the samples used for the measurements. Most of the experimental studies do not report the % of vacancies or dislocations in the samples, which makes direct comparison difficult.

Table 7.1 Comparison of bulk thermal conductivity predicted in this study with the measured values in the literature.

Crystal direction	Experiments (W/mK)	This study (No defects) (W/mK)	This study (2% Ga vacancies) (W/mK)
100	10.9 ±1 [32]; 13±1 [162]	14.5	11.1
010	27±2 [32]; 29.21 [96]	29.2	20.5

Thin film conductivity is less than bulk conductivity because some of the phonon modes with mean free paths larger than film thickness have their contribution to conductivity restricted. In other words, the mean free paths of these modes is reduced to film thickness and, therefore, thermal conductivity is reduced. The largest phonon mean free path for β-Ga_2O_3 is around 0.5 µm. The initial sharp change in thermal conductivity up to 0.5 µm is due to significant ballistic transport in the films with thickness less than 0.5 µm. Beyond 0.5 µm thickness, thermal conductivity gradually approaches the bulk value.

7.3 Temperature distribution in β-Ga_2O_3 with Joule Heating

Next, we investigate the effect of β-Ga_2O_3 domain size and phonon-phonon energy transfer on thermal transport near heat source using non-gray BTE model. We compared the temperature distribution obtained from Fourier's law and non-gray BTE simulations. In semiconductor devices, high electric field leads to hot carriers (hole or electrons) that

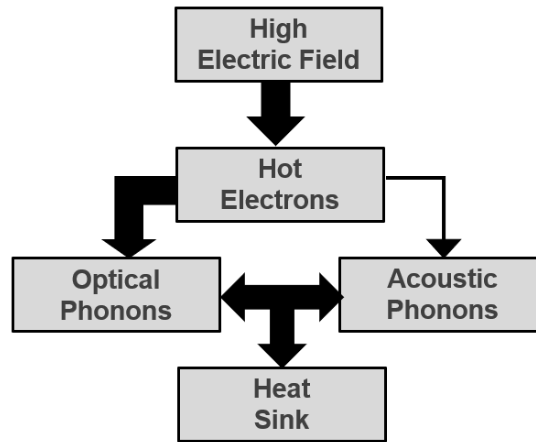


Figure 7.3. Energy exchange pathway for semiconductors during Joule heating.

have attained very high kinetic energy. These hot carriers interacts with lattice and transfer energy to phonons. Almost entire energy is transferred to optical phonons during these interactions [99, 163]. Therefore, there may be a non-equilibrium in the temperatures of different phonon modes near heat source, where these electron and phonon interactions takes place. These optical phonons then interacts with acoustic phonons and the energy is conducted to the heat sink primarily by these phonons. Figure 7.3 depicts a typical energy exchange pathway in semiconductor devices in case of Joule heating. In addition to complex phonon interactions, size of the domain can also affect the thermal transport. We have already observed in the last section that thermal conductivity is affected by the film thickness.

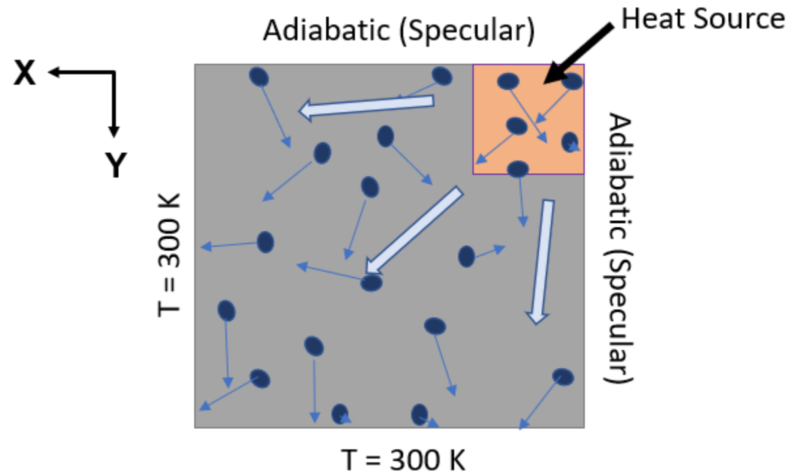


Figure 7.4. A schematic of β-Ga_2O_3 domain, heat source and the applied boundary conditions.

A β-Ga_2O_3 domain with a heat source and applied boundary conditions is chosen as shown in Figure 7.4. The top and right edge are insulated where specular reflection boundary condition is applied. The bottom and left edge are applied with isothermal boundary condition and temperature is set at 300 K. A heat source of size 0.1 μm x 0.1 μm was chosen. In β-Ga_2O_3, the electron-phonon scattering is dominated by high frequency optical phonons. Optical phonons near Γ-point in Brillouin zone and with frequency of 235 cm^{-1} (29 meV) or greater are determined to be strongly coupled with electrons [164]. Since, the exact distribution of hot electron energy to all the optical phonon modes is not available in the literature. Therefore, in the first case (referred as NG BTE-20), Joule heat is equally distributed in the top 20 phonon modes with largest frequency out of total 30 modes at the nearest k-points to Γ-point in each direction. These 20 modes are all optical modes and have frequency greater than or equal to ~ 235 cm^{-1} . In second case (referred as NG BTE-1), we applied heat source to the mode with highest frequency near Γ-point. In third case, (referred as NG BTE-30), we applied heat source to all the 30 modes equally near Γ-point.

Initially, a non-gray BTE domain of size 1.1 μm x 1.1 μm was chosen as size effects are expected to be small. Table 7.2 shows comparison between peak temperature predicted using Fourier's law and non-gray BTE models. First, if we compare the three cases of non-gray BTE model, where heat source is applied to different modes, there is negligible difference in the peak temperature predicted by them. Especially, when heat source is applied only to optical modes (NG BTE-20 and NG BTE-1), the temperatures are same. However, when the heat source is applied to all the modes including acoustic modes (NG BTE-30), there is a drop of 2 K in peak temperature compared to NG BTE-20 and NG BTE-1. This trend was expected because acoustic mode have longer mean free paths than optical modes. From these three cases, we can conclude that distribution of energy transfer to various phonon modes and phonon-phonon energy exchange do not play any significant role in the temperature prediction.

Table 7.2 Comparison of peak temperatures depending upon model employed. The error is calculated with respect to NG BTE-20 model.

Model	Description	Peak temperature (K)	% Error
NG BTE-30	Heat source is applied to all 30 modes equally	587.05	0.9
NG BTE-20	Heat source is applied to top 20 modes equally	589.67	-
NG BTE-1	Heat source is applied to 30th mode only	589.65	<0.01
Fourier-bulk	Conductivity is chosen from 5 μm film	578.21	3.96
Fourier-1	Conductivity is chosen from 1 μm film	587.23	0.84

Next, we calculated peak temperature using Fourier's law with two different thermal conductivities. In the first case (referred as Fourier-bulk), we use thermal conductivity corresponding to 5 µm film, where bulk conductivity has been recovered and there are negligible ballistic transport effects. In second case (referred as Fourier-1), we use thermal conductivity corresponding to 1 µm film. We can observe from Figure 7.2 that there is difference between peak temperatures predicted using Fourier-bulk and Fourier-1 due to some ballistic thermal transport in Fourier-1 but it is small (<4%). However, the thermal transport in domains larger than 1 µm is primarily diffusive. In addition, if we compare the peak temperature predicted using Fourier's law models and non-gray models, we observe that the difference is not significant. Therefore, ballistic effects due to the size of the domain, when domain size is around 1 µm or larger, are not important in prediction of temperature field. Retrospectively, it could have been also anticipated from thin film thickness versus conductivity trend of Figure 7.2 as conductivity nearly attains bulk conductivity value for film thickness of 1 µm or larger, given that non-equilibrium effects do not affect the peak temperature.

Table 7.3 Comparison of peak temperatures predicted using Fourier's law and non-gray BTE for different domain size.

Domain size	Peak temperature (K) using Fourier-bulk	Peak temperature (K) using NG BTE-20	% Error in peak temperature
1.1 µm x 1.1 µm	578.21	589.67	3.96
0.6 µm x 0.6 µm	506.38	522.42	7.21
0.2 µm x 0.2 µm	392.71	415.67	19.85

However, as the domain size is reduced below 1 µm, the ballistic effects starts playing bigger role in the thermal transport and Fourier's law will not give accurate results.

Three different domain sizes— 0.2 μm x 0.2 μm, 0.6 μm x 0.6 μm and 1.1 μm x 1.1 μm— of β-Ga_2O_3 were chosen. As the domain size is decreased from 1.1 μm x 1.1 μm to 0.6 μm x 0.6 μm and then to 0.2 μm x 0.2 μm, we observed that Fourier's law starts underpredicting the peak temperature as ballistic transport of phonons becomes important. Table 7.3 compares the peak temperatures predicted using Fourier-bulk and NG BTE-20. Fourier-bulk does not account for size of the domain because bulk thermal conductivity is used for all three domains with different sizes. On the other hand, non-gray BTE model accounts for size effects. The phonons with mean free path larger than domain size travel ballistically and scatter at the boundary. Thus, the effective thermal conductivity of the domain is reduced in non-gray BTE model, as discussed in section 7.2, and peak temperature predicted by non-gray BTE model is higher than that by Fourier model.

7.4 Multiscale Modeling of β-Ga_2O_3 FETs

Finally, we investigate if phonon ballistic transport play a role in heat dissipation in β-Ga_2O_3 devices. Diamond is a promising candidate for substrate material in β-Ga_2O_3 devices due to its high thermal conductivity. However, β-Ga_2O_3 and diamond heterointerface can be source of phonon scattering, which can affect the efficient heat dissipation from the hotspot. A β-Ga_2O_3 device grown on high conductivity diamond substrate is studied using a coupled BTE-Fourier model. We investigate the effect of thickness of semiconducting β-Ga_2O_3 layer on ballistic diffusive transport near the hotspot in the device.

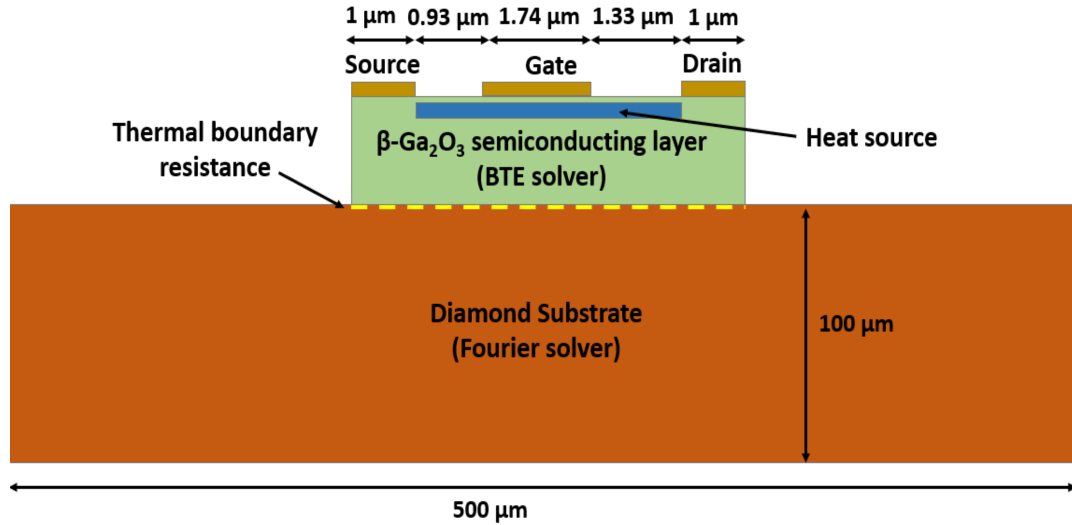


Figure 7.5. Schematic of a *β*-Ga_2O_3 FET on diamond substrate.

A typical *β*-Ga_2O_3-on-diamond device structure is considered in this study. A schematic of the device is shown in Figure 7.5, where all the relevant dimensions are shown. A silicon delta-doping layer acts as a channel and most of the Joule heating occurs in this channel when the device is on. Electrothermal device modeling was performed using TCAD Sentaurus to obtain the Joule heat generation profile of the device at Vds = 10 V, Vgs = 2 V and power ~ 2 W/mm. This profile is given as input in non-gray BTE and Fourier model simulations. The size of the device is large, so solving non-gray BTE model in the entire domain is impracticable. In addition, given the size of substrate, the thermal transport will be diffusive in it. Therefore, Fourier's law can be used in the substrate to study thermal transport. On the other hand, the *β*-Ga_2O_3 layer thickness is significantly smaller than the substrate, so ballistic transport may occur. Therefore, non-gray BTE model is used in the *β*-Ga_2O_3 layer. The diffuse scattering is assumed at the *β*-Ga_2O_3-diamond interface and the thermal boundary resistance is considered to be 5.59 x 10^{-9} m^2W/K [107]. Specular reflection boundary condition is assumed at the remaining surfaces

of the β-Ga_2O_3 layer (BTE domain). The bottom of the substrate is set to 300 K and other vertical surfaces are considered to be adiabatic in Fourier model. The thermal conductivity of the diamond is considered to be 2169 W/mK [107] for Fourier model.

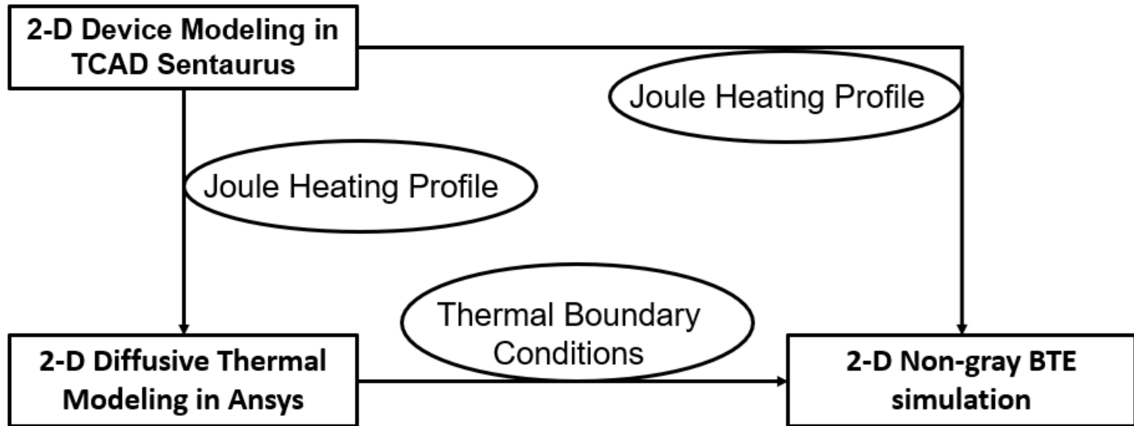


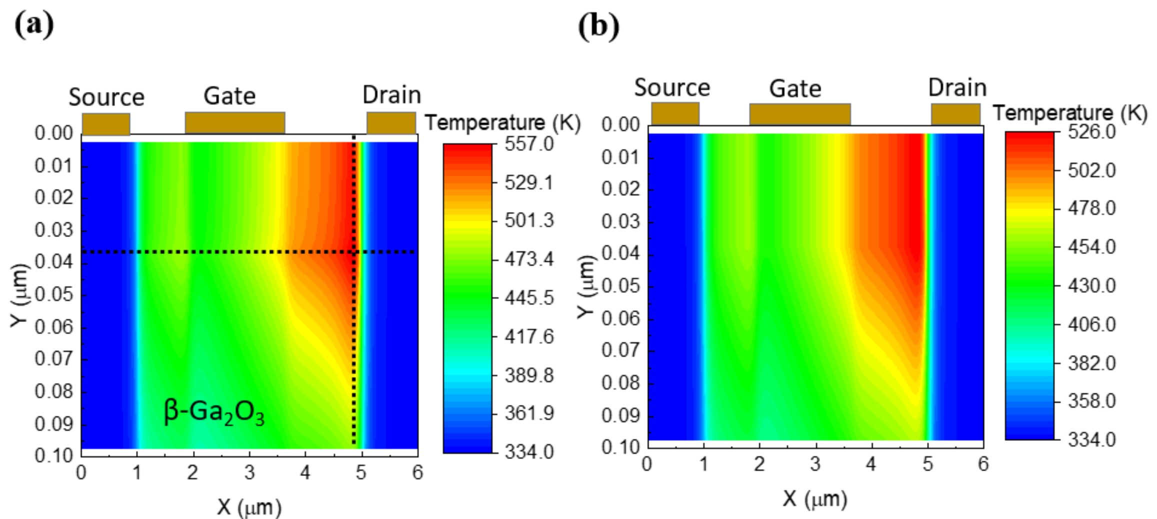
Figure 7.6. A flowchart of the procedure of multiscale modeling. Non-gray BTE model is used for β-Ga_2O_3 layer and Fourier model is used for diamond substrate.

Figure 7.6 presents a flowchart of the procedure to run non-gray BTE in β-Ga_2O_3 layer and Fourier model in diamond substrate. First, Fourier model is run in the entire device with Joule heat generation profile obtained from TCAD Sentaurus as an input. The thickness and temperature dependence thermal conductivity of β-Ga_2O_3 layer is considered as well in this simulation. It provides the temperature distribution in the substrate and at the β-Ga_2O_3-diamond interface. The interface temperature is applied as a boundary condition and Joule heat generation profile obtained from TCAD Sentaurus as an input to the non-gray BTE simulations (NG BTE-20 case from section 7.3) and the temperature field is obtained. In addition, Fourier model is also solved in the entire domain with temperature dependent bulk thermal conductivity of β-Ga_2O_3 (Fourier-bulk case from

section 7.3) . Thus, this model does not account for β-Ga_2O_3 layer thickness effects and is purely diffusive.

Three different device structures with thicknesses of β-Ga_2O_3 layer— 0.1 μm (Device-1), 0.5 μm (Device-2) and 1 μm (Device-3), are studied. These devices are operated at various power settings, which are applied by scaling the TCAD Sentaurus Joule heat profile obtained at Vds = 10 V and Vgs = 2 V to match the desired power setting. Figure 7.7 (a-e) shows comparison between the temperature field obtained using non-gray BTE and Fourier model for Device-1 at power dissipation = 61.16 W/mm. We can observe that even though temperature profiles predicted using the two models are qualitatively similar, there is quantitative difference between the two profiles. The Fourier model underpredicts the temperature as it cannot account for ballistic phonon transport.

Table 7.4 compares the peak temperature obtained using non-gray BTE and Fourier coupled model against Fourier model for different power settings and device structures with different β-Ga_2O_3 layer thickness. Figure 7.8 shows error in the Fourier



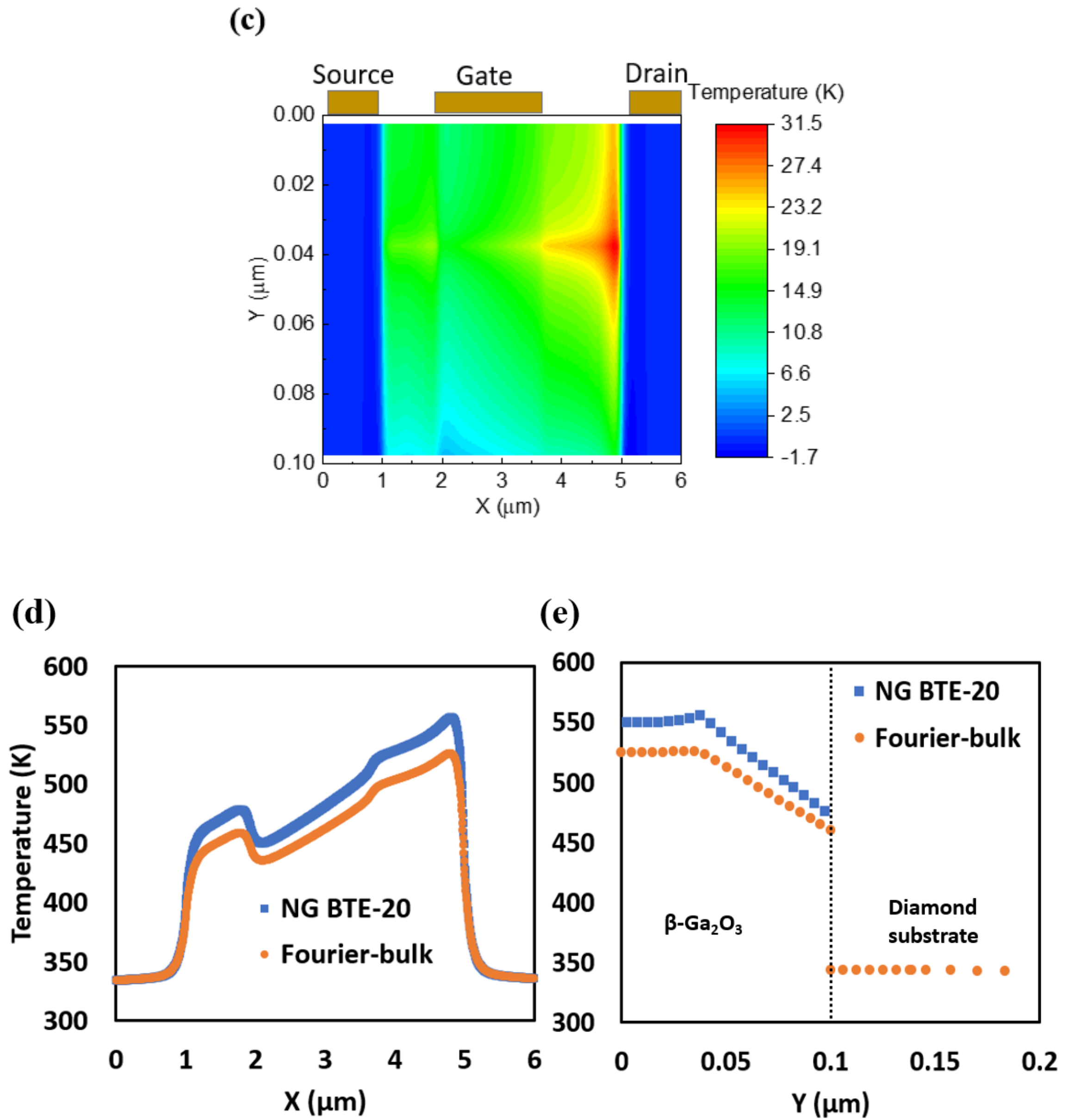


Figure 7.7. Temperature field predicted (a) using non-gray BTE (NG BTE-20) and Fourier coupled model, and (b) using Fourier model only. (c) Contour plot of the temperature difference predicted from the NG BTE-20 and Fourier model ($T_{BTE} - T_{FOURIER}$). (d) Comparison of temperature profiles predicted using non-gray BTE (NG BTE-20) and Fourier model along the horizontal dotted line (Y ~ 0.0375 µm) and (e) the vertical dotted line (X ~ 4.81 µm)

Table 7.4 Comparison of peak temperatures predicted using Fourier-bulk model in Ansys and coupled BTE-Fourier model for different device thickness.

Device thickness (μm)	Power (W/mm)	Peak temperature (K) using NG BTE-20 and Fourier coupled	Peak temperature (K) using Fourier model only	Error in peak temperature
0.1	20.39	381	370.33	10.67
0.1	40.77	466.6	445.85	20.75
0.1	61.16	556.15	525.97	30.18
0.5	10.19	384.85	379.05	5.8
0.5	20.39	482.39	471.82	10.57
0.5	30.58	592.52	578.12	14.4
1	10.19	437.42	432.66	4.76
1	20.39	607.6	602.84	4.76

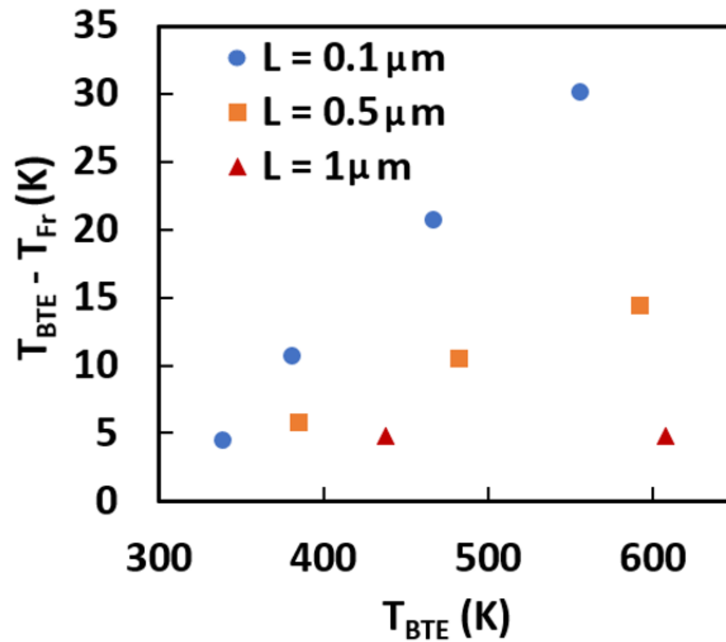


Figure 7.8. Error in the Fourier predicted peak temperature as a function of Non-gray BTE predicted peak temperature.

predicted peak temperature as a function of non-gray BTE predicted peak temperature for different film thicknesses. It is evident from Table 7.4 and Figure 7.8 that error in peak temperature predicted using Fourier's law increases as the layer thickness decreases. Because Fourier model does not consider the ballistic phonon transport effects, these effects become more prominent as the layer thickness decreases as we discussed in section 7.2. For layer thickness around 1 µm, the Fourier model can predict the temperature field with reasonable accuracy. It implies the ballistic transport is no longer significant and diffusive transport dominates for film thickness around 1 µm and greater.

7.5 Closure

In summary, non-gray Boltzmann Transport Equations (BTE) is used to study phonon transport in β-Ga_2O_3 thin films and MESFETs. First, 1-D thermal transport in β-Ga_2O_3 thin films is studied and the film thickness dependence of the β-Ga_2O_3 thermal conductivity is determined at room temperature. The thickness dependence of the thermal conductivity in thin films is attributed to the ballistic phonon transport. As the film thickness increases from 50 nm to 10 µm, the thermal conductivity also increases in both crystal directions—(100) and (010), and gradually approaches the bulk thermal conductivity value as film thickness increases beyond 1 µm. Next, thermal transport in a 2-D domain with a heat source is studied using non-gray BTE. The effect of complex phonon-phonon energy exchange and domain size on the peak temperature is studied. The peak temperatures predicted using non-gray BTE models where heat source is applied in different phonon modes and Fourier model are compared for different domain sizes. It is observed that distribution of energy transfer from electrons to different phonon modes does not lead to any significant error in the temperature prediction using the Fourier's law.

However, Fourier's law does not account for ballistic transport, so for domain with characteristics length smaller than 1 μm, Fourier's law may not accurately predict the temperature distribution. Finally, thermal transport in β-Ga_2O_3-on-diamond MESFETs at various power dissipation settings is studied using coupled non-gray BTE and Fourier model. The Fourier model alone cannot predict the temperature distribution accurately when the thickness of β-Ga_2O_3 layer is less than 1 μm. The thermal transport will be ballistic-diffusive in β-Ga_2O_3 layer. Therefore, non-gray phonon BTE should be solved in the thin β-Ga_2O_3 region of the device for accurate temperature predictions.

CHAPTER 8. SUMMARY AND FUTUTRE WORK

In this work, transport characteristics of CNT network based and β-Ga_2O_3 FETs are investigated. The extraordinary electrical, thermal, and mechanical properties of CNTs make them a promising candidate for future low-cost and high-performance devices. Random CNT network-based FETs have great potential to replace amorphous silicon, polysilicon, and organic FETs in flexible and transparent electronics. On the other hand, the ultra-wide bandgap of β-Ga_2O_3 allows its devices to achieve higher breakdown voltage, operating temperature and switching frequency. These properties give it significant advantage for power and RF electronics applications. However, low thermal conductivity of β-Ga_2O_3 poses significant challenges for developing thermal management solutions of these devices. The efficient heat removal is necessary for higher efficiency, reliability, and longer lifetime of these devices.

8.1 Summary of Contribution

8.1.1 Electrical Transport in Random CNT Network-based FETs and Application in Cryptography

Electrical transport in random CNT network-based FETs is investigated using a drift-diffusion model, which was solved using numerical simulations to predict current and potential distribution in CNT FETs. The device-to-device variation in electrical characteristic due to randomness in the network was exploited to propose a novel application of these devices in cryptography. It was shown that single-gate transistors with CNT density close to percolation threshold density can be used to generate binary keys.

Then a multi-gated CNT FET design was proposed to increase the entropy per device. It was shown that CNT FETs with four-gates can produce three different current levels, which are separate enough to avoid any bit error due to external factors such as supply voltage, temperature, etc. Thus, ternary keys can be generated using this design. In addition, each FET has six different challenge-response pairs. These six challenge-response pairs in conjunction with three current levels are used to generate base-17 (hepta-decimal) keys. A significant higher level of randomness and entropy was achieved using the multi-gated design compared to existing PUFs, which could generate only binary or ternary keys.

8.1.2 *Multiscale Electrothermal Modeling and Characterization of β-Ga_2O_3 FETs*

Electro-thermal characteristics of β-Ga_2O_3 based FETs were investigated using measurements and numerical simulations. A 2-D electrothermal model of β-Ga_2O_3 MESFETs was developed using TCAD Sentaurus. The thermodynamic carrier transport device model was chosen, and temperature and electric field-dependence of electron mobility model is incorporated in the model. The I –V characteristics predicted using the model are in good agreement with the measured I – V characteristics. The model could predict electric field, current density, volumetric heat generation profile, and peak temperature at various device operating conditions. The peak temperature is observed to be significantly different at the same power dissipation but different bias conditions. This difference is attributed to the change in the electron Joule heating profile with the applied bias voltage. This study underlined the importance of the knowledge of Joule heat generation profile in accurate prediction of temperature field in the device. Then, the effects of the location of the delta doping layer, the gate–drain spacing, and the source–drain

spacing are investigated to guide a future device fabrication. The variation in these parameters mainly affects electrical characteristics such as ON-resistance, saturation current, threshold voltage, and so on. The thermal characteristics, such as peak temperature, temperature profile, and so on, are not significantly affected at a low-power dissipation.

2-D models cannot account for heat dissipation in the third dimension. Therefore, a 3-D diffusive thermal transport model was developed in Ansys Fluent to predict accurate temperature distribution. The model was validated against thermal measurements. Microsanj thermo-reflectance imaging was performed for steady-state and transient thermal measurements. We demonstrated that maximum temperature measured at the gate is lower than the overall peak temperature, which is located inside the device in delta-doping layer near the gate-edge of the drain side. To the best of our knowledge, it was first study on transient thermal measurements of β-Ga_2O_3 FETs. A compact thermal model was developed to predict the peak temperature in the device as a function of time. Thermal time constants for device heating and cooling process are estimated to study thermal transient behavior of the device. Two device level thermal management techniques—replacement of Iron-doped β-Ga_2O_3 substrate with a high thermal conductivity substrate and deposition of a passivation layer— were studied and both the techniques could help in efficient thermal management of the device.

Steady non-gray BTE with SMRTA is used to study phonon transport in β-Ga_2O_3 thin film and FETs. The COMET method was used to solve the BTE as it is shown be significantly faster than conventional sequential method. The dependence of thermal conductivity on β-Ga_2O_3 film thickness is predicted. The thermal conductivity increases as the film thickness increases steeply up to around 1 μm and then it asymptotically

approached the bulk thermal conductivity value. The thickness dependence of the thermal conductivity in thin films is attributed to the ballistic phonon transport. Next, the effects of distribution of heat inputs to phonon modes and domain size on the peak temperature are investigated in a 2-D domain with a heat source using non-gray BTE. Finally, phonon transport in β-Ga_2O_3 MESFETs on diamond substrate near hotspot is investigated using coupled non-gray BTE and Fourier model. The ballistic effect needs to be considered for devices with β-Ga_2O_3 layer thickness less than 1 μm. The Fourier model alone may not give accurate temperature distribution and non-gray phonon BTE model should be used near hotspot in the thin β-Ga_2O_3 layer.

8.2 Future Work

Some of the topics that relevant to present thesis and open to research in future are discussed below.

8.2.1 Further Enhancement in the Randomness and Fabrication of Multigated CNTFET based PUFs

In present work, a 4-gate design of CNT FET was proposed to increase the entropy per PUF instance. However, it can be explored if the entropy per device could further be increased. There are two possible ways. Either the number of response types (current levels) or number of challenges per device could be increased. One possible way to increase the number challenges is to increase the number of gates in the device. Another possible way to increase challenges or response type is by changing the shape and size of the gate regions. The randomness would be maximum when all the response types are equally probable for a given challenge. The current design has bias towards some of the response

types. This bias can be reduced by changing the shape and size of the different gate regions. In addition, the fabrication of these CNT FETs is another important step in implementation of this design in real world. The challenges associated with the fabrication process and how those challenges could be addressed is another important area of research.

8.2.2 Two-way Coupling between TCAD Sentaurus Electrothermal Model and Non-gray BTE Model

The Joule heating profile obtained from the TCAD Sentaurus electrothermal modeling was given as an input to non-gray BTE model to estimate the temperature distribution in the device. However, the temperature distribution obtained from the non-gray BTE model can affect the Joule heating profile predicted by the TCAD model. So, feeding back the temperature profile obtained from the non-gray BTE model may improve the accuracy of the TCAD model. This two-way coupling between TCAD Sentaurus and non-gray BTE model need to be performed to check the accuracy of one-way coupled model in future.

8.2.3 Determination of Maximum Allowable Temperature for Ga_2O_3 FETs

There are a few more studies, which can help in further improving the understanding of thermal characteristics of these devices. Temperature induced catastrophic failure has been observed in these devices at higher temperatures [92] . However, there is no study on determining the maximum allowable temperature and its effect on the operation/reliability of these devices.

8.2.4 Electrothermal Characterization of Ga_2O_3 Vertical FETs

Most of the Ga_2O_3 FETs demonstrated in the past have been lateral structures. However, as per past literature, vertical FET structures may have an advantage over lateral structures for high voltage and high-power application [26]. Recently, a few vertical devices have been demonstrated as discussed in chapter 2. However, there is very few studies on electrothermal modeling and measurements of these structures. It is important to understand the electrothermal characteristics of these devices at various operating conditions for improving future designs and achieve maximum potential of the material. Since, vertical structures are more suitable for high power application, thermal management techniques for these devices should also be studied.

REFERENCES

1. Eatemadi, A., et al., *Carbon nanotubes: properties, synthesis, purification, and medical applications.* Nanoscale Research Letters, 2014. **9**(1): p. 393.

2. Pop, E., et al., *Thermal Conductance of an Individual Single-Wall Carbon Nanotube above Room Temperature.* Nano Letters, 2006. **6**(1): p. 96-100.

3. Kim, P., et al., *Thermal Transport Measurements of Individual Multiwalled Nanotubes.* Physical Review Letters, 2001. **87**(21): p. 215502.

4. De Volder, M.F.L., et al., *Carbon Nanotubes: Present and Future Commercial Applications.* Science, 2013. **339**(6119): p. 535.

5. Dürkop, T., et al., *Extraordinary Mobility in Semiconducting Carbon Nanotubes.* Nano Letters, 2004. **4**(1): p. 35-39.

6. Zhang, Y., Y. Bai, and B. Yan, *Functionalized carbon nanotubes for potential medicinal applications.* Drug Discovery Today, 2010. **15**(11): p. 428-435.

7. Tans, S.J., A.R.M. Verschueren, and C. Dekker, *Room-temperature transistor based on a single carbon nanotube.* Nature, 1998. **393**(6680): p. 49-52.

8. Franklin, A.D., et al., *Sub-10 nm Carbon Nanotube Transistor.* Nano Letters, 2012. **12**(2): p. 758-762.

9. Cao, Q. and J.A. Rogers, *Ultrathin Films of Single-Walled Carbon Nanotubes for Electronics and Sensors: A Review of Fundamental and Applied Aspects.* Advanced Materials, 2009. **21**(1): p. 29-53.

10. Wang, C., et al., *Extremely Bendable, High-Performance Integrated Circuits Using Semiconducting Carbon Nanotube Networks for Digital, Analog, and Radio-Frequency Applications.* Nano Letters, 2012. **12**(3): p. 1527-1533.

11. Chen, J., et al., *Thin dielectric-layer-enabled low-voltage operation of fully printed flexible carbon nanotube thin-film transistors.* Nanotechnology, 2020. **31**(23): p. 235301.

12. Cao, Q., et al., *Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates.* Nature, 2008. **454**(7203): p. 495-500.

13. Chen, J., et al., *Carbon nanotube thin-film-transistors for gas identification.* Sensors and Actuators B: Chemical, 2019. **281**: p. 1080-1087.

14. Cao, X., et al., *Fully Screen-Printed, Large-Area, and Flexible Active-Matrix Electrochromic Displays Using Carbon Nanotube Thin-Film Transistors.* ACS Nano, 2016. **10**(11): p. 9816-9822.

15. Kuo, Y., *Thin film transistor technology—Past, present, and future.* The Electrochemical Society Interface, 2013. **22**(1): p. 55.

16. Sun, D.-m., et al., *Flexible high-performance carbon nanotube integrated circuits.* Nature Nanotechnology, 2011. **6**(3): p. 156-161.

17. Street, R., *Introduction*, in *Technology and Applications of Amorphous Silicon*, R.A. Street, Editor. 2000, Springer Berlin Heidelberg: Berlin, Heidelberg. p. 1-6.

18. Miyata, Y., et al., *Length-sorted semiconducting carbon nanotubes for high-mobility thin film transistors.* Nano Research, 2011. **4**(10): p. 963-970.

19. Cao, Y., et al., *Review of Electronics Based on Single-Walled Carbon Nanotubes.* Topics in Current Chemistry, 2017. **375**(5): p. 75.

20. Cai, L. and C. Wang, *Carbon Nanotube Flexible and Stretchable Electronics.* Nanoscale Research Letters, 2015. **10**(1): p. 320.

21. Lee, Y., et al., *Semiconducting carbon nanotube network thin-film transistors with enhanced inkjet-printed source and drain contact interfaces.* Applied Physics Letters, 2017. **111**(17): p. 173108.

22. Cai, L., et al., *Fully Printed Stretchable Thin-Film Transistors and Integrated Logic Circuits.* ACS Nano, 2016. **10**(12): p. 11459-11468.

23. Millán, J., et al., *A Survey of Wide Bandgap Power Semiconductor Devices.* IEEE Transactions on Power Electronics, 2014. **29**(5): p. 2155-2163.

24. Roccaforte, F., et al., *Emerging trends in wide band gap semiconductors (SiC and GaN) technology for power devices.* Microelectronic Engineering, 2018. **187-188**: p. 66-77.

25. Mishra, U.K., et al., *GaN-Based RF Power Devices and Amplifiers.* Proceedings of the IEEE, 2008. **96**(2): p. 287-305.

26. Pearton, S.J., et al., *A review of Ga_2O_3 materials, processing, and devices.* Applied Physics Reviews, 2018. **5**(1): p. 011301.

27. Jessen, G., et al. *Toward realization of Ga_2O_3 for power electronics applications*. in *2017 75th Annual Device Research Conference (DRC)*. 2017.

28. Higashiwaki, M., et al., *Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β-Ga_2O_3 (010) substrates.* Applied Physics Letters, 2012. **100**(1): p. 013504.

29. Stepanov, S., et al., *GALLIUM OXIDE: PROPERTIES AND APPLICATIONS – A REVIEW.* Rev. Adv. Mater. Sci, 2016. **44**: p. 63-86.

30. Higashiwaki, M., et al., *Recent progress in β-Ga_2O_3 power devices.* Semiconductor Science and Technology, 2016. **31**(3): p. 034001.

31. Tadjer, M.J., et al., *Structural, Optical, and Electrical Characterization of Monoclinic β-Ga_2O_3 Grown by MOVPE on Sapphire Substrates.* Journal of Electronic Materials, 2016. **45**(4): p. 2031-2037.

32. Guo, Z., et al., *Anisotropic thermal conductivity in single crystal β-gallium oxide.* Applied Physics Letters, 2015. **106**(11): p. 111909.

33. Yan, Z. and S. Kumar, *Phonon mode contributions to thermal conductivity of pristine and defective β-Ga_2O_3.* Physical Chemistry Chemical Physics, 2018. **20**(46): p. 29236-29242.

34. Ghosh, K. and U. Singisetti, *Electron mobility in monoclinic β-Ga_2O_3—Effect of plasmon-phonon coupling, anisotropy, and confinement.* Journal of Materials Research, 2017. **32**(22): p. 4142-4152.

35. Ghosh, K. and U. Singisetti, *Ab initio velocity-field curves in monoclinic β-Ga_2O_3.* Journal of Applied Physics, 2017. **122**(3): p. 035702.

36. Maes, R., *Introduction and Preview*, in *Physically Unclonable Functions: Constructions, Properties and Applications*. 2013, Springer Berlin Heidelberg: Berlin, Heidelberg. p. 1-9.

37. Lenstra, A.K., et al., *Ron was wrong, Whit is right.* IACR Cryptol. ePrint Arch., 2012. **2012**: p. 64.

38. Heninger, N., et al., *Mining your Ps and Qs: detection of widespread weak keys in network devices*, in *Proceedings of the 21st USENIX conference on Security symposium*. 2012, USENIX Association: Bellevue, WA. p. 35.

39. Bar-El, H., et al., *The Sorcerer's Apprentice Guide to Fault Attacks.* Proceedings of the IEEE, 2006. **94**(2): p. 370-382.

40. Kocher, P., J. Jaffe, and B. Jun, *Differential Power Analysis*, in *Advances in Cryptology — CRYPTO' 99: 19th Annual International Cryptology Conference Santa Barbara, California, USA, August 15–19, 1999 Proceedings*, M. Wiener, Editor. 1999, Springer Berlin Heidelberg: Berlin, Heidelberg. p. 388-397.

41. Kocher, P.C., *Timing Attacks on Implementations of Diffie-Hellman, RSA, DSS, and Other Systems*, in *Advances in Cryptology — CRYPTO '96: 16th Annual International Cryptology Conference Santa Barbara, California, USA August 18–22, 1996 Proceedings*, N. Koblitz, Editor. 1996, Springer Berlin Heidelberg: Berlin, Heidelberg. p. 104-113.

42. Torrance, R. and D. James. *The State-of-the-Art in IC Reverse Engineering*. 2009. Berlin, Heidelberg: Springer Berlin Heidelberg.

43. Gao, Y., et al., *Emerging Physical Unclonable Functions With Nanotechnology.* IEEE Access, 2016. **4**: p. 61-80.

44. Rührmair, U. and D.E. Holcomb, *PUFs at a glance*, in *Proceedings of the conference on Design, Automation & Test in Europe*. 2014, European Design and Automation Association: Dresden, Germany. p. Article 347.

45. Devadas, S., et al. *Design and Implementation of PUF-Based "Unclonable" RFID ICs for Anti-Counterfeiting and Security Applications*. in *2008 IEEE International Conference on RFID*. 2008.

46. Guajardo, J., et al., *FPGA Intrinsic PUFs and Their Use for IP Protection*, in *Cryptographic Hardware and Embedded Systems - CHES 2007: 9th International Workshop, Vienna, Austria, September 10-13, 2007. Proceedings*, P. Paillier and I. Verbauwhede, Editors. 2007, Springer Berlin Heidelberg: Berlin, Heidelberg. p. 63-80.

47. Suh, G.E. and S. Devadas, *Physical unclonable functions for device authentication and secret key generation*, in *Proceedings of the 44th annual Design Automation Conference*. 2007, ACM: San Diego, California. p. 9-14.

48. Pappu, R., et al., *Physical One-Way Functions.* Science, 2002. **297**(5589): p. 2026-2030.

49. Gassend, B., et al., *Identification and authentication of integrated circuits.* Concurrency and Computation: Practice and Experience, 2004. **16**(11): p. 1077-1098.

50. Daihyun, L., et al., *Extracting secret keys from integrated circuits.* IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005. **13**(10): p. 1200-1205.

51. Gassend, B., et al., *Silicon physical random functions*, in *Proceedings of the 9th ACM conference on Computer and communications security*. 2002, ACM: Washington, DC, USA. p. 148-160.

52. Maiti, A. and P. Schaumont, *Improved Ring Oscillator PUF: An FPGA-friendly Secure Primitive.* Journal of Cryptology, 2011. **24**(2): p. 375-397.

53. Maiti, A. and P. Schaumont. *Improving the quality of a Physical Unclonable Function using configurable Ring Oscillators*. in *2009 International Conference on Field Programmable Logic and Applications*. 2009.

54. Kim, I., et al., *From Statistics to Circuits: Foundations for Future Physical Unclonable Functions*, in *Towards Hardware-Intrinsic Security: Foundations and Practice*, A.-R. Sadeghi and D. Naccache, Editors. 2010, Springer Berlin Heidelberg: Berlin, Heidelberg. p. 55-78.

55. Maiti, A., I. Kim, and P. Schaumont, *A Robust Physical Unclonable Function With Enhanced Challenge-Response Set.* IEEE Transactions on Information Forensics and Security, 2012. **7**(1): p. 333-345.

56. Yin, C.D. and G. Qu. *LISA: Maximizing RO PUF's secret extraction*. in *2010 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)*. 2010.

57. Holcomb, D.E., W. Burleson, and K. Fu. *Initial SRAM State as a Fingerprint and Source of True Random Numbers for RFID Tags*. 2007.

58. Das, J., et al., *MRAM PUF: A Novel Geometry Based Magnetic PUF With Integrated CMOS.* IEEE Transactions on Nanotechnology, 2015. **14**(3): p. 436-443.

59. Tuyls, P., et al., *Read-Proof Hardware from Protective Coatings*, in *Cryptographic Hardware and Embedded Systems - CHES 2006: 8th International Workshop, Yokohama, Japan, October 10-13, 2006. Proceedings*, L. Goubin and M. Matsui, Editors. 2006, Springer Berlin Heidelberg: Berlin, Heidelberg. p. 369-383.

60. Holcomb, D.E. and K. Fu, *Bitline PUF: Building Native Challenge-Response PUF Capability into Any SRAM*, in *Cryptographic Hardware and Embedded Systems – CHES 2014: 16th International Workshop, Busan, South Korea, September 23-26, 2014. Proceedings*, L. Batina and M. Robshaw, Editors. 2014, Springer Berlin Heidelberg: Berlin, Heidelberg. p. 510-526.

61. Suzuki, D. and K. Shimizu, *The Glitch PUF: A New Delay-PUF Architecture Exploiting Glitch Shapes*, in *Cryptographic Hardware and Embedded Systems, CHES 2010: 12th International Workshop, Santa Barbara, USA, August 17-20, 2010. Proceedings*, S. Mangard and F.-X. Standaert, Editors. 2010, Springer Berlin Heidelberg: Berlin, Heidelberg. p. 366-382.

62. Su, Y., J. Holleman, and B. Otis. *A 1.6pJ/bit 96% Stable Chip-ID Generating Circuit using Process Variations*. in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*. 2007.

63. Maes, R., P. Tuyls, and I. Verbauwhede, *Intrinsic PUFs from flip-flops on reconfigurable devices.* 2008.

64. Kumar, S.S., et al. *Extended abstract: The butterfly PUF protecting IP on every FPGA*. in *2008 IEEE International Workshop on Hardware-Oriented Security and Trust*. 2008.

65. Majzoobi, M., et al. *Ultra-low power current-based PUF*. in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*. 2011.

66. Kumar, R. and W. Burleson. *On design of a highly secure PUF based on non-linear current mirrors*. in *2014 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)*. 2014.

67. Simons, P., E.v.d. Sluis, and V.v.d. Leest. *Buskeeper PUFs, a promising alternative to D Flip-Flop PUFs*. in *2012 IEEE International Symposium on Hardware-Oriented Security and Trust*. 2012.

68. Chen, Q., et al. *The Bistable Ring PUF: A new architecture for strong Physical Unclonable Functions*. in *2011 IEEE International Symposium on Hardware-Oriented Security and Trust*. 2011.

69. Hu, Z., et al., *Physically unclonable cryptographic primitives using self-assembled carbon nanotubes.* Nat Nano, 2016. **11**(6): p. 559-565.

70. Akinwande, D., N. Petrone, and J. Hone, *Two-dimensional flexible nanoelectronics.* Nature Communications, 2014. **5**: p. 5678.

71. Artukovic, E., et al., *Transparent and Flexible Carbon Nanotube Transistors.* Nano Letters, 2005. **5**(4): p. 757-760.

72. Park, S., M. Vosguerichian, and Z. Bao, *A review of fabrication and applications of carbon nanotube film-based flexible electronics.* Nanoscale, 2013. **5**(5): p. 1727-1752.

73. Bradley, K., J.-C.P. Gabriel, and G. Grüner, *Flexible Nanotube Electronics.* Nano Letters, 2003. **3**(10): p. 1353-1355.

74. Konigsmark, S.T.C., et al. *CNPUF: A Carbon Nanotube-based Physically Unclonable Function for secure low-energy hardware design*. in *2014 19th Asia and South Pacific Design Automation Conference (ASP-DAC)*. 2014.

75. Chen, J. and S. Kumar, *Variability in output characteristics of single-walled carbon nanotube thin-film transistors.* IEEE Transactions on Nanotechnology, 2018. **17**(2): p. 353-361.

76. Higashiwaki, M., et al., *Depletion-mode* Ga_2O_3 *metal-oxide-semiconductor field-effect transistors on* β-Ga_2O_3 *(010) substrates and temperature dependence of their device characteristics.* Applied Physics Letters, 2013. **103**(12): p. 123511.

77. Green, A.J., et al., *3.8-MV/cm Breakdown Strength of MOVPE-Grown Sn-Doped* β-Ga_2O_3 *MOSFETs.* IEEE Electron Device Letters, 2016. **37**(7): p. 902-905.

78. Zhou, H., et al., *High-Performance Depletion/Enhancement-ode* β-Ga_2O_3 *on Insulator (GOOI) Field-Effect Transistors With Record Drain Currents of 600/450 mA/mm.* IEEE Electron Device Letters, 2017. **38**(1): p. 103-106.

79. Zhou, H., et al., β-Ga_2O_3 *on insulator field-effect transistors with drain currents exceeding 1.5 A/mm and their self-heating effect.* Applied Physics Letters, 2017. **111**(9): p. 092102.

80. Wong, M.H., et al., *Field-Plated Ga_2O_3 MOSFETs With a Breakdown Voltage of Over 750 V.* IEEE Electron Device Letters, 2016. **37**(2): p. 212-215.

81. Mun, J.K., et al., *2.32 kV breakdown voltage lateral β-Ga_2O_3 MOSFETs with source-connected field plate.* ECS Journal of Solid State Science and Technology, 2019. **8**(7): p. Q3079.

82. Moser, N.A., et al., *High pulsed current density β-Ga_2O_3 MOSFETs verified by an analytical model corrected for interface charge.* Applied Physics Letters, 2017. **110**(14): p. 143505.

83. Higashiwaki, M. and G.H. Jessen, *Guest Editorial: The dawn of gallium oxide microelectronics.* Applied Physics Letters, 2018. **112**(6): p. 060401.

84. Noh, J., et al., *High Performance β-Ga_2O_3 Nano-Membrane Field Effect Transistors on a High Thermal Conductivity Diamond Substrate.* IEEE Journal of the Electron Devices Society, 2019. **7**: p. 914-918.

85. Chabak, K.D., et al., *Enhancement-mode Ga_2O_3 wrap-gate fin field-effect transistors on native (100) β-Ga_2O_3 substrate with high breakdown voltage.* Applied Physics Letters, 2016. **109**(21): p. 213501.

86. Wong, M.H., et al., *All-ion-implanted planar-gate current aperture vertical Ga_2O_3 MOSFETs with Mg-doped blocking layer.* Applied Physics Express, 2018. **11**(6): p. 064102.

87. Wong, M.H., et al., *Current Aperture Vertical β-Ga_2O_3 MOSFETs Fabricated by N- and Si-Ion Implantation Doping.* IEEE Electron Device Letters, 2019. **40**(3): p. 431-434.

88. Wong, M.H., et al., *Enhancement-Mode β-Ga_2O_3 Current Aperture Vertical MOSFETs With N-Ion-Implanted Blocker.* IEEE Electron Device Letters, 2020. **41**(2): p. 296-299.

89. Hu, Z., et al., *Breakdown mechanism in 1 kA/cm^2 and 960 V E-mode β-Ga_2O_3 vertical transistors.* Applied Physics Letters, 2018. **113**(12): p. 122103.

90. Hu, Z., et al., *Enhancement-Mode Ga_2O_3 Vertical Transistors With Breakdown Voltage >1 kV.* IEEE Electron Device Letters, 2018. **39**(6): p. 869-872.

91. Li, W., et al. *Single and multi-fin normally-off Ga_2O_3 vertical transistors with a breakdown voltage over 2.6 kV.* in *2019 IEEE International Electron Devices Meeting (IEDM)*. 2019.

92. Green, A.J., et al., *β-Ga_2O_3 MOSFETs for Radio Frequency Operation.* IEEE Electron Device Letters, 2017. **38**(6): p. 790-793.

93. Chabak, K.D., et al. *Sub-Micron Gallium Oxide Radio Frequency Field-Effect Transistors*. in *2018 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*. 2018.

94. Xia, Z., et al., *β-Ga_2O_3 Delta-Doped Field-Effect Transistors With Current Gain Cutoff Frequency of 27 GHz.* IEEE Electron Device Letters, 2019. **40**(7): p. 1052-1055.

95. Moser, N., et al., *Toward high voltage radio frequency devices in β-Ga_2O_3.* Applied Physics Letters, 2020. **117**(24): p. 242101.

96. Slomski, M., et al., *Anisotropic thermal conductivity of β-Ga_2O_3 at elevated temperatures: Effect of Sn and Fe dopants.* Journal of Applied Physics, 2017. **121**(23): p. 235104.

97. Wong, M.H., et al., *Characterization of channel temperature in Ga_2O_3 metal-oxide-semiconductor field-effect transistors by electrical measurements and thermal modeling.* Applied Physics Letters, 2016. **109**(19): p. 193503.

98. Russell, S.A.O., et al., *Heteroepitaxial β-Ga_2O_3 on 4H-SiC for an FET With Reduced Self Heating.* IEEE Journal of the Electron Devices Society, 2017. **5**(4): p. 256-261.

99. Donmezer, N., et al., *The Impact of Nongray Thermal Transport on the Temperature of AlGaN/GaN HFETs.* IEEE Transactions on Electron Devices, 2015. **62**(8): p. 2437-2444.

100. Zhang, Y., et al., *Electrothermal Simulation and Thermal Performance Study of GaN Vertical and Lateral Power Transistors.* IEEE Transactions on Electron Devices, 2013. **60**(7): p. 2224-2230.

101. Singh, M., et al., *Pulsed Large Signal RF Performance of Field-Plated Ga_2O_3 MOSFETs.* IEEE Electron Device Letters, 2018. **39**(10): p. 1572-1575.

102. Chatterjee, B., et al., *Device-Level Thermal Management of Gallium Oxide Field-Effect Transistors.* IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019: p. 1-1.

103. Dumka, D.C., et al., *AlGaN/GaN HEMTs on diamond substrate with over 7 W/mm output power density at 10 GHz.* Electronics Letters, 2013. **49**(20): p. 1298-1299.

104. Chen, X., et al., *A Numerical Study on Comparing the Active and Passive Cooling of AlGaN/GaN HEMTs.* IEEE Transactions on Electron Devices, 2014. **61**(12): p. 4056-4061.

105. Nepal, N., et al., *Heteroepitaxial growth of β-Ga_2O_3 films on SiC via molecular beam epitaxy.* Journal of Vacuum Science & Technology A, 2020. **38**(6): p. 063406.

106. Cheng, Z., et al., *Thermal Transport across Ion-Cut Monocrystalline β-Ga_2O_3 Thin Films and Bonded β-Ga_2O_3–SiC Interfaces.* ACS Applied Materials & Interfaces, 2020. **12**(40): p. 44943-44951.

107. Cheng, Z., et al., *Integration of polycrystalline Ga_2O_3 on diamond for thermal management.* Applied Physics Letters, 2020. **116**(6): p. 062105.

108. Cheng, Z., et al., *Thermal conductance across β-Ga_2O_3-diamond van der Waals heterogeneous interfaces.* APL Materials, 2019. **7**(3): p. 031118.

109. Higashiwaki, M., et al., *Current status of Ga_2O_3 power devices.* Japanese Journal of Applied Physics, 2016. **55**(12): p. 1202A1.

110. Simms, R.J.T., et al., *Channel Temperature Determination in High-Power AlGaN/GaN HFETs Using Electrical Methods and Raman Spectroscopy.* IEEE Transactions on Electron Devices, 2008. **55**(2): p. 478-482.

111. Pomeroy, J.W., et al., *Raman Thermography of Peak Channel Temperature in β-Ga_2O_3 MOSFETs.* IEEE Electron Device Letters, 2019. **40**(2): p. 189-192.

112. Pavlidis, G., et al., *Transient Thermal Characterization of AlGaN/GaN HEMTs Under Pulsed Biasing.* IEEE Transactions on Electron Devices, 2018. **65**(5): p. 1753-1758.

113. Yazawa, K., D. Kendig, and A. Shakouri. *Thermal imaging characterization for high frequency and high power devices*. in *2015 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP-IAAC)*. 2015.

114. Tadjer, M.J., et al., *Electrothermal Evaluation of AlGaN/GaN Membrane High Electron Mobility Transistors by Transient Thermoreflectance.* IEEE Journal of the Electron Devices Society, 2018. **6**: p. 922-930.

115. Maize, K., et al. *High Resolution Thermal Characterization and Simulation of Power AlGaN/GaN HEMTs Using Micro-Raman Thermography and 800 Picosecond Transient Thermoreflectance Imaging*. in *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. 2014.

116. Chen, G., *Nanoscale energy transport and conversion: a parallel treatment of electrons, molecules, phonons, and photons*. 2005: Oxford university press.

117. Kittel, C., P. McEuen, and P. McEuen, *Introduction to solid state physics*. Vol. 8. 1996: Wiley New York.

118. Majumdar, A., *Microscale Heat Conduction in Dielectric Thin Films.* Journal of Heat Transfer, 1993. **115**(1): p. 7-16.

119. Loy, J.M., *An acceleration technique for the solution of the phonon Boltzmann transport equation*. 2010, Purdue University.

120. Hess, K., *Boltzmann transport equation*, in *The Physics of Submicron Semiconductor Devices*. 1988, Springer. p. 33-43.

121. Vallabhaneni, A.K., et al., *Solving Nongray Boltzmann Transport Equation in Gallium Nitride.* Journal of Heat Transfer, 2017. **139**(10): p. 102701.

122. Loy, J.M., D. Singh, and J.Y. Murthy. *Non-Gray phonon transport using a hybrid BTE-Fourier solver*. in *Heat Transfer Summer Conference*. 2009.

123. Vallabhaneni, A.K., et al. *A Study of Spatially-Resolved Non-Equilibrium in Laser-Irradiated Graphene Using Boltzmann Transport Equation*. in *ASME International Mechanical Engineering Congress and Exposition*. 2013. American Society of Mechanical Engineers.

124. Donmezer, F.N., et al. *Lattice Boltzmann and Discrete Ordinates Methods for Phonon Transport Modeling: A Comparative Study*. in *ASME 2011 International Mechanical Engineering Congress and Exposition*. 2011.

125. Murthy, J.Y., et al., *Review of Multiscale Simulation in Submicron Heat Transfer.* 2005. **3**(1): p. 5-32.

126. Narumanchi, S.V.J., J.Y. Murthy, and C.H. Amon, *Comparison of Different Phonon Transport Models for Predicting Heat Conduction in Silicon-on-Insulator Transistors.* Journal of Heat Transfer, 2005. **127**(7): p. 713-723.

127. Ali, S.A., et al., *Large-scale parallel computation of the phonon Boltzmann Transport Equation.* International Journal of Thermal Sciences, 2014. **86**: p. 341-351.

128. Ali, S.A. and S. Mazumder, *Phonon Heat Conduction in Multidimensional Heterostructures: Predictions Using the Boltzmann Transport Equation.* Journal of Heat Transfer, 2015. **137**(10).

129. Loy, J.M., S.R. Mathur, and J.Y. Murthy, *A Coupled Ordinates Method for Convergence Acceleration of the Phonon Boltzmann Transport Equation.* Journal of Heat Transfer, 2015. **137**(1).

130. Kumar, S., J.Y. Murthy, and M.A. Alam, *Percolating Conduction in Finite Nanotube Networks.* Physical Review Letters, 2005. **95**(6): p. 066802.

131. Pimparkar, N., et al., *Current–Voltage Characteristics of Long-Channel Nanobundle Thin-Film Transistors: A "Bottom-Up" Perspective.* IEEE Electron Device Letters, 2007. **28**(2): p. 157-160.

132. Kumar, S., et al., *Theory of transfer characteristics of nanotube network transistors.* Applied Physics Letters, 2006. **88**(12): p. 123505.

133. Lobb, C.J. and D.J. Frank, *Percolative conduction and the Alexander-Orbach conjecture in two dimensions.* Physical Review B, 1984. **30**(7): p. 4090-4092.

134. Frank, D.J. and C.J. Lobb, *Highly efficient algorithm for percolative transport studies in two dimensions.* Physical Review B, 1988. **37**(1): p. 302-307.

135. Kumar, S., *Electrical and thermal transport in nanotube based thin film transistors*. 2007, Purdue University: Ann Arbor. p. 162.

136. Pimparkar, N.V., *Nonlinear electronic and photovoltaic characteristics of nanonet transistors and solar cells*. 2008, Purdue University: Ann Arbor. p. 130.

137. Gupta, M.P., *Numerical investigation of carbon nanotube thin-film composites and devices*. 2014, Georgia Institute of Technology.

138. *SentaurusTM Device User Guide, O-2018.12," ed: Synopsys Inc., 2018.*

139. Kendig, D., et al. *Accurate thermoreflectance imaging of nano-features using thermal decay*. in *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*. 2017.

140. Ziabari, A., et al. *Sub-diffraction thermoreflectance thermal imaging using image reconstruction*. in *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*. 2017.

141. Kendig, D., A. Tay, and A. Shakouri. *Thermal analysis of advanced microelectronic devices using thermoreflectance thermography*. in *2016 22nd International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*. 2016.

142. Matei, C., et al., *Dynamic Temperature Measurements of a GaN DC–DC Boost Converter at MHz Frequencies.* IEEE Transactions on Power Electronics, 2020. **35**(8): p. 8303-8310.

143. Dallas, J., et al., *Thermal characterization of gallium nitride p-i-n diodes.* Applied Physics Letters, 2018. **112**(7): p. 073503.

144. Loy, J.M., *An efficient solution procedure for simulating phonon transport in multiscale multimaterial systems*. 2013, The University of Texas at Austin.

145. Kumar, N., et al., *Multigated Carbon Nanotube Field Effect Transistors-Based Physically Unclonable Functions As Security Keys.* IEEE Internet of Things Journal, 2018. **6**(1): p. 325-334.

146. Pimparkar, N., *Nonlinear Electronic and Photovoltaic Characteristics of Nanonet Transistors and Solar Cells*, in *Electrical and Coputer Enfineering*. 2008, Purdue University: West Lafayette, IN, USA.

147. Pike, G.E. and C.H. Seager, *Percolation and conductivity: A computer study. I.* Physical Review B, 1974. **10**(4): p. 1421-1434.

148. Balberg, I. and N. Binenbaum, *Computer study of the percolation threshold in a two-dimensional anisotropic system of conducting sticks.* Physical Review B, 1983. **28**(7): p. 3799-3812.

149. Rukhin, A., et al., *A statistical test suite for random and pseudorandom number generators for cryptographic applications*. 2001, Booz-allen and hamilton inc mclean va.

150. Joishi, C., et al., *Effect of buffer iron doping on delta-doped β-Ga_2O_3 metal semiconductor field effect transistors.* Applied Physics Letters, 2018. **113**(12): p. 123501.

151. Kumar, N., et al. *Electro-Thermal Simulation of Delta-Doped β-Ga_2O_3 Field Effect Transistors*. in *2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*. 2019.

152. Passlack, M., et al., *Dielectric properties of electron-beam deposited Ga_2O_3 films.* Applied Physics Letters, 1994. **64**(20): p. 2715-2717.

153. Yao, Y., et al., *Electrical behavior of β-Ga_2O_3 Schottky diodes with different Schottky metals.* Journal of Vacuum Science & Technology B, 2017. **35**(3): p. 03D113.

154. Lorenz, M.R., J.F. Woods, and R.J. Gambino, *Some electrical properties of the semiconductor β-Ga_2O_3.* Journal of Physics and Chemistry of Solids, 1967. **28**(3): p. 403-404.

155. Janowitz, C., et al., *Experimental electronic structure of $In_2O_3$and Ga_2O_3.* New Journal of Physics, 2011. **13**(8): p. 085014.

156. Krishnamoorthy, S., et al., *Delta-doped β-gallium oxide field-effect transistor.* Applied Physics Express, 2017. **10**(5): p. 051102.

157. Choi, S., et al., *The Impact of Bias Conditions on Self-Heating in AlGaN/GaN HEMTs.* IEEE Transactions on Electron Devices, 2013. **60**(1): p. 159-162.

158. Galazka, Z., et al., *On the bulk β-Ga_2O_3 single crystals grown by the Czochralski method.* Journal of Crystal Growth, 2014. **404**: p. 184-191.

159. Kumar, N., et al., *Electrothermal Characteristics of Delta-Doped β-Ga_2O_3 Metal-Semiconductor Field-Effect Transistors.* IEEE Transactions on Electron Devices, 2019: p. 1-7.

160. Wei, R., et al., *Thermal conductivity of 4H-SiC single crystals.* Journal of Applied Physics, 2013. **113**(5): p. 053503.

161. Cheng, Z., et al., *Experimental observation of high intrinsic thermal conductivity of AlN.* Physical Review Materials, 2020. **4**(4): p. 044602.

162. Handwerg, M., et al., *Temperature-dependent thermal conductivity in Mg-doped and undoped β-Ga_2O_3 bulk-crystals.* Semiconductor Science and Technology, 2015. **30**(2): p. 024006.

163. Ni, C., *Phonon transport models for heat conduction in sub-micron geometries with application to microelectronics*. 2009, Purdue University: Ann Arbor. p. 176.

164. Mengle, K.A. and E. Kioupakis, *Vibrational and electron-phonon coupling properties of β-Ga_2O_3 from first-principles calculations: Impact on the mobility and breakdown field.* AIP Advances, 2019. **9**(1): p. 015313.