

7.2 kV Three-Port SiC Single-Stage Current-Source Solid-State Transformer with 90 kV Lightning Protection

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Abstract—This article proposes a multiport modular single-stage current-source solid-state transformer (SST) for applications like photovoltaic, energy storage integration, electric vehicle fast charging, data center, etc. The 7.2 kV 50 kVA current-source SST consists of five input-series output-parallel modules, each based on 3.3 kV SiC reverse-blocking MOSFET-plus-diode modules. The proposed SST has some unique features. First, compared to the voltage-source or matrix converter-based SSTs, the current-source SST has a unique advantage of single-stage isolated AC/DC or AC/AC conversion with an inductive DC link, but no medium-voltage (MV) AC experiments have been reported. This article for the first time demonstrates MV AC current-source SST up to 7.5 kV peak. Second, the multiport SST has a buffer port for active power decoupling (APD) or energy storage integration. The double-line-frequency power ripple from single-phase AC grid normally results in a large capacitor size in MV SSTs. The APD scheme is proposed in MV applications for the first time to enable a reduced DC link and the electrolytic capacitor-less SST with high reliability. Third, as a direct grid-connected converter without line-frequency transformer, insulation and protection are critical. A medium-frequency transformer design passes 55 kV basic-insulation level (BIL) and 60 kV high potential dielectrics withstand test with only 0.09% leakage inductance. Importantly, a lightning protection scheme is presented to protect the SST itself from 90 kV BIL impulse. Fourth, the proposed current-source SST topology is a modular soft-switching solid-state transformer (M-S4T) with full-range zero-voltage switching and controlled dv/dt for low electromagnetic interference. These concepts are verified in a three-port M-S4T prototype with forced oil cooling under single-module, stacked-module, steady-state, and dynamic operations.

Index Terms—Solid-state transformer (SST), current-source inverter (CSI), current-source converter (CSC), high-frequency link (HFL), input-series output-parallel (ISOP), ZVS, medium-frequency transformer (MFT), cascaded multilevel power electronic transformer (PET).

I. INTRODUCTION

WITH increased penetration of intermittent resources such as renewable energy and electric vehicles in distribution grids, solid-state transformer (SST) or power electronic transformer (PET) [1]-[4] is an attractive solution to replace line-frequency transformer (LFT) for more flexibility and controllability as shown in a comparative study [2]. In traction

locomotive [4], renewable energy integration [5]-[7], and data center applications [8]-[9], the SST-based solutions are also promising with higher efficiency and power density compared to conventional LFT-based solutions.

Conventional SST or PET topology is typically a three-stage circuit, i.e., hard-switched rectifiers and inverters coupled with an isolated bidirectional DC/DC converter (IBDC) [3]-[4]. Due to high dv/dt more than 50 kV/ μ s from hard-switched SiC devices [10]-[12], the hard-switched rectifiers and inverters suffer from electromagnetic interference (EMI) issues [13]. Furthermore, the hard-switching losses limit the rectifier switching frequency and result in large filters [13]. The dual-active-bridge (DAB) converter [14]-[15] is normally used as the IBDC [16]-[19]. However, zero-voltage switching (ZVS) and controlled dv/dt can only be achieved within certain operating range [14]-[15], which means more losses and EMI issues outside the soft-switching range. Another conventional SST topology is based on matrix converter [20]-[22]. This topology features single-stage power conversion with fewer components and potentially higher power density. However, bidirectional switches are required. The associated commutation strategy is complicated, especially considering the leakage inductance of the medium-frequency transformer (MFT) in the SST [23]-[24]. The absence of DC link makes disturbance rejection from the grid challenging [20]-[24].

Current-source SST features single-stage power conversion and the MFT magnetizing inductance as a DC link. In addition to these advantages, a current-source soft-switching solid-state transformer (S4T) is proposed to achieve minimal conduction path and full-range zero-voltage switching (ZVS) [1]. Moreover, the S4T is universal for bidirectional AC-AC, AC-DC, and DC-DC conversion [1]. Compared to the hard-switching current-source Dyna-C SST [25], the ZVS in the proposed S4T reduces power loss, dv/dt , and the EMI. The current-source ZVS isolated high-frequency link (HFL) circuit has the soft-switching capability and associated benefits [26]. However, the resonant time in the ZVS isolated HFL circuit can be as long as 50 μ s, which increases the lost duty cycle and limits switching frequency and efficiency. In contrast, the S4T achieves a short resonant time and small lost duty cycle [1]. Similar to other SST topologies, scaling the current-source SST up to the medium-voltage (MV) level is one critical issue. The modular S4T (M-

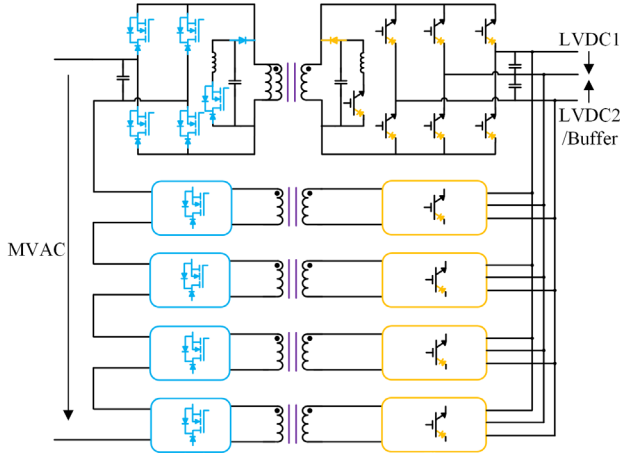
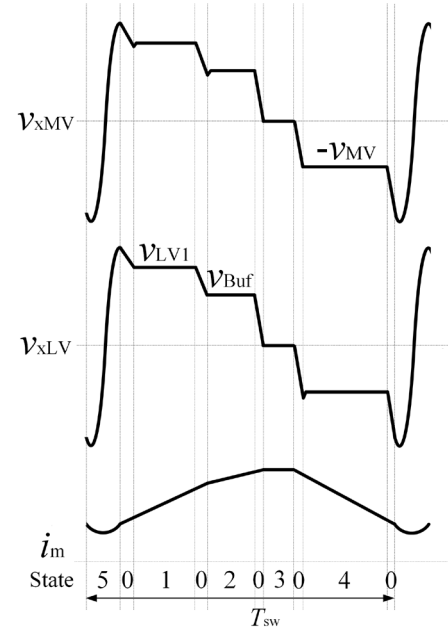


Fig. 1. Schematic of the proposed three-port modular single-stage current-source SST.

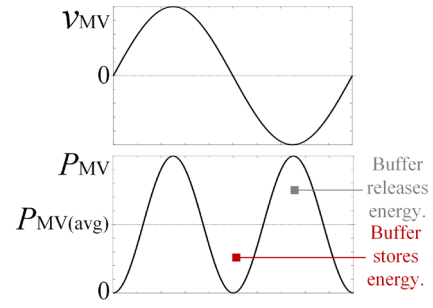
S4T) concept in [27]-[28] allows converter modules connected in series or in parallel to scale beyond single device voltage for higher voltage and higher power applications. Unlike voltage-source SST research where multiple MV prototypes have been demonstrated in [13], [29]-[31], only one MV current-source SST prototype has been reported, i.e., a 5 kV DC-DC M-S4T prototype in [27]. However, for most SST applications including utility distribution, traction locomotive, and data center, interfacing with MV AC grids are required, where the feasibility and the experiments of current-source SST have not been reported in the literature.

For a modular SST, a single-phase configuration is required to connect the converter modules input-series output-parallel (ISOP) to interface MV grid. One important issue is the double-line-frequency 120 Hz power ripple from the single-phase AC grid. If the 120 Hz ripple is buffered by the DC link, a large DC-link buffer is generally required as the DC-link voltage ripple should be kept low to decouple the two converter stages and ensure the stability in the multiple-stage SSTs [32]. However, electrolytic capacitors are not available at voltages as high as several kilovolts and suffer from reliability issue [32]-[33]. Film capacitors can be used, but they have much larger size and are among the physically largest components [13]. Therefore, it is of interest to actively decouple the 120 Hz ripple into a high-ripple buffer port for higher power density, which leads to the three-port architecture of the M-S4T in this article. The active power decoupling (APD) method of the 120 Hz buffer port for single-phase converter to boost power density is conventionally used in LV converters [33]-[35], but has not been reported in the existing literature for MV ISOP converters. Moreover, the buffer port has the flexibility to be modified to interface energy storage if needed, which enables the three-port M-S4T to integrate multiple LV sources or loads at the same time.

According to the above reasoning, a 7.2 kV 50 kVA three-port reduced-DC-link M-S4T with 120 Hz APD buffer port is proposed in this paper. Focusing on the 7.2 kV hardware, this paper reports the MV results of modular AC current-source SST and the APD for MV ISOP converters for the first time, to the authors' best knowledge. Moreover, a lightning impulse protection scheme is proposed and verified for the first time to



(a)



(b)

Fig. 2. (a) Conceptual switching-cycle waveforms of the proposed SST under LV-MV power flow direction when buffer releases energy. (b) Conceptual line-cycle waveforms to illustrate how the buffer port absorbs the 120 Hz power ripple from the single-phase MVAC port.

achieve the 90 kV basic insulation level (BIL) for the SST prototype, i.e., more than the MFT.

The rest of the paper is organized as follows. The proposed topology, the operation principle, and the control methods are discussed in Section II. Section III introduces the design and the testing of the components in the M-S4T, including a coaxial-cable-based medium-frequency transformer (MFT) to simultaneously achieve 55 kV BIL and 0.09% leakage inductance, device characterization results of a 3.3 kV SiC reverse-blocking module, resonant circuits, and the lightning protection scheme. Single-module and five-module experimental results during steady state and dynamics up to 7.5 kV peak are demonstrated in Section IV. Section V concludes the paper.

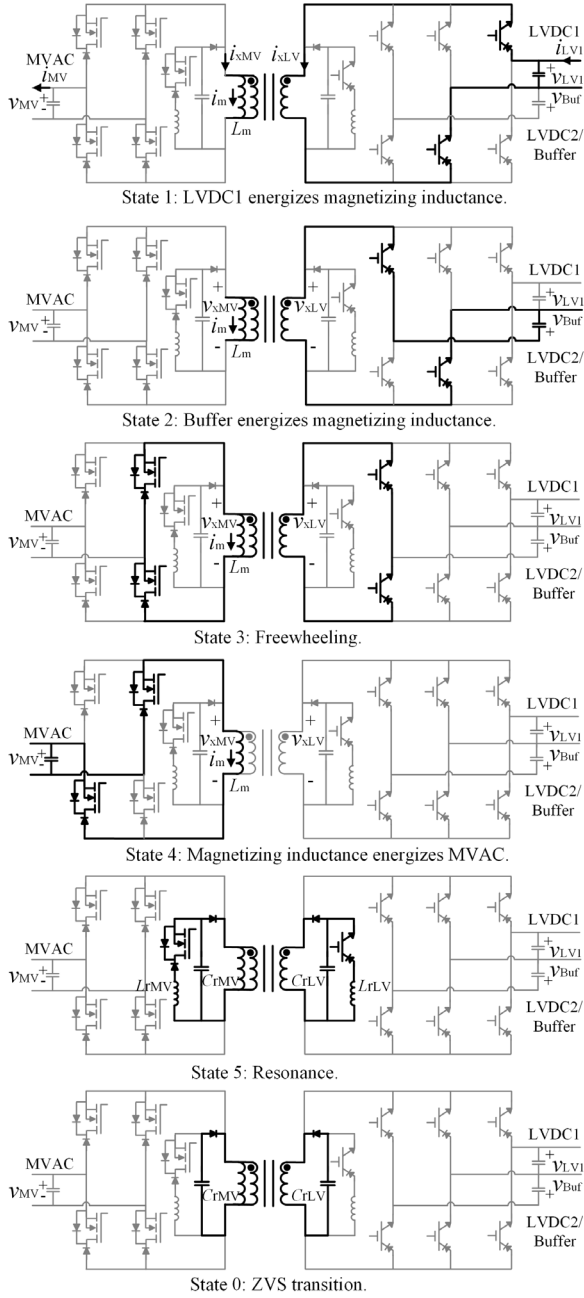


Fig. 3. Operating states of the proposed SST under LV-MV power flow direction when buffer releases energy.

II. TOPOLOGY AND CONTROL OF THE PROPOSED THREE-PORT SIC MODULAR SINGLE-STAGE CURRENT-SOURCE SST

A. Topology and Operation Principle of the Proposed SST

The topology of the proposed SST is shown in Fig. 1. It consists of five S4T with reduced conduction loss modules [1] connected in series on the MV side and in parallel on the LV side. Each S4T module has one 1.44 kV single-phase MV port and two 350 V LVDC ports. One LV port acts as a buffer port to absorb the 120 Hz ripple. This LVDC port can also be used to integrate energy storage as per application requirements. LV and

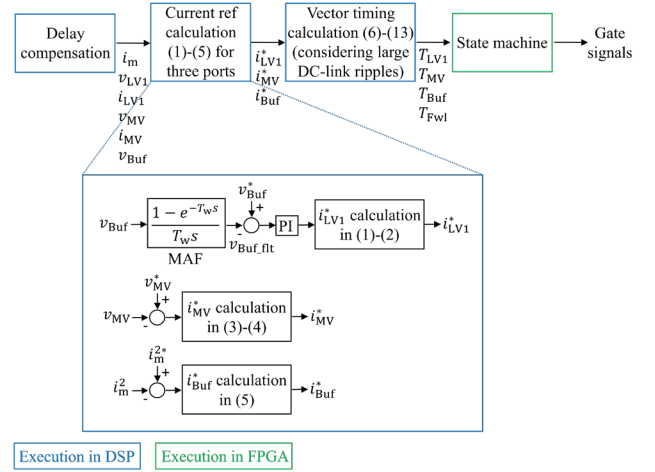


Fig. 4. Block diagram of the predictive control of the proposed three-port SST with active power decoupling and reduced DC link. Model-based delay compensation in [36]-[37] is applied.

MV semiconductor bridges use reverse-blocking devices, similar to a conventional current-source converter (CSC). The MV and LV bridges are isolated with an MFT. Auxiliary branches are installed on both sides of the MFT to realize the full-range ZVS [1]. The magnetizing inductance of the MFT acts as an inductive DC-link for this CSC-based topology.

The conceptual switching-cycle waveforms are shown in Fig. 2, while the states in a switching cycle are illustrated in Fig. 3. In this three-port configuration, the SST operation consists of three active states (states 1, 2, 4) that are interposed with a ZVS transition state (state 0) and/or a resonant state (state 5). The ZVS transition state and the resonant state adjust the voltages across the MFT (v_{xMV} and v_{xLV}) to achieve the ZVS. For example, in Fig. 2, there is a ZVS transition state 0, when the SST switches between state 1 and state 2. During this ZVS transition state, the voltages across the MFT (v_{xMV} and v_{xLV}) and the resonant capacitors (v_{CfMV} and v_{CfLV}) are discharged by the magnetizing current (i_m) until v_{xLV} reaches the voltage level of v_{Buf} . Then, the devices for the incoming state 2 can be turned on with zero voltage, i.e., $v_{xLV} - v_{Buf}$ across them to achieve the ZVS. In state 5, the resonant inductors (L_{rMV} and L_{rLV}) resonate with and flip the voltages across the resonant capacitors (C_{fMV} and C_{fLV}) and the MFT from a negative value to a positive value to facilitate the ZVS for the next switching cycle. Note that the duration of state 0 at the end of the switching cycle can be adjusted to ensure that the MFT voltages (v_{xMV} and v_{xLV}) are sufficiently negative before state 5 of the next switching cycle and higher than v_{LV1} after state 5. Therefore, the full-range ZVS can be maintained.

In Fig. 2, the state sequences change across the line cycle due to the 120 Hz power ripple in the instantaneous AC power P_{MV} . When the instantaneous AC power is higher than LVDC1 power, both the buffer and the LVDC1 ports energize L_m . In the same switching cycle, the MVAC port de-energizes L_m . When the instantaneous AC power is lower than the LVDC1 power, the LVDC1 port energizes L_m , but the buffer and the MVAC ports de-energize L_m . The state sequence where the buffer port and the LVDC1 port energizes L_m in state 1 and 2, and L_m releases energy to the MVAC port in state 4 is shown in Fig. 2.

A freewheeling state (state 3) can be added in a switching cycle as a zero vector, when necessary, to ensure a constant switching frequency.

B. Control of the Proposed SST

A predictive control method [36] for this three-port modular SST with active power decoupling and reduced DC link is used in this prototype. This control is extended from the model predictive priority-shifting control concept developed for two-port stacked low-inertia SST [37]. The power flow scenario here is the same as the experimental prototype, i.e., sinking current from a LV source and forming voltage for a MV load as shown in Figs. 2-3. Furthermore, a capacitor bank is connected to the buffer port to buffer the 120 Hz power ripple. The same principle applies to other power flow scenarios.

The control block diagram is depicted in Fig. 4. First, the current reference for each of the three ports is computed. For the LV side, the current reference (i_{LV1}^*) is calculated in (1) to absorb the DC component of the MVAC port power ($V_{MV}I_{MV}$). Moreover, a PI controller compensates the power loss in the buffer capacitor bank by regulating the DC component of the buffer port voltage (v_{Buf_flt}) in (2), which is the measured buffer port voltage filtered through a moving-average filter (MAF) [38]. The MAF window length (T_w) in Fig. 4 corresponds to 120 Hz.

$$i_{LV1}^* = V_{MV}I_{MV}/v_{LV1} + k_p(V_{Buf}^* - v_{Buf_flt}) + k_i \text{Int}_{Buf} \quad (1)$$

$$\text{Int}_{Buf} = \text{Int}_{Buf_last} + (V_{Buf}^* - v_{Buf_flt}) \quad (2)$$

For the MV side, the MV current reference (i_{MV}^*) in (3) is determined by the sum of the charge required to control the deviation of the MV voltage measurement (v_{MV}) from its reference (v_{MV}^*) in (4) and a feedforward term of the measured MV current (i_{MV}).

$$i_{MV}^* = (v_{MV}^* - v_{MV})C_{fMV}f_{sw} + i_{MV} \quad (3)$$

$$v_{MV}^* = \sqrt{2}V_{MV}^* \cos(\theta_{MV}^*) \quad (4)$$

For the buffer port, the difference between the MVAC port power, the LVDC1 port power, and the power required to adjust the magnetizing current is absorbed. It is mainly the 120 Hz power when the converter reaches steady state. The buffer port current reference (i_{Buf}^*) can be thereby calculated in (5).

$$i_{Buf}^* = (0.5L_m(i_m^{*2} - i_m^2(t))f_{sw} + v_{MV}i_{MV}^* - v_{LV1}i_{LV1}^*)/v_{Buf} \quad (5)$$

Second, the dwelling time of each port is computed. For the LV side, the vector timing is given by (6), which is the time required to deliver the reference charge ($i_{LV1}^*T_{sw}$). Note that a large switching-ripple exists on the magnetizing current in Fig. 2. The second term in (6), which is a second-order one, accounts for the charge delivery deviation from the large switching ripple, using last switching cycle's dwelling time (T_{LV1_last}).

$$T_{LV1} = \frac{i_{LV1}^*}{i_m(t)} \cdot T_{sw} - \frac{v_{LV1}T_{LV1_last}^2/(2L_m)}{i_m(t)} \quad (6)$$

After the LV vector, the magnetizing current can be updated as (7). A saturation limit can be enforced to avoid significant overcurrent or undercurrent, i.e., adjusting T_{LV1} if needed to ensure $i_m(t + T_{LV1})$ is within the preset saturation limits.

$$i_m(t + T_{LV1}) = i_m(t) + v_{LV1}/L_m \cdot T_{LV1} \quad (7)$$



Fig. 5. Devices applied in the prototype. (a) 3.3 kV Cree SiC MOSFET + SiC diode reverse-blocking module. (b) 650 V self-assembled Si IGBT + SiC diode module on a heatsink.

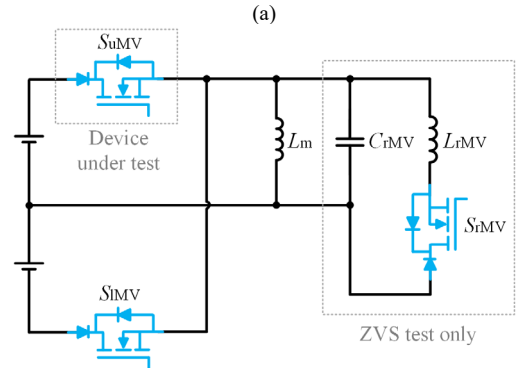
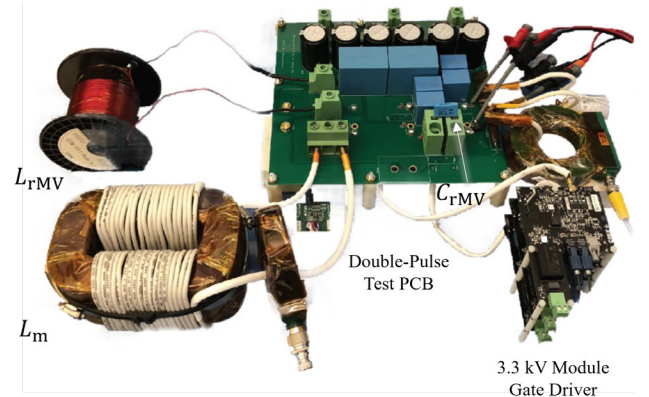


Fig. 6. (a) The photo and (b) the schematic of the double-pulse test setup for the 3.3 kV SiC reverse-blocking module characterization. The 3.3 kV module is installed under the PCB in Fig. 6 (a).

Similarly, the vector timing can be calculated as given by (8)-(9), and (11)-(12) for the buffer port and the MV port, respectively. Equation (10) means that the magnetizing current remains nearly the same as the freewheeling state in Fig. 2.

$$T_{Buf} = \frac{i_{Buf}^*}{i_m(t+T_{LV1})} \cdot T_{sw} - \frac{v_{Buf}T_{Buf_last}^2/(2L_m)}{i_m(t+T_{LV1})} \quad (8)$$

$$i_m(t + T_{LV1} + T_{Buf}) = i_m(t + T_{LV1}) + v_{Buf}/L_m \cdot T_{Buf} \quad (9)$$

$$i_m(t + T_{LV1} + T_{Buf} + T_{Fwl}) = i_m(t + T_{LV1} + T_{Buf}) \quad (10)$$

$$T_{MV} = \frac{i_{MV}^*}{i_m(t+T_{LV1}+T_{Buf}+T_{Fwl})} \cdot T_{sw} + \frac{v_{MV}T_{MV_last}^2/(2L_m)}{i_m(t+T_{LV1}+T_{Buf}+T_{Fwl})} \quad (11)$$

$$i_m(t + T_{sw}) = i_m(t + T_{LV1} + T_{Buf} + T_{Fwl}) - v_{MV}/L_m \cdot T_{MV} \quad (12)$$

Finally, the freewheeling vector duration (T_{Fwl}) can be calculated to ensure a constant switching frequency in (13), where the resonant state duration (T_{Res}) and the ZVS transition

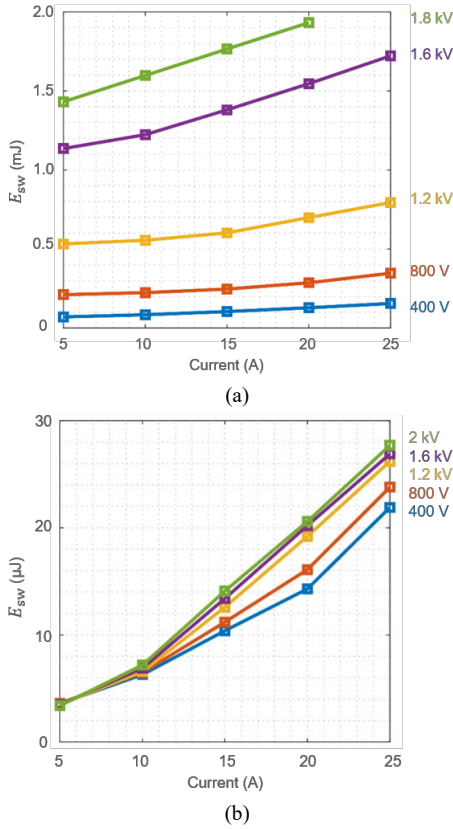


Fig. 7. 3.3 kV SiC reverse-blocking module (a) hard-switching and (b) soft-switching loss across different voltages and currents.

state duration (T_{ZVS}) correspond to states 0 and 5 in Fig. 2 (a), respectively.

$$T_{Fwl} = T_{sw} - T_{MV} - T_{LV} - T_{Buffer} - T_{Res} - T_{ZVS} \quad (13)$$

In the experiments of the five-module SST, the MV voltage magnitude (V_{MV}^*) and the phase angle (θ_{MV}^*) is received from a master controller through a communication architecture in [39]. Then, each converter module has its own distributed controller to calculate its own vector timings in the DSP to regulate its MV-side voltage for balanced voltages. The FPGA in each converter module executes state machine according to the vector sequences and the timings from the DSP. Also, the duration of the ZVS transition state in Fig. 2 can be computed and compensated in the experimental implementation.

III. DESIGN OF THE PROPOSED THREE-PORT SiC MODULAR SINGLE-STAGE CURRENT-SOURCE SST

A. Semiconductor Devices

With small switching loss from the semiconductor devices thanks to the ZVS technique, conduction loss dominates the device loss. Therefore, low conduction drop devices are selected for each 10 kVA 1.44 kV AC to 350 V DC SST module. Similar to current-source inverter (CSI), reverse-blocking modules are required. On the MV side, considering the peak voltage of 2 kV, customized 3.3 kV 45 A SiC reverse-blocking modules in Fig. 5 (a) from Cree are applied. Although the SST module's power rating is at 10 kVA, the 3.3 kV 45 A module itself is not limited

Table I. Parameters of the designed 7.2 kV 50 kVA SST prototype.

| Parameter | Symbol | Value |
|---------------------------|------------|---------|
| MV Magnetizing Inductance | L_{mMV} | 6.5 mH |
| LV Magnetizing Inductance | L_{mLV} | 180 μH |
| MV Leakage Inductance | L_{lgMV} | 6.5 μH |
| MV Resonant Inductance | L_{rMV} | 72 μH |
| MV Resonant Capacitance | C_{rMV} | 23.1 nF |
| LV Resonant Inductance | L_{rLV} | 2 μH |
| LV Resonant Capacitance | C_{rLV} | 277 nF |
| MV Filter Capacitance | C_{fMV} | 2.0 μF |
| LV Filter Capacitance | C_{fLV} | 80.0 μF |
| Buffer Capacitance | C_{Buf} | 5.3 mF |

Table II. Volume comparison of the SST prototype with and without the proposed active power decoupling scheme.

| | With (30% pk-pk ripple) | Without (2% pk-pk ripple) |
|--------------------------------------|-------------------------|---------------------------|
| Required Capacitor for 120 Hz Ripple | 5.3 mF | 79.5 mF |
| Required Capacitor Volume | 26.6 L | 399.2 L |
| SST Prototype Volume | 319.4 L | 692.0 L |
| Capacitor/SST Prototype Volume | 8.3% | 57.7% |

For a fair comparison, the same model of film capacitor is assumed as installed in the experimental prototype in Fig. 18.

to this power rating and can enable power conversion over 10 kVA. In this module, SiC diode dies are connected in series with SiC MOSFET dies in reverse-blocking configuration. On the LV-side, because no commercial CSI reverse-blocking modules with SiC diodes are available, 650 V discrete devices are used. As shown in Fig. 5 (b), two Infineon IKW75N65EL5 Si IGBTs are in parallel for each LV switch position and two GeneSiC GC50MPS06-247 SiC diodes are in parallel for each LV diode position.

The characteristics of SiC reverse-blocking modules are rarely reported in the literature. To better understand the switching performance of the customized SiC reverse-blocking module, a novel double-pulse test setup is constructed as shown in Fig. 6. The device S_{IMV} provides a current commutation path to let the device under test S_{uMV} turn on and off under a given current. The resonant branch including the resonant capacitor C_{rMV} and the resonant inductor L_{rMV} can be disconnected for double-pulse tests under the hard-switching condition. The resonant branch is connected and functions in states 5 and 0 for the ZVS testing condition as discussed in Fig. 2 (a). The switching loss measurements are illustrated in Fig. 7 from 400 V 5 A to 2 kV 25 A. Over 90% switching loss reduction is observed in the measurement results under the ZVS in Fig. 7 (b), as compared to the hard-switching case in Fig. 7 (a) [40].

B. Filters

Table I shows the designed parameters of the SST prototype, which consists of five ISOP 1.44 kV to 350 V converter modules. The switching frequency is chosen as 16 kHz, which is just higher than audible acoustic noise frequency. The turns ratio of the MFT is selected to be 6:1 ($N_{x\text{finr}}$) to match the voltage conversion ratio for each 1.44 kV AC to 350 V DC SST module. The magnetizing inductance is designed for 40% peak-to-peak ripple. The highest switching ripple current on the magnetizing

inductance occurs at the 2 kV peak of the single-phase MV AC grid (V_{MV_pk}), when the MV grid, the LV port, and the buffer port receives 20 kVA, delivers 10 kVA, and delivers 10 kVA instantaneous power, respectively. Under the rated operating point, the MV vector occupies 50% of the effective duty cycle (D_{eff}) in a switching cycle (T_{sw}), as some duty cycles are lost due to the ZVS. Then, the switching current ripple (ΔI_{mMV}) of the magnetizing current can be computed in (14) when referred to the MV side of the 6:1 MFT.

$$\Delta I_{mMV} = \frac{V_{MV_pk} D_{eff} T_{sw}}{L_{mMV} \cdot 2} \quad (14)$$

When the magnetizing current is controlled to be a constant value superimposed by the switching ripple, the DC component of the magnetizing current (I_{mMV_dc}) is determined by the current requirement at the peak of the MV AC grid. The current required is the sum of the buffer current peak, the MV current peak, and the LV port's current over the effective duty cycle as computed by (15) to be 140 A.

$$I_{mMV_dc} = \frac{I_{MV_pk} + (I_{Buf_pk} + I_{LV}) N_{xfmr}}{D_{eff}} \quad (15)$$

Based on (14)-(15), the sizing of the magnetizing inductance can be determined for 40% peak-to-peak ripple.

The capacitive filters for the three ports of each converter module are designed for peak-to-peak switching ripples under 10%. For example, the switching ripple of the MV port is given as (16). The other ports can be sized similarly.

$$\Delta V_{fMV} = \frac{I_{mMV_dc}}{C_{fMV}} \left(1 - \frac{D_{eff}}{2}\right) T_{sw} \quad (16)$$

Note that with the proposed three-port APD scheme, the ripple across the buffer capacitor (C_{Buf}) connected to the buffer port is given by (17).

$$\Delta V_{Buf} = \frac{P_{rated}}{2\pi f_{line} C_{Buf} V_{Buf}} \quad (17)$$

The buffer capacitor is designed as 5.3 mF to tolerate 30% peak-to-peak ripple. However, without the three-port APD scheme, the LV port has to absorb the 120 Hz power ripple with limited peak-to-peak voltage ripple from stringent load interface requirement. If the allowed peak-to-peak ripple is 2%, the buffer capacitance will be 79.5 mF. The 53.8% total SST prototype volume saving and the associated power density improvement can be appreciated in Table II, where the volume of the other components in the SST is assumed the same. One additional benefits of the buffer capacitor port is the capability of absorbing transient energy like a slack bus for voltage balancing, which is critical for modular reduced DC-link converter.

C. Resonant Circuit

The resonant capacitors and the resonant inductors are designed to achieve a trade-off among dv/dt , resonant time, and the voltage stress from the resonant operation and MFT leakage inductance. First, the dv/dt should be small to reduce the switching loss and the EMI, where large resonant capacitances are preferred. Second, the resonant time and the ZVS transition time should be short to reduce the lost duty cycle for high efficiency, as there is no energy transfer occurs during the lost duty cycle. To reduce the lost duty cycle, small resonant capacitances are preferred. Third, the voltage stress should be

within the device safe operating region, where large resonant capacitances are preferred. The MV resonant capacitor (C_{rMV}) and the LV resonant capacitor (C_{rLV}) are selected to be 23.1 nF and 277 nF, respectively. With the designed resonant capacitances, the dv/dt across the resonant capacitor and the devices on the MV side is calculated in (18) to be less than 800 V/ μ s.

$$\frac{dv}{dt}_{MV} = \frac{I_{mMV}}{C_{rMV} + C_{rLV} / N_{xfmr}^2} \quad (18)$$

The dv/dt is significantly reduced compared to the hard-switching condition of over 50 kV/ μ s. Moreover, The switching loss has been measured in the μ J level with a resonant capacitance of 33 nF in Fig. 7. Therefore, the first design consideration is fulfilled. Here, 33 nF is around the same level as the designed capacitances, when both of the LV and MV resonant capacitances are referred to the MV side of the MFT and summed up.

$$\frac{dv}{dt}_{LV} = \frac{I_{mLV}}{C_{rLV} + C_{rMV} / N_{xfmr}^2} \quad (19)$$

The LV-side dv/dt can also be derived by (19) to be less than 200 V/ μ s, where I_{mLV} is the MV-side magnetizing current I_{mMV} referred to the LV side of the MFT. Then, the total ZVS transition state duration in Fig. 3 can be calculated using (20) to be 5 μ s.

$$T_{ZVS} = \frac{2V_{MV_pk}}{dv/dt_{MV}} \quad (20)$$

The resonant state duration (T_r) in Fig. 3 is computed to be 4 μ s as given by:

$$T_r = \sqrt{L_{rMV} C_{rMV}} \left(2\pi - \arcsin\left(\frac{I_{mMV} V_{MV_pk} \sqrt{C_{rMV} / L_{rMV}}}{I_{mMV}^2 / 4 + V_{MV_pk}^2 C_{rMV} / L_{rMV}}\right)\right) \quad (21)$$

Equation (21) involves quantities referred to the MV side. The arcsine function in (21) corresponds to a phase angle in the range of $(\frac{\pi}{2}, \pi)$ in this case. During the resonant state in Fig. 3, the LC resonance involves the MV and the LV resonant capacitors connected in parallel through the MFT. Therefore, an accurate calculation is to plug in the average resonant capacitances like in (18) in the position of C_{rMV} in (21). The effective duty cycle can be evaluated in (22) as 86%, which means 14% duty cycle is lost for the ZVS and the controlled dv/dt . The lost duty cycle is less than 15%, which fulfills the second design consideration.

$$D_{eff} = 1 - (T_r + T_{ZVS}) / T_{sw} \quad (22)$$

Under this design of the resonant state duration and the ZVS transition state duration, the switching frequency is not further increased beyond 16 kHz to keep the lost duty cycle less than 15%. The voltage stress (v_{Stress}) across the resonant capacitors due to the resonant operation and MFT leakage inductance can be computed using (23)-(25) [41], where i_{m_vly} is the valley current of the magnetizing current considering the 40% switching ripple.

$$v_{Stress1} = \sqrt{i_{m_vly}^2 L_r / C_r + V_{max}^2} \quad (23)$$

$$v_{Stress2} = \sqrt{\left(\frac{i_{m_vly}}{2}\right)^2 L_r / C_r + \left(V_{max} + \sqrt{i_{m_lkg}^2 L_{lkg} / C_r}\right)^2} \quad (24)$$

$$v_{Stress} = \max(v_{Stress1}, v_{Stress2}) \quad (25)$$

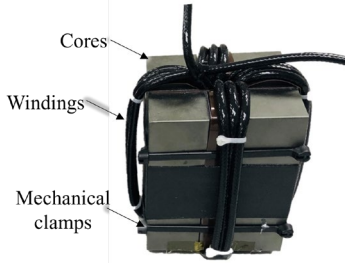


Fig. 8. MV resonant inductor prototype based on ferrite cores and Litz cables. There are two horizontal mechanical clamps and three turns vertically on each side of the core, i.e., 12 turns in total.



Fig. 9. Coaxial Litz cable for the MFT prototype to achieve low leakage and high insulation voltage at the same time.

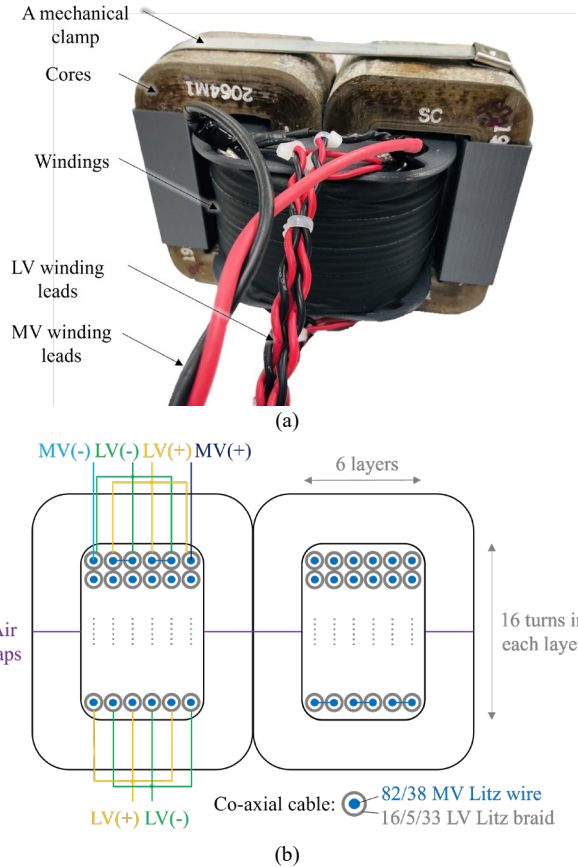


Fig. 10. (a) Photo and (b) cross-section diagram of the nanocrystalline MFT prototype. The prototype has passed 60 kV Hipot test and 55 kV BIL test.

In (23)-(24), V_{\max} corresponds to the maximum port voltage, e.g., 2 kV for the MVAC port. The voltage stress in (25) is within the safe operating region of both the MV and the LV devices, which has also been verified through simulations. Therefore, the third design consideration is fulfilled. When referred to the MV side of the transformer, C_{rMV} is larger than

Table III. Specifications of the MFT design.

| Parameter | Value |
|------------------------|--|
| Operating frequency | 16 kHz |
| Turns ratio | 6:1 |
| Saturation current | 180 A (LV) / 30 A (MV) |
| Magnetizing inductance | $>180 \mu\text{H}$ (L_{mLV}) / $>6.5 \text{ mH}$ (L_{mMV}) |
| Leakage inductance | $< 1.0\%$ of L_m |
| Loss | $< 1.0\%$ |
| Isolation level | 60 kV Hipot and 55 kV BIL |

C_{rLV} . This is because 3.3 kV devices have lower rating and voltage margin than 650 V devices when both referred to the MV side of the transformer.

The MV resonant inductor prototype is shown in Fig. 8. A medium-voltage Litz cable is applied, which consists of 82 strands of American wire gauge (AWG) 33. Four B67345B0002x087 ferrite cores and four B67345B0004x087 ferrite cores are used with 8 distributed air gaps at 0.095 mm length each. 12 turns are required to achieve a saturation current of 60 A and an inductance of 72 μH .

D. Medium-Frequency Transformer

The challenge of the 10 kVA 16 kHz MFT design is to achieve the desired magnetizing inductance (L_m), 55 kV BIL, and a leakage inductance under 1% L_m at the same time. The leakage inductance acts like a parasitic in the current-source SST and should be limited under 1% for safe operation. The specifications of the MFT are summarized in Table III. As discussed in the previous section, L_m is sized to be at least 180 μH when referred to the LV side to keep the peak-to-peak magnetizing current ripple smaller than 40%. The saturation current is chosen as 180 A to reserve some margin with respect to the magnetizing current and the ripple in (14)-(15).

SC2064M1 nanocrystalline cores are used because of the superior low-loss property compared to amorphous cores and the high saturation flux density compared to ferrite cores. A customized coaxial cable in Fig. 9 is applied for the winding of the MFT prototype in Fig. 10. The MV Litz conductor consists of 82 twisted bundles of AWG 33. The LV Litz conductor consists of 16 twisted bundles, where each bundle consists of 5 strands of AWG 33. The insulation between the MV and the LV conductors is Perfluoroalkoxy (PFA) insulation at the thickness of 0.508 mm. The same PFA insulation is applied outside the LV conductor but at the thickness of 0.279 mm. The thickness of the customized PFA insulation layer can always be increased to achieve a higher insulation level. The winding consists of 6 layers with 16 MV turns in each layer as illustrated in the MFT cross-section diagram in Fig. 10 (b). The coaxial cable has a unity turns ratio. For a turns ratio of 6:1, the outer insulation and the LV Litz braid are split at the end of each layer and then connected in parallel. In other words, the LV winding of the 6 layers are connected in parallel as shown in Fig. 10 (b). Concerning the MV winding, note that the MV insulation layer of the coaxial cable in Fig. 9 between the MV and the LV conductors remains undisturbed, and the MV winding of all the 6 layers is equivalently connected in series. This method simplifies the insulation at termination and fulfills the BIL requirement in a simple way. With the designed windings, the peak flux density (B_{pk}) in the core is 1 T.



Fig. 11. 60 kV Hipot test setup and results of the MFT prototype.

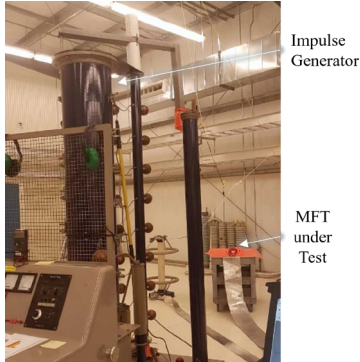


Fig. 12. 55 kV BIL test setup of the MFT prototype.

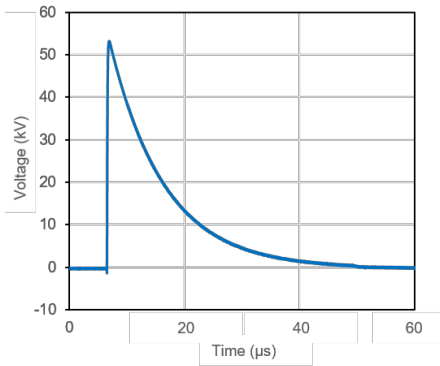


Fig. 13. Experimental waveform of the MFT prototype under 55 kV BIL test.

The DC flux bias from the DC current component of the magnetizing current has been considered, when the 1 T peak flux density is designed.

The core loss of the MFT prototype can be estimated using Steinmetz equation [42]:

$$P_V = k \cdot (f_{sw})^\alpha \cdot \left(\frac{0.5\Delta I_{mMV}}{I_{mMV_dc} + 0.5\Delta I_{mMV}} B_{pk} \right)^\beta \quad (26)$$

where k , α , and β for the nanocrystalline core is 7826.2, 1.62, and 1.98, respectively. The ac resistance factor (F_R) for Litz windings can be computed using (27).

$$F_R = 1 + \frac{(\pi n N)^2 d_s^6}{192 \delta^4 b^2} \quad (27)$$

where N is the number of turns in the Litz winding, n is the number of strands in the Litz cable, d_s is the strand diameter, δ is the skin depth, and b is the winding height. Based on (26)-(27), the core loss and the winding loss of the MFT are estimated to be 30 W and 54 W at 10 kW full power, respectively.

The MFT insulation is verified through a 60 kV high potential (Hi-pot) dielectrics withstand test as shown in Fig. 11. Moreover, the MFT passes 55 kV BIL test with the test setup in

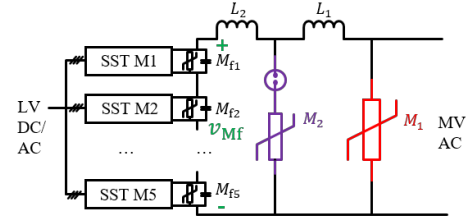


Fig. 14. Lightning protection scheme consisting of two-stage MOVs (M_1 , M_2 , M_f) and air-core inductors (L_1 , L_2) for impulse voltage attenuation.



Fig. 15. Lightning-protection-component test setup. A 90 kV 1.2 μ s/50 μ s impulse generator is connected to the setup.

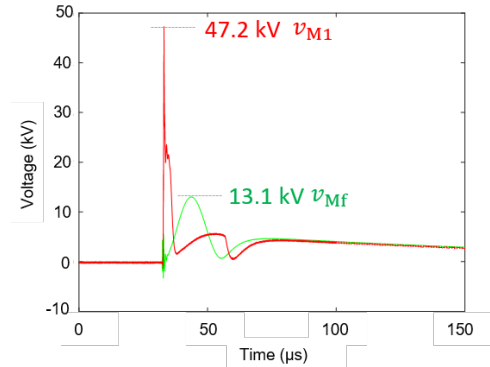


Fig. 16. Experimental waveforms of the lightning impulse test. v_{Mf} is within the safe operating voltage of the SST.

Fig. 12 and an experimental waveform in Fig. 13, where no breakdown exists in the waveform under 1.2/50 μ s impulse. L_m is measured to be 192 μ H at 150 A and 159 μ H at 180 A due to soft saturation, and the leakage inductance is measured to be 181.5 nH (both referred to the LV side). Therefore, the leakage inductance at 0.09% of the magnetizing inductance and 55 kV BIL between the MV and the LV windings are achieved simultaneously. Other aspects of the insulation of the MFT and the coaxial cable including degradation and lifetime, partial discharge, and the impact of high-frequency switching are worth further exploration in future work.

E. Lightning Protection Scheme

One critical challenge for direct grid-connected converters is to withstand the lightning impulse, which is 90 kV for this SST prototype. Conventional high-voltage DC (HVDC) converters and MV drive converters are connected to the grid through LFT. The LFT protects the HVDC converters and MV drive

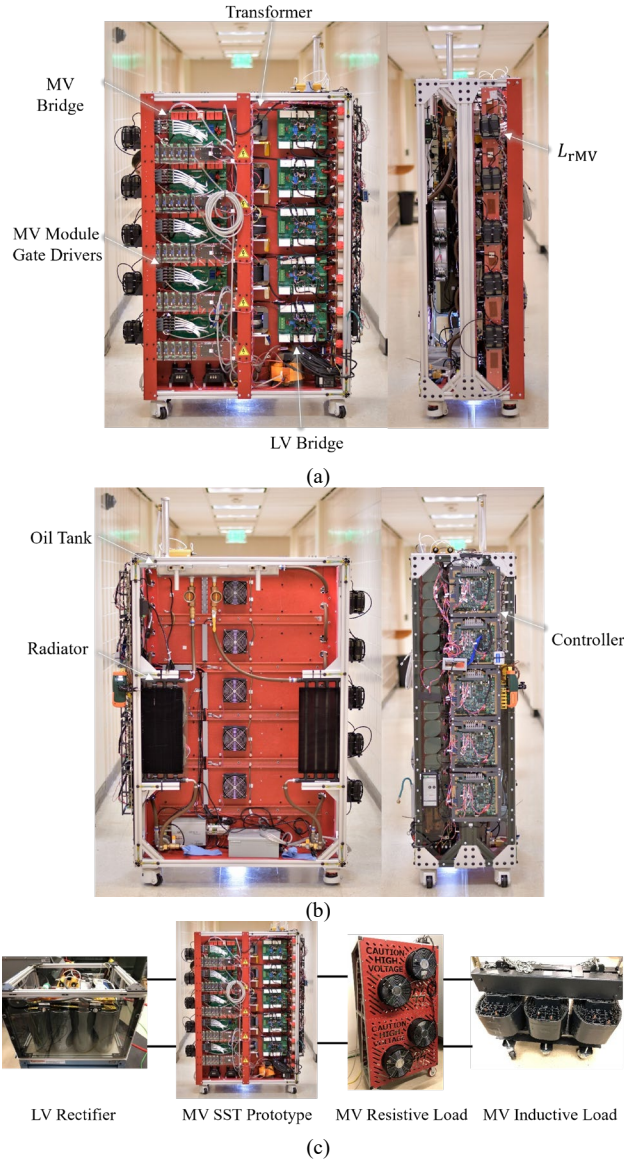


Fig. 17. (a)-(b) 7.2 kV/350 V 50 kVA oil-cooled three-port modular single-stage current-source SST prototype. Size: 58 inches by 40 inches by 8 inches, excluding cooling. (c) Experimental setup under LV-source-to-MV-load power flow direction.

converters from lightning impulse. The existing BIL standard tests the insulation of the LFT with all the voltage-clamping protection components, e.g., metal oxide varistor (MOV), and the converter disconnected. If there is no breakdown in the measured voltage waveforms of 1.2/50 μ s 90 kV impulse, the LFT is deemed passing for the test. Unfortunately, the same principle cannot be directly applied to the direct grid-connected converters such as the SST. First, without any protective MOVs or filters, the semiconductors for sure cannot survive a surge voltage as high as 90 kV. Second, the protective MOVs and filters can load the impulse generator and absorb energy, which results in clamped voltages in the waveforms instead of 1.2/50 μ s 90 kV impulse in the LFT test. Besides the challenge of the incompatibility between the BIL standard tests and the SST, another challenge lies in the mismatch between the clamping voltage of the MOV and the insulation strength of the SST. In

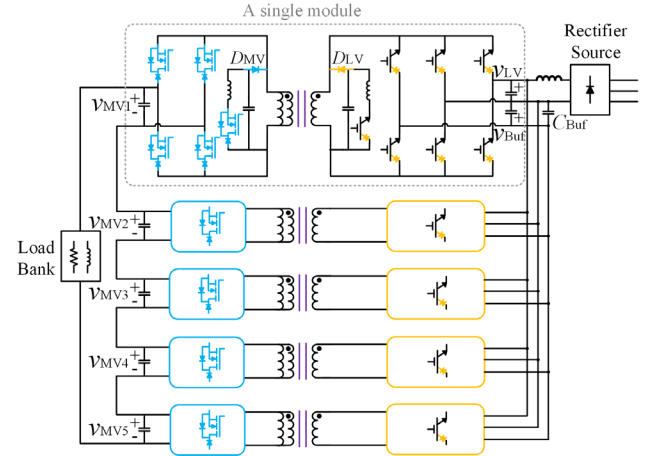


Fig. 18. Schematic of the proposed three-port modular single-stage current-source SST test setup. Single module can also be tested with the other modules bypassed.

other words, when a standard ungapped MOV is applied, the clamping voltage of the MOV exceeds the voltage level that the semiconductors inside the SST can withstand.

To address the lightning protection challenge, a two-stage lightning protection scheme is thereby proposed and the 90 kV BIL test is deemed passing if the clamped voltages are well within the voltage that the SST can stand, e.g., 15 kV for this five-module 3.3 kV-device-based SST. In Fig. 14, the two-stage protection scheme consists of MOVs (M_1 , M_2 , M_f) and inductors (L_1 , L_2). M_1 is a 15 kV Eaton UltraSIL gapped MOV, where the 15 kV rating is sufficient for 10 kV peak grid voltage. M_2 is a 3 kV Eaton UltraSIL gapped MOV. There are two reasons for selecting this gapped MOV. The first reason is that the sparkover voltage has been tested to be 12 kV, which is higher than the peak grid voltage of 10 kV. The second reason is that this MOV has a discharge voltage of 11.6 kV for 20 kA and 13.5 kV for 40 kA, which can protect the voltages imposed on the SST to be less than 15 kV. M_f is V172BB60 from Littelfuse to achieve one additional layer of protection for each module. The filter capacitor of each module is carefully selected from the same batch of the manufacturer to ensure similar capacitances. The inductors L_1 and L_2 are wound by 30 kV cable and based on air cores to avoid saturation at high surge currents. The inductances are selected to be 150 μ H to make the current sharing between M_1 and M_2 proportional to their respective energy absorption capability. Then, the lower-rated M_2 discharges a lower current than the higher-rated M_1 and the lifetime expectancy of M_2 is preserved. These inductors have some line-filtering capability but are mainly for the lightning protection purpose due to the relatively small inductance.

The testing setup is shown in Fig. 15, while the experimental waveform is illustrated in Fig. 16. Once the impulse generator is tuned to generate 1.2/50 μ s 90 kV impulse, the lightning protection components are connected at the output of the impulse generator. It can be observed that the voltage peak across M_1 is limited to 47.2 kV in Fig. 16, because of the discharge current from M_1 . Moreover, the voltage v_{Mf} has a peak voltage level of 13.1 kV, which falls within the safe operating voltage range of this SST prototype based on five ISOP 3.3-kV-device-base modules. The components in the proposed lightning

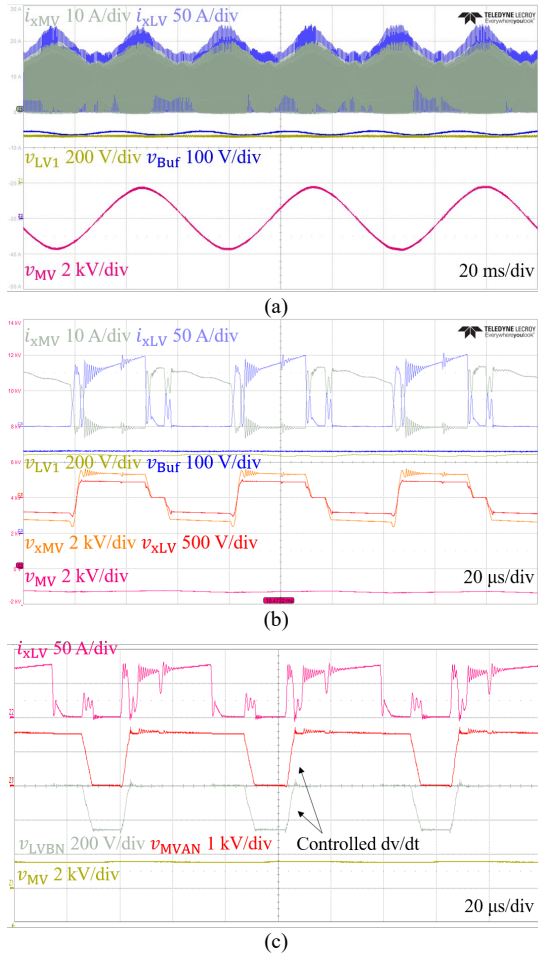


Fig. 19. (a) Single-module steady-state waveforms of the three-port current-source SST prototype at 2 kV peak 6 kW and (b) zoom-in waveforms. (c) Device voltage measurements to show the controlled dv/dt .

protection scheme have been modeled to simulate the proposed scheme, where the simulation results match experimental measurements [43]. Using the simulation model, the proposed lightning protection scheme has also been verified to pass 250/2500 μ s switching impulse test.

IV. EXPERIMENTAL PROTOTYPES AND RESULTS

A 7.2 kV 50 kVA SST experimental prototype consisting of five 1.44 kV 10 kVA modules is implemented as shown in Fig. 17 (a)-(b). The SST prototype is forced oil cooled. Two sets of oil tubes interconnect the heatsinks of the MV and the LV device modules with an oil tank and two radiators to dissipate the device power loss. An oil pump actively circulates the oil in the system. Each SST module has its own distributed controller receiving synchronization signals from a master controller to synchronize the MV voltage phase angles for voltage balancing and the switching cycle for interleaved operation. The schematic of the experimental setup is depicted in Fig. 18 under LV-to-MV power flow condition. In Fig. 18, each SST module has its own filter capacitors and input and output terminals. The MV terminals are connected in series, while the LV terminal and the buffer terminal are connected in parallel onto two copper busbars. C_{Buf} is coupled to the buffer port's busbar and implemented by fourteen paralleled 380 μ F capacitors in Fig. 17

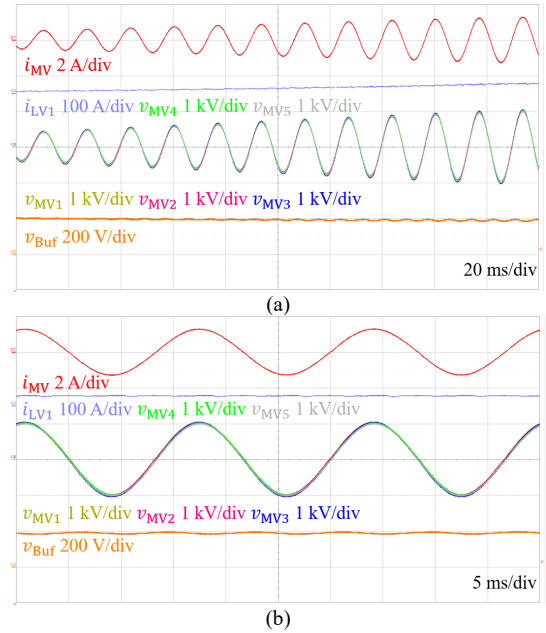


Fig. 20. Five-module waveforms of the three-port current-source SST prototype at light load, i.e., 5 kV peak 3.5 kVA under (a) voltage ramp up and (b) steady state.

(a) for the modular SST prototype. The experimental setup to test the SST with a rectifier as LV source and a resistor load bank as MV load are shown in Fig. 17 (c). The MV inductor in Fig. 17 (c) can be connected in parallel with the resistive load to demonstrate reactive power operation in addition to active power operation. Finally, special measures have been taken to achieve safe operation when the MV output of the SST is grounded during the test [44].

Fig. 19 (a)-(b) illustrates single-module steady-state waveforms of the three-port current-source SST prototype at 2 kV peak 6 kW. The line-cycle waveforms in Fig. 19 (a) verify the smooth MV voltage v_{MV} with low distortions. The buffer capacitor absorbs 120 Hz power ripple with 120 Hz voltage ripple in v_{Buf} . The switching-cycle waveform in Fig. 19 (b) illustrates the switching operation of the SST, i.e., transformer voltages v_{xMV} and v_{xLV} are alternating between positive and negative voltage levels similar to Fig. 2 (a) to transfer power among the three ports. Fig. 19 (c) shows the device voltage measurements in the SST, where the controlled dv/dt less than 800 V/ μ s is verified. In Fig. 19 (c), the ringing on the LV MFT winding current (i_{xLV}) is due to the resonance between the parasitic capacitance across the leakage diode (D_{LV}) and the MFT leakage inductance. With the resonant capacitors (C_{rMV} and C_{rLV}), there is almost no ringing on the device voltages.

Fig. 20 illustrates the five-module waveforms at light load, i.e., 5 kV peak 3.5 kVA. In Fig. 20 (a), smooth voltage ramp-up towards the steady-state 5 kV operating point can be observed, where the five module voltages (v_{MV1} - v_{MV5}) are balanced and sinusoidal. In Fig. 20 (b), the steady-state line-cycle waveforms show balanced voltages (v_{MV1} - v_{MV5}) with low distortion and sinusoidal MV load current (i_{MV}) at a light load.

In Fig. 21, the five-module waveforms of the SST prototype at 7.5 kV peak 8 kW are illustrated. Fig. 21 (a) shows smooth and balanced voltages (v_{MV1} - v_{MV5}) during voltage ramp-up. In

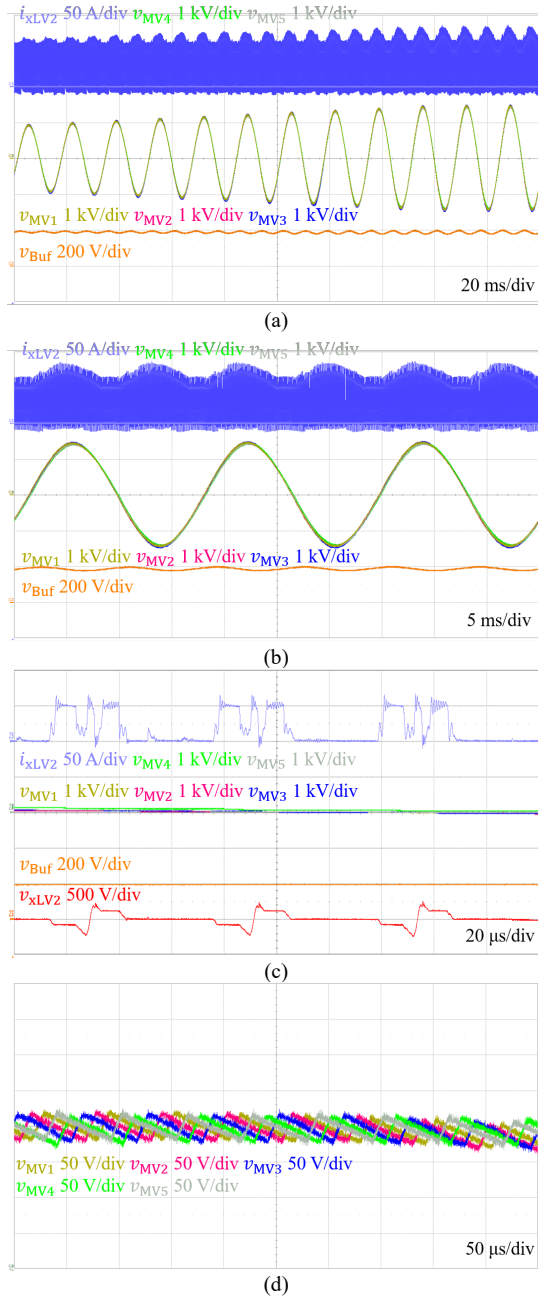


Fig. 21. Five-module waveforms of the three-port current-source SST prototype at 7.5 kV peak 8 kW at the time scales of (a) voltage ramp up, (b) steady-state line cycles, (c) switching cycles. (d) MVAC voltage-ripple zoom-in waveforms to illustrate interleaved operation.

Fig. 21, the buffer capacitor absorbs 120 Hz power ripple, and the 120 Hz voltage ripple exists in v_{Buf} . Fig. 21 (b) confirms the line-cycle operations of balanced voltages (v_{MV1} - v_{MV5}) with low distortion. Fig. 21 (c) further verifies the switching-cycle operation of module two at the zero-crossing of the MV grid. The waveforms are different from the switching-cycle waveforms at nearly the peak of the MV grid in Fig. 19 (b). Note that in Fig. 21 (c), there are still three vectors for power conversion among the three ports similar to Fig. 2 (a), as the MV vector actually corresponds to a voltage level close to zero in v_{xLV2} trace. Importantly, the interleaved operation of the five

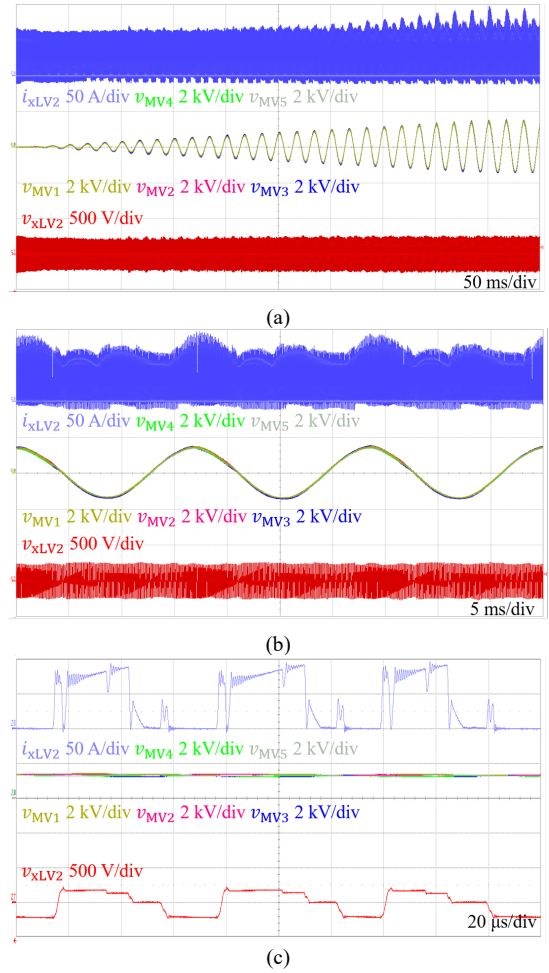


Fig. 22. Five-module waveforms of the three-port current-source SST prototype at 7.5 kV peak 20 kVA at the time scales of (a) voltage ramp up, (b) steady-state line cycles, (c) switching cycles.

modules can be clearly observed in the MV voltage-ripple measurements (v_{MV1} - v_{MV5}) in Fig. 21 (d). Each module's switching signal is displaced by 72° with respect to each other to minimize the switching ripple.

In Fig. 22, both the MV inductive load and the MV resistor load bank in Fig. 17 (c) are coupled to the MV grid formed by the SST prototype to test the reactive power operation, while only the resistive load bank is connected in Figs. 19-21. The waveforms in Fig. 22 are at 7.5 kV peak 20 kVA. In Fig. 22 (a)-(b), smooth and balanced MV voltages (v_{MV1} - v_{MV5}) can be observed during the ramp-up and the steady state. Furthermore, v_{xLV2} and its envelope verify that the voltage stress across the transformer is within the 650 V device voltage rating. As Figs. 19 (b) and 21 (c) have shown the switching-cycle operation under single-module AC peak and five-module AC zero crossing, Fig. 22 (c) verifies the switching-cycle operation at five-module AC peak, similar to Fig. 2 (a).

The dynamic results of the SST prototype are shown in Fig. 23 under five-module voltage step change from 1.5 kV to 4 kV peak. It can be observed that even during the step change, the MV voltages (v_{MV1} - v_{MV5}) are balanced. The MV voltages settle down fast to their reference values in less than 0.5 ms. Furthermore, only minor transients can be observed on the

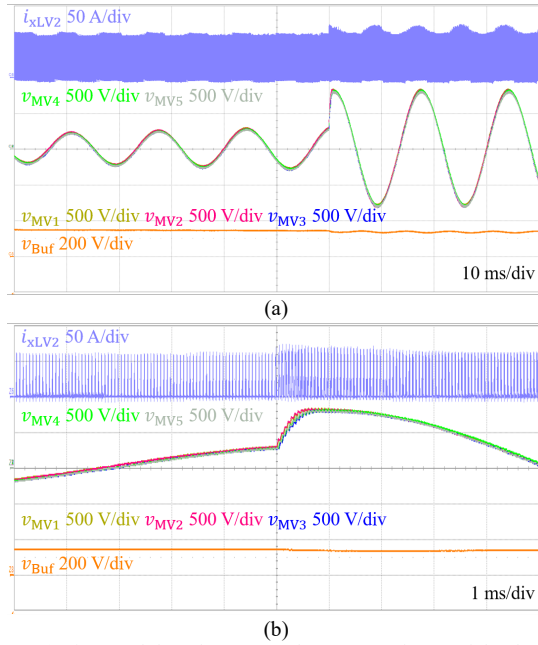


Fig. 23. (a) Five-module voltage step-change waveforms of the three-port SST prototype from 1.5 kV peak to 4 kV peak and (b) zoom-in waveforms.

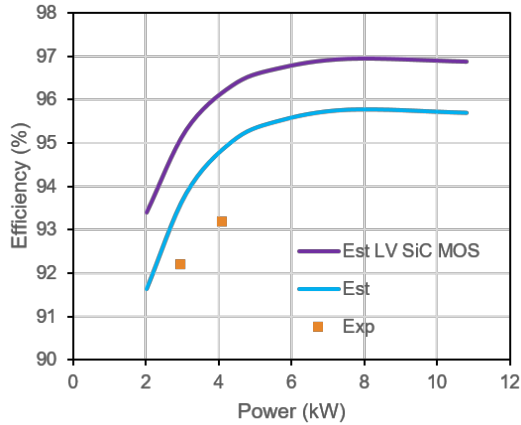


Fig. 24. Efficiency estimation and experimental measurement of a 10 kVA SST module in the prototype.

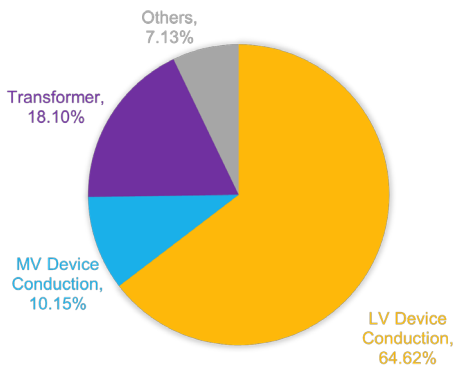


Fig. 25. Estimated loss breakdown at single-module 10 kVA power.

magnetizing current or the transformer LV-winding current (i_{xLV2}).

The measured and the estimated efficiency of one 10 kVA converter module are portrayed in Fig. 24. The estimated peak efficiency is close to 96%. The efficiency is mainly limited by 650 V discrete device conduction loss, which accounts for about 65% of the total loss, as shown in the loss breakdown estimation in Fig. 25. In future research, SiC MOSFETs can replace the Si IGBTs IKW75N65EL5 in this prototype to further improve the efficiency. Moreover, more discrete devices can be paralleled to reduce the conduction drop. For example, replacing the 650 V IGBT with SiC MOSFETs MSC015SMA070B and paralleling four SiC devices in each device position will improve the peak efficiency to about 97% in Fig. 24. When high-current low-voltage SiC reverse-blocking modules are available in the future, the low-voltage-side conduction loss can be significantly reduced. Efficiency higher than 97% can be achieved with the high-current SiC reverse-blocking modules or more discrete paralleled devices.

V. CONCLUSION

A multiport modular single-stage current-source SST is proposed in this article. The SST is suitable for applications including renewable energy integration, data center, electric vehicle fast charging, etc. The following unique features of the proposed SST have been verified experimentally.

- 1) A 7.2 kV oil-cooled prototype with five ISOP SST modules based on 3.3 kV SiC reverse-blocking modules have been built and tested up to 7.5 kV peak under steady-state and dynamic conditions. It is the first time that the experimental results of an MV AC current-source SST are reported. To the authors' best knowledge, there are no MV AC current-source SST results in the literature.
- 2) An active-power-decoupling buffer port, leveraging multiport structure, is for the first time applied in MV converters to enable a reduced DC link and electrolytic capacitor-less SST with high reliability. The volume reduction is 53.8% for the implemented SST prototype.
- 3) A direct grid-connected converter such as the SST does not have LFT. Special attention must be paid to insulation and protection, and the conventional BIL standard cannot be directly applied. An MFT prototype has been built which passes 55 kV BIL and 60 kV Hipot test with only 0.09% leakage inductance. Importantly, a lightning protection scheme has been presented and verified to protect the SST from 90 kV BIL impulse.

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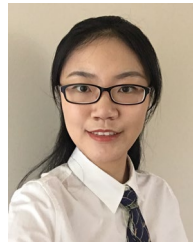
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