

**ENGINEERING A SELF-ALIGNED METAL-OXIDE-  
SEMICONDUCTOR GATE STACK FOR NANO-MODULAR  
DEVICE FABRICATION**

A Dissertation  
Presented to  
The Academic Faculty

by

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In Partial Fulfillment  
of the Requirements for the Degree  
Doctor of Philosophy in the  
School of Materials Science and Engineering

Georgia Institute of Technology  
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DEVICE FABRICATION**

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Never be so kind, you forget to be clever

Never be so clever, you forget to be kind

— Taylor Swift, *marjorie*

To my family and Ginny for their endless support

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## LIST OF SYMBOLS AND ABBREVIATIONS

A	Area
AC	Alternating current
ALD	Atomic layer deposition
AS-ALD	Area-selective atomic layer deposition
ATRP	Atom transfer radical polymerization
BEOL	Back end of line
BIBB	Bromoisobutyryl bromide
BOE	Buffered oxide etch
BPY	2,2'-bipyridine
C	Capacitance
CMOS	Complementary metal-oxide-semiconductor
$C_{ox}$	Oxide capacitance
$C_s$	Semiconductor capacitance
C-V	Capacitance-voltage
CVD	Chemical vapor deposition
$D_{it}$	Interface state density
DI H <sub>2</sub> O	Deionized water
DMF	Dimethylformamide
EDS	Energy dispersive X-ray spectroscopy
$f$	Frequency
FET	Field-effect transistor
G	Conductance

$G_p$	Parallel conductance
GPC	Growth per cycle
G-V	Conductance-voltage
IC	Integrated circuit
IEN	Institute for Electronics and Nanotechnology
IPA	Isopropyl alcohol
I-V	Current-voltage
MeCpPtMe <sub>3</sub>	Trimethyl(methylcyclopentadienyl)platinum(IV)
MLA	Maskless aligner
MMA	Methyl methacrylate
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
NW	Nanowire
ODTS	Octadecyltrichlorosilane
PE-ALD	Plasma-enhanced atomic layer deposition
PMMA	Poly(methyl methacrylate)
$q$	Charge of an electron
$R_s$	Series resistance
SAM	Self-assembled monolayer
SC-1	Standard clean 1 (part of RCA clean)
SC-2	Standard clean 2 (part of RCA clean)
SCALES	Selective coaxial lithography via etching of surfaces
SCCM	Standard cubic centimeters per minute
SEM	Scanning electron microscopy

$t$	Film thickness
TDMAHf	Tetrakis(dimethylamido)hafnium
TDMAT	Tetrakis(dimethylamido)titanium
TDMAZr	Tetrakis(dimethylamido)zirconium
TEM	Transmission electron microscopy
TMA	Trimethylaluminum
UV	Ultraviolet
$V_{FB}$	Flatband voltage
VLS	Vapor-liquid-solid
$V_T$	Threshold voltage
XPS	X-ray photoelectron spectroscopy
$\epsilon_0$	Permittivity of free space
$\epsilon_r$	Relative permittivity
$\tau$	Time constant
$\omega$	Angular frequency

## SUMMARY

Conventional integrated circuit technology has made great strides over the past 50 years and today can produce integrated circuits (ICs) with billions of nanoscale transistors. However, much of today's state-of-the-art semiconductor research focuses on technological improvements and advancements for manufacturing within the already established IC fabrication framework. The planar process for IC manufacturing involves hundreds of precise processing steps to fabricate monolithic ICs, and the development of new chip designs is an expensive and long process, which can limit process and product innovation. But what if electronics fabrication could be a more dynamic and customizable process that could still manufacture are large scales? By shifting the fabrication paradigm and embracing scalable, bottom-up manufacturing techniques, fully formed high-performance transistors can be produced and interconnected for low-cost fabrication of customizable circuitry. For example, high-performance modular nanowire transistors can be synthesized using bulk processing methods. The pre-fabricated devices can be deposited on a substrate, and metal interconnects can be adaptively printed to form circuits.

This work focuses on developing a self-aligned gate stack that would enable the production of bottom-up nanowire electronic devices and on understanding how material deposition and post-processing impacts performance of the devices. A polymer masking material is used to pattern dopant-modulated silicon (Si) nanowires. This enables the selective deposition of a high- $\kappa$  dielectric and a metal electrode via atomic layer deposition (ALD) to form a metal-oxide-semiconductor (MOS) gate stack around the channel region of the nanowire. This final structure is a functional, nano-modular field-effect transistor device that can be interconnected with other devices to form circuits.

In the first part of this work, we develop the techniques and investigate the materials needed to fabricate the self-aligned gate stack. The polymer patterning process, referred to as Selective Co-Axial Lithography via Etching of Surfaces (SCALES), has been previously demonstrated by the group on semiconductor nanowires. This work adapts the SCALES process for planar Si substrates to enable the use of characterization techniques that require samples larger than a nanowire. With the planar SCALES process, a polymer film is synthesized across the entire surface of a planar, dopant-modulated substrate and then selectively etched with potassium hydroxide. Polymer remains attached to the heavily boron-doped regions, resulting in a polymer mask aligned to the dopant pattern of the underlying substrate. This patterned polymer mask enables the use of area-selective atomic layer deposition (AS-ALD) to deposit the high- $\kappa$  dielectric and metal electrode. The selectivity of deposition is investigated for a variety of oxides and metals via AS-ALD, and ultimately hafnium oxide and platinum are determined to be the optimal materials system.

The second part of this work focuses on fabricating and optimizing the self-aligned gate stack. We first demonstrate the successful deposition of a complete MOS gate stack by selectively depositing Pt on top of HfO<sub>2</sub> on a boron-patterned Si substrate. The resulting structures are MOS capacitors that are characterized electronically to investigate how the selective deposition and post-deposition anneal impacts device performance. The quality of the oxide-semiconductor interface is particularly important for MOS device performance, so the HfO<sub>2</sub>-Si interface is investigated in detail by examining different SiO<sub>2</sub> interlayer formation techniques. Physical characterization is used to understand the relationship between the interlayer formation and electrical performance. In summary, this work develops a self-aligned gate stack fabrication process and investigates the impact of

processing on the electrical performance of the materials. And this self-aligned gate stack deposition process provides a pathway towards fabricating modular nanowire transistors.

# CHAPTER 1. INTRODUCTION

The electronics manufacturing industry has been engineering increasingly complex integrated circuits (ICs) for over 50 years. With every new technological advancement in the electronics field comes new and exciting applications. However, much of today's state-of-the-art semiconductor research focuses on improving device technology and developing new techniques that all fit within the already established fabrication framework for monolithic ICs (i.e., fabricating complete, complex circuitry on planar silicon wafers). IC manufacturing involves a complex planar process, with hundreds of steps to pattern, deposit and etch away material, resulting in complete IC chips. But if we broaden the scope of semiconductor fabrication and consider alternate approaches, the door could be opened to a number of new potential applications, ranging from on-demand printable ICs to pharmanronics which integrates electronics with pharmaceuticals to large dispersible sensor networks with a centralized computing hub. By applying a combination of materials science and chemical engineering perspectives to electronics fabrication, pre-formed, modular electronic devices can be fabricated using bottom-up processing techniques to enable customizable electronics manufacturing at a very large scale.

## 1.1 Modular Device Approach to Circuit Fabrication

This modular device approach combines bottom-up device synthesis with adaptive printing of interconnections to enable a more flexible style of circuit fabrication and reduce process complexity. High-quality, single crystalline silicon (Si) nanowires are used to fabricate the modular electronic devices via bottom-up bulk processing methods. This enables manufacturing of very large quantities of devices that can be suspended in solution

to produce a “transistor ink,” similar to colloidal nanoparticle inks. Transistors are then deposited on a substrate and optically imaged to identify the device locations. Metallic interconnections can be printed between devices to form circuits via inkjet or electrohydrodynamic jet printing of metal nanoparticle inks (e.g., Ag or Pt nanoparticle inks). The process flow is depicted in Figure 1.1. This approach would enable circuit fabrication on alternative substrates such as large area flexible surfaces and enable customizable circuit production since the circuitry can be designed after the device fabrication.

To produce a “transistor ink,” a very large quantity of modular devices is required. Production scale can be increased by leveraging large-scale bottom-up syntheses and continuous processes to fabricate the modular devices similar to manufacturing of chemicals and pharmaceuticals.<sup>2</sup> Each step of this alternate transistor fabrication approach (i.e., nanowire growth, polymer synthesis, selective polymer removal, selective gate stack deposition) can be executed in bulk solution-based or vapor-phase manufacturing processes that enable very high throughput manufacturing.

Traditional IC fabrication uses photolithography to pattern critical device features and interconnects, but it would limit the scalability of fabricating three-dimensional nanostructures. While photolithography can achieve very small feature sizes, it is expensive, requires distinct masks for every circuit design, and is particularly designed for patterning planar surfaces. New masks are required for every new circuit design, making custom circuit design expensive and more time consuming. Photolithography cannot easily be used to pattern the surface of three-dimensional structures, which is needed to pattern a conformal gate around a nanowire. This modular device approach eliminates the need for

photolithography to pattern device features by instead using a bottom-up selective patterning technique that depends on the chemical composition of the nanowire encoded during synthesis.

In addition to enabling patterning of sub-micron channel lengths without photolithography, the use of high-quality (single-crystalline) nanomaterials to fabricate the modular transistors permits good device characteristics (i.e., high mobility). Related electronics fabrication techniques (e.g., printed ICs) are already well-researched, but many of the electronics created with those technologies lack high-performance due to the use of solution-based organic materials, specifically organic semiconductors.<sup>3</sup> The decoupling of device synthesis from device interconnection with this modular approach allows the customizable printed circuits to maintain high performance. While these circuits may not equal the current state-of-the-art level of performance of conventional ICs due to lower device density and less complex interconnection, they can still function as high-performance electronics to enable alternative applications, such as on-demand IC prototyping and large-scale manufacturing of flexible electronics. However, fabricating and understanding these nanomaterial devices will require addressing several materials-based challenges that are discussed in this work.

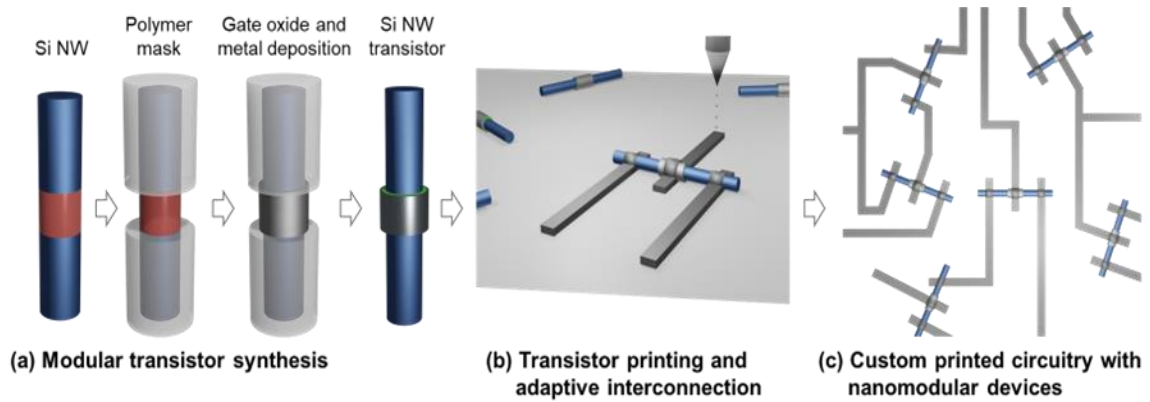


Figure 1.1. Schematic illustration of nanowire transistor fabrication and adaptive circuit printing.

## 1.2 Prototypical Nanowire Transistor Device

The general framework of this modular device approach can be applied to fabricate a variety of electronic device structures using semiconductor nanowires (e.g., resistors, diodes, transistors, etc.). This work, however, focuses in particular on the fabrication of a metal-oxide-semiconductor field-effect transistor (MOSFET) made with a Si nanowire as an initial device prototype. High-performance bottom-up transistor devices can be fabricated with Si nanowires by selectively depositing a wrap-around gate stack with atomic layer deposition (ALD). A single-crystalline nanowire is grown with dopant-modulated segments which then allows for selective patterning of a polymer mask that passivates the source and drain segments. This selective patterning process, which is referred to as selective coaxial lithography via etching of surfaces (or SCALES),<sup>4</sup> enables patterning of the transistor gate stack without using photolithography, which is the limiting fabrication step in terms of production scale and customization of circuit design. A high- $\kappa$  dielectric film and subsequent metal film can then be deposited selectively via area-selective ALD (AS-ALD) to form the gate stack around the channel, ultimately forming a

bottom-up MOSFET. The modular nanowire transistor process flow is shown in Figure 1.2.

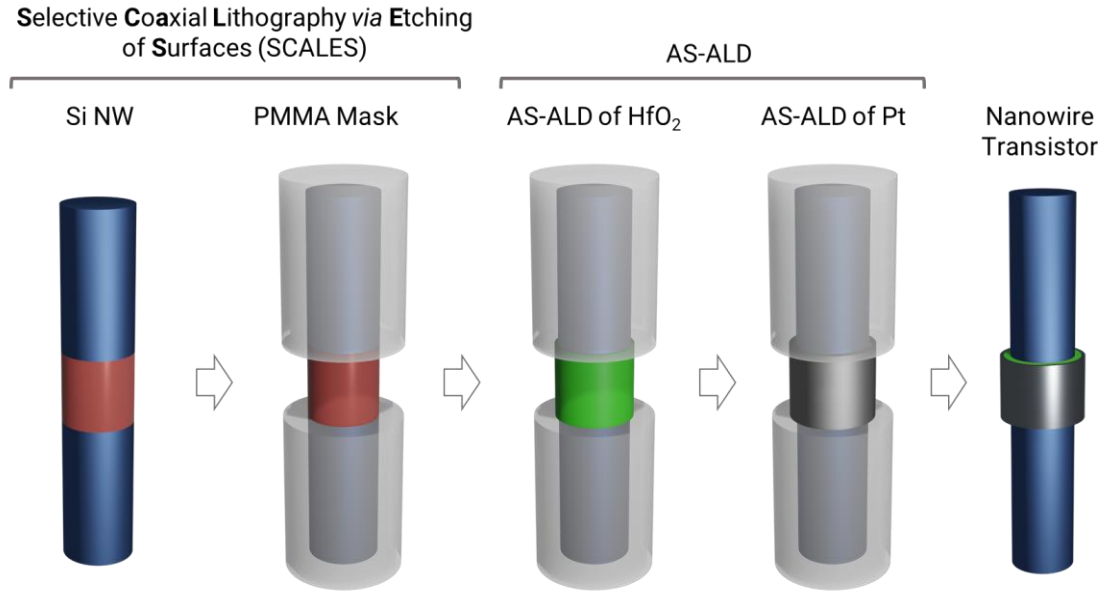


Figure 1.2. Modular transistor process flow schematic showing SCALES patterning combined with AS-ALD of  $\text{HfO}_2$  and Pt to fabricate a modular transistor device from a Si nanowire.

### 1.3 Nanowire Growth

To facilitate a bottom-up fabrication process, this modular device approach begins with the vapor-liquid-solid (VLS) growth mechanism to synthesize silicon nanowires. Semiconductor nanowires can be grown with a variety of processes, but the VLS process enables the modulation of composition along the length of the wire<sup>5</sup> which permits encoding of the source/channel/drain segments with different dopant concentrations. The VLS mechanism (depicted in Figure 1.3) is a bottom-up growth process in which a metal catalyst particle is heated to above its eutectic point to form a liquid droplet alloy consisting

of metal and semiconductor atoms. Gold catalyst particles are commonly used to grow silicon nanowires because of the relatively low-temperature eutectic point for an Au-Si alloy at 363 °C.<sup>6</sup> A semiconductor precursor gas, such as silane ( $\text{SiH}_4$ ) or germane ( $\text{GeH}_4$ ), is flowed over a catalyst-covered substrate, and the semiconductor atoms diffuse into the liquid droplet. Once supersaturation is reached, a semiconductor solid precipitates from the liquid droplet, forming a crystal layer-by-layer with a diameter about the same size as the catalyst droplet. As long as the temperature is maintained to keep the alloyed catalyst droplet liquid and new semiconductor gas is supplied, the semiconductor nanowire will continue to grow in length. The resulting material is a cylindrical, single-crystalline semiconductor “nanowire” that will have a range of crystal-orientation facets along the side-walls.<sup>7</sup> This high-quality, single-crystalline material enables good electronic characteristics for the bottom-up transistors. And dopant atoms can be introduced into the nanowire to modify the electronic properties by flowing dopant gases [e.g. diborane ( $\text{B}_2\text{H}_6$ ) for p-type and phosphine ( $\text{PH}_3$ ) for n-type doping] during nanowire growth.<sup>6</sup> Hydrochloric gas is flowed concurrently to passivate the nanowire side walls. This process is discussed in great detail in earlier work from the Filler group.<sup>8-13</sup>

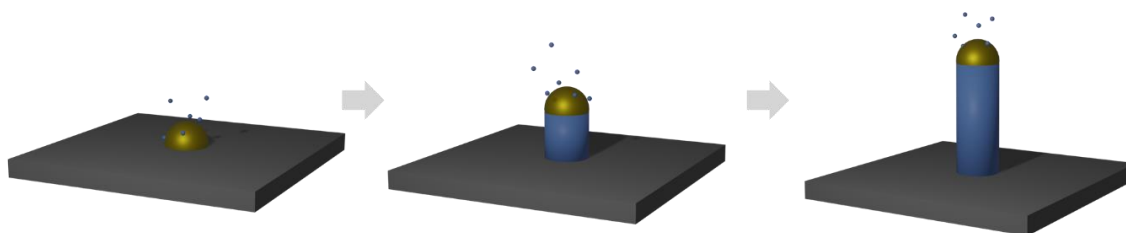


Figure 1.3. Schematic illustration of the vapor-liquid-solid (VLS) mechanism using a gold nanoparticle as a catalyst to grow a silicon nanowire with silane (blue spheres).

## 1.4 Atomic Layer Deposition

Atomic layer deposition (ALD) is a vapor phase deposition technique used to deposit thin films of material across a surface. ALD can form high-quality films with good uniformity and conformality and with very precise thickness control due to its layer-by-layer growth mechanism.<sup>14</sup> ALD processes typically involve self-limiting surface reactions in which vapor-phase precursors are pulsed into a heated chamber holding the substrate, followed by a purge step. This continues in alternating cycles with typically two precursor (reactant) gases until the desired thickness is reached. For example, as illustrated in Figure 1.4, precursor A is first pulsed in, and the molecules react with the surface, forming a monolayer of coverage. The purge step removes excess gas molecules from the chamber. Precursor B is then pulsed in, and it reacts with the layer of adsorbed A molecules on the surface, building up the first layer of the deposited material. After another purge step, the process is repeated with precursor A.<sup>15</sup>

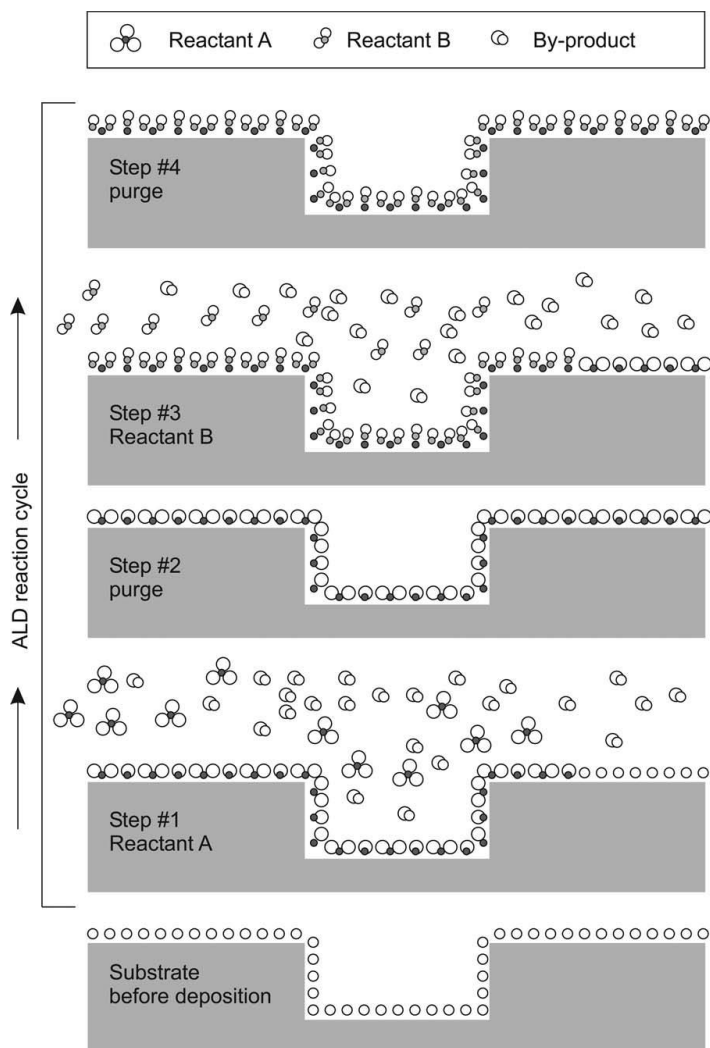


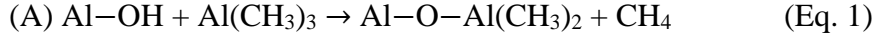
Figure 1.4. Schematic of ALD reaction cycle illustrating self-limiting reactions and purge steps [15]. Reprinted from R. L. Puurunen, *J. Appl. Phys.* 97, 9 (2005), with permission from AIP Publishing.

ALD processes are broadly studied in the literature, and a very wide variety of ALD processes have been developed to deposit many different materials, ranging from oxides (e.g.  $\text{Al}_2\text{O}_3$ <sup>15-17</sup>,  $\text{HfO}_2$ <sup>18-20</sup>,  $\text{TiO}_2$ <sup>21,22</sup>) and nitrides (e.g.  $\text{TiN}$ <sup>23,24</sup>,  $\text{Si}_3\text{N}_4$ <sup>25</sup>), to metals (e.g.  $\text{Ni}$ <sup>26</sup>,  $\text{Pt}$ <sup>27,28</sup>,  $\text{W}$ <sup>29,30</sup>) and semiconductors (e.g.  $\text{Si}$ <sup>31</sup>,  $\text{Ge}$ <sup>32</sup>) – and those are merely a few examples. Halides, such as  $\text{TiCl}_4$  and  $\text{HfCl}_4$ , are commonly used as ALD precursors and

are popular because they are thermally stable, highly-reactive, and widely available for many metals.<sup>15</sup> Halides, however, produce corrosive byproducts (e.g. HCl, HBr) that can etch the chamber as well as the deposited film. Organometallic precursors, such as alkyl compounds and cyclopentadienyl compounds, are also popular because of their high reactivity due to the very reactive carbon-metal bond.<sup>15</sup> These metalorganic precursors, in addition to commonly used alkylamide precursors, do not produce corrosive by-products but can generally decompose at lower temperatures.<sup>15,33</sup> The process temperature for these precursors therefore is typically lower than that for halide precursors.<sup>15</sup> ALD films deposited with metalorganic precursors often contain a small amount of excess carbon, hydrogen, and nitrogen due to contamination from the ligand groups.

The second precursor, typically the non-metal one, will vary based on the type of material being deposited and the reactivity of the first precursor. For oxides, water is the most common option for an oxygen source. Ozone and hydrogen peroxide have been used as a more reactive oxidizing species for precursors that do not react with water.<sup>34</sup> Molecular oxygen and oxygen plasma have also been used.<sup>35</sup> For nitride films, ammonia and nitrogen plasma are the most common nitrogen sources.<sup>36,37</sup> To deposit metal films, like Ru or Pt, a non-metal precursor like oxygen may be used to oxidatively decompose a organometallic compound to remove the ligands.<sup>38,39</sup>

A typical binary ALD process involves two half-reactions on the surface to form the layers of the film. As an example, the following is a one reaction scheme for the synthesis of Al<sub>2</sub>O<sub>3</sub> using trimethylaluminum (TMA) and H<sub>2</sub>O precursors<sup>40</sup>:



Between each half-reaction, the surface functionality alternates between either hydroxyl-terminated or methyl-terminated. The reactions are “self-limiting” because they terminate once all surface sites are occupied, meaning a monolayer (or less) has been deposited.<sup>41</sup> Because the ALD process relies on surface reactions, surface treatments of the substrate can also have an impact on deposition, particularly when comparing hydrogen-terminated Si and hydroxyl-terminated SiO<sub>2</sub>.<sup>42-44</sup> This is particularly important for electronics applications where the interface between ALD films and the silicon surface significantly impacts the performance.

In addition to the precursor chemistry and reaction mechanisms, there are a variety of other factors that also impact the film deposition, including activation energy source (i.e., thermal or plasma-enhanced), process temperature, pulse time, and purge time. For the surface reactions to occur, an activation energy needs to be supplied, typically in the form of heat. Thermal ALD involves simply heating the substrate, providing energy to allow the surface reactions to occur. For less reactive precursors, deposition of single-element films, or processes that require very low temperatures (<200 °C), plasma-enhanced ALD (PE-ALD) can be used. PE-ALD utilizes a remote plasma source that provides extra radicals to induce the reactions.<sup>14</sup> The pulse time and purge times must be optimized for each ALD process and system to achieve the best growth rate and film quality within the “ALD window” without wasting excess precursor. The “ALD window” is the range of processing temperatures that enable nearly ideal ALD behavior. Processing at lower temperatures can result in incomplete reactions or the precursors can condense. Higher

temperatures can decompose the precursors or cause the chemisorbed species to desorb and no longer be available for reaction.<sup>14</sup>

Growth per cycle (GPC) can be used to determine appropriate ALD process conditions for self-limiting growth. By measuring the GPC for varied precursor dose times, a saturation curve can be developed, like the examples in Figure 1.5a. Saturation curves typically show GPC versus pulse, and the curve should level out when it reaches saturation (meaning GPC does not increase further when more precursor is dosed), indicating self-limiting behavior.<sup>45</sup> Temperature will also play a role in the deposition rate and film quality, with higher temperature growths typically resulting in fewer impurities in the film.<sup>46</sup> As shown in Figure 1.5b, the growth per cycle decreases as temperature increases, which is generally attributed to thermally-activated dehydroxylation reactions.<sup>47</sup> It has also been shown that temperature can influence electrical properties, with decreasing interface state density at higher temperatures.<sup>17</sup>

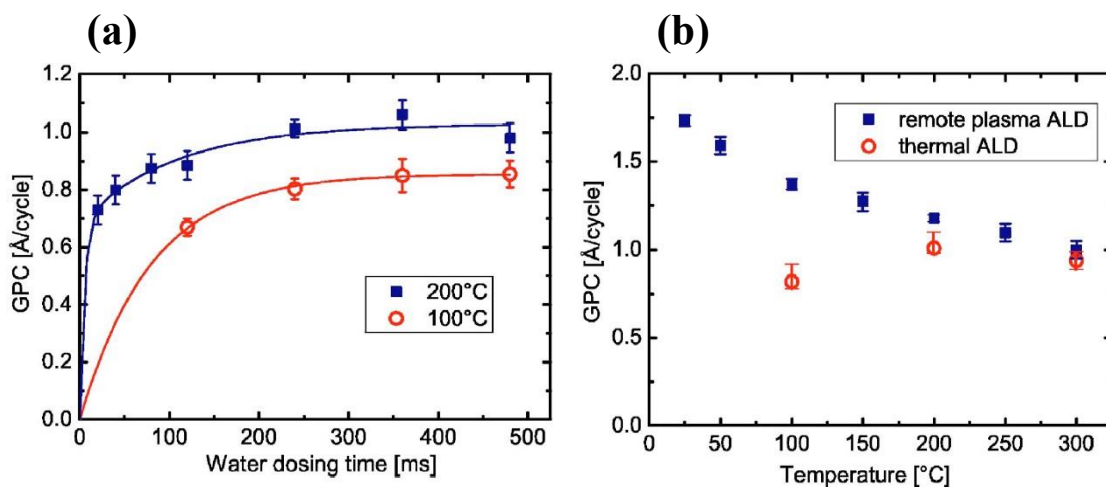


Figure 1.5. (a) Saturation curve for Al<sub>2</sub>O<sub>3</sub> deposition showing GPC as a function of water pulse time for two substrate temperatures; (b) GPC as a function of substrate temperature for Al<sub>2</sub>O<sub>3</sub> deposition [47]. Copyright 2007 The Electrochemical Society. Reproduced by permission of IOP Publishing Ltd. All rights reserved.

Because ALD can deposit high-quality, pinhole-free thin films of material conformally with precise thickness control, it has become popular for a wide variety of applications and research areas, including catalysts,<sup>48</sup> biosensing,<sup>49</sup> and protective coatings.<sup>50</sup> The main industrial application however is microelectronics fabrication, where it is used for thin film displays,<sup>51</sup> photovoltaic devices,<sup>52</sup> energy storage,<sup>53</sup> high- $\kappa$  gate dielectrics,<sup>43,54</sup> metallization layers,<sup>55</sup> and diffusion barriers.<sup>56</sup> While ALD is typically a batch process, there are techniques, such as spatial ALD, that are continuous processes that can be used for larger scale manufacturing. Spatial ALD separates precursor exposure via spatial domain instead of the traditional time domain. This means instead of pulsing precursors into a chamber one at a time, the substrate is moved to different spatial zones within the reactor where precursors are continuously supplied.<sup>45,57</sup>

#### *1.4.1 Area-Selective Atomic Layer Deposition*

Because ALD involves surface reactions, it is very sensitive to surface treatments, which can be leveraged to selectively deposit material in particular regions. This area-selective ALD (AS-ALD) is a promising for a variety of applications, particularly related to nanopatterning of ALD materials for electronics. ALD films can be compatible with conventional photolithography patterning techniques that involve lift-off and etching,<sup>58,59</sup> but the conformality of the coating can make removal of excess material difficult for lift-off.<sup>60</sup> AS-ALD involves activating or de-activating surfaces to either enable or disable deposition via ALD, which allows the film to be deposited only where desired. Activating surfaces typically involves patterning a seed layer that will catalyze the ALD surface reactions.<sup>61</sup> For example, Pt can be deposited selectively on a surface with a thin Pt seed

layer using electron beam induced deposition, while no deposition occurs on the surrounding area.<sup>62</sup>

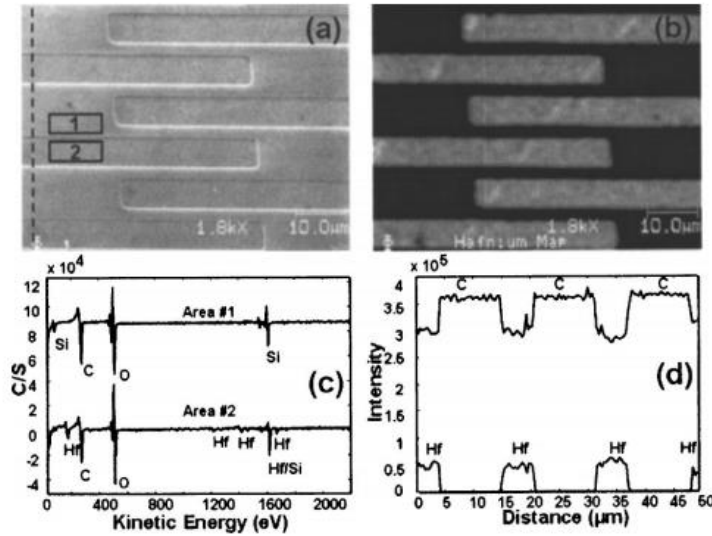


Figure 1.6. SEM images and AES analysis of ODTS pattern after  $\text{HfO}_2$  ALD. (a) SEM image; (b) Hf elemental mapping by AES; (c) area composition scan; (d) AES defined line scan [63]. Reprinted from R. Chen, H. Kim, P. C. McIntyre, D. W. Porter, and S. F. Bent, *Appl. Phys. Lett.* 86 (2005), with the permission of AIP Publishing.

De-activating surfaces is a more common form of AS-ALD, typically using either self-assembled monolayers (SAMs) or polymer films to passivate a surface. SAMs are long organic molecules with functional groups on either end to facilitate attachment to a surface. Octadecyltrichlorosilane (ODTS) with methyl tail groups is commonly attached to a silicon dioxide surface to transform it from the hydrophilic hydroxide-terminated surface to a hydrophobic methyl-terminated surface. The SAM film can be patterned with photolithography or can be selectively attached (e.g., to  $\text{SiO}_2$  and not H-terminated Si). The ALD film can then deposit selectively on the area without SAM coverage. For example, Chen et al. selectively deposited  $\text{HfO}_2$  on a patterned silicon surface using ODTS to passivate  $\text{SiO}_2$  and prevent deposition, as seen in Figure 1.6.<sup>63</sup> Other materials that have been selectively deposited via ALD using SAMs to de-activate the surface include  $\text{ZrO}_2$ ,<sup>64</sup>

$\text{Al}_2\text{O}_3$ ,<sup>65,66</sup> Ru,<sup>67</sup> Pt,<sup>28</sup> Ni,<sup>26</sup> and Co.<sup>68,69</sup> SAMs can degrade when exposed to plasma or ozone, so AS-ALD processes are typically limited to thermal ALD when using SAMs. Additionally, SAMs can take a long time, generally 24 hours and up to 48 hours,<sup>63</sup> to form a well-packed, relatively defect-free film, and the SAM's effectiveness at blocking ALD is strongly impacted by the film quality.<sup>64</sup>

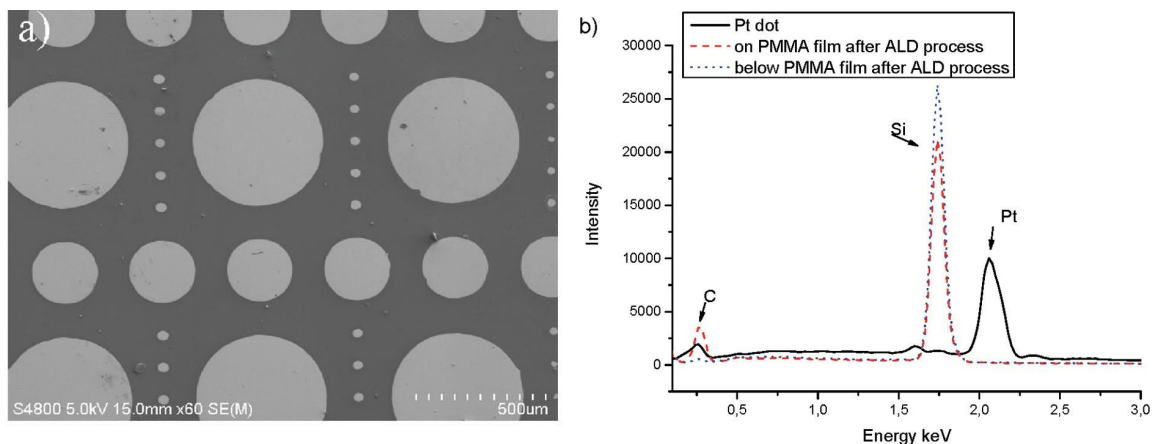


Figure 1.7. (a) SEM image of a patterned Pt film, lighter areas are Pt and darker areas are Si; (b) EDS measurements on a Pt dot, on the PMMA after Pt ALD, and on the Si surface after PMMA removal [60]. Reprinted (adapted) with permission from E. Färm, M. Kemell, M. Ritala, and M. Leskelä, *J. Phys. Chem. C* 112, 15791 (2008). Copyright 2008 American Chemical Society.

Polymer films are another option for de-activating surfaces for AS-ALD and can be easier to coat, more robust, and potentially offer better coverage than SAMs.<sup>70</sup> Polymer films can be spun-coat on a surface (like the PMMA resist used for electron beam lithography) or polymer brushes can be polymerized off of a surface. Poly(methyl methacrylate) (PMMA) and polyvinyl pyrrolidone (PVP) have been used by Färm et al. for AS-ALD of  $\text{Al}_2\text{O}_3$ ,  $\text{ZrO}_2$ ,  $\text{TiO}_2$ , Ru, Pt, and Ir.<sup>60,71</sup> The  $\text{Al}_2\text{O}_3$  and  $\text{ZrO}_2$  films did nucleate on the polymer, meaning the patterning was technically a “lift-off” process rather than area-selective deposition. However, the other materials were selectively deposited without needing “lift-off” of the polymer. Figure 1.7 shows their patterned ALD Pt film deposited

on Si with the non-growth regions masked by a spincoated PMMA film that was patterned with UV lithography. Similar to SAMs, there are also challenges in using polymer masks. Stability, in particular, is a concern for polymer films during AS-ALD processes since plasma and high temperatures can degrade the films.

Other materials that have been selectively deposited with polymer films include ZnO,<sup>59</sup> CeO<sub>2</sub>,<sup>72</sup> and Rh,<sup>73</sup> with a few examples of self-aligned AS-ALD patterning using polymers (where the ALD pattern aligns to the underlying substrate pattern). In one example from Pattison et al., a surface-initiated polynorbornene film is polymerized from initiator molecules selectively bound to copper oxide features and not on the silicon surface. The ZnO is then selectively deposited on the Si surface and not on the copper/copper oxide features.<sup>74</sup> In another example, shown in Figure 1.8, the catalytic effect of different surfaces is leveraged to pattern polymer films (polyimide and PMMA) via area-selective etching with gas-phase etchants (H<sub>2</sub> and O<sub>2</sub>).<sup>75</sup> Polyimide is etched from the Pt surface (since Pt catalyzes the combustion reaction with O<sub>2</sub> when annealed at 300 °C) and remains intact on the native SiO<sub>2</sub> surface. The polyimide then serves as a deactivating mask for ALD of iridium on top of the Pt pattern, and the Ir pattern self-aligned to the underlying Pt pattern is clearly seen in the energy-dispersive x-ray spectroscopy (EDS) maps from Figure 1.8. This self-aligned patterning approach is similar to the SCALES process employed in this work, but it uses a gas phase etchant for selective polymer patterning instead of a solution-based etchant and requires very different surfaces to designate growth and non-growth areas.

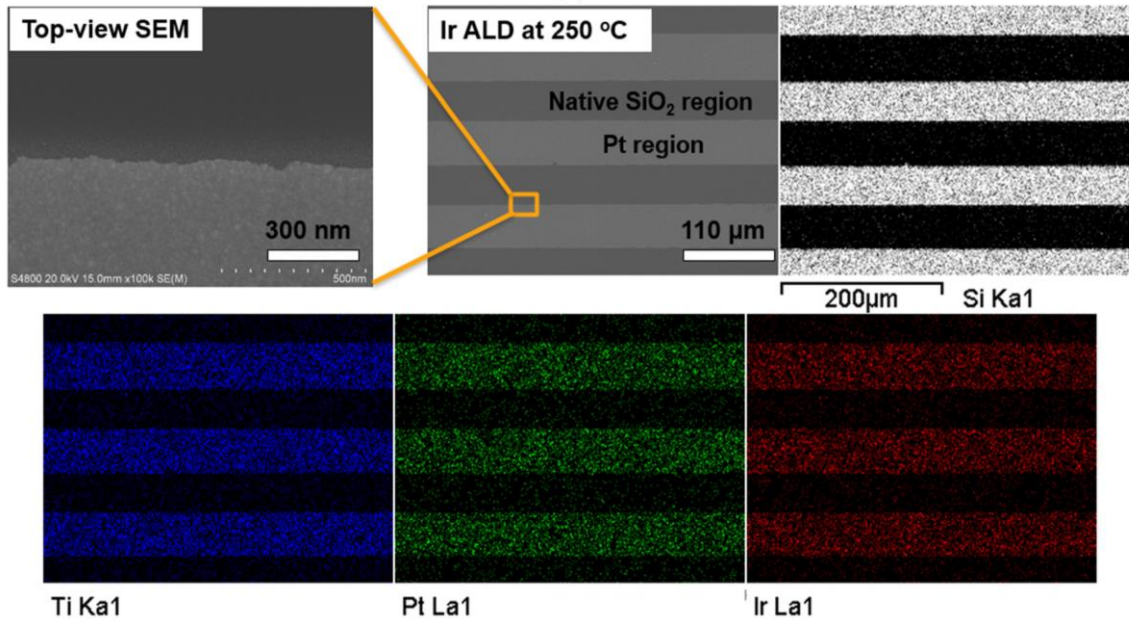


Figure 1.8. Top-down SEM images and the corresponding EDS scans demonstrating the AS-ALD of Ir on exposed Pt surface with native SiO<sub>2</sub> blocked by polyimide film (Ti is present as an adhesion layer under the Pt film) [75]. Reprinted from C. Zhang, M. Leskelä, and M. Ritala, *Coatings* 11, 1124 (2021), with the permission of Coatings.

The main advantage that AS-ALD offers as a bottom-up patterning technique is fewer processing steps when compared to conventional photolithography patterning techniques (that usually require multiple steps of photoresist patterning, film deposition or etching, and lift-off), but this is only the case if the surface deactivation does not require photolithography.<sup>61</sup> However, the majority of AS-ALD processes that do not use photolithography require pre-pattered substrates with chemically very different surfaces to distinguish between growth and non-growth surfaces. The most common distinctions are between a metal and oxide surface<sup>66,76</sup> or an oxide and hydrogen-terminated Si surface.<sup>28,63,77,78</sup> Depositing selectively on chemically similar surfaces is more difficult due to lack of inherent selectivity.<sup>79</sup> Transistor fabrication, however, requires deposition of a gate oxide and metal on a more lightly doped channel region and not on the heavily doped source/drain regions of a semiconductor surface. So, to use AS-ALD for deposition of a

self-aligned transistor gate stack, a method is needed that can deposit an oxide and metal on chemically similar surfaces that only differ by dopant concentration.

## 1.5 Metal-Oxide-Semiconductor Device Structures

### 1.5.1 MOS Capacitors as Test Structures

Metal-oxide-semiconductor (MOS) structures are an essential foundation for many electronic devices. The MOS field-effect transistor (MOSFET) has an insulated gate that modulates conductivity of the channel region depending on the voltage bias applied to the gate.<sup>80</sup> A Si MOSFET generally has heavily doped source and drain regions with a lightly doped channel, and the gate stack consists of an oxide film insulating the channel with a metal electrode on top. A traditional planar MOSFET device structure is shown in Figure 1.9a. Applying a voltage bias to the MOS gate stack repels majority charge carriers and forms a depletion layer in the channel. Applying a higher voltage to the gate eventually leads to inversion, which accumulates minority carriers in the channel at the Si-oxide interface, forming a conductive channel between the source and drain that allows current to flow through the device.

The nanowire MOSFET functions in the same way with heavily doped ends and a lightly doped channel region in the middle of the wire. A diagram of an analogous nanowire MOSFET with the gate stack deposited conformally around the nanowire is shown in Figure 1.9b. Individual nanowire transistor devices, however, are very small (typically microns in length and 50-200 nm in diameter), often smaller than the spot size for common thin film materials characterization techniques like x-ray photoelectron spectroscopy (XPS) and ellipsometry. Therefore, to investigate the materials properties of the gate stack,

especially during process development, MOS capacitors can be used as test device structures that mimic the MOSFET gate stack. A schematic diagram of a MOS capacitor is shown in Figure 1.9c. In this work, MOS capacitors composed of a metal film on top of an oxide film on a planar semiconductor substrate are used to characterize the selectively-deposited ALD gate stack needed for the nanowire transistor.<sup>81</sup> This allows the use of physical and electronic characterization techniques to investigate the gate stack materials as thin films on bulk silicon substrates. Then the same deposition and processing techniques can ultimately be extended to the nanowire transistor fabrication process.

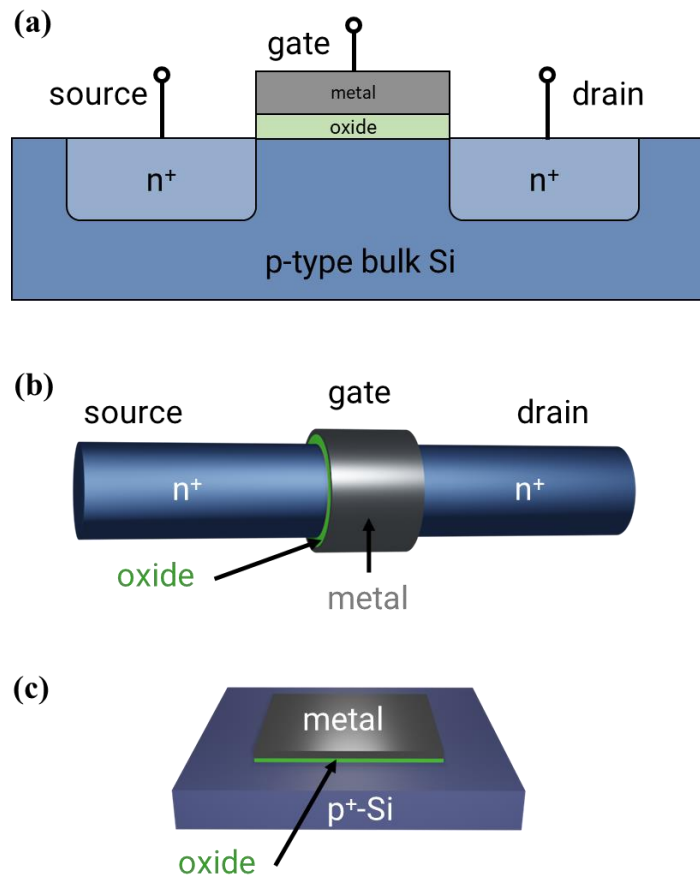


Figure 1.9. Schematic diagrams of: (a) a traditional planar MOSFET device structure; (b) a modular nanowire MOSFET with a wrap-around gate; (c) an MOS capacitor simulating the MOSFET gate stack.

### 1.5.2 Electronic Characterization of MOS Capacitors

To electrically characterize MOS capacitors, capacitance ( $C$ ) and conductance ( $G$ ) are measured as a function of applied dc gate voltage to the metal gate electrode. The capacitance-voltage ( $C$ - $V$ ) and conductance-voltage ( $G$ - $V$ ) curves are used to extract information including the oxide thickness, flatband voltage, fixed charge density, interface state density, and substrate dopant concentration. An ideal  $C$ - $V$  curve is illustrated in Figure 1.10. The total capacitance measured varies with applied voltage and is characterized by three different regimes: accumulation, depletion, and inversion. Figure 1.11 illustrates the charge carrier behavior in each of the three voltage bias regimes.

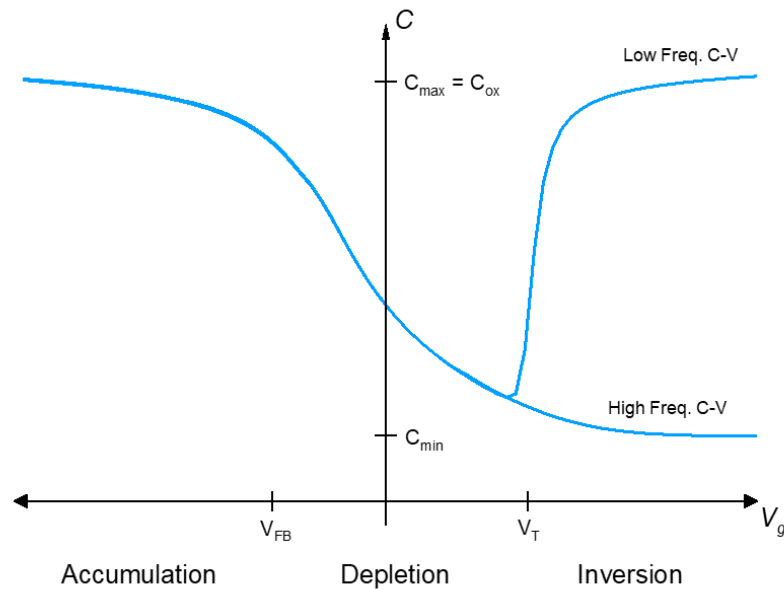


Figure 1.10. Ideal capacitance v. voltage curve for MOS capacitor on p-type semiconductor, showing both a high frequency and low frequency curve.

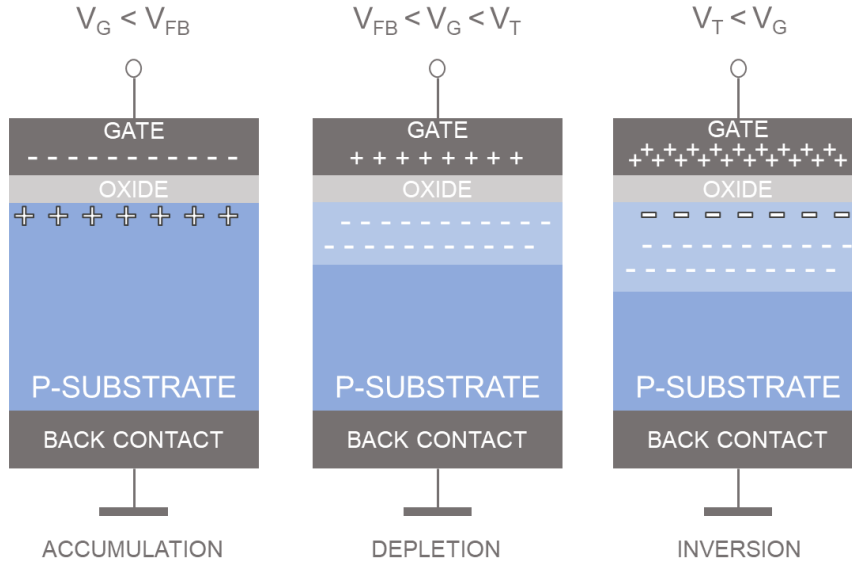


Figure 1.11. Schematic illustration of MOS structure in the three voltage bias regimes.

Accumulation occurs when a voltage more negative than the flatband voltage ( $V_{FB}$ ) is applied to the gate.  $V_{FB}$  is the voltage at which the semiconductor conduction band is flat at the oxide-semiconductor interface. In accumulation for a p-type Si substrate, the negative charge on the gate causes majority carriers (holes) to accumulate at the surface of the semiconductor, and the capacitance is approximately equal to the oxide capacitance ( $C_{ox}$ ) with the following relationship:

$$C_{ox} = \frac{\epsilon_o \epsilon_r A}{t_{ox}} \quad (\text{Eq. 3})$$

where  $t_{ox}$  is the oxide thickness,  $A$  is the capacitor area,  $\epsilon_o$  is the permittivity of free space, and  $\epsilon_r$  is the dielectric constant of the oxide, which is the maximum capacitance of the system.<sup>82</sup>

When a more positive voltage is applied, the depletion regime is reached, where the positive charge on the gate pushes away the majority carriers from the Si interface,

resulting in a depletion of majority carriers in the semiconductor, depicted by the lighter blue region in Figure 1.11. The width of the depletion layer increases with increased applied gate voltage, and the capacitance decreases as the depletion layer expands. The total capacitance is equal to the series combination of the oxide capacitance and the semiconductor capacitance of the depletion layer ( $C_s$ ) which depends on the depletion layer width:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \quad (\text{Eq. 4})$$

where  $C$  is total capacitance and  $C_{ox}$  is the same oxide capacitance described previously.<sup>82</sup>

Finally, the inversion regime is reached when the applied voltage is greater than the threshold voltage ( $V_T$ ), and an inversion layer of the negative minority carriers (electrons) is formed at the Si interface.<sup>82,83</sup> In a MOSFET, this inversion layer is what allows current to flow between the source and drain when the device is in the “on” state. If the AC frequency is low, the minority carriers are able to follow the AC bias frequency. The inversion layer acts as the bottom electrode of the capacitor, and the total capacitance is  $C_{ox}$ , as depicted in the low frequency curve in Figure 1.10. At higher AC frequencies, the inversion charge is unable to follow the AC voltage,<sup>83</sup> and the capacitance saturates and follows the high-frequency curve in Figure 1.10. The capacitance can be calculated with the relationship in Eq. 4, where  $C_s$  is the capacitance of the space charge region in inversion (which can be calculated with more detailed expressions defined elsewhere).<sup>84</sup>

### 1.5.3 Non-Ideal MOS Capacitor Behavior

Deviations from ideal behavior often occur due to defects and extra charges within the oxide and at the semiconductor-oxide interface. There are four types of defects that cause non-ideal behavior: fixed oxide charge, oxide trapped charge, mobile ion charge, and interface trapped charge (or interface states).<sup>82</sup> Figure 1.12 illustrates each of these types of charge. Excess fixed oxide charge is primarily positive charge due to structural defects in the oxide at the Si interface, and the density of this charge depends on Si crystal orientation and oxide processing parameters. Fixed oxide charge results in a shifted flatband voltage and can be minimized with annealing.<sup>84</sup> Oxide trapped charges are holes and electrons trapped within the bulk of the oxide layer that arise during oxide deposition and can also shift  $V_{FB}$ . Mobile charges are primarily due to ionic impurities (such as sodium, lithium, and potassium) that originate from contamination during fabrication. Mobile ions move within the oxide with an applied voltage bias, particularly at higher temperatures, which will result in a shifted flatband voltage.<sup>84</sup> Interface states are primarily due to interfacial defects (i.e., lattice mismatch at the interface, dangling bonds, and impurities) at the oxide-semiconductor interface. The presence of interface states can shift the  $V_{FB}$  and affect the shape of the C-V curve (e.g. large interface state density causes a stretched out curve).<sup>84</sup> The density of interface states ( $D_{it}$ ) is greatly impacted by processing conditions and is also dependent on Si crystal orientation. Generally,  $D_{it}$  for Si(100) is an order of magnitude lower than for Si(111).<sup>82</sup> A large  $D_{it}$  can be especially problematic for MOSFET performance, causing instability in  $V_T$  and reduced carrier mobility, but it can be minimized with annealing and alternate processing methods.

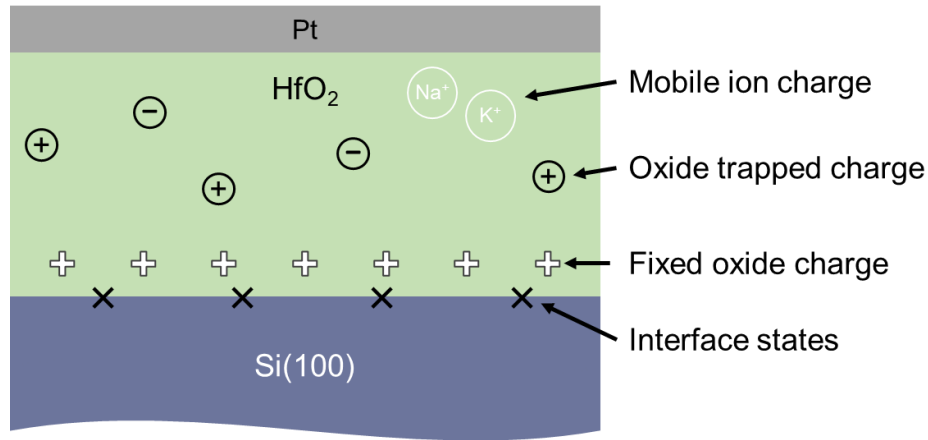


Figure 1.12. Schematic diagram of MOS capacitor illustrating types of charge defects.

#### 1.5.4 Interface State Density Estimation

The interface state density is greatly affected by the oxide deposition process and semiconductor surface treatment. There are a variety of methods used to determine  $D_{it}$ , including (among others) the quasi-static (low-frequency) method, the conductance method, deep level transient spectroscopy, and the charge-pumping method,<sup>84,85</sup> with the conductance method being one of the most common and generally considered one of the most sensitive techniques.<sup>86</sup> This method involves measuring the equivalent parallel conductance ( $G_p$ ) of the MOS capacitor as a function of voltage bias and frequency. The conductance represents the loss mechanism due to interface trap capture and emission of carriers, and, therefore, is a measure of the interface trap density. Refer to Schroder for a thorough explanation of the conductance method and equation derivations.<sup>84</sup> In brief summary, starting with a simplified equivalent circuit representing a MOS capacitor and using simple circuit conversions with the consideration of a time constant dispersion (due to the continuous distribution of interface traps throughout the semiconductor band gap), the following equation is derived for normalized conductance:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln(1 + \omega^2\tau_{it}^2) \quad (\text{Eq. 5})$$

where  $\omega$  is angular frequency (where  $\omega = 2\pi f$  and  $f$  is measurement frequency),  $q$  is electronic charge, and  $\tau_{it}$  is the interface trap time constant. The conductance is measured as a function of frequency and plotted as  $G_p/\omega$  versus  $\omega$ , and  $D_{it}$  is determined from the maximum  $G_p/\omega$ . The following expression can be used as an approximate expression for  $D_{it}$  in terms of measured maximum conductance:<sup>85</sup>

$$D_{it} \approx \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{max} \quad (\text{Eq. 6})$$

Additionally, there are limitations to consider when applying the conductance method to extract  $D_{it}$  for tunneling gate dielectrics, and the extracted values can be impacted by various parameters including series resistance, oxide capacitance, and interface state time constant.<sup>87</sup> Series resistance due to the bulk silicon and contacts is typically non-negligible and can impact the measured capacitance and conductance. The following relationships are derived from simplified equivalent circuit diagrams depicted in Vogel et al. and can be used to correct the measured C and G for series resistance:

$$C_c = \frac{C_m}{(1 - G_m R_s)^2 + \omega^2 C_m^2 R_s^2} \quad (\text{Eq. 7})$$

$$G_c = \frac{\omega^2 C_m C_c R_s - G_m}{G_m R_s - 1} \quad (\text{Eq. 8})$$

where  $C_m$  and  $G_m$  are measured capacitance and conductance,  $C_c$  and  $G_c$  are corrected capacitance and conductance,  $\omega$  is frequency and  $R_s$  is series resistance.<sup>87</sup>

### 1.5.5 High- $\kappa$ Dielectrics in MOS Structures

Historically, a high-quality, thermally grown SiO<sub>2</sub> layer provided an effective dielectric layer with a smooth, stable, low-defect density interface with the Si substrate for MOS devices.<sup>88,89</sup> However, as transistor channel length and SiO<sub>2</sub> thickness was reduced to increase the speed and performance of MOSFETs, a limit was reached in SiO<sub>2</sub> thickness (10-12 Å) due to high leakage current and reduced reliability of these ultra-thin SiO<sub>2</sub> layers.<sup>89,90</sup> This led to the now universal use of high- $\kappa$  dielectric materials for gate oxides because physically thicker films can be used to achieve equivalent capacitance.<sup>89</sup> The thicker films of high- $\kappa$  dielectric results in reduced leakage current.

A variety of high- $\kappa$  materials have therefore been studied for use in electronics technology, including aluminum oxide (Al<sub>2</sub>O<sub>3</sub>), hafnium oxide (HfO<sub>2</sub>), zirconium oxide (ZrO<sub>2</sub>), and titanium oxide (TiO<sub>2</sub>), to name just a few.<sup>42,54,89,91</sup> HfO<sub>2</sub>, in particular, is favorable because it can have suitable dielectric properties (i.e., band gap, dielectric constant, low leakage current) and good thermal stability with Si.<sup>43,92-94</sup> These high- $\kappa$  materials can be deposited with several different methods, including molecular beam epitaxy,<sup>95</sup> reactive sputtering,<sup>96-98</sup> and metalorganic chemical vapor deposition (MOCVD),<sup>99,100</sup> in addition to atomic layer deposition. Variations of chemical vapor deposition (CVD), which includes ALD, can deposit high-quality, conformal films with good thickness control and high throughput, making them promising options in terms of processing compatibility.<sup>101</sup>

### 1.5.6 Oxide-Semiconductor Interface with ALD HfO<sub>2</sub>

As explained in the previous sections, the preparation and quality of the oxide-semiconductor interface can have a significant impact on the electronic performance of MOS devices. It is widely known that ALD oxide films (including HfO<sub>2</sub>) nucleate better on SiO<sub>2</sub> surfaces than H-terminated Si surfaces.<sup>102-104</sup> This can be seen in Figure 1.13 from Gusev et al. in which TEM images show poor nucleation leading to island formation of HfO<sub>2</sub> on the bare Si surface (Figure 1.13a) and a continuous, uniform layer on the SiO<sub>2</sub>/Si surface (Figure 1.13b).<sup>43</sup> Additionally, it was shown by Cho et al. that depositing HfO<sub>2</sub> via ALD on a Si substrate with a very thin SiO<sub>2</sub> layer results in the formation of a hafnium silicate interfacial layer that can impact the thermal stability of the crystal structure of the resulting HfO<sub>2</sub> film.<sup>18</sup> Presence of an initial SiO<sub>2</sub> layer between the Si surface and HfO<sub>2</sub> can therefore enhance deposition of a uniform HfO<sub>2</sub> film but can negatively impact electronic performance due to the parasitic effect of an extra capacitance in series with the high- $\kappa$  oxide capacitance. To reduce this effect, the initial SiO<sub>2</sub> interlayer should be as thin as possible.

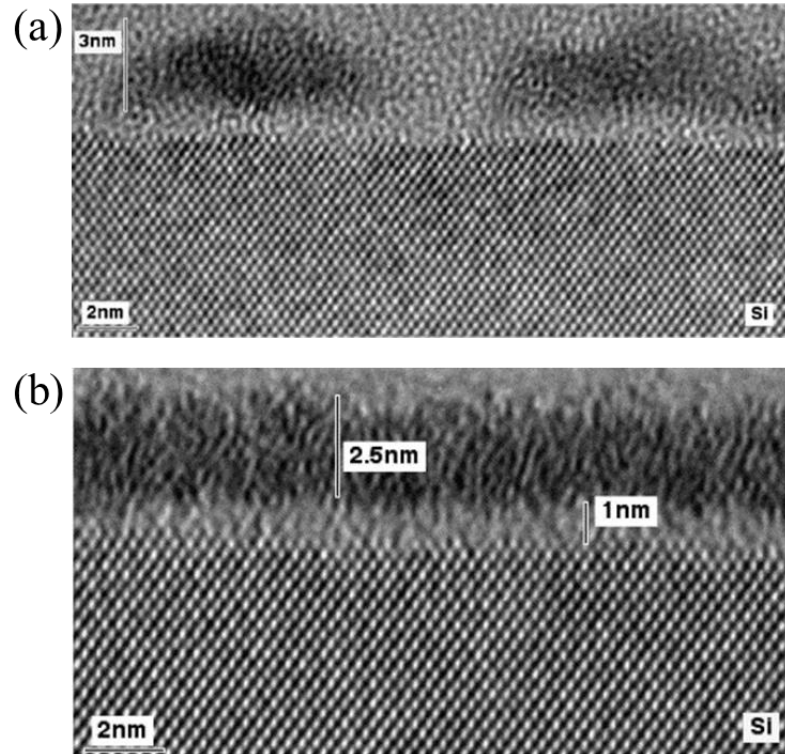


Figure 1.13. High-resolution TEM cross-section images of ALD HfO<sub>2</sub> films on (a) bare Si and (b) SiO<sub>2</sub>/Si [43]. Reprinted from E. P. Gusev, C. Cabral, M. Copel, C. D’Emic, and M. Gribelyuk, *Microelectron. Eng.* 69, 145 (2003), Copyright (2003), with permission from Elsevier.

There have been multiple studies investigating the use of different oxidation techniques to form a very thin SiO<sub>2</sub> interlayer underneath ALD HfO<sub>2</sub> films. Green et al. compared HF-last Si, rapid thermally oxidized SiO<sub>2</sub> interlayers and wet chemical oxidation interlayers (SC-1, SC-2, ozonated H<sub>2</sub>O) and found that the large concentration of -OH groups on the chemical oxide surfaces encourages the best growth of continuous HfO<sub>2</sub> films with almost no nucleation delay.<sup>103</sup> Another study looked in detail at the effect of the thickness of an SC-1 chemical oxide interfacial layer on electrical performance of HfO<sub>2</sub> MOS capacitors and showed improved C-V performance (indicating better interface state density) with the increasing interfacial layer thickness (films ranged from 0.4 to 0.5 nm in thickness).<sup>102</sup> Considering the importance of interface defects on electronic performance

along with these studies on interfacial layers, it is clear that careful treatment of the Si surface prior to ALD of a gate oxide is quite important and an SiO<sub>2</sub> interlayer will likely improve deposition and device performance.

## 1.6 Existing Nanowire Electronics Technology

Over the past 20 years, nanowire electronic devices have gained popularity in research due to the unique properties that nanoscale dimensions have to offer, and there are near-future plans to implement top-down nanowire transistor devices commercially.<sup>105</sup> With many different nanowire synthesis techniques available, nanowire electronic devices can vary widely in terms of composition, structure, and function. Semiconductor devices have been made with many different materials, including Group IV semiconductors (i.e. Si, Ge),<sup>106</sup> Group III-V semiconductors (e.g. GaAs, GaN),<sup>107-109</sup> and Group II-VI semiconductors (e.g. CdSe, ZnS).<sup>110-112</sup> The nanowires themselves can be homogenous or heterostructures (axially or radially), all of which lend different advantages and capabilities. And a variety of applications have been explored for nanowire electronic devices, including chemical and biological sensing with FETs,<sup>113-116</sup> flexible electronics,<sup>117,118</sup> and optoelectronics,<sup>119-121</sup> among many others.

With the nanowire electronics field showing such promise, there are many demonstrations of electronic devices made with Si nanowires. They range from very simple cross bar structures<sup>122,123</sup> (shown in Figure 1.14) and single nanowire heterostructure devices<sup>124</sup> to more complex structures, such as nanowire transistors with wrap-around gates<sup>125,126</sup> (with one example shown in Figure 1.15), similar to the device structure this work aims to help develop. The main unique factor about this work's approach to nanowire

device fabrication is the aim to use a fully bottom-up process to make circuits with nanowire transistors. Many nanowire electronic devices use some sort of top-down, conventional fabrication technique (e.g., photolithography or electron beam lithography), which limits the scalability of the final product. For more examples and details about other nanowire electronics, there are several literature reviews published that highlight the many different nanowire electronic devices that have been fabricated and modelled.<sup>106,127-131</sup>

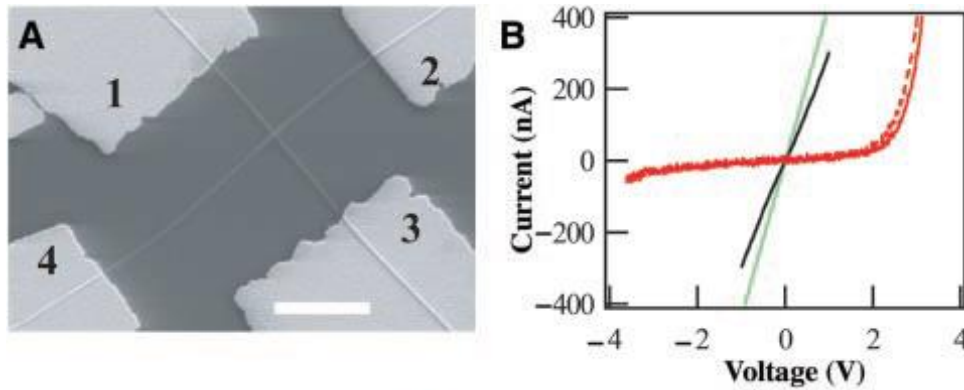


Figure 1.14. Example of a Si nanowire electronic device: (a) SEM image of crossed p-type and n-type Si nanowires, scale bar is 2  $\mu\text{m}$ ; (b) black and green lines show I-V behavior of the individual NWs, red curves show I-V behavior of the p-n junction [122]. From Y. Cui and C. M. Lieber, *Science* 291, 851 (2001). Reprinted with permission from AAAS.

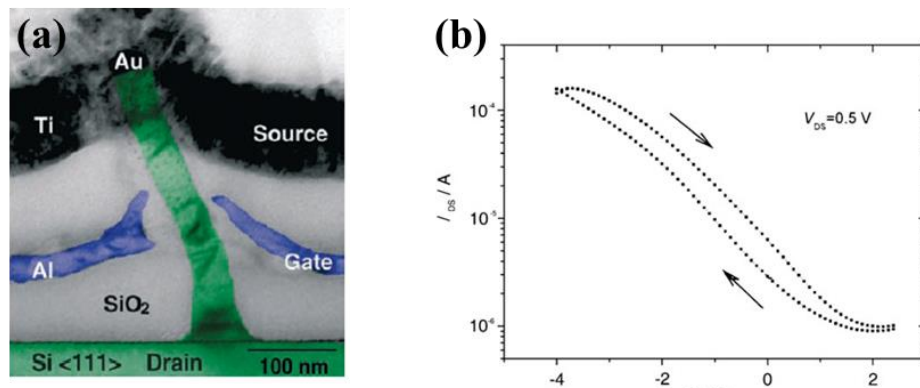


Figure 1.15. Example of a Si nanowire electronic device: (a) TEM image of a conventionally fabricated top-down wrap-around gate nanowire FET; (b)  $I_d$ - $V_g$  behavior of multiple NW FETs contacted in parallel [125]. Reprinted (adapted) with permission from V. Schmidt, H. Riel, S. Senz, S. Karg, W. Riess, and U. Gosele, *Small* 2, 85 (2006). Copyright 2006 John Wiley and Sons.

There are several factors that make nanowires interesting for electronics applications. Semiconductor nanowires can be produced in high-yield with well-controlled dimensions and composition due to the bottom-up nature of the VLS synthesis techniques. This work leverages the chemical differences between heavily doped and lightly doped or intrinsic Si to selectively pattern the polymer film, and the dopant modulation can easily be incorporated during the bottom-up nanowire growth, unlike conventional electronics fabrication that requires multiple steps and high temperatures to drive in dopant material. Additionally, the bottom-up synthesis results in single-crystalline material which lends good electrical properties (i.e. high carrier mobility).<sup>132,133</sup> Additionally, using Si nanowires is beneficial because of the interface stability and high material compatibility with oxides and metal-silicides.

There are a number of challenges to be addressed, as well, for VLS bottom-up nanowire devices. Si nanowires synthesized with the VLS mechanism can have vastly different surface properties based on the growth parameters. Cylindrical VLS nanowires typically have facets of different crystal orientations on the side walls and the gold from the catalyst can spread along the wire.<sup>134,135</sup> It is known that crystal orientation can have a significant impact on interface state density (i.e., it is higher on  $\langle 111 \rangle$  surfaces than  $\langle 100 \rangle$ ), which can limit the effective mobility for nanowires with faceted sidewalls.<sup>136</sup> The surface preparation of the nanowires for devices will therefore be particularly important, and any potential spreading of gold would need to be addressed (either with alternate nanowire growth parameters or a post-processing gold etch) to prevent diffused gold particles from shorting the devices. Additionally, according to the IEEE International Roadmap for Devices and Systems: Beyond CMOS, some major challenges to be

addressed for bottom-up nanowire transistors are device yield and uniformity as well as position registry for nanowires transferred to other substrates.<sup>105</sup>

## **CHAPTER 2. ADAPTING SCALES PATTERNING FOR PLANAR SILICON SUBSTRATES**

The SCALES patterning process was developed particularly for use on VLS nanowires, in which dopant modulation can easily be incorporated along the length of the wire. However, as mentioned in section 1.5.1, nanowire structures are much smaller than the spot size needed for many materials characterization techniques, so this work adapts the same process for planar Si samples with larger feature sizes to enable the use of those characterization techniques. This chapter will describe the methods developed for each step of the SCALES patterning process, including dopant-patterned substrate fabrication, polymer synthesis, patterning with potassium hydroxide (KOH) etching, and the post-patterning clean.

### **2.1 Nanowire Growth Process**

As mentioned in CHAPTER 1, the ultimate aim of this project is to fabricate bottom-up transistors using Si nanowires. The actual growth of the nanowires is outside the scope of this work, and the nanowire growth has been developed and performed by a number of other researchers for the project. Refer to earlier work from the group for a more detailed description of the VLS growth process and processing parameters.<sup>4,13,137</sup> Briefly, Si(111) or SiO<sub>2</sub> substrates are prepared with either gold nanoparticles (100 nm in diameter) or patterned with electron beam (e-beam) evaporated gold circles (~220 nm in diameter) to act as the catalyst for growth. The substrates are loaded in a cold-wall commercial CVD furnace (EASYTUBE 300, FirstNano CVD) and annealed at 650 °C to desorb contaminants. The temperature is then lowered to the nucleation temperature (~500 °C for

Si NWs) and then raised to the desired nanowire growth temperature (between 480 °C and 600 °C for this project) while flowing silane ( $\text{SiH}_4$ ) gas (100 SCCM) with hydrogen (1000 SCCM) as a carrier gas. Hydrogen chloride ( $\text{HCl}$ ) gas is also sometimes flowed (100 SCCM) to passivate the nanowire sidewalls and stabilize the gold droplet during growth. For dopant modulated nanowires, either phosphine ( $\text{PH}_3$ ) or diborane ( $\text{B}_2\text{H}_6$ ) gas is flowed with  $\text{SiH}_4$  (at much lower flowrates, between 0.5 and 50 SCCM) to incorporate n-type or p-type dopant atoms, respectively.

## 2.2 Dopant-patterned Substrate Fabrication

Demonstrating the SCALES patterning process on planar samples requires Si substrates that are pre-patterned with heavily and lightly doped regions. The following procedure was developed for this purpose, and the resulting patterned substrates are then used for AS-ALD of gate stack structure. The overall fabrication process involves patterning a hard  $\text{SiO}_2$  mask on a Si wafer and using solid source diffusion to dope the exposed areas, as illustrated in Figure 2.1.

First we clean a bare 100 mm lightly boron-doped Si(100) wafer (0.01-0.02  $\Omega\text{-cm}$ , Virginia Semiconductor) with the standard RCA cleaning process, described in Table 2.1 (with a thorough DI  $\text{H}_2\text{O}$  rinse between each step).<sup>138</sup> This process is performed at the CMOS Cleaning Station (Marcus) with chemicals provided by the cleanroom, including  $\text{H}_2\text{O}_2$  (30%, J.T. Baker),  $\text{NH}_4\text{OH}$  (29%, J.T. Baker),  $\text{HCl}$  (37%, J.T. Baker), and  $\text{HF}$  (49%, J.T. Baker). The passivating oxide layer is then stripped (30 sec in 1%  $\text{HF}$ ) before transferring to the Tystar Mini Tube (1 or 2) furnace for a dry thermal oxidation at 1100

°C for 13 hours and 35 min to form a thick SiO<sub>2</sub> layer (~500 nm thick, though SiO<sub>2</sub> film may be thicker).

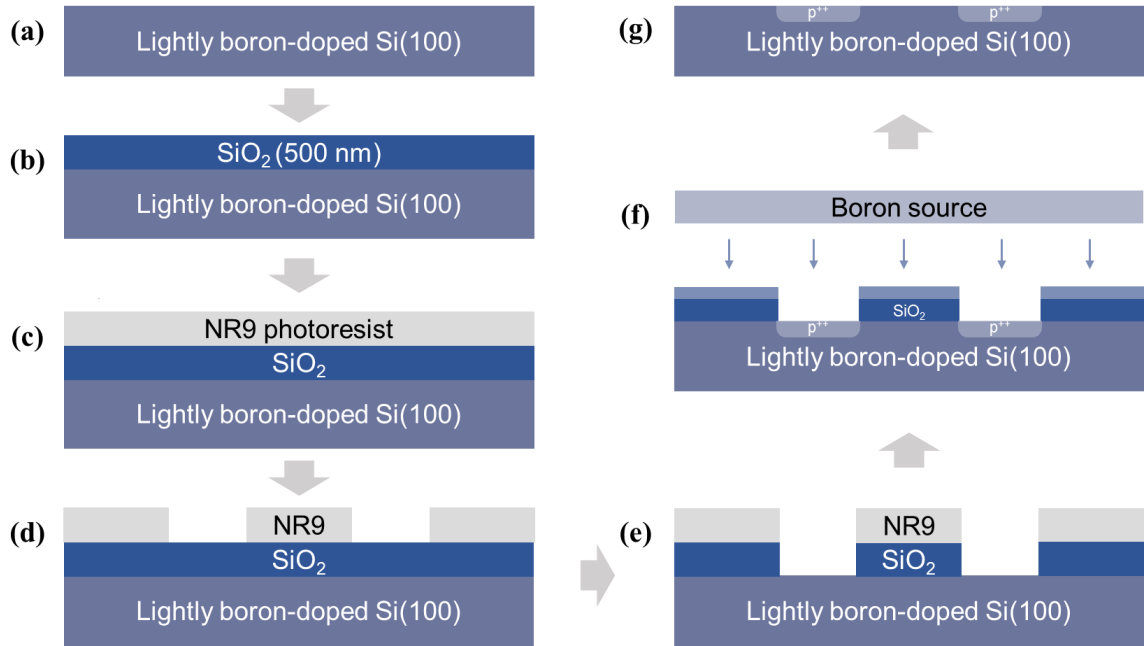


Figure 2.1. Schematic diagram of the fabrication process for boron-patterned substrates.

(a)-(e) steps to pattern a hard SiO<sub>2</sub> mask; (f) solid source dopant diffusion to dope exposed areas; (g) final patterned substrate with regions of heavily and lightly doped Si.

Table 2.1. Procedure for standard RCA clean.

	Purpose	Process Conditions
Step 1 (SC-1):	Organic clean	5 DI H <sub>2</sub> O:1 H <sub>2</sub> O <sub>2</sub> :1 NH <sub>4</sub> OH, 75 °C, 10 min
Step 2 (optional):	Oxide strip	1% HF, room temperature, 30 sec
Step 3 (SC-2):	Ionic/metallic clean	5 DI H <sub>2</sub> O:1 H <sub>2</sub> O <sub>2</sub> :1 HCl, 75 °C, 10 min

To pattern the hard SiO<sub>2</sub> mask, negative photoresist (NR9-1500PY, Futurrex) is spincoated on the wafer (10 sec ramp, 40 sec dwell, 3000 rpm) and soft baked at 150 °C for 1 min. Maskless UV photolithography with the Maskless Aligner (MLA, Heidelberg MLA 150) is used to expose the photoresist with the 375 nm wavelength laser and a dose of 850 mJ-cm<sup>-2</sup>. MLA exposure parameters may vary over time. Immediately following the exposure, the wafer is baked at 100 °C for 1 min and then developed with RD6 (Resist Developer RD6, Futurrex) for 10-12 s, and additional development time may be needed. The hard mask is then etched with buffered oxide etch (BOE, 6:1 BOE, J.T. Baker) at the CMOS Cleaning Station. After using an etch test to determine the etch rate of ~1.3 nm/s, the wafer is submerged in BOE for ~420 sec to fully etch away the exposed SiO<sub>2</sub> (this time will vary based on SiO<sub>2</sub> thickness). The bare Si surface should be hydrophobic when the SiO<sub>2</sub> is completely removed. The wafer is soaked in acetone for at least 2 min (or longer if necessary) to remove the photoresist.

Before the dopant diffusion step, the wafer undergoes another RCA clean (without step 2 oxide strip to protect the SiO<sub>2</sub> mask) to remove any contamination from the photolithography process. The native oxide is stripped with a 15 sec etch in 1% HF (in the Pettit cleanroom) immediately prior to the dopant diffusion. The wafer is then transferred to the Tystar Nitride 2 furnace for solid source diffusion of boron with a B<sub>2</sub>O<sub>3</sub> source (GS-183, BoronPlus) at 1050 °C for 2 hours. Finally, a long BOE etch (~10 min) at the Marcus CMOS Cleaning Station is used to remove the hard SiO<sub>2</sub> mask and the borosilicate glass film. While an HF etch should be able to remove the borosilicate glass layer,<sup>139</sup> additional BOE etch time or a nitric acid mixture<sup>140</sup> may help if needed. After this final step, the wafer should look like bare silicon wafer with a fully hydrophobic surface, and the pattern

features can be seen very faintly at certain angles in light. Note, the procedure described here is for making p-type boron-doped Si, but the same process can be used to make n-type phosphorus-doped substrates (with the  $P_2O_5$  source in the Tystar Nitride Furnace 1).

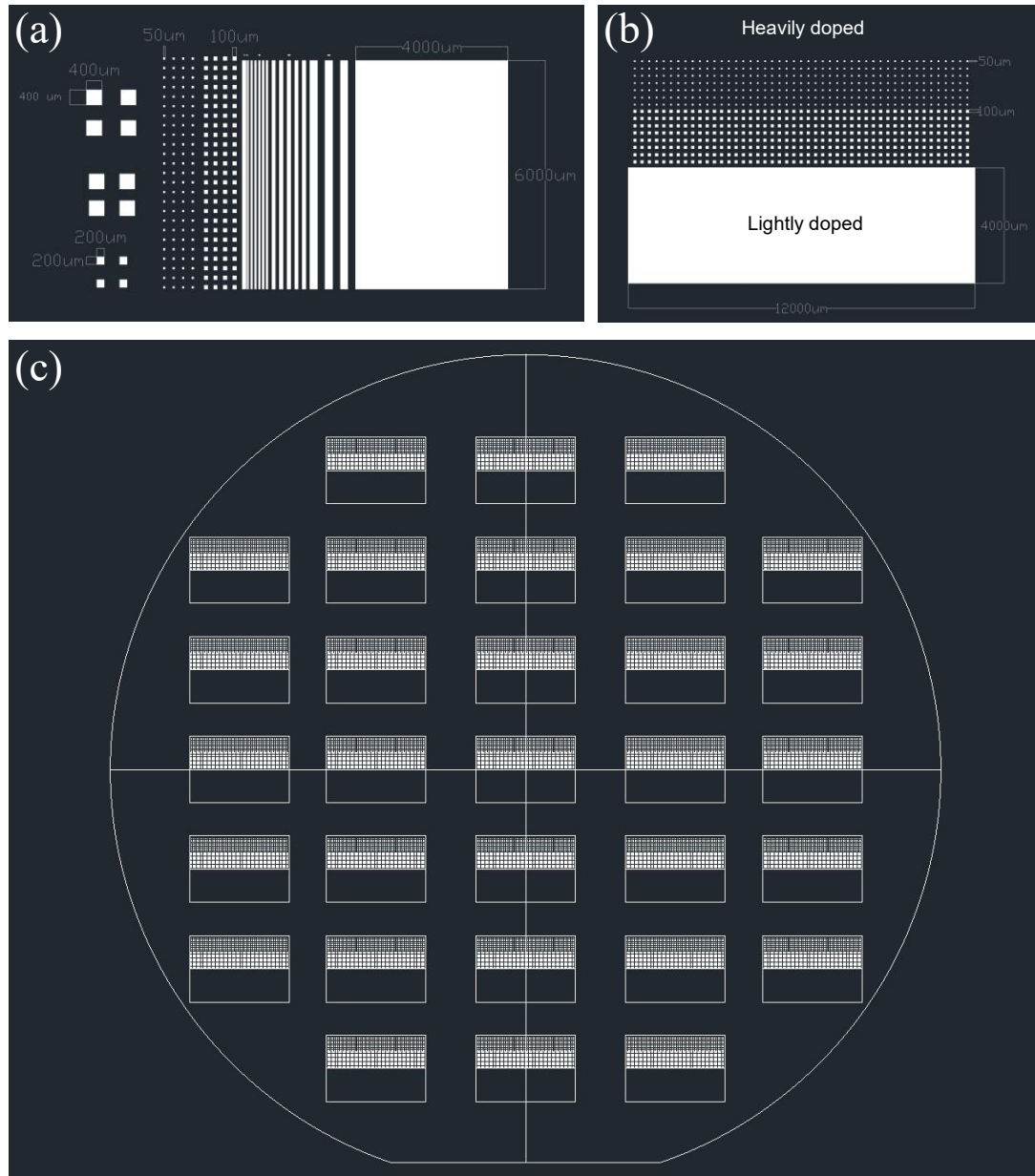


Figure 2.2. Dopant-patterned substrate mask designs: (a) and (b) Two versions of the individual substrate pattern with features of varying size ( $50\ \mu\text{m}$ ,  $100\ \mu\text{m}$ ,  $200\ \mu\text{m}$ ,  $400\ \mu\text{m}$ ) and a very large area for surface characterization; (c) Full 100 mm wafer design with 31 individual patterns repeated.

Since we use the MLA to pattern the hard SiO<sub>2</sub> mask, almost any pattern can be designed for the doped/undoped areas. But keep in mind the junction depth of the dopants will be between 0.5-1 μm at 1050 °C, so we must also assume lateral diffusion of the same amount. Therefore, feature sizes less than a micron or two are not likely to remain distinct. The MLA mask designs used to fabricate the substrates are shown in Figure 2.2. Two versions of the individual substrate pattern (Figure 2.2a and b) show square and line features with dimensions between 50 μm and 400 μm, and both include a large box (dimensions greater than 4 mm) to enable XPS and ellipsometric characterization. The lines and large squares are meant for mapping the AS-ALD patterns and the large arrays of smaller squares (100 μm x 100 μm and 50 μm x 50 μm) are meant for self-aligned capacitor fabrication. On the final substrates, everything outside the pattern (black regions) will be heavily doped, and everything inside the white pattern will remain lightly doped. Figure 2.2c shows the full wafer design with repeated individual patterns, meant to be scribed or diced into pieces after fabrication. The oxidation and doping furnaces are designed for 100 mm wafers, so ideally a full wafer should be used for the duration of the fabrication.

### **2.3 Poly(methyl methacrylate) Brush Synthesis**

Typically, polymer films for AS-ALD use are spincoated and then patterned with photolithography, like the poly(methyl methacrylate) (PMMA) films used by Färm et al.<sup>60</sup> These polymer films can easily be removed by soaking in a solvent like acetone. To remove the photolithography step, this work uses what we refer to as the SCALES (or selective co-axial lithography via etching of surfaces)<sup>4</sup> process (adapted for planar samples). This requires a polymer film that is chemically bonded to the substrate surface (often referred to as a polymer brush), in this case a Si wafer, so the masked regions remain intact during

the etching step. This work uses a full coverage PMMA brush synthesized with a surface-initiated atom transfer radical polymerization (ATRP) reaction. The film is then patterned using a wet KOH etch to remove PMMA from the lightly doped regions, leaving behind a PMMA mask covering the heavily doped regions, which enables the use of AS-ALD to form a self-aligned MOS gate stack structure. This section describes the PMMA polymerization in detail, and the next sections will cover the KOH etch and post-patterning clean.

### *2.3.1 PMMA Synthesis Procedure*

This surface-initiated PMMA polymerization procedure was initially developed by a previous researcher on the project, Dr. Amar Mohabir. Refer to his dissertation for details of the original process development and use of SCALES on nanowires.<sup>13</sup> The procedure has been adapted for this work for use on planar samples with updates to improve reproducibility. The overall polymerization involves three steps, as depicted in Figure 2.3. First the anchoring molecule, 11-undecen-1-ol (or undecenol), is attached to a bare H-terminated surface, forming a SAM. Next the initiator molecule, bromoisobutyryl bromide (BIBB), is attached by reacting with the hydroxyl group on the undecenol. Finally, the ATRP reaction is initiated from the tertiary bromine on BIBB, polymerizing the monomer, methyl methacrylate (MMA), to form a PMMA brush anchored to the Si surface.

Beginning with a bare Si substrate (e.g., a boron-patterned Si wafer with heavily and lightly doped regions), we gently clean the surface with a 30 min UV-ozone treatment (ZoneSEM Desktop Sample Cleaner, Hitachi). During the clean, the Teflon beaker for BOE is filled with nitric acid (70%, Sigma-Aldrich) and heated to 60 °C for about 30 min

to minimize contaminants. The native oxide is then removed from the surface of the Si sample with a 20 sec etch in BOE (6:1 BOE, Sigma-Aldrich) before being transferred to the glovebox. All polymerization steps are performed in a low-oxygen, low-moisture, nitrogen-purged glovebox (OMNI-LAB). Solutions that are purged with nitrogen (ultra-high purity N<sub>2</sub>, Airgas) are removed from the glovebox (in a septum vial) and purged with a Schlenk line to minimize trace amounts of oxygen and moisture, and then transferred back into the glovebox. (Note: generic ratios for mixtures are stated in the procedure with the exact amounts used for one polymerization batch in parentheses.)

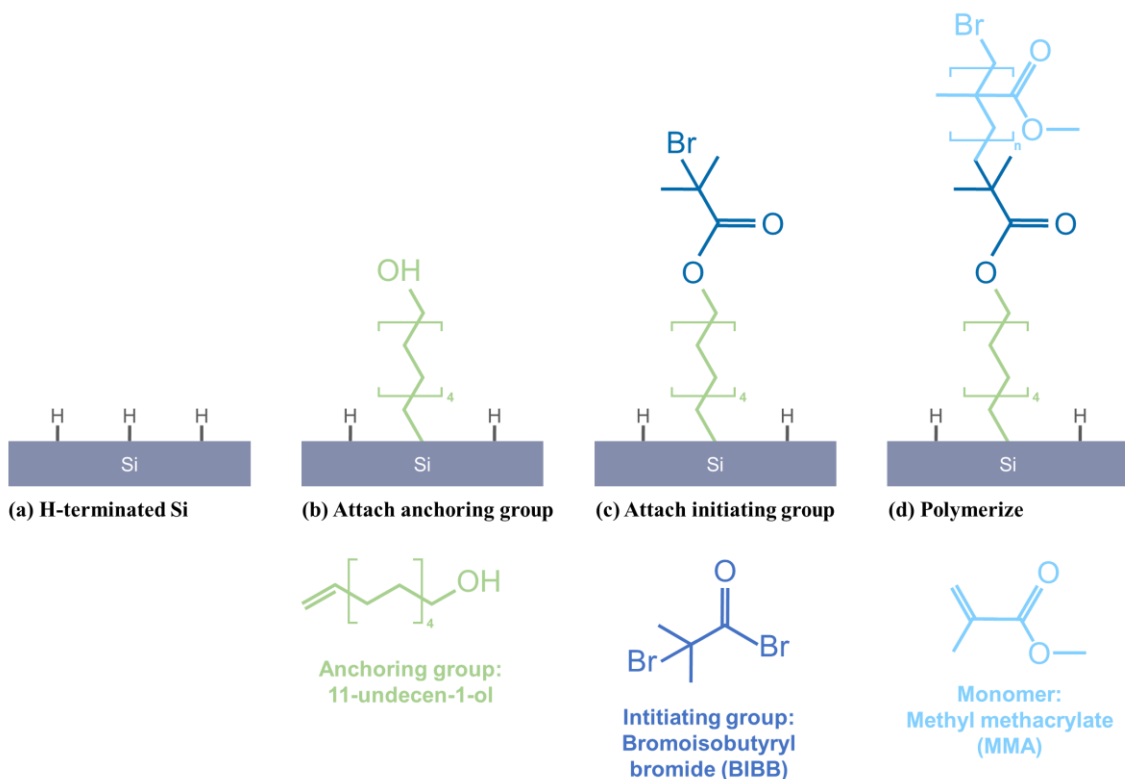


Figure 2.3. Reaction scheme for the three-step polymerization of PMMA. First, undecenol is attached to a bare Si surface (a) via hydrosilylation (b). Next, BIBB is attached to the -OH group on undecenol (c). Finally, PMMA is polymerized from the tertiary bromine on the BIBB initiating group (d).

The first step of the polymerization is to attach the anchoring molecule, undecenol, to the Si surface via a hydrosilylation reaction. A mixture of 5% undecenol (98%, Sigma-

Aldrich) and mesitylene (98%, Sigma-Aldrich) is prepared (1 mL undecenol + 19 mL mesitylene) and purged with N<sub>2</sub> for 20 min. We then pipette ~5 mL of solution into each vial with the Si samples laying face-up on the bottom. The vials are heated at 150 °C for 2 hours in heated well hotplate (SBH2000 Block Heater, Stuart). This enables the hydrosilylation reaction where the alkene double bond attaches to the Si surface, essentially forming a SAM across the substrate.<sup>141-143</sup> After 2 hours, the samples are removed from the vials, rinsed with extra mesitylene for about 30 seconds and then gently blown dry to prevent undesirable drying effects that can impact film uniformity.

The –OH group at the end of the undecenol can then react with the acyl halide part of the initiator molecule, BIBB, to attach the initiator to the substrate.<sup>144</sup> Using a separate vial for each sample, BIBB is attached via reaction at room temperature for 2 hours with a mixture of toluene (99.8%, Sigma-Aldrich), triethylamine (99.5%, Sigma-Aldrich) and BIBB (98%, Sigma-Aldrich) in a 28:1:4 ratio by volume. The toluene (7 mL) and triethylamine (0.25 mL) are first mixed in each vial, the sample is then placed in the vial face-up, and BIBB (1 mL) is pipetted dropwise into the vial over a period of ~5 min via a quartz tube with a stopcock valve. Each sample is then removed from the vial and thoroughly rinsed in toluene, acetone (99.5%, Sigma-Aldrich), and methanol (99.8%, Sigma-Aldrich) for 5 min each to remove excess anchoring and initiator molecules.

Finally, PMMA is polymerized off of the initiator molecule via an ATRP reaction at 90 °C.<sup>145</sup> The monomer solution is prepared by combining CuBr<sub>2</sub> (99%, Sigma-Aldrich), CuBr (98%, Sigma-Aldrich), and 2,2'-bipyridine (BPY, 99%, Sigma-Aldrich) with a 1:2:9 ratio by weight to a mixture of anhydrous dimethylformamide (DMF, 99.8%, Sigma Aldrich) and methyl methacrylate (MMA) monomer (99%, Sigma-Aldrich) with a ratio of

3:32 by volume. The CuBr acts as a catalyst, the CuBr<sub>2</sub> serves as a deactivating catalyst, and the BPY is a ligand that can complex with the copper species to assist solvation.<sup>145,146</sup> The catalyst powders are first weighed in a vial (20 mg CuBr<sub>2</sub> + 40 mg CuBr + 180 mg BPY), and then the DMF (1.5 mL) is added and swirled around to dissolve the powders. The MMA (16 mL) is forced through a syringe packed with Al<sub>2</sub>O<sub>3</sub> (Alumina inhibitor remover, Sigma-Aldrich) to remove the monomethyl ether hydroquinone (MEHQ) inhibitor before being added to the DMF solution, and the solution is then purged with N<sub>2</sub> for 20 min. The monomer solution is pipetted into each vial (~4mL) with BIBB-coated samples facing up and heated at 90 °C for the duration of the polymerization in a block heater (VWR Digital Heatblock). A 4-hour polymerization is typically performed to achieve a PMMA thickness around 40-60 nm. ATRP reactions generally polymerize at a controllable, linear growth rate, so a shorter polymerization time should result in shorter polymer chains and thus a thinner film.<sup>147</sup> After 4 hours, the samples are rinsed with acetone and then soaked in acetone overnight (~15-20 hours). A detailed procedure for this polymerization with notes for our specific lab setup can be found in Appendix A.

### 2.3.2 *PMMA Film Characterization*

After the polymerization, we can confirm the film thickness with ellipsometry and the film composition with XPS characterization. More detail about the specific measurement parameters can be found in Appendix B, but results from ellipsometric measurements of the PMMA films typically report thicknesses between 35 nm and 55 nm for the 4 hour polymerization, though we do see a fair amount of variability with films as thin as 20 nm and as thick as 70 nm. In terms of uniformity across the substrate, ellipsometry typically indicates the range of measured thickness values around 2-4 nm but

sometimes as much as 10 nm. XPS characterization confirms the accurate composition of the film with peaks in the C(1s) and O(1s) regions that are consistent with those expected for PMMA.<sup>148</sup> Figure 2.4a shows the chemical structure of PMMA, and (b) and (c) show the C(1s) spectrum and O(1s) spectrum, respectively, with each deconvoluted peak labelled with the corresponding carbon and oxygen components in the structure diagram. The deconvoluted peaks in the C(1s) region are located at 284.9 eV, 285.7 eV, 286.9 eV, and 289.0 eV, and the deconvoluted peaks in the O(1s) region are located at 532.1 eV and 533.6 eV, which closely align with the peak positions seen in literature for PMMA.<sup>148</sup>

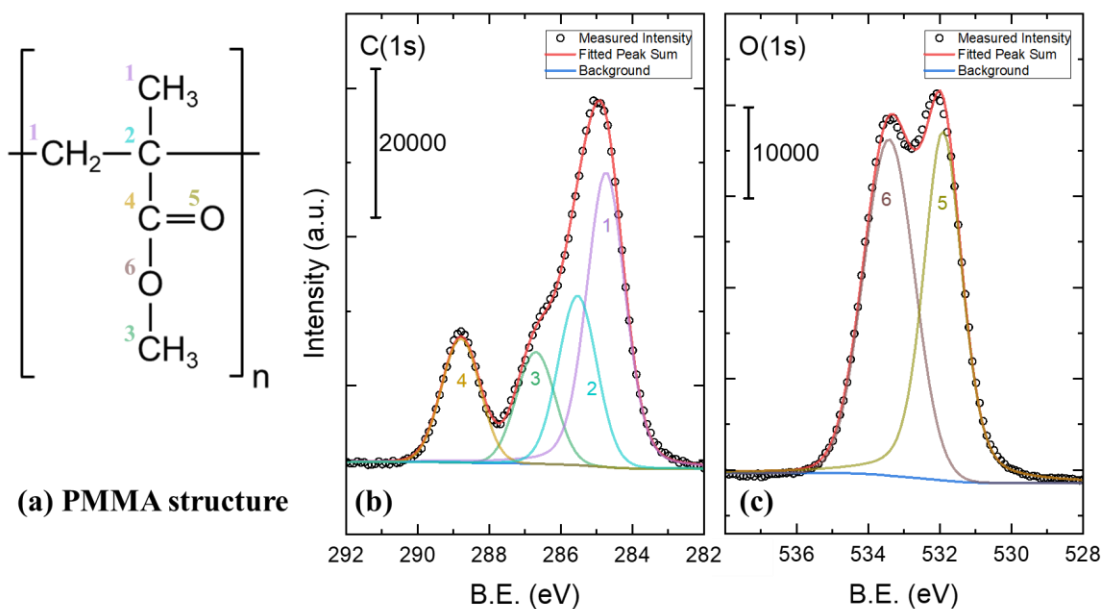


Figure 2.4. (a) PMMA chemical structure; (b) C(1s) XPS spectrum of PMMA film with fitted peaks; (c) O(1s) XPS spectrum of PMMA film with fitted peaks.

### 2.3.3 PMMA Synthesis Process Improvements

With the initial development of this surface-initiated PMMA synthesis, we were not consistently able to successfully synthesize a film, and when there was a film, the

thickness was not consistent between polymerization runs. Figure 2.5 highlights the inconsistency of PMMA film thickness between different polymerization runs. The exact same procedure was followed for Run A and Run B, yet the average film thickness of Run A is five times larger than that of Run B. To address this variability, we thoroughly investigated all relevant process parameters and possible sources of variability for each step of the polymerization and altered the procedure in a few ways.

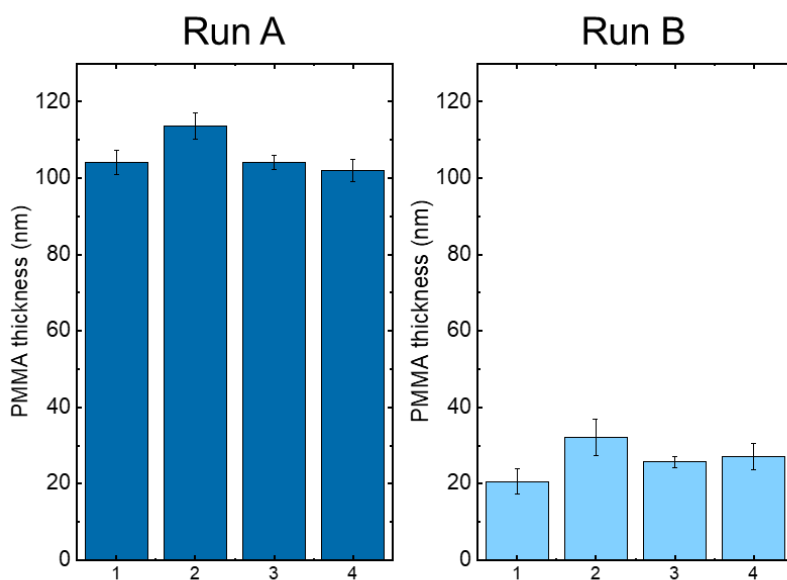


Figure 2.5. Bar graphs showing average PMMA film thickness of four samples in two different polymerization runs.

First, it is known that temperature is an important process parameter for the hydrosilylation reaction in the undecenol attachment.<sup>149</sup> We noticed deviations between the setpoint and the actual temperature on the heating block, so the block heater was switched to one with better control in the appropriate temperature range to allow for more precise control. Another step lacking precise control was the dropwise addition of BIBB for the initiator attachment since this was performed by hand with a syringe in the previous procedure. Using a pipette with a stopcock valve to add the BIBB dropwise enables the

steady addition of BIBB to each sample and allows for consistency between each polymerization run. These changes also improved the polymerization success rate significantly.

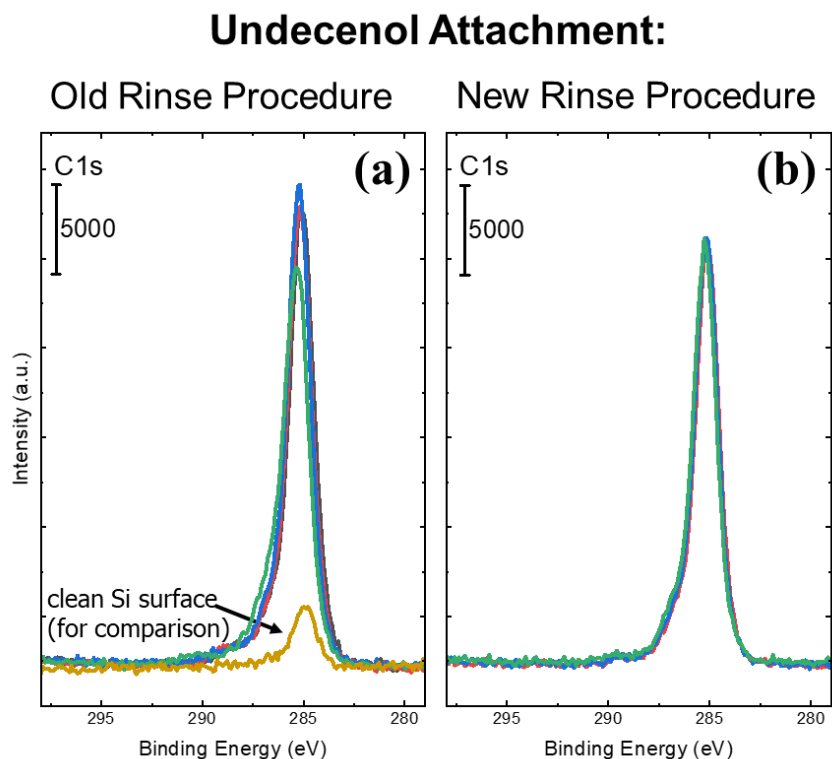


Figure 2.6. XPS scans on four samples from one run in the C(1s) region after undecenol attachment with the old (a) and new (b) rinse.

Next, the undecenol and BIBB attachment are investigated with XPS characterization. The previous procedure used only a quick mesitylene rinse after the undecenol attachment and a quick toluene rinse after the BIBB attachment. Similar polymer synthesis processes in literature use more thorough rinsing procedures with multiple consecutive solvent rinses.<sup>150-152</sup> A new rinsing procedure was investigated, consisting of three consecutive solvent rinses (toluene, acetone, methanol) for 5 minutes each. Figure 2.6 and Figure 2.7 show XPS data to investigate the impact of the new rinse procedure. Four separate samples from a single polymerization run were analyzed with

XPS after the undecenol attachment step including rinsing (Figure 2.6) and after the BIBB attachment step including rinsing (Figure 2.7). Looking at the C(1s) region for undecenol, we can see a large peak corresponding to the C-C bonds in undecenol. Figure 2.6a shows slightly different peak heights with the old rinse, indicating different amounts of undecenol on the surface. With the new rinsing procedure in Figure 2.6b, we see more consistent peaks, indicating the new rinse successfully removes any excess, unattached undecenol from the surface.

### BIBB Attachment:

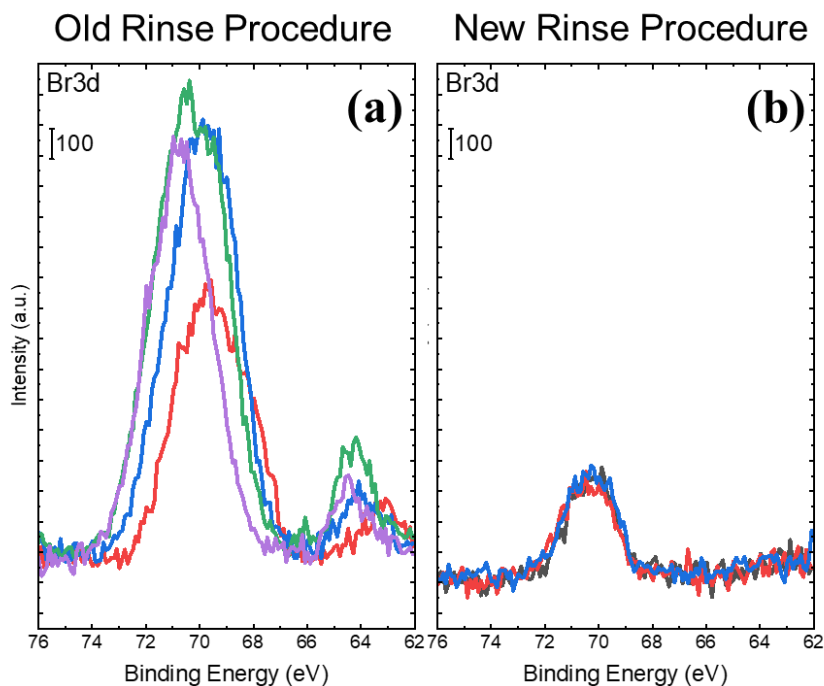


Figure 2.7. XPS scans of four samples in one run in the Br(3d) region after BIBB attachment with the old (a) and new (b) rinse.

A similar XPS experiment for the BIBB attachment step shows the same improvement, seen in Figure 2.7. Looking at the Br(3d) region, we see peaks corresponding to the bromine bond in the BIBB molecules on the surface. With the old rinse we see larger peaks with varying heights, but with the new rinse we see smaller and more consistent

peaks, again indicating the removal of excess, unattached BIBB from the surface. We ultimately determined that using a quick mesitylene rinse after the undecenol attachment and the thorough three-solvent rinse after the BIBB attachment results in consistent initiator attachment between runs (similar to the results seen in Figure 2.7b), since the thorough rinse after the BIBB step can rinse away unattached undecenol and excess BIBB simultaneously. After implementing all of these process improvements, we are now able to successfully synthesize PMMA close to 100% of the time with much more consistent film thickness between runs.

## **2.4 KOH Etch Procedure for Planar Samples**

After polymerizing a PMMA brush across the entire Si surface, the next step in the SCALES patterning process involves selectively removing PMMA from the lightly doped Si regions. It is shown in literature that the etch rate of Si with potassium hydroxide (KOH) decreases with increased dopant concentration.<sup>153</sup> This is true for both n-type and p-type Si, though there are likely different etch-stop mechanisms for n-type versus p-type Si,<sup>154,155</sup> and other parameters (e.g., Si crystal orientation, KOH concentration, and process temperature) also impact etch rate.

For both p-type and n-type Si, one generally recognized mechanism for KOH etching of Si is the competition between oxidation rate of the surface Si atoms and diffusion rate of the oxidation products into the electrolyte. When hydroxyls in the electrolyte solution react with surface Si atoms, they form an SiO<sub>x</sub> surface layer and weaken the Si bonds with the bulk Si. Then additional hydroxyl groups attack the Si, and a soluble silicate forms that diffuses into the electrolyte solution, etching away the top Si atoms. If the oxidation rate is

slower than the diffusion rate, then the oxidation products have time to diffuse into the electrolyte, and etching occurs. If the oxidation rate is faster, then the oxidation products don't have time to diffuse into the solution and an oxide layer builds up, passivating the surface and preventing further etching.<sup>156</sup> The etch stop that occurs for heavily doped Si is attributed to the enhanced oxidation rate of Si with high carrier concentration. It is suggested that heavily n-type and p-type Si can spontaneously form a thin, passivating oxide layer when exposed to aqueous KOH, and the strain in the Si surface due to the high dopant density may be responsible for the increased oxidation rate.<sup>154,155</sup>

To pattern the planar boron-doped Si substrates for self-aligned capacitors, we use a cyclic etch process involving cycles of exposure to an aqueous KOH solution followed by exposure acetone to selectively remove PMMA from the lightly doped regions. The KOH likely diffuses to the Si surface and etches away the top layer, removing the polymer chains with it, and the alternating acetone cycle helps re-solvate the PMMA chains since PMMA is not soluble in water.<sup>157</sup>

To perform the selective etch, the PMMA-covered substrates are removed from the overnight acetone rinse and then removed from the glovebox. In one cycle, the substrates are dipped in a solution containing KOH, DI H<sub>2</sub>O, and isopropyl alcohol (IPA, 99.9%, Sigma-Aldrich) in a 1:8.5:3 ratio by volume (1 mL KOH + 8.5 mL DI H<sub>2</sub>O + 3 mL IPA) for 30 seconds then removed and immediately dipped in acetone for 30 seconds. This cycle is repeated until the PMMA is fully removed from the lightly doped regions, typically requiring 25-50 cycles. The final step is a rinse with deionized (DI) H<sub>2</sub>O rinse and then the substrate is blown dry with N<sub>2</sub>.

A typical PMMA-covered boron-patterned substrate before etching can be seen in the top-left of Figure 2.8, and the following images after every 5 cycles of KOH etching illustrate the progressive removal of PMMA from the lightly boron-doped regions (inside the boxes). For this sample, after 35 cycles, we can see the bare Si surface in the large rectangle feature, but the PMMA remains intact in the heavily doped region outside of the boxes. Ellipsometry can be used at this point to measure the thickness of the remaining film, and we typically see about a 10 nm reduction from the starting film thickness. And ellipsometry typically measures 1.5-3 nm on the bare Si surface, indicating very little PMMA remaining and a thin oxide film resulting from the etch process and exposure to ambient.

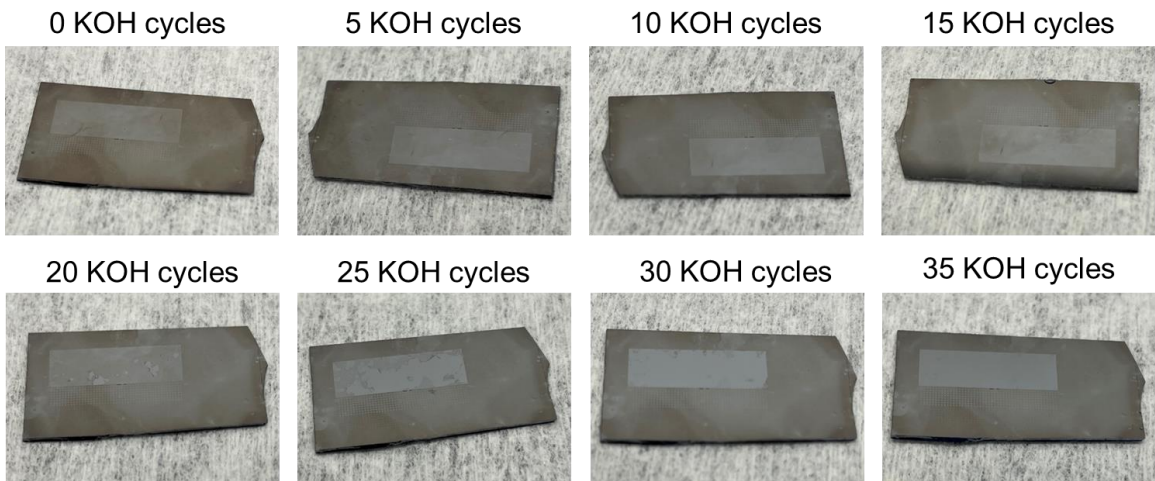


Figure 2.8. Images depicting the progressive removal of PMMA from the lightly doped regions of a boron-patterned Si substrate after 35 KOH etch cycles.

XPS, ellipsometry and optical microscopy can all be used to confirm the complete removal of the PMMA film. Figure 2.9 shows optical microscope images of a PMMA-covered boron-patterned substrate before and after KOH etching. We can clearly see that the PMMA film has been removed from the lightly doped square regions after the etch.

This procedure produces fairly consistent results with the boron-patterned Si(100) samples. Although, some samples take up to 55 or 60 cycles to fully remove PMMA from the lightly doped regions, and about 1 out of every 10 samples did not etch selectively (meaning the PMMA is etched from the whole substrate before it is removed from lightly doped regions). This is significantly better than the phosphorus-patterned samples that were prepared with the same fabrication process but did not show any consistent selective KOH etching. These inconsistencies are possibly due to non-uniformity of doping and etching during fabrication and to the difference in etch stop mechanism for p-type versus n-type Si, although we expected the phosphorus-doped samples to perform similarly to the boron-doped ones.

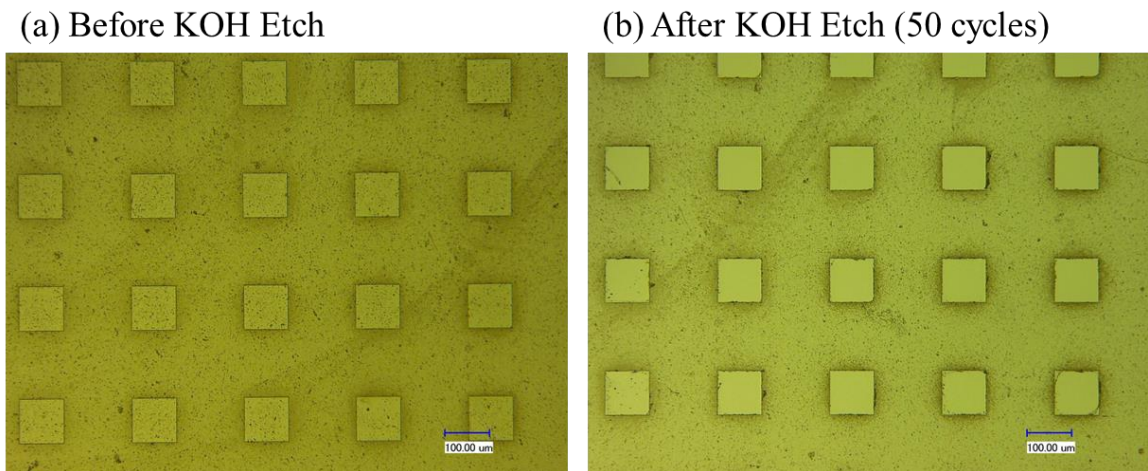


Figure 2.9. Optical microscope images of PMMA-covered boron-patterned substrate before (a) and after (b) KOH etch process.

## 2.5 Post-Patterning clean

After the SCALES patterning process, there is typically residual organic material present on the exposed Si surface, and sometimes potassium contamination from the KOH

etch is present as well. The dashed line curves in Figure 2.10 show XPS scans in the C(1s) region of a boron-patterned Si substrate after polymerization and a subsequent KOH etch. We see that PMMA has been removed from the lightly doped regions (Figure 2.10b) with only a small carbon peak left, while the PMMA remains intact on the heavily doped regions (Figure 2.10a). Additionally, the small doublet peak positioned near 294 eV can be attributed to potassium, which we have seen multiple times but not after every KOH etch.

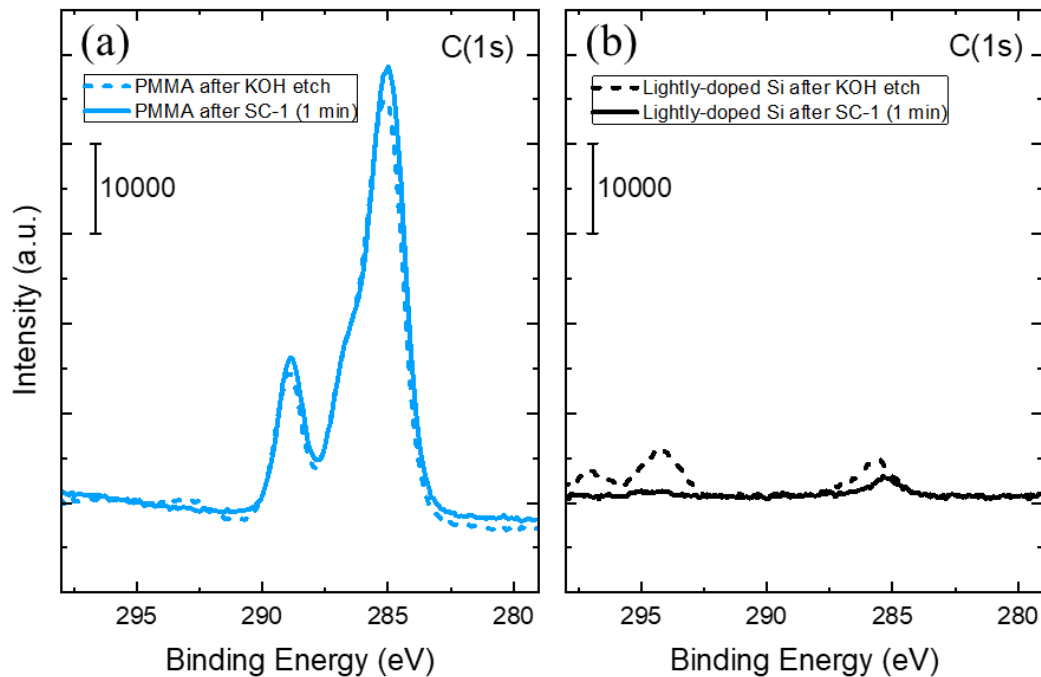


Figure 2.10. XPS characterization of PMMA film on heavily doped Si (a) and exposed lightly doped Si (b) of a boron-patterned Si substrate after KOH etch (dashed line) and after subsequent SC-1 treatment (solid line).

To address these issues, we need a surface cleaning procedure that will remove residual organics (and potassium) without destroying the patterned PMMA film. Plasma cleans, vacuum anneals, and UV/Ozone treatment can all be used to clean residual organic material,<sup>158</sup> but they are fairly aggressive treatments that will likely damage the PMMA film at the same time. Wet chemical treatments are an alternative option that are compatible

with large-scale manufacturing. While not able to selectively clean only the exposed Si, a wet chemical clean can be diluted to achieve a less aggressive treatment that might not damage the PMMA with a short exposure. The RCA cleaning process (detailed in Table 2.1) is commonly used in semiconductor fabrication and has steps to remove both organic and ionic contaminants. Cleaning the semiconductor surface prior to gate stack fabrication is essential to achieve a clean semiconductor-oxide interface, so an RCA clean is a practical option to remove PMMA residue, remove ionic contamination, and clean the exposed Si surface. However, the full 10 min organic clean (SC-1) fully stripped the PMMA film in some experiments. So a diluted SC-1 solution (5 DI H<sub>2</sub>O:1 H<sub>2</sub>O<sub>2</sub>:**0.25 NH<sub>4</sub>OH**) is used,<sup>159</sup> and the treatment length is shortened from 10 min to 1 min. This modified RCA clean with a dilute SC-1 treatment successfully cleans the Si surface and removes any lingering potassium contamination, as evidenced by the small reduction in peak height of the C(1s) peak and the disappearance of the K2p doublet in the XPS spectra in Figure 2.10b. Ending the RCA clean with the SC-2 step leaves a thin passivating SiO<sub>2</sub> film on the exposed Si surface. This oxide can serve as an interlayer between the Si substrate and deposited HfO<sub>2</sub> for an MOS structure, or it can be removed before using alternate surface oxidation techniques, which will be further discussed in CHAPTER 5.

## CHAPTER 3. AREA-SELECTIVE ATOMIC LAYER DEPOSITION PROCESS DEVELOPMENT

Depositing a self-aligned MOS gate stack structure requires selective deposition of an oxide film on a semiconductor surface followed by selective deposition of a metal on the oxide. The major challenge with that goal is finding a material system that enables selective deposition of both an oxide and a metal that will also function well as an MOS capacitor. CHAPTER 2 describes the SCALES process we use to pattern a planar Si substrate with a PMMA film that aligns with the underlying dopant pattern. The next step is to combine SCALES patterning with AS-ALD to deposit a gate stack structure that functions as an MOS capacitor. The following sections discuss the development of the ALD processes for our self-aligned Pt/HfO<sub>2</sub>/Si MOS structures.

### 3.1 Oxide Atomic Layer Deposition

#### 3.1.1 AS-ALD Gate Oxide Selection

As seen in Section 1.4.1, there are many examples of selective oxide deposition via AS-ALD, especially with spincoated PMMA films<sup>60</sup>. We first aim to investigate selectivity of deposition with a few readily available options in the cleanroom. Using the Cambridge ALD system (Cambridge NanoTech Fiji F202 ALD) in the Marcus Cleanroom, we tested deposition of four different oxides: titanium dioxide (TiO<sub>2</sub>/titania), zirconium dioxide (ZrO<sub>2</sub>/zirconia), aluminum oxide (Al<sub>2</sub>O<sub>3</sub>, alumina), and hafnium dioxide (HfO<sub>2</sub>/hafnia). Three types of substrates were prepared: H-terminated Si(100) (treated with 1% HF for 30 sec prior to deposition), Si(100) with native oxide, and PMMA-covered Si(100) (a 40-60 nm film synthesized via surface-initiated polymerization). Since plasma processes and high

temperatures can damage PMMA films, only thermal ALD recipes are used at 200 °C with argon as the purge gas. The standard recipes developed by the IEN cleanroom staff were used since they have been optimized for this particular system, and the precursors for TiO<sub>2</sub>, ZrO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, and HfO<sub>2</sub> are tetrakis(dimethylamido)titanium(IV) (TDMAT), tetrakis(dimethylamido)zirconium(IV) (TDMAZr), trimethylaluminum (TMA), and tetrakis(dimethylamido)hafnium(IV) (TDMAHf), respectively, with H<sub>2</sub>O as the oxidizer. The ALD process parameters for each oxide are listed below in Table 3.1.

Table 3.1. ALD process parameters for oxide deposition.

	<b>Precursors (A, B)</b>	<b>A pulse (sec)</b>	<b>Purge (sec)</b>	<b>B pulse (sec)</b>	<b>Purge (sec)</b>	<b>Temp (°C)</b>	<b>Cycles</b>
TiO <sub>2</sub>	H <sub>2</sub> O, TDMAT	0.06	15	0.2	30	200	60
ZrO <sub>2</sub>	H <sub>2</sub> O, TDMAZr	0.06	15	0.06	15	200	60
Al <sub>2</sub> O <sub>3</sub>	H <sub>2</sub> O, TMA	0.06	20	0.06	20	200	60
HfO <sub>2</sub>	H <sub>2</sub> O, TDMAHf	0.06	15	0.25	20	200	60

According to ellipsometry measurements, the Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub> and ZrO<sub>2</sub> films were about 6 nm thick and the TiO<sub>2</sub> film about 3.5 nm thick, with similar values for the H-terminated Si and Si with native oxide. As we can see from XPS characterization in Figure 3.1, the TiO<sub>2</sub>, ZrO<sub>2</sub>, and HfO<sub>2</sub> films all exhibit good selective deposition, with significant peaks in the appropriate XPS region on the H-terminated Si and Si with native oxide and almost no peak on the PMMA-covered Si, indicating very little deposition. The HfO<sub>2</sub> and ZrO<sub>2</sub> samples do show very small peaks on the PMMA substrate, but they are insignificant compared to the other substrates. The Al<sub>2</sub>O<sub>3</sub> film, however, shows very little selectivity in deposition, with clear peaks on all three substrates. The TMA precursor used for Al<sub>2</sub>O<sub>3</sub> is smaller than the other three precursors and is known to infiltrate polymer films in the vapor phase, which likely enables better nucleation of a film.<sup>160-162</sup> While TiO<sub>2</sub> did show the best

selectivity with no deposition on PMMA, it typically has a high gate leakage and is therefore not a good option for a gate dielectric.<sup>163</sup> Since HfO<sub>2</sub> showed good selectivity with the PMMA brush and is a well-studied high- $\kappa$  dielectric commonly used in electronic applications,<sup>94,164</sup> it was selected as the best option for the self-aligned gate oxide material.

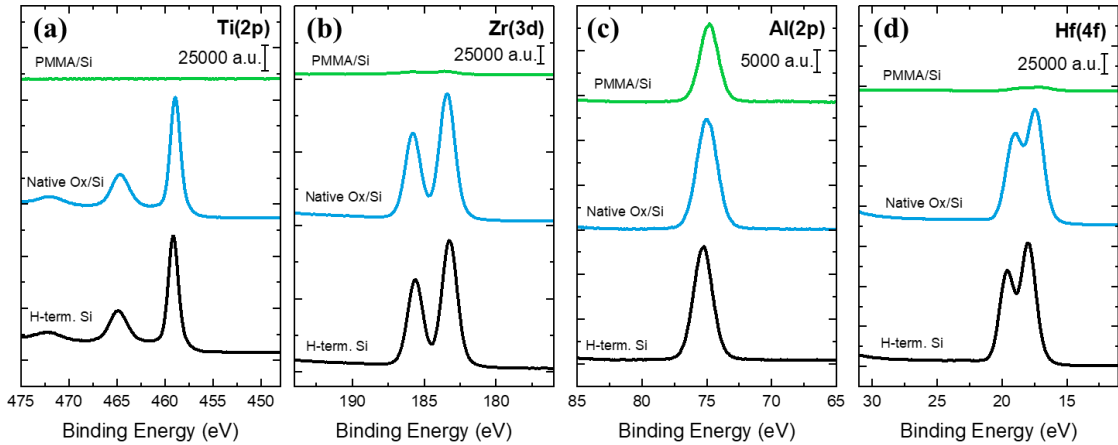


Figure 3.1. XPS data to investigate selectivity of deposition for four oxides on H-terminated Si, Si with native oxide, and PMMA-covered Si samples: (a) TiO<sub>2</sub> ALD; (b) ZrO<sub>2</sub> ALD; (c) Al<sub>2</sub>O<sub>3</sub> ALD; and (d) HfO<sub>2</sub> ALD.

### 3.1.2 Characterizing Spatial Selectivity of AS-ALD with Patterned PMMA Films

After selecting HfO<sub>2</sub> for the self-aligned gate oxide, we next wanted to investigate the area-selective deposition of HfO<sub>2</sub> with a patterned PMMA film. As a preliminary experiment, before the development of SCALES patterning with boron-patterned Si substrates, a PMMA-covered substrate was patterned with photolithography and reactive ion etching (Advanced Vacuum Vision 320 RIE) with oxygen plasma (50 SCCM, 150 W, 3 min) to etch the polymer film. After patterning the PMMA, HfO<sub>2</sub> was deposited via thermal ALD with the recipe in Table 3.1, and then the remaining PMMA was etched away with the same O<sub>2</sub> plasma process.

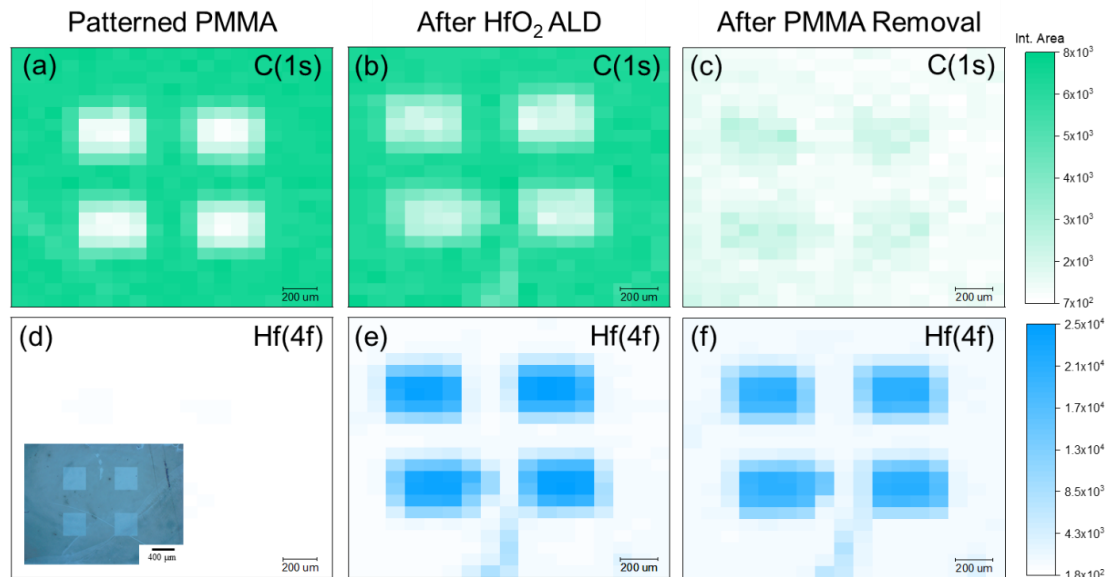


Figure 3.2. XPS area maps of a selectively deposited  $\text{HfO}_2$  film. Each pixel indicates the integrated area of one XPS scan. PMMA was removed with an  $\text{O}_2$  plasma etch. (a-c) Area map of  $\text{C}(1s)$  photoelectron spectra indicating presence of PMMA; (d-f) Area map of  $\text{Hf}(4f)$  photoelectron spectra indicating presence of  $\text{HfO}_2$ . Inset in (d) is an optical microscope image of the patterned PMMA film on Si.

To examine the spatial selectivity of deposition, XPS area mapping was used for characterization. The XPS area maps are shown in Figure 3.2, with the  $\text{C}(1s)$  spectra (a-c) and  $\text{Hf}(4f)$  spectra (d-f) after each step (i.e., patterned PMMA film with  $\text{O}_2$  plasma,  $\text{HfO}_2$  ALD, PMMA removal with  $\text{O}_2$  plasma). To construct the XPS area maps, the  $\text{C}(1s)$  and  $\text{Hf}(4f)$  photoelectron spectra were collected across a 1.8 mm by 2 mm area (one scan per pixel, 30  $\mu\text{m}$  spot size). The background was removed in MATLAB using a spline approximation (`msbackadj` function), and the pixels indicate the integrated area of intensity at each point. The large pixel size and less-defined edges come from the 30  $\mu\text{m}$  spot size, which was difficult to align well with the pattern edges, leading to intermediate intensity values at the pattern edges. However, despite the poor resolution, we can still clearly see the pattern in the PMMA film in (a) and (b) and the subsequent removal of the PMMA in

(c). And in the Hf(4f) spectra, we can see the deposition of HfO<sub>2</sub> primarily in the exposed Si squares in (e).

EDS maps are a good alternative for compositional mapping with better resolution than the XPS map. An SEM image and EDS maps of the same PMMA patterned Si after HfO<sub>2</sub> ALD are shown in Figure 3.3. The C Kα1 map in Figure 3.3d clearly demonstrates the striped PMMA pattern, and the Hf map shows a stronger intensity inside the HfO<sub>2</sub> stripes, indicating HfO<sub>2</sub> deposition in between the PMMA stripes. The extra noise in the Hf Mα1 scan is due to overlap with a large Si signal from the Si substrate.

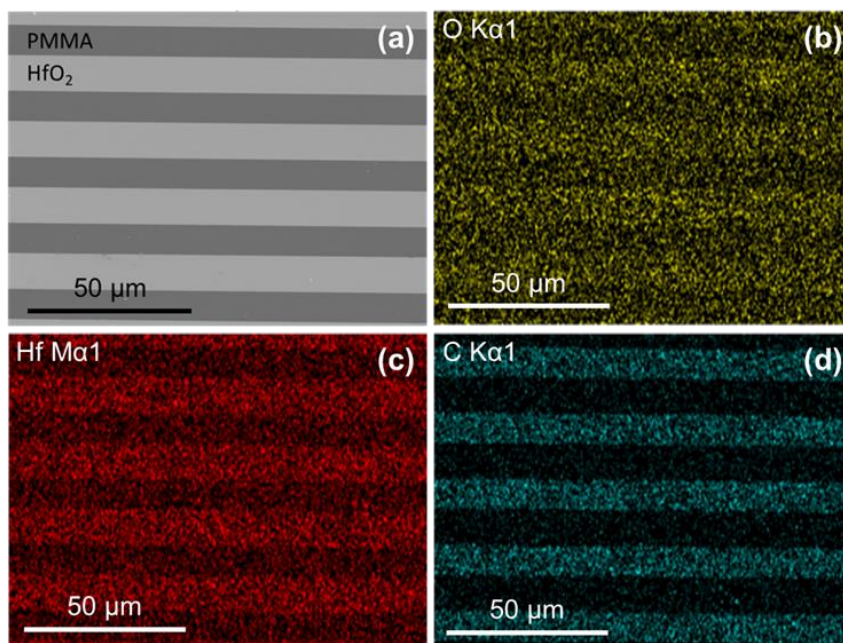


Figure 3.3. (a) SEM image of AS-ALD HfO<sub>2</sub> on Si substrate patterned with PMMA; (b-c) EDS elemental mapping of O, Hf, and C.

## 3.2 Metal Atomic Layer Deposition

### 3.2.1 AS-ALD Gate Metal Selection

Selective deposition of a metal gate electrode on top of the high- $\kappa$  dielectric is required to form the complete MOS structure. While AS-ALD of metals is less studied in literature than oxides, there are still plenty of examples, including Ru<sup>67</sup> and Rh<sup>73</sup> for capacitor structures, as well as Pt,<sup>28</sup> Ni,<sup>26</sup> Co,<sup>68</sup> and TiN<sup>165</sup> with SAM-deactivated surfaces. Pt in particular has been deposited selectively with polymer films (i.e., PMMA<sup>60</sup> and poly(vinyl pyrrolidone)<sup>71</sup>). TiN would also be a suitable option due to its versatility since the effective work function can be tuned with annealing conditions.<sup>166</sup> ALD precursors for both Pt and TiN are readily available on the same Cambridge ALD system used for the oxides, and both materials have been shown to function well as gate electrodes.<sup>167,168</sup>

One major drawback, however, is that the standard cleanroom recipes for both Pt and TiN use plasma-enhanced ALD (PE-ALD). The TiN recipe on our system uses TDMAT and N<sub>2</sub> plasma, and the plasma is required since we do not have ammonia (NH<sub>3</sub>) gas hooked up to the system. Although the Cambridge ALD system uses a remote plasma source, an initial selectivity test of TiN indicates damage to the PMMA film during deposition. TiN was deposited via 60 cycles of PE-ALD at 200 °C on the same three substrates as the oxide experiment [i.e., H-terminated Si(100), Si(100) with native oxide, and PMMA-covered Si(100)]. The TiN recipe consists of a pulse of TDMAT for 0.2 sec, a 10 sec purge, exposure to N<sub>2</sub> plasma (40 SCCM, 300 W) for 20 sec, and a 5 sec purge. XPS characterization seen in Figure 3.4 of the Ti(2p) photoelectron spectrum shows Ti peaks on all three substrates, indicating no selective deposition. Ellipsometric measurements of

the PMMA film show a reduction in film thickness from 50 nm to 5 nm, so the PMMA was likely damaged by the plasma and no longer served to deactivate the Si surface. TiN ALD could potentially be a viable option for future work if a non-plasma ALD precursor, such as  $\text{NH}_3$ , is available.

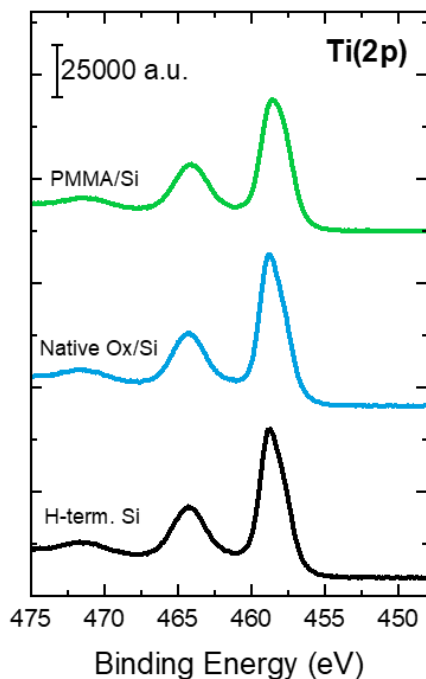


Figure 3.4. XPS characterization to investigate selectivity of deposition of TiN PE-ALD on H-terminated Si, Si with native oxide, and PMMA-covered Si.

The standard Pt PE-ALD recipe uses trimethyl(methylcyclopentadienyl)-platinum(IV) ( $\text{MeCpPtMe}_3$ ) and  $\text{O}_2$  plasma (20 SCCM, 300 W), with exposure times of 1 sec and 10 sec, respectively, with 10 sec purges. An initial deposition experiment was performed to test the recipe with 100 cycles of the plasma recipe at 200 °C on Si with native oxide. XPS characterization of the Pt(4f) spectrum shows a large doublet at 71 eV, indicating deposition of Pt metal (Figure 3.5a). However, when the same recipe was run (without pulsing Pt to conserve the precursor) to investigate the impact of the plasma on a PMMA-covered Si substrate, the PMMA film decreased in thickness from 90 nm to 2 nm.

And XPS characterization of the C(1s) spectrum shows a large decrease in carbon peak height after the plasma exposure (Figure 3.5b).

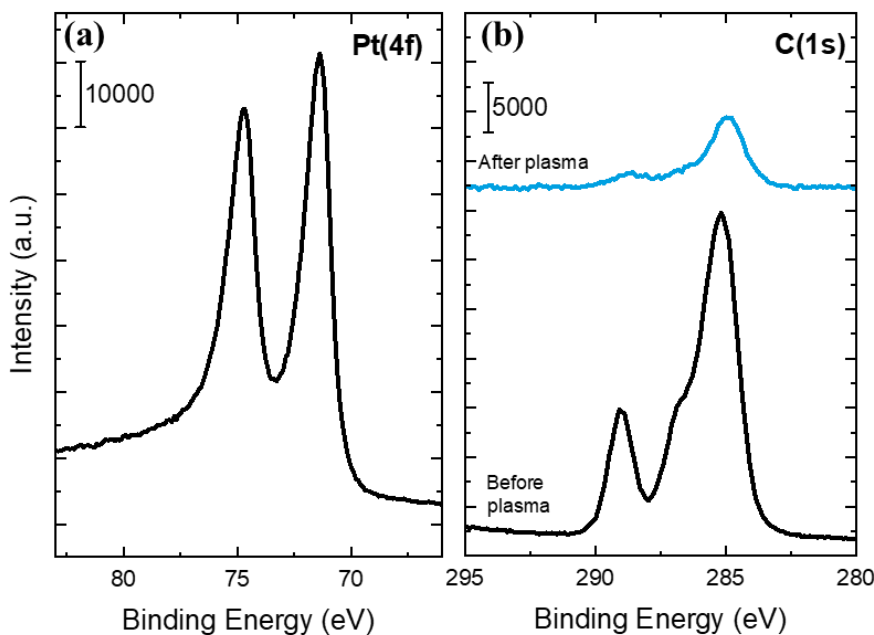


Figure 3.5. XPS characterization to investigate the PE-ALD of Pt: (a) a large doublet in the Pt(4f) photoelectron spectrum indicates deposition of Pt metal on Si with native oxide substrate; (b) C(1s) spectra showing degradation of PMMA due to plasma process.

### 3.2.2 Developing Thermal Pt ALD Recipe

Although the IEN cleanroom standard Pt ALD recipe uses MeCpPtMe<sub>3</sub> and O<sub>2</sub> plasma, it has been widely shown in literature that Pt can be deposited via thermal ALD with MeCpPtMe<sub>3</sub> and O<sub>2</sub> gas.<sup>39,169</sup> After reviewing examples of thermal Pt ALD with MeCpPtMe<sub>3</sub> and oxygen gas in the literature,<sup>168,170</sup> a recipe was developed for thermal ALD of Pt at 300 °C consisting of a 1 sec and 10 sec exposure to MeCpPtMe<sub>3</sub> and O<sub>2</sub> (20 SCCM), respectively, with 10 sec purges in between. The background argon flow was reduced from the standard 280 SCCM to 140 SCCM to lengthen residence time of the precursors.

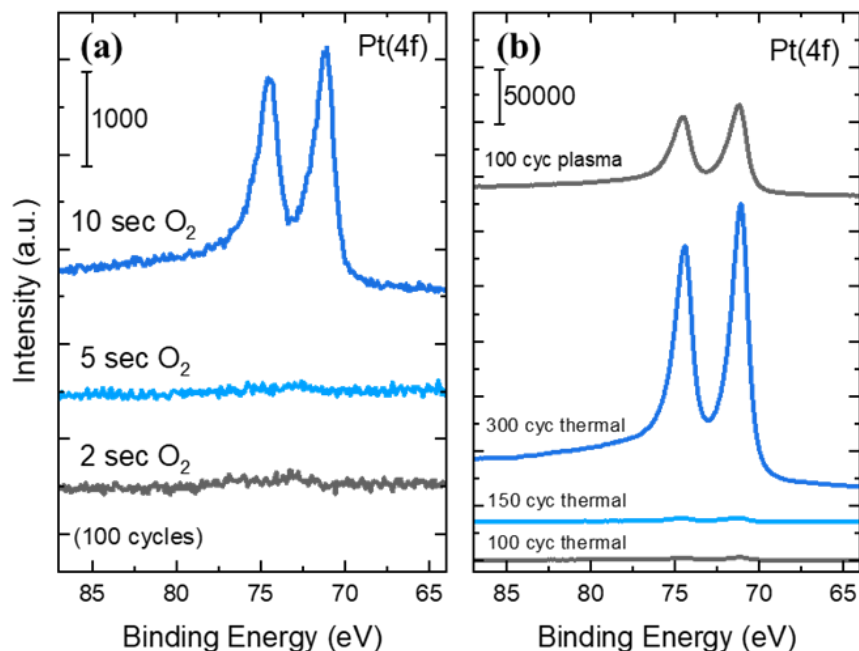


Figure 3.6. Pt(4f) XPS characterization to investigate thermal ALD of Pt: (a) XPS characterization to investigate length of O<sub>2</sub> exposure for thermal ALD of Pt; (b) XPS characterization of 100, 150, and 300 cycles of thermal ALD compared with 100 cycles of plasma ALD.

XPS characterization of Pt films on Si(100) with native oxide is shown in Figure 3.6. In Figure 3.6a, the optimal O<sub>2</sub> exposure time is investigated by comparing Pt(4f) XPS spectra after 100 cycles of thermal ALD with various O<sub>2</sub> exposure times (e.g., 2 sec, 5 sec, and 10 sec). No Pt peaks are perceptible for 2 sec and 5 sec O<sub>2</sub> exposures, but we do see a doublet at 71 eV with the 10 sec exposure, indicating Pt metal deposition. A full investigation of the optimal Pt and O<sub>2</sub> exposure times was not performed to obtain a saturation curve for the sake of conserving the expensive and somewhat limited supply of Pt precursor. However, after testing the 1 sec Pt exposure and 10 sec O<sub>2</sub> exposure thermal recipe for 100, 150 and 300 cycles, we do see successful deposition of a coalesced Pt film (seen in Figure 3.7a), which should be sufficient for the metal gate electrode. From the SEM cross section in Figure 3.7b, the Pt film appears to be ~20 nm thick after 300 cycles.

This agrees with profilometry measurement across a scratch in the film. And looking at the XPS spectra in Figure 3.6b, we see a very small doublet at 71 eV after 100 and 150 cycles of thermal ALD, indicating a small amount of deposition. But after 300 cycles of thermal ALD, we get a much thicker film, which correlates with the much larger Pt(4f) doublet. This XPS data does suggest a fairly large nucleation delay for thermal Pt ALD, especially when comparing the XPS spectra for 100 cycles of thermal ALD with 100 cycles of plasma ALD, which is also seen in literature.<sup>171</sup> But with a sufficient number of cycles (i.e., 300 cycles), an adequate film can be deposited on both native SiO<sub>2</sub> and HfO<sub>2</sub> covered substrates (Figure 3.7).

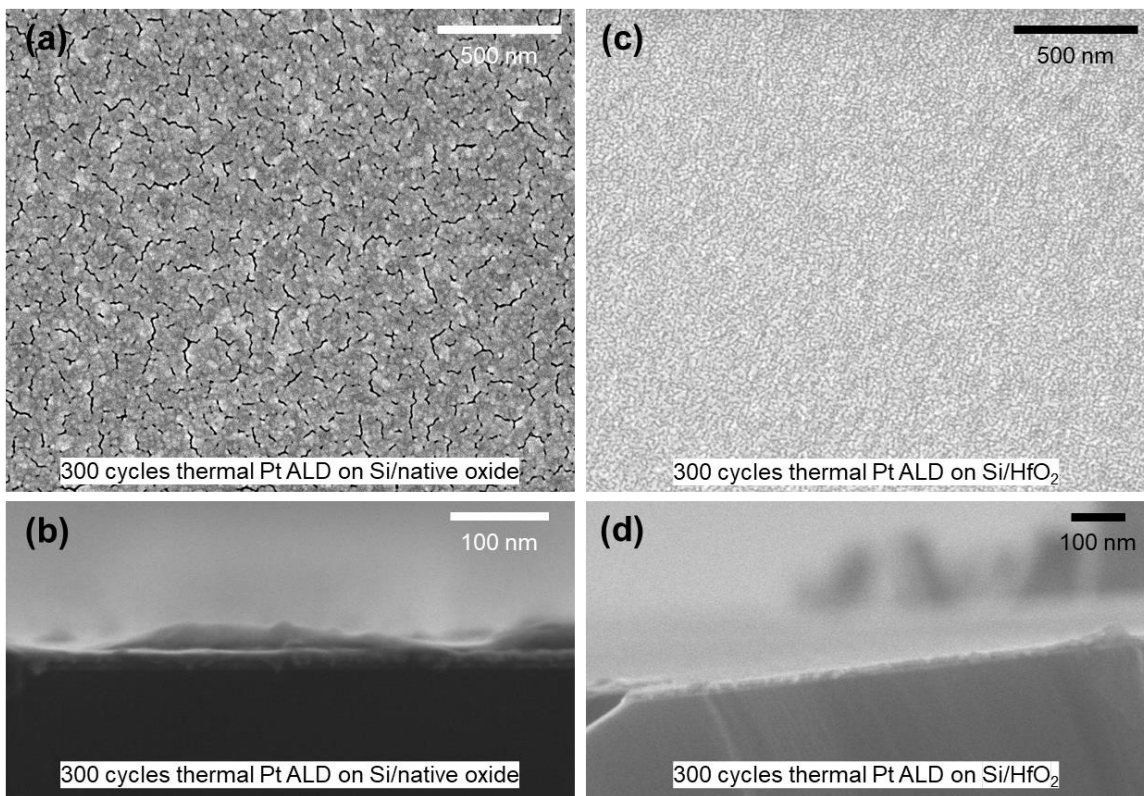


Figure 3.7. Top-down (a) and cross-sectional (b) SEM images of Pt film on Si with native oxide deposited via 300 cycles of thermal ALD; Top-down (c) and cross-sectional (d) SEM images of Pt film on Si with ~5 nm HfO<sub>2</sub> deposited via 300 cycles of thermal ALD.

### 3.2.3 *Area-Selective ALD of Pt*

After developing a thermal ALD recipe to deposit Pt, we next need to investigate selectivity of Pt deposition with PMMA as a deactivating mask. Deposition of Pt was studied on four different surfaces: PMMA-covered Si, HfO<sub>2</sub> on Si, ZrO<sub>2</sub> on Si, and Si with native oxide. After depositing 300 cycles of thermal Pt ALD at 300 °C, XPS characterization shows significant presence of Pt on all three oxide-covered samples and no clear indication of Pt on PMMA, seen in Figure 3.8a. And from looking at the C(1s) XPS spectra (in Figure 3.8b), we still see carbon peaks corresponding to PMMA, indicating that the approximately one hour long thermal recipe at 300 °C does not degrade the PMMA film. Additionally, the PMMA sample was exposed to O<sub>2</sub> plasma after ALD, and XPS spectra showed no significant presence of Pt underneath the Pt film. After establishing successful AS-ALD of Pt using the surface-initiated PMMA, we can next combine all the process steps detailed in CHAPTER 2 and CHAPTER 3 (i.e., SCALES patterning on planar substrates, AS-ALD of HfO<sub>2</sub>, and AS-ALD of Pt) to fabricate fully self-aligned MOS gate stack structures.

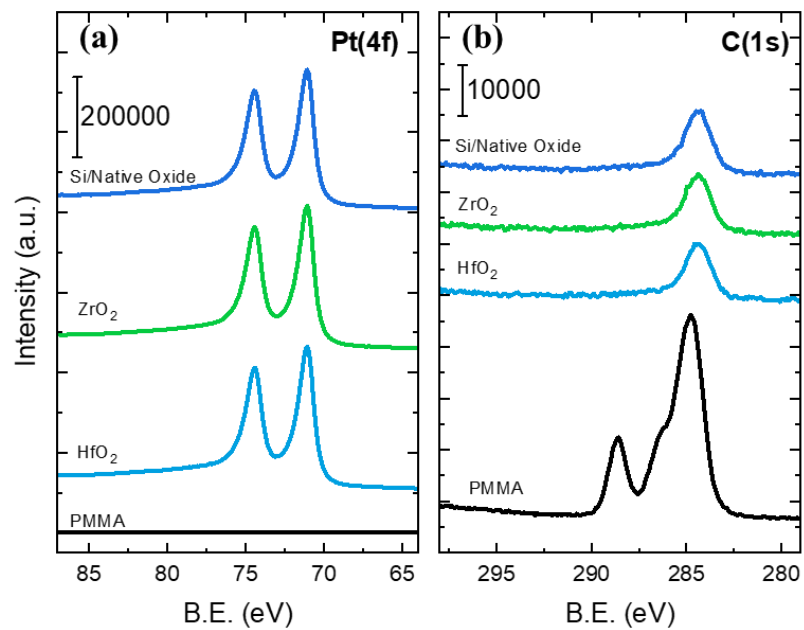


Figure 3.8. XPS characterization of thermal Pt ALD on different surfaces of the Pt(4f) photoelectron spectra (a) and the C(1s) photoelectron spectra (b).

## CHAPTER 4. DEPOSITING A SELF-ALIGNED GATE STACK STRUCTURE USING SCALES PATTERNING COMBINED WITH AS-ALD<sup>1</sup>

In this chapter a metal-oxide-semiconductor gate stack that is self-aligned with the underlying silicon doping profile is demonstrated. We combine a new hybrid bottom-up patterning technique with atomic layer deposition to selectively deposit a platinum-hafnium dioxide-silicon MOS gate stack. A PMMA brush is blanket grown from a Si(100) surface and selectively removed from the lightly-doped ( $\sim 10^{18} \text{ cm}^{-3}$ ) regions using a doping-selective KOH etch. The PMMA brush that remains on the heavily-doped ( $\sim 10^{20} \text{ cm}^{-3}$ ) regions effectively blocks the ALD of both  $\text{HfO}_2$  and platinum. MOS capacitors exhibit promising capacitance-voltage characteristics, with a  $\text{HfO}_2$  dielectric constant of  $\sim 25$  and an average interface state density of  $2.1 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$  following forming gas anneal.

### 4.1 Introduction

One of the critical issues for the fabrication of high-performance silicon transistors is the alignment between the edge of the gate stack and the edge of the underlying doped source-drain regions of the silicon channel. Too much overlap results in a large fringe capacitance and a reduction in device speed while too much underlap can result in too large of an access or series resistance.<sup>172,173</sup> Achieving an optimized alignment within an integrated high- $\kappa$ /metal gate stack can require complicated integration schemes such as the

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<sup>1</sup> Adapted from Brummer A. C. Brummer, A. T. Mohabir, D. Aziz, M. A. Filler, and E. M. Vogel, Appl. Phys. Lett. 119, 142901 (2021); <https://doi.org/10.1063/5.0062163>, with the permission of AIP Publishing. Copyright 2021 AIP Publishing.

replacement metal gate technique.<sup>174</sup> The processing and integration becomes even more challenging for gate all around (GAA) transistors with either lateral<sup>175</sup> or vertical silicon nanowires<sup>176</sup> where numerous process steps are required to align the gate stack over the channel.

The overall objective of this work is to develop a process that aligns an MOS gate stack to the underlying channel based only on its compositional doping pattern, largely irrespective of the geometry. As a first step to achieving this objective, we combine a new hybrid bottom-up patterning technique with area-selective atomic layer deposition to deposit hafnium dioxide (HfO<sub>2</sub>) and platinum (Pt) thin films based on the local carrier concentration of a Si wafer to fabricate a high-quality planar MOS capacitor. The availability of self-aligned device structures, such as MOS capacitors, would be valuable for a variety of emerging device applications, like vertical nanowire transistors monolithically integrated into the back end of line (BEOL)<sup>177</sup> and flexible electronics requiring lower temperature processes and alternative patterning techniques that are more scalable than conventional photolithography.<sup>178</sup> This work demonstrates a patterning and deposition technique that could be further developed to fabricate devices for such applications.

Atomic layer deposition allows for the area-selective and low temperature deposition of thin films intimately aligned with compositional patterns of the underlying substrate, largely irrespective of the geometry. The most common techniques for AS-ALD involve the use of self-assembled monolayers<sup>26,63-68,179</sup> or other polymeric materials<sup>59,60,70,71,74,180</sup> to mask the surface by preventing ALD precursors from chemisorbing. These techniques often require photolithography to pattern the surface

modification layer<sup>26,60,70,71</sup> or use surfaces patterned with different materials<sup>63,66,74,181</sup> to apply the masking material selectively based on the underlying substrate. For example, a SAM can be assembled only on silicon dioxide (SiO<sub>2</sub>) regions of a patterned silicon wafer, leaving hydrogen-terminated silicon exposed.<sup>63</sup> This allows for deposition of self-aligned features based on the underlying substrate but requires the underlying materials (silicon and SiO<sub>2</sub>) to have significantly different properties.

There are a number of challenges associated with the AS-ALD of a high-performance MOS gate stack. For BEOL and flexible electronics, one needs low temperatures and AS-ALD is well suited in this regard.<sup>61</sup> However, a high-performance gate stack needs high-quality materials and low defect density interfaces. While there has been some electrical characterization of AS-ALD films in the literature,<sup>58,59,66,67</sup> there have been relatively few AS-ALD studies for such applications. In many cases, a self-aligned gate stack also requires selective deposition on chemically similar materials with only variation in dopant concentration designating the pattern (e.g., source/channel/drain), which is currently difficult to achieve with AS-ALD.

## 4.2 Methods

In this work, we combine a new hybrid bottom-up patterning technique with AS-ALD to deposit HfO<sub>2</sub> and Pt thin films based on the local carrier concentration of a Si wafer. The patterning technique is a derivative of selective co-axial lithography via etching of surfaces (SCALES),<sup>4</sup> which was originally demonstrated on cylindrical nanowires (hence co-axial) but is equally amenable to planar substrates. The SCALES technique begins with the blanket growth of a polymer brush, followed by its selective removal based on differences in the etch rate of the underlying substrate. This work uses a PMMA brush

chemically bonded to the silicon surface, as an alternative to the more commonly used spin-coated PMMA, which allows for selective removal based on the underlying Si carrier concentration by leveraging the selective etch properties of KOH.<sup>153</sup> KOH diffuses through the PMMA, removing a few layers of lightly-doped Si, which also removes the PMMA from these regions. The PMMA remains on the heavily-doped Si, serving as a mask. There are many masking materials, from SAMs to polymers, that are likely useful depending on the situation. Here, we study the model polymer PMMA to demonstrate key process steps, but we expect a variety of derivative methods will work as well. Using the SCALES patterning technique with PMMA in combination with AS-ALD, we fabricate a self-aligned gate stack with promising capacitance-voltage characteristics.

Si(100) with doping levels of  $\sim 10^{18} \text{ cm}^{-3}$  (lightly-doped) and  $\sim 10^{20} \text{ cm}^{-3}$  (heavily-doped) is used as the substrate to mimic a typical MOSFET structure. A lightly boron-doped Si(100) wafer is patterned with a 500 nm-thick SiO<sub>2</sub> mask before being doped with boron via solid state diffusion (2 h at 1050 °C, B<sub>2</sub>O<sub>3</sub> source). The masked regions (100 μm x 100 μm squares and a large 4 mm x 6 mm rectangle for XPS characterization) remain lightly-doped while the rest of the Si substrate is heavily boron-doped. A PMMA brush is synthesized to deactivate the Si surface using an adaptation of a previously described procedure.<sup>4</sup> Briefly, an anchoring molecule (11-undecen-1-ol) is attached to the hydrogen-terminated Si surface via hydrosilylation at 150 °C for 2 hours. Next, an initiating group (bromoisobutryl bromide) is attached at room temperature for 2 hours. Finally, PMMA is polymerized at 90 °C for 4 hours via atom transfer radical polymerization of methyl methacrylate. The PMMA brush is selectively removed from the lightly-doped regions via

cycles of exposure to KOH solution (1 mL 45 wt% KOH : 3 mL IPA : 8.5 mL DI H<sub>2</sub>O) to etch the Si and acetone to solvate the PMMA.

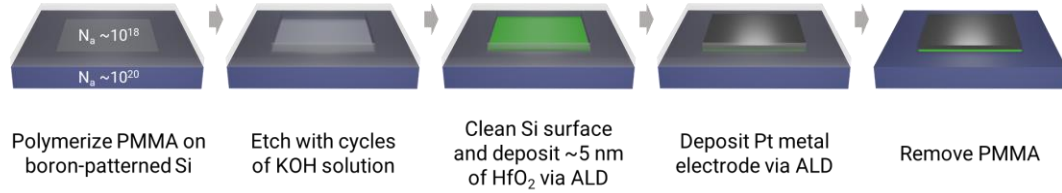


Figure 4.1. Schematic diagram of the fabrication process to make self-aligned MOS capacitors.

To fabricate a gate stack leveraging the SCALES-patterned PMMA mask, HfO<sub>2</sub> and Pt are deposited via AS-ALD. A modified RCA clean consisting of 1 min in SC-1 (5 DI H<sub>2</sub>O : 1 H<sub>2</sub>O<sub>2</sub> : 1 NH<sub>4</sub>OH) at 75 °C, 30 sec HF etch, and 10 min in SC-2 (5 DI H<sub>2</sub>O : 1 H<sub>2</sub>O<sub>2</sub> : 1 HCl) at 75 °C is used to clean the exposed Si before depositing the oxide and metal layers. The organic SC-1 clean is shortened to one minute to minimize damage to the patterned PMMA film, and the SC-2 clean forms a ~ 2 nm-thick passivating layer of chemical oxide on the Si surface. HfO<sub>2</sub> is then deposited selectively with 60 cycles of thermal ALD using tetrakis(dimethylamido)hafnium (TDMAHf) and H<sub>2</sub>O precursors at 200 °C. The exposure times for TDMAHf and H<sub>2</sub>O are 0.25 and 0.06 s, respectively, followed by purge times of 20 and 15 s. Immediately following HfO<sub>2</sub> deposition, platinum is selectively deposited with 300 cycles of thermal ALD using trimethyl(methylcyclopentadienyl)platinum(IV) (MeCpPtMe<sub>3</sub>) and O<sub>2</sub> precursors at 300 °C. The exposure times for MeCpPtMe<sub>3</sub> and O<sub>2</sub> are 1 and 10 s, respectively, followed by purge times of 10 s. All materials are deposited with a Cambridge Fiji ALD system with argon as a carrier/purging gas and a total chamber pressure of 0.45 Torr. A schematic

diagram of the full fabrication process flow is shown in Figure 4.1, and an image of a completed self-aligned MOS capacitor sample on a boron-patterned Si substrate is shown in Figure 4.2.

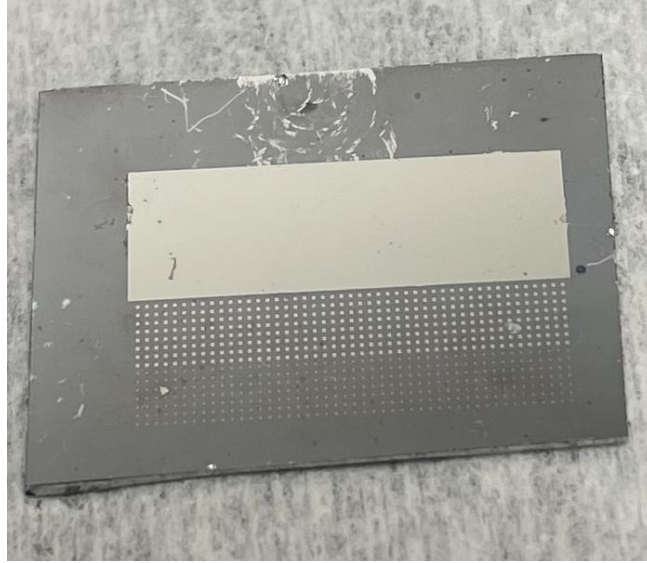


Figure 4.2. Image of boron-patterned Si substrate with self-aligned AS-ALD Pt-HfO<sub>2</sub>-Si MOS capacitors (small squares are 50  $\mu\text{m}$  x 50  $\mu\text{m}$  capacitors, large squares are 100  $\mu\text{m}$  x 100  $\mu\text{m}$  capacitors, and large rectangle for XPS is 4,000  $\mu\text{m}$  x 12,000  $\mu\text{m}$ ).

### 4.3 Results and Discussion

X-ray photoelectron spectroscopy (XPS) is used to characterize the selective removal of PMMA from the lightly-doped silicon. The XPS measurements are conducted using a monochromatic Al K $\alpha$  source with a spot size of 400  $\mu\text{m}$  and pass energy of 50 eV. Figure 4.3 shows typical C(1s) XPS spectra for the heavily- and lightly-doped silicon immediately after the polymerization process and after 25 etch cycles. After polymerization (Figure 4.3a), both the heavily- and lightly-doped silicon show strong C(1s) peaks characteristic of PMMA. It is known that the C(1s) photoelectron spectrum shows

four strong peaks for PMMA corresponding to the C-C/C-H, C in  $\alpha$ -position to the ester group, C-O, and O-C=O components at 285.0 eV, 285.7 eV, 286.8 eV, 289.1 eV, respectively.<sup>148,182</sup> Following 25 etch cycles (Figure 4.3b), the C(1s) spectrum is unchanged for the heavily-doped silicon, while the C(1s) peaks reduce by 90% for the lightly-doped Si. The C(1s) signal observed for the heavily-doped silicon after PMMA removal is equivalent to that of adventitious carbon (not shown).

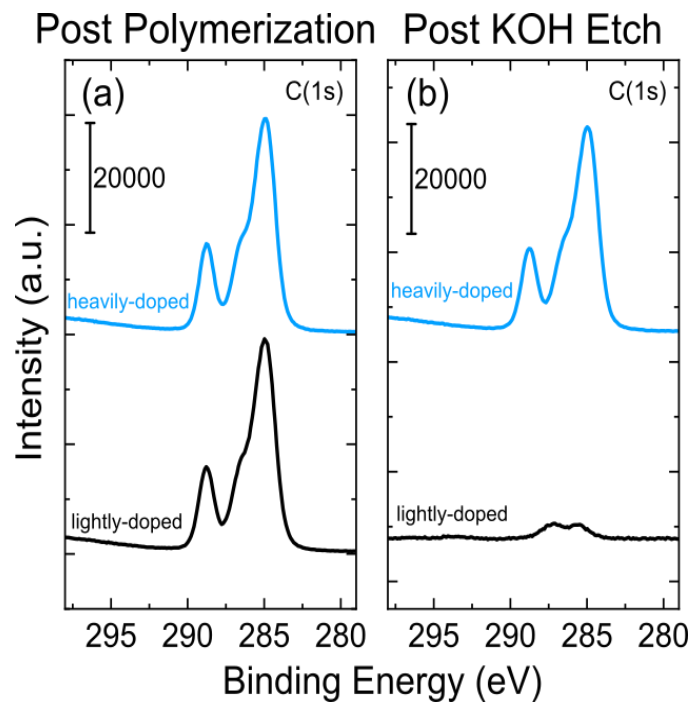


Figure 4.3. XPS characterization of surface-initiated polymerization before and after selective KOH etch. C(1s) spectra on the heavily-doped (blue) and lightly-doped (black) regions after PMMA polymerization (a) and after the KOH etch (b). Reprinted from Brummer A. C. Brummer, A. T. Mohabir, D. Aziz, M. A. Filler, and E. M. Vogel, *Appl. Phys. Lett.* 119, 142901 (2021) with the permission of AIP Publishing. Copyright 2021 AIP Publishing.

PMMA removal as a function of number of etch cycles is investigated and characterized with XPS integrated area ratios as well as spectroscopic ellipsometry. As seen in Figure 4.4a and b, the constant C(1s) and Si(2p) peak areas on the heavily-doped

Si verify the durable attachment of the PMMA brush. On the lightly-doped Si, the C(1s) peak area decreases, and the Si(2p) peak area correspondingly increases as the PMMA is removed. Spectroscopic ellipsometry is performed using a Woollam M200 Ellipsometer, and the CompleteEASE software is used for fitting with the PMMA, SiO<sub>2</sub>, and HfO<sub>2</sub> film models. Ellipsometry data in Figure 4.4c shows that the PMMA film thickness remains relatively constant on the heavily-doped Si while it decreases down to just a few nanometers on the lightly-doped Si. The achievable feature size relies on the underlying dopant profile and the polymer properties, as there likely will be some polymer overlapping the dopant junction. The degree of overlap and achievable feature size are expected to depend on the structure and length of the polymer and will be characterized with future work. Overall, the results indicate that the process can achieve selective masking based on the underlying doping concentration.

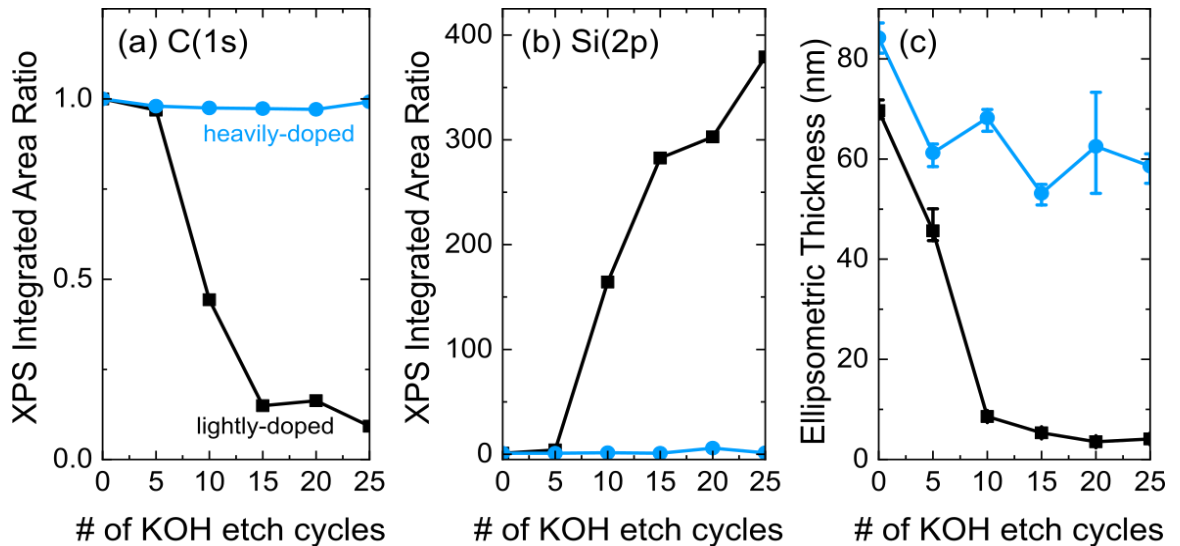


Figure 4.4. XPS and ellipsometric characterization of PMMA brush during KOH etch process: (a) Integrated area of the C(1s) XPS spectrum (normalized to initial peak area) vs number of etch cycles; (b) Integrated area of the Si(2p) XPS spectrum (normalized to initial peak area) vs number of etch cycles; (c) PMMA film thickness measured with ellipsometry vs number of etch cycles. Reprinted from Brummer A. C. Brummer, A. T. Mohabir, D. Aziz, M. A. Filler, and E. M. Vogel, *Appl. Phys. Lett.* 119, 142901 (2021) with the permission of AIP Publishing. Copyright 2021 AIP Publishing.

Next the selectively deposited Pt-HfO<sub>2</sub>-Si gate stack is characterized with XPS after each step. Though the deposition temperatures are above the glass transition temperature of PMMA (~115 °C),<sup>183</sup> the polymer brush offers robust passivation against ALD. The Hf(4f) XPS spectra taken after HfO<sub>2</sub> ALD in Figure 4.5a show a doublet with peaks at 16.7 eV and 18.3 eV in the lightly-doped region, confirming the selective deposition of HfO<sub>2</sub> on the exposed Si surface. As can also be seen, minimal HfO<sub>2</sub> deposits on the PMMA covering the heavily-doped regions. A comparison of integrated XPS peak areas for the lightly- and heavily-doped Si regions reveals a deposition selectivity of 30:1. Notably, an examination of TiO<sub>2</sub> and ZrO<sub>2</sub> AS-ALD shows these materials are also compatible with this process (see Figure 3.1 in Section 3.1.1). The Pt(4f) XPS spectra taken after Pt ALD in Figure 4.5b show a strong doublet with peaks at 71.2 eV and 74.5 eV verifying selective deposition of Pt on top of HfO<sub>2</sub> in the lightly-doped regions with very little deposition on the PMMA on the heavily-doped regions. Here, the deposition selectivity between the lightly- and heavily-doped Si regions is found to be 69:1, consistent with what is observed with SAMs<sup>28</sup> and spincoated PMMA.<sup>60</sup>

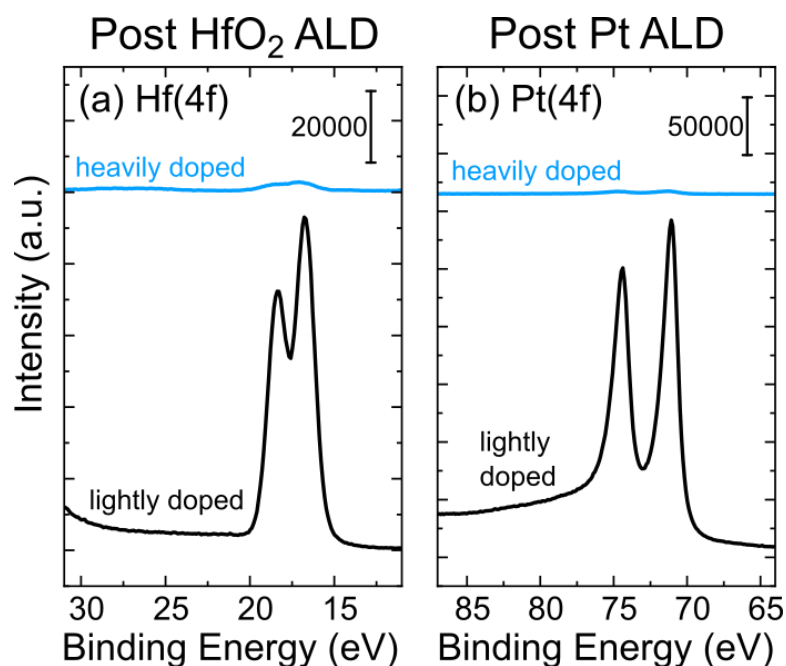


Figure 4.5. (a) Hf(4f) XPS spectra after HfO<sub>2</sub> ALD of PMMA-covered heavily-doped Si region and of lightly-doped Si region; (b) Pt(4f) XPS spectra after Pt ALD (immediately following HfO<sub>2</sub> ALD) of PMMA-covered heavily-doped Si region and of lightly-doped Si region. Reprinted from Brummer A. C. Brummer, A. T. Mohabir, D. Aziz, M. A. Filler, and E. M. Vogel, *Appl. Phys. Lett.* 119, 142901 (2021) with the permission of AIP Publishing. Copyright 2021 AIP Publishing.

Energy dispersive x-ray spectroscopy (EDS) is used to characterize the resulting self-aligned MOS structures to examine the spatial selectivity of deposition. Figure 4.6a shows an SEM image of four 100  $\mu\text{m}$  x 100  $\mu\text{m}$  MOS capacitors that are aligned with the lightly-doped Si (square) patterns. Figure 4.6b, c, and d show EDS maps for Si, Hf, and Pt, respectively, confirming the presence of HfO<sub>2</sub> and Pt mainly within the square patterns. The Hf M $\alpha$ 1 peak overlaps with the large Si K $\alpha$ 1 peak from the substrate, and the extra noise makes the pattern less clear, but a stronger intensity can be seen inside the square patterns where HfO<sub>2</sub> is present under the Pt layer.

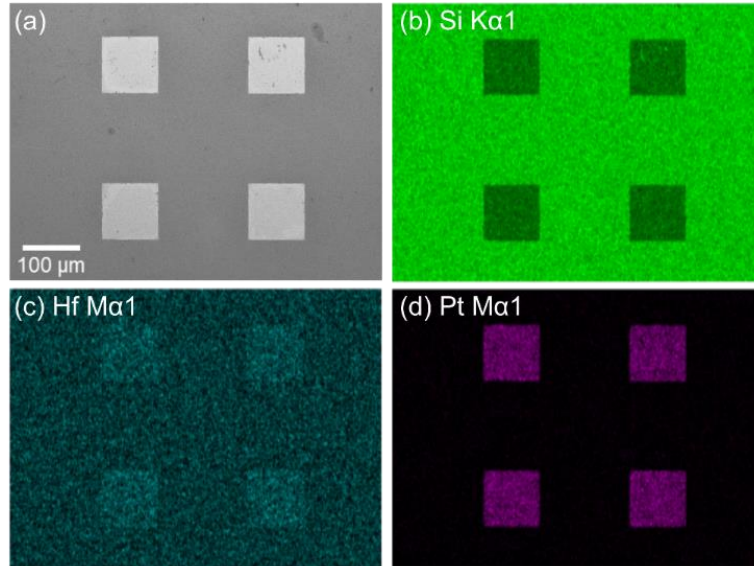


Figure 4.6. EDS characterization of self-aligned Pt-HfO<sub>2</sub>-Si MOS capacitors: (a) SEM image of four, square capacitors; (b) Si elemental mapping by EDS; (c) Hf elemental mapping by EDS; (d) Pt elemental mapping by EDS. Reprinted from Brummer A. C. Brummer, A. T. Mohabir, D. Aziz, M. A. Filler, and E. M. Vogel, *Appl. Phys. Lett.* 119, 142901 (2021) with the permission of AIP Publishing. Copyright 2021 AIP Publishing.

The MOS capacitors are characterized with capacitance-voltage (C-V) measurements to study the electrical properties of the selectively deposited gate stack and investigate the impact of a forming gas anneal, which has been shown in literature to reduce interface state density.<sup>184,185</sup> Capacitance and conductance are measured at 100 kHz with a voltage sweep range from 3 V to -3 V using a Keithley 4200-SCS semiconductor analyzer. Figure 4.7 shows the C-V behavior of three different MOS capacitors before and after a forming gas anneal at 400 °C for 30 min (96% N<sub>2</sub>/ 4% H<sub>2</sub>). With an oxide thickness of 6.1 nm of HfO<sub>2</sub> and a 2 nm-thick interlayer of SiO<sub>2</sub> (estimated from ellipsometry measurements), the maximum capacitance (from Figure 4.7) is used to estimate a relative dielectric constant of ~ 25.3, as expected for HfO<sub>2</sub>.<sup>186</sup> The C-V curves demonstrate typical MOS characteristics and show improved behavior after the forming gas anneal, indicated

by the curve's reduced stretch out. The average interface state density of MOS capacitors following AS-ALD is  $8.0 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$ , as approximated using the conductance peak and (Eq. 6 from Section 1.5.4:

$$D_{it} \approx \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{max} \quad (\text{Eq. 6})$$

The inset plot in Figure 4.7 shows that  $D_{it}$  can be reduced by a factor of 4 using a forming gas anneal. The  $D_{it}$  is relatively high for silicon-based MOS capacitors, however, and future work will be performed to improve the interface quality with alternate surface cleaning techniques and improved interfacial layers.

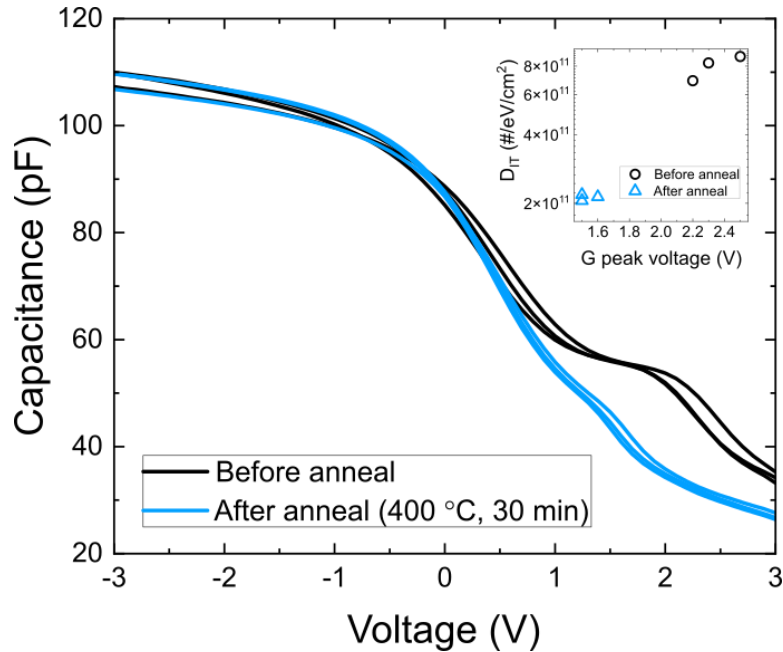


Figure 4.7. Capacitance vs voltage behavior of three selectively deposited Pt-HfO<sub>2</sub>-Si MOS capacitors before and after forming gas anneal. Reprinted from Brummer A. C. Brummer, A. T. Mohabir, D. Aziz, M. A. Filler, and E. M. Vogel, Appl. Phys. Lett. 119, 142901 (2021) with the permission of AIP Publishing. Copyright 2021 AIP Publishing.

#### 4.4 Conclusions

In summary, a self-aligned gate stack structure is demonstrated with a process that combines SCALES and AS-ALD. The PMMA brush grafted from the Si(100) surface is

selectively removed based on the underlying semiconductor carrier concentration and serves as a mask for ALD.  $\text{HfO}_2$  and Pt are then selectively deposited via AS-ALD, forming MOS capacitors suitable for a gate stack. Current-voltage measurements show expected MOS capacitor behavior and improvement upon forming gas anneal. This process can be used to fabricate complex nano- and micro-structure devices without photolithography, which holds promise for BEOL processes and flexible electronics applications. And this self-aligned MOS gate stack deposition process can be applied to Si nanowires in future work to fabricate modular transistor devices.

## **CHAPTER 5. INVESTIGATING WET CHEMICAL OXIDATION METHODS TO FORM SiO<sub>2</sub> INTERLAYERS FOR SELF-ALIGNED GATE STACKS**

In this chapter, self-aligned MOS capacitors are studied with several low temperature, wet chemical silicon dioxide (SiO<sub>2</sub>) interlayers to understand their impact on electrical performance. Self-aligned MOS capacitors are fabricated with a bottom-up patterning technique that uses a poly(methyl methacrylate) brush and dopant-selective KOH etch combined with area-selective atomic layer deposition of HfO<sub>2</sub> and Pt. The wet chemical pre-treatments used to form the SiO<sub>2</sub> interlayer include HF-last, 80 °C H<sub>2</sub>O, and SC-2. Capacitance-voltage measurements of these area-selective capacitors exhibit a HfO<sub>2</sub> dielectric constant of ~19, irrespective of pre-treatment. After a forming gas anneal, the average interface state density decreased between 1.8 and 7.5 times. The minimum observed  $D_{it}$  is  $1 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$  for the HF-last treatment. X-ray photoelectron spectroscopy shows an increase in stoichiometric SiO<sub>2</sub> in the interfacial layer after the anneal. Additional carbon is also observed; however, comparison with capacitors fabricated in a non-selective process reveals minimal impact on performance.

### **5.1 Introduction**

Alignment between the edge of a gate stack and the edge of the underlying doped source-drain regions of the Si channel is a critical issue for the fabrication of high-performance transistors. Excess overlap results in large fringe capacitance and reduced device speed while too much underlap can result in extra series resistance.<sup>172,173</sup> Achieving proper alignment within an integrated high- $\kappa$ /metal gate stack can require complex integration schemes such as the replacement metal gate technique.<sup>174</sup> Processing and

integration becomes even more challenging for gate-all-around transistors with either vertical<sup>176</sup> or lateral<sup>175</sup> silicon nanowires, where numerous process steps are required to align the gate stack over the channel (e.g., selectively etching a gap across the channel and depositing a dummy gate for source/drain doping, then replacing the dummy gate with a high- $\kappa$  gate stack). The ability to form self-aligned device structures, such as MOS capacitors, would simplify fabrication of gate-all-around transistors and benefit a variety of emerging device applications, including vertical nanowire transistors monolithically integrated into the back end of line (BEOL)<sup>177</sup> and flexible electronics that require lower process temperatures and patterning techniques that are more scalable than conventional photolithography.<sup>178</sup>

Atomic layer deposition (ALD) allows for low-temperature and area-selective deposition of thin films closely aligned with patterns on the underlying substrate, largely irrespective of geometry. The most common techniques for AS-ALD involve using self-assembled monolayers (SAMs)<sup>26,63-67,69,179</sup> or other polymeric materials<sup>59,60,70,71,74,180</sup> to deactivate the surface by preventing the chemisorption of the ALD precursors. These techniques typically require photolithography to apply the masking material, either to pattern the surface modification layer<sup>26,60,70,71</sup> or to pattern the deposition of different materials that have intrinsic chemical differences.<sup>63,66,74,181</sup>

Our previous work demonstrated a fabrication process that combines a bottom-up patterning technique with AS-ALD to deposit HfO<sub>2</sub> and Pt thin films based on the local carrier concentration of the underlying Si substrate, ultimately forming self-aligned MOS capacitors.<sup>81</sup> The bottom-up patterning technique is a derivative of selective co-axial lithography via etching of surfaces (SCALES).<sup>4,137</sup> Patterning with SCALES begins with a

poly(methyl methacrylate) (PMMA) brush grown from a Si surface via atom-transfer radical polymerization. We selectively remove the polymer film from the lightly doped Si regions by etching with an aqueous potassium hydroxide (KOH) solution. The PMMA film remains attached to the heavily doped Si regions which then serves as a mask for AS-ALD of HfO<sub>2</sub> and Pt. The resulting self-aligned MOS capacitors yielded expected capacitance-voltage behavior.

A thin SiO<sub>2</sub> layer is often required to form a low defect density interlayer between Si and high- $\kappa$  dielectrics,<sup>93,187</sup> as well as to improve ALD nucleation of HfO<sub>2</sub>.<sup>103</sup> To form this interlayer, a high-temperature thermal oxidation technique is typically used. However, high temperature thermal oxidation is not possible with the current SCALES process because the polymer cannot withstand high process temperatures. Other chemical oxidation methods have also been studied to improve ALD film nucleation and reduce interface state density, including treatments such as hydrogen peroxide, standard cleans 1 and 2 (SC-1 and SC-2 from RCA clean), nitric acid and heated water (H<sub>2</sub>O).<sup>103,188</sup>

In this work, self-aligned (area-selective deposition) Pt-HfO<sub>2</sub>-Si MOS capacitors are compared with conventional (non-selective deposition) capacitors to investigate the impact of a variety wet chemical processes (i.e., HF etch, 80 °C H<sub>2</sub>O, and SC-2) for forming the SiO<sub>2</sub> interlayer. Physical characterization methods (i.e., ellipsometric spectroscopy and x-ray photoelectron spectroscopy) are used to understand the relationship between the various SiO<sub>2</sub> interlayer formation techniques and the electrical performance of the capacitors. Capacitance-voltage characteristics exhibit similar performance between area-selective and non-selective capacitors, and average interface state density is reduced to  $1.9 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$  after a forming gas anneal (FGA). X-ray photoelectron spectroscopy

indicates in an increase in the amount of stoichiometric SiO<sub>2</sub> in the interfacial layer after the FGA. Additional carbon is also observed in the area-selective interfacial layer after the FGA which does not significantly impact performance.

## 5.2 Experimental Methods

### 5.2.1 Non-selective Capacitor Fabrication

For conventional “non-selective” capacitors, Si(100) with a p-type doping level of  $\sim 10^{18}$  cm<sup>-3</sup> was used. A modified RCA clean was first performed: 1 min in dilute SC-1 (5 DI H<sub>2</sub>O:1 H<sub>2</sub>O<sub>2</sub>:0.25 NH<sub>4</sub>OH) at 75 °C, 30 s HF etch, and 10 min in SC-2 (5 DI H<sub>2</sub>O:1 H<sub>2</sub>O<sub>2</sub>:1 HCl) at 75 °C. This was followed by an HF etch (30 s in 1% HF) to remove the native oxide prior to formation of the SiO<sub>2</sub> interlayer. Three different wet chemical oxidation techniques were investigated as pre-treatments to form the thin SiO<sub>2</sub> interlayer: HF-last treatment (30 s in 1% HF followed by DI H<sub>2</sub>O rinse), hot water (30 s in 1% HF then 10 min in ultra-pure DI H<sub>2</sub>O at 80 °C), and SC-2 treatment (30 s in 1% HF then 10 min in 5 DI H<sub>2</sub>O:1 H<sub>2</sub>O<sub>2</sub>:1 HCl at 75 °C). These chemical oxides are compared with a high temperature rapid thermal processing (RTP) oxidation (30 s in 1% HF, 3 min in RTP furnace flowing 5 SCCM O<sub>2</sub> at 900 °C, 1% HF etch to reduce thickness).

Immediately following oxidation, the samples were transferred to the ALD chamber (Cambridge Fiji ALD system with argon as a carrier/purging gas and a total chamber pressure of 0.45 Torr) to deposit  $\sim 6$  nm of thermal HfO<sub>2</sub> at 200 °C using 55 cycles of tetrakis(dimethylamido)hafnium (TDMAHf) and H<sub>2</sub>O. The exposure times for TDMAHf and H<sub>2</sub>O were 0.25 and 0.06 s, respectively, followed by purge times of 20 and 15 s. Electron-beam evaporation was used to deposit 75 nm of Pt through a shadow mask,

forming 85  $\mu\text{m}$  x 85  $\mu\text{m}$  square MOS capacitors. The final process step was a forming gas anneal (FGA, 5 SCCM, 96%  $\text{N}_2$  / 4%  $\text{H}_2$ ) for 30 min at 400  $^\circ\text{C}$ , and results are shown for annealed and unannealed capacitors.

### 5.2.2 Area-Selective Capacitor Fabrication

To fabricate the self-aligned “area-selective” capacitors, p-type Si(100) was patterned with a thick  $\text{SiO}_2$  mask and then doped with boron via solid state diffusion (2 h at 1050  $^\circ\text{C}$ ,  $\text{B}_2\text{O}_3$  source) to fabricate heavily boron-doped ( $\sim 10^{20} \text{ cm}^{-3}$ ) substrates with lightly boron-doped ( $\sim 10^{18} \text{ cm}^{-3}$ ) 100  $\mu\text{m}$  x 100  $\mu\text{m}$  square regions. This doping profile enables the use of SCALES and AS-ALD to form the self-aligned structures. With the SCALES process, a poly(methyl methacrylate) (PMMA) brush anchored to the Si surface was synthesized<sup>137</sup> across the entire substrate and selectively removed from the lightly-doped regions via cycles of exposure to potassium hydroxide (KOH) solution (1 mL 45 wt% KOH:3 mL IPA:8.5 mL DI  $\text{H}_2\text{O}$ ) to etch the Si and acetone to solvate the PMMA. The substrate was then cleaned with the same modified RCA clean described previously, followed by 1% HF etch and thin  $\text{SiO}_2$  oxidation using the same oxidation treatments described in the non-selective capacitor methods. However, the thermal oxidation requires very high temperature which degrades the PMMA film used for patterning, so only the chemical oxide pre-treatments were used to fabricate the area-selective capacitors. After oxidation, samples were transferred to the ALD chamber for selective deposition of  $\text{HfO}_2$  and Pt on the exposed lightly doped Si.  $\text{HfO}_2$  was deposited with 55 cycles of thermal  $\text{HfO}_2$  ALD at 200  $^\circ\text{C}$  using the same recipe as the non-selective capacitors. Following the  $\text{HfO}_2$  deposition, Pt was deposited with 300 cycles of thermal Pt ALD at 300  $^\circ\text{C}$  using

(trimethyl)methylcyclopentadienylplatinum(IV) (MeCpPtMe<sub>3</sub>) and O<sub>2</sub>. The exposure times for MeCpPtMe<sub>3</sub> and O<sub>2</sub> were 1 and 10 s, respectively, followed by purge times of 10 s. This fabrication process is described in detail in previous work.<sup>81,137</sup> The final process step was a FGA (5 SCCM, 96% N<sub>2</sub> / 4% H<sub>2</sub>) for 30 min at 400 °C, and results are shown for annealed and unannealed capacitors.

### 5.2.3 Electrical Characterization

Capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were conducted with a Keithley 4200-SCS semiconductor analyzer and Cascade Microtech probe station. Capacitance and conductance were measured at 100 kHz with a voltage sweep from 2 V to -2 V. The conductance method was used to extract interface state density (D<sub>it</sub>) using (Eq. 6 from Section 1.5.4:

$$D_{it} \approx \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{max} \quad (\text{Eq. 6})$$

where q is electronic charge,  $\omega$  is angular frequency, and G<sub>p</sub> is the conductance peak after extracting and correcting for series resistance using the relationships defined by Vogel et. al.<sup>87</sup> The measured capacitance (C<sub>m</sub>) and conductance (G<sub>m</sub>) were corrected using Equations (Eq. 7 and (Eq. 8 from Section 1.5.4:

$$C_c = \frac{C_m}{(1 - G_m R_s)^2 + \omega^2 C_m^2 R_s^2} \quad (\text{Eq. 7})$$

$$G_c = \frac{\omega^2 C_m C_c R_s - G_m}{G_m R_s - 1} \quad (\text{Eq. 8})$$

where  $C_c$  is corrected capacitance,  $G_c$  is corrected conductance and  $R_s$  is series resistance. Series resistance was extracted by numerically iterating the  $R_s$  value in the corrected conductance equation until  $G_c$  is minimized throughout accumulation (or approximately equal to tunneling conductance).

#### 5.2.4 *Physical Characterization*

Spectroscopic ellipsometry was used to measure film thickness. Spectroscopic ellipsometry was performed with a Woollam M200 ellipsometer, and CompleteEase software (J.A. Woollam) was used for all spectra fitting for the  $\text{SiO}_2$  and  $\text{HfO}_2$  films. X-ray photoelectron spectroscopy (XPS) was used to physically characterize the composition of the  $\text{SiO}_2/\text{HfO}_2$  thin films. XPS measurements were performed with a Thermo Scientific K-Alpha X-ray photoelectron spectrometer system with a monochromatic Al  $K\alpha$  source using a spot size of 400  $\mu\text{m}$  and pass energy of 50 eV. The Si(2p) peak at 99.4 eV corresponding to elemental Si bonds from the substrate was used as a reference peak, and the spectra were shifted to correct the effects of experimental charging. XPS spectra from the capacitors did not detect the  $\text{SiO}_2$  interlayer underneath the  $\text{HfO}_2$  layer and Pt electrode due to the limited penetration depth of XPS (~5-10 nm).<sup>189</sup> To overcome this, separate samples with a thinner  $\text{HfO}_2$  film and without the Pt film were fabricated for XPS measurements. The substrates were prepared in the same way as the capacitor samples with only 30 cycles of  $\text{HfO}_2$  ALD and no Pt deposition, and XPS spectra were obtained immediately after processing.

### 5.3 Results and Discussion

Figure 5.1 shows representative curves of C-V behavior for non-selective and area-selective capacitors before and after the FGA. The C-V curves exhibit expected behavior for MOS capacitors. A difference in maximum capacitance measured for each pre-treatment is noted in addition to presence of interface states. Small variations in SiO<sub>2</sub> thickness for different oxidation methods are likely responsible for the differences in the measured maximum capacitances. Ellipsometry measurements during fabrication indicate that the HfO<sub>2</sub> film thickness for all of the non-selective capacitors was 6.2 nm with the following SiO<sub>2</sub> interlayer thicknesses from each pre-treatment: 0.7 nm from HF, 1.1 nm from 80 °C H<sub>2</sub>O, 1 nm from SC-2, and 1.4 nm from thermal oxidation. Similarly for all of the area-selective capacitors, the HfO<sub>2</sub> film was 6.1 nm thick with slightly thicker SiO<sub>2</sub> interlayer thicknesses: 1.0 nm from HF, 1.5 nm from 80 °C H<sub>2</sub>O, and 1.5 nm from SC-2. The differences in thickness between the selective and non-selective cases may be due to a difference in surface roughness from the KOH etching, which can result in overestimation of film thickness for ellipsometry.<sup>190</sup>

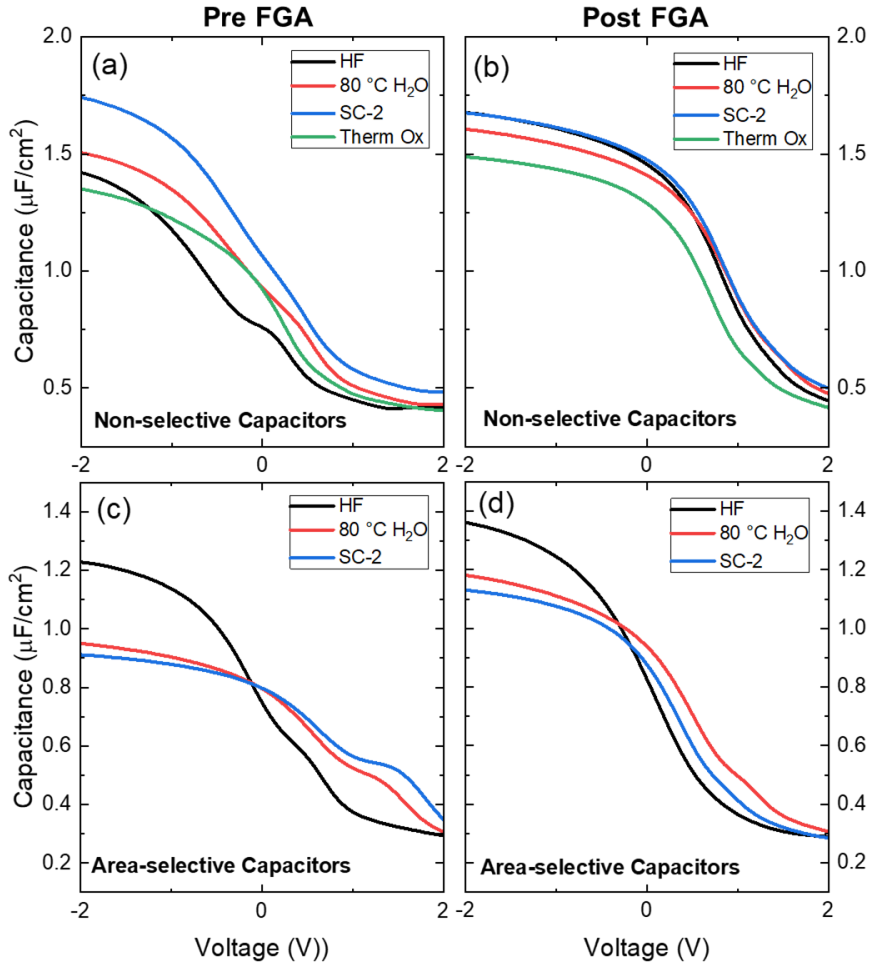


Figure 5.1. Capacitance-voltage characteristics of non-selective (a and b) and area-selective (c and d) Pt-HfO<sub>2</sub>-Si MOS capacitors before (a and c) and after (b and d) a FGA. Each graph shows a representative C-V curve of one capacitor with each SiO<sub>2</sub> interlayer treatment: HF, 80 °C H<sub>2</sub>O, SC-2, and thermal oxide (non-selective only).

Both sample sets show improved performance after the FGA as indicated by the reduced stretch out of the curves. The slight differences in maximum capacitance after the FGA can likely be attributed to a combination of factors including formation of Hf silicate at the interface,<sup>191</sup> increased dielectric constant due to polycrystallization,<sup>186</sup> and diffusion of carbon residue to the surface (*vide infra*). Combining the measured SiO<sub>2</sub> and HfO<sub>2</sub> thicknesses with maximum capacitances between 1.3 and 1.7 μF/cm<sup>2</sup> yields an

estimate of a relative dielectric constant of  $\sim 20$  for the non-selective  $\text{HfO}_2$  films, which is expected for ALD  $\text{HfO}_2$ .<sup>192</sup> Similarly for the area-selective  $\text{HfO}_2$  films with maximum capacitances measured between  $0.9$  and  $1.2 \mu\text{F}/\text{cm}^2$ , a relative dielectric constant of  $\sim 19$  is estimated, which is very similar to that of the non-selective capacitors.

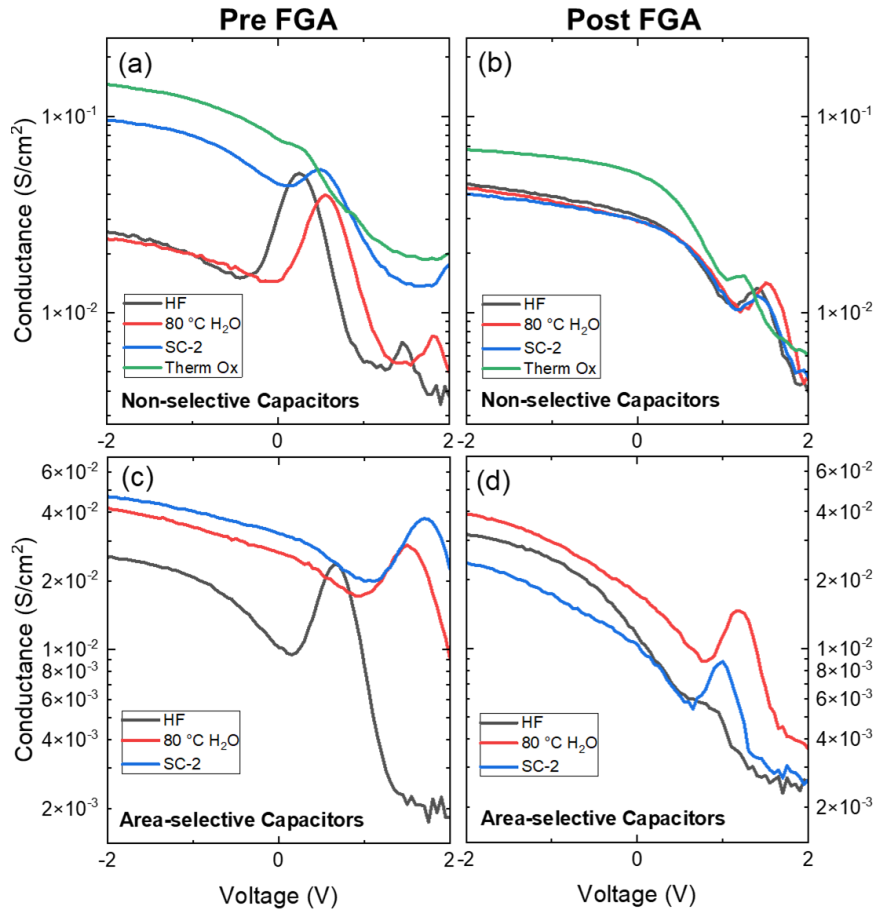


Figure 5.2. Conductance-voltage behavior of non-selective (a and b) and area-selective (c and d) Pt- $\text{HfO}_2$ -Si MOS capacitors before (a and c) and after (b and d) a FGA. Each graph shows a representative G-V curve of one capacitor with each  $\text{SiO}_2$  interlayer treatment: HF,  $80^\circ\text{C H}_2\text{O}$ , SC-2, and thermal oxide (non-selective only).

The humps observed in the pre-FGA capacitance curves indicate significant interface state density ( $D_{it}$ ), so conductance measurements are used to better investigate  $D_{it}$ . Figure 5.2 shows the voltage dependence of measured conductance ( $G_m$ ) for a device

with each oxidation technique for both the non-selective and area-selective capacitors. The peaks seen in the  $G_m$  curves are attributed to interface states.  $D_{it}$  is extracted for 5 capacitors for each interlayer type before and after FGA as shown in Figure 5.3. The interface state density is observed to decrease significantly with the FGA. The average  $D_{it}$  decreases from  $8.5 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$  to  $1.9 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$  for the non-selective capacitors and from  $5.7 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$  to  $1.9 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$  for the area-selective capacitors. These post FGA values are similar to what is typically observed for  $\text{HfO}_2/\text{Si}$  gate stacks ( $\sim 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$ ).<sup>193,194</sup> The  $D_{it}$  for the wet chemical  $\text{SiO}_2$  interlayers is similar to that of the thermal oxide, and there is no significant difference between the non-selective and area-selective samples. The results show that the area-selective process does not have a negative impact on electrical performance relative to the non-selective process, and using any of the wet chemical interlayer techniques results in formation of an interface that functions similarly to the thermal oxide interlayer. However, the standard deviations of the  $D_{it}$  are larger for the area-selective processes as compared to the non-selective process (*vide infra*).

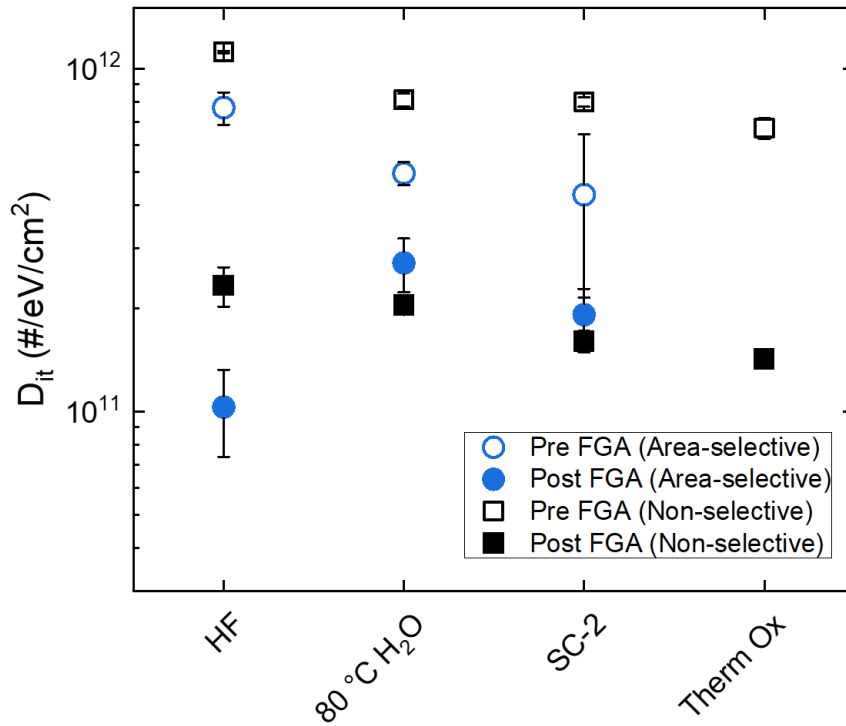


Figure 5.3. Estimated  $D_{it}$  values for non-selective (black) and area-selective (blue) Pt-HfO<sub>2</sub>-Si MOS capacitors before and after the FGA.

XPS is used to physically characterize the oxide-semiconductor interface of the capacitor structure to understand the impact of the processing on the composition of the interlayer. Figure 5.4 shows XPS spectra of the Si(2p) region obtained from HfO<sub>2</sub>/SiO<sub>2</sub>/Si substrates that were treated with the same initial processing steps as the capacitors (i.e., modified RCA clean, interlayer oxidation, HfO<sub>2</sub> ALD, and FGA for the non-selective set; PMMA, KOH etch, modified RCA clean, interlayer oxidation, HfO<sub>2</sub> ALD, and FGA for the area-selective set). All substrates show the expected elemental Si doublet peak near 99.4 eV (seen in Figure 5.4c for substrates after FGA) due to the bulk Si substrate. The oxidized Si(2p) peak for stoichiometric SiO<sub>2</sub> would be expected near 103.5 eV (referenced to elemental Si at 99.4 eV).<sup>195</sup> Peaks representing lower oxidation states of Si (Si<sup>1+</sup>, Si<sup>2+</sup>,

Si<sup>3+</sup>) and Hf silicate compounds have binding energies between 99.4 eV and 103.5 eV.<sup>196-198</sup> With the exception of the pre-anneal HF-treated substrates, all samples have a small peak near 103.5 eV (seen in Figure 5.4). These peaks are broader and slightly closer to the elemental Si peak than a stoichiometric SiO<sub>2</sub> peak would be, indicating they are likely a convoluted peak consisting of multiple overlapping peaks attributed to SiO<sub>2</sub>, Si suboxides in multiple oxidation states (SiO<sub>x</sub>), and Hf silicate compounds.

With the HF pre-treatment, no clear Si(2p) suboxide photoelectron peak is observed before the FGA (but a subtle left-side shoulder of the elemental Si(2p) peak allowed for fitting of a very small suboxide peak for comparison). This suggests very minimal formation of an interlayer during ALD. After the FGA, the appearance of an Si(2p) suboxide peak at 103.0 eV and 102.8 eV for the non-selective deposition substrate and the area-selective deposition substrate, respectively, indicates formation of an interfacial layer between the Si and HfO<sub>2</sub> film, which is typically seen with annealing of HfO<sub>2</sub> films.<sup>199,200</sup> Excess oxygen in the HfO<sub>2</sub> film in the form of hydroxyl groups can react with Si at the interface to form an interlayer upon thermal treatment.<sup>199</sup> Oxygen impurity in the forming gas is also a possibility, which could allow for diffusion of oxygen through the HfO<sub>2</sub> layer to facilitate SiO<sub>2</sub> growth at the interface.<sup>201</sup>

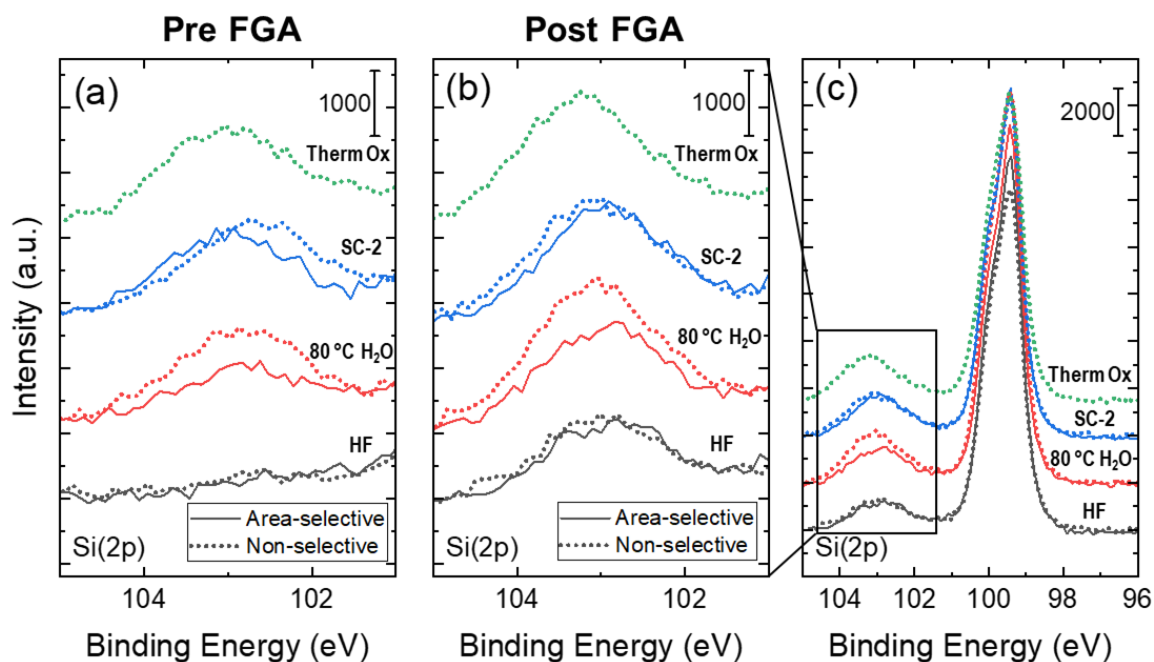


Figure 5.4. Si(2p) XPS spectra of non-selective (dotted line) and area-selective (solid line) HfO<sub>2</sub> films on Si with different SiO<sub>2</sub> interfacial layers before (a) and after (b) the FGA; (a) and (b) show a narrower region to see the oxidized Si(2p) peaks in more detail; (c) shows the full Si(2p) spectrum of all substrates after the FGA.

After the FGA, an increase in the peak area of the Si(2p) suboxide photoelectron peak is observed for all interlayer types and most of the peaks blueshift. Figure 5.5a shows the peak positions of the Si(2p) suboxide peak for each interlayer type before and after annealing. Figure 5.5b shows the ratio of integrated intensity of the suboxide Si(2p) peak normalized to the integrated intensity of the elemental Si(2p) peak before and after the FGA for each interlayer type. In general, we see the Si(2p) suboxide peak shift to a binding energy 0.2-0.3 eV higher after the FGA. The integrated intensity ratio of the Si suboxide peak shows a 30-80% increase for the 80 °C H<sub>2</sub>O treated substrates, 10-20% increase for the SC-2 treated substrates, and 40% increase for the thermal oxide treated substrate. This increased intensity and shift towards the binding energy of stoichiometric SiO<sub>2</sub> (i.e., 103.5

eV) for most cases suggests formation of higher quality SiO<sub>2</sub> at the interface after the FGA. This correlates with the improved electrical performance we observe. Suboxide states of Si induce strain and dangling bonds at the interface, which can trap charges and lead to electronic interface defects.<sup>202</sup> The FGA leading to more stoichiometric SiO<sub>2</sub> at the interface is therefore consistent with a reduced interface state density.

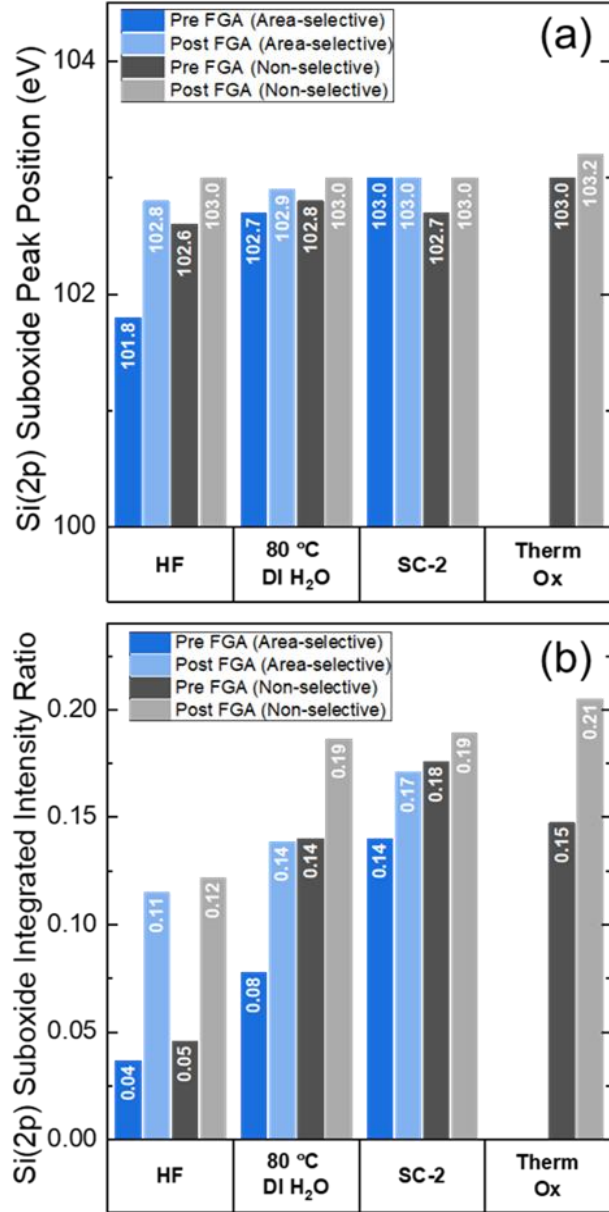


Figure 5.5. XPS peak positions of the suboxide Si(2p) peak (a) and ratio of XPS integrated intensity of the suboxide Si(2p) peak to integrated intensity of elemental Si(2p) peak (b) before and after the FGA for area-selective deposition and non-selective deposition HfO<sub>2</sub>/SiO<sub>2</sub>/Si substrates treated with different SiO<sub>2</sub> interlayer formation techniques.

The Si(2p) suboxide peak from the SC-2 treated area-selective deposition substrate is the only one that does not shift position after the FGA. For the SC-2 pre-treatment, the Si(2p) spectra from the non-selective deposition substrate indicate a Si suboxide peak shift

from 102.7 eV to 103.0 eV after annealing, but the position of the Si suboxide peak from the area-selective deposition substrate remains unchanged at 103.0 eV. The integrated area of the peak did increase, however, suggesting an increase in the amount of interfacial  $\text{SiO}_x$  consistent with what we observe with the other substrates.

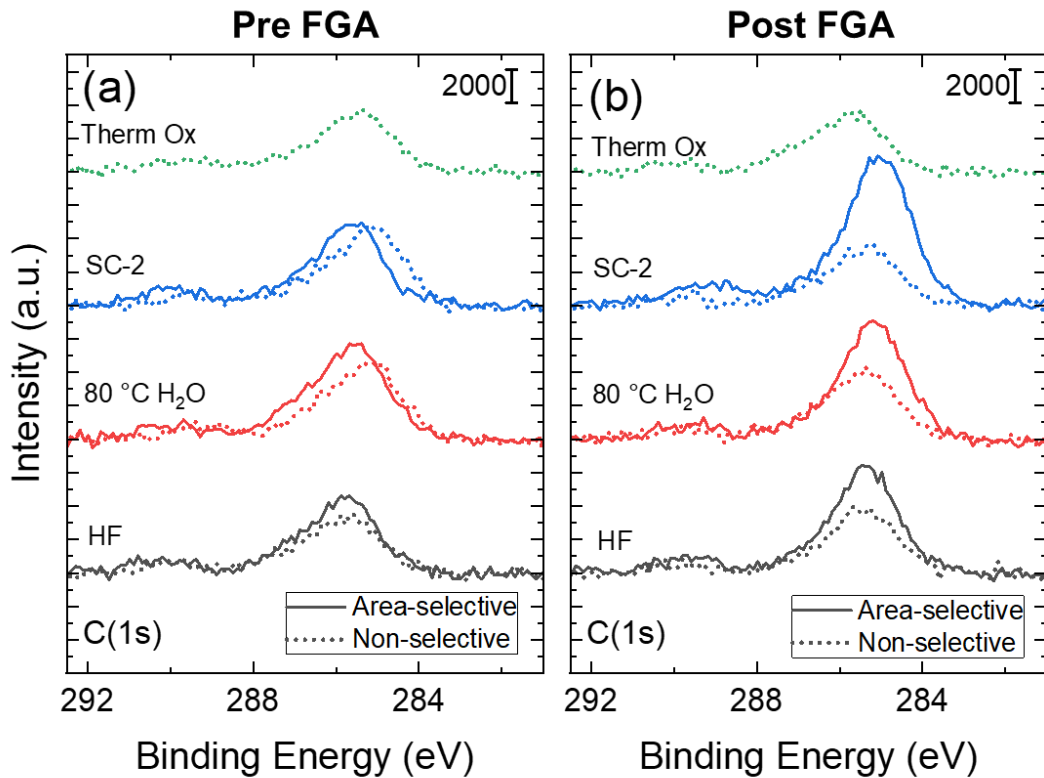


Figure 5.6. C(1s) XPS spectra of non-selective (dotted line) and area-selective (solid line)  $\text{HfO}_2$  films on Si with different  $\text{SiO}_2$  interfacial layers before (a) and after (b) the FGA.

XPS spectra in the C(1s) region for all substrates are shown in Figure 5.6. The  $\text{HfO}_2$  ALD precursor (TDMAHf) contains methyl carbon groups, so a small amount of carbon is expected in the  $\text{HfO}_2$  film in addition to adventitious carbon. Figure 5.6a shows very similar spectra for all substrates before the FGA, with the small expected C(1s)

photoelectron peaks at 285 eV and 289 eV.<sup>203</sup> After annealing however, there is a notable difference between the non-selective and area-selective capacitors. While the C(1s) spectra from the non-selective capacitors show no change in carbon content after annealing, the C(1s) spectra from the area-selective capacitors all show larger carbon peaks. This is likely due to carbon residue leftover from the patterned PMMA diffusing up through the HfO<sub>2</sub> film. The average  $D_{it}$  of the area-selective and non-selective capacitors is similar, so this extra carbon present on the surface and in the film does not lead to more electrically active defects at the interface. However, the area-selective capacitors do exhibit more variation in performance, indicated by larger standard deviations for  $D_{it}$ . The extra processing steps for the area-selective deposition substrates (i.e., polymer synthesis and KOH etch) likely roughen the surface and leave carbon residue distributed unevenly across on the Si surface. This can result in more extrinsic defects and impurities in some regions of the substrate, leading to more variability in electrical performance. A more thorough cleaning procedure after patterning the PMMA film should be investigated with future work to minimize the excess carbon observed in the film to ensure more reliable performance between devices.

#### **5.4 Summary and Conclusions**

In summary, Pt-HfO<sub>2</sub>-Si MOS capacitors are studied to compare self-aligned area-selective structures with conventional non-selective devices. Various chemical oxidation techniques, including HF-last, 80 °C H<sub>2</sub>O, and SC-2 treatment, are used to form an SiO<sub>2</sub> interfacial layer to compare with a high temperature thermal oxidation. The area-selective capacitors perform as well as the non-selective capacitors, and all oxidation treatments exhibit similar electrical performance, with interface state densities near  $2 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$  after a FGA. XPS data for the HfO<sub>2</sub>-Si interface indicates an increase in SiO<sub>2</sub> in the

interfacial layer after the FGA, which is consistent with the improved interface state density. XPS data also shows presence of extra carbon after annealing the area-selective samples, but this does not significantly impact performance.

## CHAPTER 6. CONCLUSIONS AND FUTURE PERSPECTIVES

### 6.1 Conclusions

The ability to fabricate customizable circuits on demand could provide a pathway to new electronics applications and would lower the cost barrier for electronics innovation. This vision to create customized on demand circuits requires high performance, pre-formed, nano-modular transistors. This work further developed a process to pursue that goal of fabricating nanowire transistors with the successful deposition of a self-aligned gate stack. By leveraging the chemical differences of materials to selectively etch and deposit high- $\kappa$  dielectrics and metal films, surfaces were patterned without conventional photolithography to manipulate device structures.

This work adapted and improved an existing polymer brush patterning technique to be used on planar Si substrates. Dopant-patterned substrates were designed and fabricated to enable the planar fabrication process. And the polymer synthesis procedure was studied systematically to gain understanding about process variability. With insight from physical characterization of each step of the polymerization, the polymer synthesis was improved with equipment upgrades and alternate rinsing procedures to achieve more reliable polymer film thicknesses.

Area-selective atomic layer deposition was investigated to deposit a self-aligned gate stack. Selectivity of deposition of a variety of materials (high- $\kappa$  dielectric oxides and metals) was analyzed to select a materials system for the gate stack. Due to the suitable material properties and compatibility with the polymer patterning process, HfO<sub>2</sub> and Pt were ultimately selected to fabricate a self-aligned gate stack on planar Si substrates. The

performance of the self-aligned gate stack structure was investigated with physical characterization to verify the composition of the self-aligned pattern.

Self-aligned MOS capacitor devices were characterized electrically to examine how the materials processing impacts device performance. The selectively deposited capacitors performed similarly to conventionally fabricated capacitors with expected capacitance-voltage behavior and improvement after a forming gas anneal. Different wet chemical oxidation treatments (i.e., HF-last, 80 °C H<sub>2</sub>O, and SC-2) were studied to form an SiO<sub>2</sub> interlayer between the Si surface and HfO<sub>2</sub> film. The interlayer treatments were used to fabricate self-aligned capacitors and conventional capacitors. And the selectively deposited devices again performed as well as conventional devices with slightly more variability. All capacitors exhibited similar performance with interface state densities near  $2 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$  after the forming gas anneal. And physical characterization of the HfO<sub>2</sub>-Si interface indicated an increase in amount of SiO<sub>2</sub> in the interlayer after annealing, which is consistent with the improved interface state density.

The self-aligned gate stack developed with this work lends itself to a variety of applications, including incorporation in BEOL applications or formation of complex bottom-up nanowire device structures. This technique can be extended to other material systems with future work. And because the process employs scalable (mostly solution-based and vapor-phase) techniques, it can easily be adapted for large scale manufacturing. The development of this self-aligned gate stack provides a pathway towards fabrication of bottom-up nanowire transistors that could ultimately enable the low-cost production of customizable, on demand circuits.

## 6.2 Future Perspectives

This work has developed a process to selectively deposit a gate stack aligned to the underlying substrate dopant concentration which provides a pathway towards fabricating nano-modular transistors with nanowires. However, there are still a number of challenges to be overcome to achieve the objective of fabricating circuits. This section discusses those challenges to be addressed with future work.

### 6.2.1 Future Work with Self-Aligned Capacitors

As shown in previous sections, we have successfully deposited self-aligned MOS capacitor devices with this work that function as well as conventionally fabricated capacitors. The selective deposition process does however lead to more variability in performance with larger standard deviations for average interface state density. This likely results from the SCALES process. There is typically leftover carbon residue after the polymerization, KOH etch, and modified RCA clean dispersed randomly across the surface. XPS spectra show that this carbon appears to diffuse through the ALD films during the anneal.

More thorough cleaning processes should be investigated to address the presence of excess carbon. SC-1 treatment contains H<sub>2</sub>O<sub>2</sub>, DI H<sub>2</sub>O and ammonium hydroxide heated to 75 °C to remove organic contamination. We use a diluted SC-1 treatment for only 1 min instead of 10 min to perform a less aggressive treatment that doesn't strip the PMMA mask. However, since there does appear to be carbon residue left after the gentle SC-1 treatment, a more thorough clean should be investigated. Potential alternatives include using dilute nitric or sulfuric acid, using sonication while in solution, or a combination of longer

treatment time with lower temperature.<sup>138</sup> It is also known that KOH etching can roughen silicon surfaces,<sup>204</sup> which could have an impact on the interface state density. This could be studied with atomic force microscopy to investigate surface roughness before and after KOH etching and again after the modified RCA clean.

This work specifically uses HfO<sub>2</sub> and Pt with boron-doped Si substrates, but this process could be adapted for other material systems. Selective deposition of alternative oxides (e.g. Al<sub>2</sub>O<sub>3</sub> and ZrO<sub>2</sub>) and metals (e.g. Co and TiN) could be investigated to fabricate MOS capacitors with a similar process to compare performance. Using different precursors and/or different polymer brush masks could enable different selective deposition outcomes. And selective deposition of TiN in particular could be investigated with a thermal ALD using ammonia gas instead of N<sub>2</sub> plasma. Additionally, to make the overall process more universal for incorporation in BEOL CMOS technology, the use of n-type substrates should be explored. This work focused on using boron-doped Si substrates because initial tests with phosphorus-doped substrates were inconclusive. Successful SCALES patterning of phosphorus-doped substrates may be achieved with a more detailed investigation of KOH etching on n-type Si.

### *6.2.2 Transition from Planar Substrates to Nanowires*

Since this planar self-aligned gate stack process opens a pathway to fabricating nanowire devices, transitioning from planar substrates to nanowires is a natural next step. There are a variety of roadblocks to address, however. We see that SCALES patterning behaves differently on nanowires than planar substrates. Geometric differences (i.e., cylindrical shape as opposed to flat surface) can likely lead to differences in polymer

density, which can therefore lead to differences in the way KOH diffuses through the polymer. This can be addressed with alterations to the SCALES process, such as KOH etching after attaching undecenol attachment but before polymerization.

Because of the round geometry, Si nanowires will have different crystal orientations around the nanowire circumference. Additionally, crystal orientation is a known factor impacting interface state density,<sup>136</sup> so this will certainly lead to differences in performance between the planar and nanowire devices. Dopant-patterned planar substrates of different crystal orientation could be fabricated to probe the impact of crystal orientation and to get baseline estimates of interface state density for each. The planar studies from this work are useful for demonstrating the gate stack deposition process and gaining insight about process parameters, but, ultimately, future work must transition to demonstrating reliable SCALES patterning and AS-ALD on nanowires.

### *6.2.3 High Throughput Manufacturing*

The ultimate vision of being able to disperse transistors across any substrate and then print interconnections between them requires a very large amount of nano-modular devices. To manufacture very large quantities of nanowire devices, we can leverage the paradigm shift from two-dimensional fabrication (i.e., planar wafers) to three-dimensional manufacturing (i.e., solution-based processing in reactors).<sup>2</sup> The bottom-up, solution-based techniques used for SCALES patterning were pursued for their ability to be scaled up using chemical reactors. ALD processes can achieve higher throughput via a continuous process like spatial ALD.<sup>57</sup> And nanowires can be synthesized at a larger scale by growing them in high surface area silica microcapsules.<sup>205,206</sup> Producing nanowire devices at a very large

scale will also likely require separations for quality control, similar to chemical processing. Techniques to sort nanowires based on characteristics like carrier density and geometry can be considered, such as electro-orientation spectroscopy and density gradient ultracentrifugation.<sup>2</sup>

#### 6.2.4 *Interconnecting Nanowire Devices*

Forming customized circuits with modular nanowire devices requires interconnections between the devices. One way to interconnect devices is by printing metal lines between devices with metallic nanoparticle inks. The dispersed nanowire devices could be imaged to identify the location of each device and connections can be manually designed or software can be programmed to adaptively design interconnection pathways to form circuits. Potential printing techniques to use include inkjet printing,<sup>207</sup> aerosol jet printing,<sup>208</sup> and electrohydrodynamic jet (e-jet) printing,<sup>209</sup> with e-jet printing offering the best resolution and smallest feature size.

Achieving good ohmic contact between the semiconductor nanowire and metallic nanoparticles will be a challenge. We know that printing directly to nanowires does not give good contact because current cannot easily flow through the native Si oxide layer on the nanowire. Typically metal-semiconductor contacts are annealed to form metal silicides, but Pt requires higher temperatures (500-600 °C) to form a silicide.<sup>210</sup> Since annealing at high temperatures after gate stack deposition is not an option, pre-formed ohmic contacts could be investigated as an alternative approach. For instance, with very highly doped ends on a nanowire, a separate SCALES patterning step could be combined with AS-ALD to

deposit Pt on the ends of the wire. The nanowire could be annealed to form a silicide before gate stack deposition, and the printed interconnects could contact the silicide segment.

## APPENDIX A. PMMA POLYMERIZATION PROCEDURE

Table A.1. Detailed procedure for PMMA polymerization.

	Step	Process Details
1	Setup	<ul style="list-style-type: none"> <li>• clean HF beaker - fill with HNO<sub>3</sub> and leave on hot plate (turn to black line, ~ 60 °C)</li> <li>• turn on left side hotplate in glovebox (high setting, dial on 10, 150 °C)</li> <li>• gather and label vials</li> <li>• gather ~10 syringes and needles (remove packaging)</li> </ul>
2	Prepare samples	<ul style="list-style-type: none"> <li>• Cut wafer to fit flat in vials</li> <li>• UV ozone treatment for 30 min               <ul style="list-style-type: none"> <li>○ Select <i>vacuum storage</i> on UV Ozone tool in MCF to leave in vacuum after ozone ends</li> </ul> </li> </ul>
3	Prepare 5% u-ol solution	<ul style="list-style-type: none"> <li>• Transfer vials/syringes into glovebox</li> <li>• Combine 19 mL mesitylene (<i>mesi</i>) and 1 mL undecanol (<i>u-ol</i>) in septum vial</li> <li>• Fill ~5 mL of mesitylene in mesi vial</li> <li>• Transfer u-ol out of glovebox to purge with N<sub>2</sub> for ~10 min</li> <li>• Note: Need to make a fresh solution each (polymerization does not work as well if using an old solution – often end up with thinner PMMA film)</li> </ul>
4	Etch native SiO <sub>2</sub>	<ul style="list-style-type: none"> <li>• 10-20 sec dip in BOE (undiluted), rinse with DI H<sub>2</sub>O and blow dry               <ul style="list-style-type: none"> <li>○ Work quickly to prevent oxide regrowth</li> </ul> </li> <li>• Immediately transfer samples and purged u-ol solution into glovebox               <ul style="list-style-type: none"> <li>○ Note: hotplate should be heated to 150 °C by now</li> </ul> </li> </ul>
5	U-ol deposition	<ul style="list-style-type: none"> <li>• Place samples in labelled u-ol vials face up</li> <li>• Syringe ~5 mL of u-ol solution in each vial</li> <li>• Place in hotplate wells for <b>2 hours at 150 °C</b></li> </ul>
6	Prepare PMMA solution	<ul style="list-style-type: none"> <li>• Note: can prepare PMMA solution now or during BIBB step</li> <li>• Notes on measuring:               <ul style="list-style-type: none"> <li>○ use twisting motion with plastic scoops to measure and drop in vial</li> <li>○ Pull arms back to same position each time while waiting for scale to stabilize to get accurate mass measurements</li> </ul> </li> <li>• Carefully measure catalysts in septum vial: (recommended order)               <ul style="list-style-type: none"> <li>○ 20 mg CuBr<sub>2</sub> (black powder)</li> <li>○ 40 mg CuBr (yellow powder)</li> <li>○ 180 mg BPY (white powder)                   <ul style="list-style-type: none"> <li>▪ (<i>BPY = 2,2'-bipyridyl or 2,2'-bipyridine</i>)</li> </ul> </li> </ul> </li> <li>• Syringe 1.5 mL of dimethylformamide (<i>DMF</i>) into septum vial               <ul style="list-style-type: none"> <li>○ Solution immediately turns dark brown</li> <li>○ Swirl carefully to help dissolve catalysts</li> </ul> </li> </ul>

Table A.1 (continued)

6	<p>Prepare PMMA solution  (continued)</p>	<ul style="list-style-type: none"> <li>• Meanwhile, remove inhibitor from methyl methacrylate (<i>MMA</i>) solution:               <ul style="list-style-type: none"> <li>○ Measure 16 mL MMA into MMA vial</li> <li>○ Remove plunger from Al<sub>2</sub>O<sub>3</sub> packed syringe and place syringe in rem vial</li> <li>○ Carefully drop all 16 mL of MMA into the syringe and let flow through inhibitor-removing Al<sub>2</sub>O<sub>3</sub> (drips through slowly)</li> </ul> </li> <li>• Syringe the inhibitor-removed MMA into septum vial and cap tightly</li> <li>• Note: solution should dark brown in color (almost looks like soy sauce) and we do typically see a little bit of undissolved particulates at bottom</li> <li>• Transfer out of glovebox to purge with N<sub>2</sub> for ~10-15 min then back into glovebox</li> </ul>
7	Rinse samples	<ul style="list-style-type: none"> <li>• Remove vials from hotplate and let cool for a few minutes               <ul style="list-style-type: none"> <li>○ Remove vials with large tweezers to avoid melting gloves</li> </ul> </li> <li>• Place sample in mesi rinse vial for 30 sec then remove and blow dry with squeeze bottle               <ul style="list-style-type: none"> <li>○ Blowing dry is important for film uniformity</li> </ul> </li> <li>• Repeat for each sample</li> </ul>
8	BIBB deposition	<ul style="list-style-type: none"> <li>• Using large glass syringe, put ~10 mL toluene (<i>tol</i>) in tol rinse vial and 7 mL toluene in each BIBB (<i>bromoisobutyryl bromide</i>) vial</li> <li>• Add 0.25 mL of triethylamine (<i>TEA</i>) in each BIBB vial using 1 mL syringe</li> <li>• Place each sample face up in a BIBB vial</li> <li>• Syringe BIBB into pipette to very slowly (drop-by-drop) add 1 mL of BIBB in each BIBB vial</li> <li>• Cap vials and let sit for <b>2 hours</b> at <b>room temp</b></li> <li>• Turn on right side hot plate, set point 90 °C</li> <li>• Note: We tried using a stir bar to stir solution at this step, but that was scratching the Si surface, so now we skip that and it still works well without it</li> </ul>
9	Rinse samples	<ul style="list-style-type: none"> <li>• Note: rinse vials should be at least half full</li> <li>• Place sample in toluene rinse vial for 5 min, then move to acetone rinse vial for 5 min, then methanol rinse vial for 5 min, then blow dry</li> <li>• Repeat for each sample concurrently</li> </ul>
10	Polymerization	<ul style="list-style-type: none"> <li>• Note: Hot plate should be heated to 90 °C by now</li> <li>• Place samples face up in labelled PMMA vials and syringe ~4 mL of PMMA solution in each vial</li> <li>• Place in hotplate wells for <b>4 hours</b> at <b>90 °C</b></li> </ul>

Table A.1 (continued)

11	Final rinse	<ul style="list-style-type: none"> <li>• Remove vials from hotplate and let cool for a few minutes</li> <li>• Place sample in acetone rinse vial for 10-20 sec then remove and place in acetone soak vial to leave overnight</li> <li>• Repeat for each sample</li> <li>• Next day, remove each sample and blow dry with squeeze bottle</li> <li>• Notes on thickness:             <ul style="list-style-type: none"> <li>○ PMMA films after 4 hr are typically brown (~ 40-60 nm)</li> <li>○ A blue colored film is ~ 100 nm, which we used to see with the old process but rarely with the new one</li> </ul> </li> </ul>
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## APPENDIX B. CHARACTERIZATION METHODS

### B.1 Physical Characterization

#### *B.1.1 Spectroscopic Ellipsometry*

Spectroscopic ellipsometry measurements were performed with a Woollam M200 Spectroscopic Ellipsometer (J. A. Woollam), and the accompanying CompleteEASE software was used for all spectra fitting. Measurements were typically made with an array or line of 3-5 points on each sample. And the CompleteEASE materials database provided models for Si, HfO<sub>2</sub>, SiO<sub>2</sub> (native oxide), SiO<sub>2</sub> (thermal oxide), Al<sub>2</sub>O<sub>3</sub>, ZrO<sub>2</sub>, TiO<sub>2</sub>, PMMA, TiN, and Pt. Films with multiple layers (e.g., HfO<sub>2</sub> with SiO<sub>2</sub> underneath) were typically fit by measuring the first film thickness and then assuming that film thickness when fitting the top layer.

#### *B.1.2 X-ray Photoelectron Spectroscopy*

X-ray Photoelectron Spectroscopy (XPS) measurements were performed with the K-Alpha X-ray Photoelectron Spectrometer System (Thermo Scientific) in the IEN Materials Characterization Facility. This XPS has a monochromatic Al K $\alpha$  source and kinetic energy of 1486.6 eV. The measurements were made with a pass energy of 50 eV and a spot size of 400  $\mu\text{m}$  (except for XPS area mapping), and the flood gun was used for non-conductive samples. The typical detection depth is  $\sim 5$  nm. All XPS peak fitting was performed with XPS Peak 4.1 software. For XPS mapping, the minimum spot size (30  $\mu\text{m}$ ) was used with only 1 scan per point (to reduce experiment run time). MATLAB (MathWorks) was used to analyze the XPS map data.

### *B.1.3 Scanning Electron Microscopy and Energy Dispersive X-ray Spectroscopy*

Scanning Electron Microscopy (SEM) was performed using the Hitachi SU8230 FE-SEM (Field Emission-SEM) in the IEN Materials Characterization Facility. Energy Dispersive X-ray Spectroscopy (EDS) was also performed with the Hitachi SU8230 FE-SEM and analyzed with Oxford Instruments Aztec software.

## **B.2 Electrical Characterization**

A Keithley 4200-SCS semiconductor parameter analyzer and Cascade Summit 12000 semi-automatic probe station (formerly Cascade Microtech, currently FormFactor, Inc.) were used for all electrical characterization at room temperature and ambient pressure. Between one and four 19  $\mu\text{m}$  DCP-HTR probe tips (FormFactor, Inc.) were used to contact devices, depending on the measurement type.

### *B.2.1 Capacitor Measurements*

To perform Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) measurements with the Keithley, the four red SMA-to-SMA cables (CA-447 cables, Keithley) are connected to the four inputs (i.e., HCUR, HPOT, LPOT, and LCUR) on the CVU (4210-CVU, Keithley). SMA-to-BNC adapters are attached to the other end of each cable. The LPOT and LCUR cables are connected to the two chuck connections on the probe station to form CVL. And the HCUR and HPOT cables are attached to two slots on the probe station, and those two probe station cables are connected to a single probe tip manipulator (with a DCP-HTR probe tip inserted) to form CVH. To compensate for extra capacitance due to cabling, the Connection Compensation process is used. First, acquire

CVU compensation data for custom cable length, then acquire CVU compensation data for open corrections. For additional setup information and troubleshooting, refer to the Keithley Manual and Keithley Application Notes found online.

The CV test is then performed by gently probing the top metal electrode on one device. A CVU voltage sweep is applied to CVH from 2 V to -2 V (a wider range to higher voltages can impact the oxide properties and ultimately affect measurement results). The AC voltage is 50 mV and measurement frequency is typically 100 kHz (though a range of frequencies is typically measured for each device, from 1 MHz down to 10 kHz). For best results, the Keithley CV test should be run in quiet mode, and make sure the open cable compensation box is checked (to apply connection compensation). The measurement model should be the parallel RC circuit. And the output file will include capacitance and conductance values at a given voltage for each data point. A typical C-V (a) and G-V plot (b) at three frequencies obtained with this method is shown in Figure B.1.

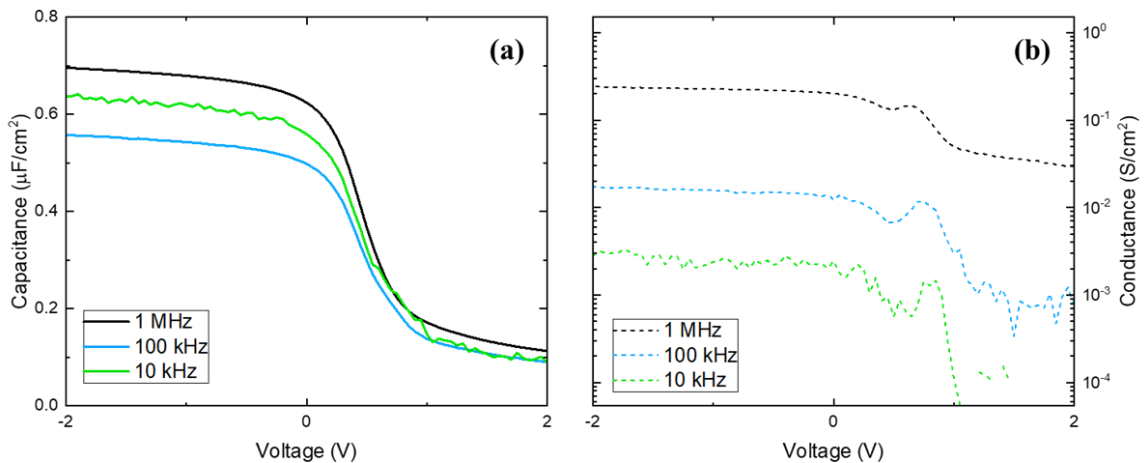


Figure B.1. Representative C-V (a) and G-V (b) curves (normalized to device area) at three frequencies for a TiN-Al<sub>2</sub>O<sub>3</sub>-Si(100) (p-type Si, 0.01-0.02  $\Omega\text{-cm}$ ) MOS capacitor (85  $\mu\text{m}$  x 85  $\mu\text{m}$ ) used as a test device, fabricated with a shadow mask.

To measure the DC current leaking through the capacitors, two BNC-to-BNC cables are connected to two Force SMUs on the Keithley. One cable is connected to the chuck port on the probe station and the other is connected to a port on the probe station that connects to one probe tip manipulator. An I-V measurement is then performed by applying a voltage sweep and measuring current on the probe. A typical voltage sweep from 2 V to -2 V is sufficient to measure leakage current, but a wider range can be used to find breakdown voltage.

### *B.2.2 Resistor and Transistor Measurements*

As an early proof-of-concept for fabricating electronic devices with Si nanowires, we made resistor, diode and transistor devices using conventional fabrication techniques. While this does not align with the modular device framework and does require photolithography for patterning, it was a good way to study the electrical properties of the nanowires earlier in the project. Resistor measurements were particularly useful to estimate the dopant concentration of p-type and n-type nanowires, especially since we do not have a readily available physical characterization technique to measure nanowire dopant concentration. We also fabricated nanowire MOSFET devices to test the baseline electrical performance of the nanowires synthesized in the lab.

To fabricate nanowire resistor and diode devices, the nanowires were mechanically transferred onto a Si substrate with a thick insulating SiO<sub>2</sub> layer. The MLA was used to pattern either two or four metal electrodes along the length of the wire. The substrate was dipped in HF or BOE for 15 sec prior to metal deposition to etch the native oxide layer. Metal was deposited via e-beam evaporation, typically 20 nm of titanium (as an adhesion

layer) followed by 120 nm of gold. Finally, acetone was used to lift-off the photoresist, with the pads remaining to contact the wires. An optical microscope image of a four-electrode nanowire resistor is shown in Figure B.2a. To measure electrical performance with the Keithley, BNC-to-BNC cables were connected from the Force SMUs on the Keithley to the ports on the probe station. Each pad was probed, and a voltage sweep was applied while measuring current. A current-voltage (I-V) curve from a two-electrode measurement of a p-type nanowire is shown in Figure B.2b, and I-V curves showing diode behavior of p-n nanowire devices is shown in Figure B.2c. Four-electrode measurements were typically used to more accurately estimate carrier concentration by minimizing contact resistance. In a four-electrode measurement, a current is applied across the outer two pads and the voltage drop between the inner two pads is measured. This voltage drop combined with the nanowire dimensions can be used to extract resistivity of the nanowire, which can be correlated with carrier concentration.

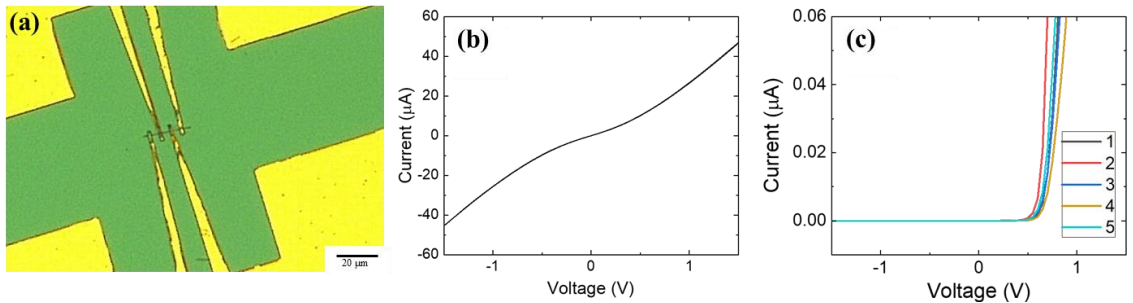


Figure B.2. (a) Optical microscope image of a 4-electrode nanowire resistor device; (b) I-V curve from a 2-electrode measurement of a p-type Si nanowire; (c) I-V curves showing diode behavior of p-n nanowire devices.

The fabrication process for the nanowire MOSFETs was mostly developed by other researchers in the group and is outside the scope of this work. However, I did help bridge the gap between researchers and fabricated and measured some NW transistors as

an early study. Briefly, to fabricate the transistor devices, n-p-n nanowires (dimensions in Figure B.3a) were mechanically transferred onto a thick-SiO<sub>2</sub> substrate and the gate oxide (Al<sub>2</sub>O<sub>3</sub> in this case, but HfO<sub>2</sub> is now used) was deposited across the entire wire-covered substrate via ALD. The source/drain were patterned with the MLA, and then e-beam evaporation was used to deposit 20 nm Ti and 120 nm of Au. Then the gate was patterned with the MLA, and e-beam evaporation was used to deposit 120 nm Al (with a 20 nm Ti/120 nm Au capping layer). The final device can be seen in the optical microscope image in Figure B.3b. Electrical characterization was performed with the Keithley by connecting three probes to the Force SMUs and probing each pad (i.e., source, drain, gate). A constant voltage bias is applied across the source and drain, and the drain current is measured while sweeping the voltage applied to the gate electrode. Figure B.3c shows the drain current and gate current for an applied gate voltage between 2 V and -2 V. Other researchers in the group are improving the fabrication process and studying these nanowire transistors in detail to be published in future work.

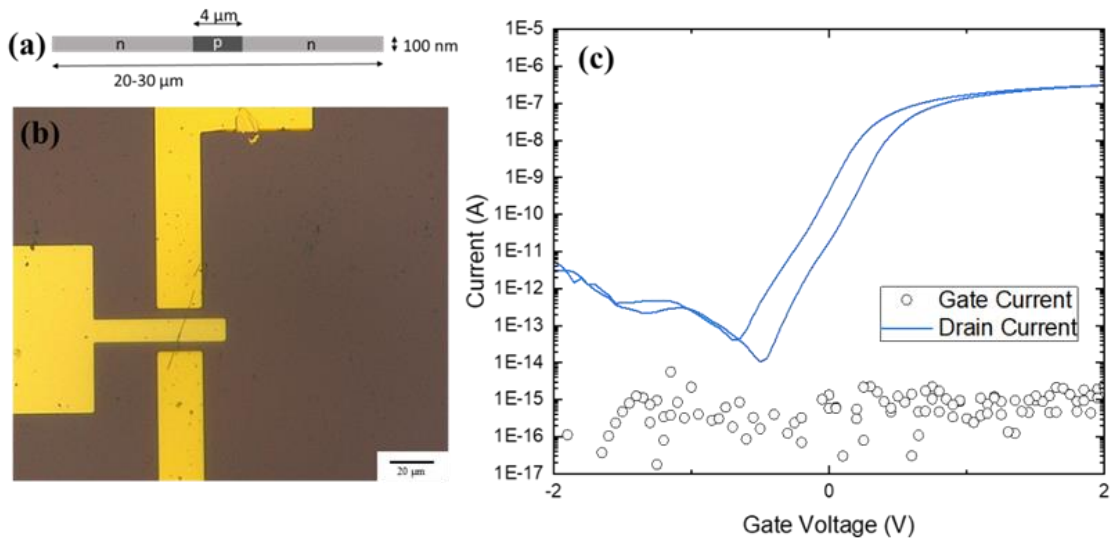


Figure B.3. (a) Schematic diagram of n-p-n nanowires used in the transistor device; (b) optical microscope image of a nanowire transistor; (c) I-V behavior of n-p-n nanowire transistor device.

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