

**SILICON-GERMANIUM DEVICES AND CIRCUITS  
FOR CRYOGENIC AND HIGH-RADIATION  
SPACE ENVIRONMENTS**

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Edward Wilcox

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SILICON-GERMANIUM DEVICES AND CIRCUITS  
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Approved by:

Dr. John D. Cressler, Advisor  
School of Electrical and Computer Engineering  
*Georgia Institute of Technology*

Dr. Gregory Durgin  
School of Electrical and Computer Engineering  
*Georgia Institute of Technology*

Dr. Ioannis Papapolymerou  
School of Electrical and Computer Engineering  
*Georgia Institute of Technology*

Date Approved: April 5, 2010

This work is dedicated, to nobody's surprise, to Roy "Doc" Halladay.

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## SUMMARY

This work represents several years' research into the field of radiation hardening by design. The unique characteristics of a SiGe HBT, described in Chapter 1, make it ideally suitable for use in extreme environment applications.

Chapter 2 describes the total ionizing dose effects experienced by a SiGe HBT, particularly those experienced on an Earth-orbital or lunar-surface mission. In addition, the effects of total dose are evaluated on passive devices.

As opposed to the TID-hardness of SiGe transistors, a clear vulnerability to single-event effects does exist. This field is divided into three chapters. First, the very nature of single-event transients present in SiGe HBTs is explored in Chapter 3 using a heavy-ion microbeam with both bulk and SOI platforms [31]. Then, in Chapter 4, a new device-level SEU-hardening technique is presented along with circuit-design techniques necessarily for its implementation. In Chapter 5, the circuit-level radiation-hardening techniques necessarily to mitigate the effects shown in Chapter 3 are developed and tested [32].

Finally, in Chapter 6, the performance of the SiGe HBT in a cryogenic testing environment is characterized to understand how the widely-varying temperatures of outer space may affect device performance.

Ultimately, the built-in performance, TID-tolerance, and now-developing SEU-hardness of the SiGe HBT make a compelling case for extreme environment electronics. The low-cost, high-yield, and maturity of Si manufacturing combine with modern

bandgap engineering and modern CMOS to produce a high-quality, high-performance BiCMOS platform suitable for space-borne systems.

## CHAPTER 1

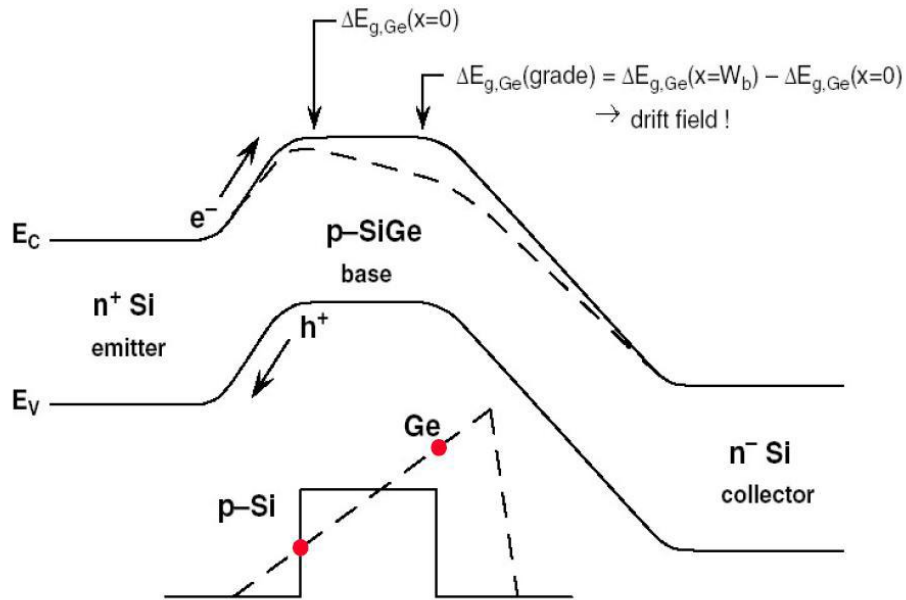
### INTRODUCTION TO SILICON GERMANIUM

Silicon-Germanium (SiGe) BiCMOS technology is a strong platform for emerging high-frequency circuit designs. The latest generations of SiGe technology combine the extreme performance metrics of exotic III-V platforms with the manufacturability, yield, and cost advantages present in standard silicon processing. Modern SiGe BiCMOS platforms combine SiGe heterojunction bipolar transistors (SiGe HBTs) with advanced CMOS scaling to enable fabrication of radar transceivers, high-speed data converters, high-frequency communication links, and a host of other circuitry designed for extreme temperature and radiation environments, such as those found in orbit or in deep space [1]. While older Si-only platforms suffer under low-temperature or high-radiation conditions, it is well-established that SiGe HBTs see performance improvements at low-temperature [2] and negligible degradation even after lengthy radiation exposure [3].

For years, the Si BJT has played a central role in the semiconductor and integrated circuit world. The very name of Silicon Valley speaks to the massive investment in and profitability of silicon platforms. Such enormous research that has been put into silicon technology over the decades has resulted in incredibly cheap, reliable, and simple manufacturing and design processes. The mysterious world of the III-V transistor and other bandgap-engineered technologies occupies only a small slice of the overall semiconductor pie due to the expensive cost and low-yield typical of these advanced platforms. Only applications requiring the highest-speed, lowest-noise, and highest-gain

transistors have sought to use heterojunction devices in the past. The silicon-germanium HBT, made possible with advances in processing techniques such as UHV/CVD (ultra-high vacuum chemical vapor deposition), offers a similar level of bandgap-engineering performance that is compatible with existing silicon processes. Only the epitaxial growth of a SiGe base is added, while retaining the yield and economies-of-scale attributable to silicon [7].

The performance of a SiGe HBT is due to this germanium gradient built across the base, from collector to emitter. Because silicon and germanium have different bandgap energies, their combination has an intermediate bandgap energy, so grading germanium across the base creates a bandgap gradient whose inherent electric fields sweep minority electrons across the base, from emitter to collector, at high speed, as diagrammed in Fig. 1.



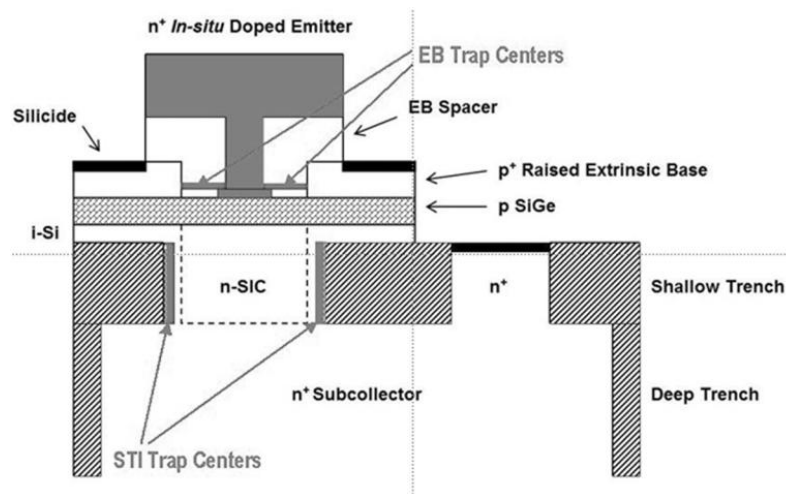
**Figure 1.** Energy band diagram of a SiGe HBT, showing the effects of a germanium gradient across the base. Germanium doping profile is illustrated at the bottom (after [7]).

The following research further characterizes performance of the SiGe HBT in extreme environments, such as those found in the high-radiation and low-temperature environment of outer space, and explores techniques to both characterize their effects and mitigate their consequences.

## CHAPTER 2

### TOTAL DOSE EFFECTS IN SIGE TECHNOLOGY

The study of radiation effects on SiGe technology can be divided into two broad topics: total ionizing dose (TID), and single event effects (SEE). TID effects are those caused by long-term exposure to radiation, which slowly ionizes the oxides within a device and typically appears as increased base-leakage current [4]. For SiGe transistors, the primary concern is the introduction of oxide traps in the thin emitter-base spacer [5] shown in Fig. 2.

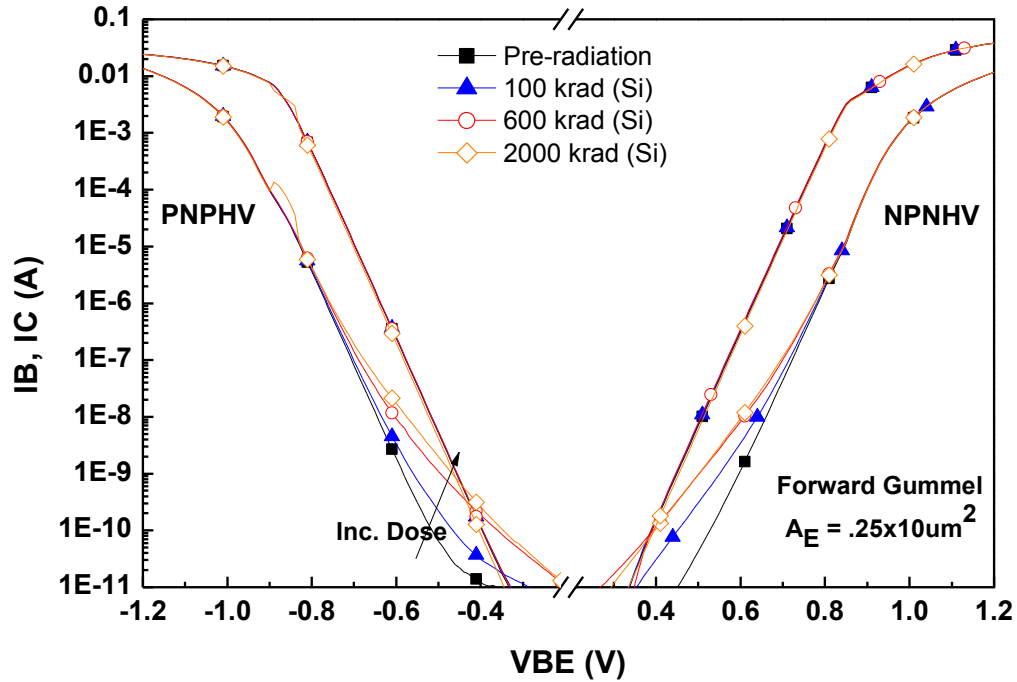


**Figure 2.** Cross sectional diagram of a SiGe HBT showing locations of radiation-induced traps (after [29]).

Because of the high-doping of the base and narrow width of the spacer oxide, the consequences of total dose exposure are minimized compared to traditional Si devices [4]. Over time, long-term exposure to the particle fluxes seen on a typical space mission can lead to significant changes in device performance, and eventually circuit failure.

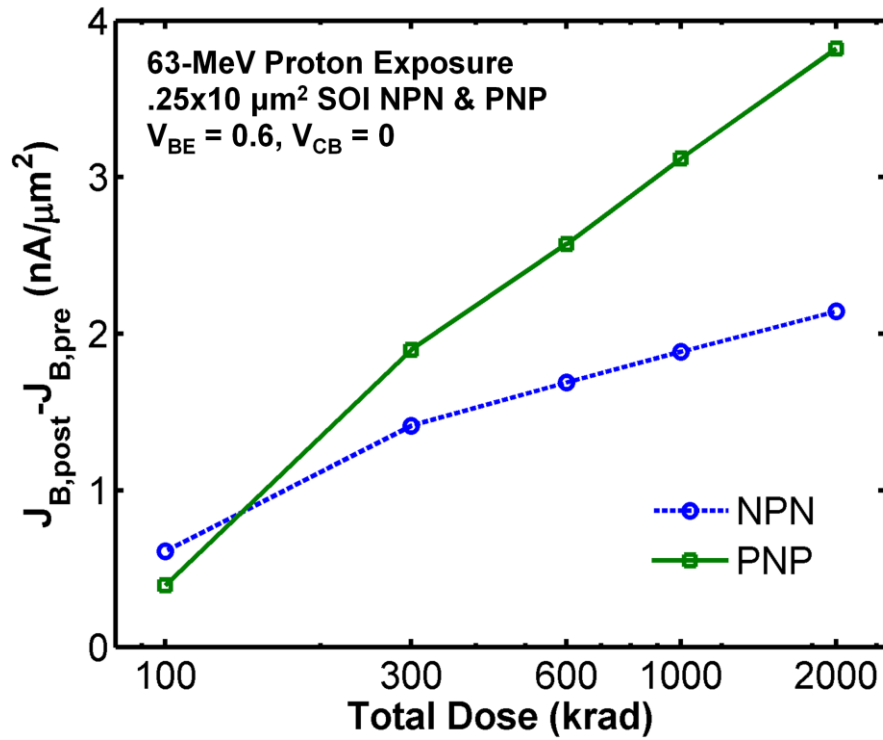
In preparation for the single-event experiment to be described in Chapter 3, a variety of SiGe transistors were exposed to proton radiation to evaluate their response and confirm their TID-hardness. Because the devices-under-test were individual test structures from a new 50-GHz peak- $f_T$  complementary SiGe platform built on SOI, a novel comparison between *npn* and *pnp* transistors was possible. Total-dose testing was performed at the Crocker Nuclear Lab at the University of California at Davis. The devices were irradiated with a 63-MeV proton beam with a dose rate of approximately 1 krad/s. The dosimetry, performed with a 5-foil secondary emission monitor, calibrated against a Faraday cup, is accurate to about 10% [9]. Multiple devices, including both *npn* and *pnp* transistors, were exposed to a 63-MeV proton beam until they reached equivalent doses of up to 2 Mrad in SiO<sub>2</sub>. Pre-, intermediate-, and post-irradiation measurements were performed on-site using an Agilent 4156 Semiconductor Parameter Analyzer, with all terminals grounded during exposure. A variety of devices for each type (*npn* and *pnp*) were measured with varying emitter dimensions.

Fig. 3 shows the forward Gummel characteristics for both the *pnp* and *npn* devices before and after exposure. The transistors showed only minimal degradation, even at 2 Mrad. At common VBE conditions approaching 0.8 to 0.9 volts, the radiation-induced change in  $\beta$  is negligible, demonstrating this technology's expected built-in TID tolerance.



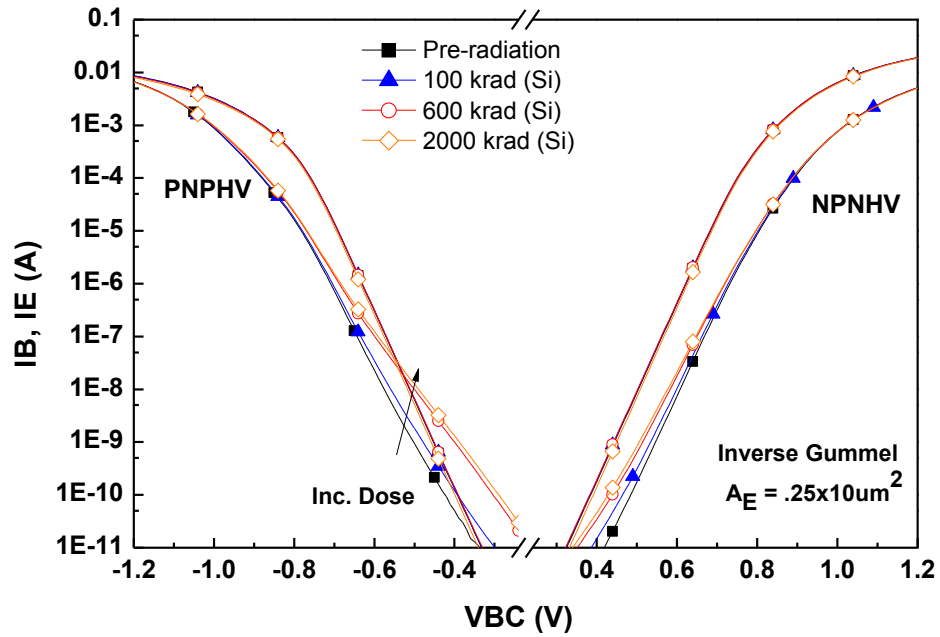
**Figure 3.** Forward Gummel measurements taken throughout proton exposure, up to 2 Mrad.

Because any differences between the *npn* and *pnp* devices are not apparent in Fig. 3, a figure was generated showing the base current density as a function of logarithmic total dose for a fixed  $V_{BE}$  of 0.6 V. That data, shown in Fig. 4, indicates little difference between the two at low doses, but a larger variation above 600 krad. While the increased vulnerability of the *pnp* device is worth investigating further, it disappears entirely at higher  $V_{BE}$  conditions, and would be irrelevant at the doses expected for an Earth-orbit or lunar mission (< 100 krad) [10].



**Figure 4.** Base leakage current relative to pre-radiation data for *npn* and *pnp* devices.

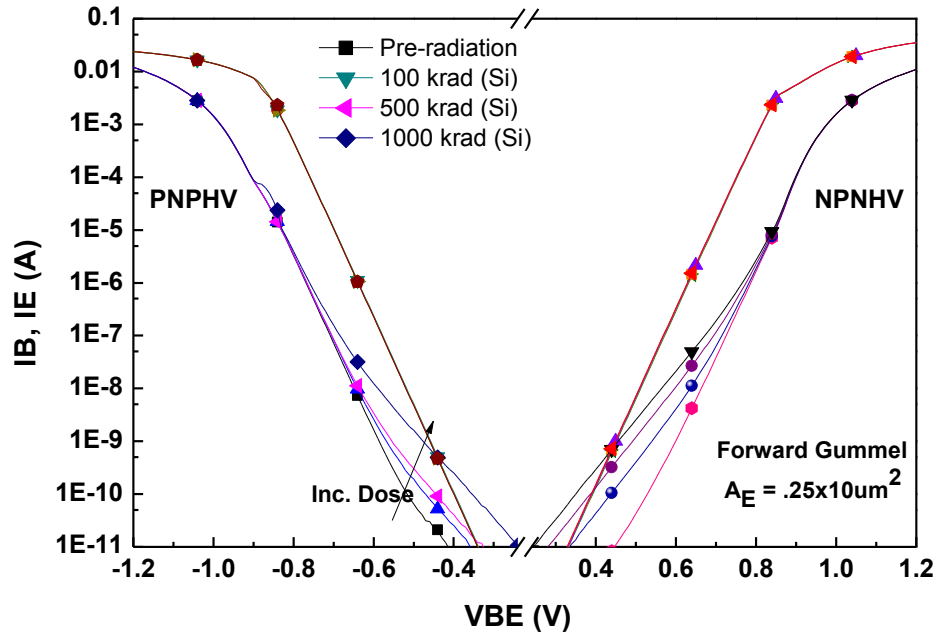
While measuring the forward gummel data for each dose point, it was trivial to also measure the inverse gummel as well. For this measurement, the physical base and emitter are held at ground while the physical collector is pulled low and acts as the electrical emitter. Because the device is physically operating differently, the leakage currents created by radiation-induced oxide traps could differ from the forward mode. Fig. 5 shows the inverse gummel proton data for *npn* and *pnp* transistors.



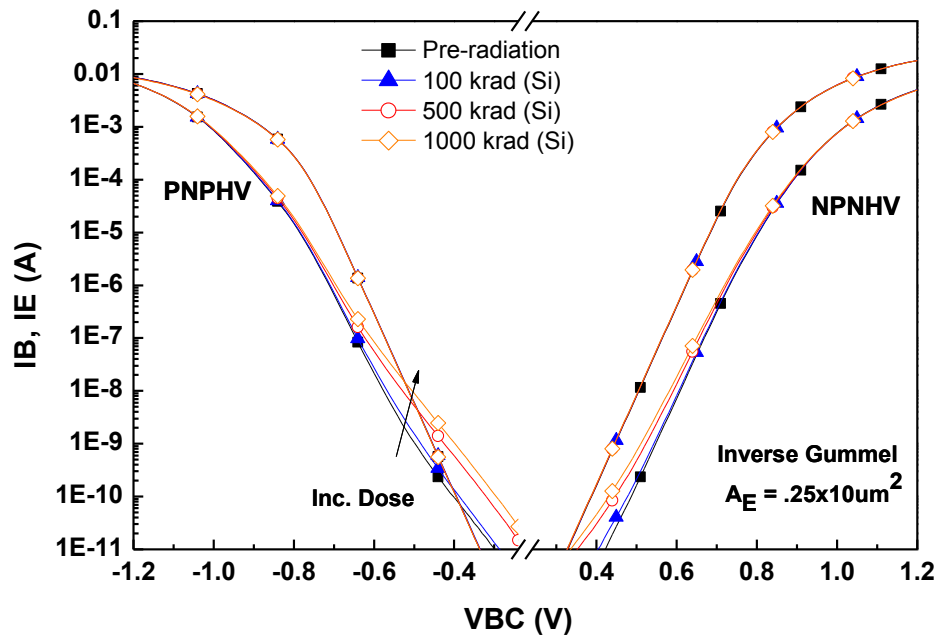
**Figure 5.** Inverse gummel curves during proton exposure for *npn* and *pnp* devices.

Interestingly, the inverse mode appears to be less sensitive to total dose than the forward mode for both the *npn* and *pnp* devices. Without more detailed information about the device structure of these SOI transistors it is impossible to identify the cause with certainty, but it would appear that the device is less subject to oxide trap creation when operated in the inverse mode.

To gain more total dose data on these complementary SOI devices, an X-ray experiment was conducted at Vanderbilt University. The same trends apparent in the proton data are evident in the X-ray shown in Fig. 6. The *pnp* device is slightly more vulnerable to excess base current caused by radiation than the *npn*, while in both cases the inverse mode operation (Fig. 7), while not ideal for most high-performance applications, appears to be more TID-immune, perhaps shedding some light on the sensitive regions of the actual transistors.



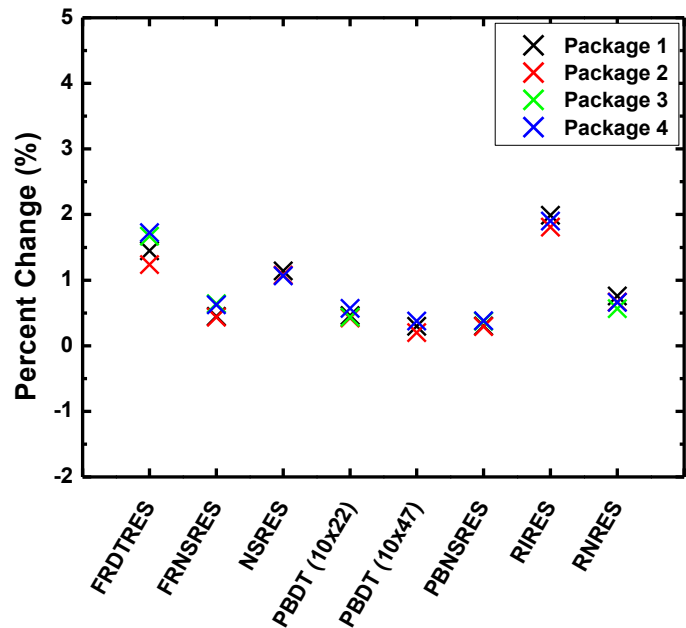
**Figure 6.** Effects of x-ray radiation on complementary SiGe on SOI devices.



**Figure 7.** Effects of x-ray radiation on devices operated in the inverse mode.

Active devices, such as the bipolar transistors studied above, are of course only part of a real circuit, which typically relies on passive components, such as resistors,

inductors, and capacitors, for proper functionality. Circuit design for extreme environments, therefore, can only be done safely with some knowledge of the radiation-hardness of these passives. To characterize the standard resistors included in a first-generation BiCMOS platform, a variety of test structures were exposed to 63 MeV proton radiation at the Crocker Nuclear Lab at UC Davis, as described previously. The resistor test structures were wire bonded and grounded throughout exposure, and the results are presented in Fig. 8.



**Figure 8.** Changes in resistance for eight different resistor structures present in IBM 5AM after 1 Mrad (SiO<sub>2</sub>) proton radiation.

The resistors measured included four each of eight different structure types. The most commonly used in circuit design include the PBDT (P+ Poly over DT) and the FRDT (high sheet resistance P+ Poly over DT). The PBDT in particular shows almost no change in resistance after 1 Mrad, while no resistor shows more than a 2% change. Because these changes are less than typical process variation, it can be reasonably

assumed by the circuit designer that radiation-induced resistor damage is negligible for standard space applications.

## CHAPTER 3

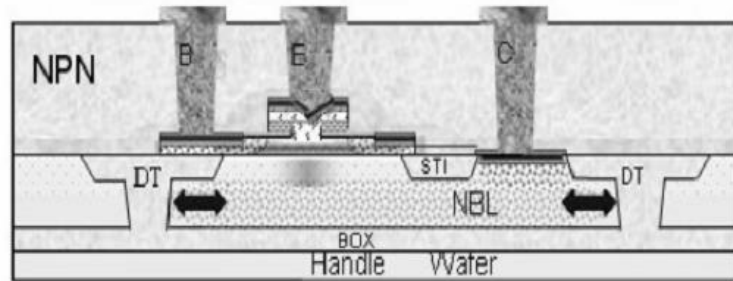
### SINGLE EVENT TRANSIENTS IN SIGE DEVICES

The other half of the radiation field is the study of single-event effects. Single-event effects are those caused by individual charged, energetic particles passing through the device structure. Energy deposited in the wake of the particle can cause significant voltage perturbations and the introduction of faulty data into a circuit. While it has been documented that SiGe HBTs have a built-in immunity to TID up to extremely high doses, there are clear vulnerabilities to single event effects [6, 7, 8].

Extensive research is currently on-going to develop an SEE-hard SiGe HBT to complement its built-in TID hardness [11, 12]. Whether in orbit around the Earth, or operating on the surface of another planet or moon, electronic systems are continuously exposed to bombardment from a variety of particles. Earth-orbital missions are particularly concerned with particles trapped in the Earth's magnetic field. High speed protons and electrons form two massive belts (the Van Allen belts) that circle the Earth and interact with any electronics in their path. Other particles, not trapped by Earth's magnetic fields but instead transiting across deep space, include solar flares and galactic cosmic ray, which consist of particles travelling at enormous energies (many GeV) [30]. Such ion strikes leave a trail of free carriers in their wake as they pass through the active regions of a semiconductor [13]. The induced electric fields and the associated recombination currents lead to perturbations on the transistor nodes. The effects of such perturbations on the system level can vary depending on the device type, system application, operating conditions, and so forth. As such, the broad topic of single-event

effects can be further broken down by the different phenomena caused by an ion-strike, such as single-event transients (SET), single-event upset (SEU), single-event latch-up (SEL), single-event functional interrupt (SEFI), and so on.

A classical single-event upset occurs when a highly-energetic, charged particle passes through a transistor, creating a cone of electron-hole pairs, primarily in the large, lightly-doped subcollector and substrate regions of a bulk npn SiGe HBT. This deposited charge is then collected by the reverse-biased subcollector-substrate junction [13] and swept into the collector node, where it may directly affect the circuit output. A SiGe HBT on SOI device, such as those described in the TID experiment from Chapter 2, may therefore be less susceptible to single-event effects because it lacks the reverse-biased substrate junction [14], as shown in Fig. 9.



**Figure 9.** Cross-section of an NPN SiGe on SOI device.

Without the presence of a bulk silicon substrate, the sensitive volume of the transistor should be restricted to just the active base, emitter, and collector regions, and thus the device should collect less charge as the ion passes through.

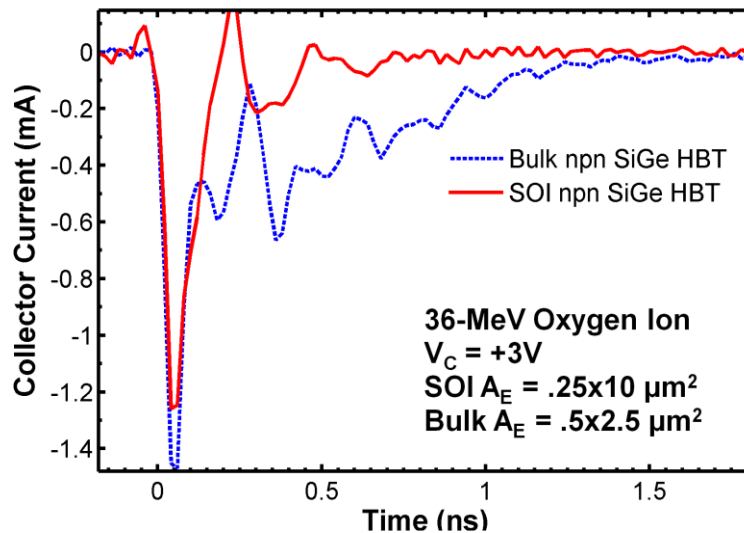
Previous investigations of device-level SEU sensitivity have focused on total charge collected by each terminal of a transistor [14, 15]. Such measurements require just an integrated charge collected over several tens of nanoseconds. However, they do not

provide a sense of the actual dynamics of the ion strike, nor do they allow a comparison of length of time the voltage is perturbed. Characterization of single-event transients is still a relatively new field, and requires extremely high-speed test equipment to capture small current transients that may last on the order of 200 ps. However, a better understanding of the exact transient waveforms occurring in SiGe HBTs can be used to develop better models to simulate ion strikes and construct circuits in such a way to minimize the effects of such transients.

Such an experiment was conducted using time-resolved ion-beam induced charge collection (TRIBICC) at Sandia National Laboratory using a heavy-ion microbeam that rasters 36-MeV oxygen atoms across the device area. The transients resulting from each ion strike were captured with a Tektronix DPO72004 20-GHz (50 GS/S) real-time oscilloscope. Each individual transient can then be viewed on its own as a function of time, or the peak amplitude can be plotted over the two-dimensional device cross-section to see the sensitive regions of the transistor. For this experiment, the same complementary SiGe on SOI transistors were used from Chapter 2, and were packaged using a custom-designed, high-speed radiation test fixture. The test structures were individually wire-bonded to microstrip transmission lines that led to SMA connectors and 40-GHz RF cables attached to the 20-GHz real-time oscilloscope, identical to the setup used to capture the circuit transients in [16]. An additional set of bulk SiGe npn HBTs with similar performance metrics were measured as well for comparison.

Fig. 10 shows an average of eight emitter-center ion-strike transients for both the SOI npn HBT and a standard bulk SiGe platform. This represents a “worst-case” strike, and averaging reduces some of the noise in the raw data to better facilitate comparisons.

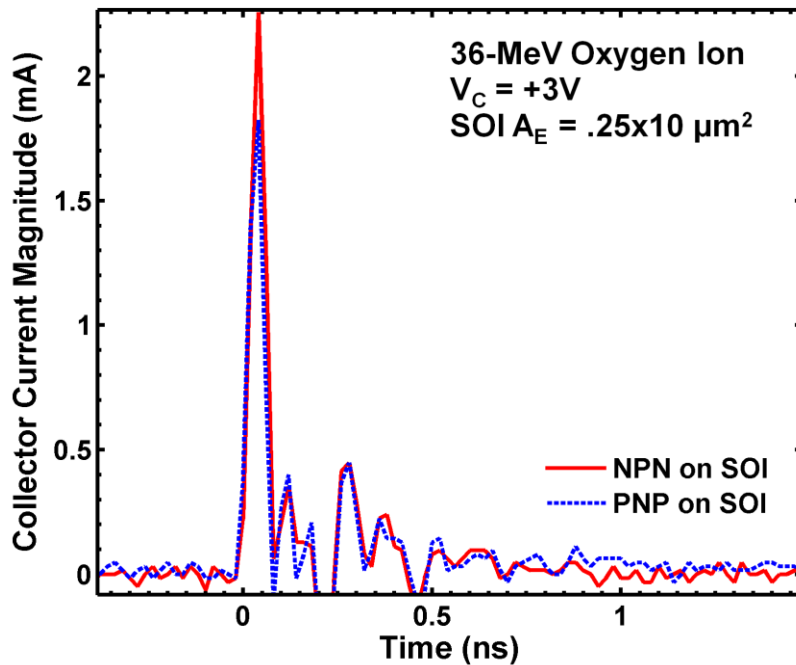
The SOI SiGe HBT recovers to zero transient current within approximately 250 ps, followed by a brief period of harmonic ringing associated with the minimal (though non-zero) capacitance of the measurement setup. The bulk *npn* SiGe HBT shows a significantly longer transient tail, however, which does not vanish until approximately 1.5 ns. Other research on bulk SiGe HBT devices with a similar peak *f*T has also shown a collector current transient that fades slowly over the course of a nano-second or longer [17] when an “off” transistor is struck. The present SiGe on SOI technology seems to completely eliminate the “long tail” of the transient strike present in the bulk technology. This raises the possibility of a potentially overhead-free SEU tolerant as-built SiGe on SOI platform.



**Figure 10.** Comparison of transient length for bulk and SOI SiGe *npn* transistors.

Worst-case transient waveforms were selected from both the *pnp* and *npn* transistors and their magnitudes are plotted in Fig. 11. The *npn* device shows a somewhat higher amplitude for the initial strike, about 2.5 mA, but both have nearly identical

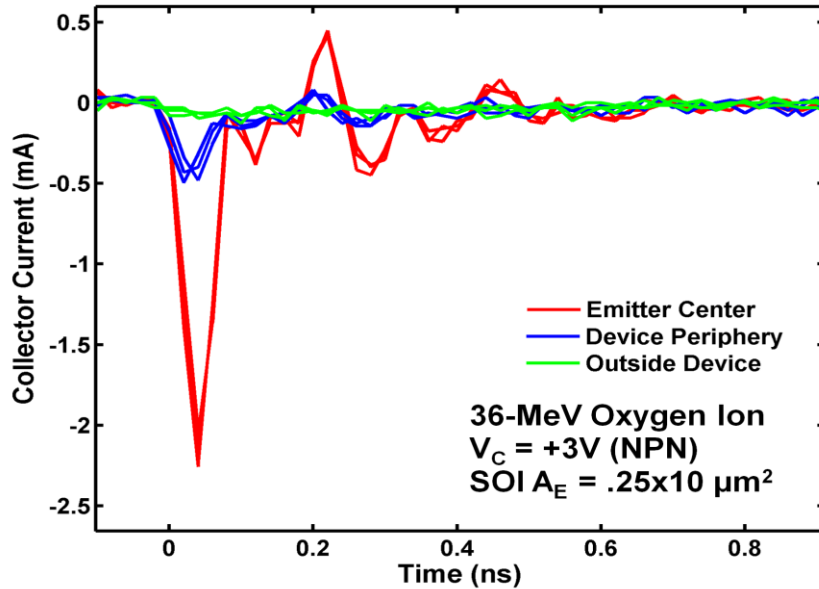
duration, in the 150 ps range. There appear to be no dramatic differences in SEU-sensitivity between the *npn* and *pnp* devices grown on SOI, attributable to the similar device stackup (but with reversed doping) for each. It should be noted that the amplitudes shown earlier in Fig. 10 appear smaller than those in Fig. 11 only because of the averaging employed in Fig. 10.



**Figure 11.** Comparison of *npn* vs. *pnp* devices (both SiGe on SOI).

Fig. 12 shows a selection of transients from different regions of the SOI *npn* device. A total of nine waveforms are presented, representing three distinct regions of device sensitivity. The largest peaks are from emitter-center strikes, while those from outside the deep trench isolation hold constant at zero, reinforcing the idea of the SOI transistor's complete immunity to external ion strikes. The intermediate-level transients are randomly selected from just outside the emitter stripe, but still inside the deep-trench.

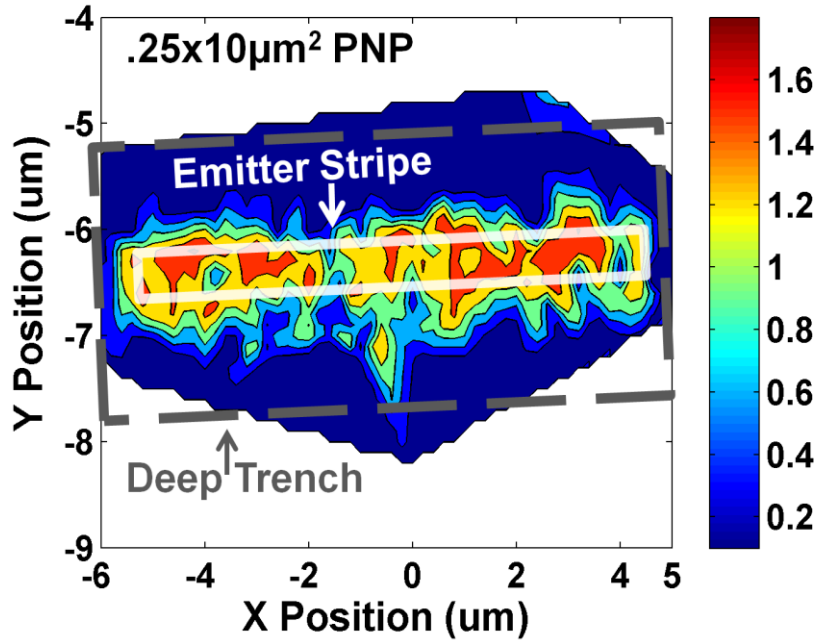
Because the very nature of SOI technology implies isolation from external events due to the lateral deep trench isolation and buried oxide below the device, it is logical to expect no transient current from an outside-DT strike, while a typical bulk platform is only isolated laterally and not vertically.



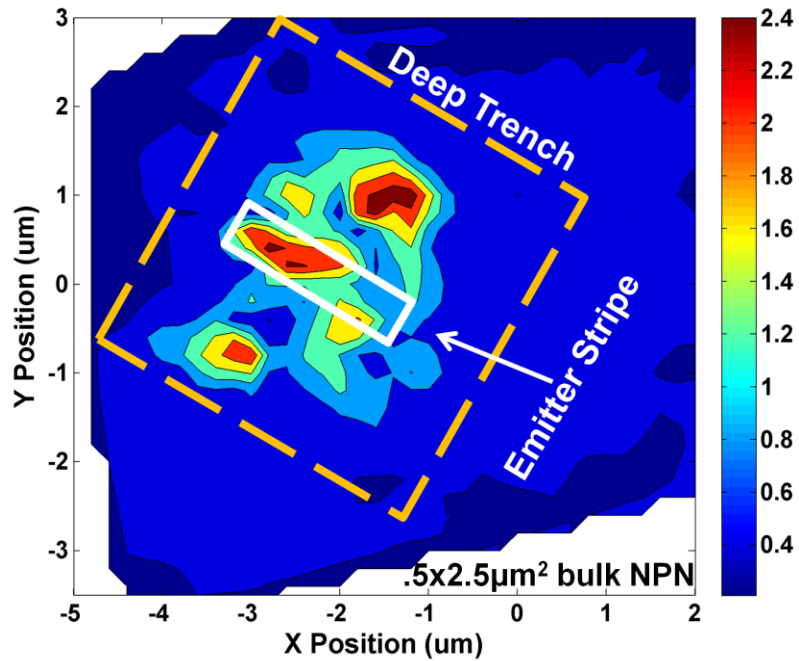
**Figure 12.** Selection of heavy-ion transients from varying locations on the transistor.

Since the microbeam was swept across a rectangular area and transients were saved for each point, a two-dimensional plot can be generated showing the peak collector current transient as a function of strike location. Such a plot can be used to evaluate the most sensitive areas of the device, and also to calculate the total sensitive cross-section. Fig. 13 clearly highlights the sensitive area of the *pn*p SiGe HBT on SOI. The rectangular outline of the device is quite distinct, and the 10  $\mu\text{m}$  device width can be measured directly. Similarly, the plot of bulk SiGe HBT transients is shown in Fig. 14. In the case of the bulk device, the transients occur over a much larger area relative to the active

emitter size, and in fact share a similar total sensitive area to the much-larger SOI transistor.



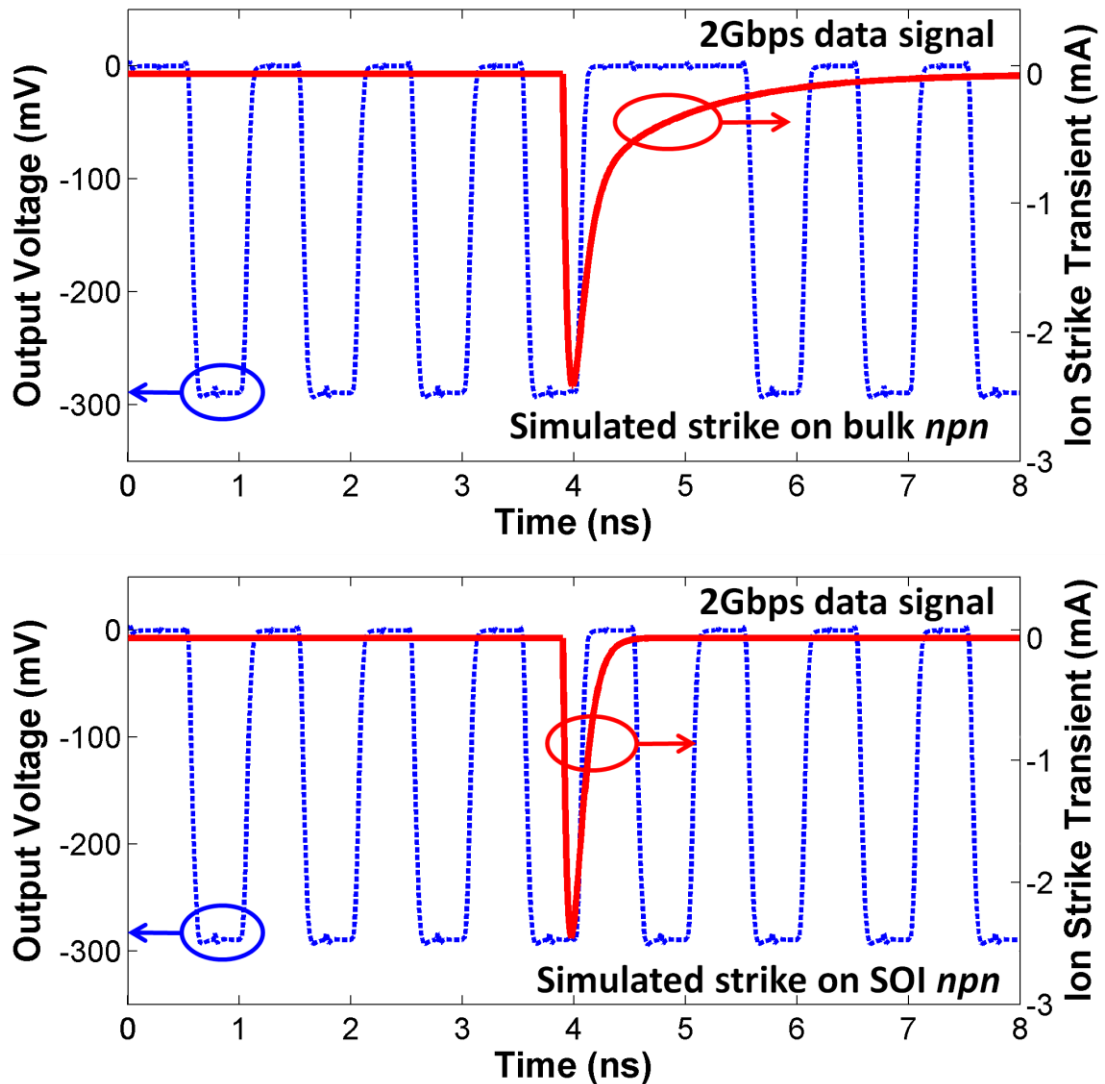
**Figure 13.** Peak IC transient as a function of 2-D position above the device.



**Figure 14.** Peak IC transient as a function of 2-D position for a bulk *npn*.

Dramatically reducing the duration of a single-event transient spike will directly benefit both analog and digital circuit designers. For analog applications, any reduction in transient duration will be easier to filter out and easier to recover from. For digital applications, a typical transient in a bulk platform, lasting on the order of a nanosecond, will become more of a risk as switching frequencies approach and exceed 1 GHz. At that speed, the signal will be upset for multiple clock edges and upset is likely to occur. Reducing the transient duration by an order of magnitude should reduce the number of bit upsets latched into, and propagated through, a digital circuit. To verify this, a simple *npn* SiGe HBT flip-flop circuit was simulated, and transients approximating those from bulk SiGe platforms were injected first, followed by transients approximating those measured for the SiGe HBT on SOI device for direct comparison. Fig. 15 shows an ion strike

occurring near a clock edge, where the data output of a bulk flip-flop (top) is corrupted while the output of the SOI flip-flop remains unaffected (bottom). The long ( $> 1$  ns) diffusion tail of the bulk transient, the primary difference between the two simulated ion strikes, appears to directly affect flip-flop SEU sensitivity. At higher data rates the bulk device becomes subject to increasing numbers of multiple-bit upsets, while the SOI device remains hard.



**Figure 15.** Simulated flip-flop output after ion strike to bulk (top) and SOI (bottom) devices.

To gain a quantitative sense of the expected improvement in SEU hardness, the start time of the injected transient current pulse was varied across one data period (1 ns) in 50 ps intervals, and the number of bits in error for each strike was recorded in Table 1. Such an exercise can pinpoint specific conditions under which the circuit is more vulnerable. The circuit built with bulk *npons* had at least one bit in error regardless of the strike time, and included more multiple-bit upsets than single-bit upsets. The circuit hardened with SOI devices was only vulnerable during a specific window that lasted 55% of the data period, and it never produced a multiple-bit upset thanks to its short duration. As one can readily see, the potential benefits for SEU improvements in moving from a bulk to SOI SiGe platform are quite clear.

TABLE 1  
BREAKDOWN OF SIMULATED BIT UPSETS

	Occurrences	
	SOI	Bulk
No bits upset	8	0
Single bit upset	12	9
Two bits upset	0	11

The new transient data for a complementary SiGe SOI platform establish a dramatic shortening of single-event transients caused by a heavy-ion strike. Because the SiGe on SOI devices lack the reverse-biased subcollector-substrate junction, far less charge is swept into the collector terminal of the device during an ion strike, improving its SEU response. Collector transients on the order of 150 ps were captured on both the npn and pnp devices, compared to 1 ns or longer for a bulk SiGe technology with similar

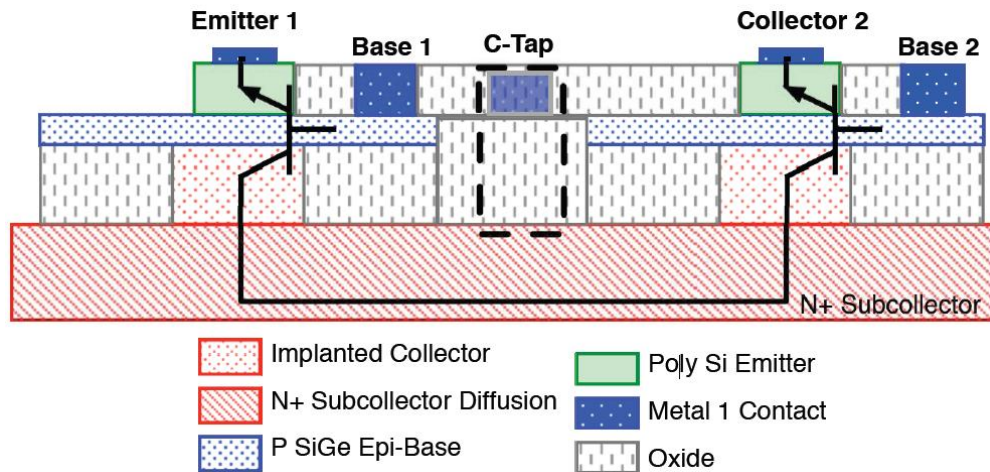
performance. Corresponding flip-flop simulations suggest a significant improvement in SEU rate should be possible using SOI, without any area or power penalty.

## CHAPTER 4

### DEVICE-LEVEL RADIATION HARDENING BY DESIGN

The field of Radiation Hardening By Design (RHBD) can be subdivided into device-level and circuit-level hardening. Separate from Radiation Hardening By Process, in which the actual semiconductor manufacturing processes are modified to reduce radiation sensitivity, device-level RHBD uses only minor modifications to an existing device without typically violating any major design rules. The modifications are ideally transparent to the fab, and should not incur any additional costs for fabrication. One example of device-level RHBD is the N-ring method presented in [11] which includes a highly-doped N<sup>+</sup> subcollector ring around the device. The additional p/n junction collects stray carriers created in the wake of an ion strike and prevents them from reaching the transistor, but has only limited benefit when the ion strike occurs directly through the emitter of the device. A new technique for device-level RHBD is the Inverse Mode Cascode topology, presented in [18, 19, 20].

This Inverse Mode Cascode device is a standard *npn* HBT with an extra base-emitter stackup present in the same shared subcollector. Electrically, this appears as a cascaded pair of *npns* where the bottom device is operated in forward mode and the top device is operated in inverse mode. The two electrical transistors share the same physical collector, as shown in Fig. 16 [19].



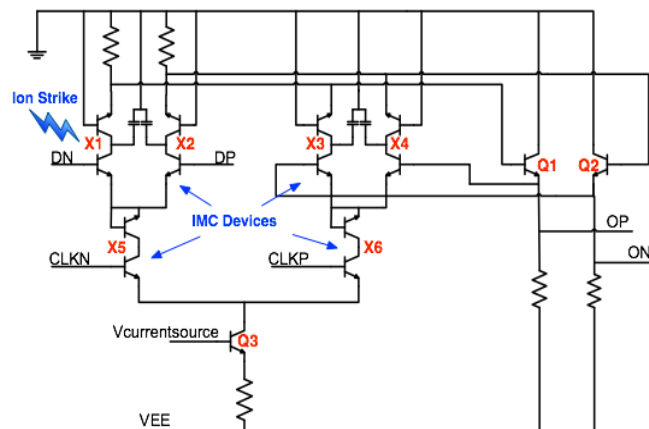
**Figure 16.** Cross-sectional diagram of the Inverse Mode Cascode transistor

A heavy-ion strike on a SiGe transistor deposits significant charge into the substrate and subcollector of the device. Because of the strongly reverse-biased subcollector-substrate junction, this charge is quickly swept to the collector terminal. The base and emitter, which are both limited to very thin active layers in the device, are far less sensitive than the collector. As such, circuits that couple the collector to the device output, such as CML logic circuits, are particularly susceptible to single event upsets. Modifying the device to decouple the collector from the circuit output would eliminate this risk [18]. The Inverse Mode Cascode transistor has an electrical collector that is really the physical emitter on the upper device. Therefore, the collector node of the IMC device is not particularly vulnerable to single event upset. The majority of the deposited charge from an ion strike is shunted away from the device by a connecting a capacitive element (such as a capacitor or reverse-biased diode) to the shared subcollector (C-TAP) [19].

Device-level characterization of this hardening technique has begun, with promising initial results. As described in [18], the total charge collected by the IMC

device's collector node is reduced to almost nil when the device is equipped with a subcollector contact to shunt charge away from the electrical collector. [18] also presents 3-D simulations to suggest that the transient duration for an ion strike on the IMC device is on the order of tens of picoseconds. Further testing of the device will establish its radiation-hardness in a circuit environment, such as those described in [19].

Applying the IMC device to a circuit is not entirely trivial, but can be done with minimal redesign and nearly no layout penalty. From a functional point of the view, the IMC operates as a cascade pair, and presents a collector, base, and emitter much like an ordinary transistor. The device only requires the addition of an upper-base bias line (which may be tied to the collector, creating a diode connected upper device). Correcting for the additional diode drop present in the cascade pair requires some minor redesign for most applications, including the flip-flop shown in Fig. 17. This circuit substitutes IMC devices for the sensitive data and clock transistors in a D-flip flop, and includes an additional pair of small level-shifting transistors to account for the extra VBE drop present between the IMC collector and base.



**Figure 17.** D-Flip Flop constructed with IMC transistors used for sensitive nodes.

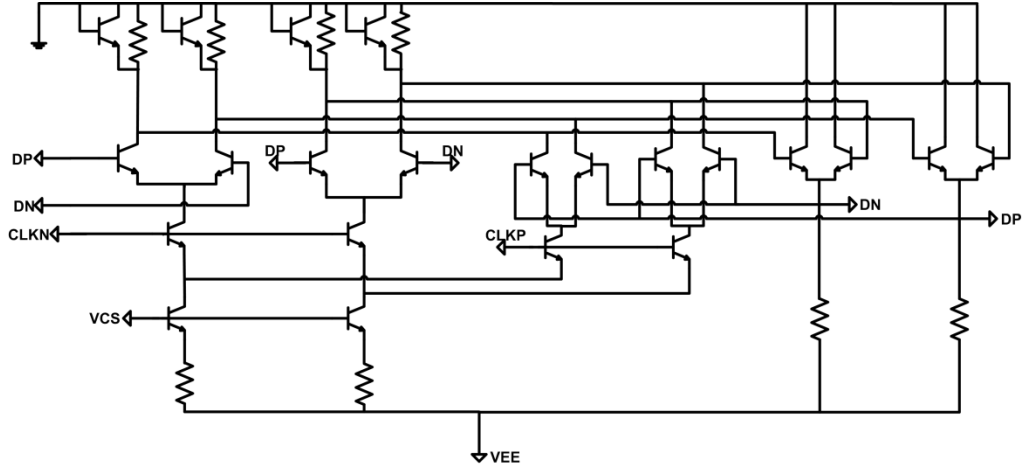
## CHAPTER 5

### CIRCUIT-LEVEL RADIATION HARDENING BY DESIGN

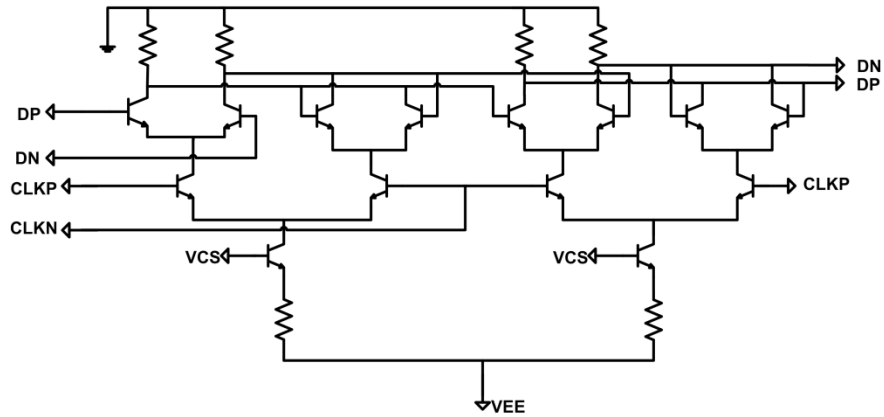
After analyzing the total dose response in Chapter 3 and measuring the device-level transient response in Chapter 3, the next step is naturally to apply that knowledge to an entire circuit. The study of device-hardening, while very complex and challenging in its own right, eventually must lead to hardened circuits, either by switching to a Radiation Hardened By Process solution (i.e. SOI) [21] or by adapting existing circuit topologies to be more robust to the ion strikes they inevitably encounter. While the former may be a simple change (but an expensive one), the latter is more complicated. Taking an off-the-shelf technology and building it to be Radiation Hardened By Design potentially offers a cheap and reliable alternative to expensive process changes. While the most obvious and often-used approach is Triple Modular Redundancy [22], which provides triplication of critical systems, this chapter presents a circuit design technique that provides substantial SEU-hardness for a digital shift register without requiring the transistor area or power consumption of full-blown TMR hardening. In addition, the effects of SEU-hardening just some parts of the larger register are explored as a method of circuit hardening with very limited area penalty. Results from a comprehensive heavy-ion broad-beam experiment at Texas A&M are presented to confirm the expectations and quantify the radiation hardness.

The Gated Feedback Cell (GFC), as described in [22, 23, 24], and shown as a schematic in Fig. 18, includes an OR-gated output on redundant pass and storage cells within a traditional master/slave flip-flop, such as that shown in Fig. 19. The gated

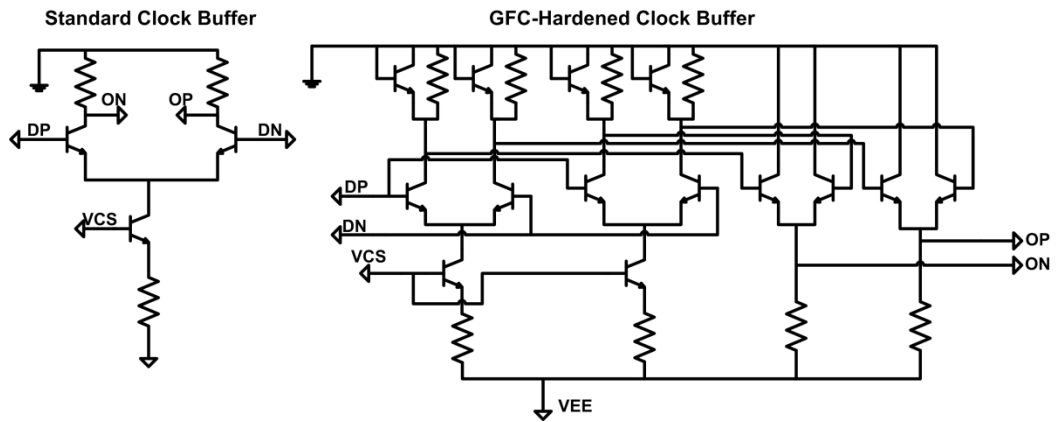
output, which is tied to the collector nodes of each pass and storage cell, serves to mitigate upsets caused when the collector node is struck by an ion and drops to a lower voltage [22]. Because the sensitive subcollector-substrate junction is reverse-biased, electrons generated from an ion strike are swept into the positively-biased collector, effectively lowering the node voltage until the circuit can recover. Because the transistor is most vulnerable when it is switched off, a state in which its collector voltage is highest in this circuit, an ion strike should present itself most often as a collector node switching from high to low. Since the redundant circuit elements are connected with an OR gate, a single transistor being struck and switched low should not affect the output of the circuit which will still be driven high by the unaffected (and still turned off) transistor. Unless both of the redundant circuits are simultaneously struck, the OR output should be unaffected. Additionally, a diode clamp is present on each of the load resistors to provide a lower-resistance path from collector to ground after an ion strike, allowing the collected charge to dissipate faster and reducing the total duration of the event [22]. Similarly, the GFC technique can be applied to a typical CML clock buffer, by adding a redundant differential-pair and OR-ing the two outputs, as shown in Fig. 20. Previous testing of the GFC architecture implemented in IBM's first-generation SiGe 5HP process has been shown to reduce a shift register's saturated cross-section to approximately 30% that of the unhardened shift register [24], and testing in IBM's 130 nm, third-generation 8HP SiGe process has shown similar results. An improvement in LET threshold from 0.01 to 2.2 by GFC-hardening has also been demonstrated in 8HP [22].



**Figure 18.** Schematic of a GFC-hardened D-flip flop (DFF) master cell.

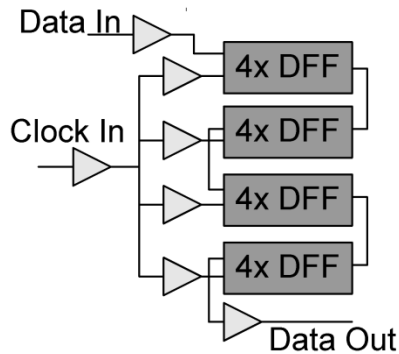


**Figure 19.** Schematic of a typical, unhardened D-flip flop



**Figure 20.** Schematic of an unhardened CML buffer (left) and a GFC-hard buffer (right).

As part of a large radiation hardening by design (RHBD) experiment, a number of 16-bit shift registers were fabricated using IBM's first-generation SiGe BiCMOS 5AM process (0.5  $\mu\text{m}$ , 47 GHz peak  $f_T$ ) [25]. Three high-speed circuits were present on each die, with common input pads and separate output pads. A current-source voltage line was used to toggle each circuit 'on' or 'off' for independent testing. As shown by the block diagram in Fig. 21, a high-speed differential data signal was fed through an input buffer to the first flip-flop stage. The differential clock signal was fed through a buffer stage that also provides appropriate level-shifting to an initial clock buffer which then feeds four intermediate clock buffers, which in turn each feed four flip-flops. The data output of the 16th flip-flop was fed through a buffer stage to the bond pads.

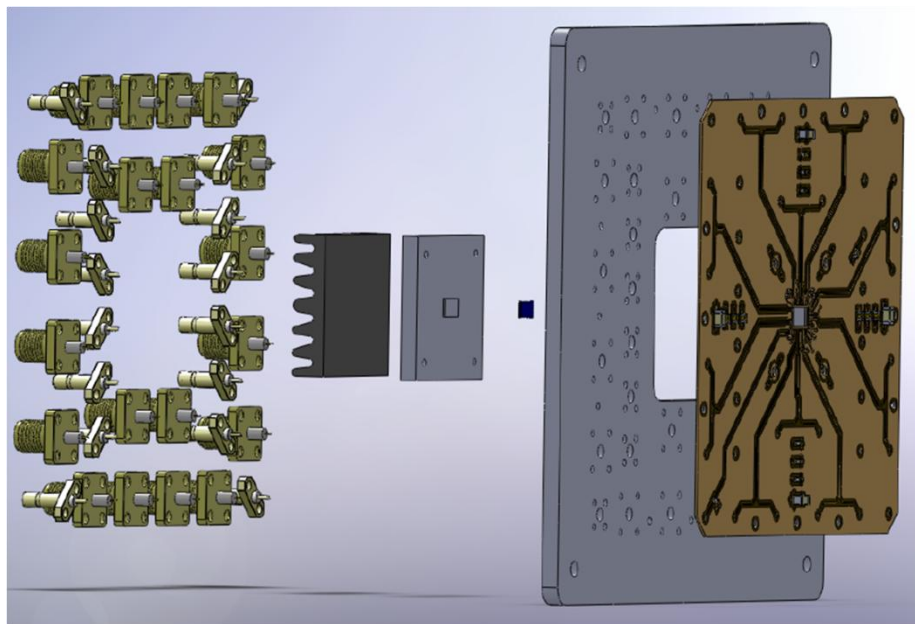


**Figure 21.** Block diagram of 16-bit shift register with clock distribution and data buffers.

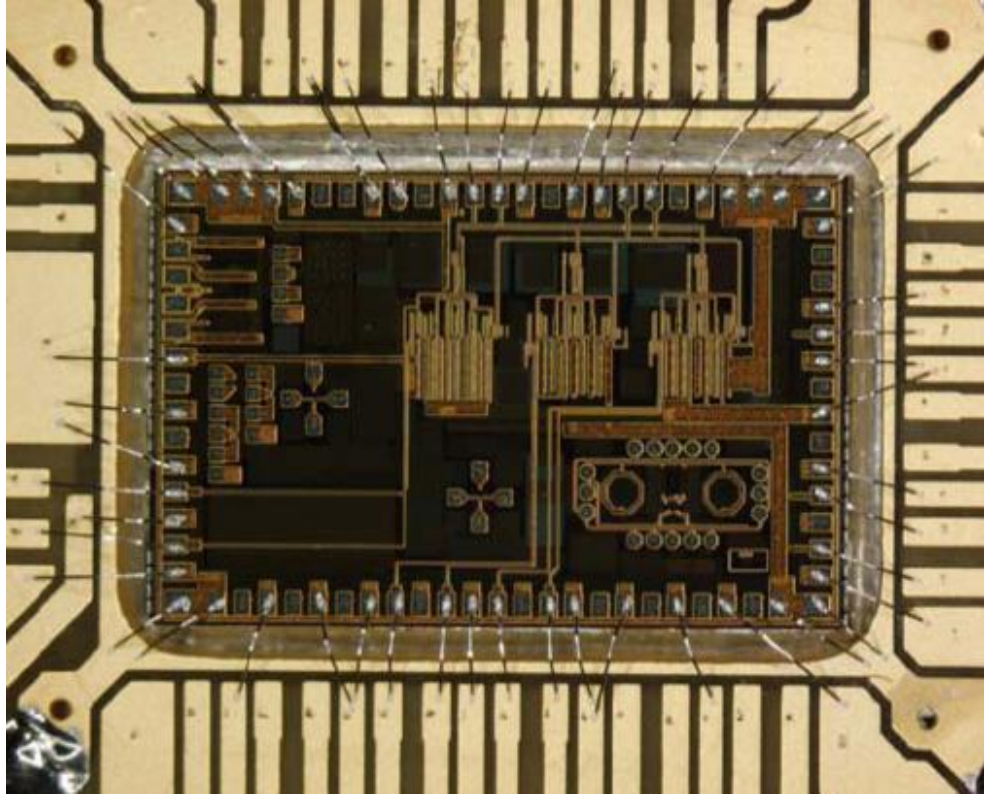
A set of unhardened and GFC-hardened independent clock buffer chains were also fabricated. They consist of 9 clock buffers attached in series, along with input/output level-shifters. The rail voltage for all circuits, with the exception of the unhardened clock buffers, is -5.2 V. The unhardened clock buffers required -3.0 V operation to match other circuitry under evaluation.

Broad-beam, heavy-ion testing was performed at the Texas A&M Cyclotron Institute. Effective LETs from 1.8 to 86.5 MeV/mg/cm<sup>2</sup> were achieved with Neon, Argon, Xenon, Krypton, and Gold ions. The fixture was rotated to 45 and 60 degree angles for some ion species to yield additional effective LET points, as calculated using the  $\cos(\theta)$  model [26].

Each die was attached and wire-bonded to a test fixture developed by the Mayo Foundation. The package provided DC bias pins through SSMB connectors, and high-speed data pins through SMA connectors. The test fixture is shown in Fig. 22, and the die with the unhardened register is shown in Fig. 23.



**Figure 22.** Exploded view of the high-speed test fixture used for radiation testing.



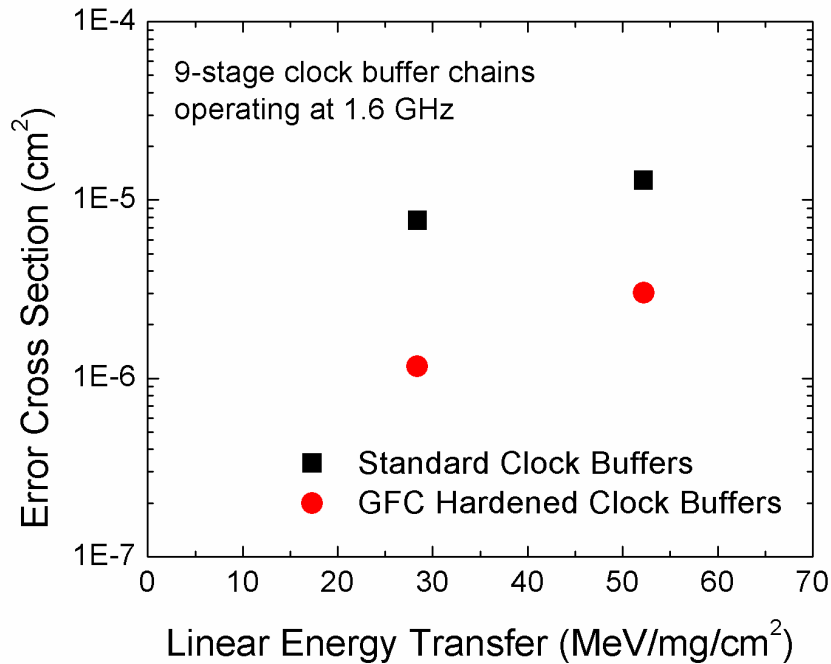
**Figure 23.** Photograph of the SiGe die (5mm x 3mm) bonded to the test fixture.

Clock and data signals were input to the circuit from an Anritsu MP1763B Pattern Generator, and the output was fed to an Anritsu MP1764B Bit Error Rate Tester (BERT). Each heavy-ion test was run to a fluence sufficient to create enough errors for statistical purposes (typically well over 100 bit errors at a fluence of  $1 \times 10^7$  ions/cm<sup>2</sup>). The number of bits in error, as recorded by the BERT was recorded after each experiment, along with the total fluence.

In addition to the broad-beam, heavy-ion experiment at Texas A&M, proton testing was performed with 63 MeV protons at the Crocker Nuclear Lab at UC Davis, as described in [3]. Identical shift registers were tested using the same BERT setup as described above, but the test setup for the clock buffers was different than at Texas

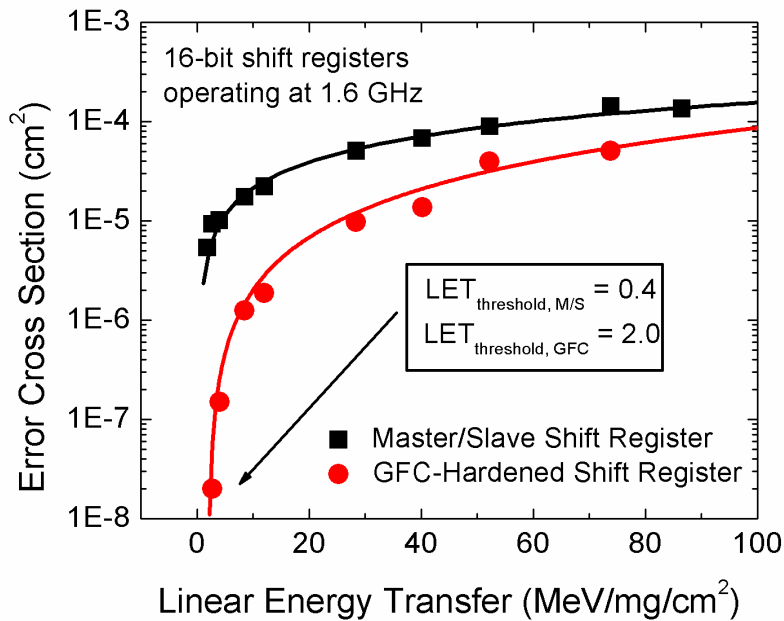
A&M. A high-speed scope was instead used to capture pulse widths of less than 300 ps or more than 480 ps on a 1400 MHz square wave. A control experiment showed that the scope method triggered on more events that did not upset the BERT, and hence is more sensitive. Each proton run was to a total fluence of  $5 \times 10^{12}$  protons/cm<sup>2</sup>, or a total dose of 674 krad(SiO<sub>2</sub>). Because of the extremely low LETs characteristics of high-energy protons, the test was not designed to generate a classical cross-section vs. LET curve, but instead to detect any unexpected proton sensitivities.

Fig. 24 shows the error event cross-section as a function of heavy-ion LET for the clock buffer chains. Limited data points are available for the clock buffers due to time constraints at Texas A&M, but exposures were completed with 15 MeV Krypton and Xenon. While a saturated cross-section and LET threshold cannot be clearly established, the data support a 76-85% reduction in cross-section for the GFC-hardened clock buffer.



**Figure 24.** Sensitive cross section vs. LET for independent clock buffer chains

The GFC-hardened flip-flop offers a similar reduction in error event cross-section under heavy-ion irradiation, as shown in Fig. 25. Both circuits are 16-bit shift registers operating at 1.6 GHz, and both utilize the GFC-hardened clock tree in an attempt to isolate the flip-flops as the sensitive elements. A truly saturated cross-section is not apparent from these data, but at a high LET of 73.8, the GFC shift register reduces the sensitive cross-section by 65%. At lower LET values more realistically encountered in space [26], in this case 28.4 MeV/mg/cm<sup>2</sup>, the GFC-hardened register has an 81% smaller sensitive cross-section.



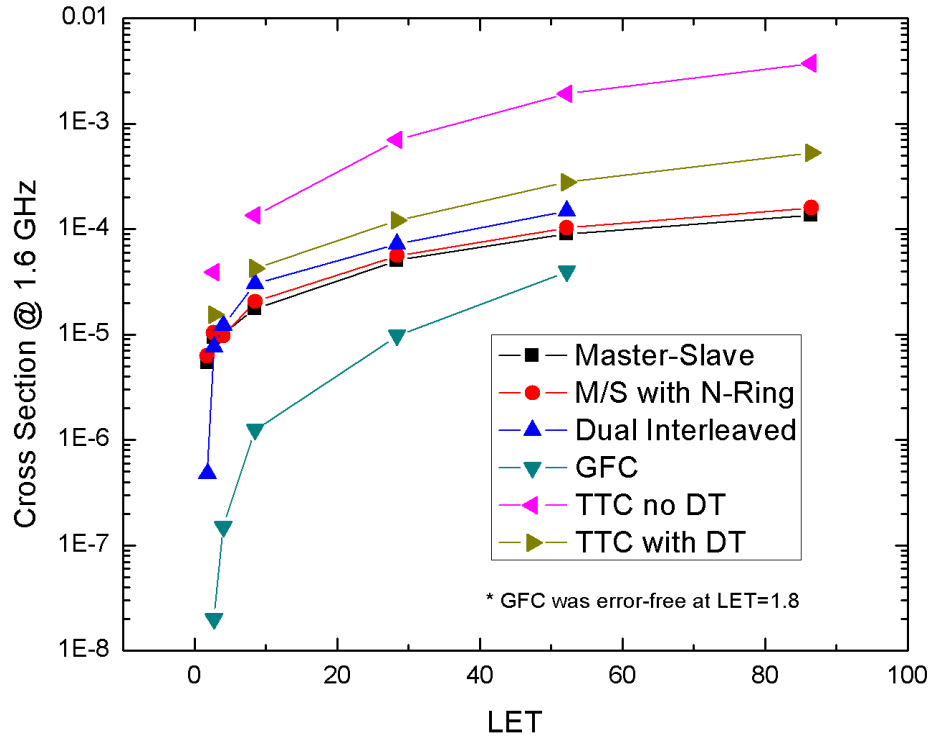
**Figure 25.** Sensitive cross section vs. LET for a full 16-bit shift registers.

Effectiveness of the GFC hardening increases more dramatically at the lowest LETs, reducing cross-section by 98.5% at an LET of 4, and by 99.7% at LET of 2.7. The

GFC-hardened shift register ran error-free at an LET of 1.8, even when the run was extended to a higher-than-usual total fluence of  $1 \times 10^8$  ions/cm<sup>2</sup>.

An estimated error-free LET threshold was obtained from the Weibull curve fit to the data, as described in [26]. For the unhardened M/S shift register, which did not operate error-free at any LET tested, the threshold is estimated to be 0.4 MeV/mg/cm<sup>2</sup>. The threshold LET for the GFC-hardened register is 2.0 MeV/mg/cm<sup>2</sup>, which closely matches the 8HP GFC result reported in [22].

In addition to the GFC circuits primarily studied in this experiment, a variety of other RHBD techniques were explored using the same shift register topology. These include a triple-tail cell, in which the clock is decoupled from the data path, and the N-ring, in which a dummy N<sup>+</sup> subcollector ring is placed outside the DT-isolation to provide an alternative recombination path for charges generated in the substrate. The results for these circuits, as well as the GFC, are plotted together in Figure 26.



**Figure 26.** Heavy-ion test results on numerous SEU-hardening experiments. The Master-Slave device represents a baseline comparison as an unhardened circuit.

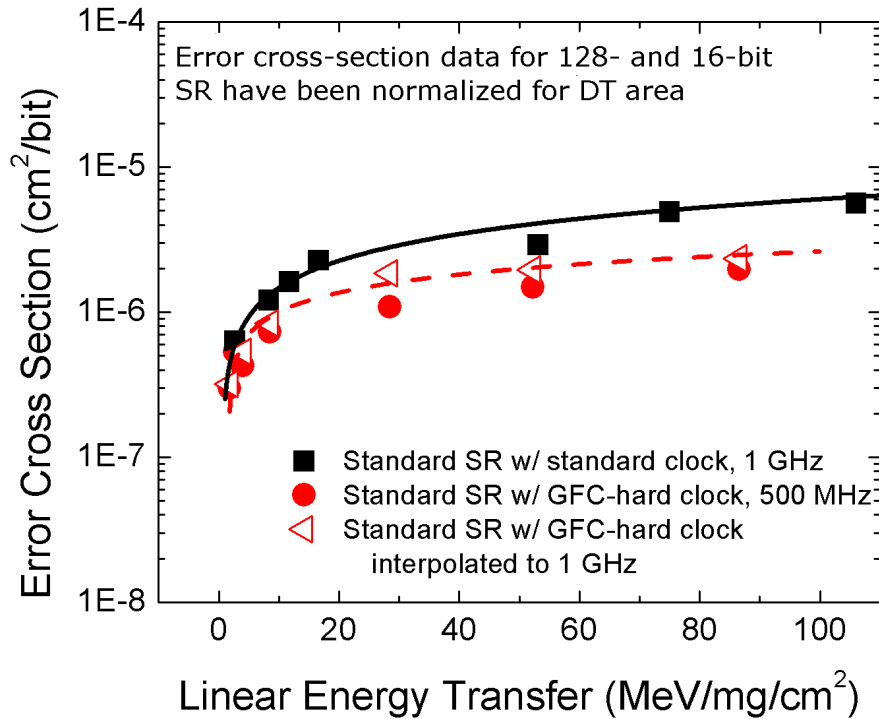
The "TTC" circuit (triple-tail cell) was an experimental attempt to decouple the clock path from the data patch, and resulted in substantial weakening of the SEU-response. A version was also taped-out with the DT-isolation removed, which left the devices with no lateral isolation at all. As one would naively assume, the lack of isolation dramatically increased the number of bit upsets.

The N-ring hardening technique has shown significant reduction in charge collection during device-level microbeam testing, particularly for outside-DT ion strikes [11]. However, in the 5AM circuits tested no such improvement was seen. In fact, although the circuits were identical in every way except for the additional N-ring, those hardened circuits were slightly softer at every LET point measured.

Another shift register, designed using the dual-interleaved technique described in [22] also failed to improve sensitive cross-section for the 5AM circuitry. Indeed, only the gated-feedback technique (GFC) offered any substantial improvements over the unhardened circuit in this experiment.

Given the effectiveness of GFC-hardening on the standalone clock tree, a post-experiment attempt was made to compare the unhardened master/slave shift register with the GFC clocks (the register used in this experiment) to a completely unhardened master/slave from a previous experiment. Ideally, this would allow extraction of the clock tree's radiation hardness from that of the overall circuit. Raw data for a completely unhardened register was available from the 2005 CREST program, and a nearly-identical (but 128-bit long) 5AM master/slave shift register was selected [12]. The unhardened CREST register was normalized for total deep trench area to very closely match the 16-bit configuration of the master/slave from the current experiment. The D-flip flop tail currents and rail voltages were identical.

Data is presented in Fig. 27 as the error event cross-section per bit as a function of LET. The two solid shapes show experimental data, while a dashed line with open shapes represents a linear-interpolation of 1.6 GHz and 500 MHz data to demonstrate the expected performance at 1 GHz. Even after interpolation adjusts the error-rate upwards to approximate 1 GHz operation, the unhardened master/slave register with a hardened clock shows a higher zero-error threshold LET (1.7 vs 0.5) and a reduced high-LET sensitive cross-section (54% smaller at LET of 86.5), indicating that a certain amount of circuit hardening is possible by changing just the sensitive clock distribution network.



**Figure 27.** Effects of radiation-hardening only the clock tree in a larger digital circuit.

To verify functionality and SEU-hardness in a proton environment, an additional experiment was performed at the UC Davis Crocker Nuclear Lab. The results of 63-MeV proton irradiation are summarized in Table II. The total proton fluence was  $5 \times 10^{12}$  protons/cm<sup>2</sup>. The GFC-hardened shift register and clock buffer circuits both show that error cross-section is reduced by an order of magnitude compared to their unhardened versions. Proton error event cross sections are significantly lower than those for the higher-LET heavy ion particles utilized at Texas A&M as expected.

TABLE II  
PROTON SENSITIVITY RESULTS

Circuit	Error Cross-Section	Event	Notes
M/S SR w/ hard tree	clock	$1.40 \times 10^{-11} \text{ cm}^2$	1.4 GHz, BERT
GFC SR w/ hard tree	clock	$1.40 \times 10^{-12} \text{ cm}^2$	1.4 GHz, BERT
Standard clock chain	buffer	$3.76 \times 10^{-12} \text{ cm}^2$	1.4 GHz, Scope
GFC clock buffer chain		$4.00 \times 10^{-13} \text{ cm}^2$	1.4 GHz, Scope

Proton results verify hardness of GFC DFFs and buffers. The shift registers were tested using a BERT to detect bit error events, and the clock buffers were tested with an oscilloscope triggering on large pulse-width variations.

The Gated Feedback Cell technique offers significant SEU mitigation, especially at low LET values. A shift register built with GFC flip flops can reduce the sensitive cross-section of the circuit by an order of magnitude or more at LET's below 10, with a penalty of 2.6x in transistor count and 2.7x in current draw compared with a standard master/slave register. The area and power tradeoffs are summarized in Table III.

TABLE III  
CIRCUIT TRADE-OFFS

Circuit	Transistor Count	Current Draw
M/S SR w/ std clock tree	239*	45 mA*
M/S SR w/ hard clock tree	294	60 mA
GFC SR w/ hard clock tree	646	162 mA
TMR SR w/ hard clock tree (with M/S DFFs, vote at end)	910*	190 mA*
Standard clock buffer chain	27	9 mA
GFC clock buffer chain	126	36 mA

Data excludes input and output buffers which would appear in both circuit topologies.  
All SR are 16 bits.

Typical RHBD techniques focus on hardening the flip-flops and other sequential logic elements, but the effect on clock buffer circuitry cannot be ignored. A simple hardening of the clock tree yields an additional reduction in cross-section, with greater improvement shown at higher LET values, which also indicates that the clock buffers are less sensitive at low-LET than the flip-flops. Adding the GFC clock buffers to an ordinary M/S shift register requires only a 23% transistor area increase while reducing upset cross-section by up to 85%, indicating a potentially disproportional sensitivity of the overall circuit to clock upsets, at least for higher LET values. Combining both GFC-hardened circuits does, however, clearly offer area and power savings compared to conventional Triple Modular Redundancy for circuits that can still tolerate a certain level of single event upsets.

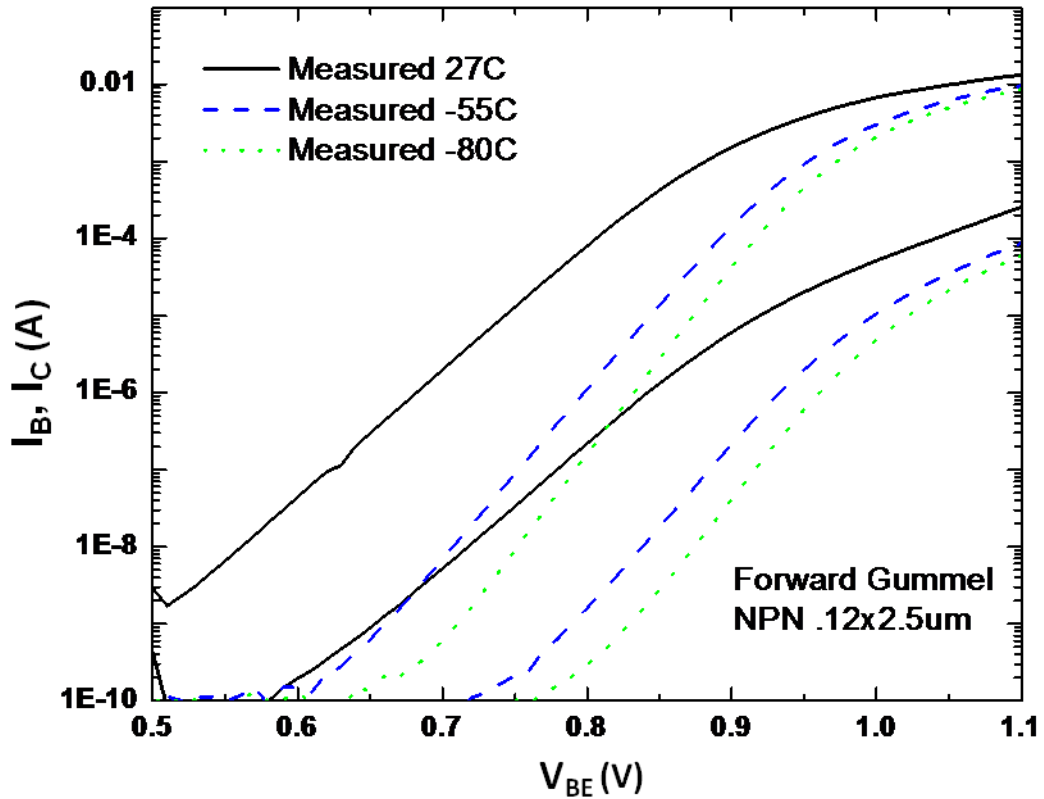
## CHAPTER 6

### CRYOGENIC OPERATION OF SIGE DEVICES AND CIRCUITS

A critical obstacle facing system designers for space missions is the extreme variation in temperature present in orbital and lunar missions. Without an atmosphere to moderate temperatures throughout the day and night, the surface of moon can vary in temperature from a bitterly cold  $-180^{\circ}\text{C}$  at night to a blazing  $120^{\circ}\text{C}$  during the day. In the shadowed polar craters, nighttime temperatures plunge as low as  $-230^{\circ}\text{C}$  (a mere 43 K!) [10]. Conventional electronics packages require power-hungry heating elements for the 14-day lunar night and large radiative coolers for the equally long daytime bake. An off-the-shelf silicon platform that could perform well across the entire range would save designers the power and weight required to maintain a narrow temperature range while also simplifying the mission and increasing reliability. Such a platform exists with silicon-germanium BiCMOS. Fourth-generation SiGe transistors with a room-temperature  $f_T$  of 300 GHz have been shown to operate as fast as 500 GHz when cryogenically chilled to 4K with liquid helium [27]. SiGe devices also function above  $200^{\circ}\text{C}$ , providing a comfortably large margin around even the extreme temperature ranges of lunar operation [28].

Despite their published extreme temperature operation, commercial design kits are typically not modeled beyond commercial or military spec ranges. To design a commercial application operating below  $-55^{\circ}\text{C}$ , it is necessary to carefully evaluate device performance and model-to-measurement accuracy. Such an exercise was completed with IBM's third-generation 8HP BiCMOS platform, and both AC and DC

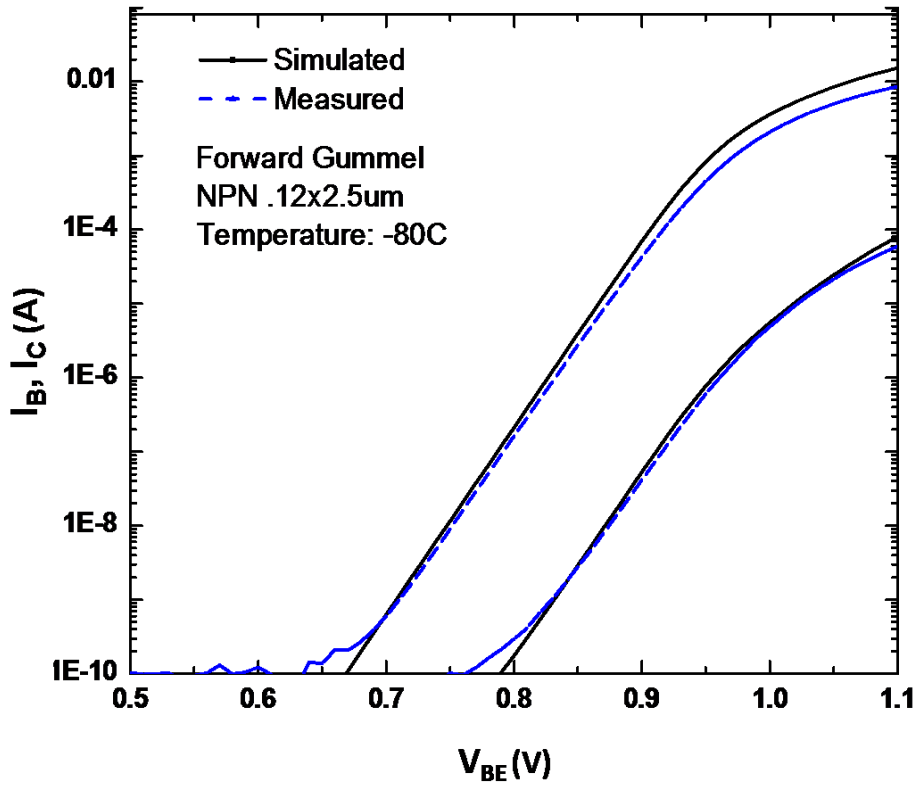
measurements were checked against simulation down to  $-100^{\circ}\text{C}$ . DC measurements were completed using a closed-cycle cryostat pumped down to a vacuum and cooled with a mechanical chiller. An Agilent switching matrix and Agilent 4155 parameter analyzer were controlled with a MATLAB script that automated the measurement process. A slew of DC performance metrics, including forward and inverse gummels and output characteristics, were measured for various device geometries over multiple 8HP wafers. Fig. 28 shows the forward gummel characteristics of a third-generation bulk HBT over temperature.



**Figure 28.** Forward gummel characteristics of a third-generation HBT down to  $-80^{\circ}\text{C}$ .

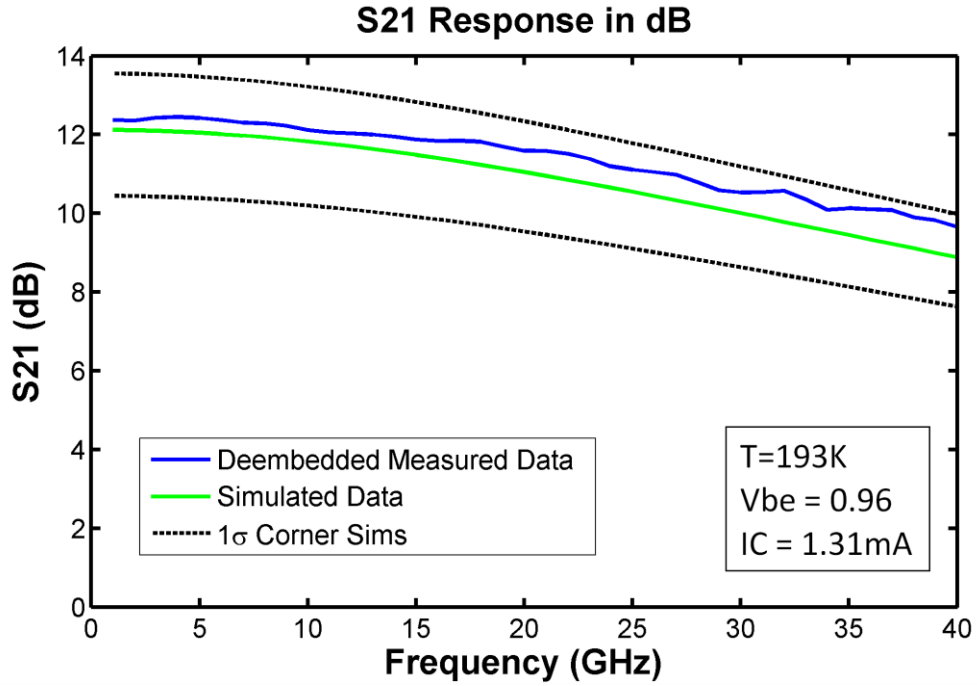
Cooling the transistor to  $-80^{\circ}\text{C}$  improves current gain ( $\beta$ ) for a given  $I_C$  and increases the  $V_{BE}$  required for a specific bias current. To verify model-to-measurement

fidelity, the  $-80^{\circ}\text{C}$  data was superimposed with simulation data from the standard design kit models, as shown in Fig. 29.

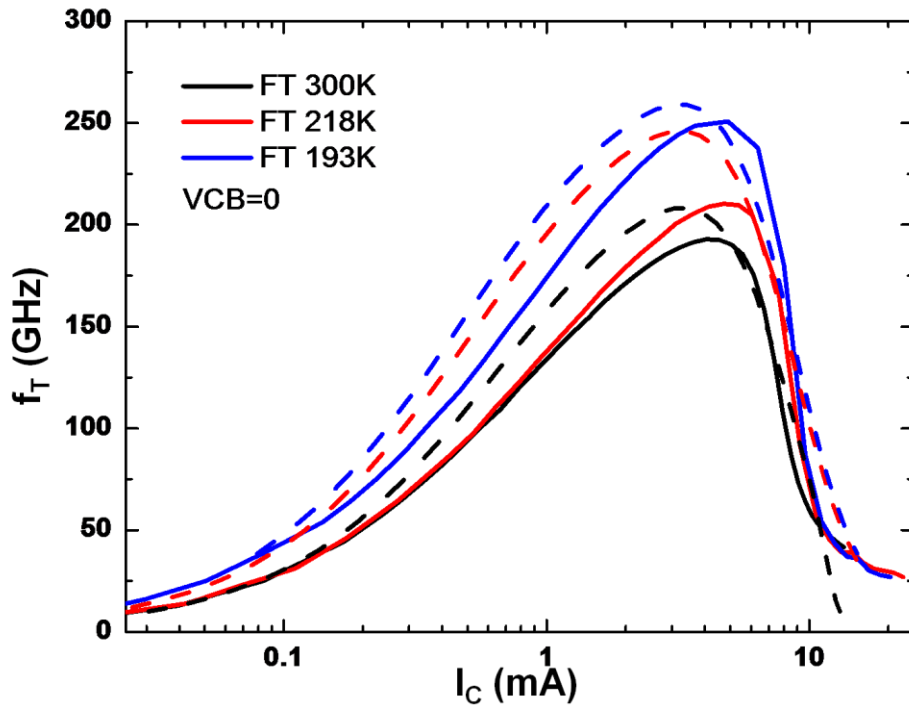


**Figure 29.** Model-to-measurement comparison at  $-80^{\circ}\text{C}$  for third-generation HBT.

AC performance at cryogenic temperatures was measured using a custom Lakeshore 40-GHz cryogenic probing station. The open cycle station was chilled using liquid nitrogen, and a heating element used to maintain a stable temperature. The standard 40-GHz GSG probes mounted in the probing station were connected with RF cables to an Agilent network analyzer for s-parameter measurements. Data was taken down to  $193\text{ K}$  ( $-80^{\circ}\text{C}$ ) and de-embedded for parasitics. The  $S_{21}$  is presented in Fig. 30 at  $-80^{\circ}\text{C}$ . The unity gain cutoff frequency for the device is presented in Fig. 31.



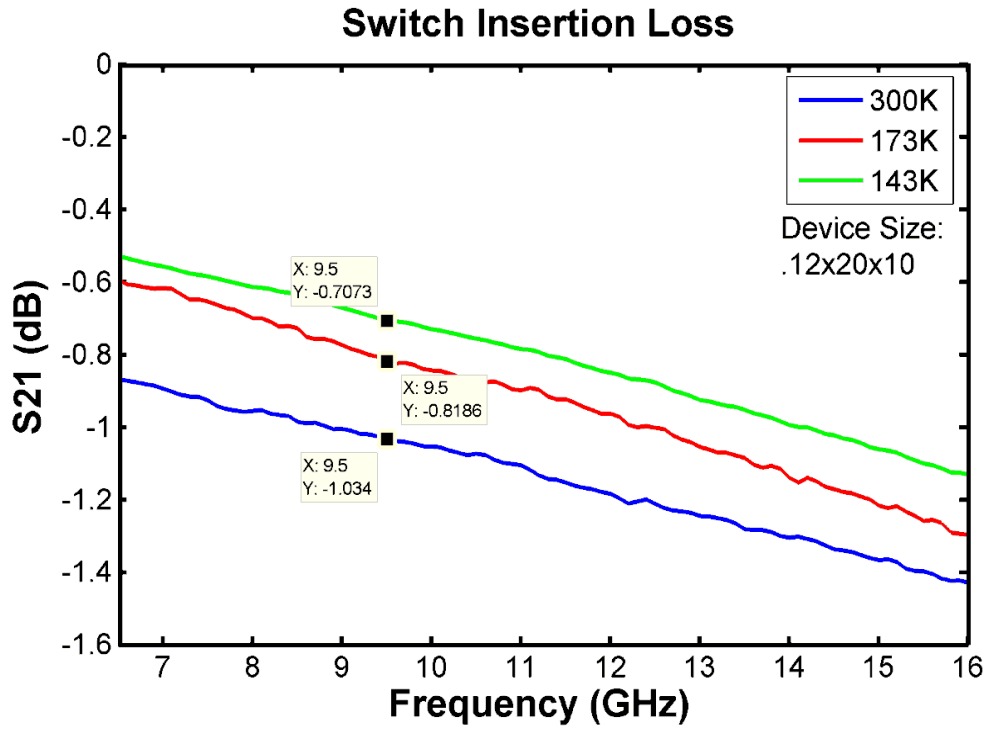
**Figure 30.** S21 for a .12x3.0 HBT at -80°C vs. simulation and corner sims.



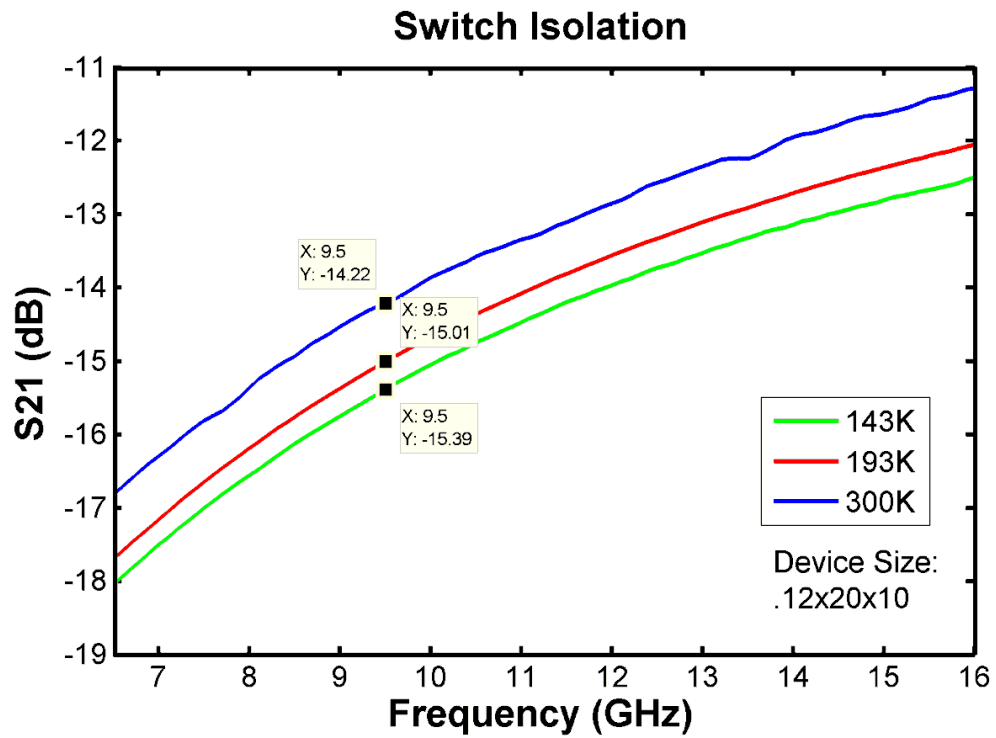
**Figure 31.** Unity gain cutoff frequency ( $f_T$ ) over temperature, compared to simulation (dotted lines).

The S21 of the device is improved at cryogenic temperatures, and fits within 1-sigma corner simulations, indicating a strong measurement-to-model correlation even at -80°C. The speed of the device is also improved at lower temperature as shown in Fig. 31 above, and is in relatively good agreement with modeled data. While an offset exists between model and measurement, it remains constant from room temperature down to -80°C as performance improves.

In addition to HBT performance, a series of nFET switch structures were measured at cryogenic temperatures to understand the impact of cooling on the FET-based switches, which are poorly modeled in pass-gate configuration at any temperature. The single-pole, single-throw (SPST) switches were operated with 1.2 V applied to drain and source, with the gate switched on and off with 1.2 V and 2.4 V applied. Calibrated s-parameter measurements revealed improved insertion loss, shown in Fig. 32, and improved isolation, shown in Fig. 33.



**Figure 32.** Insertion loss for SPST switch during cryogenic operation.



**Figure 33.** Isolation measurements for SPST switch during cryogenic operation.

The insertion loss measurements shown in Fig. 32 are particularly appealing to space-based RF systems that rely on RF-CMOS switches. Significantly improved isolation offers the possibility of adding additional CMOS switches in series to improve isolation, or the reduction in amplifier gain to improve other metrics. With the integration of highly-scaled CMOS with high-speed SiGe HBTs, space-based RF systems can be integrated onto a single chip containing the RF front-end and CMOS controls that operates comfortably in the harsh temperatures of outer space.

## CHAPTER 7

### CONCLUSIONS AND FUTURE WORK

With its compelling high-speed mixed-signal and RF-design performance, and its built-in TID hardness and cryogenic suitability, SiGe BiCMOS technology is a perfect candidate for low-cost, commercial-off-the-shelf (COTS) extreme environment applications such as satellites and lunar probes.

Due to the thin, epitaxial doping profile and raised-extrinsic nature of its base, the SiGe HBT is TID-hard as-built to several Mrad, far more than most missions are expected to encounter. On-going research into single-event effects in SiGe has revealed not only the mechanisms of single event upsets, but also the shape and duration of the ultra-high speed transients expected from such a heavy-ion strike. Efforts to counter single-event effects in SiGe through both device- and circuit-level radiation hardening by design show promising results for a future SEU-hard SiGe platform.

Finally, the thorough characterization of SiGe performance at cryogenic temperatures has led to a better understanding of analog and RF performance in commercially available platforms at below-published-spec temperatures. Such knowledge will be used to design the next generation of high-speed RF communications and radar systems to be used in extreme environment applications.

Moving ahead, there is significant future work to be done in this field. Early investigation of the Inverse Mode Cascode device looks promising at a device level, and circuit-implementations must be characterized in a heavy-ion broadbeam. With the increasing power of 3-D TCAD simulation tools run in a mixed-mode environment, the

possibility exists to use mass computer power to solve the problem of single-event upsets. Using simulations tools first to analyze the dynamics of an ion strike, and then to design devices and circuits around such knowledge, may lead to a reduction in the amount of charge (or transient magnitude) experienced during an ion strike. Finally, there are unexplored problems with the combination of low-temperature and radiation. Beam experiments with cryogenic testing are not easy when the device is passively exposed, but running an active digital circuit at cryo while exposed to a heavy-ion broadbeam could yield some interesting new results.

Indeed, the future of the SiGe platform looks bright. Further research at many universities and research labs may lead to an eventual terahertz transistor with an operating temperature range of several hundred degrees C and the ability to function in the harsh radiation environments encountered not just in outer space, but in nuclear power and medical facilities right here on Earth.

## REFERENCES

- [1] Cressler, J.D., "On the Potential of SiGe HBTs for Extreme Environment Electronics," *Proceedings of the IEEE*, vol.93, no.9, pp.1559-1582, Sept. 2005.
- [2] B. Banerjee, S. Venkataraman, Y. Lu, S. Nuttinck, D. Heo, E. Chen, J. D. Cressler, J. Laskar, G. Freeman, and D. Ahlgren, "Cryogenic performance of a 200 GHz SiGe HBT technology," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2003, pp. 171–174.
- [3] Sutton, A.K., Haugerud, B.M., Prakash, A.P.G., Bongim Jun, Cressler, J.D., Marshall, C.J., Marshall, P.W., Ladbury, R., Guarin, F., Joseph, A.J., "A comparison of gamma and proton radiation effects in 200 GHz SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol.52, no.6, pp. 2358- 2365, Dec. 2005.
- [4] Babcock, J.A., Cressler, J.D., Vempati, L.S., Clark, S.D., Jaeger, R.C., Hameed, D.L., "Ionizing radiation tolerance and low-frequency noise degradation in UHV/CVD SiGe HBT's," *IEEE Electron Device Letters*, vol.16, no.8, pp.351-353, Aug 1995.
- [5] Cressler, J.D., Krithivasan, R., Gang Zhang, Guofu Niu, Marshall, P.W., Kim, H.S., Reed, R.A., Palmer, M.J., Joseph, A.J., "An investigation of the origins of the variable proton tolerance in multiple SiGe HBT BiCMOS technology generations," *IEEE Transactions on Nuclear Science*, vol.49, no.6, pp. 3203- 3207, Dec 2002.
- [6] Najafizadeh, L., Phillips, S.D., Moen, K.A., Diestelhorst, R.M., Bellini, M., Saha, P.K., Cressler, J.D., Vizkelethy, G., Turowski, M., Raman, A., Marshall, P.W., "Single Event Transient Response of SiGe Voltage References and Its Impact on the Performance of Analog and Mixed-Signal Circuits," *IEEE Transactions on Nuclear Science*, vol.56, no.6, pp.3469-3476, Dec. 2009.
- [7] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*, Boston, MA: Artech House, 2003.
- [8] Krithivasan, R., Niu, G., Cressler, J.D., Currie, S.M., Fritz, K.E., Reed, R.A., Marshall, P.W., Riggs, P.A., Randall, B.A., Gilbert, B., "An SEU hardening approach for high-speed SiGe HBT digital logic," *IEEE Transactions on Nuclear Science*, vol.50, no.6, pp. 2126- 2134, Dec. 2003.
- [9] K.M. Murray *et al.*, *Nucl. Instrum. Meth. Phys. Res. A*, vol. 281, pp. 616–621, Sep. 1989.

- [10] Cressler, J.D., "SiGe BiCMOS Technology: An IC Design Platform for Extreme Environment Electronics Applications," *Proceedings of the IEEE Reliability Physics Symposium, 2007*, pp.141-149, 15-19 April 2007.
- [11] Sutton, A.K., Bellini, M., Cressler, J.D., Pellish, J.A., Reed, R.A., Marshall, P.W., Guofu Niu, Vizkelethy, G., Turowski, M., Raman, A., "An Evaluation of Transistor-Layout RHBD Techniques for SEE Mitigation in SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol.54, no.6, pp.2044-2052, Dec. 2007.
- [12] Marshall, P., Carts, M., Currie, S., Reed, R., Randall, B., Fritz, K., Kennedy, K., Berg, M., Krithivasan, R., Siedleck, C., Ladbury, R., Marshall, C., Cressler, J.D., Guofu Niu, LaBel, K., Gilbert, B., "Autonomous bit error rate testing at multi-gbit/s rates implemented in a 5AM SiGe circuit for radiation effects self test (CREST)," *IEEE Transactions on Nuclear Science*, vol.52, no.6, pp. 2446- 2454, Dec. 2005.
- [13] Varadharajaperumal, M.; Niu, G.; Krithivasan, R.; Cressler, J.D.; Reed, R.A.; Marshall, P.W.; Vizkelethy, G.; Dodd, P.E.; Joseph, A.J.; , "3-D simulation of heavy-ion induced charge collection in SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol.50, no.6, pp. 2191- 2198, Dec. 2003.
- [14] Varadharajaperumal, M.; Guofu Niu; Cressler, J.D.; Reed, R.A.; Marshall, P.W.; , "Three-dimensional Simulation of heavy-ion induced charge collection in SiGe HBTs on SOI," *IEEE Transactions on Nuclear Science*, vol.51, no.6, pp. 3298- 3303, Dec. 2004.
- [15] Bellini, M., Phillips, S.D., Diestelhorst, R.M., Cheng, P., Cressler, J.D., Marshall, P.W., Turowski, M., Avenier, G., Chantre, A., Chevalier, P., , "Novel Total Dose and Heavy-Ion Charge Collection Phenomena in a New SiGe HBT on >Thin-Film SOI Technology," *IEEE Transactions on Nuclear Science*, vol.55, no.6, pp.3197-3201, Dec. 2008.
- [16] Najafizadeh, L., Phillips, S.D., Moen, K.A., Diestelhorst, R.M., Bellini, M., Saha, P.K., Cressler, J.D., Vizkelethy, G., Turowski, M., Raman, A., Marshall, P.W., , "Single Event Transient Response of SiGe Voltage References and Its Impact on the Performance of Analog and Mixed-Signal Circuits," *IEEE Transactions on Nuclear Science*, vol.56, no.6, pp.3469-3476, Dec. 2009.
- [17] Pellish, J.A., Reed, R.A., McMorrow, D., Vizkelethy, G., Cavrois, V.F., Baggio, J., Paillet, P., Duhamel, O., Moen, K.A., Phillips, S.D., Diestelhorst, R.M., Cressler, J.D., Sutton, A.K., Raman, A., Turowski, M., Dodd, P.E., Alles, M.L., Schrimpf, R.D., Marshall, P.W., LaBel, K.A., , "Heavy Ion Microbeam- and Broadbeam-Induced Transients in SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol.56, no.6, pp.3078-3084, Dec. 2009.

- [18] Phillips, S.D., Thrivikraman, T., Appaswamy, A., Sutton, A.K., Cressler, J.D., Vizkelethy, G., Dodd, P., Reed, R.A., , "A Novel Device Architecture for SEU Mitigation: The Inverse-Mode Cascode SiGe HBT," *IEEE Transactions on Nuclear Science*, vol.56, no.6, pp.3393-3401, Dec. 2009.
- [19] Thrivikraman, T.K., Appaswamy, A., Phillips, S.D., Sutton, A.K., Wilcox, E.P., Cressler, J.D., , "A novel device structure using a shared-subcollector, cascoded inverse-mode SiGe HBT for enhanced radiation tolerance," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting, 2009*, pp.79-82, 12-14 Oct. 2009.
- [20]T. K. Thrivikraman *et al.*, "Inverse mode SiGe HBT cascode device and fabrication method," U.S. Patent app. no. 61/035,903, March 11 2009.
- [21]Schwank, J.R., Ferlet-Cavrois, V., Shaneyfelt, M.R., Paillet, P., Dodd, P.E., , "Radiation effects in SOI technologies," *IEEE Transactions on Nuclear Science*, vol.50, no.3, pp. 522- 538, June 2003.
- [22]Krithivasan, R., Marshall, P. W., Nayeem, M., Sutton, A. K., Kuo, W.-M., Haugerud, B. M., Najafizadeh, L., Cressler, J. D., Carts, M. A., Marshall, C. J., Hansen, D. L., Jobe, K.-C. M., McKay, A. L., Niu, G., Reed, R., Randall, B. A., Burfield, C/A., Lindberg, M. D., Gilbert, B. K., Daniel, E. S., , "Application of RHBD Techniques to SEU Hardening of Third-Generation SiGe HBT Logic Circuits," *IEEE Transactions on Nuclear Science*, vol.53, no.6, pp.3400-3407, Dec. 2006.
- [23]S. E. Kerns and B. D. Shafer, "The design of radiation-hardened ICs for space: A compendium of approaches," *Proc. IEEE*, vol. 76, pp. 1470–1509, Nov. 1988.
- [24]D. L. Hansen, P. Chu, K. Jobe, A. L. McKay, and H. P. Warren, "SEU cross sections of hardened and unhardened SiGe circuits," *IEEE Transactions on Nuclear Science*., vol. 53, no. 6, pp. 3579–3586, Dec. 2006.
- [25]D. C. Ahlgren *et al.*, "Manufacturability demonstration of an integrated SiGe HBT technology for the analog and wireless marketplace," in *IEDM Tech. Dig.*, 1996, pp. 859–862.
- [26]E. Petersen, J. Pickel, J. Adams Jr., and E. Smith, "Rate prediction for single event effects—A critique," *IEEE Transactions on Nuclear Science*, vol. 39, no. 1, pp. 1577–1599, Feb. 1992.
- [27] Krithivasan, R., Yuan Lu, Cressler, J.D., Jae-Sung Rieh, Khater, M.H., Ahlgren, D., Freeman, G., , "Half-terahertz operation of SiGe HBTs," *IEEE Electron Device Letters*, vol.27, no.7, pp. 567- 569, July 2006.
- [28]J.D. Cressler, Editor, *The Silicon-Heterostructure Handbook*, CRC Press, Boca Raton, FL, 2006.

- [29] Sutton, A.K., Haugerud, B.M., Yuan Lu, Wei-Min Lance Kuo, Cressler, J.D., Marshall, P.W., Reed, R.A., Jae-Sung Rieh, Freeman, G., Ahlgren, D., , "Proton tolerance of fourth-generation 350 GHz UHV/CVD SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol.51, no.6, pp. 3736- 3742, Dec. 2004
- [30] Stassinopoulos, E.G., Raymond, J.P., "The space radiation environment for electronics," *Proceedings of the IEEE* , vol.76, no.11, pp.1423-1442, Nov 1988
- [31] Wilcox, E., Phillips, S., Madan, A., Cressler, J.D., Vizkelethy, G., Marshall, P.W., Babcock, J.A., Kruckmeyer, K., Eddy, R., Cestra, G., Zhang, B., "Single Event Transient Hardness of a New Complementary (npn + pnp) SiGe HBT Technology on Thick-film SOI," Submitted to *NSREC 2010*.
- [32] Wilcox, E., Phillips, S., Cressler, J.D., Marshall, P.W., Carts, M.A., Pellish, J.A., Richmond, L., Mathes, W., Randall, B., Post, D., Gilbert, B., Daniel, E., "Non-TMR SEU-Hardening Techniques for SiGe HBT Shift Registers and Clock Buffers," In publication, *IEEE Transactions on Nuclear Science*, 2010.