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(54) **METHOD TO MODIFY THE CONDUCTIVITY OF GRAPHENE**

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(52) **U.S. Cl.**
USPC **257/40**; 257/24; 257/E51.038; 977/788; 977/936

(58) **Field of Classification Search**
USPC 257/24, 40
See application file for complete search history.

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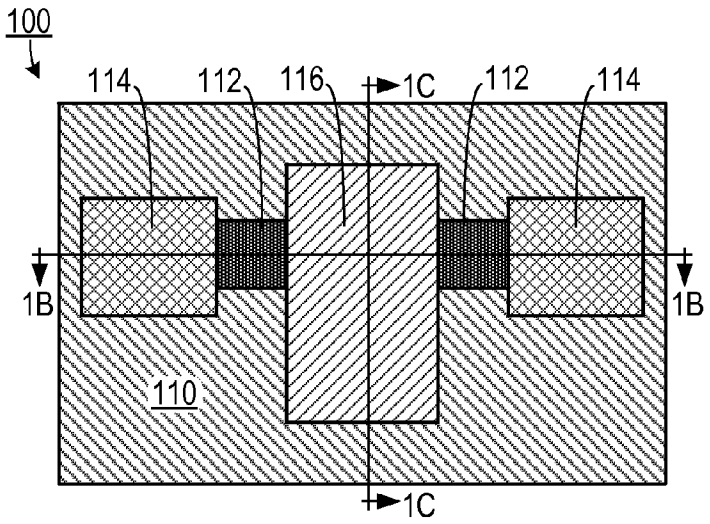
(57) **ABSTRACT**

A gated electrical device includes a non-conductive substrate and a graphene structure disposed on the non-conductive substrate. A metal gate is disposed directly on a portion of the graphene structure. The metal gate includes a first metal that has a high contact resistance with graphene. Two electrical contacts are each placed on the graphene structure so that the metal gate is disposed between the two electrical contacts. In a method of making a gated electrical device, a graphene structure is placed onto a non-conductive substrate. A metal gate is deposited directly on a portion of the graphene structure. Two electrical contacts are deposited on the graphene structure so that the metal gate is disposed between the two electrical contacts.

19 Claims, 2 Drawing Sheets



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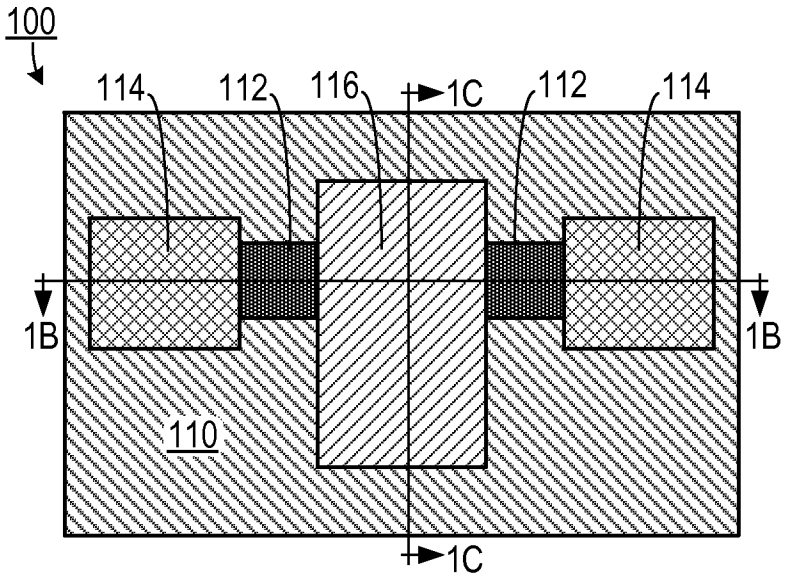

FIG. 1A

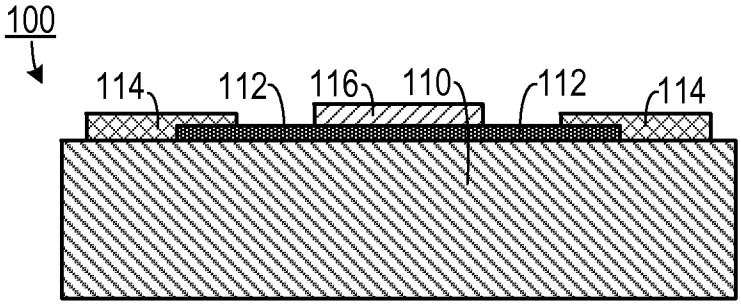

FIG. 1B

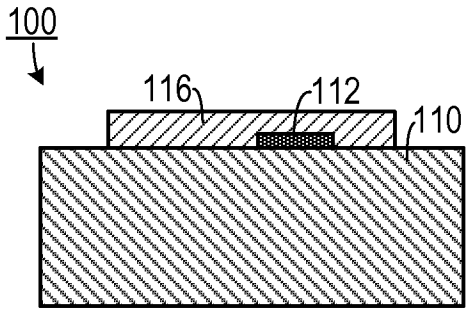

FIG. 1C

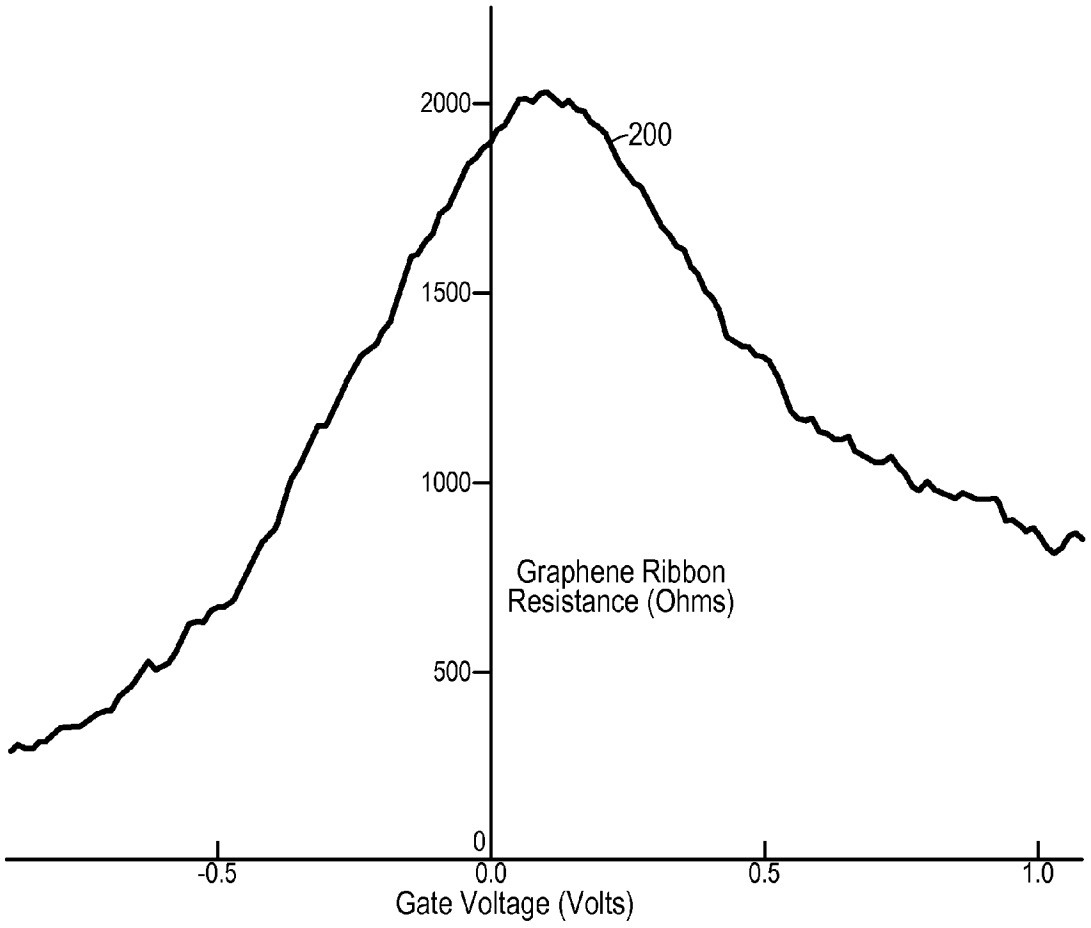
2000
1500
1000
500
0
200
Graphene Ribbon
Resistance (Ohms)
-0.5
0.0
0.5
1.0
Gate Voltage (Volts)

FIG. 2

METHOD TO MODIFY THE CONDUCTIVITY OF GRAPHENE

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application claims the benefit of U.S. Provisional Patent Application Ser. No. 61/250,722, filed Oct. 12, 2009, the entirety of which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to graphene devices and, more specifically, to a gated graphene device.

2. Description of the Related Art

Graphene has demonstrated numerous properties that make it suitable as a material for electronics. An important property of graphene is that its conductivity depends on the density of charge carriers (either electrons or holes) in the graphene. For example, when a voltage difference is applied between the ends of a graphene ribbon then a current will flow through the ribbon. The magnitude of the current depends on the density of the charge carriers in the graphene ribbon. This density can be modified using an electrostatic gate that selectively applies an electric field to a portion of the graphene ribbon, thereby modifying the resistance of the graphene ribbon in the vicinity of the gate.

Existing graphene electronic devices typically employ an electrostatic gate that includes a dielectric material that is deposited on a graphene sheet and a metal layer that is deposited on the dielectric material. Applying a potential difference between the metal layer and the graphene ribbon establishes an electric field at the graphene ribbon, which modifies the charge density in the graphene ribbon and its conductivity.

The effectiveness of the electrostatic gate is measured by the magnitude of the potential difference that is required to produce a certain change in the conductivity of the graphene ribbon. Typically, thinner dielectric layers are preferable. However, a dielectric layer that is too thin tends to leak and undesirable current flows from the metal layer to the graphene ribbon.

Applying a dielectric material to the graphene can be difficult because many dielectric materials do not adhere well to graphene. Therefore, graphene is typically modified chemically when applying a dielectric layer thereto. However, such chemical modification can degrade the quality of the graphene. Also, it is difficult to produce sufficiently thin dielectric layers on graphene using most conventional processes. This results in a need for relatively large potential differences to be applied between the gate and the graphene ribbon to produce a suitable gating effect in active graphene electronic devices.

Therefore, there is a need for a method of applying a gate to graphene that does not require application of a dielectric layer.

SUMMARY OF THE INVENTION

The disadvantages of the prior art are overcome by the present invention which, in one aspect, is a gated electrical device that includes a non-conductive substrate and a graphene structure disposed on the non-conductive substrate. A metal gate is deposited directly on a portion of the graphene structure. The metal gate includes a first metal that has a high contact resistance with graphene. Two electrical contacts are each placed on the graphene structure so that the metal gate is disposed between the two electrical contacts.

In another aspect, the invention is a gated electrical device that includes a silicon oxide substrate and a graphene ribbon disposed on the substrate. The graphene ribbon includes at least one layer of graphene. A copper gate layer is deposited directly on a portion of the graphene structure. Two electrical contacts are each placed on the graphene structure so that the metal gate is disposed between the electrical contacts. The electrical contacts include titanium coated with gold.

In yet another aspect, the invention is a method of making a gated electrical device, in which a graphene structure is placed onto a non-conductive substrate. A metal gate is deposited directly on a portion of the graphene structure. The metal gate includes a first metal that has a high contact resistance with graphene. Two electrical contacts are deposited on the graphene structure so that the metal gate is disposed between the two electrical contacts.

These and other aspects of the invention will become apparent from the following description of the preferred embodiments taken in conjunction with the following drawings. As would be obvious to one skilled in the art, many variations and modifications of the invention may be effected without departing from the spirit and scope of the novel concepts of the disclosure.

BRIEF DESCRIPTION OF THE FIGURES OF THE DRAWINGS

FIG. **1**A is a top plan view of one embodiment of a graphene transistor.

FIG. **1**B is a cross-sectional view of the embodiment shown in FIG. **1**A, taken along line **1**B-**1**B.

FIG. **1**C is a cross-sectional view of the embodiment shown in FIG. **1**A, taken along line **1**C-**1**C.

FIG. **2** is a graph showing resistance as a function of gate voltage in one experimental embodiment.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the invention is now described in detail. Referring to the drawings, like numbers indicate like parts throughout the views. Unless otherwise specifically indicated in the disclosure that follows, the drawings are not necessarily drawn to scale. As used in the description herein and throughout the claims, the following terms take the meanings explicitly associated herein, unless the context clearly dictates otherwise: the meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." Methods of generating an patterning a graphene ribbon are disclosed in U.S. Pat. No. 7,015,142, issued to deHeer et al., which is hereby incorporated by reference.

As shown in FIGS. **1**A-**1**C, one embodiment of a gated electrical device **100**, such as a field effect transistor, includes a non-conducting substrate **110**, such as silicon oxide or silicon carbide. A graphene ribbon **112** (or other graphene structure) is disposed on the non-conducting substrate **110**. A metal layer **116** is deposited onto the graphene ribbon **112**. The metal layer **116** includes a metal that exhibits a large contact resistance at its interface with the graphene ribbon **112**. Two electrical contacts **114** are deposited at the ends of the graphene ribbon **112**. The electrical contacts **114** include a material that has a relatively low contact resistance with the graphene ribbon **112**. In a transistor embodiment, the two metal contacts **114** can act as a source and a drain and the metal layer **116** can act as a gate.

One experimental embodiment employed a graphene ribbon **112** that was 1 μm wide and 10 μm long and grown on the surface of a silicon carbide crystal and patterned into the shape of a ribbon using known lithographic techniques (see, e.g., U.S. Pat. No. 7,015,142). The metal gate layer **116** included a 10 nm thick copper layer. (In one alternate embodiment, aluminum and similar metals can be used as the metal layer **116**.) The electrical contacts **114** were metal leads that included a layer of titanium that was coated with a layer of gold. (Other materials may be used for the electrical contacts so long as such the interface between such materials and the graphene ribbon **112** exhibits low resistance.) The metal leads **114** made good electrical contact with the graphene ribbon **112** in contrast to the copper layer **116**, which made poor electrical contact with the graphene layer **112**.

The metal may be deposited using one of several different methods of the type typically used in the micro electronics industry. One method employs evaporation of the metal onto to graphene surface so that it condenses on the graphene. A mask is used to define where the metal is deposited. The metal may be subsequently heated (i.e., annealed) to improve the crystal quality of the metal.

A graph **200**, as shown in FIG. **3**, relates resistance measurements of the graphene ribbon embodied in a field effect transistor in the experimental embodiment as a function of a voltage applied to the gate. As can be seen, the resistance of the ribbon is modulated by the gate voltage such that relatively small changes to the gate electrode voltage cause relatively large resistance changes in the portion of the graphene ribbon that is in close proximity to the metal gate electrode.

In one method, a graphene layer (or multiple graphene layers) is gated by applying certain metals directly to the graphene layer so that it is in physical contact with the graphene. Certain metals (e.g., copper and aluminum) can be applied directly to the graphene layer without an interposing dielectric layer and can still function as a gate.

Despite the direct physical contact between the metal and the graphene, the contact resistance between the metal and the graphene layer is large so that a significant potential difference can be sustained between the two without it causing unacceptable large currents to flow between the two. Consequently, the metal layer on top of the graphene sheet can serve as a gate and function in a manner that is similar to existing electrostatic gates.

It has been experimentally determined that the electronic properties of the graphene are not significantly altered due to the application of a metal on top of the graphene layer. Hence, in this method there is no need to apply a dielectric layer on top of the graphene layer in the gate area. Two advantages of this method include. (1) the complications of applying a dielectric are circumvented; and (2) only small potential differences applied to the gate are required to produce relatively large conductivity changes in the graphene layer.

The physical reason that the contact resistance between the metal layer and the graphene sheet are relatively large can be explained by properties of the materials. In one explanation, the Fermi surface in momentum space of a lightly doped graphene layer consists of 6 circles that are positioned in a hexagonal pattern. The Fermi surface of a gate metal layer lies within the hexagonal pattern of the Fermi surface of the graphene layer. As a result, the transfer of an electron from the metal to the graphene requires a substantial potential difference and, thus, the contact resistance is relatively large. Other physical mechanisms may also apply as well.

The scope of this invention may include many electrical structures (including metal structures, conducting polymer structures, and metal alloy structures) of many different shapes. The scope of this invention may also include methods to modify the work function of the metal layer on top of the graphene, in which the charge density on the graphene layer is modified as well. This will allow the graphene to be electrically biased without applying a voltage to the metal layer. For example, a thin copper layer may be applied to the graphene layer on top of which an aluminum layer is applied so that the work function of the resulting metal layer is modified, which will change the charge density in the graphene layer.

While the metal gate layer is deposited directly on the graphene ribbon, it is possible that the graphene, the metal gate layer, or both are modified (e.g., oxidized by an ambient gas) during or after the depositional process and that this modification results in the desirable properties of this invention. Additional treatments to the metal and the graphene ribbon may create desirable effects. Such treatments may include: heating the metal coated graphene; exposing the metal coated graphene to gasses in order to modify the graphene/metal interface; and exposing the metal coated graphene to chemical either in a liquid or a gaseous state to modify the graphene/metal interface. It is intended that the scope of claims below extend to all embodiments disclosed here, including embodiments in which the graphene ribbon or the metal gate are modified during the depositional process.

The above described embodiments, while including the preferred embodiment and the best mode of the invention known to the inventor at the time of filing, are given as illustrative examples only. It will be readily appreciated that many deviations may be made from the specific embodiments disclosed in this specification without departing from the spirit and scope of the invention. Accordingly, the scope of the invention is to be determined by the claims below rather than being limited to the specifically described embodiments above.

What is claimed is:

1. A gated electrical device, comprising:

a. a non-conductive substrate;

b. a flat graphene structure disposed on the non-conductive substrate;

c. a metal gate deposited directly on a portion of the flat graphene structure, the metal gate including a first metal that has a high contact resistance with graphene wherein the first metal comprises copper; and

d. two electrical contacts, each placed on the flat graphene structure so that the metal gate is disposed between the two electrical contacts.

2. The gated electrical device of claim **1**, wherein the substrate comprises a material selected from a group consisting of: silicon oxide and silicon carbide.

3. The gated electrical device of claim **1**, wherein the graphene structure comprises a graphene ribbon.

4. The gated electrical device of claim **1**, wherein the graphene structure comprises a single layer of graphene.

5. The gated electrical device of claim **1**, wherein the graphene structure comprises a plurality of layers of graphene.

6. The gated electrical device of claim **1**, wherein the graphene structure has a Fermi surface that includes a hexagonal pattern and wherein the first metal has a Fermi surface that lies within the hexagonal pattern of the Fermi surface of the graphene.

7. The gated electrical device of claim **1**, wherein the two electrical contacts include a second metal that has a low contact resistance with graphene.

8. The gated electrical device of claim **7**, wherein the second metal comprises a titanium layer.

9. The gated electrical device of claim 8, wherein the titanium layer is coated with gold.

10. A gated electrical device, comprising:

a. a silicon oxide substrate;

b. a graphene ribbon disposed on the substrate, the graphene ribbon including at least one layer of graphene;

c. a copper gate layer deposited directly on a portion of the graphene structure; and

d. two electrical contacts, each placed on the graphene structure so that the metal gate is disposed between the electrical contacts, the electrical contacts including titanium coated with gold.

11. A method of making a gated electrical device, comprising the steps of:

a. disposing a flat graphene structure onto a non-conductive substrate;

b. depositing a metal gate directly on a portion of the flat graphene structure, the metal gate including a first metal that has a high contact resistance with graphene wherein the first metal comprises copper; and

c. depositing two electrical contacts on the flat graphene structure so that the metal gate is disposed between the two electrical contacts.

12. The method of claim 11, wherein the substrate comprises a material selected from a group consisting of: silicon oxide and silicon carbide.

13. The method of claim 11, wherein the graphene structure comprises a graphene ribbon.

14. The method of claim 11, wherein the graphene structure comprises a single layer of graphene.

15. The method of claim 11, wherein the graphene structure comprises a plurality of layers of graphene.

16. The method of claim 11, wherein the graphene structure has a Fermi surface that includes a hexagonal pattern and further comprising the step of selecting the first metal so that the first metal has a Fermi surface that lies within the hexagonal pattern of the Fermi surface of the graphene.

17. The method of claim 11, wherein the electrical contacts include a second metal that has a low contact resistance with graphene.

18. The method of claim 17, wherein the second metal comprises a titanium layer.

19. The method of claim 18, further comprising the step of coating the titanium layer with gold.

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