

**MODELING, DESIGN, FABRICATION AND
CHARACTERIZATION OF GLASS PACKAGE-TO-PCB
INTERCONNECTIONS**

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The Academic Faculty

by

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**MODELING, DESIGN, FABRICATION AND
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INTERCONNECTIONS**

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“The highest forms of understanding we can achieve are laughter and human compassion” – Richard Feynman

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SUMMARY

Emerging I/O density and bandwidth requirements are driving packages to low-CTE silicon, glass and organic substrates for higher wiring density and reliability of interconnections and Cu-low k dielectrics. These are needed for high performance applications as 2.5D packages in large-size, and also as ultra-thin packages for consumer applications that are directly assembled on the board without the need for an intermediate package.

The trend to low-CTE packages (CTE of 3-8ppm/°C), however, creates large CTE mismatch with the board on which they are assembled. Interconnection reliability is, therefore, a major concern when low CTE interposers are surface mounted onto organic system boards via solder joints. This reliability concern is further aggravated with large package sizes and finer pitch. For wide acceptance of low CTE packages in high volume production, it is also critical to assemble them on board using standard Surface Mount Technologies (SMT) without the need for under-fill.

This research aims to demonstrate reliable 400 micron pitch solder interconnections from low CTE glass interposers directly assembled onto organic boards by overcoming the above challenges using two approaches; 1) Stress-relief dielectric build up layers on the back of the interposer, 2) Polymer collar around the solder bumps for shear stress re-distribution. A comprehensive methodology based on modeling, design, test vehicle fabrication and characterization is employed to study and demonstrate the efficacy of these approaches in meeting the interposer-to-board interconnection requirements. The effect of varying geometrical and material properties of both build-up

layers and polymer collar is studied through Finite Element Modeling. Interposers were designed and fabricated with the proposed approaches to demonstrate process feasibility.

CHAPTER 1

INTRODUCTION

1.1 Evolution of low CTE, Large and Thin Interposers and Packages

Advances in transistor scaling and miniaturization based on Moore's scaling law have brought continuous improvements in electronic systems in the last 40 years. This trend of transistor-scaling and their large-scale integration on a single IC leading to further advances in SOC continues. However, SOC can't integrate certain IC functions such as DRAMs, RF and MEMS cost effectively. Georgia Tech PRC has been pioneering an alternative approach known as the system-on-package (SOP). The SOP can be in 2D, 2.5D or 3D.

The continuous need for higher logic-to-memory bandwidth and logic-to-logic bandwidth, coupled with increased transistor scaling and the evolution of multicore processors resulted in a dramatic reduction in I/O pitch over the past few years and is expected to continue in the future. To support the large number of ICs for high-performance applications such as networking, the current package is thus expected to migrate to larger size, exceeding 60 mm in the near future as shown in Figure 1. Further, these packages should be assembled onto the board using standard low-cost surface-mount ball-grid array technologies (SMT BGA). The evolution of mobile communication markets, on the other hand, resulted in the convergence of digital with wireless functions into ultrathin and portable products. The total product thickness is expected to be less

than 6 mm in the future, resulting in a need for thinner packages as also shown in Figure 1.

The most important role of the package substrates, consistent the above needs, is to provide reliable and high-density chip-to-package interconnections with high density wiring achieved with fine-pitch RDL and micro-vias. They should also ensure the reliability of ultra-low K dielectrics in the ICs and package-board interconnections. The initial multichip packages in 1980s were based on 35-61 layers of ceramic substrates. These packages went up to 125 mm in size for high-end server applications and were connected to the board using Pin Grid Arrays. The 1990s saw a transition from ceramic to organic packages for several reasons including lower cost, better performance and board level reliability. Following years of development, the use of organic packages has been established widely within the packaging industry (Figure 2).

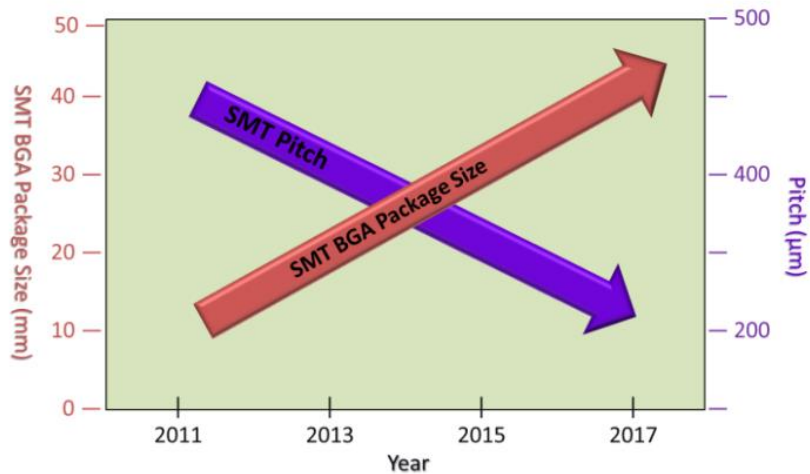


Figure 1: Trend to large, thin packages with reduced SMT pitch

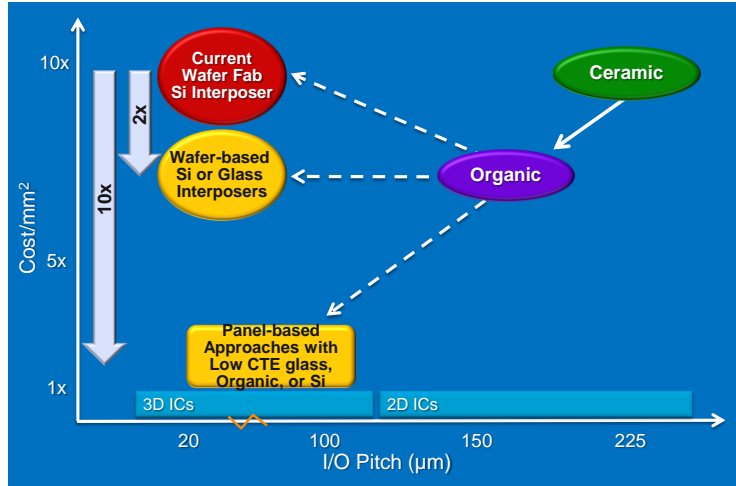


Figure 2: Package trend from ceramic to organic to large, thin, low CTE substrates using panel-based processes for low cost

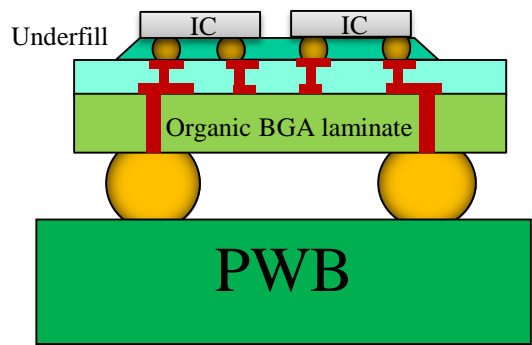


Figure 3: Traditional Organic BGA on PCB

Organic packages (Figure 3), however, have a number of shortcomings which limit their use in integrated systems. Poor dimensional stability limits lithographic design rules leading to low I/O pitch. Another concern is mismatch in CTE between the organic interposer (18ppm/°C) and silicon (3ppm/°C) chip, creating an interconnection reliability concern. The low thermal conductivity of the package has a negative effect on thermal performance. Lastly, and perhaps most importantly, the low elastic modulus of the organic package material leads to warpage during substrate fabrication and assembly at chip and board levels. Organic packages are continuously evolving with low CTE and higher stiffness to address these limitations.

To address the current challenges with organic interposers, semiconductor companies introduced silicon as an interposer material. Good dimensional stability coupled with its ultra-smooth surface finish enabled very high I/O densities. Fabrication equipment for wafer processing is widely available and the good CTE match between IC and the interposer reduces the interconnection reliability concern at the chip level. The use of silicon interposers, however, has its own set of challenges. The semiconducting nature of the material leads to electrical losses that may be too high for packaging applications. Costs for via formation and metallization run high when moving to fine pitch. Silicon also scores low on large area availability with wafers of size up to only 300mm, currently available.

Glass interposer's, pioneered by GT-PRC, are the newest alternative to silicon and organics, and show promise in a number of areas. The low dielectric constant and loss tangent give rise to excellent electrical properties. With a manufacturing process established in the display industry, glass is available as large and thin panels at a low cost. The cost of thinning down silicon interposers is eliminated by the availability of ultra-thin (<100 μ m) glass panels. In addition to high dimensional stability up to 500-600°C and a very smooth surface finish, glass also demonstrates high resistance to process chemicals. With mechanical and electrical properties favorable to their wide use as a package substrate, low-CTE glass, organic and silicon substrates are projected to become prevalent in both 2.5D and 3D package architectures.

1.2 The need for reliable interposer to board interconnections

In order for low CTE packages to be successfully accepted in high-volume production, it is critical that they be assembled onto PCB in an SMT-compatible manner at low cost and with high reliability. The CTE mismatch between these low TCE packages and PCB creates strains in solder joints because of the temperature differentials

due to a variety of internal and external events. Devices generate heat internally during operation, while external variations can be caused by load fluctuations, environmental temperature changes, and device on/off cycles. Lastly, large package sizes required by an increasing number of high-performance and mobile applications amplify the strain seen in the interconnections. Fatigue damage in surface mounted components can be reduced by the use of under-fills. However, under-fills increase the cost of the assembly while degrading electrical performance and hinder re-workability.

The chip-to-package reliability problem seen with the use of organic interposers can be addressed by using low CTE interposer-on-package approach (Figure 4). However, this approach creates a major barrier in achieving thinner products, a key requirement for mobile communication products as the CTE mismatch is transferred to the board level. Hence, a new class of interconnection technologies is required to directly mount interposer on the board, wherein the interposer becomes the package.

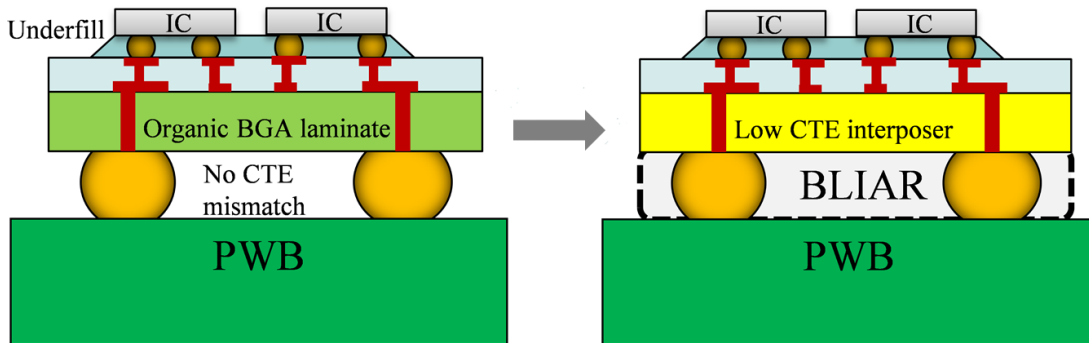


Figure 4: Low CTE interposer on package approach

1.3 Literature Review on Package-to-Board Interconnections

1.3.1 Current Approaches to low-CTE package-to-board interconnections

Two types of low-CTE package to board interconnection technologies are widely used. Large LTCC multi-chip packages use land grid array (LGA) and pin grid array (PGA) interconnections. Intel CPUs have been using PGA packages since the mid-90s. These packages can go up to 125 mm in size and are cost-effective for use in high-end applications. The interconnections are not SMT compatible, and pitch has not been scaled beyond 1000 μm .

The second type is small (~5mm) wafer level packages produced in high volume using SMT processes. Several approaches were developed to induce strain relief in these package-to-board interconnections - either using low modulus dielectrics between the bump and pads in order to de-couple the strain from the CTE mismatch between wafer-level packaged chip and board, or compliant metal structures to create strain-relief in the interconnections, or a combination of both approaches. These are summarized in Figure 5 and are briefly reviewed next.

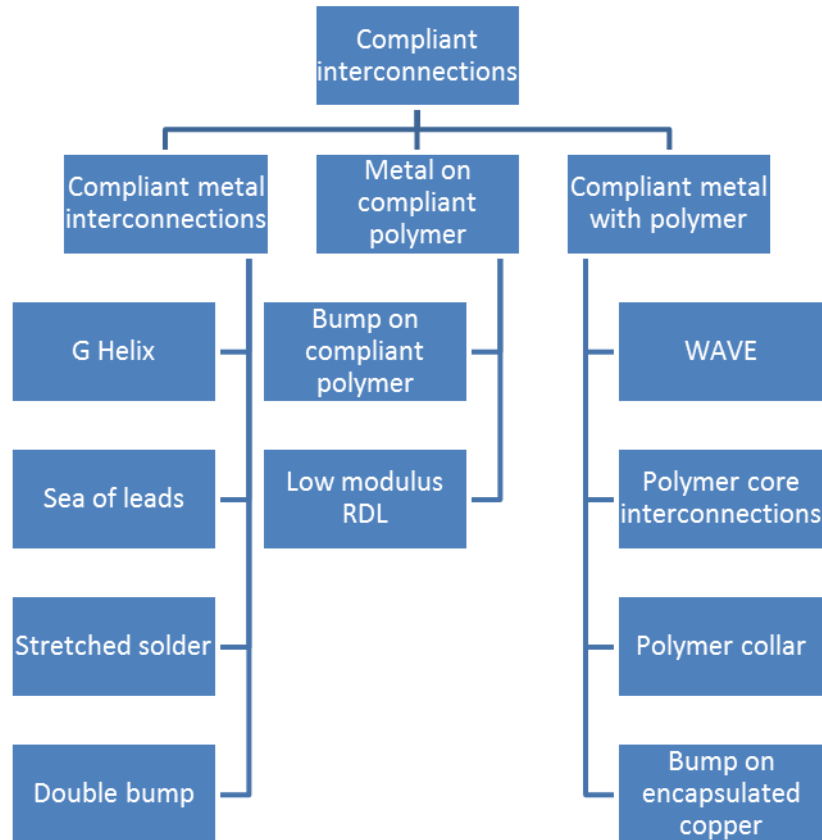


Figure 5: Summary of Compliant interconnections

1.3.2 Previous research on reliable board-level interconnections

The challenges seen in the assembly of low-CTE packages on to PCB are similar to those faced in chip to organic package and large WLP packages to PCB assembly. Chip-level interconnections reported in literatures that propose to address CTE-mismatch stresses can potentially be applied to the problem at hand.

1.3.2.1 Compliant metal interconnections

The G-helix [1] is a highly compliant, WLP-compatible alternative which utilizes a free-standing copper structure (Figure 6). These structures have been shown to survive more than a 1000 thermal cycles after chip to organic substrate assembly without any

under-fill. A major disadvantage with this approach is the direct increase in electrical parasitics with increased mechanical compliance.

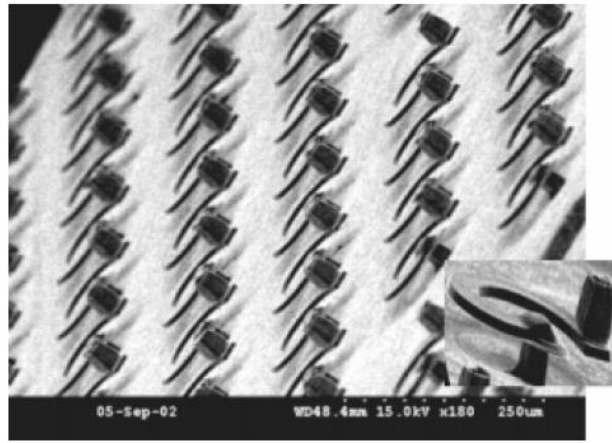


Figure 6: SEM micro-graph of G-helix interconnections

Increased compliance has been demonstrated by increasing the chip-to-package interconnection stand-off height with a stacked solder ball process [2]. High-lead solder balls were first embedded in a stress compensation layer after which the second solder ball is stencil printed onto the first. This structure is highly reliable and SMT compatible but significantly adds to interconnection standoff and electrical path length.

Stretched solder interconnections [3] propose to change the site of solder failure from the joint – pad interfaces to the center of the interconnection. The hourglass shape resulting from stretching the solder (Figure 7) improves interconnection reliability through the creation of a high aspect ratio joint with high compliance. It was shown that fatigue life could be improved to 2000 thermal cycles by increasing the aspect ratio of the joint to 2.8. Disadvantages to this approach include a non-standard assembly process in which it is hard to precisely control the shape of the stretched joint, and an increased interconnections stand-off height.

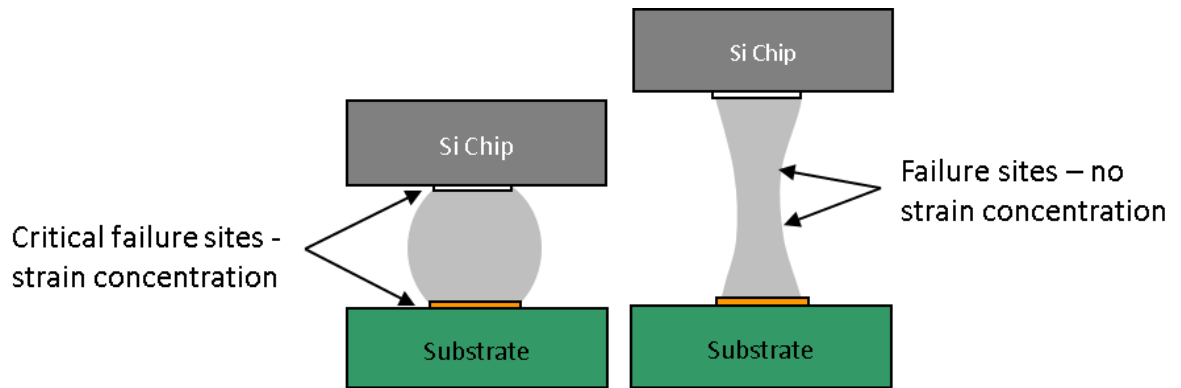


Figure 7: Conventional spherical solder vs. stretched solder joint

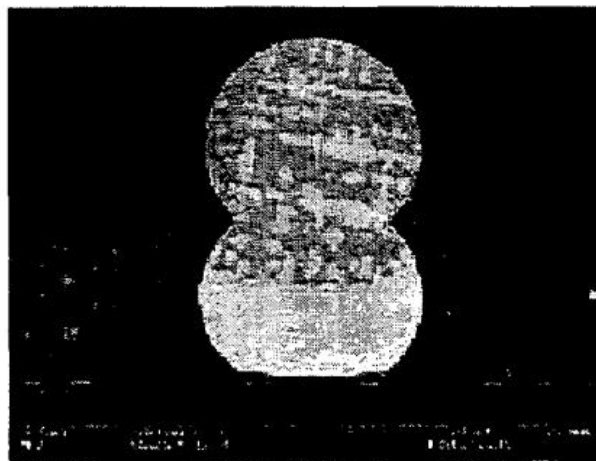


Figure 8: Cross section of stacked ball structure

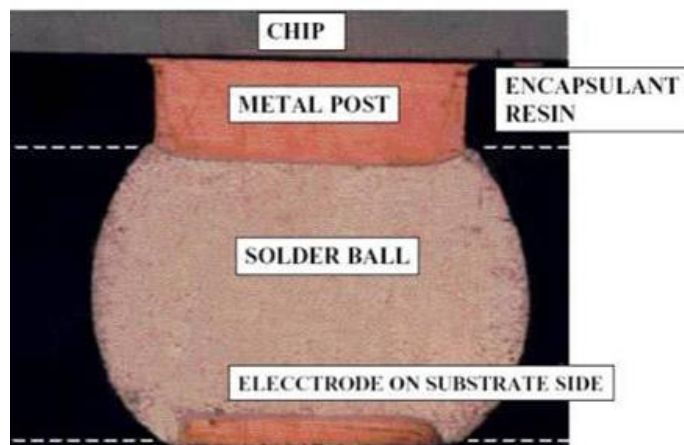


Figure 9: Bump on encapsulated copper post technology

Encapsulated copper post technology [4], shown in Figure 9, is another method that increases interconnection standoff to provide increased compliance. BGA pads are replaced by electroplated copper posts to mechanically de-couple the solder balls from the chip surface. The posts are encapsulated in an epoxy material through transfer molding.

1.3.2.2 Metal on compliant polymer

The Ball-on-polymer approach [4] to improving reliability of large array WLPs places the solder ball on over a layer of polymer thin film to avoid a direct connection between the ball and the silicon chip. This approach uses the low modulus polymer thin film to reduce solder ball deformation through the stress buffer effect. It was found that increasing the thickness of the polymer layer enhances reliability for 6 mm x 6 mm silicon chips assembled onto PCB.

ELAStec WLP by Infineon and IZM [5] proposes to avoid excessive straining of the solder joint by replacing the solder bump with printed S-shaped silicone bumps for added resilience. Electrical connections are provided through electro-deposited copper and nickel lines placed on top of the bump surface. This method introduces an additional concern in the possibility of over straining the metal lines. Furthermore, printing silicone bumps is a non-standard processing step.

1.3.2.3 Compliant metal with Compliant Polymer

Wide Area Vertical Expansion (WAVE) technology proposed by Tessera [6] is a WLP solution that introduces a low modulus compliant layer between the die and the

interconnection layer. A flexible electrical link between the contacts on the chip and the solder balls is built into the compliant layer. This method allows the chip to be mounted without the need for Underfill and effectively decouples the stress of CTE mismatch. Although this method is SMT compatible, non-standard fabrication steps are introduced which may not be cost effective from the perspective of high volume manufacturing. Another disadvantage is the increase in stand-off height required to provide the required compliance.

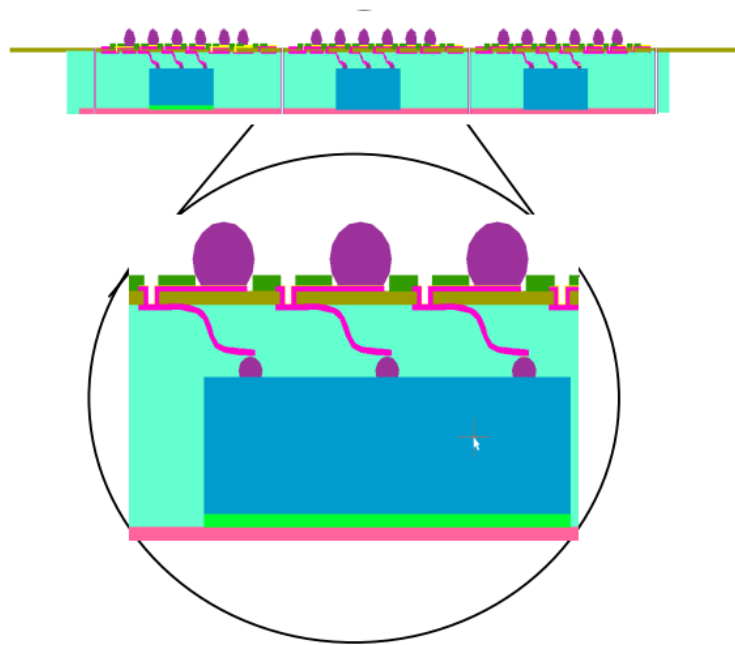


Figure 10: Compliant WAVE interconnections proposed by Tessera

Polymer core BGA is a compliant approach proposed by Kyocera for improving interposer to PCB reliability [7]. Using a ceramic package assembled onto PCB, electrical performance was preserved while improving reliability 2 to 3 times as compared to a traditional BGA. This approach, however, suffers from the disadvantage of additional process steps in the formation of the solder balls.

A high-density compliant interconnection solution has been proposed in the form of the Sea of Leads (SoL) technology [8]. The partially non-adherent leads aim to mitigate chip-to-PCB reliability issues by mechanically de-coupling the chip and the board and providing both in-plane and z-axis compliance. This approach has the capacity to enable ultra-high I/O densities but has not been established as an SMT solution due to its process complexity.

1.3.2.4 Previous Research on Glass package to PCB interconnections

Previous work on glass package to PCB interconnections at GT-PRC used a stress buffer layer on either side of the glass interposer to enhance interconnection reliability of 7.2 mm x 7.2 mm packages. Modeling results suggest that equivalent plastic strain in the outermost solder ball saturates beyond a certain package size [9]. High CTE glass was shown to be a better package material as compared to poly-silicon, undergoing up to 1700 thermal cycles before the first occurrence of joint failure [10].

1.3.3 Interconnection materials

Until less than a decade ago, Sn-Pb solders had been widely used in BGA assemblies due to their low melting point (resulting in lower reflow temperatures) and high wettability. However, due to the toxicity of lead and regulations against its use in electronic products, a number of new solder alloys have been introduced to replace these once commonly used materials.

Sn-Ag-Cu (SAC) solders have since become the preferred choice of solder alloy for BGA assemblies. The higher melting point of these materials (217 - 220°C) as

compared to that of Sn-Pb solders (180-190°C) translates into a higher reflow temperature of about 260°C to achieve good wetting. Due to the larger number of metals in the alloy, there is potential for a wider variety of intermetallics in the solder joint, making strain relief methods more critical. Another issue in the use of SAC solders is the head-on-pillow defect that arises out of the use of solder paste during assembly. This problem can be solved through the use of flux on the PCB instead of paste. SAC does however come with its advantages. The strength of the solder joint is higher due to higher resistance to gold embrittlement as compared to Sn-Pb alloys. SAC alloys also perform better under thermal fatigue in less extreme thermal cycling conditions.

Low-silver SAC (1% Ag) have become increasingly popular in BGA assemblies due to their improved performance over SAC 305 and SAC 405 alloys in component drop tests [11]. Reliability of components in hand-held and mobile devices is regularly characterized by drop shock tests making SAC 105 solders the dominant choice for such applications.

1.3.4 Life Prediction approaches for solder joints

Solder joint fatigue can be grouped in two categories, low cycle fatigue (LCF) and high cycle fatigue (HCF). LCF occurs when the interconnection strain is in plastic range and components are subjected to failure within 10^4 thermal differentials before failure, while the HCF regime occurs when the strain is in the elastic range and the fatigue life is between 10^4 and 10^8 cycles. The strains seen in thermally cycled solder interconnections usually belong to the LCF regime. The fatigue life of a solder joint is determined by considering the damage accumulated over all the cyclic temperature variations. Failure

occurs when the total accumulated strain exceeds the inherent ability of the solder material to sustain damage. The primary failure mode occurring in BGA assemblies is cracking at the intermetallic layer in the solder joints [12].

Creep failure is considered the dominant failure mechanism in SnPb solder materials. Lead-free solder materials call for critical consideration of plastic deformation as well. Two main damage metrics are used to predict the LCF lifetime of solders under cyclic thermal loading: the plastic strain range and the variation of inelastic energy density, taking into account stress and strain, over a load cycle. Based on these damage metrics, several fatigue models are commonly used to estimate the life expectancy of solder joints [13].

The energy density approach expressed in Morrow's model (Equation 1) predicts total number of cycles to failure in terms of inelastic strain energy density (W_p) and material-dependent ductility coefficient (A) and fatigue exponent (n). Inelastic strain energy density is determined by integrating over the region within the stable hysteresis loop.

Equation 1: Morrow's Energy Density model

$$N_f^n W_p = A$$

The plastic strain range approach, summarized in the Coffin-Manson model and its derivatives, can be expressed in the form shown in Equation 2. The total number of cycles to failure is expressed as a power law function of plastic strain range per cycle ($\Delta\varepsilon_p$) with the use of temperature dependent material constants, fatigue ductility

coefficient (C) and fatigue ductility exponent (m). These material constants are determined experimentally.

Equation 2: Coffin Manson plastic strain model

$$N_f^m \Delta \epsilon_p = C$$

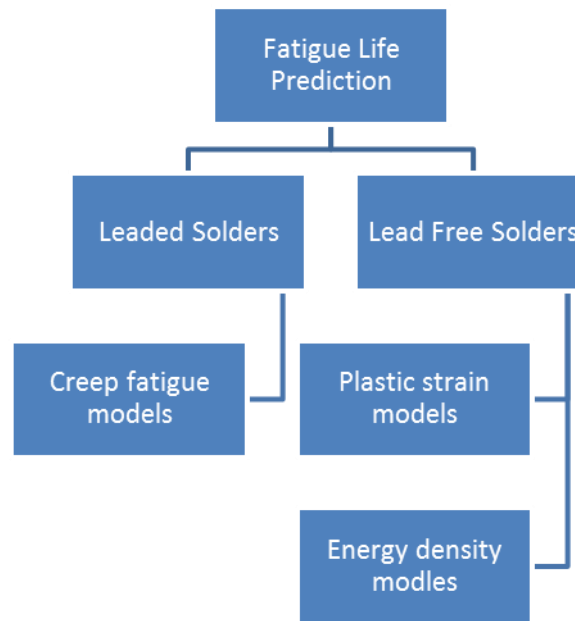


Figure 11: Fatigue life prediction models for solders

This thesis utilizes the plastic strain based Coffin-Manson model to evaluate solder fatigue life. Although the model does not account for time-dependent effects such as ramp rates and hold times, its simplicity and the availability of extensive experimental data on solder materials make it an attractive approach.

Table 1: Limitations of reviewed approaches

Prior Art		Chip/Package Size	Chip/Package material	Interconnection pitch	Limitations
Compliant Metal Interconnections	G-Helix	10 mm x 10 mm	Silicon	100/200 μm	-Increased electrical parasitics -Non-standard processing
	Double Ball	10 mm x 10 mm	Silicon	500 μm	-Increased stand-off height -Increased interconnection resistance
	Stretch Solder	20 mm x 20 mm	Silicon	600 μm	-Non-standard processing -Increased stand-off height
	Ball on copper post	6mm x 6mm	Silicon	500 μm	-Increased stand-off height
Metal on Polymer	Ball on Polymer	6 mm x 6 mm	Silicon	500 μm	-Not demonstrated for large packages
	ELAStec	10 mm x 10 mm	Silicon	500 μm	-Non-standard bump formation -Possibility of overstraining metal lines
Metal with Polymer	WAVE by Tessera	12.5 mm x 12.5 mm	Silicon	500 μm	-Non-standard processing -Increased stand-off height
	Polymer core BGA	21 mm x 21 mm	Ceramic	1000 μm	-Non-standard ball fabrication
	Sea of Leads	10 mm x 10 mm	Silicon		-Non-SMT compatible -Non-standard processing

1.4 Thesis objective

The objective of this thesis is to model, design and demonstrate reliable 400 μm pitch solder interconnections from low CTE glass interposers directly assembled onto organic FR-4 PCB. The two major technical challenges to achieving these objectives are 1) the CTE mismatch between the large glass package (4-10 ppm/ $^{\circ}\text{C}$) and PCB (16-18

ppm/°C), and 2) the requirement to achieve package re-workability through the elimination of underfill after assembly.

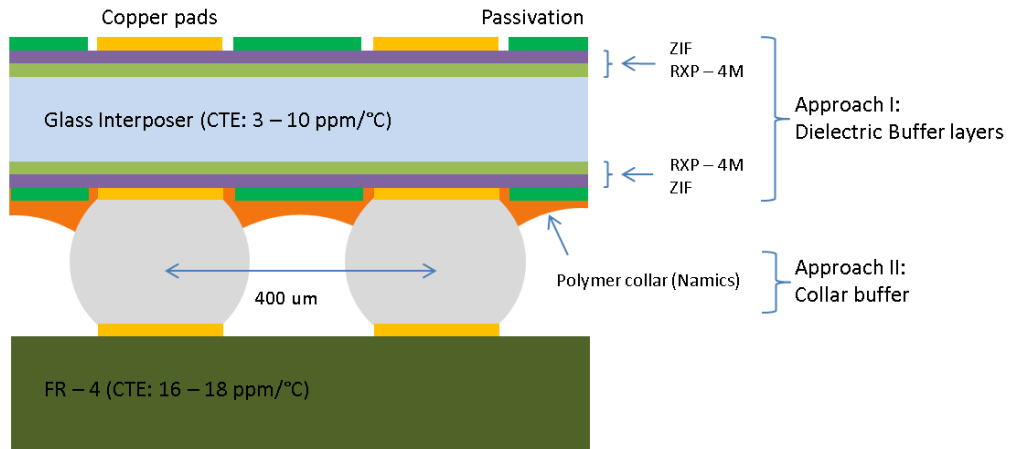


Figure 12: Approaches to solder strain relief

Two approaches (Figure 12) are employed to overcome the above mentioned challenges, 1) Dielectric build-up layers on both sides of the interposer for strain relief through increased interposer compliance, and 2) Polymer collar applied around the solder bumps to re-distribute the shear stress arising out of the mismatch after assembly.

Dielectric build-up layers act as stress buffer layers absorb the shear deformation of the interposer assembly arising from the CTE mismatch between low-CTE glass and PCB. The deformation of these layers helps reduce the strain in the solder joints, thus increasing the fatigue life of the interconnections. This behavior can be thought of as similar to that in a network of springs (Figure 13). The high modulus of the polymer chosen for the build-up layer increases the effective CTE of the interposer layer, bringing it closer to that of the board.

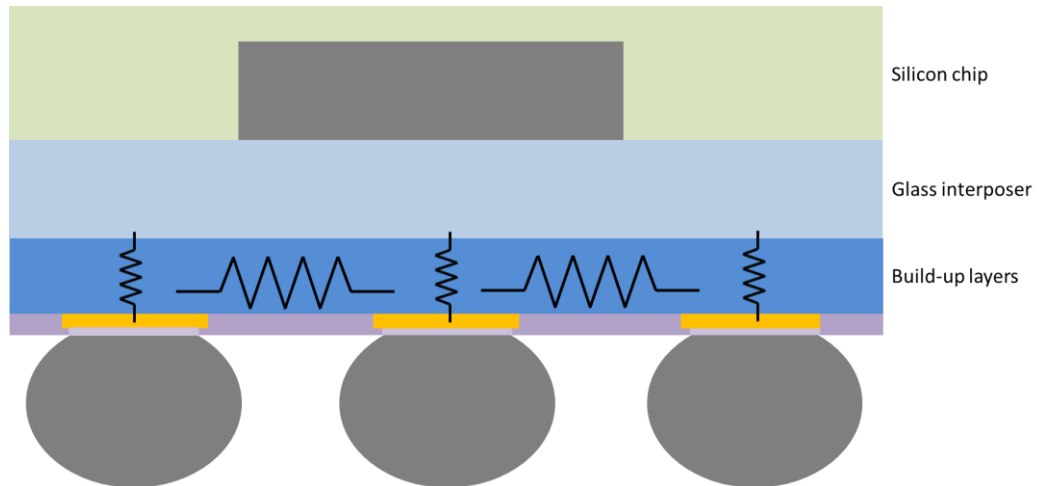


Figure 13: Dielectric build-up layers act as a network of springs

The interface between the solder joint and the package pads is critical due to presence of brittle intermetallic compounds that form at this junction. The circumferential polymer collar serves to block shear deformation of the solder joint at this interface, shifting the regions of high plastic strain lower down the height of the ball. In this manner the polymer collar acts as a partial underfill and maintains the re-workability of the assembly.

The two chosen approaches comply with the assembly process used in traditional SMT interconnections and have a negligible effect on electrical performance. The advantages these two approaches provide over those described in the previous section are listed in Table 1.

In order to examine the efficacy of these two methods in providing high reliability interconnections, a design of experimental study was devised with consideration given to pad design, package material CTE, and package thickness. This study incorporated learning from previous work on glass interconnection reliability. Finite element analysis

of the glass interposer assembled onto PCB was then done to understand and verify the physical mechanisms behind the chosen approaches and simulate the fatigue life of the various experimental variations. The effect of varying the geometrical and material properties of both build-up layers and polymer collar was studied. A test vehicle was designed in line with the needs of the semiconductor industry in terms of fine interconnection pitch and large package size. Interposers and boards were fabricated and subsequently assembled via BGA solder bumps to demonstrate process feasibility and extract experimental reliability data. Reliability testing was done through Thermal Cycling and standardized Drop Testing.

1.5 Thesis outline

This body of research demonstrates that a re-workable Surface Mount Technology (SMT) interconnection technology that is highly reliable between glass interposers and PCB. The organization of this thesis follows the order described in the previous subsection.

Chapter 2 concentrates on modeling and design to predict the strain relief and fatigue-life for the two proposed approaches. The rationale behind chosen experimental variations is explained and details of the interposer layout and design rules are covered. Next, the PCB design for both sets of reliability tests, i.e., thermal cycling test and drop test is covered. The next half of the chapter covers finite element modeling of the interposer structure to confirm strain relief mechanisms and optimize material and geometrical parameters related to the two approaches

Chapter 3 covers glass interposer fabrication. An overview of process flow is provided along with a discussion of each process step. This discussion is followed by a report on the issues seen during the glass interposer fabrication, along with the proposed solutions for each of them. An overview of the interposer coupon yield from two fabrication cycles is provided along with directives for improving the same.

Chapter 4 covers board level interposer assembly with the polymer collar. The process flow for applying the polymer collar material to the interposer is discussed, followed by the interposer assembly and subsequent polymer curing. Observations from process development that could be issues for manufacturability are discussed in detail with each discussion concluding by a practical solution to the problem. The next subsection concerns with the optimization of the polymer collar height. An experimental setup was devised and implemented in order to choose the optimum collar height before transferring this process technology to the large body size interposers.

Chapter 5 covers large body size interposer assembly, reliability testing and characterization. Given the yield of fabricated interposers and following the design of experiment (DOE) covered in Chapter 2, interposer coupons were assembled onto test PCBs. The results of the post-assembly inspection and reliability testing are detailed. The chapter concludes with a discussion of reliability results and conclusions with regard to the most reliable experimental variations.

Chapter 6 highlights the major results obtained out of the work covered in each chapter. Improvements to the experiments are suggested along with possible directions for future work on the topic of board level interconnection reliability of large low-TCE BGA packages.

CHAPTER 2

MODELING AND DESIGN FOR RELIABILITY

This chapter describes the modeling to predict the reliability of large low CTE glass package to PCB interconnections. Various package materials, geometries and assembly structures were considered using a comprehensive Design of Experiments (DOE) for modeling. An analysis of strain relief mechanisms for each of the design variations is then presented after simulating the structures through FEM. Optimal designs are recommended based on the modeling results.

2.1 DOE for Modeling

FEM was used to analyze the efficacy of the chosen approaches in relieving solder strains in the low CTE package to PCB assembly. The aim of FEM study was three-fold: 1.) compare the solder strains between all the package material and structural variations and provide optimal design guidelines for reliable package-to-board interconnections, 2.) study various assembly material and process options, including the effect of adding a molding compound to the top of the interposer, 3.) provide an understanding of the strain relief mechanisms.

2.1.1 Interposer or package selection

The glass packages and geometries used in the experimental test vehicle follow design guidelines consistent with the targeted pitch and package size. Two variations of the glass material were studied, with the only difference being that of glass CTE. Two interposer body sizes were used as part of the study. Pre-fabricated 7.2 mm x 7.2 mm

interposers were used for polymer collar process development and height optimization. Packages with 18.4 mm x 18.4 mm were fabricated, assembled and subjected to reliability testing. An overview of interposer design is provided in Table 2.

The BGA pitch on interposers of both sizes was fixed at 400 μm resulting in fully-populated arrays of 400 and 2025 interconnections for 7.2 mm and 18.4 mm interposers respectively.

Table 2: Interposer Test Vehicle Overview

Parameter	Options
Interposer Size	7.2 mm x 7.2 mm, 18.4 mm x 18.4 mm
Build-up Dielectrics	RXP-4M (20 μm) and ZIF (20 μm)
Interposer Material	Glass (3.8 ppm/ $^{\circ}\text{C}$), Glass (9.8 ppm/ $^{\circ}\text{C}$)
Interposer Pad Definition	NSMD, RMD

2.1.1.1 Choice of build-up layers

The interposer was designed with two dielectric layers laminated on each side of the glass panels in order to set up a structure similar to that present in a 4-metal-layer interposer stack-up (Figure 14). This also served to increase the effect of the dielectric build-up layers on solder strain relief.

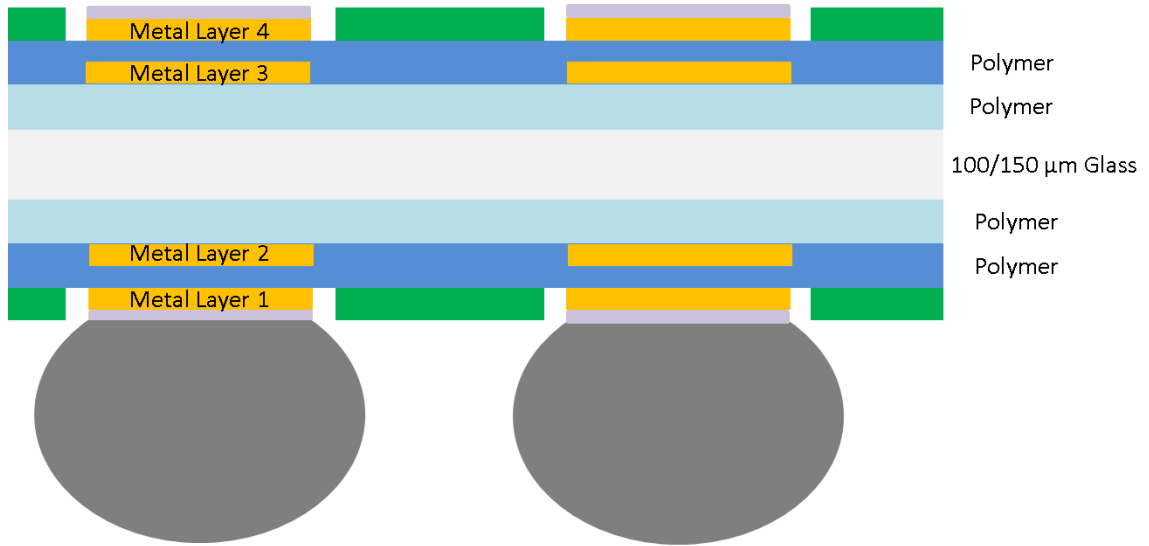


Figure 14: 4 metal layer interposer stack-up

The two materials considered for build-up layers were ZIF and RXP-4M (Table 2). The processing of ZIF is well documented and easy to integrate into the fabrication process flow. ZIF shows excellent adhesion with glass and copper traces. RXP-4M is a newer material under development and requires an increased amount of surface preparation for good adhesion to underlying layers.

Table 3: Material choices for build- up layers

Polymer Material	Elastic Modulus (GPa)	CTE (ppm/°C)	Poisson's Ratio
ZIF	7000	24	0.3
RXP-4M	1880	50	0.3

The first dielectric layer was chosen to be RXP-4M. Previous research on glass packages with a single build-up layer showed higher fatigue life with RXP-4M as compared to interposers laminated with a ZIF film. The lower loss tangent of RXP-4M is also advantageous for fine line wiring. A ZIF thin film was chosen as the second build-up layer due to the fact that it flows into the conformally plated vias to a higher degree of uniformity than RXP-4M.

2.1.1.2 Package assembly design rules

There are 2 main ways of designing the pads for any kind of assembly-level: solder mask defined (SMD) and non-solder mask defined (NSMD). In both cases, design standards have been established by the semiconductor industry based on modeling, assembly and reliability studies (reference attached documents). SMD pads are more common for balling as the surface tension of the solder mask is required to form the ball during reflow. However, PCB boards are generally NSMD to allow more “alignment tolerance” and a stronger bond. Resin mask defined (RMD) pads reduce the chance of solder bridges at a low interconnection pitch but can make routing more difficult due to the larger pad size. Symmetrical design is desirable, though uncommon. But, ideal design rules aim at having the same landing pad on both interposer and board side. In mind, the test vehicle incorporated both NSMD and RMD pad designs. With the copper pad diameter set at 225 μm , passivation opening was set to 340 μm and 180 μm in the NSMD and RMD interposers respectively. The pad diameter was kept constant to negate the effect of different pad sizes on interposer warpage.

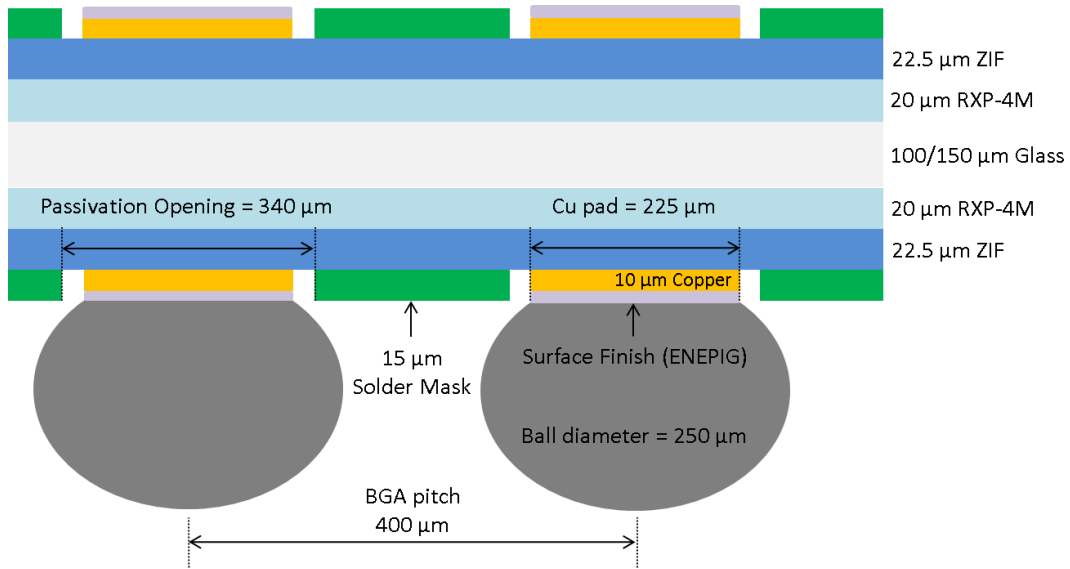


Figure 15: Design rules for NSMD interposers

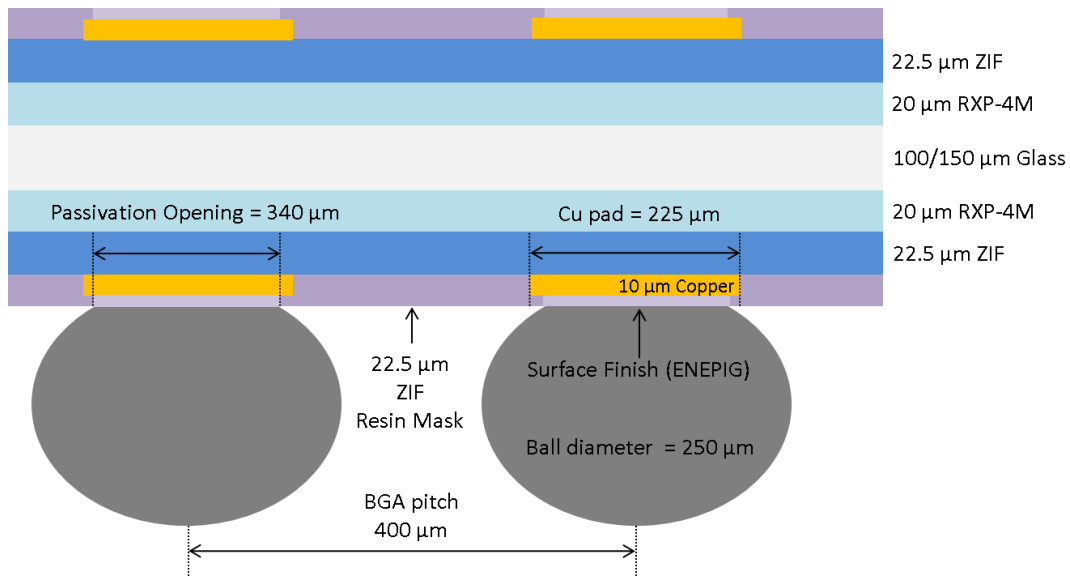


Figure 16: Design Rules for RMD interposers

Figure 17 outlines the 3 main fabrication and assembly variations present in this experiment. Given the relatively low performance of RMD interposers at 400 μm BGA pitch in previous studies, it was decided to test only NSMD interposers without the

polymer collar. These variations were fabricated with both low CTE and high CTE glass interposers leading to a total of 6 design variations.

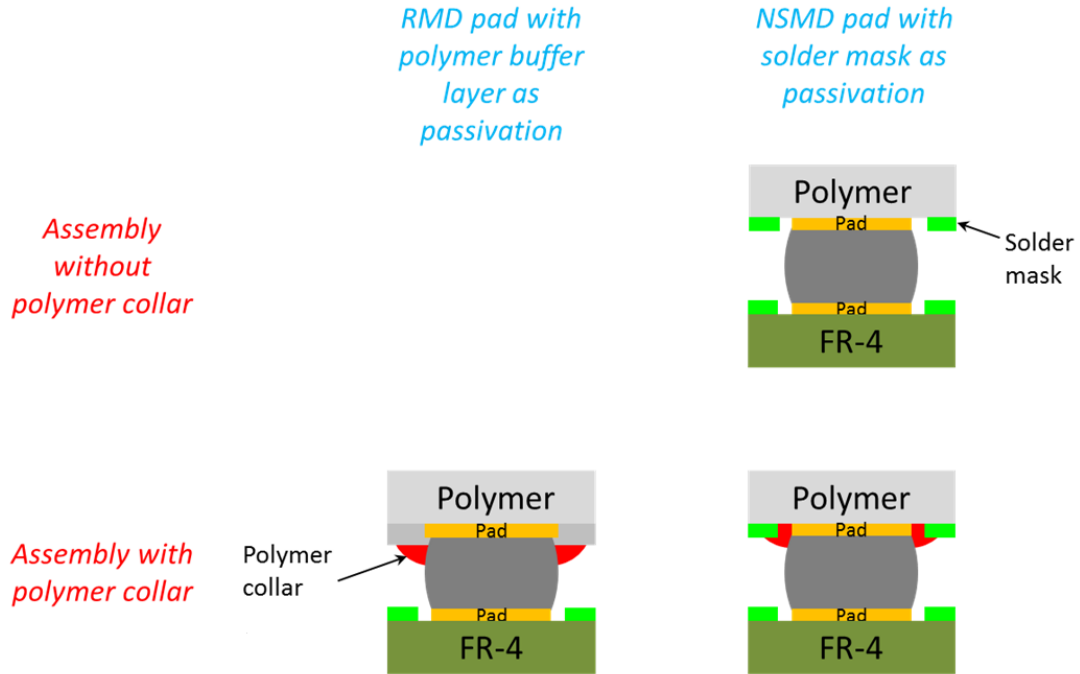


Figure 17: Fabrication/Assembly Variations

2.2 Modeling Studies

2.2.1 Model Construction in ANSYS

Two-dimensional (2D) half-symmetry models of glass and silicon interposers at various package sizes were created in ANSYS. These models were built along the diagonal of the package to capture the strain in the furthest SMT solder joint. Symmetry boundary conditions were applied to the left boundary of the package, with the bottom corner pinned. A section of the modeled structure is shown in Figure 18. This section was duplicated to arrive at the required package size.

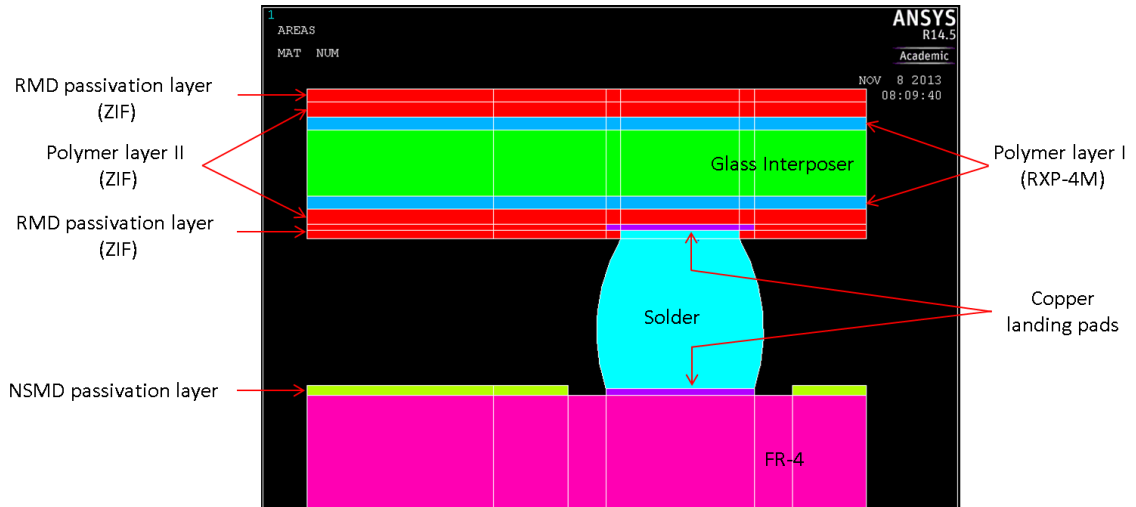


Figure 18: Unit Section of FEM structure

As reliability experiments are long and require a substantial amount of tested samples, thermo-mechanical modeling is a method of choice to estimate the fatigue life of solder joints and provide design guidelines for reliability. The reliability of second-level interconnections can be evaluated through TCT following the JESD22-A104D standard, which involves 2 additional reflow at 260C peak temperature, followed by thermal cycles at -40/125C with 15 min dwell time at each temperature extreme, at a rate of 1cycle/h. Due to the CTE mismatch between the stack-up materials, this thermal loading induces stress and strain in the structure, especially in the solder joints. In modeling, it is common to recreate this thermal loading to obtain the stress distribution in the structure and evaluate the plastic strain in the solder joints, which has been established as a critical factor for their reliability. Fatigue models predict the number of cycle to failure for these interconnections as a function of a damage metrics, which, in this case, is solder plastic strain.

The modeled package was first subjected to a temperature drop from 260°C to 25°C (room temperature) to emulate the residual stresses created in the package structure during the cool down phase of the SMT reflow process. Thermal cycling following JESD22-A106B thermal shock conditions was then applied. The ramp up and ramp down time was 1 minute, while the dwell time at both high- and low-temperature extremes was 5 minutes. The switch to thermal shock conditions is motivated by computational time. Equivalent plastic strain range in the last (10th) cycle is used as damage metric in the assessment of interconnection reliability. The Coffin Manson model (Equation 4) was used for fatigue life calculations with $C = 0.235$, and $m = 0.57$.

Equation 3: Coffin Manson model for low cycle fatigue life calculations

$$N_f^m \Delta \epsilon_p = C$$

Lead free solder SAC105 was used in both the modeling and the fabricated test vehicle due to better performance under drop testing conditions. The viscoplastic properties of the solder material were represented through the Anand model (Figure 19, Table 4). All other materials were modeled to be elastic in nature. As the materials used in this study are still in development phase by the suppliers. Material properties of the dielectric layers and polymer collar material are not known and cannot be evaluated for proprietary reasons. 217°C was chosen as the stress-free reference temperature for all models due to the proximity of this value to the solder melting temperature. For the purpose of verifying the strain relief mechanisms, results on high-CTE glass interposers are presented.

$$\dot{\epsilon}_{inel} = A^* e^{-\frac{Q}{RT}} * \left(\sinh\left(\xi \frac{\sigma}{s}\right) \right)^{\frac{1}{m}}$$

$$\dot{s} = \left\{ h_0 |\mathbf{B}|^a \frac{B}{|B|} \right\} \dot{\epsilon}_{inel}$$

$$B = 1 - \frac{s}{s^*}$$

$$s^* = \hat{s} \left(\frac{\dot{\epsilon}_{inel}}{A} e^{\frac{Q}{RT}} \right)^n$$

Figure 19: Constitutive equations for the Anand model

Table 4: Anand model parameters for SAC 105

Anand Parameter	Units	Value
A	1/s	8.2645e7
Q/R	K	8.7395e3
ϵ	-	0.994
m	-	2.17946e-2
s	MPa	7.7867
n	-	9.3855e-2
h₀	MPa	3486.50
a	-	1.091281
s₀	MPa	0.7514

Table 5: Material Properties

Material	E (GPa)	CTE (ppm/°C)	Poisson's Ratio	Material Behavior
Glass (High CTE)	74	9.8	0.23	Elastic
Glass (Low CTE)	77	3.8	0.22	Elastic
Silicon	130	2.7	0.28	Elastic
FR-4	24	16	0.3	Elastic
Solder	Temperature Dependent	22	0.34	Visco-plastic
Copper	121	17.3	0.3	Plastic

2.2.2 Simulation of strain relief mechanisms

This section focuses on understanding the mechanism behind the two chosen strain relief approaches. Modeling is done with two different interposer materials – glass, the promising new interposer material, benchmarked against already established silicon. A large interposer size of 18.4 mm is considered for these simulations. The initial focus will be on: high-CTE glass as the interposer material offers highest reliability of board-level interconnections. RMD pad design is considered due to its wider use in interposer assemblies.

2.2.2.1 Dielectric Build-up layers

Dielectric build-up layers improve reliability through self-deformation and act as stress buffer layers. The deformation of the dielectric layer can be measured as elastic XY shear strain in the region above and adjacent to the solder joint (Figure 20). In principle, this effect can be observed with either a low modulus dielectric layer or a less compliant, high CTE dielectric layer.

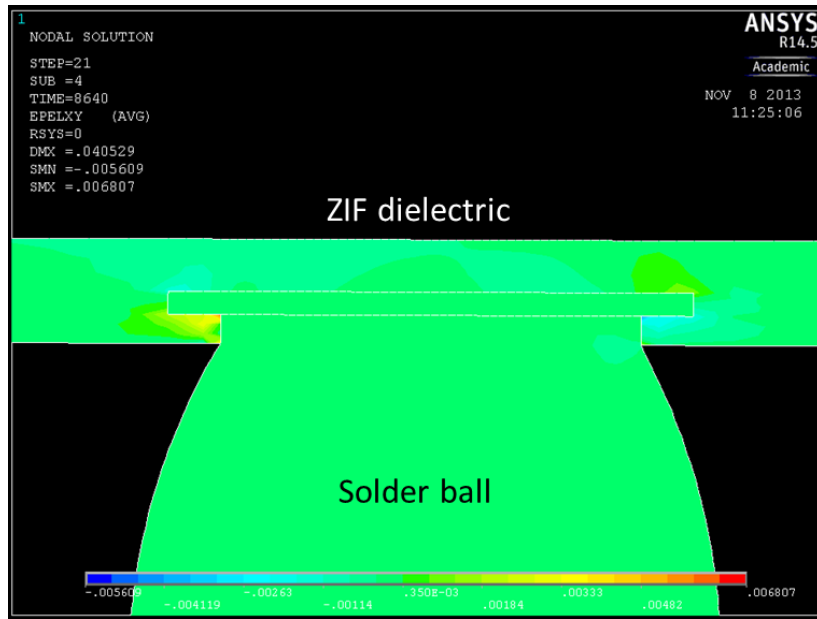


Figure 20: Dielectric Layer deformation measured as elastic XY shear strain

The test vehicle uses two dielectric layers laminated on either side of the interposer in order to simulate a 4 metal-layer stack-up. As shown in Figure 21, addition of a second dielectric layer decreases the maximum plastic strain range seen in the solder joint by 8.2 %. In addition, there is a decrease in the elastic XY shear strain in the region around the solder joint pad due to the increased compliance of the layer. The inclusion of two buffer layers in the test vehicle as opposed to one is therefore justified

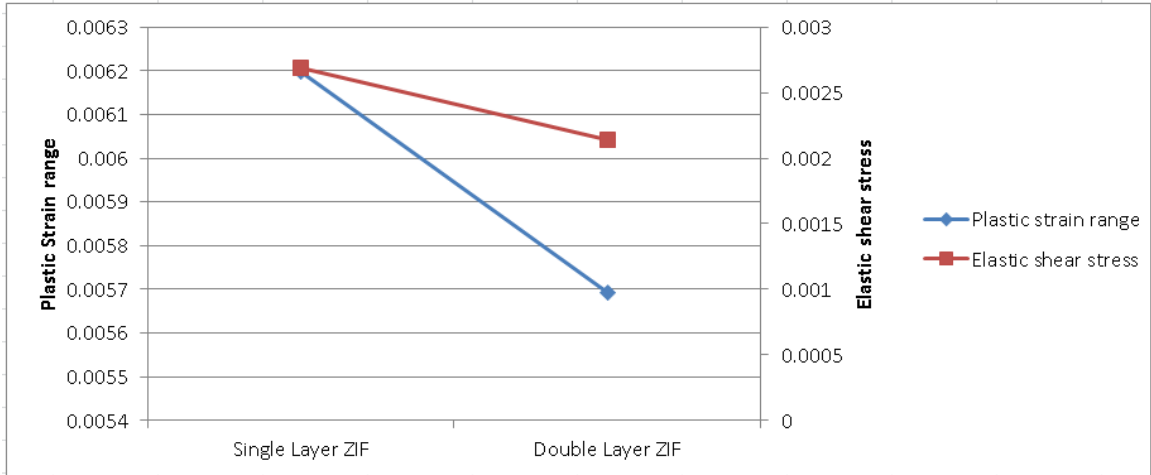


Figure 21: Effect of increasing the number of dielectric build-up layers

As expected, warpage increases when the thickness of the build-up layers is increased (Figure 22).

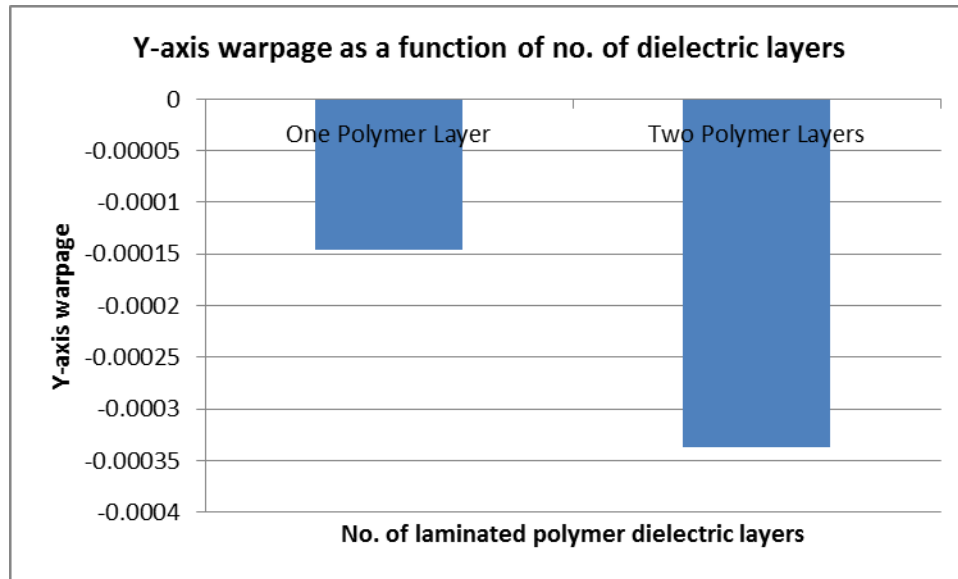


Figure 22: Effect of no. of dielectric layers on warpage

In order to understand the mechanism behind stress buffer strain relief in large interposers, an 18.4 x 18.4 mm RMD assembly was simulated with varying values of the

modulus of the second polymer layer. At low values of modulus, the dielectric layer is able to deform to a large extent (Figure 24), reducing the plastic solder strain (Figure 23). At large moduli, the dielectric layer does not deform, but plastic strain is nonetheless reduced due to an increase in the effective CTE of the interposer structure.

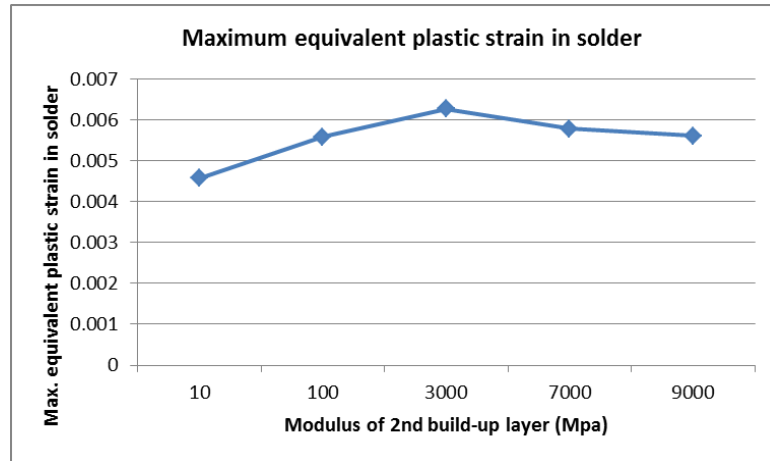


Figure 23: Variation of maximum plastic strain with modulus of 2nd build up layer

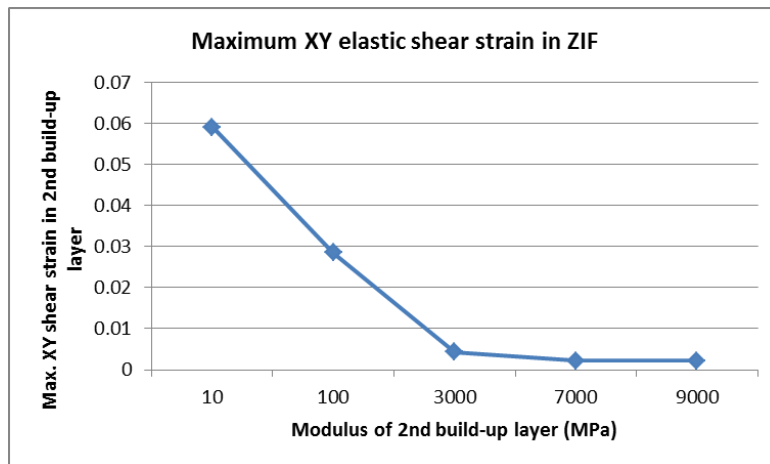


Figure 24: Variation of XY elastic shear strain in ZIF layer with modulus of 2nd build up layers

To confirm this result, the values of maximum shear strain in the package substrate were extracted (Figures 25 and 26). This maximum value is seen at the interface of the RXP-4M and glass interposer at the free edge of the assembly. With reduced compliance in the second build-up layer at high modulus values, a higher strain concentration is seen in the substrate, indicating that the CTE mismatch is now accommodated by warpage of the substrate.

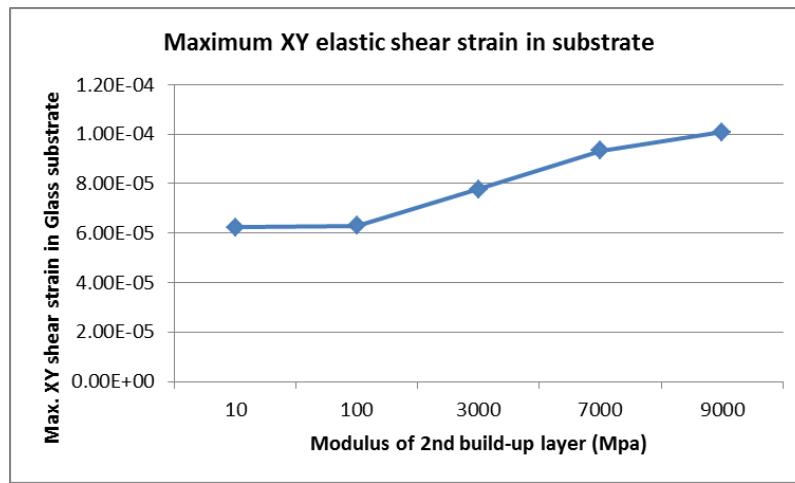


Figure 25: Maximum XY elastic shear strain in the glass substrate with the modulus of the 2nd build up layer

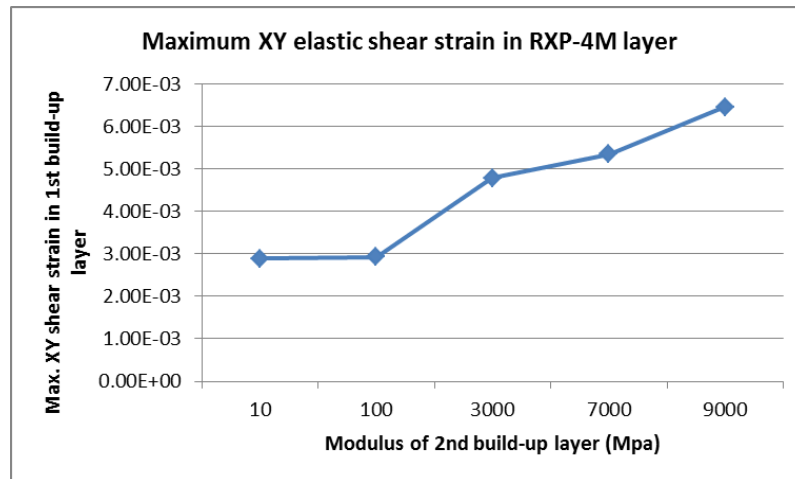


Figure 26: Variation in XY elastic shear strain in RXP-4M layer with modulus of 2nd build up layer

2.2.2.2 Polymer Collar

The circumferential polymer collar is applied to the balled interposer by spin coating. Table 6 lists the variations of polymer collar height used in this analysis.

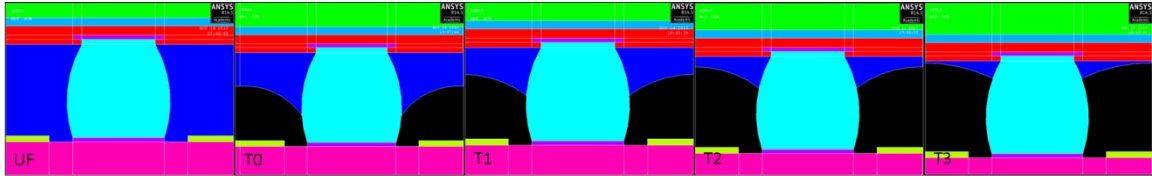


Figure 27: Variations in collar height

Table 6: Variations of polymer collar thickness used for analysis

Collar type	Height between/on solder balls
UF	Collar material applied as an underfill
T0	~170 μm
T1	~110 μm
T2	~80 μm
T3	~55 μm

High CTE glass interposer assemblies featuring build-up layers with each of the 5 collar types were simulated at a package size of 18.4 mm x 18.4 mm. The plastic strain range was extracted at four critical positions on the outmost solder ball. In the cases involving the collar, the measurement was made at the interface between collar and solder (Figure 28).

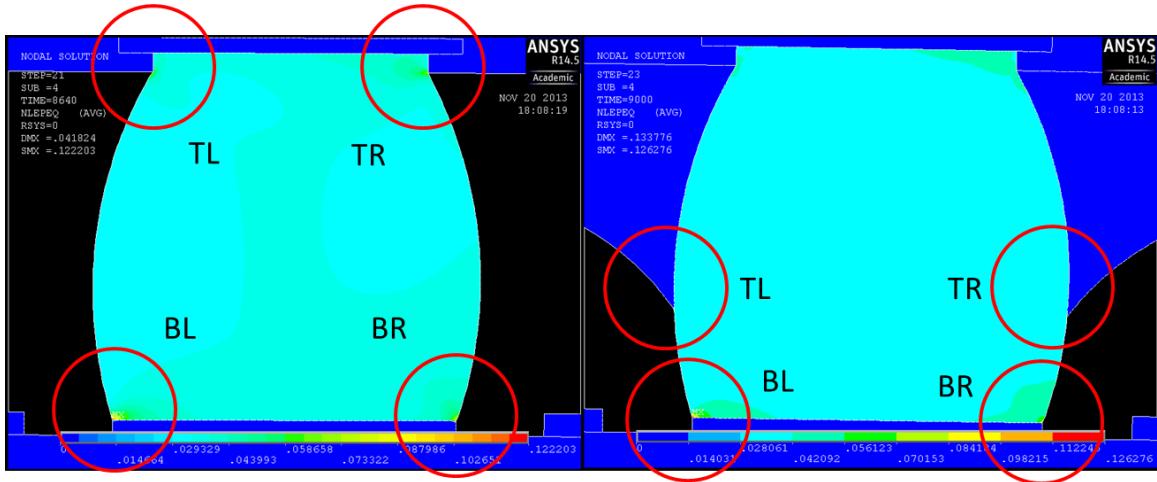


Figure 28: Positions of maximum solder plastic strain concentration for the cases of only build-up (left) and thick collar (right). Maximum strain in both cases can be seen at the bottom left corner of the joint

In the case of the assemblies with collar, regions of high plastic strain were transferred from the package interface to that between the joint and collar. Maximum plastic strain range was seen on the bottom left corner of solder joints in all simulations. The addition of the collar material serves to reduce the plastic strain range at all four corners of the joint. Although maximum strain is still on the board side of the assembly, the collar cannot be applied to the board as this would hinder rework-ability.

The results of these simulations confirm that this approach acts like a partial underfill. This is seen from the trend of decreasing strain range with increasing collar thickness (Figure 29). The thickest polymer collar (T0) provides the largest buffer to shear deformation and therefore shows the least strain range at the bottom left location. Relative strain range reduction at the bottom left corner of the solder joint is noted in Table 7.

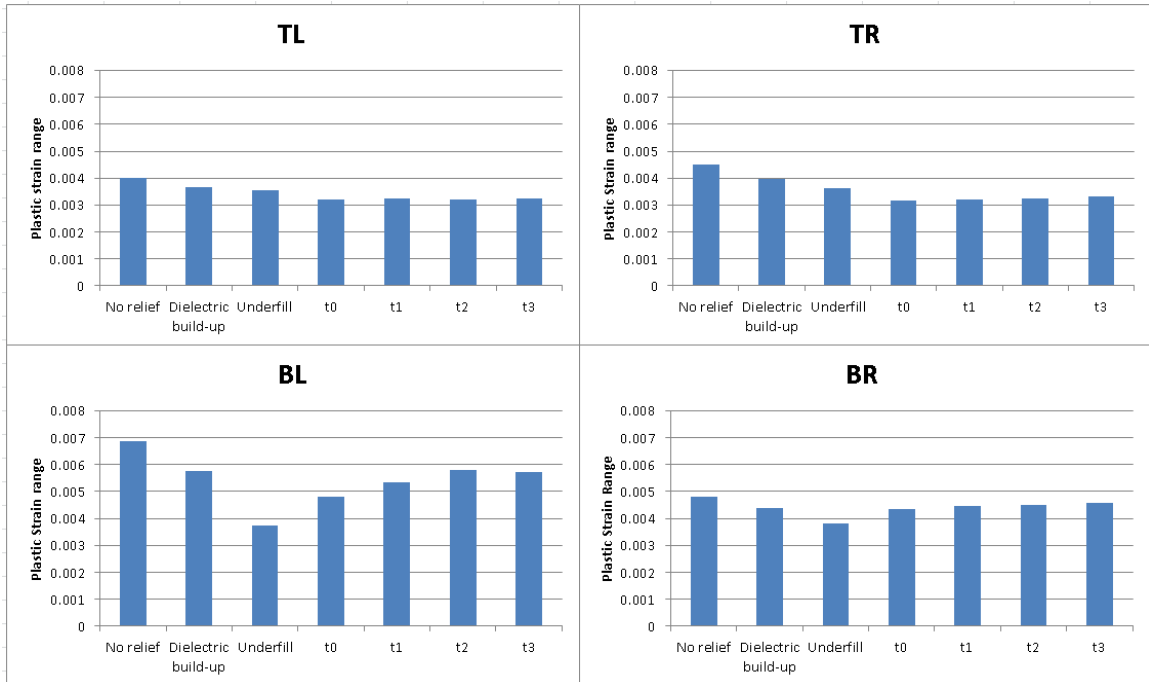


Figure 29: Plastic strain ranges at the 4 critical locations on the solder joint

The structure build with underfill shows the same value of strain at all four critical points on the solder ball. It may be observed that the polymer collar of all thicknesses provides more strain relief than underfill on the package side. This can be explained by the fact that the collar is transferring the strain away to the part of the solder ball which has more volume.

Table 7: Reduction in plastic strain range at the bottom left of the solder joint

Transition	Reduction in plastic strain range at BL corner
Only dielectric layers to T0	16.7 %
Only dielectric layers to T1	7.4 %

2.2.2.3 Effect of interposer material

The effect of interposer material on reliability is modeled for three interconnection structures. High CTE glass, being the closest CTE match to the FR-4 PCB shows lowest strain range, followed by low CTE glass and poly-silicon. High CTE glass is therefore the best interposer material choice when considering only board level reliability.

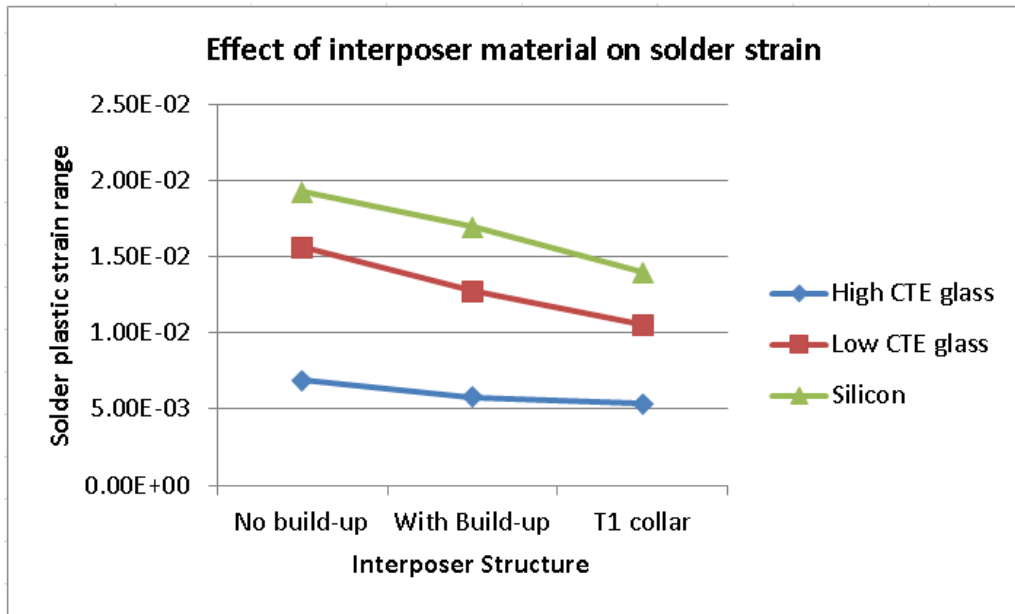


Figure 30: Effect of interposer material on solder plastic strain range

2.2.3 Applicability to large package sizes

2.2.3.1 Dielectric Build-up layers: Effect of package size

The size of the package was varied in order to study its effect on solder strain with and without dielectric build-up layers. Results suggest that solder plastic strain range tends to saturate at large package sizes (Figure 31). The reduction in solder strain range with the addition of the build-up dielectric layers was found to be almost constant with increasing package size (Table 8).

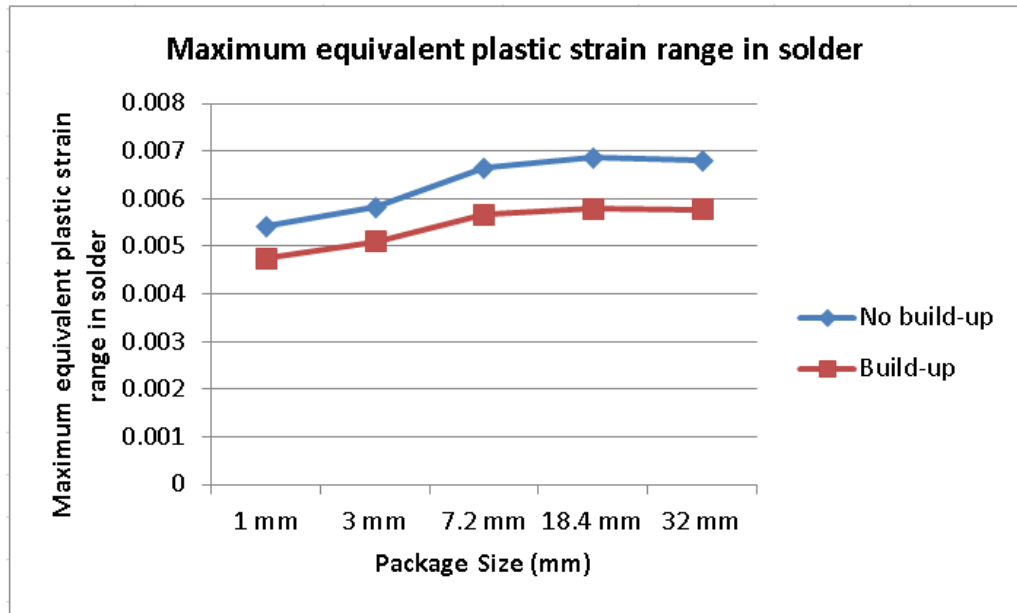


Figure 31: Effect of varying package size on solder strain range with only build-up layers

This result may be explained through the following mechanism. At large package sizes, the warpage of the interposer assembly is large enough that the solder ball itself suffers little deformation as compared to the case of a small package. Plastic strain in larger interposers is therefore accommodated by increased warpage of the assembly itself. This behavior may have a negative effect on the structural integrity of the package while increasing the risk of failure in other layers.

Table 8: % Reduction in solder strain range with the addition of the build-up layers

Package Size	% Reduction in solder strain range
7.2 mm x 7.2 mm	14.7 %
18.4 mm x 18.4 mm	15.7%
32 mm x 32 mm	15.1%

2.2.3.2 Polymer Collar: Effect of package size

Interposers simulated with build-up layers and T1 type collar at varying package size seem to follow the same trend of strain saturation seen in the case on only build-up layers. The behavior can be explained as before. Figure 17 compares the plastic strain range of interposers with only build-up layers to those with build-up layers and T1 collar (Figure 32). It can be observed that the change in strain range due to the polymer collar is negligible at small package sizes. Moving to larger package sizes however, improves the efficacy of polymer collar strain relief. Strain reduction is 6.65% and 7.48% at package sizes of 7.2mm and 18.4 mm.

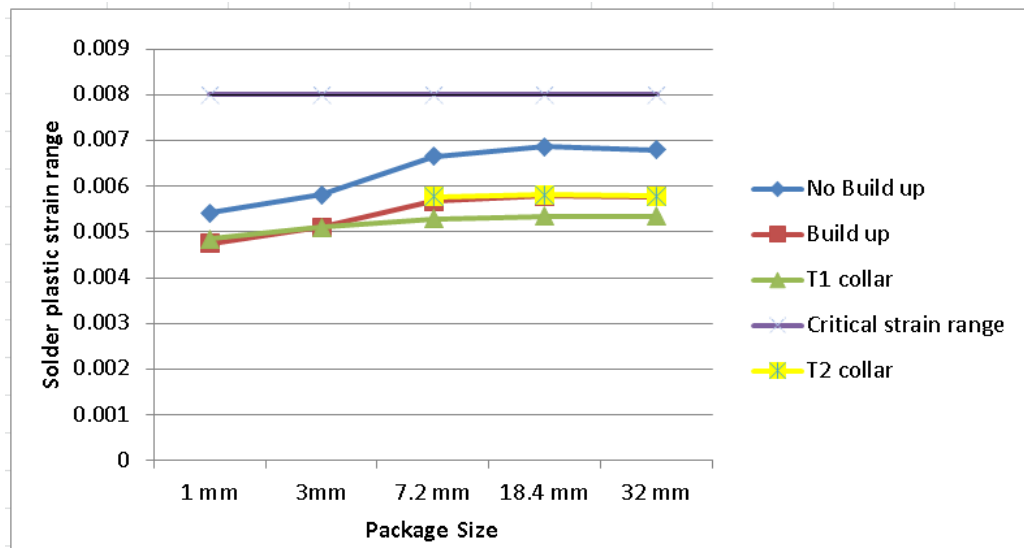


Figure 32: Effect of package size on polymer collar strain relief

2.2.4 Design guidelines from modeling

2.2.4.1 Recommendations for 18.4 mm interposers

Based on the results derived from modeling the interposer assembly, the following are recommendations for the design of the 18.4 mm test vehicle:

- Two build-up layers provides more buffer to strain relief, however, modeling shows that warpage may also increase due to the thicker package size. This may be a concern when moving to very large package sizes.
- Thicker collar reduces strain range, however, thick collars may affect assembly yield due to the residue on the ball surface (Chapter 4). Therefore a compromise must be reached between strain reduction and assembly feasibility.
- Package size may be pushed to 30 mm using current strain relief approaches. However, 2D modeling does not take 3D effects and process variations into account.
- Design test vehicle with ball pitch of 400 μm as this process has been established with minimal bridging. Ball pitch may be reduced in future experiments but introduces a new variable in the current study.

2.2.4.2 Reliability Test Vehicle Design

A reliability test vehicle was designed for the 18.4mm glass interposers. The test vehicle consisted of an interposer assembled onto a PCB via a 45x45 area array at 400 μm pitch (2025 solder balls). The solder balls were connected via daisy chains made up by dog-bone structures on both interposer (Figure 33) and PCB (Figure 34).

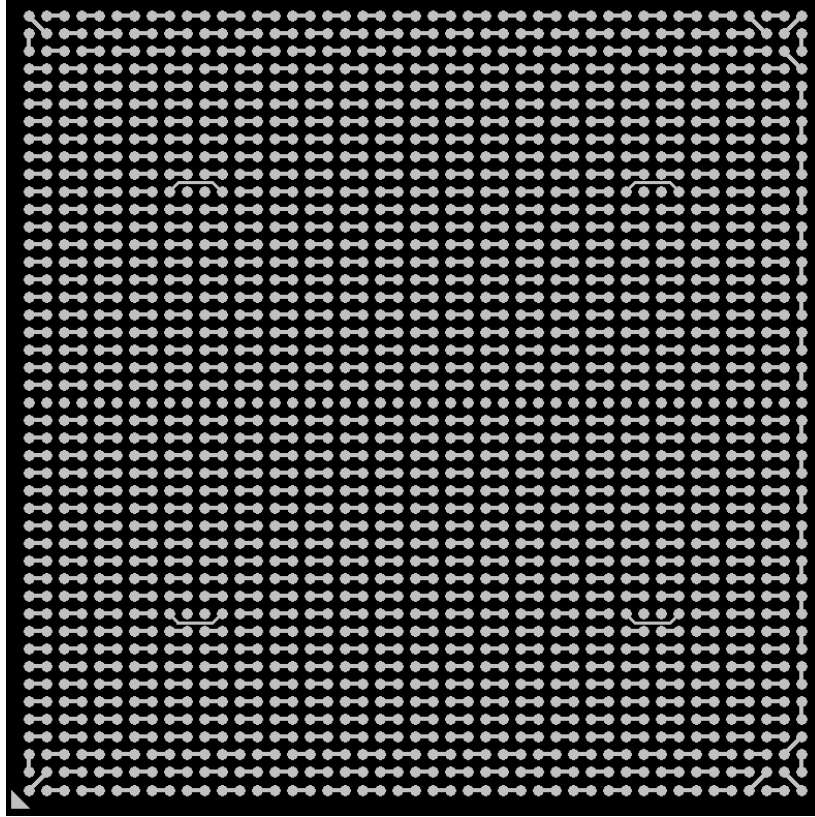


Figure 33: Dog-bone structures on interposer side of the test vehicle

Table 9 summarizes the specifics of the interposer design. Trace width was fixed based on ease of defect free fabrication. Ball diameter was chosen as 250 μm based on the prevalent use of this size in the industry. Ball pitch was fixed at 400 μm .

Table 9: Interposer Design rules

Parameter	Value
Copper trace width	60 μm
Copper thickness	10-12 μm
Ball diameter	250 μm
Copper pad diameter	225 μm

The test PCB was designed to complete the daisy chains set up on the interposer side. 4 daisy chains were placed at the corners of the package (4-probe structures in Figure 34) to test the most critical solder balls. The rest of the solder interconnections are divided up into side and internal chains.

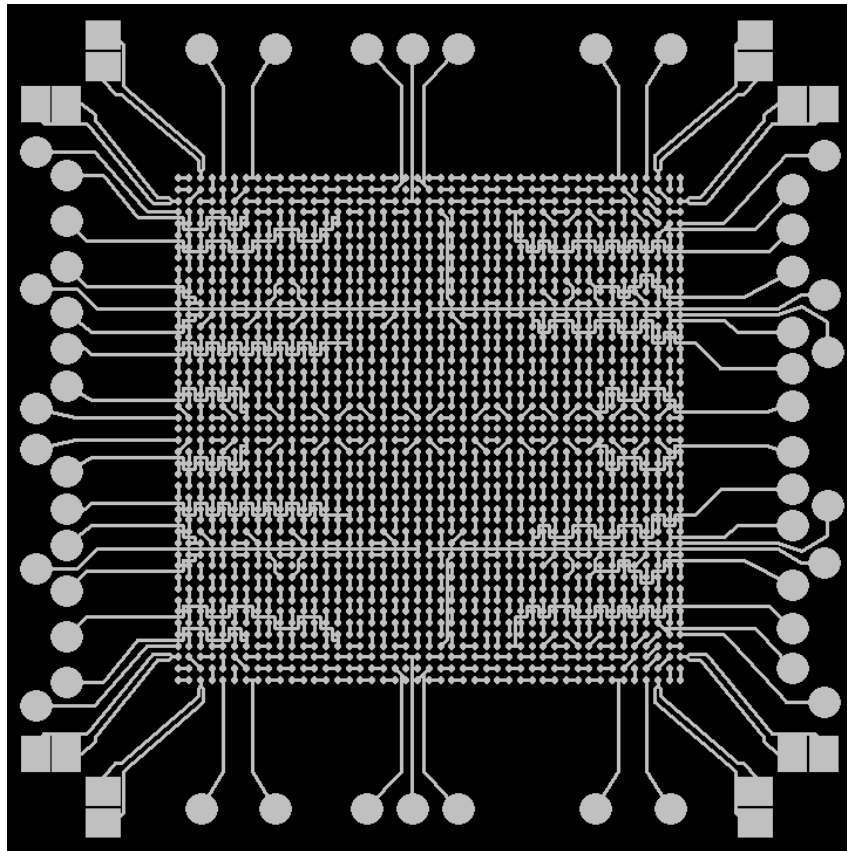


Figure 34: Designed PCB coupon for reliability

The details of interposer fabrication are covered in Chapter 3. Single layer PCB fabrication was performed by an external supplier. OSP surface finishing on the PCB and all patterning was done within a tolerance of 10%.

CHAPTER 3

GLASS INTERPOSER FABRICATION

This chapter describes the fabrication of 18.4 mm x 18.4 mm size glass interposers. Two fabrication cycles were conducted. After a discussion of the fabrication process flow, details of the fabrication yield and process analysis from each of the cycles are provided.

3.1 Panel Layout Design

Figure 35 shows an overview of the glass panel design, based on the design rules established in Chapter 2. Interposers are connected to the PCB via a 45x45 area array at 400 μm pitch. Alignment via holes were drilled at 8 locations on the panel (encircled in blue) to enable front-back side alignment during photolithography. This was required to ensure that the interposer structure was symmetrical with respect to build-up (Figure 36). The side of the interposer with higher yield is used for ball attachment. The other side can be used to study copper adhesion during thermal cycling. The passivation layer (both NSMD and RMD) was aligned using plated copper fiducials present at the four corners of the panel.

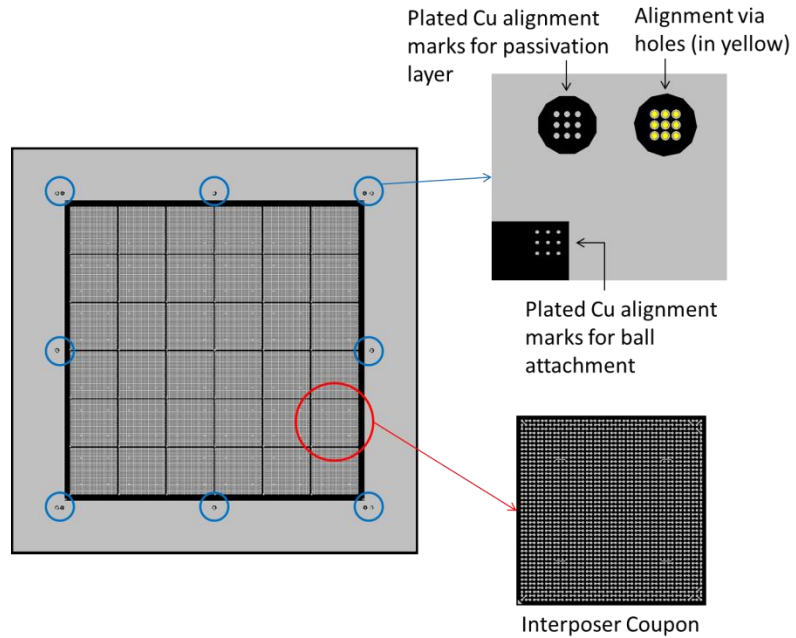


Figure 35: Panel Layout



Figure 36: The copper patterning is mirrored to reduce imbalance in the interposer structure

3.2 Fabrication Process Flow

Figure 37 illustrates the fabrication process flow of the glass interposer panels. The following sub-sections detail each process step.

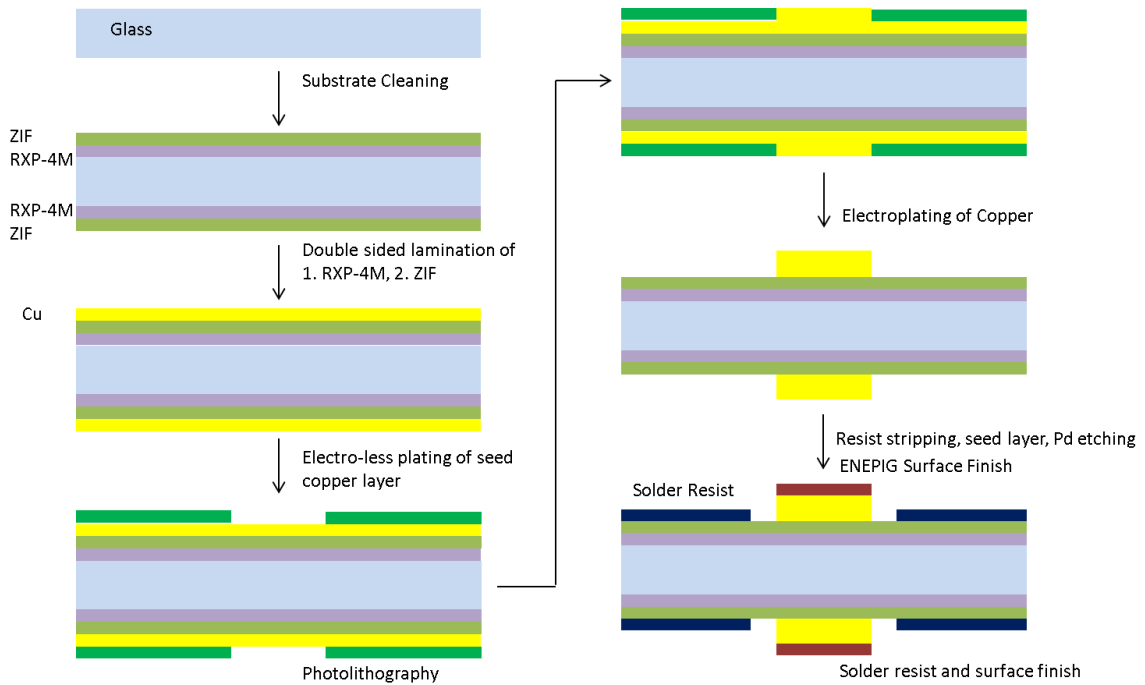


Figure 37: Panel level fabrication process flow for glass interposers

3.2.1 Dielectric lamination

The glass panels were first cleaned to remove any particulate matter from their surfaces through consecutive rinses with isopropanol solution (IPA), acetone, and de-ionized water. This was followed by baking in an atmosphere of air at 100-120°C for 10 minutes. Following this cleaning step, the panels were then laminated with RXP-4M and then ZIF thin films.

3.2.1.1 Lamination of RXP-4M thin-film

Adhesion of the glass surface was improved through surface treatment with amino-silane. The panels were baked after each application of the solution. Lamination of the dry-film polymer was done in a hot press with a peak temperature of 246.11°C and

peak pressure of 2 tons. The temperature/pressure profile used for RXP-4M lamination is reproduced in Figure 38. Pressure is released during the cool-down phase to allow the substrate to contract freely.

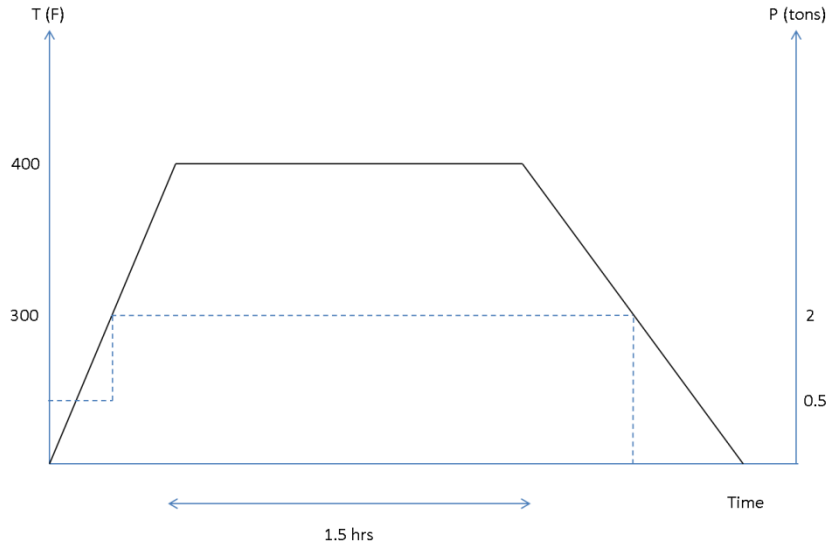


Figure 38: Temperature/Pressure profile for lamination of RXP-4M on to glass using hot press

3.2.1.2 Lamination of ZIF thin-film

The exposed RXP-4M surface is cleaned with de-ionized water prior to lamination of the ZIF dry film. Lamination is done in a vacuum laminator at 93.33°C. The panels were then subjected to hot pressing to even out the surface of the uncured polymer. Curing was carried out by baking the panels at 180°C for 1 hour.

3.2.2 Alignment via drilling and electro-less plating of Copper

After lamination of the two build-up dielectric layers, the glass panels were sent to an external supplier for laser drilling of alignment vias through the glass. A 0.3 μm thick seed layer of copper was subsequently plated onto the panels using chemistry

provided by Atotech (Table 10). This process deposits palladium which acts as a promoter for copper deposition causing a contamination issue that will be covered in the following sections. The panels were plated using a vertical frame causing some amount of edge chipping. This chipping becomes more critical while working with thinner glass. The plated copper was then annealed by baking the panels at 120 °C for 1 hour. The seed layer forms the basis of the semi-additive process for copper patterning.

Table 10: Process steps for electro-less plating of copper

Process step	Surface cleaning
Sweller solution	Rinse
Permanganate treatment	Rinse
Neutralizer	Rinse
Conditioner	Rinse
Pre-dip solution	
Activator	Rinse
Reducer	Rinse
Electro-less plating	Rinse
Acid dip	Rinse
Anti-tarnish solution	

3.2.3 Photo-lithography and electro-plating of metal layers

Contact photolithography was used to pattern the metal dog-bone layer. A 15 μm thick dry film negative photoresist was used to achieve the target copper thickness of 10-12 μm . The thin film photoresist (RY-5315) was first laminated onto both sides of the panels using a hot-roll process at 125°C. The panels were then exposed to UV light in a Karl-Suss MA6 mask aligner through a negative-type mylar mask for 6 seconds. Development was then carried out in MF319 solution with a conveyor speed of 7mil/minute. After visually inspecting the panels to verify proper development and alignment, each side was subjected to the plasma de-scum process to remove any photoresist residue from the seed Cu surface that would affect the yield and quality of the electrolytic plating anchor.

A FR4 dummy board was first plated in the electrolytic plating bath to verify and optimize the process conditions. The board was treated in an acid bath to remove any oxidation from the seed copper surface before being introduced into the electrolytic bath. A current density of 20ASD was applied for 1 hour. After completion, the dummy board was rinsed in DI water and inspected for plating quality. The glass panels were then put through the same process steps, after optimization of the conditions. The final thickness of the dog-bone layer was measured to be 10-13 μm on average.

The thin film photoresist layer was then removed using a resist stripping solution, followed by Cu Seed layer micro-etching. The micro-etching step was followed by a Pd etching step to remove all contamination from the surface of the underlying ZIF. This second etching step is critical as Pd particles embedded in the ZIF polymer can act as a

promoter for electro-less Ni plating during the surface finishing step, introducing metal contamination before the ball attachment step on NSMD panels. Depending on the roughness of the ZIF surface, Pd particles may be trapped at varying depths on the polymer surface. Increasing the etching time could have a negative effect as the solution etches copper..

The electro-plated copper is then annealed at 130 °C for 1 hour. Blistering on the surface of the plated copper may be seen if any contamination was introduced during the lamination steps. The panels are cleaned once again with an acid solution and subsequently coated with anti-tarnish.

3.2.4 Passivation layer

3.2.4.1 Solder mask for NSMD design

A photosensitive 15µm thick dry film FZ – 2715 manufactured by Hitachi Chemical was used as passivation layer for the NSMD panels. This material is a negative type photoresist. Liquid solder resist was not use as it is difficult to achieve uniformity over the panel area through spin coating. . The bondfilm surface preparation process (Atotech) was first applied to the panels to improve the adhesion between the copper dog-bone layer and the dry film material to prevent delamination during subsequent process steps and testing. The material is then laminated onto both sides of the panels using a vacuum lamination process at 150 °C. A negative mask is used during UV exposure for 13 seconds on the mask aligner tool. After development and plasma de-scum, curing is carried out in two stages. The first is UV curing for 75 seconds on each side followed by baking in an oven at 150 °C for 1 hour.

3.2.4.2 RMD passivation

A 17.5 μm ZIF dry-film is used to form the passivation layer on the RMD panels. The solder mask was replaced by ZIF for the RMD resist layer due to the lower stiffness of the latter. Lamination was done using the same process described in the section on dielectric lamination. The panels were then sent to Micron Laser Tech to laser drill holes in the ZIF up to the dog-bone pads. Plasma etching was done after this step to remove any ZIF residue from the surface of the exposed copper pads.

3.2.5 Ball Attachment and Dicing

Collaboration was established with Nanium, a company specializing in wafer-level technologies, for BGA balling by ball drop at panel-level and singulation.

3.2.5.1 Fiducial preparation for BGA ball attachment

As mentioned in the previous chapter, each panel has a 3x3 array of plated copper fiducials at each corner for balling and dicing alignment (Figure 39). These copper pads were exposed by opening 75 μm diameter holes in both NSMD and RMD passivation layer processes. Due to non-uniform plating over the panel surface, i.e. edge effects resulting in thinner plating on the corners and edges as compared to the center, copper patterns near the corners and edges were over-etched. As a result, there was not enough contrast between the exposed copper fiducials and the surrounding resist for recognition by the automatic production line printer used for flux printing and ball drop at Nanium.

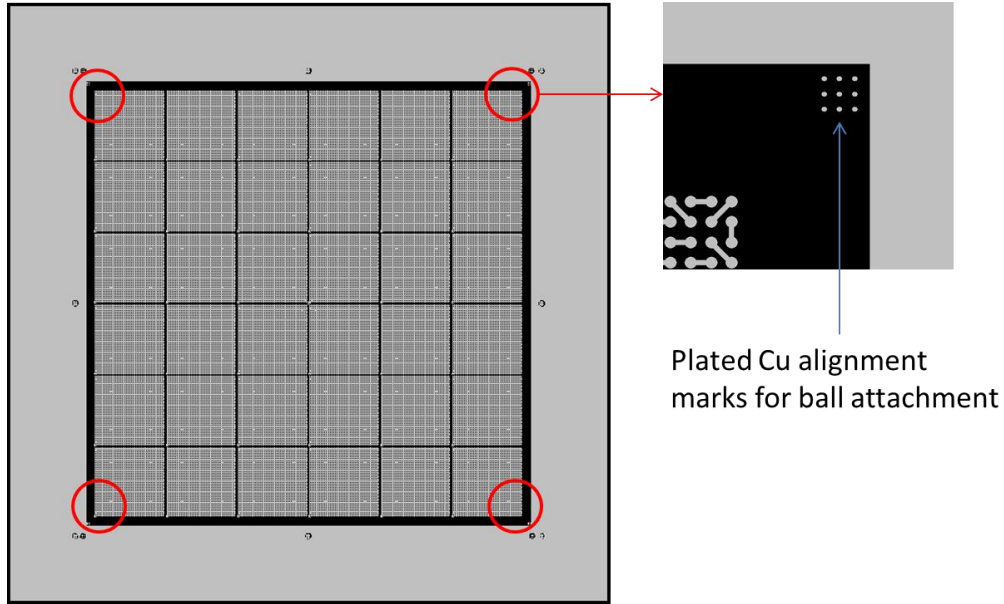


Figure 39: Alignment fiducials for ball attachment

To solve this issue, the passivation openings at these locations were first enlarged to a diameter of 110 μm and drilled deeper through all polymer layers on both NSMD and RMD panels. The holes were then filled with white water-based opaque enamel. The increased depth of the holes enabled proper filling with the enamel paint. White paint was used to provide enhanced contrast with the passivation layers. The panels were left to dry overnight and then baked at 150 $^{\circ}\text{C}$ for 1 hour. The surface of the fiducials was then fine polished to remove the excess enamel material.

3.2.6 Critical aspects of fabrication and process improvements

The processing challenges listed in Table 11 were observed in the initial fabrication cycle. Analysis and solutions to these challenges are proposed to be implemented in the next fabrication cycles.

Table 11: Processing challenges and possible solutions

Process Step	Issue	Reason	Solution
Electro-less plating	Cu delamination (blisters) after annealing at 120 °C	<ol style="list-style-type: none"> 1. Internal Stress in Cu 2. Insufficient de-smear treatment (process was developed for a ZIF build-up) 	<ol style="list-style-type: none"> 1. Reduce Cu thickness to reduce internal stress 2. Gradually ramp temperature up and down during anneal 3. Increase de-smear time
ENEPIG Surface Finish	ENEPIG plating seen on ZIF outside of the dog-bone area (Figure 4)	Residual Pd on ZIF surface (left over from the electro-less plating step) is attacked by the Nickel plating solution	Increased Pd etching, difficult since etching solution also etches copper



Figure 40: ENEPIG plating onto the ZIF surface surrounding the NSMD copper pads

3.3 Yield of Fabrication Cycle I

Table 12 lists a summary of all the panels fabricated during the first fabrication cycle with their design specifications. At least one panel was assigned to each fabrication/assembly variation for each of the three interposer materials.

Table 12: Summary of Cycle I interposer panels

	Thickness	Size	RMD	NSMD	NSMD+collar
Low CTE glass	150 μm	6in x 6in	P1	P2	P3
High CTE glass	150 μm	5.5in x 5.5in	P4	P5	P6, P10, P13
Silicon	200 μm	6in x 6 in	P7	P8	P9
Trials (Glass) Used for balling and singulation trials	180 μm	6in x 6in	T1	T2	

3.3.1 BGA balling and dicing trials on glass panels

Glass panels T1 and T2 were intended for process trials, down to balling and singulation. As the passivation process was not yet optimized, it was decided to only use these panels for mechanical dicing trials and edge quality evaluation. Interposer singulation was carried out successfully with no micro-cracks on the coupon edges

(Figure 41) or within the substrates themselves (Figure 42) observed by C-SAM analysis and SEM edge observation.

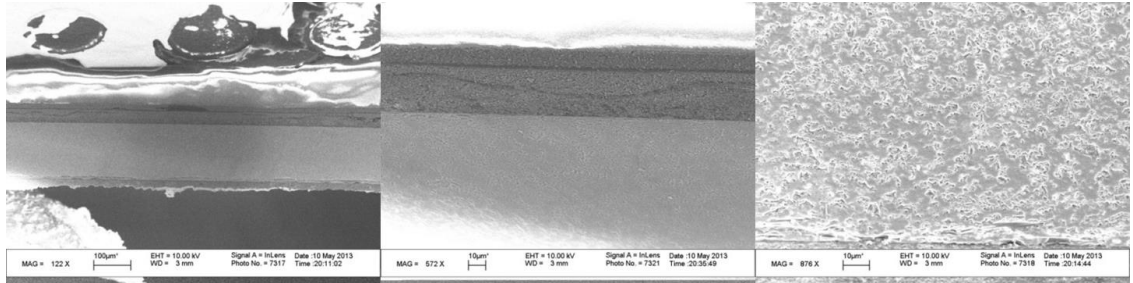


Figure 41: SEM images of the edge of the singulated glass interposer coupons, showing a very smooth surface

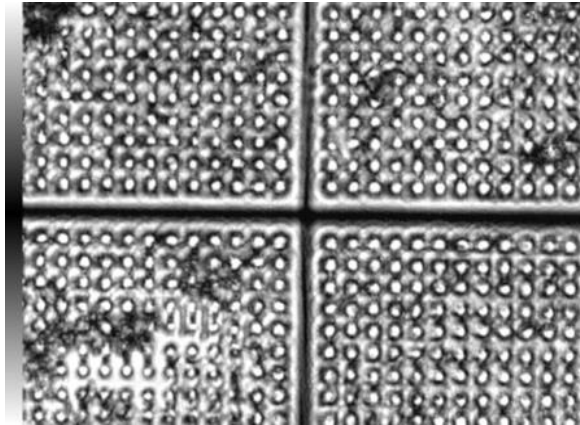


Figure 42: C-SAM imaging of interposers after dicing showing no cracks in the singulated coupons

3.3.2 Silicon Panels

It was initially intended to fabricate and characterize silicon interposers to benchmark their reliability performance against the glass interposers (or the other way around benchmark the glass interposer against the Si interposer). However, panels P7, P8 and P9 cracked during the high temperature/pressure RXP-4M lamination process. The

highly brittle nature of the poly-silicon panels made them incompatible with this lamination process. As the polymer lamination process is not compatible with Si panels, it was not possible to fabricate Si interposers with the same build-up as the glass ones.

3.3.3 Yield evaluation of glass panels and reliability DOE plan

The yield of the fabricated glass interposers was evaluated after BGA balling and singulation. Considering the yield, a DOE plan for preliminary evaluation was then established and discussed. All panels from the first fabrication cycle were fabricated with high-CTE glass.

3.3.3.1 NSMD balling yield

As a result of the exposed trace area in the NSMD pad design (Figure 43), and considering that the pitch was $400\ \mu\text{m}$ for $250\ \mu\text{m}$ diameter solder balls, the risk of solder bridging during the ball attachment process was high.

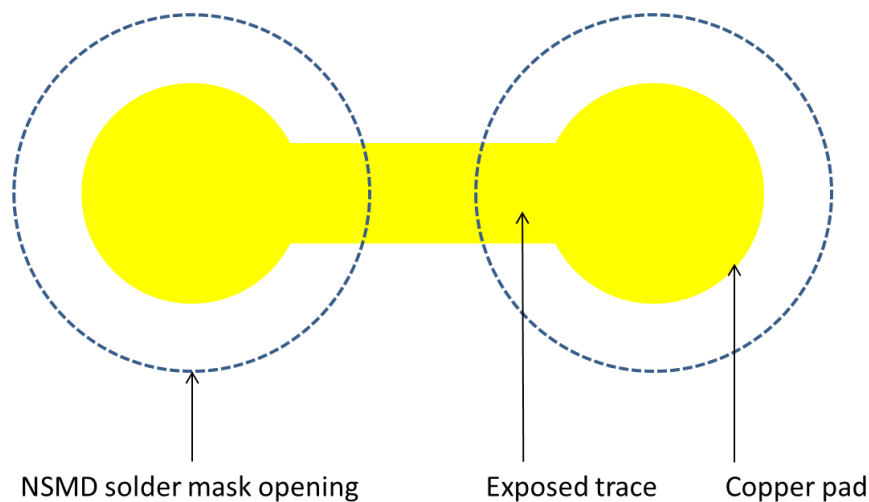
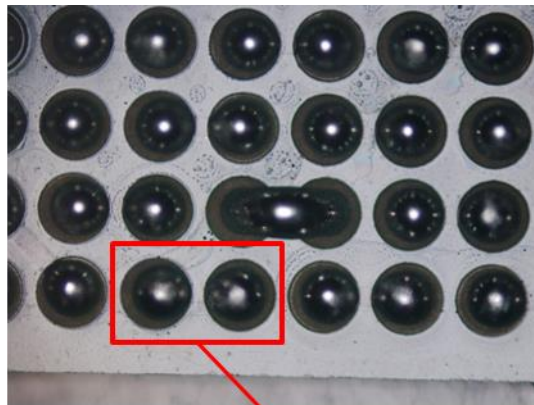


Figure 43: Exposed traces in NSMD design

The ball attachment process involved stencil printing of flux material followed by ball dropping onto the pads. Since the exposed trace was plated with ENEPIG surface finish and most likely covered by flux, it provided good solder wettability. As a result, major solder bridging was seen on some NSMD panels (Figure 44). Nanium was able to optimize their ball drop process for two panels (Table 13), allowing for well yielded interposer coupons for reliability testing. 16 well yielded coupons were selected for preliminary tests with and without the polymer collar.



Pitch < 400um due to exposed trace

Figure 44: NSMD ball bridging

Table 13: NSMD balling yield

Panel #	Observed Issues in ball attachment step	Comments
P6, P13	Major solder bridging	Used for balling process optimization
P10	Limited bridging	Process with optimized parameters
P5	No bridging	Processed with optimized

		parameters
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3.3.3.2 RMD balling yield

In the RMD design, only the landing pad is exposed which is beneficial for balling yield. Indeed, the RMD panel processed at Nanium showed no solder bridging and had high interposer coupon yield. As before, the 16 best samples were chosen for reliability testing with and without the polymer collar.

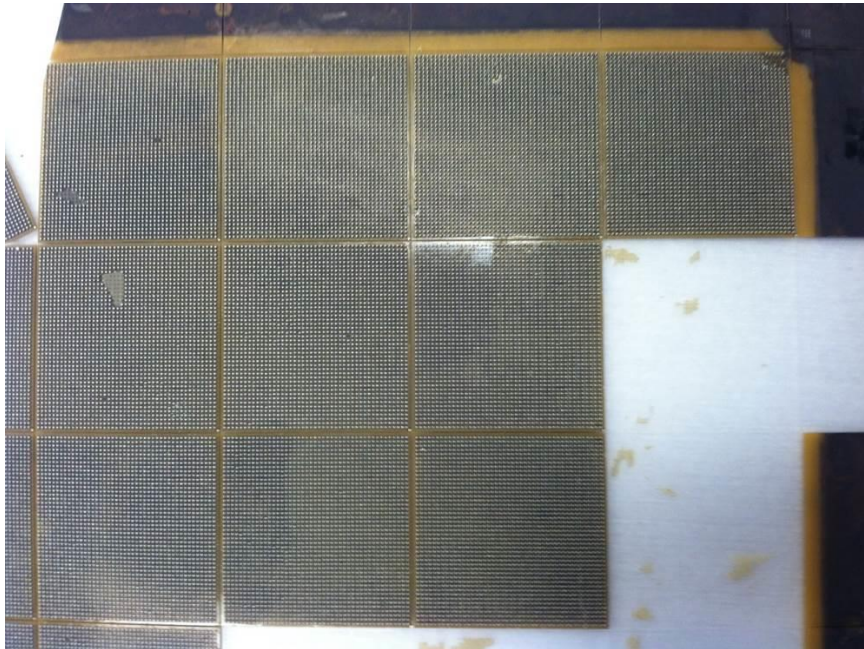


Figure 45: No bridging seen on the RMD panel after ball attachment

3.3.3.3 Evaluation of ball shear strength

Solder ball shear tests following JESD22-B117A are an industry standard used to assess the ability of solders to withstand shear forces that may be experienced during

manufacturing, testing, transport, and end-use. This test is destructive and applied prior to end-use assembly.

All samples were sheared through the ball (Figure 46), indicating a robust ball attachment process.

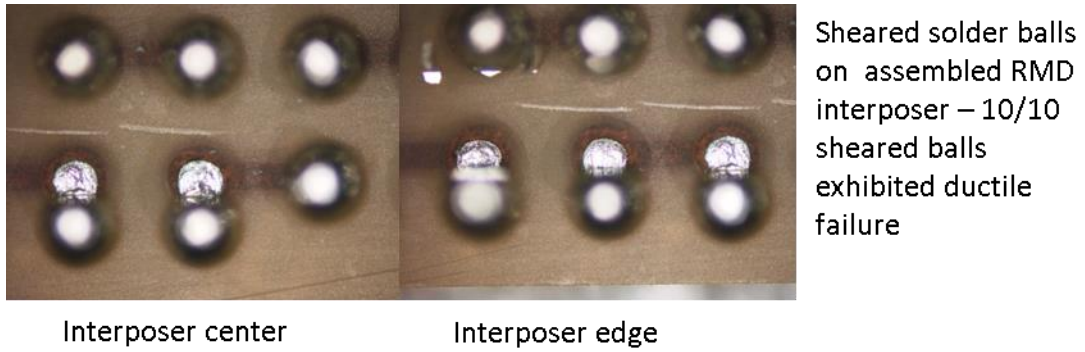


Figure 46: Shear testing on balled interposers resulted in ductile shears indicating good ball attachment

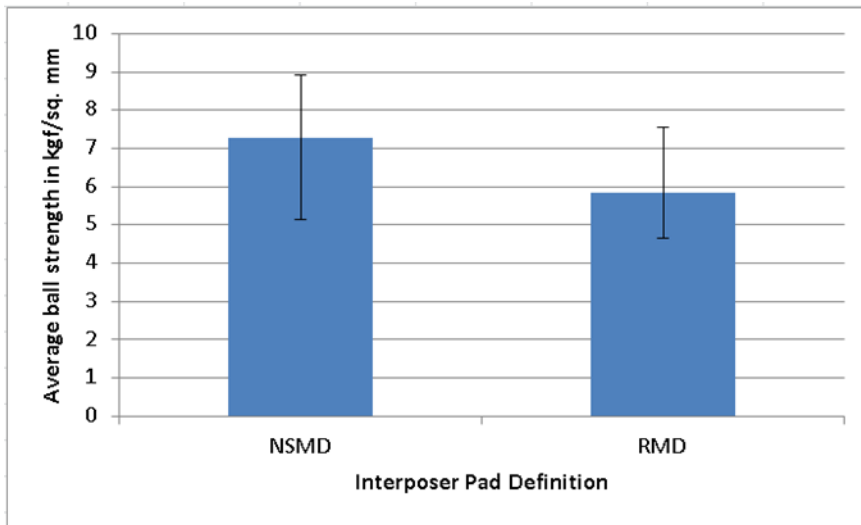


Figure 47: Measurement of average ball attachment strength for NSMD and RMD coupons subjected to the ball shear test

3.4 Conclusions

Glass panels were fabricated following NSMD and RMD design rules. With processes being in a developmental stage, a few issues were found which are detailed with proposed solutions. Inspection was done at every stage of processes to ensure the quality of processing. Lower yield samples were set aside for polymer collar and assembly process development while high yield samples were used for reliability testing.

CHAPTER 4

POLYMER COLLAR PROCESS DEVELOPMENT

This chapter describes the process of creating polymer collars around the solder balls on 7.2 x 7.2 mm and 18.4 mm x 18.4 mm glass interposers. The collar application process by spin-coating was discussed first. Various process options for removing the polymer residue on the solders were explored and compared. The role of key process parameters in minimizing solder residue is discussed, followed by recommendations for the front-up approach. The solder-pad interfaces with and without polymer collars are compared at the end of the chapter.

4.1 Collar Application and Assembly Process Flow

4.1.1 Collar Application Process

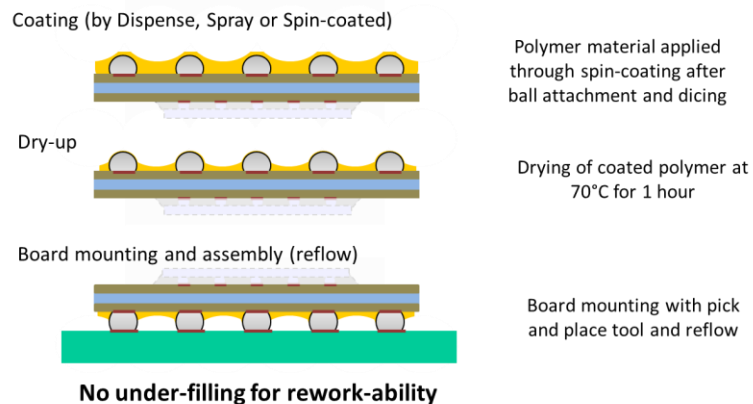


Figure 48: Polymer collar application process

An epoxy underfill without fillers (NAMICS XXXX) is spin coated onto the balled side of diced interposers (Figure 48) as the collar material. The interposers are then dried in an oven at 70°C for an hour to evaporate the solvent content. Drying is performed below the curing temperature of the collar material. Flux is dispensed onto the test PCBs. The interposers are then picked and placed onto a PCB panel using a Finetech Matrix flip-chip bonder with a 20 mm x 20 mm gimbal tool to accommodate 18.4 mm interposers. They are then batched reflowed in a reflow oven at 260°C peak temperature.

4.1.1.1. Spin Coating on square substrates

When spin coated, the corners of the substrate experience increased air friction, leading to a higher evaporation rate in these regions. The resin at the corners therefore dries up and impedes the fluid flow of the material being driven outward by centrifugal forces. This mechanism leads to build up of material at the corners (Figure 49).

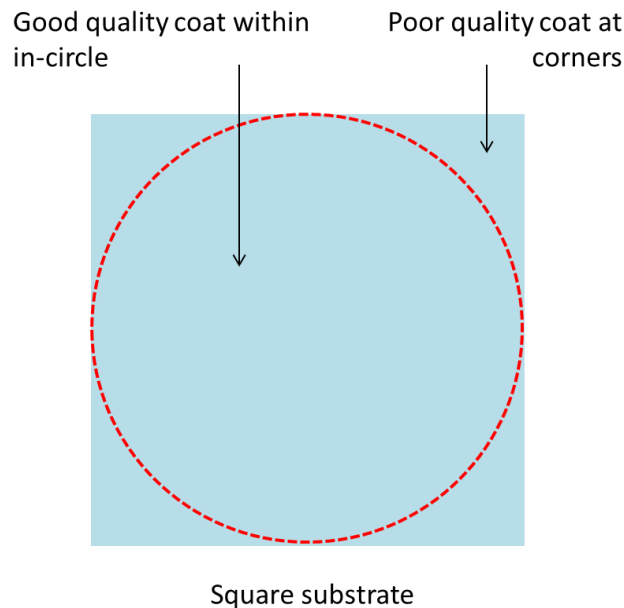


Figure 49: Material build-up at substrate corners during spin coating

Material properties enforce a constant contact angle at the solid-liquid-gas interface at the edges of the substrate (Figure 50). Since the substrate periphery experiences higher air friction and therefore dries faster, the outward moving material flows over this bead and dries, enhancing the effect.

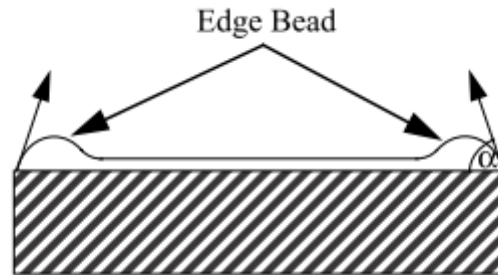


Figure 50: Edge bead effect [14]

4.1.1.2. Polymer collar application on 7.2 mm interposers

The polymer collar material is spin coated onto 7.2 mm interposers for 30 seconds. Three different coating speeds, 1000, 2000 and 3000 rpm were used in order to characterize the variation of polymer thickness with speed. The height of the deposited material was measured from the surface of the interposer at two locations, between and on the side of the solder ball (Figure 51). Cross sectional images of the deposited collar and height measurements of the same are reproduced in Figures 52 and 53. These cross-sections and measurements were made after drying the material and free reflow of the interposers. The relatively small size of the 7.2mm substrate and its closer approximation to a uniform circular substrate led to uniform deposition of the material. As can be seen from the collected data, the height of the deposited collar after drying is uniform. Measurements were taken from at peripheral and central solder balls and the maximum measurement variation is below 10%.

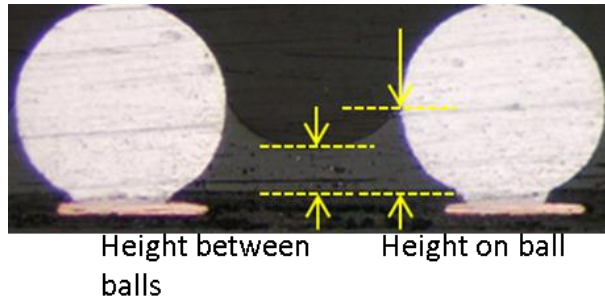


Figure 51: Measurement locations for collar height

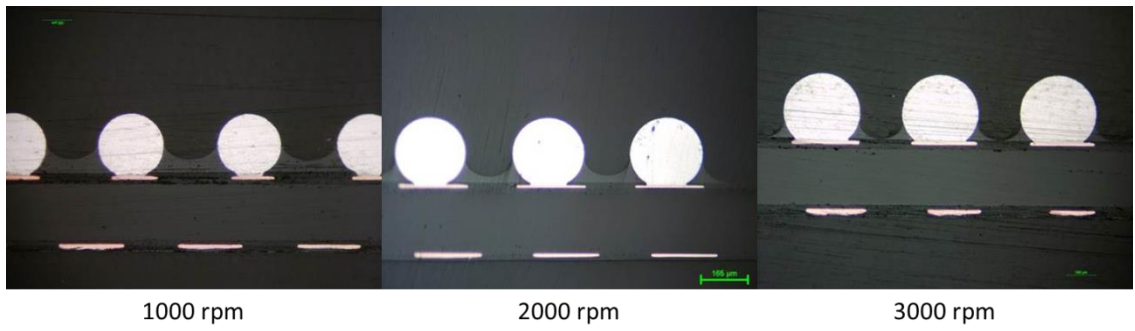


Figure 52: 7.2mm interposer with polymer collar cross sections at 1000, 2000 and 3000 rpm

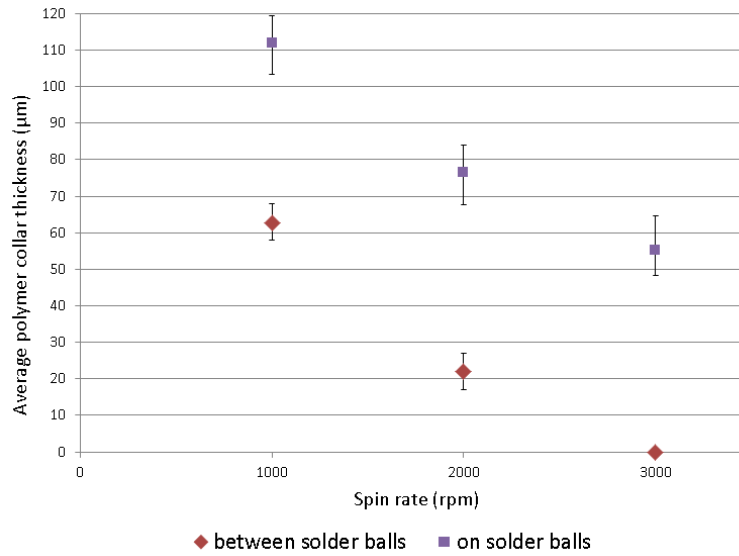


Figure 53: Deposited material thickness on 7.2 mm interposers for different spin rates

4.1.1.3 Polymer collar application on 18.4 mm x 18.4 mm interposers

The larger 18.4 mm interposers posed a problem due to their shape being a further deviation from that of an ideal circular substrate. Initial trials using the process steps applied to the 7.2 mm interposer resulted in highly non-uniform deposition around the periphery and across the interposer.

Two enhancements to the process resulted in a solution to this issue. Dummy interposers were placed around the test interposer (Figure 54) to simulate a larger substrate size. This eliminated the edge bead effect as well as the corner effects for the test interposer.

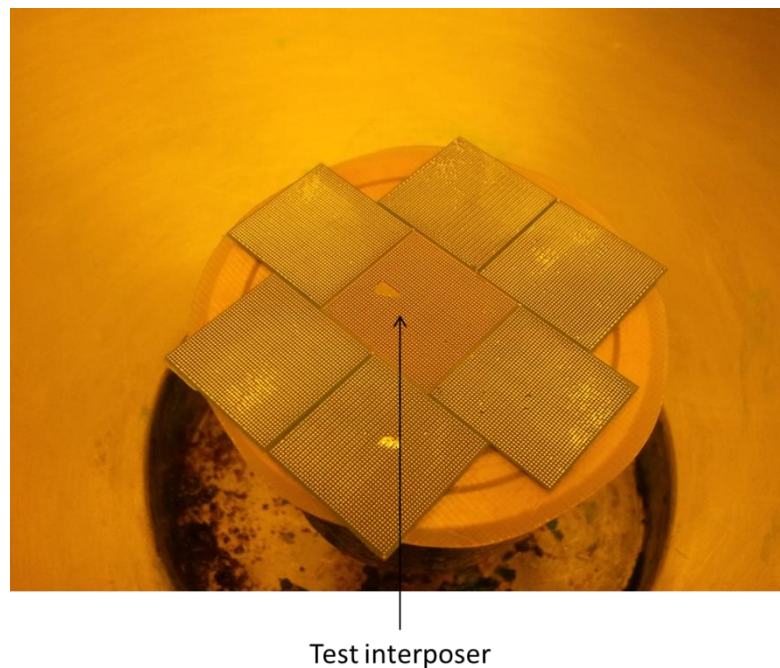


Figure 54: Simulation of a larger substrate for uniform coating

In addition, the coating profile was modified to include spreading and uniformity phases, to allow the material to deposit uniformly over the surface of the test interposer.

Cross sectional images of the deposited collar, and the heights resulting from the modified process are reproduced in Figures 8 and 9. In the case of the larger interposers, maximum variation in coated height was larger at about 20%. This value indicates that process optimization could still be done to obtain a more uniform height.

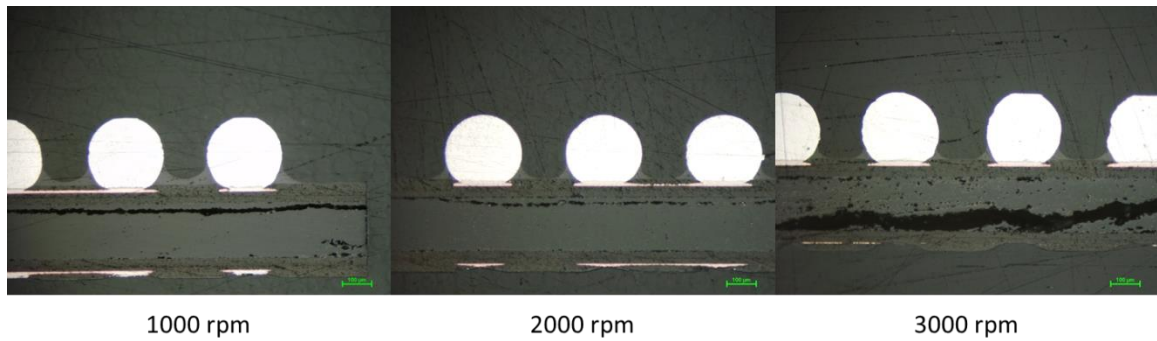


Figure 55: 18.4 mm interposer with polymer collar cross sections at 1000, 2000 and 3000 rpm

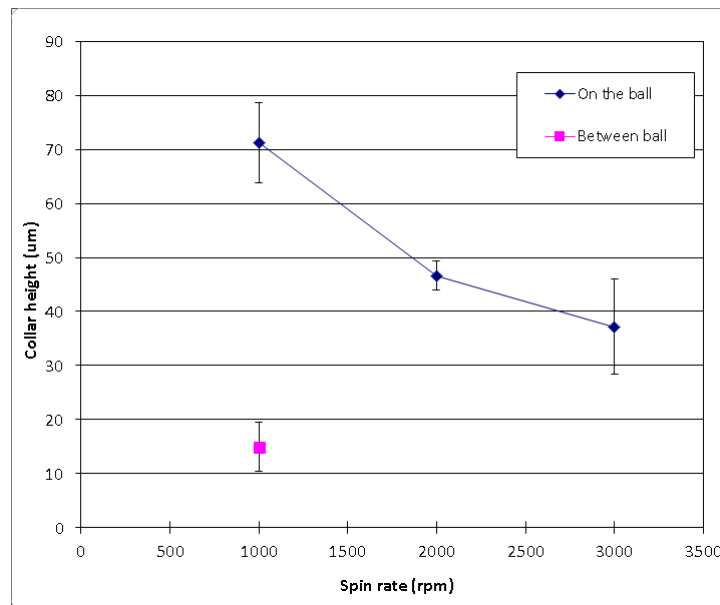


Figure 56: Deposited material thickness on 18.4 mm interposers for different spin rates

4.2 Polymer Residue – Issues for Manufacturability

As a result of the spin coating process, a thin layer of polymer material was expected to be found on the surface of the solder balls (Figure 57). The presence of this residue was detected and confirmed through SEM imaging before and after the coating process (Figure 58). The material was designed to melt during reflow so as to ensure formation of a reliable solder joint.

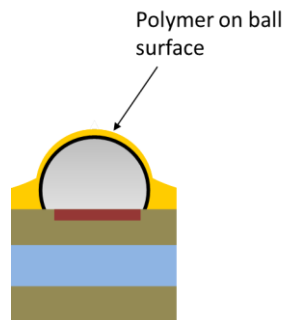


Figure 57: Polymer residue on the ball surface.

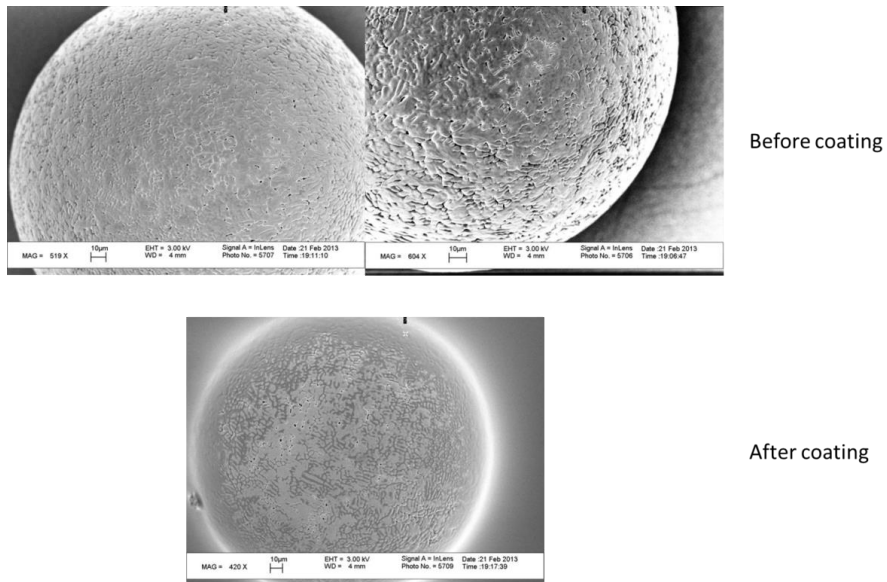


Figure 58: SEM confirmation of the residue on ball surface

4.2.1 Residue removal methods

This sub-section details the three approaches used to remove the polymer residue on the surface of the balls: 1.)Plasma etching, 2.)Sand-blasting and 3.)Solvent wipe cleaning.

4.2.1.1 Plasma etching

The first approach to remove the polymer residue was plasma etching. The conditions used for this process are listed in Table 14. The results of this approach are summarized below.

Table 14: Plasma etching conditions

Parameter	Condition
Composition	CHF ₃ (10 sccm) / O ₂ (50 sccm)
Pressure	10 mtorr
Power	300 W
Time	15 and 30 minutes

3D microscopy was used to measure the profile of the solder ball before and after 15 minutes of plasma etching. The side profiles (Figure 59) show that while the ball looks rough right after spin coating, after etching it is much smoother, indicating removal of the residue from the ball surface. However, it can be seen from these images that the collar around the base of the ball was also etched in the process.

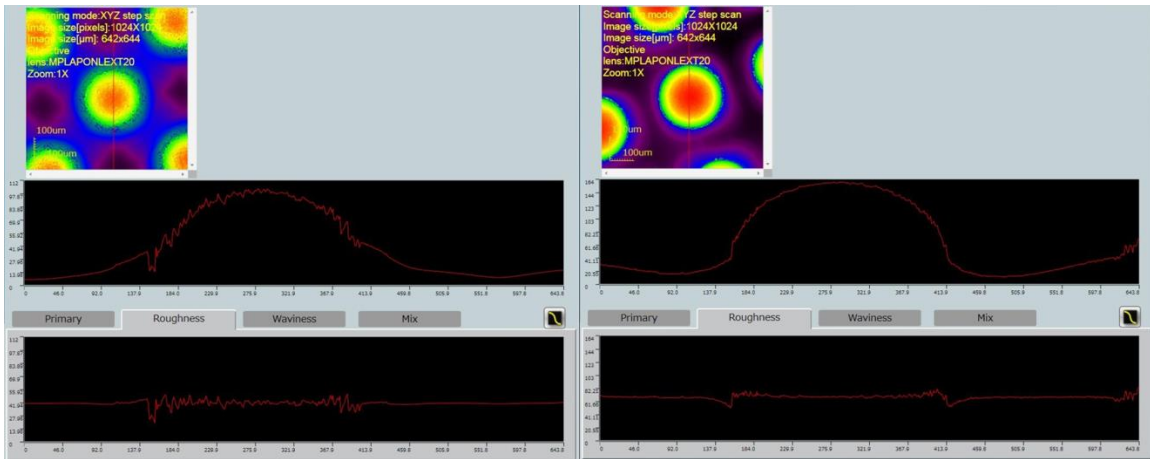


Figure 59: Side profile of solder ball before (left) and after (right) 15 minutes of plasma etching

SEM imaging was then conducted on the samples to examine the surface of the balls in order to confirm this result. Figure 60 shows the top surface of the solder ball before and after 30 minutes of etching at low magnification.

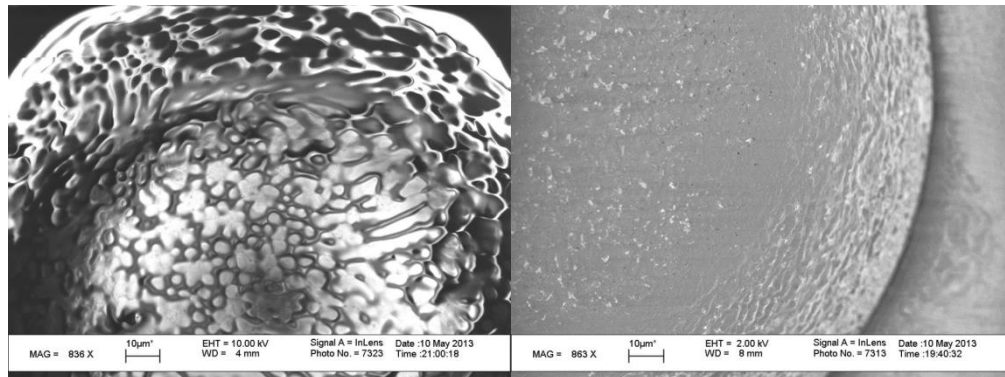


Figure 60: Ball surface before (left) and after (right) 30 minutes of plasma etching

Imaging at higher magnification (Figure 61) compares the surface of the ball after 15 and 30 minutes of plasma etching. While the residue seems to have been almost completely removed after 30 minutes, (comparing to Figure 58) it must be noted that the increased etching time would have removed more of the collar material. The possible

alteration caused to the microstructure on the surface of the ball after etching is not acceptable by industry standards.

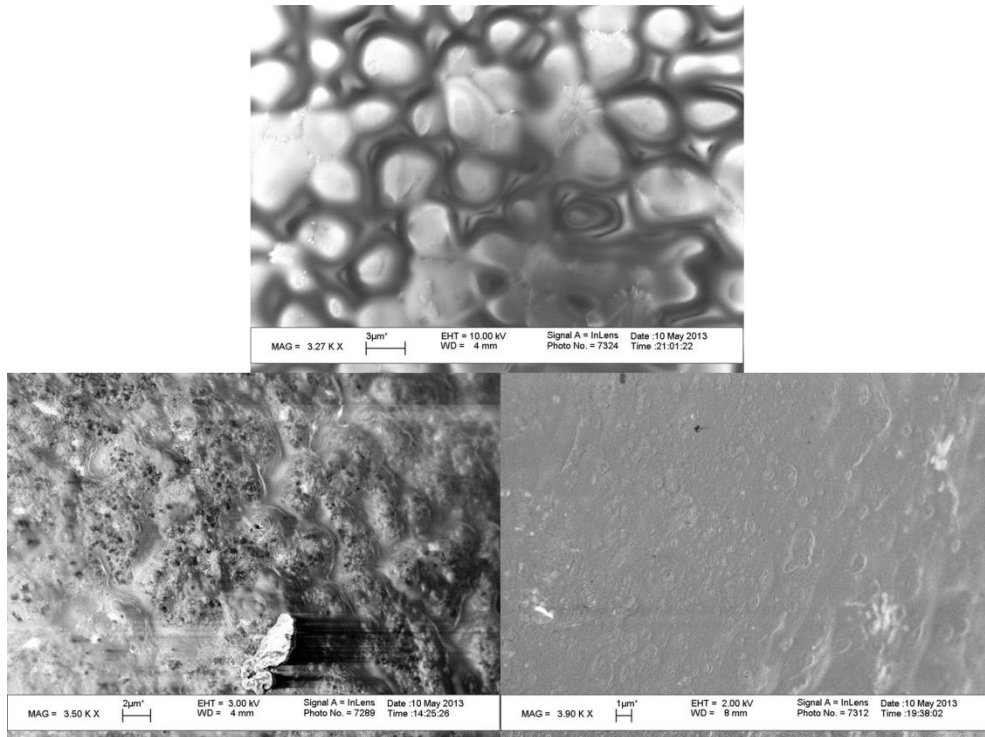


Figure 61: Ball surface before (top) and after 15 minutes (bottom left) and 30 minutes (bottom right) of plasma etching

3.2.1.2 Sand Blasting

The second approach explored to remove polymer residue was sand blasting of ball surface. The experimental setup used to evaluate this method is detailed in Table 15.

Table 15: Sand blasting experimental setup

Medium/grain diameter: pumicite / 250 μm	
Pressure	30 psi

Time (seconds)	10,20, 30
Medium/grain diameter: pumicite / 35-75 μm	
Pressure	25 psi
Time (seconds)	5, 10, 30

In the trials with 250 μm pumicite, the solders balls suffered serious damage at all three durations (Figure 62). In the case of some samples, the interposer itself cracked. This trial was found to be too harsh and therefore, a smaller grain size was chosen for the next trial.

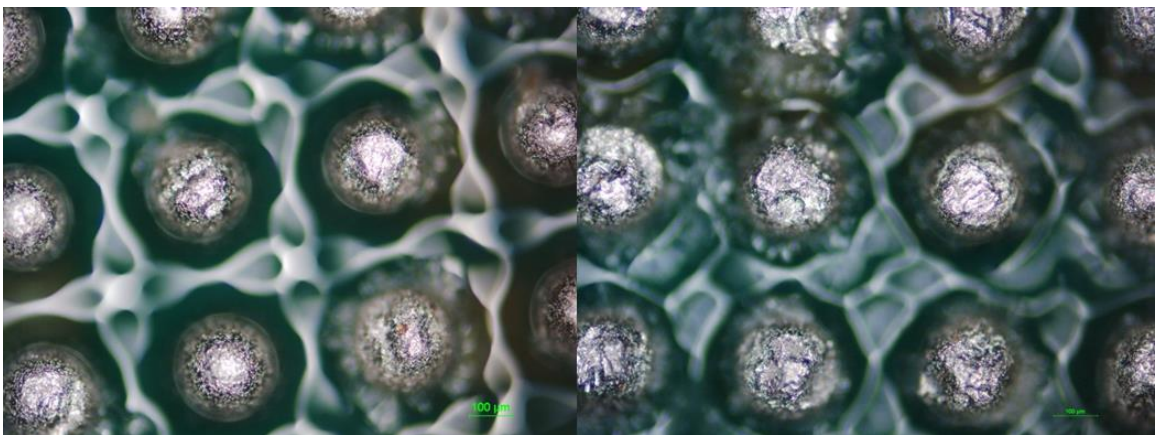


Figure 62: Damage on solder ball surface after 5 sec (left) and 30 sec (right) of sand blasting with 250 μm diameter pumicite

In trials conducted with 35 μm diameter particles, the surface of the solder ball was not damaged when blasted for 10 seconds. However, damage did occur at 20 and 30 seconds (Figure 63). In all three cases, however, it was found that the pumicite got embedded in the polymer material (Figure 64).

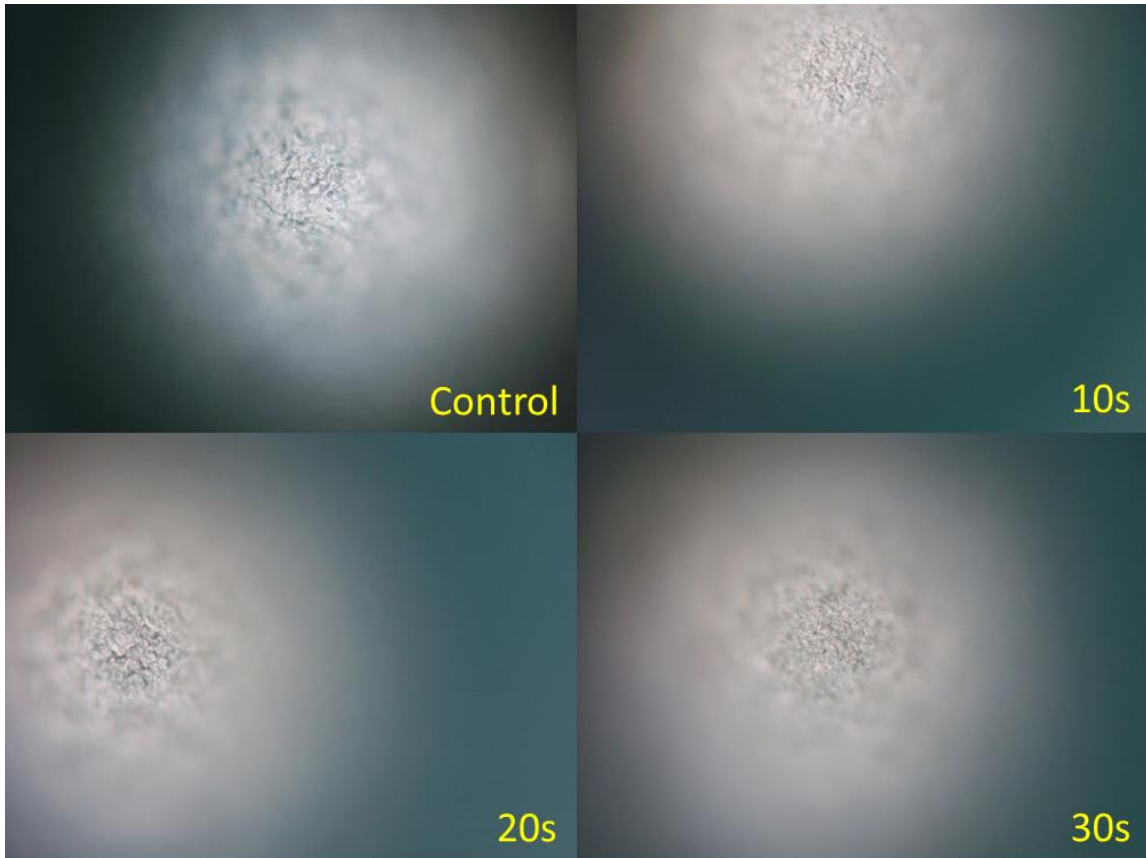


Figure 63: Close up of ball surface with 35 um sand blasting

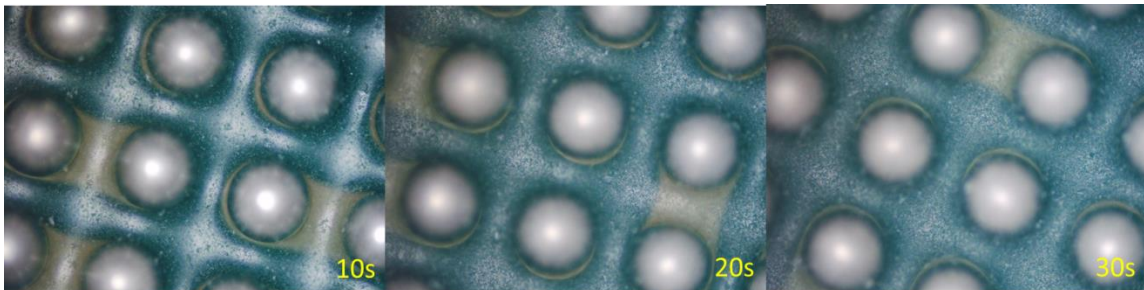


Figure 64: Pumicite particles embedded in collar material

While sand blasting was seen to remove the residue from the surface of the ball, it proved to be a very hard process to optimize. Damage to the ball surface and embedding of pumicite particles are also major issues that prevent it from being used as a manufacturable process for residue removal.

3.2.1.3 Solvent Wipe Cleaning

The third approach to remove the polymer residue from the top surface of the solder balls was to wipe the top surface of the balls right after the polymer drying stage with a Texwipe cleanroom wipe dipped in acetone. Since the polymer material is not cured at this stage, the residue is easily removed (Figures 65).

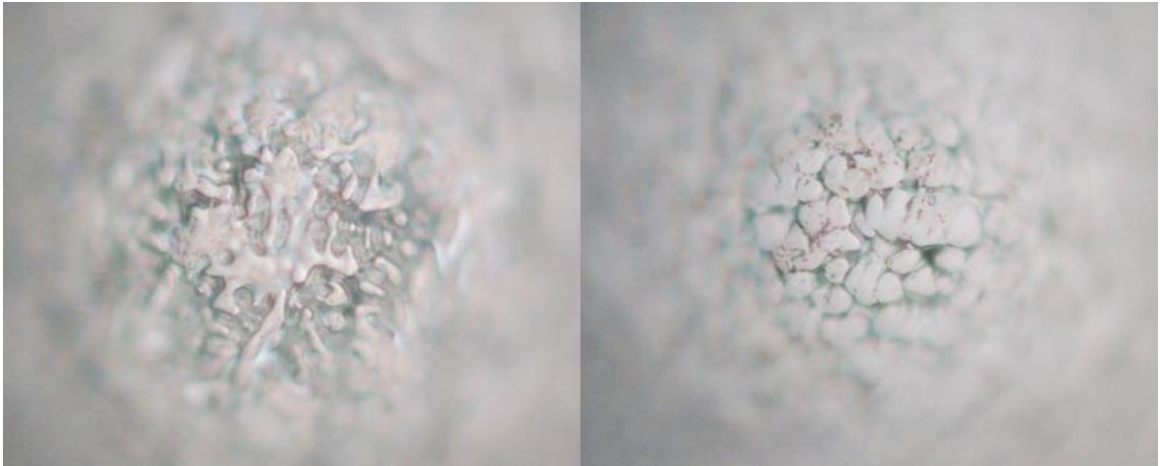


Figure 65: Close-up of the surface of a ball before (left) and after (right) solvent wipe cleaning

The solvent comes in contact with only the top surface of the ball. Therefore, the material deposited between the balls is unaffected, leaving the collar intact (Figure 66).

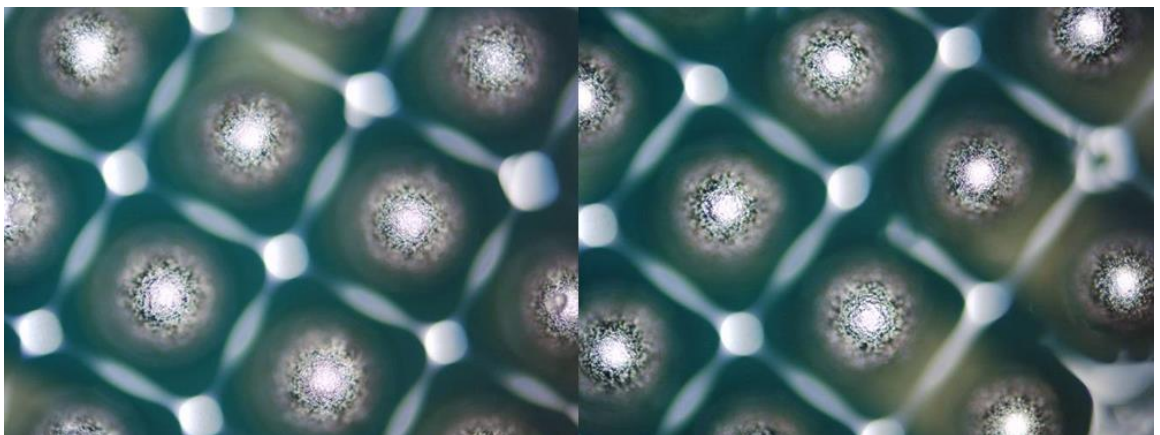


Figure 66: Top surface of balls before (left) and after (right) solvent wipe cleaning.

Comparing the three approaches for residue removal, it may be concluded that the solvent wipe cleaning seems to efficiently remove the residue with negligible damage caused to the collar itself. This process can be efficiently implemented by dipping the balls in acetone and then IPA using the same infrastructure used for flux dipping prior to assembly.

3.2.2 Interface analysis for interconnection yield

To study the effect of the polymer collar on IMC formation, samples were assembled, cross-sectioned and imaged. No difference in the IMC formation was observed with and without polymer residue (Figure 67). It was concluded that polymer residue will not affect interconnection yield.

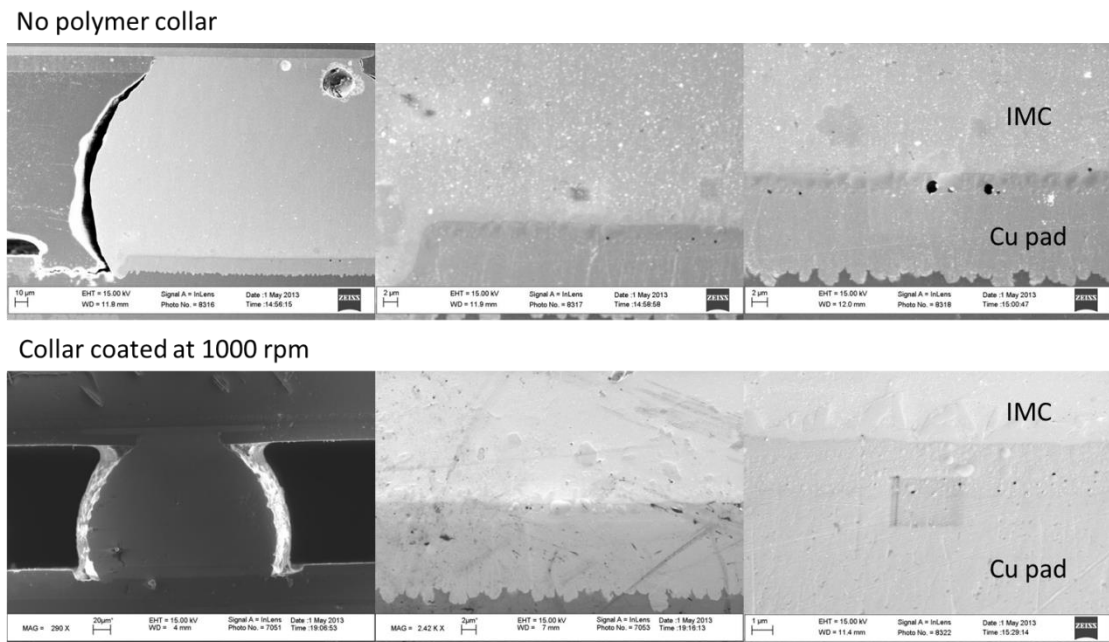


Figure 67: Interface analysis with and without polymer collar

3.2 Conclusions

A manufacturable process for polymer collar application was developed for large body size interposers. It was found that the collar material has no negative effects on assembly yield. Methods for the removal of polymer residue from the surface of the ball were explored and an industry compatible solution is presented.

CHAPTER 5

LARGE BODY SIZE INTERPOSERS ASSEMBLY FOR RELIABILITY

This chapter describes the SMT assembly of 7.2 mm x 7.2 mm and 18.4 mm x 18.4 mm glass interposers or packages described in Chapter 3 and 4. Two assembly fabrication cycles were conducted – one with printing and the other with solder ball attach and tacky flux. After discussing the fabrication process flow, details on the fabrication yield from each of the cycles is provided. The chapter this demonstrates the assembly of the large low CTE packages with the novel low-stress SMT-compatible board-level interconnection approaches.

5.1 Assembly process development

There are two approaches for ball-attached SMT compatible package BGA to board assembly (Figure 68), using solder paste or tacky flux on the PCB side. The polymer collar material does contain a fluxing agent, however, the BGA on the interposer still needs to tack to the board. Additionally, incorporating a similar reflow profile for assembly both with and without collar allows for a more definitive comparison. This section details results of assembly with the two approaches and an analysis of the same. The approach most suitable to our application is selected for the assembly of samples for reliability

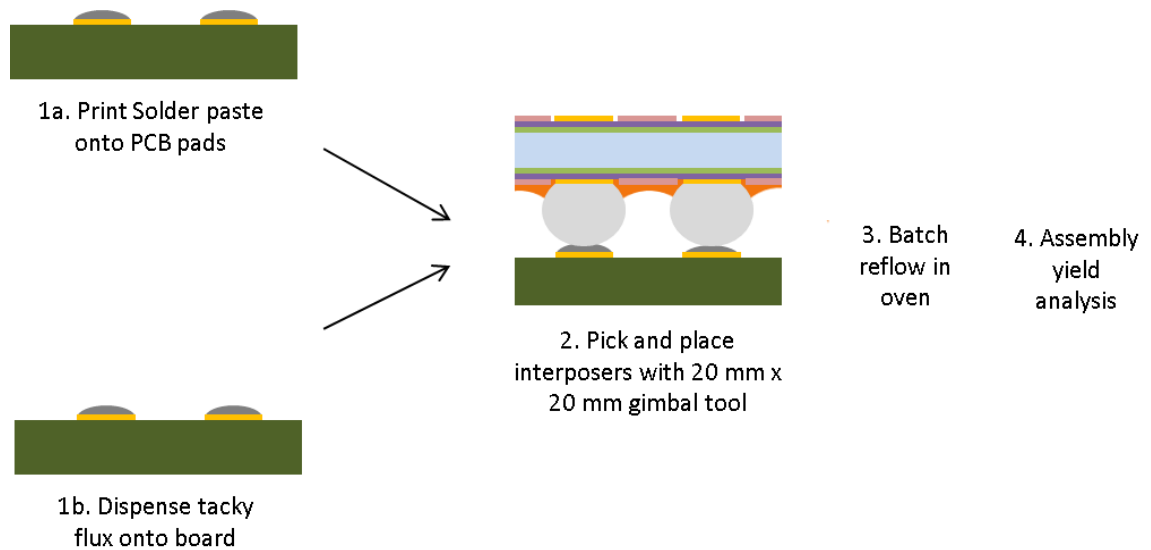


Figure 68: Two major approaches to package-to-board assembly

5.1.1 Assembly with solder paste

Assembly was first attempted using solder paste printing on to the board due to unavailability of the tacky flux for lead free solder applications. A thin (check how thick the stencil is – should be mentioned in mils) layer of SAC105 solder paste (AMTECH CHIPQUIK LF-4300 with grain size of 15-25 μm) was first printed onto the PCB using a patterned stencil aligned on the board, with round openings 230 μm diameter. Interposers were then pick and placed using the semi-automatic Finetech Matrix flip-chip bonder with a 20 mm x 20 mm vacuum-locked gimbal tool. The placement pressure was kept to a minimum to minimize spreading of the solder paste so as to prevent bridging. The boards were then reflowed in a reflow oven at a peak temperature of 260°C, to form a uniform joint between pad and interposer made from the solder paste and the BGA solder ball (Figure 69).

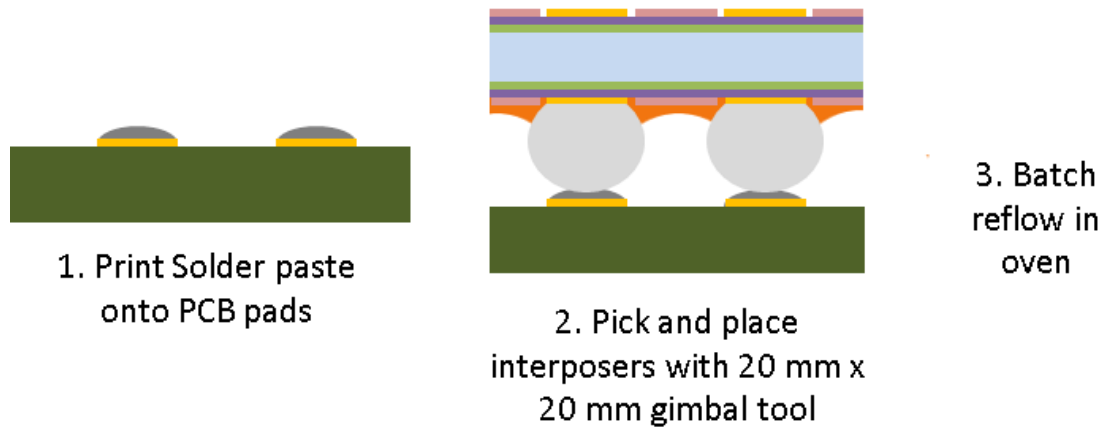


Figure 69: Interposer assembly using a solder paste based process

Samples assembled using this approach were x-rayed after reflow to determine the interconnection yield. Beading was observed between the interconnections, as can be seen in Figure 70, with beads from 5 μm to 30 μm . (please label the beading in the figure) This beading effect results from solder particles contained in the printed paste being dispersed on the board. This beading effect could only be observed with samples with polymer collar, especially in the case of a thick collar. The collar material melts at 100-110°C and tends to flow onto the PCB, displacing particles of solder paste that have not yet reflowed. With the solder paste, the solder particles are fairly small in size and easy to displace from their initial position, especially after interposer placement. This mechanism explains why exaggerated beading was seen on samples with thick collar. This effect will introduce additional reliability concerns, such as bridging, as these solder beads are free to move. As a result, an alternative method using tacky flux for placement was considered.

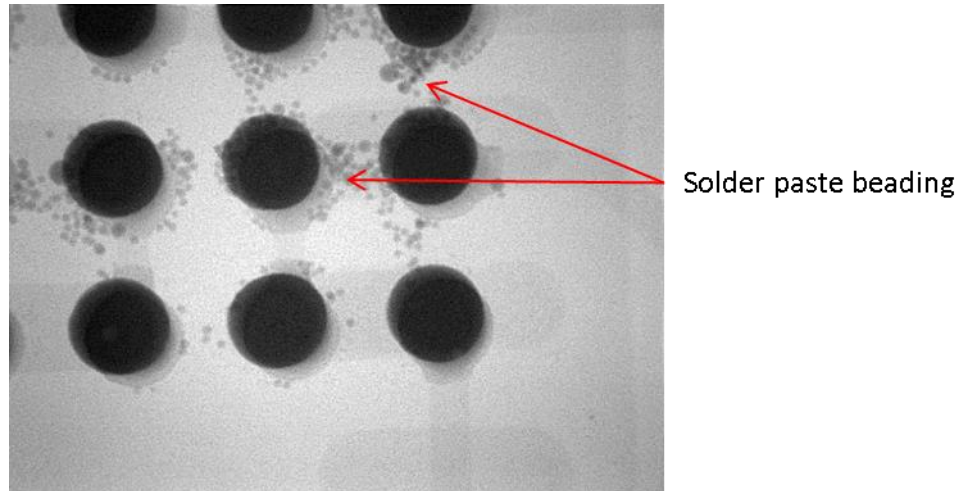


Figure 70: Solder paste beading after reflow of an assembly with thick collar

5.1.2 Assembly with tacky flux for lead-free applications

To avoid additional reliability hazards, the solder paste was substituted with tacky flux (Alpha NCX-FD) specifically developed for lead-free applications, which is still active at the peak reflow temperature of 260C (Figure 71). Ball-attached BGA packages were used for the assembly. The reflow conditions were optimized to match the recommended profile by the flux supplier (measured profile in Figure 72). Reflow conditions with flux had to be optimized to ensure proper wetting and limit solder ball voiding. Voiding up to 25% is acceptable by industry standards, but a much lower rate was achieved

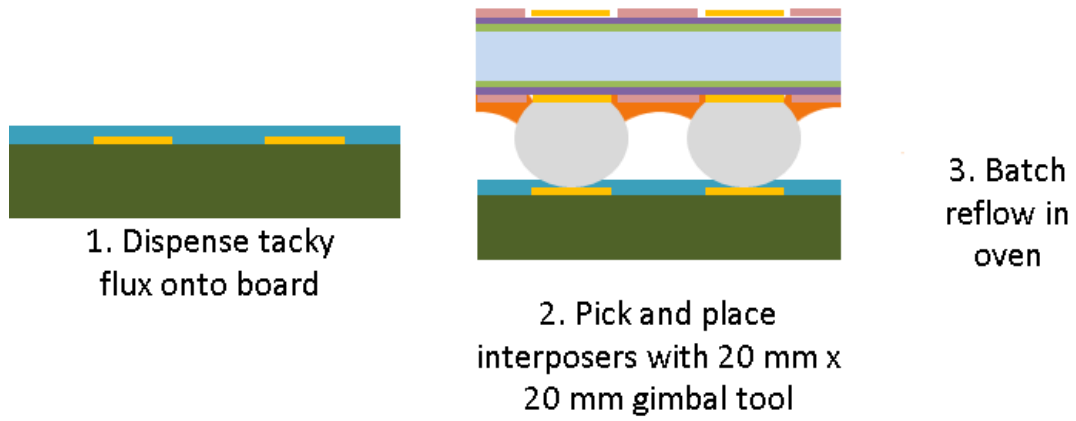


Figure 71: Assembly flow using a tacky flux based process

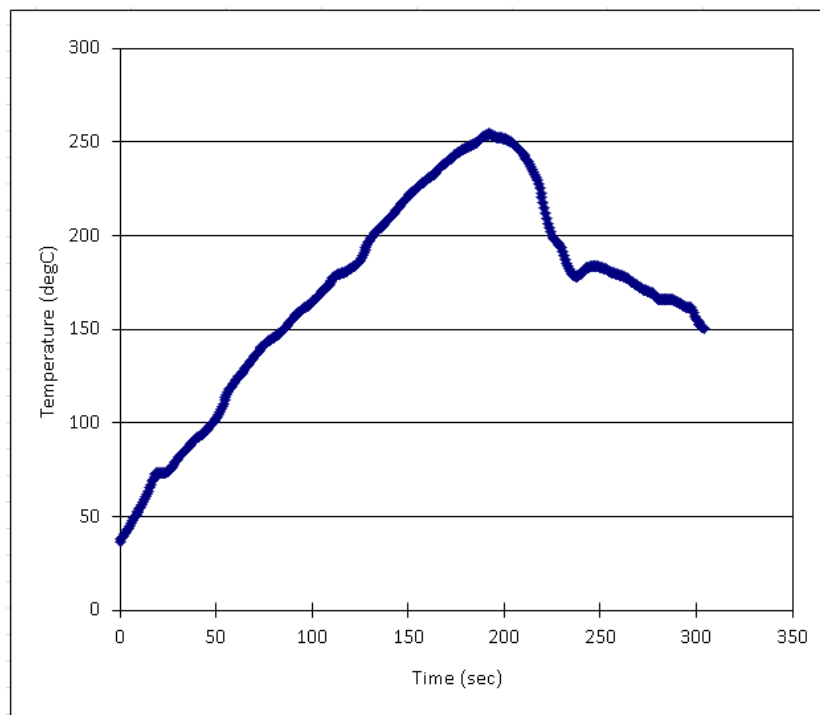


Figure 72: Measured reflow profile

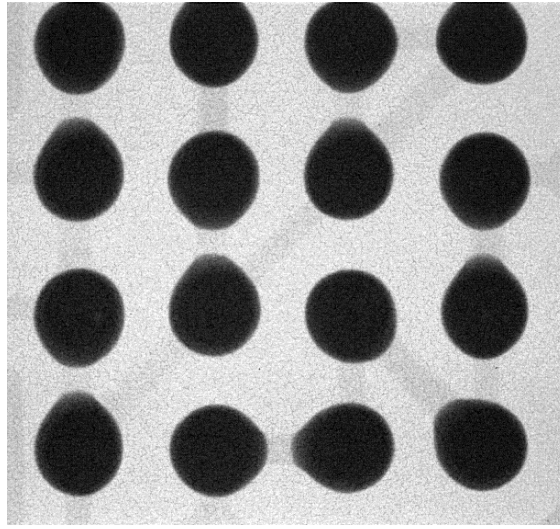


Figure 73: No beading seen with tacky flux based assembly

5.1.3 Assembly process evaluation

Process conditions for assembly with and without polymer collar were optimized based on trials with pre-fabricated 7.2 mm interposers. Assembly with flux and different collar heights confirmed good alignment and 100% yield.

Leakage of polymer collar onto the board can be observed in interposers assembled with the polymer collar (Figure 74). This occurs because the melting point of the collar material is lower than the reflow temperature and hinders reworkability. This phenomenon is most severe in the case of material coated at 1000 rpm due to the presence of largest amounts of material. Therefore, a compromise has to be made between buffering capability of thicker collar and board side leakage.

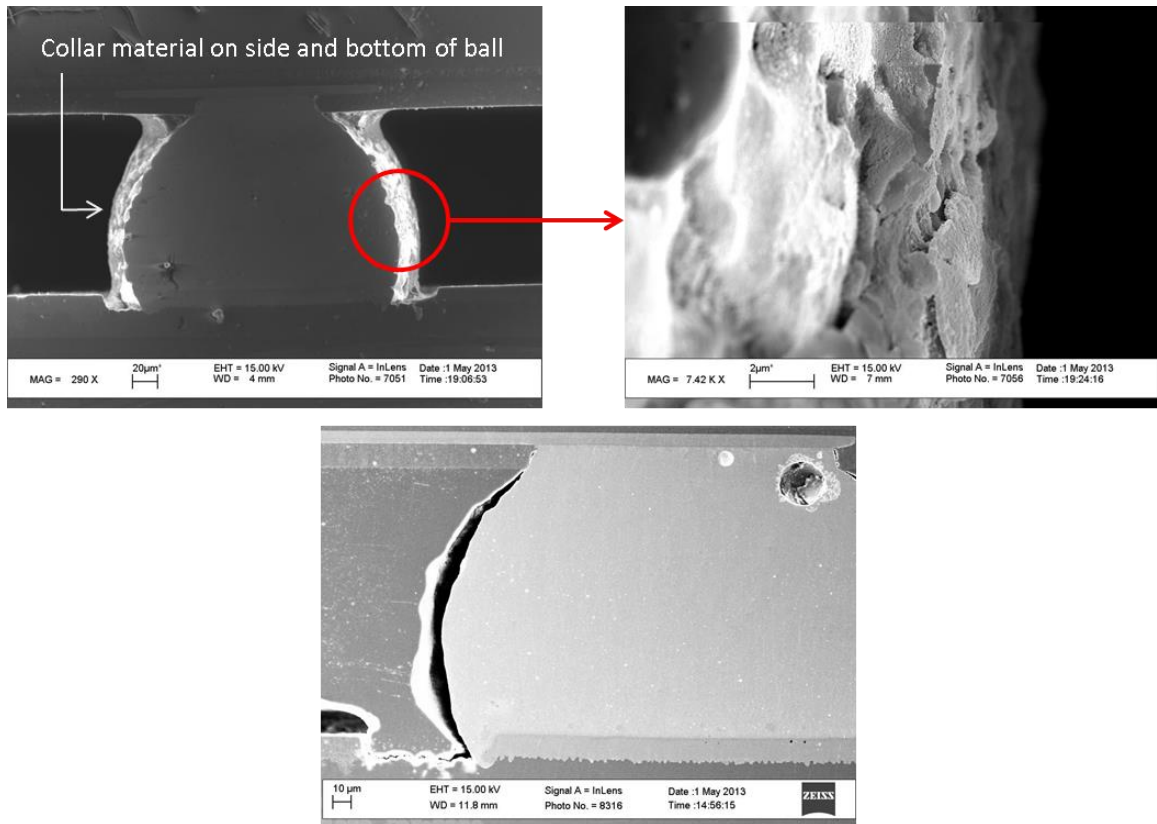


Figure 74: Leakage of material onto ball and PCB after assembly with 1000 rpm collar(top), solder joint without collar

5.1.4 Self-alignment of solder joints

Solder joints are advantageous in their ability to self-align during reflow, placing relatively low constraints on placement accuracy for a BGA pitch of 400 µm. An important consideration for assembly with polymer collar is the ability of the joints to self-align. This self-alignment capability was evaluated using the thickest possible collar, serving as the worst case scenario. Increasing states of misalignment were deliberately established during the placement of interposers onto the board. Samples were x-rayed before and after reflow to document the introduced misalignment and evaluate behavior after reflow.

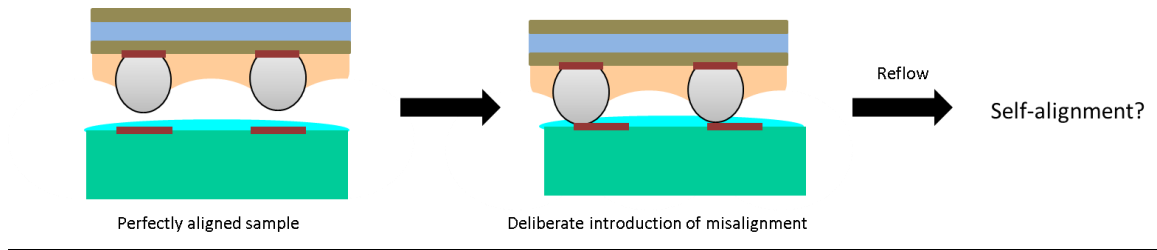


Figure 75: Deliberate introduction of misalignment before reflow

The results of this study indicate that the thickest collar variation does not prevent the balls from self-aligning even when misaligned by about $\frac{3}{4}$ of the pad (170 μm), unless the ball is placed in contact with multiple PCB pads (Figure.6). The polymer collar is thus perfectly compatible with current SMT assembly processes.

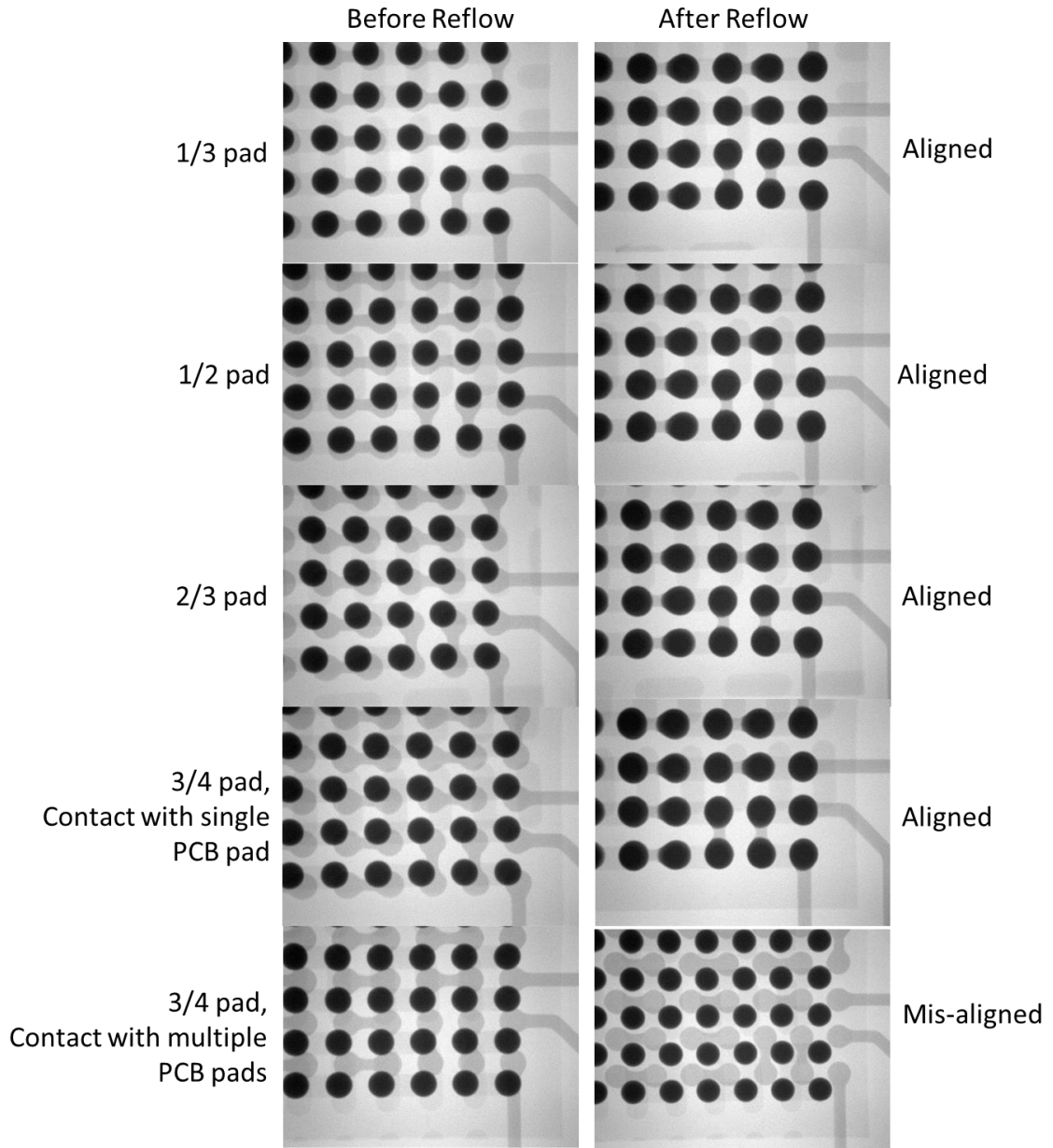


Figure 76: X-ray images of interposers misaligned during pick and place, before and after reflow

5.2 Reliability of large body size BGA glass packages

Previous work on 7.2 mm BGA glass packages demonstrated highly reliable interconnections (up to 1700 thermal cycles) using a single dielectric build-up layer as a

stress buffer. This research extends this concept to larger package sizes. Therefore, the overall objective of this research was two-fold, i.e., evaluate the efficacy of the polymer collar as a strain relief mechanism and demonstrate the reliability of an 18.4 mm glass BGA package, although this chapter mostly focuses only on assembly and initial yield. Interposers with 7.2 mm were used to compare interconnection reliability with different polymer collar heights. Due the medium package size, no differences are expected in their reliability performances. However, this size was chosen due to sample availability. The evaluation of large package reliability was done with 18.4 mm glass packages, with and without the polymer collar. The large glass interposers will be evaluated with several design and material variations with and without polymer collar. Reliability testing is done with reference to the JESD22-A104D standard for thermal cycling. Assembly was followed by pre-conditioning with 2 additional reflows at a peak temperature of 260°C. Thermal cycling was then done between -40°C and 125°C with a 15 minute dwell time and a rate of 1 cycle/hour.

5.2.1 Reliability of 7.2mm BGA package

Initial evaluation of the effect of polymer collar on interconnection reliability was done on 7.2mm interposers.. The DOE plan presented in Table 17 was created for this purpose. Samples were assembled without collar, and with collars spin coated at 1000 rpm, 2000 rpm, and 3000 rpm. Polymer residue on the ball surface was removed by solvent wipe before assembly. All reliability samples were built and systematically characterized by x-ray (interconnection yield), C-SAM (glass breakage and delaminations) and DC electrical testing. The interposer design features 12 daisy chains as indicated in Figure 77.

Table 16: DOE for 7.2 mm reliability evaluation with collar

Assembly variation	No Collar	Collar at 3000 rpm	Collar at 2000 rpm	Collar at 1000 rpm
No. of samples	10	10	10	5

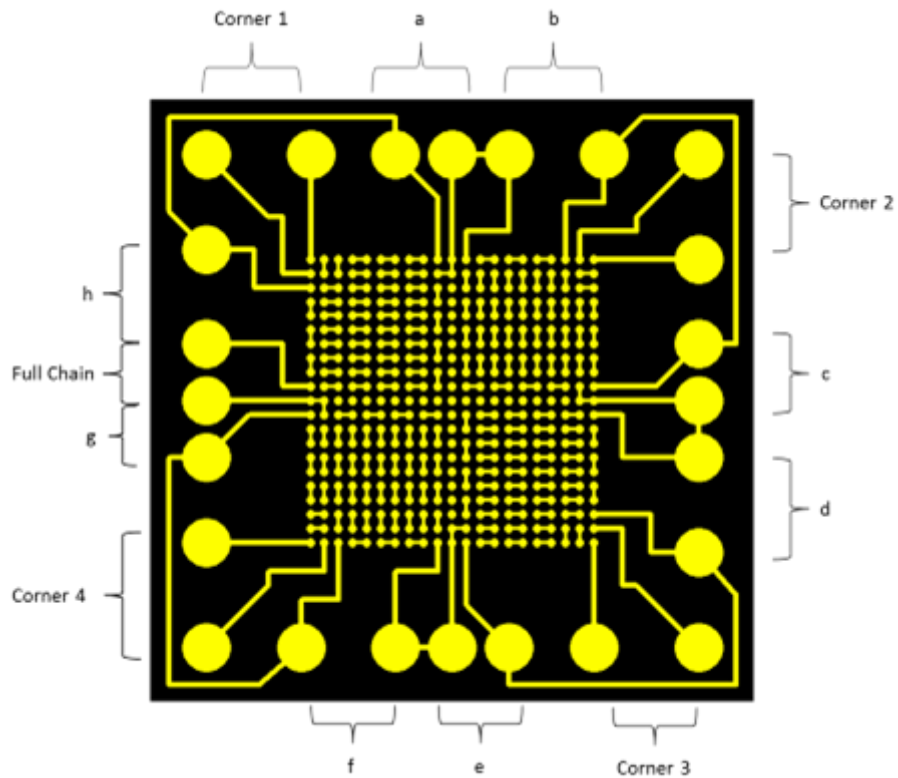


Figure 77: 7.2 mm board probing points

The resistance of all daisy chains was measured for each sample after assembly and carefully monitored as the test progressed. Table 17 lists the average value of each chain right after assembly and reflow. Yield after assembly was at a 100%.

Table 17: Daisy chain resistance measurements after assembly

Sample/R	no collar	3000 rpm	2000 rpm	1000 rpm
C1	0.352	0.359	0.39	0.394
a	0.366	0.38	0.379	0.382
b	0.448	0.512	0.448	0.442
C2	0.366	0.401	0.395	0.383
c	0.38	0.385	0.411	0.390
d	0.479	0.471	0.489	0.476
C3	0.358	0.4	0.394	0.372
e	0.385	0.394	0.383	0.370
f	0.481	0.45	0.508	0.440
C4	0.359	0.386	0.394	0.420
g	0.377	0.48	0.35	0.370
Full Chain	1.158	1.15	1.147	1.162
h	0.459	0.477	0.435	0.480

Daisy chain resistance was monitored at regular interval during thermal cycling (Figure 79). These 7.2mm samples were fabricated during the start of the program and there were issues to do with the adhesion between RXP-4M and glass which have since been solved through additional surface treatment. Despite early signs of build-up layer de-lamination (Figure 78), most samples failed only after 500 thermal cycles. It must be noted that the samples failed at after 500 cycles not due to solder strain, but due to loss of contact between interposer and solder balls.

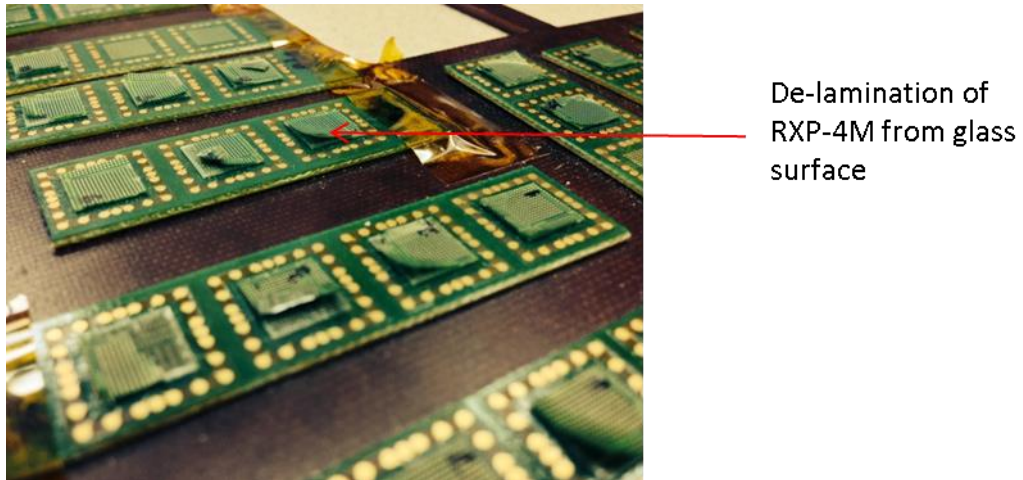


Figure 78: RXP-4M de-lamination on assembled 7.2mm interposers

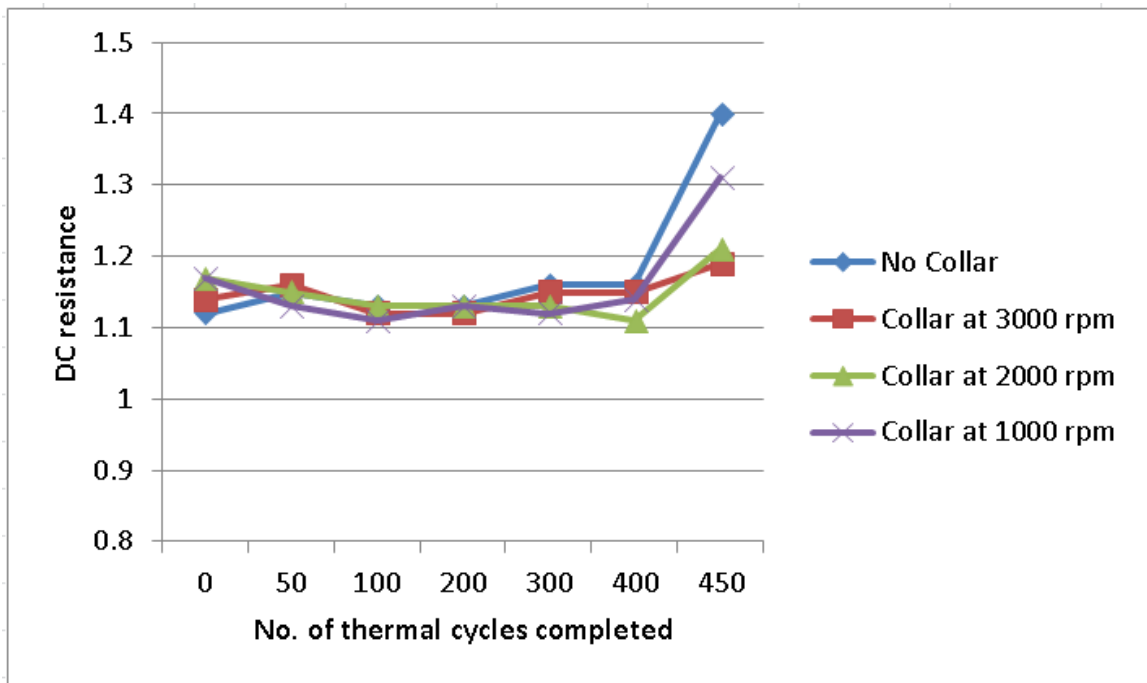


Figure 79: Daisy chain resistance measured during thermal cycling

5.2.2 Reliability of 18.4mm BGA glass packages

A DOE plan was formulated to evaluate the thermo-mechanical reliability of 18.4mm BGA glass package vs. glass CTE, with and without polymer collar as stress

relief mechanism. Samples variations are presented in Table 18. All samples were assembled using optimized conditions described in section 5.1.2. After assembly, samples were subjected to 2 more reflows at a peak temperature of 260°C to serve as pre-conditioning. A 150 µm thick, 12 mm x 12 mm die was then attached via underfill to two interposers within each variation, to simulate the effect of chip-level assembly on BGA reliability. Thermal cycling was then conducted between -40°C and 125°C, with a 1 minute ramp time and 15 minutes of dwell time at the extremes.

The samples showed defects associated with mostly bridging and missing balls due to imperfect interposer and balling yield as disclosed in Chapter 3. C-SAM confirmed only minor delamination but no breakage of the glass. Electrical testing of the interposers showed perfect yield of the defect-free daisy-chains.

Table 18: DOE for preliminary reliability evaluation

	NSMD		RMD	
	Without collar	With collar	Without collar	With collar
Total no. of samples	8	8	8	8
No. of samples with die attached	2	2	2	2

Figure 77 shows x-ray images taken after the assembly of RMD and NSMD interposers without collar. The irregular solder shape on NSMD interposers discussed in Chapter 3 can be seen here. Solder balls on the RMD interposer are regular in shape as no traces were exposed between the balls. X-ray analysis of the samples before and after reflow confirms that the reflow process does not introduce additional defects. Cross section images of interposers assembled with and without collar show good ball attachment (Figure 78).

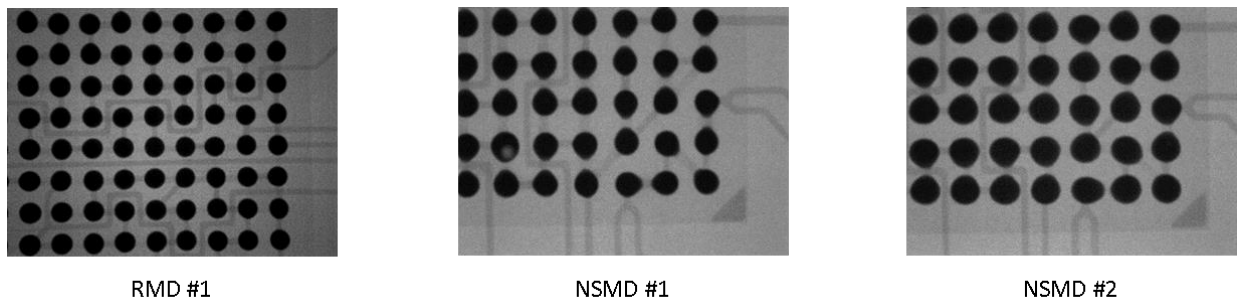


Figure 80: X-ray close ups of assembled 18.4 mm glass interposers

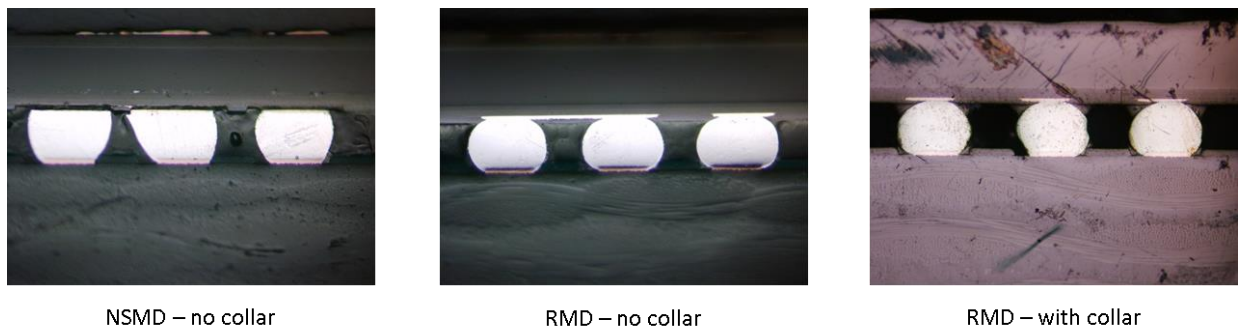


Figure 81: Cross sections of 18.4 mm glass interposers assembled with and without polymer collar

Due to the large number of solder joints, the DC resistance of corner chains was monitored during thermal cycling. Figure 82 shows the variation of DC resistance at the

four corners of the interposers after assembly and reflow. The yield of these corner daisy chains is also mentioned on each plot. The samples were subjected to 200 thermal cycles and no early failures were seen in daisy chains that were functional after assembly.

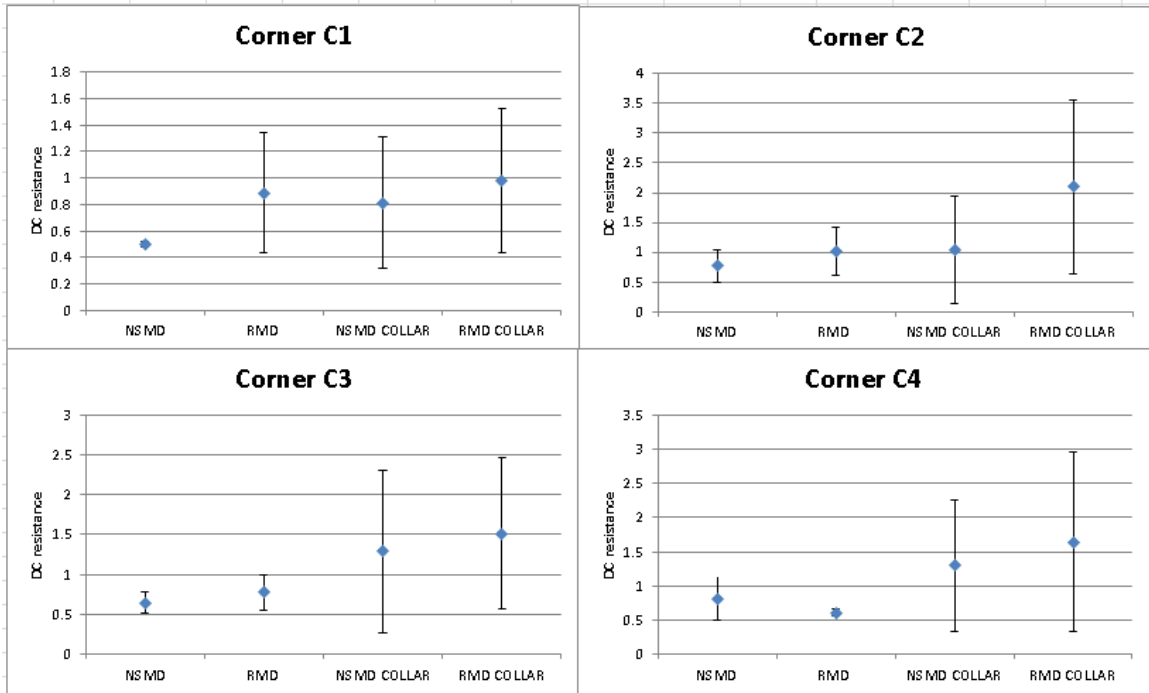


Figure 82: DC resistance variation at the four corners of the interposer

5.3 Conclusions

. An industry compatible assembly process for large interposers with polymer collar was demonstrated. Due to the issue of material leakage onto the PCB, the collar thickness has to be compromised. Higher thickness leads to better strain relief but increases the amount of leakage. A solution to this issue could be found through material development with considerations made to the reflow temperature profile.

Samples with 7.2 mm, assembled and tested for thermal-cycling reliability, were found to fail after 500 cycles. This was due to the afore-mentioned delamination issue that was seen on all the samples. Samples with 18.4 mm have survived 200 cycles with no early failures in the corner joints.

CHAPTER 6

SUMMARY AND FUTURE WORK

6.1 Summary

With transistor scaling reaching the fundamental physical limits of CMOS technology, package-enabled multi-IC integration is the most efficient approach to system miniaturization, cost and performance. Package sizes are expected to exceed 60 mm in the near future in order to support the large number of ICs for high-performance applications. These packages must be compatible with standard, low-cost SMT technologies so as to be a viable option for high-volume and low cost production. To address these needs, GT – PRC has pioneered the study of glass interposers as a low-cost alternative to traditionally- used organic and silicon packages. Glass offers the advantages of high dimensional stability, excellent electrical properties, availability as an ultra-thin substrate, and low CTE to ensure reliable chip to package interconnections. This research begins to demonstrate that large low TCE substrates such as glass can be surface-mount assembled directly on the board.

SMT- compatible reliable interconnections between low-CTE glass packages and PCB are a major barrier to establishing glass as the prevalent and low cost package material for next generation electronic systems. This research explores two strain relief approaches for fine-pitch solder interconnections between low-CTE glass packages and PCBs, i.e., dielectric build-up layers and polymer collars. Reworkability is ensured through the elimination of underfill.

FEM was used to study the mechanism behind these two approaches and their applicability at large package sizes. Build-up layers relieve strains through a stress buffer effect while the circumferential polymer collars act as a partial underfill. Modeling of 2D interposer assemblies suggests that addition of a polymer collar can reduce maximum solder strain range by up to 20% for large package sizes (Figure 83). Modeling also suggests that glass may be used at large package sizes while maintaining maximum plastic solder strain range below the critical limit (0.008). It must be noted, however, that this 2D modeling is simplified to study the fatigue of the solder joints only, and does not accurately account for the actual warpage behavior of the package which can also play a role in the board-level reliability. An extensive representation of the geometry and stack-up materials, considering an application-dependent Cu coverage with intermediate copper re-distribution layers, and modeling of the fabrication process from the bare glass down to board-level assembly, including first-level assembly, underfilling and molding, might be necessary to emulate the correct warpage behavior of the package.

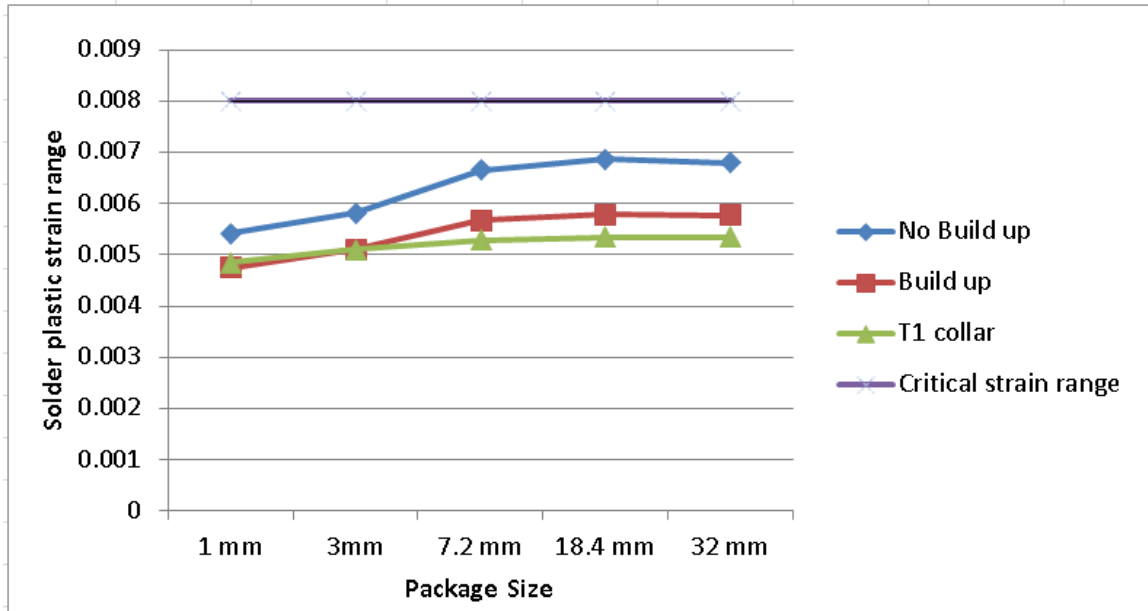


Figure 83: Comparison of strain relief approaches for increasing package sizes

Based on modeling results, a 400 μm interconnection pitch test vehicle was designed and fabricated at a package size of 18.4mm for the purpose of demonstrating large package assembly and preliminary reliability studies. Relevant fabrication challenges like surface blisters after electro-less plating were discussed, setting up the stage for improved processing for future research in this area. Recommendations on a new stack-up for the next fabrication cycle are provided.

Substantive work was performed to develop the polymer collar approach, with strain relief, into a manufacturable, SMT-compatible solution. Process development was conducted on 7.2 mm and 18.4 mm interposers, starting with the application process through spin coating. Three strategies for removal of the polymer residue from the solder ball surface – plasma etching, sand blasting and solvent wipe – were explored and compared, resulting in an industry-compatible, front-up solution to the same: solvent dip using infrastructure for flux dipping.

High yield assembly was achieved with 18.4 mm glass interposers both with and without polymer collars. Tacky flux was first dispensed on the PCB with either OSP or ENEPIG finish onto which interposers were then picked and placed using a standard flip-chip bonder. The assembly was subsequently batch reflowed in a reflow oven at a peak temperature of 260°C, resulting in the formation of good quality joints with an acceptable level of voiding. Thick polymer collars were shown to have negligible derogatory effects on the self-alignment of solders during reflow.

Due to the relatively low number of samples resulting from new fabrication processes, glass interposers were used for initial reliability evaluation through thermal cycling. Failure modes were classified as related to non-optimal processes (early failure) or thermo-mechanical fatigue.

6.2 Recommendations for Future Work

A first demonstration of large glass package to PCB assembly with and without polymer collars was presented through this thesis. Recommendations for the next stage of research in the area are listed below:

- 3D Finite Element Analysis of more realistic assembly geometries incorporating process modeling and accurate material stack-up (Cu coverage).
- Simulation of the effect of chip-to-package assembly with over molding on board-level interconnection reliability.
- Switch to a ZIF/ZIF build-up structure for process ability and homogeneity of the build-up layers.

- Use photo-definable (photo-sensitive) dry film or liquid-type passivation instead of ZIF. Laser drilling of openings in ZIF leaves residue on copper pads and hinders manufacturability.
- Further material development for polymer collars for increased compatibility with solder assembly and reflow processes.
- High-frequency testing of polymer collar assemblies to ensure signal integrity in the presence of polymer residues.
- Concentrate on RMD pad design to enhance ball attachment yield.
- Thermal cycling and drop-testing on statistically significant sample sets to definitively establish the reliability of large glass-to-PCB interconnections.

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