

**FRONTEND WEAROUT ANALYSIS AND MODELING FROM
DEVICE TO INTEGRATED CIRCUITS FOR RELIABILITY AND
YIELD ENHANCEMENT SYSTEM**

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The Academic Faculty

by

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**FRONTEND WEAROUT ANALYSIS AND MODELING FROM
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*Dedicated to my parents Hoseung Cha and Younghee Baek,
and sister Jooyeon Cha
for their endless love and belief.*

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SUMMARY

With the aggressive scaling of CMOS technology, Negative Bias Temperature Instability (NBTI) and Gate Oxide Breakdown (GOBD) become serious issues for transistors. NBTI is an important wearout mechanism which affects MOSFET devices by shifting the threshold voltage (V_{th}) as the device ages. GOBD is also an important wearout mechanism affecting MOSFET devices, and is expressed by a voltage dependent ohmic model or as a gate leakage current. The impacts of NBTI and GOBD degrade the operating performance of circuits, and, in extreme cases, causes a circuit to behave incorrectly due to violations of timing constraints. Hence, it is important to understand circuit performance degradation due to various wearout mechanisms to better understand the relationship between process-level physical models and circuit lifetime.

In this research, I assume that no on-chip circuitry is available for wearout monitoring. Under this assumption, I find a relationship between the threshold voltage shift and degradation in the ground signal to extract NBTI parameters. The NBTI parameters are derived from the threshold voltage shift, which is extracted from a shift in the ground signal with time. Similarly, the GOBD parameters are derived from the minimum gate dielectric resistance, which is extracted from the shift in the power and ground signal with time. Therefore, this research proposes the link between the device level wearout model and the system level reliability model. Also, it not only accounts for the impact of gate bias voltage and temperature, but also considers real usage scenarios when estimating lifetime, where processors have multiple states of operation. Furthermore, it also proposes how to extract NBTI and GOBD model parameters for each chip to enable the estimation of the remaining life of individual chips.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Moore's law expects that the density of integrated circuits (ICs) will be approximately doubled every two years. To meet the law, device geometries continue to be scaled down in deep sub-micron VLSI circuits as the clock frequency increases and per-chip costs decrease [1]. However, the relentless scaling of CMOS technology makes circuits more susceptible to manufacturing defects, reliability, and process variation [2]. Especially, NBTI and GOBD are known as major factors that make an integrated circuit vulnerable. However, because the physical mechanisms of the degradation of a MOSFET are not fully understood and process variation makes every chip have different features affecting reliability, the exact extrapolation of the circuit lifetime at various conditions is still difficult [3]. To address this difficulty, many studies proposed various methods to predict the lifetime of an IC more accurately.

Furthermore, because the aggressive scaling exacerbates the process variation and reliability problems, the power and operating frequency constraints become more stringent in integrated circuits. Therefore, in order to maximize the circuit performance and minimize the constraints, many kinds of adaptive control systems can be implemented in the integrated circuit against aging and process variation issues. The systems control the various factors for example, supply voltage, body bias, and operating frequency to avoid the constraints.

1.2 Research objective and contribution

The objective of this research is to extract NBTI and GOBD model parameters to enable the estimation of the remaining life of individual chips. For the model parameter extraction, the device-level models of both reliability mechanisms are modelled with the Random Telescope Noise (RTN) model. Because the reliability models are a function of temperature, supply voltage, and stress time, we calculate the time-dependent performance degradation. Furthermore, the performance degradation can predict lifetime as well, and can enable the optimization of timing guardbands or circuit adaptation based on a prediction of the increase in delay as a function of time, temperature, and usage. The proposed approach involves the use of measurements of variation in the ground, power supply, and I/O signals. These measurements are linked to not only extract model parameters but also to estimate the remaining lifetime of ICs accurately.

Furthermore, equipped with the calibrated model parameters for individual chips, we build a reliability aware critical path extraction method to analyze the delay degradation of the extracted critical paths in a system. Based on the performance degradation analysis, we design a yield and reliability tolerant system by using a self-adaptive clock duty cycle controller (DCC) system to avoid timing violations of critical paths in an integrated circuit. Although the DCC module has area and power consumption overhead issues, the DCC system can extend a circuit's lifetime and improve the yield of the circuit as well. Therefore, we suggest a method to optimize the number of DCC modules in a system to maximize the advantages and minimize the disadvantages.

1.3 Literature survey

Focusing on the previous work related to the device-level reliability models and aimed at estimating the remaining lifetime through simulation of lifetime, a literature survey follows.

1.3.1 Device-level models for NBTI

With the scaling of CMOS technology, Negative Bias Temperature Instability (NBTI) has become a serious issue for transistors. Normally, degradation due to NBTI is modeled based on test structure data or ring oscillators embedded within product die.

During the last decade, the reaction-diffusion (R-D) model has been used to explain the NBTI effect in a pMOS device, which is the breaking and rebonding of hydrogen-silicon bonds at the silicon-gate dielectric interface. The hydrogen-silicon bonds diffuse into the bulk of the oxide [4]. However, although the R-D model explains the threshold voltage shifts produced by DC bias and temperature stress, it could not explain the speed of recovery and the impact of the dynamic gate bias [5]-[9]. Therefore, recently, the charge trapping and detrapping (T-D) model is being considered as a more likely explanation of the NBTI mechanism [5],[6], in which the defects in the SiO₂ layer can capture and emit charged carriers, resulting in threshold voltage (V_{th}) degradations.

Starting with a physical model of NBTI, which characterizes the threshold voltage shift as a function of time, the device-level models can be used to derive gate-level simulation models and system lifetime [10]-[13]. In order to apply the device-level degradation to the system, many researches have used the activity, power, and temperature profile of the integrated circuit and propagate the information to each device and calculate the degradation of the devices in a system by using the NBTI physical model. Based on the link

between the device and system-level reliability model, the system-level prediction of lifetime enables the optimization of timing guardbands or circuit adaptation based on a prediction of the increase in delay as a function of time, temperature, and usage. This can be done with look-up tables of frequency and voltage pairs as a function of time under operation [14]. This approach assumes that the NBTI model is known, and hence errors result if failure rate parameters or operating history are not estimated correctly. Also, because the lifetime of a circuit is jointly affected by NBTI and PV, circuit timing has to consider both effects.

1.3.2 Device-level models for GOBD

Gate oxide breakdown (GOBD) is a serious reliability issue for MOS transistors. In general, wearout due to GOBD is modeled based on test structure data and is expressed by a voltage dependent ohmic model or as a leakage current.

Many studies classify stress induced leakage current (SILC) modes in three categories: A, B, and C-mode SILC [15],[16]. A-mode SILC is induced by trap-assisted tunneling (TAT) mechanisms where electrons pass from the cathode to the anode via defect sites (neutral traps) in the SiO₂ by the electrical field [17],[18]. A-mode SILC degrades into B-mode SILC when the oxide experiences partial breakdown, also known as soft breakdown (SBD) [15],[19]. During soft breakdown, the circuit can operate correctly. When the oxide fails to operate as an oxide, this corresponds to C-mode SILC, which is the so-called hard breakdown (HBD) [20].

For previous technology generations with a thick oxide (>10nm) layer with a high gate voltage (>3V), the gate leakage current is derived by the Fowler-Nordheim tunneling model [21]. However, for the recent technology generations with a thin oxide (<3nm)

layer, defects in the oxide can be generated by lower gate voltages [21]. This is referred to as intrinsic breakdown (BD). Several mechanisms have been proposed to explain intrinsic BD. The lowest energy process is the trap creation mechanism due to hydrogen emission from the anode [22],[23]. The statistics of trap generation models have suggested a relationship between a gate leakage current increase and stress time [24],[25]. Experimental observations prove that the mean time failure is a function of the total gate oxide surface area, temperature, and gate voltage due to the weakest-link character of oxide breakdown [26]. However, when abstracting this relationship to the system level, it is important to take into account details of circuit operation, not just the surface area.

1.3.3 The estimation method of the remaining lifetime

Prior work has aimed at estimating the remaining lifetime through simulation of lifetime. Due to NBTI, the V_{th} of the MOSFET increases with a stress time. The increased V_{th} is the cause of drive current reduction. The reduction in the drive current of a MOSFET results in temporal performance degradation of a circuit. To overcome the performance degradation, previous researchers have suggested a one-time solution to extend the lifetime of a circuit, such as sizing [27] or synthesis [28]. Also, [29] proposed an adaptive body bias control technique by using a leakage current sensor to compensate for the increased threshold voltage, and [30] proposed a forward body bias control technique by using a lookup table to find an optimal body bias and supply voltage for the circuit. Also, the device-level models can be used to derive gate-level simulation models and system lifetime, which can be done with look-up tables of frequency and voltage pairs as a function of time under operation [30]. Although the suggestions can not only extend a lifetime but

the approaches assume that the wearout model is known. Hence, errors result if failure rate parameters or operating history are not estimated correctly.

In the past, many researchers have used a measuring methods that directly accesses the device-under-test (DUT) to monitor current variation for NBTI. For GOBD, previous oxide breakdown measurement techniques have been invasive, requiring direct access to DUTs and peripheral circuitry. Also, statistical methods are suggested to monitor the yield of gate oxide layers in a manufacturing production line [31],[32]. This technique can be used for statistically binning the oxide reliability of integrated circuits upon the completion of manufacturing but cannot be used to dynamically monitor chip reliability and degradation throughout its lifetime.

Alternative approaches have involved on-chip circuitry. Specifically, ring oscillators [33] are used to analyze real-time MOSFET aging in order to measure device degradation. They compare the frequency difference between the stressed and fresh ring oscillator frequency and extract the phase difference between them, which is attributed to the V_{th} shift due to NBTI degradation. In [34], they used MOSFETs to starve the current supplied to a NAND gate ring oscillator. Then, they measured the change in the frequency of oscillation and voltage amplitude of the NAND ring oscillator. Also, because the chip frequency depends on the speed of critical paths, replica critical paths can be used to analyze degradation [35].

However, the ring oscillators or the replica critical paths do not share the same ambient environment because of the difference in their on-die locations, and the critical paths within a datapath can change as a result of degradation [36]. Hence, on-chip circuitry may not produce an accurate prediction of the aging rate and model parameters of the true

critical paths and devices. Another method, involving direct monitoring of critical paths [37],[38], entails some area overhead and the correct selection of the vulnerable critical paths. Another approach involving direct monitoring of aging, involves the use of specially designed latches that detect delay errors, at the expense of significant power overhead per latch [39],[40]. All of these techniques need to be incorporated in a design prior to tapeout.

1.3.4 Design for yield and reliability enhancement

Because of the aggressive scaling of CMOS technology, process variations and reliability have affected integrated circuits. Therefore, many prior methods try to improve it while the circuit is in operation. These techniques include modified flip-flops, controllable PLLs, and dynamic voltage and frequency scaling (DVFS) techniques [39],[40],[41].

To avoid the timing variations from the lack of timing margins, we suggest a self-adaptive clock duty-cycle controller system using a modified buffer with a comparator. Although the previous studies [39],[40],[41] need additional circuits which take additional clock cycles for error detection and recovery stages, our proposed system generates a warning signal before an error occurs. Furthermore, the duty cycle controller system doesn't change the actual clock frequency but just modifies the duty cycle adaptively to enhance the yield and to extend the lifetime of a microprocessor in real-time.

CHAPTER 2

DEVICE PHYSICS STUDY: DEVICE LEVEL WEAROUT MODELS FOR NBTI AND GOBD

2.1 Negative Bias Temperature Instability (NBTI) Model

During the last decade, the reaction-diffusion (R-D) model has been used to explain the NBTI effect on MOSFETs, which is the breaking and rebonding of hydrogen-silicon bonds at the silicon-gate dielectric interface [43]. However, although the R-D model explains the threshold voltage shifts produced by DC bias and temperature stress, it cannot explain the speed of recovery and the impact of the dynamic gate bias [44]-[48]. Therefore, recently, the charge trapping and detrapping (T-D) model is considered as a more likely explanation of the NBTI mechanism [44],[45].

Random Telegraph Noise (RTN), that is, charge trapping and detrapping of oxide defects, has been observed in submicron FETs. Defects, which are located in the dielectric layer in MOSFETs, capture and emit charges [49]. If a defect captures a charged carrier in the gate dielectric, unexpected current noise occurs, and the charged defects affect the mobility and scattering in the device [49],[50].

For a device under constant bias, because charge trapping depends on the Fermi level only [50], the current remains constant on average and does not change with time. In digital ICs, the gate voltage (bias) and the Fermi level change abruptly because of the digital input signals. This increases the probability of trapping, and the number of captured charges increases over time. Therefore, the gradually increasing number of occupied traps changes the channel conductivity, which is a source of bias temperature instability. In the T-D model, the number of defects which trap charge has a functional relationship with bias

voltage, temperature (T), and time (t). These defects lead to an average and standard deviation of threshold voltage degradation.

First, the number of defects undergoing capture and reemission is modeled with the Poisson distribution with time constants corresponding to emission (τ_e) and capture (τ_c) [51],[52]. The distribution associated with the number of defects that capture charge functionally relates to bias, temperature (T), and time (t). The time constants are uniformly distributed on the log scale and the distribution is linked to the Fermi energy level and temperature [53].

$$\tau_c = 10^p \cdot (1 + \exp(-q)), \quad (1)$$

$$\tau_e = 10^p \cdot (1 + \exp(q)), \quad (2)$$

where $p \in [p_{min}, p_{max}]$ and $q = (E_t - E_F)/k_B T$, $E_t \in [E_v, E_c]$, p is the signal frequency range on the log scale, E_F is the Fermi Level, k_B is the Boltzmann constant (eVK^{-1}), T is temperature (K), and E_v and E_c are the energy levels of the valance and conduction band, respectively.

The number of defects, $n(t)$, for a specific device is distributed according to a Poisson distribution [54]. $n(t)$ is integrated over the time constants to give [55]:

$$\mu(n(t)) \simeq \varphi(T, E_F) \cdot (A_{NBTI} + B_{NBTI} \cdot \log(t)), \quad (3)$$

$$\sigma(n(t)) \simeq \varphi(T, E_F) \cdot \sqrt{A_{NBTI} + B_{NBTI} \cdot \log(t)}, \quad (4)$$

where A_{NBTI} and B_{NBTI} are constants, t is the stress duration and should be larger than 0, and $\varphi(T, E_F)$ is an U-shape function that depends on the trap energy density distribution in the band-gap, which is a function of temperature and Fermi level.

The fluctuation in average V_{th} is determined by multiplying Eq. (3) by δ , the shift in V_{th} due to a single trap [56], to get

$$\Delta V_{th}(t) = \delta \cdot n(t) \quad (5)$$

Therefore, using Eq. (5), we obtain the theoretical average and standard deviation of the shift in threshold voltage for each MOSFET device in our system. Note that the relative variation in the number of defects, $\sigma(n(t))/n(t)$ decreases as a function of time, as does the relative variation in the threshold voltage. This is consistent with experimental observations of delay variations in circuits [57].

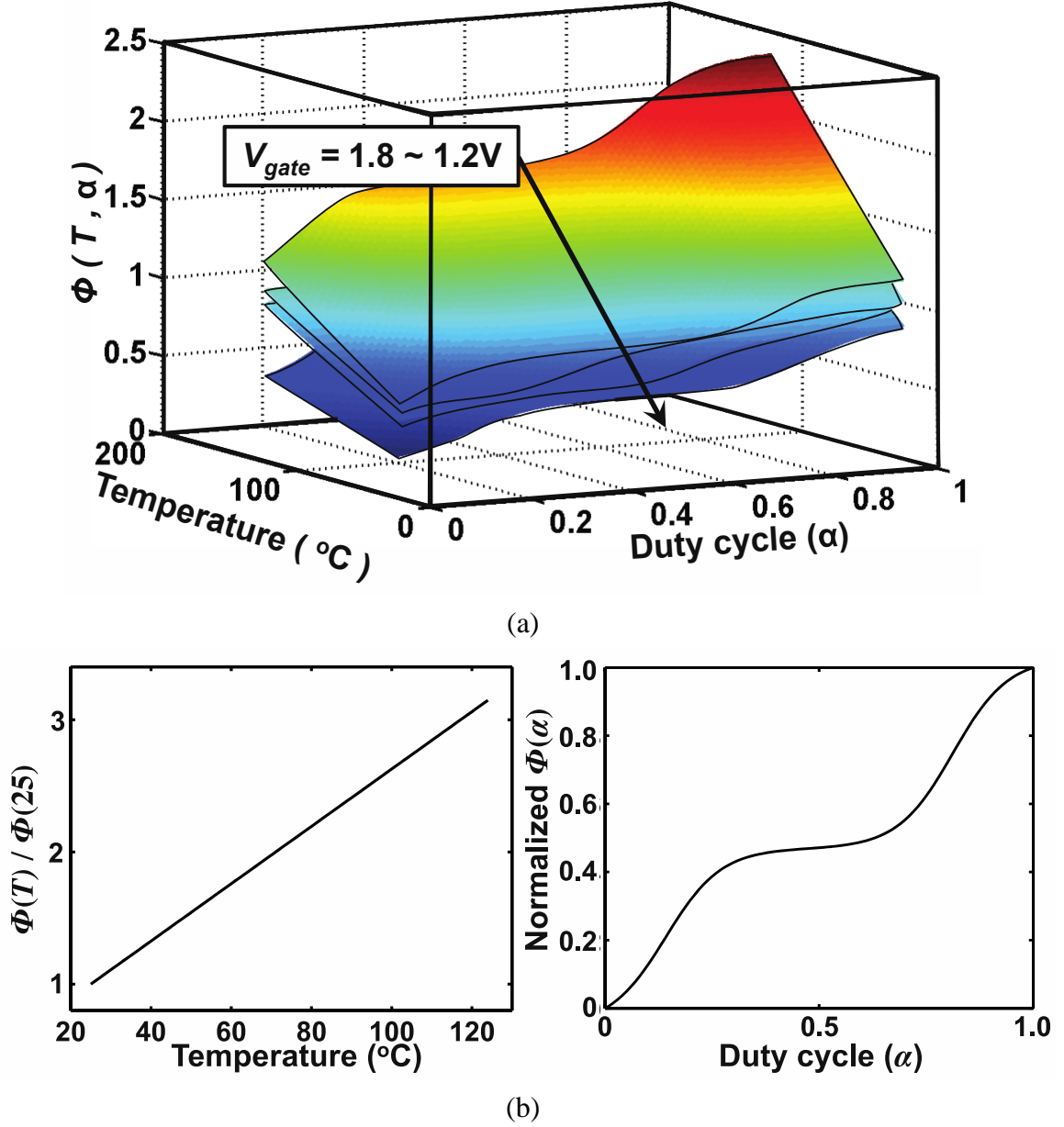


Fig 2.1. The dependence of the threshold voltage shifts on the duty cycle and temperature. The threshold voltage is a linear function of $\varphi(T, \alpha)$, as noted in Eqs. (1) and (3), where $\Delta V_{th} = \delta \cdot \varphi(T, E_{F,eff}) \cdot (A + B \cdot \log(t))$ and where $E_{F,eff}$ is a function of α , according to Eq. (4). (b) The temperature and duty cycle dependence of $\varphi(T, E_{F,eff})$.

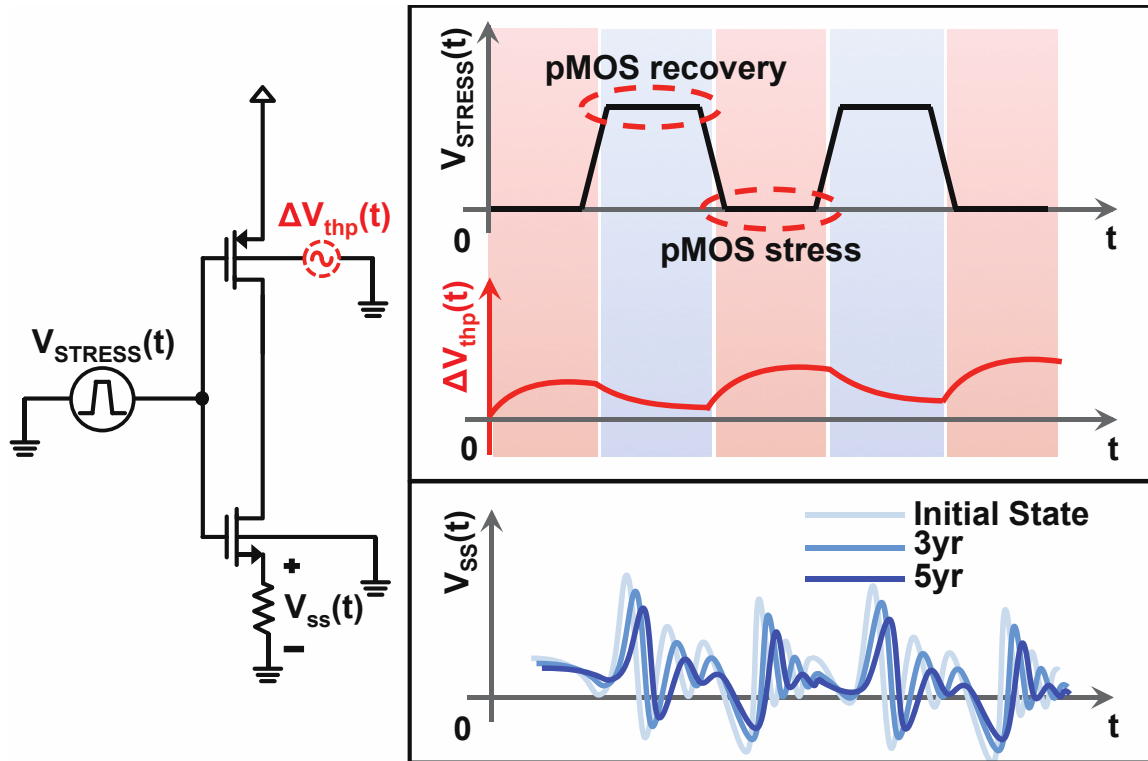


Fig. 2.2. Simple example of the impact of stress and recovery on Δv_{th} and the corresponding ground signal, $V_{SS}(t)$, at different time points.

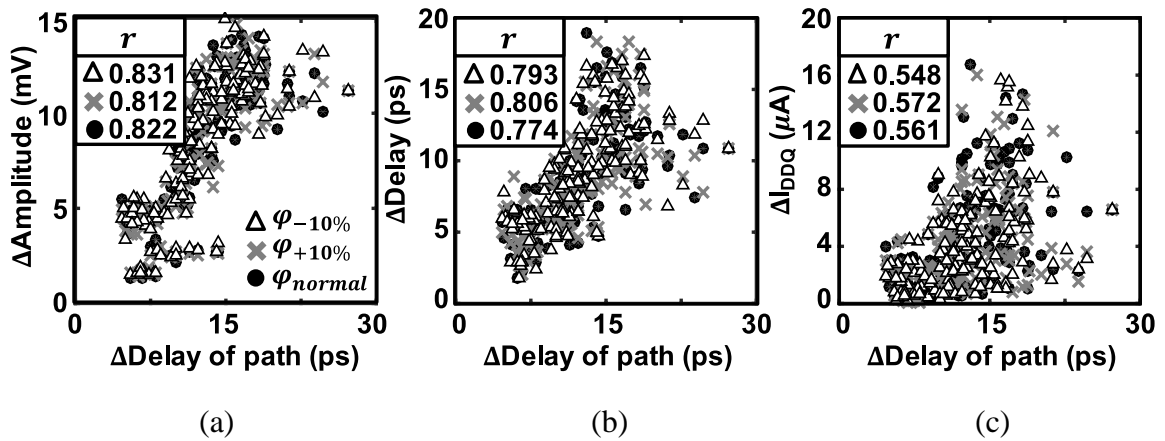


Fig. 2.3. Correlation between output path delay degradation and (a) $\Delta\text{Amplitude}$ of the bounce signal, (b) ΔDelay of the ground bounce signal, and (c) ΔI_{DDQ} .

Digital circuit operation has stress and recovery periods. The fraction of time under stress is called the duty cycle, α . Instead of modeling V_{th} shift for each stress and recovery period separately, it is best to choose an effective Fermi level, as a function of duty cycle [56]:

$$E_{F,eff}(\alpha) = \alpha \cdot E_{F,on} + (1 - \alpha) \cdot E_{F,off} \quad (6)$$

The effective Fermi level is used to determine the evolution of threshold voltage degradation. Therefore, $\varphi(T, E_{F,eff})$, in combination with Eqs. (3) and (6) estimates the shift of the threshold voltage as a function of time. For example, it can be seen that as α approaches one, when there is no time for recovery, degradation is much more significant. This is illustrated in Fig. 2.1, using the U-shaped trap density distribution function for $\varphi(T, E_{F,eff}(\alpha))$ which is affected by not only temperature and duty cycle (Fig. 2.1(b) [49],[55]), but also is affected by the gate voltage (Fig. 2.1(a)). When we calculate $\varphi(T, E_{F,eff}(\alpha))$, the range between the conduction and valance band is one of the important factors. The conduction to valance band range is affected by the gate voltage, because the gate voltage affects the amount of band bending of the conduction and valance band energy [44],[59].

Fig. 2.2 illustrates the shift in MOSFET threshold voltage for a switching inverter, showing stress and recovery cycles due to the NBTI effect. It also illustrates a ground signature signal, which shows the degradation in delay and amplitude of the ground signal as a function of time under stress.

In order to verify that the bounce signal variation and the circuit delay degradation have a reasonable relationship, we calculate the correlation, r , between delay degradation of the output paths and the amplitude and delay shifts of the ground bounce signal. The results

are shown in Figs. 2.3(a) and 2.3(b). The graphs show that the correlation between the parameters of the ground bounce signal and circuit delay is high.

For fitting the NBTI model, we only extract the A_{NBTI} and B_{NBTI} coefficients in Eq. (3). $\varphi(T, E_F)$ is also an important model parameter, and we use theoretical values for $\varphi(T, E_F)$ in our simulation. To verify that $\varphi(T, E_F)$ does not affect the ability of our models to predict circuit delay, we varied $\varphi(T, E_F)$ by $\pm 10\%$ and $\pm 20\%$ and checked whether the value $\varphi(T, E_F)$ impacts the correlation between the ground bounce signal and path delay. As can be seen in Fig.3, the variation in the correlation factors are less than 4%. Therefore, we can neglect errors in $\varphi(T, E_F)$ when calibrating the NBTI device-level model, and it is sufficient to estimate A_{NBTI} and B_{NBTI} . Once A_{NBTI} and B_{NBTI} are estimated, the extracted bounce signals can be used to predict path delay caused by the shift in threshold voltage (V_{th}).

Even if the theoretical values of $\varphi(T, E_F)$ are not accurate, degradation in $\Delta Amplitude$ and $\Delta Delay$ can predict critical path delay. Fig. 2.3(c) shows that the correlation between I_{DDQ} and delay is less effective, as mentioned in the introduction.

2.2 Gate Oxide Breakdown (GOBD) Model

GOBD is one of the key reliability issues for CMOS devices. GOBD results in stress induced leakage currents (SILC), which are induced by trap-assisted tunneling mechanisms where electrons pass from the cathode to the anode via defect sites (neutral traps) in the gate dielectric because of the electrical fields [60]-[63]. When the gate dielectric experiences partial breakdown, it is known as soft breakdown (SBD) [60],[64]. The circuit speed degradation considered in this work models soft breakdown.

Experimental observations indicate that the mean time to failure is a function of the total gate dielectric surface area, temperature, and gate voltage, due to the weakest-link character of gate dielectric breakdown [27]. However, when abstracting this relationship to the system level, it is important to take into account details of circuit operation, not just the surface area. Using a set of test patterns to determine stress and temperature, the time under stress is the time that the gate of an nMOS or pMOS device has the supply voltage and ground voltage applied, respectively. This time depends on the input patterns and the propagation of these patterns to each MOSFET. In order to model circuit performance degradation under breakdown, time dependent resistance models [25],[65] and time dependent leakage current models [66] have been proposed for SPICE simulation.

The devices are partitioned into groups that experience equivalent stress and temperature. More specifically, for an nMOS device, the time under stress is the time that the gate has the supply voltage applied. This time depends on the input patterns and the propagation of these patterns to each MOSFET. For each group of devices, the next step is to determine the number of devices experiencing different numbers of soft breakdown paths. This is done using the percolation model.

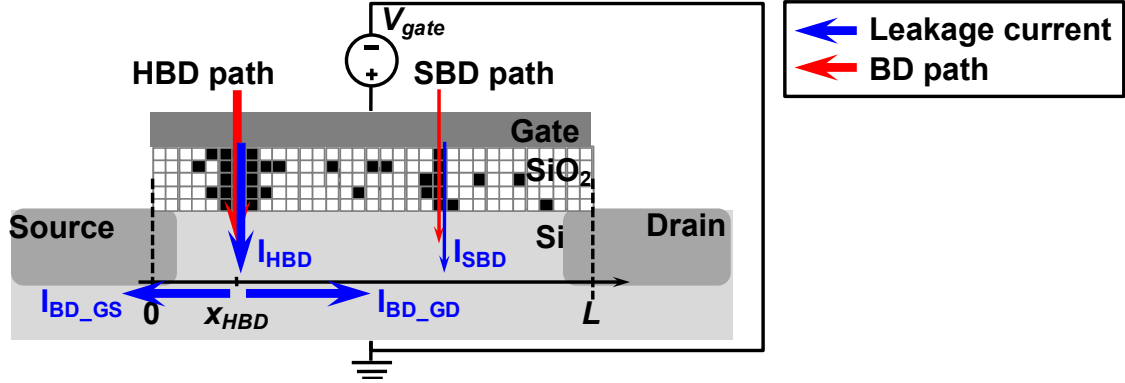


Fig. 2.4. Defect generation in the gate dielectric layer based on a 2D percolation model for soft breakdown and hard breakdown paths.

Fig. 2.4 shows the percolation model (PM) concept that involves placing neutral traps randomly within the oxide and analyzing the number of resistive conduction paths in a 2D matrix representing the gate dielectric layer [67]. We have expanded the model to 3D to count an accurate number of conduction paths. In the percolation model, the defect generation rate depends only on the gate voltage. Therefore, during electrical stress, the trap density in the gate dielectric increases with stress time t as a power law in the anode hole injection model. Stress is converted to a number of traps [68],[69]:

$$N_{trap}(t, V_G) = A_{GOBD} \cdot \exp(B \cdot V_G) \cdot t^\beta \times \tau_{OX}WL \times \exp(-\theta \cdot T) \quad (7)$$

where A , B , and β are fitting constants, and τ_{ox} , W , and L are oxide thickness, gate width, and length, respectively, and $\theta \approx 0.01^\circ\text{C}^{-1}$ [69].

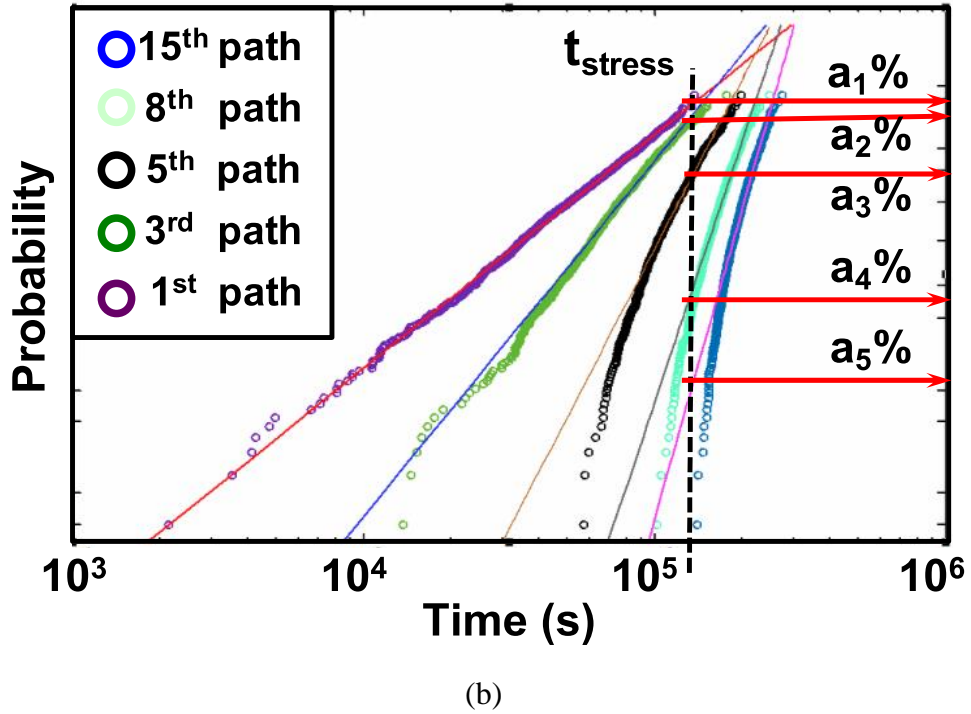
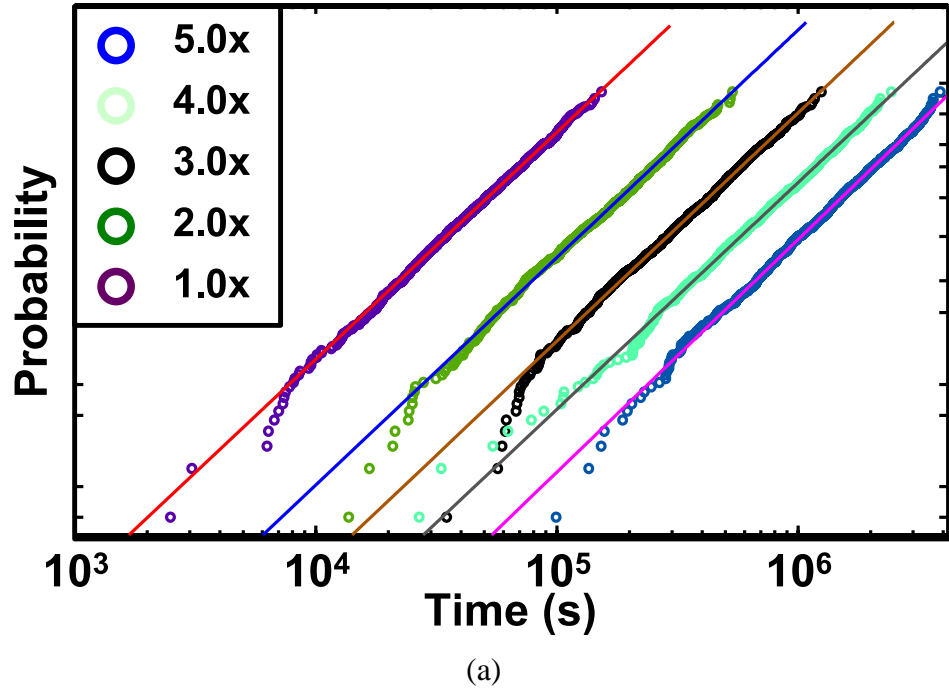


Fig. 2.5. Time distribution of defect generation in SiO₂ layer. (a) The probability distribution of the time of occurrence of the k^{th} SBD path for different gate sizes. (b) The probability distribution of the number of SBD paths for a fixed gate size as a function of time.

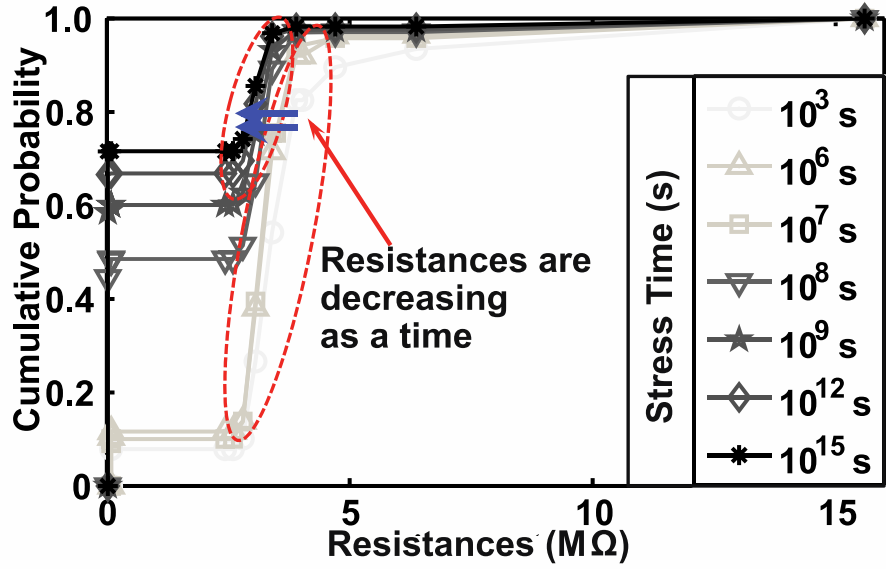
Fig. 2.5 shows the PM simulation results and the probability distribution of the time of occurrence of conduction paths in the gate dielectric layer as a function of gate size (Fig. 2.5(a)). It also shows the number of SBD paths as a function of time (Fig. 2.5(b)). Then, as we can see in Fig. 2.5(b), if we know the stress time and the gate voltage of a MOSFET, the probability of a fixed number of conduction paths can be estimated. The results in Fig. 2.5 indicate the probability that at least n paths are observed in the oxide. To find the probability that there are exactly n paths, it is necessary to subtract the $(n-1)^{\text{th}}$ curve from the n^{th} curve. Hence, given a time under operation, the time under stress is determined for each group of devices.

This is used to look up probabilities of different numbers of SBD paths. The number of devices in the group multiplies the probabilities to estimate the expected number of devices with each number of breakdown events in the group. The time under stress for the i^{th} device is a function of bias. Let α_i , where $0 \leq \alpha_i \leq 1$, be the fraction of time under stress for the i^{th} device. Then, $t_{stress,i} = t\alpha_i$, where t is the time under operation. Let $p_i = f_{SBD(n)}(t_{stress,i})$ be a probability of n SBD paths for the i^{th} device. Therefore, $p_i = f_{SBD(n)}(t\alpha_i)$. If the group of devices has N devices, then Np_i devices are randomly selected to have n breakdown paths at time t . Each sample randomly selects the devices experiencing SBD. Next, the SBD leakage resistance is calculated with the QPC model [70],

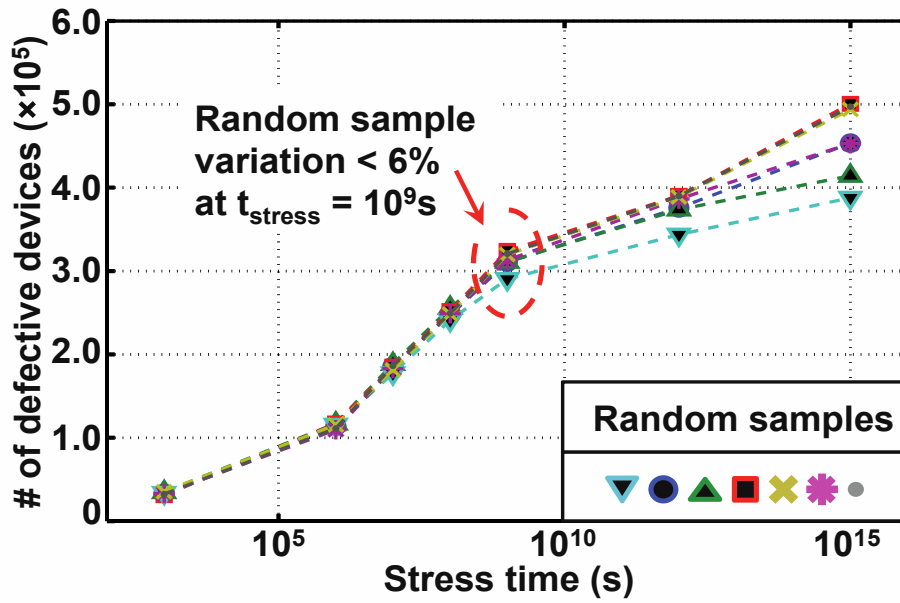
$$R_{SBD} \approx V_G / \left[\frac{4e}{\hbar\alpha} N \cdot \exp(-\alpha \cdot \Phi) \cdot \sinh\left(\frac{\alpha e(V_G - V_0)}{2}\right) \right], \quad (8)$$

where $\Phi = 3 \sim 4eV$, $V_0 = 0 \sim 0.5V$, $\alpha = 2 \sim 3eV^{-1}$, h is Plank's constant, e is the electron charge, and N is number of SBD conduction paths [70]. The location of SBD, gate-

to-drain vs. gate-to-source, is randomly selected. The location of SBD, gate-to-drain vs. gate-to-source, is randomly selected.



(a)



(b)

Fig. 2.6. (a) Time dependent degraded resistance cumulative distribution in an example microprocessor. (b) Number of devices undergoing soft breakdown as a function of time in an example microprocessor.

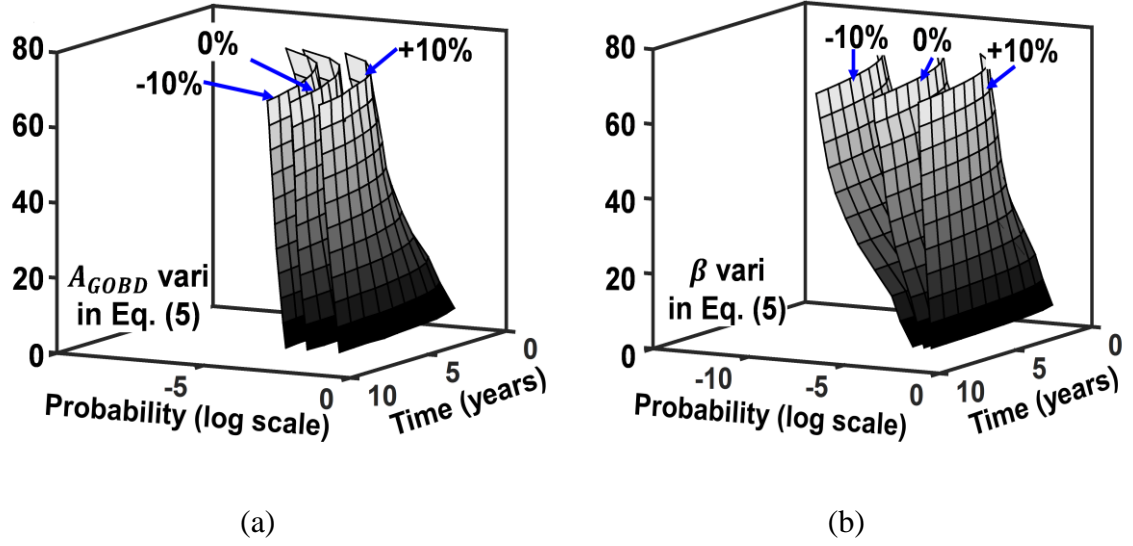


Fig. 2.7. The probability distribution of the conductivity due to SBD paths as a function of time due to variation in (a) A_{GOBD} and (b) β in Eq. (7).

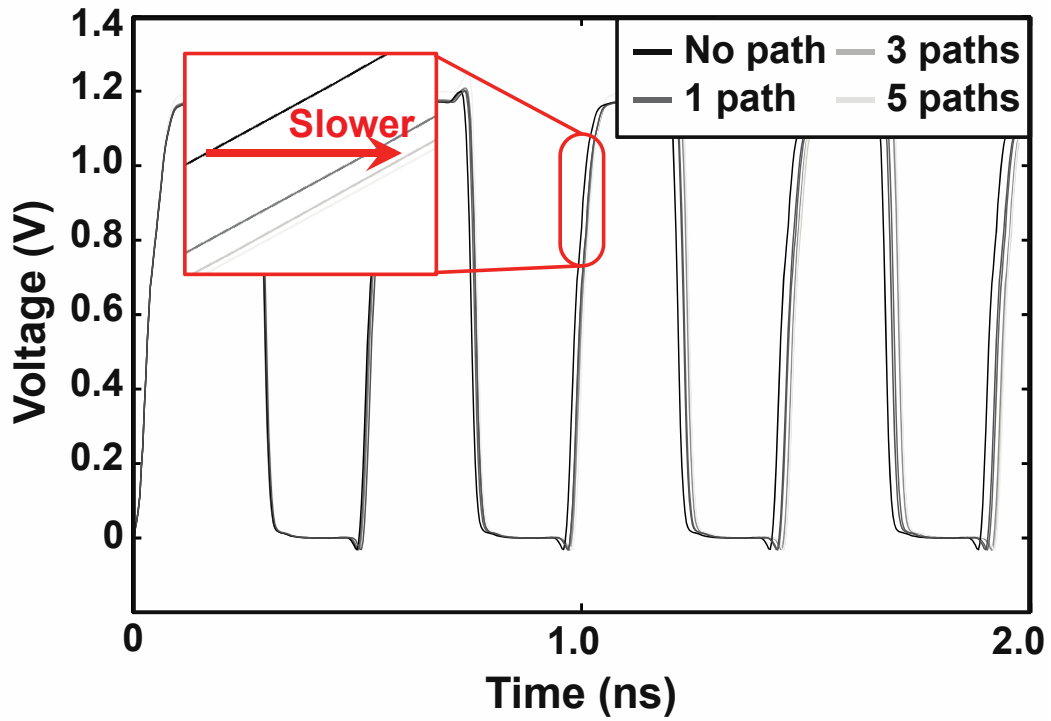


Fig. 2.8. The impact of SBD on ring oscillator performance.

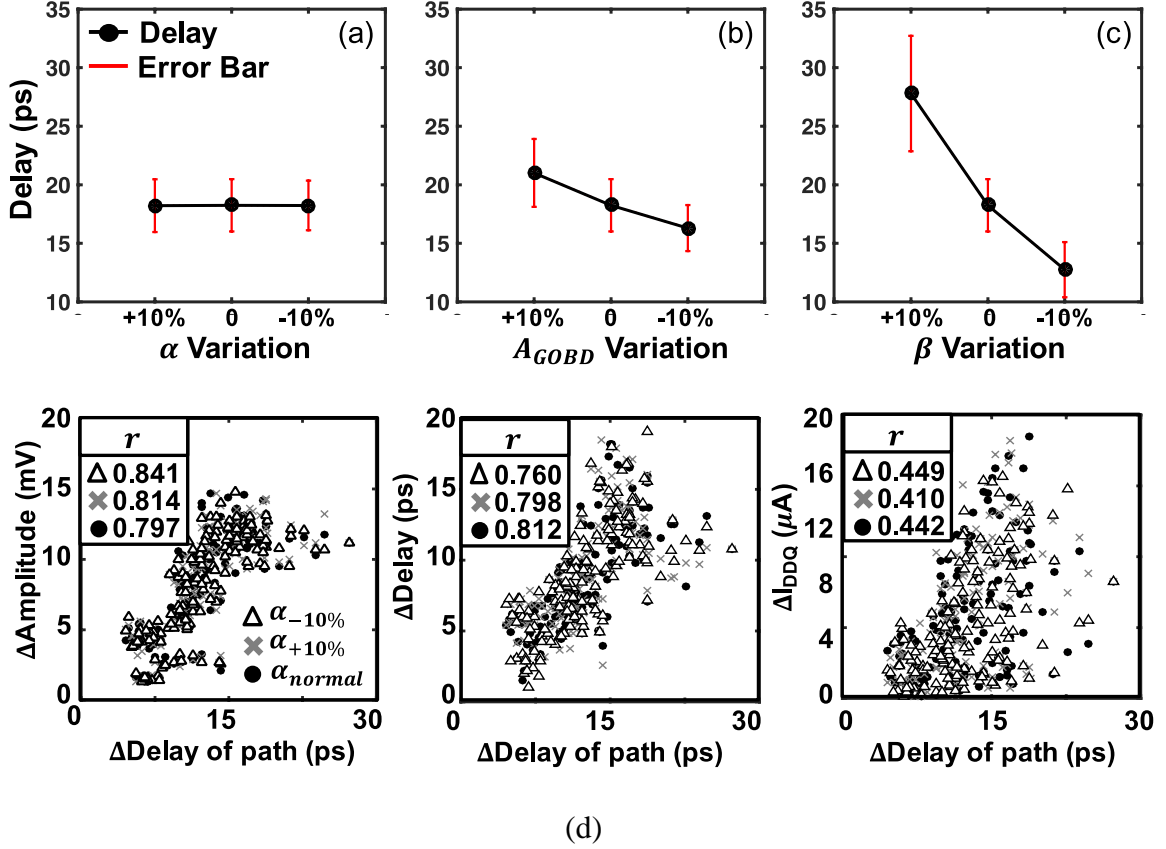


Fig. 2.9. Critical paths delay degradation after 10 years as a function of GOBD model coefficients: (a) $\pm 10\%$ α variation, (b) $\pm 10\%$ A_{GOBD} variation, and (c) $\pm 10\%$ β variation. (d) Correlation result with α variation, similar to Fig 2.3.

Fig. 2.6(a) shows the cumulative probability of degraded gate dielectric resistances, for an example circuit. It clearly shows that some of the gate dielectric resistances are decreasing as a function of stress time. Fig. 2.6(b) shows that the number of defective devices increases as a function of time. Note that the devices are selected randomly. Therefore, using seven samples, the difference in the minimum defective resistance at different time points is computed. The result shows that, although variation increases, it is under 6% at 10^9 's stress time (~ 30 years).

Eqs. (7) and (8) can be combined to extract the probability distribution of conductivity vs. time of individual devices. Fig. 2.7 shows the probability distribution of conductivity vs. stress time with $\pm 10\%$ variation of A_{GOBD} and β . As can be seen from Fig. 2.7, the effect of A_{GOBD} in Eq. (7) is the onset of GOBD, and the effect of β in Eq. (7) is variation in the time for the onset of GOBD among devices.

The impact of SBD on a ring oscillator is illustrated in Fig. 2.8. It can be seen that SBD causes delay, while not degrading signal swing. Also, we calculated and applied R_{GOBD} to a number of critical paths after 10 years of operation with different values of A_{GOBD} and β coefficients in Eq. (7) and α in Eq. (8). Then, we extracted the delay and delay variation. The results are shown in Fig. 2.9. It can be seen that A_{GOBD} and β strongly impact critical path delay, while α does not. Therefore, it is sufficient to extract A_{GOBD} and β . These parameters can be determined from $N_{trap}(t)$, as suggested by Eq. (7). Fig. 2.9(d) also shows that the correlation factors are not affected by errors in α in Eq. (8).

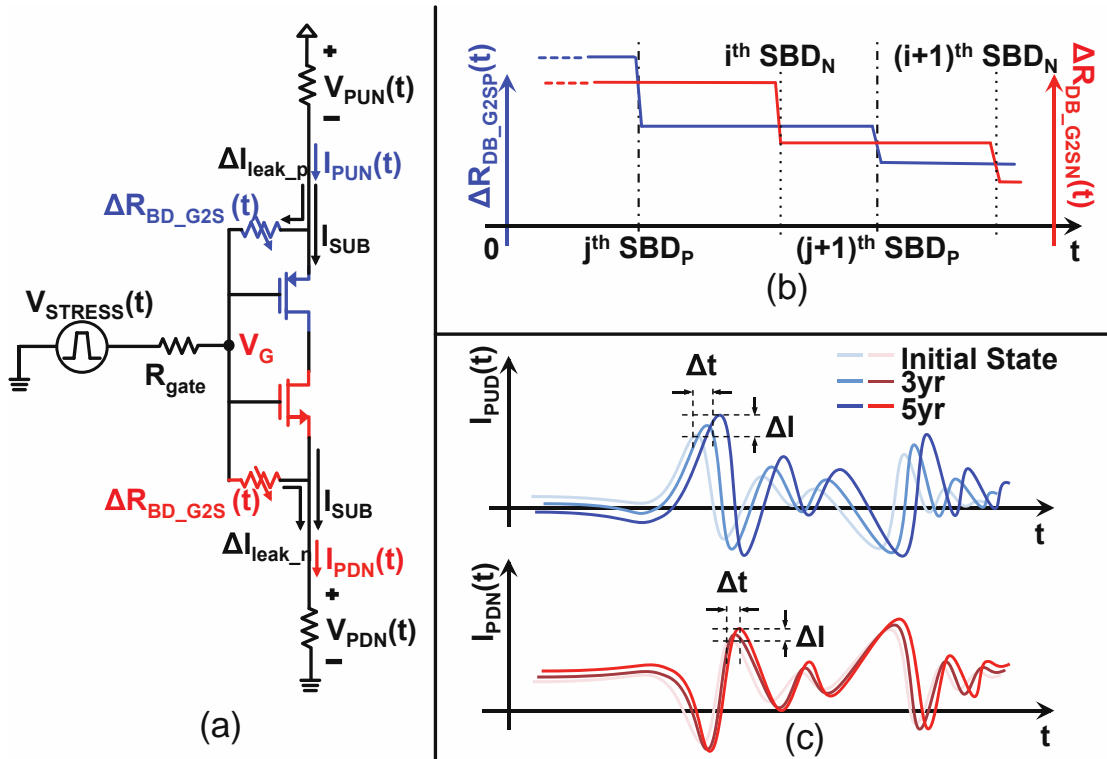


Fig. 2.10. Gate oxide breakdown resistance modeling for a device: (a) Inverter with GOBD resistance inserted for the nMOS and pMOS, (b) the changes in the pMOS GOBD resistance (blue) and nMOS GOBD resistance (red), and (c) power/ground current degradation.

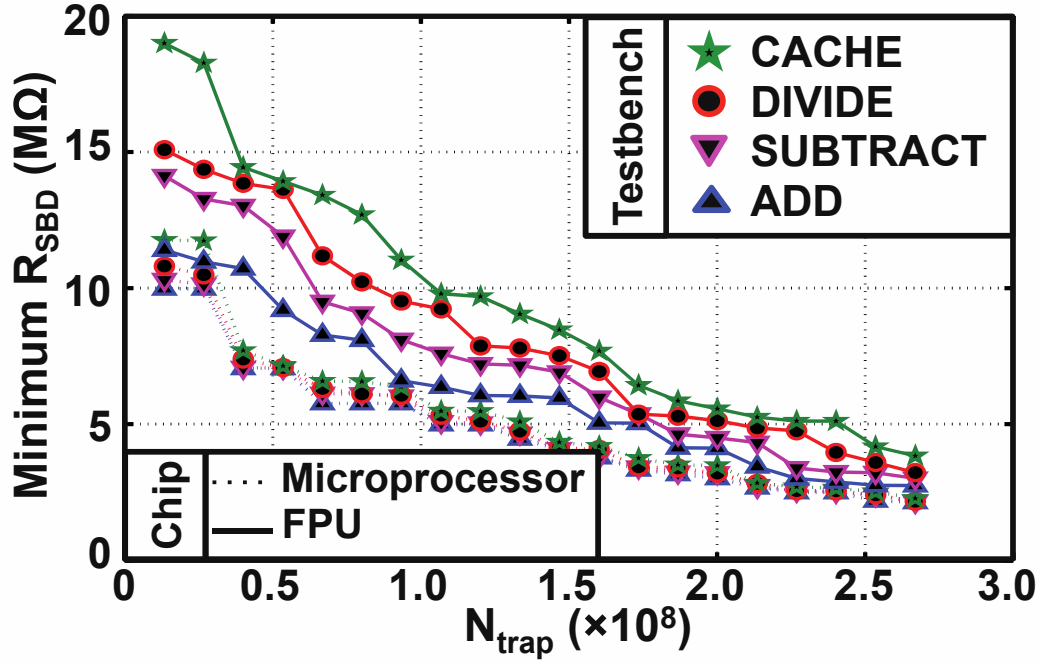


Fig. 2.11. Minimum resistance vs. N_{trap} for the FPU and microprocessor circuits for a variety of test benches.

Also, Fig. 2.10(a) shows that the impact of voltage stress is a reduction in resistances $\Delta R_{\text{BD_G2S}}$ for a few of the pMOS and nMOS devices. $\Delta R_{\text{BD_G2S}}$ decreases as stress increases, as the number of conduction paths increases, as shown in Fig. 2.10(b). As resistance decreases, both the power supply current, $I_{\text{PUD}}(t)$, and the ground current, $I_{\text{PDN}}(t)$, experience more bouncing as a function of time, as shown in Fig. 2.10(c), because new leakage current paths ($\Delta I_{\text{leak_P}}$, $\Delta I_{\text{leak_N}}$) are formed. As the leakage currents increase, the power supply voltage, $V_{\text{PUN}}(t)$, and the ground voltage, $V_{\text{PDN}}(t)$, display more bouncing. Not only does the total current increase, but also the gate voltage (V_{gate}) is divided by $\Delta R_{\text{BD_G2S}}$ and R_{poly} , and I_{SUB} also decreases due to the leakage current paths. The decreased I_{SUB} and reduced V_G cause the circuit speed to decrease. Hence, we can monitor

power/ground voltage bounce to detect GOBD in a circuit. The declining gate oxide resistance is a symptom of GOBD. In order to extract GOBD model parameters, we relate the minimum resistance to N_{trap} in Eq. (7), then we can model N_{trap} as a function of time. This is shown in Fig. 2.11. This result is a function of the circuit and the test bench studied. Fig. 2.11 shows that if we can estimate the minimum resistance, then we can model N_{trap} as a function of time. As with NBTI, all devices experience different amounts of stress, which translates to an average increase in observable power supply current. In this work, we aim to extract $N_{trap}(t)$, from which the parameters in Eq. (7) are determined.

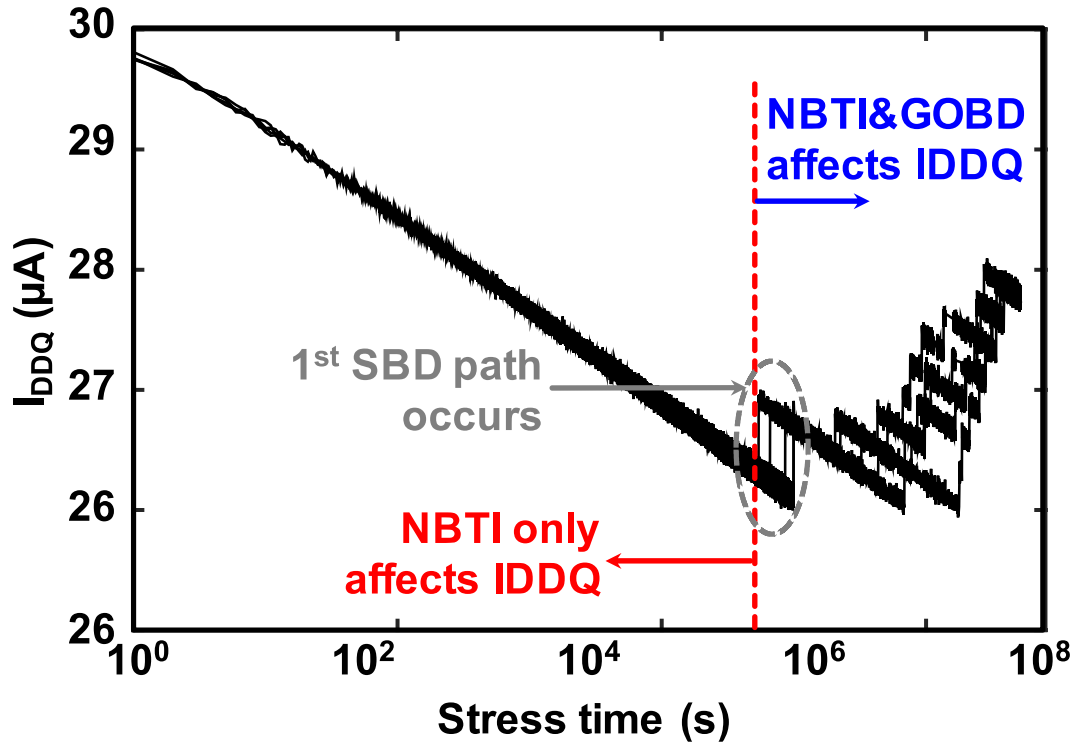


Fig. 2.12. Static current variation of a MOSFET as stress time with GOBD and NBTI effect

2.3 Device-to-Device Variation of Degradation

The physical models to explain the device-level reliability phenomenon are based on random models for NBTI and GOBD. Therefore, even though the coefficients of each device-level mathematical model for NBTI and GOBD are fixed, each MOSFET has different degradation factors for the same stress time and stress and temperature conditions. In order to consider the variation, in NBTI, we used the Eq. (4) to calculate the standard deviation of ΔV_{th} due to degradation, which is in addition to variation due to process parameters.

For GOBD, we also considered the randomness of the GOBD effect, because we use the probability distribution functions to calculate the number of conduction paths in each MOSFET in a system at a certain stress time, given values for stress voltage and temperature. Therefore, even though some MOSFETs may have the same amount of stress time with the same stress and temperature conditions, random variation can result in devices with different numbers of conduction paths.

Fig. 2.12 shows the static current degradation as a function stress time with the combined effect of NBTI and GOBD. Because of the threshold voltage increase by NBTI, the current decreases initially. However, after some time, the GOBD effect starts to create conduction paths and the gate leakage current increases. Because of the leakage current variation of each MOSFET in a system as a function stress time, the total leakage current of the overall system will change, and this can be seen in the ground and power supply voltage signal of the system. Therefore, the degradation of ground and power supply signals average the effect of shifts in threshold voltage and conduction paths through the gate oxide. This averaging nevertheless accounts for the workload seen by the circuit, either during stress testing or during in-field operations.

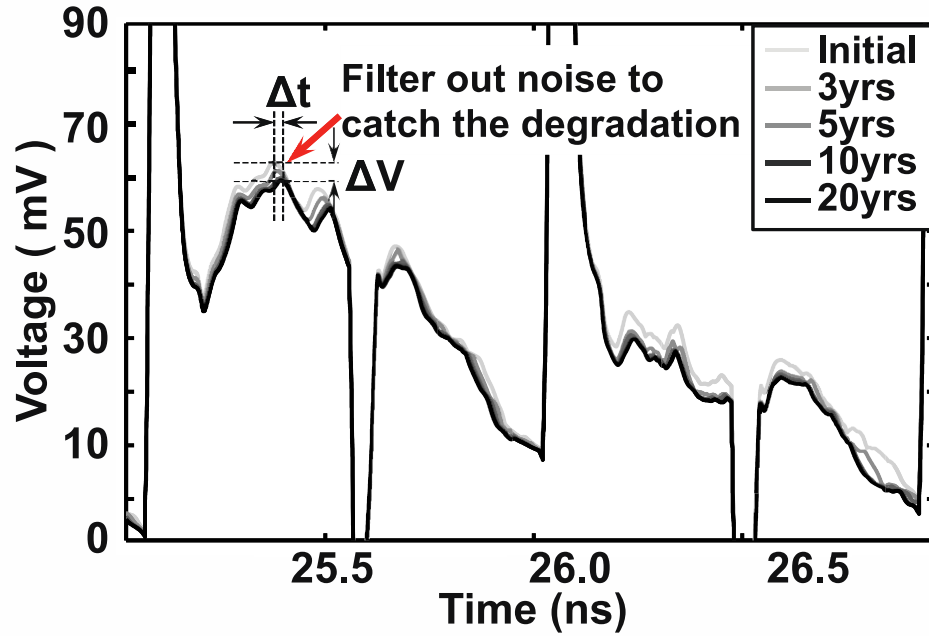
CHAPTER 3

SIMULATION STUDY: SIGNATURE SIGNAL ANALYSIS AND MODELING FOR NBTI AND GOBD

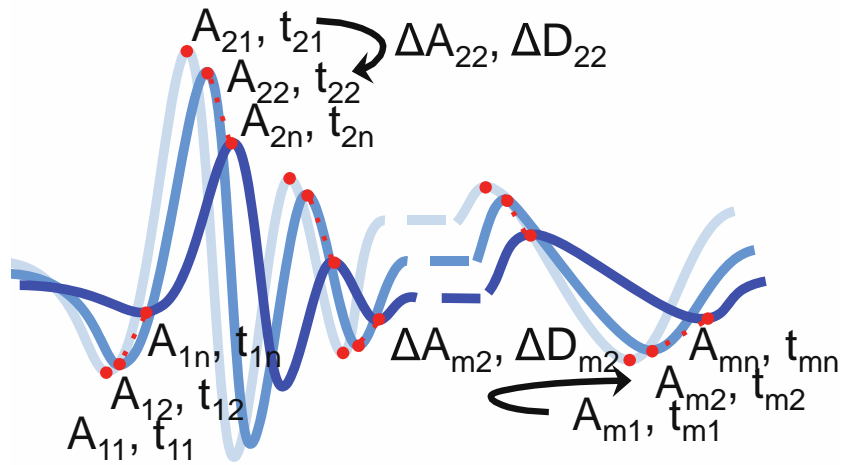
We first determine a model relating NBTI and GOBD to ground and supply voltage bounce. We have considered several different chips and test benches. The chips include a Microprocessor, a Floating Point Unit (FPU), and a Finite Impulse Response (FIR) filter.

The Microprocessor is a RISC processor with an external memory. It has around 1.4 million MOSFETs. The FPU and FIR filter have 20k and 8k MOSFETs, respectively. We simulate each of these systems with SPICE to obtain ground voltage signatures. The test benches determine the stress of each transistor. Hence, variation among the test benches provides an indication of variation due to the applied test patterns. It allows us to extract the best test bench for the purpose of parameter extraction. For example, for the microprocessor, the shift is largest for the ADD test bench and the least for the CACHE test bench. For process variation, we model the average initial threshold voltage (V_{th}^0) and channel length (L^0) for pMOS and nMOS devices, since these factors are not controlled well by the process, and they are important for timing.

In a circuit in operation, the degradation may be different than any test bench. The actual degradation depends on workload. Assumptions about a variety of workloads are taken into account when estimating the remaining lifetime. For the purpose of model extraction, the use of a test bench allows calibration of the model to known stress conditions.



(a)



(b)

Fig. 3.1. (a) A part of a signature signal for the effect of NBTI. (b) Finding the amplitude and delay points in the ground signature.

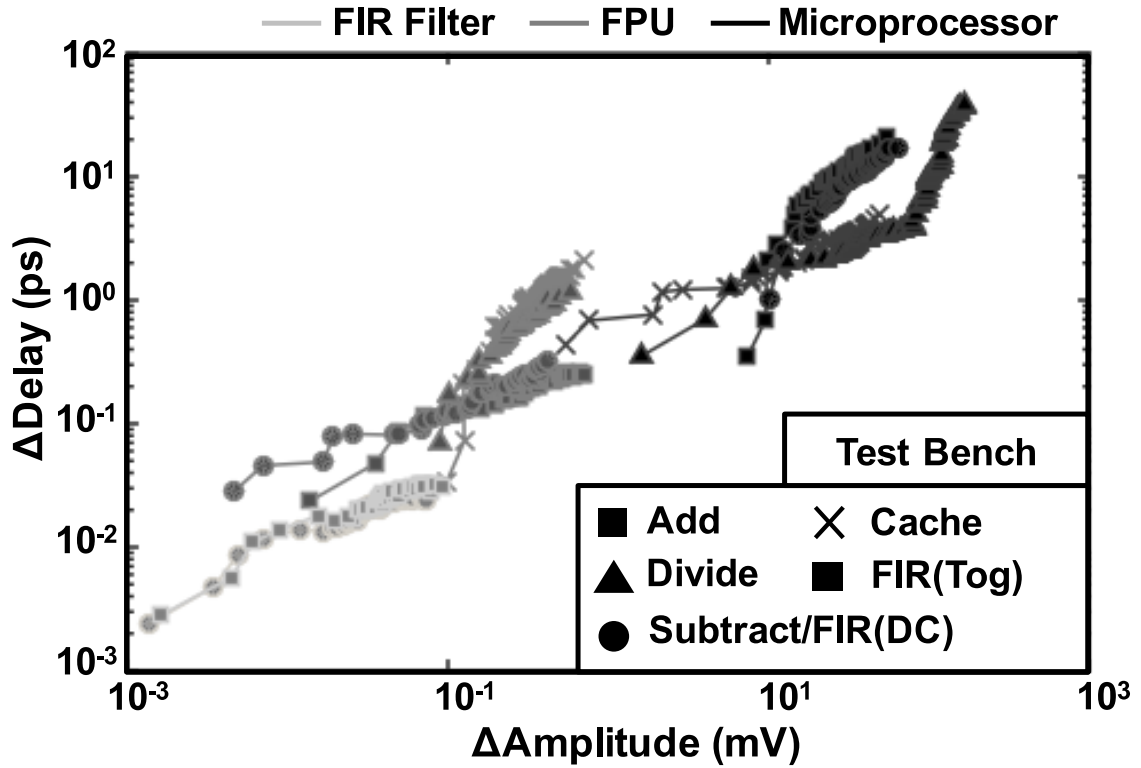


Fig. 3.2. Shift in delay and amplitude data distribution for NBTI and GOBD for multiple circuits and multiple test benches.

3.1 Data Extraction

Given a power supply and ground voltage signature, our method extracts the degradation in voltage and the shift in delay as a function of time. Fig. 3.1 shows the ground voltage signature as a function of the threshold voltage shift for NBTI. To simulate the effect of NBTI, signatures are generated with an initial random set of process parameters, to mimic a true process, at different time points with random and systematic degradation in threshold voltage, to mimic the impact of stress. We apply the impact of NBTI stress to

each MOSFET using Eqs. (3) and (4), where Eq. (3) is the systematic component and Eq. (4) is the random component.

Similarly, for GOBD, we generate a set of degraded resistances based on the stress distribution, random PV, and a random selection of SBD paths. The signatures on the power supply and ground, which are affected by the time dependent degraded resistances, are computed for an input pattern.

After applying the NBTI and GOBD effects and simulating the power supply and ground signals, the shifts in delay (ΔD) and amplitude (ΔA) are computed at each peak, as illustrated in Fig. 3.1(b). Each signature has several maxima and minima, where the number of maxima and minima depends on the applied input pattern. The average amplitude and delay degradation as a function of time in operation is computed. Fig. 3.1(b) shows as example signature signal and shows the data peak points used to extract shift data (ΔA for shifts of peak point amplitude and ΔD for shifts of peak point time).

Fig. 3.2 shows delay and amplitude shift data for NBTI and GOBD for different circuits and test benches. It can be seen that if the circuit has a larger number of devices, then the shift in amplitude and delay is larger for the same shift in threshold voltage, because more affected devices determine the voltage signature. Therefore, the observable shift in the ground voltage bounce depends on the number of devices in a circuit.

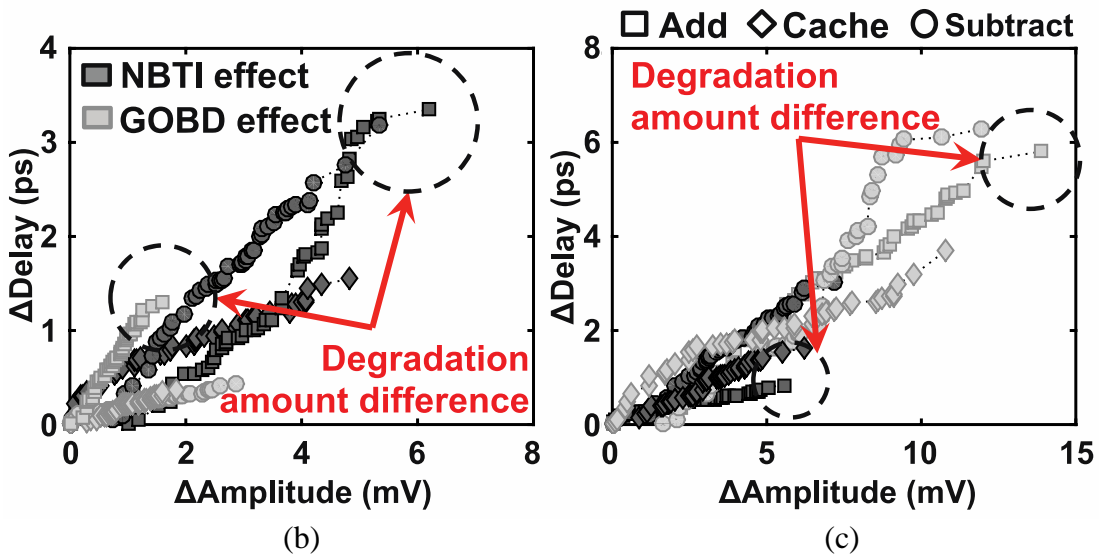
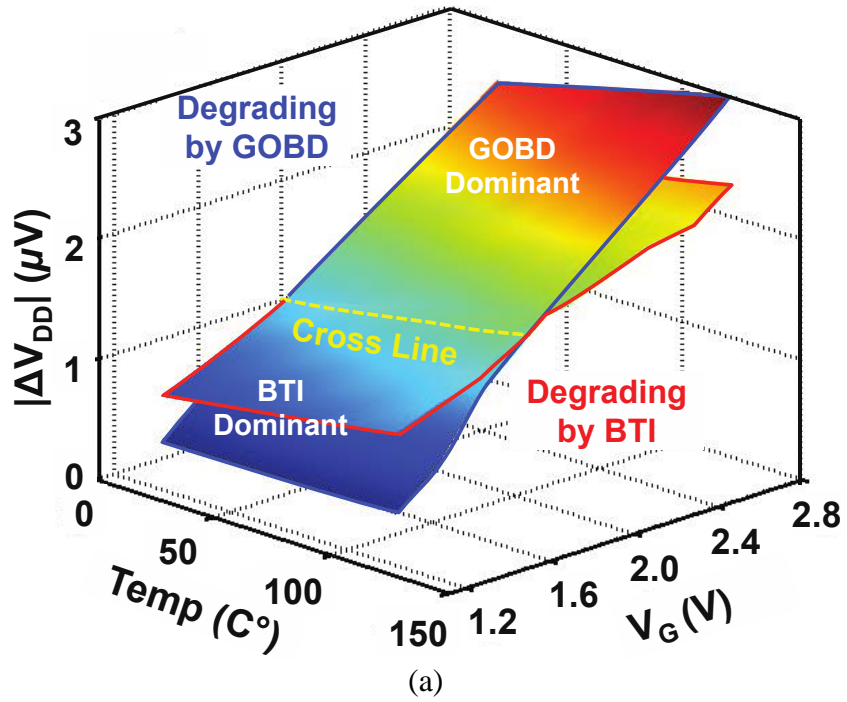


Fig. 3.3. (a) Stress conditions vs. amplitude degradation for the same stress time. (b) Shifts in delay and amplitude data due to NBTI and GOBD for NBTI dominant stress conditions and (c) GOBD dominant stress conditions.

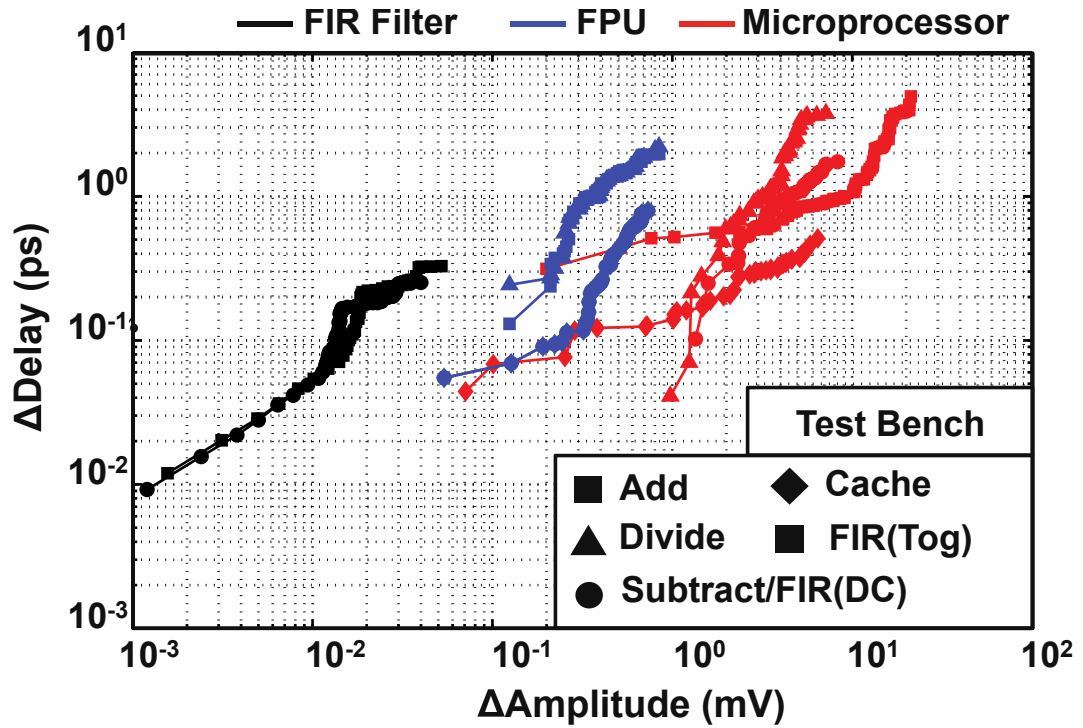


Fig. 3.4. Shift in delay and amplitude data distribution for NBTI for multiple circuits and multiple test benches.

3.2 Distinguishing NBTI and GOBD

The characteristics of the static leakage current in a circuit are used to find the stress conditions that make NBTI and GOBD dominant, as illustrated in Fig. 3.3(a). We can see that NBTI is dominant at low gate voltages and GOBD is dominant at high gate voltages. Fig. 3.3(b) and (c) shows some shifts in amplitude and delay at the NBTI and GOBD stress conditions, indicating a wide difference in both delay and amplitude shifts due to NBTI and GOBD. Fig. 3.4 shows additional delay and amplitude shift data for NBTI for different circuits. It can be seen that if the circuit has a larger number of pMOSs, then the shift in amplitude and delay is larger for the same shift in threshold voltage, because more affected pMOSs determine the voltage signature. Therefore, the observable shift in the ground voltage depends on the number of pMOSs.

In our examples, the primary stress conditions to observe NBTI is at stress voltages of 1.4V and 1.6V, while the primary stress conditions to observe GOBD is at 2.2V and 2.7V. However, the data is somewhat confounded. At NBTI stress conditions, there is still GOBD degradation, and at GOBD stress conditions there is NBTI degradation. Hence, we use an iterative procedure to extract NBTI and GOBD. First, we estimate the GOBD parameters from data at 2.2V and 2.7V. The impact of GOBD at 1.4V and 1.6V is estimated, and the data from GOBD is subtracted. Then we estimate threshold voltage shift due to NBTI with the resulting data at 1.4V and 1.6V. Models are used to estimate the degradation due to NBTI at 2.2V and 2.7V. The result is subtracted from the data at 2.2V and 2.7V. The GOBD model is then re-extracted. The revised model is then used to estimate GOBD at 1.4V and 1.6V. The iterations continue until convergence.

3.3 Data Extraction and Modeling for NBTI

NBTI causes the mean and standard deviation of the threshold voltages of MOSFETs to increase. In addition to the random initial Gaussian distribution of the initial threshold voltages, the amount of the increase is modeled as described in the previous section. We combine the initial distribution with the shift in threshold voltage to generate the virtual NBTI effect. Both the amplitude and delay degradation in the ground signature signal can independently estimate the threshold voltage shift.

Specifically, the delay and amplitude degradation are functions of the V_{th} shift, i.e.,

$$\Delta V_{th.del} = f_1(T, V_{DD}) \cdot \Delta A^{f_2(T, V_{DD})} + \delta_a(T, V_{DD}) \quad (9)$$

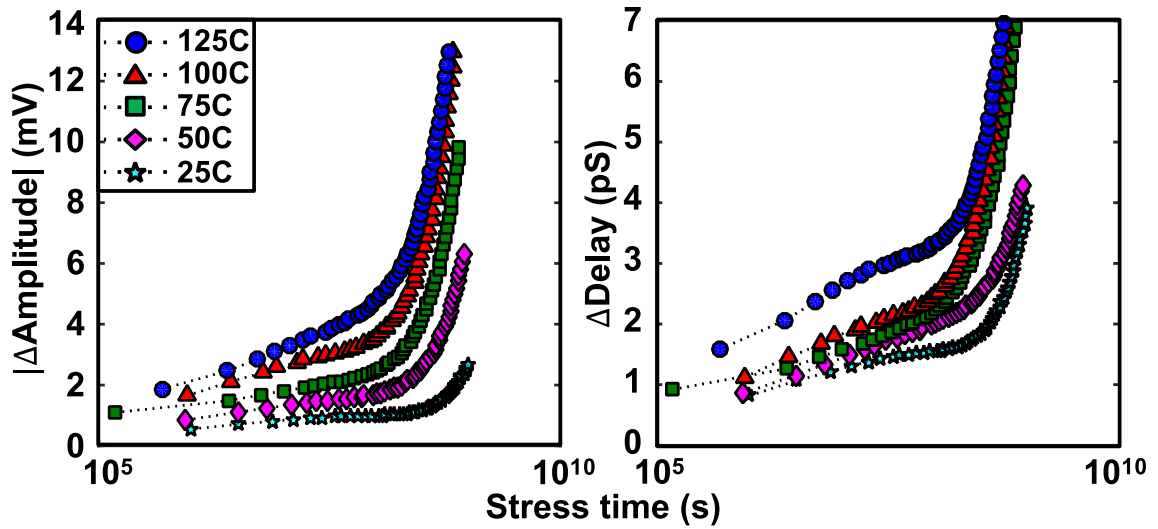
$$\Delta V_{th.amp} = g_1(T, V_{DD}) \cdot \Delta D^{g_2(T, V_{DD})} + \delta_a(T, V_{DD}) \quad (10)$$

where $f_{1,2}(T, V_{DD})$, $g_{1,2}(T, V_{DD})$, and $\delta_{d,a}(T, V_{DD})$ are the fitting constants which are functions of stress conditions (temperature (T) and supply voltage (V_{DD})).

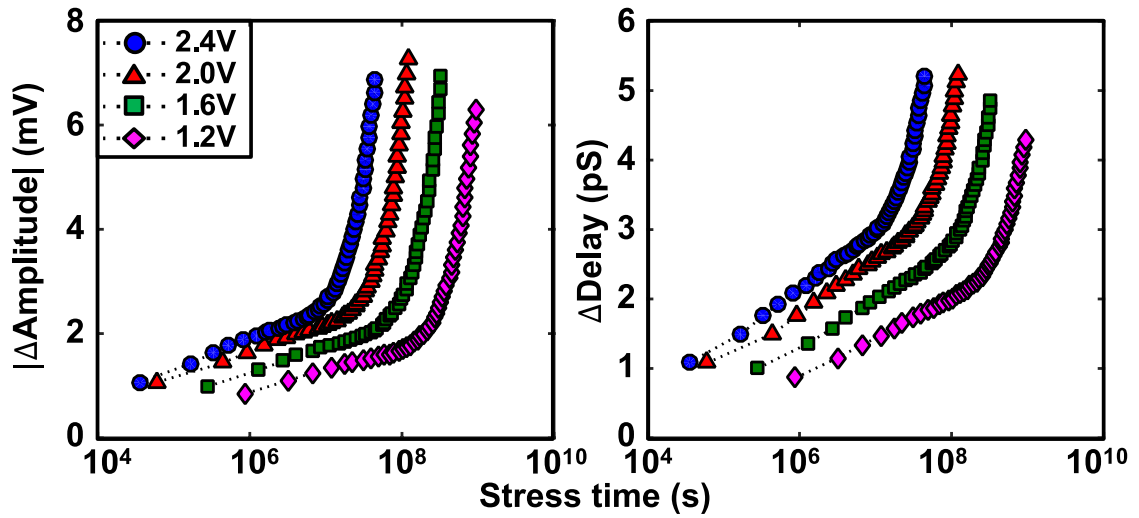
Then, in order to improve accuracy, the two functions are combined together, with the fitting coefficient, ξ :

$$\Delta V_{th} = \xi \cdot \Delta V_{th.del} + (1 - \xi) \cdot \Delta V_{th.amp} \quad (11)$$

In Eq. (3) and (5), because $\varphi(T, E_{F,eff})$ increases as a function of temperature and gate voltage, the shift in threshold voltage become larger for larger values of temperature and gate voltage at each time point, which corresponds to larger amplitude and delay shifts at the peak points of the ground signature signal.



(a)



(b)

Fig. 3.5. (a) Temperature dependence of the extracted data as a function of stress time with a 1.2V supply voltage. (b) Supply voltage dependence of the extracted data at a temperature of 50°C.

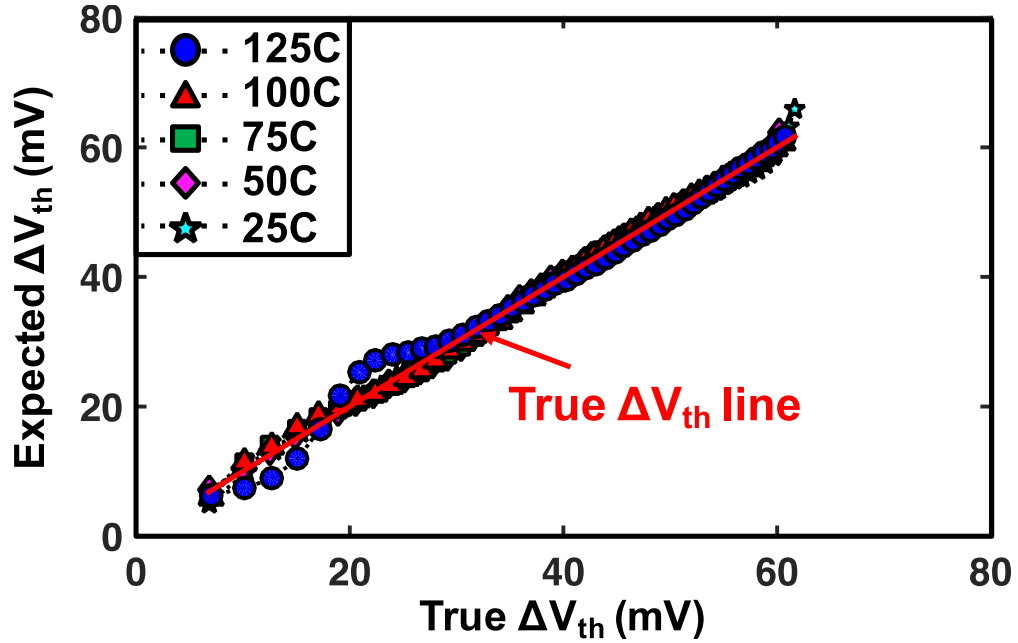


Fig. 3.6. Model vs. actual V_{th} shift at different temperatures.

Fig. 3.5(a) and (b) compare the amplitude and delay shifts at different temperatures for the same supply voltage and different supply voltages at the same temperature to show the effect of stress. The amplitude decreases and delay increases with supply voltage and temperature. Using the degradation data in Fig. 3.5(a) and (b), we fit the degradation data using Eqs. (7) and (8) to extract the estimated shift in threshold voltage and combine them with Eq. (9). Fig. 3.6 compare the average threshold voltage shifts with the true shift in threshold voltage to show the accuracy of our model at the 1.2V supply voltage. The data are fit for several stress conditions (supply voltages: 1.2~2.0V, and temperatures: 25°C~125°C) with Eq. (9), and the standard error is less than 3.5mV. Given an extracted threshold voltage shift as a function of time and temperature, computed using the model in Eq. (9), the model parameters in Eq. (3), A_{NBTI} and B_{NBTI} , can be computed. We need to check if our methodology can correctly extract NBTI model parameters using signature

TABLE 3.1.
THE % ERROR IN COMPUTING THE COEFFICIENTS IN EQ. (1)

Chip		Microprocessor		FPU		FIR	
Test Bench		Add	Cache	Add	FTI	Toggle	DC
A_{NBTI}	μ	2.91	2.82	2.27	2.02	1.23	1.11
	σ	0.31	0.41	0.62	0.75	0.82	0.92
B_{NBTI}	μ	1.90	1.83	1.32	1.31	1.25	1.17
	σ	0.32	0.45	0.64	0.78	0.85	0.96

data. To do this, we assume process-level values are given for coefficients A_{NBTI} and B_{NBTI} in Eq. (3).

Each device is assigned a random initial threshold voltage. NBTI degradation models are applied to each device, and the degraded signature signal is simulated. From the degradation of the signature signal, the shift in amplitude and delay is found, and the average degradation in threshold voltage is estimated. From the shift in threshold voltage as a function of time, we estimate coefficients A_{NBTI} and B_{NBTI} . TABLE I shows the average and standard deviation of the error rate for each coefficient, based on several simulation runs for each of the circuits and test benches using full chip simulations. The error rates are less than 3%.

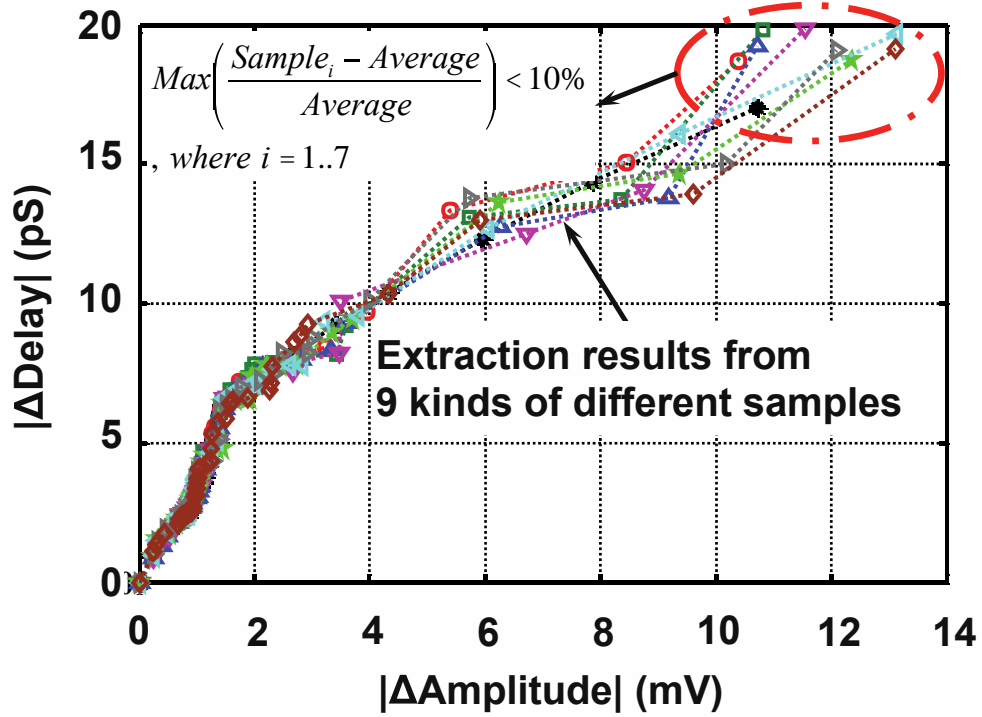


Fig. 3.7. The variation of Δ Delay and Δ Amplitude degradation for several random re-
sistance distribution samples for the microprocessor.

3.4 Data Extraction and Modeling for GOBD

We next construct a relationship between the power supply and ground signals and GOBD in circuits. Our method extracts the degradation in amplitude and shift in delay as a function of time with power/ground voltage signals. Fig. 3.7 shows the delay and amplitude degradation data for several samples. In each sample, different devices experience soft breakdown. This graph shows the effect of randomness in the selection of the SBD location and the R_{SBD} value. Although the variation among samples is increasing with time, its effect ($<10\%$) is small.

The modeling of the degraded oxide resistance and the shifts in amplitude and delay is similar to NBTI, i.e.,

$$\mu(N_{trap})_{del} = h_1(T, V_{DD}) \cdot \Delta D^{h_2(T, V_{DD})} + \varepsilon_d(T, V_{DD}), \quad (12)$$

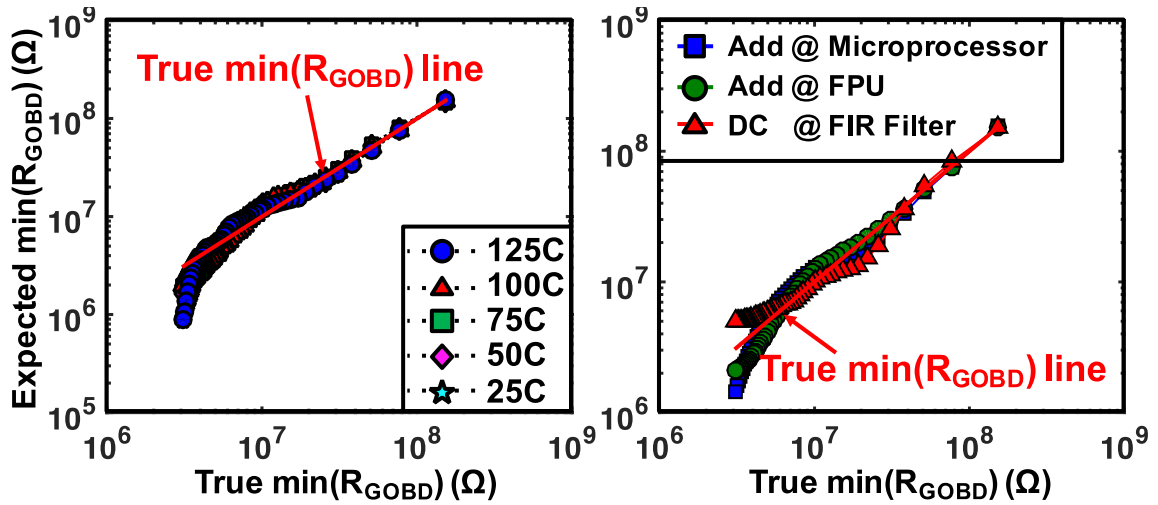
$$\mu(N_{trap})_{amp} = k_1(T, V_{DD}) \cdot |\Delta A|^{k_2(T, V_{DD})} + \varepsilon_a(T, V_{DD}), \quad (13)$$

$$\mu(N_{trap}) = \xi \cdot \mu(N_{trap})_{del} + (1 - \xi) \cdot \mu(N_{trap})_{amp}, \quad (14)$$

where $h_{1,2}(T, V_{DD})$, $k_{1,2}(T, V_{DD})$ and $\varepsilon_{a,d}(T, V_{DD})$ are fitting coefficients, which are a function of the stress conditions for Eqs. (12) and (13). In Eq. (14), we combine Eqs. (12) and (13) by using a fitting constant, ξ , to use both delay and amplitude variable for better fitting result.

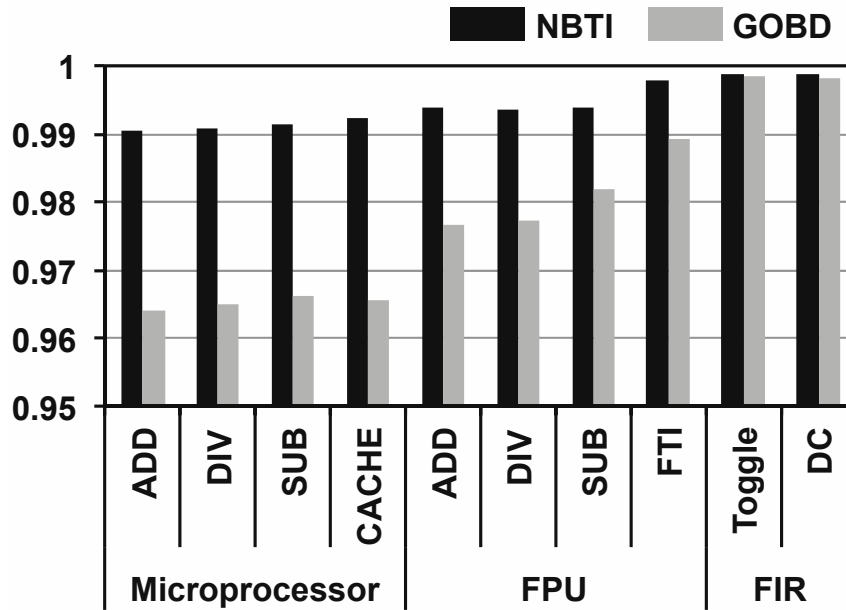
As we can see with Eqs. (10)-(12), first, we calculate the number of defects for every MOSFETs in a system. Based on the number of defects, we use PM simulation to compute the number of conduction paths and QPC model to compute the estimated R_{SBD} for each MOSFET. Then, we apply the R_{SBD} values to individual MOSFETs, and analyze the degradation of the power and ground signature signals.

Then, we compare the applied the average number of defects to the MOSFETs to the corresponding delay and amplitude degradation data computed from the power and ground signatures to find the fitting constants for Eqs (12)-(14).



(a)

(b)



(c)

Fig. 3.8. Evaluation of the system-level GOBD model. (a) Temperature dependence of the model vs. actual R_{SBD} with a 1.2V supply voltage. (b) Testbench dependence of the Model vs. actual R_{SBD} degradation with a 1.2V supply voltage. (c) R-Square value for each test bench and several circuit designs.

Fig. 3.8(a) and (b) compare the accuracy of Eqs. (12) and (14) for several temperatures and several test benches, respectively. They show an estimate of the minimum resistance (most worn out MOSFET) in comparison with the actual minimum resistance in the circuit under SBD. They compare the applied minimum resistance with the oxide resistance computed from the ground signature using out model.

Fig. 3.8(c) presents the GOBD and NBTI model accuracy using R^2 , the coefficient of determination. To make a comparison, parameter values (A_{GOBD}, β) in Eq. (5) are assumed. These are applied to generate a GOBD resistance distribution. The signature is computed and used to extract N_{trap} with Eq. (6). The results are then used to compute R^2 in Fig. 3.8(c). The CACHE and FTI test benches stress fewer MOSFETs compared to the other arithmetic test sets, and it appears that the model is more accurate if a smaller number of MOSFETs are stressed. On the other hand, the shift is smaller, which impacts our ability to determine model parameters experimentally.

CHAPTER 4

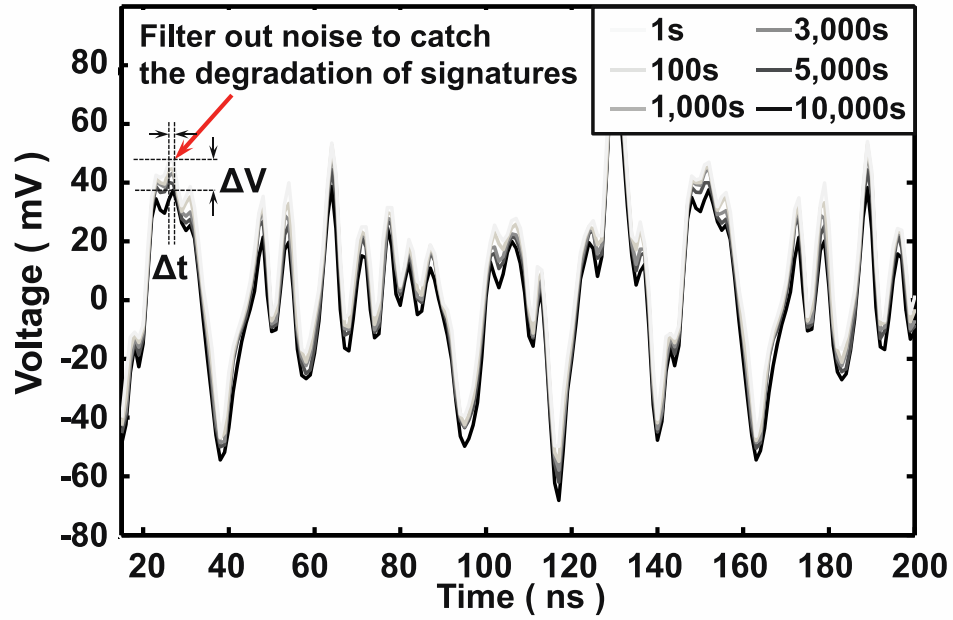
MEASUREMENT STUDY: EXPERIMENTAL DATA COLLECTION, ESTIMATION, AND ANALYSIS USING CHIPS

The iterative procedure that was used for simulation data is now applied to experimental data. Namely, initially the GOBD parameters were estimated at higher supply voltages. Next NBTI parameters were estimated at lower supply voltages, after subtracting the effect of GOBD. The iterative process continues until convergence, as mentioned in Chapter 3.

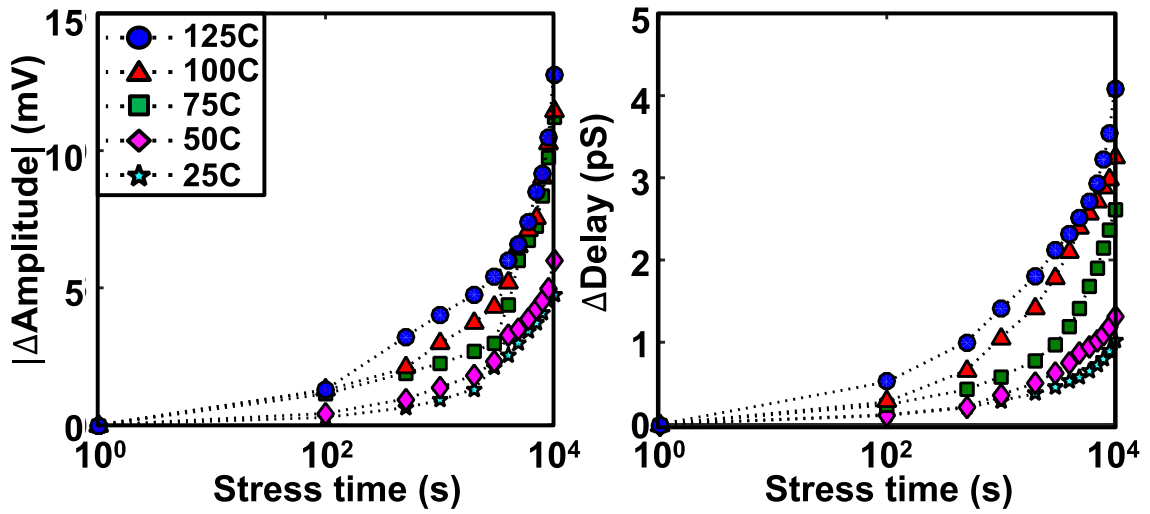
4.1 Data Collection for NBTI

The V_{th} degradation models have been applied to extract NBTI parameters for several microprocessor test chips. In this case study, we considered supply voltages of 1.4V, 1.6V, and 1.8V, and temperatures of 40°C, 60°C, 80°C, 100°C, and 120°C. Our purpose is to show that shifts in the amplitude and delay of peak points in the signature signal are measureable, and hence can be used to estimate the shift in V_{th} caused by the NBTI effect.

Also, we applied a DC input signal to stress the chips in order to avoid HCI degradation which occurs during transitions of signals ($0 \rightarrow 1$ or $1 \rightarrow 0$). A dynamic test bench is applied during testing so that ground bounce signal can be observed and the amount of degradation can be measured. We have used a sampling oscilloscope and have used the “average” and “bandpass filter” functions to filter out the noise and jitter. These functions use 512 samples of the same time point to generate a stable ground signal. The sampling is every 0.2 picosecond, which is sufficient to see delay variation and degradation. The voltage resolution is also sufficient to measure the amplitude shift.



(a)

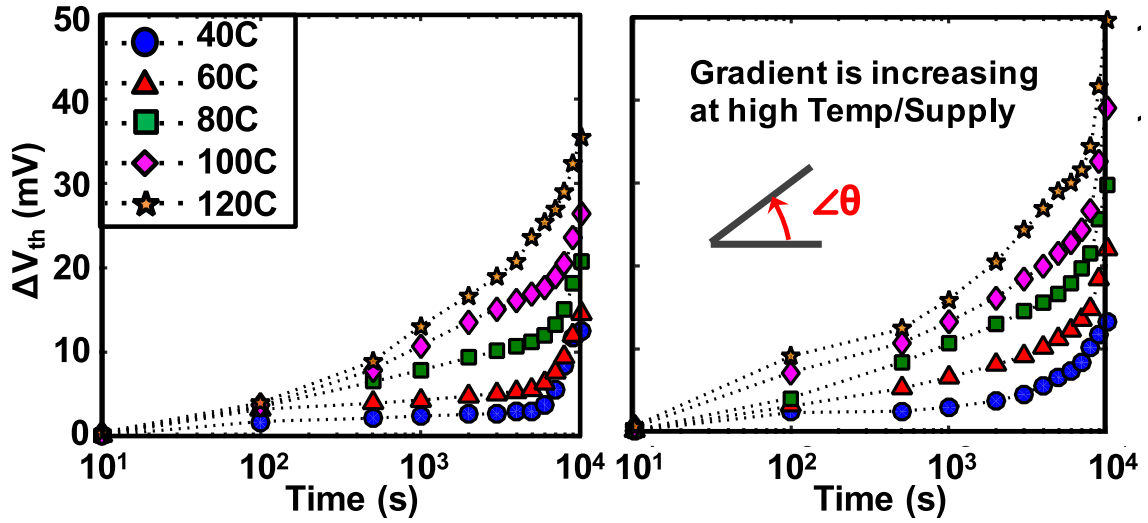


(b)

Fig. 4.1. Measurement of signature signal degradation. (a) Degradation of the ground signature signal when tested with a supply voltage of 1.6V and at a temperature of 100°C. (b) Degradation of amplitude and delay extracted from the ground signature signal for the circuit tested with a supply voltage of 1.6V.

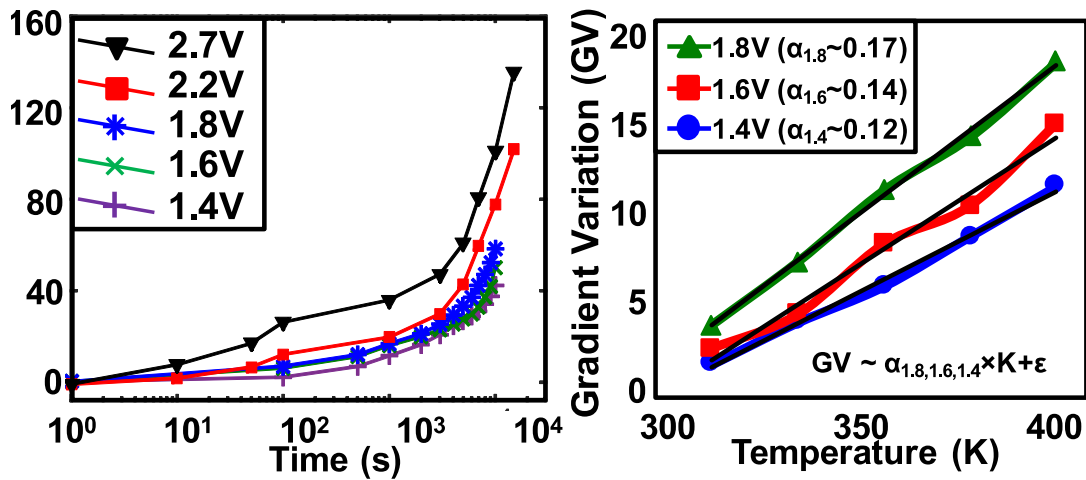
After intervals of voltage and temperature acceleration stress testing, we monitor the ground and power supply bouncing signal. The NBTI and GOBD induced ground and power supply voltage bounce was recorded with an oscilloscope, and the shifts in amplitude and delay were computed at peak points of the ground signal.

In Fig. 4.1(a), we capture the voltage signature degradation as a function of time for different input voltages and temperatures at a low supply voltage where NBTI is dominant. The extracted deg-radiation data is shown in Fig. 4.1(b).



(a)

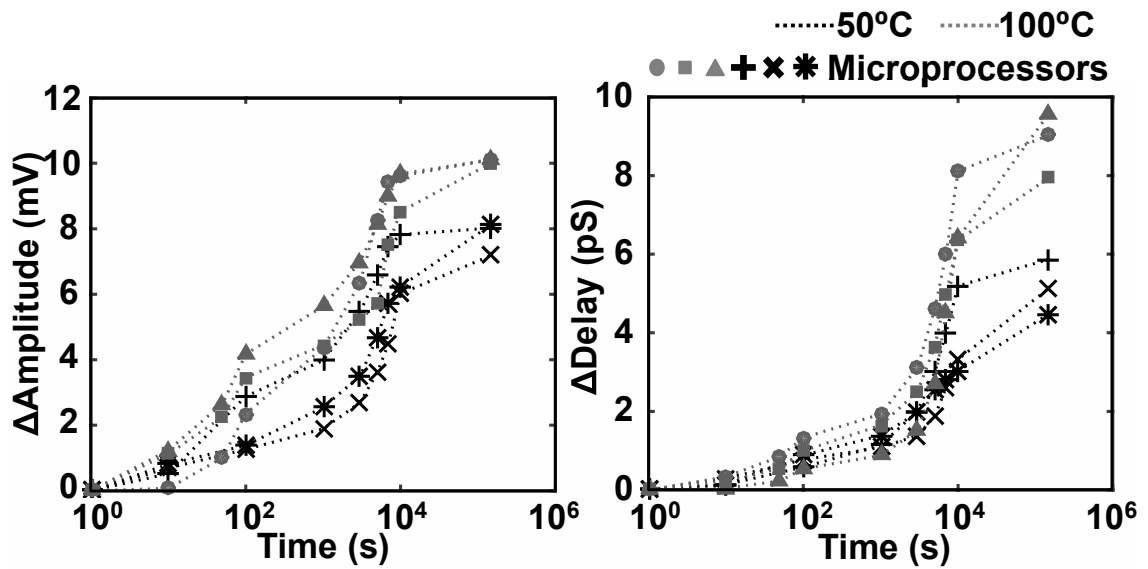
(b)



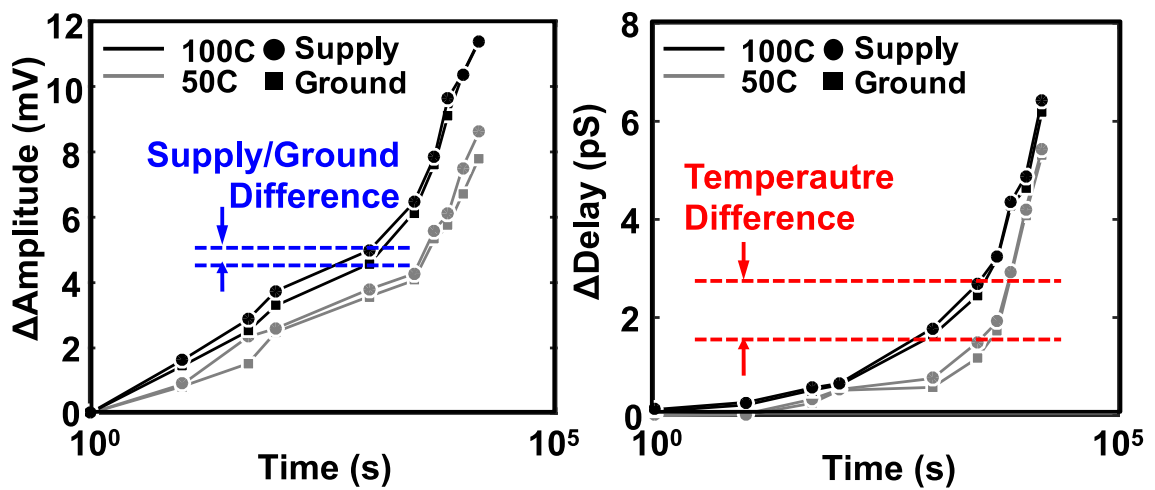
(c)

(d)

Fig. 4.2. The amount of threshold voltage degradation for the microprocessor derived by Eq. (9) for (a) input voltage 1.4V, (b) input voltage 1.6V, and (c) Temperature 100°C. (d) Temperature dependence of the threshold voltage gradient variation.



(a)



(b)

Fig. 4.3. Amplitude and delay shifts from measurements. (a) Degradation of amplitude and delay extracted from the ground signature signal tested with 2.2V and 50°C and 100°C. (b) Difference between shifts observed in the supply and ground signature signals. (This is the average of two groups of three chips stressed at 100°C and 50°C, respectively.)

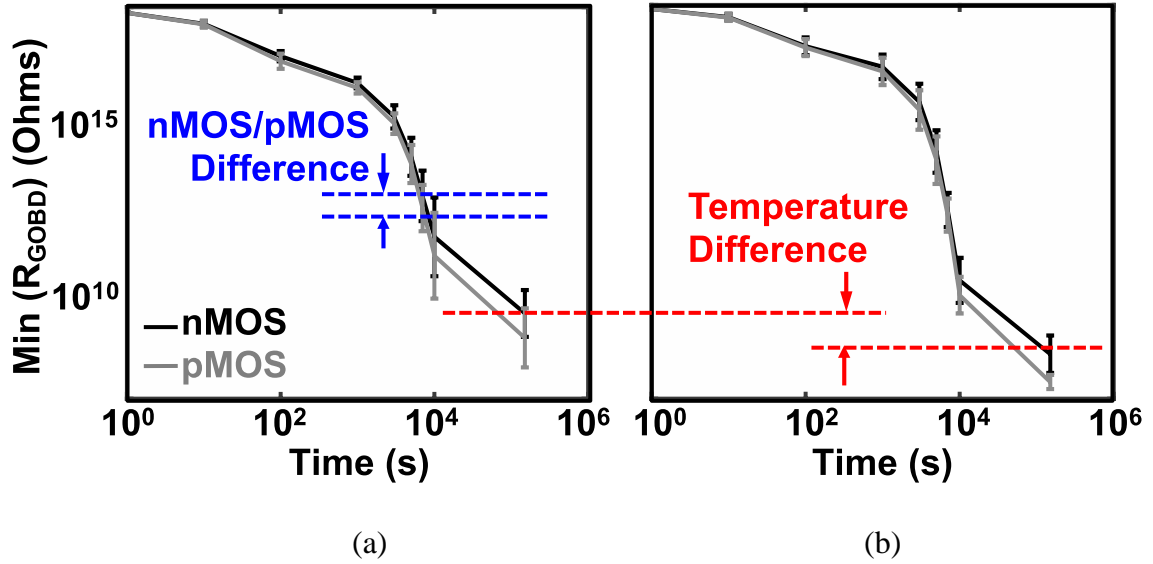


Fig. 4.4. Extracted degraded oxide resistances for nMOS and pMOS devices in the microprocessor for the stress conditions ((a)-50°C and (b)-100°C) as a function of stress time.

Using Eq. (11), the extracted V_{th} drift data are shown in Figs. 4.2(a)-(c). These degradation results are similar to data in the literature [54],[58],[71]. Also, in Fig. 4.2(d), we can see the relationship between the gradient variations (GV) of threshold voltage degradation as a function of stress time and the different applied temperatures. The α (temperature gradient) is increasing as a function of the applied gate voltage, and α is similar to data in [54].

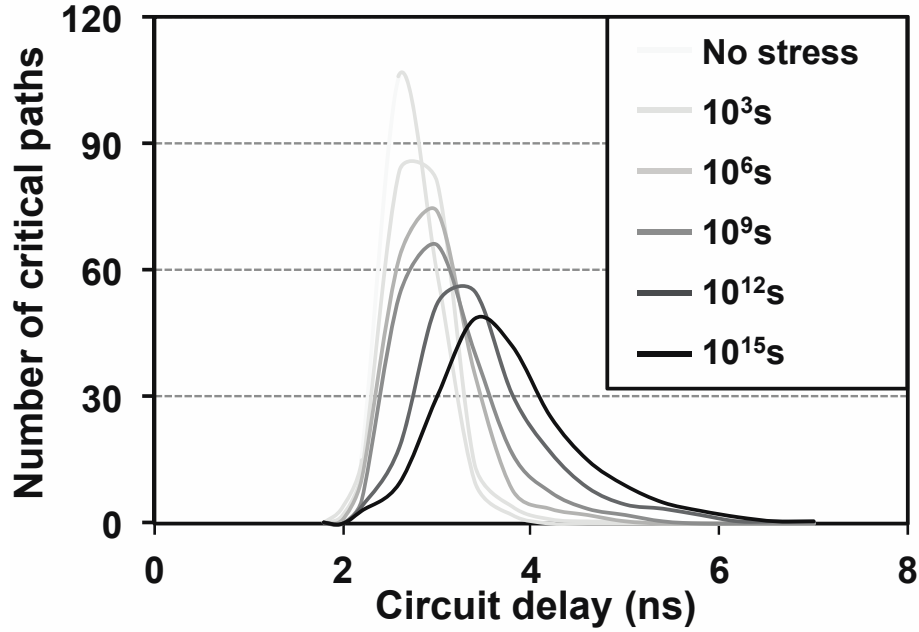
4.2 Data Collection for GOBD

The microprocessor chips were stressed with a 2.2V supply voltage, together with temperature stress. The shifts in delay and amplitude were computed. Fig. 4.3(a) shows the shifts in delay and amplitude were computed. Fig. 20(a) shows the shifts in amplitude and delay for several microprocessors with different temperatures (50°C and 100°C). It is

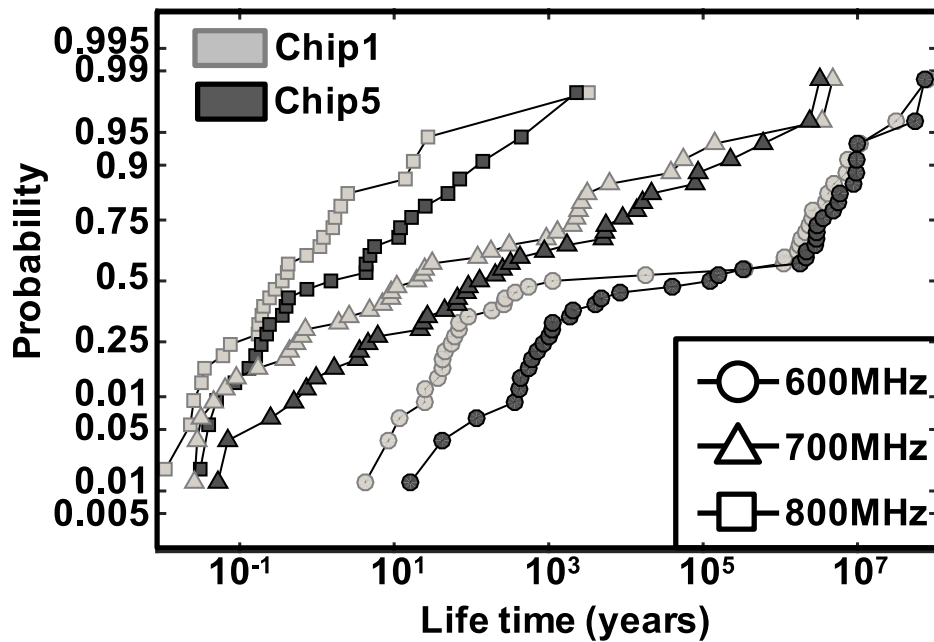
evident that the shift is larger for higher temperatures. The ground signature signal is affected by nMOS degradation, while pMOS degradation causes shifts in the power supply signature signal. Therefore, we use both the ground and power supply signature signals to extract both the nMOS and pMOS oxide degradation resistances.

The ground and power supply shifts are shown in Fig. 4.3(b), which is the average shift of the two groups (50°C and 100°C) of the six microprocessors. The amplitude degradation results show that the supply degradation is slightly larger than the ground degradation, and the difference is larger for tests at higher temperatures. This result matches previous experimental results which compare degradation in nMOS and pMOS devices [58],[71], and experimentally show the temperature dependence of GOBD [72].

Based on the shift data, we extracted the average number defects per MOSFET and calculated the worst degraded oxide resistance as a function of stress time in Fig. 4.4. As expected, the results show that nMOS degradation is less than pMOS degradation, and higher temperatures cause MOSFETs to degrade more quickly. Moreover, variation increases.



(a)



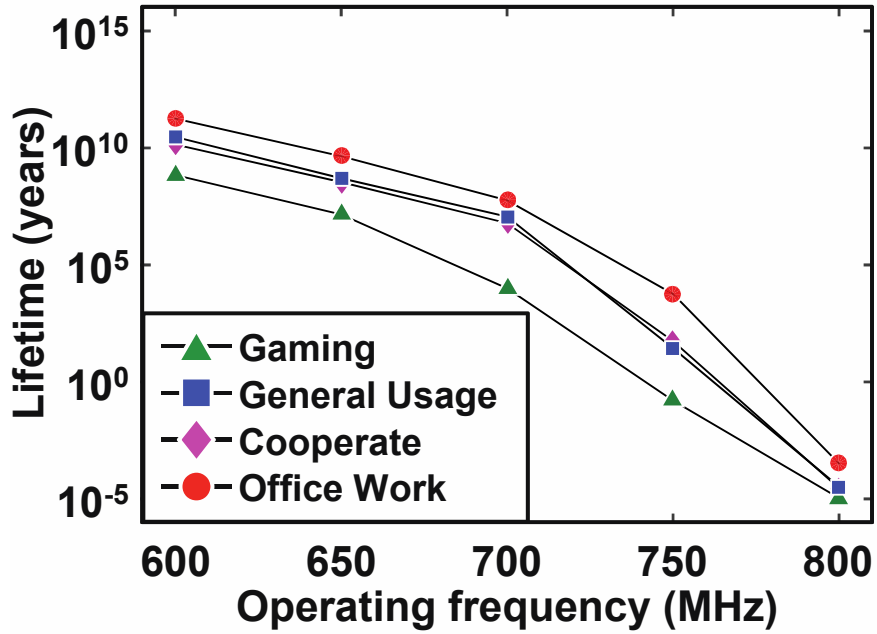
(b)

Fig. 4.5. System-level dynamic timing analysis result for the NBTI and GOBD effect. (a) The delay degradation of the top 100 critical paths as a function of stress time. (b) Lifetime distribution comparison between Chip 1 and Chip 5 for a set of operating frequencies.

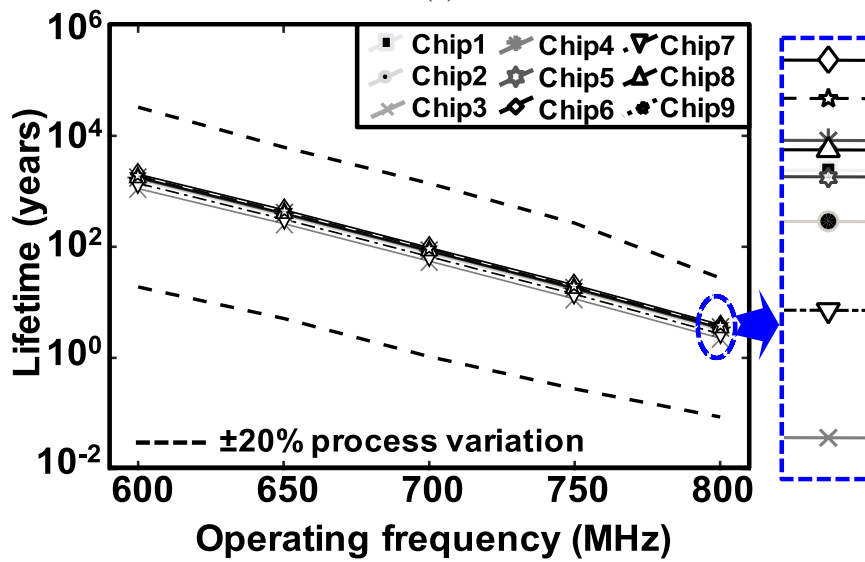
4.3 Performance Degradation and Lifetime Analysis

In order to further study the joint impact of NBTI and GOBD on a RISC microprocessor, we use statistical timing analysis in order to extract the critical paths of the system [73],[75]. This method extracts paths using samples from the full PV space, and hence provides a more complete set of critical paths. After the selection of paths, Monte Carlo analysis determines the distribution of delay. Extending statistical characterization for standard cells to full paths has to deal with two challenges. One is the gate-by-gate accumulated transition-time error per stage, and the other challenge relates to the PV affected input capacitance of a standard cell.

In order to address these problems, the method in [73] consists of gate-level models constructed with Multivariate Adaptive Regression Splines [74] and Pi-models for the interconnect network [75]. The statistical timing analysis methodology in [73] combines a block-based method to select the critical paths and a path-based method to compute the delay distribution with SPICE-level accuracy. It is not sufficient to just perform timing analysis to determine the impact of NBTI and GOBD on lifetime. It is also necessary to determine the time under stress and temperature experienced by each device [57]. Stress is a function of the test bench and the use scenario. $\varphi(T, E_F)$ is calibrated by the test conditions for each device to enable simulation of BTI. The breakdown resistances for GOBD are similarly calibrated. Fig. 4.5(a) shows the number of critical paths as a function of stress time. It can be seen that the delays of critical paths degrade and the variation of delays increases as a function of time. The operating frequency degrades accordingly. Fig. 4.5(b) compares the lifetime distribution of ‘Chip 1’ and ‘Chip 5’ for several operating frequencies. Because timing violations determine the operating frequency, as the operating frequency



(a)



(b)

Fig. 4.6. (a) Median lifetime as a function of operating frequency to show the work-load dependence. (b) Lifetime as a function of operating frequency for each individual micro-processor chip based on the NBTI and GOBD parameters extracted for each chip. The dotted lines indicate the impact of process variations on lifetime. A 10% standard deviation in channel length and threshold voltage has been assumed.

increases the timing margins decrease and the lifetime decreases. Fig. 4.6(a) shows the workload dependence of the median lifetime as a function of the operating frequency. We can see that the gaming workload causes the most stress. Fig. 4.6(b) shows the median lifetime as a function of frequency for each individual chip, based on the extracted NBTI and GOBD parameters. Each chip has unique values of NBTI and GOBD parameters. The extracted NBTI parameters primarily affect the slope of the lifetime as a function of the operating frequency (B in Eq. (3)). This causes the lifetime of some chips to be more sensitive to operating frequency. The dotted lines in Fig. 4.6(b) indicate the two-sigma confidence bounds on the lifetime due to process variations. It can be seen that process variations have a significant impact on lifetime. Initial process parameters affect the intercept of the x-axis (A in Eq. (3)). As a result, some chips start out more vulnerable to NBTI and GOBD.

4.4 Performance Analysis with Parameter Extraction

Note that in Fig. 4.6(b), the confidence bounds caused by process variations are very wide. They are wide because of uncertainty in process parameters. For process parameter extraction, we consider four parameters for each chip: the channel lengths of nMOS and pMOS devices and the average threshold voltages of nMOS and pMOS devices. In order to extract these parameters, the output delay and transition times of nine outputs were measured. We have used an experimental design involving a Taguchi orthogonal array [76] to simultaneously vary each of the four parameters (nMOS and pMOS channel lengths and threshold voltages). To determine the sensitivity of each output (delay and transition time) to each of the parameters, equations were determined for each of the outputs (nine delays and nine transition times) using linear regression [77]. The equations are of the form: $y=A+Bx$, where y is a vector of the 18 outputs, x is a vector of the four

TABLE 4.1
EXTRACTED PROCESS PARAMETERS

Chip	1	2	3	4	5	6	7	8	9
nMOS L (nm)	83	83.1	84.1	82	83.3	83.2	83	83.4	83.4
pMOS L (nm)	113	113	112	114	113	113	113	113	113
nMOS V_{th} (mV)	206	203	203	202	205	206	202	204	204
pMOS V_{th} (mV)	-144	-144	-144	-143	-144	-144	-144	-144	-144

process parameters, A is a 18-dimensional vector, and B is a 18 x 4 dimensional matrix. Simulation data determines the parameters in A and B , and measured data determines y . The best fit for parameters is estimated with:

$$x = (B^T B)^{-1} B^T (y - A). \quad (13)$$

We determined that the 18 outputs provide sufficient degrees of freedom for accurate parameter extraction. The extracted parameters are shown in Table 4.1. Given the extracted parameters, one remaining source of uncertainty is within-die variation.

Even with parameter extraction, we determined that there are some differences between the simulated vs. measured delays, due to unmodeled parasitics and parameters. By comparing the predicted vs. measured delays, we found that the measured delays are 2ps larger, and the standard deviation of unmodeled errors is 10.4ps.

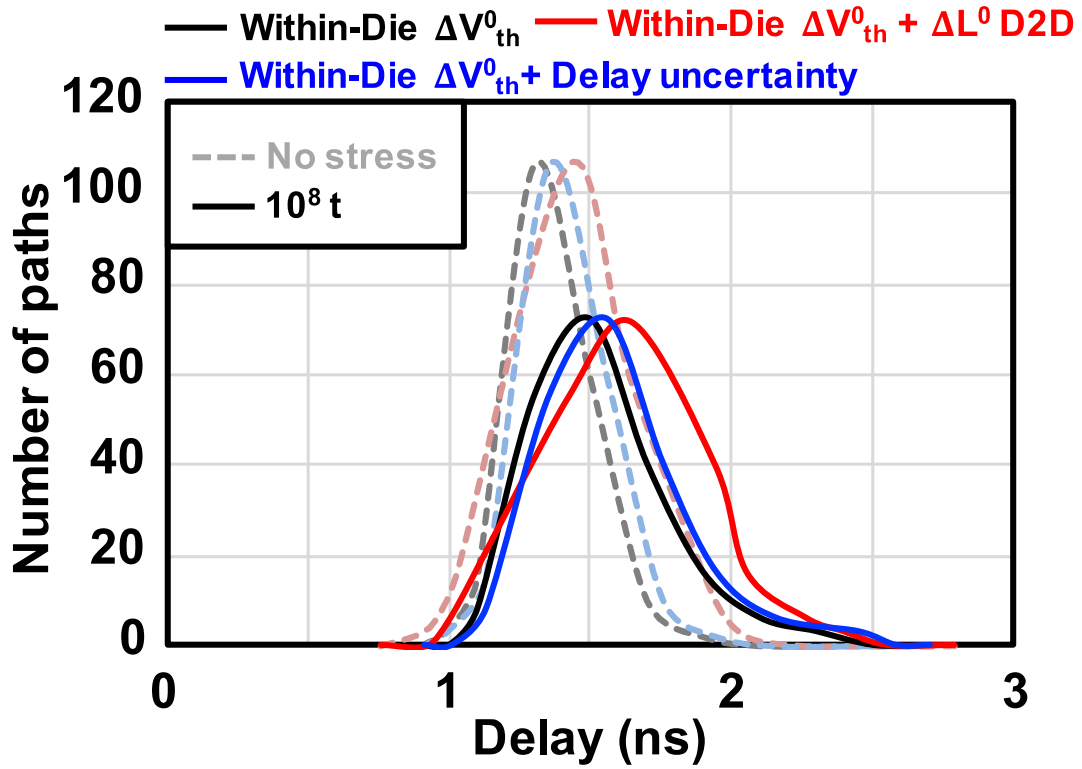


Fig. 4.7. Critical path delay distribution before (red) and after (black) parameter extraction, together with added uncertainty in the extracted delay (blue). Dotted lines correspond to no stress and solid lines correspond to the stressed case.

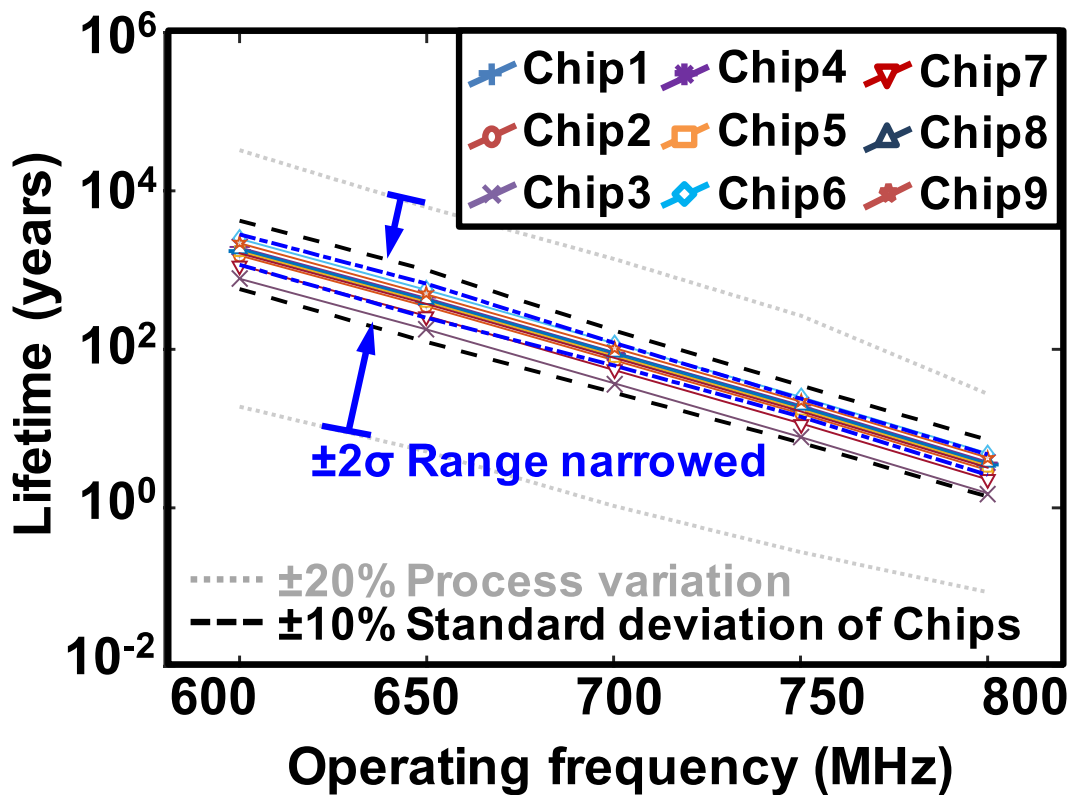


Fig. 4.8. Median lifetime as a function of operating frequency for each individual micro-processor chip based on the NBTI and GOBD parameters extracted for each chip. The dotted lines indicate the impact of process variations and uncertainty in delay on lifetime. A 20% standard deviation in within-die threshold voltage variation has been assumed.

Fig. 4.7 shows the impact of variation on the critical path delay distribution for three cases: (a) die-to-die random variation in channel length and random within-die variation in threshold voltage (the case where no process variation data is extracted), (b) random within-die variation in threshold voltage (the case with extracted mean values for channel length and threshold voltage), and (c) random within-die variation in threshold voltage and variation due to unmodeled errors in delay. It can be seen that the impact of unmodeled errors is small. The revised confidence bounds, accounting for both unextracted within-die variation in threshold voltage and unmodeled errors between observed and estimated delays are shown in Fig. 4.8. It can be seen that the process variations have a significant impact on lifetime, and with better parameter extraction, the lifetime uncertainty decreases substantially. Note that the variation among our chips is not large. This is due to the fact that the chips came from a single lot.

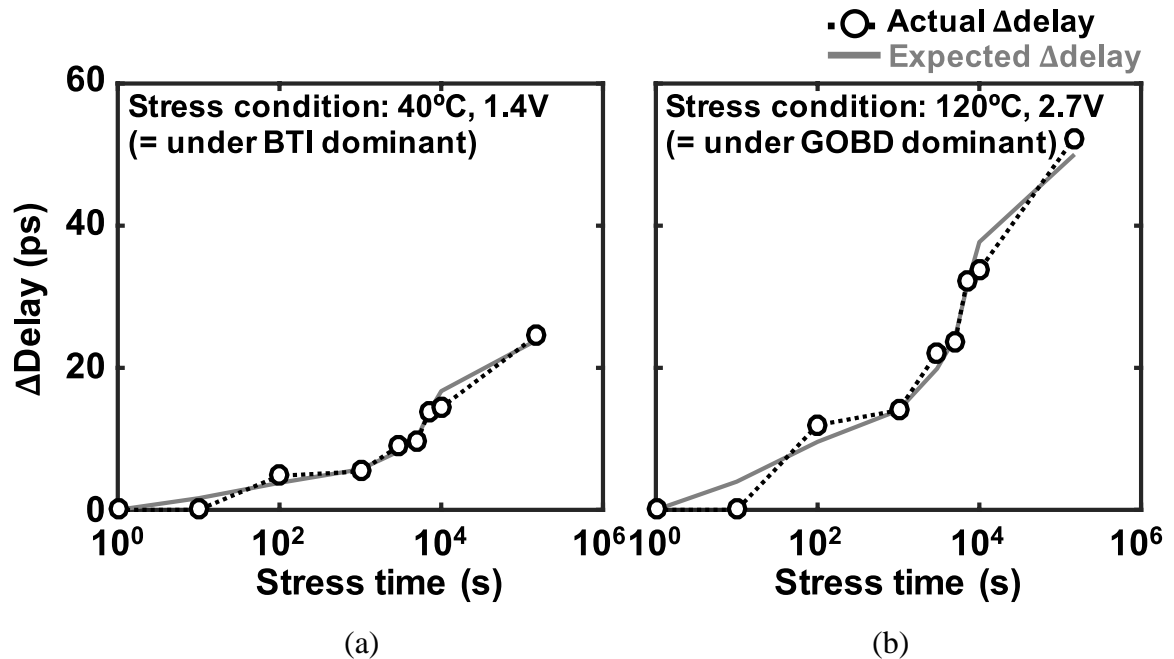


Fig. 4.9. Comparison result between the measured delay degradation data for an output of a chip (Microprocessor) and the delay degradation computed using simulation, calibrated with extracted parameters from the power supply and ground bounce signals. (a) Delay comparison under the BTI dominant case (40°C, 1.4V). (b) Delay comparison under the GOBD dominant case (120°C, 2.7V).

4.5 Verification of Measurement Results

Fig. 4.9 shows a comparison between the actual circuit output port delay degradation and the simulated critical path delay to the output port. After we calibrated the model parameter for the chip and stress condition and, the estimated result is pretty well matched with the measured actual path delay degradation.

CHAPTER 5

DESIGN STUDY: DESIGN FOR RELIABILITY AND YIELD ENHANCEMENT

The lifetime of the system is affected by reliability and PV. In Fig. 5.1, let's say that the red combinational logic path (Data1) is vulnerable to a setup time violation. Such a setup time violation can be caused by process variations and delay degradation due to BTI and GOBD. The blue critical path (Data 2) can cause a hold time violation, which can be caused by a gate-to-drain GOBD resistance and process variations. Therefore, if we have enough timing margin between the data transition and clock edge timing to avoid hold/setup time violations, the lifetime of the system will be extended. Therefore, we have proposed a clock duty cycle controller (DCC) system to manage the clock duty cycle by modifying the timing between the delay of critical paths and positive clock edges. It consists of the timing violation sensors (TVS) in a FSM controller, a DCC buffer, and a FSM.

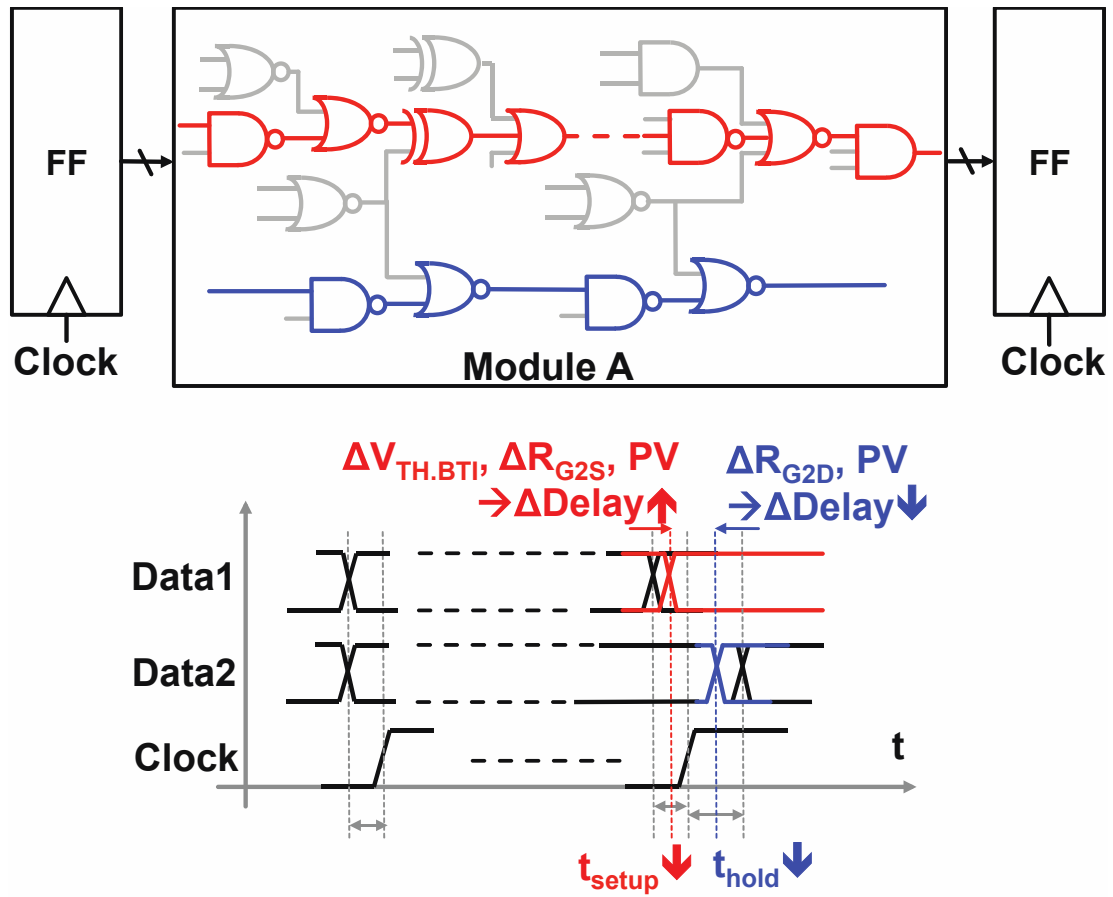


Fig. 5.1. The example of red and blue critical path delays which cause the setup and hold time violations, respectively. The red path (data1) is vulnerable to a setup time violation which can be caused by delay degradation and process variations. The blue path (data2) is vulnerable to a hold time violation which can be caused by process variations.

5.1 Self-Adaptive duty cycle controller (DCC) system

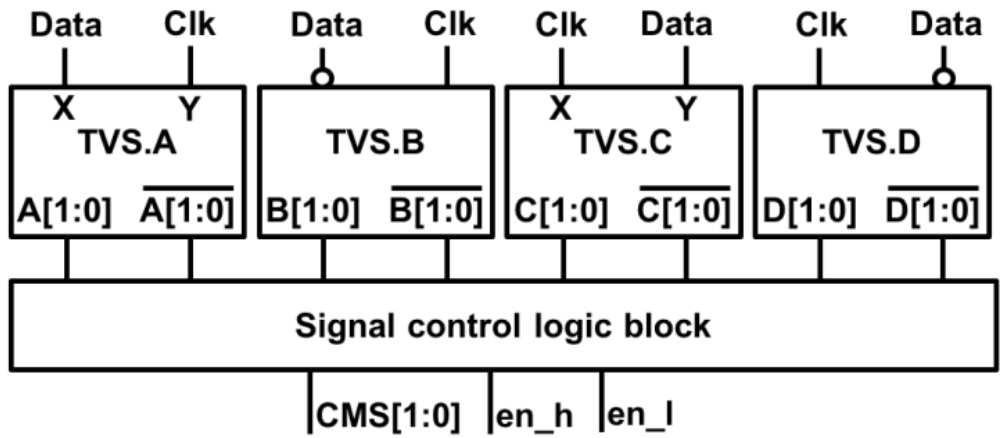
5.1.1 Timing violation sensor (TVS)

In order to control the clock duty cycle, first, a sensing circuit should monitor the timing margin between a clock edge and the data transition time. The TVS system monitors the timing gap and generates a warning signal before the degraded paths violate the setup or hold time margins.

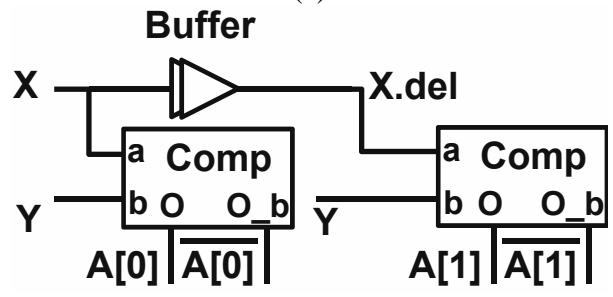
Many previous studies have proposed delay sensors, including analog sensors [78], dynamic logic-based sensors (including latches and stability checkers) [41-42],[79-80], and sensors involving both analog (the comparator) and dynamic logic (flip flops) [39],[81]. We have implemented the third type of sensor. Our proposed system uses a positive feedback comparator between two input signals (clock and data) which avoids errors due to RC delay mismatch. More details can be found in [81].

Our proposed system uses a positive feedback comparator between two input signals (clock and data) which avoids errors due to RC delay mismatch. It generates a trigger signal before a delay error occurs [81]. The TVS system must monitor two transition cases (0->1 and 1->0). Therefore, the timing violation sensor (TVS) must be aware of both rising and falling signals. Moreover, to generate a proper warning signal for a timing violation, the system must detect both hold and setup time violations.

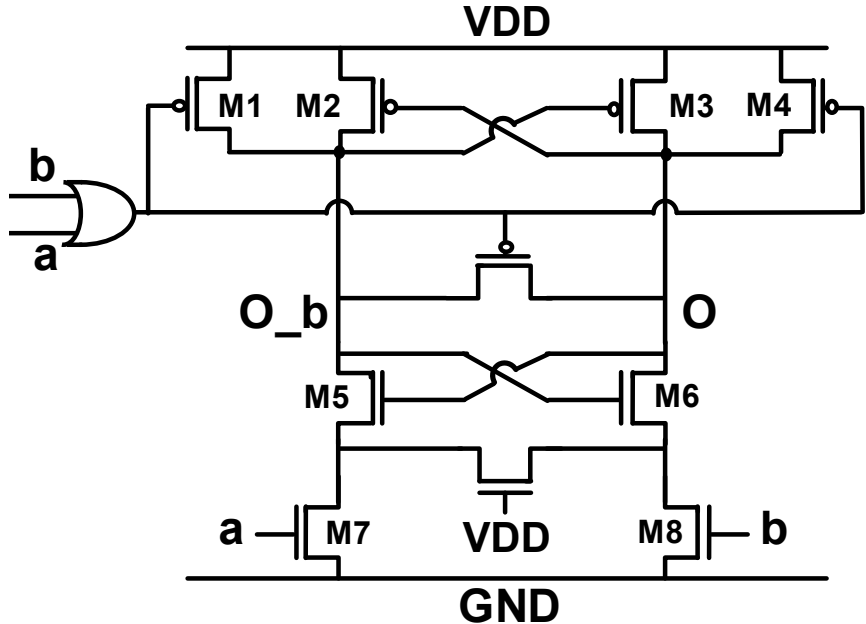
To detect a setup time violation, an additional buffer is added to the data path, and for a hold time violation, the buffer is added to the clock path. In order to recognize each case (a total of four cases), we modify the input signals for each TVS.



(a)



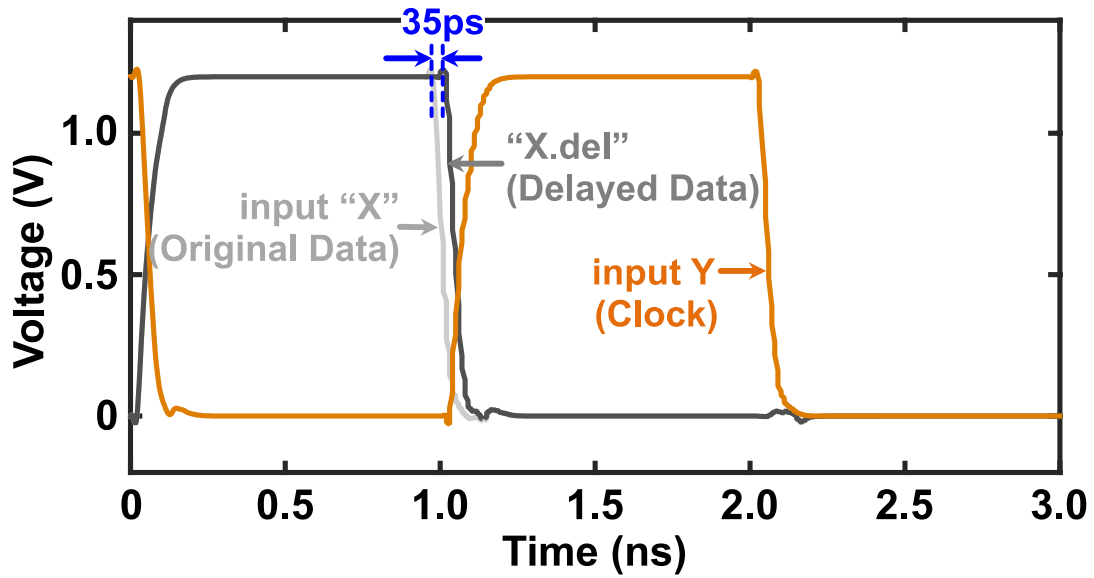
(b)



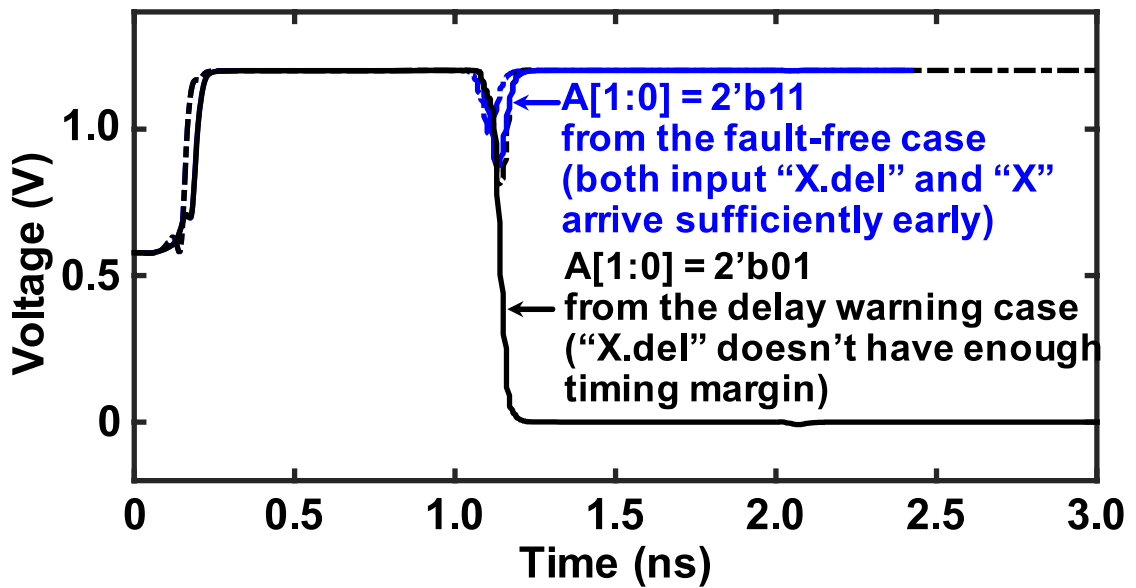
(c)

Fig. 5.2. Sensing a timing margin between a clock edge and a data transition. (a) The timing violation sensors (TVSs) connected to a FSM controller. (b) A timing violation sensor (TVS). (c) A comparator, which is inside the TVSs.

We need two TVSs for setup time and two TVSs for hold time, as shown in Fig. 5.2(a). In Fig. 5.2(b), each TVS consists of two comparators [81] with one buffer. For the setup time sensors, X is the data path and Y is the clock path, and vice versa for the hold time sensors. The comparator consists of positive feedback amplifiers, as shown in Fig. 5.2(c). The sense amplifier has two positive feedback loops, (M2, M3) and (M5, M6). If a rising signal (0->1) on input 'a' arrives sufficiently earlier than input 'b', the outputs 'O_b/O' become '0/1'. Conversely, if the input 'b' arrives earlier than 'a', the output 'O_b/O' become '1/0'. To check the timing violation detection range, we consider the 10% process variation. Also, for the degradation effect, we assume that, because O_b/O will be 0/1 state for the normal status (no violation), M3 and M5 are fully stressed and others are equally degraded during operation. After 10year operation, it can detect up to 5ps range to sense the delay between input 'a' and 'b'.



(a)



(b)

Fig. 5.3. (a) An example case of the lack of a timing difference between a clock edge and X.del, where the delay of input X is increased to input X.del. (b) The comparator output is changed from 2'11 to 2'01.

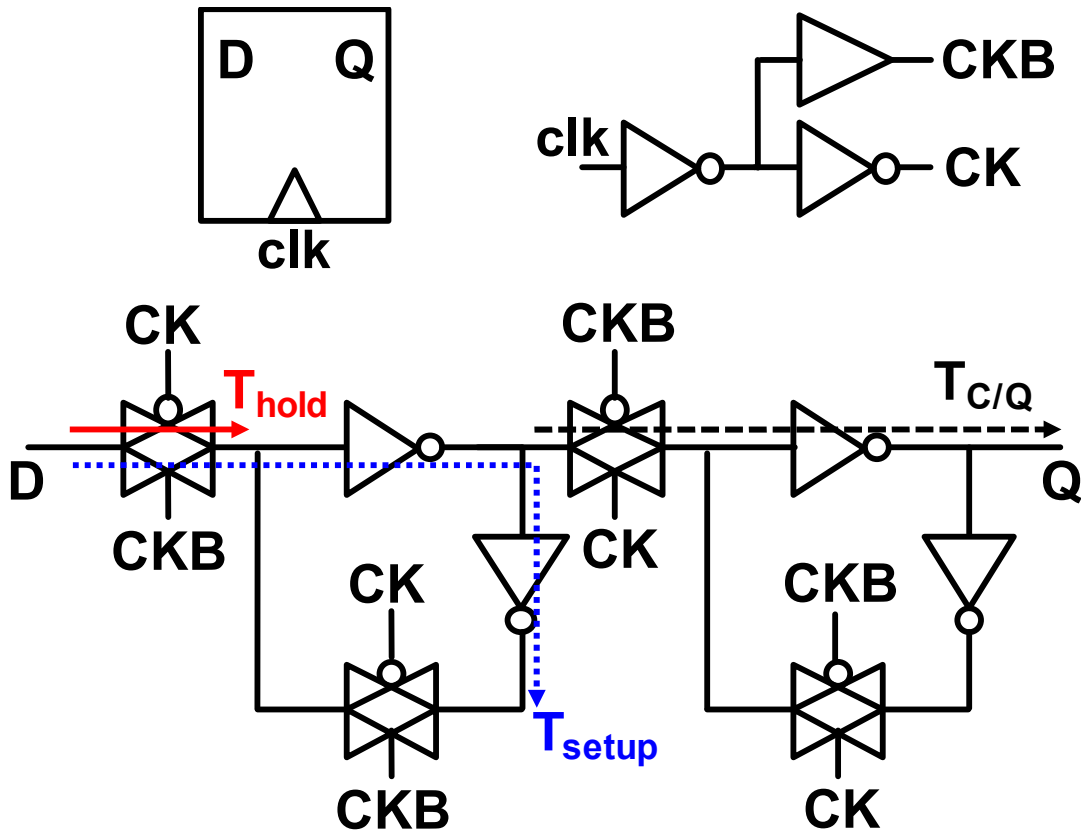
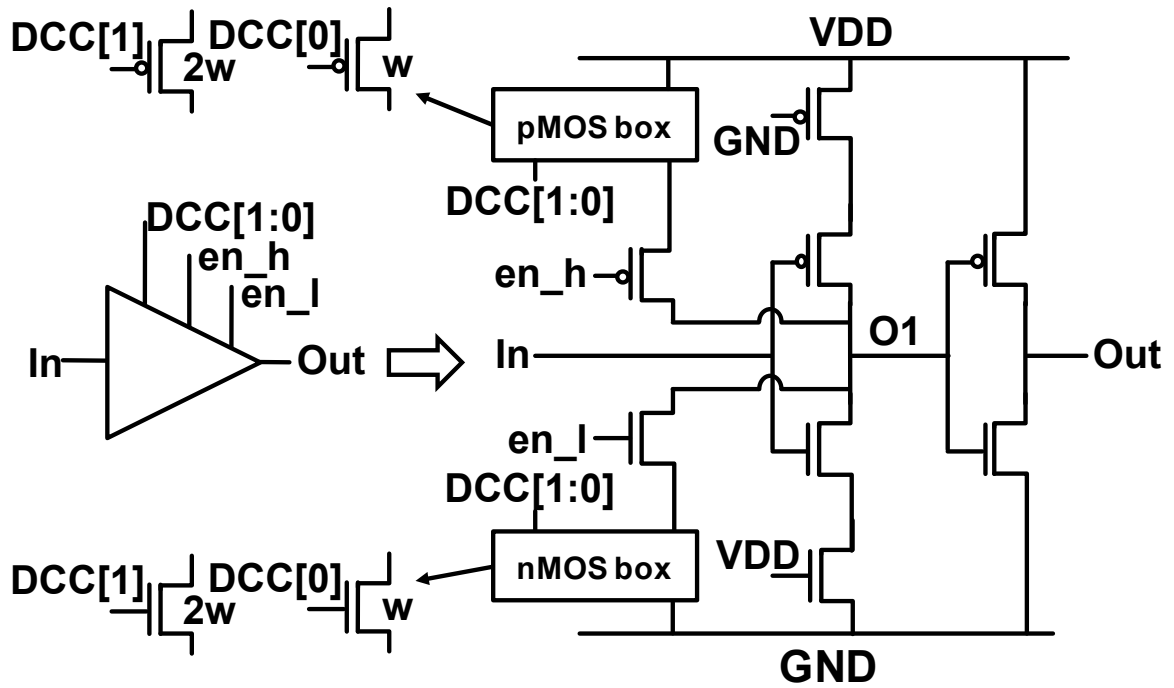


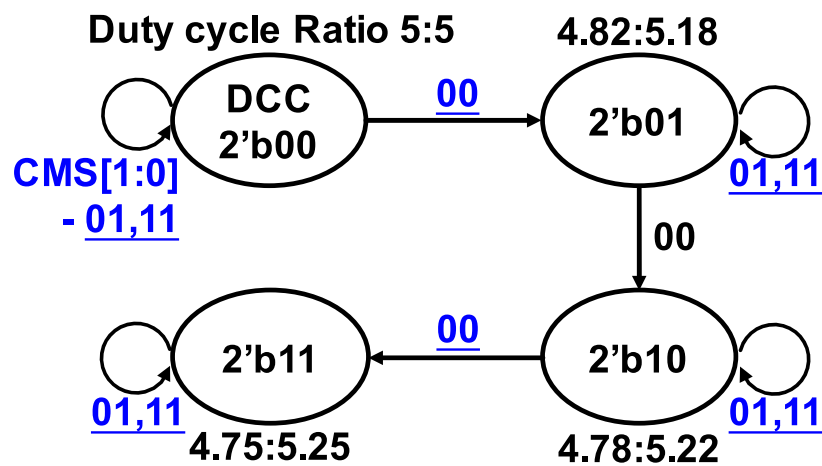
Fig. 5.4. A flip flop used in the DCC system.

Fig. 5.3 shows an example of how to detect when duty cycle correction is required for the falling data signal case (1->0). Because of delay degradation, the comparator cannot differentiate the timing of the clock edge and delayed data signal (X.del and Clk in Fig. 5.2(b)), which means that the TVS sensor output becomes '0'. Then, because A[1] is the comparison result of the timing difference between delayed data (caused by the buffer) and the clock, the A[1] signal becomes zero. Therefore, A[1:0] becomes 11->01.

The flip flops are connected at the end of the data paths. The setup and hold time margins are a characteristic of a FF. The buffer delay should be chosen properly to avoid timing violations for the FF. We designed a flip flop (FF) in Fig. 5.4 has setup and hold time margins of $25\text{ps} \pm 10\text{ps}$ (because of PVT variation and aging). Therefore, in order to cover the timing violation range, the buffer is designed to have a 35ps delay from X to X.del in Fig. 5.2(b). Based on the TVS output signal, the signal control logic block generates the control bits, CMS[1:0], and the signals, en_h and en_l, for different scenarios and delay degradation cases.



(a)



(b)

Fig. 5.5. Duty cycle controller (DCC) module. (a) Duty cycle controllable (DCC) buffer.

(b) A DCC finite state machine (FSM) to generate the DCC[1:0] signal to control the DCC buffer.

5.1.2 Duty-cycle controllable buffer

Based on the control signals from the TVS, we need to manage the clock duty cycle to manage the timing of the clock edge. For example, the clock edge timing should be pushed back to give enough setup time margin or moved forward to increase the hold time margin between the sequential logic and critical combination paths. Therefore, if the clock duty cycle ratio is adjustable, we can not only avoid timing violations, but also there is no performance degradation of the system, because the system operating frequency is not affected. The clock duty cycle ratio is adjustable using the DCC buffer in Fig. 5.5(a).

The buffer consists of two inverters (an inverter chain). The pMOS and nMOS transistor arrays (pMOS and nMOS boxes) are located between two inverters. DCC[1:0] controls the pMOS and nMOS boxes. There are additional MOSFETs to connect the output O1 and each box. The DCC[1:0] bit is generated by the finite state machine (FSM) in Fig. 5.5(b) which is controlled by the CMS[1:0] bit (Controller Mode Select) which is from the timing violation sensor (TVS) in Fig. 5.2(a). By controlling DCC[1:0], and the en_h, and en_l signals, we manage the rising/falling time of the first inverter output. Because the transition time can be changed, the duty cycle ratio of the final output signal can be controlled by setting how many pMOS or nMOS transistors are open or closed in Fig. 5.5(a). If we apply a high gate voltage, the nMOS transistors in the nMOS box will cause the rise time to increase at O1 in Fig. 5.5(a). The high/low ratio of the clock signal at “Out” will be decreased. Therefore, if the critical path signal timing approaches a setup violation, en_h needs to be high to make the high to low ratio of a clock duty cycle decrease and vice versa for the case of a hold time violation. For different DCC[1:0] values, the duty cycle

ratio is changed according to the FSM diagram in Fig. 5.5(b). The variable range of the controllable duty cycle is up to $\pm 10\%$.

TABLE. 5.1

OVERALL FLIP FLOPS DEGRADATION (%) AFTER 10 YEARS

	$ T_0 - T_{10yrs} /T_0 \times 100$		
	Setup	Hold	Clock-Q
Average (%)	17.3	8.4	12.1
Variation (%)	4.3	2.2	3.13

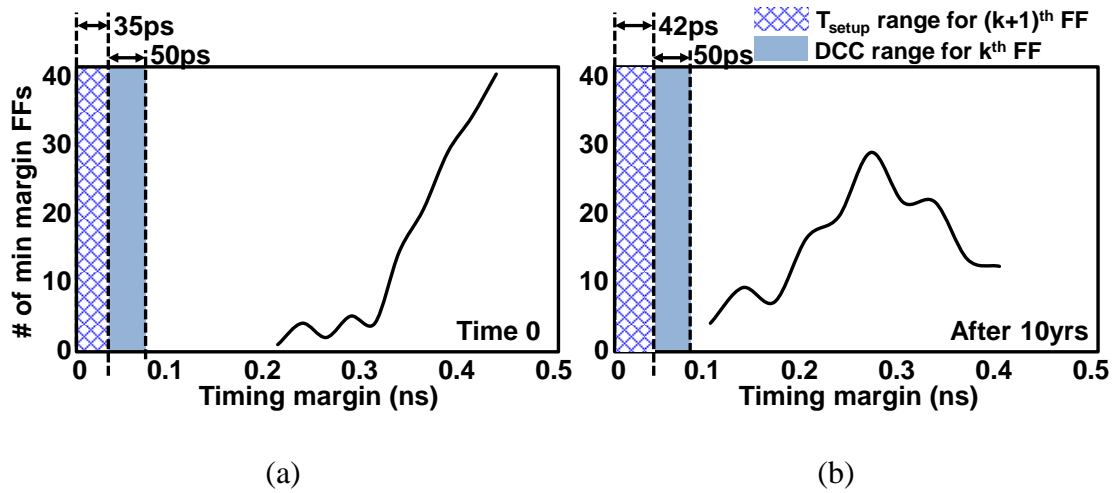


Fig. 5.6. Timing margin distribution for next stage FFs that follow paths connected to DCC-controlled FFs. (a) The distribution at time zero and (b) The distribution after 10 years of operation for case II.

5.1.3 Criteria of DCC module insertion for vulnerable FFs.

When the DCC modules are inserted for the number of vulnerable FFs, we need to review several issues to avoid the possible problems. First, we need to verify that DCC modules can cover the FF degradation effects. Therefore, we extract 150 most degraded FFs based on the activity profiles, and analyze the degradation of the FF specification. Table 5.1 shows the FF degradation about T_{setup} , T_{hold} , and $T_{\text{Clock-Q}}$ ranges after 10years operation under test benches. T_{setup} degrades larger than T_{hold} , because a signal needs to pass through more gates for T_{setup} than T_{hold} in Fig. 8(c). Also, because the maximum degraded setup time is less than 35ps, we our module can monitor and make the timing violation warning signals.

Also, we identified a set of next stage FFs and determined the timing margins for them. Because DCC modules finally change the timing of output signals because of the adjusted clock duty cycle, and the modified timing can cause the timing issues of next FFs. Therefore, when a DCC module changes the clock duty cycle of k^{th} FF, we need to analyze timing margin of $(k+1)^{\text{th}}$ FFs to avoid the possible timing violation issues. Because of the area overhead, we avoid an additional management circuitries for the $(k+1)^{\text{th}}$ FFs timing margin checker and feedback system. However, we used the sophisticated statistical static timing analysis [73] and use the worst cases degradation scenarios of critical paths and FFs degradation to check the timing margin of the $(k+1)^{\text{th}}$ FFs. The results are shown in Fig 5.6 for the case II and III. Fig. 5.6(a) is the timing margin distribution for $(k+1)^{\text{th}}$ FFs of 150 number of FFs, and Fig. 5.6(b) is the distribution for $(k+1)^{\text{th}}$ FFs of 543 number of FFs. As we can see Fig. 5.6(b), after 10 years operation, we have 3 number of insufficient

timing margin $(k+1)^{\text{th}}$ FFs. Hence, DVFS is only required when these FFs run out of margin, and this happens later than the potential timing violations of DCC-monitored FFs. Then, we compare the impact on circuit lifetime at different operating frequencies. Finally, we check the 4 performance factors and evaluate overall performance improvement of the system for different cases. To do this, we use Monte Carlo simulations with initial process variations for multiple voltage-frequency combinations.

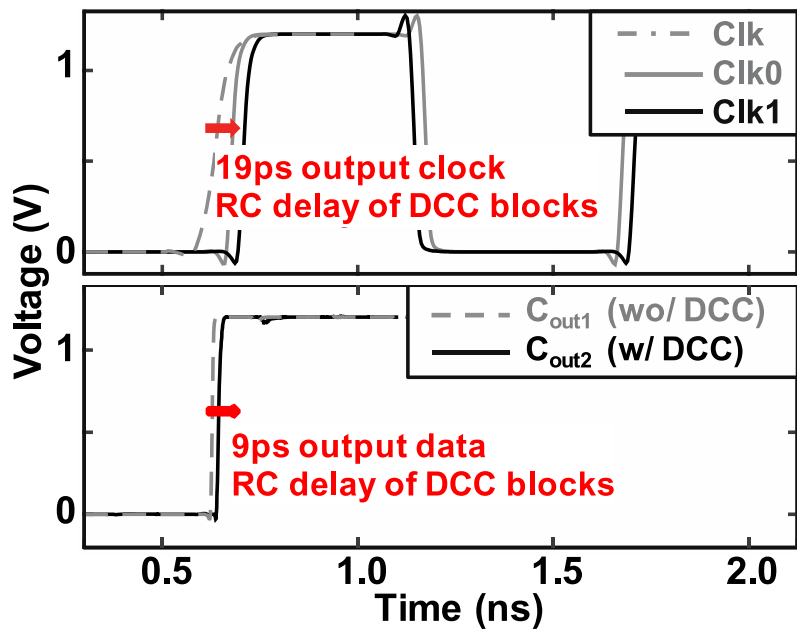
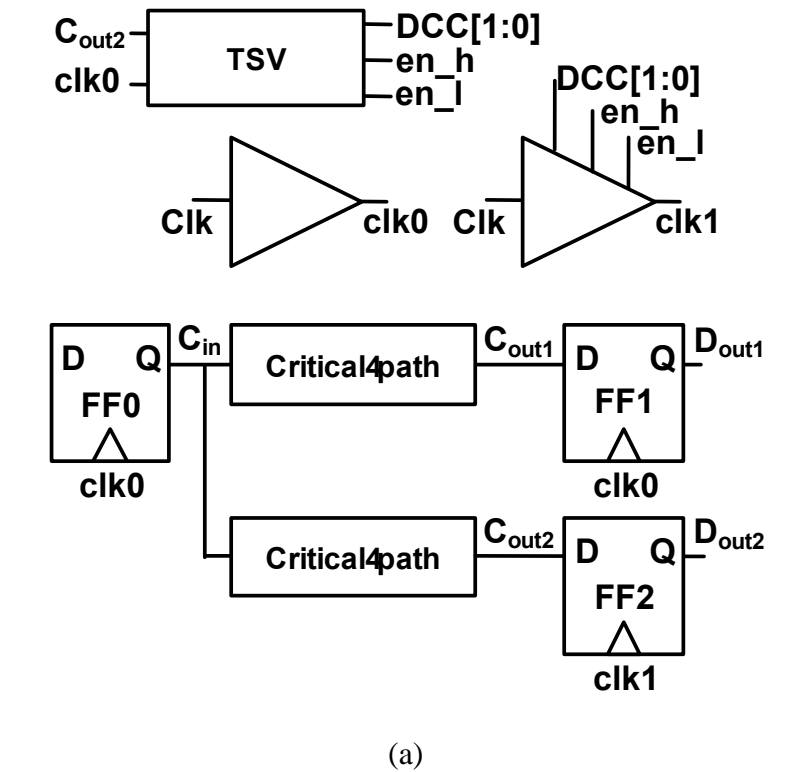


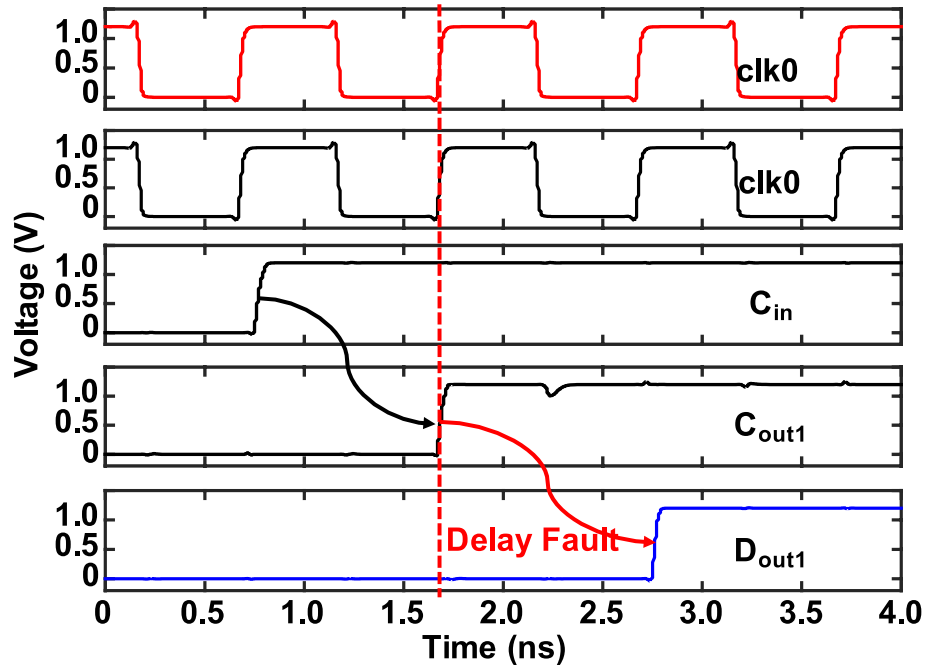
Fig. 5.7. An example to show how a delay fault can be fixed. (a) Two critical paths with different clocks which are controlled by the DCC system. (b) The RC delay of the DCC block a clock signal and a data path.

5.2 Performance Analysis with the DCC system

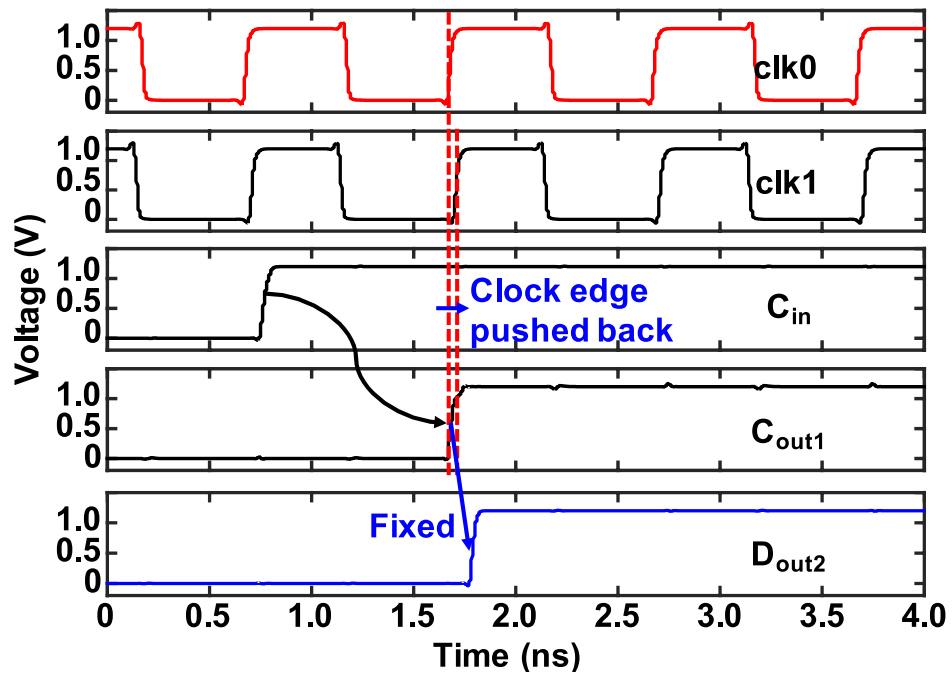
In order to check the ability of our self-adaptive DCC system, we analyze several cases studies. First, we extract an example critical path from the RISC processor and check whether increasing delays can be rectified or not. Second, we have analyzed four performances: yield, lifetime, power overhead, and area overhead for three cases. The cases vary the number of DCCs included in the design: (i) without DCCs, (ii) with 150 DCCs for the extracted critical paths using STA at various stress times, and (iii) with 3370 DCCs for every flip flop in the system. The system is analyzed using Monte Carlo simulations with process parameter variations, aging, and multiple voltage-frequency combinations.

5.2.1 The example fault case and fault correction

To check whether the self-adaptive DCC system can fix timing violations without changing the operating frequency, we extract a critical path which failed at a certain stress time. The sample circuit in Fig. 5.7(a) mimics the delay degradation of the critical path. The example consists of two identical critical paths. Because of the RC delay of the DCC block, as illustrated in Fig. 5.7(b), the data path delay increases by 9ps and the clock path delay increases by 19ps. Therefore, we use one additional buffer for FF0 in Fig. 5.7(a), in order to match and compensate for the additional RC path delay.



(a)



(b)

Fig. 5.8. (a) A faulty example caused by a setup time violation (without the DCC system).

(b) An example fixed by the DCC system

Each critical path output connects to a flip flop, shown in Fig. 5.4. The clock signal of the output flip flop of the original circuit (FF1) has the same clock signal as the input flip flop (FF0). Because of the large delay degradation of the critical path, the setup time margin is inadequate. However, the second critical path uses a modified clock signal which is controlled by the duty cycle controller buffer and a TVS. The modified clock signal is fed into its output flip flop (FF2). As we can see from the result in Fig. 5.8(a), in the first case, because of delay degradation, the path has a timing violation. Therefore, the D_{out1} signal (the red dotted line) does not follow the C_{out1} data with the correct timing. However, because the duty cycle of the $clk1$ signal is controlled by the DCC buffer, the timing of the positive clock edge is pushed back, as shown with the blue line in Fig. 5.8(b). Because of the fixed duty cycle, FF2 has sufficient timing margin to read the C_{out2} data and to get the D_{out2} data.

The movement of the clock edge of FF2 affects the timing of any paths originating from FF2. If these paths have sufficient margin, then the lifetime of the circuit is extended without performance degradation.

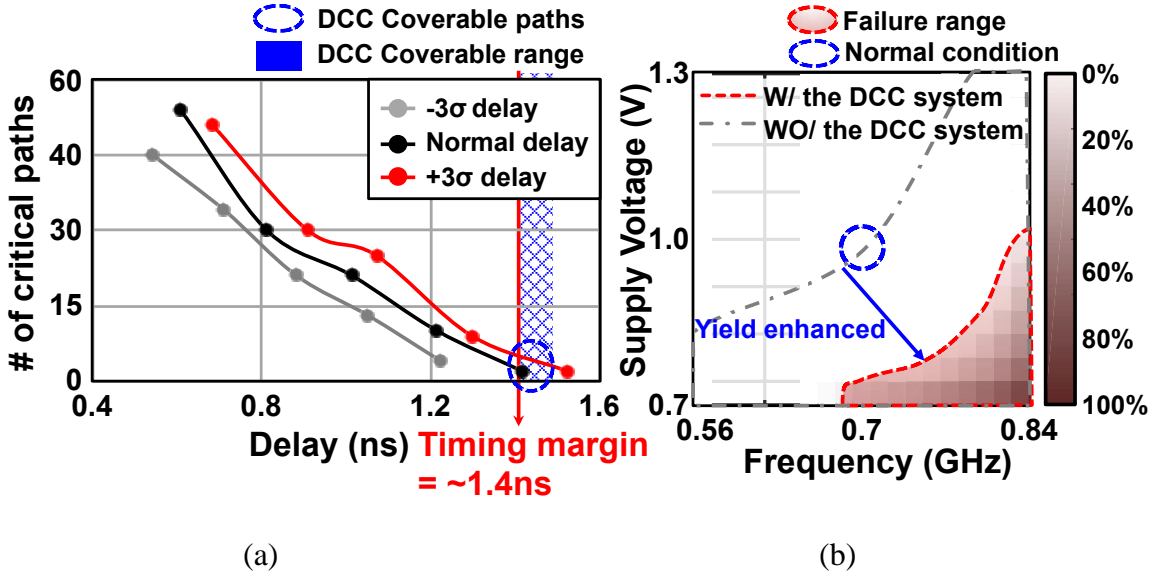


Fig. 5.9. DCC system performance evaluation. (a) The delay distribution of a number of extracted critical paths from the microprocessor, after 10 years of operation with three sigma process variations. (b) Failure probability distribution for different voltage-frequency combinations, computed with Monte Carlo simulations, after 10 years of operation.

5.2.2 Analysis of the lifetime improvement

The DCC system can control the clock duty cycle by up to $\pm 5\%$, which means that if the system operating frequency is 1GHz, it can control the clock edge timing by up to ± 50 ps. In order to check the ability of our self-adaptive DCC system to fix delay degradation, we have considered a RISC processor as an example [83] and analyze four performances: yield, lifetime, power overhead, and area overhead for four different cases.

To check the system capability, first, we applied degradation to the microprocessor and extracted the degraded critical paths. Because the normal operating frequency of the RISC system is 700MHz, the timing margin is 1.4ns. As can be seen in Fig. 5.9(a), after 10 years of operation, several critical paths (on the right side of the red arrow) create timing

violation problems. (The red and black lines are the nominal $\pm 3\sigma$ PV results, respectively.) 150 DCCs can cover the lack of timing margins (the blue area). This means that the DCCs can compensate for 10 years of critical path degradation for the nominal case.

The gray dotted line in Fig. 5.9(b) shows the failure probability distribution at different voltage-frequency conditions. The case without the DCC system is illustrated with the gray dotted line. The probability of failure data is computed with Monte Carlo simulations using process parameter variations and degradation due to aging. Although a few critical paths fail due to timing at nominal conditions (700MHz, 1V), as indicated by the blue dotted line, the probability of failure is high if there are small variations in supply voltage and operating frequency. Because the DCC system can cover many timing violations, the red dotted line in Fig. 8(b) shows that many degraded critical paths can be made to work correctly. The figure shows that all paths can avoid timing violations at nominal. Also, the range of operating conditions where the system fails is reduced because of the DCC system.

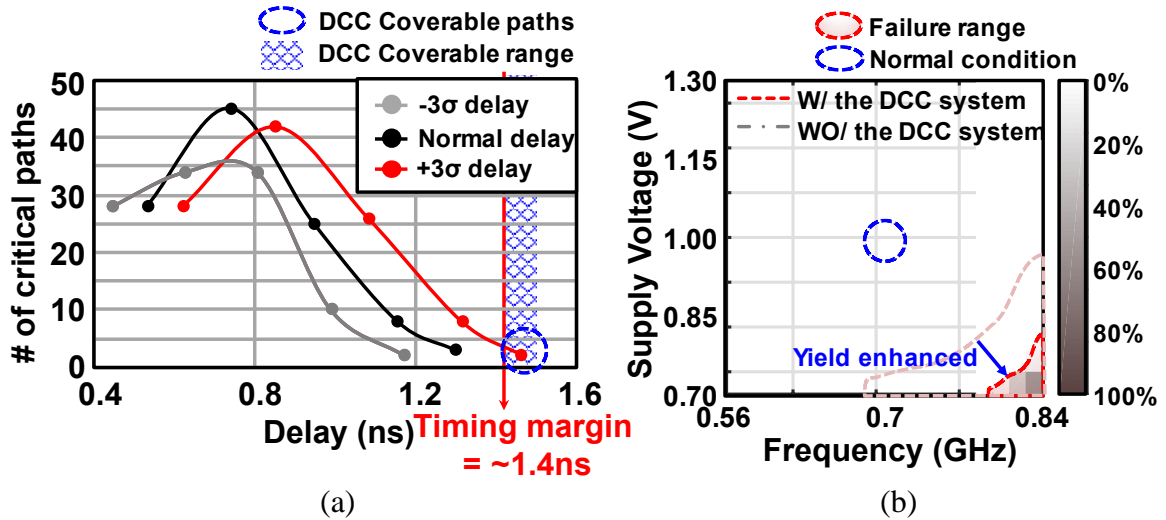


Fig. 5.10 (a) The delay distribution of the extracted critical paths at time zero. (b) Failure probability distribution for different voltage-frequency combinations, computed with Monte Carlo simulations at time zero.

Next, the DCC system not only extends circuit lifetime, but it also enhances the yield of the circuit as well. As can be seen in Fig. 5.10(a), when we use Monte Carlo simulations to determine the number of critical paths at time zero, accounting for initial process parameter variations for the extracted critical paths, the paths have a large range of delay variation. Even though the circuit is not degraded, there can be paths with timing margin problems because of extreme values of process parameters, which cause the delay to increase beyond the red line. However, because the timing violations are within the covered range (blue area) of the DCC system, these circuits can be repaired. Fig. 5.10(b) shows the yield enhancement effect. The operating conditions where failures occur is reduced. Therefore, it can be seen that circuit yield is enhanced via the self-adaptive DCC system.

Although the proposed system extends the lifetime and enhances the yield of the circuits, the overall system will be damaged by a power and area overhead factor because of the DCC blocks. Each DCC module with delay sensor consumes 185pW and occupies an area of around 163 μm^2 .

TABLE 5.2.

COMPARISON OF OVERHEAD FOR VARYING NUMBERS OF DCCs

Case	Failure Prob. At Time 0	Failure Prob. After 10 Years Operation	% Area Overhead	% Power Overhead
WO/ DCC	$3.77 \cdot 10^{-2}$	$2.90 \cdot 10^{-1}$	0	0
150 DCCs	$1.17 \cdot 10^{-2}$	$7.84 \cdot 10^{-2}$	$7.82 \cdot 10^{-3}$	$2.72 \cdot 10^{-3}$
3,370 DCCs	$8.30 \cdot 10^{-3}$	$1.44 \cdot 10^{-2}$	$1.76 \cdot 10^{-1}$	$6.12 \cdot 10^{-2}$

TABLE 5.3.

COMPARISON OF THE PROPOSED SYSTEM AND PREVIOUS WORKS ABOUT PERFORMANCE ENHANCEMENT

Factors	[82]	[41]	[83]	This paper
Area overhead	2%	2.5%	5.6%	0.8%
Power Overhead	3%	3% @ 0.1% err rate	3%	0.3%
Coverage @ t = 0	Not mentioned	Not mentioned	97.5%	98.8%
Coverage @ t = 10yr	Not mentioned	Not mentioned	Not mentioned	92.2%

Table 5.2 compares the impact on overhead of different numbers of DCCs. It can be seen that most critical paths can be corrected with only 150 DCCs in our example microprocessor. Table 5.3 compares the proposed DCC system which includes 150 DCC modules and other previous state-of-of-the art works aimed at increasing the lifetime of circuits [41],[43],[82]. After synthesizing the RISC system with 150 DCC modules, the system has less power overhead. While considering different voltage-frequency combinations with Monte Carlo simulations, including aging, the fault coverage result for the RISC microprocessor with the DCC system is greater than 98.8% at time zero and 92.2% after 10 years of operation.

CHAPTER 6

CONCLUSION

To complete the research objectives, first, I presented a method to extract NBTI and GOBD parameters from chips without the availability of embedded test structures for NBTI and GOBD. Since these two wearout mechanisms affect both the power supply and ground signals, I have proposed a method to estimate the impact of each separately. I have used simulation to develop an equation to determine the relationship between the ground signature and an average threshold voltage shift, from which the NBTI failure rate parameters are computed. I have also used simulation to find a relationship between the defect generation rate parameters and the power supply and ground signatures in order to estimate parameters related to the defect generation rate for GOBD. The method involves measuring shifts in amplitude and delay of the ground and power supply signals during operation. The ability to measure shifts in the ground signal has been demonstrated experimentally.

This approach enables the estimation of NBTI and GOBD degradation on a chip-by-chip basis. It determines an average threshold voltage shift and GOBD defect generation rate, from which wearout distribution parameters are estimated, using a known test bench. I have also shown that lifetime is strongly dependent on process parameters, and have extracted key process parameters. Lifetime simulation with arbitrary workloads can then be used to estimate the remaining lifetime of a chip. Extraction of process parameters tightens the confidence bounds on lifetime.

Also, based on the calibrated device-level models, I developed a self-adaptive DCC system for lifetime and yield enhancement. The system compensates for variation in critical path delays caused by aging and can be extended to handle other resistive defects. The

system controls the clock duty cycle to increase timing margins in order to avoid timing violations without performance degradation. The method is validated with calibrated statistical Monte Carlo simulations, where the digital system is degraded based on device models. The DCC system has a small overhead in terms of power and area, while extending system lifetimes substantially.

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