

GNEP Readiness at Georgia Tech Final Report

**PD/PI: Dr. Farzad Rahnema
Professor and Chair of the NRE/MP Programs**

**Co-PD/PI(s): Dr. Nolan E. Hertel, Professor &
Mr. Dwayne P. Blaylock, Interim Manager of NRE/MP Laboratories**

Summary

To prepare the Georgia Tech Nuclear and Radiological Engineering (NRE) program for research efforts needed in the Global Nuclear Energy Partnership the program used the funding to enhance both its computational and experimental capabilities. Approximately half the funding (\$50,175) was used to purchase a department based high performance computing cluster. The remaining funds were used in the purchase of a flash Analog-to-Digital (ADC) digitizer.

Georgia Tech Global Nuclear Energy Partnership Computational Cluster (GTGCC)

The GTGCC is a moderate size high performance computing cluster that was delivered and installed at Georgia Tech in the fall of 2008. This cluster is a shared resource that is available to all NRE faculty members, students and collaborators with the NRE faculty on GNEP related research projects. It is envisioned that the GTGCC will be used in numerous research areas over the coming years including: design and analysis of integral and fast reactors, analysis of advanced fuel cycles, nuclear materials modeling, development of new computer codes, and others. To meet these diverse computational requirements the GTGCC is configured with 21 nodes connected by a high speed network. Each node has two quad core processors along with 32 Mb of memory. Final configuration of the software suite is ongoing and at a minimum the following nuclear engineering codes will be installed used for modeling of various research projects.

- MCNP/MCNPX
- SCALE
- NJOY
- REBUS
- MC²
- ERANOS

In addition a complete suite of compilers, (FORTRAN, C, C++, etc) has been installed that allows the GTGCC to be used as a developmental platform for new computer codes

Experimental Equipment Upgrades

To enhance its experimental capabilities a dual channel flash ADC digitizer from Aquis was purchased for use with an existing fast organic scintillator. The digitizer has dual Xilinx Virtex 5 field programmable gate array (FPGA) for processing the data. The benefit of this system beyond current technology is that the FPGA boards can be programmed for application specific tasks. The digitizer board can be programmed to correct for pulse pileup and apply a pulse pileup correction. Operating at 2.5 GHz the digitizer allows pulse shape discrimination to be performed on the rising edge of the pulse, thus allowing a high speed, low latency detector system. The digitizer board can also produce a pulse height spectrum, and transmit the corresponding data to a single computer that is used to collect the data.