

**RECONFIGURABLE CMOS RF POWER AMPLIFIERS
FOR ADVANCED MOBILE TERMINALS**

A Dissertation
Presented to
The Academic Faculty

By

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In Partial Fulfillment
Of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology

August 2011

RECONFIGURABLE CMOS RF POWER AMPLIFIERS FOR ADVANCED MOBILE TERMINALS

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[To my wife and parents]

ACKNOWLEDGEMENTS

First of all, I would like to appreciate the monumental support that both my advisor Prof. James Stevenson Kenny and former advisor Dr. Joy Laskar gave me to work in this research. Without their inspiration and teaching, I certainly would not have achieved this goal.

I also would like to thank Prof. Kevin T. Kornegay, Prof. Waymond Scott, and Prof. Paul A. Kohl, for serving as my defense committee members.

I am very grateful to Dr. Chang-Ho Lee for his great support and guidance throughout this study. I am also indebted to Dr. Kyutae Lim for his valuable support.

The support from former and present PA Group members has been invaluable: Dong Ho Lee, Kyu Hwan An, Ockgoo Lee, Hyungwook Kim, Jeongwon Cha, Eungjung Kim, Jihwan Kim, Hamhee Jeon, Michael Oakely, Hyunwoong Kim, Yan-Yu Huang, Kun Seok Lee, Kwanyeob Chae. I would like to express my special gratitude to Hyungwook Kim and Jihwan Kim for their comments, help in the design, and their tremendous encouragement. I would acknowledge all my colleagues at the Microwave Application Group, Sanghyun Woo, Joonhoi Hur, Sang Min Lee, Jong Min Park, Kwan-Woo Kim, Taejoong Song, Jaehyouk Choi, Seungil Yoon, Michael Lee, Sungho Beck, Taejin Kim, Hyungsoo Kim, and Kilhoon Lee. I wish to thank Angelika Braig for her continuous support.

I also would like to acknowledge Samsung Design Center engineers, Dr. Jae Joon Chang, Dr. Woonyun Kim, Dr. Wangmyong Woo, Dr. Changhyuck Cho, Dr. Yunseo

Park, Dr. Minsik Ahn, Dr. Ki Seok Yang, Dr. Jeonghu Han, and Mr. Jungjoo Lim for their valuable supports.

Most importantly, none of this would have been possible without the love and patience of my family. My very special thanks to the one person whom I love, My wife, Jung Eun, whose love and support have sustained me and continue to make my life full of happiness. My future daughter has also been a great source of joy. I am especially grateful to my parents, Jae-Ho Yoon and Joo-Myung Lee and my parents-in-law, Seung-Ho Lee and Ok-Hee Park for their love and support. Without their love and support, this dissertation would not have been possible. I would also like to recognize my sister, Young-Mi Yoon, brothers-in-law, Jung-Hoon Ju and Won-Seok Lee, for their love and support.

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LIST OF ABBREVIATIONS

2G	second generation
3G	third generation
4G	fourth generation
ADS	advanced design system
AM-AM	amplitude-amplitude modulation
ATU	antenna-tuning unit
CG	common gate
CMOS	complementary metal-oxide-silicon
CPU	central process unit
CS	common source
DNW	deep N-well
DUT	device under test
EDGE	enhanced data rates for GSM evolution
EER	envelope elimination and restoration
ET	envelope tracking
EVM	error-vector-magnitude
GaAs	gallium arsenide
GPRS	general packet radio service
GSM	global system for mobile communications
HB	harmonic balance

HP	high power
IC	integrated circuit
IEEE	institute of electrical and electronics engineers
IIP3	third order input intercept point
IMD3	two-tone third-order inter-modulation distortion
IS-95	interim standard 95
LP	low power
LSSP	large-signal S-parameter
LTE Advanced	long-term-evolution advance
MEMS	micro-electro-mechanical systems
MIM	metal-insulator-metal
OFDM	orthogonal frequency-division multiplexing
P_{1dB}	1-dB gain variation point
P_{1dB}	1-dB gain compression point
PA	power amplifier
PAE	power-added-efficiency
PCB	printed circuit board
$P_{lin.max}$	maximum linear output power
P_{sat}	saturation output power
Q	quality factor
QAM	quadrature amplitude modulation
RF	radio frequency

SiGe	silicon germanium
SOI	silicon-on-insulator
SOS	silicon-on-sapphire
SPI	serial peripheral interface
TFF	toggle flip-flop
VNA	vector network analyzer
VSWR	voltage standing-wave ratio
WCDMA	wideband code division multiple access
WLAN	wireless local area network

SUMMARY

In recent years, tremendous growth of the wireless market can be defined through the following words: smartphone and high-data rate wireless communication. This situation gives new challenges to RF power amplifier design, which includes high-efficiency, multi-band operation, and robustness to antenna mismatch conditions. In addition to these issues, the industry and consumers demand a low-cost small-sized wireless device. A fully integrated single-chip CMOS transceiver is the best solution in terms of cost and level of integration with other functional blocks. Therefore, the effective approaches in a CMOS process for the abovementioned hurdles are highly desirable.

In this dissertation, the new challenges are overcome by introducing adaptability to a CMOS power amplifier. Meaningful achievements are summarized as follows. First, a new CMOS switched capacitor structure for high power applications is proposed. Second, a dual-mode CMOS PA with an integrated tunable matching network is proposed to extend battery lifetime. Third, a switchless dual-band matching structure is proposed, and the effectiveness of dual-band matching is demonstrated with a fully-integrated CMOS PA. Lastly, a reconfigurable CMOS PA with an automatic antenna mismatch recovery system is presented, which can maintain its original designed performance even under various antenna mismatch conditions. Conclusively, the research in this dissertation provides various solutions for new challenges of advanced mobile terminals.

CHAPTER 1

INTRODUCTION

1.1. Background

Since the first mobile phone appeared in 1960s, the use of a mobile phone has been explosively increasing over the last few decades. Figure 1 shows how fast the number of mobile phone subscriptions has increased during the last decade. This popularization of mobile phones has affected and changed daily life for hundreds of millions of people all around the world. At the same time, wireless communication technology has also remarkably evolved to satisfy various consumers' demands, which is usually defined by "generation."

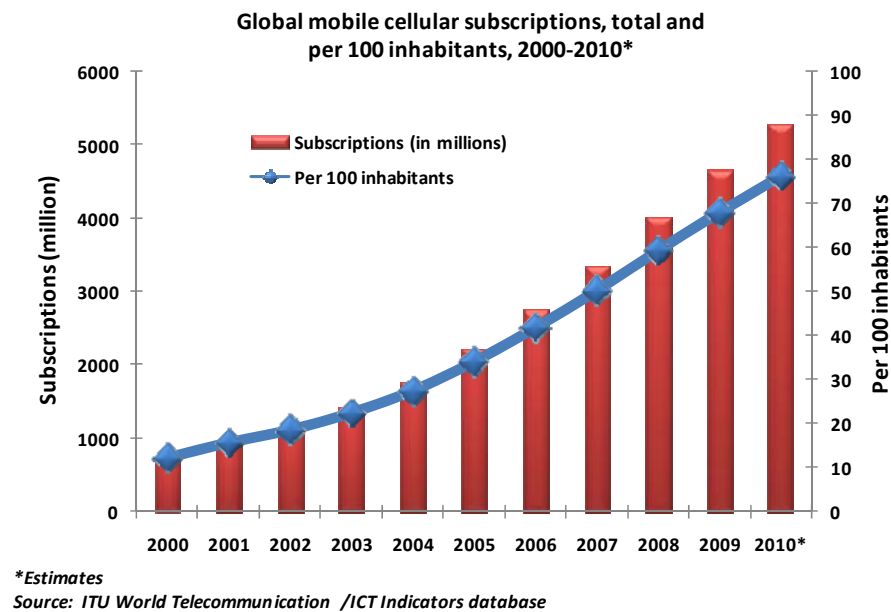


Figure 1. Global mobile cellular subscriptions.

Figure 2 shows how much proportion is occupied by each generation among the total worldwide mobile subscribers. As described in Figure 2, a new generation continuously overtakes the previous generation. We can understand the reason why a new generation is constantly introduced by summarizing the distinctions between generations. In the early 1990s, the second generation (2G) was introduced. The main standards of 2G are global system for mobile communications (GSM) and interim standard 95 (IS-95). 2G phones use digital networks that make it possible to improve voice quality as well as send text messages and voicemail. Meanwhile, the data rate is quite limited, so an intermediary phase, 2.5G was introduced in the late 1990s, which includes general packet radio service (GPRS) and enhanced data rates for GSM evolution (EDGE). It delivers packet-switched data capabilities to existing GSM networks, and it allows users to send graphics-rich data as packets.

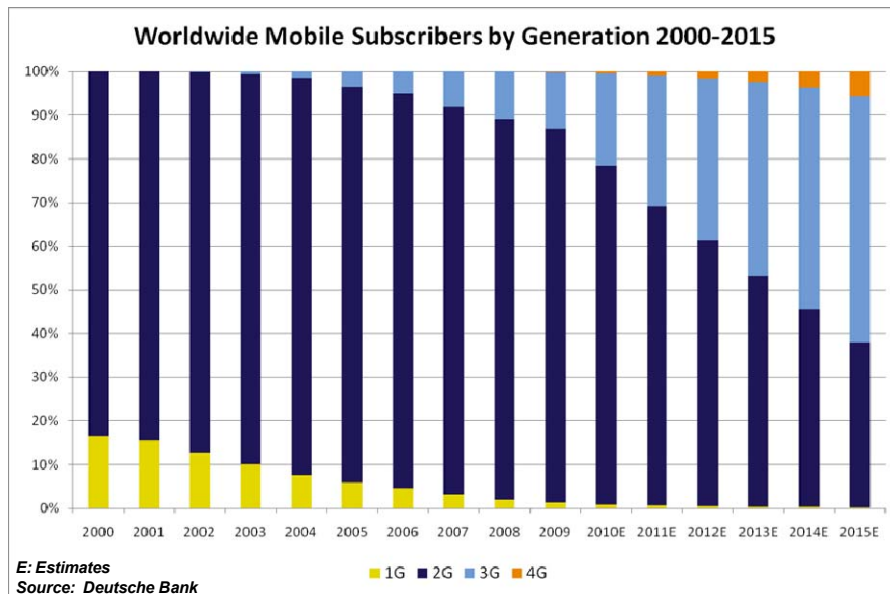


Figure 2. Worldwide mobile subscribers by generation.

The advantage of the third generation (3G) over 2G is speed. The main standard of 3G is wideband code division multiple access (WCDMA). With 3G, it is possible to watch streaming video and engage in video telephony. One of the other main objectives behind 3G is to standardize a single global network protocol instead of the different standards adopted previously in Europe, the U.S. and other regions. The fourth generation of cellular wireless standards (4G) is a successor to the 3G and 2G families, of which the key feature is a high data rates. For example, long-term-evolution advanced (LTE Advanced) requires a peak download data rate of 1 Gbit/s and a peak upload rate of 500 Mbit/s. Its substantial improvements of the data rate can enable multimedia messaging services, including video services.

Keeping pace with this trend, the recent biggest alteration in the mobile phone market is the advent of advanced mobile terminals, i.e. smartphones. After the introduction of Apple Inc.'s iPhone, the smartphone is getting more attention by both consumers and manufacturers because it becomes an essential device for laymen. According to the technology research firm iSuppli, a smartphone unit shipment growth of 35.5% was expected in 2010, while overall mobile handsets were expected to grow 11.3%. This gap implies that a large portion of traditional mobile handsets is being replaced by the smartphone. Figure 3 presents the worldwide smartphone shipment forecast reported by iSuppli Corp.. As described in Figure 3, the number of smartphone users is expected to increase explosively in the near future.

What makes smartphones so attractive to users? The biggest distinct features of smartphones compared to previous mobile handsets are their multi-tasking abilities. A smartphone can be described as a notebook on the palm. With a smartphone, users can

watch a video, listen to MP3 files, surf the internet, download a movie, send/receive an E-mail, take a picture, etc. For supporting these new features, the smartphone requires more advanced components inside such as a high performance mobile central process unit (CPU), a high resolution screen, and a large capacity memory system. This sophisticated requirement is also applied to the radio frequency (RF) circuitry. In this research, the requirements of the RF circuitry, especially the power amplifier (PA), are investigated.

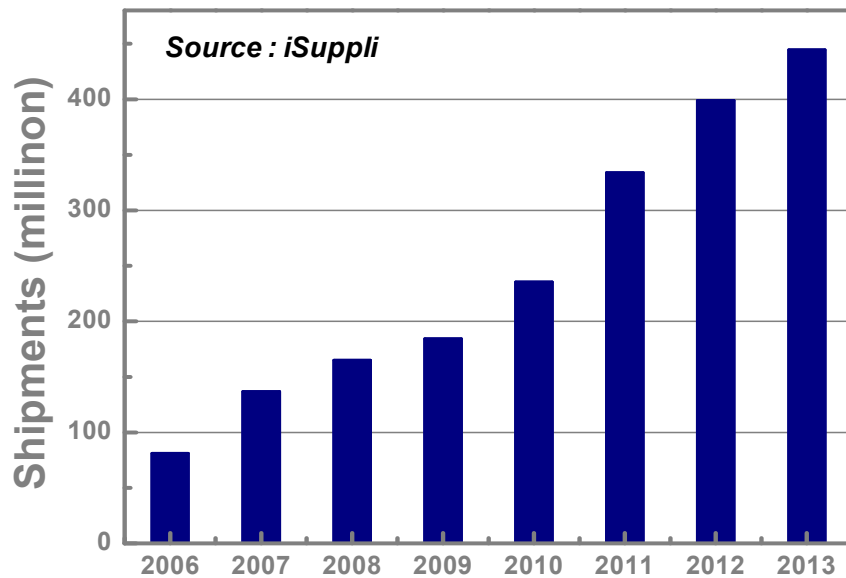


Figure 3. Worldwide smartphone shipment forecast.

1.2. Motivation

1.2.1. Challenges in Advanced Mobile Terminals

Both of the aforementioned trends such as high data rate, usage increase of smartphones introduce new challenges to RF integrated circuit (IC) designers. Among the

RFIC components, a PA is investigated in this thesis. The following characteristics introduce requirements of a PA for the advanced mobile terminals: battery lifetime, multi-band operation, and robustness to antenna mismatch conditions.

1.2.1.1. Battery lifetime

Since the introduction of a mobile phone, battery lifetime has always been a major concern for terminal users. Many researchers have strived for extending the battery lifetime, and efficiency of a PA is mainly at the center of attention. Since the PA is the most power-hungry component in a handset device, the efficiency of the PA has a great effect on the battery lifetime. As the smartphone era has come, the battery lifetime is getting more challenging, which originates from two main aspects.

One of them is the multi-tasking capability of the smartphone. Smartphone users utilize the device for various applications besides making a phone call. They frequently use the smartphone as a camera, a video player, a web surfing device, an MP3 player, etc. Since the device is to be used for various purposes with a limited battery capacity, it requires very high efficient circuitry to extend the battery lifetime. The other part is related with an advanced wireless standard for high data-rate wireless communications. Most of the recently developed smartphones have two different operation modes: 2G (GSM) and 3G (WCDMA). Theoretically, the 2G standard employs a constant envelope signal that makes it possible to take advantage of a very efficient switching PA, while a linear PA with a relatively low efficiency must be utilized in the 3G standard because of a non-constant envelope signal. Figure 4 shows talk time differences of the latest smartphones according to the operation modes. As shown in Figure 4, all of the recent

smartphones have much less talk time in the case of 3G operation. Although the 3G standard enables greatly improved high-data-rate wireless communication, it is accompanied by high power consumption. Consequently, both the multi-tasking capability and the advanced wireless standard have a negative impact on the battery lifetime, and increase strong demands for a highly efficient linear PA.

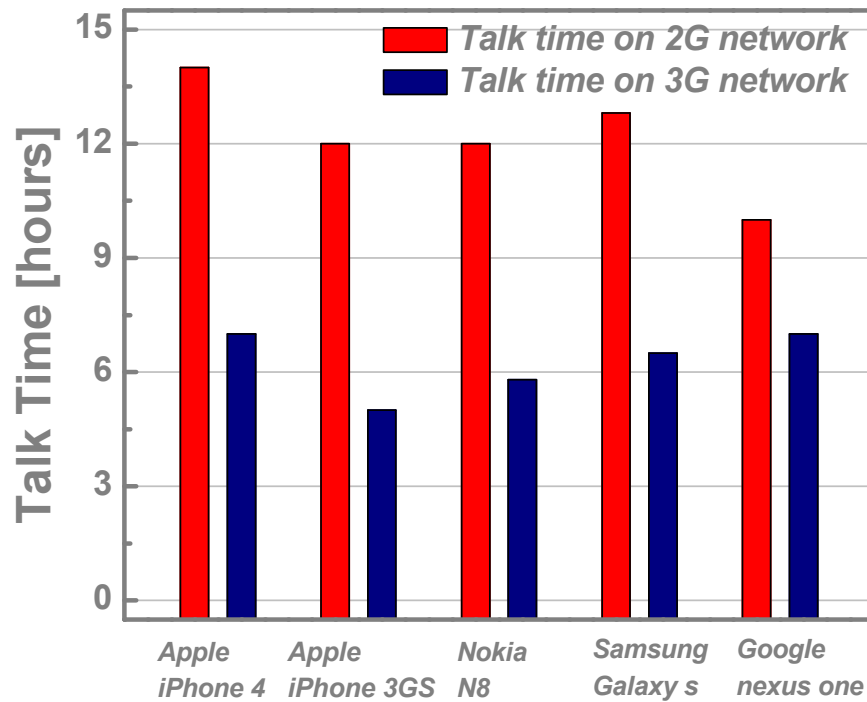


Figure 4. Talk time of the latest smartphones according to the operation mode.

1.2.1.2. Multi-Band Requirements

As the mobile phone has developed, an additional noticeable feature is a multi-band requirement. Table 1 shows present and near future frequency bands for the mobile phone. As described in Table 1, the number of frequency bands is increasing as the wireless

standards evolve. Since a conventional PA can efficiently cover only one frequency band, a large number of PAs are necessary in a beyond-3G mobile phone as shown in Figure 5. Consequently, more board area and cost are required to implement the PA for a multiband handset. However, if one signal path in Figure 5 can support more than one frequency, the total cost and area of the PA can be decreased thanks to the reduced number of parallel PAs. Therefore, there have been increasing interests in a multi-band PA, of which input and output matching networks can be reconfigured according to the frequency bands.

Table 1. Frequency bands in a mobile phone.

	Application	Standard	Frequency (MHz)
3G	Cellular	Quad-Band GSM/EDGE	850, 900, 1800, 1900
		Quad-Band UMTS/HSDPA/HSUPA	850, 900, 1900, 2100
	WLAN	IEEE 802.11n	2400-2484
	PAN	Bluetooth	2402-2480
Beyond 3G	Cellular	Mobile WiMAX	2300-2700
			3300-3700
			4900-5900
		Long Term Evolution	700, 800, 900, 1700, 1800, 1900-2100, 2600
	WLAN	IEEE 802.11n	5150-5350

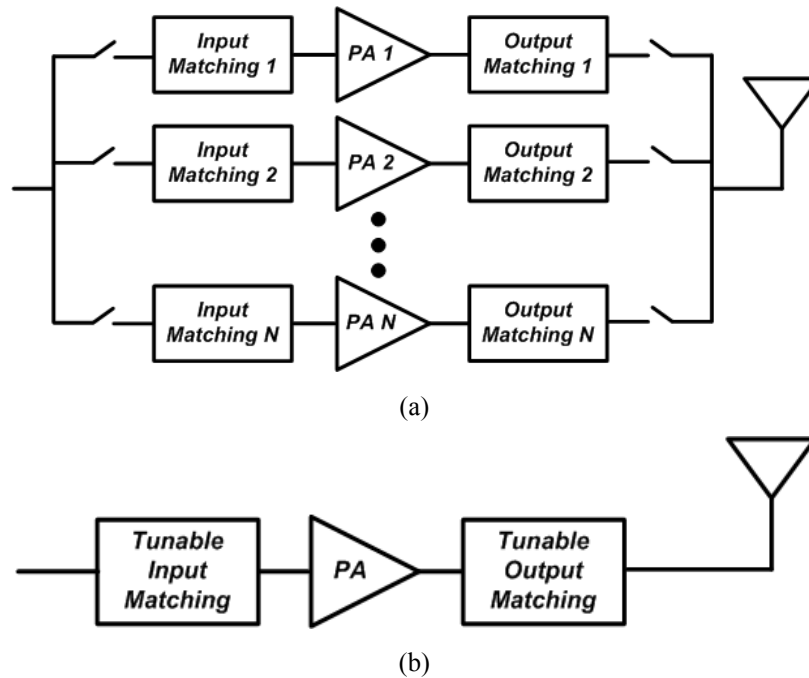
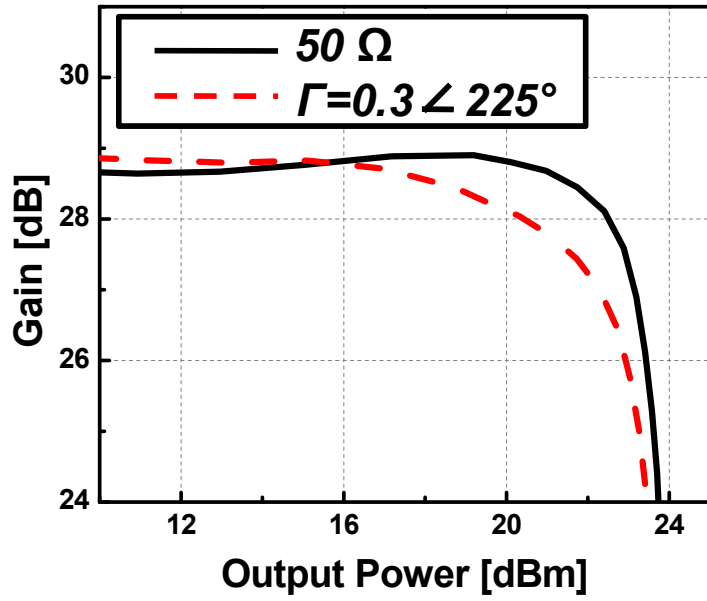


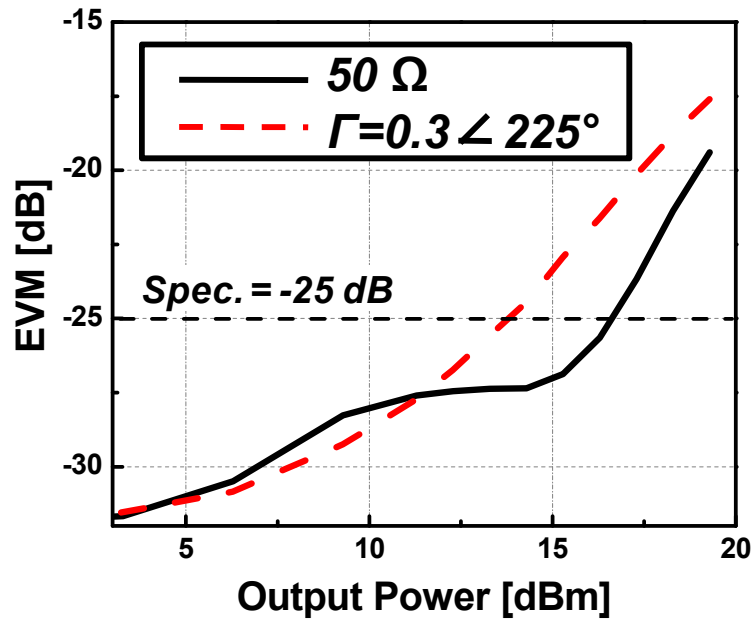
Figure 5. Multiband PA. (a) A conventional structure and (b) reconfigurable multiband PA.

1.2.1.3. Antenna Mismatch Effect

Typically, the RF PA is designed and measured under the condition of 50- Ω antenna impedance. However, the antenna impedance is easily varied by environmental changes due to a human body and/or side walls. Thus, the output matching impedance of the PA can be altered significantly in real circumstances. Moreover, the varied load impedance critically affects the performance of the PA in terms of output power, gain, linearity, efficiency, and reliability. The antenna mismatch effect is getting more attention as an advanced mobile phone appears. This is because the advanced wireless standard requires a very highly linear PA that is significantly affected by the antenna mismatch.



(a)



(b)

Figure 6. Measured results under a mismatch condition: (a) power gain and (b) EVM.

Figure 6 shows a measured example of a linear PA under a mismatch condition. The black lines present the normal 50- Ω condition, and dashed red lines present a mismatched condition ($\Gamma=0.3<225^\circ$). Figure 6(a) presents the single-tone measurement results, and Figure 6(b) shows the error-vector-magnitude (EVM) measurement results with the Institute of Electrical and Electronics Engineers (IEEE) 802.11g 64-quadrature amplitude modulation (QAM) orthogonal frequency-division multiplexing (OFDM) signal with the specification of -25 dB. From Figure 6(a), the maximum output power is very close to each other regardless of a mismatch condition. However, the maximum linear output power that is the largest output power before violating the EVM specification is greatly degraded at a mismatched condition. This measurement result indicates that a linear PA experiences severe performance degradation from antenna mismatch effects.

In addition, the recent mobile phone are typically held in the user's hands while being used for multimedia applications, so the advanced mobile terminal experiences mismatched antenna impedance more often. Therefore, much research has been conducted to resolve the antenna mismatch problems.

1.2.2. Research on CMOS PA

In addition to aforementioned issues such as battery life time, multi-band operation, and antenna mismatch effect, the industry and consumers demand a low-cost small-sized wireless device. A fully integrated single-chip complementary metal-oxide-silicon (CMOS) transceiver is the best solution in terms of the cost and level of integration with other functional blocks. A major bottleneck for obtaining a true single chip CMOS radio is the integration of the PA. Because standard CMOS technology possesses intrinsic

drawbacks such as low quality factor (Q) due to the lossy substrate [1], low breakdown voltage of transistors [2], and parasitic components [3], non-CMOS technologies such as Gallium Arsenide (GaAs) and Silicon Germanium (SiGe) prevail in the PA designs thanks to their superior large signal performance. Despite the inferior fundamental characteristics of CMOS technology, much research is being conducted to complete a fully integrated CMOS single chip radio. Since all of the digital, analog, and small signal RF components have been integrated in CMOS technology, the integration of the PA into a standard CMOS process is very attractive in terms of both cost and form factor. Figure 7 shows the number of papers that contain both “CMOS” and “power amplifier” in their titles from the IEEExplore website. As presented in Figure 7, an increasing number of CMOS PA papers are being published to overcome the obstacles toward a single chip radio.

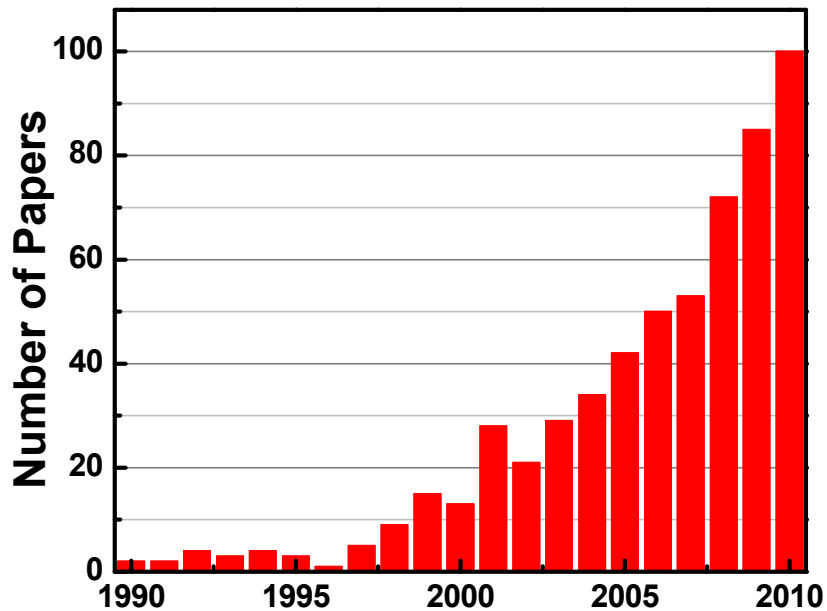


Figure 7. The number of papers that contain both “CMOS” and “power amplifier” in their titles.

1.3. Organization of the Thesis

Based on the background and motivation, the objective of this research is to exploit standard CMOS technologies for developing RF PAs that can overcome newly emerging challenges for advanced mobile terminals.

Chapter 2 presents a high-power and highly linear switched capacitor which can sustain a large voltage swing across it. The presented CMOS switched capacitor is a suitable component for a tunable matching network for PA applications. Chapter 3 presents a dual-mode CMOS PA with enhanced low-power efficiency to improve the battery lifetime. Chapter 4 presents a dual-band CMOS PA with a switchless matching network. An LC resonant structure is utilized for a concurrent dual-band matching network. Chapter 5 presents a CMOS PA immune to antenna mismatches. In this design, an output matching network is manually modified to recover degraded output power, efficiency, and linearity under mismatch conditions. An automatic antenna mismatch recovery system is presented in Chapter 6. A new method to detect and recover a mismatch condition is proposed and verified with measurement results. Finally, Chapter 7 summarizes and concludes the work in this dissertation.

CHAPTER 2

A HIGH-POWER AND HIGHLY LINEAR CMOS SWITCHED CAPACITOR

2.1. Introduction

As more efficient communication systems have been developed, a number of communication standards that have different operating frequencies and modulation schemes have been adopted. Because different frequency bands and modulation schemes require distinct RF circuit and system designs, various standards require the parallel composition of several independent signal paths that consequently increase the size and cost of the system. Therefore, the design of adaptive RF circuits has been thoroughly investigated to decrease the cost and size.

Meanwhile, the implementation of tunable transmitter blocks, especially of a PA, is challenging due to the large signal operation. To accept large voltage swings as shown in Figure 8, a switched capacitor for a PA application should possess two important characteristics: power capability and linearity. The power capability indicates how large of a signal can be sustained while characteristics of the switched capacitor does not change. Otherwise, a matching condition varies with the power level. In addition, if the tunable capacitor has poor linearity, the signal will deteriorate, which will result in a more distorted spectral mask.

Most of the previous tunable capacitors for a reconfigurable PA employ special processes such as micro-electro-mechanical systems (MEMS) [4], switched capacitors with PIN diodes [5], and diode-based varactors on silicon-on-glass technology [6]. Although these special technologies satisfy the requirements of power capability and linearity, they are not compatible with standard CMOS processes. Accordingly, a switched capacitor in a standard CMOS process can significantly contribute to the production of a cost-effective and compact multi-function CMOS PA. Even though there is a conventional CMOS switched capacitor [7], [8], the proposed structure shows highly improved power capability and linearity.

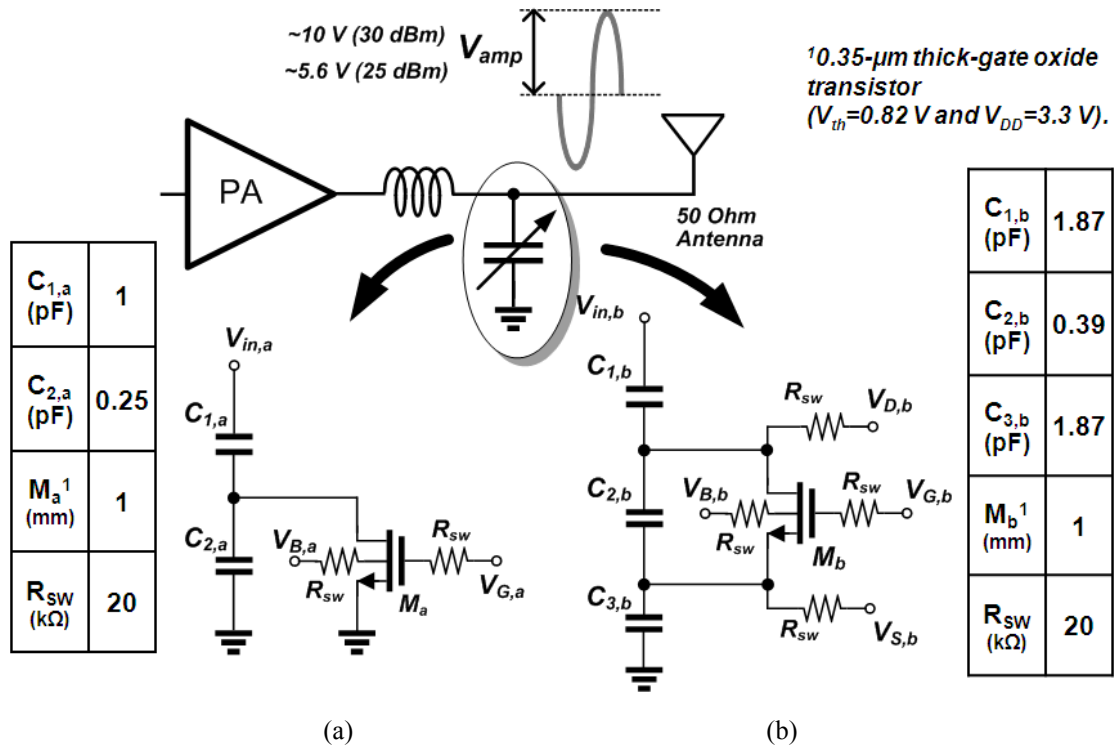


Figure 8. An example of a reconfigurable power amplifier with switched capacitors: (a) a conventional structure and (b) a proposed structure.

2.2. The Proposed Switched Capacitor

A conventional and the proposed structure for a CMOS switched capacitor are presented with designed components values for this design in Figure 8(a) and 8(b), respectively. Both structures use metal-insulator-metal (MIM) capacitors and a deep N-well (DNW) NMOS transistor. The high-value resistors, R_{sw} , are used to obtain the AC open while supplying DC bias. The bias conditions and capacitance values of two structures are described in Table 2. To obtain the equivalent capacitance values with the same quality factor when the switch is on, both $C_{1,a} = \frac{C_{1,b} \cdot C_{3,b}}{C_{1,b} + C_{3,b}}$ and $R_{on,M_a} = R_{on,M_b}$ are to be satisfied. Afterwards, the values for $C_{2,a}$ and $C_{2,b}$ are decided to obtain the same off-state value. Small signal characteristics with respect to frequency are presented in Figure 9. Both structures show similar small signal performance, and have the capacitance of 1 pF in the on-state, and 0.5 pF in the off-state. The relative low Q of the proposed structure in the off-state can be increased by using a larger value of R_{sw} such as 80 k Ω , which is illustrated with a triangular symbol in Figure 9.

Table 2. Bias conditions and capacitance value according to on/off states.

Mode	Conventional Structure			Proposed Structure			
	Bias		Capacitance	Bias			Capacitance
	$V_{G,a}$	$V_{B,a}$		$V_{G,b}$	$V_{D,b}, V_{S,b}$	$V_{B,b}$	
ON	V_{DD}	GND	$C_{1,a}$	V_{DD}	GND	GND	$C_{1,b} // C_{3,b}$
OFF	GND	GND	$C_{1,a} // (C_{2,a} + C_{off,a})$	GND	V_{DD}	GND	$C_{1,b} // C_{3,b} // (C_{2,b} + C_{off,b})$

**denotes series connection of capacitors.
 C_{off} is the parasitic capacitance of a transistor*

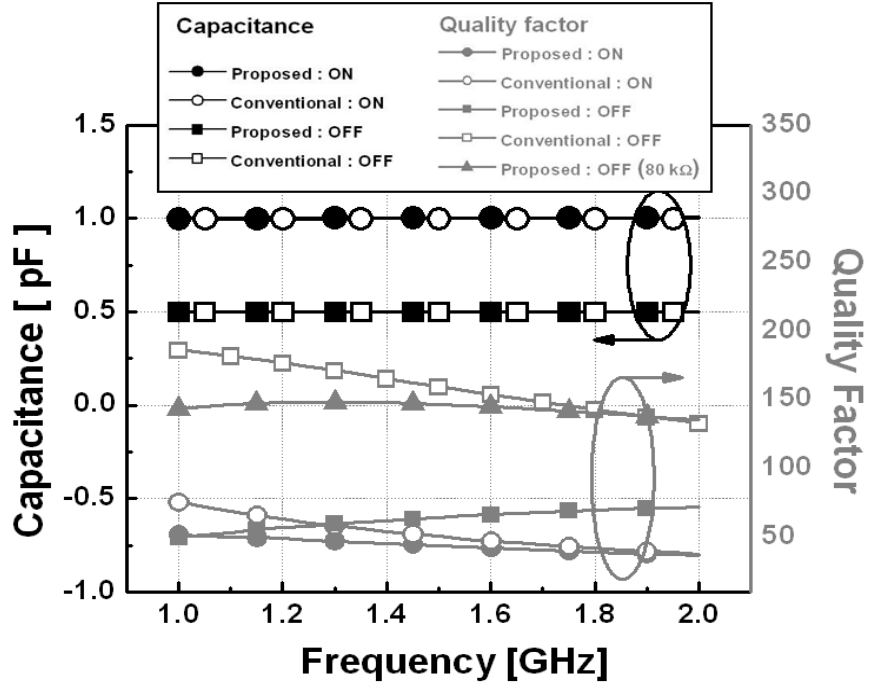


Figure 9. The simulated Q and capacitance of the proposed and conventional structures.

The power capabilities of the proposed and conventional structures are analyzed and compared. In both structures, the voltage swing across the switch transistor in the off-state condition is much larger than in the on-state. Thus, the power capability is mainly determined by the off-state. Figure 10(a) and (b) represent the equivalent circuits of switched capacitors in Figure 8(a) and (b) with an off-state switch, respectively. In the equivalent circuits, a signal path to the p-substrate through the DNW is neglected for simplicity. To keep an off-state condition of the switch transistor, the positive peak of the voltage between the gate and source (V_{gs}) should be less than the threshold voltage (V_{th}). Since the proposed structure has a reverse DC bias of V_{DD} across the gate and source, V_{gs} of the proposed structure is not limited by V_{th} but limited by $V_{th}+V_{DD}$. More detailed analysis is presented in the following section with simulation results.

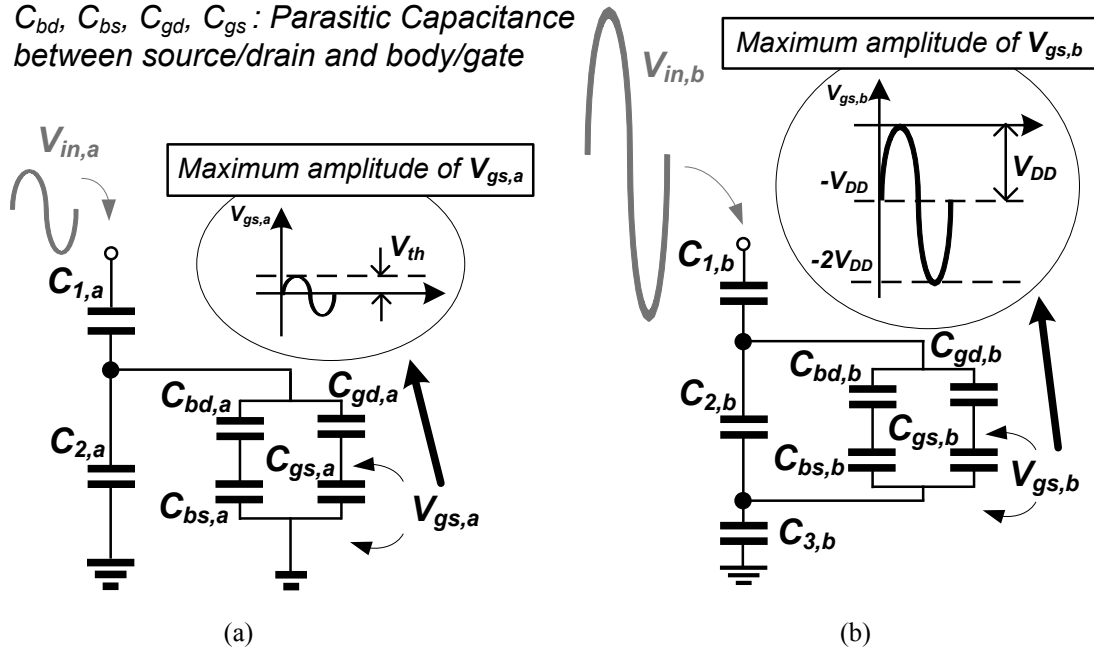


Figure 10. Small signal equivalent circuit for (a) a conventional structure and (b) the proposed structure when the switch is off.

In the case of designed switched capacitors with a 2:1 tuning ratio, the total applied voltage swing (V_{in}) is four times larger than V_{gs} . Thus, the allowable amplitude of V_{in} for Figure 8(a) and (b) are $4 \cdot V_{th}$ (3.3 V) and $4 \cdot V_{DD}$ (13.2 V), respectively. Certainly, if the tuning ratio changes, the absolute value of the allowable amplitude of V_{in} also changes. However, the ratio between the allowed values of V_{in} , which is 12-dB (V_{DD}/V_{th}) in this case, does not change.

Figure 11 shows simulated capacitance and Q values of the designed switched capacitors according to the applied voltage amplitude across the switched capacitor. The proposed structure maintains its capacitance constantly up to 13.2 V of V_{in} , while the capacitance of the conventional structure starts to increase around 3.3 V of V_{in} because of

switch turning-on. This result demonstrates much improved power capability of the proposed structure and matches well with the calculation result. Meanwhile, the Q value does not approach to the result with the turn-on switch in Figure 9 but decreases to zero. This discrepancy occurs because the switch transistor partially turns on due to the applied signal rather than completely turns on.

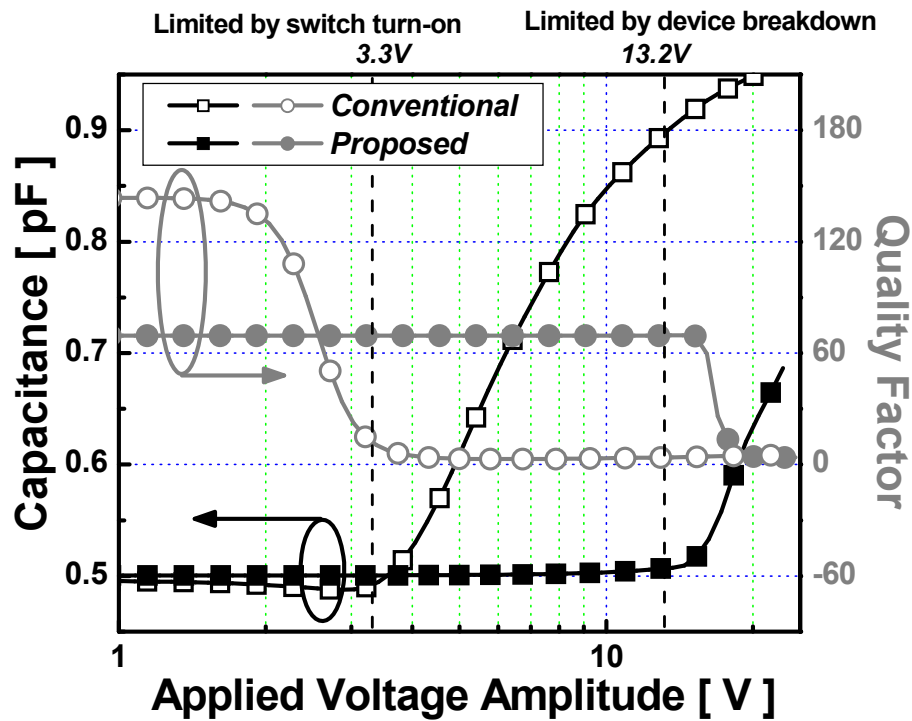


Figure 11. The simulated Q and capacitance of the proposed and conventional structures with respect to applied voltage amplitude across the switched capacitor when the switch is off ($f=1.8$ GHz).

The linearity is typically measured by two-tone third-order inter-modulation distortion (IMD3). The proposed structure shows improved IMD3 characteristics thanks to the improved power capability compared to the conventional structure in the high-power region. In addition, the p-n junction is reverse-biased by V_{DD} in the proposed structure, while it is zero-biased in the conventional structure. Thus, the proposed structure improves linearity in the low-power region by shifting the bias condition that minimally affects the depletion capacitance of the junction. The linearity performance is compared with measurement results in the next section.

2.3. Measurement Results

We utilized the measurement setup in Figure 12 for one-tone large-signal characterization, which can demonstrate the impedance variation of a switched capacitor. The incident power (P_{inc}) and reflected power (P_{ref}) for the device under test (DUT) are measured. Since the amount of reflected power is determined by the impedance of the DUT, the variation of the power ratio (P_{inc}/P_{ref}) is an indication of whether the impedance of the DUT is varied or not. Since purely imaginary impedance reflects all of the incidence power, the $50\ \Omega$ termination is placed next to the DUT in the measurement. Figure 13 represents the one-tone measurement results, which are in good agreement with the simulation data. In the on-state, the results for both cases show constant capacitance values with respect to the applied power. It indicates that both on-state capacitors can maintain their capacitance values at a constant value up to more than 30-dBm. In contrast, when the switch is off, the results are entirely distinct. If a signal greater than 20-dBm, which is close to a theoretical limit of $4 \cdot V_{th}$ (3.3 V), is applied to the conventional

structure, the amount of reflected power significantly increases, which indicates the increase of the capacitance value. The capacitance value becomes about 0.8 pF at 30-dBm power level. However, the proposed structure maintains its capacitance value up to a power level of 30-dBm. This result shows that the proposed structure has a significantly improved power capability.

Figure 14 shows the two-tone measurement results by using the test setup in [7]. We use two 2-MHz-spaced signals ($f_1=1.8$ GHz and $f_2=1.802$ GHz). In the on-state, both structures show similar results for the same reason in Figure 13. However, in the off-state, the IMD3 characteristic for the conventional structure is significantly inferior to that of the proposed structure. For instance, the proposed structure shows more than 34-dB improved IMD3 characteristics at 18-dBm power level. This measurement result is a very meaningful demonstration of the high-power application of the proposed structure in terms of linearity.

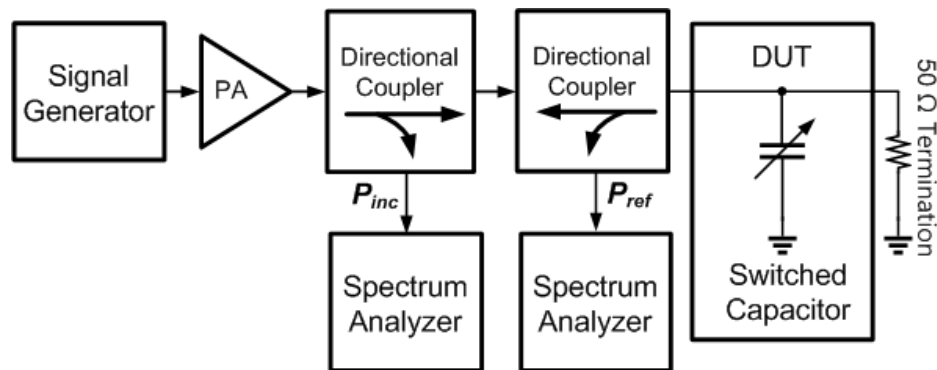
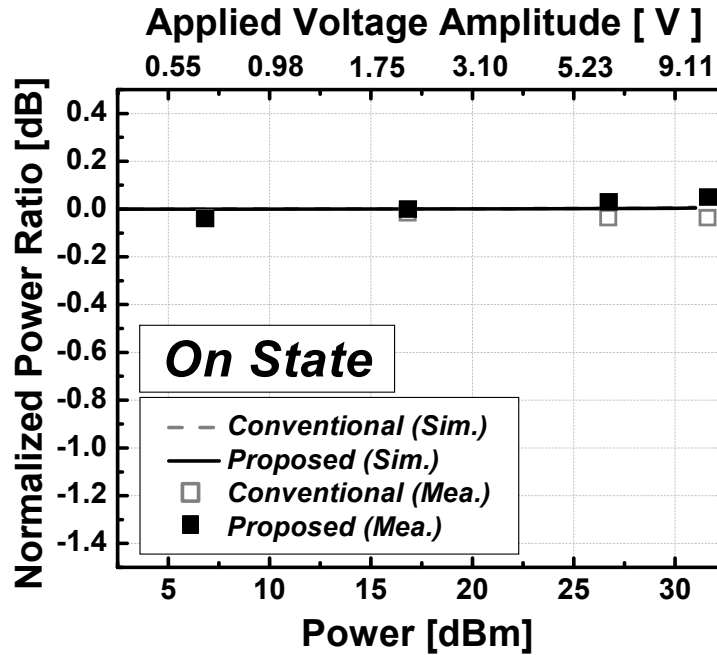
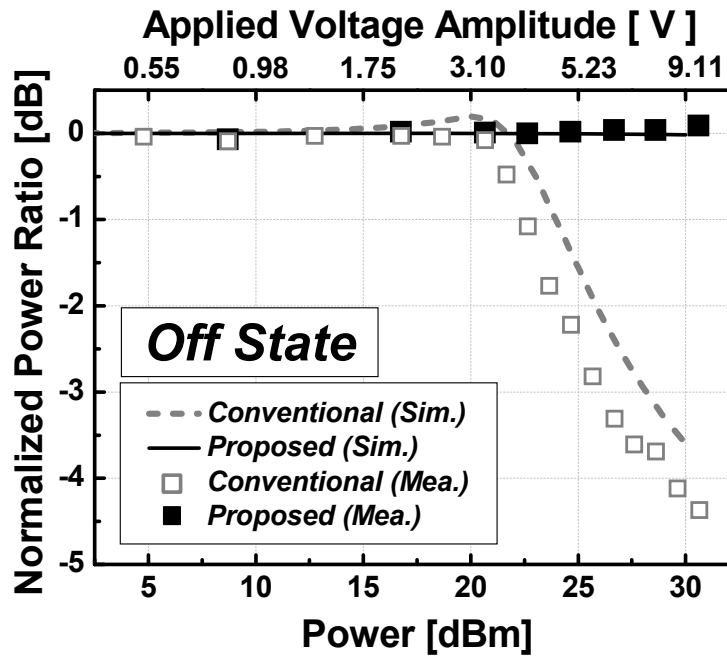


Figure 12. One-tone large signal measurement test setup.



(a)



(b)

Figure 13. One-tone large signal measurement results with (a) on-state switch and (b) off-state switch. Lines represent simulation results, and symbols are measurement results ($f=1.8$ GHz).

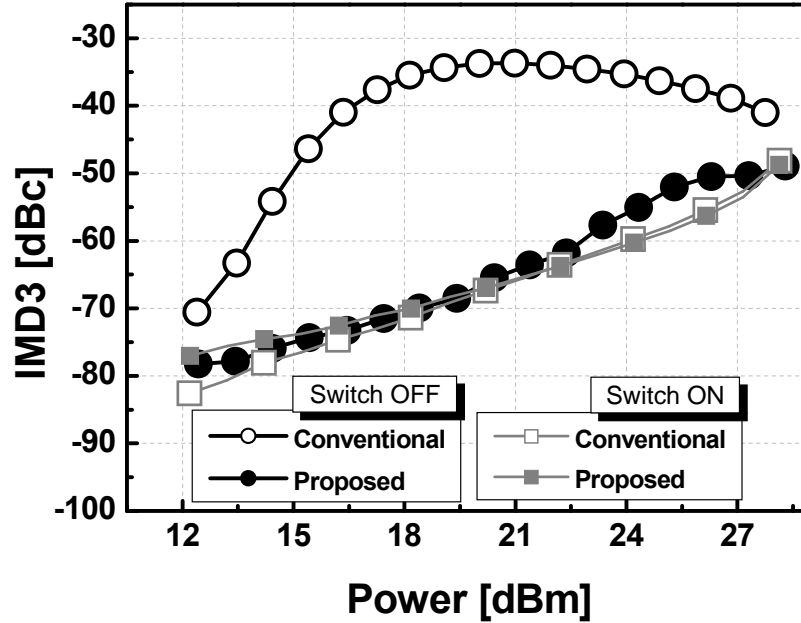


Figure 14 Two-tone measurement results for the conventional (open symbol) and the proposed (solid symbol) structure ($f_1=1.8$ GHz and $f_2=1.802$ GHz).

2.4. Power Handling Capability of Switched Capacitor

In Chapter 2.3, the conventional and the proposed switched capacitors are compared in terms of power capability. In this section, the maximum allowable voltage amplitudes for each structure with respect to a tuning ratio and the number of stacked switch transistors are derived and compared. Since the power capability of the switched capacitor is mainly determined by off-state operation, it is necessary to investigate off-state operation for deriving the maximum allowable voltage amplitude.

In the case of Figure 8(a), the turn-on and turn-off capacitance are equal to $C_{1,a}$ and $C_{1,a} \parallel C_{2,a,total}$, respectively, where \parallel represents a series combination of two capacitors, and $C_{2,a,total}$ indicates $C_{2,a} + (C_{bd,a} \parallel C_{bs,a}) + (C_{gd,a} \parallel C_{gs,a})$. If the ratio between the turn-on and -off capacitance is $N:1$, the following equations can be derived.

$$C_{1,a} : (C_{1,a} \parallel C_{2,a,total}) = N : 1. \quad (1)$$

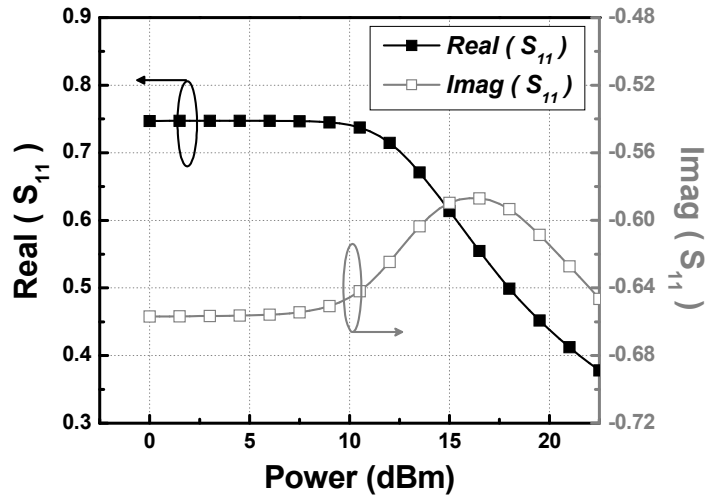
With given equation (1), the total voltage swing across the switch transistor, M_a , is

$$V_{ds,a} = \frac{C_{1,a}}{C_{1,a} + C_{2,a,total}} V_{in,a} = \left(1 - \frac{1}{N}\right) V_{in,a}. \quad (2)$$

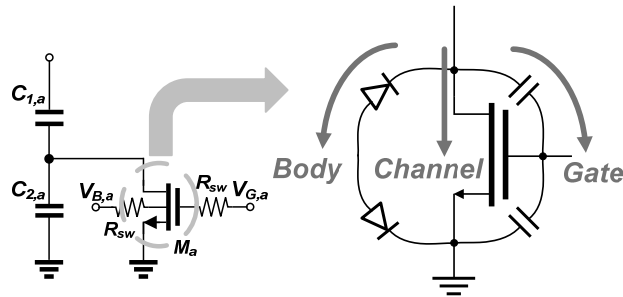
If it is assumed that two capacitors, $C_{gd,a}$ and $C_{gs,a}$, have the same value, the applied voltage to $C_{gs,a}$ (V_{gs}) is half of the $V_{ds,a}$,

$$V_{gs,a} = \frac{1}{2} \left(1 - \frac{1}{N}\right) V_{in,a}. \quad (3)$$

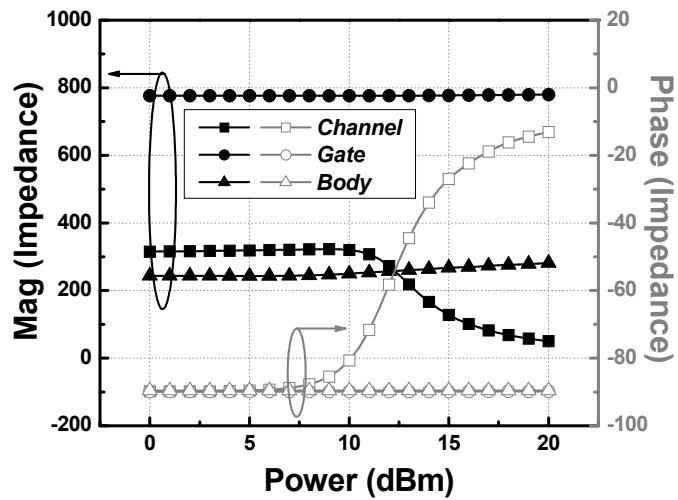
By the same derivation, the applied voltage swing across junction diodes, $C_{bd,a}$ and $C_{bs,a}$ is equal to the equation (3).



(a)



(b)



(c)

Figure 15. (a) Simulated impedance according to the power level, (b) three different current paths, and (c) simulated impedance depending on the signal paths with respect to power level in a turned-off switched capacitor.

When a large voltage swing is applied to a turned-off switch transistor, undesirable distortion can be originated from different causes, which include channel formation of a transistor and forward biasing of a junction diode. If a channel formation is the main cause, voltage differences between a gate and a source/drain should be less than the threshold voltage (V_{th}). On the other hand, if the junction diode is more critical, voltage differences between a body and a source/drain also should be less than junction turn-on voltage ($V_{on, junction}$). Therefore, understanding which mechanism is more decisive is required to define a voltage limitation.

Figure 15(a) shows the result of a large-signal S-parameter (LSSP) simulation in Advanced Design System (ADS). The switched capacitor that has the tuning ratio of 2:1 (i.e. 1.0/0.5 pF at on/off-state) and a thick-oxide switch transistor is used for this simulation. As shown in Figure 15(a), the off-state impedance starts to distort around the 10-dBm power level. To find out the major source of this distortion, the signal path through the switch transistor is divided into three parts which are body, channel, and gate as described in Figure 15(b). By referring the amount of current through the different paths, the impedance of each signal path is extracted and presented in Figure 15(c). Since the transistor is turned off, all of the signal paths show capacitive impedance at the small signal region. However, after 10-dBm power level, the magnitude of the channel impedance decreases significantly, and the phase approaches starts to show resistive characteristics, while the other two paths remain capacitive. Therefore, we can conclude that the distortion of the switched capacitor under large-signal operation comes from the channel formation of the switch transistor. Since the junction diodes are connected in series with reverse direction, they cannot be forward biased at the same time. As a result,

V_{th} is more critical for turn-on phenomenon than $V_{on, junction}$, which means that $V_{gs,a}$ should be less than V_{th} . Therefore, the maximum allowable voltage amplitude to the conventional switched capacitor with a tuning ratio of N is derived as

$$\frac{1}{2} \left(1 - \frac{1}{N}\right) V_{in,a} < V_{th} . \quad (4)$$

$$V_{in,a} < \frac{2 \cdot N \cdot V_{th}}{N-1} . \quad (5)$$

In the case of the proposed structure in Figure 8(b), the turn-on and turn-off capacitances are equal to $C_{1,b} \parallel C_{3,b}$ and $C_{1,b} \parallel C_{3,b} \parallel C_{2,b,total}$, where $C_{2,b,total}$ indicates $C_{2,b} + (C_{bd,b} \parallel C_{bs,b}) + (C_{gd,b} \parallel C_{gs,b})$. By the similar manner with Figure 8(a), the applied voltage amplitude across $C_{gs,b}$ and $C_{bs,b}$ with the tuning ratio of $N:1$ is

$$V_{gs,b} = V_{bs,b} = \frac{1}{2} \left(1 - \frac{1}{N}\right) V_{in,b} . \quad (6)$$

Although the equation (6) is the same with (3), the cause of power handling limitation is different from Figure 8(a). Since the reverse DC bias of V_{DD} is applied to V_{bd} , V_{bs} , V_{gd} , and V_{gs} , the maximum allowable voltage swing that can be accepted by $V_{gs,b}$ is not V_{th} but $V_{th} + V_{DD}$. However, if the magnitude of the applied signal to $C_{gs,b}$ is larger than V_{DD} , the total applied voltage across the gate oxide becomes more than $2 \cdot V_{DD}$, which may induce device reliability [2]. In common CMOS PA design practice, the maximum voltage swing across any two nodes in the device should be below twice the nominal supply voltage

($2 \cdot V_{DD}$). As a result, the power capability of Figure 8(b) is not restricted by the device turn-on but is limited by device reliability, which is $2 \cdot V_{DD}$. Therefore, the maximum voltage amplitude that can be applied to Figure 8(b) is given as following:

$$\frac{1}{2} \left(1 - \frac{1}{N}\right) V_{in,b} < V_{DD}. \quad (7)$$

$$V_{in,b} < \frac{2 \cdot N \cdot V_{DD}}{N-1}. \quad (8)$$

Meanwhile, the stacked switch structure is widely utilized to increase power handling capability in a high-power switch design [7], [10]. The proposed switched capacitor can also adopt the stacked structure to increase allowable voltage amplitude. Figure 16 presents the general structures of the switched capacitors with the stacked switches. The equation (5) and (8) for the maximum allowable voltage amplitude can be generalized. The generalized equation for Figure 16(a) and (b) are shown as equation (9) and (10), respectively.

$$V_{in,a} < \frac{2 \cdot M \cdot N \cdot V_{th}}{N-1}. \quad (9)$$

$$V_{in,b} < \frac{2 \cdot M \cdot N \cdot V_{DD}}{N-1}. \quad (10)$$

, where M represents the number of stacked transistors.

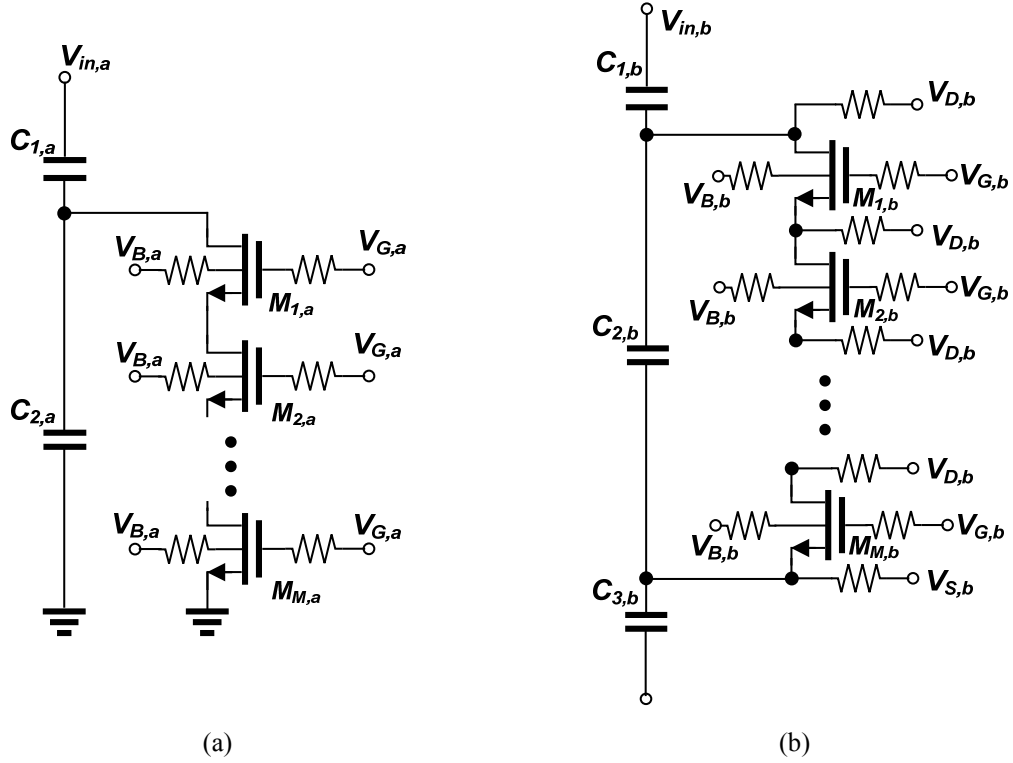


Figure 16. The switched capacitor with M-stacked switch transistors: (a) conventional structure and (b) proposed structure.

Consequently, all the dependant variables of the maximum allowable voltage amplitude that are a tuning ratio (N), a type of a switch transistor (V_{th} and V_{DD}), and the number of stacked switch transistors (M) are considered in equation (9) and (10). The calculated maximum allowable voltage swing across the switched capacitor for the conventional and proposed structure with both a thin and a thick gate-oxide transistor is illustrated in Figure 17. When designing a switched capacitor for high-power applications, the presented data in Figure 17 is to be referred to decide the type of a transistor and the required number of stacked transistors. As depicted in Figure 17, the maximum voltage amplitude is strongly dependent on the tuning ratio as well as the type of the switch

transistor. Since the applied voltage to the switch transistor increases as a tuning ratio increases, the switched capacitor with a larger tuning ratio is to have less power capability. In both kinds of transistor, the proposed structures have much improved power handling capability. For example, the maximum voltage amplitude of the proposed structure with even single switch transistor is larger than that of the conventional structure with three-stacked switches.

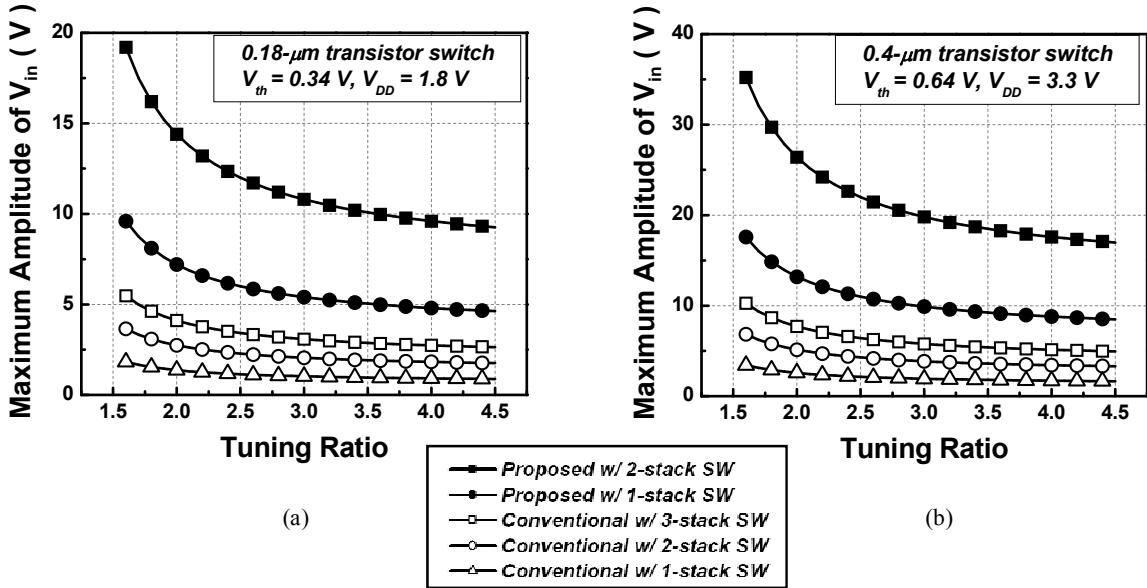


Figure 17. Calculated maximum allowable voltage amplitude across a switched capacitor according to the tuning ratio: (a) a 0.18- μm thin gate-oxide and (b) a 0.4- μm thick gate-oxide switch transistor.

The calculated limitation of the voltage swing across the switched capacitor is confirmed with a LSSP simulation. For the purpose of comparison, we explored four kinds of switched capacitors with 2:1 tuning ratio (i.e. 1.0/0.5 pF at on/off-state). Table 3 summarizes the structures and all the design parameters for four switched capacitors. All of four switched capacitors have the same quality factor (Q) of 30 in the on-state, and Q is larger than 100 for all cases in the off-state at 2.4 GHz. Since the large-signal operation is limited by the turn-off state, the off-state switched capacitors are investigated. The value of the S_{11} of the turned-off switched capacitor (0.5 pF) is calculated on the assumption of the 50 Ω termination, which is $0.75-j0.66$ at 2.4 GHz. Both real and imaginary of S_{11} should be constant up to certain power level of which the switched capacitor is expected to be valid.

Table 3. The capacitance of the MIM capacitors and width of switch transistors of the four kinds of switched capacitors.

	Structure	C_1 (pF)	C_2 (pF)	C_3 (pF)	M_1 (mm)	M_2 (mm)	M_3 (mm)
CASE 1	Figure 8(a)	1	0.58	N/A	0.58	N/A	N/A
CASE 2	Figure 8(b)	1.93	0.67	1.93	0.6	N/A	N/A
CASE 3	Figure 17(a) w/ 2-stacked SW	1	0.52	N/A	1.17	1.17	N/A
CASE 4	Figure 17(a) w/ 3-stacked SW	1	0.43	N/A	1.73	1.73	1.73

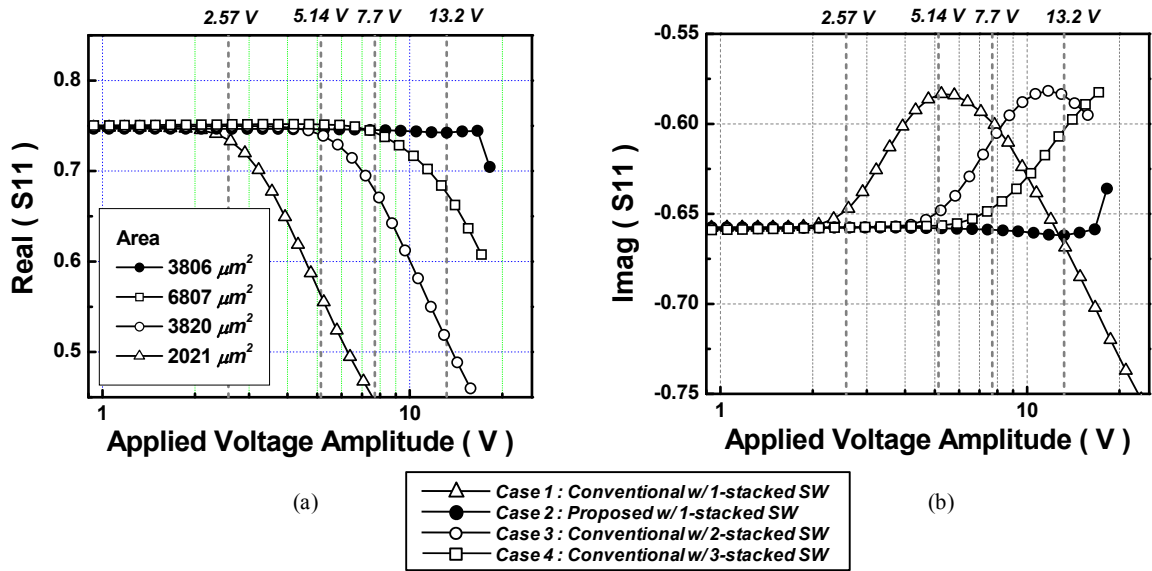


Figure 18. LSSP simulation results with four kinds of tunable capacitor (case 1, 2, 3, and 4): (a) real of S_{11} and (b) imaginary of S_{11} .

Figure 18 presents simulated S-parameters according to the applied voltage amplitude. By the equation (7) and (8), the maximum allowable voltage amplitudes for case 1, 2, 3, and 4 are calculated as 2.57, 13.2, 5.14, and 7.7 V, respectively, which are illustrated with dotted vertical gray lines in Figure 18. In cases of conventional structures, the simulated voltage amplitude, from which S_{11} starts to deviate from the designed value, is well coincident with calculated value. However, the proposed structure maintains its value up to more than calculated limitation. Since the power capability of the proposed structure is not limited by a distortion but by device reliability, the distinction between the calculation and simulation occurs. As illustrated in Figure 18, the proposed structure maintains its value up to much higher voltage level than the conventional structure. Even

though the proposed structure is much suitable for a high-power application, four switched capacitors compared in Figure 18 have different areas. Since the proposed structure requires more layout area, the area needs to be taken into account for more reasonable comparison, and Figure 18(a) contains the area information. The proposed structure has comparable area with the two-stacked conventional switched capacitor. Therefore, it is reasonable to conclude that the proposed structure has better power capability while considering even area.

In addition, there is another design parameter to be considered for a switched capacitor. Figure 19 illustrates a simulated maximum possible Q values according to a tuning ratio for both a thin and thick-oxide transistor. Since a large transistor has more parasitic capacitance, there exists maximum size of a switch transistor to obtain a certain tuning ratio. Therefore, the maximum value of Q is inversely proportional to a tuning ratio as described in Figure 19. Accordingly, if the required tuning ratio is decided, the maximum Q value is determined. Figure 19 presents another interesting results between a thin and thick-oxide transistor. Even though a required width of a thick-oxide transistor is larger than that of a thin-oxide for the same Q value, the resulting tuning ratios show similar values with each other. This is because a parasitic capacitance per unit width of the thick-oxide transistor is smaller than that of the thin-oxide.

Meanwhile, if the required Q value of a tunable matching network is less than the maximum value presented in Figure 19, a parallel capacitor to the switch transistor ($C_{2,a}$ and $C_{2,b}$ in Figure 8) can be used to design a switched capacitor with a less Q value and better linearity under the same tuning ratio. Since most of nonlinearities originate from a active device, the switched capacitor with a smaller transistor and larger $C_{2,b}$ has better

linearity characteristics. Fig. 20 presents the simulated third order input intercept point (IIP3) of switched-capacitors according to the tuning ratio and Q values. A 20-MHz spacing two tone signal ($f_1=2.39$ and $f_2=2.41$) is used for this simulation. As illustrated in Fig. 20, a switched capacitor with a less Q value presents an improved linearity performance. Consequently, designing a switched capacitor with the minimum required Q is beneficial with respect to linearity. As a results, the required minimum Q value along with a tuning ratio and maximum applied voltage swing is essential information when designing a switched capacitor.

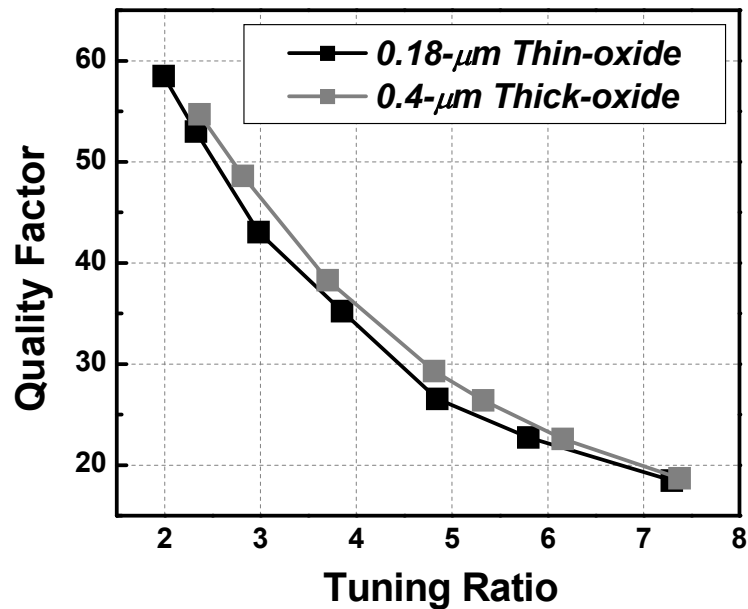


Figure 19. Simulated maximum possible quality factor according to a tuning ratio.

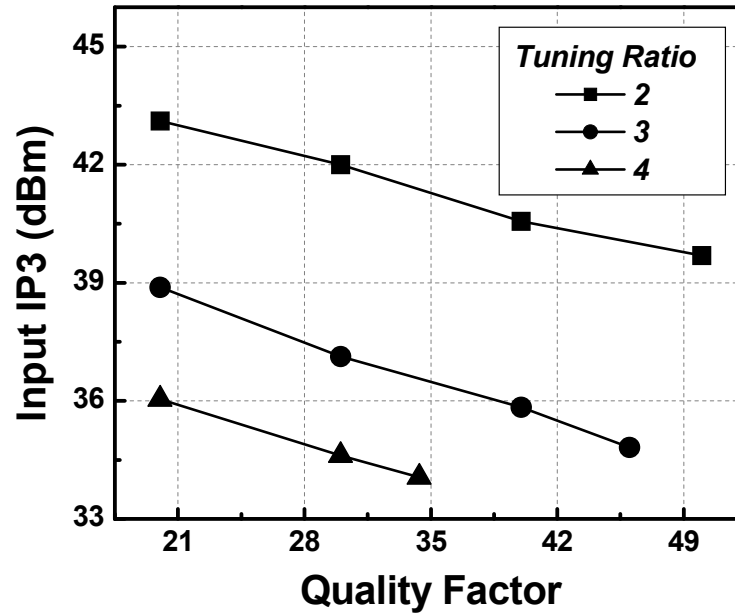


Figure 20 IIP3 of the turned-off switched capacitor according to the Q value.

2.5. Conclusions

In this chapter, the new switched capacitor structure for high-power applications in a CMOS technology is introduced. The maximum allowable voltage amplitude to the switched capacitor is derived and validated with simulations. The derived voltage limitation is to be a guideline when designing the switched capacitor for high-power applications.

CHAPTER 3

A DUAL-MODE CMOS PA WITH ENHANCED LOW-POWER EFFICIENCY

3.1 Introduction

As introduced in Chapter 1, battery lifetime has been a major concern for terminal users ever since a mobile terminal was introduced. Many researchers have strived for extending the battery lifetime, and especially the improvement of low-power (LP) efficiency is at the center of attention. The output power of a PA must be adaptable to a power control signal. Therefore, the average efficiency of a PA is determined by taking into account the probability distribution function of the output power level. In most cases, the percentage of time that a PA operates at backed-off power is dominant [11]. Meanwhile, the efficiency of a conventional PA decreases rapidly as the output power is backed off from the maximum power level. Thus, the efficiency enhancement in a LP region is significant to extend the battery lifetime.

To improve the LP efficiency of a PA, diverse techniques have been proposed. Among reported techniques, dynamic bias control [12, 13], envelope tracking (ET) [14], and envelope elimination and restoration (EER) [15] can be categorized into one group. These techniques change the bias condition dynamically according to the instantaneous output power level. Even though these techniques are effective to increase the efficiency over the entire output power range, they have practical challenges such as significant gain

variation, limited efficiency and bandwidth of a DC-DC converter, and mismatch between amplitude and phase. Furthermore, a supply voltage modulation method in a CMOS PA introduces an additional issue related with a cascode structure, which is typically employed in a CMOS PA design to sustain high voltage stress. Decreasing a supply voltage easily makes a cascode structure out of the saturation condition. Consequently, these techniques induce various linearity problems, so additional complicated circuits should be considered to achieve linearity requirements.

On the other hand, physical size reduction methods form another major group with less complexity [16]-[22]. This technique generally introduces the LP mode with a reduced size power transistor to improve the LP efficiency. Even though the size reduction approach is effective with relatively simple structure, it requires a load line adaptation to be a more complete solution. As shown in Figure 21, the DC current consumption decreases with size reduction, and it helps to improve the efficiency in the LP mode. However, if a load-line for the high-power (HP) mode is used for the LP mode, the maximum voltage swing at the drain node is limited and much smaller than that with the optimized LP mode load-line. (i.e., $V_{\max1}$ is much smaller than $V_{\max2}$.) Accordingly, the LP mode with a fixed matching network can not generate maximum output power and maximum efficiency.

Because of this constraint, a load-line adaptation exploiting a tunable matching network has been widely utilized to maximize the efficiency [6], [7], [23], [24]. However, most of the tunable matching networks have been implemented using special process devices such as a varactor in a silicon-on-glass technology, a MEMS device, an off-chip commercial component, which are not suitable for a fully integrated CMOS PA [6], [23],

[24]. Even though an integrated tunable matching network in a Si-based technology was successfully demonstrated in [7], it was implemented in a silicon-on-insulator (SOI) CMOS technology rather than a standard CMOS process. In this design, the dual-mode CMOS PA with an integrated tunable matching network in a standard CMOS process is presented [25].

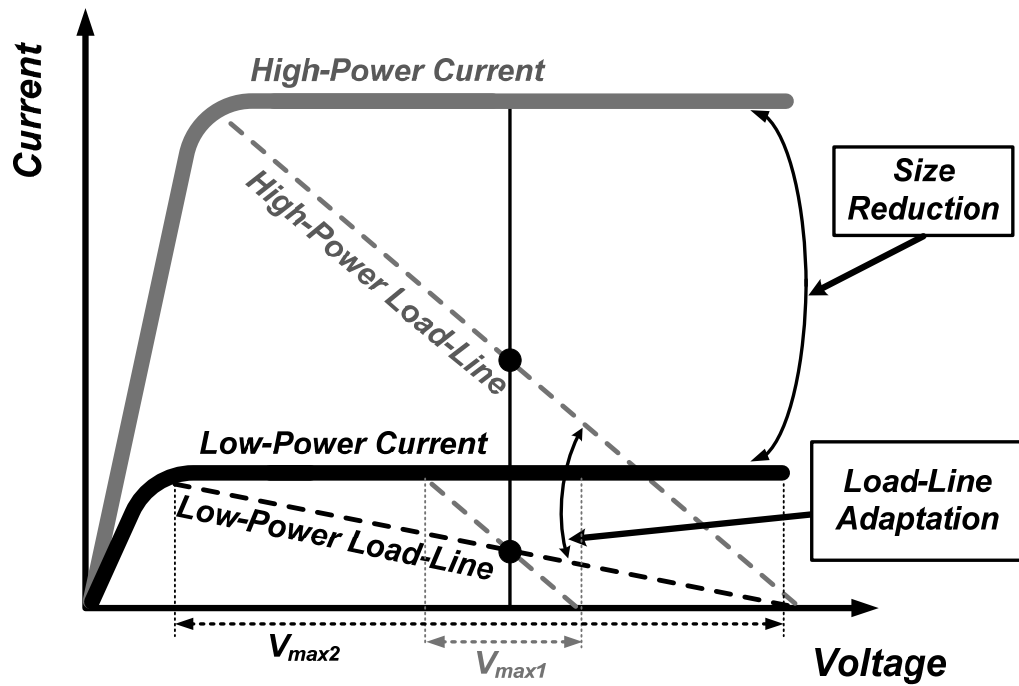


Figure 21. Diagram of load-lines according to the power modes.

3.2 Schematic and Operation

The schematic of the dual-mode CMOS PA with switched capacitors is shown in Figure 22, exploiting a single-ended structure. Even though this design utilizes the single-ended topology, the proposed technique is also applicable to a differential design. The proposed PA has two-stage topology to have sufficient gain, and both a driver and power stage of it exploits a cascade structure to avoid the possibility of the device failure. A thick-oxide transistor is used as a common-gate (CG) device to sustain a large-voltage swing across the drain and the gate, and a thin-oxide transistor is used as a common-source (CS) device to secure sufficient gain.

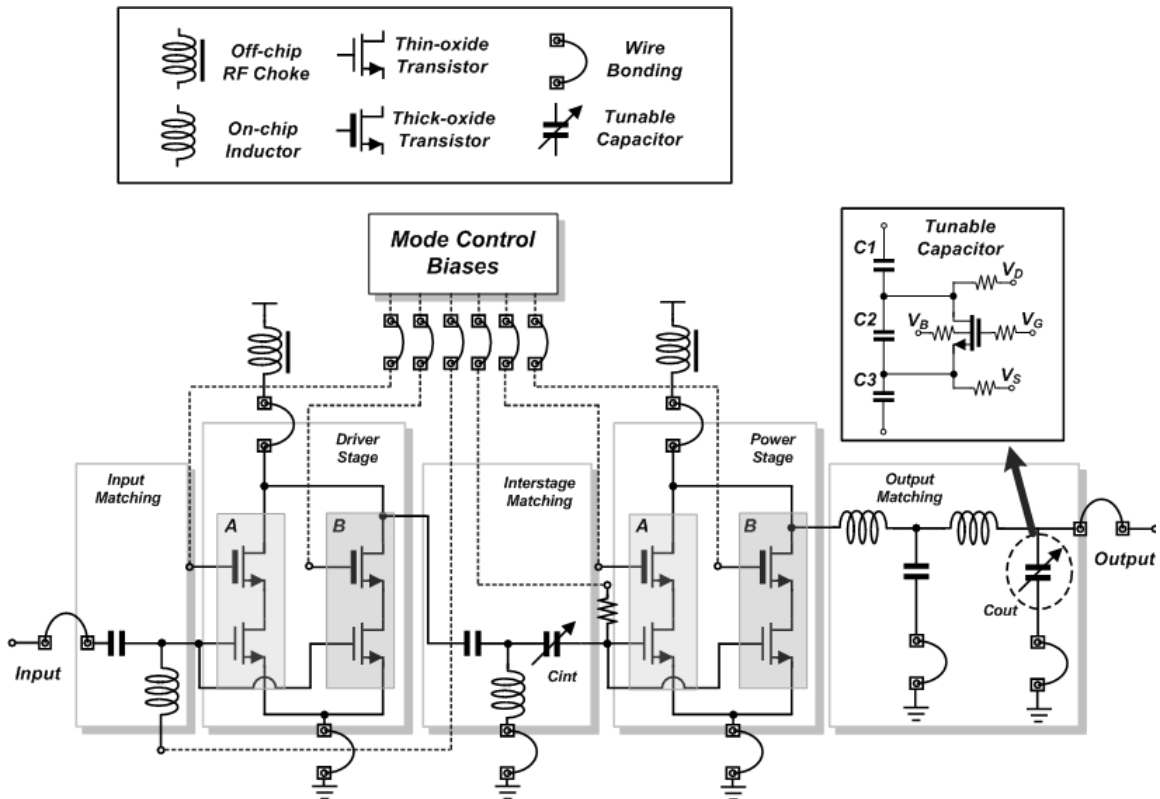


Figure 22. Schematic of the dual-mode CMOS PA with an integrated tunable matching network.

The operation of the PA in Figure 22 can be understood with the help of Figure 21. The PA has two distinct power-modes, a HP mode and a LP mode, which have different current levels and load lines for each operation as described in Figure 21. The different current levels set the power capabilities [16], [22], and the different current levels require distinct load lines, which are essential for the PA to have optimized efficiency in both modes [26]. The tunable matching network is employed to support required optimum matching impedance for the HP and LP mode. In this design, the different current levels are realized by area resizing, and the load lines are accomplished by utilizing the switched capacitor. The gate biases and transistor sizes for the driver and the power stages and the required value of switched capacitors are summarized in Table 4.

Table 4. Area resizing information and tunable capacitor values.

<i>Mode</i>	<i>Driver stage resizing</i>			<i>Power stage resizing</i>			<i>Tunable Capacitor</i>	
	<i>Vg_cs</i> ¹ (V)	<i>Used Tr. Size</i> ² (μm)		<i>Vg_cs</i> (V)	<i>Used Tr. Size</i> (μm)		<i>Cint</i> (pF)	<i>Cout</i> (pF)
		<i>CS</i> ³	<i>CG</i> ⁴		<i>CS</i>	<i>CG</i>		
<i>HP</i>	0.47	400	500	0.5	2500	3500	1.9	1.4
<i>LP</i>	0.5	80	100	0.53	500	700	2.6	2.5

¹Gate bias of the common-source transistor

²Used. Tr. Size is controlled by gate bias of the CG transistor

³Common source and ⁴common gate

First, the different current levels are achieved by utilizing a cascode structure. Both the driver stage and the power stage have two different paths which are indicated with “A” and “B” in Figure 22. In both stages, the sizes of transistors in “B” are four times larger than those in “A”. For the HP mode operation, both A- and B- paths are turned on, while in the LP mode, the B-paths are turned off by setting the gate bias of the CG transistor to GND. When the B-paths are turned off, the magnitude of the voltage difference between the gate and the drain (V_{gd}) of the CG transistor in B-paths can be significantly high. The high voltage stress problem is relieved with thick-oxide CG transistors and its safe operation was confirmed with a simulation. Second, a tunable matching network is accomplished by exploiting the switched capacitor. Both of the inter-stage and the output matching networks are modified.

3.3 Tunable Matching Network Design

Among the two tunable matching networks (inter-stage and output matching), the output matching network is investigated because it requires higher power operation. Figure 23 shows two required output matching points that are corresponding to the HP and LP modes. Both matching points are determined by a load pull analysis to obtain a high output power as well as high efficiency. If we consider a parallel device capacitance at the drain node, it can be confirmed that the required load impedance at LP mode is larger than that of HP as explained in Figure 21. Two impedance points are realized by employing a two-stage LC matching network with a switched capacitor as described in Figure 23, which also presents all design values for inductors and capacitors to realize the impedance points at 2.4 GHz. When designing a tunable matching network, two design

issues related with a switched capacitor should be considered: a power loss and power handling capability.

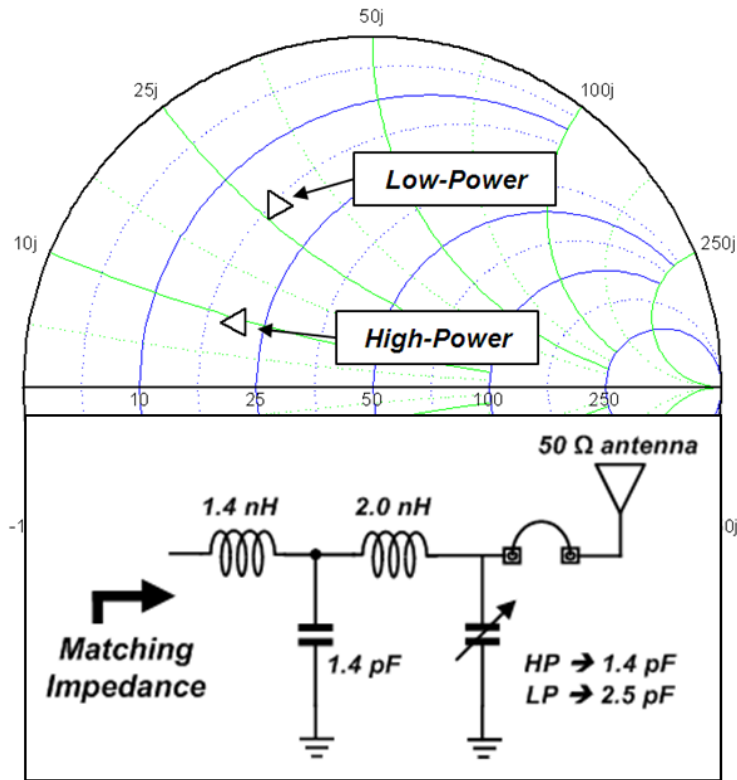


Figure 23. Optimum matching impedances for both high- and low-power modes. The tunable matching network is presented with components' values.

First, the power loss needs to be considered when the switched capacitor is in the on-state. Since the Q value of the switched capacitor in the on-state is much lower than that of a MIM capacitor, the power loss of the tunable matching network can significantly increase compared to the fixed matching network with a MIM capacitor. In this design, the switched capacitor becomes the on-state in the LP mode. Figure 24 exhibits the maximum available gain of the output matching network in the LP mode according to the

Q value of the switched capacitor. As described in the Figure 24, the power loss due to the degraded Q value becomes substantial when Q is less than 20. Therefore, more than 30 of the Q value for the on-state switched capacitor is required to minimize the power loss introduced by the tunable matching network.

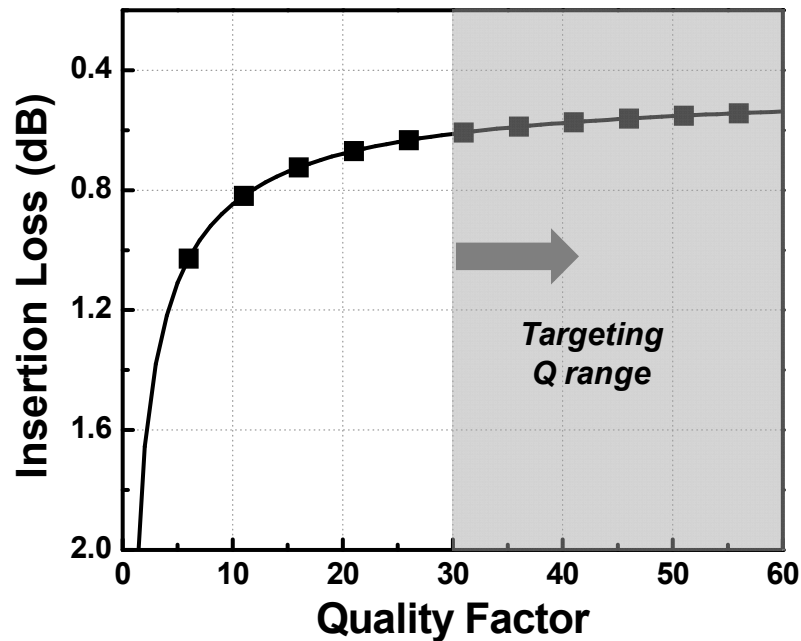


Figure 24. Maximum available gain of the output matching network according to the quality factor of the switched capacitor in the LP mode.

Secondly, the power handling capability must be considered when the switched capacitor is in the off-state, which is the HP mode in this design. The maximum allowable voltage amplitude in Figure 17 should be the guideline for this consideration. In this design, the required tuning ratio of the switched capacitor is 1.78 (2.5 pF divided by 1.4 pF), and the maximum voltage swing across the switched capacitor is 5.5 V. From

the Figure 17, the proposed structure with a thin or thick gate-oxide transistor switch can handle more than 5.5 V of voltage swing under the tuning ratio of 1.78. In this design, a 0.18- μm thin-oxide transistor is used to show superior high-power performance of the proposed structure.

Two tunable matching networks were designed and compared. One was implemented with a conventional switched capacitor with a 0.18- μm transistor, and the other was implemented with a proposed switched capacitor with a 0.18- μm transistor [27]. Both switched capacitors have the capacitance of 2.5 pF with the Q of 35 in the on-state and the capacitance of 1.4 pF with the Q of more than 150 in the off-state at 2.4-GHz. By using the equation (9) and (10), the maximum allowable voltage amplitudes for the conventional and proposed structure are 1.6 V and 8.2 V, respectively.

To compare the power capability of the tunable matching networks with two different switched capacitors, the input impedances of the matching networks are simulated as the applied power increases. By referring these simulation results, it can be validated whether the targeted matching impedance is well maintained or not under the large-signal environment. Figure 25 exhibits the simulated results, in which the triangle symbols indicate the target impedance points for the HP and LP modes. The applied power increases up to 29-dBm at the 50- Ω antenna port, which is corresponding to the voltage amplitude of 9 V across the switched capacitor that is much larger than the targeted output power.

As illustrated in Figure 25, both tunable matching networks well maintain their matching points in the case of the LP mode. In the LP mode, the switched capacitor is on, so the applied voltage to the switch transistor is not significant. Thus, increasing power

level does not affect the matching impedance of the tunable matching network. On the contrary, In the HP mode, the switched capacitor is turned off, so the applied voltage to the switch transistor is substantial. As a result, the HP mode shows distinct results between the conventional and the proposed structure. The tunable matching network with the proposed structure maintains its initial designed matching impedance while that with the conventional structure varies according to the power level. When the matching impedance deviates from the original designed point, the power level with the corresponding voltage amplitude across the switched capacitor for the conventional structure is illustrated in Figure 25. The matching impedance starts to distort at the voltage amplitude of 2.1 V. The impedance deviation is more investigated in Figure 26.

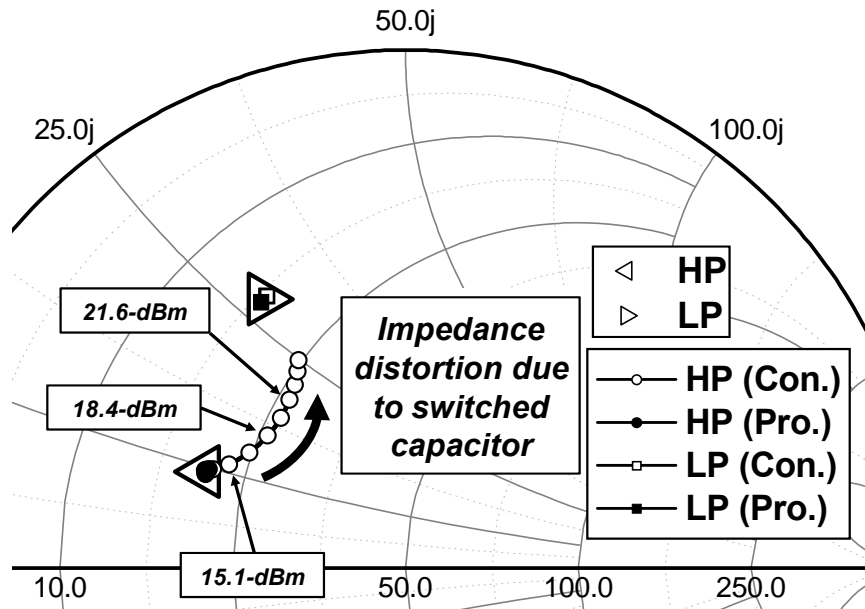


Figure 25. The variation of the matching impedance points according to the power level.

Figure 26 presents the simulated real and imaginary part of the matching impedance according to the voltage amplitude across the switched-capacitor in the HP mode. The calculated maximum allowable voltage amplitude of 1.6 V and 8.2 V are indicated with dashed lines. The expected maximum voltage amplitude in this design, 5.5 V, is also presented. As illustrated in the Figure 26, the tunable matching network with the conventional switched capacitor starts to distort the matching impedance after 1.6 V, while that with the proposed structure maintains its matching impedance up to 10 V. From the results in both Figure 25 and 26, it can be confirmed that the matching network with the proposed structure can guarantee the desired matching impedance with a sufficient margin.

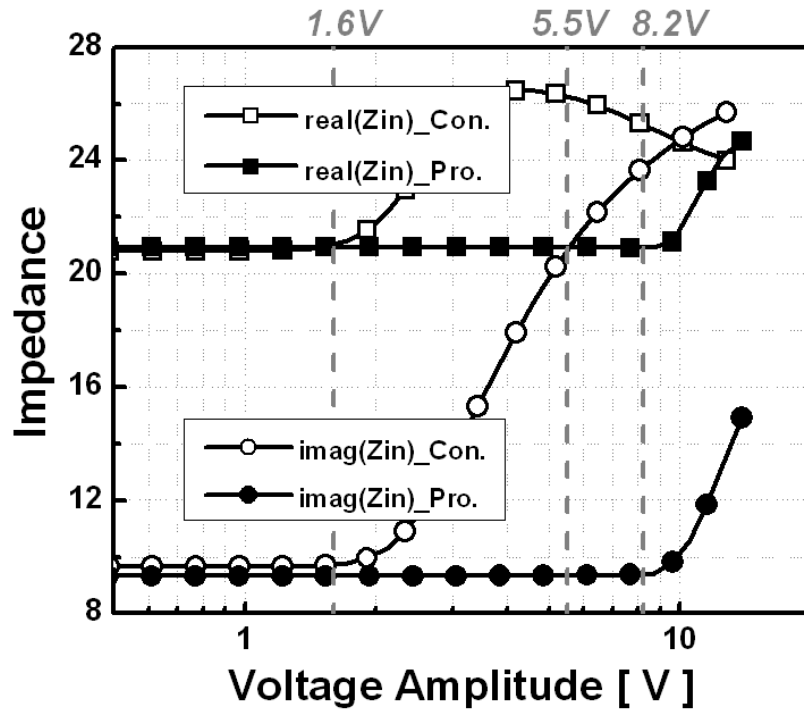


Figure 26. The matching impedance with the conventional and proposed switched capacitor in the HP mode according to the voltage amplitude across the switched capacitor.

The performance of the PA with above two tunable matching networks is simulated and compared with that of a fixed matching network with a MIM capacitor. Critical performance degradation of the conventional structure is predicted and its comparison results are presented in Figure 27, which shows power gain and power-added-efficiencies (PAE) for all three cases (the conventional structure, the proposed structure, and the MIM capacitor). Both tunable matching networks show same gain and efficiency at the small-signal region. However, the maximum output power of the conventional structure is much lower than that with the MIM capacitor, while the proposed structure maintains the same value. The efficiency presents same tendency. The gain with the conventional structure moves away from the result with the MIM capacitor at the power level of 15 dBm, which is coincident with the value shown in Figure 25.

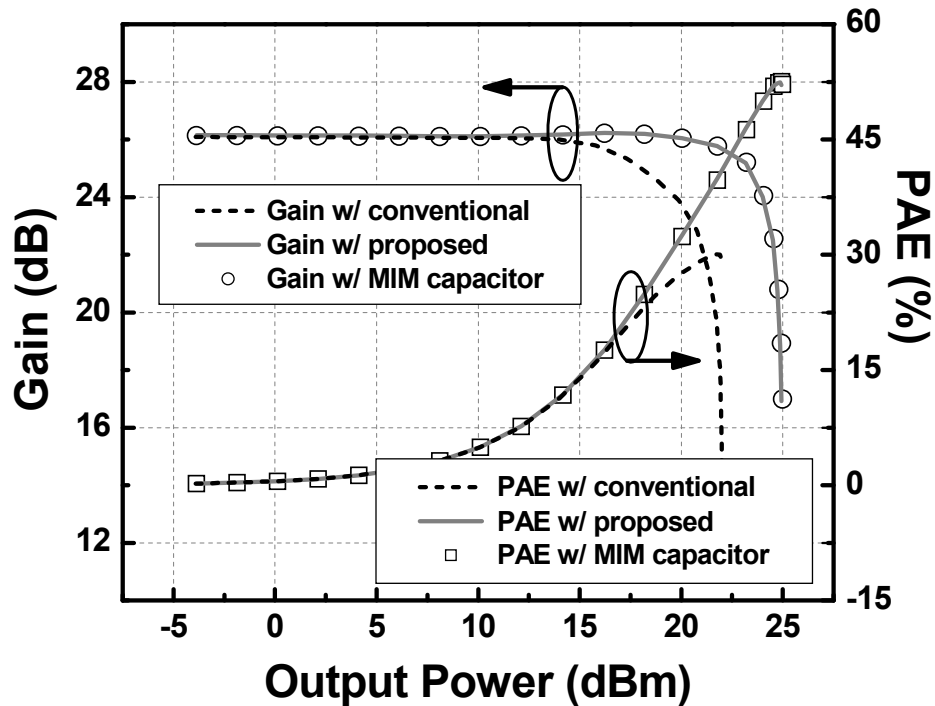
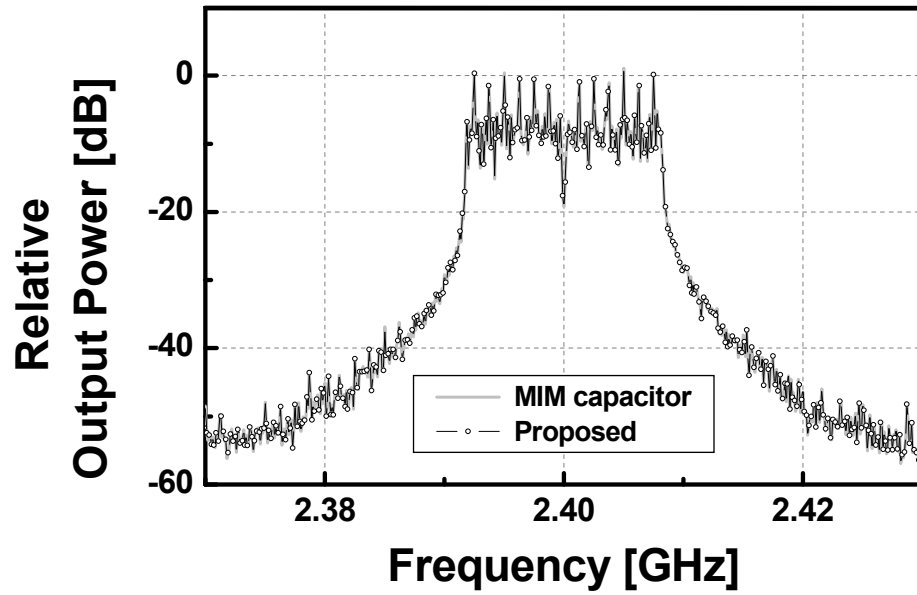
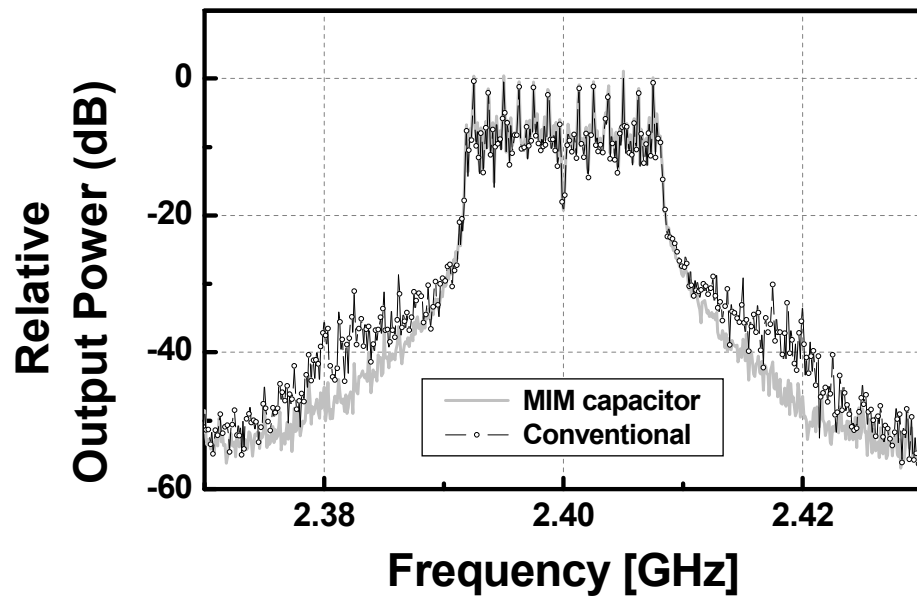


Figure 27. Simulated power gain and PAE comparison.



(a)



(b)

Figure 28. Simulated output spectrum comparison between (a) the proposed structure and MIM capacitor and (b) the conventional structure and MIM capacitor.

The well-confined spectrum mask is another major required feature of a PA. Since any non-linearity components from the tunable matching network affect to output signal, the spectrum mask might be distorted due to the tunable component. Figure 28 illustrates

the output spectrums at the power level of 16 dBm. The spectrum with the proposed structure is exactly matched with result from the MIM capacitor, while the spectrum with the conventional structure is significantly degraded. Until now, the adequate result with the proposed structure is presented with simulation results. In the following section, the effectiveness of the tunable matching network with the proposed switched capacitor is verified with measurement results.

3.4 Experimental Results

Figure 29 illustrates the die photograph of the dual-mode PA, which is fabricated in a 0.18- μm standard CMOS process. The size of the chip is $1.27 \times 0.69 \text{ mm}^2$ including all pads, and black circles in Figure 29 indicate switched capacitors, which is designed with the proposed structure. The die is attached on a printed circuit board (PCB) with 50 Ohm input/output termination, and the loss from the board is compensated.

The measured power gain and DC current of both modes with 2.4-GHz single-tone signal are shown in Figure 30, and the PAEs are illustrated in Figure 31. The saturation output power (P_{sat}) of the HP and LP mode are 23.2 dBm and 17.2 dBm. The 1-dB gain compression point ($P_{1\text{dB}}$) of the HP mode and LP mode are 22.3 dBm and 16.0 dBm, and the quiescent currents are 40 mA and 12 mA, respectively. The PAE at $P_{1\text{dB}}$ in the HP mode is 40%, and that of the LP mode is 28%. The introduced LP mode improves the efficiency significantly at the low-power region.

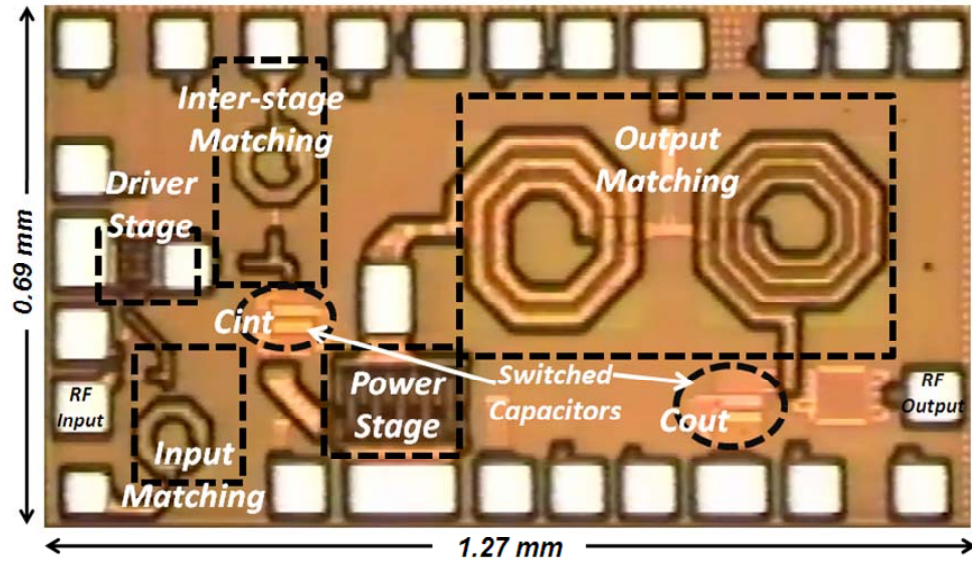


Figure 29. Die photograph of the dual-mode CMOS PA.

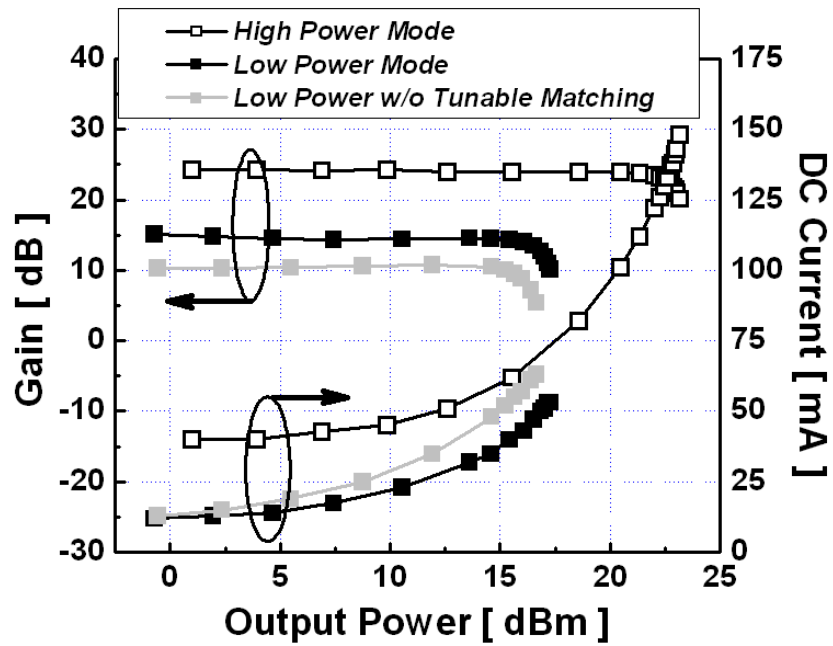


Figure 30. Measured power gain and DC current with 2.4-GHz single-tone signal.

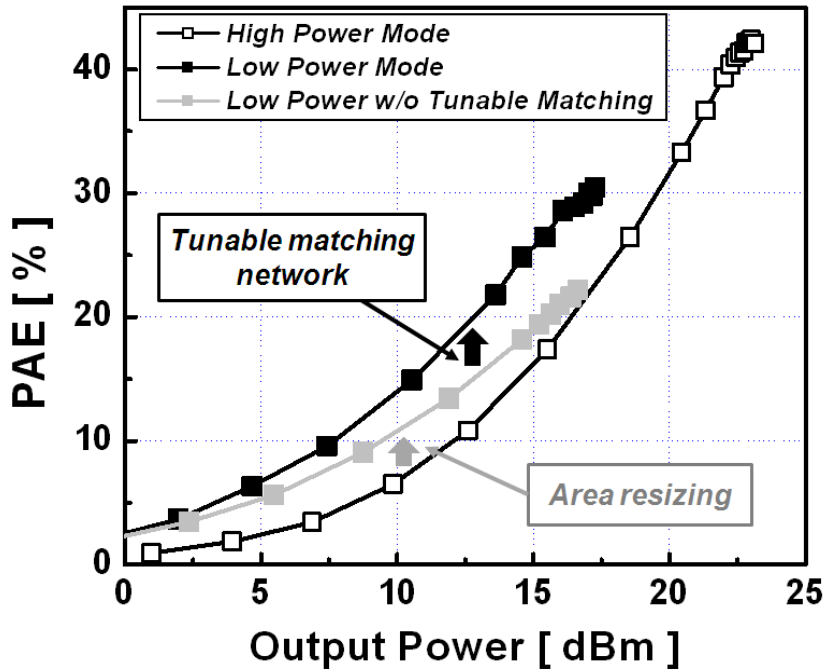


Figure 31. Measured PAEs with 2.4-GHz single-tone signal.

Both Figure 30 and 31 include the results of the LP core size with the HP mode matching (indicated as Low Power w/o Tunable Matching), which are denoted with gray lines. With this condition, the DC current at 0-dBm output power is coincident with the LP mode, while it deviates from the LP and accesses to the HP mode results as the output power increases. This is because of smaller impedance than required optimum value. With the smaller impedance, the current swing at the drain node of the PA increases quickly and approaches to the HP mode result. This tendency is also relevant to efficiency results. The efficiency measurement results presented in Figure 31 demonstrate how effectively the efficiency in the LP mode is enhanced with the assist of the tunable matching network. The gray line in Figure 31 is the efficiency improvement boundary

that is possible from the area resizing only, and further enhancement from the gray line to the LP mode is achievable by incorporating the tunable matching network.

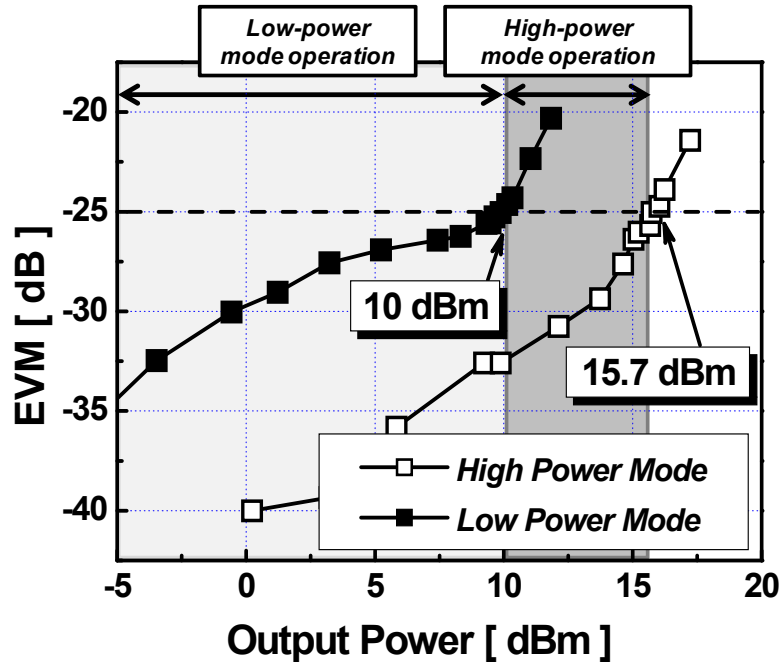
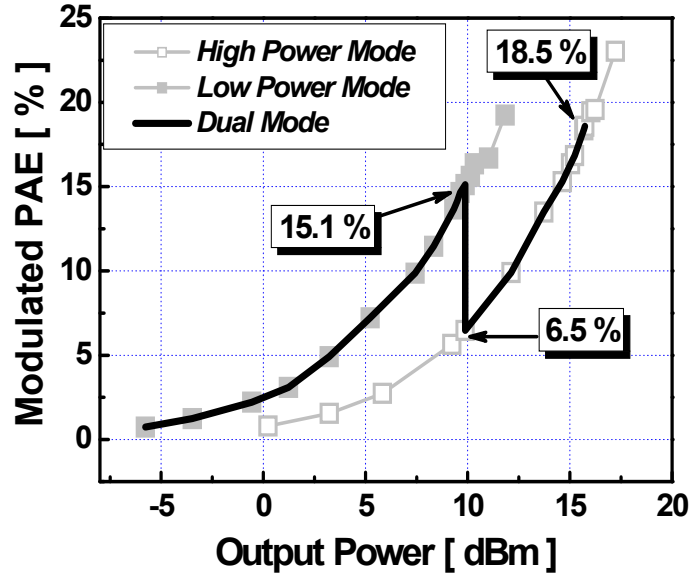


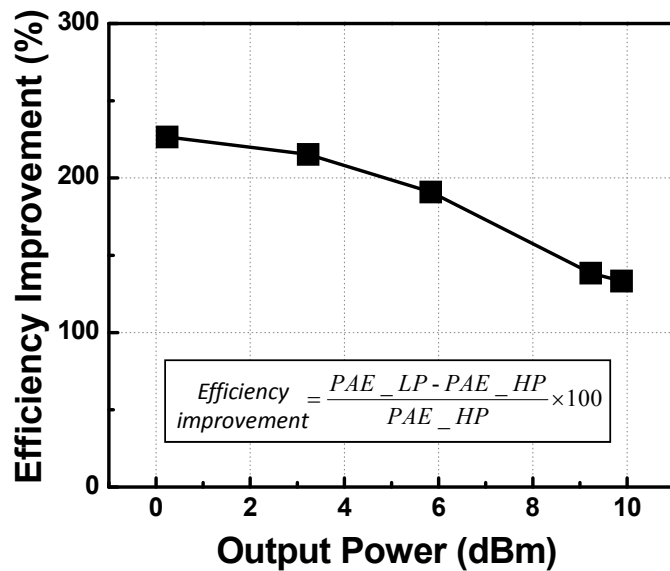
Figure 32. Measured EVMs with WLAN 802.11g 54-Mbps 64-QAM OFDM signal at 2.4-GHz.

The PA is also fully characterized with 802.11g signal to evaluate linearity and verify the effectiveness of the dual-mode PA for the wireless local area network (WLAN) application. WLAN 802.11g 54-Mbps 64-QAM OFDM signal at 2.4 GHz is applied to each mode. Figure 32 illustrates EVM measurement results with its specification (-25 dB). Maximum linear output power of the LP and HP modes are 10 dBm and 15.7 dBm, respectively. Since both power modes satisfy the linearity requirements up to the 10-dBm, it is beneficial to use the LP mode under 10-dBm output power to raise the average

efficiency. Thus, the LP mode is practical up to 10 dBm (light gray region), and the HP mode is useful from 10 to 15.7 dBm (gray region).



(a)



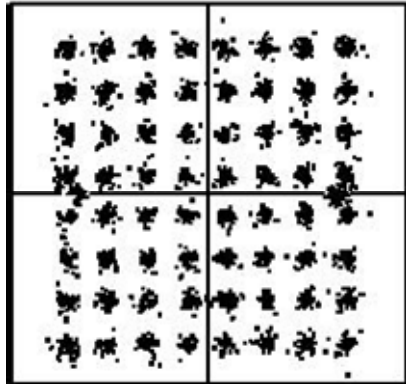
(b)

Figure 33. (a) Measured modulated PAEs with WLAN 802.11g 54-Mbps 64-QAM OFDM signal at 2.4 GHz and (b) the efficiency improvement by the low-power mode.

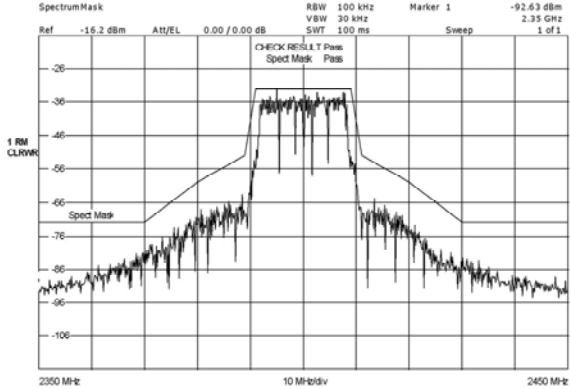
Figure 33 shows the average channel efficiency with the modulated signal and the amount of efficiency improvement. The efficiencies at the maximum linear output power of the LP and HP modes are 15.1% and 18.5%, respectively. The black solid line in Figure 33(a) represents the trajectory of the average efficiency while satisfying the linearity requirement. Figure 33(b) illustrates the amount of the efficiency improvement. More than 130 % efficiency improvement is achieved at entire power range between 0 and 10-dBm. At the transition point between the LP and HP modes, the modulated efficiency increases from 6.5 % to 15.1 % (132 % improvement).

The transmit constellation and spectral mask of the HP and LP modes are also measured. Well confined mask and EVM constellation for the HP mode at 15.7-dBm output power and the LP mode at 10-dBm output power are shown in Figure 34. At the maximum linear output power of both the LP and HP modes, the output spectrum is well confined within specification mask, which implies that the tunable matching network does not destroy linearity performance of the PA.

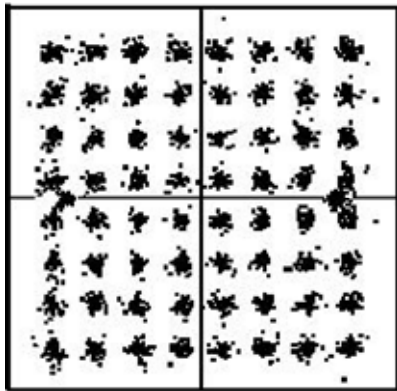
The measured performance of the dual-mode PA is compared with other recent multi-mode CMOS PAs, which is presented in Table 5. Efficiency enhancement by employing the LP mode is presented according to the back-off level. As shown in Table 5, the PA presented in this paper achieves noticeable efficiency improvement comparing to others. The efficiency enhancement by the PA in this work is approximately twice better than other multi-mode CMOS PAs. The employment of the tunable matching network produces this great improvement compare to the other multi-mode PAs. This is possible because the proposed PA can achieve the different optimum matching condition for each mode simultaneously.



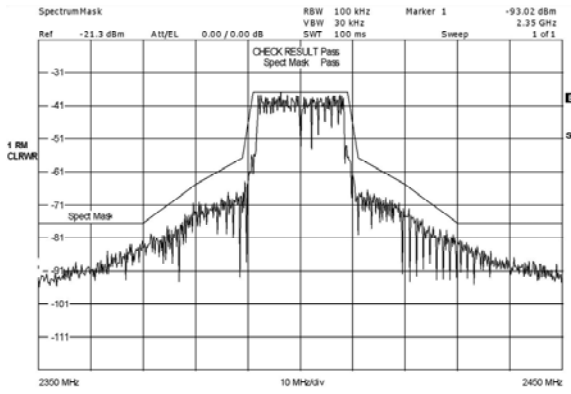
(a)



(b)



(c)



(d)

Figure 34. (a) Rectangular constellation diagram, (b) output spectrum at 15.7 dBm (-25-dB EVM) in the HP mode, (c) rectangular constellation diagram, and (d) output spectrum at 10 dBm (-25-dB EVM) in the LP mode.

Table 5. Low-power efficiency comparison with recent WLAN CMOS PA.

Reference	Frequency [GHz]	Peak Pout/PAE [dBm/%]	Supply [V]	CMOS Technology [nm]	Size [mm ²]	Number of Modes	Absolute PAE Increase @ Back-Off Power Level [%]		
							7 dB	10 dB	13 dB
[17]	2.4	31/27	3.3	180	1.98	3	4.33	4.1	4.2
[18]	2.4	27/32	1.2	130	2	2	5.4	4.0	3.4
[19]	2.4	30.1/33	3.3	90	4.32	2	N/A	4.1	3.2
[20]	2.1	30.7/35.8	3.3	180	1.98	3	5.4	4.6	6.0
[21]	2.45	23/29	1.5	130	5.48	2	3.3	4.3	3.6
This work	2.45	23.1/42	3.3	180	0.88	2	8.7	8.7	7.2

3.5 Conclusions

This chapter presents the dual-mode CMOS PA with the integrated tunable matching network in a standard CMOS process, which has enhanced low-power efficiency. For this aim, the newly introduced high-power switched capacitor is utilized. The efficiency enhancement by the PA in this work is approximately twice better than other multi-mode CMOS PAs. The application of the tunable matching network produces this great improvement compare to the recently reported multi-mode PAs. The proposed PA can achieve the required optimum matching impedances for each operation mode simultaneously. Of course, the application of the tunable matching network is not limited to the efficiency enhancement method. It could be utilized for diverse purpose such as multi-mode multi-band applications, antenna mismatch correction, wherever tunability matters with high voltage swings.

CHAPTER 4

A FULLY-INTEGRATED CONCURRENT DUAL-BAND CMOS POWER AMPLIFIER WITH SWITCHLESS MATCHING NETWORK

4.1 Introduction

Recently various wireless communication standards arouse the strong demand for a mobile device with multi-mode and multi-band feature. An RF PA is also required to support multiple standards. A conventional multi-standard PA is implemented with parallel composition of multiple PAs for each frequency of interest, as described in Figure 5. While this conventional architecture has optimized performances for each frequency band, the total cost and area are increased along with the number of supported frequencies. If one signal path in Figure 5(a) can support more than one frequency, the total cost and area of the PA can be decreased thanks to the reduced number of parallel PAs. Therefore, there have been increasing interests in a multi-band PA, of which input and output matching networks can be reconfigured according to the frequency bands, as shown in Figure 5(b) [6], [28]-[31].

Among the reported methods for multi-band PAs, composite right/left-handed transmission lines, MEMS switches, and varactors in a silicon-on-glass technology are utilized in [6], [28], [29]. Even though these methods present adequate multi-band performance, they have relatively bulky structures and require special technologies. Thus, they show drawbacks with respect to integration and cost wise. On the other hand, a

switched variable inductor and capacitor have been employed for a dual-band matching network without integration issues [30], [31]. However, it is not desirable to use the switch in an output matching network of a PA because of large signal operation and an additional loss from the switch. The voltage amplitude at the output matching network of a PA is too large for the turned-off switch to maintain its off state condition beyond certain power level [27], [30], [31]. This characteristic makes it highly challenging to use a switched-inductor or capacitor for a tunable output matching network of a PA. In addition, the switch employed in the matching network introduces inevitably an additional loss because of a decreased quality factor of passive elements including switches.

This design utilizes a parallel resonate LC structure to implement a dual-band matching network without any switches. Since the proposed structure is free from any switches, the voltage amplitude at the matching network is not a constraint. The additional power loss presented by the switched-component will be also relieved. Therefore, the aforementioned issues, which are integration, large-signal operation, and the additional loss, will be resolved with this structure.

4.2 Dual-Band Matching Structure

The proposed dual-band matching network utilizes a parallel resonant LC structure, shown in Figure 35, which is composed of two inductors and a capacitor. Both the inductors (L_1 and L_2) are realized with bond wires which will reduce the total chip area as well as power loss due to a high quality factor. The frequency response of the structure shows different inductance values according to the frequency.

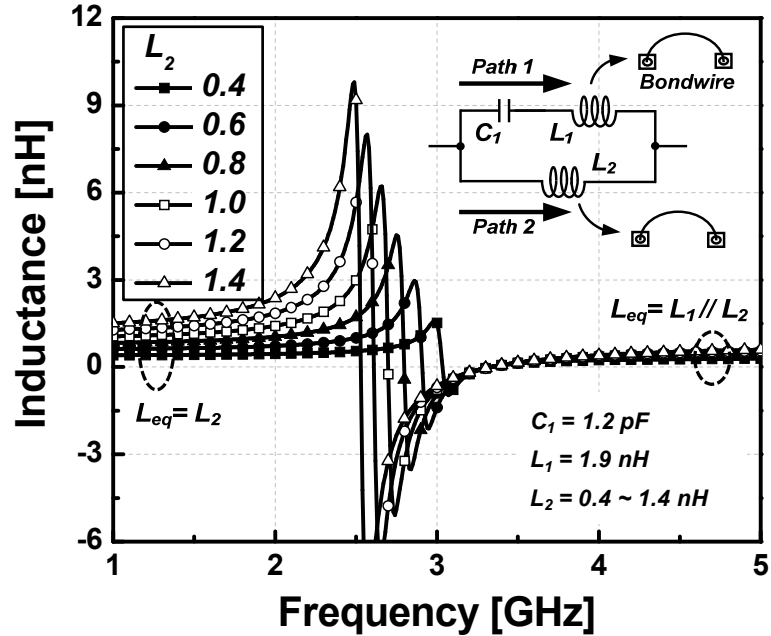


Figure 35. A resonant LC structure and its simulated inductance values according to the frequency.

The inductance of the resonant LC structure in Figure 35 can be derived according to the frequency. At low frequency, the impedance through the path 1 is dominated by a capacitor. In this case, the impedance of C_1 is much larger than that of L_2 . As a result, the equivalent inductance value (L_{eq}) at low frequency regime is the same as L_2 . Whereas, at high frequency region, the impedance of L_1 dominates the path 1, and the structure becomes a parallel combination of two inductors ($L_{eq} = L_1 // L_2$). Between these two extreme frequencies, there are parallel and series LC resonant frequencies. Figure 35 presents the simulated frequency response of the parallel LC structure according to the value of L_2 with fixed value of C_1 and L_1 , which are employed values at the output matching network of the proposed PA. As described in Figure 35, the inductance value is

dependent on the frequency as well as the combination of each component value. A dual-band CMOS PA is designed by utilizing these characteristics.

4.3 CMOS Dual-Band PA Design

Figure 36 illustrates the schematic of a 2.45/3.8 GHz dual-band CMOS PA. It is composed of three parts, which denote an input matching network, a power transistor, and an output matching network. The PA core is realized with a one-pair of differential cascode structure, which can reduce reliability issues. A thick-oxide transistor with 1.5-mm channel width is used as a CG device, while a thin-oxide transistor with 0.75-mm channel width is used as a CS device. With a supply voltage of 3.3 V, the gate bias voltage of the CS and CG device are set to 0.5 V and 2.8 V, respectively.

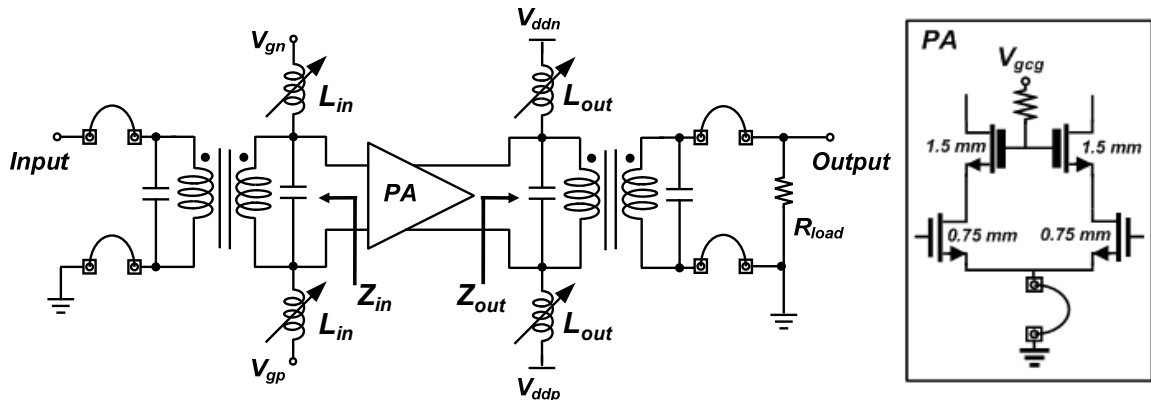


Figure 36. The schematic of the dual-band CMOS PA.

The input/output transformers are used for impedance transformation as well as a balun to change the differential signal to a single-ended signal. Since the output transformer is critical to secure output power and efficiency, it needs to be carefully designed to minimize losses at both frequencies. The transformer size is optimized by using Momentum simulation in ADS. The optimized size is $500 \times 500 \mu\text{m}^2$, with a 2:2 turning ratio. It exhibits better than 0.8-dB of insertion loss at both frequencies.

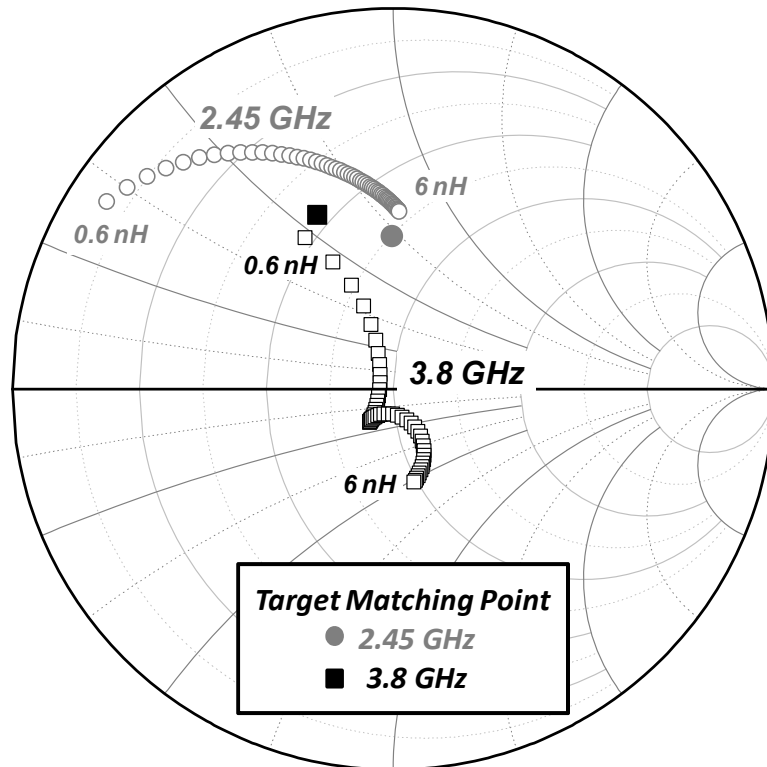


Figure 37. The simulation output matching impedance (Z_{out} in Figure 36) according to the inductance value of L_{out} .

Both input and output matching networks utilize the resonant LC structures that are placed at L_{in} and L_{out} in Figure 36 to obtain different required matching impedances (Z_{in} and Z_{out} in Figure 36) according to the operating frequency. Figure 37 shows the simulated output matching impedance, Z_{out} , with respect to inductance value (L_{out} in Figure 36). As shown in Figure 37, the optimum matching points require different inductance value of L_{out} for each frequency. That is, the required value at 2.45 GHz is about 6 nH, while that of 3.8 GHz is 0.6 nH. The resonant LC structure makes it happen to obtain these two different inductance values and accomplish two optimum matching points at each frequency at the same time.

4.4 Measurement Results

The dual-band PA is implemented with a 0.18- μm RF CMOS process. Figure 38 shows a microphotograph of the chip with size of $1.46 \times 0.7 \text{ mm}^2$ including all bonding pads. The implemented bond-wire inductors for L_1 and L_2 of both input and output matching networks are described in the Figure 38. The chip is assembled on a 2-layer FR-4 evaluation board for the measurement with 50Ω input/output terminations. The losses from the board are compensated. Figure 39 represents S-parameter measurement results. It shows well matched frequency responses at 2.45 and 3.8 GHz. As presented in Figure 39, the dual-band PA shows concurrently matched performance for the two frequency bands without any switching operations.

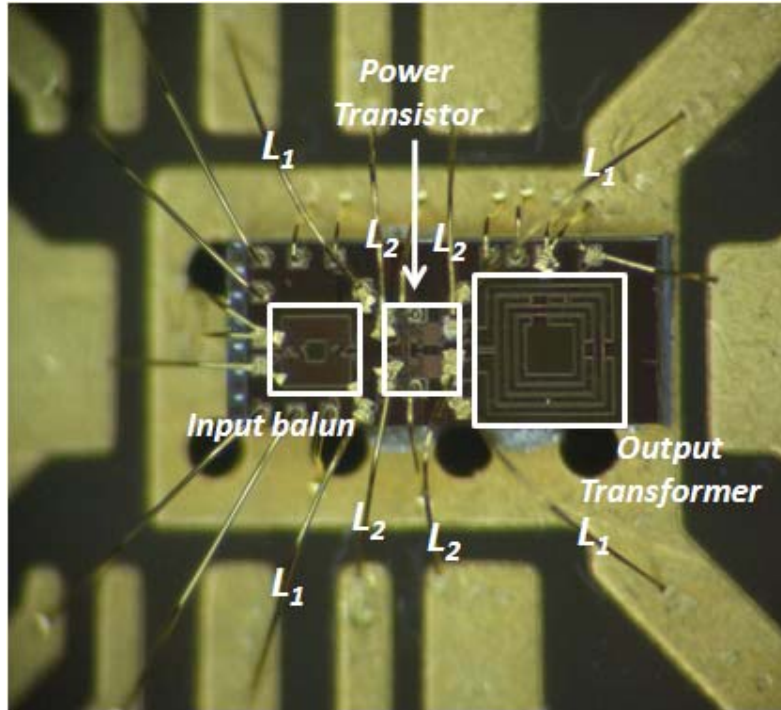


Figure 38. The microphotograph of the dual-band CMOS PA.

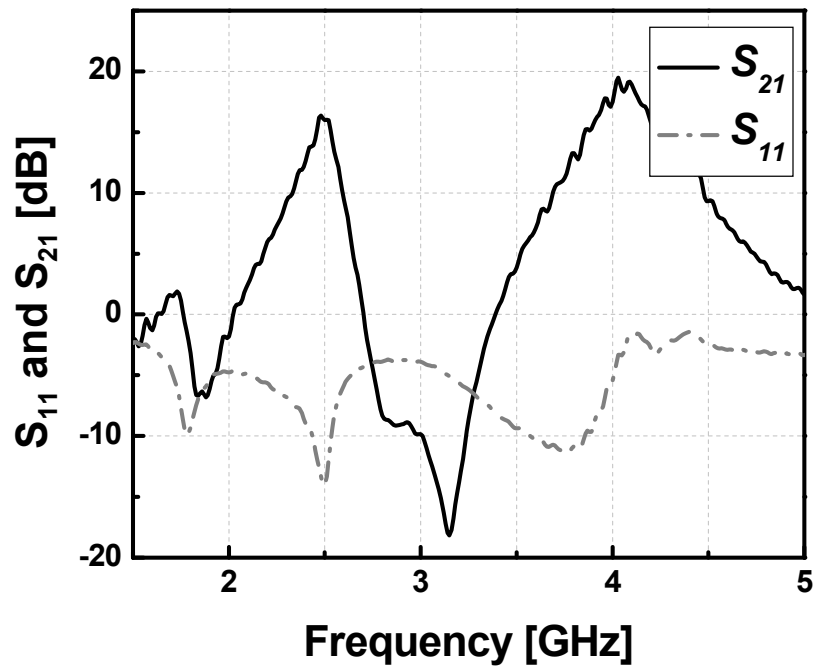
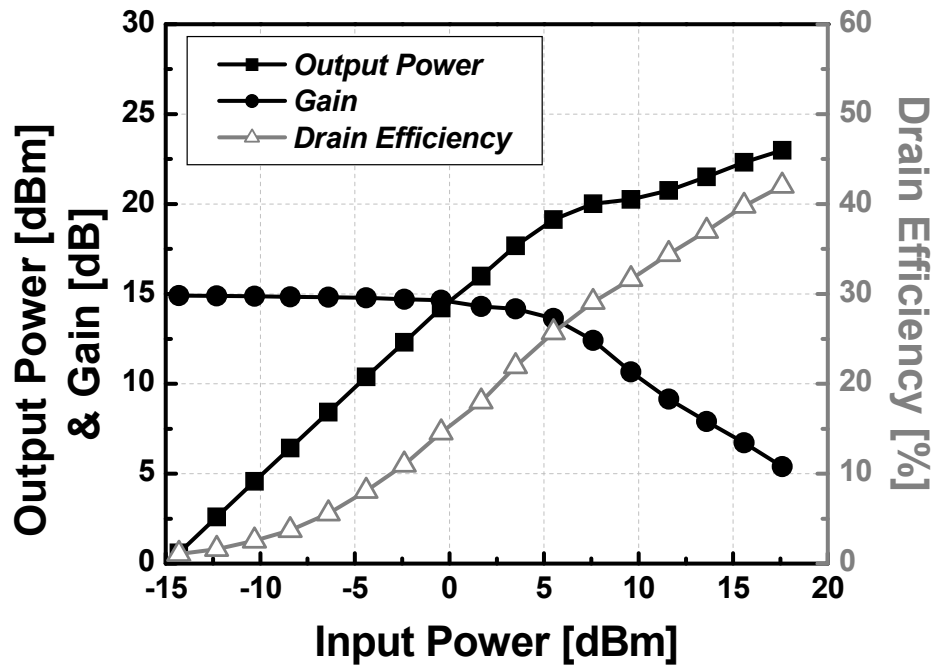
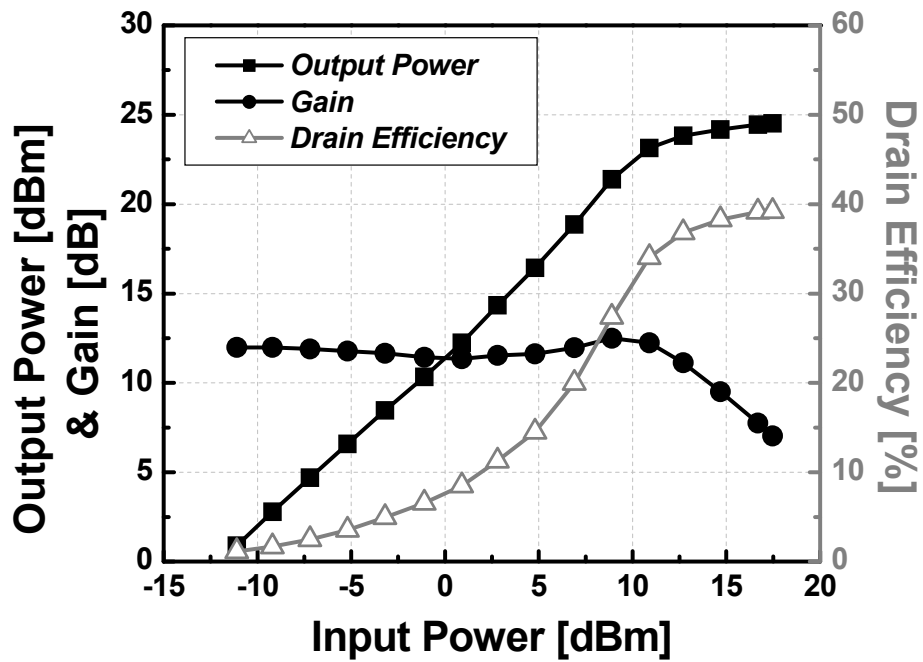


Figure 39. Measured S_{11} and S_{21} .



(a)



(b)

Figure 40. One-tone measurement results at (a) 2.45 GHz and (b) 3.8 GHz.

The measured power gain, output power, and efficiency at both frequencies according to the input power are shown in Figure 40. Since the PA has a power stage only, the efficiency performance is evaluated with drain efficiency. The linear power gain and the maximum output power are 14.8-dB and 23.4-dBm at 2.45 GHz and 12.0-dB and 24.5-dBm at 3.8 GHz, respectively. The drain efficiencies at the maximum power are 42 % at 2.45 GHz and 39 % at 3.8 GHz.

Figure 41 represents the large-signal frequency response. Both the output power and drain efficiency are maximized at designed frequencies of 2.45/3.8 GHz. These measurement results along with the single-tone power sweep results in Figure 40 demonstrate the effectiveness of the resonant LC structure as a multi-band matching component.

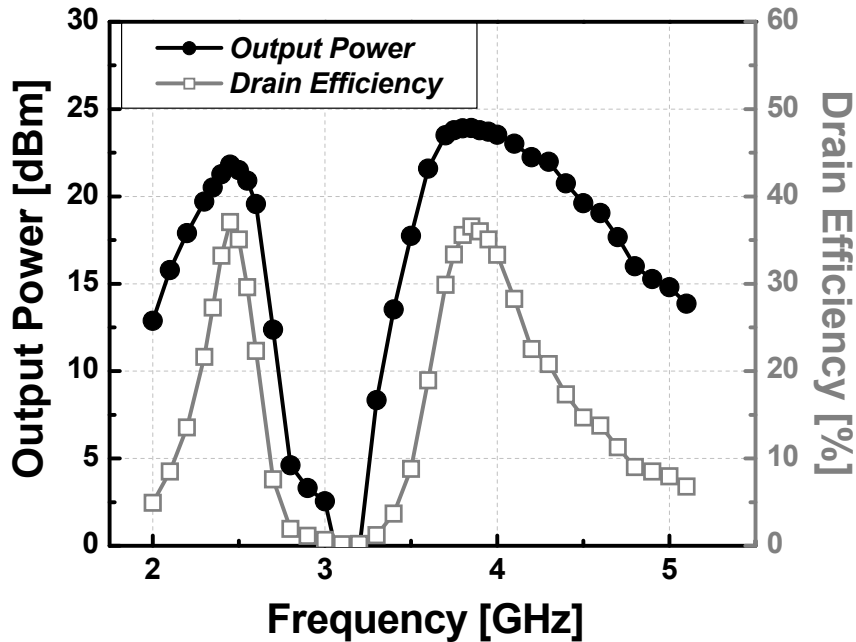


Figure 41. Measured large-signal frequency response.

4.5 Conclusions

A switchless dual-band matching structure is presented and the effectiveness of the proposed structure is demonstrated with a fully-integrated concurrent dual-band CMOS PA. The concurrent dual-band PA delivers the maximum output power and maximum efficiency at two frequencies, 2.45 and 3.8 GHz without any switching operation. The measured maximum output power and drain efficiency of the dual-band PA are 23.4 dBm and 42 % at 2.45 GHz, 24.5 dBm and 39 % at 3.8 GHz, respectively. The switchless dual-band matching structure will be a suitable component to achieve an integrated compact multi-band PA.

CHAPTER 5

AN ANTENNA MISMATCH IMMUNED CMOS POWER AMPLIFIER

5.1 Introduction

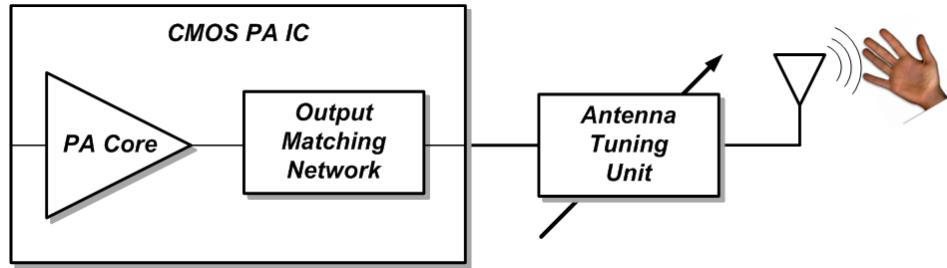
Typically, a RF PA is designed and measured under the condition of 50- Ω antenna impedance. However, the antenna impedance is easily varied by environmental changes due to a human body and/or side walls. Thus, the output matching impedance of the PA can be altered significantly in real circumstances. Moreover, the varied load impedance critically affects the performances of a PA such as output power, gain, linearity, efficiency, and reliability. Therefore, much research has been conducted to resolve the antenna mismatch problems.

The related research can be divided into two main categories, device failure and performance degradation. The former should be considered in the case of extreme mismatch conditions with a higher than 10:1 voltage standing-wave ratio (VSWR). Under such an extreme mismatch condition, the power gain is generally reduced to avoid a device breakdown [32]. On the other hand, when the VSWR is moderate compared to the former case, less than about 3:1, the performance degradation needs to be considered. In [33], four different methods of preserving the PA output power and the linearity under moderate mismatch conditions are compared, which are output power adaptation, load-line adaptation, supply voltage adaptation, and the use of an isolator. Among the compared methods, the load-line adaptation is the best solution to preserve the PA

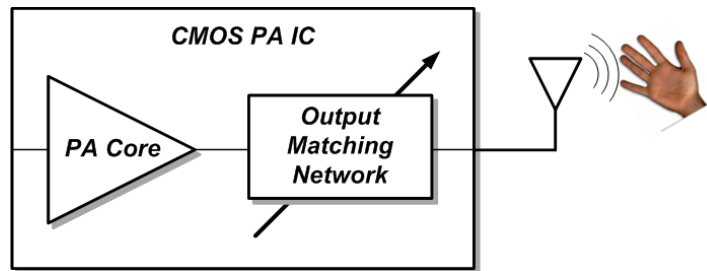
performance under a mismatch condition because it directly compensates the mismatched impedance.

There have been direct approaches to correct the load impedance when the impedance mismatch occurs. Most of the approaches place an additional component, called an antenna-tuning unit (ATU) between a PA and an antenna as described Figure 42(a) [5], [34], [35]. Even though the methods in [5], [34], [35] are useful to compensate for the antenna mismatch, they have shortcomings in terms of integration and power loss. Since the tunable matching networks in [5], [34], [35] are accomplished with special processes such as PIN diode, MEMS, and silicon-on-sapphire (SOS), those matching networks cannot be integrated with a standard CMOS process. Furthermore, the efficiency is inevitably degraded because of the power loss in the additional matching network between the PA and the antenna. Consequently, if the reconfigurable matching network can be integrated to compensate for the variation in the antenna impedance as shown in Figure 42(b), the size and power loss problem can be relived simultaneously.

In this chapter, an integrated CMOS PA with a reconfigurable matching network is proposed to maintain the output power and the linearity of the PA under antenna mismatch conditions. The implementation of the proposed tunable matching network and its impedance transformation is explained.



(a)



(b)

Figure 42. Antenna mismatch recovery methods: (a) an antenna tuning unit between a PA and an antenna and (b) a reconfigurable output matching network to compensate an antenna mismatch.

5.2 Reconfigurable Output Matching Network

When designing a reconfigurable output matching network, it is required to consider power loss and coverage of it. Power loss is one of the key characteristics of an output matching network for a PA. Since the power loss of the output matching directly affects the output power as well as the efficiency, it is necessary to minimize the power loss of the matching network. In addition, to maintain a designed PA performance under a wide

range of antenna impedances, the reconfigurable matching network should have enough matching coverage.

When the antenna mismatch is not considerable (i.e., a reflection coefficient (Γ) of the antenna is less than 0.15), the performance degradation of the PA is within an acceptable range. Thus, we set the circle of $|\Gamma|=0.3$ as the antenna mismatch impedance to be recovered by the reconfigurable matching network. The reconfigurable output matching network should be able to transform the antenna impedances with $|\Gamma|=0.3$ to the initially designed impedance point. A switched capacitor in [27] is utilized to reconfigure the matching network. Meanwhile, a tuning ratio of the switched capacitor between on/off states is set as 2.5:1 for safe operation. If the tuning ratio is larger than 2.5:1, the switched capacitor cannot sustain its off-state condition in this design.

Three LC matching networks, shown in Figure 43, are initially considered. Since a one-stage LC matching network in Figure 43(a) has a one-dimensional tunability, it is not possible to cover all angles. In the case of Figure 43(b), unless there is restriction with respect to the tuning ratio of the switched capacitor, a two-stage LC matching network can provide enough coverage. However, it cannot support all angles of $|\Gamma|=0.3$ under the limited tuning ratio. Finally, a three-stage LC matching network, shown in Figure 43(c), can support all of the angles with $|\Gamma|=0.3$ with the limited tuning ratio. If the number of stages is increased, coverage area can be expanded. However, power loss of an output matching network will also increase. Therefore, it is necessary to minimize the number of stage while satisfying a coverage requirement.

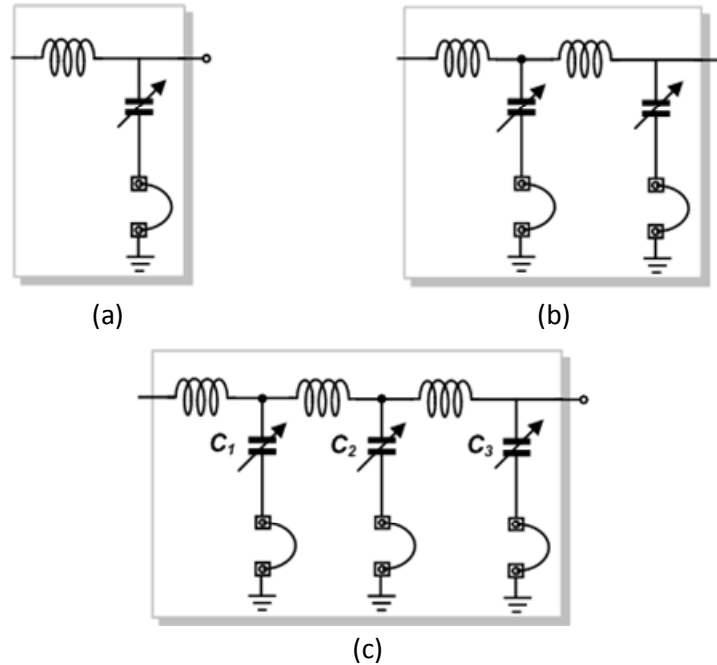
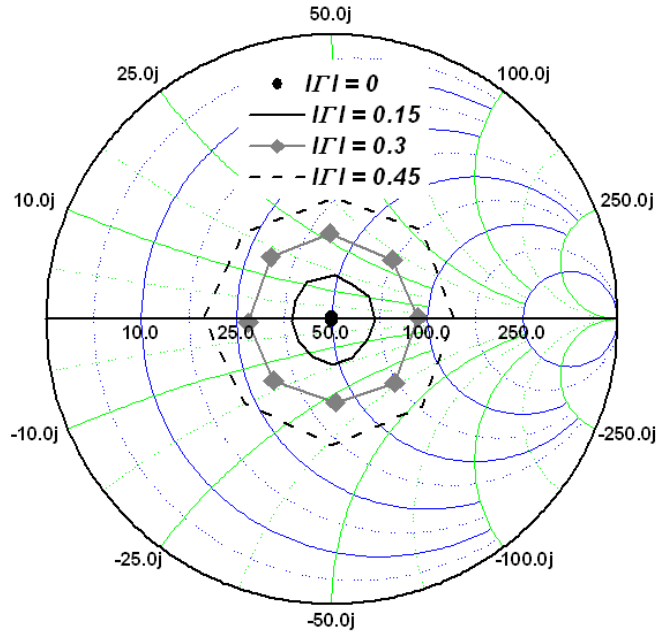


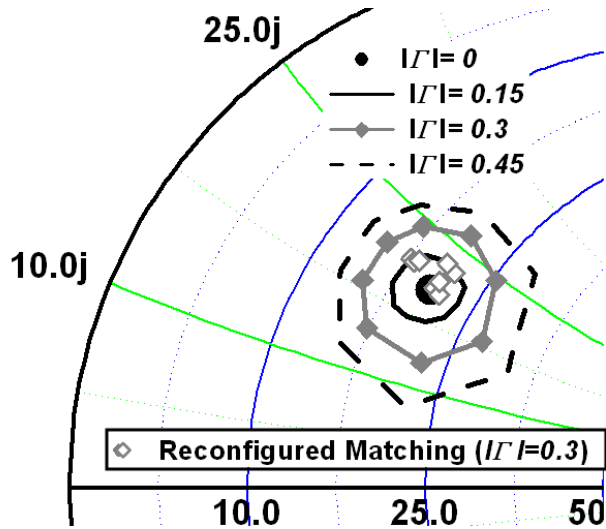
Figure 43. Reconfigurable output matching networks: (a) one-stage LC matching, (b) two-stage LC matching, and (c) three-stage LC matching.

The output matching network is implemented with ten switched capacitors. The C_1 has four tunable capacitors, and each of C_2 and C_3 consists of three capacitors. Figure 44(a) shows the realized antenna impedance according to the value of $|\Gamma|$, and Figure 44(b) represents the measured transformed matching impedances at 2.4 GHz. The impedances shown in Figure 44 are measured with a vector network analyzer (VNA), and various antenna impedances are realized by using Maury Microwave load-pull system. All the lines in Figure 44(b) represent the transformed impedances with fixed matching networks, while the open square symbols indicate the transformed impedance with the reconfigured matching network. In the case of the fixed matching network, the transformed impedances move away from the targeted impedance point, the black circle, as the antenna mismatch increases. Whereas, the reconfigured matching network make

the transformed impedances much closer to the optimum point under the antenna mismatch condition. Therefore, it is expected that the reconfigurable matching network can help the PA maintain its performance under antenna mismatch conditions.



(a)



(b)

Figure 44. (a) Measured antenna impedances with various Γ and (b) measured transformed matching impedances.

5.3 Antenna Mismatch Immuned PA Design

The schematic of the proposed reconfigurable PA is shown in Figure 45. A single-ended structure is used for this design. To avoid the possibility of oxide breakdown, a cascode structure is exploited in both the drive stage and the power stage. A thick-oxide transistor is used as a common-gate device to sustain a large voltage swing, while a thin-oxide transistor is used as a common-source device for enough gain. A tunable capacitor also utilizes a thick-oxide transistor for safe operation. A serial peripheral interface (SPI) digital block is used to control ten switched capacitors. Figure 46 illustrates the die photograph of the PA, which is fabricated in a 0.18- μm RF CMOS process. The size of the chip is 1.44 mm \times 0.75 mm including all pads. White dotted circles indicate switched capacitors.

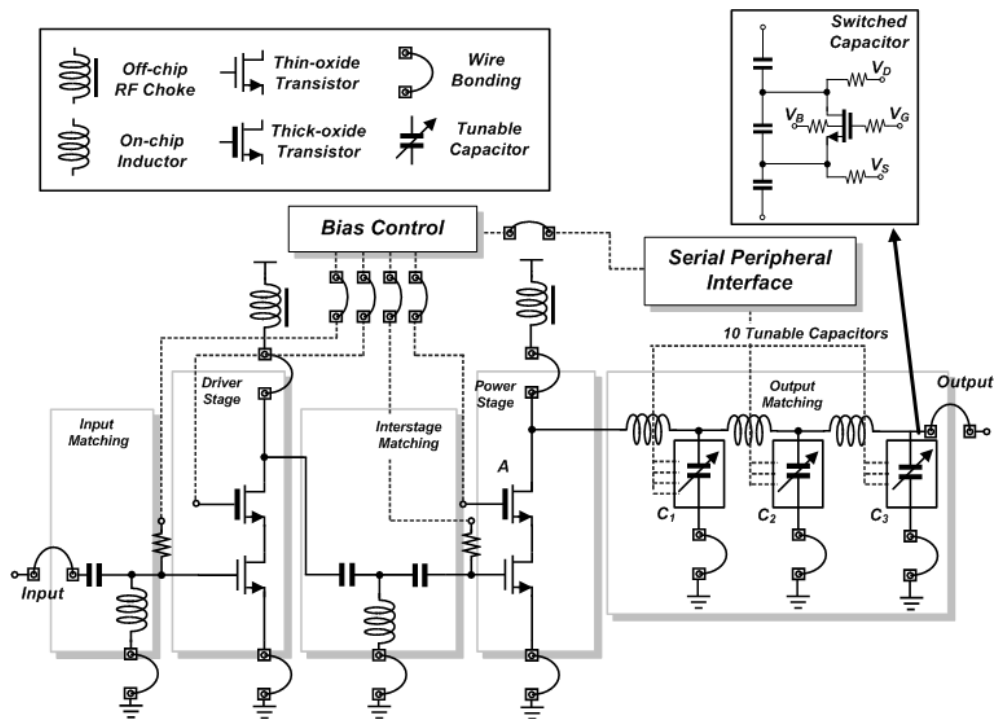


Figure 45. Schematic of the antenna mismatch immuned reconfigurable PA.

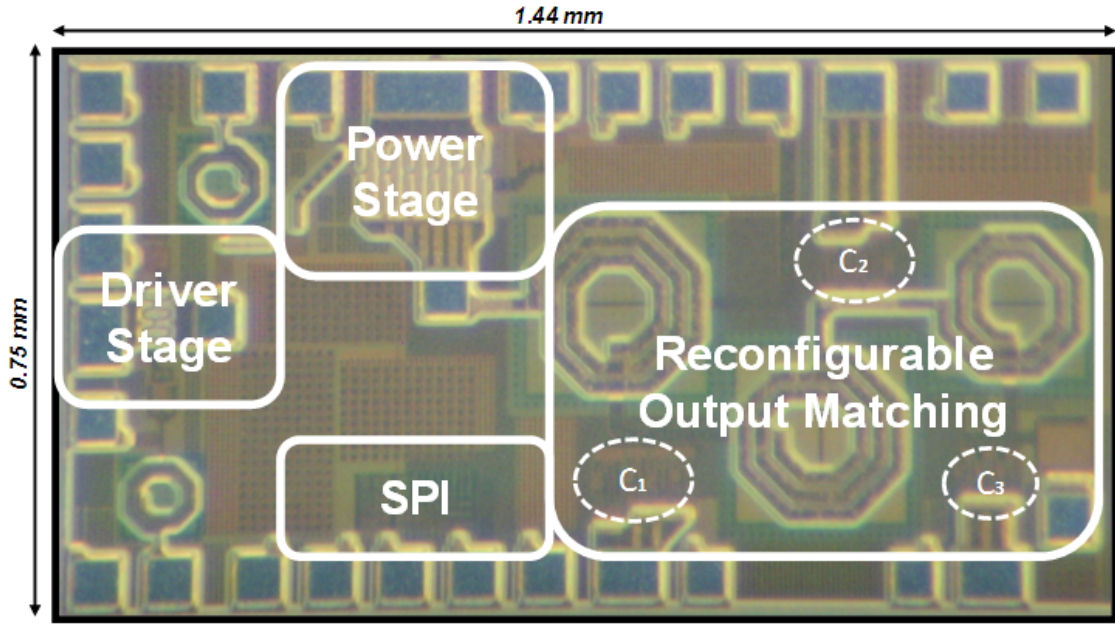
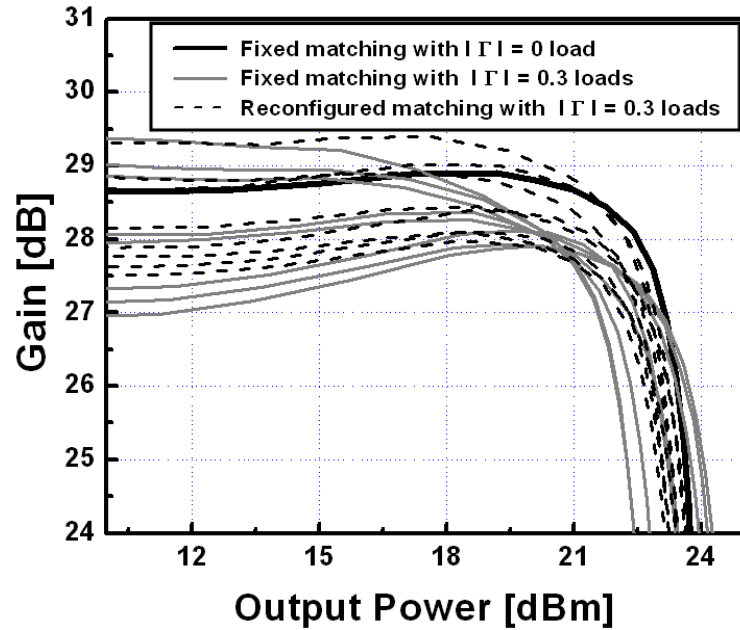


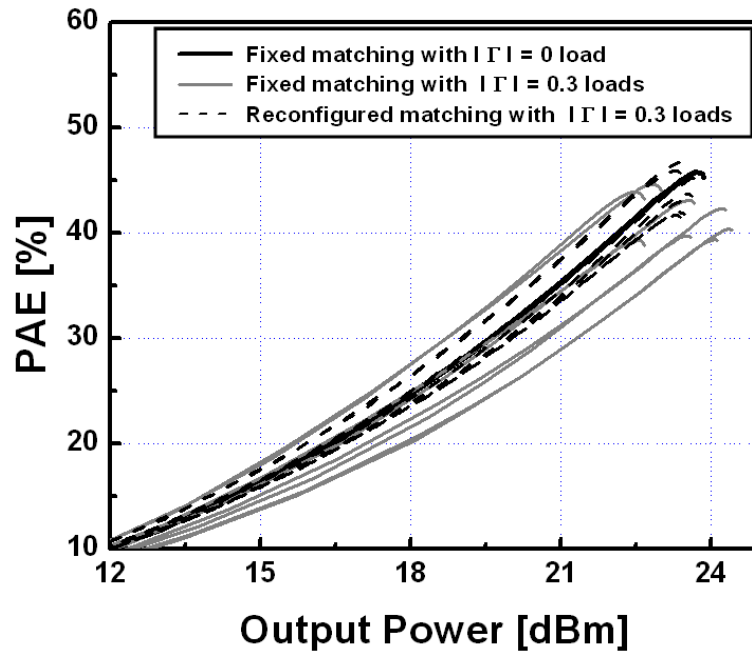
Figure 46. Die photograph of the antenna mismatch immuned reconfigurable PA.

The measured power gain and PAE with a 2.4-GHz single-tone signal are shown in Figure 47. In Figure 47, the load impedance with $|\Gamma|=0$ indicates a 50- Ω condition, and the $|\Gamma|=0.3$ load conditions indicate a constant reflection coefficient ($|\Gamma|=0.3$) circle with a 45° angle step, which denotes 0°, 45°, 90°, etc. In addition, the fixed matching condition represents the matching network that assumes the load impedance to be 50- Ω , while the reconfigurable matching network implies that the matching network is adjusted according to the load impedance. Figure 47(a) illustrates considerably distorted amplitude-amplitude modulation (AM-AM) characteristics with the fixed matching network under mismatch conditions. The distorted gain curves might degrade the EVM characteristics. Meanwhile, the distorted AM-AM features are restored by the reconfigurable matching network. Gain variation is decreased, and the flatness of the gain curve is also maintained after adapting the matching network. Figure 47(b) presents PAE measurement results.

Utilizing the reconfigurable matching network increases the PAE and reduces the PAE variation, so the efficiency curves approach to the normal 50- Ω condition.



(a)



(b)

Figure 47. Single-tone measurement results under the antenna mismatch condition at 2.4 GHz: (a) power gain and (b) PAE.

Figure 48 shows EVM measurement results. The PA was fully characterized with an 802.11g signal to evaluate the linearity and verify the effectiveness of the performance improvement by employing the reconfigurable matching network. IEEE 802.11g 54-Mbps 64-QAM OFDM signal at 2.4 GHz is used. In the case of the fixed matching network, the EVM specification is violated at much lower output power. By adjusting the output matching network, EVM violation happens at higher output power levels because the matching impedance is recovered to the initial design point by the proposed reconfigurable matching network.

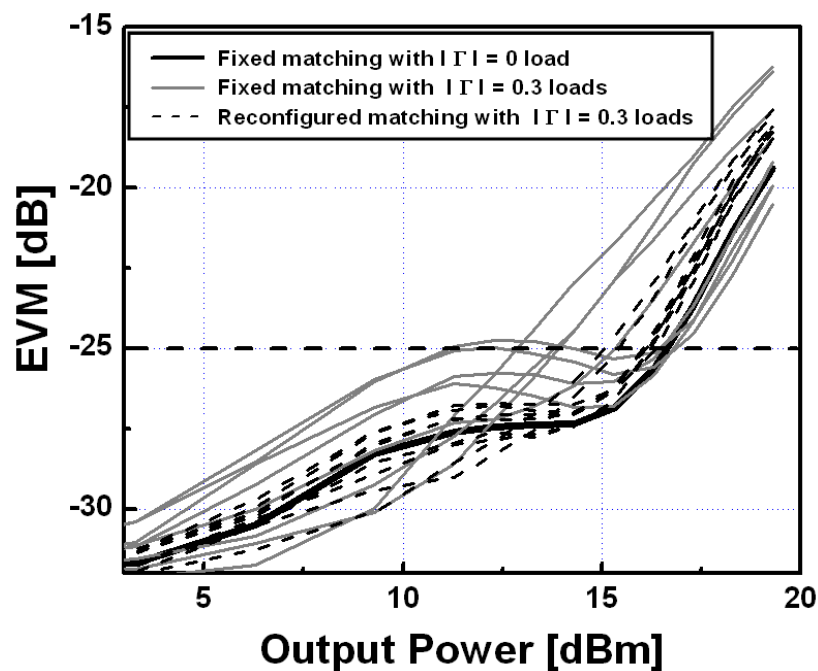


Figure 48, EVM measurement results under antenna mismatch conditions. The IEEE 802.11g 54-Mbps 64-QAM OFDM signal at 2.4 GHz is used for the EVM test.

Figure 49 shows maximum linear output power ($P_{lin,max}$) and PAE with respect to load impedance angles with $|\Gamma|=0.3$. $P_{lin,max}$ indicates a usable output power without any specification violation. At the normal operation condition with 50- Ω load impedance, $P_{lin,max}$ and PAE is 16.6-dBm and 21%, respectively. However, these values are considerably decreased under the mismatch condition of $|\Gamma|=0.3$ through all angles with the fixed matching network. Meanwhile, the reconfigurable matching network recovers both of the degraded $P_{lin,max}$ and PAE very close to the normal operation results. For example, the maximum linear power is increased from 11.1-dBm to 16.1-dBm, and PAE is improved from 8.1% to 19% at $\Gamma=0.3\angle 45$. This result implies that the proposed PA can maintain its target performance even under the antenna mismatch condition.

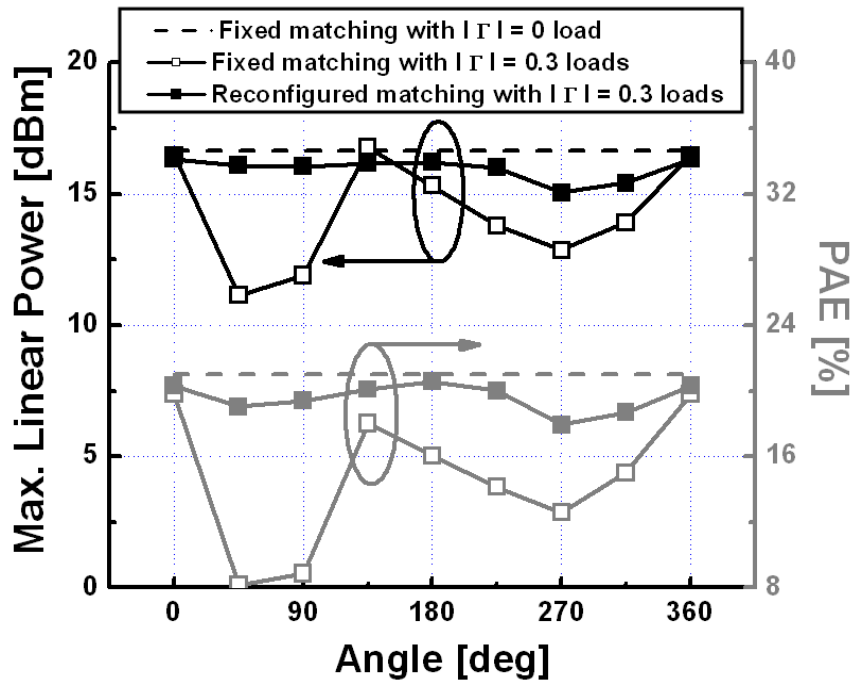


Figure 49. Maximum linear output power and PAE at the maximum linear output power level which satisfies -25-dB EVM specification.

5.4 Conclusions

In this chapter, a reconfigurable CMOS PA for improving the robustness to antenna mismatch is presented. The output matching network is implemented with a three-stage LC matching, and its impedance recovery is demonstrated with measurement. The complete PA performance is compared between a fixed and a reconfigurable matching network under the mismatch condition of $|\Gamma|=0.3$. By utilizing the reconfigurable matching network, both the maximum linear power and PAE are considerably enhanced over all angles. The maximum linear power and PAE are improved by about 5-dB and 11% at $\Gamma=0.3\angle 45^\circ$, respectively. The improvement from the reconfigurable matching network makes the proposed design very promising for achieving an integrated CMOS PA which can circumvent the antenna mismatch problem. The analog and digital circuits for detection and control are presented in the next chapter.

CHAPTER 6

A RECONFIGURABLE CMOS PA WITH AUTOMATIC ANTENNA MISMATCH DETECTION AND CONTROL CIRCUITS

6.1. Introduction

In chapter 5, the effectiveness of the integrated tunable matching network to compensate for the variation of the antenna impedance is demonstrated with measurement results. Along with a tunable matching network, a detection and control circuit to recover distorted impedance is another necessary sub-block for a complete automatic recovery system.

The requirements and types of automatic antenna tuning unit are well organized in [38]. It is meaningful to restate the requirements of the detection and control circuits. First, since environmental fluctuations for antennas occur on a time scale of milliseconds, the speed of the control loop is not a major bottleneck. Next, the demands of the detection and control circuits must be low to simplify implementations and minimize the power consumption of the control loop itself. These requirements should be considered when designing an automatic recovery circuit.

In [38], a number of automatic antenna tuners are categorized by the way adaptation is done or the way the impedance is measured: analytic computation [41], methods that

use the phase information of RF signals [34], [42], gradient methods [5], and trial-and-error method [43].

Many approaches are based on the exact antenna impedance measurement, and it is required to have information on both the amplitude and phase of a signal at the RF frequency (2.4 GHz in this design) to detect the antenna impedance [34], [37]. However, obtaining phase information of the voltage and current at RF frequencies demands relatively high performance detection circuitry. Therefore, a detection method by using only RF signal amplitude is highly desirable and one of the methods is introduced in [38]. The method presented in [38] recovers the distorted antenna impedance to $50\ \Omega$ as shown in Figure 50(a). However, the antenna tuning unit in Figure 50(a) is an additional component on the transmission path, so inevitably introduces extra loss. In addition, it increases the total cost of the transmitter.

Figure 50(b) presents a diagram of the proposed CMOS PA with an automatic antenna mismatch recovery system. As explained in Chapter 5, while most of the previous works recover the distorted antenna impedance to $50\ \Omega$, the presented method proposes a way that maintains the matched impedance looking into the output matching network under mismatch condition. This design also requires only the signal amplitude information for the recovery process, so the total recovery system can be very simple. Since the distorted antenna impedance is recovered by using the output matching network itself with only amplitude information, it will be a very effective method in terms of signal power loss, total chip cost, and complexity.

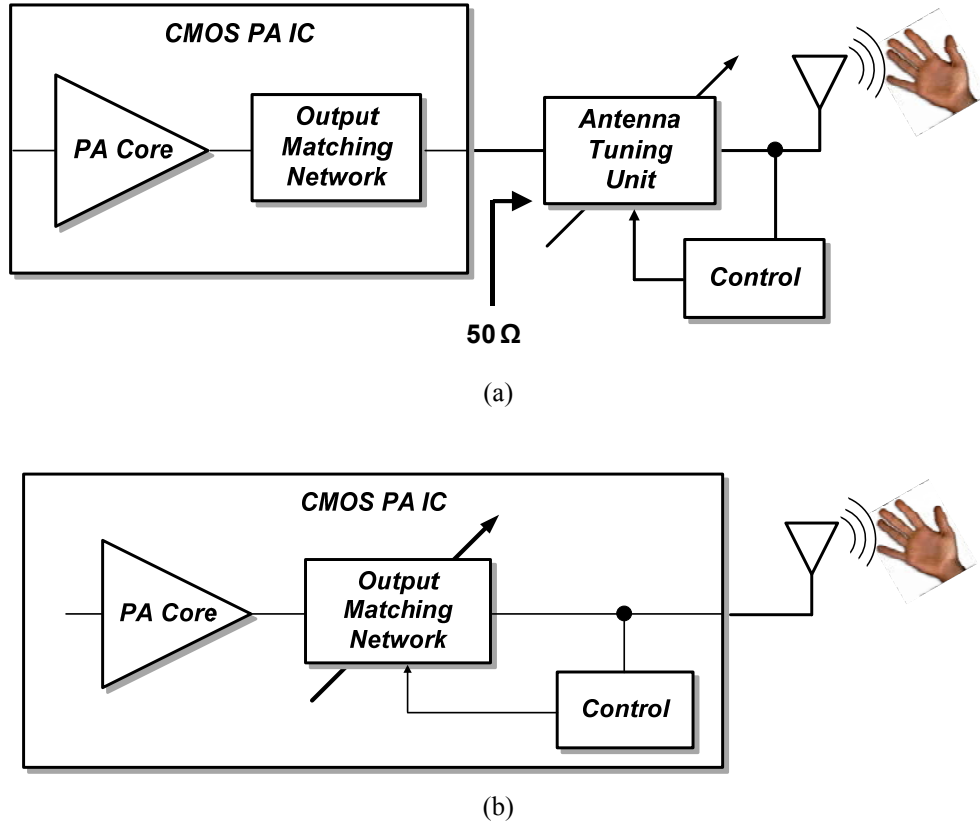


Figure 50. Antenna mismatch recovery system: (a) an antenna tuning unit between a PA and an antenna and (b) an output matching network to compensate an antenna mismatch.

6.2. New Impedance Detection Method

In this section, the newly proposed impedance detection procedure is presented. Figure 51 illustrates the output matching network for this design, which is a three-stage LC matching network. The PA core described in Figure 51 includes an input matching network, a driver stage, an inter-stage matching network, and a power stage. The three-stage LC output matching network itself is used to recover the mismatched antenna impedance. The results shown in Figure 51 are obtained by using an S-parameter

simulation in ADS. This result shows how much the matching impedance is deviated from the targeted point due to antenna mismatch. As shown in Chapter 5, if the matching impedance at node A moves away from the initial design point, the PA performance such as output power, efficiency, and linearity is degraded. Therefore, the purpose of this work is to maintain the matched impedance at node A and B constantly regardless of mismatched antenna impedance. The impedance modification will be obtained by changing the value of a switched capacitor bank.

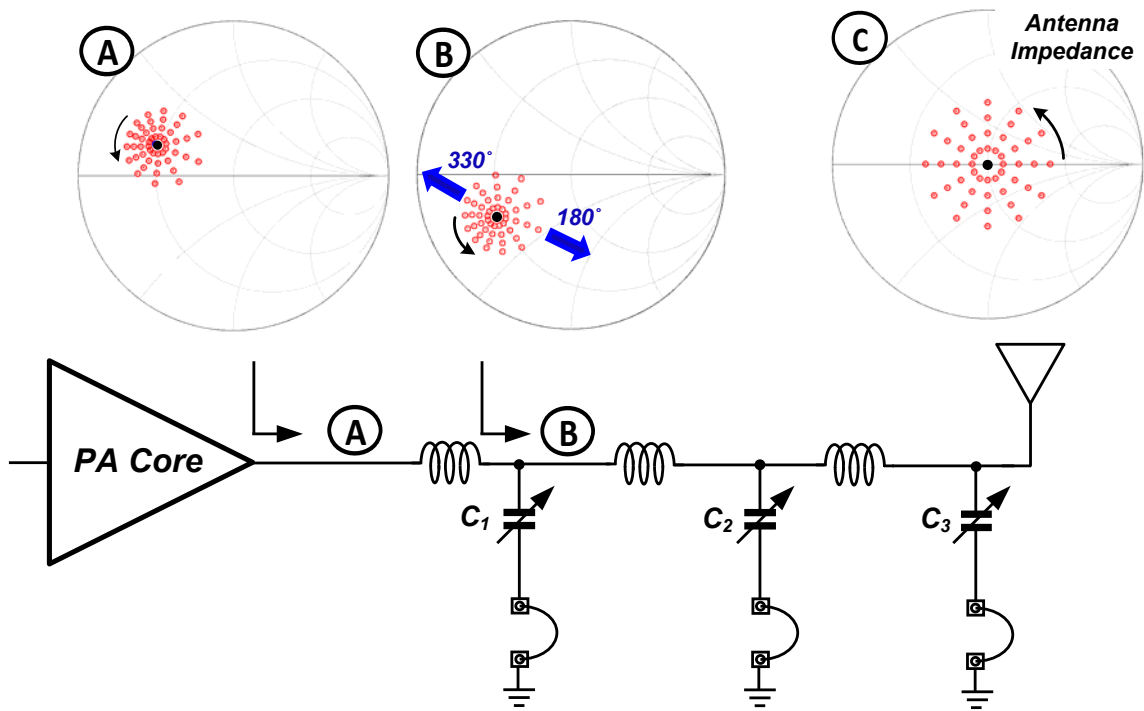


Figure 51. Three-stage LC output matching network. Impedance distortion at node “A” and “B” due to mismatched antenna impedance.

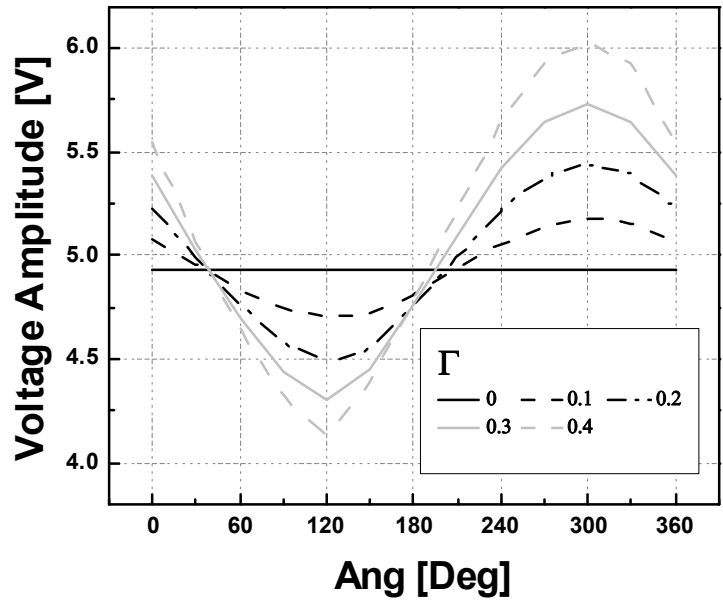
In Figure 51, red open circles on the rightmost Smith chart C present probable distorted antenna impedance, and the solid black dot on the center indicates the well-matched 50Ω impedance. The magnitude of the reflection coefficient (Γ) of distorted impedance has a 0.1 step (i.e., 0.1, 0.2, 0.3, and 0.4 from center to edge), and the angle has a 30° step (i.e., 0° , 30° , 60° etc.). The Smith charts A and B show matched impedances looking into the output port from the corresponding node (A and B) according to the antenna impedance when the capacitance values of C_1 , C_2 , and C_3 are set for the 50Ω condition. Black dots on the Smith chart A and B also indicate the results of well-matched 50Ω condition. As shown in Figure 51, when the amount of mismatch increases, the transformed load impedance at the drain node moves away from the target impedance point. Accordingly, the performance degradation will be getting worse.

As explained previously, a typical method to overcome this is to detect the mismatched impedance and update the matching network according to the detection results. However, direct detection of the antenna impedance at RF frequencies requires quite complex circuitry, and the relation between the switched capacitor combination and the distorted antenna impedance should be given in advance. Thus, an additional look-up table is necessary for this approach. Even though the method is simple and straight forward, the complexity of the implementation makes this approach less attractive. Therefore, if the distorted condition can be restored without any direct impedance measurement and look-up tables, that is much more desirable.

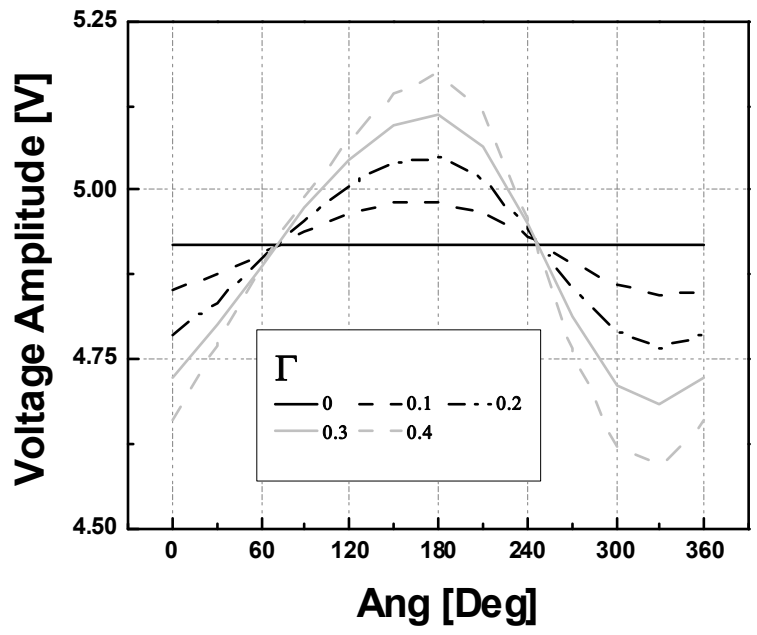
Since the proposed recovery system will be integrated with the PA itself, the inside information from the PA can be utilized. As pointing out from Figure 51, the matched impedances at nodes A and B move farther from the targeting impedance when the

amount of mismatch increases. If we look more closely, it is possible to discover useful information from the matching network. The magnitude of impedance increases along a certain direction, while it decreases toward the opposite direction. For example, in the Smith chart B, the magnitude of the impedance along the direction of 180° from the black dot becomes larger than that of the black dot because both real and imaginary values increase. On the other hand, the magnitude decreases along the 330° direction. Meanwhile, if a certain signal power level is applied to the input of the PA, the voltage amplitude at node B is proportional to the magnitude of impedance looking into the output port. Therefore, the voltage amplitude at node B under the condition of the same input power can tell whether it has been restored to its original targeting point or not. By the way, the impedance magnitude at a particular angle between 180° and 330° becomes comparable with that of the black dot point. Thus, the voltage amplitude information at a single point (A or B) cannot guarantee complete recovery to the original matching impedance. Consequently, voltage amplitudes at both nodes A and B are to be a criterion to decide whether the load impedance is recovered or not under mismatch conditions.

Figure 52 shows the simulated voltage amplitude at nodes A and B with -7 dBm input power and $50\ \Omega$ matching network. The $|\Gamma|$ of the antenna impedance is varied from 0 to 0.4, and the angle of Γ is changed from 0° to 360° with a step of 45° . The voltage amplitude at each point is obtained by using a harmonic balance (HB) simulation in ADS. As explained previously, the voltage amplitudes at both nodes become larger at a certain angle, and smaller at an opposite angle than that of the well-matched condition ($\Gamma=0$). The deviation from the matched value also increases as the reflection coefficient becomes large because the impedance difference between two points enlarges.



(a)



(b)

Figure 52. Simulated voltage amplitudes at node (a) A and (b) B in Figure 51 according to the reflection coefficient.

As expected in Figure 51, the voltage amplitude under the mismatch condition becomes the same with that of the well-matched condition at a particular angle (e.g., around 60° and 240° in Figure 52(b)). Therefore, only one node voltage cannot assure a return to the optimum matching point, and information from both nodes A and B is necessary to make a decision. Consequently, if we have the information of the voltage amplitude at nodes A and B under the $50\ \Omega$ condition with a certain input power level, the mismatched antenna impedance can be recovered by finding capacitor bank code that makes the voltage amplitudes at nodes A and B the same as the known matched values.

In other words, the proposed method does not require any information of the directly measured antenna impedance. Rather, we keep changing the matching network until the voltage amplitudes at nodes A and B are close enough simultaneously to the original designed values, which allow to find the capacitor bank combinations for mismatch recovery with only the signal amplitude information.

Figure 53 summarizes the automatic antenna mismatch recovery flow. First, if a mismatch occurs, the control loop is enabled, and the counter starts. The counter sets all of the capacitor bank bits as one, and peak detectors detect the voltage amplitude at nodes A and B. Next, check whether the detected voltages exist within a specified voltage range or not. If both values satisfy the condition (i.e., both detected voltage amplitudes are close enough to values under the $50\ \Omega$ matched condition), stop the counter and maintain the corresponding capacitor bank code, or keep decreasing the capacitor bank code by the counter. Keep the described iteration until the counter approaches the final state. If there is no successful capacitor combination until the last counter state, it means the current mismatch condition cannot be recovered with the corresponding tolerance. Therefore, the

voltage range needs to be increased to relax the recovery requirement. An increase of the voltage range can lead to finding a solution, and the capacitor bank combination can be acquired.

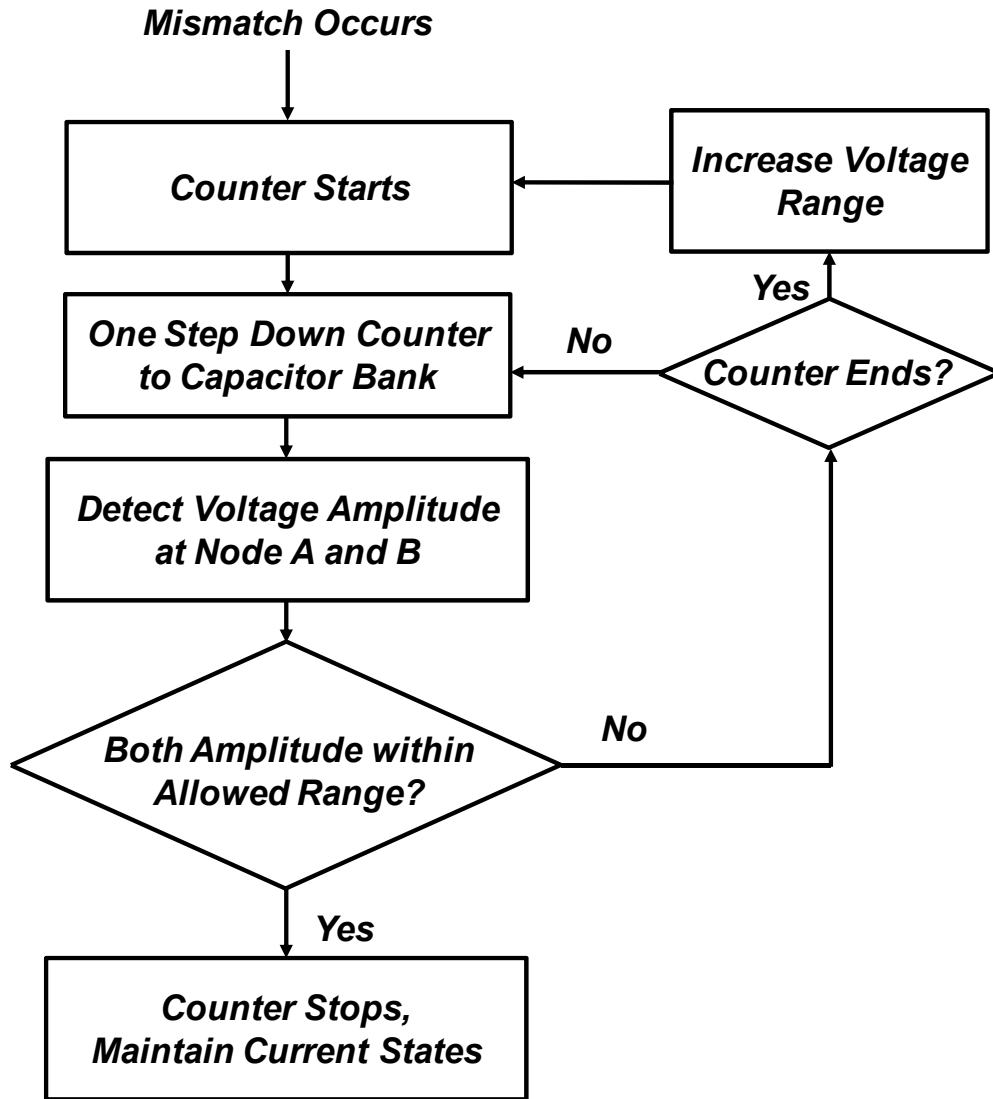


Figure 53. Automatic antenna mismatch recovery flow.

6.3. Design of Detection and Control Circuits

The schematic of the proposed PA is shown in Figure 54. In the PA core side, to avoid the possibility of oxide breakdown, a cascode structure is exploited in both the drive stage and the power stage. A thick-oxide transistor is used as a common-gate device to sustain a large voltage swing, while a thin-oxide transistor is used as a common-source device for sufficient gain. After initial schematic design, the PA has been more optimized with layout information. RC parasitic extraction was performed for power transistors by using Calibre XRC, and EM simulation software (ADS Momentum) is also utilized to consider metal line connections.

Seven switched capacitors are used to tune the output matching network, and the high-power and highly linear switched capacitor structure presented in [27] is employed. By modifying the value of the seven bit capacitor bank, the distorted impedance is able to be recovered to the desired matching point up to $\Gamma=0.3$. Beyond the $\Gamma=0.3$ VSWR circle, the tunable output matching network can recover the distorted impedance with an increased error. All switched capacitors are designed with thick-oxide transistor switches, and the tuning ratio for each switched capacitor between *ON* and *OFF* states is set to 2.5 to ensure safe large signal operation. The switched capacitor can maintain its off-state condition up to more than 20 V_{p-p} (peak-to-peak) voltage swing across it, which is sufficiently large for this design.

In the following sections, more detailed designs of sub-blocks such as a peak detector, a comparator, a switched capacitor, and a counter are presented.

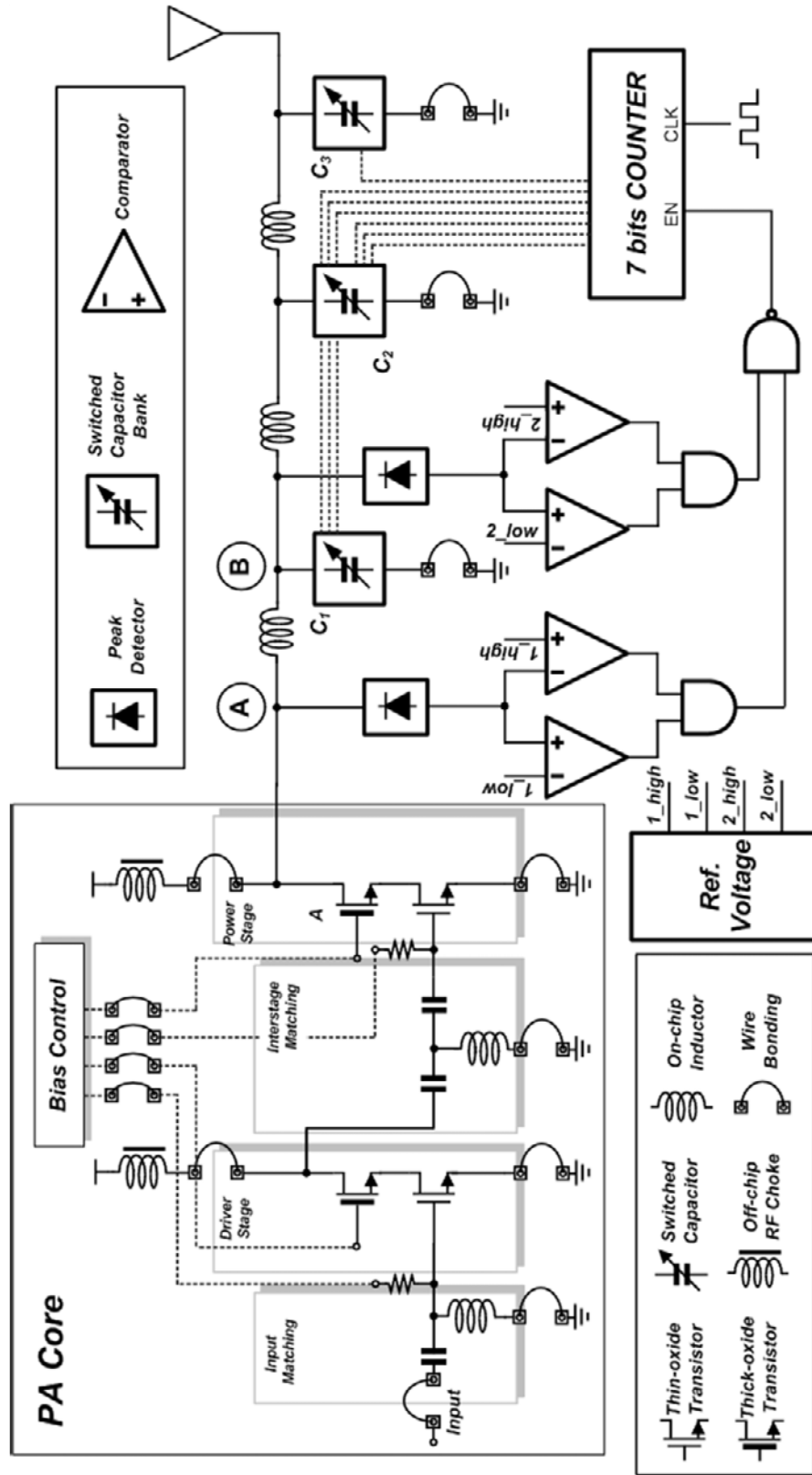


Figure 54. The schematic of the CMOS RF PA with automatic antenna mismatch recovery.

6.3.1. Peak Detector

The voltage amplitudes at nodes A and B are detected by using a peak detector, of which the output signal is proportional to the peak amplitude of its input voltage [40], [44]. Figure 55 shows the schematic of the peak detector. V_{in} is connected to the detecting nodes (i.e., nodes A and B), and V_{out} is connected to a comparator. Diode connected transistor M_1 is used to bias the transistor M_2 . The RC network consisting of R_1 , R_2 , C_1 , and C_2 plays two roles here: providing sufficiently large input impedance and voltage dividing according to their impedance ratio including the transistor M_2 . The parallel $R_{det}C_{det}$ network should present a low-enough cutoff frequency to generate a DC like output signal. The transmission gate with M_3 and M_4 is used to disconnect the power line when the detection process is not activated.

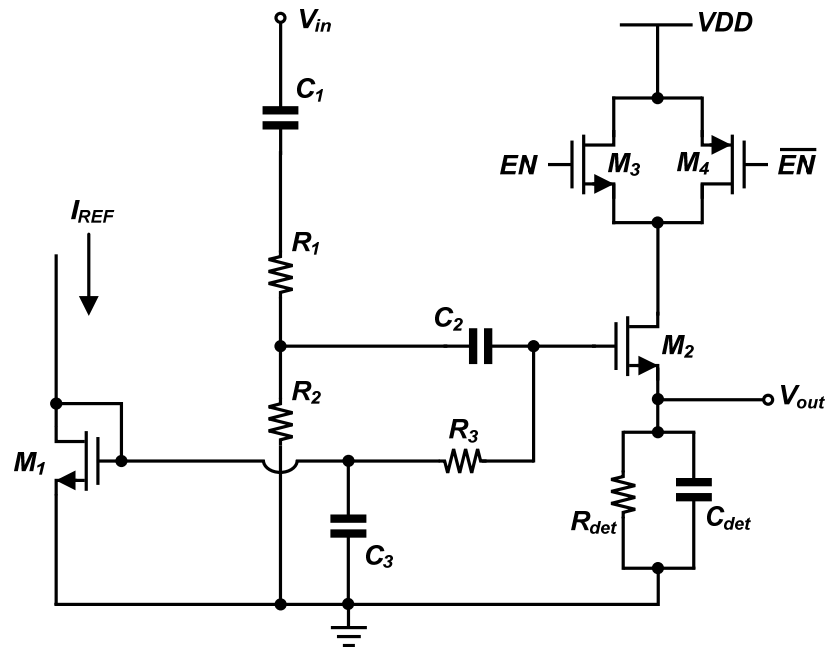


Figure 55. Schematic of the peak detector.

The requirements of the peak detector can be summarized as follows:

- Large enough input impedance to avoid performance degradation of the PA by connecting it to an output matching network
- Linear relationship between the amplitudes of V_{in} and V_{out}
- Fast enough transient response to reduce the total recovery time.

The minimum value of input impedance is determined through simulation, which shows that at least 2 k Ω input impedance is required to avoid unwanted effects by connecting a peak detection circuit to the output matching network. If this value is too low, that can introduce a reduced output power as well as reduced efficiency. Therefore, in this design, the peak detector has more than 3 k Ω input impedance.

To guarantee a linear relationship between V_{in} and V_{out} , it is important to define the range of V_{in} . Every possible combination of the switched capacitor bank is considered under maximum distorted conditions (e.g., 3:1 VSWR) to find the range of V_{in} . The simulation shows that voltage amplitudes at node A and B exist between 0.5 and 5. Figure 56 presents the simulated output voltage of the peak detector according to the amplitude of V_{in} . It can be confirmed that the linear relation between V_{in} and V_{out} is well defined over the entire range.

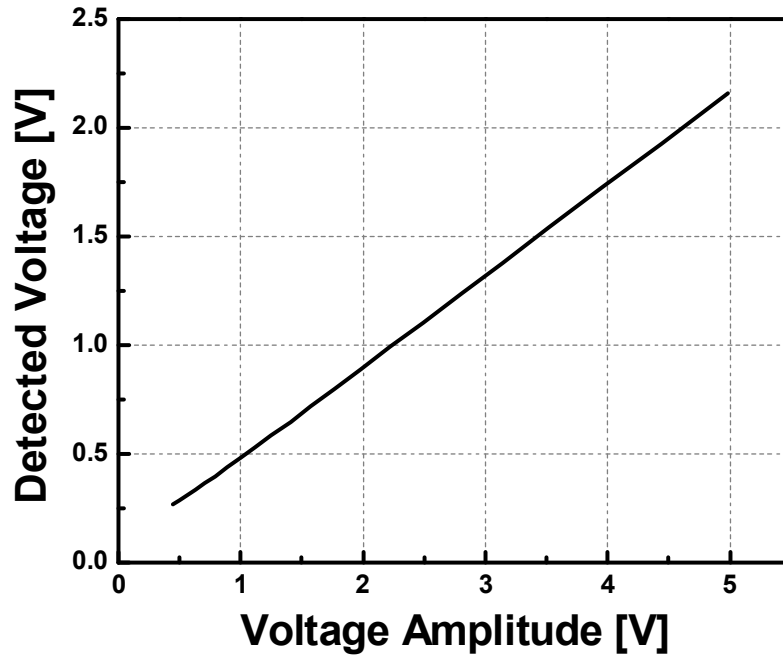


Figure 56. Simulated detected voltage of the peak detector.

Next, it is also necessary to define how long the circuit takes to detect the amplitude. Since every recovery step requires a large number of detection processes, it is beneficial to minimize the required time for a fast recovery procedure. However, there is a trade-off between the required response time and precision. The response time is proportional to the size of C_{det} , while the size of the ripple at the output signal is inversely proportional to C_{det} . Therefore, if C_{det} is reduced for fast detection, the ripple size of the detected signal increases and has a detrimental impact on the accuracy of detection. Therefore, the size of C_{det} should be carefully decided. Meanwhile, there is another approach to reduce the response time with same value of C_{det} . If the size of the transistor M_2 is increased, the speed of charging at V_{out} node can be increased, and it helps to reduce the response time.

However, the larger size of M_2 induces a smaller voltage swing at the gate of M_2 . Consequently, the ratio between the detected voltage (V_{out}) and the amplitude of V_{in} is decreased, and this approach is not helpful to improve the overall characteristics of a peak detector.

For this design, we set as a guideline that the magnitude of the ripple should be less than 2 mV and the response time is to be less than 0.5 μs . The simulation results are presented in Figures 57 and 58, and show that the results satisfy the aforementioned design target.

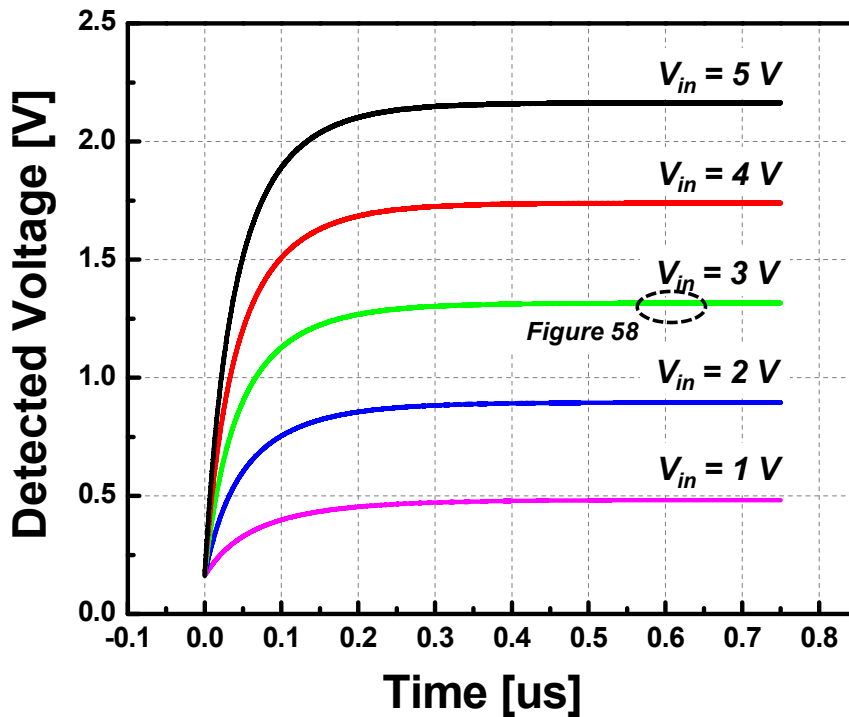


Figure 57. Transient response of the peak detector.

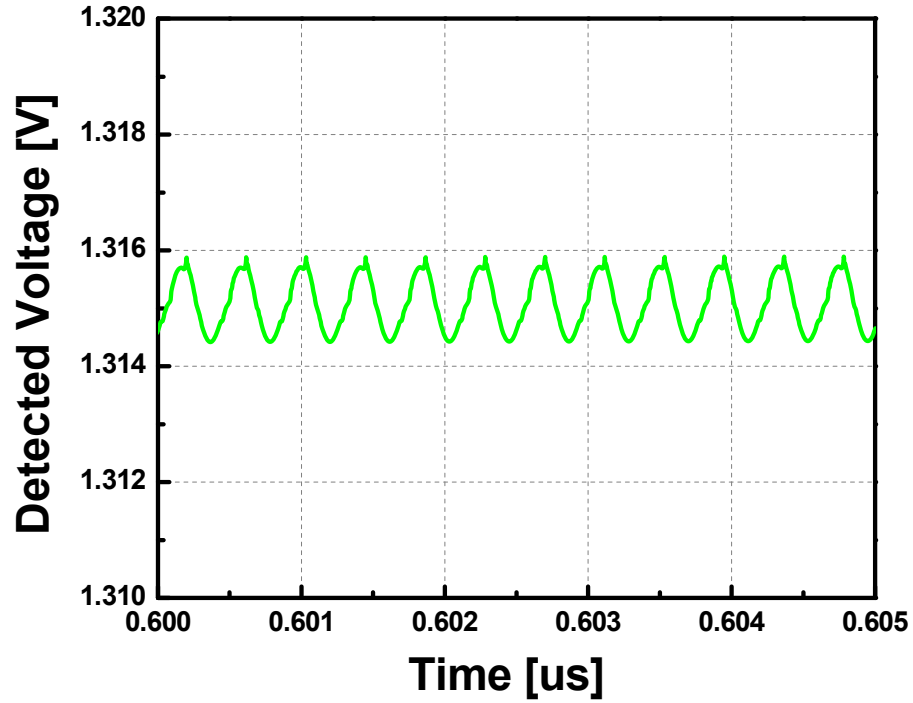


Figure 58. The size of ripple of the peak detector.

6.3.2. Comparator

A comparator is used to decide which input signal is higher than the other among the two input signals. Two comparators with an AND logic gate are used to judge whether the detected voltage is located within the allowed range as shown in Figure 54. Figure 59 presents the schematic of the comparator [45]. The two inputs are connected to the gates of the input differential pair transistors, MP_3 and MP_4 . If the signal applied to MP_4 (V_{inp}) is higher than that to MP_3 (V_{inn}), V_{out} becomes a high state. The MN_5 stage is used to increase the gain, and MP_8 and MN_8 are used to avoid any unwanted signal going into the next stage when the comparator is not in use.

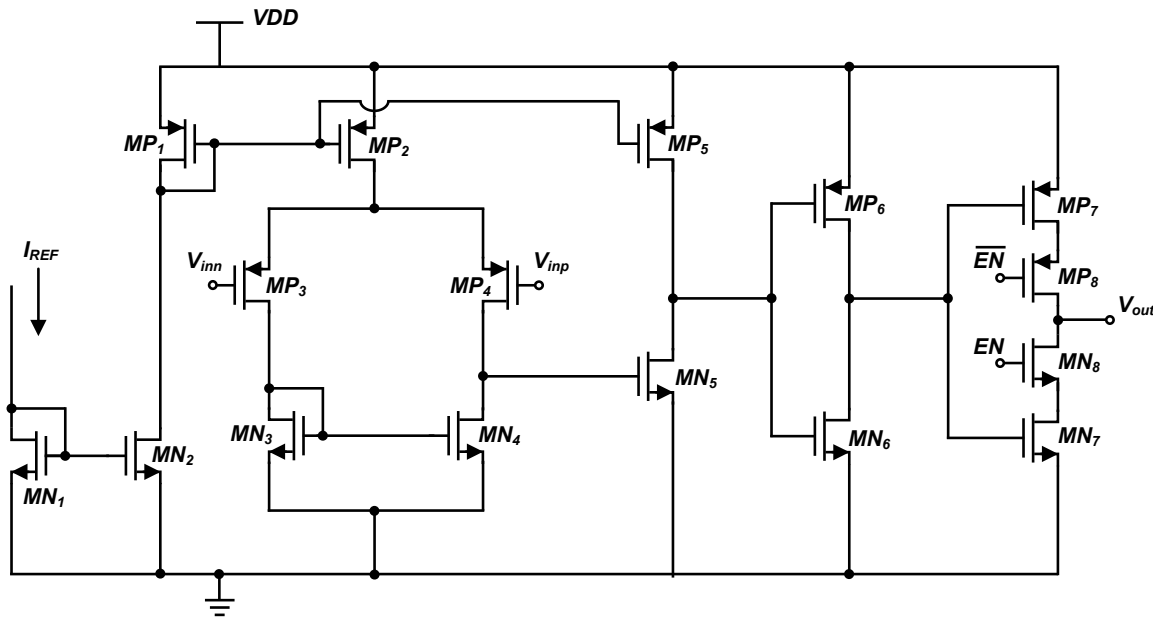


Figure 59. Schematic of the comparator.

The comparator should be able to handle the output signal of the peak detector. As presented in Figure 56, the output signal varies between 0.3 and 2.2 V. Therefore, the input transistor of the comparator is designed with PMOS differential input pairs to handle the relatively low-level signal range. Comparison performance within the required input voltage range is confirmed with simulations. Figure 60 presents the simulation results at two extreme cases that are lowest and highest input voltage levels. One of the input signals is set as a DC value (i.e., 0.3 and 2.2 V), while the other signal is toggling with 10 mV amplitude around that DC value. Figure 60(a) and (c) present two input signals, and Figure 60(b) and (d) present two simulated output signals for the case of 0.3

and 2.2 V, respectively. The comparator responds well according to the input level for both cases.

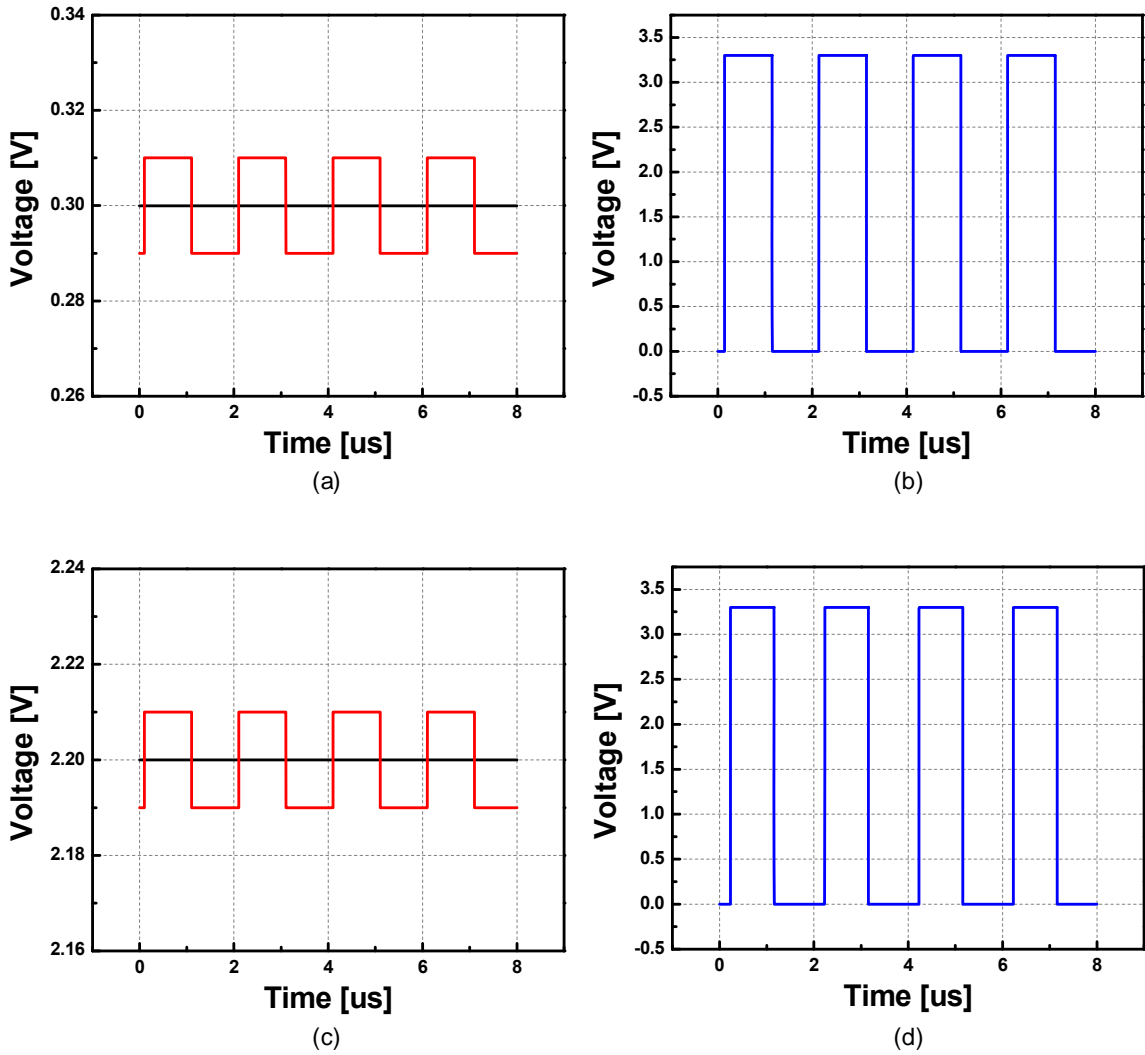
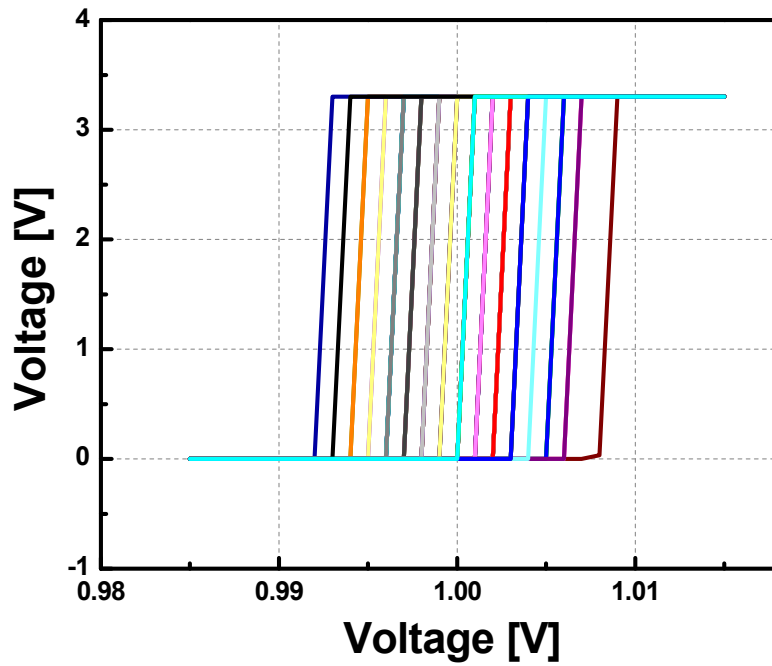


Figure 60. Transient simulation results of the comparator: (a) two input signals at 0.3 V, (b) output signal at 0.3 V input level, (c) two input signals at 2.2 V, and (d) output signal at 2.2 V input level.

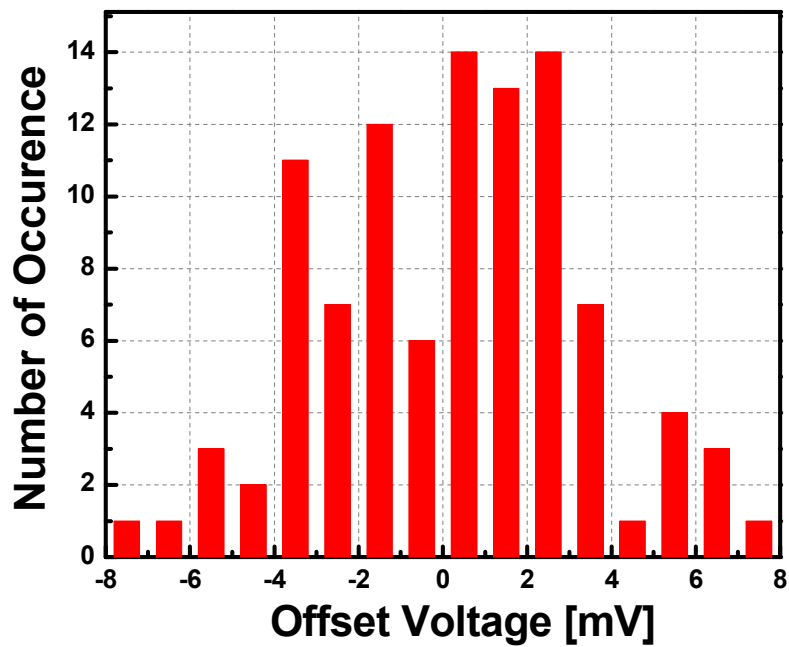
Since the input signal to the comparator is a low-frequency signal very close to DC, it is not critical how fast the input signal can be processed by this circuit. Rather, it is important how quickly the circuit can reach the steady state. That is, the rising or falling time of the output signal is an important characteristic in this application to reduce total recovery time similar to the peak detector case. In terms of both rising and falling times, the comparator requires less than 10 ns, which is much less than that of the peak detector. Therefore, the required time period for the comparator is a minor factor when calculating the total recovery time.

Next, it is important to minimize the offset voltage value for precise comparison results. To reduce offset voltage, both the channel length and the width of the input differential pair transistors are increased. Figure 61 shows the Monte Carlo simulation results, of which the number of iterations is 100. During the simulation, one input signal is set to 1V, while the other signal is varied from 0.98 to 1.02 V. At the nominal condition, transition of the output signal is expected to occur at 1 V. However, the transition happens between 0.99 and 1.01 due to an offset voltage as presented in Figure 61(a).

Figure 6.12(b) shows the number of occurrences according to the magnitude of the offset voltage. As shown in Figure 61(b), the offset voltage of the comparator mainly exists within ± 5 mV, which is to be considered when designing the overall recovery system. This offset value is important when deciding the minimum resolution of the detectable voltage. Offset cancelation techniques will be useful to improve the comparison precision.



(a)



(b)

Figure 61. Offset voltage distribution of the comparator from a Monte Carlo simulation. (a) Transient response and (b) offset voltage distribution.

6.3.3. Switched Capacitor

Among the detection and control circuitry, a switched capacitor needs to be considered when estimating the required time period for each comparison step. Since each switched capacitor consists of a large switch transistor and resistor, it requires a relatively long rising and falling times. Therefore, the required time period is one of the major factors of the total recovery time. Figure 62 presents simulated rising and falling times of all of the seven switched capacitors. The result shows that at least $2 \mu\text{s}$ is required to guarantee enough time to respond.

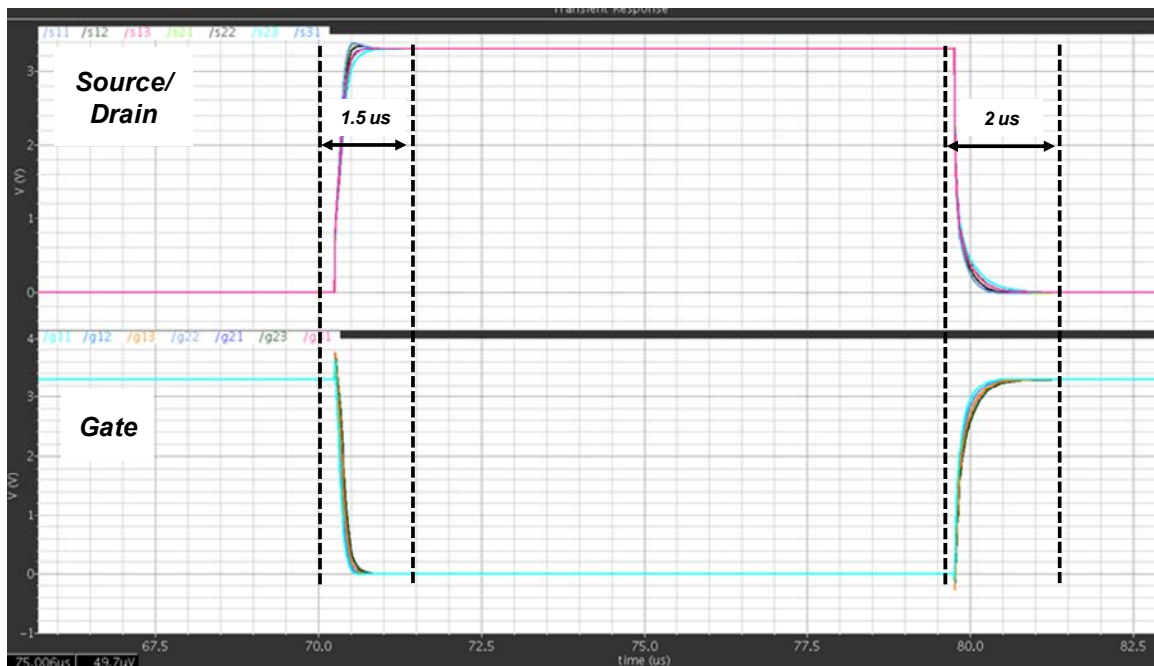


Figure 62. Transient response for turning on/off of a switched capacitor.

6.3.4. Seven-bit Counter

A seven-bit counter is used to change the state of the switched capacitor banks. Seven toggle flip-flops (TFF) are cascaded to implement the seven-bit counter. It outputs the value “1111111” then “1111110” then “1111101”, etc., until it hits “0000000”. The counter will be stopped when the output reaches a final value, and it means that a mismatch condition is not recovered. Figure 63 shows the output signals when the counter hits the last value without satisfied recovery. If a mismatch is not restored, the acceptable voltage range is to be increased, and the counter will start again. Figure 64 presents the other case, in which a mismatch is recovered before the counter reaches the end of states. A successful mismatch recovery is indicated by a “*Completion*” bit. If a mismatch recovery is achieved, the “*Completion*” bit changes to the high state. As illustrated in Figure 64, the counter stops changing values right after the “*Completion*” bit changes to the high state.

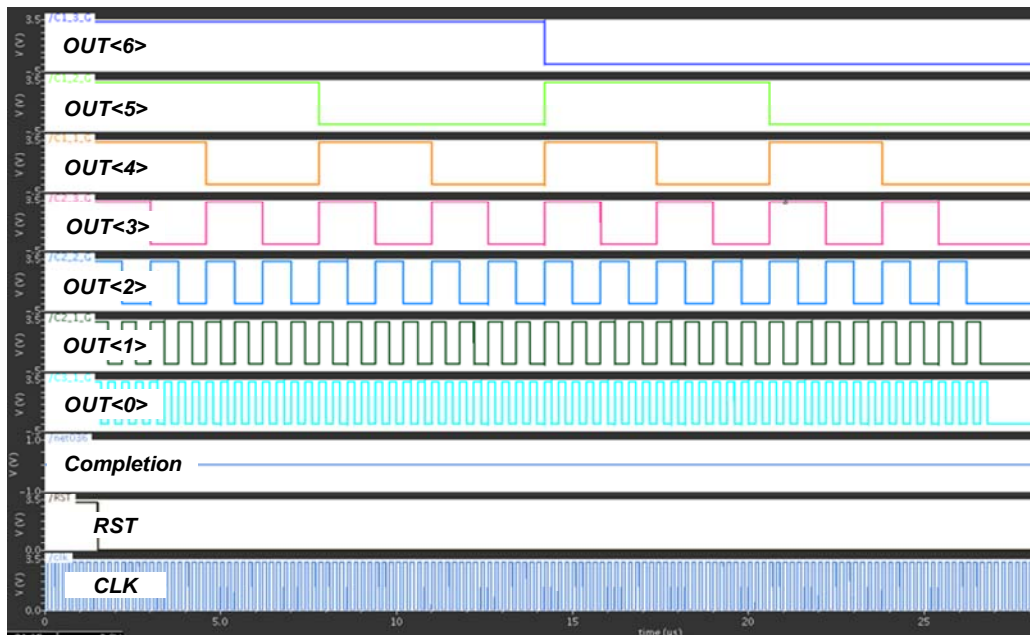


Figure 63. The counter output signal without mismatch recovery.

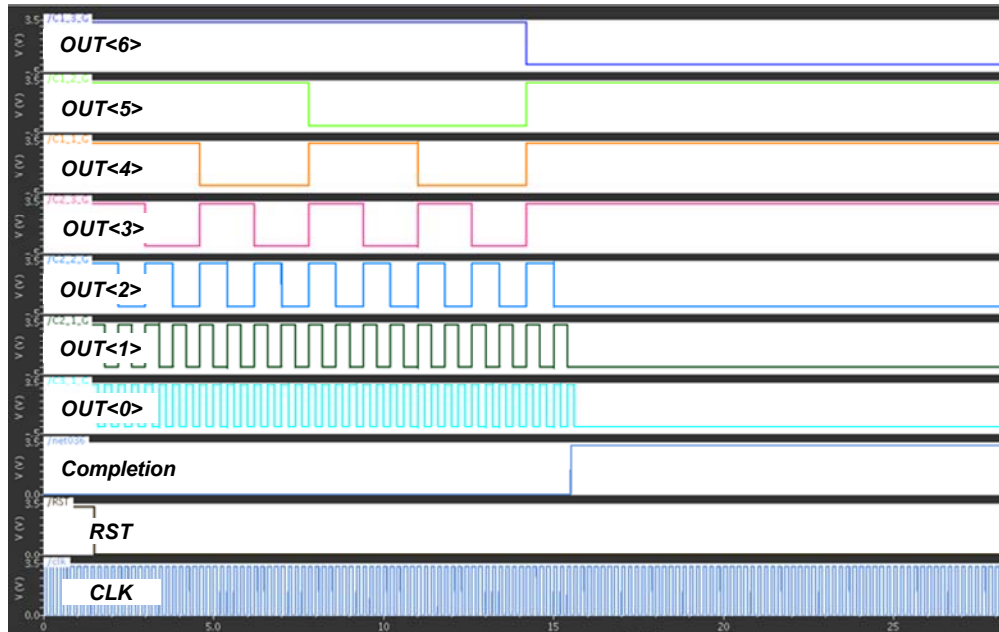


Figure 64. The counter output signal when mismatch recovery is achieved.

6.4. Simulation Results

Figure 65 presents the simulated matching impedance under the mismatch condition. The top-right Smith chart illustrates the mismatched antenna impedance with $\Gamma=0.3<0^\circ$, and the top-left Smith chart presents impedance points looking into the output matching network, where open circles represents all possible matching impedances at node A according to the combination of the capacitor banks, and the solid black dot indicates the desired matching point. In this section, it is necessary to confirm that the proposed detection procedure can find the right answer among all possible candidates, which is the closest matching point to the desired black dot.

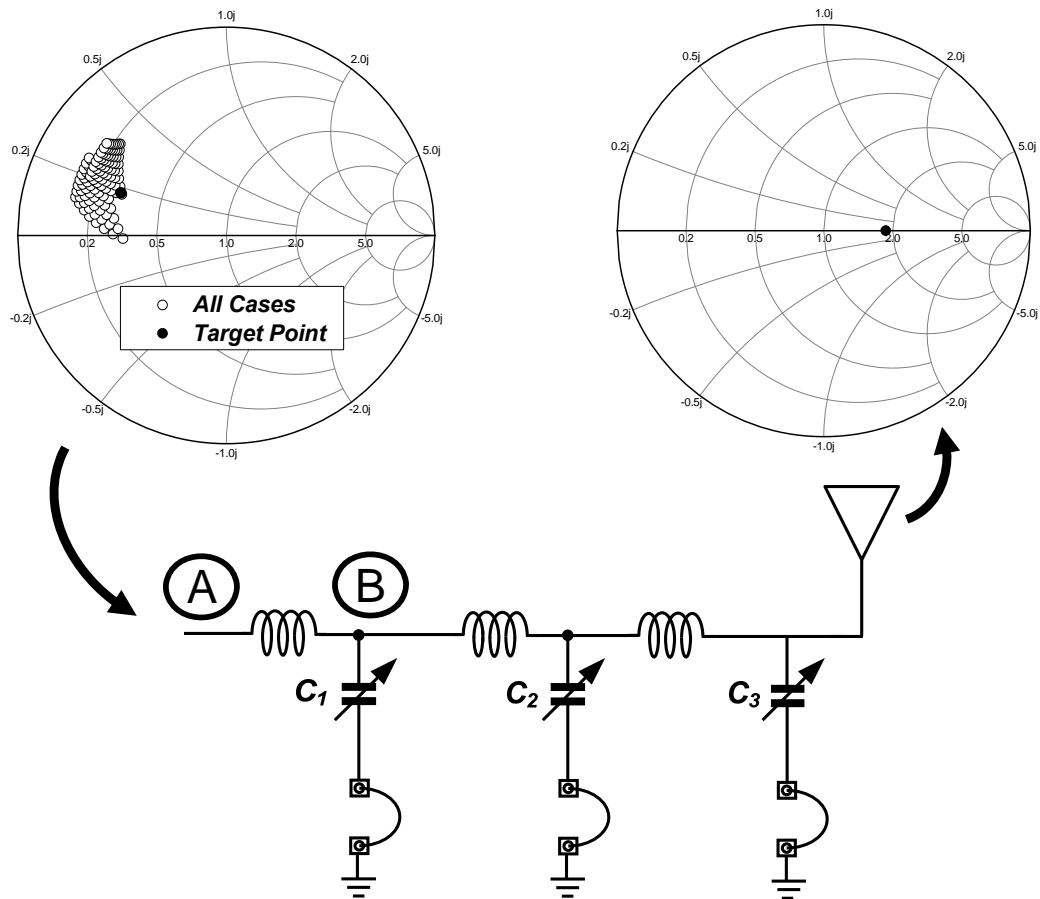
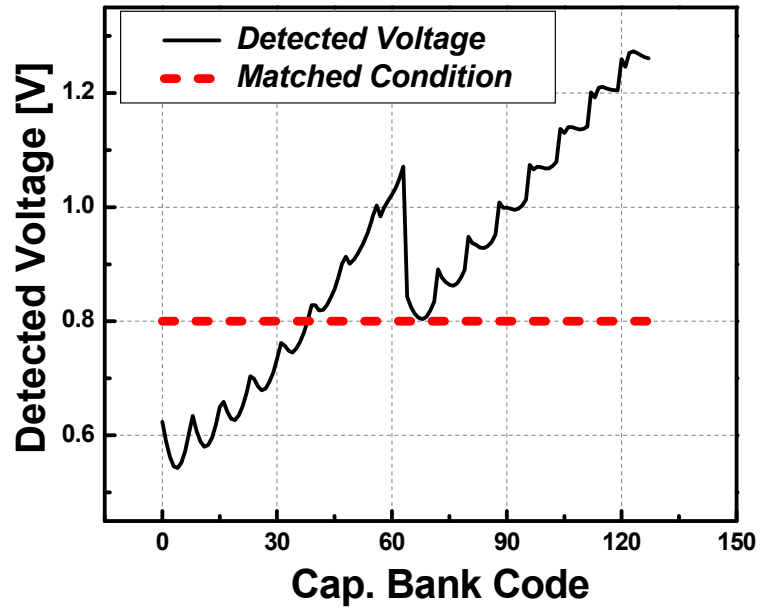
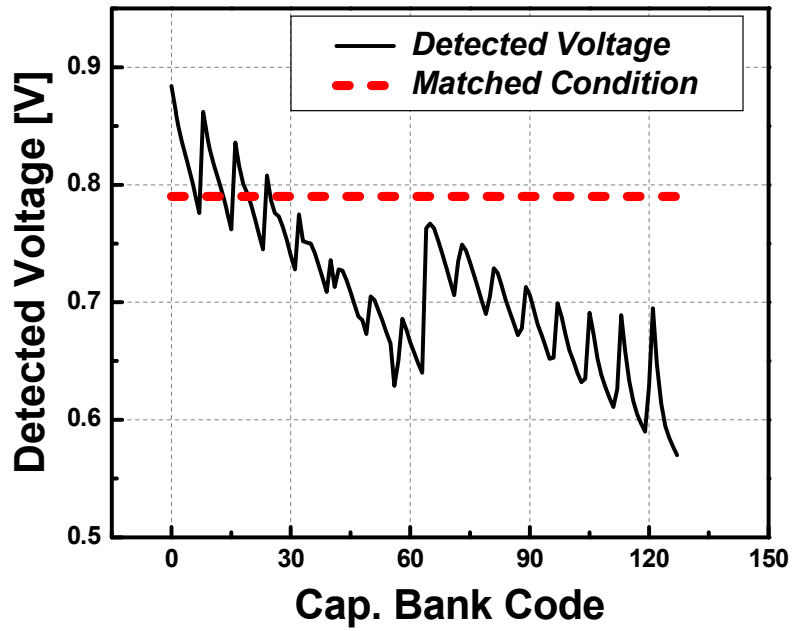


Figure 65. Simulated matching impedance according to the capacitor bank code under the mismatch of $\Gamma=0.3\angle 0^\circ$.

First, we check the voltage amplitudes at nodes A and B under the constant input power condition while changing a capacitor bank. The detected voltage amplitudes at nodes A and B (with -7 dBm input power) according to the capacitor bank code are illustrated in Figure 66. Seven bits of capacitor bank has total 128 code numbers. The red dashed lines in Figure 66 present the voltage amplitudes for the well-matched condition, which are 0.8 V and 0.79 V at nodes A and B, respectively. The black lines present the detected values.



(a)



(b)

Figure 66. Simulated detected voltage amplitude at nodes (a) A (V_A) and (b) B (V_B).

As previously explained, when the detected voltages of the two nodes are as close as possible to the red dashed lines at the same time, a corresponding capacitor bank code will be considered as a solution for mismatch recovery. For that comparison, we need to define an offset voltage that indicates how close the detected voltage exists to the target value. To select a correct capacitor bank, an offset value should increase from small enough value.

First, the simulation is performed with a 20 mV offset voltage. A 20 mV offset can be understood as follows: if the detected voltage at nodes A (V_A) and B (V_B) place between 0.78 (0.8-0.02) and 0.82 (0.8+0.02) V and 0.77 (0.79-0.02) and 0.81 (0.79+0.02) V, respectively, the corresponding case is considered as an exact solution. Figure 67 shows the comparison results with different offset values. Figures 67(a) and (b) present the case of a 20 mV offset. Node A has 9 capacitor bank codes that satisfy 20 mV offset voltage range, and node B has 15 cases. However, there is no concurrent solution for both nodes (Figure 67(b)). It means that this mismatch condition cannot be restored with a 20 mV offset voltage.

Therefore, the offset value is increased further. If the offset value is increased to 40 mV (i.e., $0.76 < V_A < 0.84$ and $0.75 < V_B < 0.83$), the number of solutions for each node increases to 16 at node A, and 30 at node B, which is illustrated in Figure 67(c). Among these cases, three cases satisfy the condition of nodes A and B at the same time as illustrated in Figure 67(d). Among those three cases, the first-appearing combination will be the detected solution.

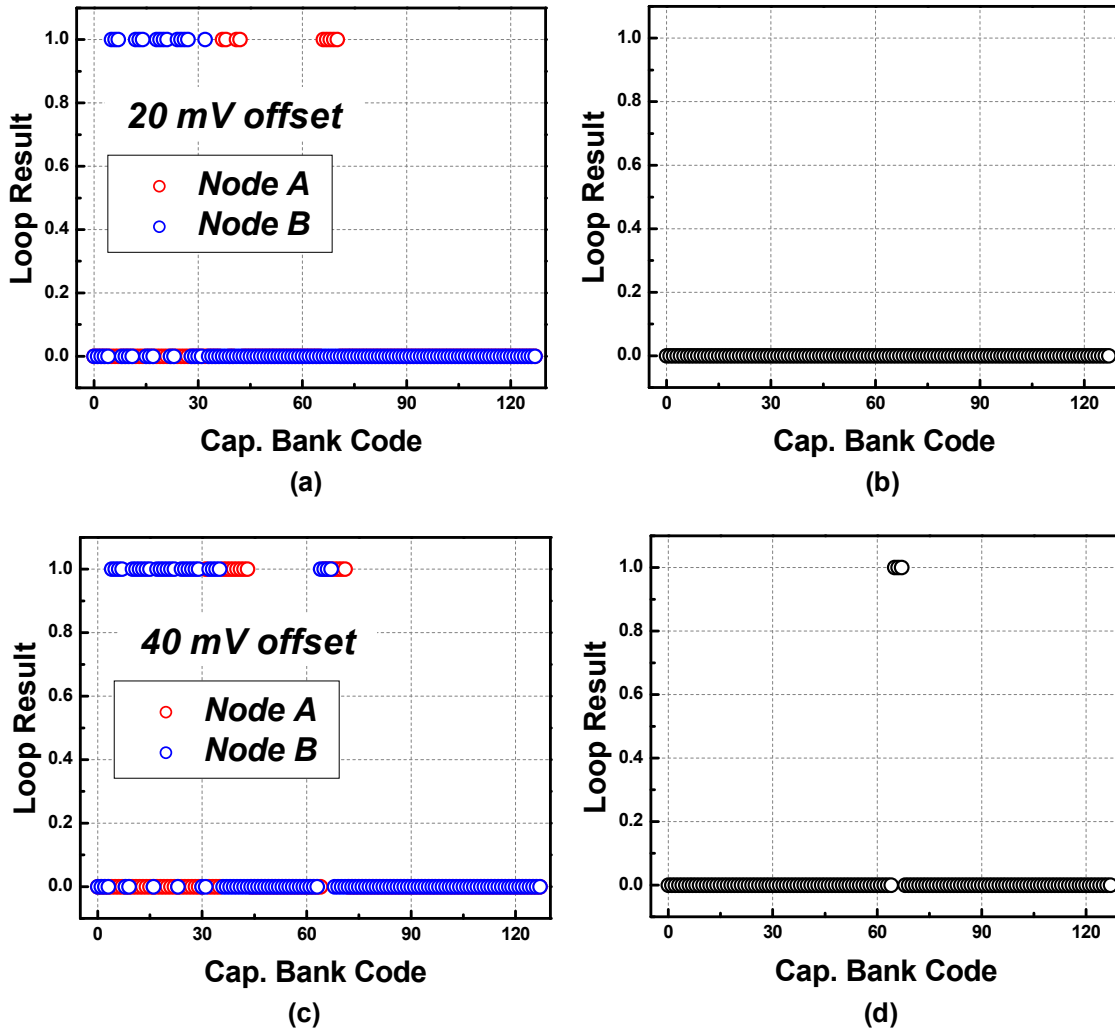


Figure 67. (a) Solutions for each node A and B with 20 mV offset, (b) common solutions for both conditions with 20 mV offset, (c) solutions for each node A and B with 40 mV offset, and (b) common solutions for both conditions with 40 mV offset.

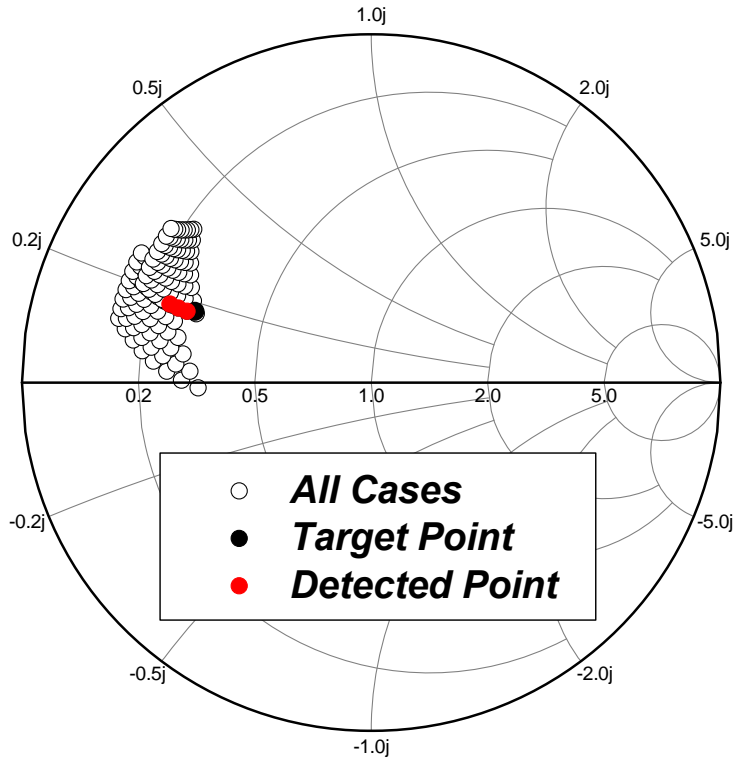


Figure 68. Detected impedance points with 40 mV offset at the mismatch condition of $\Gamma=0.3<0^\circ$.

Placing the selected combinations on the Smith chart is necessary to check how closely the points are attained by the introduced method. Figure 68 shows three detected impedance points, illustrated with red dots. As shown in Figure 68, the position of three selected points is very close to the desired point. This simulation result verifies that the proposed mismatch recovery method is valid at the mismatch condition of $\Gamma=0.3<0^\circ$.

Since this result is based on the condition of $\Gamma=0.3<0^\circ$ mismatch, all other angles need to be confirmed through same procedure. All around angles with a step of 45° are considered in this simulation. At each simulated angle, the offset value increases from 20 mV with a step of 20 mV. In other words, the offset voltage is initially set to 20 mV. If

the recovery solution is not found with an assigned offset value, the detection loop restarts from the beginning with bigger offset values such as 40, 60, 80 mV.

Figure 69 shows the overall simulation results. Each case has mismatched conditions of $\Gamma = 0.3 < 0^\circ, 0.3 < 45^\circ, 0.3 < 90^\circ, 0.3 < 135^\circ, 0.3 < 180^\circ, 0.3 < 225^\circ, 0.3 < 270^\circ,$ and $0.3 < 315^\circ$. Each Smith chart includes the target impedance point (black solid symbol), implementable impedance points by changing switched capacitors (black open symbols), detected impedance points by the proposed procedure (red symbols), and the offset voltages. The offset voltage means the offset amplitude value when the detected point has been selected. Some of the cases find the solution with 20 mV offset, while the other cases find it with 40 mV.

As illustrated in Figure 69, all of the cases show that the detected points exist very close to the target point, which demonstrates that the proposed detection procedure is not limited to a certain angle, but is useful to find the right answer all over the angles. Therefore, it can be confirmed that the proposed approach is a practical method to recover a mismatch condition with minimal circuit complexity.

In the next section, the measurement results will show how close the impedance points can be selected by the proposed mismatch recovery system. In addition, the PA performance will be compared between before and after the recovery process.

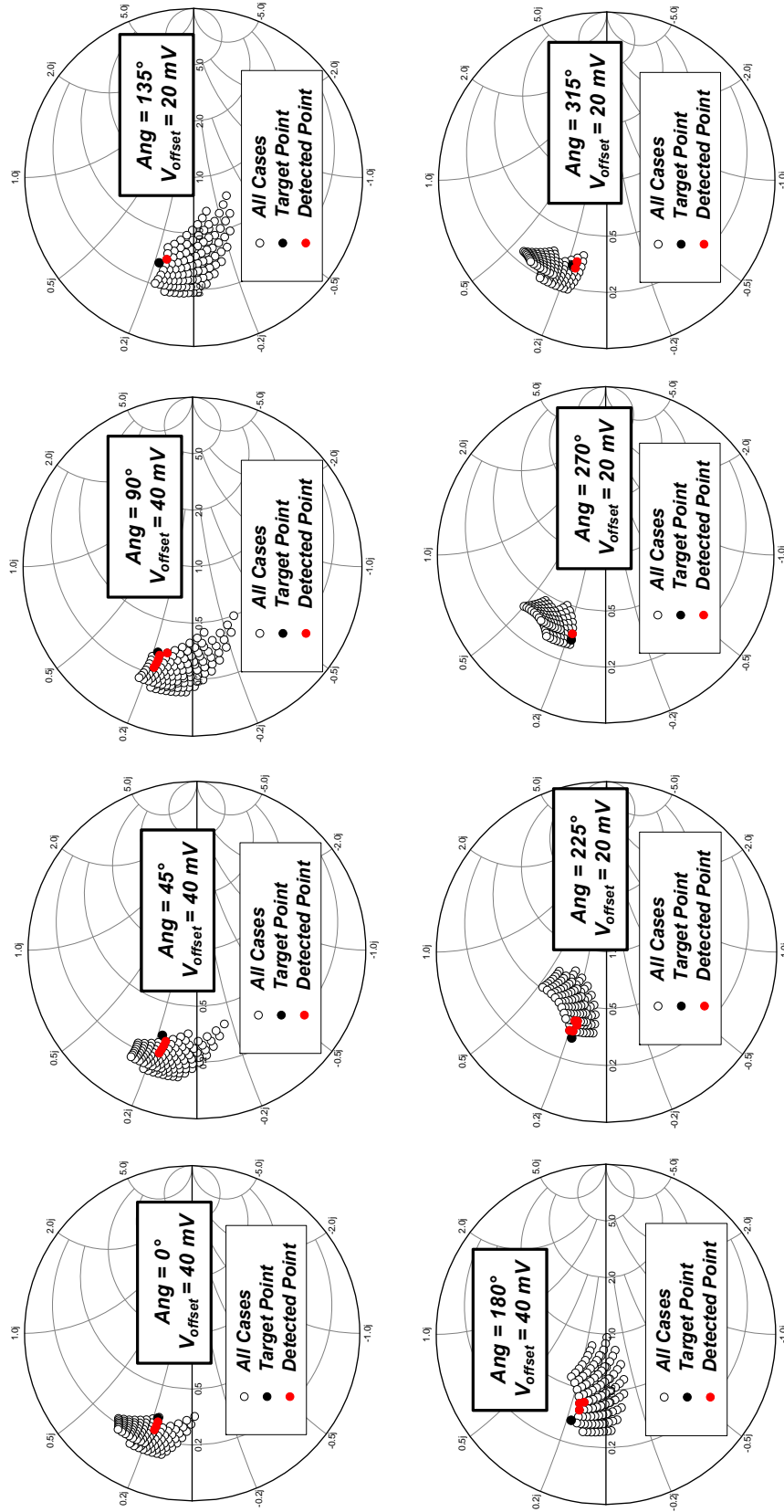


Figure 69. Detected impedance points after recovering step at all around angles.

6.5. Experimental Results

6.5.1. Measurement Setup

In this measurement, the voltage amplitude information under the well-matched $50\ \Omega$ condition is required for comparison. First, we measure manually the voltage amplitude at node A and B under the $50\ \Omega$ condition. With acquired voltage amplitudes, the mismatch recovery procedure will be verified by controlling offset voltage values. There are two indicators to check the result of the recovery loop. One of them (*Completion*) can tell whether the recovery is successful or not, and the other one (*End*) indicates the end of the counter. The following procedure shows the measurement steps.

- Measure the voltage amplitudes at the $50\ \Omega$ condition.
- Realize arbitrary mismatched antenna impedance by using Maury Microwave load-pull system.
- Set the reference voltage with a 20 mV offset voltage.
- Enable the counter and check the two decision bits (*Completion* and *End*).
- If the counter stops without a successful recovery (*Completion=0, End=1*), then increase the offset voltage with a 20 mV step and restart the counter.

After the mismatch condition is recovered by the above procedure (*Completion=1*), the PA performances will be compared before and after the recovery process. By

comparing the two results, we can demonstrate the effectiveness of the proposed design to maintain the performance under arbitrary mismatch conditions.

The measurement test bench in Figure 70 is used for the characterization of the PAs. A CMOS PA IC is attached on a PCB, and connected to the Maury Microwave load-pull tuner, which is capable of implementation arbitrary impedance from 0.8 to 18 GHz. The current source and arbitrary signal generator are used as a constant current biasing for analog circuits and a clock generator for digital circuits, respectively. DC power supplies are used to bias the gates of core cell transistors of the PA as well as V_{dd} of analog and digital circuits.

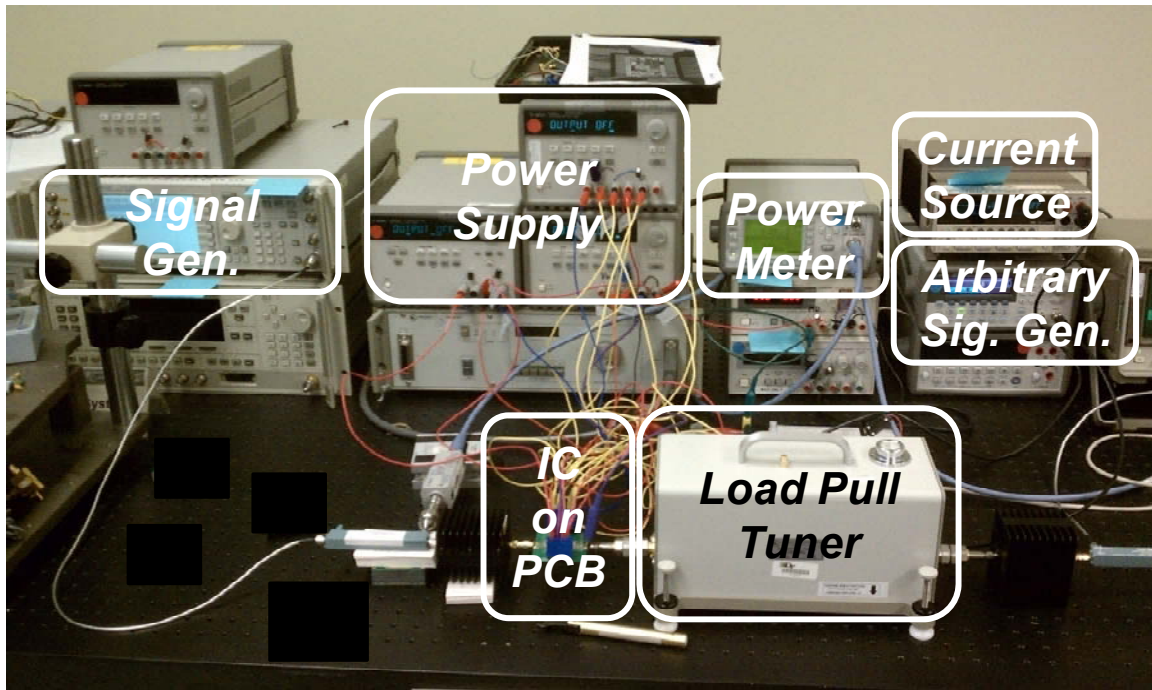


Figure 70. Measurement test bench.

6.5.2. Measurement Results

Figure 71 illustrates the die photograph of the proposed mismatch restorable PA, which is fabricated in a 0.18- μm RF CMOS process. This is the first fully-integrated CMOS PA which is capable of automatically recovering antenna mismatch conditions. The size of the chip is 1.65 mm \times 0.86 mm including all pads. White boxes indicate key circuit blocks such as the peak detector, comparator, SPI, counter, driver stage, and power stage.

The SPI circuit is used to control various components such as switched capacitors, MUX addresses, and reference voltage selection, which is summarized in Table 6 with respect to the register addresses.

Figure 72(a) shows the implemented mismatched antenna impedance at $|\Gamma| = 0.3$ with eight different angles (0° , 45° , 90° , 135° , 180° , 225° , 270° , 315°), and Figure 72(b) illustrates transformed impedance at the drain node looking into the output matching network at 2.4 GHz. The square symbol indicates original targeting impedance under the 50 Ω antenna condition, while the black circle symbols present distorted matching impedance under a mismatch condition ($|\Gamma| = 0.3$) without any recovery function. When obtaining black circles, the output matching network is set as the 50 Ω condition, and the antenna impedance is changed. As illustrated in Figure 72(b), the matching impedances under mismatch conditions are far from the targeting point. The performance degradation caused by this alteration will be confirmed by the following measurement results.

Table 6. The SPI control description.

Register Adress	Control Description
Reg. 0	Counter Reset and Automatic Recovery Start
Reg. 1	Manual Control Switched Capacitor Banks
Reg. 2	Ref. Voltage Selection for 1_high
Reg. 3	Ref. Voltage Selection for 1_low
Reg. 4	Ref. Voltage Selection for 2_high
Reg. 5	Ref. Voltage Selection for 2_low
Reg. 6	Output Mux Control (Read Recovery Results)
Reg. 7	Read & Enable Peak Detection Circuit

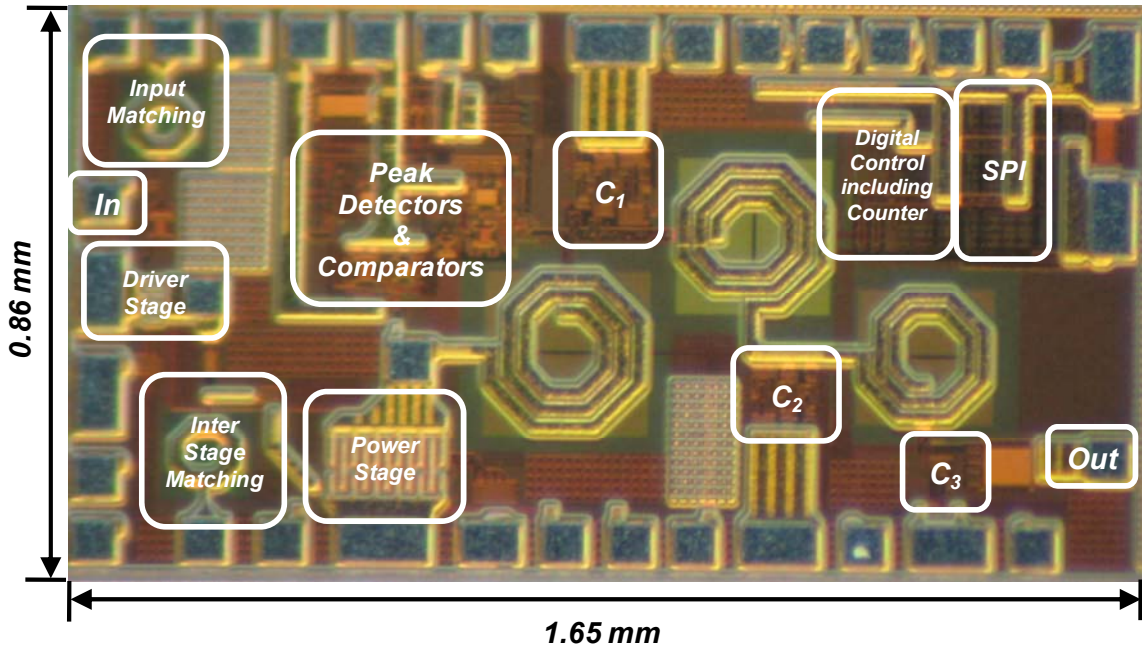
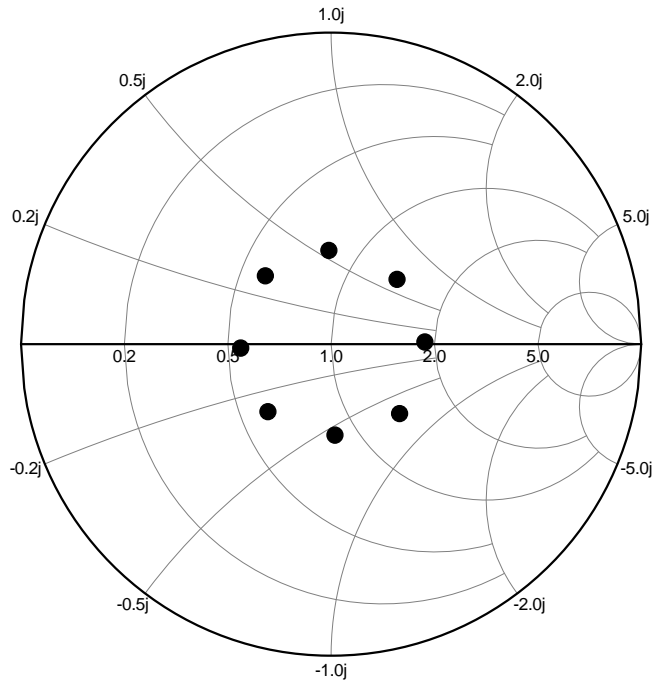
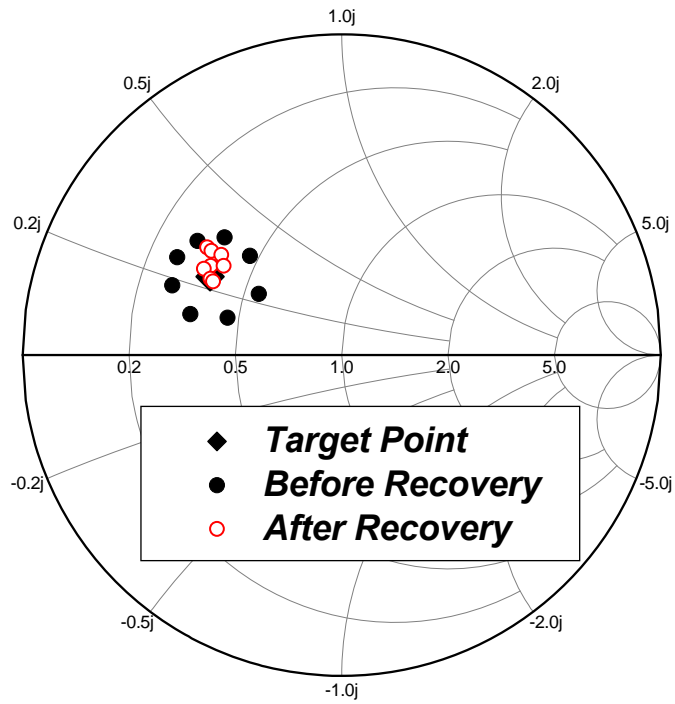


Figure 71. Die photograph of the mismatch restorable PA.



(a)



(b)

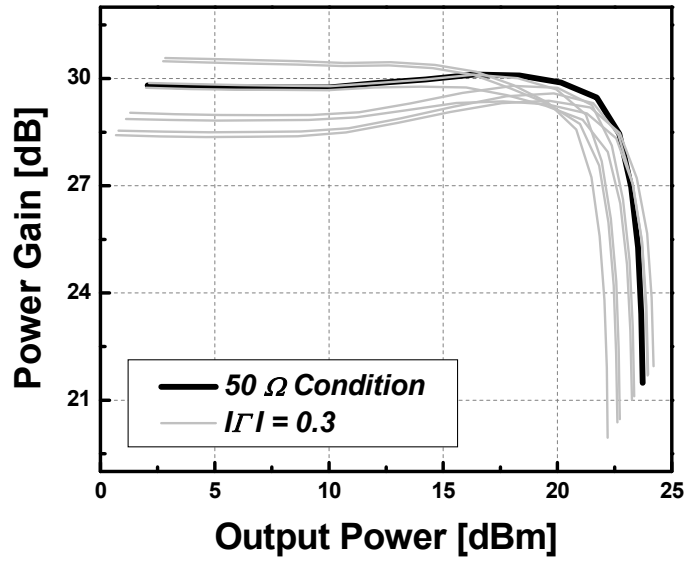
Figure 72. (a) Implemented mismatched antenna impedance and (b) transformed impedance looking into output matching network.

On the other hand, red open circles in Figure 72(b) are obtained after activating the automatic recovery loop. After starting the control loop, the *Completion* bit is checked whether a recovery process is successful or not. The offset voltage is increased and the control loop is reactivated until the *Completion* becomes a high state. When the *Completion* changes to a high state, the detected combination of capacitor banks is acquired by using the SPI control. After that, the red open circles in Figure 72(b) are obtained by using a VNA with the corresponding recovered capacitor bank under a mismatch condition. As it can be confirmed in Figure 72(b), the matching impedance at the drain node closely approaches to the targeting point after a recovery step. Thus, the improved performance is expected after recovery process.

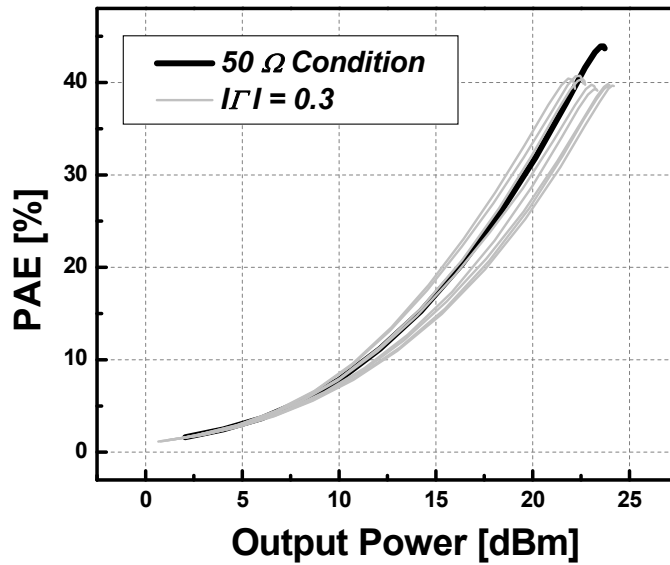
The measured power gain and PAE with a 2.4-GHz single-tone signal are shown in Figure 73. Figure 73 includes a well-matched 50 Ω condition and mismatched conditions with $|\Gamma|=0.3$, which indicates a constant reflection coefficient ($|\Gamma|=0.3$) circle with a 45° angle step as shown in Figure 72(a). For this measurement, the output matching network is set as the 50 Ω condition, and the measured characteristics show how serious the PA performance is degraded due to mismatched impedance. As shown in Figure 73, both maximum output power and efficiency are decreased under mismatch conditions. Along with the reduced output power level and efficiency, considerably distorted AM-AM characteristics are raised, which implies that the linearity characteristic is also degraded.

The results after recovery completion are presented in Figure 74, which also includes previous results illustrated in Figure 73. Therefore, how much the performance is preserved by utilizing the proposed mismatch recovery system can be validated. In the case of power gain, red dashed lines (w/ recovery) become closer to the matched result,

and the variation is reduced. That is, the maximum output power level as well as the distorted AM-AM features is restored by the mismatch recovery system. In the case of efficiency, the mismatch recovery system increases the PAE and reduces the PAE variation. Therefore, the efficiency curves also approach to the normal 50- Ω condition.

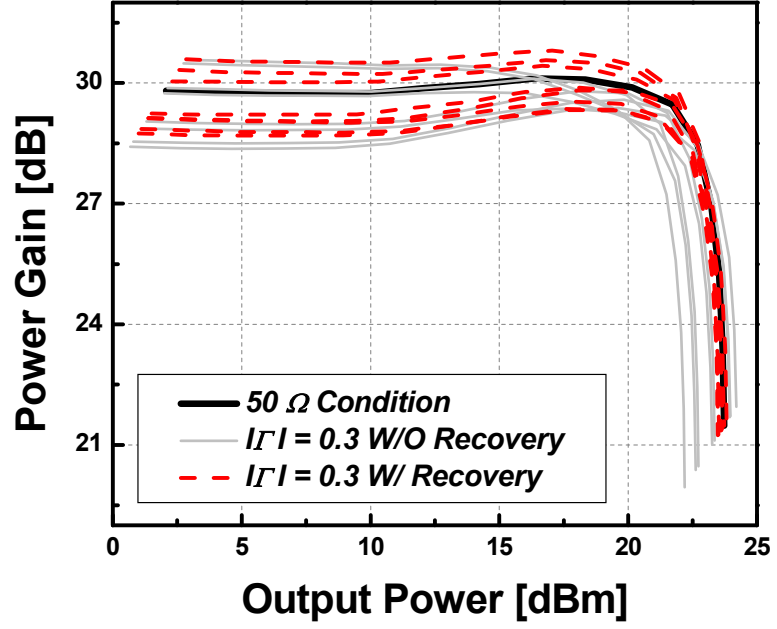


(a)

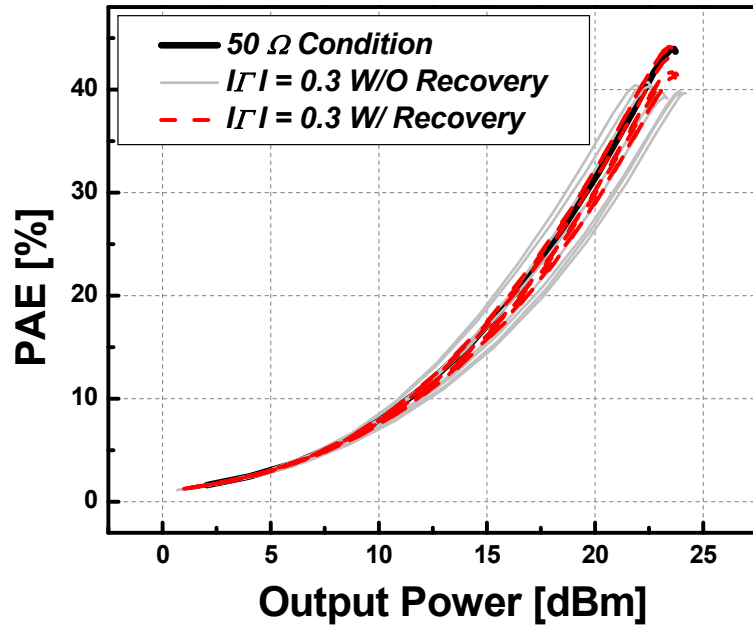


(b)

Figure 73. Measured (a) power gain and (b) efficiency at mismatched conditions.



(a)

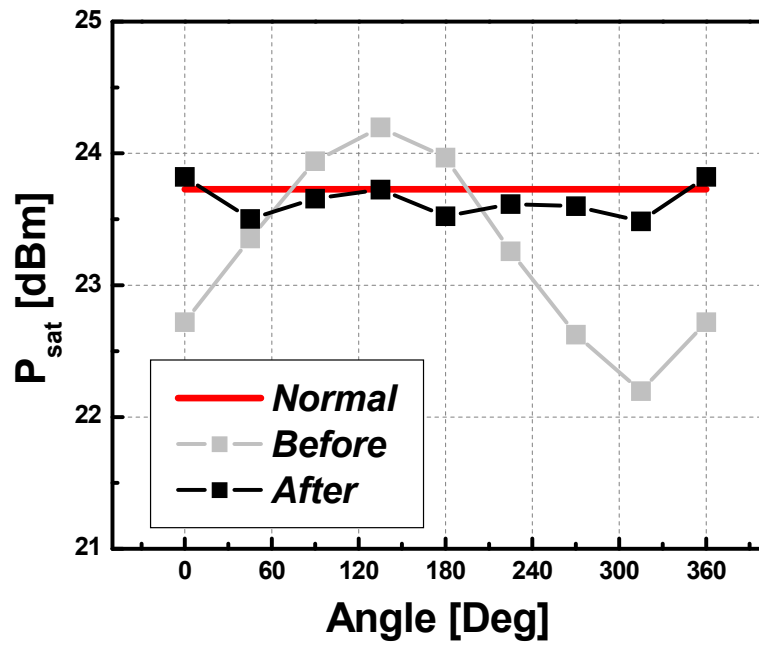


(b)

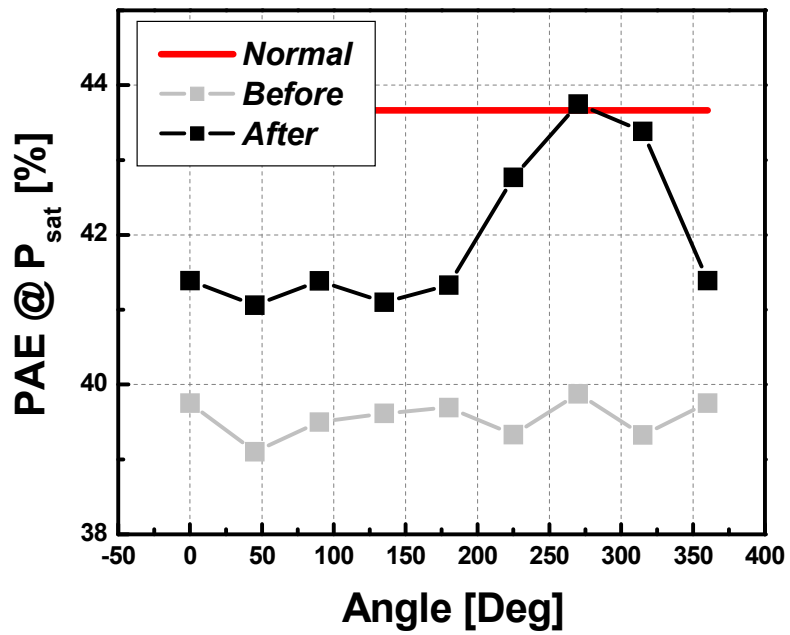
Figure 74. Measured (a) power gain and (b) efficiency at mismatched conditions after recovery procedure.

The improvement by using the recovery system is also able to be identified by another indicator. First, the maximum output power level and efficiency can be used for the purpose of comparison. If the well-matched condition is maintained, both should have close enough values to the original design. Figure 75 presents P_{sat} and PAEs at P_{sat} . The red line indicates the normal 50- Ω condition, and gray/black lines mean before/after recovery action. As shown in Figure 75, both the maximum output power and efficiency approach the normal 50- Ω condition after recovery operation.

Even though the results in Figure 75 are a meaningful indicator of performance improvement, the other indicator considering linearity characteristic can be also used to understand how much performance is improved, which is 1-dB gain variation point (P_{1dB}). Typically, P_{1dB} is defined as 1-dB gain compression point. However, in this design both the gain expansion and compression under a mismatch condition are significant, so P_{1dB} is defined as 1-dB gain variation from the small signal value. Figure 76 shows P_{1dB} and PAE at P_{1dB} . Both power and efficiency at P_{1dB} are much improved after recovery operation, and approach very close to the normal 50- Ω condition. These measurement results show that the proposed method is very effective at improving a mismatched condition.

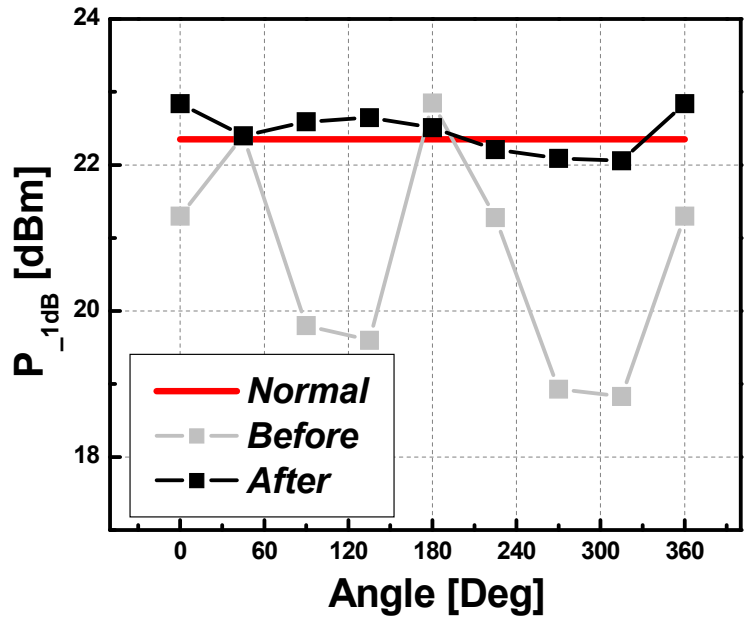


(a)

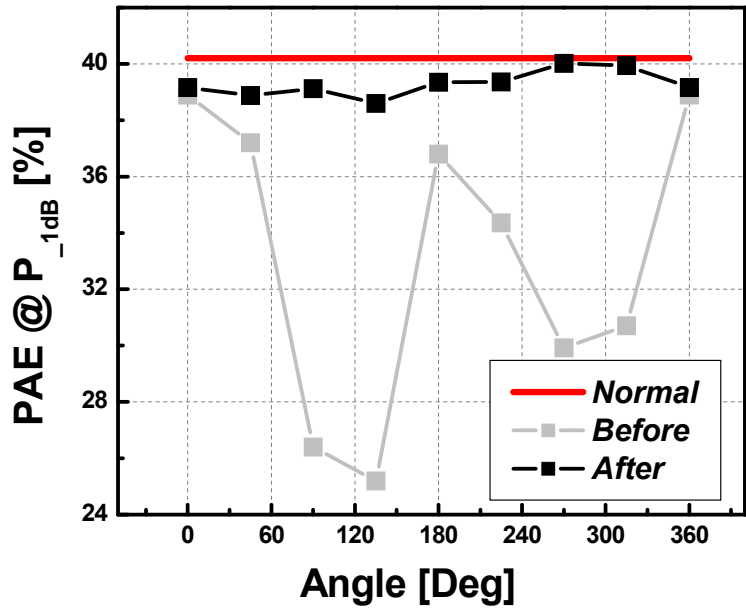


(b)

Figure 75. (a) Maximum output power (P_{sat}) and (b) PAE at P_{sat} .



(a)



(b)

Figure 76. (a) P_{1dB} and (b) PAE at P_{1dB} .

6.6. Conclusions

In this chapter, a reconfigurable CMOS PA with automatic antenna mismatch recovery system is presented. The proposed PA utilizes the integrated output matching network itself to compensate the mismatched impedance, and also has a fully-integrated recovery system. To our knowledge, this is the first PA design which can recover a mismatched condition for itself. The presented research proposes the simple mismatch detection method and demonstrates its effectiveness with measurement results. After recovery action, the output power as well as efficiency is improved close to the normal 50- Ω condition. By adapting this method, the PA can maintain its original designed performance even under various mismatch conditions.

CHAPTER 7

CONCLUSIONS

In recent years, the field of CMOS PA is getting more interests from both academia and industry. At the time of this writing, a CMOS PA is already integrated with other RF transceiver components for WLAN applications. Furthermore, this effort will not stop here, and it is expected to expand further to cellular applications for a single chip radio solution. At this point, the following achievements of this research will contribute to obtain a PA with better overall performance.

The achievements can be summarized as follows:

- A new CMOS switched capacitor structure for high-power applications is proposed. The proposed structure demonstrates considerably improved power handling capability and linearity over the conventional structure. Consequently, it will be a promising component to implement a tunable CMOS PA. The maximum allowable voltage amplitude to the switched capacitor is derived and validated with simulations. The derived voltage limitation is to be a guideline when designing the switched capacitor for high-power applications.
- The dual-mode CMOS PA with the integrated tunable matching network in a standard CMOS process is presented, which has enhanced low-power efficiency. The proposed PA achieved the required optimum matching impedances for each operation mode simultaneously. Therefore, the application of the tunable matching network produces a great improvement compared to the recently reported multi-mode

PAs. The improved efficiency in this design is approximately twice as good as other multi-mode CMOS PAs reported so far.

- A switchless dual-band matching structure is proposed and the effectiveness of the proposed structure is demonstrated with a fully-integrated concurrent dual-band CMOS PA. The concurrent dual-band PA delivers the maximum output power and maximum efficiency at two frequencies, 2.45 and 3.8 GHz without any switching operation. The switchless dual-band matching structure will be a suitable component to achieve an integrated compact multi-band PA.
- A reconfigurable CMOS PA for improving the robustness to antenna mismatch is proposed. Since the output matching network itself with a three-stage LC matching is utilized to recover a mismatched condition, it is very effective in terms of the size and power loss. The improvement from the reconfigurable matching network makes the proposed design very promising for achieving an integrated CMOS PA which can circumvent the antenna mismatch problem.
- Lastly, a reconfigurable CMOS PA with automatic antenna mismatch recovery system is presented. The proposed PA also utilizes the integrated output matching network itself to compensate the mismatched impedance, and has a fully-integrated automatic recovery system. To our knowledge, this is the first PA design which can recover a mismatched condition for itself. After the recovery action, the output power as well as efficiency is improved very close to the normal 50- Ω condition. By adapting this method, the proposed PA can maintain its original designed performance even under various mismatch conditions.

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