

Proximity Lithography in Sub-10 Micron Circuitry for Packaging Substrate

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Abstract—Rapid changes in the semiconductor industry will continue toward higher functionality that leads to higher input/outputs (I/O) counts, pushing packaging towards higher density architectures. In the next two to three years, the I/O pitch will fall within $100\ \mu\text{m}$ for area array die and $30\ \mu\text{m}$ for periphery die. That raises an important question to the packaging industry: How will the rapid shrinkage of the I/O pitch affect the package substrate for chip attaching? The answer is sub-10 micron copper line technology. Theoretical and experimental studies on the limitations of using mercury i-line ultraviolet photolithography have been carried at the Packaging Research Center at Georgia Tech. Furthermore, ultra fine copper line routing substrates are demonstrated for flip chip attaching by using semi-additive metallization process.

Index Terms—Flip-chip devices, interconnections, lithography, packaging, printed circuit board (PCB) substrates, printed circuit fabrication.

I. INTRODUCTION

THE International Technology Roadmap for Semiconductors (ITRS) [1] predicts that the pad pitch of microprocessor packages will be $120\ \mu\text{m}$ in 2011 and down to $95\ \mu\text{m}$ in 2016 for area array flip chips [2] while the periphery pad pitch would be down to $25\ \mu\text{m}$ in 2016. A build-up substrate consisting of multiple wiring layers with routing line width and space below $10\ \mu\text{m}$ will be needed. Fig. 1 illustrates the needs of routing line width and space for an area array flip chip with I/O pitch of $100\ \mu\text{m}$ and pad diameter of $40\ \mu\text{m}$. For $60\ \mu\text{m}$ spacing between two adjacent pads, the line width must be $20\ \mu\text{m}$ or less so that two rows of copper lines can be routed between the pitches. When three signal rows need to be accessed, $12\ \mu\text{m}$ line width and space are required. If four signal rows need to be accessed, $8.5\ \mu\text{m}$ line and space becomes necessary. The maximum number of I/O escaped per layer is calculated and listed in Fig. 1. The more the number of I/Os that are achieved (or fanned out per layer), the greater is the reduction in layer count. The

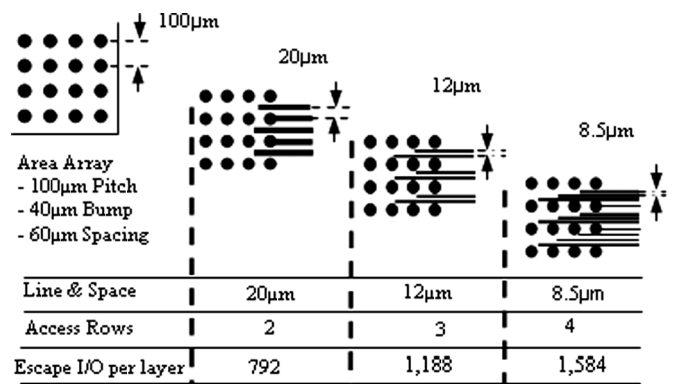


Fig. 1. Routing requirements for an area array flip chip with $100\ \mu\text{m}$ pitch.

main advantage with lower layer count is the reduction in material consumption and the time saving in fabrication, which result in lower cost. Using fewer layers, the number of processing steps is also reduced, and the yield will be increased. In addition, the package will be more reliable. The realization of such fine feature size, while maintaining low cost, is a key challenge for the packaging industry.

Fig. 2 illustrates the advances of packaging technologies from earlier dual in line package (DIP) technology [3] in the 1970s, to surface mount technology (SMT) in the 1980s, such as quad flat package (QFP) [4], etc. to current advanced IC packages, such as ball grid array (BGA), chip scale package (CSP) [5], etc., in the 1990s, and system-in-package (SIP) [6] in the 2000s, and to highly integrated system-on-package (SOP) system technology [7]. The SOP offers advantages over the 3-D packaging and the SIP. The 3-D packaging is a general concept of stacking of similar or dissimilar chips such as DRAMs with processor and flash memory. The SIP goes beyond to embed actives and passives that are discrete, thick, and bulky components. The SOP goes further in the ultimate 3-D integration of components in thin-film form at microscale in the short term, and nanoscale in the long term.

Photolithography is a dominant process used in microfabrication on both semiconductor and packaging board substrates. It uses ultraviolet (UV) light to transfer and define a latent pattern from a photomask to a light-sensitive photoresist. Then, chemical treatment will engrave the relief pattern into the material underneath the photoresist. There are three basic UV photolithography methods: contact printing [8], proximity printing [9], and projection imaging [9]. Proximity and contact printing technologies play a dominant role in the printed circuit board (PCB) and

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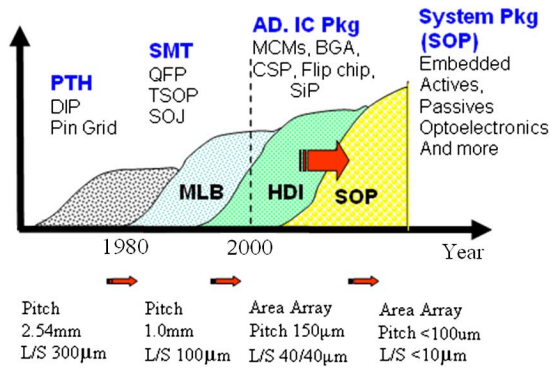


Fig. 2. Packaging advances and Trends: DIP type package (1970s), SMT (1980s), advanced IC packages (BGA, CSP, etc. 1990s, and SiP, 2000s), and next generation SOP.

packaging industry, while projection imaging is used in semiconductor IC manufacturing.

The semiconductor industry has developed features of 30 nm for high performance microprocessors. While the feature size that the packaging industry can produce is about 15 ~ 20 μ m, a huge technical gap exists between semiconductor industry and packaging industry. In order to keep the pace with semiconductor process development, a process for finer pitch wiring substrate is necessary. In this paper, we investigate the key factors that hinder the finer feature size formation on packaging substrates and explore the minimum size of lines and spaces that can be obtained based on the high pressure mercury i-line photolithography.

II. THEORETICAL ANALYSIS OF PROXIMITY PHOTOLITHOGRAPHY

The pattern definition in the resist in proximity photolithography is a two-step process consisting of a latent image formation via the exposure, followed by development process to generate a relief structure. Therefore, limitation factors in both exposure and development processes will be considered. The exposure process, as well as the post processes (e.g., baking and developing), have to be optimized to realize fine lines and spaces.

The primary resolution limitation of proximity photolithography is diffraction of light at the edge of an opaque feature on the photomask as the collimated UV beam passes through an adjacent clear area. To simplify the analysis, the discussions of diffraction effect are based on the assumption of fully spatially coherent UV exposure light. Fig. 3(a) illustrates how light is “bent” and diverted by an equal line and space grating (i.e., a grating with equal width of the wire and the space between the adjacent wires) on the mask due to diffraction. The intensity distribution of UV light inside the photoresist can be estimated by computer simulation based on the Fresnel diffraction theory [10]. As an example, the light intensity distribution of the UV beam passing through a photomask (with 10 μ m line and space grating) on the photoresist is shown in Fig. 3(b), given an 80 μ m air gap between the photomask and the resist. The light intensity of the UV beam on the resist outside the desired exposure area (as shown in Fig. 3(b), especially where the intensity is above

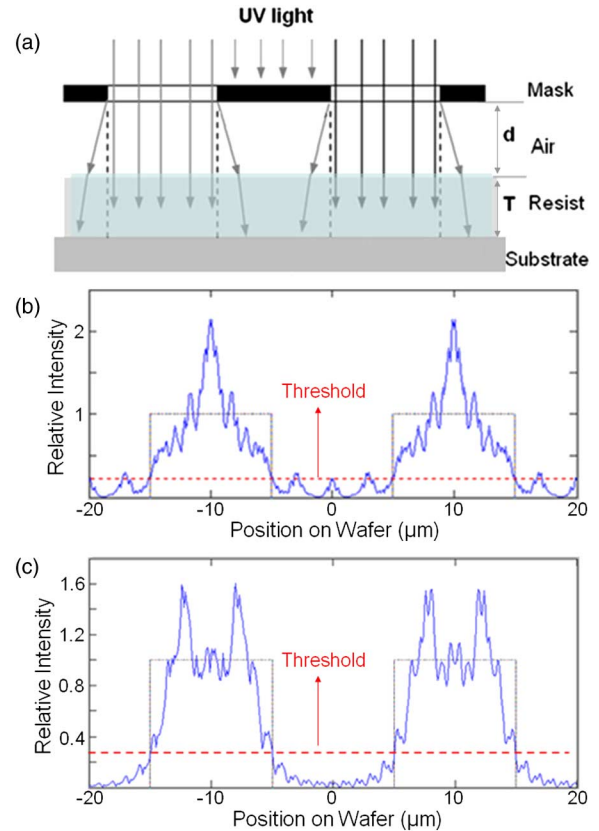


Fig. 3. (a) Schematic of UV light propagation through a photomask containing a grating with equal lines (white rectangles) and spaces (black rectangles); and simulation of light intensity distribution inside the photoresist at the wavelength of 365 nm under the photomask of 10 μ m line and 10 μ m space, with (b) the air gap of 80 μ m, and (c) the air gap of 30 μ m. The dotted lines in (b) and (c) show the sensitivity threshold of the photoresist. For light intensity above the threshold, the change in the material properties occurs.

the red line) is comparable to the threshold sensitivity of the resist, which will result in the resist residue between the desired patterns on the substrate and make it difficult to form structures with 10 μ m resolvable feature size under such exposure conditions. While the air gap is reduced, the maximum light intensity diffracted outside the open area of the mask decreases and will eventually become negligible compared to the sensitivity threshold of the resist. An example of this case for the fabrication with a 30 μ m air gap is shown in Fig. 3(c). It is clear from Fig. 3(c) that 10 μ m feature size structures can be achieved under this exposing condition with 30 μ m air gap using the optimized developing process.

III. EXPERIMENTAL STUDY AND DISCUSSION ON GAP EFFECT

To optimize the exposing and development processes, it is necessary to study the sensitivity of the photoresist experimentally. A layer of 7.5- μ m-thick photoresist NT-90 was spin-coated on a bare silicon substrate. The sample was covered by a moving opaque mask at a constant speed under UV exposure, so that the exposure dose varies linearly along the sample. Then, the whole sample experiences the same postprocess (baking and developing). The residual photoresist thickness was measured by a contact surface profiler (DekTek 303). Fig. 4 shows the relationship between the residual photoresist NT-90

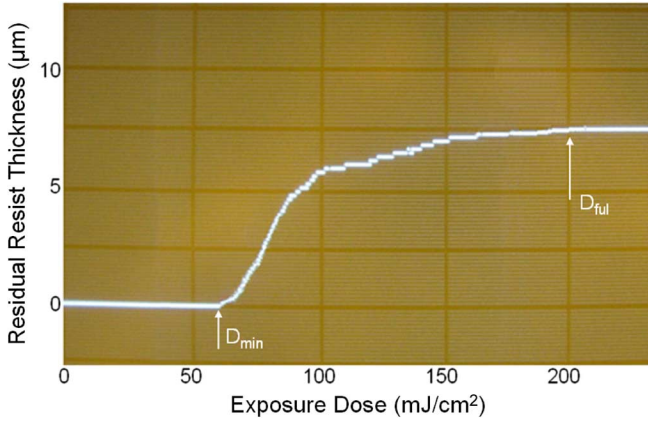


Fig. 4. Experiment results for the residual photoresist thickness dependence on the light exposure dose. The initial photoresist NT-90 thickness is $7.5 \mu\text{m}$, and the light intensity is $24 \text{ mW}/\text{cm}^2$ at the wavelength of 365 nm .

thickness and the exposure dose. From Fig. 4, we can define two important parameters representing the threshold properties of this negative photoresist: $D_{\min} = 62 \text{ mJ}/\text{cm}^2$ (the minimum exposure dose required to produce insolubilized residue) and $D_{\text{ful}} = 200 \text{ mJ}/\text{cm}^2$ (the minimum exposure dose for the full sensitization of the resist). In the following experiments, a 10% overexposing dose over D_{ful} (i.e., $0.1 * D_{\text{ful}} = 20 \text{ mJ}/\text{cm}^2$) is applied to ensure the full sensitization of the whole layer of the photoresist.

Well-controlled process conditions are necessary since the minimum achievable feature size is very sensitive to the process conditions, such as exposure dose, baking (temperature and time), development (solution concentrations, temperature, and time), etc.

Our experimental steps are as follows: 1) design a photomask with three groups of testing comb structures. Each pattern group contains comb structures with different lines and spaces from 2 to $84 \mu\text{m}$, and these three groups are placed in parallel at equal distance on the chromium mask, 2) spin-coat a layer of $8\text{-}\mu\text{m}$ -thick resist NT-90 on a silicon substrate, 3) place the photomask on the photoresist with a small tilting angle of 0.3° , so that these test structures at different locations on the photomask will have different air gaps to the photoresist, as shown in Fig. 5, 4) full-field UV exposure at the dose of $220 \text{ mJ}/\text{cm}^2$, 5) bake and develop, and 6) measure the resolvable minimum feature sizes by studying the defined features with optical microscopy and scanning electron microscopy (SEM). All the patterns go through the same exposure and development simultaneously. Fig. 5 shows the schematic of the mask design and exposure experimental setup. The gap distances between the mask and the photoresist are $30 \mu\text{m}$ (d_1), $60 \mu\text{m}$ (d_2), and $90 \mu\text{m}$ (d_3) for the three different groups, respectively. A high pressure mercury UV light source with collimated i-line output is employed in the experiment. The minimum lines and spaces achieved in our experiments are 7 , 10 , and $12 \mu\text{m}$ for gaps at 30 , 60 , and $90 \mu\text{m}$, respectively. Fig. 6 shows the microscope image of a comb structure with lines and spaces of $7 \mu\text{m}$ fabricated on an $8\text{-}\mu\text{m}$ -thick photoresist at the air gap of $30 \mu\text{m}$. It is also found that the contrast of line edge deteriorates as the gap distance increases. When the photomask is laid down onto the photoresist

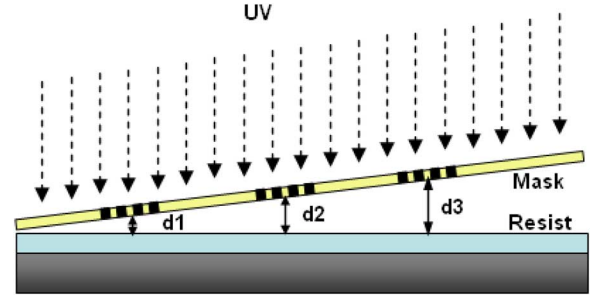


Fig. 5. Schematic of mask design and experimental setup for UV exposure at different air gaps.

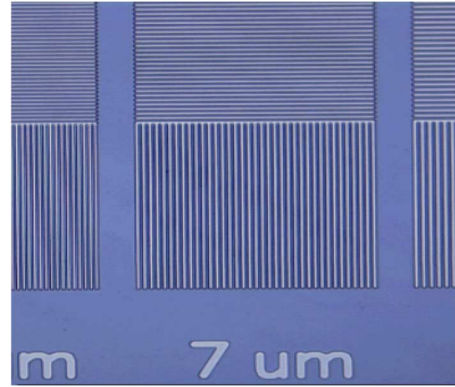


Fig. 6. Optical micrograph of fabricated comb structures with equal line width and space. $7 \mu\text{m}$ lines and spaces are resolved on an $8\text{-}\mu\text{m}$ -thick photoresist at a gap of $30 \mu\text{m}$ by using i-line UV lithography.

in the contact mode, i.e., the air gap is almost zero, $5 \mu\text{m}$ line and space is achieved. Feature sizes less than $6 \mu\text{m}$ are difficult to recognize under an optical microscope, thus, SEM pictures are used for evaluation of such structures.

The Fresnel's diffraction theory predicts a square root relationship between the minimum definable feature size L_{\min} of a periodic structure and the product of the wavelength λ and the air gap d between mask and wafer [10]. Considering the thickness of the photoresist, the minimum achievable L_{\min} can be expressed as [11]

$$2L_{\min} = k\sqrt{\lambda(d + T/2)} \quad (1)$$

where T is the thickness of the photoresist. The proportionality factor k is usually determined experimentally. If small tolerances of exposure and development in the photoresist are allowed, k is given a value of 3 [12]. Based on this assumption, the following expression of L_{\min} is now widely used

$$2L_{\min} = 3\sqrt{\lambda(d + T/2)}. \quad (2)$$

Given the optimized fabrication recipe for NT-90 photoresist and the facilities and environment in our substrate clean room, the factor k determined from our experimental data is 4. Thus, in our experiment, L_{\min} is expressed as

$$2L_{\min} = 4\sqrt{\lambda(d + T/2)}. \quad (3)$$

The difference of proportionality factor k in (2) and (3) is the overall consequence of the entire fabrication factors, such as,

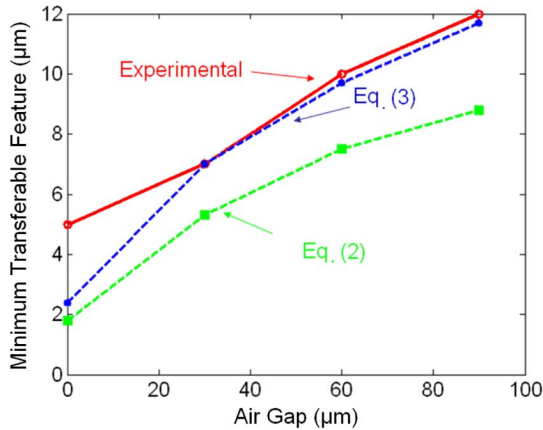


Fig. 7. Calculated (dash lines) and fabricated minimum (solid) line and space L_{\min} at various air gaps between the photomask and the photoresist on an $8\ \mu\text{m}$ thick NT-90 photoresist under UV exposure.

the difference in sensitivity of the chosen photoresist, properties of the collimated UV light, and the mechanical stability of the exposure system. Fig. 7 shows the curves of experimental minimum transferrable feature sizes and corresponding calculated value, according to (2) and (3) at different air gaps. The experimental data agree well with (3), except at the zero air gap. The big size difference at the contact mode can be explained by the process effect. In general, the aspect ratio of features that can be developed for most resists is 1:1. In this experiment, the thickness of the photoresist is $8\ \mu\text{m}$. If $2\ \mu\text{m}$ line and space needs to be resolved, the aspect ratio will be 4:1. It becomes harder to remove the thick unexposed polymer with high aspect ratio in the development process. The finest line and space that we obtained is $5\ \mu\text{m}$ (with the aspect ratio of 1.6:1).

IV. METALLIZATION TECHNIQUES FOR FINE COPPER LINE FORMATION

Photoresists, dry film, or liquid, are used for image transfer from photomasks to substrates [13]. A dry film is supplied as a three-layer sandwich with a polyester cover layer and a polyethylene separator sheet. This stack provides a reliable imaging system with a suitable resolution and a simple process for high volume production. The dry film has been the dominant process for the image formation in the packaging and PCB industry. In general, the minimum line and space that can be formed is about $1.2 \sim 1.5$ times the thickness of the resist in a manufacturing environment and down to $0.7 \sim 1.0$ in a laboratory. The thinnest dry film photoresist currently provided at production volume is $15\ \mu\text{m}$ (i.e., 0.6 mil). Therefore, the finest circuit traces that can be fabricated by using dry film photoresist is about $18 \sim 22\ \mu\text{m}$ in production and $10 \sim 15\ \mu\text{m}$ in the laboratory. Liquid photo-resist has higher imaging resolution ability and can be formed in any thickness. As the advanced package moves towards higher pin counters, finer pitch, and thinner profile, liquid photoresist technology should be used. As the stripes of photoresist get finer, the adhesion becomes weaker, and photoresist adhesion promoter is needed.

Two types of processes typically used for metallization are subtractive process and additive process [14]. The subtractive process utilizes chemical solution to etch copper away through

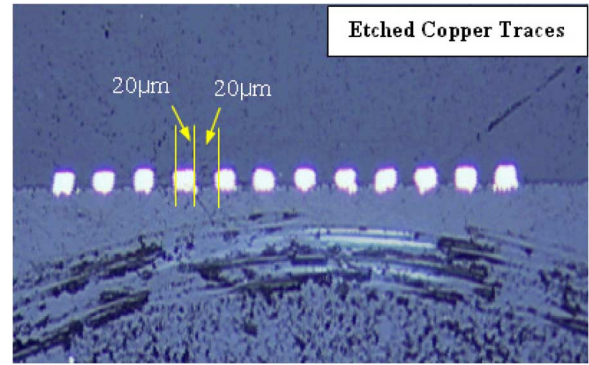


Fig. 8. Microscopic picture of wet-etched copper traces of $20\ \mu\text{m}$ line and space on a $12\text{-}\mu\text{m}$ -thick copper foil on BT laminate. Note that the etched copper traces have vertical walls, and rough surface of the copper foil limits the fine line formation by etching.

open areas of photoresist to form the circuitry. Fig. 8 shows copper traces of $20\ \mu\text{m}$ feature size by etching $12\ \mu\text{m}$ clad copper foil with subtractive process on a Bismaleimide-Triazine (BT) laminate board. Note that the etched copper traces have sharp vertical walls and equal line and space widths. Further reduction of the copper line width is limited by the roughness of the bottom surface of the copper foil. Additive process utilizes electrolytic plating to fill copper in the patterned photoresist (pattern plating). Electrolytic plating requires a thin conductive layer as electrode, called the seed layer. There are two ways to provide the electrode: 1) a very thin copper foil, e.g., $3\ \mu\text{m}$, using resin coated copper (RCC) technology [15], or 2) electroless copper plating [16] ($0.5\ \mu\text{m}$ thick) on resin. The additive processes 1) and 2) actually are semi-additive processes (SAP) [17]. The SAP consists of dielectric film surface treatment [16], a thin layer of conductive layer (seed layer) formation, photoresist application, UV exposure, development, and electrolytic plating. The surface treatment usually uses permanganate etching to create topography of the resin, especially for epoxy. For some advanced dielectrics, plasma is used to micro-roughening of the resin or a combination of the two methods. The created topography and micro-roughening of resin greatly increases the surface area that results in the enhancement of adhesion of plated copper on the resin. The thin layer of conductive layer is typically formed by electroless copper plating in the PCB and packaging substrate fabrication. After copper is plated to a designed thickness, the photoresist is stripped away and the seed layer is etched off. This technology is currently well used in high density packaging substrates and the PCB industry. The method of SAP-II has the advantages of achieving fine feature copper lines and high traces definition since only a half micron copper seed layer needs to be removed. The minimum line width achieved depends on the minimum size of the photoresist structures and the quality of process controls.

We have produced $10\ \mu\text{m}$ copper lines and spaces by using dry film photoresist in the Next Generation Substrate Laboratory of the Packaging Research Center (PRC) at Georgia Tech. Fig. 9 shows four pairs of copper traces with lines and spaces of 10 , 15 , 20 , and $25\ \mu\text{m}$ on an ajinomoto build-up film-based (ABF-based) BT substrate by using a dry film DuPont photoresist (MAX5015) with the thickness of $15\ \text{m}$. The developer

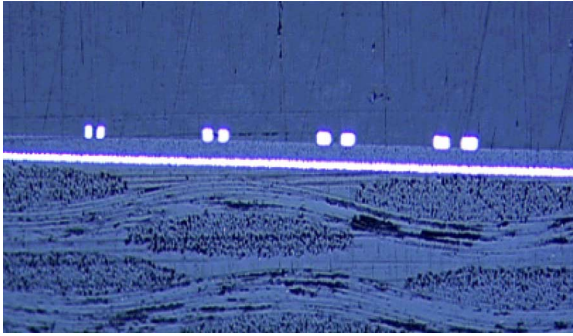


Fig. 9. Microscopic picture of plated copper traces with line width and space width of 10/15/20/25 μm on an ABF/BT substrate by using a dry film photoresist provided by DuPont. The copper thickness is 18 μm .

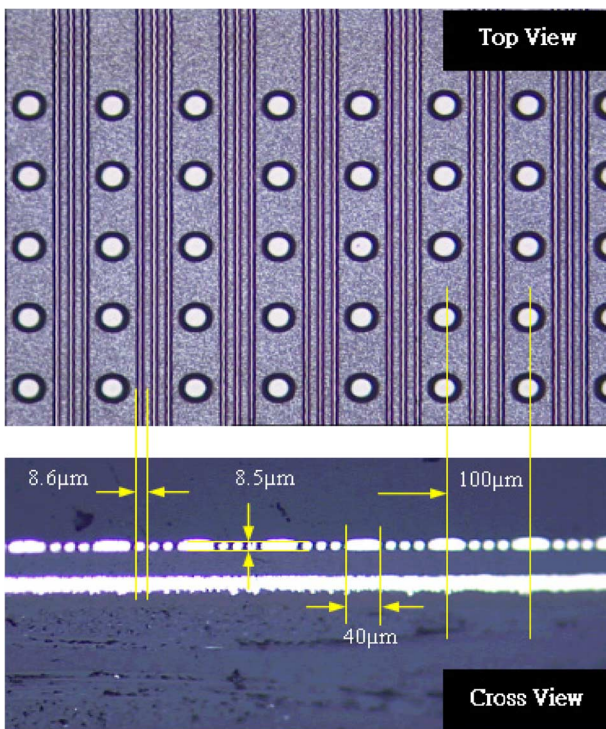


Fig. 10. Microscopic picture of the ultra-fine line routing on ABF build-up for flip chip with 100 μm pitch. Bonding pad size is 40 μm in diameter. Line and space is 8.6 μm ; three lines are routed within a pitch; and copper thickness is 8.5 μm . Routing capability is four rows per pitch and 10 000 Pads/ cm^2 .

of the DuPont photoresist is 0.8%–1.0% disodium carbonate. The copper traces with the thickness of 18 μm are plated using SAP II.

Fig. 10 shows the top view and the cross section of flip chip mounting pad structures and routing lines on an ABF/BT substrate by using the SAP II process. The pad diameter is 40 μm and the pitch is 100 μm . Also, there are three metal lines routed in the pitch. The space between the adjacent pads is 60 μm , so the minimum routing line width is less than 8.6 μm . The routing capability of 4 rows per pitch and 10 000 pads/ cm^2 can be achieved. Copper thickness measured is 8.5 μm . The aspect ratio is 1:1. With process optimization, it is possible to form line and space widths down to 5–6 μm with the SAP II process.

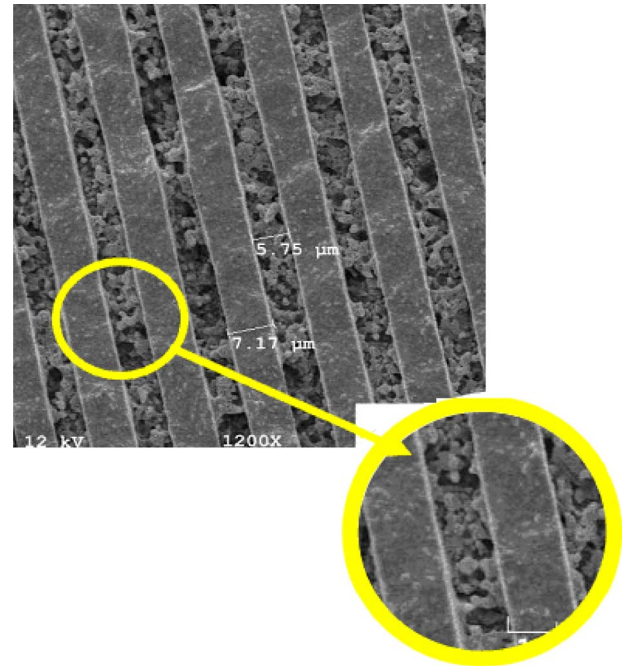


Fig. 11. SEM micrograph of copper traces with 7 μm lines and 6 μm spaces on an ABF/BT substrate. The lower right shows a close look of the copper traces and the dielectric surface.

Fig. 11 shows a SEM picture of copper lines with 7 μm line widths and 6- μm -wide spaces. Again, the dielectric film is ABF, and the substrate is glass fiber reinforcement BT laminate.

In order to improve SAP plated copper adhesion to the dielectric surface and enhance catalyst adsorption, micro-roughening the dielectric is required. The complex dielectric surface structure under the copper lines is shown in the magnified picture in Fig. 11. It consists of particles embedded in the resin. The particles are fillers added to the resin for reducing the coefficient of thermal expansion (CTE). The micro-roughness is formed due to the permanganate etching during the chemical besmear process. The micro-roughness interlocks the plated copper to make the bond strength as high as more than 1 kg/cm. However, the surface topography and roughness creates a big challenge to fine line and space formation. During development, the photoresist may lift off the particles and leave residues in the recessed areas. It becomes difficult to form the circuitry traces when the filler size becomes comparable to the line and space size. Another factor that will affect the fine line lithography is an undulating surface. The undulating surface is often caused by the buried copper traces. The unexposed photoresist is easily washed off on the convex areas and is difficult to wash off from the concave areas on the undulating surface during development. A smooth and flat surface is necessary for ultra fine line lithography.

V. CONCLUSION

The theoretic analysis based on Fresnel diffraction indicates that the key factors that hinder the finer feature size formation is the air gap between the photoresist and the mask. To experimentally study the dependence of the minimum transferable feature

size on the air gap, we designed a simple and unique experiment that guarantees the same resist thickness and the same optimized fabrication process for the group samples under different air gaps. The experimental data confirm the validity of the theoretic analysis. We also showed that an expression for the minimum transferable feature size is obtained from the experiments. Furthermore, we explored the metallization techniques for fine copper line formation, and demonstrated 8.5- μm copper line routing substrates by using semi-additive metallization process in the PRC at Georgia Tech. We believe that this investigation on the Sub-10 μm copper routing circuitry technique is important and fundamental for the future flip chip substrate packaging.

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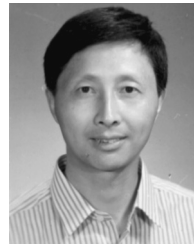
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Mr. Liu has received Global Collaboration Award by NSF-PRC, Outstanding Contributions and Service-Award to the NSF-PRC Programs. He has received numerous professional national level awards in China. He has published over 100 papers. One of them was voted as "Favorite American Journal of Physics (AJP) Paper since 1933" and listed in the AJP All Star list.



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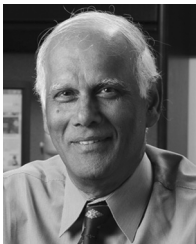
He is presently Director of Product Design and Development at The Center for Assistive Technology and Environmental Access, Georgia Institute of Technology, Atlanta. Supported by NIH, NIDDR, and NSF, his main research interest is design planning and management. Simultaneously, he is developing devices in the fields of rehabilitation engineering and healthcare. One of his original, influential works was to introduce design structure matrix methodology as a quantitative tool to plan the product environment for disabled people and hospital patient rooms. He has developed more than ten products from 2005 to present, which are patented and being licensed.



Venky Sundaram (M'10) received the B.S. degree in metallurgical engineering from IIT Mumbai, Mumbai, India, and the M.S. and Ph.D. degrees in materials science and engineering from the Georgia Institute of Technology, Atlanta.

He is the Director of Research at the Packaging Research Center (PRC), Georgia Tech and also serves as the Program Manager for the Silicon and Glass Package Consortium. He has been with the PRC since 1997 focusing on system-on-package technology, ultra-high density substrates and systems integration research. He is advising iNEMI on the new wiring density initiative. He is a co-founder of Jacket Micro Devices, an RF substrate and module Georgia Tech PRC Spin-off Company acquired by AVX. He has several U.S. and international patents and has more than 100 publications in the systems packaging technology space.

Dr. Sundaram has won several best paper and poster awards and serves as session Chair for advanced packaging topics at international conferences. He is a member of the IEEE CPMT Technical Committee of High Density Substrates.



Rao R. Tummala (F'94) is a Distinguished and an Endowed Chair Professor in Electrical and Computer Engineering and in Materials Science and Engineering at the Georgia Institute of Technology, Atlanta. He is also the Founding Director of an NSF Engineering Research Center (ERC) called the Microsystems Packaging Research Center (PRC) pioneering Moore's Law for Systems by his system-on-package vision. The PRC has been one of the largest and most comprehensive academic micro-systems packaging research, education, and

industry collaboration centers involving more than 100 students and 15 faculty from Electrical and Computer Engineering, Mechanical Engineering, Chemical Engineering, and Materials Science and Engineering Departments, and 70 global companies from the U.S., Europe, and Asia. He is also an Eminent scholar for the State of Georgia. Prior to joining Georgia Tech, he was a Fellow at IBM Corporation where he invented a number of major technologies for IBM's products for displaying, printing, magnetic storage, and packaging. He was the lead materials scientist pioneering the industry's first plasma display in the 1970s and technical leader for the industry's first low-temperature, co-fired ceramic (LTCC) in 1980s. He published over 400 technical papers, holds 71 U.S. patents and inventions, and authored the first modern reference book called *Microelectronics Packaging Handbook* in 1988, and the first undergraduate textbook in 2001.

Prof. Tummala has received 30 academic, industry, and professional society awards. He is a fellow of the IEEE, IMAPS, and the American Ceramic Society; a member of the National Academy of Engineering, and was the President of the IEEE-CPMT Society and the IMAPS Society.



Ali Adibi (SM'08) was born in Shiraz, Iran, in 1967. He received the B.S.E.E. degree from Shiraz University, Shiraz, Iran, in 1990, the M.S.E.E. degree from the Georgia Institute of Technology, Atlanta, in 1994, and the Ph.D. degree from the California Institute of Technology, Pasadena, 1999. His Ph.D. research resulted in a breakthrough in persistent holographic storage in photorefractive crystals.

He is a Professor in the School of Electrical and Computer Engineering and the Director for the Center for Advanced Processing-tools for Electromagnetic/acoustics Xtals (APEX) at the Georgia Institute of Technology, Atlanta. He worked as a postdoctoral scholar at the California Institute of Technology from 1999 to 2000. He has been an Assistant Professor from 2000 to 2004 in the School of Electrical and Computer Engineering at the Georgia Institute of Technology, where he is now an Associate Professor. His research interests include integrated nanophotonics, reconfigurable integrated photonic structures, lab-on-chip bio and chemical sensing, holographic data storage, phononic crystal structures and acoustic metamaterials, design, characterization, and applications of photonic crystals for chip-scale WDM and biosensing; spectrometers for bio and environmental sensing; high resolution optical imaging for biomedical applications; ultra-dense and ultra-fast optical interconnects; and optical communication and networking. He is a member of the editorial board for Springer Optical Science series, and a topical editor for *Applied Optics*.

Dr. Adibi has been the Conference Chair for the "Photonic Crystal Materials and Devices" conference in the Photonic West Meeting since 2001, and the Program Chair for the "Nanotechnology" program in the Photonic West Meeting since 2002. He has served as a technical committee member for several conferences organized by IEEE, Optical Society of America (OSA), and The International Society for Optical Engineering (SPIE). He is the recipient of numerous awards including the Presidential Early Career Award for Scientists and Engineers (PECASE, from the White House), the Packard Fellowship (from the David and Lucile Packard Foundation), the NSF CAREER Award (from National Science Foundation), the Technology Achievement Award from the International Society for Optical Engineering (SPIE), the SCEEE Young Faculty Development Award (from the Southeastern Center for Electrical Engineering Education), the NASA Space Act Award (from NASA), SPIE's Young Investigator Award, Outstanding Junior ECE Faculty Award (from Georgia Tech), Howard Ector Outstanding Teacher Award (from Georgia Tech), Richard M. Bass Outstanding Teacher Award (from Georgia Tech), Charles H. Wilts Prize from Caltech (best EE thesis of the year), New Focus Student Award from the Optical Society of America, Top Student (D. J. Lowell) Award from SPIE, and the Oscar P. Cleaver Award from Georgia Tech (Outstanding EE graduate student of the year). He is a member of OSA and SPIE. He is also the Chair of the IEEE LEOS Atlanta Chapter.