

FREQUENCY DIVIDERS DESIGN FOR MULTI-GHz PLL SYSTEMS

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FREQUENCY DIVIDERS DESIGN FOR MULTI-GHz PLL SYSTEMS

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SUMMARY

A programmable digital frequency divider suitable for millimeter wave Phase-Locked Loops (PLL) applications implemented in a 90 nm standard CMOS process has been presented. The frequency divider architecture features 4 parallel divider chains, each one of them implementing a single division ratio. The desired frequency division ratio is then selected using the two control bits of an output 4 to 1 multiplexer. To the extent of maximizing the frequency of operation, each frequency divider block has been realized using dynamic precharge-evaluation logic. The design of an improved dynamic logic D-FF is presented, and an alternative technique to implement high speed non-power-of-2 division ratios is considered. Post-layout simulations have shown a maximum operating frequency of 5 GHz with a power consumption of 7.14 mW from a 1V supply. The maximum speed of operation is also dependent upon the voltage supply, showing a higher maximum input frequency when the voltage supply is increased. A list of claim and innovations is presented in the conclusion, and recommendations for future work are presented as well.

CHAPTER 1

INTRODUCTION

During the past 10 years, the connectivity features of electronic devices have seen a tremendous expansion. This phenomenon can be explained by considering different points of view. On one side, the improvement of the microelectronics processes, especially for complementary metal oxide semiconductor (CMOS) technology, allowed a drastic reduction of the power consumption, and an increase of the maximum operating frequency at which active devices can operate. This two combined factors allowed the integration on a single silicon die of both digital signal processing at base-band, and radio frequency signal conditioning, filtering and amplification at frequencies up to several gigahertz. The possibility of integrating all the functionalities of a full wireless transceiver on a single chip, allowed a consistent cost scaling and a reduction of the silicon die area compared to compound semiconductors technologies. Under this point of view, the technology improvement created a new space into the market for new possible applications, and the phenomenon can be seen as “technology driven”. Under another perspective, the need for high-speed and flexible communication systems, can be seen as something required by the every day growing global society, for both business and personal uses. It’s difficult to make a definitive statement on what perspective should be

adopted on this point, but one result of the high speed wireless networks diffusion, is the overcrowding of the electromagnetic spectrum. An increasingly number of new standards and regulations (FCC in the United States), allows the efficient use of the available frequency spectrum, and intelligent channel access techniques (like CDMA, WCDMA, etc.) permit the simultaneous use of common frequency bands by multiple users. Nonetheless, the newest wireless applications (like high-quality video streaming) are extremely demanding in terms of bandwidth. To face this problem, the allocation of new frequency bands has been necessary, and the frequency spectrum in the multi gigahertz range has been allocated. Inside this category of new frequency bands, the 7 GHz wide spectrum around 60 GHz (IEEE 802.15 WPAN standard) is one of the newest and more promising. The challenges in 60 GHz radio applications are several, like the high attenuation in the air due to the oxygen absorption peak, and the difficulties in operating inexpensive technologies (like CMOS) at such high frequencies (lossy substrate and low transconductance devices). The recent scaling of CMOS processes down to 90-65-45 nm, allowed the operation of standard Si-CMOS processes at frequencies above 60 GHz, and the remaining limiting factor that the CMOS technology is still facing is the maximum output power delivered to the transceiver antenna. However, since the 60 GHz radio is mainly intended for short-range applications (short-range radar and wireless personal area networks), this last consideration is not that an issue. Consequently, several realizations of 60 GHz integrated transceivers have been proved to work, and have been recently published in the technical literature [1], [2].

In the overall transceiver system architecture, the frequency synthesis from a fixed reference frequency (i.e. from a crystal oscillator) is an essential building block.

Because of its better noise performances compared to other solutions (i. e. direct frequency synthesis), and channel selection availability through the loop division ratio modulation, the phase lock loop (PLL) frequency synthesis is the natural choice for such an application.

This work is intended to focus on the frequency synthesis problem at multi gigahertz frequencies. Specifically, the design of a programmable frequency divider chain for a PLL frequency synthesizer is taken into consideration. The purpose of the presented programmable divider is to enable frequency-channel selection capability in a PLL frequency synthesizer system. The maximum input frequency for this device is up to 5 GHz with 7.14 mW power consumption with 1 V voltage supply, while the available division ratio ranges from 24 to 27 in unity steps.

CHAPTER 2

MULTI-GHz FREQUENCY SYNTHESIS

2.1 – Phase-Locked Loop Frequency Synthesizers

The implementation of the frequency synthesis in a multi GHz application is often performed closing a voltage controlled oscillator (VCO) into a loop, to the extent of phase-locking the output frequency to an input reference frequency signal. The reason for that, is that there are no practical means to generate a pure (in terms of phase noise) and stable (frequency drift free) reference frequency above few GHz. Such a feedback system, able to lock a high frequency VCO output to a much lower reference frequency signal, is called phase locked loop (PLL) [3]. The typical arrangement for a PLL system is shown in Fig. 1.

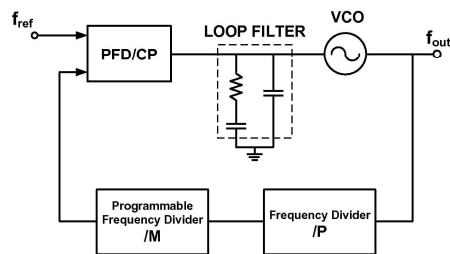


Fig. 1. Typical PLL system architecture.

To describe the behavior of a PLL frequency synthesizer, a linearized model is often used. Moreover, to the extent of emphasizing the phase-locking mechanism, the phase domain is chosen for the analysis. In order to proceed with the analysis, each building block of the PLL needs to be modeled in the phase domain.

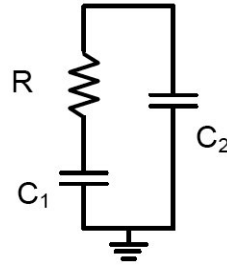
The *phase-frequency detector (PFD)* can be interpreted as a functional block having the output signal proportional to the phase difference between the two input signals. The proportionality factor is set to be 1 (unitless).

The *charge-pump (CP)* can be modeled as a trans-conductive block, transforming the phase difference into a proportional current. The proportionality factor k_ϕ is defined as follows:

$$\left\{ \begin{array}{l} k_\phi = \frac{I_p}{2\pi} \quad \left[\frac{\mu\text{A}}{\text{rad}} \right] \\ I_p : \text{charge - pump maximum output current} \end{array} \right.$$

Following the loop path clock-wise, the block after the CP is the *loop filter*: its purpose is to integrate the current pulses generated by the PFD/CP blocks. The transfer function of the loop filter has the units of impedance [Ω], being the output voltage generated from the CP output current. The impedance of the loop filter will be identified with $Z(s)$. Since the loop filter must integrate the input current, its transfer function will be a low-pass type. For the purposes of this work, the second order loop filter that will be considered is the one reported below:

$$\begin{cases} Z(s) = \frac{1}{Cs} \frac{1 + \tau_1 s}{1 + \tau_2 s} \\ C = C_1 + C_2 \\ \tau_1 = RC_1 \\ \tau_2 = R(C_1 + C_2) \end{cases}$$



In the phase domain, the *voltage-controlled oscillator (VCO)* can be modeled like an integrator having a proportionality factor of k_{vco} . The proportionality factor units are [Hz/V]. The VCO transfer function will therefore be: k_{vco}/s .

Each *frequency divider* block performing a frequency division by a factor of N , will divide the phase of the input signal by N as well. Therefore, a frequency divider block can be modeled with a simple divide-by- N block.

The resulting block diagram for the linearized PLL is shown in Fig. 2.

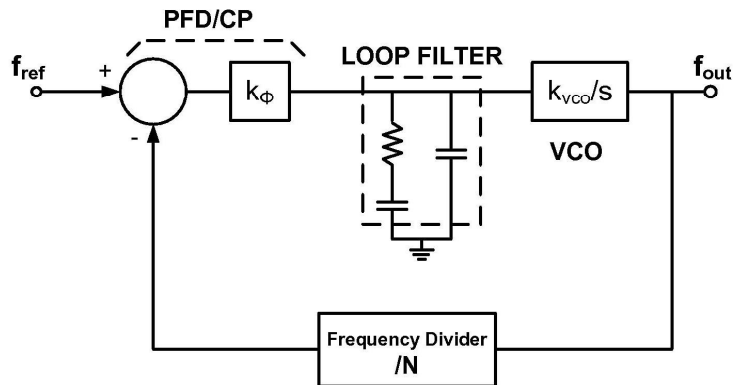


Fig. 2. Linearized PLL model.

In the phase domain, the transfer function of the PLL from the reference signal phase (θ_{ref}), to the VCO output signal phase (θ_o) is the following:

$$\frac{\theta_o}{\theta_{ref}} = \frac{\omega_o/s}{\omega_{ref}/s} = \frac{\omega_o}{\omega_{ref}} = \frac{k_\phi Z(s)k_{vco}}{s + \frac{k_\phi Z(s)k_{vco}}{N}}$$

As can be seen, the transfer function for the phases of the input/output signals, is the same as for the frequencies of the input/output signals. Applying the final value theorem to evaluate the asymptotic behavior of the system at locking ($t \rightarrow \infty$), we have:

$$\left. \frac{\omega_o}{\omega_{ref}} \right|_{t \rightarrow \infty} = \lim_{s \rightarrow 0} \frac{s \cdot k_\phi Z(s)k_{vco}}{s + \frac{k_\phi Z(s)k_{vco}}{N}} = N$$

So, the PLL performs a frequency multiplication of the input signal by a factor N . From this relationship, it is evident that if N changes to $N+1$, the output frequency f_o will increase by f_{ref} . Therefore, the programmability of the frequency divider in the feed back loop allows the output frequency to change in steps having a minimum spacing equal to the input reference frequency. If an output frequency step bigger than the reference frequency is needed, the frequency divider chain can be rearranged placing a fixed divide-by- P frequency divider stage (prescaler), in front of a programmable frequency divider stage (M). This way, the overall division ratio will be $M \cdot P$, and the output frequency step will be $P \cdot f_{ref}$.

2.2 – Frequency Dividers in Phase-Locked Loops

In modern integrated transceivers operating at microwave frequencies, one of the most critical parts is the frequency divider chain of the PLL frequency synthesizer. Being the VCO output frequency in the order of several GHz, the problem of actually implementing the frequency division at such high frequencies is a non trivial one. In fact, depending on the frequency that needs to be divided, different approaches can be used. The simplest way to implement a clock frequency division is to design a digital counter, with a digital logic resetting the counter after a number of input clock cycles equal to the division ratio have been counted. The drawback of this kind of solution is the limited maximum frequency of operation due to the digital logic with which the counter is implemented. Usually, such a frequency divider will operate up to few GHz (typically no more than 3-4 GHz). On the other side, such a frequency divider has the advantage of low power consumption, and the possibility of being programmable by dynamically changing the resetting logic (and thus the division ratio). When a higher frequency division is necessary, a purely analog solution has to be taken into consideration. The two main solutions to multi-GHz frequency division are: master-slave (MS) latch divider, and injection-locking divider (ILD). The MS divider employs a two stage regenerative divider (Fig. 3) based on analog differential latch (Fig. 4) to perform a divide-by-2 frequency divider stage.

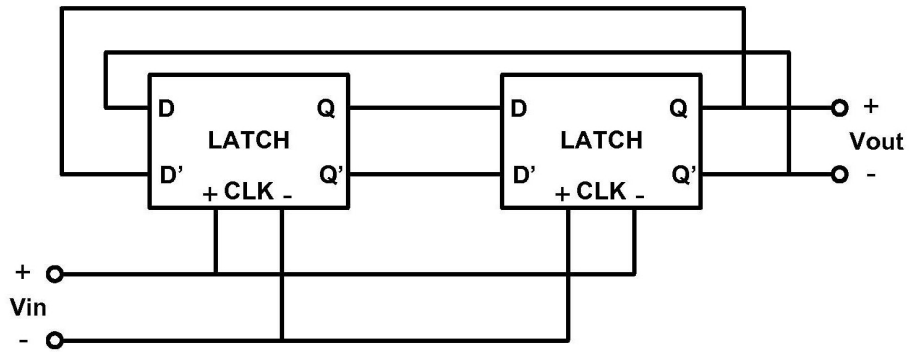


Fig. 3. Master-Slave frequency divider block diagram.

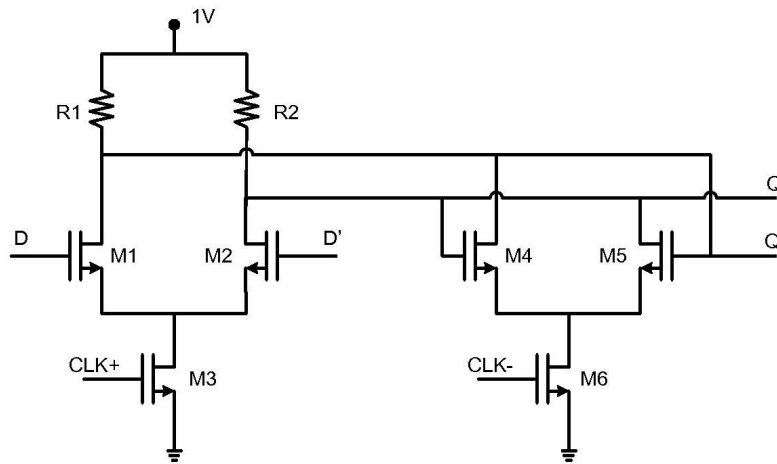


Fig. 4. D-latch possible implementation for master-slave frequency divider.

The ILD solution, instead, exploits the injection pulling effect on a VCO tuned at a frequency the half of the injected one. A possible implementation for the ILD is by means of a cross-coupled LC-tank VCO. To the extent of injecting the input differential signal, a NMOS-PMOS couple is used across the output terminal of the VCO (Fig. 5).

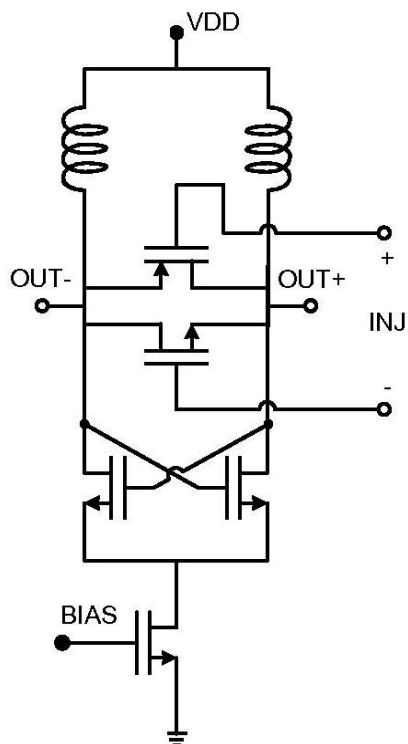


Fig. 5. Injection-locking frequency divider cross-coupled implementation.

The ILD solution allows the highest frequency of operation but, in general, offers a narrower bandwidth and higher power consumption when compared with the MS solution. In actual millimeter-wave PLL frequency synthesizers, a possible approach is to employ an ILD for the very first stage of the frequency divider chain (being the one operating at the highest frequency), and to use MS divider stages until the frequency is scaled down to values (3-4 GHz) at which a fully digital frequency divider can be used. The resulting architecture is shown in Fig. 6.

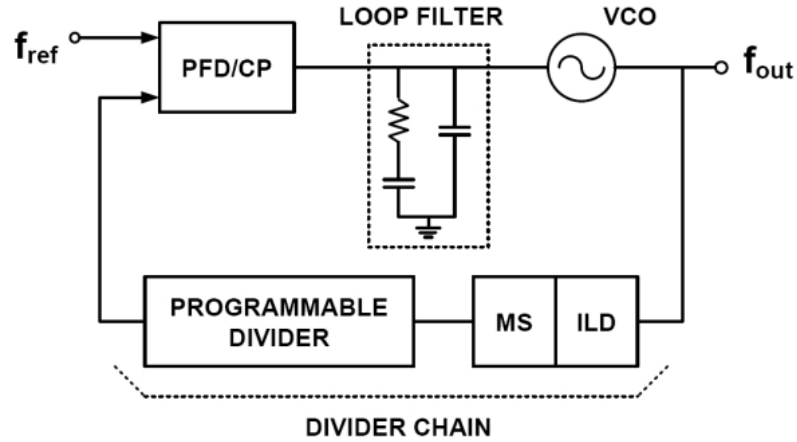


Fig. 6. Millimeter-wave PLL frequency synthesizer architecture.

In the system of Fig. 6, the digital frequency divider is indicated as a programmable divider, thus allowing a frequency channel selection capability. It is straightforward to understand that, the highest the maximum frequency of operation of the programmable frequency divider, the smaller the number of ILD/MS frequency divider stages. Moreover, the lower the number of high frequency divider stages, the lower the power consumption as well. Therefore, it is in the interest of the designer to maximize the maximum operating frequency of the digital frequency divider portion of the divider chain, in order to achieve a lower power consumption of the overall PLL. Another aspect to point out in the design economy is the area consumption of the MS/ILD blocks compared with the area consumption of digitally implemented frequency dividers. Since the ILD/MS dividers are full custom analog blocks incorporating inductors, the chip area required for their implementation is, in the most cases, wider than the area required for digitally implemented frequency synthesizer blocks. Moreover, a digital frequency synthesizer can be implemented using standard-cell libraries and

dedicated computer aided design (CAD) tools allowing a minimization of the layout area and a verification of the timing constraints.

CHAPTER 3

PROGRAMMABLE FREQUENCY DIVIDER

3.1 – Implementation of Frequency Dividers in PLLs

The implementation of channel selection in a PLL frequency synthesizer requires programmable frequency dividers operating at high frequency. The most straightforward way to implement a divide-by-2 digital frequency divider is to use a toggle flip-flop (T-FF). A possible implementation for a T-FF is shown in Fig. 7 (a).

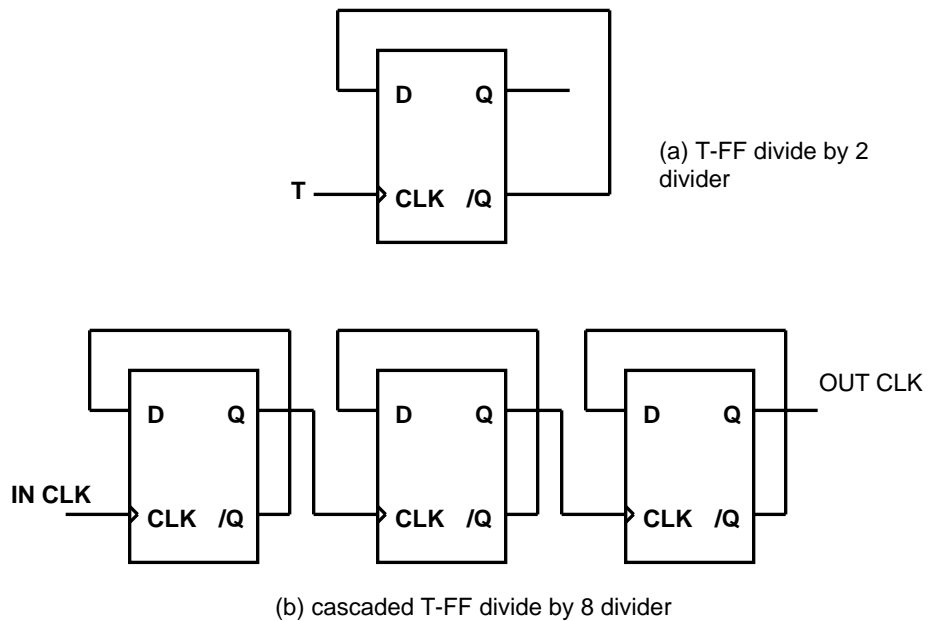


Fig. 7. Divide-by-2 T-FF (a) and derived divide-by-8 (b) structures.

As can be seen from Fig. 7 (a), a T-FF can be implemented using a D-FF feeding back the negate output /Q to the input D. The input clock to be divided is then provided at the CLK input. Cascading n T-FF stages as shown in Fig. 7 (b), it is possible to divide the input frequency by a factor of 2^n . Therefore, the limitation of this approach is that the division ratio will be constrained to be a power of 2. As already stated in Chapter 2, to the extent of switching the output frequency to the next adjacent channel, it may be needed to change the division ratio to the next integer value, requiring the programmable frequency divider to divide by a non-power-of-2 division ratio. For this reason, another approach to the frequency divider implementation is needed every time a non-power-of-2 division ratio is required.

A possible approach to divide the frequency of a clock by a non-power-of-2 division ratio is to implement a counter with an appropriate reset logic. The reset logic is needed to load the initial state (zero) every time the counter reaches a number of cycles corresponding to the desired division ratio. The block diagram for such a frequency divider implementation is shown in Fig. 8.

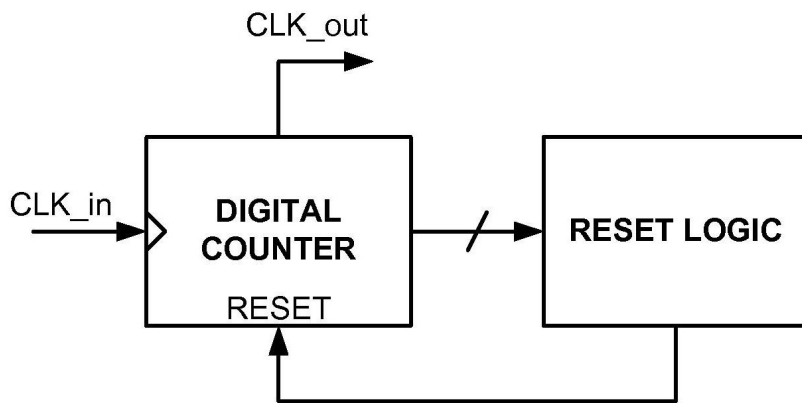


Fig. 8. Digital frequency divider block diagram.

In this work, the focus will be on the implementation of a programmable frequency divider featuring divide-by-24-25-26-27 division ratios. The architecture of the frequency divider is made up of four frequency divider chains. The desired division ratio is then selected by mean of an output multiplexer controlled by two control bits. The resulting structure is shown in Fig. 9.

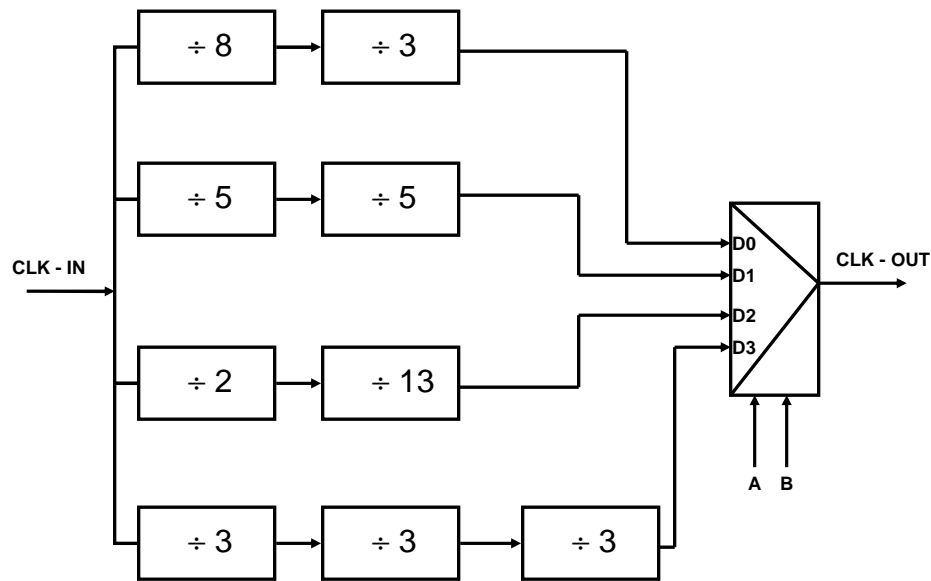


Fig. 9. Programmable frequency divider system diagram.

To the extent of better contextualize the use of the above programmable frequency divider, a 53 GHz PLL frequency synthesizer with output channel selection application is next considered. For a 53 GHz application, the very first frequency division (down to approximately 26 GHz) is usually implemented through an ILD [4], and the

subsequent fixed division ratio dividers can be implemented using a dynamic MS topology. At the end of this chain, the programmable frequency divider can be placed with less stringent maximum operating frequency requirements. As already seen in Chapter 2, this frequency scaling technique causes the minimum output frequency step to be wider than the input reference frequency by a factor equal to the fixed division ratio chain. Even though the channel spacing is set to be in the order of 2 GHz, the use of an input reference frequency in the order of tens of MHz can facilitate achieving a fixed division ratio up to 80-100.

The 53 GHz PLL architecture herein considered is shown in Fig. 10.

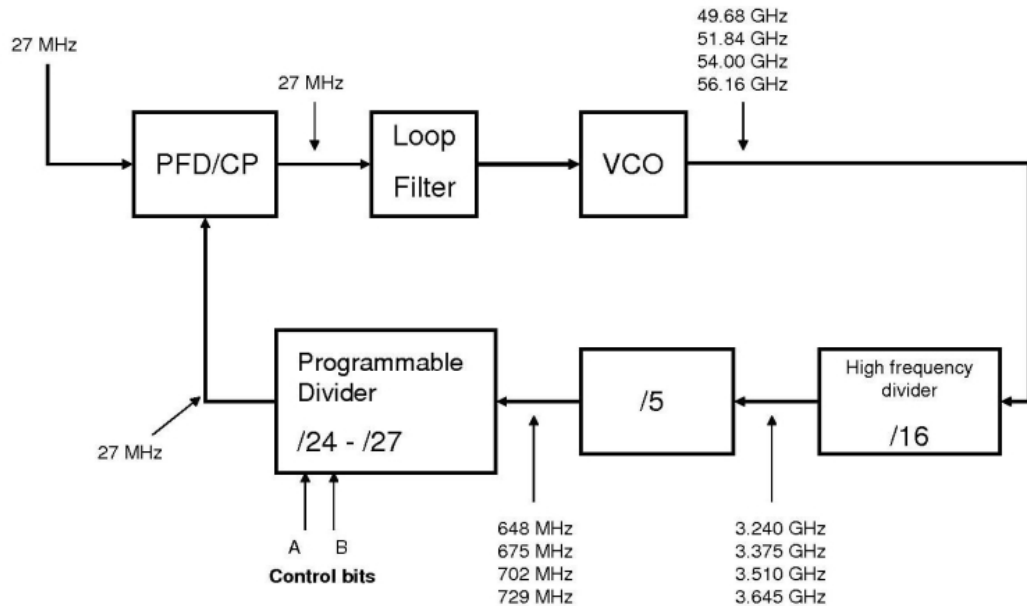


Fig. 10. 53 GHz PLL frequency synthesizer exemplifying the application of the presented programmable frequency divider.

Switching the division ratio from one value to an adjacent one, the output frequency will experience a step of 2.16 GHz, while the programmable frequency divider input frequency will range from 648 MHz to 729 MHz.

In the following sections, the operating principles, and the actual implementation of each frequency divider block used to synthesize the complete programmable frequency dividers, are reported.

3.2 – Divide-by-2 frequency divider

The divide-by-2 block is implemented using a simple T-FF. As previously stated, a T-FF can be realized using a D-FF with the negate output fed back to the data input (Fig. 7 (a)). Therefore, the core of the T-FF is a D-FF, and its maximum operating speed will set the maximum frequency that the T-FF can divide. In order to achieve the maximum possible operating frequency, it is necessary to select the appropriate implementation for the D-FF, choosing between the different circuit topologies available. Standard cells D-FF are usually implemented exploiting a positive feed back memory element, with the additional logic needed for clear, preset, and other functionalities that may be desired. A possible schematic for a CMOS D-FF is shown in Fig. 11. Such a realization for the D-FF is said to be *static*, since the memory element stores the state of the D-FF as far as the power is supplied. It is noteworthy to mention that a static random access memory (SRAM) element, exploits the same mechanism to store its logic state.

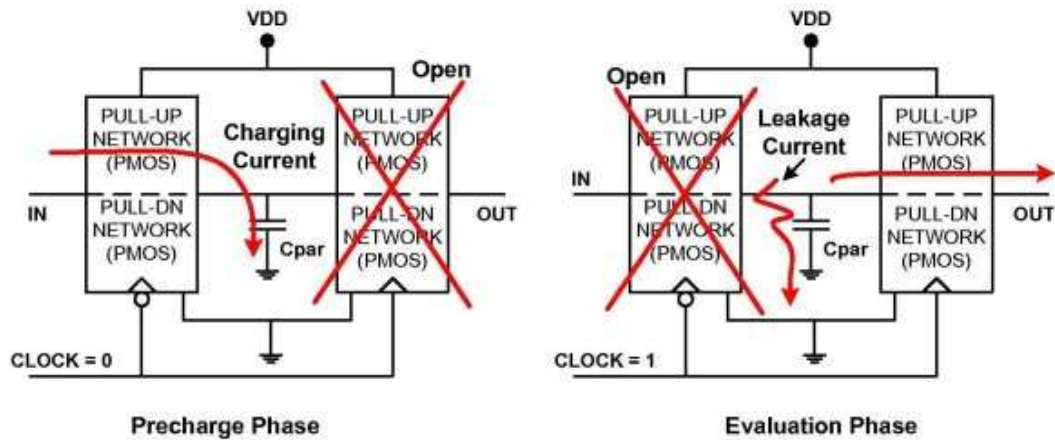


Fig. 12. Pre-charge and evaluation phases in a dynamic logic.

The circuit shown in Fig. 12 is positive edge-triggered, meaning that the input D is sampled in correspondence of the clock rising edge. The input portion of the circuit (pre-charge), is transparent when the clock is in the low state (logic 0). During this time interval, the node A is reproducing the logic value provided at the input node D. When the clock switches to the high state (logic 1), the input portion of the circuit becomes no longer transparent to the input, and the logic value stored at the node A is passed to the output node Q. Since the output Q reproduces the input value at the time the clock switches from the low state to the high state (but it could have been the opposite), this kind of logic is said to be edge-triggered.

For the purposes of this work, the selected D-FF topology is shown in Fig. 13. The presented schematic is an evolution of the D-FF proposed in [6].

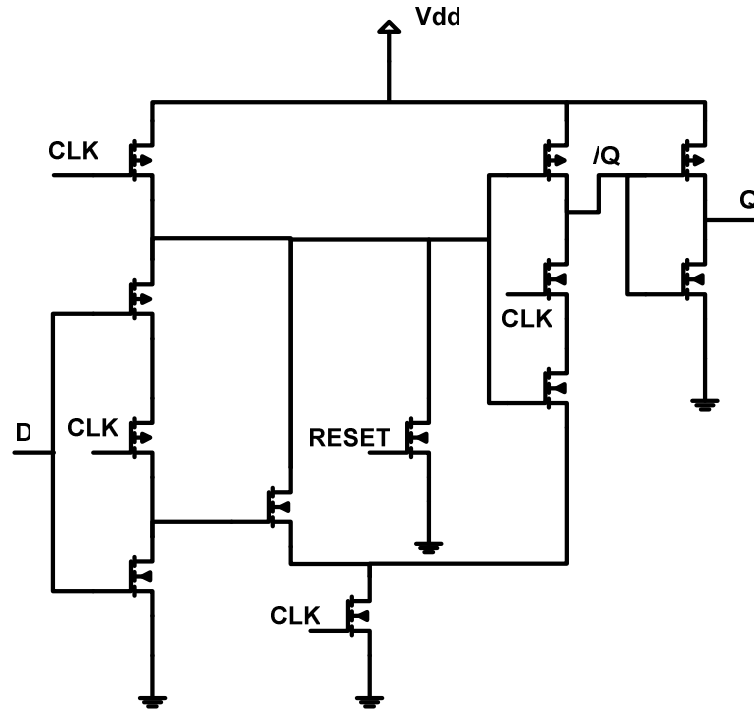


Fig. 13. D-FF implementation.

As can be seen, a fast reset is implemented with a NMOS transistor connected to the pre-charged node. In fact, being the pre-charge node a small capacitive load, a NMOS device shunted to ground can discharge the node (and therefore reset the D-FF) in few tenths ps. The layout of the D-FF implemented in a 90 nm CMOS technology is shown in Fig. 14.

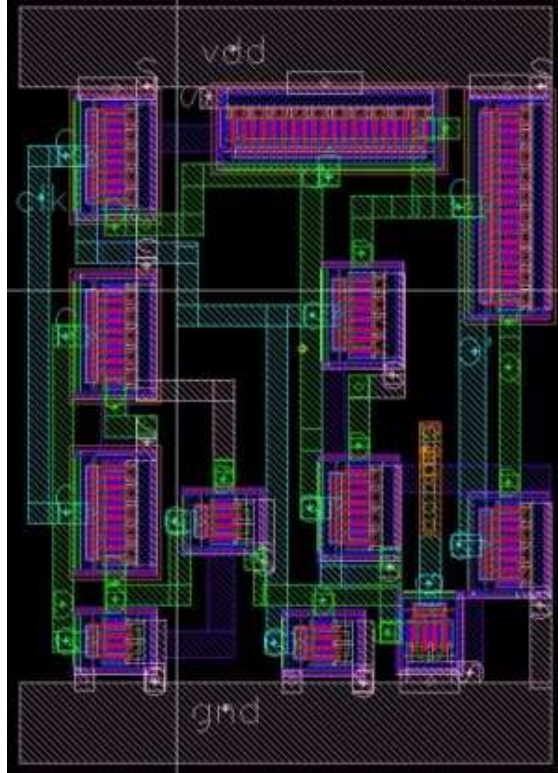


Fig. 14. CMOS dynamic logic D-FF layout.

3.3 – Divide-by-8 frequency divider

The divide-by-8 frequency divider block is realized by a simply cascading 3 divide-by-2 blocks (each one of them being a T-FF, as shown in Fig. 7 (b)). The maximum frequency of operation for this block is the same as for the divide-by-2 block, since the input stage is the one operating at the highest frequency. The final layout of the divide-by-8 block is shown in Fig. 15.

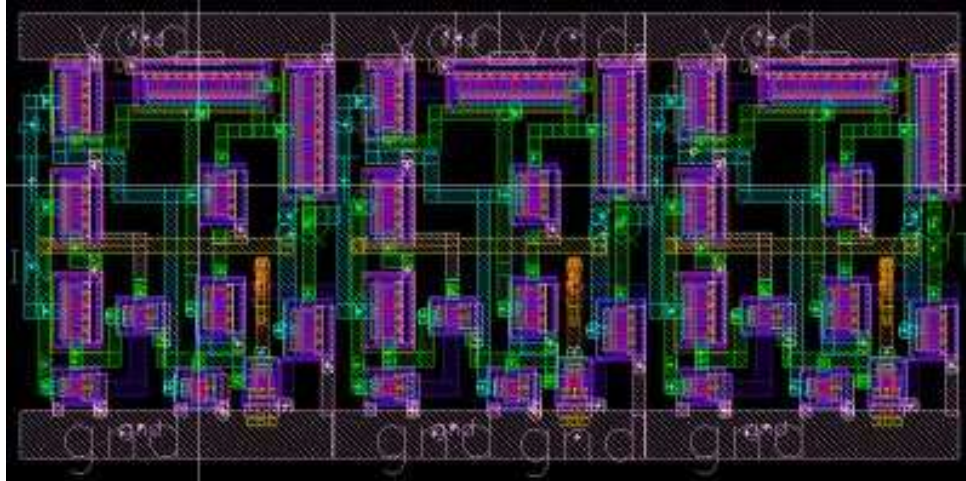


Fig. 15. CMOS dynamic logic divide-by-8 block layout.

3.4 – Divide-by-3 frequency divider

In order to divide the input clock by 3, the conventional approach of using a T-FF cannot be used. In fact, a cascaded T-FF frequency divider allows only divide by power of 2 division ratios. Other approaches are available, like the one employing a counter with reset (Fig. 8). This kind of solution, however, has the drawback of an increased complexity, since a digital counter needs to be implemented. Therefore, another approach has been chosen for the implementation of the divide-by-3 and divide-by-5 frequency dividers. The solution chosen has been first presented in [5] and exploits two main building blocks: a half-transparent register, and a D-Latch element (Fig. 16). The principle of operation of this kind of divider is to differentiate the behavior of the feedback loop depending on the output logic value. Using a half-transparent register to give different delays to the logic value 1 (1 clock cycle) and to the logic value 0 (2 clock cycles), odd division ratios can be easily obtained. Using this approach, and cascading n-

2 half-transparent registers in front of the D-Latch element, a divide-by-n frequency divider is obtained.

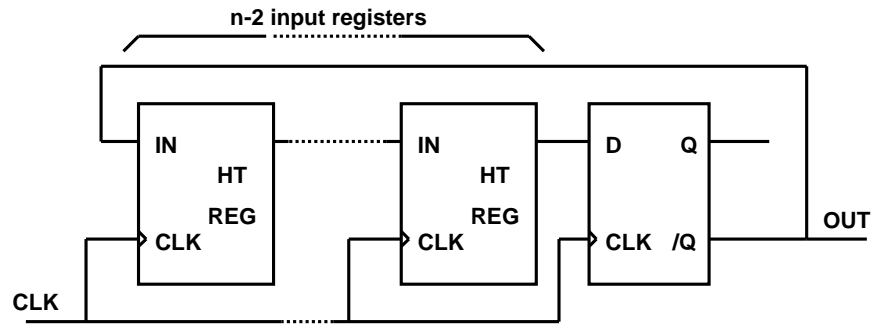


Fig. 16. Divide by n divider block diagram.

Since the division ratio equals $n-2$, the minimum division ratio that can be implemented is 3. The resulting architecture is reported in Fig. 17.

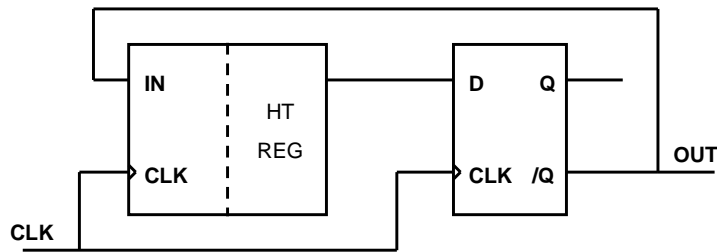


Fig. 17. Divide-by-3 block implementation.

The implementation of the half-transparent register is shown in Fig. 18, while the D-FF has been implemented following the schematic reported in Fig. 19.

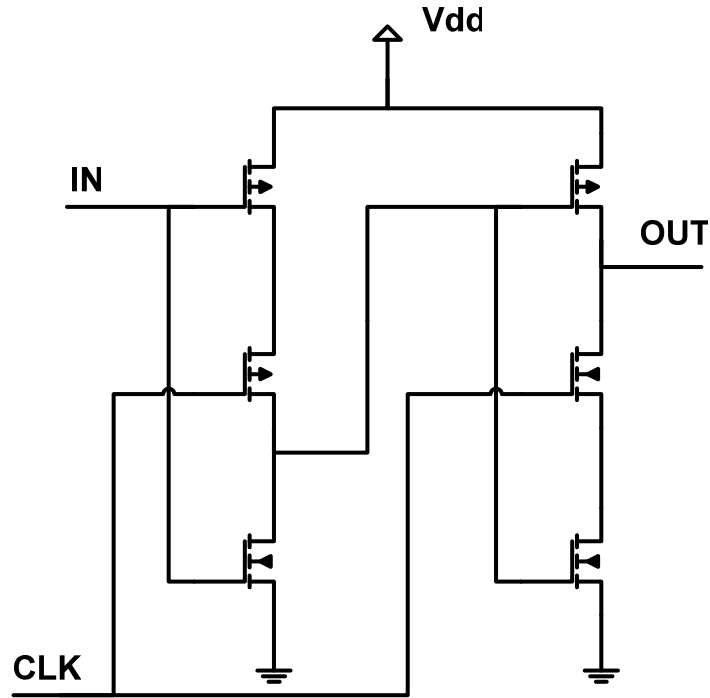


Fig. 18. Half-transparent register implementation.

The reason why the D-FF implementation of Fig. 19 differs from the one of Fig. 13, is that the former doesn't need any reset signal for proper operation of the frequency divider, while the reset signal is essential for the implementation of the frequency dividers presented in the following sections.

The layout of the half-transparent register shown in Fig. 18, is reported in Fig. 20, while the layout corresponding to the D-FF shown in Fig. 19, is reported in Fig. 21.

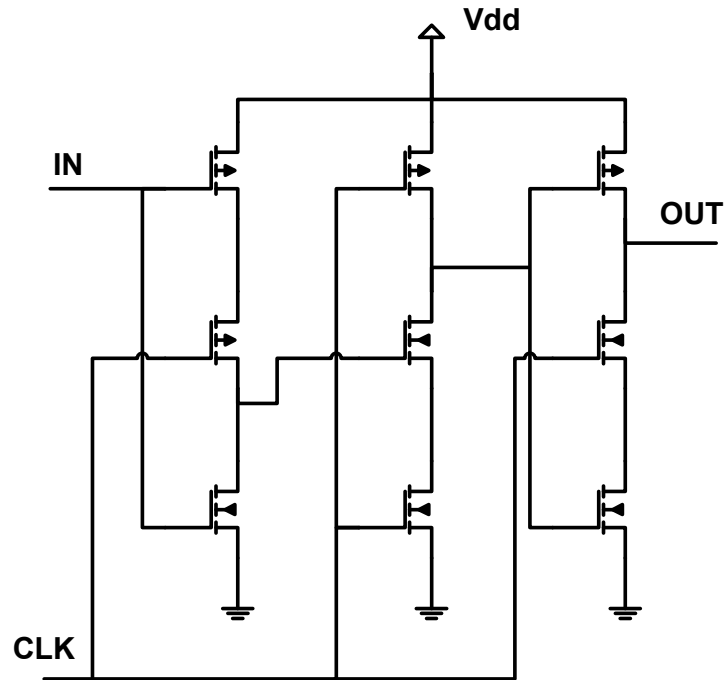


Fig. 19. D-FF implementation for divide-by-3 and divide-by-5 blocks.

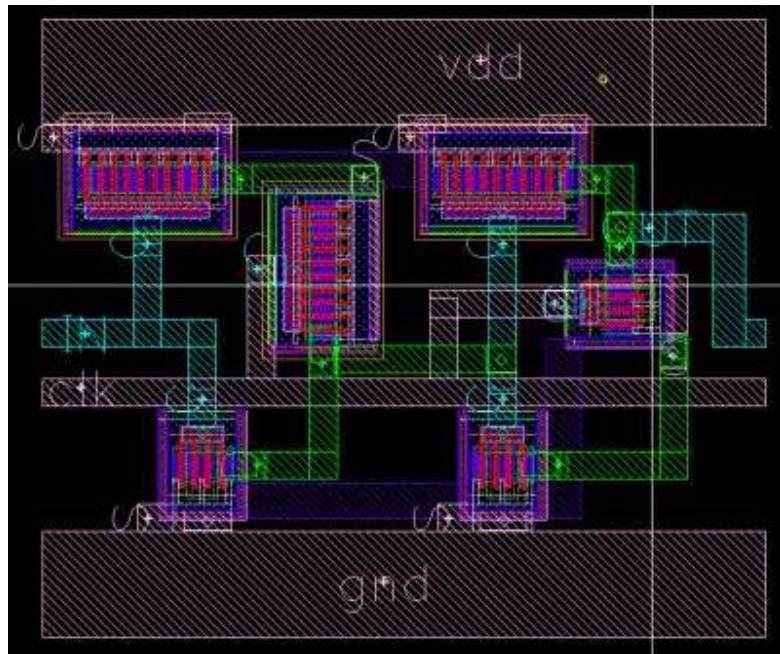


Fig. 20. Half-transparent register layout.

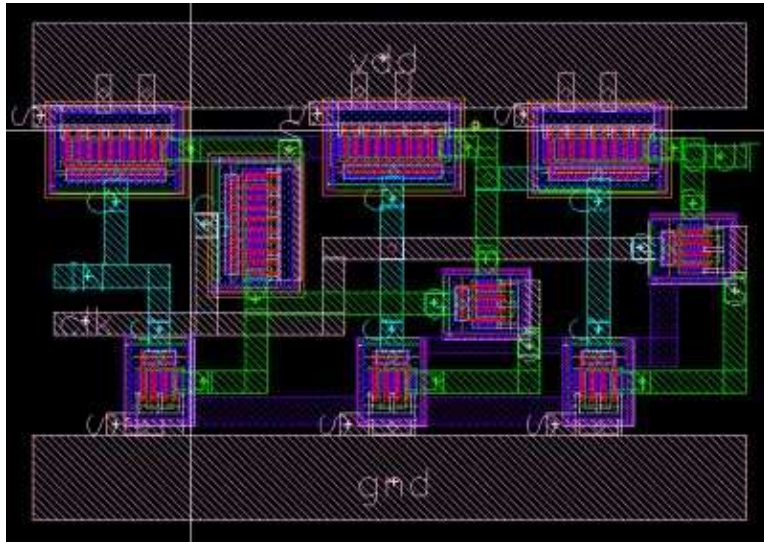


Fig. 21. D-Latch implementation layout.

The final layout for the divide-by-3 frequency divider is obtained cascading the half-transparent register and the D-Latch. In order to facilitate the connection, the two blocks have been laid out with the same height. The resulting layout is shown in Fig. 22.

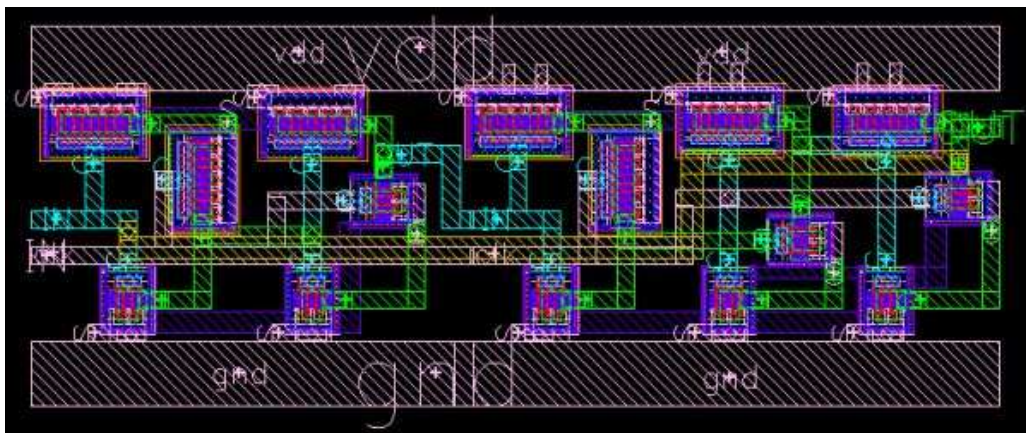


Fig. 22. Divide-by-3 frequency divider layout.

3.5 – Divide-by-5 frequency divider

The divide-by-5 frequency divider block is realized following the same architecture used for the divide-by-3 frequency divider. Therefore, the same half-transparent register and D-Latch blocks have been used. The only difference relies in the number of half-transparent registers placed in front of the D-Latch. For the divide-by-5 frequency divider, the number of stages required is 3. The resulting layout is shown in Fig. 23.

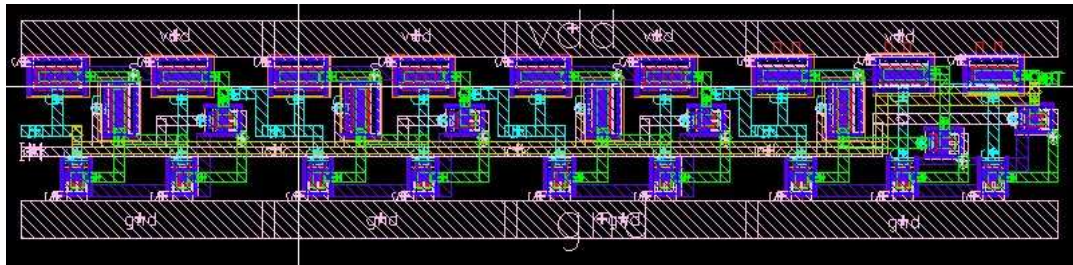


Fig. 23. Divide-by-5 frequency divider layout.

3.6 – Divide-by-13 frequency divider

The divide-by-13 divider block is implemented following the principle exemplified in Fig. 8. Therefore, the implementation of a synchronous counter with reset is required.

The approach followed to implement the frequency divider, exploits JK-FF based static digital counter. The circuit schematic for a three bits counter is shown in Fig. 24. As can be seen, the counter is made up of three JK-FF, with a simple AND gates additional logic. The principle of operation is that each JK-FF has to toggle when all the

JK-FF in front of it are set to 1. To achieve this logic functionality, the AND gates logic is exploited.

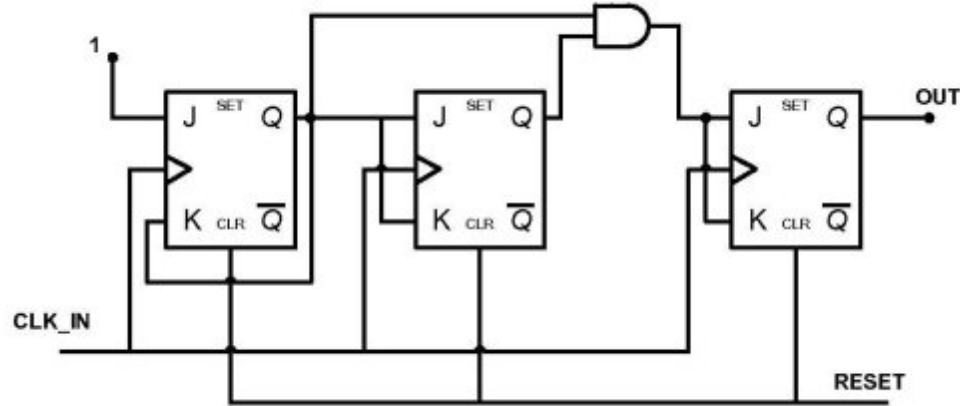


Fig. 24. JK-FF based digital counter.

In normal operation, the RESET signal is always not set (logic 0), and the counter will count all the states, starting from 0 to 2^n-1 , where n is the number of JK-FF stages. Since the frequency divider implemented with the digital counter features a division ratio equal to the number of states the counter goes through, if the division ratio N differs from 2^n , counter needs to be reset after N cycles. To this extent, an additional logic generating the RESET signal is used. In the case of the divide-by-13 frequency divider, the minimum number of counter stages is 4 ($2^4 = 16$). To the extent of maximizing the operative frequency, the RESET signal can be pipe-lined, so that the delay introduced by the recognizing logic can be as long as the clock period, without affecting the correctness of operation. The resulting divide-by-13 frequency divider is shown in Fig. 25.

As can be easily seen, a possible implementation for the additional logic necessary to implement the JK-FF functionality is the one shown in Fig. 26.

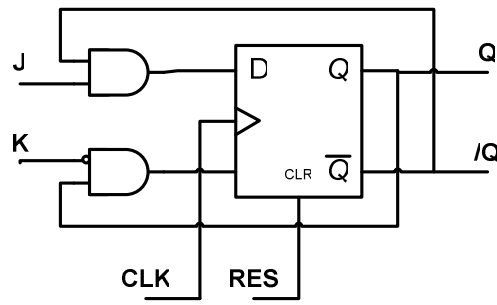


Fig. 26. JK-FF implementation with D-FF and additional input logic.

The transistor level D-FF implementation is the one reported in Fig. 13, featuring a fast RESET functionality. The resulting layout for the JK-FF is shown in Fig. 27.

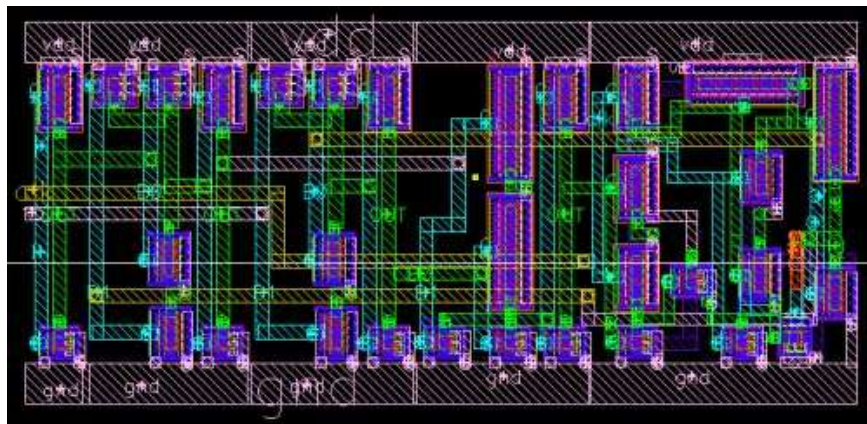


Fig. 27. JK-FF layout.

The divide-by-13 frequency divider layout is reported in Fig. 28.

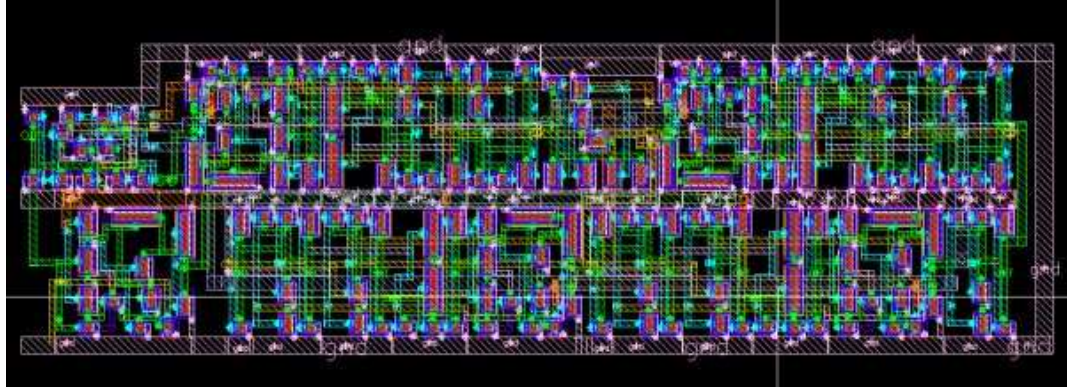


Fig. 28. Divide-by-13 frequency divider layout.

3.7 – Output Frequency Selector

The output frequency selection functionality is realized by mean of a digital multiplexer. The maximum frequency of operation for this block does not represent a relevant issue for the frequency divider, since the output frequency is the lowest in the circuit, and the performance bottleneck is likely to be represented by the input frequency dividers (divide-by-8/5/2/3). Moreover, the channel switching operations won't happen at a speed higher than few MHz, even if a channel-hopping feature needs to be implemented. Therefore, a static architecture for the output multiplexer represents a good compromise in terms of simplicity and compactness. The schematic for a possible implementation of a four-input multiplexer is shown in Fig. 29. The multiplexer final layout is reported in Fig. 30.

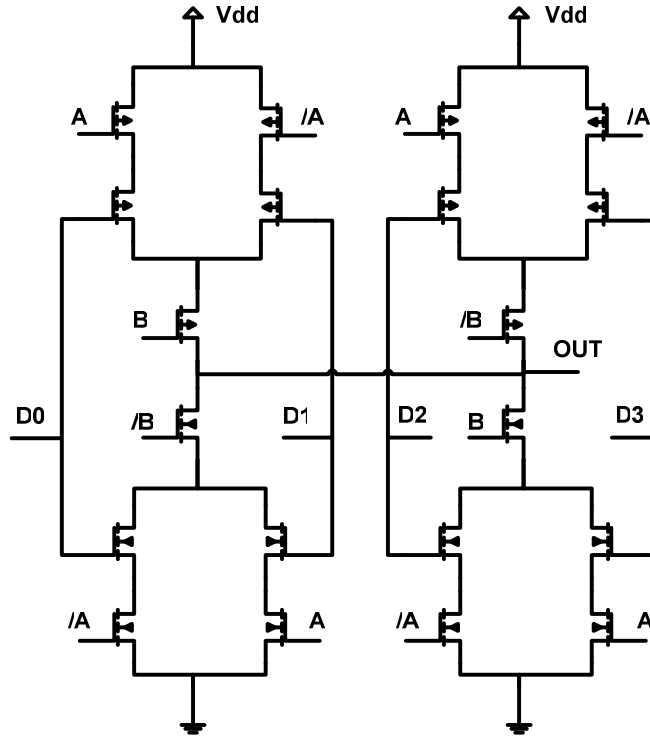


Fig. 29. Output frequency selector (4 to 1 Multiplexer) schematic.

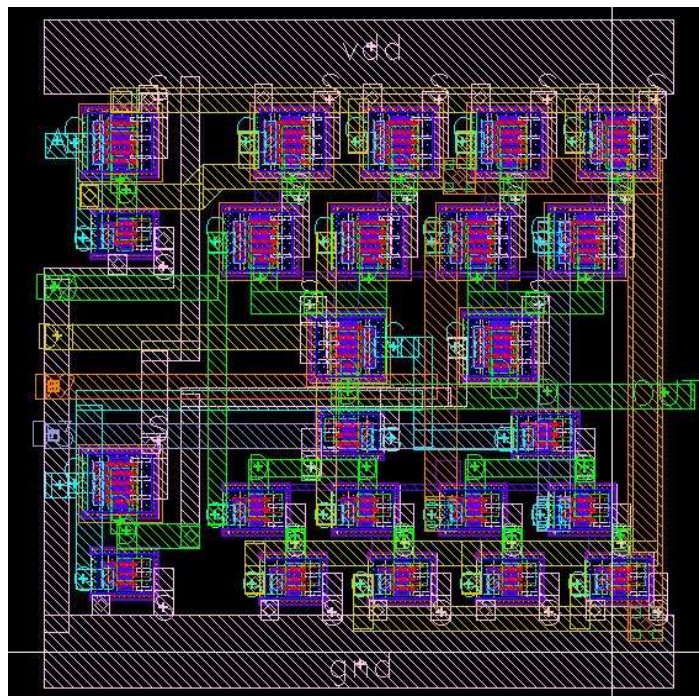


Fig. 30. Output frequency selector layout.

3.8 – Complete Programmable Frequency Divider

The layout of the implemented programmable divide-by-24 to divide-by-27 blocks in a standard 90nm CMOS process is shown in Figure 11 (as represented in the Cadence™ Virtuoso environment). In the diagram, the single divider chains are highlighted in red. Each divider chain is placed horizontally, and all the chains are fed with the same input signal. Actually, each division ratio is realized at the same time, and the output selection is made using the output multiplexer. The complete layout of the programmable divider is enclosed in a rectangle of 109 x 200 μm^2 .

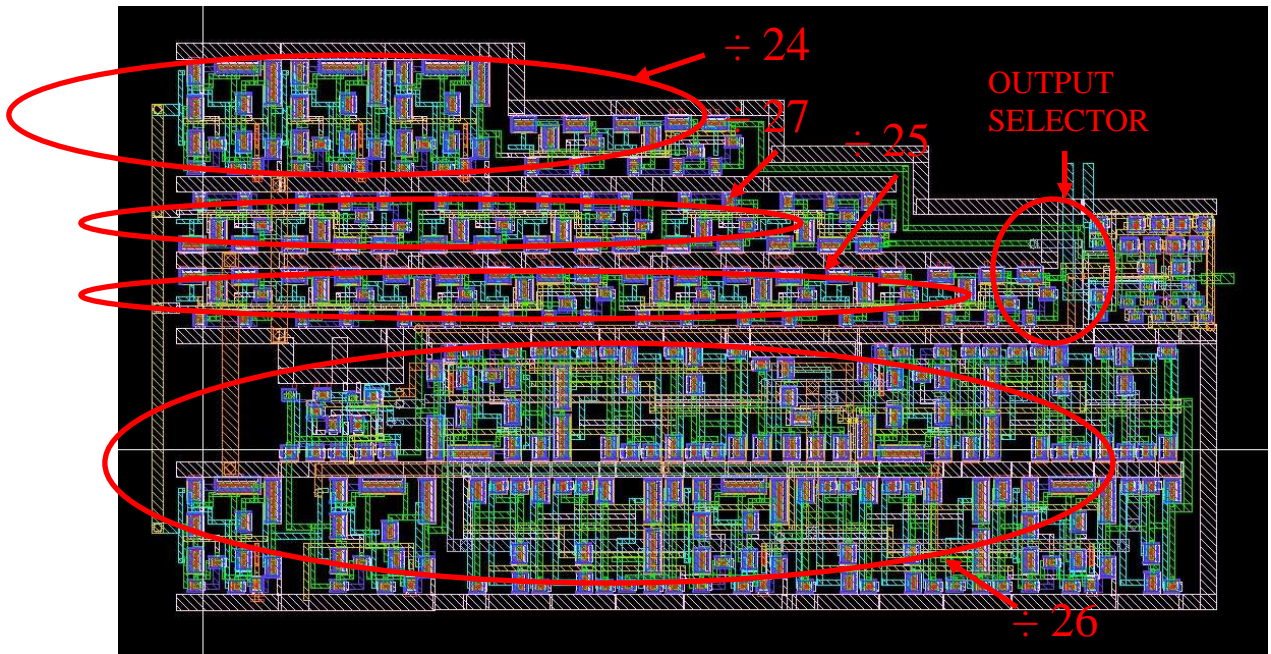


Fig. 31. Complete frequency divider layout.

CHAPTER 4

SIMULATION RESULTS

4.1 – Simulation Environment Setup

In order to estimate the performance of the designed programmable frequency divider, a simulation environment capable to take into account the actual models for the CMOS technology employed needed to be used. Moreover, post-layout parasitic effects need to be considered as well. To this extent, Cadence™ Analog Environment, and Virtuoso Layout editor have been used. The technology employed for this design is a standard 90 nm CMOS from ST-Microelectronics.

Transient simulations have been employed to evaluate the maximum frequency of operation for the frequency divider. To the extent of taking into account the worst-case scenario for the loading condition, the divider output has been loaded with a 500 fF capacitor. To take into account the parasitic effects on the input waveform, the input square wave has been filtered with an RC ladder element. The resulting setup is reported in Fig. 32. The square wave input signal alternates between +1 V and 0 V, while the input RC ladder filter elements, R_s and C_s , have the values of 100 Ω and 100 fF. The power supply has been set to +1 V.

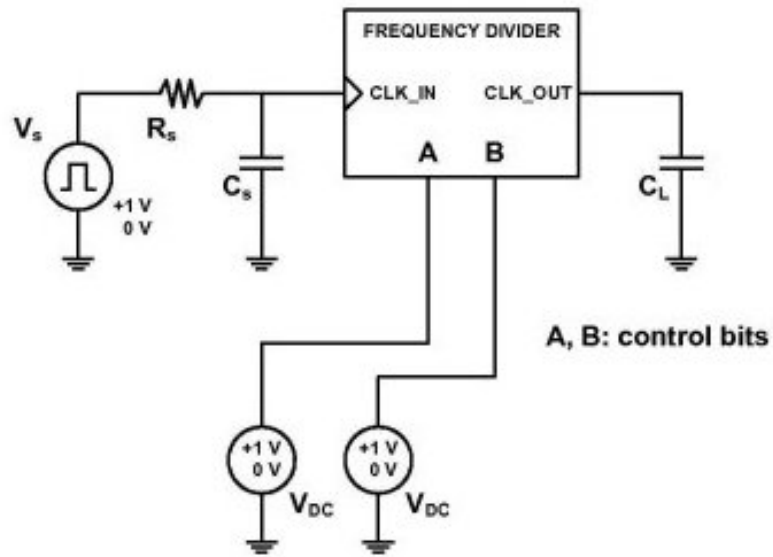


Fig. 32. Simulation setup for transient analysis.

4.2 – Transient Simulation Results

Parasitic-extracted simulations (Fig. 33) showed the divider working properly until 5 GHz with a power consumption of 7.14 mW from the 1 V supply. To the extent of evaluating the impact of a variation in the voltage supply to the maximum operating frequency, the voltage supply has been swept from 0.9 V to 1.1 V. The results are reported in Fig. 34.

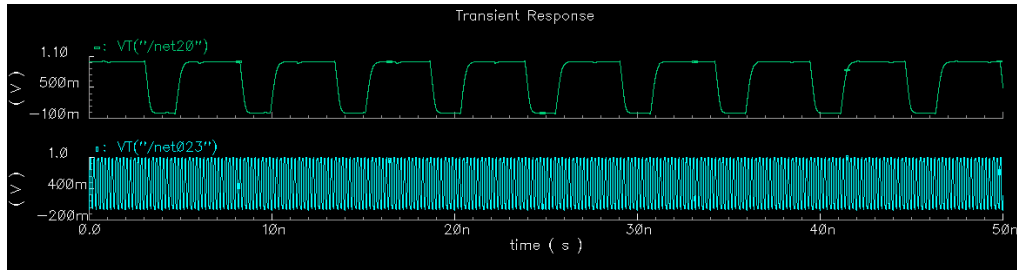


Fig. 33. Parasitic extracted simulation results at 5 GHz.

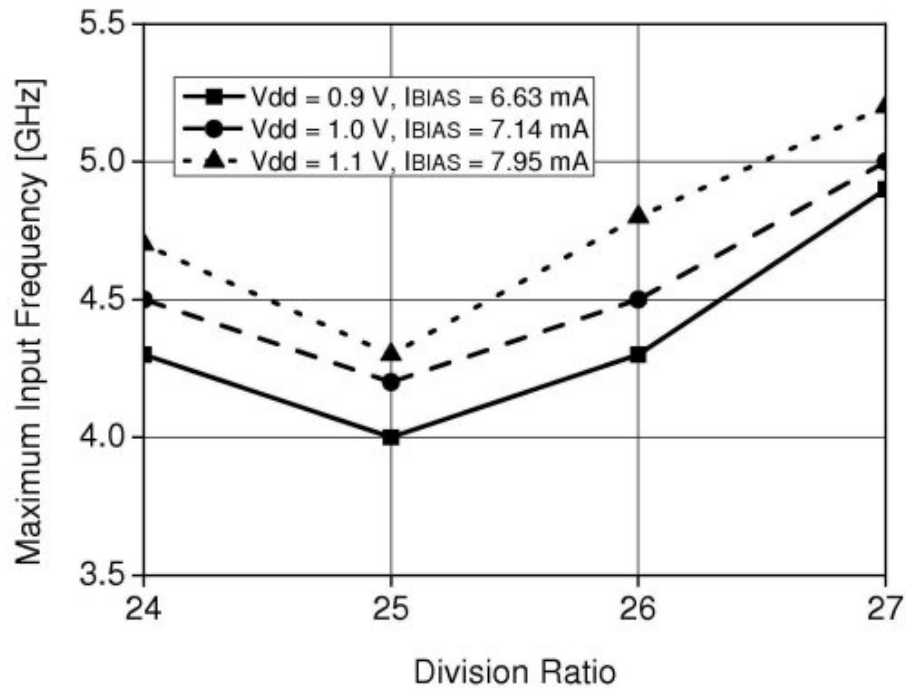


Fig. 34. Maximum input frequency vs. Division ratio for different voltage supplies.

As can be seen from Fig. 34, when a voltage supply of 1.1 V is applied, the maximum operating frequencies for all the available division ratios is increased. Conversely, when the voltage supply is decreased to 0.9 V, the maximum operating frequencies are reduced as well. For more clarity and clarification, the numeric results are reported in Table II.

TABLE 2

PROGRAMMABLE FREQUENCY DIVIDER PERFORMANCE.

Division Ratio	Maximum Input Frequency [GHz]	Current Consumption [mA]	Voltage Supply [V]
24	4.3	6.63	0.9
25	4.0		
26	4.3		
27	4.9		
24	4.5	7.14	1.0
25	4.2		
26	4.5		
27	5.0		
24	4.7	7.95	1.1
25	4.3		
26	4.8		
27	5.2		

CHAPTER 5

CONCLUSIONS

In this work, a programmable frequency divider suitable for millimeter wave phase-lock loops has been presented. The frequency divider has been implemented in a 90 nm standard CMOS technology. To the extent of maximizing the operative input frequency, the higher frequency digital blocks of the frequency divider have been realized using dynamic precharge-evaluation logic. Moreover, a non-conventional method to implement non-power-of-2 division ratios has been used for the higher frequency divider stages (input stages). In the following, a list of claims, innovations, and possible improvements for the presented design, is reported:

1) This approach represents a trade-off between dynamic charge-sharing logic dividers and a purely static architecture, offering higher maximum speed of operations with respect to previously published dividers [7], and obtaining a much lower overall power consumption for the complete programmable divider;

2) The addition of a fast reset implementation in the evaluation stage of the dynamic D-FF (Fig. 13) allowed higher speed reset in the divide-by-13 divider compared with traditional static D-FF designs;

3) The implemented architecture is modular, and therefore easily expandable: addition of new frequency division ratios and/or output channels can be done just adding the required divider chains and setting the needed number of control bits to the output multiplexer;

4) Since the presented programmable frequency divider is suited for PLL applications, not 50% output frequency duty-cycle does not represent an issue thanks to the edge-triggered logic implemented in the most phase-frequency detectors (PFDs): this fact allows the simplification of the divider architecture thus allowing higher maximum operating frequencies;

5) Power consumption can be further reduced without any maximum speed degradation, switching off the unused divider chains when the desired one is selected by the output multiplexer;

6) Since the reported [8] voltage-controlled oscillators (VCO) maximum bandwidth for standard CMOS implementations is in the order of 5-8% of the 60 GHz center frequency, channel switching capability is a requirement to exploit the whole 7 GHz frequency spectrum. Moreover, recent developments in the standard definition (IEEE 802.15 working group for WPAN) have set the channel bandwidth to be in the order of 2 GHz, thus requiring a channel selection implementation in a multiplexed operational environment.

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