GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION
SPONSORED PROJECT INITIATION

Date: 8/10/80

Project Title: Study of Heterogeneous Distributed Microcomputer Network Using Measured Data and Analytical Simulation Models

Project No: E-21-616

Project Director: Dr. J. H. Schlag

Sponsor: U.S. Army Research Office; P.O. Box 12211; Research Triangle Park, NC 27709

Agreement Period: From 6/10/80 Until ~~6/9/81~~ ~~6/9/82~~ 9/9/82

Type Agreement: Short Form Research Contract No. DAAG29-80-K-0009

Amount: $74,973

Reports Required: Semi-Annual Progress Report; Interim Technical Report(s); Publication Reprint(s); Final Technical Report

Sponsor Contact Person (s):

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Property Administration, Plant Clearance, and Close-out Duties
ONRRR - Georgia Tech

Defense Priority Rating: None

Assigned to: Electrical Engineering (School/~~Laboratory~~)

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SPONSORED PROJECT TERMINATION/CLOSEOUT SHEET

Date 3/19/84

Project No. E-21-616 — School/~~Lab~~ Electrical Engineering

Includes Subproject No.(s)

Project Director(s) Dr. J. H. Schlag — GTRI / ~~GIT~~

Sponsor U.S. Army Research Office, Research Triangle Park, NC

Title Study of Heterogeneous Distributed Microcomputer Network Using Measured Data and Analytical Simulated Models

Effective Completion Date: 9/9/82 (Performance) 11/9/82 (Reports)

Grant/Contract Closeout Actions Remaining:

- [ ] None
- [ ] Final Invoice or Final Fiscal Report (Done 4/26/83)
- [x] Closing Documents
- [x] Final Report of Inventions
- [x] Govt. Property Inventory & Related Certificate
- [ ] Classified Material Certificate
- [ ] Other

Continues Project No. — Continued by Project No.

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MEMORANDUM

TO: DALE MURRAY

FROM: J.H. SCHLAG

SUBJECT: PROGRESS REPORT FOR PROJECT DAAG29-80-K-0009 FOR PERIOD 6/11/80 TO 6/30/80

I. ACTIVITIES

TASK 1. DESIGN AND IMPLEMENTATION OF NON-INTRUSIVE MONITOR EQUIPMENT

The emphasis of the current non-intrusive monitor study is to develop a method of reading the microprocessor memory without affecting the operation of the communication CPU. Several methods have been investigated that could be applied to the 8080 and 6800 microprocessors. The most promising technique is being implemented on one of the existing 6800 memory boards.

TASK 2. DESIGN AND IMPLEMENTATION OF TRAFFIC GENERATING EQUIPMENT

The work on this task has not been started. Work should begin during the fall quarter.

TASK 3. DEVELOPMENT OF ANALYTIC/SIMULATION MODEL FOR AIRMICS/GA. TECH NETWORK

The object of current work is to develop queueing theory models for the network operating in its most elementary modes. A model consisting of some six or seven queues has been devised for a flow of packets from a source around a fixed path through two nodes and back to the source node. This model has been studied analytically to relate total packet delay and various queueing delays to line capacity CPU processing time and packet transmission rate.

Some attention has been given to the study of the Multi-command Network Project Report with the objective of understanding the nature of typical Army Data Processing Installations. The thrust of this part of the study will be to formulate a typical data processing environment for use in studying the AIRMICS/Ga. Tech network.

TASK 4. EVALUATION AND TEST OF SIMULATION MODEL WITH THE EXPERIMENTAL NETWORK

The work on this task has not been started. Work should begin during the winter quarter.

II. FUNDS EXPENDED

A. SALARIES

NAME	HOURS	COST
J.H.SCHLAG	40	893.75
J.L.HAMMOND	80	2180.00
T.P.BARNWELL	0	0.00

TOTAL SALARY DURING PERIOD	4398.75
TOTAL SALARY TO DATE	4398.75
FUNDS REMAINING FOR SALARY	32475.25

B. TRAVEL

No travel was used during the report period

TOTAL TRAVEL FUNDS EXPENDED TO DATE	0.00
TOTAL TRAVEL FUNDS REMAINING	0.00

C. OTHER COSTS

MATERIALS AND SUPPLIES EXPENDED TO DATE	0.00
MATERIALS AND SUPPLIES REMAINING	5000.00

III. EQUIPMENT

EQUIPMENT ORDERED DURING REPORTING PERIOD

DESCRIPTION	COST
NONE	

EQUIPMENT FUNDS EXPENDED TO DATE	0.00
EQUIPMENT FUNDS REMAINING	1500.00

IV. PROJECTED ACTIVITIES

The projected activities for the next reporting period will be to extend the existing effort on Task 1. and Task 3. No effort is projected for Task 2. and 4. Some minor AIRMICS assistance will be required in defining application data for Task 3.

MEMORANDUM

TO: DALE MURRAY

FROM: J.H. SCHLAG

SUBJECT: PROGRESS REPORT FOR PROJECT DAAG29-80-K-0009 FOR PERIOD 7/1/80 TO 7/31/80

I. ACTIVITIES

TASK 1. DESIGN AND IMPLEMENTATION OF NON-INTRUSIVE MONITOR EQUIPMENT

The non-intrusive monitor for the 6800 microprocessor has been sucessfully prototyped using two different techniques. The first technique provides a method for the slave CPU to read the memory of the master CPU as an I/O devices. With this process the slave CPU sends out the desired memory address to an output holding register and the memory is modified to present this memory location to a data holding register any time the memory is not being used by the master CPU. A single flip flop is used as a flag to indicate that data is vaild in the output data register. This technique has the advantage that it can be used with a master CPU that is different than the slave CPU. The disadvantage of this technique is the additional hardware and wiring of a second address and data bus.

The second technique uses two 6800 microprocessors on the same bus that share the same memory. This is accomplished by running the slave CPU with an inverted clock. This means that the master CPU accesses the memory during one phase of the clock and the slave accesses during the other. A small amount of dead time is required to allow the memory to switch between processors. This technique has the advantage of requiring very little additional changes to the existing microprocessor hardware.

TASK 2. DESIGN AND IMPLEMENTATION OF TRAFFIC GENERATING EQUIPMENT

The work on this task has not been started. Work should begin during the fall quarter.

TASK 3. DEVELOPMENT OF ANALYTIC/SIMULATION MODEL FOR AIRMICS/GA. TECH NETWORK

Queueing theory models have been developed for elementary operating modes of the network. These modes include circulation of a fixed number of messages around possible loops in the network. The models have been analyzed to give relations between delay time and the number of messages circulating for fixed processing rates of the host and node CPUs and for fixed line capacities.

A model has also been developed and analyzed for a portion of the network including two hosts and the portion of the network between two interconnecting nodes. For this case, end-to-end delay can be expressed in terms of the line capacities, host CPU processing rates, node CPU processing rates and the processing rate of one peripherial device for each host.

TASK 4. EVALUATION AND TEST OF SIMULATION MODEL WITH THE EXPERIMENTAL NETWORK

The work on this task has not been started. Work should begin during the winter quarter.

II. FUNDS EXPENDED

A. SALARIES (BUDJECT = $36274.00)

NAME	HOURS	COST
J.H.SCHLAG	40	893.75
J.L.HAMMOND	80	2180.00
T.P.BARNWELL	0	0.00
GRAD. STUDENTS	160	1325.00

TOTAL SALARY DURING PERIOD	4398.75
TOTAL SALARY TO DATE	8797.50
FUNDS REMAINING FOR SALARY	28076.50

B. TRAVEL (BUDJECT = $0.0)

No travel was used during the report period

TOTAL TRAVEL FUNDS EXPENDED TO DATE	0.00
TOTAL TRAVEL FUNDS REMAINING	0.00

C. OTHER COSTS (BUDJECT = $5000.00)

MATERIALS AND SUPPLIES EXPENDED TO DATE	0.00
MATERIALS AND SUPPLIES REMAINING	5000.00

III. EQUIPMENT (BUDJECT = $1500)

EQUIPMENT ORDERED DURING REPORTING PERIOD

DESCRIPTION	COST
NONE	

EQUIPMENT FUNDS EXPENDED TO DATE	0.00
EQUIPMENT FUNDS REMAINING	1500.00

IV. PROJECTED ACTIVITIES

The projected activities for the next reporting period will be to extend the existing effort on Task 1. and Task 3. No assistance will be required in defining application data for Task 3.

MORANDUM

O: DALE MURRAY

FROM: J.H. SCHLAG

SUBJECT: PROGRESS REPORT FOR PROJECT DAAG29-80-K-0009 FOR PERIOD 8/1/80 TO 8/31/80

I. ACTIVITIES

TASK 1. DESIGN AND IMPLEMENTATION OF NON-INTRUSIVE MONITOR EQUIPMENT

Development of the multiport communication processor has almost been completed with the sucessful testing of a processor node with two CPU'S working from the same memory. Four additional control units will be built to convert the additional nodes to the multi-processor configuration. Parts have been ordered to build 6 additional memory boards, 3 additional serial I/O boards, and 5 additional CPU'S. A major effort has been started to update the communication node software. The old processor program is being rewritten to eliminate problems found in the initial debuging process and to streamline the processor operation. This update should improve the reliability and speed of the network.

TASK 2. DESIGN AND IMPLEMENTATION OF TRAFFIC GENERATING EQUIPMENT

The work on this task has not been started. Work should begin during the fall quarter.

TASK 3. DEVELOPMENT OF ANALYTIC/SIMULATION MODEL FOR AIRMICS/GA. TECH NETWORK

PROGRESS NOTES dated September 2,1980 have been prepared summarizing results of work on this task to date. The NOTES cover the following topics : (1) Elementary queueing network models for the Host and Switching Nodes of the AIRMICS/GEORGIA TECH NETWORK, (2) Approach to the analysis of these models, (3) Proposed basic experiments with the network, (4) A proposed two host experiment.

The work concerned with item (3) and (4), i.e. devising experiments to be done with the network, was done during the last report period. These experiments were formulated as a first step in verifying the analytical models.

Also during the last report period, the queueing models were used to give relations for the following average variables:

1. Delay time for each Channel, Node and Host CPU

2. End - to - End Delay

3. Queue Lengths at each storage element

4. Utilization Factors

5. Variances of each of the quantities

All of the quantities can potentially be measured in experiments with the network.

TASK 4. EVALUATION AND TEST OF SIMULATION MODEL WITH THE EXPERIMENTAL NETWORK

The work on this task has not been started. Work should begin during the winter quarter.

II. FUNDS EXPENDED

A. SALARIES (BUDJECT = $36874.00)

NAME	HOURS	COST
J.H.SCHLAG	40	893.75
J.L.HAMMOND	80	2180.00
T.P.BARNWELL	0	0.00
GRAD. STUDENTS	160	1325.00

TOTAL SALARY DURING PERIOD	4398.75
TOTAL SALARY TO DATE	13196.25
FUNDS REMAINING FOR SALARY	23677.75

B. TRAVEL (BUDJECT = $0.0)

No travel was used during the report period

TOTAL TRAVEL FUNDS EXPENDED TO DATE	0.00
TOTAL TRAVEL FUNDS REMAINING	0.00

C. OTHER COSTS (BUDJECT = $5000.00)

MATERIALS AND SUPPLIES EXPENDED TO DATE	3118.00
MATERIALS AND SUPPLIES REMAINING	1882.00

III. EQUIPMENT (BUDJECT = $1500)

EQUIPMENT ORDERED DURING REPORTING PERIOD

DESCRIPTION	COST
NOVA 4 PORT INTERFACE	1500.00

EQUIPMENT FUNDS EXPENDED TO DATE	1500.00
EQUIPMENT FUNDS REMAINING	0.00

IV. PROJECTED ACTIVITIES

the objectives of: (1) making the models represent the network more accurately and (2) analyzing the more accutate models.

Work will continue on the processor software and the completion of the additional processor hardware. An effort will be started to formulate the performance monitor software for the slave CPU and the Nova 3.

MEMORANDUM

TO: DALE MURRAY

FROM: J.H. SCHLAG

SUBJECT: PROGRESS REPORT FOR PROJECT DAAG29-80-K-0009 FOR PERIOD 9/1/80 TO 9/31/80

I. ACTIVITIES

TASK 1. DESIGN AND IMPLEMENTATION OF NON-INTRUSIVE MONITOR EQUIPMENT

The parts have begun to arrive for the additional memory boards, serial I/O boards, and CPU boards. The memory boards have been fabricated and the memory board parts are being installed as they arrive. The CPU and serial I/O boards have been etched and are presently being drilled.

Some minor modifications were made in the multiport control printed circuit board to add a real time clock and timing control input to the system. The real time clock will increment a memory location every one millisecond to simplify performance timing and the timing control input will permit a single clock to to time the operation of all of the communication processors.

The effort to update the processor communication software is proceeding as scheduled.

TASK 2. DESIGN AND IMPLEMENTATION OF TRAFFIC GENERATING EQUIPMENT

The major effort on this task is being delayed by the delievery of the Data General 4 port interface. Some work has been done in designing the basic software configuration for the traffic monitor.

TASK 3. DEVELOPMENT OF ANALYTIC/SIMULATION MODEL FOR AIRMICS/GA. TECH NETWORK

The queueing models discussed in the PROGRESS NOTES of September 2,1980 are elementary but never the less are representative of what is typically used in analyzing networks such as the AIRMICS/GEORGIA TECH NETWORK. Planned experiments with the physical network will provide data to show how well the elementary models represent the actual performance of the network.

Since the elementary models developed are unlikely to provide an exact representation of the network behavior, efforts are now underway to develop more accurate models. Work during the report period involved additional study of the literature in an effort to find an approach giving a more accurate representation.

Several approaches, which claim better accuracy than that obtained by the first elementary model, have been found. These approaches are now being studied to determine if they can be applied and if the claim of better accuracy is valid.

EXPERIMENTAL NETWORK

The work on this task has not been started. Work should begin during the winter quarter.

II. FUNDS EXPENDED

A. SALARIES (BUDJECT = $36874.00)

NAME	HOURS	COST
J.H.SCHLAG	40	893.75
J.L.HAMMOND	80	741.00
T.P.BARNWELL	0	0.00
GRAD. STUDENTS	160	2175.00
STUDENT ASSISTANTS	77	375.00

TOTAL SALARY DURING PERIOD	4184.75
TOTAL SALARY TO DATE	17381.00
FUNDS REMAINING FOR SALARY	19493.00

B. TRAVEL (BUDJECT = $0.0)

No travel was used during the report period

TOTAL TRAVEL FUNDS EXPENDED TO DATE	0.00
TOTAL TRAVEL FUNDS REMAINING	0.00

C. OTHER COSTS (BUDJECT = $5000.00)

MATERIALS AND SUPPLIES EXPENDED TO DATE	3318.00
MATERIALS AND SUPPLIES REMAINING	1682.00

III. EQUIPMENT (BUDJECT = $1500)

EQUIPMENT ORDERED DURING REPORTING PERIOD

DESCRIPTION	COST
NOVA 4 PORT INTERFACE	1500.00

EQUIPMENT FUNDS EXPENDED TO DATE	1500.00
EQUIPMENT FUNDS REMAINING	0.00

IV. PROJECTED ACTIVITIES

The continuation of the model analysis will center or model accuracy of the models discovered durning this report period.

The work on the performance monitor should increase this month if the 4 port interface is recieved from Data General.

MEMORANDUM

TO: DALE MURRAY

FROM: J.H. SCHLAG

SUBJECT: PROGRESS REPORT FOR PROJECT DAAG29-80-K-0009 FOR PERIOD 11/1/80 TO 11/31/80

I. ACTIVITIES

TASK 1. DESIGN AND IMPLEMENTATION OF NON-INTRUSIVE MONITOR EQUIPMENT

All of the multiport control P.C. boards have beeen fabricated and three have been filled with parts and tested. The framework for the three additional communication boxes have been constructed and the new power supplies have been tested. The major portion of the construction of the remaining boxes is finished, except for the mechanical mounting and testing.

One point of interest, is that the multiport control boards appear to have different maximun operating frequencies. This is appears to be differencies in bus drivers and noise margins, but since the lowest upper frequency is still .9 mhz no real problem is expected.

TASK 2. DESIGN AND IMPLEMENTATION OF TRAFFIC GENERATING EQUIPMENT

The Data General 4 port interface connection system is being modified to use standard RS232 connectors which willl mount on the back of the NOVA 3 computer. This will greatly simplify the problem of connecting the NOVA to the communication network. No new problems have been incountered with the NOVA/node communication hardware or software.

TASK 3. DEVELOPMENT OF ANALYTIC/SIMULATION MODEL FOR AIRMICS/GA. TECH NETWORK

It seems appropriate at this time to review a statement of the task objective and an outline of the approach being taken.

TASK OBJECTIVE:

To develop and evaluate a queueing theory model for the AIRMICS/Georgia Tech Network. (Although outside of the scope of the present project, the model can be used to improve the design of the network. It can also be used in designing adaptive features for routing and flow control.)

APPROACH:

Step 1. Develop a queueing theory model which assumes infinite buffers and tractable distributions for traffic and standard network tasks.

Step 2. Adjust the parameters of the model to correspond to values measured from the network and computed results with measured results for message delay, throughput, utilization,etc., for the whole network and components of the network.

Step 3. Refine the model so that it more closely approximates capacity.

Other refinements may be required based on an analysis of the correspondence between measured and computed results.

Progress to date, through November, with respect to the approach outlined above is as follows.

Step 1 above has been completed and the results summarized in the PROGRESS NOTES of September 2,1980. These Notes describe the queueing theory models which follow using the assumptions given. They also outline several experiments and classes of experiments which can be performed with the physical network to obtain desired measured results.

Step 2 of the stated appraoch will be carried out when instrumentation of the network has been completed.

Current studies are directed toward developing the finite buffer model of Step 3. Development of a useful analytical model of this type will require an advancement over existing techniques. An analytical model would be desirable for later incorporation into adaptive networks.

An approach based on the use of a Markov chain to model the system queues is currently being studied. It is too soon to predict whether or not the approach will be sucessful. If it is not, numerical techniques or simulation can be resorted to, although these techniques are not as desirable as analytic ones.

TASK 4. EVALUATION AND TEST OF SIMULATION MODEL WITH THE EXPERIMENTAL NETWORK

The work on this task has not been started. Work should begin during the winter quarter.

II. FUNDS EXPENDED

A. SALARIES (BUDGET = $36874.00)

NAME	HOURS	COST
J.H.SCHLAG	40	893.75
J.L.HAMMOND	80	741.00
T.P.BARNWELL	0	0.00
GRAD. STUDENTS	160	2175.00
STUDENT ASSISTANTS	77	375.00

TOTAL SALARY DURING PERIOD	4184.75
TOTAL SALARY TO DATE	25750.50
FUNDS REMAINING FOR SALARY	11123.50

B. TRAVEL (BUDGET = $0.0)

No travel was used during the report period

TOTAL TRAVEL FUNDS EXPENDED TO DATE	0.00
TOTAL TRAVEL FUNDS REMAINING	0.00

MATERIALS AND SUPPLIES EXPENDED TO DATE 4320.00

MATERIALS AND SUPPLIES REMAINING 680.00

III. EQUIPMENT (BUDGET = $1500)

EQUIPMENT ORDERED DURING REPORTING PERIOD

DESCRIPTION	COST

EQUIPMENT FUNDS EXPENDED TO DATE 1500.00

EQUIPMENT FUNDS REMAINING 0.00

IV. PROJECTED ACTIVITIES

The projected effort in the model analysis will center on the Markov Chain analysis.

The projected effort in the network fabraction and testing will center on finishing the board construction and the communication software.

MEMORANDUM

TO: DALE MURRAY

FROM: J.H. SCHLAG

SUBJECT: PROGRESS REPORT FOR PROJECT DAAG29-80-K-0009 FOR PERIOD 12/1/80 TO 12/31/80

I. ACTIVITIES

TASK 1. DESIGN AND IMPLEMENTATION OF NON-INTRUSIVE MONITOR EQUIPMENT

All the P.C. boards for the five communication boxes have been fabricated and the communication boxes have been constructed. The only construction left to complete the nodes is to modify the CPU boards for multiport use and to wire the bus connections on the back of the cummunication boxes.

TASK 2. DESIGN AND IMPLEMENTATION OF TRAFFIC GENERATING EQUIPMENT

The final version of the new software on the communication processor is being put together and checked for assembly and loader errors. This part of the software with the performance monitor will complete the node software package. The performance monitor section has been completed for several months. Debugging of the system software should begin in the next report period.

TASK 3. DEVELOPMENT OF ANALYTIC/SIMULATION MODEL FOR AIRMICS/GA. TECH NETWORK

Work during the report period was directed toward the finite buffer system discussed in the November 1980 Monthly Report.
A Markov Chain model was used to represent the queues. Using this approach and an innovative reduction technique to reduce the number of states, it was possible in some special cases to find desired system parameters such as blocking probabilities, delay, throughput, etc.
Work is continuing to extend the Markov Chain approach and the reduction technique to more general systems. The extent of the applicability of this method is not yet clear.

TASK 4. EVALUATION AND TEST OF SIMULATION MODEL WITH THE EXPERIMENTAL NETWORK

The work on this task has not been started. Work should begin during the winter quarter.

II. FUNDS EXPENDED

A. SALARIES (BUDGET = $36874.00)

NAME	HOURS	COST

J.L.HAMMOND	80	555.75
T.P.BARNWELL	0	0.00
GRAD. STUDENTS	160	1087.50
STUDENT ASSISTANTS	77	375.00

TOTAL SALARY DURING PERIOD	2688.25
TOTAL SALARY TO DATE	28438.75
FUNDS REMAINING FOR SALARY	8435.25

B. TRAVEL (BUDGET = $0.0)

No travel was used during the report period

TOTAL TRAVEL FUNDS EXPENDED TO DATE	0.00
TOTAL TRAVEL FUNDS REMAINING	0.00

C. OTHER COSTS (BUDGET = $5000.00)

MATERIALS AND SUPPLIES EXPENDED TO DATE	4520.00
MATERIALS AND SUPPLIES REMAINING	480.00

III. EQUIPMENT (BUDGET = $1500)

EQUIPMENT ORDERED DURING REPORTING PERIOD

DESCRIPTION	COST

EQUIPMENT FUNDS EXPENDED TO DATE	1500.00
EQUIPMENT FUNDS REMAINING	0.00

IV. PROJECTED ACTIVITIES

The projected effort in the model analysis will center on the Markov Chain analysis.

The projected effort in the network fabraction and testing will center on finishing the board construction and the communication software.

E-21-616

THE STUDY OF A HETEROGENEOUS DISTRIBUTED MICROCOMPUTER NETWORK USING MEASURED DATA AND ANALYTIC/SIMULATION MODELS

Final Report Part II

BACKGROUND ON EVOLUTION OF SPANET

By

J. L. Hammond
J. H. Schlag
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332

1. TESTBEDS FOR MICROPROCESSOR NETWORK RESEARCH

Many of the components of computer-communication networks, both hardware and software, are not amenable to exact analytic models. Thus there is a need for experimentation with testbed networks to understand network operation. H. K. Berg [1], in an introduction to a special issue of Computers devoted to distributed system testbeds, expands on the need for experiments with testbeds. In his article he quotes a number of other authors who make the same point.

A useful testbed must have two essential components, a flexible network for experimentation and an instrumentation system for observing the network under test. The network should consist of a flexible and modular set of components which make possible the study of a wide range of systems.

Although a number of testbeds are discussed in the literature, there is little experimental data available. In spite of the desire for a very flexible structure, for understandable reasons, many testbed structures are special purpose and can support only a limited number of architectures.

The special issue of Computer, October 1982, on Distributed System Testbeds has articles describing three different testbeds which are located at Mitre, System Development Corp., and Carnegie-Mellon. Details of these networks are contained in the articles.

Other testbed facilities are CHIMPNET at Honeywell [2], and the network at the National Bureau of Standards (NBS) [3].

2. CHOICE OF DESIGN OBJECTIVES FOR SPANET

Local computer networks seem destined to play a role of increasing importance in distributed processing. Within the class of local computer networks the contention-type structure has a number of advantages in terms of reliability cost, and ability to reconfigure networks.

Given the important role foreseen for contention-type local networks, the U.S. Army Institute for Research in Management Information and Computer Science has a need to be able to study such networks and to assess the performance of particular type networks for specific military applications.

What is desired is a low cost facility which can be conveniently programmed to make realistic performance studies of a variety of specific applications of contention-type local computer networks. It is anticipated that the performance of a pair of stations, operating over a network loaded to various degrees with traffic from sources not a part of the study, will be of interest, in addition to the performance of the network as a whole.

Such studies could obviously be carried out using the brute force approach of building a test bed with a number of different networks deployed. Each network would have to be loaded with stations producing prescribed traffic and the number of stations to achieve full loading could approach 1000 for the Ethernet, as an example. This approach to a test facility is not cost effective, and the present project is directed toward the design and construction of a much lower cost, emulation type, alternative which will model network performance with a combined hardware/software facility.

In summary, the project objectives are to design and construct an emulation facility for studying the performance of full scale contention-type local networks, such as Ethernet. Station-to-station and high level network performance are desired and this constrains the emulation to model or duplicate the performance of Data Link and higher layers in the protocol hierarchy as well as the Physical Layer. At the same time, required results do not include detailed studies of the Physical Layer hardware.

To make the facility versatile it should be possible to change the type of contention algorithm by a change in software. Project funding is not sufficient to provide more than a few physical stations. Thus the effect of the majority of stations for a heavy load condition will have to be produced with software. This software should have adjustable parameters which can set the level and character of background loading.

The facility will also be equipped to measure such quantities as average packet delay, average packet arrival rate, throughput, and other quantities used in specifying performance.

3. EVOLUTION OF SYSTEM-LEVEL SPANET DESIGN

The class of local networks of interest can have as many as 1000 stations. The requirements for the emulation facility as stated in Section 2 make it necessary to combine the majority of the stations and represent them by some equivalent device or software. The remaining several stations can be realized by actual hardware or the majority of their functions can be performed by actual hardware.

A reasonable structure for the emulation facility, consistent with the above requirements, includes two actual host computers with interfaces and a computer acting as a artificial traffic generator, also with interface equipment. How the three pieces of physical hardware interface to each other depends on the philosophy of emulating the actual network. Two approaches were considered in detail.

In one approach time would be scaled so that interfacing could take place through low speed RS-232 ports. In this approach a low speed counterpart would exist in hardware for most of the components of both the Network Processor and the Transceiver Interface of the network. In the time scaled emulation, an RS-232 port would interconnect the Transceiver Interfaces rather than the Transceiver/Coaxial cable in the actual system.

A study of the contention mechanisms showed that for proper time scaled operation it would be necessary to scale the coupling delay up to tens of milli-seconds in the RS-232 coupling, from values in the microsecond range for the actual cable.

The time scaled approach is feasible and a facility could be constructed at reasonable cost. It has the serious drawback, however, that everything including the host computers in the two physical stations, must run at reduced speed. Thus no part of the emulated network would be working exactly as it does in the actual network.

Another approach was developed which allows most of the equipment of the two stations to operate essentially as it does in the actual network. This approach is favored over the one just described and it is discussed in detail in the first part of the report.

The favored emulation approach preserves two User Devices (typically host computers) and their associated Network Processors in physical hardware. The remainder of the network including the Transceiver Interfaces and Transceivers for the two Users Devices, the Cable, and all other User Devices and their associated interfacing equipment is emulated with a software program and a "Switch" between the two actual User Devices. The Switch is expected to be realized by software control of pointers in a memory shared by the physical User Devices.

4. HARDWARE IMPLEMENTATION

The original intent of the proposed research was to implement two network topologies. One for the mesh network as shown in Figure 4.1 and one for the bus network as shown in Figure 4.2. The mesh network configuration is the same as the network developed in the 1979 AIRMICS project with a upgrade of the microprocessor node from a Motorola 6800 to a Motorola 68000. The bus network, on the other hand, represented a new area of interest for both Georgia Tech and AIRMICS.

4.1 Bus Configuration Hardware

As mentioned in the previous section, the bus hardware configuration was proposed as an extension to the mesh network experience developed in the previous AIRMICS/Georgia Tech contracts. The original bus configuration concept was to use the five 68000 microprocessors as nodes on a 9600 baud TTL serial bus. The existing microprocessor systems would be used as host to drive the 68000 nodes. The bus length delays between the nodes would be simulated by using RC time constants on the TTL serial bus line.

This initial proposed configuration for the bus network had a number of shortcomings:

1. The 9600 baud TTL serial link was not at all close to the present state of the art in bus network transmission speeds, a fact which could leave questions in many people's minds about the validity of the bus experiments.
2. With only five stations driven from microprocessor hosts, it is impossible to generate enough traffic to adequately load even a moderate speed, modern bus network.

3. A RC time constant can be used to implement time delays which are a fraction of one bit time on the bus transmission. In modern bus networks, the bus link delay can easily exceed the length of one bit in the transmission.

4. The performance monitoring of every node in the network that was implemented as part of the mesh store and forward configuration was extrememly valuable in tracking messages that might travel through several mesh nodes before reaching the destination node. In the bus network, if most of the nodes are operating with the same scenario and all messages are traveling on the bus from one mode directly to the destination node, then gathering performance information from one or two nodes in the system should produce adequate statistics on the overall performance of the network communications.

It was felt that the originally proposed configuration could be implemented and that experiments could be successfully run on the network. Because of the restrictions listed above, it was felt that the results of such experiments would not be well accepted by the network research community. For this reason, steps were taken to implement a new configuration that would remove this set of restrictions.

In order to increase the speed of the bus transmission from 9600 baud to 10 megabytes, the bus line was implemented as a TTL signal access through high speed parallel I/O lines from the microprocessor nodes. Instead of using this line as a bit by bit transmission of the network messages the line is simply used to indicate the busy or idle periods on the bus. The actual message content is transferred from one microprocessor node to the other by using a shared memory between the two micro systems. This process allows the microprocessors to simulate bus activity in the ten megabyte range. This increase in bus speed simulation represents a factor of approximately 1000 over the original configuration.

The second restriction, the maximum number of stations on the bus, was eliminated by building a combination hardware/software background traffic generator that could be used to load the bus representing a large number of additional nodes on the bus. An off-line software package was developed to generate a number sequence of busy and idle times representing a particular scenario of bus configurations. This software package permits a great number of variations to be programmed into the particular scenario that is generated. Hardware was used to take the number sequences from the software bus simulator and generate actual busy idle digital signals on the network bus. This technique permitted the number of stations on the bus to be expanded from 5 nodes to several hundred nodes.

The third restriction, the maximum time delay permissible with RC filters, was eliminated by building hardware programmable digital time delays using 4000 bit digital memories. Six memories were built to provide programmable delays to and from each of the major nodes in the simulation system. This hardware permits accurately controlled delays from .2 to 409.6 microseconds in .1 microsecond increments. Before these specialized delay circuits were designed and built, considerable effort was expended to find commercially available circuits or chips available from other network experiments. Because there were no circuits or hardware available, these specialized delays were designed and manufactured on printed circuit boards as a special part of the bus network experiment. We feel that this is a unique and valuable application of state of the art digital technology to the study of bus networks.

The fourth restriction, the mesh network performance evaluation technique, was eliminated by collecting data on only 2 of the nodes in the bus network system. Since each node in the system is simulated as one of n identical nodes, collecting statistical information from 2 of the n nodes should be adequate to investigate the network performance. Since each of the nodes should have basically the same statistical performance, the use of 2 nodes for performance evaluation allowed us to verify experimentally the fact that under the same operating conditions the node performance changes very little between the 2 nodes. In the mesh network the shared memory is used as a communication media between the node central processor and the performance monitor central processor. In the bus network the 2 central processors with shared memory are used as 2 nodes in the bus network with messages transported through the shared memory. Since the complete multi-byte message can be transferred between processors by changing pointers in a message queue, the effected transmission time can be reduced to several microseconds. In an actual bus network situation operating at 10 megabits, the minimum transmission time for a 100 byte message would be 80 microseconds. This means that under normal conditions the microprocessor will have additional time to store performance monitoring data without interrupting the flow of messages through the processing system. At the end of the bus experiment, the message performance data is transferred to the central Nova 4 computer for performance analysis. This technique allows the bus network to be adequately monitored without producing a excess of redundant data and also permits the shared memory to be used for message transmission instead of performance monitoring.

By reconfiguring the bus experiment hardware and eliminating the 4 major restrictions of the original proposed configuration, the resulting bus network now provides a versatile, real time experimental test bed for analyzing a wide variety of experimental networks. The effort required to eliminate the restrictions was significant especially in the areas of the modification of the real time bus delay and the development of the software algorithms and programs for generation of the background traffic.

One additional configuration change was implemented in the bus system. A third central processor was added to the 2 node central processors and shared memory. The purpose of this additional central processor is to handle all serial traffic into and out of both microprocessor nodes and to establish message queues for the nodes in the shared memory. This process permits the 2 node microprocessors to run in a relatively uninterrupted fashion while the third I/O processor handles the individual message character. This particular implementation was undertaken not to eliminate a particular restriction of the initial bus configuration but rather to improve the predictability of the node software loop timing. Two sets of the software have been written for the I/O central processor. The first software package reads serial messages from the 2 hosts that drive the microprocessor node and pack the messages into the shared memory for transmission to the other node. The messages are handled in a character by character RS232 serial protocol. This program can handle data at a maximum of 9600 baud from each of the trafficking hosts. In order to extend the capability of the system above the 9600 baud limit an alternate program has been written that will receive a 2 byte message from the trafficking host indicating the number of bytes in the message and internally generate the equivalent of a message of that number of bytes. With this technique, the trafficking host can send a 2 byte message which generates a hundred byte message internally. This technique has permitted the serial traffic to be extended from 9600 baud to 32000 baud. Both of these I/O programs can be held in the I/O processor ram memory or E prom memory, and the particular version to be run is controlled by the starting address of the microprogram.

4.2 Mesh Network

The original goal of the mesh network project was to upgrade the hardware performance of the mesh network experiment of the previous contract. This project, then, represented a expansion of current capabilities rather than an extension into a new area for Georgia Tech and AIRMICS. The initial approach to this project was to buy Motorola 68000 based hardware identical to the hardware configuration of the previous project which was based on 6800 based hardware. The software code from the 6800 project would then be translated into 68000 based language. Tests would then be run to verify the performance of the network. Even though this was a perfectly sound proposed project, a number of problems developed which barred the successful completion of the project.

The most significant problem in completing the mesh network was the fact that a fixed amount of personal services and resources were available to do both the mesh and the bus network combined. The resources required to expand the scope of the bus network into a viable experiment reduced the available resources for the mesh project. We felt that this change of priority was warranted because the bus network expanded AIRMICS capability to a greater degree than the mesh network. Since the mesh network is a repeat of the previous project, it was also felt that if no problems arose the project might be completed with a lesser amount of effort predicted, resulting in the completion of both the expanded bus network and the mesh network.

The major technical problem that arose in the mesh project was the unexpected configuration of the 68000 serial communication board. When the 68000 microprocessors were ordered, this technology was extremely new and the available information about this new product was very sparse. A unit was configured which contained 2 central processors sharing a common memory and a 4 port serial communication board with the help of the Motorola technical staff. Considerable time was spent talking with the Motorola technical staff to make sure that this configuration would work as we expected. Our major concerns were with the multiple access to the shared memory rather than the action of the I/O processor. The published performance specifications of the I/O processor did meet or exceed all our technical requirements.

When the hardware arrived, all parts of the system were as expected except for the I/O processor. What we expected in the I/O processor was 4 programmable configured serial ports interfaced directly to the main central processor through the Versabus. The unit received had all the hardware capability that we expected except that it was controlled by a preprogrammed microprocessor on the I/O board. This meant that the communication board was a lot more powerful than we had predicted, but the additional power was not under our control. Our initial reaction to the unexpected microprocessor was that it would either make the programming job a whole lot easier or a whole lot harder depending on the predetermined protocol and its adequate documentation. At this point we discussed the option of removing the ROM memory from the I/O board and reprogramming the processor to meet our own requirements. Even though this avenue would allow us better control on the outcome of the project, it would require a considerable amount of extra personal services resources. We felt that this addition would eliminate any chance of completing both the mesh and the bus network. The decision was made to stay with the preprogrammed processor with the assumption that it would save the badly needed time on the project.

However, this was not the case. The 2 major problems with the preprogrammed processor were the rigidity of the I/O protocol and the extremely poor documentation. Six weeks of the project elapsed in an attempt to get adequate documentation from Motorola in the form of better descriptions, listings of the I/O program or adequate circuit diagrams. After numerous promises from Motorola, we received the same document marked "preliminary" that we had received with the original equipment. Since Motorola has drastically changed the design of this particular circuit board in the their product line, it is not predicted that extremely detailed documentation will ever be available. Considerable time has been spent trying to get the I/O processor to work adequately in the mesh network, but each of these efforts has failed. These efforts were terminated when they jeopardized the completion of the bus experiments.

Future efforts to complete the mesh experiment could proceed along three optional paths. The first option would be to continue to work with the existing hardware which is somewhat unpredictable, but potentially could pay off very quickly. The second option would be to abandon the existing I/O processors and buy the newer, better documented units from Motorola. A third option would be to reprogram the existing units to the protocol that we require. The first of these options is still probably the most cost effective for a limited number of resource dollars expended.

4.3 Remaining Budget

Some equipment money was left at the end of the project because we could only encumber money based on the list price of the equipment being purchased, and remaining funds cannot be expended after the contract date. A number of purchases were actually invoiced after the contract date, and the competitive bid price of these units was considerably less than expected, but the differential funds could not be expended because of the contract date. The total dollars left of the contract is $3,555.01.

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