HYBRID (CURRENT/VOLTAGE MODE) DIGITAL POWER AMPLIFIER AND BIDIRECTIONAL DIGITAL FRONT-END CIRCUITS IN SILICON

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HYBRID (CURRENT/VOLTAGE MODE) DIGITAL POWER AMPLIFIER AND BIDIRECTIONAL DIGITAL FRONT-END CIRCUITS IN SILICON

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To my family and friends

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"Only those who confront unusual challenges can flaunt unusual success."

— *Vincent Okay Nwachukwu*

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IoT	Internet-of-Things
PAPR	Peak-to-average power ratio
QAM	Quadrature amplitude modulation
OFDM	Orthogonal frequency division multiplexing
PBO	Power back off
RF	Radio frequency
CMOS	Complementary metal-oxide-semiconductor
AM	Amplitude modulated
PM	Phase modulated
PA	Power amplifier
RX	Receiver
TX	Transmitter
MIMO	Multi-in multi-out
DAC	Digital-to-analog convertor
DPD	Digital pre-distortion
TRX	Transceiver
SAW	Surface Acoustic Wave
FBAR	Film bulk acoustic resonator
DE	Drain efficiency
DPD	Digital pre-distortion
OOB	Out-of-band
LNA	Low noise amplifier

SCPA	Switched capacitor power amplifier
C-DPA	Current mode digital power amplifier
V-DPA	Voltage mode digital power amplifier
EM	Electromagnetic
ESD	Electrostatic discharge
I/O	Input/output
PCB	Printed circuit board
CW	Continuous wave
ADS	Advanced design system
EVM	Error vector magnitude
LUT	Look-up-table
AWG	Arbitrary waveform generator
ACLR	Adjacent Channel Leakage Ratio
SHS	Sub harmonic switching
SFCPA	Switched/Floated capacitor power amplifier
ENOB	Effective number of bits
NF	Noise Figure
OMN	Output matching network
IIP3	Third-order input intercept point
IIP2	Second-order input intercept point
LO	Local oscillator
DSB	Double side band

SUMMARY

The advent of Internet-of-Things (IoT), smart factories, and mobile devices has caused a surge of connected devices and proliferation of wireless sensor nodes. Modern communication systems, which need to be connected everywhere and at all times, require each device to be compact, and impose stringent standards for the RF systems. Transmitters, in face of the explosive increase in data rates require high speed complex modulation schemes with high spectral efficiency and large peak-to-average power ratios (PAPRs), such as high-order quadrature amplitude modulations (QAMs) and orthogonal frequency-division multiplexing (OFDM) are needed. In addition, due to the nature of modern society that must always be connected, battery life is also becoming increasingly important. As a result, due to the complex modulation that requires high PAPR, efficiency in the power Back off (PBO) state as well as maximum power is becoming more critical. From a receiver perspective, massive RF applications lead to a crowed spectrum, making receivers susceptible to mutual interference. Hence, along with cost and power consumption, interference robustness is becoming a major concern for the radios targeting these applications. As the demands of these modern communication systems become more diverse and complex, it is increasingly necessary to approach them in new ways.

Analog RF circuits have been studied intensely, but suffer from many circuit level and system level limitations. For example, analog PAs frequently operates at the output 1dB compression point (P_{1dB}) to ensure its amplitude and linearity, which reduces PA efficiency [1-4]. In addition, most analog RF circuits have a separate function with matching/filtering networks between each stage to ensure performance, which makes

further area-reduction difficult. Digital RF circuits are able to overcome many of these inherent limitations of analog approaches and their achievable performance has been highlighted in proportion to the recent technology of complementary metal-oxide-semiconductor (CMOS). Therefore, a lot of research has been conducted on digital RF circuits. This thesis work aims at expanding upon this. In particular, this dissertation presents several AM-PM behavior analyses and compensation techniques in digital Power Amplifiers (PAs) and circuit innovation to support completely integrated digital front-end circuitry, which can be one of solutions for modern communication systems.

Chapter 2 presents a summary of the past state-of-the-art works on digital PAs and mixer first receivers. Digital PAs can be largely divided into two types: a voltage mode method and a current mode method. This chapter explains the operating principles of the voltage mode and the current mode method, and describes the limitations of the existing method and the latest research on it. In addition, we explain the basic behavior of N-path filter, a receiver (Rx) method that splits capacitors like digital PA, and we also describe the latest studies. Understanding the operating principles and limitations on these TX/RX circuit architectures the state-of-the-art will help understand the motivation operation of the proposed techniques in this work.

Chapter 3 presents a digital power amplifier AM-PM compensation technique utilizing a single transformer footprint. The AM-PM distortion behavior of the current mode/voltage mode PAs is detailed and an AM-PM compensation technique for both modes is introduced. The proposed architecture provides enhanced linearity through adaptive biasing and hybrid current/voltage mode Doherty-based power combining, which can also operate over broadband.

Chapter 4 proposes a new bidirectional class-G digital Doherty switched capacitor transmitter and N-Path quadrature receiver in CMOS. Through sharing on-chip capacitor banks, typically occupying a major portion of the digital Tx or Rx chip area, as well as the RF passive matching networks, the overall size can be radically reduced. This proposed architecture has advantages not only in terms of area reduction but also in terms of performance. Based on the linearity principle analyzed in Chapter 3, the proposed structure also has excellent linearity, and also shows an analysis of the efficiency that depends on the sequence of operation in which each cell is turned on.

Chapter 5 provides a conclusion to this dissertation.

CHAPTER 1. INTRODUCTION

Recently, there is a growing amount communication platform such as smart factory, IoT, and portable devices, each of which transmit and receive various data among another. Due to this increased communication speed and data traffic, new technologies are being explored for more linear and broadband hardware to satisfy the growing demand. In addition, in order to fully take advantage of the available frequency bandwidth while still supporting explosive data rates, highly spectral efficient modulation schemes are being developed and employed such as high-order quadrature amplitude modulations (QAMs) and orthogonal frequency-division multiplexing (OFDM). However, these modulation schemes put strict requirements on the transmitter (Tx) hardware. QAM and OFDM have high PAPR which degrades the Tx's modulation efficiency and places stricter linearity requirements. In addition, communication hardware should be as compact as possible for various platforms. Therefore, we have design challenges of implementing broadband, linear, efficient, and compact TX designs to fully take advantage of the available frequency spectrum. Moreover, in the case of PA, the last active circuit stage of transmitter and most critical for performance, there are various trade-off relationships, as shown in figure 1-1[5], and it is the stage of the greatest power consumption. Because this is closely linked to battery life, efficient power consumption according to RF output power is particularly essential for mobile devices. Power saving techniques are become even more important in applications such as multi-in multi-out (MIMO), which are used to achieve high data rates in a single system but whose power consumption scales by the number of array elements.

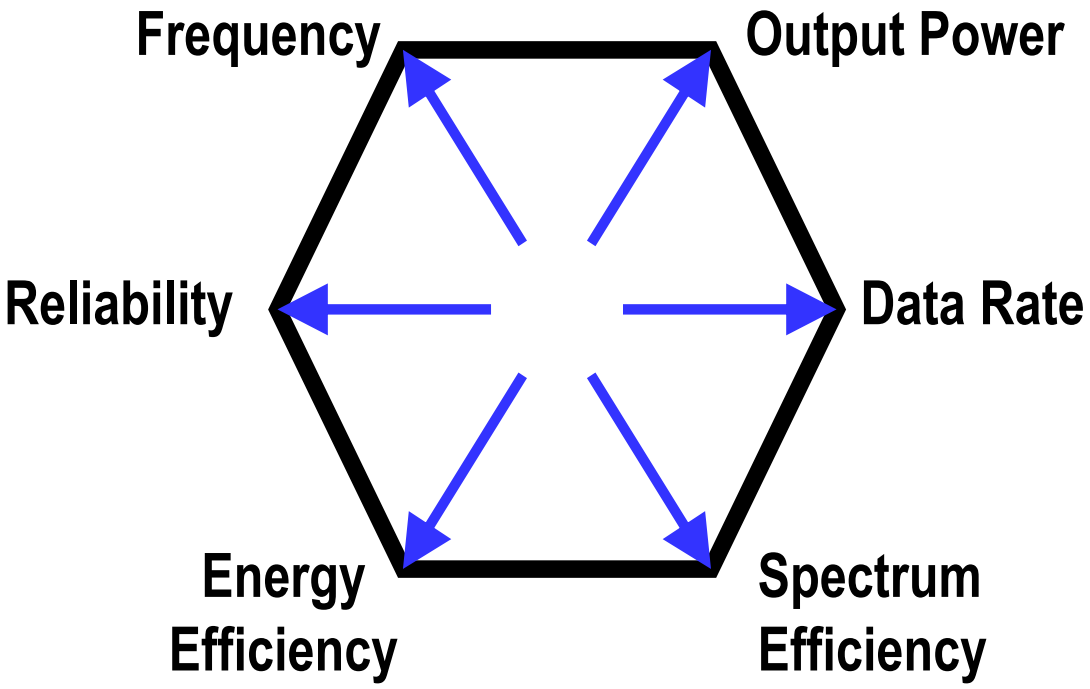


Figure 1-1 PA design trade off relationship

Several broadband analog PAs are recently reported to support multiple RF bands and standards [6-10] but analog PAs inherently suffer from low efficiency. Furthermore, analog PAs often operate from the output 1-dB compression point (P_{1dB}) to ensure sufficient amplitude and phase linearity, which is generally at the 1- 3dB power back off (PBO) point from the PA saturated output Power (P_{sat}) and thus results in reduced PA efficiency. For these reasons, digital power amplifiers (DPAs) and transmitters are one of the most promising technologies as alternative options. CMOS can be used to create high integrability at a low price, combine components such as the Digital-to-Analog converter (DAC), mixer, etc., within a single block, reducing area and power overhead [11]. In addition, digital PAs continue to become more attractive in terms of switch speed and

power consumption as process technology advances. Moreover, unlike analog power amplifiers, digital PAs theoretically achieve 100% drain efficiency. While current work only can demonstrate drain efficiencies as high as 49.4% [12], it only further verifies that the achievable efficiency is limited by the PA implementation rather than the theoretical foundations and that further research is required to truly take advantage of this PA architecture.

As mentioned earlier, modern communication systems require complex modulation schemes, which require stricter standards not only for efficiency but also for linearity. However, several technologies that increase efficiency could deteriorate the linearity[13, 14]. As a result, Digital Pre-Distortion (DPD) techniques are also studied to compensate for nonlinearity, however this also requires more data processing, increases power consumption, and limits the modulation bandwidth. Therefore, research on inherent PA linearity is becoming increasingly important.

Digital circuits can also offer benefits for the receiver implementation, particularly for seamless transmitter integration for full transceiver (TRX) implementation. The traditional receiver architectures often uses Surface Acoustic Wave filters (SAW) or Film Bulk Acoustic Resonator (FBAR) filters with high-Q values, but it is non-tunable, requiring multiple filters present for multiband operation, resulting in increased overall cost and area overhead[15]. However, N-path filter-based mixer first receivers provide inherent sharp filtering during down conversion, removing the need for external filters. In addition, since the mixer first receiver can also take advantage of reduced power consumption and

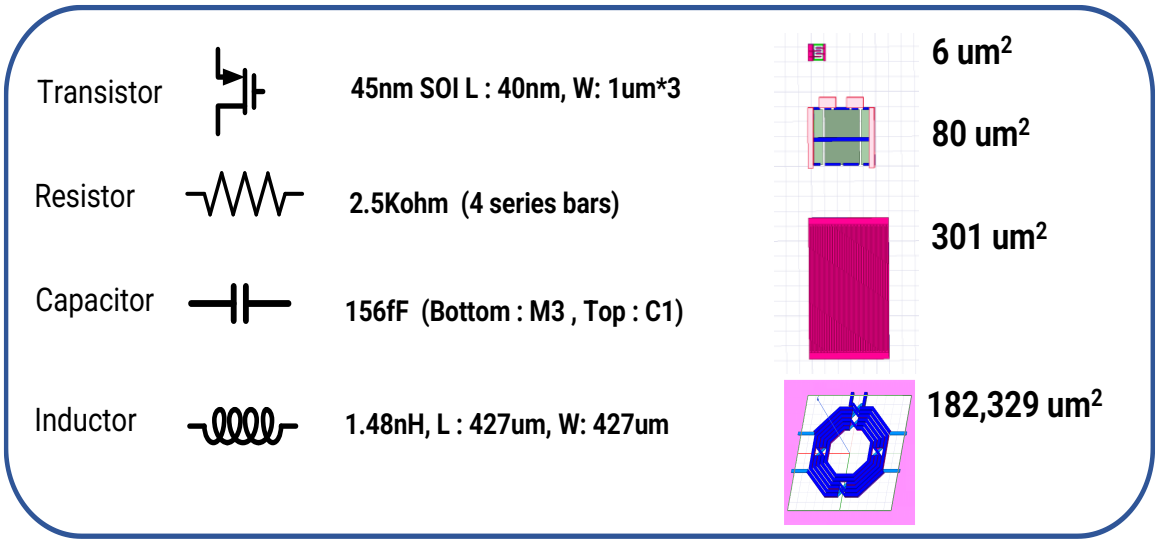


Figure 1-2 Examples of each component size used in CMOS digital PA.

improved switch speed with the continued development of CMOS, like digital PA, it will be important to study together with the research of digital PA.

As mentioned earlier, the RF digital TRX frontends naturally offer excellent RF performance, reconfigurability, and wideband operations, but they commonly rely on architectures based on binary and/or unary arrays of sliced active and passive devices, which can result in a substantial area overhead. Figure 1-2 illustrates an example of the size of each element used in a CMOS digital PA. As shown in the figure, each element has a different size physically required, and it would be very important in researching digital circuits to make optimum use of large area elements such as output matching networks (inductors) and capacitors for compact implementation.

In summary, existing digital RF hardware offers many advantages, however there are several limitations that prevent them from becoming widely adopted. Some of the issues are listed below:

1) Although digital PA can theoretically achieve 100% Drain Efficiency (DE), in practice, non-idealities limit the achievable DE below 100%. Moreover, by using complex modulation schemes for modern communication systems, high PAPR is unavoidable. However, traditional digital PA circuits are less efficient at PBO state. Therefore, it is a need for research that not only increases the DE at the peak output power, but also improves the efficiency in the PBO status to operate efficiently in complex modulation schemes.

2) Linearity is crucial for supporting the complex modulation methods used in modern communication. However, the linearity worsens the more technologies are applied to enhance high efficiency in PBO states in line with high power and high PAPR. The DPD technology could be a solution to this when linearity is poor, however it has several limitations. First, it must characterize the PA precisely to cancel out the PA non-linearity. Second, DPD inevitably increases the power consumption and complexity of the overall system. Finally, even with DPD, not all nonlinearities can be eliminated, especially as the load on the antenna varies as the PA non-linearities are load dependent. Therefore, it is necessary to have inherently good linearity performance.

3) In modern communication systems, where IoT and small portable devices are in high demand, miniaturization of RF circuits is becoming increasingly important. In the case of digital circuits, multiple functions can be applied to a single chip to reduce the total area. However, these digital circuits still require bulky passive elements to ensure operation. For example, switched capacitor PAs require a large capacitor bank with scaled switches. The N-path mixer-first

RXs also require large differential capacitor banks, which scale with the quadrature operations and number of N-paths. Therefore, a new architecture is needed for how to utilize physically large capacitors well in digital circuits. In addition, it is important to implement the minimum number of output matching networks that occupy the largest area.

During my five-year study in the Georgia tech GEMS/ ETH Zurich IDEAS lab, the major research theme of my PhD consisted of new digital PA/front-end architectures and innovative circuits techniques, to achieve compact, linear, and efficient operation for small-size applications such as IoT and portable devices. Several major contributions of my PhD thesis are highlighted below:

1) We propose a compact one footprint hybrid Doherty digital PA. The proposed structure improves linearity and realizes miniaturization by connecting the current mode and voltage mode PA to one output matching network. A proof-of-concept PA has been designed and fabricated in 45nm RF CMOS SOI process, which achieves a peak PAE of 37.6% with a P_{sat} of over 21.8dBm from 1.2 to 2.4GHz. The PA also achieves a 1.2×/1.4× PBO efficiency enhancement, compared to the ideal class-B at 3/6dB PBO at 1.2GHz. This proposed digital PA supports 20MSym/s 64-quadrature amplitude modulation (QAM) at 14.8dBm average output power and 22.8% average PA DE while maintaining error vector magnitude (EVM) lower than -23dB without any phase pre-distortion.

2) We proposed a single footprint transformer for current/voltage mode hybrid digital PA. This is the first implementation to combine current mode and voltage mode digital PA in a single footprint. This allows hybrid digital PA using current mode and voltage mode to be implemented in a small area. Furthermore, this single footprint transformer operates broadband.

3) We analyze the principle of AM-PM distortion behavior of current mode DPA and proposed adaptive biasing technique to mitigate the nonlinearity of current mode DPA. Moreover, we analyze the principle of AM-PM behavior of voltage mode DPA as well and proposed class-G DPA as hybrid Doherty digital PA architecture. In addition, it was analyzed that the efficiency of Doherty digital PA varies according to the sequence of operation in which PA is turned on, and the optimal sequency of operation was applied accordingly.

4) We propose a fully integrated bidirectional class-G digital Doherty switched capacitor transmitter and N-Path Quadrature receiver (Rx) in CMOS. Through sharing on-chip capacitor banks, typically occupying a major portion of the digital TX or RX chip area, as well as the RF passive matching networks, the overall size can be radically reduced. Moreover, the overall performance could be further improved by eliminating the need for an integrated T/RX switch and its corresponding loss and area overhead. As a proof-of-concept, the joint bidirectional class-G digital Doherty switched-capacitor TX and N-path Quadrature RX through capacitor bank sharing is implemented in a 45-nm CMOS SOI process. The TX demonstrates a Pout 1dB bandwidth (BW) of 1.6-3.1 GHz, a fractional BW >63%, and peak output power (P_{out}) of 22.5dBm at

2.4GHz. The peak drain efficiency (DE) of the TX is 49.5% at 1.8GHz and 41.5%/38.7%/31.6%/18.1% for the peak/2.5/6/12dB power back off (PBO) at 2.4GHz. The DE improvement compared to class-B PA is 1.24×/1.51×/1.72× at 2.5/6/12dB PBO. The TX is measured using 64-QAM/20MHz modulation without the use of AM-PM pre-distortion or pattern based DPD. It achieves an excellent -27.1dB EVM, -31.31dBc ACLR, 14.6dBm average Pout and 25.8% average DE at 1.6GHz. The RX achieves a noise figure (NF) of 7.6dB at 2.2GHz and a conversion gain of 17dB with a 12 MHz bandwidth. In addition, the proposed RX front-end achieves < -60 dBm LO leakage over the operating frequency range.

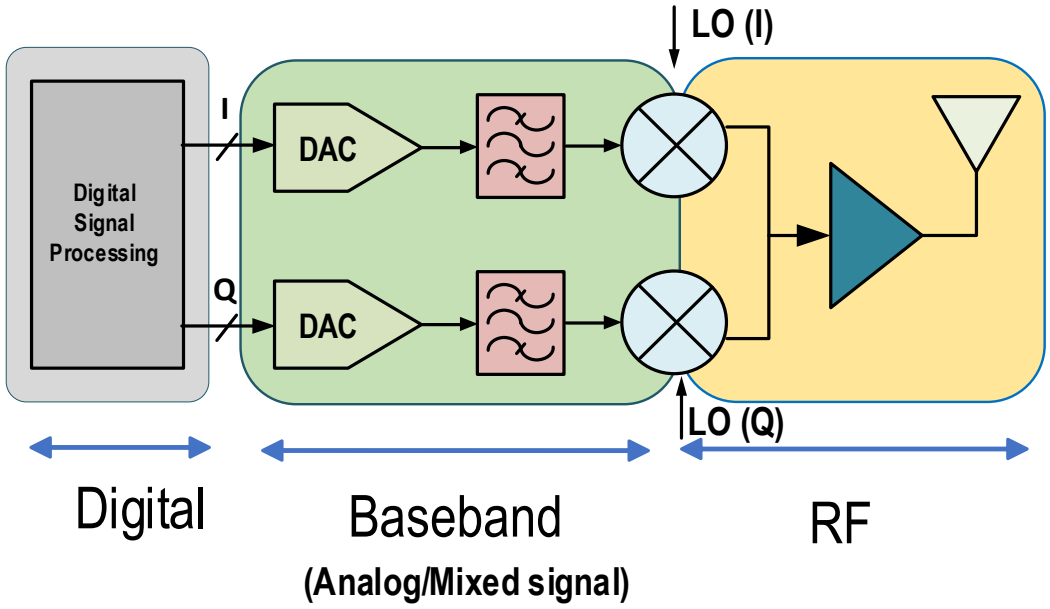
The remainder of this dissertation is organized as follows. Chapter 2 details the past work in digital power amplifier and mixer first receiver. In Chapter 3, the behavior of non-linearity of digital PA both current mode and voltage mode will be explained. We also propose a single footprint hybrid (current/voltage) digital PA that compensates for its AM-PM distortion. A novel bidirectional front-end circuit is detailed in Chapter 4. This dissertation is summarized in Chapter 5.

CHAPTER 2. PRIOR ART ON DIGITAL POWER AMPLIFIER AND MIXER FIRST RECEIVER

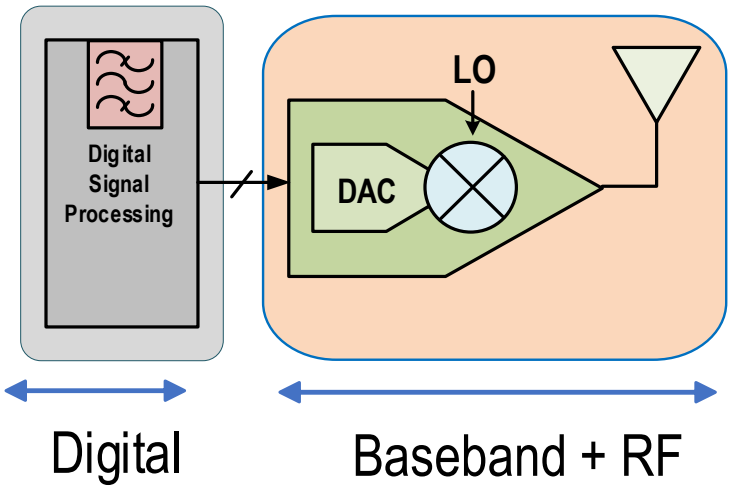
This chapter presents a study on past works on digital TXs/RXs to better understand their inherent limitations in linearity and miniaturization and to motivate the proposed digital PA and bidirectional digital front-end architecture covered in chapter 3 and 4. We discuss the digital PA and mixer first receiver, in this section, respectively.

2.1 Prior Work in Digital Power Amplifier

With the advancement of CMOS technology, digital power amplifiers are in the spotlight[16-22]. In particular, as shown in Fig 2-1, unlike conventional analog Tx architecture, the digital Tx structure can integrate multiple circuit functions within a single chip, making it a very attractive research topic in modern communication that requires miniaturization for IoT and portable devices. In addition, due to the increase in switch speed with the development of CMOS, it is possible to operate at higher frequencies and consume less power, causing many studies on digital PA to become active. Furthermore, digital PAs can achieve 100% drain efficiency as the loss at the amplifier can be zero if the switching device is assumed to be “ideal”. On the other hand, in other amplifiers such as analog PA, the theoretical efficiency is inevitably less than 100% due to the limitations of the linear mode operation of the devices [23]. Thus, the possibilities of these digital amplifiers are attractive enough to be further researched in the future.



(a) Analog Tx architecdture



(b) Digital Tx architecture

Figure 2-1 (a) Analog Tx architecture (b) Digital Tx architecture.

These digital PA can be divided into two main types: the voltage mode DPA and current mode DPA. We will now look at the basic operation and the past studies of each mode of digital PA.

2.1.1 Voltage Mode Digital PA (SCPA).

Switched Capacitor Power Amplifier (SCPA) is one of the popular voltage mode digital PAs. It consists of capacitor arrays, which are switched between the ground and the supply voltage or held at a signal ground at the carrier frequency. It operates like a class-D PA with a capacitive voltage divider in series resonance with the matching network.

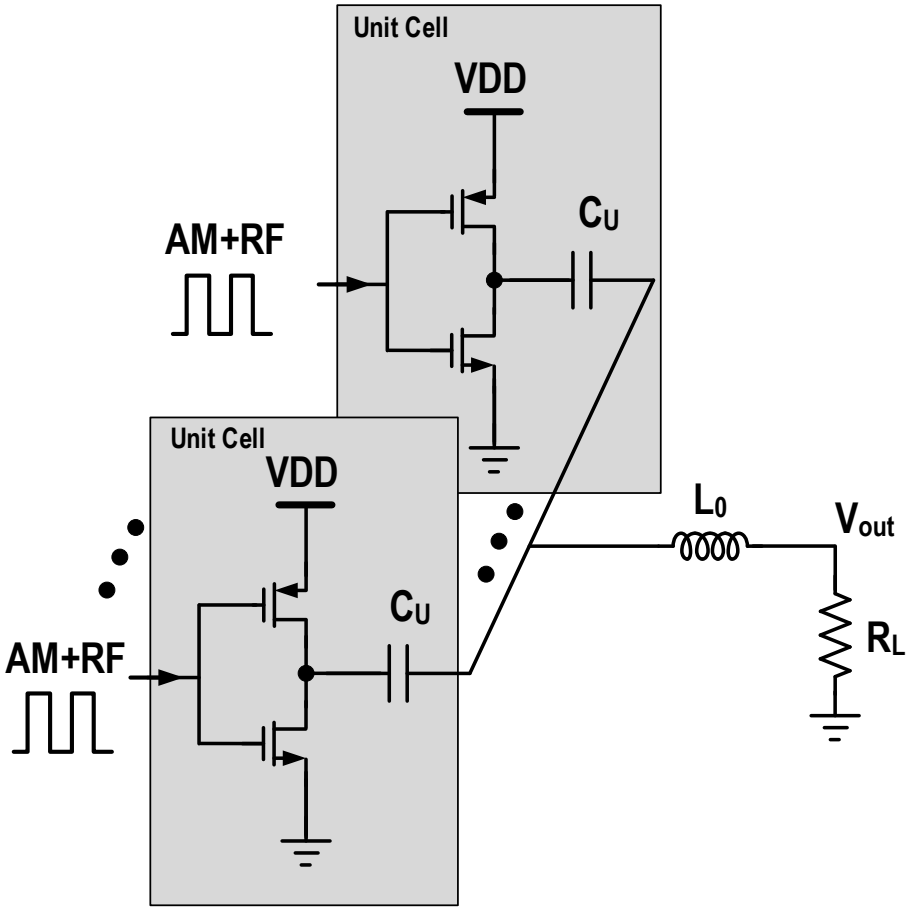


Figure 2-2 Schematic of SCPA

The output matching network resonates out harmonic frequency, thus only the fundamental component at the RF carrier frequency flows to the output. The conventional schematic of SCPA is shown in Fig. 2-2. The input signal of the cell with the AM code enabled goes into square waves. This square wave is filtered by bandpass matching network so only the fundamental harmonic goes through, saving wasted harmonic power. Hence, a resonant tank consisting of capacitor array (C_u) and inductance (L_0) is inserted in series with R_L in order to allow only the sinusoidal current though R_L [24]. Ideally, there is no overlap between the current waveform and the voltage waveforms, causing there to be no switching loss, which in principle achieves 100% efficiency. Figure 2-3 shows the block diagram and equivalent circuits of ideal single-ended SCPA. This architecture control output amplitude by selecting the number n of capacitors switched between VDD and GND among the total number N of capacitors in the array. At this time, high accuracy is achieved by utilizing the precision capacitance ratio traditionally provided by CMOS. However, the voltage mode DPA has low output power because the output voltage swing cannot exceed its supply voltage. The output voltage swing and output power of the SCPA are shown in the equation below:

$$V_{out} = \frac{2}{\pi}\left(\frac{n}{N}\right) \times V_{DD} \tag{2-1}$$

$$P_{out} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2 \times \frac{{V_{DD}}^2}{R_{opt}} \tag{2-2}$$

For this reason, research has been conducted to increase the output power of voltage mode DPA through various technologies such as device stacking or complex power combining

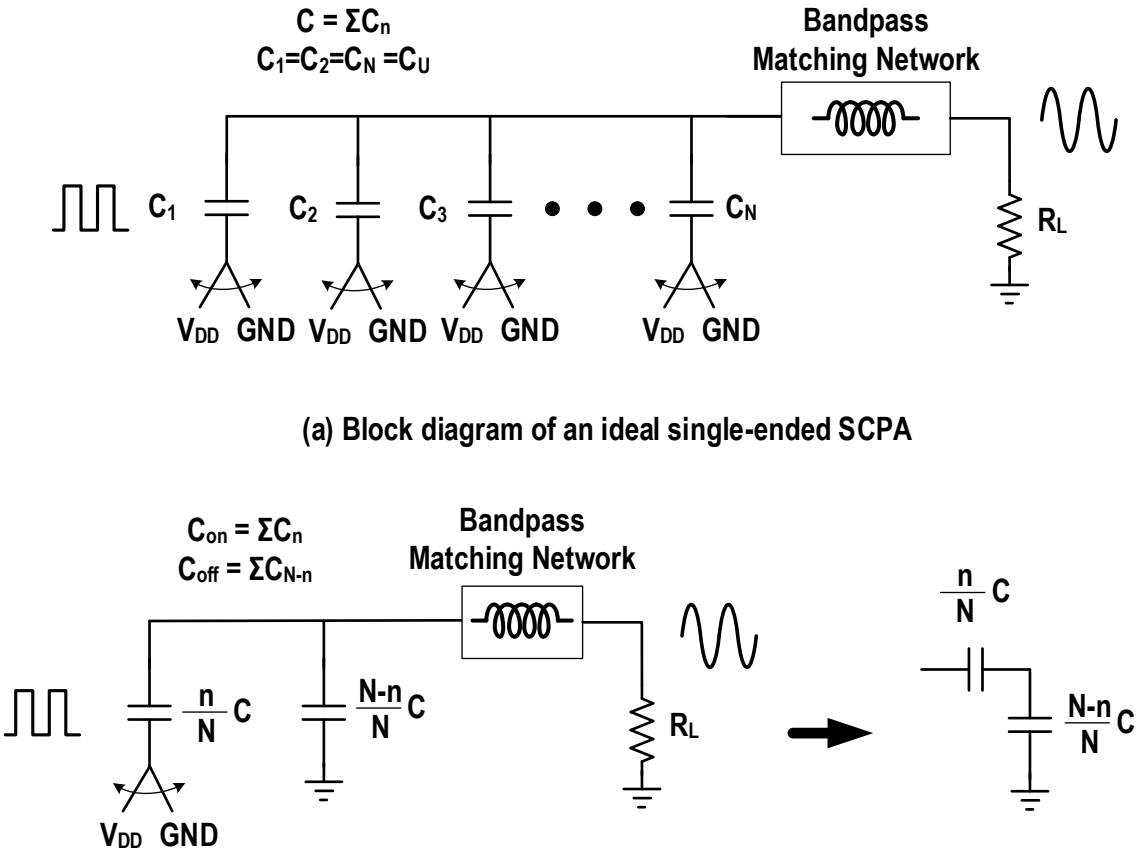


Figure 2-3 (a) Block diagram of an ideal single-ended SCPA and (b) Equivalent circuit of an ideal single-ended SCPA

output matching networks [25]. Figure 2-4 also shows past research to increase the efficiency and output power of voltage mode digital PA. The Doherty PA architecture (Fig. 2-4 (a)) is a popular solution to achieve PBO efficiency enhancement. It achieves the PA PBO efficiency enhancement through active load impedance modulation. The Class-G structure (Fig. 2-4 (b)) shows efficiency enhancement in PBO status through supply voltage

modulation. In addition, the subharmonic switching structure (Fig. 2-4 (c)) achieves improvement in PBO efficiency by toggle the switching PA cells at the subharmonic of the

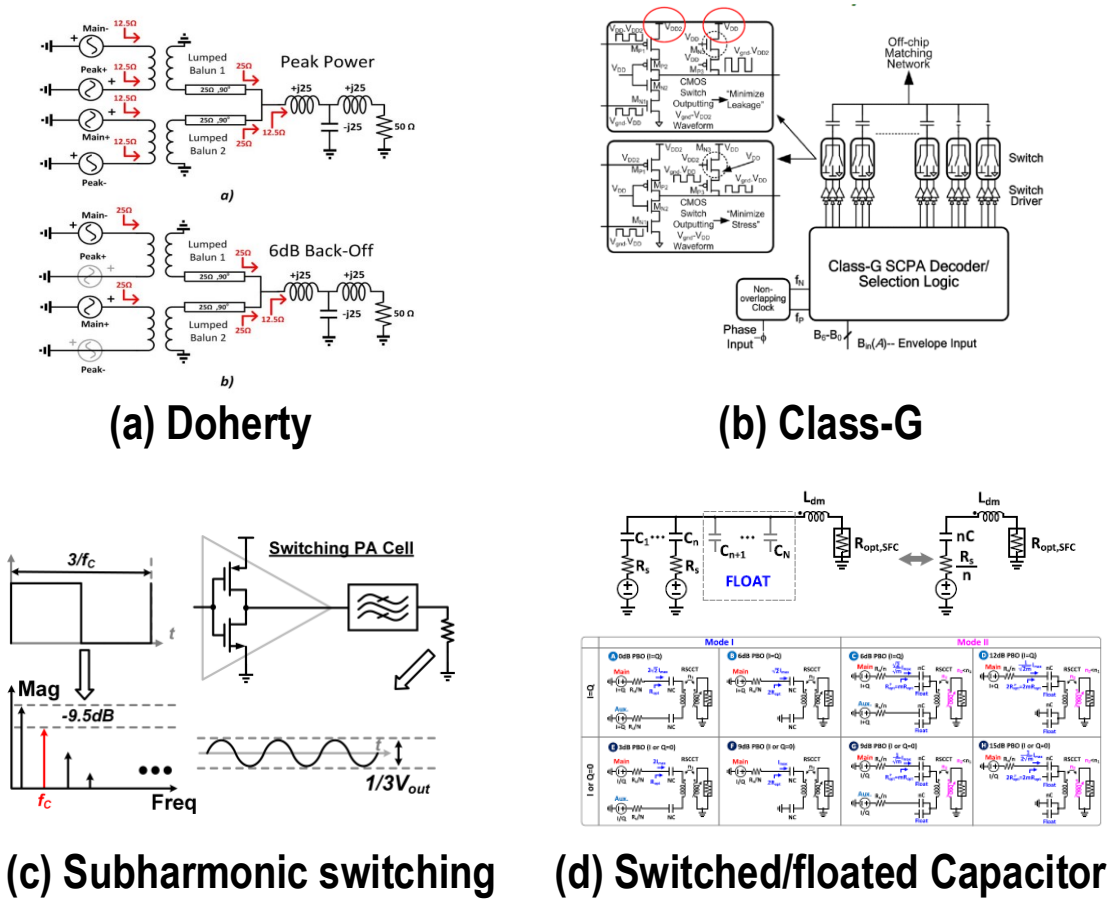


Figure 2-4 Prior work in voltage mode DPA (a) Doherty digital PA[26] (b) Class-G digital PA [27] (c) Subharmonic switching (SHS) digital PA [28] (d) Switched/floated capacitor PA (SFCPA) [29].

carrier frequency, e.g., one-third of the carrier frequency. This architecture can reduce the conduction loss of the PA, switching capacitance dynamic loss, and provide better impedance matching. Finally, the switched/floated capacitor power amplifier (Fig. 2-4 (d)) reduces dynamic power consumption by expanding a capacitor connection to floating status from VDD or GND status. This increases the efficiency at power back-off status by

reducing dynamic power consumption that is needed to charge/discharge by floating an unused capacitor array. As described above, various studies have been conducted in voltage mode digital PA to increase power and efficiency, but there is a trade-off for size, efficiency, output power, linearity, and complexity. In particular, since linearity tends to decrease as various techniques are applied, research considering linearity is increasingly necessary.

2.1.2 Current Mode Digital PA (Class D^{-1})

As the demand for operating at higher frequencies increases, research on the current mode digital PA is also increasing [14, 30-32]. This is because the voltage mode DPA has some limitations as the operating frequency increases. For the voltage mode DPA, the drain capacitance of the transistor is not part of the matching network and must be charged and discharged every cycle, resulting in CV^2f power dissipation. Therefore, the loss scales with frequency. Another disadvantage of the conventional voltage mode DPA is that PMOS devices that have higher on-resistance than NMOS devices are used. In general, the PMOS switch size needs to be increased 2-3 times to achieve a similar on-resistance to NMOS switches due to the difference in mobility of the devices, which significantly increase input capacitance significantly and makes the driver design more difficult.

The model of current mode DPA (class-D^{-1}) is shown as Fig. 2-5. This is dual of a conventional class-D PA, which is voltage mode PA. In class-D^{-1} PA, the current through the transistor is a square wave, whereas the output voltage is sinusoidal. There is a parallel-connected filter, with resonant frequency set to the carrier frequency. Due to the filter

resonance, there is no voltage across the transistors at each switching time and so-called zero voltage switching (ZVS) is achieved. Even if the transistors have some output capacitance, it can be incorporated as part of the output parallel filter.

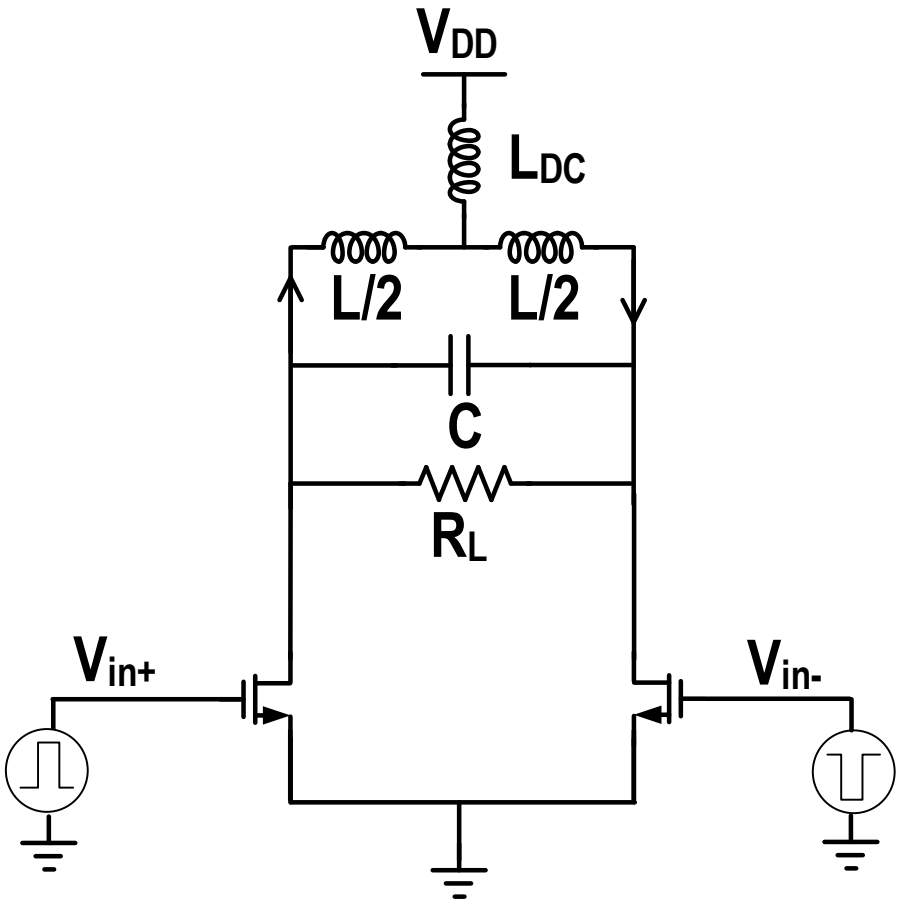


Figure 2-5 Model of the class-D^{-1} power amplifier.

Another advantage is that unlike SCPA, the class D^{-1} can have their output swing beyond the supply voltage and thus achieve higher output power. The output voltage swing and output power of the class-D^{-1} are shown in the equation below:

$$V_{out} = \pi\left(\frac{n}{N}\right) \times V_{DD} \tag{2-3}$$

$$P_{out} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2 \times \frac{{V_{DD}}^2}{R_{opt}} \tag{2-4}$$

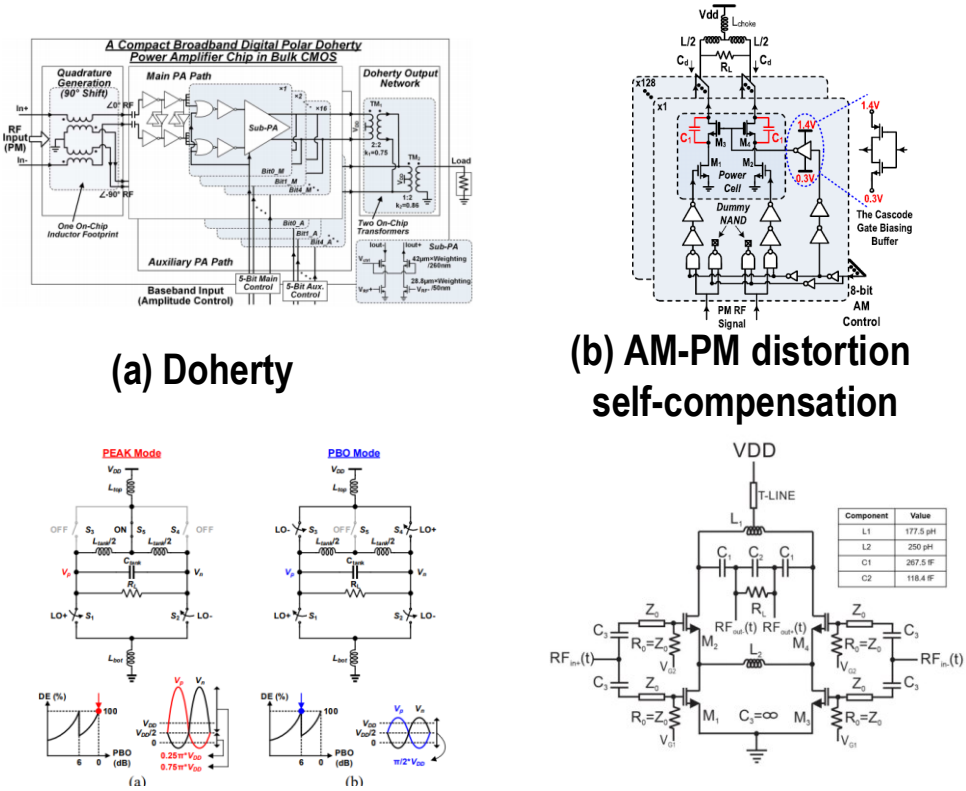


Figure 2-6 Prior work in current mode DPA. (a) Doherty mode PA [33] (b) AM-PM distortion self-compensation technique [34] (c) Single supply PBO efficiency enhancement [35] (d) 28GHz cascode in class-D^{-1} PA [36]

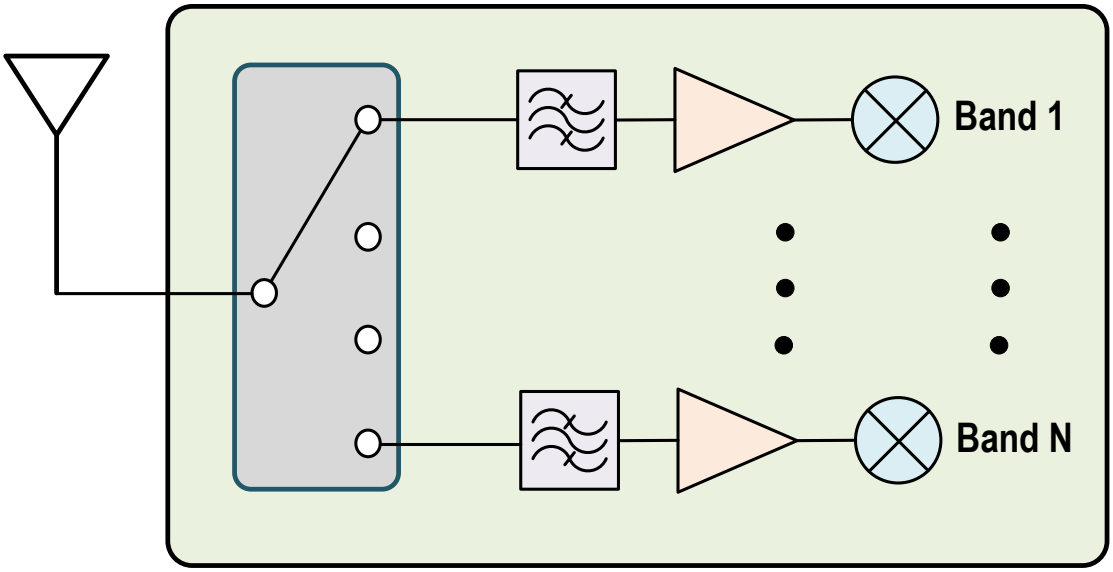
The current mode DPA has high output power, but relatively poor linearity. Although AM-AM distortion of current mode DPAs can be mitigated by optimum AM control code selection, they typically exhibit excessive AM-PM distortion. [13, 32, 37].

Therefore, research that can alleviate their AM-PM distortion is becoming increasingly important. Figure 2-6 also shows past research to improve the efficiency and the linearity of current mode digital PAs. The Doherty PA architecture (Fig. 2-6 (a)) is also a popular solution to achieve PBO efficiency enhancement through load impedance modulation and is a widely used solution in current mode DPA as well as in voltage mode DPA. AM-PM distortion self-compensation technique (Fig. 2-6 (b)) is applied by feedforward capacitors in differential cascode power cells. Through feedforward capacitors, the variation in the output capacitance is reduced to mitigate AM-PM distortion. Figure 2-6 (c) shows that the output voltage is changed through additional switches to increase the PBO efficiency even with single supply voltage. Figure 2-6 (d) is current mode DPA to operates 28GHz by employing a stacked topology in 22nm FDSOI. In order to use high output power, it uses the cascode configuration to prevent breakdown. As shown above, various studies have been conducted to improve efficiency, and output power in current mode DPA, but due to large AM-PM distortion, DPD is required for modulation measurement, except for Fig. 2-6 (b) to which the technology for AM-PM compensation is applied. Accordingly, further research is needed to improve linearity for current mode DPA in order not to use complex DPD.

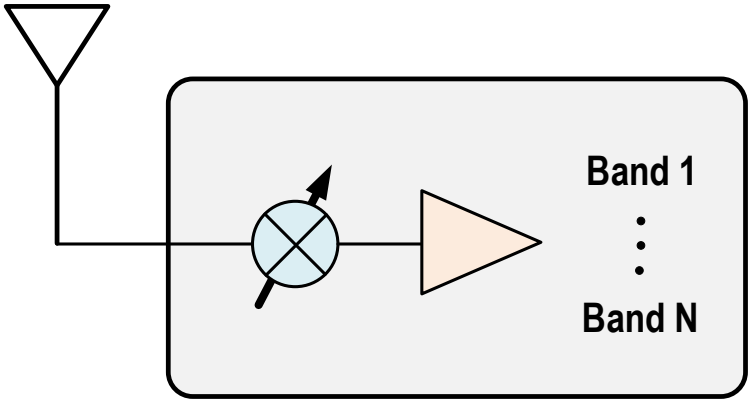
2.2 Prior Work in Mixer First Receiver

The transmitter is not the only thing we need to focus on in the complexity of the spectrum. Due to the growing number of devices, complex spectrum, vulnerable receivers due to mutual interference, and studies of low power and small size, like transmitters,

indicate that more research is needed on receivers as well as transmitters. Accordingly, we should also look at CMOS receivers together. To attenuate the blockers and enhance their out-of-band (OOB) selectivity, CMOS receivers typically use high-Q external filters [e.g., surface acoustic wave filters (SAW) and film bulk acoustic resonator (FBAR)] or off-chip and on-chip LC resonant tanks. Figure 2-7 shows the block diagram of the conventional



(a) Conventional receiver structure



(b) Mixer first receiver structure

Figure 2-7 Block diagram of (a) Conventional receiver structure (b) Mixer first receiver structure

receiver and the mixer first receiver structure. Conventional receiver's filters are not tunable, impose both size and cost, and introduce 2-3 dB in-band loss. However, the mixer first receiver can be a SAW-less solution compatible with CMOS integration with a single chip in a modern communication system that requires multi-band and miniaturization. Also, it does not use a LNA, so it consumes relatively less power consumption. As a result, passive mixer-first receivers have been much studied recently by this demand[38-45].

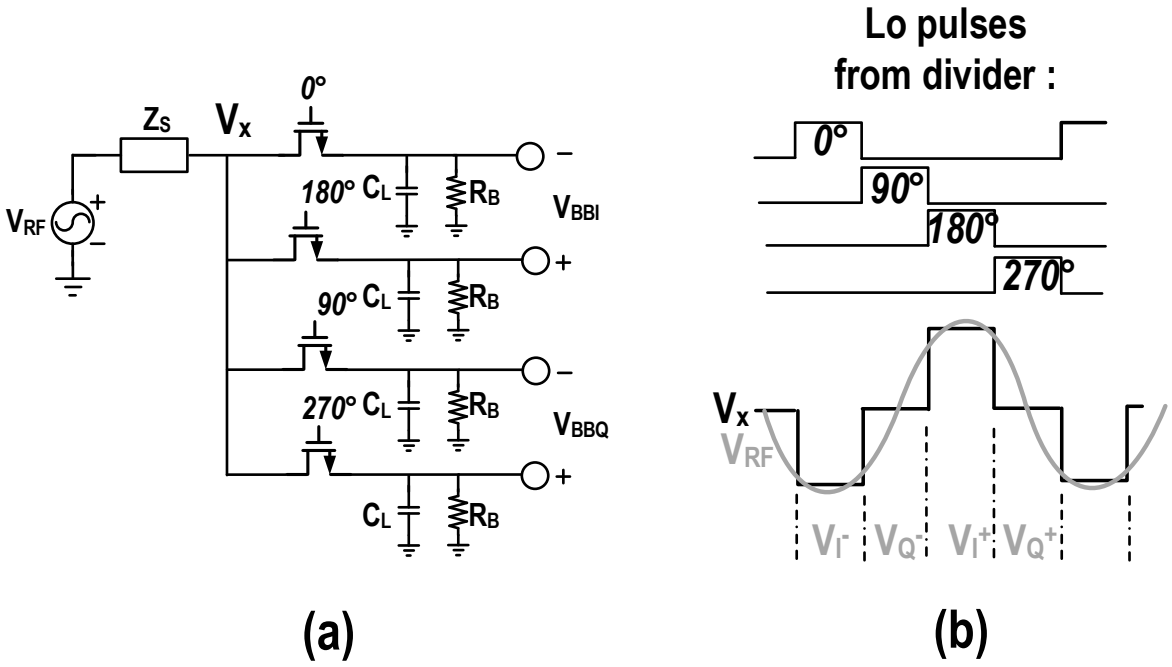
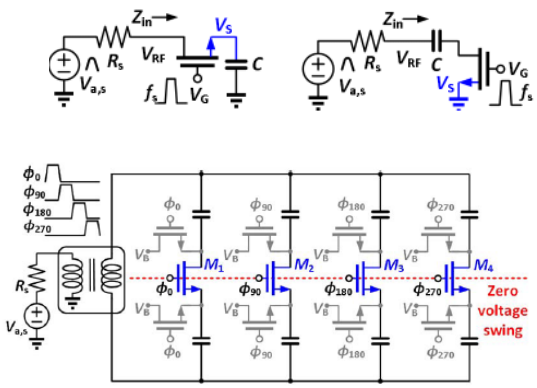


Figure 2-8 (a) Model of 4 phase passive mixer with sampling capacitor C_L and load resistor R_B (b) LO driving waveforms and resulting virtual voltage at Vx

Figure 2-8 shows the model of 4 phase passive mixer with sampling capacitor C_L and load resistor R_B and LO driving waveforms. A quadrature passive mixer is connected directly to an antenna. Each switch is loaded with a capacitor, and a resistive load. Non-overlapping LO pulses with a 25% duty cycle are used to drive the switches. We can regard

the four parallel switch resistances as one as the antenna port will only see one path at a time due to the non-overlapping nature of the pulses. The signal from that LO pulse is sampled onto the corresponding switch as each switch closes. The baseband resistors R_B are loaded into four capacitors. The switches sample the RF voltage onto four capacitors loaded by the baseband resistors R_B. Due to the phase-split nature of the LO, mixer, differential baseband signal both I (from the 0° and 180° switches) and Q (from 90° and 270°) components are produced [46]. A passive mixer performs the same basic frequency translation function as an active mixer, with the additional feature of bidirectional impedance transparency. A passive mixer simultaneously up-converts the signals on its baseband port and down-converts those on its RF port [47]**.** This two-way frequency translation property provides passive-mixers with a number of benefits over active-mixers with little penalty in performance, providing new opportunities as well as distinct design challenges.

Figure 2-9 shows prior work for the mixer first receiver. In Figure 2-9 (a), bottom-plate mixing technique to improve linearity by reducing the gate-source voltage modulation of the MOSFET switches is proposed. Figure 2-9 (b) also provides enhanced selectivity by using capacitive negative feedback across the baseband amplifier serves as a blocker bypassing path, while an extra capacitive positive feedback paths synthesizes a complex pole pair at the input of the BB amplifier, which is upconverted to the RF port to obtain steeper RF bandpass filter roll-off and reduced distortion. The capacitive stacking technique in Fig. 2-9 (c) achieved 2× voltage gain after down conversion by reading out the voltage from the bottom plate of N-path capacitors instead of their top plate. The mixer



(a) Bottom plate mixing

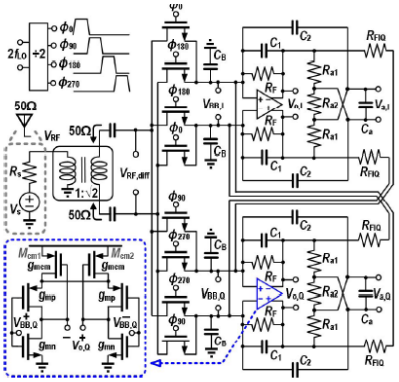


Fig. 6. Circuit details of the proposed RX and low-noise BB amplifier.

(b) Enhanced selectivity

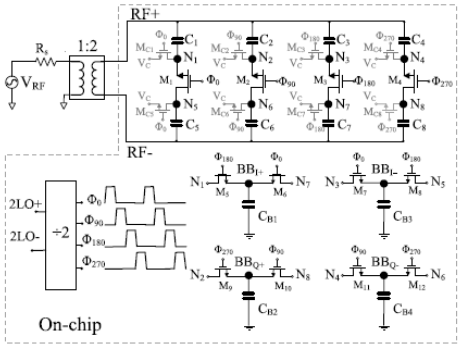


Fig. 10. Complete architecture of the implemented RF front end.

(c) Capacitive stacking

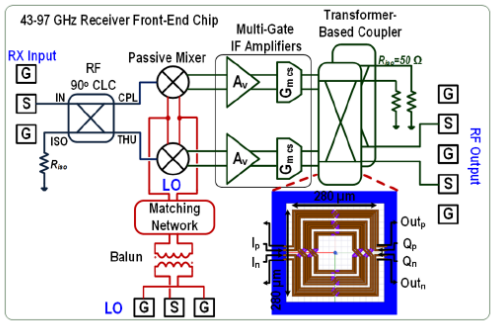


Fig. 2. Proposed receiver front-end.

(d) mmWave mixing

Figure 2-9 Prior work in Mixer first receiver (a) Bottom plate mixing[48] (b) enhanced selectivity[49] (c) Capacitive stacking[15] (d) mm-Wave mixing [50]

first receiver also operates millimeter-wave (mm-Wave) frequency (43-97 GHz) by implementing low-IF topology as shown in study Fig.2-9 (d). In the case of mixer first receivers, gain and selectivity performance are improved through various approaches, but the capacitor size determines the overall size as it is implemented using a capacitor array like digital PA.

2.3 Conclusion

Multiple studies have been demonstrated in literature on digital RF circuits. To have high power, broadband, small size, linearity, and high efficiency at PBO status required by modern communication system, digital PAs have been studied in various ways, respectively, voltage mode DPA and current mode DPA. However, each study has a different trade-off, and accordingly, research on techniques that can create synergetic effects is needed. It also requires careful implementation and fundamental understanding of the mechanisms behind the PA non-idealities. Therefore, this paper analyzes the characteristics of current mode PA and voltage mode PA and proposes a structure that can complement each other based on this. It should be noted that none of the class-G DPA studies, which are frequently used in digital PA to improve PBO efficiency, have proven the underlying principle of its AM-PM distortion. In addition, it should be accompanied by research focusing on improving the entire system performance of the through seamless integration of the Tx/Rx as well as integration of the current/voltage digital PA. Therefore, this paper proposes new circuit architectures that improve both the TX inherent performance and integrability of the TX and RX in a compact form factor.

CHAPTER 3. A DIGITAL POWER AMPLIFIER WITH BUILT-IN AM-PM COMPENSTAION AND A SINGLE-TRANSFORMER OUTPUT NETWORK

3.1 Introduction

Modern wireless communication systems adopt spectrally-efficient modulation schemes to enhance the link throughput within a given frequency bandwidth at the cost of a large PAPR. This poses stringent requirements on the energy efficiency of RF power amplifiers for both peak output power and also at PBO to ensure efficiency under modulation. Therefore, there is an increasing interest in exploring PBO efficiency enhancement technique to achieve high PA average efficiency under these high-PAPR modulation schemes [28, 51-54]. Doherty load modulation is one of the widely used techniques to boost PA PBO efficiency. However, when the Doherty PA's main path and auxiliary (Aux) path do not cooperate well together, they have limited linearity and require large area to support the load modulation output matching network [33, 55, 56]. Outphasing PAs support PBO efficiency enhancement but require significant baseband computation to generate the outphasing signals often with limited dynamic range [57-60]. Envelope Tracking (ET) PAs exhibit a trade-off for the envelope tracker's own efficiency, dynamic range, speed, and accuracy, which are unsuitable for high-speed (>100MHz) and high-PAPR signals [61-64].

Analog PAs are widely used in modern wireless communication systems. However, their designs cannot be readily transferrable across process nodes, benefit from device scaling, or support direct synthesis. Thus, there is an increasing interest in digital power amplifier (DPA) research [65-72]. DPAs support the ability to implement multiple functionalities within one compact formfactor block, extensive digital reconfigurability,

and performance and design tracking aggressive CMOS process scaling.

A DPA can be generally divided into two categories based on their power cells, the current mode DPA such as the class-D^{-1}, and the voltage mode DPA such as the Switched Capacitor Power Amplifier (SCPA). Current mode DPAs typically support higher output power levels for a fixed supply voltage as the output voltage swing can exceed the supply voltage, but they suffer from large signal non-linearities due to distortion [73-75], except for some recent designs which utilize built-in analog compensation techniques, such as AM-PM linearization [34]. Voltage mode DPAs achieve good linearity and efficiency but provide limited output power levels as their output voltage swing is lower than the supply voltage [26, 76, 77]. Recently, a hybrid technique that improves the linearity by implementing the current mode and voltage mode DPAs together has been demonstrated [37]. However, it sacrificed peak drain efficiency (DE) of the current-mode DPA by tuning on only half of its total power cells and suffers from area overhead and major passive loss penalty by connecting three transformers in series as its output matching network.

While a large amount of research to increase the PBO efficiency for complex modulation communication has been conducted, the techniques applied typically deteriorate the overall linearity [12, 29, 37, 78]. Therefore, many digital PAs inevitably use 2-dimensional digital predistortion (2D DPD) tables or models to compensate for their linearity. However, using 2D DPD comes with various limitations. First, it is necessary to accurately characterize the PA and create an inverse function in the 2D space. Second, it increases the system power consumption and complexity. Furthermore, it is often incapable of sufficiently cancelling all the PA nonlinearity. In particular, output impedance variations may aggravate DPD performance [79]. Therefore, it is essential to ensure intrinsic PA linearity with built-in linearization.

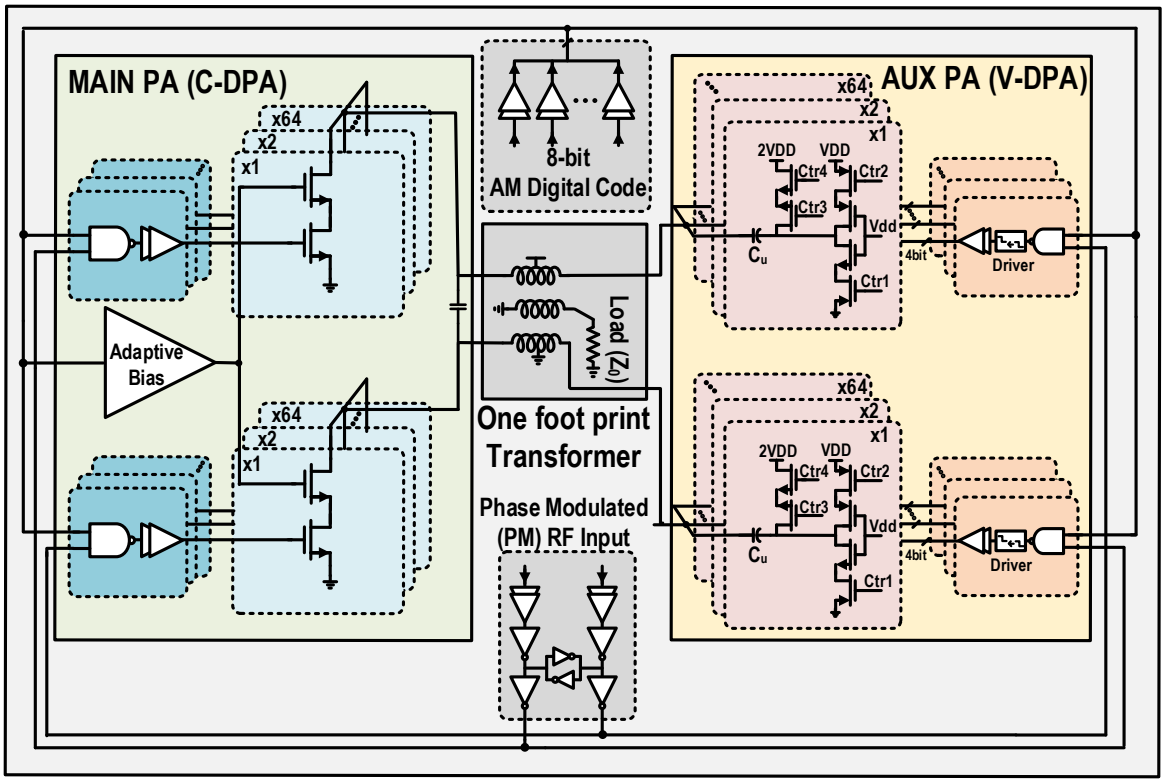


Figure 3-1 Top schematics of proposed hybrid polar Doherty digital PA.

To address the aforementioned issues, we propose a fully integrated single footprint hybrid current-voltage mode digital Doherty PA [80]. In our proposed DPA topology, adaptive biasing is implemented for the current mode DPA to minimize its AM-PM nonlinearity. A class-G DPA with its own AM-PM compensation characteristics is used for the voltage mode DPA, and a hybrid self-compensation technique consisting of a current mode DPA and voltage mode DPA are implemented using a single footprint transformer is used for the overall DPA. Note this reported design differs from the design in [81], in that it implements two paths as a single transformer, utilizes all cells in the current mode DPA using adaptive biasing scheme, and improves linearity and efficiency using characteristics of class-G DPA. This chapter is organized as follows. Section 3-2 introduces the proposed hybrid polar Doherty digital power amplifier architecture. Section 3-3 presents the analysis of AM-PM distortion within the current/voltage mode DPAs and

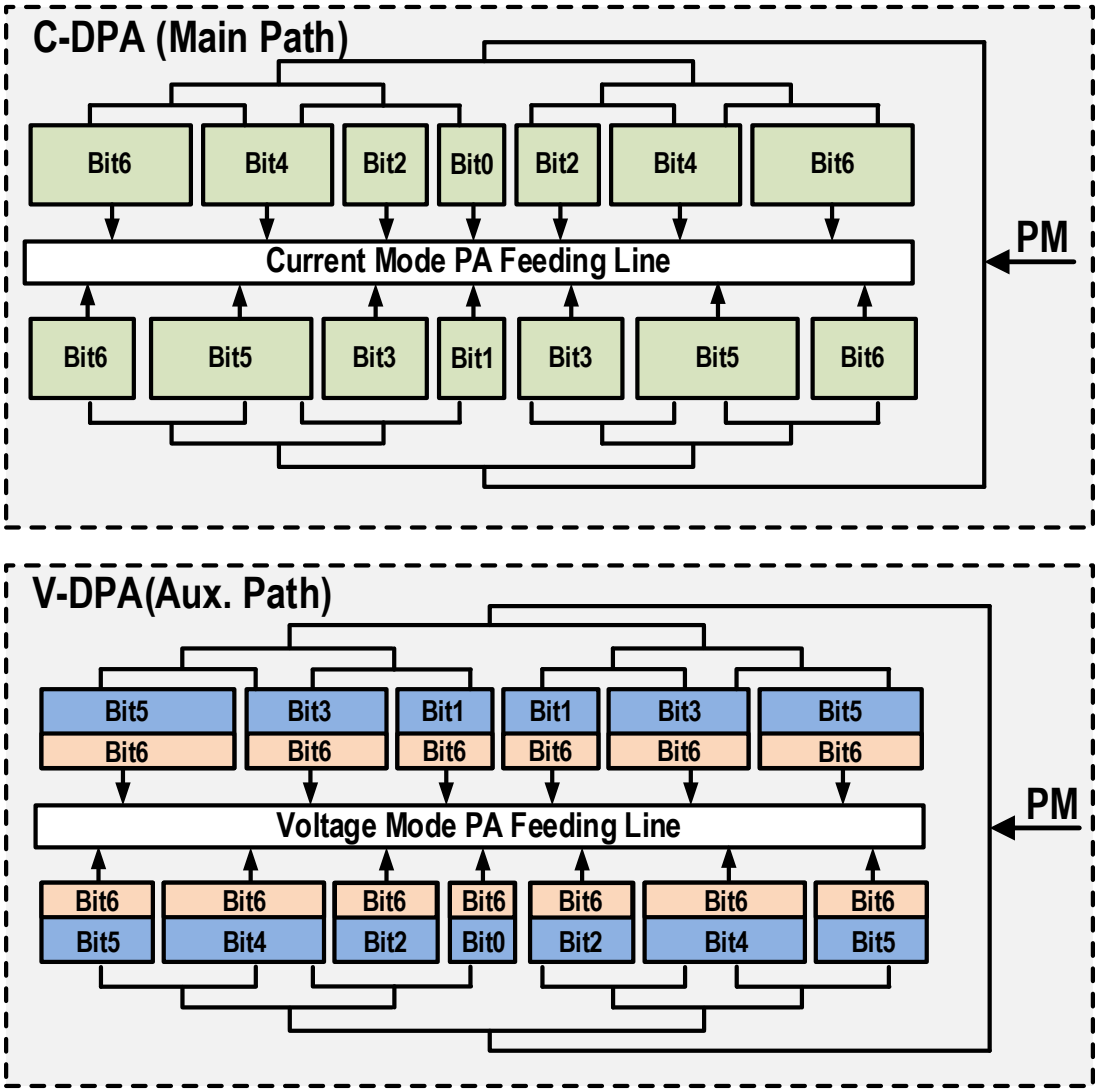


Figure 3-2 Routing line floorplan for the Main and Aux (auxiliary) PA paths.

proposes methodologies to improve the linearity of both, and measurement results are shown in Sections 3-4. Section 3-5 concludes this paper.

3.2 Proposed Architecture

Figure 3-1 shows the system architecture of the proposed hybrid (current/voltage) polar Doherty digital PA and routing line floorplan for the Main and Aux PA paths is shown in Fig 3-2. This proposed architecture consists of a current mode DPA, a voltage mode DPA,

PM driver, AM driver, adaptive biasing R2R DAC, and an AM buffer array and a single transformer output network. 8-bit AM codes control both the output power and adaptive biasing. The constant envelope PM carrier signal is buffered by a comparator and a digital driver that then feed the two sub-PAs. The AM signal is digitized to an 8-bit parallel AM control code and is then fed to the PA to control the numbers of PA cells enabled. The main path (C-DPA) and Aux path (V-DPA), which are distributed symmetrically along the output feedline, apply a fork shape configuration to minimize the phase offset and deliver PM signals evenly to the Main and Aux paths.

3.2.1 Single Transformer Broadband Load Modulation Network for Hybrid Voltage/Current DPA

This design utilizes a single footprint parallel-combining transformer to achieve the broadband Doherty power combining network [67]. The transformer occupies 430μm × 430μm die area. Figure 3-3 shows the proposed single footprint transformer load modulation output matching network. To achieve the desired impedance transformation ratio and enhance the quality factor, the three-coil parallel-combining transformer is implemented with nine turns, of which three turns are the two primary inductances (connected to the Main and Aux path PAs) and the other six turns are the secondary inductance (connected to the 50Ω antenna load). The passive efficiency of this single footprint transformer at the peak PA output power is shown in Fig. 3-4. Note that this proposed load modulation architecture doesn't need a large switch in the aux path to provide a short, because the voltage mode PA used in Aux path provides a low impedance when turned off, supporting a very compact formfactor. However, if a current mode PA is used in the Aux path, when the current mode is turned off, a switch is then required, because the current mode DPA shows high impedance when turned off, which will load the PA

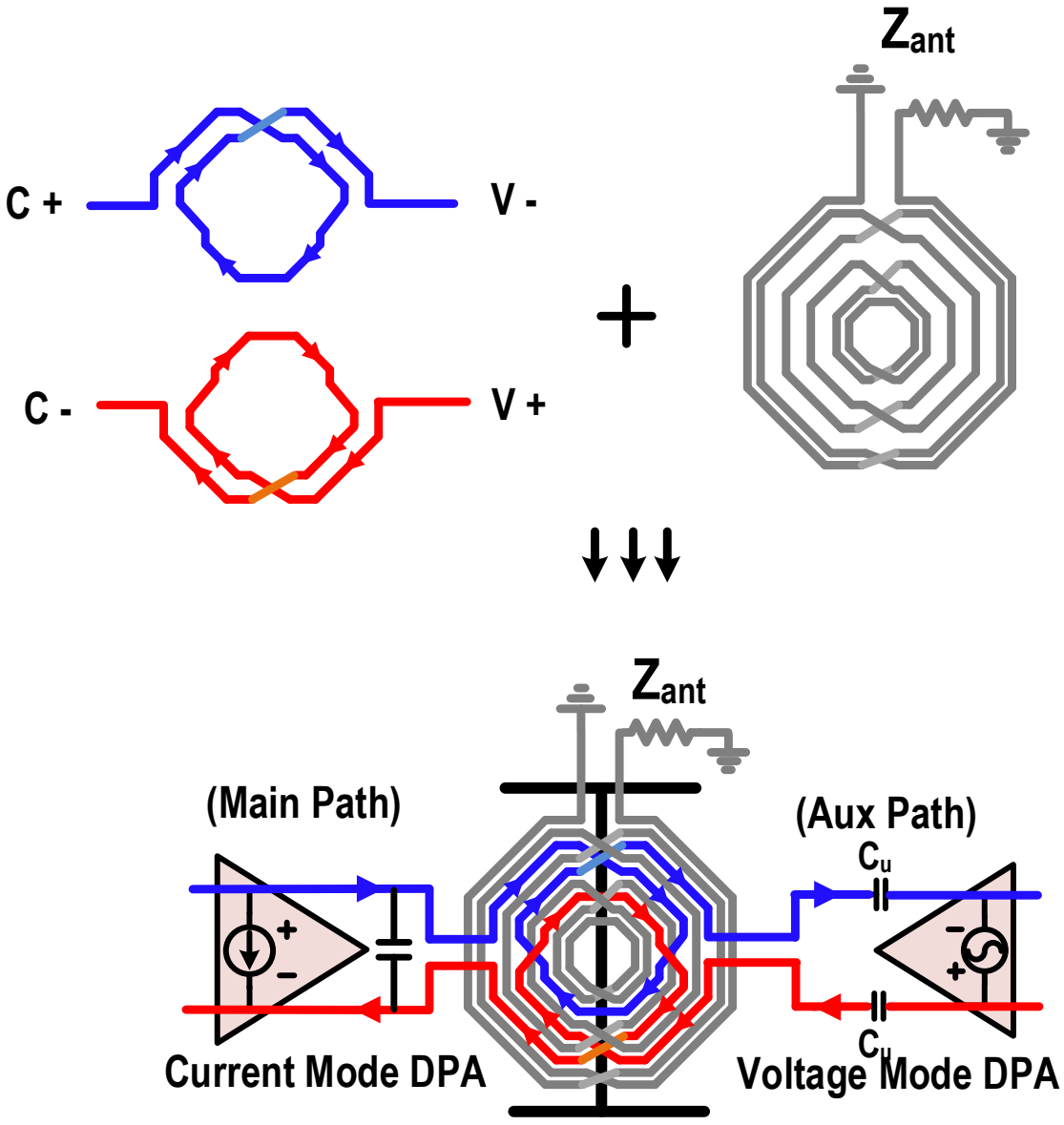


Figure 3-3 Proposed single footprint transformer as the DPA output matching network. Note the Main-path AP is current-mode, while the Aux-Path PA is voltage-mode.

output passive network and degrade its efficiency. To the author's knowledge, this is the first demonstration of power combing current mode and voltage mode DPAs in a single transformer footprint by using a single transformer-based parallel combining network.

Note this output passive network is not designed to realize any impedance inverter properties to ensure its broadband operation, since the turning-on sequence of the voltage/current-mode PAs perform effective Doherty active load modulation. This is detailed as follows. The output voltage swing in the differential current mode[74] and voltage mode PAs [11], with n out of N unit cells turned on are as follows:

$$V_{out\_Current\_mode} = \pi\left(\frac{n}{N}\right) \times V_{DD} \tag{3-1}$$

$$V_{out\_Voltage\_mode} = \frac{4}{\pi}\left(\frac{n}{N}\right) \times V_{DD} \tag{3-2}$$

The impedance at the main and Aux PA output for a Doherty PA can be derived as equation (3-3) and (3-4):

$$Z_{Main} = \frac{R_L}{1 + \frac{V_{Aux}}{V_{Main}}} \tag{3-3}$$

$$Z_{Aux} = \frac{R_L}{1 + \frac{V_{Main}}{V_{Aux}}} \tag{3-4}$$

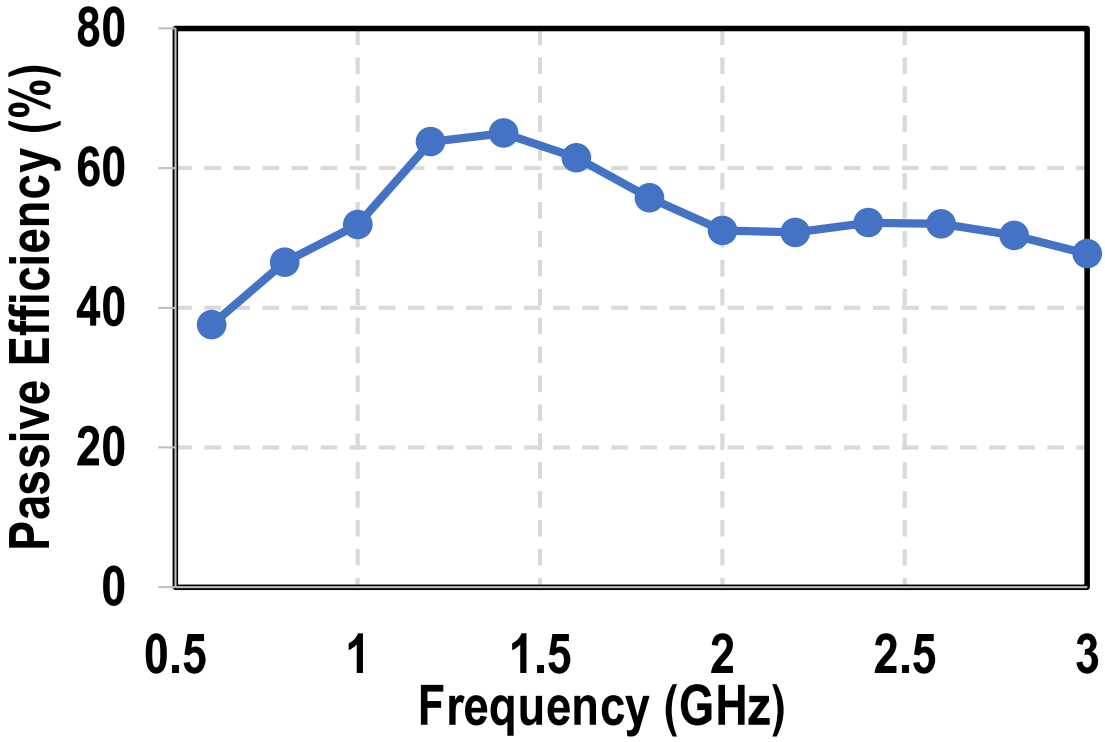


Figure 3-4 EM simulated passive efficiency of the PA output.

where V_{Main} and V_{Aux} are the Main and Aux amplifier voltages, respectively. Replacing equations (3-1) and (3-2) into (3-3) and (3-4) the impedance presented to each PA can be derived as

$$Z_{Main} = R_L \frac{1}{\left(1 + \frac{4}{\pi^2} \times \frac{2n+m}{2^M - 1}\right)} \tag{3-5}$$

$$Z_{Aux} = R_L \frac{1}{(1 + \frac{\pi^2}{4} \times \frac{2^M - 1}{2n+m})} \tag{3-6}$$

where M is total number of bits for VDPA, and m and n are the number of "ON" power cells of VDD mode and 2VDD mode in VDPA, respectively. Thus, depending on the AM

turn-on sequence, each PA experiences proper active load modulation, achieving deep PBO efficiency enhancement.

3.2.2 Overall Operation of Proposed DPA Architecture

The proposed hybrid single footprint transformer digital PA combines one main path C-DPA and one Aux path V-DPA, Class-G DPA, to achieve built-in AM-PM compensation and PBO efficiency enhancement. In the low power region, as the output power increases, current DPA cells sequentially turn on until 5.2 dB PBO shown as Fig 3-5 (a). At this time, if the output voltage of Main and Aux path are equal, it would be 6 dB

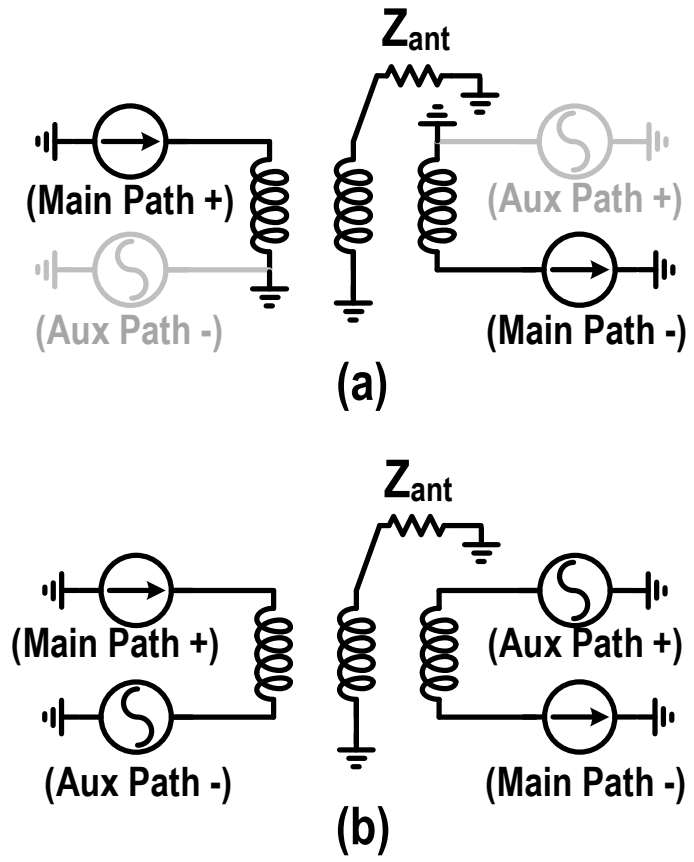
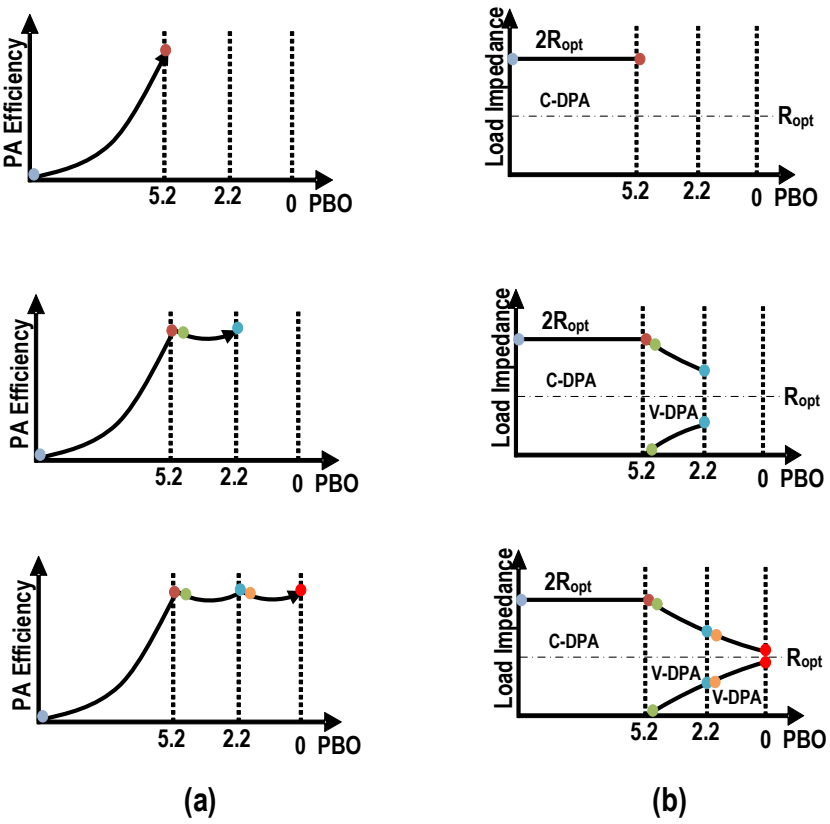


Figure 3-5 Block diagram of (a) Main operation (5.2 dB PBO) (b) Main and Aux operation (2.2dB PBO or 0 dB PBO).



	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6
AM1	ON						

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6
AM127	ON	ON	ON	ON	ON	ON	ON

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6
AM128	ON	ON	ON	ON	ON	ON	ON
	VDD						

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6
AM192	ON	ON	ON	ON	ON	ON	ON
	VDD	VDD	VDD	VDD	VDD	VDD	VDD

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6
AM193	ON	ON	ON	ON	ON	ON	ON
	2VDD	VDD	VDD	VDD	VDD	VDD	VDD

	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6
AM255	ON	ON	ON	ON	ON	ON	ON
	2VDD	2VDD	2VDD	2VDD	2VDD	2VDD	2VDD

Class-D^{-1}	
	ON
	OFF

Class-G	
	VDD
	2VDD
	OFF

(c)

Figure 3-6 Simulated results of (a) PA efficiency, (b) Load impedance and (c) Example of operation sequence.

PBO after all the cells of Main path are turned on like conventional Doherty structure, however the proposed architecture has different output voltages and impedances between main path and Aux path as shown in equation (3-1) ~ (3-4), thus when all the cells of Main path are turned on, theoretically, it achieves an efficiency peak at 5.2 dB PBO due to Doherty load modulation. After all the cells of the main path are turned on, the unit cells of the Aux path are gradually turned on in VDD mode. When the cells of Aux path are fully turned on to VDD mode, the overall PA achieves an additional efficiency peak by class-G operation at 2.2dB PBO, and then the Aux PA cells are gradually turned on to 2VDD mode as well (Fig 3-5 (b)). Figure 3-6 illustrates the efficiency, load impedance, and overall turn-on sequence of each PA operation.

3.3 Theory of AM-PM Distortion of Digital PA

There are two main sources of linearity distortion for PAs, AM-AM and AM-PM [82]. Since AM-AM distortion can be compensated through proper selection of the AM control code [34], we will focus on AM-PM distortion. The principles for the occurrence of AM-PM distortion the methods to improve/compensate for it regarding the current mode DPA and the voltage mode DPA, respectively are described below.

3.3.1 Current Mode Digital PA AM-PM Compensation

We will first review the behavior of conventional current mode, class-D^{-1} PA, and its main causes of AM-PM distortion. Figure 3-7 shows the schematic for class-D^{-1} PA composed of N-bit segment binary-weighted cells. The nonlinearity of the current mode DPA is mainly caused by the output capacitance C_d variations against output power

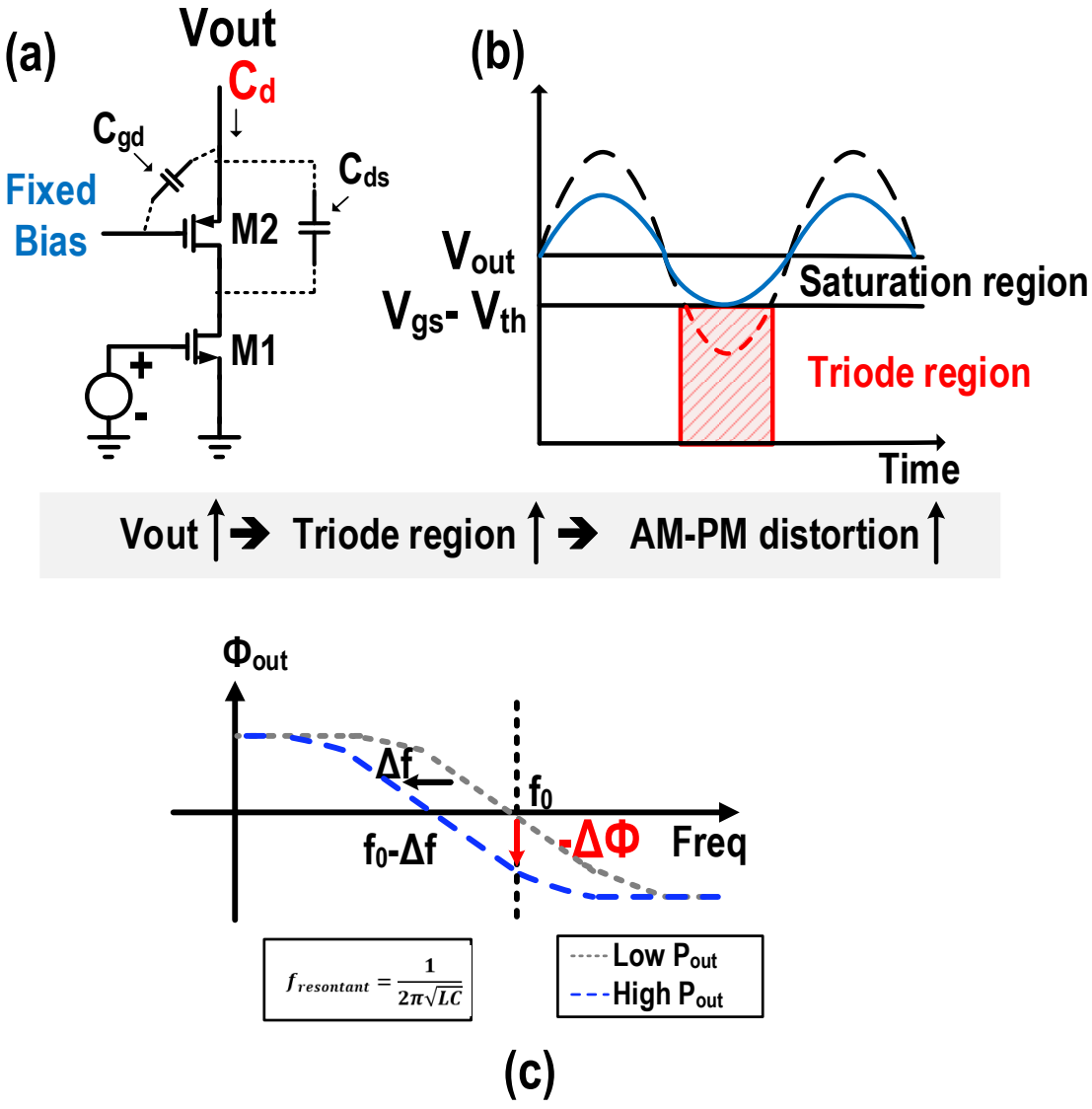


Figure 3-7 (a) Conventional current mode DPA schematic (b) Output voltage swing according to each region (c) Phase nonlinearity behavior of conventional current mode DPA.

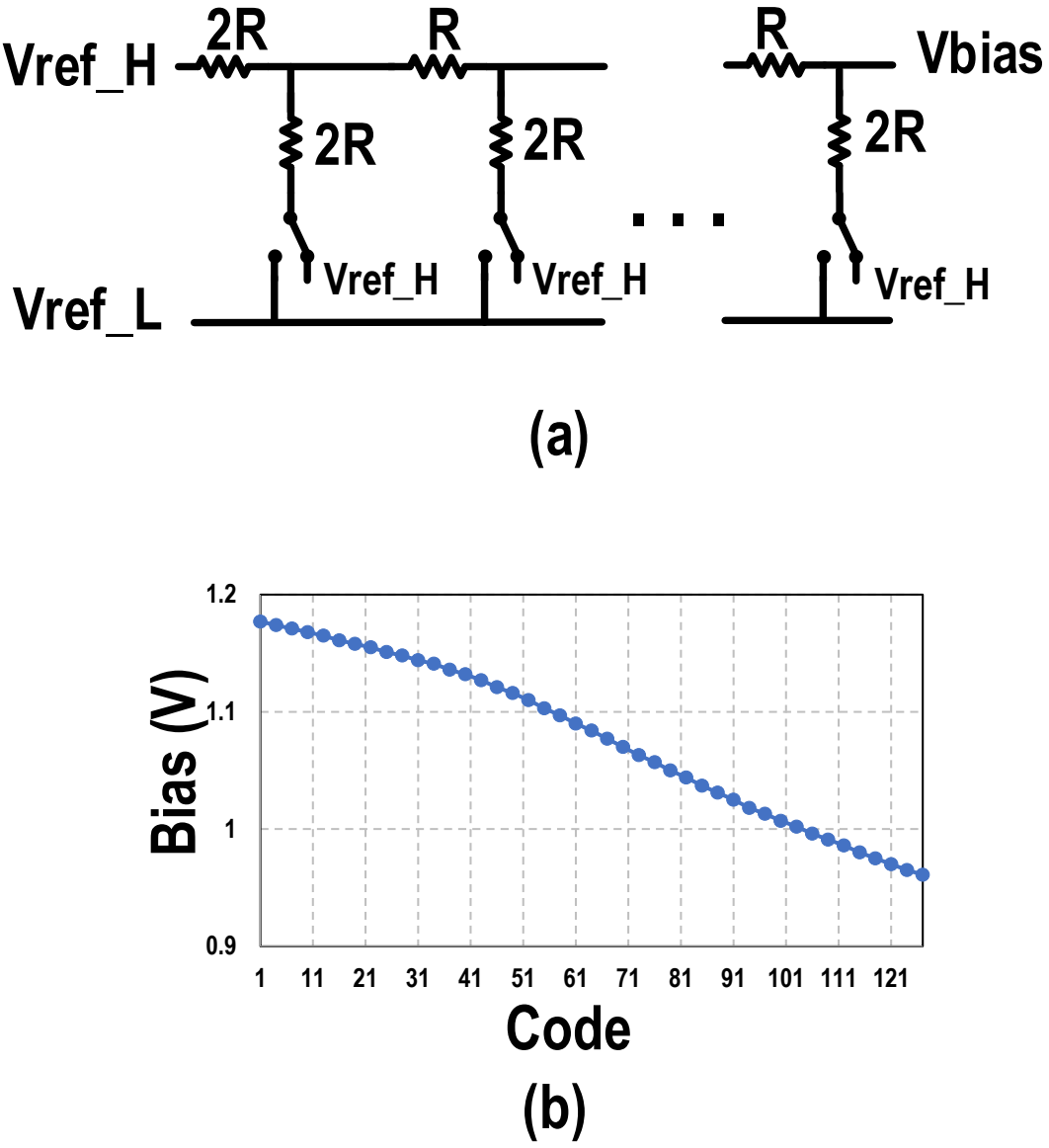


Figure 3-8 (a) Schematic of R2R DAC (b) Simulated results of adaptive biasing.

level [34]. C_d can be derived as C_{gd} + (1-1/|A|) × C_{ds}, where C_{ds} is the total effective capacitance between the drain and the source of M_2 and A is the voltage gain of the cascode transistor (M_2) [83]. First the C_{gd} of the cascode transistor (M_2 in Fig.3-7) is varied according to the device operation region as the below equations (3-7) -(3-9) [84].

$$C_{gd\_triode} = \frac{WLC_{ox}}{2} + WC_{OV} \tag{3-7}$$

$$C_{gd\_saturation} = WC_{OV} \tag{3-8}$$

$$C_{gd\_off} = WLC_{OV} \tag{3-9}$$

where W is the cascode transistor gate width; L is the gate effective length; C_{ov} is the drain-gate overlap capacitance; and C_{ox} is the gate-oxide capacitance. As more digital cells are turned on, the output voltage swing of V_{out} node increases. At this time, since the gate bias is fixed, as V_{out} increases, M_2 operates in the triode region for a longer period, which increases C_d. In addition, when the power cell is turned off, $C_d = C_{gd\_off}$, since C_{ds} is terminated with high impedance, providing low capacitance. In summary, as more cells are turned on in the conventional current mode DPA, more cells operate in triode for longer periods, hence the total PA output capacitance increases as a function of output power. This modulated capacitance shifts the resonance frequency, which causes AM-PM distortion as shown in Fig.3-7 (c). As the output power increases, the AM-PM goes increasingly negative, and we call it as lagging AM-PM. To reduce the time-period during triode region, we use adaptive biasing on the cascode device. As more cells are turned on, the bias voltage is decreased as shown in Fig.3-8 (b). This operation shortens the interval in the triode region, which reduces the capacitance variation over output power. As shown in Fig. 3-9, employing adaptive biasing reduced the total AM-PM distortion from 11.3° to 6.7° at 2.4GHz.

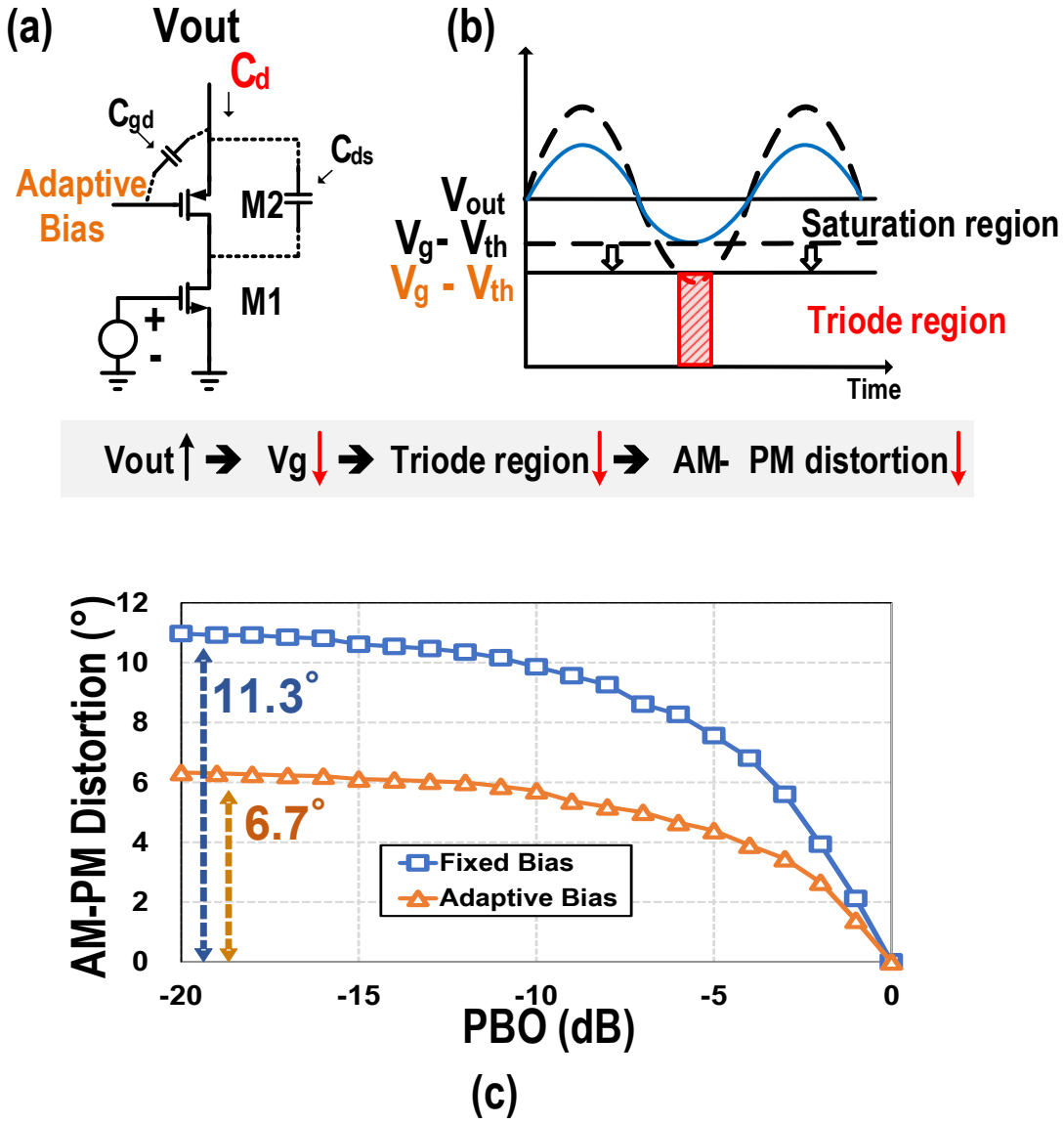


Figure 3-9 (a) Schematic of R2R DAC (b) Output voltage swing according to each region (c) Simulated results of adaptive biasing.

3.3.2 Voltage Mode Digital PA AM-PM Compensation

In this section, we analyze and show the AM-PM distortion behavior of voltage mode digital PA, conventional SCPA, and class-G. As shown in Fig.3-10, the conventional single-ended SCPA consists of an M-bit binary weighted unit cell and a bandpass matching network. The output power level is determined according to the number of cells turned on by the AM code selected (m), whose bottom plates are switched between V_{DD} and GND at the carrier frequency. The capacitance of the unswitched cells $(2^M-(m+1)) \times C_u$ is shorted to ground, while the capacitance looking into the switched-on cells is $m \times C_u$. Hence, the equivalent capacitance (C_{out}) looking into the PA continue to be $(2^M - 1) \times C_u$ regardless of number of cells turned ON. Hence, the inductance (L_{ind}) continues to resonate at the same

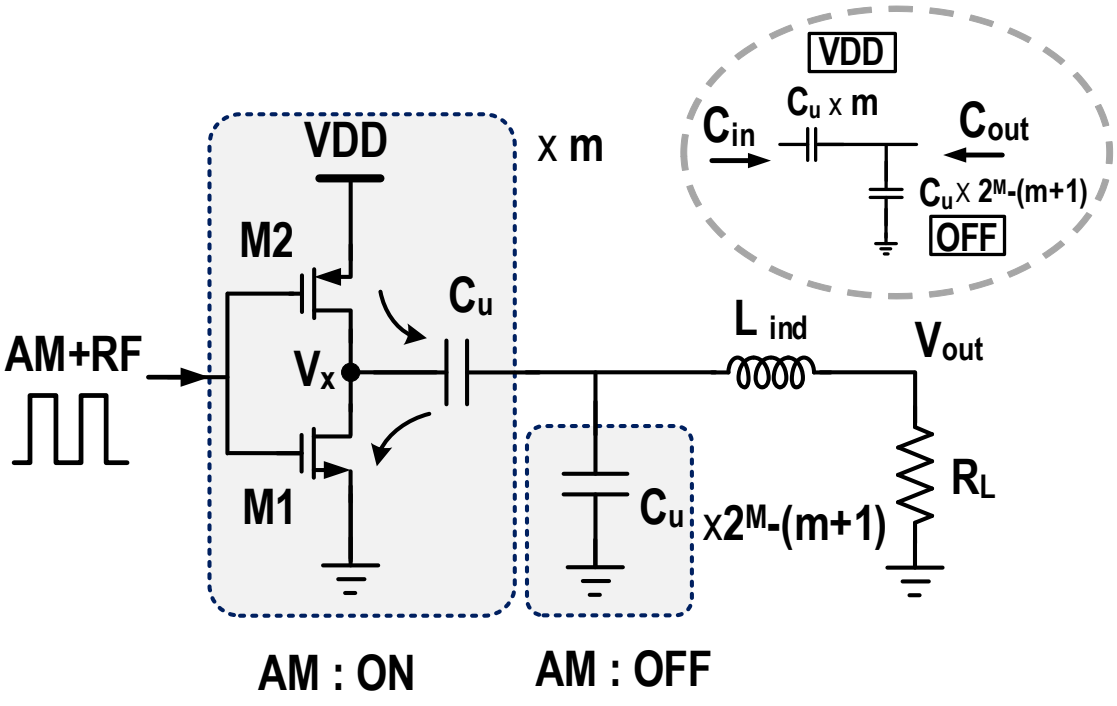


Figure 3-10 Schematic of conventional SCPA

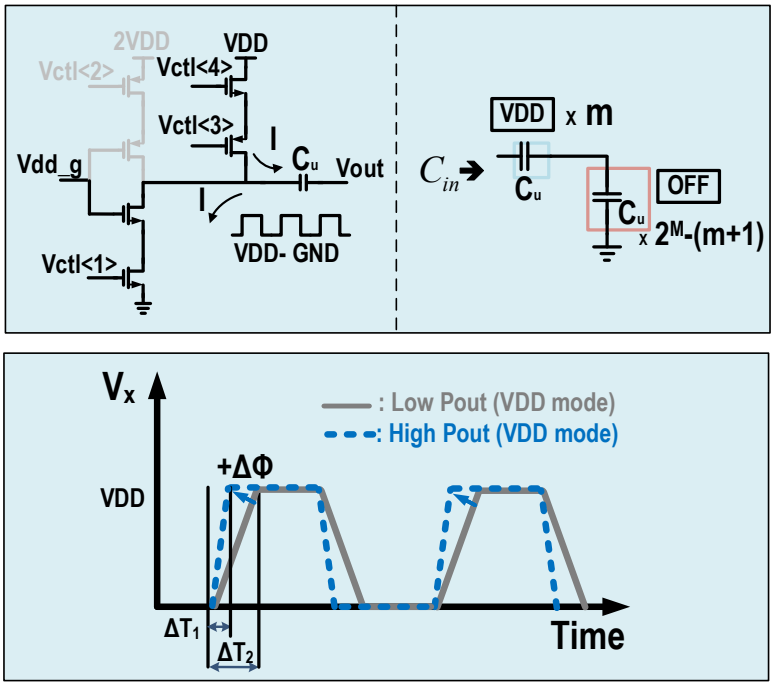


Figure 3-11 Class-G AM-PM distortion VDD operation

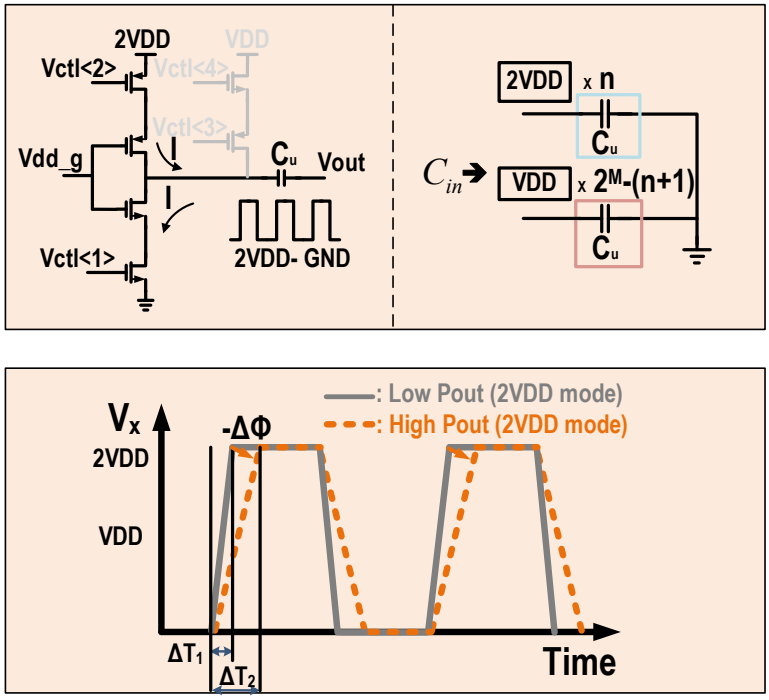


Figure 3-12 Class-G AM-PM distortion 2VDD operation

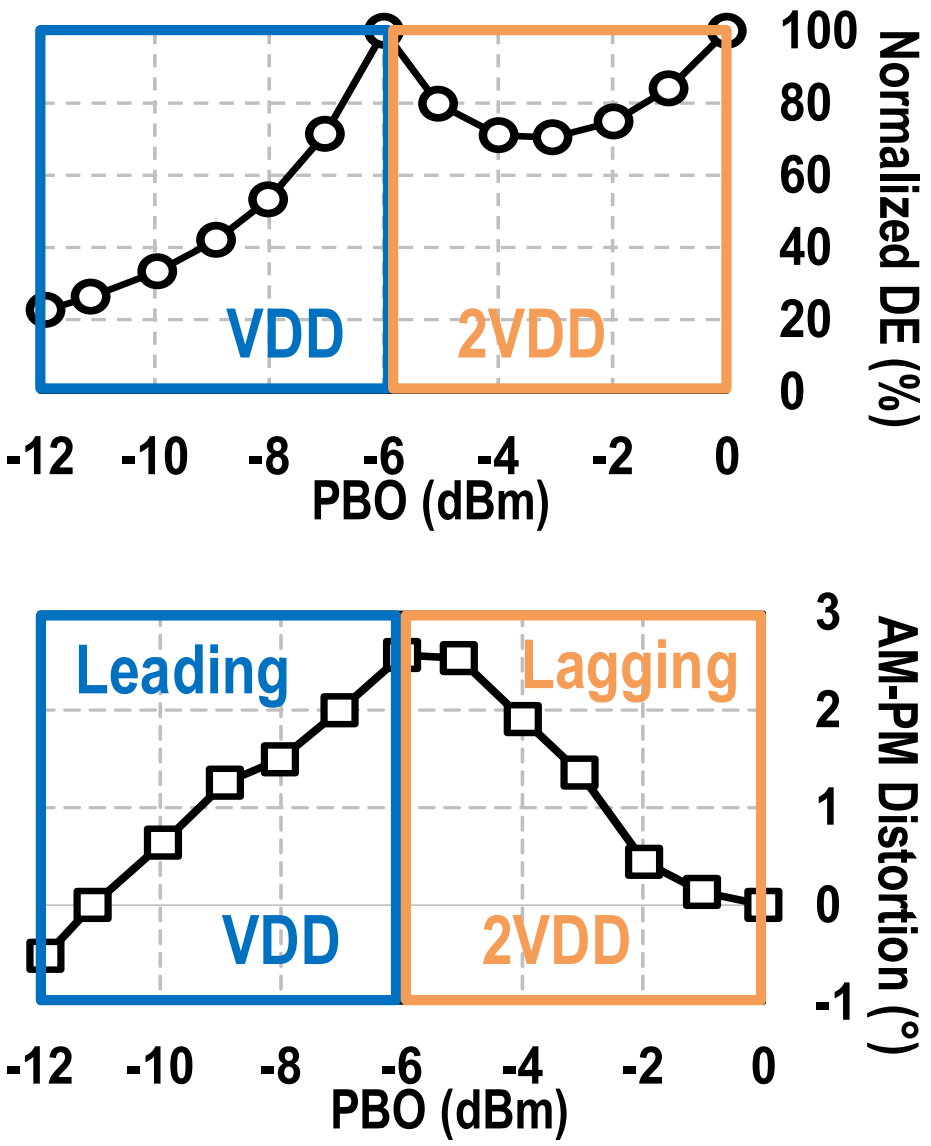


Figure 3-13 Simulated results of class-G about (a) Drain efficiency (b) AM-PM distortion.

frequency, and we can assume there is same phase between V_x and V_{out}. On the other hand, the equivalent capacitance C_{in} observed by the PA cells changes as a function of number of cells turned on as follows:

$$C_{in} = \frac{m(2^M - (1+m))}{2^M - 1} \times C_u \tag{3-10}$$

where M is the total number of bits of the SCPA, and m is the number of "ON" SCPA power cells. The charging/discharging time (Δt) of C_{in} can be expressed as the following:

$$\Delta t = C_{in} \times \frac{V_x}{mI} \tag{3-11}$$

where I is the current driving strength of the SCPA unit power cell. C_{in} is substituted in (3-11) and as a result, the transition charging/discharging time (Δt) at V_x can be further derived as [81]

$$\Delta t = C_u \times \left(1 - \frac{m}{2^M - 1}\right) \frac{V_{DD}}{I} \tag{3-12}$$

As shown in this equation, the larger the number of unit cells (m) turned on, the shorter the transient time, corresponding to a positive frequency shift, and a corresponding leading behavior, which is inverse from the current mode DPA AM-PM distortion. We can expand this concept to the class-G DPA. A voltage mode amplifier can be represented as a capacitive divider, and Fig. 3-11 and Fig. 3-12 show the VDD mode and 2VDD mode of class-G operation respectively. In class-G VDD mode, AM-PM distortion demonstrates a leading behaviour, the same as the conventional SCPA. However, when operating in the 2VDD mode, it can be expressed as a capacitive divider with two input sources as shown in Fig.3-12 and it can be expressed by the following charging/discharging equation:

$$C_{in} = C_{VDD} + C_{2VDD} \tag{3-13}$$

$$\Delta t = C_u \times \left(\frac{2^M + n + 1}{2^M - 1}\right)\frac{V_{DD}}{I} \tag{3-14}$$

where n is number of tuned on unit cells as 2VDD. As summarized in Fig.3-11, for VDD mode, as the number of VDD cell (m) turned on increases, the charging/discharging time becomes shorter, which illustrates the leading AM-PM distortion behaviour. However, in the case of 2VDD mode shown in Fig.3-12, as the number of unit cells (n) transitioning from VDD to 2VDD is increased, the output power increases, the charging/discharging time becomes longer, and lagging AM-PM distortion behaviour occurs. Looking at the simulation results of class-G operation, as shown in Fig.3-13, the efficiency improves at 6dB PBO thanks to class-G operation[27], and at the same time, the AM-PM distortion direction transitions from leading to lagging, and hence compensates itself. The magnitude of leading AM-PM distortion of the V-DPA can be manipulated by the driving strength of the SCPA power cells and the size of C_u, which is a direct trade-off with the efficiency and output power[81].

3.3.3 AM-PM Operation of Proposed Architecture

The AM-PM non-linearity as a function of the output power level is self-compensated by the proposed architecture. First, the AM-PM distortion of current mode DPA has a lagging (negative) behavior according to output capacitance. However, it is mitigated by adaptive biasing. Second, as the DPA in the voltage mode DPA is turned on in VDD mode, the direction of AM-PM distortion is changed to the leading (positive) behavior, opposite to the previous current mode, which is a characteristic of the hybrid

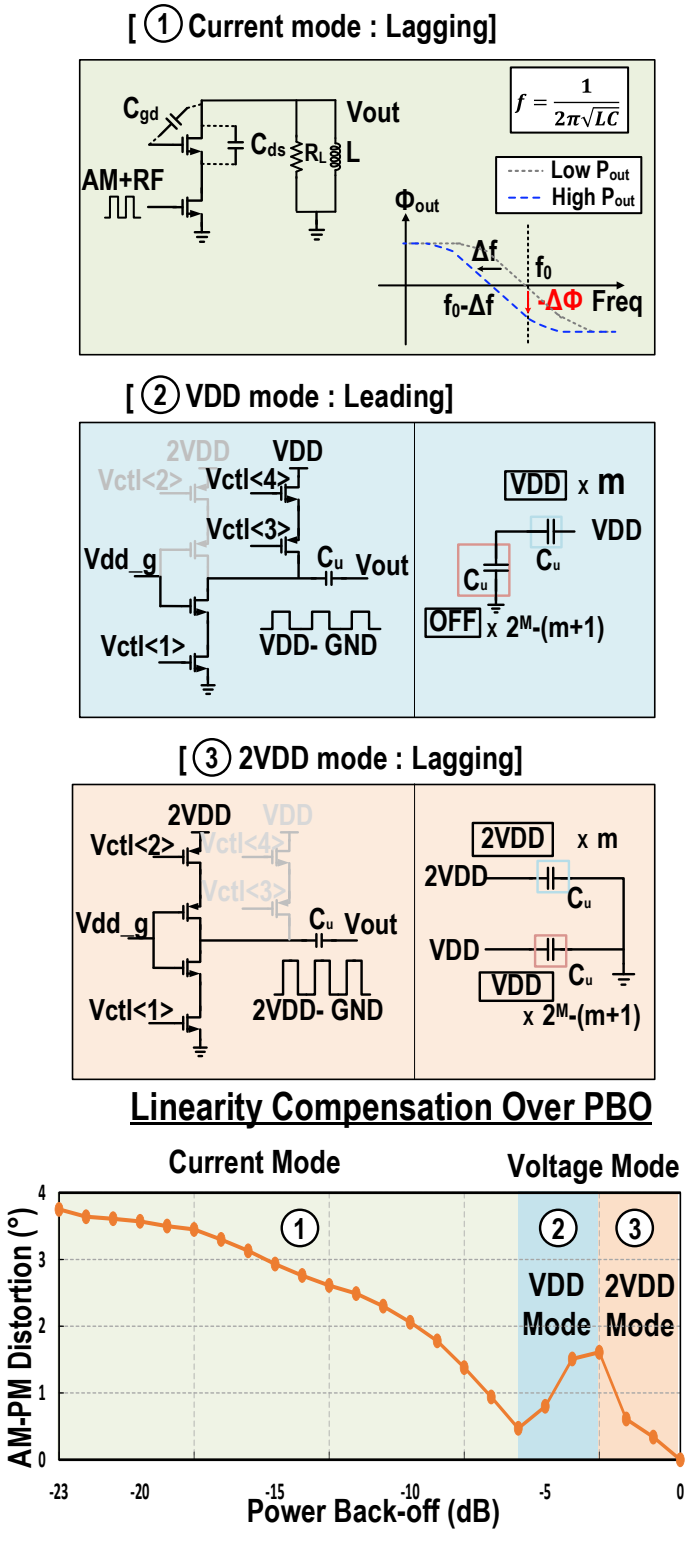


Figure 3-14 Simulated results of AM-PM distortion according to their operation region.

(current/voltage) operation. Third, the AM-PM distortion behavior changes its direction back to lagging as the cells in the Aux path change to 2VDD mode. Figure 3-14 illustrates the simulation results of the AM-PM distortion that changes as each mode is operated in proposed architecture.

3.4 Measurement Results

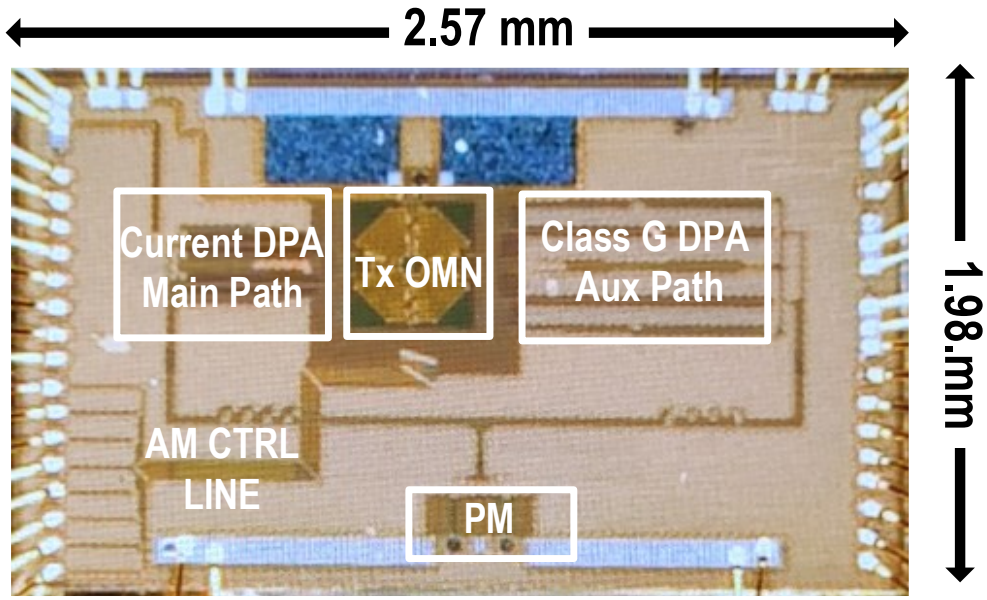


Figure 3-15 Chip microphotograph

A proof-of-concept hybrid polar Doherty DPA is implemented in the Globalfoundries 45nm CMOS SOI process with a chip size of 2.57mm × 1.98mm including all decoupling capacitors and electro-static discharge (ESD) I/O pads (Fig. 3-15). This is a fully integrated DPA design with C-DPA and V-DPA power cells, adaptive bias, output passive network, AM and PM drivers. The chip is mounted on an FR4 PCB board and wire-bonded to facilitate the probing-based testing. The DC supplies are 1.1V and 2.2V for class-G operation. We first characterize the DPA using continuous wave (CW) signals with a 50Ω standard load. A single-

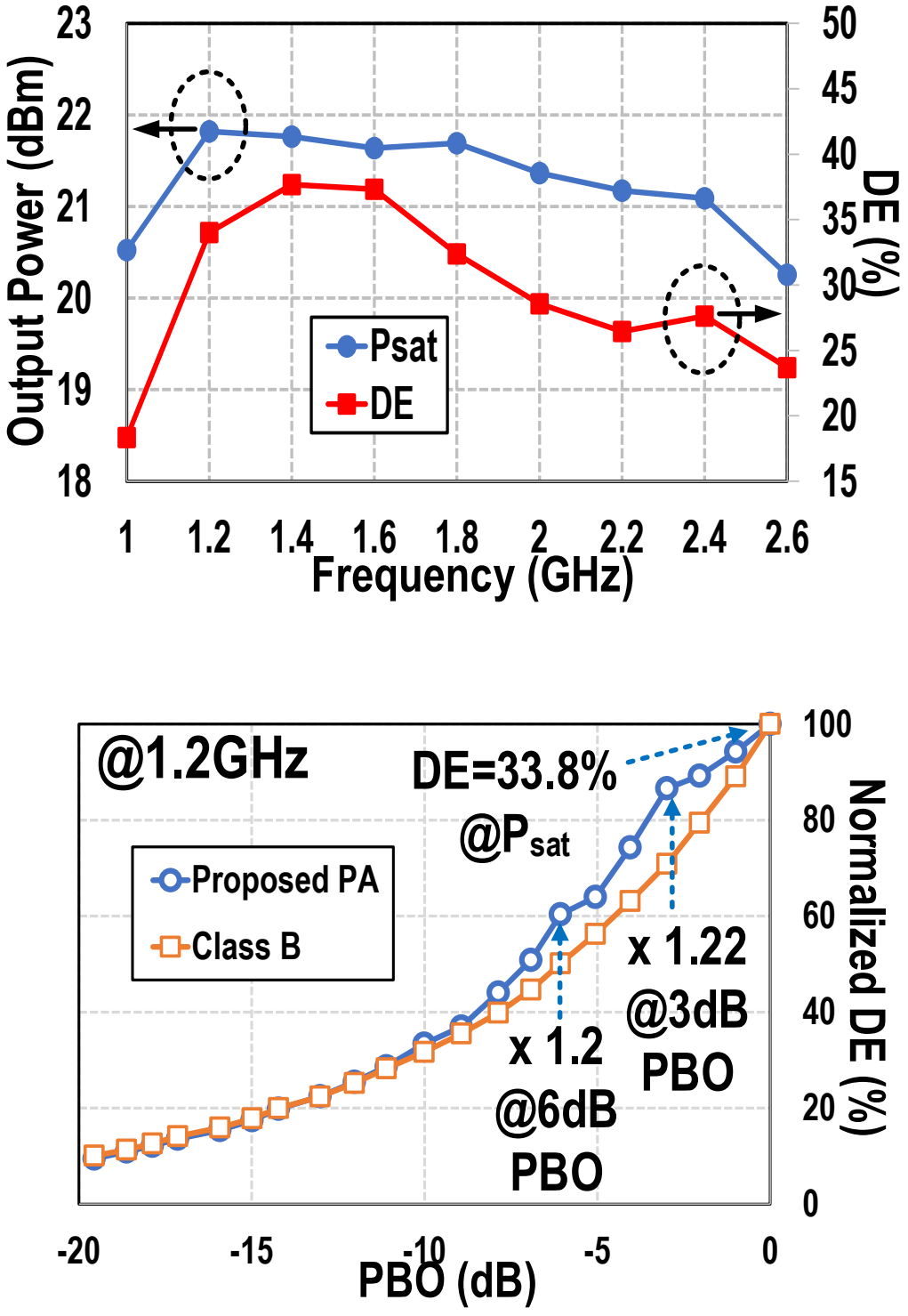


Figure 3-16 CW measurement results (a) Power and DE according to frequency and (b) DE according to PBO

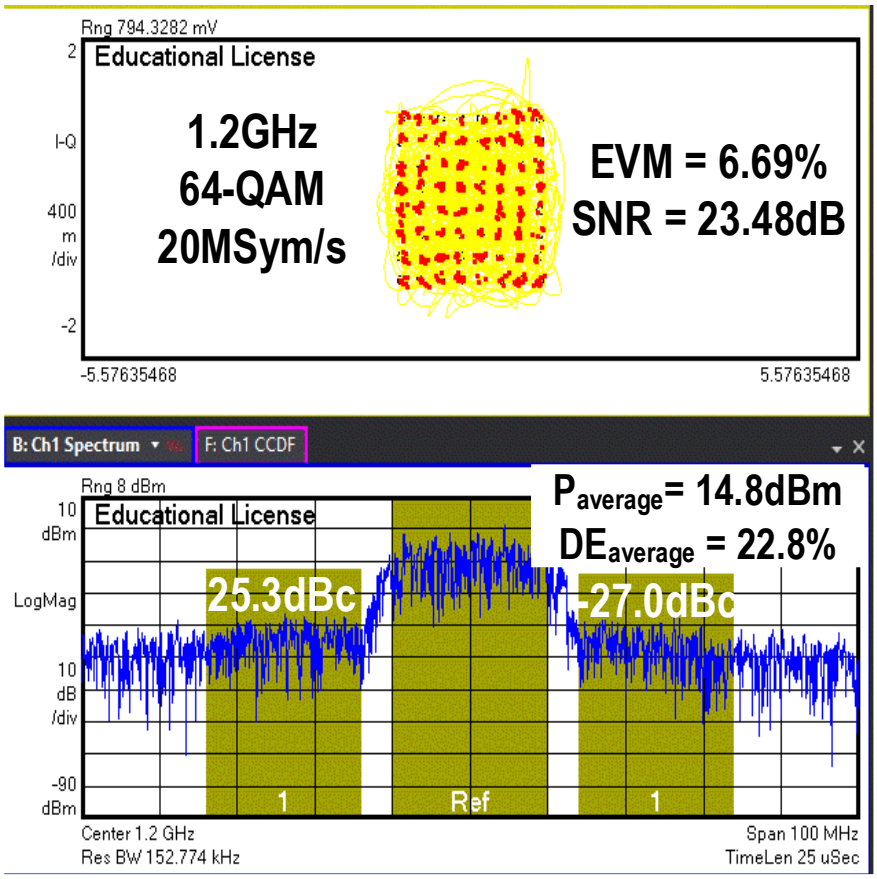


Figure 3-17 Modulation measurement with 20Msym/s 64-QAM at 1.2GHz

ended phase modulation (PM) signal is first converted by an off-chip balun (Krytar4010180) to generate the differential signals and fed to an input PM driver. The AM sequence is controlled using an USB-1024LS with custom LabVIEW code. The amplified single-ended output signal is measured by an RF power meter (Keysight N1913A). Figure 3-16 summarizes the CW measurement results. The measured Peak Pout is 21.8dBm at 1.2GHz and 1dB bandwidth is from 1.2-2.4GHz, which fractional bandwidth of 66%. The peak DE is 37.8% at 1.4GHz and DE is 33.8%/29.3%/20/4% for the peak/3dB/6dB/ PBO at 1.2GHz, which demonstrates 1.2×/1.22× PBO efficiency enhancement, compared to the ideal class-B. The PA is then characterized with modulation. Desired complex modulation signals are synthesized in Advanced Design System (ADS) and decomposed into their corresponding AM and PM

signals for polar operation. The memoryless 1-D AM-AM lookup table (LUT) for each PA is made based on the characterized CW test and a pattern generator (Keysight 16822A) generated the 8-bit AM control LUT. The PM signals are generated by the arbitrary waveform generator (AWG) (Tektronix AWG7002A). Since the timing alignment between AM path and PM path is very critical for the modulation performance[31], we used a pulse function generator (Agilent 81160A) to generate the trigger pulses for AWG and pattern generator to synchronize the AM and PM signal with a fine control delay. The output signals from the PA are demodulated by a real-time oscilloscope (Keysight MSO840A). Figure 3-17 shows the demodulated 20MSym/s single-carrier 64 QAM signal at 1.2GHz without any phase pre-distortion. It achieves 14.8dBm average P_{out} and 22.8% average DE, 23.48dB EVM and -25.36dBc ACLR. Table 3-1 shows the comparison of the proposed hybrid single transformer with state-of-the-art RF CMOS digital PAs. This proposed the single transformer footprint hybrid current-voltage digital Doherty PA achieves broadband operation compared to the state-of-the-art.

3.5 Conclusion

This chapter present a compact broadband hybrid current/voltage mode digital Doherty PA with a single transformer as its output network and built-in large-single AM-PM distortion compensation, which is capable of supporting large PAPR and high-speed modulation signals without any DPD linearization. An adaptive biasing scheme is proposed to minimize the current mode DPA's inherent AM-PM nonlinearity. Class-G operation within the voltage mode PA is introduced to achieve efficiency enhancement and AM-PM

nonlinearity reduction. A current/voltage mode DPA architecture is proposed to support AM-PM cancelation, removal of unnecessary switches, and support load modulation within a single transformer network.

Table 3-1 Comparison of the state-of-the-art Digital Power Amplifier at GHz RF Frequency

	This work	RFIC 2017	JSSC 2017	ISSCC 2018	JSSC 2020	VLSI 2021
Architecture	**Hybrid Current/Voltage Mode Digitial Doherty PA**	Current-Mode Digital Doherty PA	Polar Class-G VMD	Voltage-Mode Digital Doherty PA	Three-way Hybrid Current/Voltage mode Digital Doherty PA	Single-Core Inverse Class-D PA
Process [nm]	**45**	40	45	55	45	65
Number of Matching Networks	**1**	2	2	1	3	1
Passive Network Area [mm^2]	**0.185**	0.504*	-	0.166*	0.461	0.146*
Supply [V]	**1.1 / 2.2**	0.7	1.2/2.4	1.2/2.4	1.2	1.4
Frequency [GHz]	**1.2**	2.5	3.5	1.7	2.3	2
1dB RF BW [GHz]	**1.2 - 2.4 (66%)**	2.3 - 2.8 (21%)	2.9 - 4.3 (38%)	1.7 - 2 * (16%)	2.1 - 2.5 (17%)	-
Peak Power [dBm]	**21.8**	21.4	25.3	27	22.4	23.3
PEAK DE/PAE [%]	**37.6**	49.5	30.4 (PAE)	25.4 (PAE)	38.5	34.9
Number of η peaks	**2**	1	2	1	2	1
Modulation	**64 QAM 20MHz**	64 QAM 20MHz	1024 QAM 10MHz 32 Carrier	QPSK NB-IoT 180KHz	64 QAM 40MHz	64 QAM 10MHz
Avg. Power [dBm]	**14.8**	13.9	14.8	23*	15.3	16.7
Avg. efficiency [%]	**22.8**	24	18 (PAE)	17.9* (PAE)	24.7	25.2
EVM [dB]	**-23.5**	-30	-40.3	-21.6	-32	-28.5
DPD	**No**	Yes	Yes	No	No	Yes

*Estimate from figure

CHAPTER 4. A COMPACT CMOS BIDIRECTIONAL DIGITAL TRANSCEIVER FRONT-END WITH CAPACITOR BANK AND TRANSFORMER MATCHING NETWORK REUSE

4.1 Introduction

Spectrally efficient complex modulation schemes are widely employed to support the exponential growth in data traffic. However, this places stringent requirements on the RF electronic frontends, including strict linearity due to high PAPR. Large PAPR also results in reduced energy efficiency for power amplifiers as the PAs often need to operate at power back-off (PBO) modes. This poses major challenges in traditional analog RF transceiver designs. In parallel, with the technology advance and maturity of electronic frontend at RF frequencies, it is now increasingly important to explore RF transceiver (TRX) frontend solutions with ultra-compactness to support low-cost small form-factor high-volume applications, such as IoT and portable mobile devices. Most existing analog TRX systems consist of chains of separate TX/RX functional blocks (Fig.4-1) with corresponding inter-stage matching/filtering networks to ensure performance, making further area-reduction difficult. In contrast, digital TRXs realize multiple block functionalities within a single block to drastically reduce the overall TRX complexity and overhead. For example, the digital TX contains digital-to-analog converter (DAC), mixer, filters, and the PA all together[11], and thus they offer excellent RF performance within a compact area. In addition, the digital TRX has performance compatible with aggressive CMOS process scaling and supports extensive reconfigurability and wideband operation for multi-band multi-standard radios. Therefore, there is recently a surge of interest to

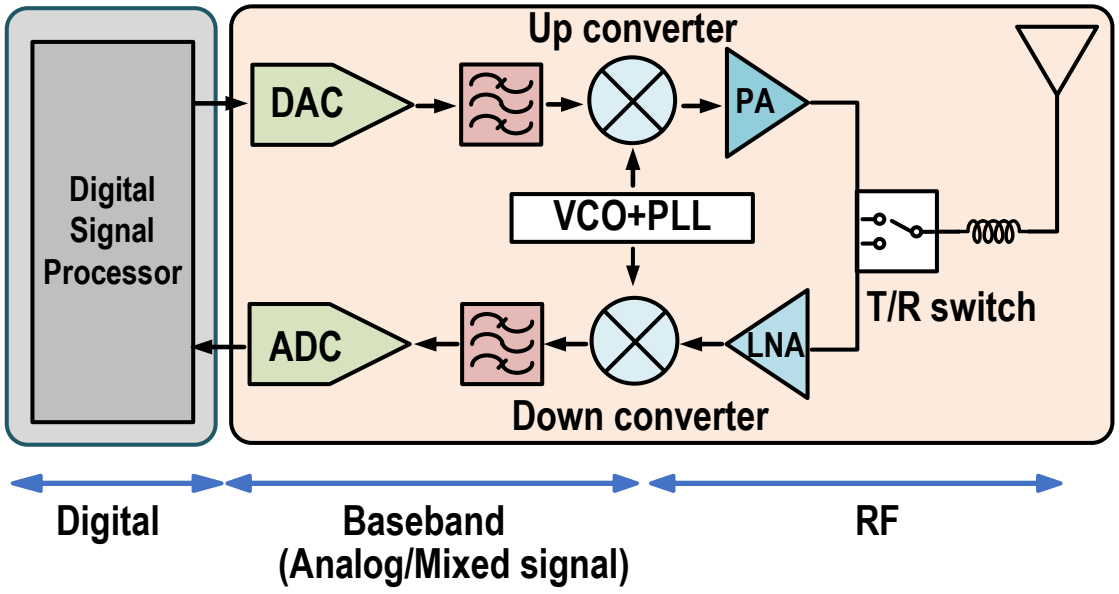


Figure 4-1 Block diagram of analog transceiver

explore high-performance digital TRX frontends. Digital PAs (DPAs), a key building block within the digital TX, have been studied extensively[20, 74, 85] and can be broadly divided into two general categories. One is the voltage-mode DPAs such as the switched capacitor PAs (SCPAs), which achieve good linearity and efficiency, but also suffer from limited output power, since their output voltage swing is lower than the supply voltage[19, 26, 69, 76]. An alternative is the current-mode DPA such as the inverse class-D, which realizes higher output power as its output voltage swing can exceed its supply voltage, but may exhibit large nonlinearities due to distortion[13, 33, 73, 75], except for some recent designs for AM-PM compensation [34]. Due to the increased PAPR in complex modulation schemes, PAs with PBO efficiency enhancement have become essential to ensure overall high system efficiency[5]. A fully integrated digital Doherty PA was first demonstrated in[86]. Examples include class-G PAs[27, 51, 87] with digital supply modulations, and Doherty PAs[12, 56, 67, 88, 89] and Outphasing PAs[58, 59, 63, 90] with active load

modulations. Other solutions include the Sub-Harmonic Switching (SHS) PA[28, 78, 91] and the Switched/Floated Capacitor Power Amplifier (SFCPA)[29, 92] with tri-state floating capacitors. Recent designs also demonstrate hybrid use of voltage- and current-mode PAs in digital Doherty PAs for balanced linearity and efficiency performance[81].

In parallel, Mixer first RX architectures have attracted extensive research focuses as well for wideband, compact, and high dynamic range radios[40, 93, 94]. In particular, the N-path mixer-first receivers are a popular choice due to their inherent capabilities of high linearity, sharp and tunable front-end filtering, and wideband carrier frequencies[43, 45, 95-100]. The N-path mixer-first RXs also potentially consume low power due to the removal of the LNA and are area efficient due to their inherent reconfigurable bandpass filtering, removing the need for bulky and narrowband SAW filters. Recent designs also show that mixer-first RXs can be extended to wideband high mm-Wave frequencies[50, 101, 102].

While RF digital TRX frontends naturally offer excellent RF performance, reconfigurability, and wideband operations, they commonly rely on architectures based on binary and/or unary arrays of sliced active and passive devices, resulting in a substantial area overhead compared to their analog RF counterparts. For digital TXs, the current-mode digital TXs require a large array of class-D^{-1} RF current sources, while the voltage-mode switched capacitor digital TXs require a large capacitor bank with scaled switches. In both cases, sliced PA arrays require large binary/unary array configurations to ensure high Effective number of bits (ENOB), e.g., 8-bits to 14-bits[103] and high TX dynamic range. Although mixed-signal PAs with hybrid analog/digital configurations substantially reduce the ENOB requirements and achieve super-resolution, they require separate analog paths

and are not fully digital in nature[52]. On the other hand, N-path mixer-first RXs require large differential capacitor banks as well, which scale with the quadrature operations and number of N-paths. In summary, although digital RF TRXs merge multiple functional blocks, their practical implementations often exhibit large chip areas fundamentally due to their nature of sliced digitized operations.

In this chapter, we propose a compact CMOS broadband bidirectional digital TRX frontend with capacitor bank and transformer matching network reuse. The bidirectional digital TRX functions as a class-G digital Doherty switched-capacitor TX in its TX-mode and an N-Path quadrature differential RX in its RX-mode[65]. To radically save chip area, we exploit extensive sharing of the switched capacitor banks and the TRX-antenna transformer matching networks in the TX- and RX-modes combined with inherent digital TRX configurability. Moreover, the bidirectional digital TRX front-end eliminates the need for an integrated T/RX switch, hence eliminating the area overhead and loss/linearity constraints of the T/RX switch. This chapter is organized as follows. We present the proposed bidirectional digital TRX architecture, its operation and theoretical analysis of the digital class-G Doherty switched-capacitor TX in Section 4-2. The detailed circuit implementation is described in Section 4-3. Section 4-4 presents the measurement results and comparison with the state-of-the-art works. Section 4-5 concludes this chapter.

4.2 Operation of Bidirectional Digital Transceiver

Figure 4-2 shows the architecture of a 2-way digital TX, an N path mixer-first receiver, and the proposed bidirectional digital transceiver. The 2-way digital TX can operate as a 2-way digital Doherty TX with parallel power combining. The proposed bidirectional digital TRX merges a 2-way switched capacitor digital TX and an N-path mixer first receiver together through passive reuse. The transformer-based TRX-antenna interface matching network is shared by the TX and RX operations. As on-chip transformer antenna interface banks (C_u), which often occupy a large chip area of the switched capacitor PA and N-path switched capacitor RX, are now shared between the TX/RX modes in our bidirectional TRX architecture as well. Finally, our proposed TRX architecture eliminates the need for an integrated T/RX switch. This reduces antenna-interface loss/linearity constraints and further saves chip area, which improves the overall TRX system performance, such as NF, output power, linearity, and energy efficiency.

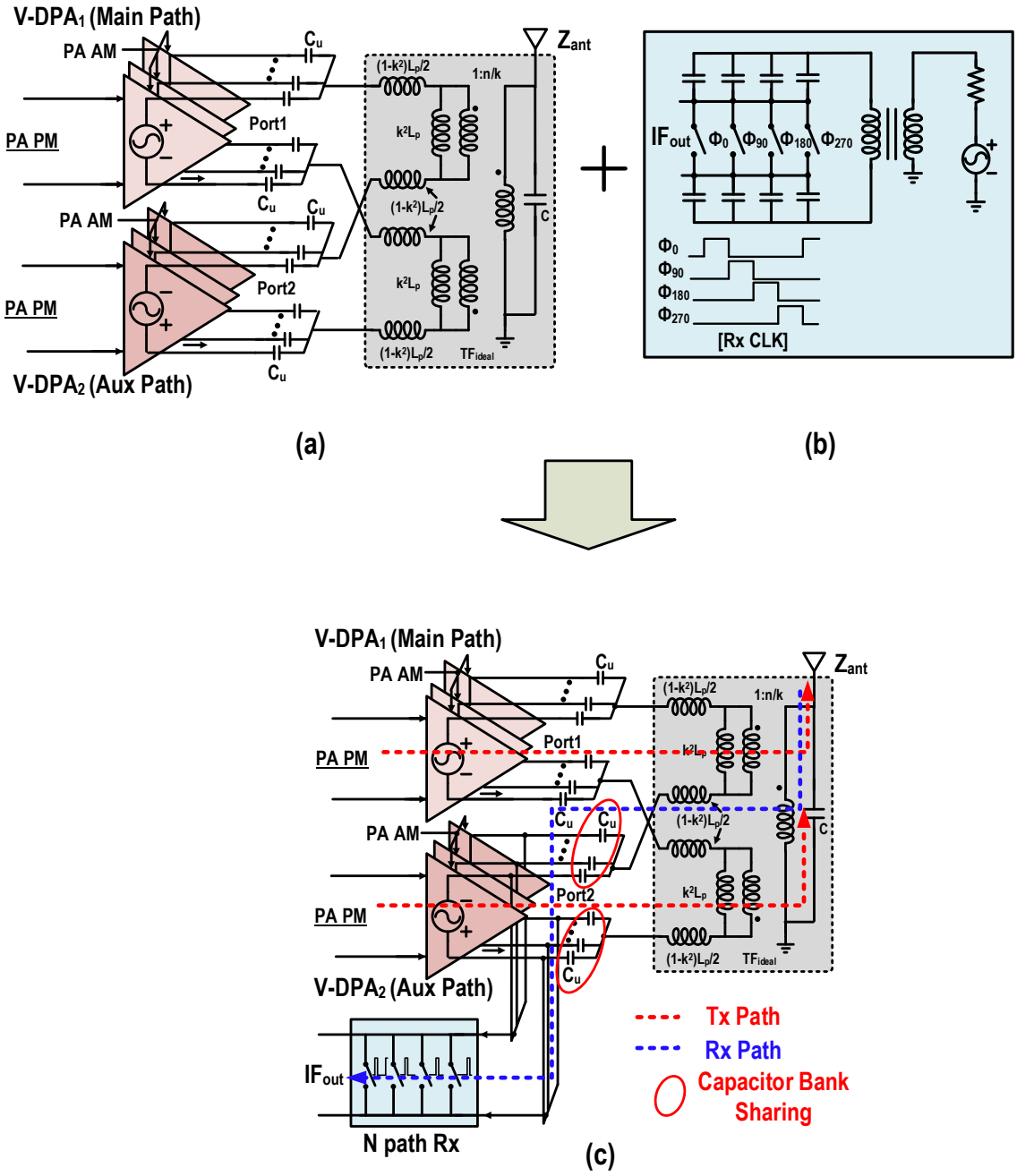


Figure 4-2 (a) A 2-way power combined digital TX that can operate as a 2-way digital Doherty Tx with parallel power combining. (b) An N-path mixer-first Rx. (c) Proposed bidirectional digital TRX architecture with capacitor bank and TRX-antenna passive network reuse

4.2.1 *Digital Transmitter Operation Mode*

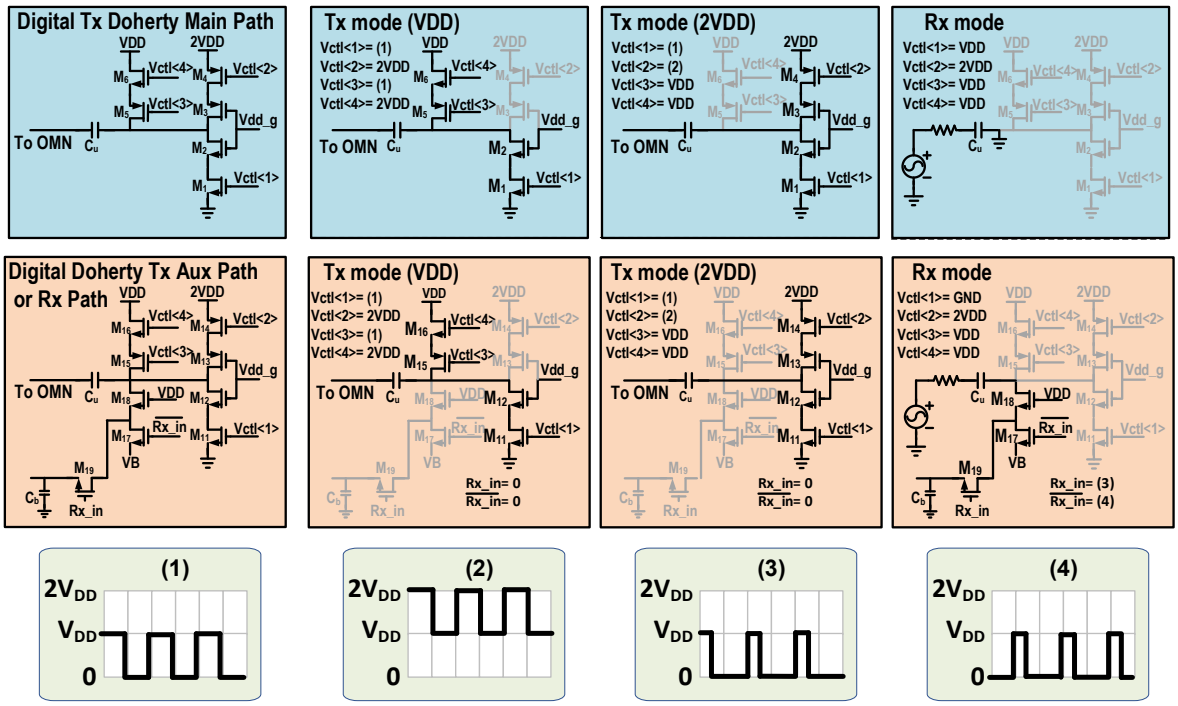


Figure 4-3 TX/RX operation of proposed bidirectional digital TRX frontend

In the TX mode, the proposed digital TRX frontend consists of two PA paths in a parallel transformer-based power combining. The two PA paths serve as the main and auxiliary (Aux) paths, thus realizing a 2-way parallel Doherty PA configuration [55]. A class-G 2-level supply modulator is added to the 2-way switched-capacitor Doherty PA to boost the backoff efficiency (Fig. 4-3). The TX mode is divided into two operations, the

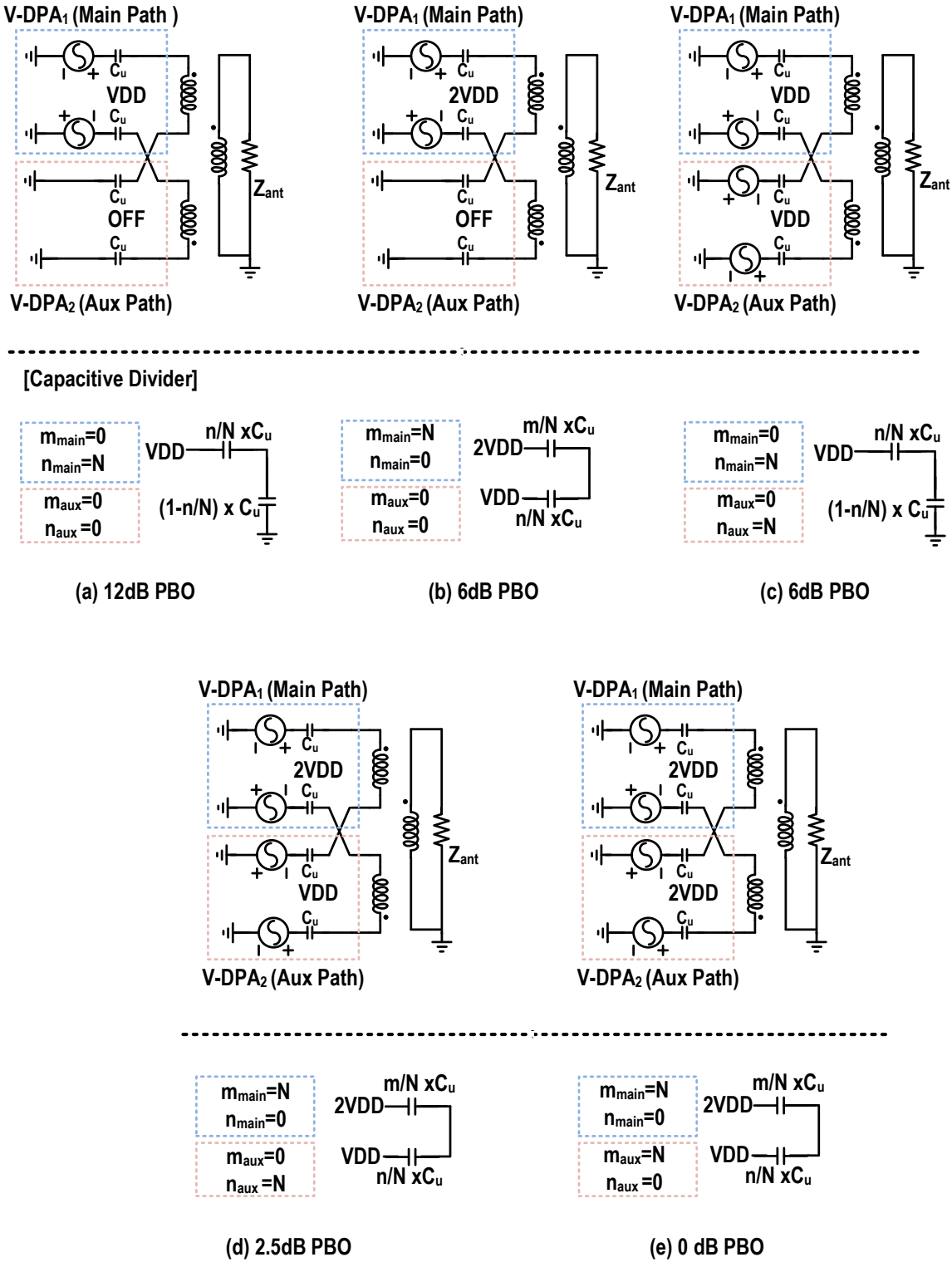


Figure 4-4 TX operation (a) 12dB PBO (b) 6dB PBO (c) 6dB PBO (d) 2.5dB PBO (e) 0dB PBO

VDD mode and 2VDD mode, depending on the class-G operation and the output power level. While in TX mode operation, the main path operates exactly the same as class-G operation and the transistors (M_{17}~M_{19}), which is not related to TX operation in Aux path, are turned off. Thus, it acts identically to class-G operation. The transistor, M_{18} is added to prevent breakdown when the TX operates in 2VDD mode. In this operation, we adopt the natural supply transition class-G architecture[27] to minimize phase discontinuity. The proposed TX operation is the following. As the output power increases, each Main switched capacitor PA cell turns on sequentially until 12dB PBO. When the Main cell path is fully turned on, the Aux cells gradually turn on, which improves the efficiency peak at 6dB due to Doherty load pull operation. After the Main and Aux PAs are fully switched on to VDD mode, the Main PA cells are gradually switched from VDD to 2VDD mode. This improves the efficiency at 2.5dB PBO, and then the Aux PA cells are gradually turned on to 2VDD mode as well. The complete turn on sequence is detailed in Fig. 4-4 (a)-(c)-(d)-(e). An alternative turn-on sequence is the following. All the cells of the Main path are sequentially turned on to VDD mode (up to 12dB PBO) and then sequentially switched to 2VDD mode (up to 6dB PBO). Then, for the Aux cells, we gradually turn them on to VDD (up to 2.5dB PBO) and change them sequentially to 2VDD mode (Fig. **Error! Reference source not found.**4-4 (a)-(b)-(d)-(e)). We explain in detail below the differences between the two turn-on sequences and how they work within the proposed structure. The major performance equations V_{out}, P_{out}, Q_{load}, $\eta(DE)$ of differential class-G SCPA in Fig.4-4 are given below[87]:

$$V_{out} = \frac{2}{\pi}[(2m_M + n_M + 2m_A + n_A)Vdd] \tag{4-1}$$

$$P_{out} = \frac{Vout^2}{2R_L} = \frac{1}{R_L}\frac{2}{\pi^2}Vdd^2(2m_M + n_M + 2m_A + n_A)^2 \tag{4-2}$$

$$Q_{load} = \frac{2\pi fL}{R_L} = \frac{1}{2\pi fCR_L} \tag{4-3}$$

$$\eta = \frac{P_{out}}{P_{out} + P_{cd} + P_{sw}} = \frac{1}{1 + \frac{P_{cd}}{P_{out}} + \frac{P_{sw}}{P_{out}}} \tag{4-4}$$

where, m, n, and Q_{load} are the fraction of unit cells operating in 2VDD mode, the fraction of unit cells operating in VDD mode, and the loaded quality factor of the output matching network (OMN), respectively. In addition, the subscripts M and A indicate the Main and Aux path, respectively. The power dissipation of capacitive divider (P_{cd}) and switching loss (P_{sw}) are defined as the following[26]:

$$\begin{aligned} P_{cd} = {} & [4m_M(1 - m_M) - 4m_M n_M + n_M(1 - n_M) + \\ & 4m_A(1 - m_A) - 4m_A n_A + n_A(1 - n_A)]CV_{DD}^2 f \end{aligned} \tag{4-5}$$

$$P_{sw} = \frac{{V_{dd}}^2}{2\pi R_{ON}}\frac{f}{f_{SW}}(4m_M + n_M + 4m_A + +n_A) \tag{4-6}$$

When we look at the losses relative to the power delivered to output matching network, it can be seen that P_{cd} of different sequences are the same regardless of the operation sequence but P_{sw} is different according to each sequence following by below equation.

$$\frac{P_{sw}}{P_{out}} = \frac{\pi}{4}\frac{R_L}{R_{on}}\frac{f}{f_{sw}}\frac{(4m_M + n_M + 4m_A + +n_A)}{(2m_M + n_M + 2m_A + n_A)^2} \tag{4-7}$$

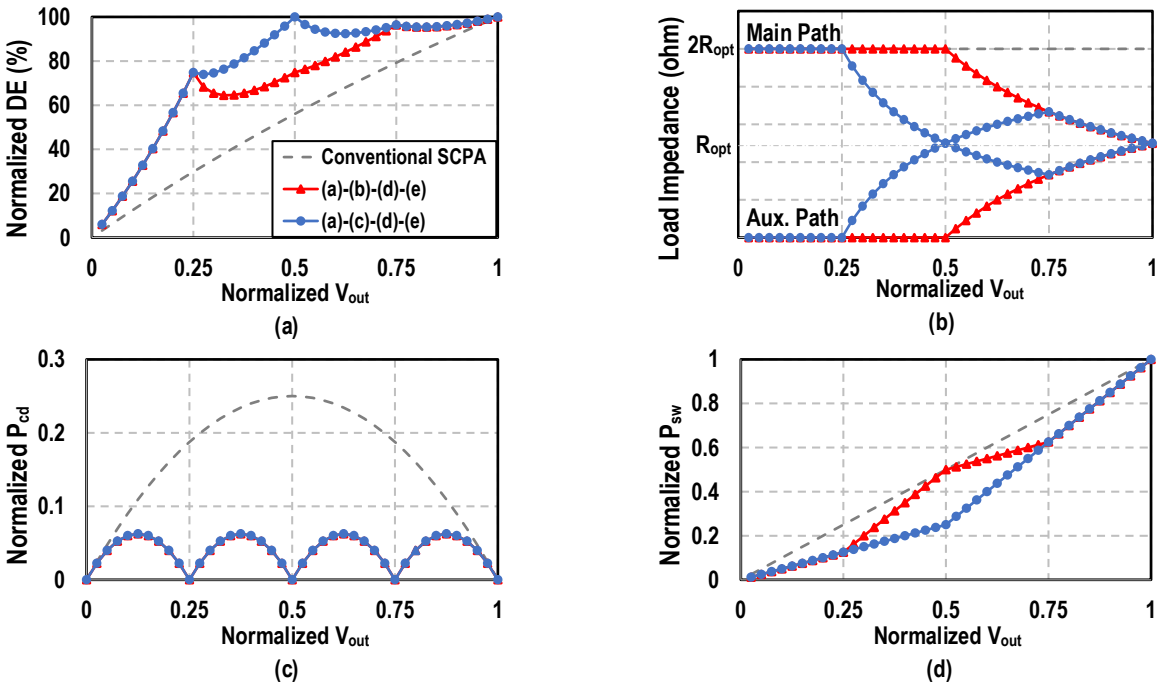


Figure 4-5 Comparison of a conventional SCPA and the class-G turning on sequences of a 2-way Doherty PA (a) Normalized DE (b) Load impedance (c) Normalized capacitive divider loss (d) Normalized switching loss (Q_{load}=1, R_{on} =3ohm, f_{sw}=24GHz, f=2.4GHz)

Where, R_{ON} and f denote on-resistance and operating frequency, respectively.

Letting A = $\frac{\pi}{4}\frac{R_L}{R_{on}}\frac{f}{f_{sw}}$, the relative switching loss to the power delivered the output matching network at 6 dB Back off depending on the sequence becomes the following:

$$\frac{P_{sw}}{Pout}\left(6dB, Fig.4.(b)\right) = A \tag{4-8}$$

$$\frac{P_{sw}}{Pout}\left(6dB, Fig.4.(c)\right) = \frac{1}{2}A \tag{4-9}$$

Figure 4-5 shows the results of the normalized efficiency, load impedance and normalized losses according to sequence (a-b-d-e) and sequence (a-c-d-e) assuming that other losses

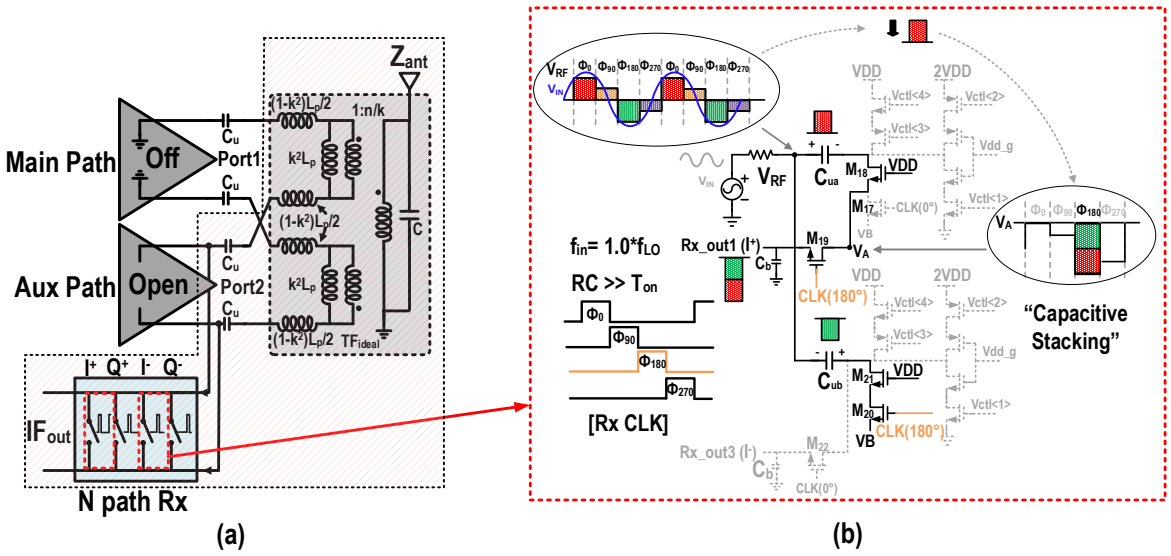


Figure 4-6 (a) Overall operation in RX mode of proposed bidirectional TRX and (b) Schematic operation of RX mode.

(Insertion loss, conduction loss) are the same. From these results, the TX operation uses sequence (a-c-d-e) method in order to have the best PBO efficiency performance.

4.2.2 Mixer First Receiver Operation Mode

The overall operation of the mixer first RX and the equivalent circuit schematic operation are highlighted in Fig. 4-3 and Fig. 4-6 (a)-(b). During RX mode operation, VDD is connected to the gate of M_1 (V_{ctl}<1> in figure 4-3) of the Main path, and the Main path is shorted to GND through M1, resulting in a low impedance. Since the TX cells are turned off, this is equivalent to the TX operating in the very low power region. Therefore, due to the Doherty operation of the OMN, the impedance presented to the Aux path increases, enhancing OOB linearity and voltage gain. For the Aux path, the transistors associated with TX operation are turned off and floated (M_{11}-M_{16}) as detailed in figure 4-3. Therefore, the

TX path inherently has minimal impact of the RX operation and hence it is possible to perform RX operation properly without an additional switch in the Main PA path.

In the RX mode, the proposed circuit performs bottom plate sampling to achieve better linearity by reducing the modulated on-resistance[48]. The RX operation in our proposed architecture adopts the capacitive stacking technique to achieve additional voltage gain for enhanced sensitivity [15].

We now detail the conceptual operation of the proposed receiver cell. To ease the analysis, we assume that V_{RF} consists of a single sinusoidal wave input, and we consider the behavior of a bottom plate N-path mixer first receiver with resistor and capacitors as shown in figure 4-6. The switches are ideal and have negligible on resistance. We assume the RC time constant is much larger than the on-time (T_{on}) of the switch. All the switches are driven by 4-phase non-overlapping 25% duty-cycle clocks provided by a divide-by-2 circuit. As the single-ended RX input is converted to a differential signal at the N-Path mixer through the transformer-based balun, the output is differential quadrature as well. The capacitor, C_{ua}, which is connected to the bottom plate, is connected to the read-out capacitor (C_b) though the switch, M_{18}. After a large number of switching cycles, each capacitor is assumed to have stored the average value of the input signal seen during its ON-time. Applying a 180-degree LO to M_{20} turns on and turns off the M_{17} operating in different phases. Since this structure uses a 4-phase clock for quadrature receiving, we can ensure that the voltage charged to C_{ua} and the voltage charged to C_{ub} are anti-phase. Therefore, the read-out capacitor, C_b, can get as much voltage gain as the C_{ua} and C_{ub} combined. The voltage at each C_u is the down-converted baseband voltage stored in the capacitor because $f_{in} = f_{Lo}$. This results in a 6-dB

voltage gain occurring similarly at 0°, 90°, and 270°. For these in-band signals, the baseband (BB) current is converted to a BB voltage V_{BB} via transimpedance amplifiers (TIAs)[49].

4.3 Proposed Bidirectional TRX Architecture

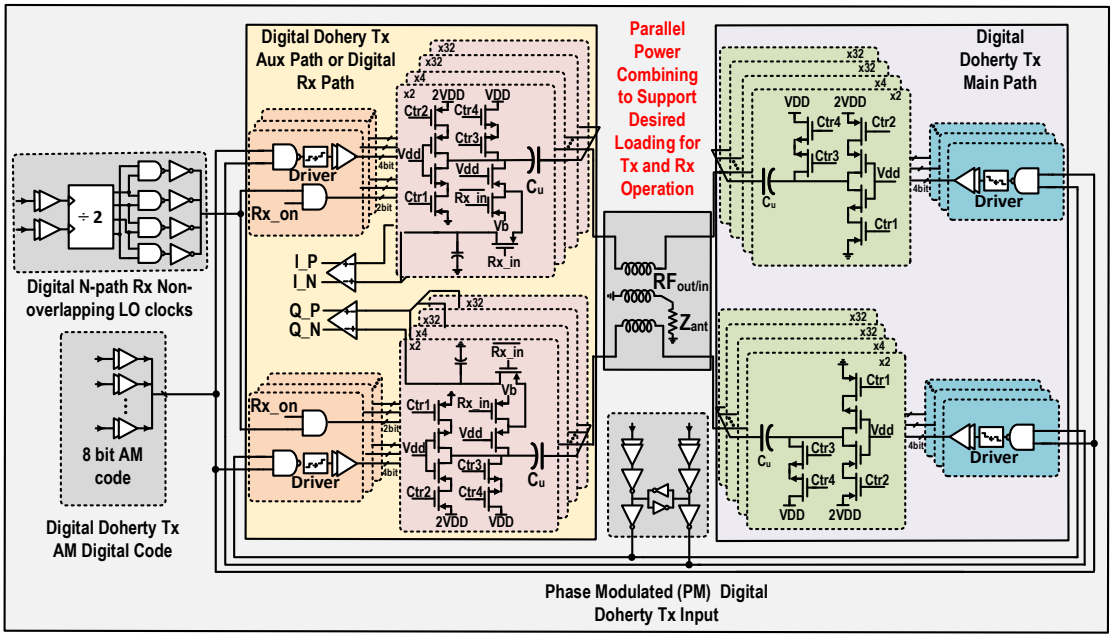


Figure 4-7 Top schematic of proposed architecture

Figure 4-7 shows the top schematic of the proposed bidirectional digital transceiver with single transformer footprint parallel Doherty output matching network. This proposed structure consists of a parallel Doherty OMN, a conventional class-G DPA, a newly proposed T/RX class-G PA, Phase modulated (PM) digital TX input driver, RX 4- phase non-overlapping clock, an 8-bit AM driver and an RX op-amp. In TX mode, the Main and Aux path are controlled by an 8-bit AM code. 1 bit enables the RX mode, and when enabled, all schematics related to TX are disabled as shown in figure 4-3. The proposed transceiver is implemented in 45nm SOI CMOS process with 1.98mm x 2.57 mm chip area

(including pads). The IC is wire bonded to a PCB to provide DC and control inputs and the RF is probed.

4.3.1 Proposed Bidirectional T/Rx Schematics

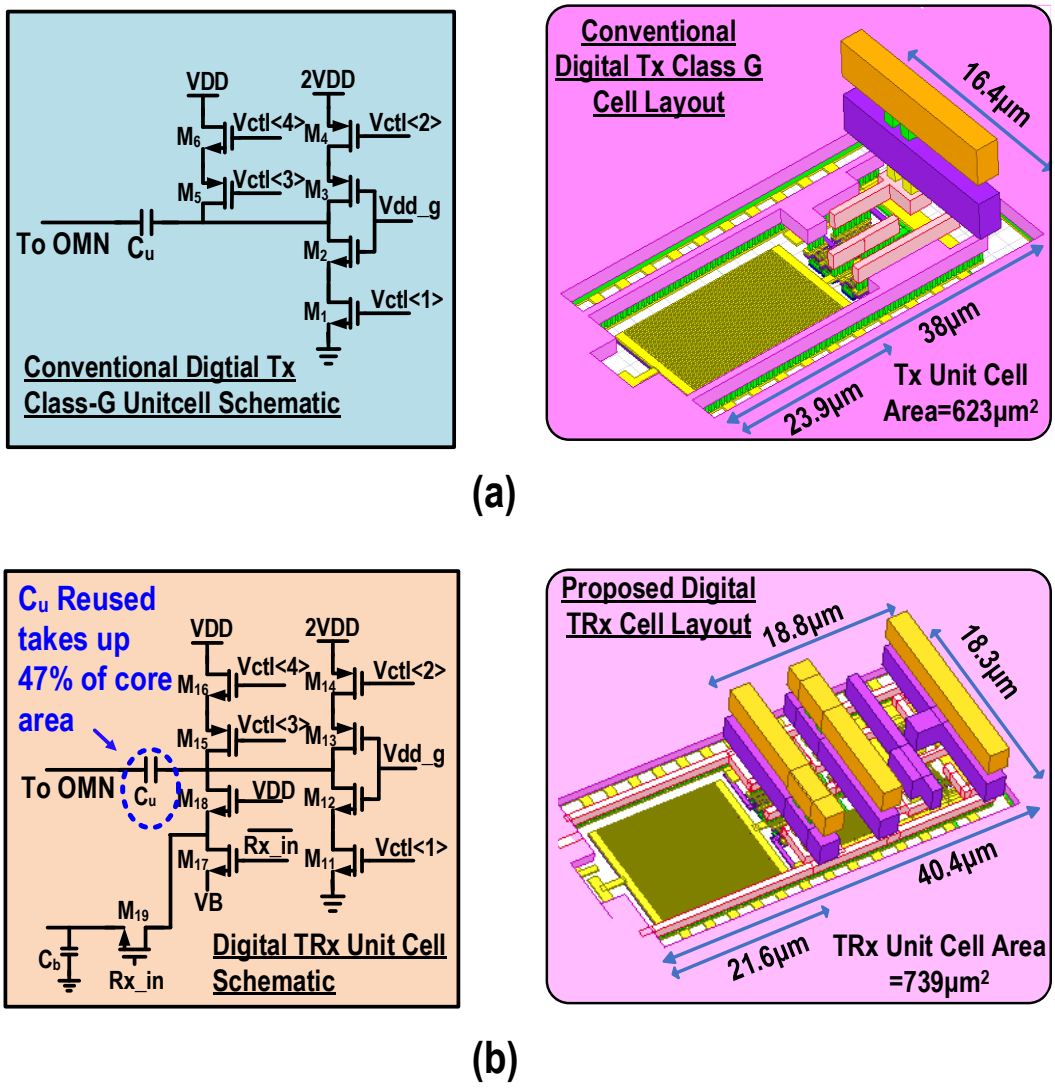


Figure 4-8 Schematics and layout of (a) Conventional class-G unit cell (b) Proposed digital T/RX class-G unit cell.

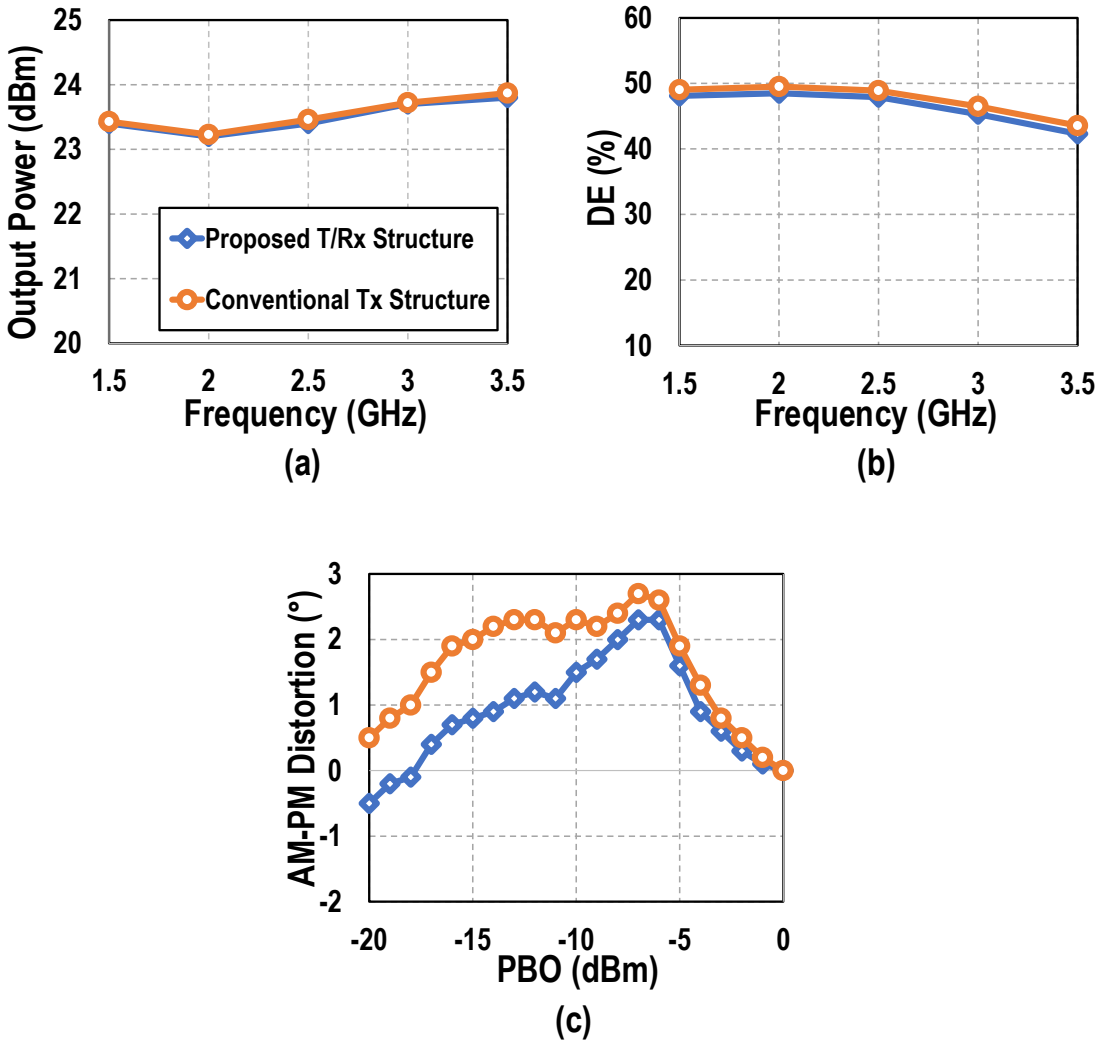


Figure 4-9 Simulated results of proposed T/Rx structure and conventional Tx structure (a) Output power (b) Drain Efficiency (c) AM-PM distortion.

Figure 4-8 shows schematics and layout in detail. Figure 4-8 (a) shows the schematic and layout of the conventional class-G unit cell. It occupies a total area of 623μm^2. Within the cell, the capacitor size occupies a high area overhead, accounting for 47% of core area in class-G switched capacitor PA unit cell. Figure 4-8 (b) shows the schematic and layout of the proposed bidirectional T/RX cell. The value of shared capacitor is the same, and layout is approximately 740μm^2 primarily due to the additional required read out capacitor (C_b) for

the receiver. By sharing the capacitors that occupy the largest area in the SCPA and N path mixer first receiver, we can add the RX functionality with an additional area overhead of only 19%. In addition, the Aux TX path is extended to share with the RX mode. The Aux TX path is chosen for the TRX sharing because the Doherty Aux path typically has lower impact on the overall TX gain and linearity compared to the Main path[52] . Figure 4-9 shows the simulated Tx results with conventional class-G structure and newly proposed T/RX class-G structure. As we can see in the Fig. 4-9, the results of newly proposed T/Rx structure are almost same as conventional class-G.

4.3.2 Output Matching Network (OMN)

The 3-D EM model of the single footprint output network and its simulated passive efficiency according to frequency are shown in Fig. 4-10. This OMN supports Doherty operation and parallel power combining. The OMN occupies an area of 0.212mm^2. It achieves a wide band operation from 1.2GHz to 5GHz with a loss less than 1dB for the band of interest. Figure 4-11 shows the output waveforms of the Main and Aux paths when the RX mode and TX mode are enabled for operation, and the corresponding load impedance seen in each path during the operation. Note that there is an inherent tradeoff between the transmitter and receiver. In the RX mode, high input impedance is desired to get better OOB linearity (IIP3)[15]. However, in TX mode, the output impedance should be proposed lower to increase the output power. To meet these requirements, this proposed circuit uses parallel Doherty output matching networks. In RX mode, the Main path is

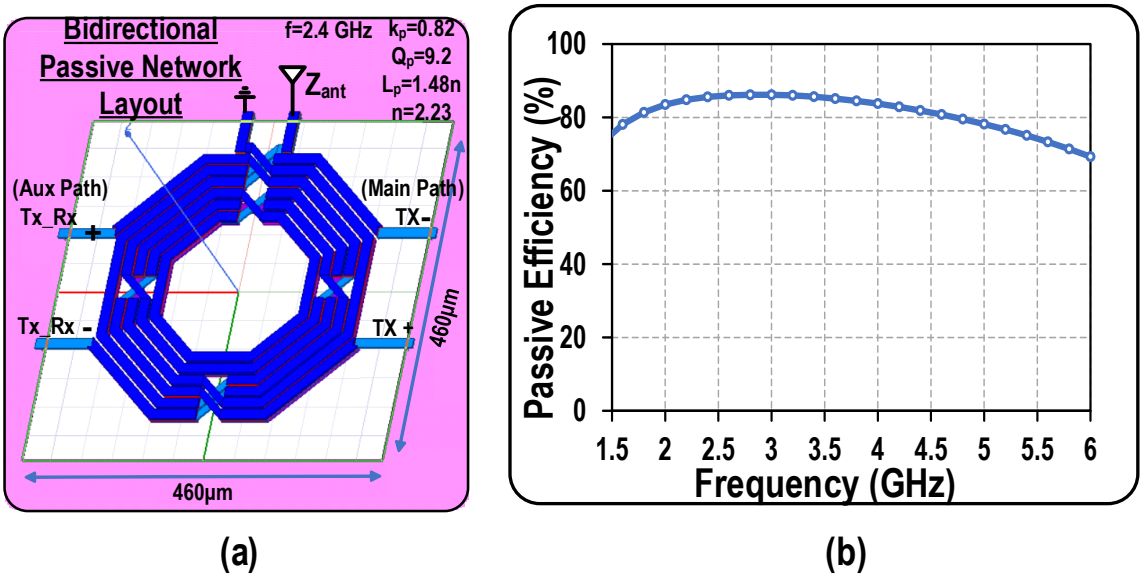


Figure 4-10 (a) 3-D EM model of single footprint transformer (b) Simulated results of passive efficiency.

turned off and is low impedance thanks to voltage mode operation [81]. Thus, its impedance is around 50 ohms. For TX mode, each cell turns on gradually according to the required output power, and the turning on sequence follows as analyzed in Section 4-2 to get better efficiency in PBO status. Once the Main cell turns on to VDD mode (Fig. 4-11 (b)), the Aux path also turns on to VDD mode (c) and thus employs Doherty operation and achieves backoff efficiency enhancement. After all the turned-on cells are operating in VDD mode, the Main cells start to turn on to 2 VDD mode (d) and then the Aux cells start to change from VDD to 2VDD mode (e). The active load modulation impedance of each PA path is derived below:

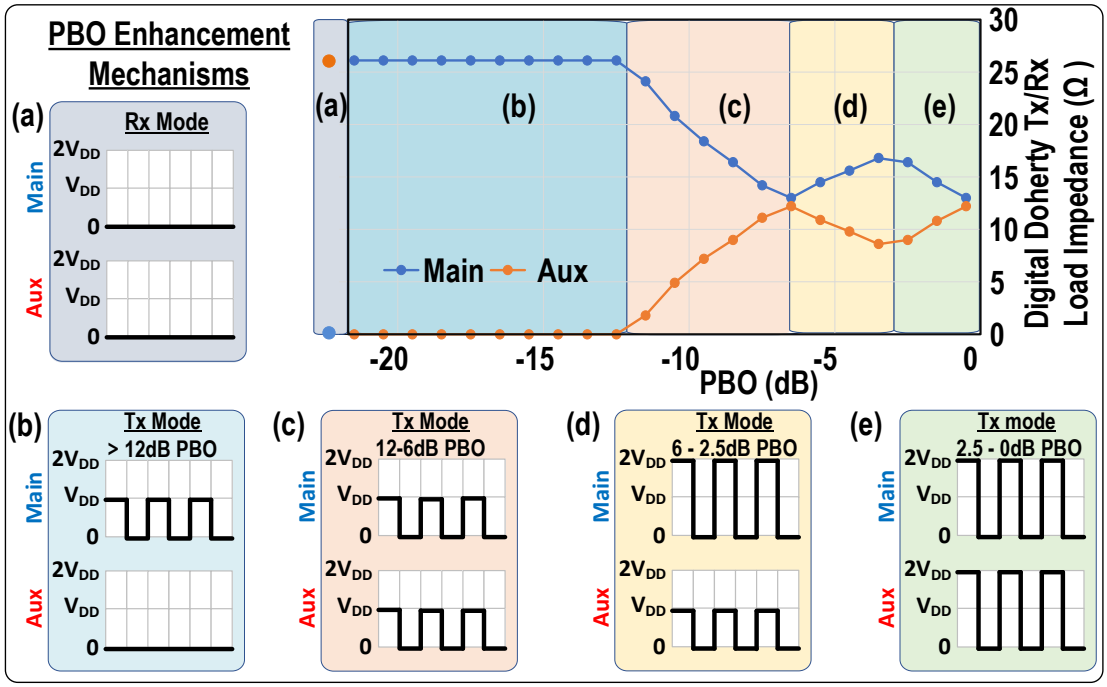


Figure 4-11 Active load impedance of each operation (a) RX mode (b) TX mode less than 12dB PBO (c) TX mode 12-6dB PBO (d) TX mode 6-2.5dB PBO (e) TX mode 2.5-0dB PBO

$$Z_{Main} = R_L(\frac{k}{n})^2 \frac{1}{(1+\frac{2m_A+n_A}{2m_M+n_M})} \tag{4-10}$$

$$Z_{Aux} = R_L(\frac{k}{n})^2 \frac{1}{(1+\frac{2m_m+n_m}{2m_A+n_A})} \tag{4-11}$$

where k is the magnetic coupling coefficient of OMN, n is the turn ratio of OMN, m and n are the number of bits turned on power cell of 2VDD and VDD, respectively. The overall active modulation results are shown as Fig. 4-11.

4.3.3 Routing Line Floorplan

In TX mode, the Main and Aux path are controlled by an 8-bit AM code. The Main and Aux paths consist of 7-bits. Among them, 6-bits control the number of unit cells in an unary and binary manner and 1-bit controls the supply modulation between 2VDD mode and VDD mode. There is 1-bit control, Rx-on. When the Rx-on bit is turned

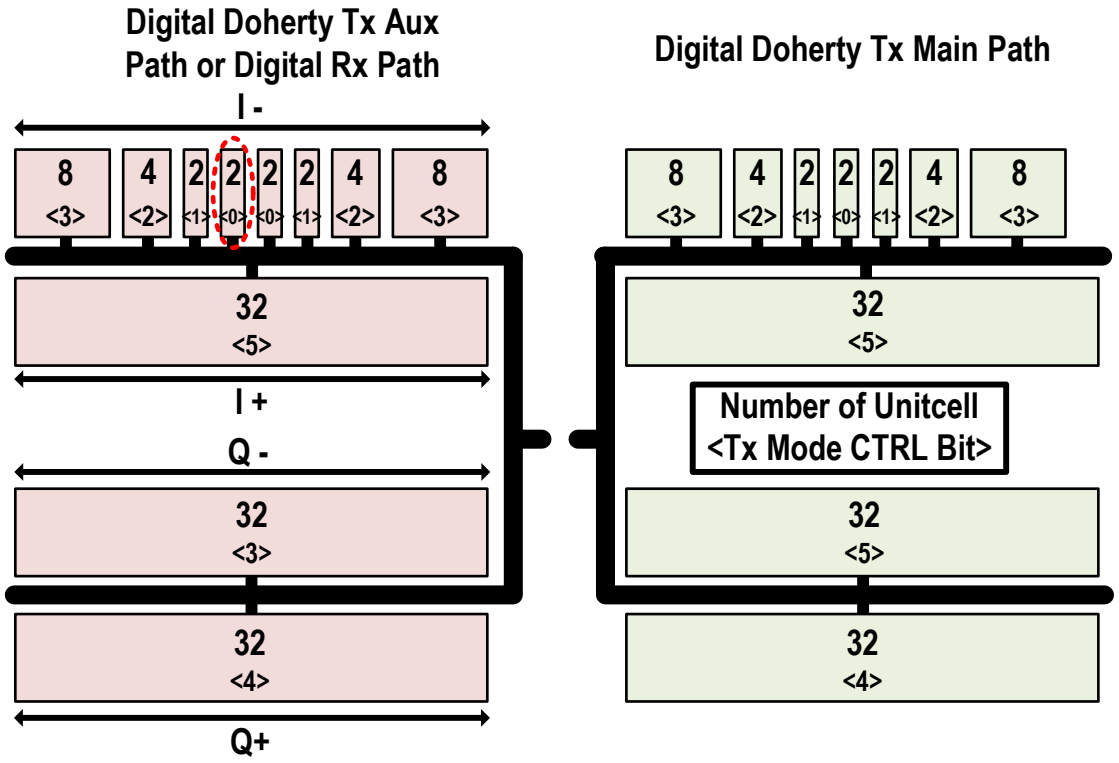


Figure 4-12 Routing line of Main path and Aux path

on, all the Tx cells are turned off. The Main and Aux cells are distributed symmetrically along the output feeding to minimize phase offsets. Additional minimum sized cells are added in the Aux path to balance the I/Q signals when in RX mode.

4.4 Measurement Results

The bidirectional digital transceiver is implemented in the Global-Foundries 45-nm CMOS SOI process, and the chip photograph is shown in Fig. 4-13. This is a fully integrated design with two sub-PAs, output passive network, input TX PM driver and AM buffer array, RX mode PM driver and op-amp. The dc supply is 2.2V and 1.1V for the PA and drivers respectfully. The chip is mounted on an FR4 printed circuit board (PCB) and on-wafer probed for the following measurements.

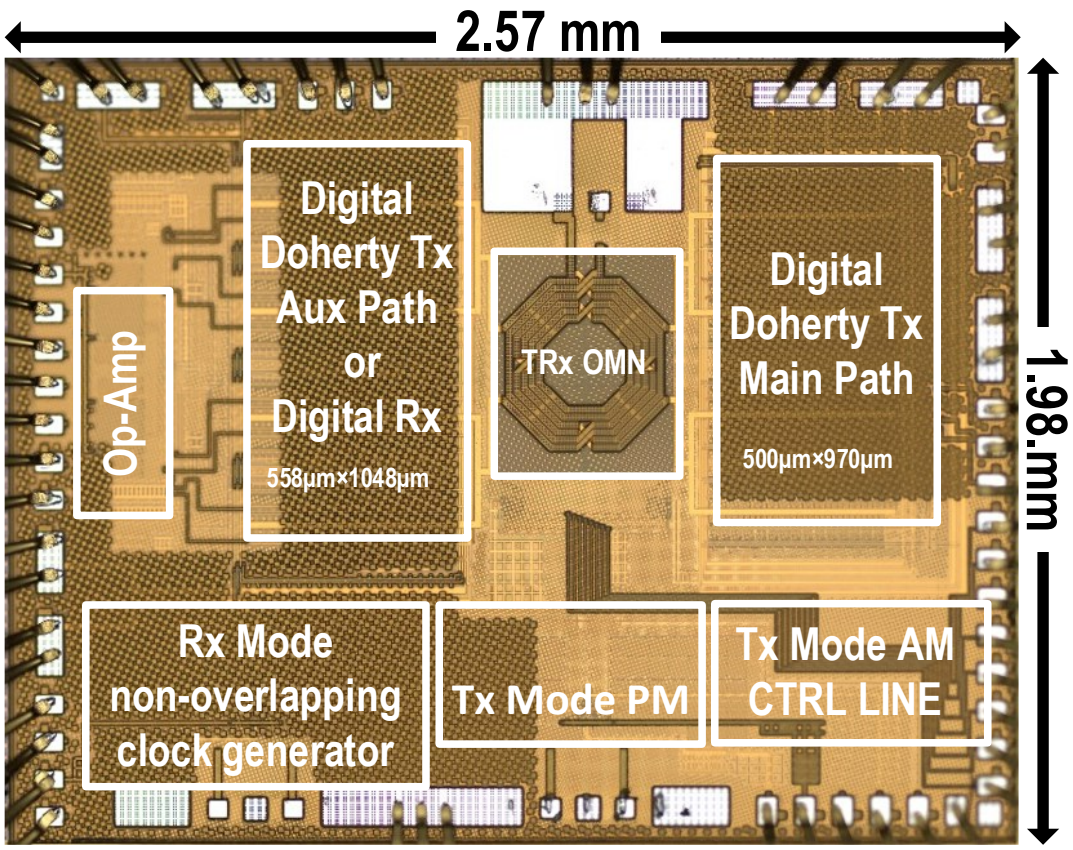


Figure 4-13 Chip photograph

4.4.1 Transmitter CW Measurement Results

Figure 4-14 shows the test setup for CW measurement. The PA is first characterized using continuous wave (CW) signals with a 50 ohms standard load. A CW signal is generated by a signal generator (N5193B) (Keysight), converted to a differential signal by an off-chip balun (Krytar4010180), and fed to the PA differential input. The PA output is monitored by a power meter (N1913A) to measure Pout and PA efficiency. The AM sequence is controlled using an USB-1024LS with custom LabVIEW code. Figure 15 shows the measured PA output power and the drain efficiency. The measured peak PA P_{out} and Peak/2.5dB/6dB/12dB PBO drain efficiency (DE) are 22.8dBm and 42%/38%/32%/18% at 2.4GHz, respectively. The PBO efficiency enhancement is 1.25×/1.51×/1.72× at 2.5/6/12dB PBO respectively compared to a class B PA. The measured peak drain efficiency is 49.5% at 1.8GHz. This design supports wideband operation from 1.8GHz to 3GHz and its fractional bandwidth is 63%.

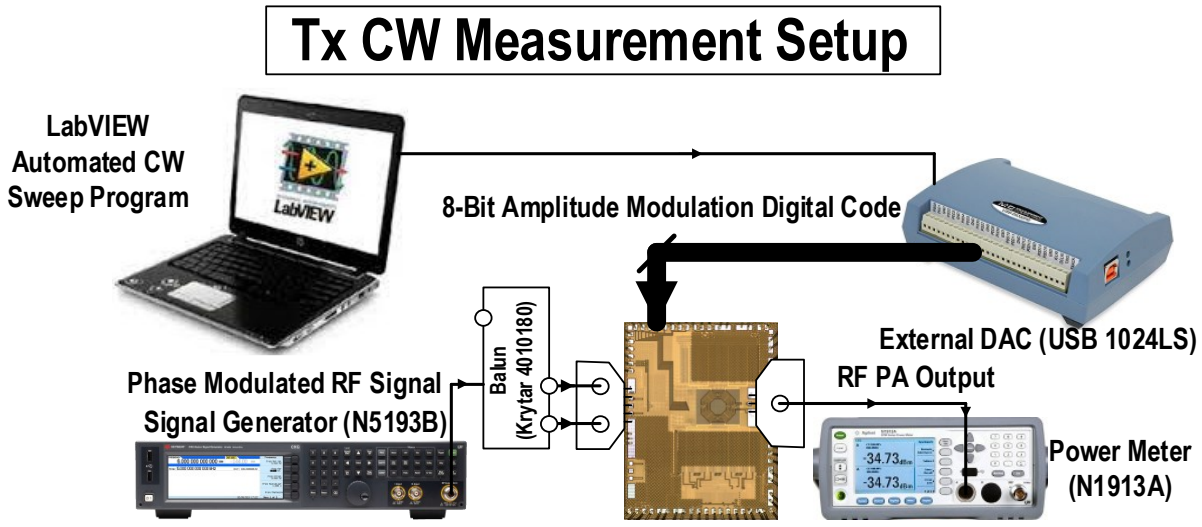


Figure 4-14 TX CW measurement setup

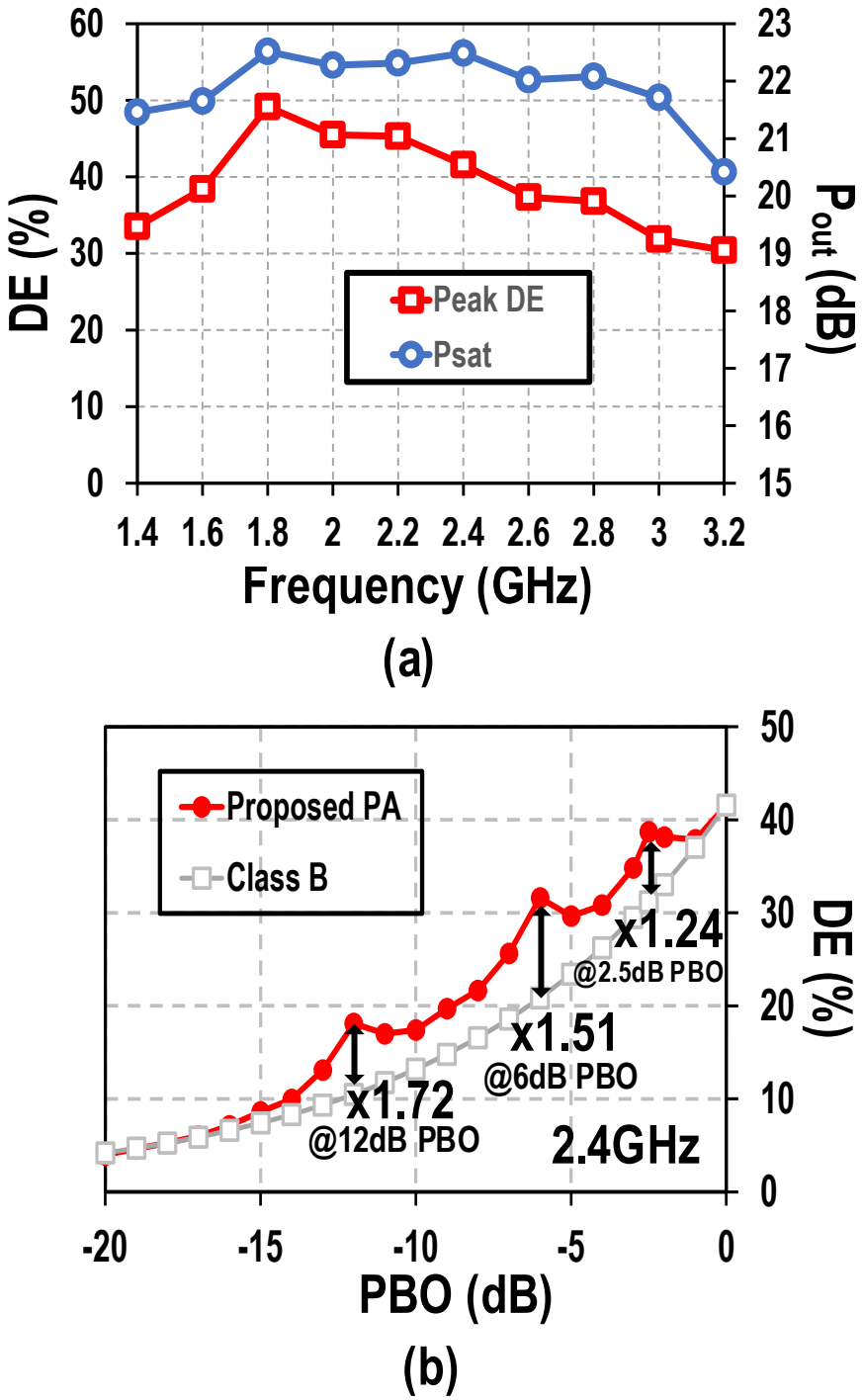


Figure 4.15 (a) TX output power and drain efficiency (b) PBO efficiency enhancement results.

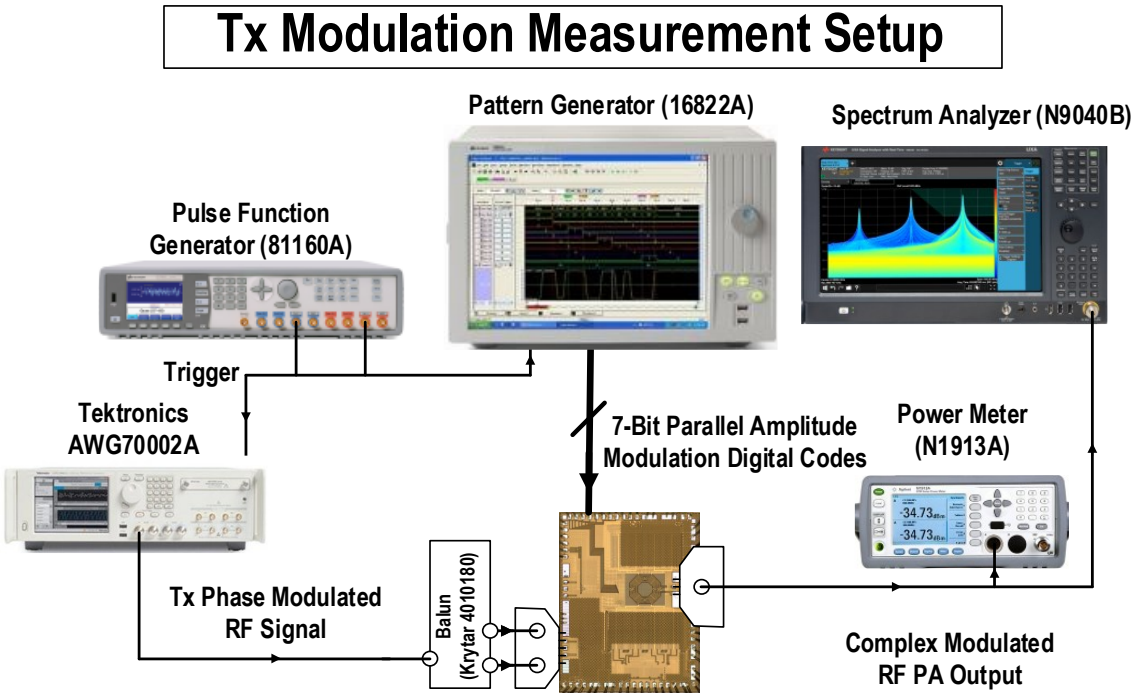


Figure 4.16 TX modulation measurement setup

4.4.2 Transmitter Modulation Measurement Results

The PA is then characterized with modulated signals. High-order modulated signals are generated in advanced design system (ADS) and separated into AM and PM signals for polar operation. The memoryless 1-D AM-AM lookup table (LUT) that can be readily generated is used to control the desired AM signals. The AM-AM LUT is generated by a pattern generator (Keysight 16822A) for the modulated AM signals. An arbitrary waveform generator (Tektronix AWG7002A) generates the RF PM signals (64-QAM).

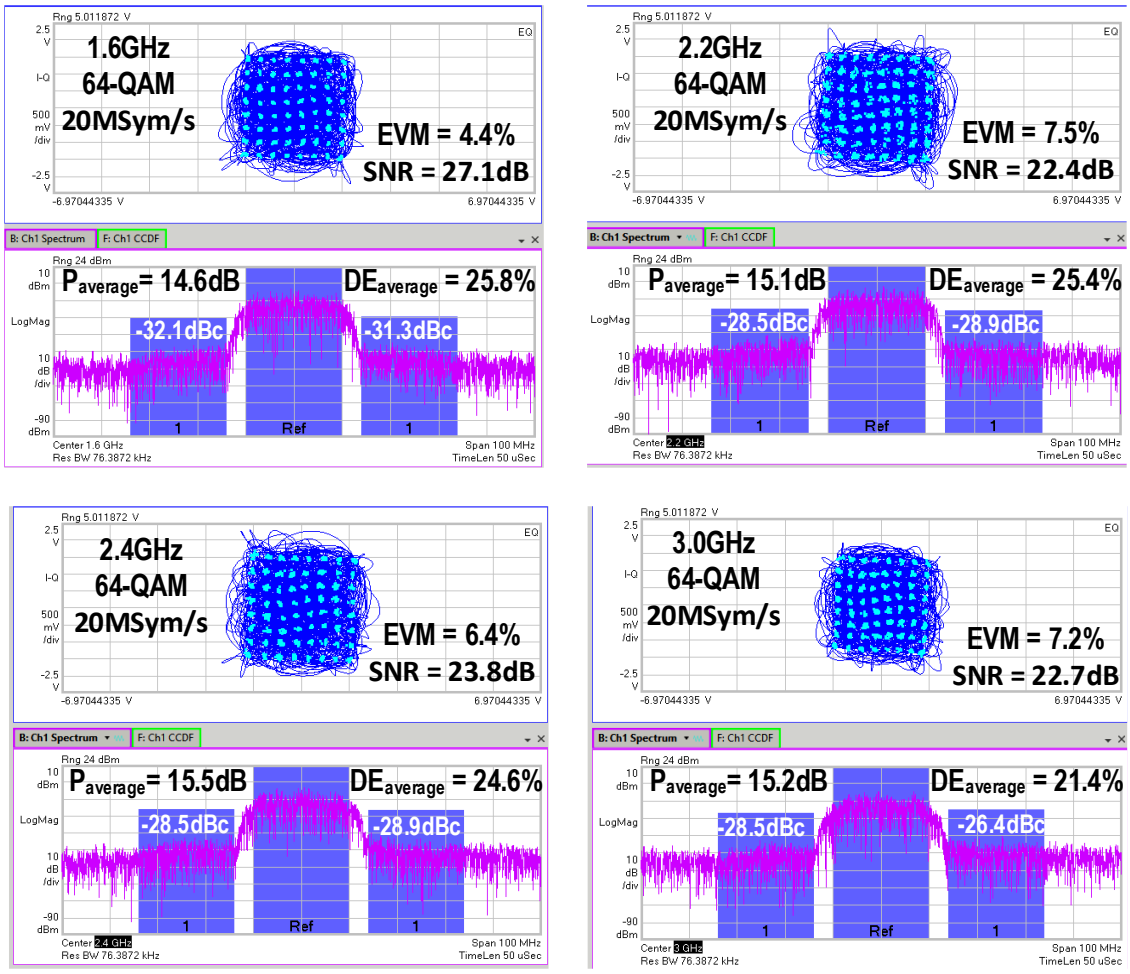


Figure 4-17 TX modulation results at 1.6GHz, 2.2GHz, 2.4GHz, and 3.0GHz without any phase compensation

The output signals from the PA are demodulated by a real-time oscilloscope (Keysight MSO840A) or Spectrum analyzer (Keysight N9040B). A pulse function arbitrary generator (Agilent 81160A) triggers 16822A and AWG7002A to synchronize the AM and PM signals with a fine delay control. We use single-carrier 64-QAM with 20Msym/s for modulation tests. Figure 4-17 shows the demodulated error vector magnitude (EVM), adjacent channel leakage ratio (ACLR), average output power (P_{avg}), and average DE(DE_{ave}) with single-carrier 64-QAM at 1.6GHz, 2.2GHz, 2.4GHz and 3.0GHz. The measured $Pout_{ave}$ value is 14.6 dBm with 25.8 DE_{ave}. The measured EVM is 4.4%, while

the ACLR is -32.1/-31.3 dBc at 1.6GHz. Note that no DPD is performed during modulation tests. The TX performance summary of the proposed bidirectional transceiver and the comparison with other state-of-the-art digital transmitters is shown in Table 4-2. We achieve competitive efficiency, bandwidth, and area with respect to the state of the art while also supporting embedded RX functionality.

4.4.3 Receiver Results

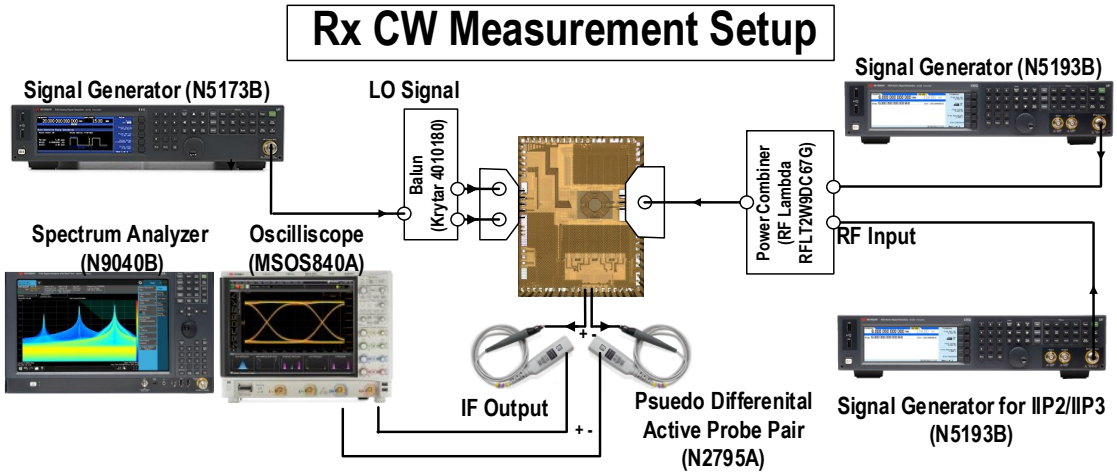


Figure 4-18 RX modulation measurement setup

Figure 4-18 shows the test setup for RX measurement. A CW signal is generated by a signal generator (N5193B) (Keysight), converted to a differential signal by an off-chip balun (Krytar4010180), and fed to the LO differential input. The input signal is fed to the mixer first receiver and the I/Q outputs are used to measure gain. We achieve a conversion gain of 17dB from 1.6GHz to 3.0GHz with 12 MHz bandwidth. RX has a low

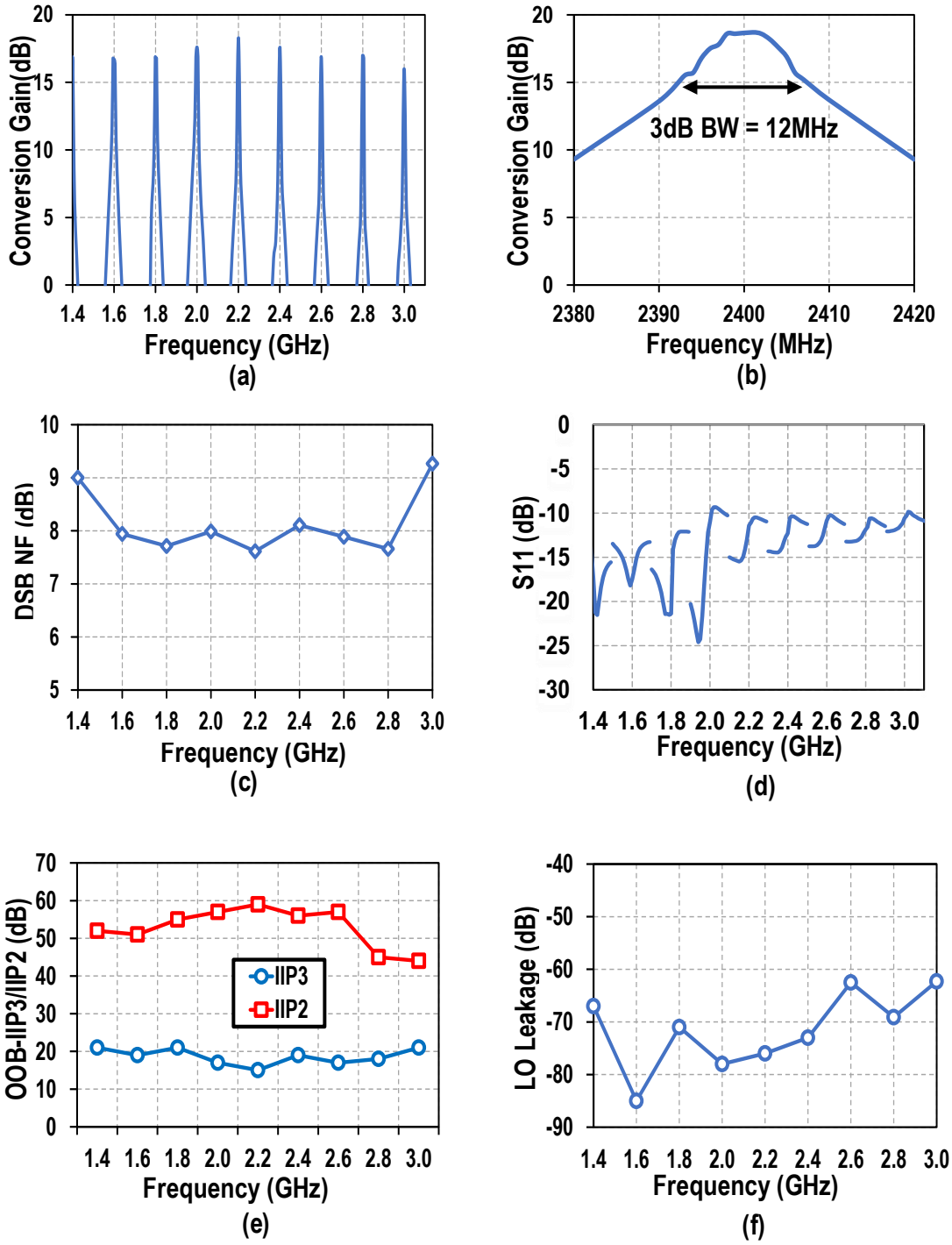


Figure 4-19 RX results (a) Conversion gain (b) Bandwidth of conversion gain (c) DSB Noise figure (d) S11 (e)OOB-IIP3/IIP2 (f) LO Leakage

return loss of <-10dB across the operational bandwidth, i.e., F_{LO} = 1.6 to 3GHz. The OOB IIP3 is -30dB and OOB IIP2 is -59 dB. The proposed front-end achieves <-60 dBm. LO leakage across the operation frequency range. Figure 4-19 shows the RX performance summary of the proposed bidirectional transceiver and the comparison with other state-of-the-art N path mixer first receivers is shown in Table 4-3. As we can see from the results, this proposed architecture is implemented with a small area compared to the state of the art due to the transformer and capacitor reuse.

4.5 Conclusion

This Chapter presents a bidirectional digital transceiver architecture by sharing OMN and capacitor banks. The proposed new architecture exhibits the highest peak DE and a competitive bandwidth. Furthermore, this proposed design supports additional receiver functionality without any performance degradation. To the author's knowledge, this is the first demonstration of a bidirectional digital T/RX sharing a switched capacitor and single transformer matching network. This work also presents the smallest RX core area compared to the reported designs as it shares the capacitors in TX. The potential area savings and performance enhancement of this design makes it a promising candidate for compact formfactor applications.

Table 4-2 Comparison of the state-of-the-art Digital Transmitters

	This work	JSSCC 2016 * Hu	JSSC 2017 * Vorapipat	JSSCC 2019 * Yoo	RFIC 2019 * Hung	JSSCC 2019 * Zhang	ISSCC 2020 * Yoo
Architecture	Polar T/Rx class G	Class-G + Doherty polar	Class-G +Doherty polar	Class-G IQ-cell-shared	Quadrature Doherty class- G	Polar Multi-SHS class-G	Polar TI-Doherty single-supply Class-G
Technology	45nm SOI	65 nm	45nm SOI	65 nm	65 nm	65 nm	65 nm
Bidirectional Operation	Yes	No	No	No	No	No	No
Matching Network	1 Transformer	2 Transformer	2 Transformer	2 Transformer	2 Transformer	3 transforemr	2 Transformer
Supply [V]	2.2 / 1.1	2.8 / 1.4	2.4 /1.2	2.5 / 1.2	2.55 /1.25	3.6 /2.4	2.5
Frequency [GHz]	2.4	3.71	3.5	2.2	2.2	2.2	2.4
1dB RF BW [GHz]	1.6 - 3.1Ghz (63.8%)	3.1 - 4.7(41%)	2.9 - 4.3 (38.9%)	N/A	N/A	1.65 - 2.2 (28.5%) **	NA
Peak Power [dBm]	22.8dBm	26.7dBm	25.3dBm	30.1dBm	27.8dBm	28.7dBm	30.0dBm
Peak DE/PAE	49.5% (DE)	40.2% (DE)	30.4% (PAE)	37% (PAE)	32.1% (PAE)	42.4% (DE)	40.2% (DE)
Number of η peaks	3	2	3	1	4	5	6
Modulation	20MHz Single-Carrier 64 QAM	1MHz Single-Carrier 16 QAM	10MHz Single-Carrier 256 QAM	20MHz Single-Carrier 64 QAM	20MHz Single-Carrier 1024 QAM	5MHz 52 Sub-Carriers 16 QAM	10MHz Single-Carrier 1024 QAM
Avg. Power [dBm]	14.6dBm	20.8dBm	19dBm	19.5dBm	21.0dBm	22.8dBm	23.2dBm
Avg. Efficiency	25.8% (DE)	28.8% (DE)	24% (PAE)	14.7% (SE)	18.4% (SE)	31.4% (DE)	36.2% (DE)
EVM [dB]	-25.8	-24	-35	-40.7	-43	-24.7	-44.5
Acitve Area (OMN+Cells) [mm^2]	1.281	1.571**	0.327**	1.202**	0.904	2.966**	1.341**
DPD	No	No	Yes	Yes	Yes	Yes	No

* Unidirectional digital Tx/Rx performance without including the passive loss of the T/R switch
** Estimated from paper

Table 4-3 Comparison of the state-of-the-art Mixer First Receivers

	This work	JSSC10* Andrews	RFIC15* Nejdel	ISSCC15* Z.Lin	RFIC 16* Westerveld	JSSC18* Lien	JSSCC 2020* Purushothaman
Technology	45nm SOI	65nm	65nm	65nm	65nm	45nm SOI	22nm FDSOI
Bidirectional Operation	Yes	No	No	No	No	No	No
Frequency [GHz]	1.4 - 3.1	0.1 - 2.4	2 - 3	0.1 - 1.5	0.03 - 0.3	0.2 - 8	0.6 - 1.3
DC Power [mW]	64 @2.4GHz	37.2 - 69.6	27.4 - 75.4	11	43.2 - 46.1	56 - 296	0.4 - 0.78
Gain [dB]	17	40 - 70	7.5	38	21 - 36	21	9 - 14
IF BW [MHz]	12	10	3-10	2	2-40	10	16
DSB-NF [dB]	7.6 - 9.5	3 - 5	2.5 - 4.5	2.9	6	2.3 - 5.4	5 - 9
OOB IIP3 [dBm @ f/BW]	15 @ 10	25 @ 10	26 @ 33.3	10 @ 15	41 @ 20	39 @ 8	25 @ 10
OOB IIP2 [dBm @ f/BW]	59 @ 10	56 @ 10	65 @ 33.3	47 @ 15	90 @ 20	88 @ 8	66 @ 10
LO Leakage [dBm]	< -60	<-65	<-60	N/A	N/A	<-65	<-70
Supply [V]	1.1	1.2 / 2.5	1.2	0.7 / 1.2	1.2	1.2.	0.8
Active Area [mm^2]	0.13	0.75**	0.23**	0.028**	0.8**	0.8**	0.23**
Matching Network/Balun	On-Chip	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip

* Unidirectional digital Tx/Rx performance without including the passive loss of the T/R switch
** Estimated from paper

CHAPTER 5. CONCLUSION

In this dissertation, we presented novel digital PA and digital RF front-end architectures related to linearity and miniaturization required in modern communication systems. The presented techniques/works can support a variety of existing/emerging applications such as IoT, portable devices. More specifically, we present a hybrid current mode/ voltage mode digital PA and bidirectional digital front-end architecture that uses one output matching network to support broadband highly linear power combining and concurrent TX/RX impedance transformation. Continued research on this work will allow the incorporation of more diverse digital PA technologies, enabling the design of miniaturized chips with further enhanced linearity performance that can communicate without the need for DPD.

5.1 Research Summary

In Chapter 2, we review the state-of-the-art digital power amplifier and mixer first receiver. For digital PAs, they can be divided into voltage mode and current mode. The structure and operating principles of SCPA in voltage mode DPA and class-D^{-1} DPA in current mode DPA are explained, and the research directions that have been further studied for each method are also explained. The mixer first receiver also describes the structure and operation principles and the research trend of the mixer first receiver. The limitations of all these designs are detailed to properly motivate the proposed two architectures in this thesis.

Chapter 3 proposed a single footprint hybrid current/voltage mode digital Doherty PA with built-in large signal AM-PM distortion compensation, capable of supporting large PAPR and high-speed modulation signals without any DPD linearization. The principle of AM-PM distortion in voltage mode DPA and current mode DPA are analyzed and an adaptive biasing scheme in current mode DPA is proposed to mitigate the AM-PM distortion. Class-G operation as voltage mode PA was introduced to achieve efficiency enhancement and AM-PM nonlinearity reduction. In addition, to improve linearity through a hybrid method, current mode DPA was implemented in the main path and voltage mode DPA in the Aux path. For the first time, the voltage mode digital PA and the current mode digital PA were made into a Doherty structure using a single transformer. The chip prototype achieves a peak PAE of 37.6% with a P_{sat} of over 21.8dBm from 1.2-2.4GHz. The PA also achieves a 1.2×/1.4× PBO efficiency enhancement, compared to the ideal class-B at 3/6dB PBO at 1.2GHz. This proposed digital PA supports 20MSym/s 64-quadrature amplitude modulation (QAM) at 14.8dBm average output power and 22.8% average PA DE while maintaining error vector magnitude (EVM) lower than -23dB without any phase pre-distortion.

Chapter 4 presents a bidirectional digital transceiver architecture by sharing OMN and capacitor banks. Furthermore, this proposed design supports additional receiver functionality without any performance degradation. To the author's knowledge, this is the first demonstration of a bidirectional digital T/RX sharing a switched capacitor and single transformer matching network. This work also presents the smallest RX core area compared to the reported designs as it shares the capacitors in TX. The potential area savings and performance enhancement of this design makes it a promising candidate for

compact formfactor applications. We also detail the theory on the efficiency as a function of the order of the Doherty operation in, whereby we propose an optimal order of operation. The proposed new architecture exhibits the highest peak DE and a competitive bandwidth. The TX demonstrates a Pout 1dB bandwidth (BW) of 1.6-3.1 GHz, a fractional BW >63%, and peak output power of 22.5dBm at 2.4GHz. The peak drain efficiency (DE) of the TX is 49.5% at 1.8GHz and 41.5%/38.7%/31.6%/18.1% for the peak/2.5/6/12dB power back off (PBO) at 2.4GHz. The DE improvement compared to class-B PA is 1.24×/1.51×/1.72× at 2.5/6/12dB PBO. The TX is measured using 64-QAM/20MHz modulation without the use of AM-PM pre-distortion or pattern based DPD. It achieves an excellent -27.1dB EVM, -31.31dBc ACLR, 14.6dBm average Pout and 25.8% average DE at 1.6GHz. The RX achieves a noise figure (NF) of 7.6dB at 2.2GHz and a conversion gain of 17dB with a 12 MHz bandwidth. In addition, the proposed RX front-end achieves < -60 dBm LO leakage over the operating frequency range.

5.2 Future Work

This research mainly focuses on the new architecture to enhance linearity and to maximize digital RF advantages by reusing passive components. This dissertation represents only the beginning of research on this architecture. There is a plethora of opportunities to extend the application of CMOS digital RF circuits. Several interesting opportunities for future work are as follows:

1. Although the proposed PA operates broadband, it only operates below 5GHz. PA research on extending the operating frequency is needed to meet the current

growing data traffic demands. By applying the current mode DPA, which is advantageous at high frequencies, and the adaptive biasing technique proposed in Chapter 3, it will be worth studying digital PA that operates without DPD by improving AM-PM even at higher frequencies.

2. In this paper, the principle of AM-PM nonlinearity of class-D^{-1}, SCPA and Class-G structure was analyzed using time domain. It would be meaningful to analyze the nonlinearity of AM-PM of each DPA through frequency domain and study the nonlinearity that changes by power combining through output networks, including Doherty structures.
3. The new structure of implementing Tx/Rx using capacitors and output networks, which are passive devices, is now considered to be the same as opening the door to new research. Based on the new circuit structure used in this paper it would be worthwhile to study the optimal digital front end by combining mixer first receiver with various digital PA structures such as SHS and SFCPA as well as class-G structure.

5.3 Research Publications

5.3.1 Conference Publications

[1] **J. Lee**, D. Jung, D. Munzer, and H. Wang, "A Compact Single Transformer Footprint Hybrid Current-Voltage Digital Doherty Power Amplifier," Proc. IEEE Radio Frequency Integrated Circuits **(RFIC)**, Jun. 2022.

[2] **J. Lee**, D. Jung, D. Munzer and H. Wang, "A Compact Wideband Joint Bidirectional Class-G Digital Doherty Switched-Capacitor Transmitter and N-Path Quadrature Receiver through Capacitor Bank Sharing," 2022 IEEE Custom Integrated Circuits Conference **(CICC)**, 2022, pp. 1-2.

5.3.2 Journal Publications

[1] **J. Lee**, D. Jung, D. Munzer, and H. Wang, " An Ultra-Compact CMOS Broadband Bidirectional Digital Transceiver Frontend with Capacitor Bank and Transformer Matching Network Reuse," IEEE Access,2022.

[2] D. Munzer, N. S. Mannem, **J. Lee** and H. Wang, "A Broadband Mm-Wave Current/Voltage Sensing-based VSWR-Resilient True Power/Impedance Sensor Supporting Single-Ended Antenna Interfaces," IEEE Journal of Solid-State Circuits (JSSC), 2022.

[3] N. S. Mannem, J. Park, E. Erfani, E. Liu, **J. Lee** and H. Wang, "A Reconfigurable Phase-Time Array Transmitter Achieving Keyless Secured Transmission and Multi-Receiver Localization for Low-Latency Joint Communication and Sensing," IEEE Journal of Solid-State Circuits (JSSC), 2023.

[4] **J. Lee**, D. Jung, D. Munzer, and H. Wang, " A Digital Power Ampligier with Built-In AM-PM Compensation and A Single-Transformer Output Network," IEEE Open Journal of the Solid-State Circuits Society (OJ-SSCS), Under Review.

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