Characterization of Commercial Dielectric Zaristo-700 as a Redistribution Layer Material for Advanced Packaging

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CHARACTERIZATION OF COMMERICAL DIELECTRIC ZARISTO-700 AS A REDISTRIBUTION LAYER MATERAL FOR ADVANCED PACKAGING

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SUMMARY

This body of work, in detail, outlines the fundamental steps taken to characterize a material for novel use in RDL build-up layers for advanced packaging. The material (Zaristo-700) discussed in this was only used in RF applications, and now we are exploring use in the wiring layers. In the PRC, research into thin films, spin-on films, and many other dielectrics have been published before. It is important to understand that this work is necessary to establish a "library" or catalog of information on all the materials we use to be able to provide the correct material depending on the goals of future projects. Below is the outline of how this thesis is organized.

For chapter 1, a brief introduction on the evolution of the microelectronics industry through Moore's Law, the importance of packaging, an introduction to dielectric materials, and the purpose of exploring dielectrics (Zaristo-700) for use in redistribution layer build-ups (RDL).

In chapter 2 we will focus on the methodologies of how to fabricate the tri-layer stacks of the Zaristo-700. All the techniques have been used prior, but the novelty of this work comes from building up three layers of this Taiyo, Ink. dielectric. The concept of the three metal layers is derived from Chris Blancher, where an eight-metal layer design was used in another project not containing this dielectric.

Chapter 3 is on system fabrication, more specifically how every step is optimized before fabrication is completed. Images of testing and the wafers during each process step are showcased here.

Chapter 4 has detailed descriptions of the electrical measurements done on test structures (daisy-chains and capacitor pads), and an analysis of warpage of the two Si substrates used after fabrication through Shadow-moir*é* measurements.

Chapter 5 is a discussion of the results and analyses conducted in Chapter 4, and what was learned from this body of work. Next, we go through a checklist to see if everything was accomplished through this demonstration.

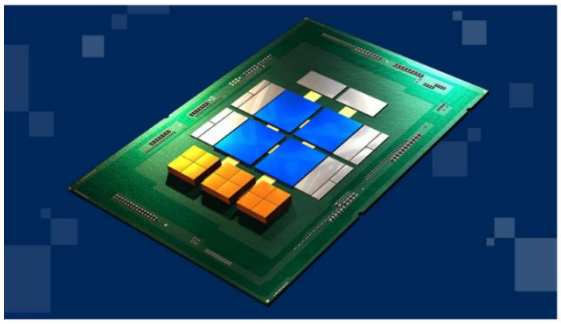
Lastly, Chapter 6 is the conclusion of this project and future directions for the demonstration of the Zaristo-700 tri-layer stack-up. Recommendations for future researchers and items that were not reached become the next steps for these test structures.

CHAPTER 1. INTRODUCTION

Since the introduction of the transistor by Bell Labs in 1947, the microelectronics industry has had spectacular scientific advances due to the day-to-day necessities of the human population. Moore's Law is what dictated the growth of microprocessors, stating that every two years the number of transistors in ICs doubles. But as the complexity of these devices increases, continued miniaturization of them becomes extremely difficult. This led to the slowing of Moore's Law and the scaling of microelectronics could no longer follow it. Addressing these challenges is done by the development of advanced packaging systems. Packaging technologies supply the industry with unique scaling for microprocessors, so the added pressure of following Moore's Law is removed [1].

Industry is looking to newer technologies that revive decade old concepts, such as chiplet technology, to address the challenges posed by scaling. The concept of a "chiplet" has been around for some time but was brought into the limelight by researchers at the University of Michigan. It originates from the combination of "chip" and "petite" and is translated to meaning small. Chiplet based designs offer a potential solution to the increasing size, costs, and difficulty of manufacturing monolithic ICs as specialized chiplets can be combined and assembled into a more complete system. Architectures based off chiplet designs give companies more benefits over the traditional SoC (system-on-a-chip) which include, performance, reduced power consumption, and increased design flexibility. This is the future of extending Moore's Law and help industry keep up with the predictions calculated by it. Smaller chips may not require or accept the most advanced SoC applications, therefore chiplet technology allows for easier fabrication with little to no

defects. Later, it will be discussed on how advanced packaging is the way to maintain via density predictions based on Moore's Law (*Figures 1a and 1b)*.



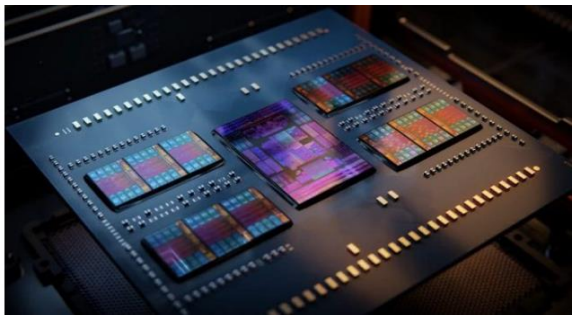


Figure 1a and 1b: Intel and AMD Chiplet Schematics (AMD offer 96 5.0 nm Cores across 12 chiplets).

1.1 Concepts of Advanced Packaging

A relevant question to ask is "what is packaging and why is it important?" Back in the day the simple answer would have been protection of the ICs and their subsequent units. Four key functionalities of a package, during the period of Moore's Law, were known as power distribution, dissipation of heat, signal distribution, and package distribution. Otherwise known as interconnecting, powering, cooling, and protecting the system components of the devices. As miniaturization continues, advanced package processing accounts for system design and testing for more complex applications and increased yields. Packaging is not only for protection, as the end goals have changed in that systems are now consumer electronics. Such as smartphones, tablets, advanced computing and so on. These systems are known as Heterogeneous integration or 3DI where the packaging architecture makes up for connecting system components [2].

The advanced packaging sector is heavily impacted by how material intensive it is. Included in this are a large family of materials such as ceramics, glasses, composites, polymers, and metals. For the purposes of this thesis, dielectrics/polymer-based materials are the focus for the build-up of the RDL in a package. The *redistribution layer* (RDL) is the layer of material in which the metal wiring layers are made (*Figure 2)*. Dielectrics are materials with much wider bandgaps than that of semiconductors, in which they can only be insulators that are excellent or poor in nature depending on their k value. This constant is referred to as the dielectric constant where it defines whether a dielectric material is a good insulator for protection or good for signaling speed in the metal wiring of an RDL in a package [3].

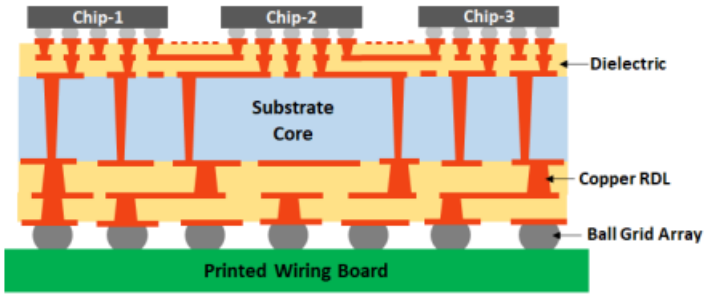


Figure 2: Schematic of standard RDL dielectric within the packaging substrate.

1.2 Key Addresses of Dielectric Properties

Dielectrics are extremely vital, not just for their properties, but for what they mean in the realm of packaging. In general, we use them for increasing the reliability of the complex packages created to solve the world's most pressing issues. They not only provide physical and structural stability, but they give us more functionality for the function of a

package. The main reason for dielectrics in the RDLs of advanced packages and the silicon substrate (CMOS) processes are for isolation between the wiring routes within it.

Properties of dielectrics are the keys to solving physical and electronic issues of both high-tech and low-tech applications. The main properties and measurable parameters are the resistivity, loss tangent, dielectric constant, surface adhesion, and leakage current. It is known that for present day applications low-k dielectrics are promoted for their higher signal speeds and lower heat dissipation. To understand the difference between low and high, we must discuss what the dielectric constant is (κ). This constant is a measure of a material's ability to store electrical energy. Meaning a material with a high dielectric constant stores more electrical energy or charge, than a material with a low dielectric constant. To be a low-k dielectric the material must have a k-value less than that of SiO_2 ($\kappa < 3.9$). For consideration as a high-k dielectric, the material's k-value is greater than SiN ($\kappa < 7$). It will be demonstrated that low-k materials are in demand for quick response, higher speed, and little-to-no delay applications. A comparison between the two categories is necessary to establish what is considered "high" or "low."

1.3 The General Industry Trend

The silicon-based dielectrics have been the key dielectrics in the manufacturing of ICs and other semiconductor devices for decades. Industry has the tendency to want low-k dielectrics as their performance for more sophisticated applications tends to be excellent. Low-k dielectrics allow for faster signaling speeds and due to their small k-values they can discharge parasitic capacitance out of the RDL. These materials allow for physical transistor scaling to continue without the pressure of keeping up with Moore's Law, and

therefore higher density applications for improved computing power can be fabricated. Miniaturization has been the goal of industry for decades, but the physical limitations are being met so Low k's are the material of choice to go around these blockades. Buzzwords like 3D-ICs and Heterogeneous Integration (3D-HI) float around in industry as wafer-to-wafer, chip-to-wafer, or chip-to-chip mean the limitations can be overcome. This is the future of IC fabrication, where Moore's Law stopped, HI can continue a new law of scaling that relieves the pressure on chipmakers. In brief, instead of scaling laterally (x) or vertically (y), 3D-ICs (HI) are scaling in the third dimension or z-direction as industry calls it. Looking at *Figure 3*, hybrid and fusion bonding applications are shown. The difference between the two is that hybrid bonding is the joining of two patterned wafers along a hybrid interface with exposed metal connections to form the electrical contacts. Where fusion bonding is the joining of a patterned wafer and a carrier wafer or blanket wafer, and with further processing direct access to the backside of the device wafer is enabled. "As transistor sizes continue to shrink to realize Moore's Law, traditional scaling strategies through lateral device dimension reduction have become more challenging… On the other hand, 3D integration technologies such as direct wafer bonding enables next generation device scaling by stacking devices in the transverse direction." [4]

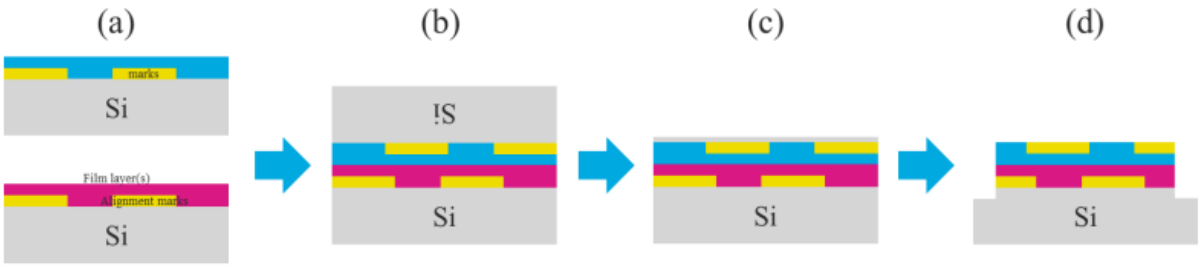


Figure 3: Schematic of permanent bonded wafer integration. (a) Incoming silicon wafers with film stack and alignment marks. (b) Direct wafer-to-wafer (W2W) bonding. (c) Bonded wafers are annealed at elevated temperature for extended time and roughly thinned by mechanical grinding step. (d) Adding thinning steps to remove the remaining device silicon substrate and expose the pattern stack.

Low-k dielectrics are the key to solving the issues above such as density, pitch-scaling within the RDL, and the parasitics that are a result of the more powerful devices within the high-tech computing applications. Therefore, the dielectrics market will rapidly expand to include the growth of the global semiconductor industry and to sustain advancement of 3D-ICs as going in the z-direction is the future [5].

1.4 The Pros and Cons of Higher-κ Dielectrics

As stated in the introduction, high-k dielectrics have k-values above 7.0 and are highly desirable in FEOL transistor work. It is widely known that high-k materials are light-weight, and their fabrication process is facile. In the paper, *Recent advances in polymer-based electronic packaging materials,* there are higher-k materials documented to support why they are necessary and important. But they come with their own set of challenges, hence why they are not utilized in this space. They can be used in the RF sector of advanced packaging for the properties of high break-down voltage and low dielectric loss. These properties are promising for embedded capacitor and electrical energy storage applications. For the higher-k dielectrics, they are used to prevent tunneling effects which increases leakage current in most cases (*Figure 4*). But as it will come to light not all "high-k" materials increase leakage current by a large amount. On a positive note, the higher the dielectric constant the more the materials act as an insulator and as stated are used for protection to isolate copper and other metal wiring layers from each other. Higher-k dielectrics are used in high-speed communication devices that operate with low loss. As well as in BEOL processes for the creation of device gate oxides. "Traditional Dennard

scaling of the SiO_2 gate oxide thickness, with dielectric constant k~3.9-4.0, reached a non-manufacturable limit over a decade ago… New high-k gate dielectrics were required to maintain the gate-to-channel electric field, while ensuring a sufficiently thick oxide layer to be manufacturable… Common examples are SiON, HfO_2, HfSiON, and Al_2O_3." [6] For reference the dielectric constants of HfO_2 is 25 and Al_2O_3 is 9, where some considered to be "high" are closer to 3.0-3.1 which are well within the low-k region.

After reviewing the general industrial trends for polymer dielectrics, low-k is the clear winner in terms of demand for keeping up with the pitch and density scaling of advanced computing applications. Briefly mentioned, SiO_2 has been the reference oxide for many years and now there is a catalog of dielectric properties that people are looking to in industry. The values that researchers are looking to and being guided by are the loss tangent and dielectric constants of materials. In advanced packaging technologies, industry looks to CTE (coefficient of thermal expansion), Young's Modulus (E), and loss tangent of the material. Even for high-k dielectrics these numbers are important, because high-k materials are especially used to create capacitors. In the example given above for gate oxides, the listed parameters are crucial to manufacturability: uniformity, defect density, leakage current, trap density, and breakdown strength. Keeping these numbers in check guarantees a high yield for manufacturability of these advanced devices.

In a paper published by Stanford University [7], when choosing a new high-k dielectric technology there are major requirements to keep in mind. First, it must have a high enough k that it will be used for a reasonable number of years of scaling. Second, the oxide is in direct contact with the Si channel, so it must be thermodynamically stable with it. Third, it must form a good electrical interface with Si. Lastly, it must have a few bulk

electrically active defects. Now, for a gate-oxide the k-value should be higher than SiO_2's of 3.9 since the goal is to be the perfect insulator. Of course, there is a tradeoff with the capacitance of the dielectric meaning it will store more charge as dielectric constant increases. As previously stated, it all depends on the application of interest to a company, whether a low-k or high-k dielectric fits the process.

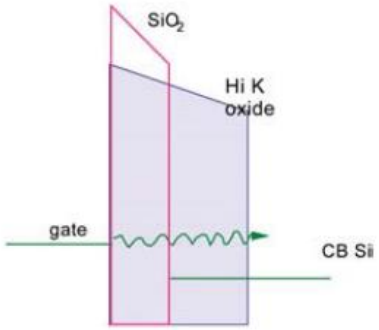


Figure 4: Schematic of direct tunneling through a SiO_2 layer and the more difficult tunneling is through a thicker layer of high κ oxide.

1.5 PRC Research Interest in Dielectrics

Research has taken a multitude of forms, and in this case the data can be seen as an aside to the fabrication steps of the project. Data is the result a scientist looks for when they are stuck at a certain point in either the creation of the samples or at the end when a single answer is needed. A material doesn't have to be novel to solve the higher-level issues, instead one that has already been used for other applications can be explored. The material of choice for this project is Zaristo-700, a dry-film dielectric that has a thickness of 30.0 µm. Its dielectric constant of 3.0-3.1 is somewhat on the high end of the spectrum for the more sophisticated devices of today. But, due to the recent interest in exploring Zaristo-700's properties for possible usage in advanced packaging has been brought to light. In

Table 1, the dielectric constants of today's advanced RDL materials are listed to demonstrate that Zaristo-700 is lower and considered to be within range of these values.

Table 1: List of State-of-the-art RDL Dielectrics

Technology	Package Architecture	Dielectric	Diel. Const.	Diel. Thickness (µm)	RDL L/S/via (µm)	Process
Shinko iTHOP [2,5]	2.5D organic interposer	Polymer	3.9	>5	2/2/10	Semi-additive
Amkor SWIFT [6,7]	Fan-out (wafer)	Polyimide	3–3.6	>15	2/2/10	Semi-additive
SEMCO [8]	Fan-out (panel)	PBO	3.1	>5	2/2/6	Semi-additive
Kyocera APX [3,9]	2.5D organic interposer	Epoxy	3.1	>8	6/6/15	Semi-additive
DNP [10]	2.5D glass interposer	Polyimide	3–3.6	>12	2/2/20	Semi-additive
Amkor SLIM [11]	2.5D interposer	SiO_2	4	>2	2/2/2	Damascene
Intel EMIB [1]	Si bridge	SiO_2	4	>2	2/2/2	Damascene
TSMC CoWoS [4]	2.5D Si interposer	SiO_2	4	>2	0.5/0.5	Damascene

Zaristo-700 has a much lower dielectric constant as compared to those of the "high-k" dielectrics which have a constant above that of SiO_2 (3.9 and above). The leakage current measurements will show that leakage current before and after environmental tests is not heavily affected. Usually for RDL build-up a low-k dielectric would be more effective, but if there are "high-k" dielectrics that are considered borderline in terms of their constants why not give them a shot. Taiyo Ink. is investigating ways to implement this dielectric as an advanced packaging material used for not only stability of a multi-layered structure but for improvements in electrical parameters, such as leakage current, within the RDL and the physical changes to the silicon substrate as it's a thicker dielectric.

1.6 Statement of Purpose

At the Georgia Institute of Technology (GT), in the cleanroom facilities and laboratory spaces the *tri-layer demonstration* samples are fabricated and tested. There is a checklist of tests and tools that are made use of for characterization of new dielectrics in the PRC. For the purposes of master's thesis work, material properties and electrical

properties are being examined as well as measured. Analysis of electrical parameters will provide us insight into how to improve future stack-up architectures for Taiyo Inc. First, it is more proper to understand the fundamentals of how these tri-layer samples are created. That is where the measurements of daisy-chain and capacitor pads on the tri-layer samples come in, because stacking three layers of a very thick dielectric lowers the overall capacitance. Secondly, having three metal layers complicates the via connections from M3-to-M2-to-M1 where laser drilling conditions must be optimized along with surface treatments to ensure the via reaches the landing pad below.

Despite most of the cleanrooms today housing 300-mm processes, starting at the smaller wafer sizes allows us to determine if this multi-layered idea can be scaled up for the Zaristo-700 dielectric. When it comes time to do the assembly procedure for this package, CMP (chemical mechanical planarization) and other grinding mechanisms can be utilized due to the substrate being silicon. As we will explore, the CTE and adhesion of Zaristo-700 is excellent and contributes to making a great material for the RDL wiring layers. Taiyo Ink. has stated that this version of the dielectric film accounts for issues such as stability in how long it can sit, delamination during or after curing, delamination during fabrication processes, and so on. Whereas some of the dielectric films of other companies still are having these problems. This research is working towards answering the unknowns about this dielectric and how well it will function as a future RDL build-up material through characterization and analysis of its properties (*Figures 5a and 5b)*.

CHAPTER 2. METHODOLOGIES

This chapter contains an overview of the combination of test structures selected, flow diagrams of the fabrication process, and a review of the literature that fueled this research. As stated, there was a combination of test structures chosen for the areas of measurement. Daisy chains and capacitive pads provided the avenue to understand how at each layer of the dielectric (Zaristo-700) the resistance and leakage current values were within reason.

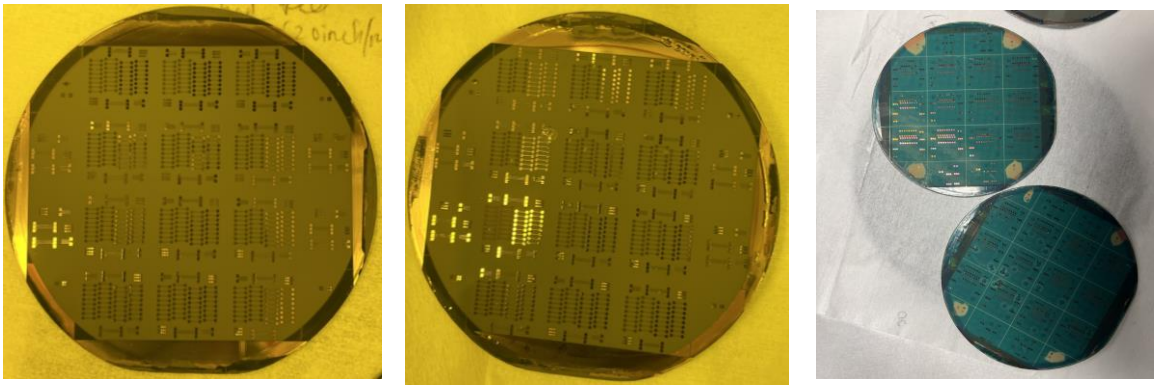


Figure 5a and 5b: (a) Zaristo-700 Tri-layer Si substrates 1 and 2 before solder resist application (SR). (b) Zaristo-700 tri-layer Si substrate with SR applied.

2.1 Packaging Substrate Properties

To expand on the make-up of these samples, it is always good to start with the substrate, what are these layers built up on and so forth. Silicon, obviously, is the most widely known and used for the semiconductor industry (Tummala's Textbook). 4-inch Si wafers are being used due to the excellent properties they exhibit, such as it being a high-temperature material. This means that it can withstand higher temperature processing within the fabrication process. As well as great dimensional stability that allows for the

complex circuitry to be wired into it, as we see today in the advanced devices being released today. One of the most important properties of the substrate is its CTE (coefficient of thermal expansion). CTE is the quantification of the change in component dimension due to temperature changes (heat) in environment of the system ($ppm/℃$). Heat dissipation and CTE mismatch are amongst the biggest issues for current high-performance 3D-IC architectures (Wafer-level, chip-level, panel-level, etc.). CTE of silicon is on par with that of the Si-Ics, so there is less room for CTE mismatch. When the CTE of the build-up material starts to not match those of the metals and substrate used, common failure modes are fatigue through propagation of cracks and warpage of the substrate itself. This can lead to interconnect failure, die-cracking, and complete failure of the substrate itself. Si wafers are fragile and can shatter or cleave on their own when exposed to repetitive amounts of stress (Lab report for 4754). "Core and build-up dielectrics are the key materials in a substrate. They determine signal speed, heat transfer, warpage, and both chip-level and board-level reliabilities." [8]

2.2 Zaristo-700 Tri-layer Fabrication

2.2.1 Lamination and Cure

Meiki Vacuum Laminator MVLP 300 is utilized to create each layer of dielectric. The conditions match those of Taiyo Inc. and are a two-step process as the PRC capabilities are in one laminator chamber. The first step is done under vacuum for 30 seconds at a temperature of 140 ºC, with an applied pressure at 0.8 MPa. A second step with only pressure of 0.8 MPa for a total of 60.0 seconds at 140 ºC is done. Curing of Zaristo-700 is

required in an inert atmosphere of nitrogen, so an N_2 oven is used for 1 hour at a constant temperature of 200 ºC.

2.2.2 Seed Layer Deposition

Before the deposition of the seed layer there is a necessary pre-treatment of the wafer-to-dielectric surface. Plasma clean steps are vital to ensure the surface in which the titanium and copper layers are deposited on are contaminate free. Meaning there should be no particles or any other physical defects on the dielectric. The selected tool is an Oxford RIE system, that is constantly optimized with a 4.0-minute Argon plasma recipe. It applies a power of 153 W, pressure of 0.036 Torr, and with a flow rate of 50 sccm.

Denton Discovery RF/DC Sputterer was the tool of choice for the Ti/Cu seed layer of this tri-layer demonstration. The standard protocol for seed layer composition in a tri-layer dielectric stack consists of a ~0.2 angstrom titanium and copper metal layers. For a higher quality metal layer, the longer Denton is allowed to pump down, as close as possible to 6.0E-6 Torr. The deposition takes place in an Ar_2 enriched environment without breaking vacuum. The Denton tool is more automated than that of its Unifilm counterpart and only the current supplied to the sources can be changed within reason. On the software interface, there are optimized recipes and steps for each part of the deposition process such as loading, unloading, and running the TiCu seed layer recipe.

The second seed layer sputtering tool, otherwise known as the Unifilm Multisource Sputtering System, can be used to sputter the TiCu films on the Si substrate. It has a deposition monitor to measure source distributions quickly and accurately, a computer-controlled planetary system to ensure proper substrate holder spinning during sputtering

steps. With this tool it has the capability for controlling the metal film deposition rate, and it ranges between 1000 angstrom and 500 angstrom or however the tool owners deem fit.

2.2.3 Hitachi RY-5115 Photoresist

The PR of choice is the Hitachi RY-5115 dry film resist, that is applied through lamination. Resist thickness is 15.0 µm and using the Meiki Vacuum Laminator at vacuum of 30 seconds, pressure of 0.3 MPa for 60 seconds.

A direct-write laser tool known as the Heidelberg MLA150 creates features of interest, daisy-chains and vias. The optimized dosage for this project has been determined for a 375 nm laser at 180 mJ/cm^2 with a defocus of +1. Defocus

Development is done on a conveyor system, where the developer bath is monitored, and the conditions of it change daily. Once it needs to be changed, all the parameters used for prior samples will need to be re-optimized.

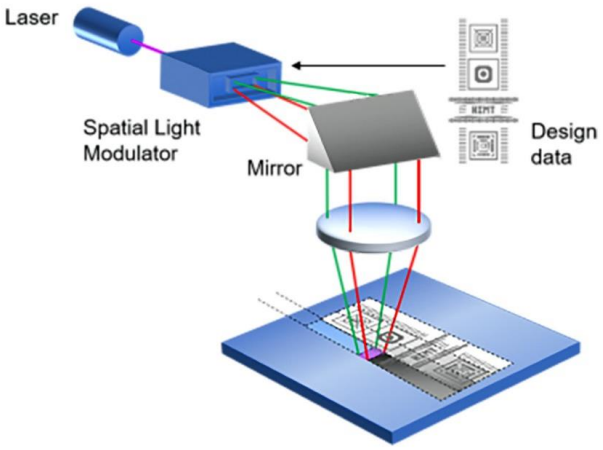


Figure 6: Heidelberg MLA150 Direct Writing Maskless Laser Lithography process

2.2.4 Cu Electroplating

Oxford RIE platform is once again used to clean the surface of the samples before electroplating is to be done. If there is any debris or unwanted specimen on the wafer surface, the metal layer being created into the features will not deposit evenly. The O_2 clean process setting are 3.0-minutes, flow rate is 50.0 sccm, 253-254 W, and pressure of 0.102 Torr.

For this demonstration a 5.0-7.0 μm thick copper layer was needed, each time the thickness is slightly different. Before plating begins on the samples, we run a dummy sample to get an estimation on the plating rate of the tank for that day and time. To replicate the copper foil is taken through the exact same steps as a sample is, to try to replicate the actual plating process. First, an acid wash dip in H_2SO_4, is necessary to clean off any oxidation or debris from the surface. All three acid washes had the wafers dipped, in the plating frames, for ~1.0 minutes. The longer a dummy sample is run for, and the more samples run on the system strengthens the plating solutions, which ensures a higher quality copper plated. Using a thickness gauge, by pressing down on the non-shiny side of the foil, the amount of copper before is measured to calculate the amount that is plated afterwards. To calculate this value, the difference between after and before is taken, and there is the approximate plating rate for however long the dummy is run. In this case, the dummies are run for 60 minutes (1 hr.), so the values below will be multiplied by 60 minutes and then divided by 60 to get how long the samples should be plated for. This value ends up being

25 minutes or 1500 seconds, as the plating tank screen counts up in seconds. For the three dummy runs of each metal layer, approximately the same conditions were met: 13.5 μm, 15.4 μm, and 13.9 μm's of copper plated after 1.0 hour.

After the dummy samples are completed, the two wafers are then plated. The conditions for plating are as follows: current on the front and back rectifiers were 6.1 and 5.8 amps. Before plating the second wafer, the copper thickness is checked on the Keyence Optical Microscope at 150x and measuring across a feature of known line-space (L/S) or pitch. Chapter 5 will discuss the issues that occurred during fabrication and how those ended up affecting the final test vehicles.

2.2.5 PR Stripping and Cu Seed Layer Etch

IC-2 is the PR stripping chemical and is done by submerging the wafers into enough stripping solution for 2-3 samples or however many there are. This process should take no more than 60 seconds, as for this project it took between 35-50 seconds. Done at 60 ºC on a hot plate.

Copper Etch solution 49-1 is a quick process as well and researchers can tell if the copper is etched away when a poof of black fog shows in the solution. This was done on a hot plate at 50 ºC where the wafers are submerged entirely into the etcher solution in a glass dish.

2.2.6 Removal of Ti Seed Layer

Oxford system is once again utilized for etching the Ti layer before Novabond. The recipe is pre-determined for this fabrication process and is a CHF_3/Ar oxide treatment

where three different gases are utilized. CHF_3 has a flow rate of 30 sccm, Ar is 20 sccm, and O_2 is 5.0 sccm. An overall pressure of 0.027 Torr, power of 203 W, with a process time of 12.0 seconds to ensure the Ti seed layer is completely removed. This is a crucial step before Novabond or else the RDL is compromised.

2.2.7 Surface Adhesion Treatment

A surface pre-treatment for bonding a new layer of dielectric to the previous metal layer. Or else the film would delaminate immediately from the copper. This solution-based adhesion promoter for dielectric-to-copper is done by submerging the samples in the beakers, and each step of the Novabond process is timed. It's crucial to ensure the wafer will not fall into the beakers, so dark green alligator clips with locking handles are used. *Table 2* displays the correct order for dipping samples and the timing for each step of the surface adhesion treatment.

Table 2: Novabond Treatment order and solution conditions

Process	Temperature (°C)	Time (s)
Softclean UC	30	30
DI Rinse	-	120
Conditioner	50	60
Coating Solution	70	360 (6.0 min)
DI Rinse	-	120
Reducer	35	60
DI Rinse	-	120
Protector	35	60

DI Rinse	-
Dry	
Sample	-

Soft-Clean UC is a blue solution that cleans the surface of the RDL, to ensure there is nothing on it which includes any oxides. Poured into a 5000 mL beaker and heated to a temperature of 30 ºC. Conditioner solution clears the surface uniformly which readies it to accept the coating solution. A 5000 mL beaker is placed on a hot plate and heated to a uniform temperature of 50 ºC. Coating solution is what clears the crystalline surface and a new nanocrystalline surface (newly ordered) is formed. A 5000 mL beaker is placed on a hot plate and heated to 70 ºC. Reducer is a sodium hydroxide solution that does exactly as its name states, it reduces the copper in the RDL as it turns darker in color (almost black). If the copper starts to bubble, that means the treatment has worked to create an adhesion promoter layer on the RDL surface. This solution is heated to 35 ºC and must be constantly agitated using a stir bar on medium speed. Protector solution protects against the re-oxidation of the surface and from chemical attacks that would further reduce the copper before lamination of the next dielectric layer. It is recommended to leave the sample for longer than the 60 seconds in the table above, as we used 2.0 minutes or 120 seconds to ensure the reduced copper surface would not further oxidize in between the time of the Novabond treatment and lamination of next dielectric layer.

2.2.8 Femtosecond Laser Via Drilling

Laser drilling for vias connecting each metal layer was completed using the OPTEC Femtosecond Micromachining System laser. The laser in use is not meant for drilling through dielectrics and other thicker films. To achieve the best results, the conditions are optimized each time we went to drill M2-to-M1 and M3-to-M2 layers. The laser engineer, Henry Su, and former PRC student Chris Blancher were the ones to do the drilling for this demonstration. They perfectly curated the conditions for my dielectric each time and spent a great deal of time working with me. In *Table 3*, the optimized laser conditions for M2-to-M1 and M3-to-M2 are listed. The layout for the twelve coupons on each wafer is such that the left-half of the daisy chains has only M2-to-M1 vias, and the right-half contains M3-to-M2 vias. We optimized two via sizes: 23 µm diameter vias on landing pads of 35 µm and 30 µm diameter vias with landing pads of 50 µm.

Table 3: Optimized Femtosecond Laser Via Drilling Conditions for each metal layer.

Wafer #	Via Diameter (µm)	Metal Layer	Speed (mm/s)	Jump Speed	Laser Power (W)	Burst Time	Repetitions	Laser On Delay	Laser Off Delay
1	30	**M2-to-M1**	35	50	35	1000	1	50	150
1	23	**M2-to-M1**	35	50	45	1000	2	50	150
1	30	**M3-to-M2**	35	50	18	1000	2	50	150
1	23	**M3-to-M2**	30	50	23	1000	2	50	150
2	30	**M2-to-M1**	35	50	35	1000	2	50	150

2	23	**M2-to-M1**	35	50	45	1000	2	50	150
2	30	**M3-to-M2**	35	50	18	1000	2	50	150
2	23	**M3-to-M2**	20	50	18	1000	2	50	150

2.2.9 Electrical Test Measurement Process (E-test)

Electrical measurements showcase whether a package is working. After all the research and optimization of the fabrication processes, these values help to build a case for a new kind of technology. The electrical measurements were done using a Signatone Probe Station inside of a controlled atmosphere glove box with an exterior liquid nitrogen tank. Two small metal probes contact the aluminum pads to obtain the capacitance, frequency sweeps, and IV curves (*Figures 8-12)* for the ITO samples discussed below (*Figure 7*).

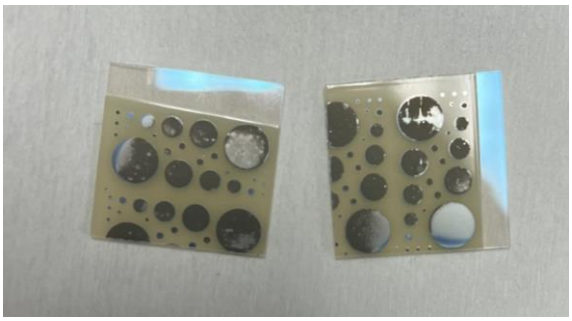


Figure 7: ITO Glass slide samples after Leakage Current and HAST measurements.

The new materials checklist for PRC outlines the kind of sample for checking leakage current measurements before and after environmental testing. Meaning before and

after HAST measurements or Highly Accelerated Stress Testing. The HAST tool is utilized for predicting how a material can survive in extreme conditions, otherwise known as an environment in which the material could be exposed to in an application. Another JEDEC standard for package reliability testing. Reliability is known as the probability of a system or device to perform a function as designed for a specific amount of time. The test is performed in a pressurized chamber at 85% relative humidity (RH) and 130 ºC for 100 hours. After HAST results are to be discussed in Chapter 5 of this work.

Sample creation for this testing were ITO (Indium-tin-oxide) glass slides with a layer of dielectric laminated on the side of the ITO. A multimeter is used to check which side the ITO is on by measuring a resistivity of ~20 Ω. After dielectric lamination an electron-beam evaporator was used to deposit the aluminum film. The Georgia Tech Denton Explorer is a six-pocket evaporator system used to coat samples with a variety of metals and dielectrics. A high-intensity beam of electrons is focused on the center of a crucible containing, in this case Al (aluminum), the material to be evaporated. Inside the processing chamber, the glass slides sit on a sample holder that locks/sits into two pegs, one in front of the holder and behind it. You can load multiple samples on the rotating sample holder, but the evaporation takes place from bottom up, as the crucible slot is below the sample on the bottom of the chamber. A mask with varying diameter circles is taped to the samples so that Al pads are deposited across the glass slides. From the advisement of the tool trainer, an Al film of 5.0 kilo-angstroms (500 nm or 5000 angstroms) at a deposition rate of 2.0 angstroms/second. This rate was selected to ensure a uniform and high-quality aluminum film was deposited.

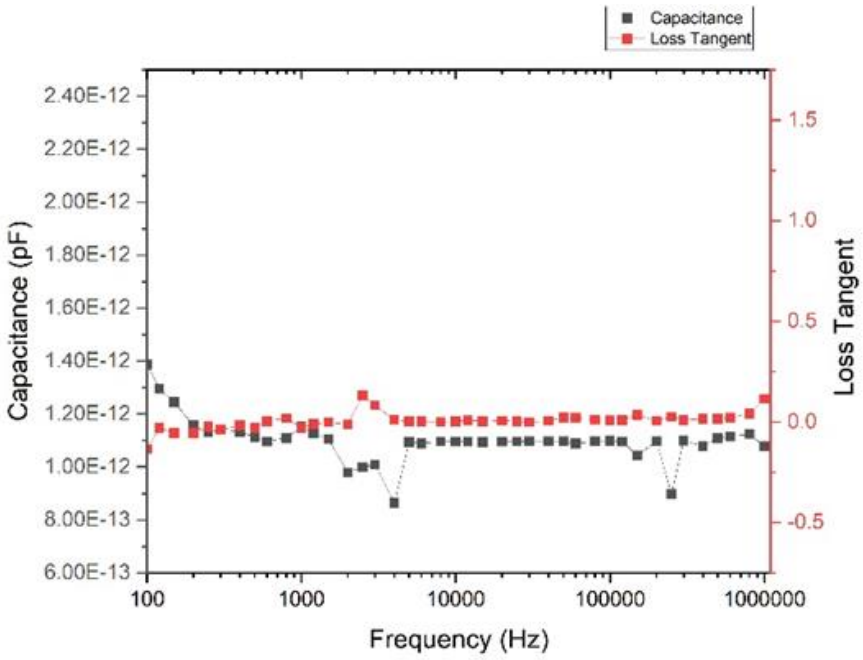


Figure 8: Frequency sweep of second smallest Al electrode pad before HAST.

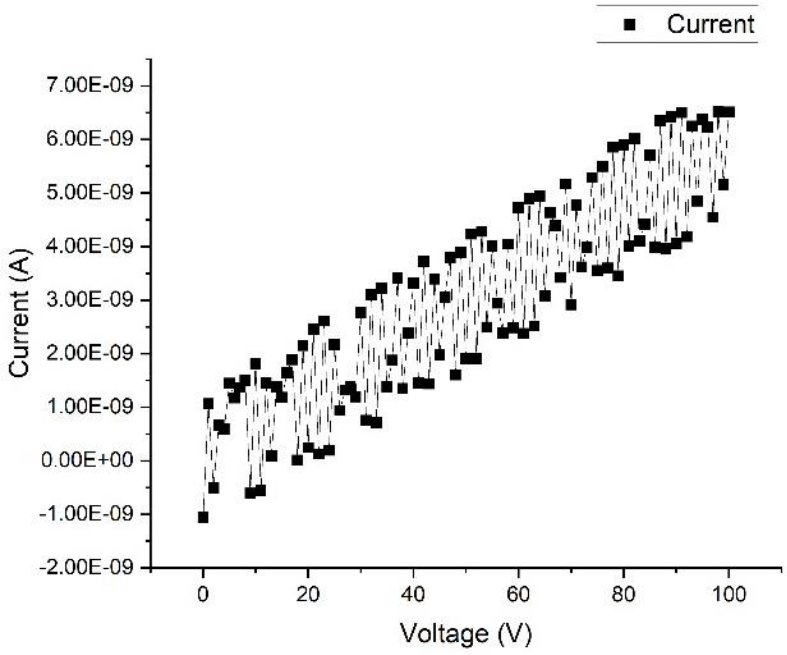


Figure 9: IV curve of the smallest Al electrode pad size with a voltage sweep from 0 to 100 V before HAST.

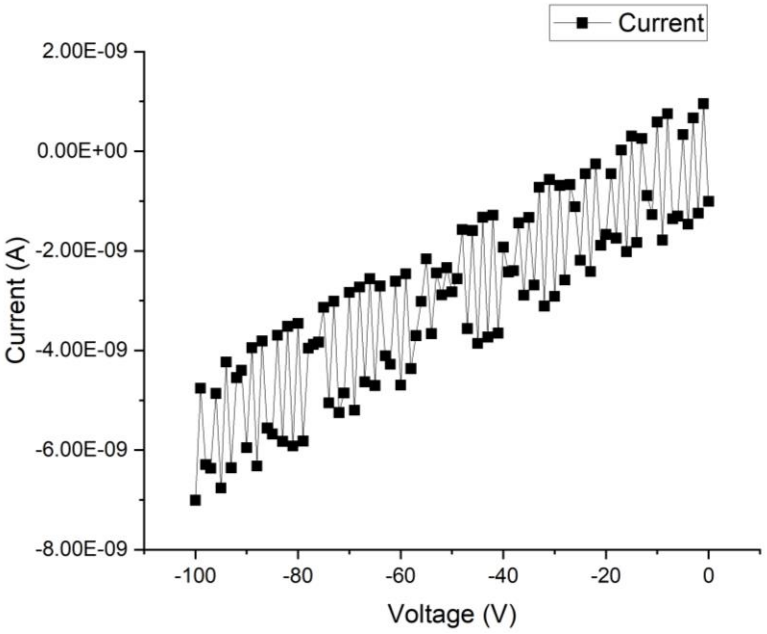


Figure 10: IV curve of smallest Al electrode pad size with a voltage sweep from 0 to (-100 V) before HAST.

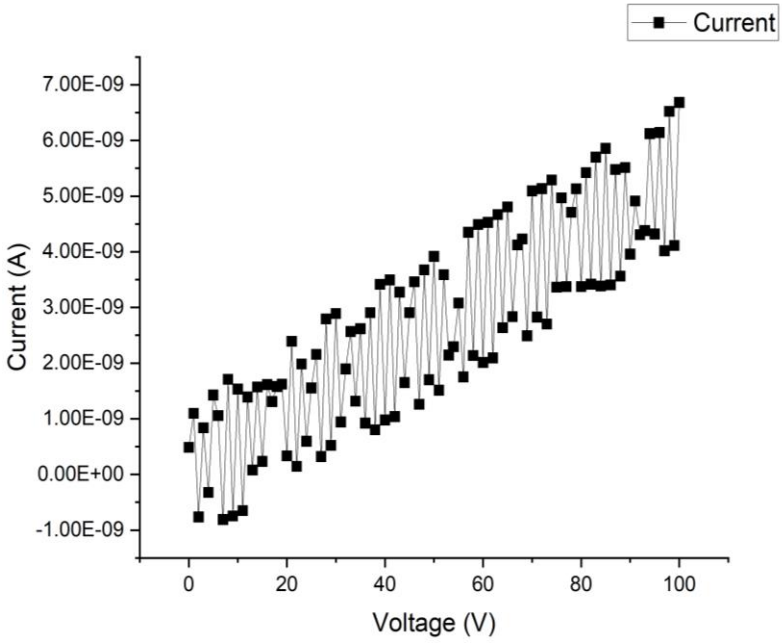


Figure 11: IV curve of second smallest Al electrode pad size with a voltage sweep from 0 to 100 V before HAST.

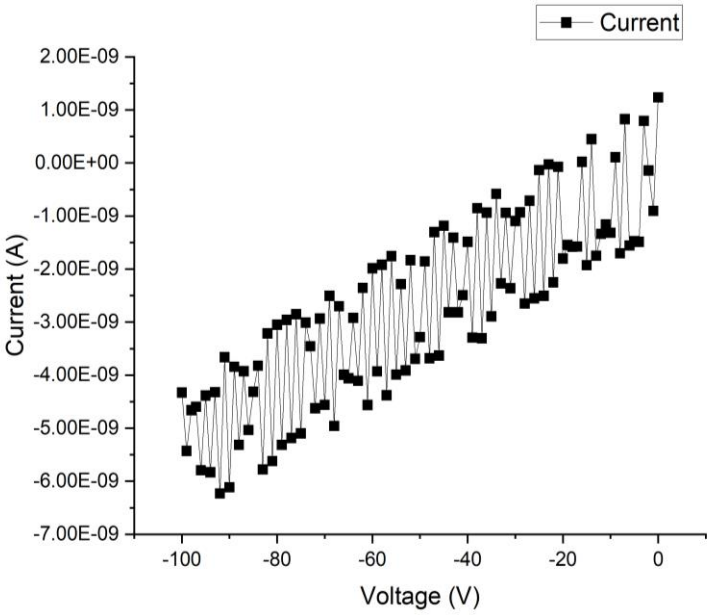


Figure 12: IV curve of second smallest Al electrode pad size with a voltage sweep from 0-to (-100 V) before HAST.

After further analysis, the capacitance and loss tangent of the Zaristo-700 dielectric show little to no change as seen above in *Figure 8* during frequency sweep mode. The IV characteristics are well within their limits and behave as planned for a dielectric of this thickness. With a positive and negative voltage sweep from 0 to 100 V and 0 to -100 V, no breakdown is shown by the material. The data above is trending in the correct directions for the specific voltage sweeps as it stays at 2.0 nA before HAST (*Figures 9-12)*, and in *Section 4* it is observed the leakage current stays at 2.0 nA after HAST.

CHAPTER 3. SYSTEM FABRICATION

It has been made clear, in the last chapter, the importance of the RDL build-up process and the fabrication steps that are needed to create the metal wiring layers on the Si substrates. System fabrication is about tying each layer of dielectric to the next, and ensuring they are properly functionalized. Therefore, we can figure out what ways are there to bring each unit together to form each layer in the same manner. Process optimization is a shared practice between academia and industry as both rely on it to create functional product lines and demonstrations such as the Zaristo-700 tri-layer.

Before the fabrication process, measurement methodologies, and data analysis comes the schematics and AutoCAD designs that are necessary in making the project become tangible. From the bottom up, in AutoCAD, each metal layer is laid out and all the dimensionality for the Heidelberg to do its job is planned. *Figures 11-13* are images of the AutoCAD layers with the first metal layer (M1) in green, second metal layer (M2) in purple, and the third metal layer (M3) in red.

Figure 14 is of the solder resist (SR) mask design, and how it is only on top of the pads that are to be utilized for testing. Chapter 4 and 5 explain the issues with the connectivity of the metal layers and why sometimes electrical measurements are unobtainable. There can be a multitude of problems as to why the final stack-up is not fully functional.

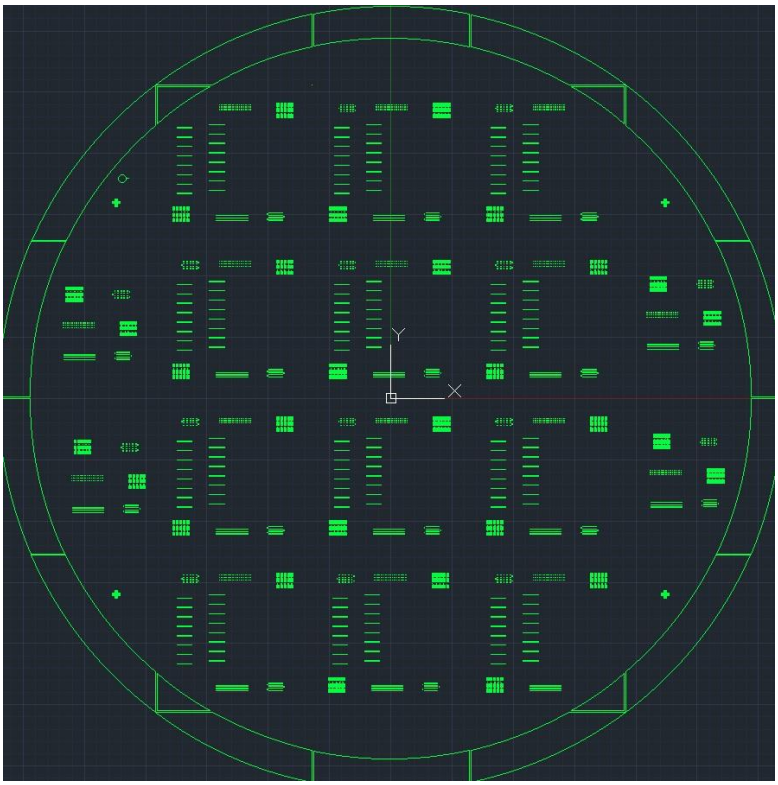


Figure 13: AutoCAD schematic of M1 (in green) in the Tri-layer stack-up.

Figure 14: AutoCAD schematic of M2 (in purple) on top of M1 wiring layer in the Tri-layer stack-up.

Figure 15: AutoCAD schematic of M3 (in red) on top of M2 and M1 wiring layers in the Tri-layer stack-up.

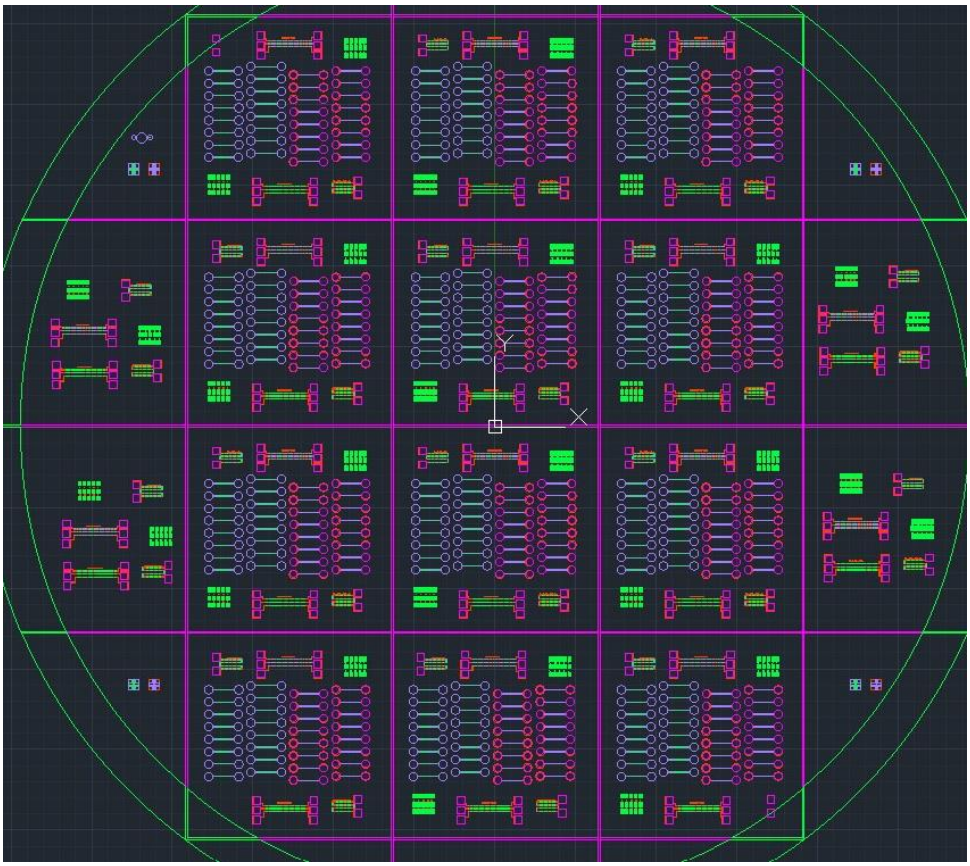


Figure 16: AutoCAD schematic of the Solder Resist (SR) Mask with dicing lanes.

3.1 Optimization of Units

Analysis of the Zaristo-700 dielectric was necessary to see how it behaves as a RDL build-up layer. In this section, we will discuss the JEDEC process of peel testing, dose testing, and the optimization of the laser via drilling as included in Chapter 2. Three different kinds of samples were fabricated for each test, where for peel testing two wafers were needed and two wafers were used for dose testing. Multiple samples were created to statistically demonstrate the data is sound and can be repeated.

3.1.1 Metal and Dielectric Property Analysis

Shown in the second chapter of this thesis, the peel test process is used for demonstrating the adhesion properties of the Zaristo-700 dielectric. Two blanket adhesion samples were fabricated which include four layers of material, as depicted in *Figure 15*. Si substrate is 4.0 inches, next is the 30 µm Zaristo-700, a 300 nm TiCu seed layer, and ~20-30 µm of electroplated copper. Blanket means these samples were unpatterned, because the samples had the sole purpose of testing adhesion strength between the copper and dielectric.

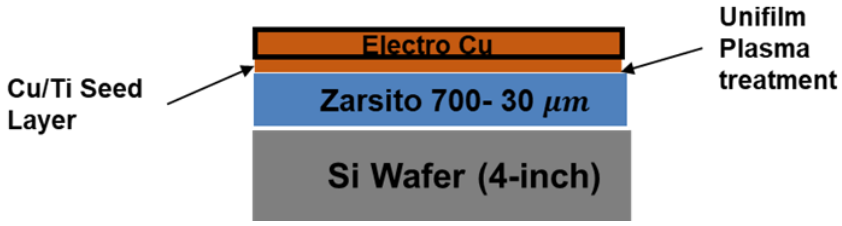


Figure 17: Peel Test Sample Schematic.

As a vital part of process optimization for characterization of new dielectric materials to the PRC, adhesion tests provide information on if during fabrication is the sample at risk for delamination. This failure mechanism known as delamination is when a film starts or completely peels away from the material layer below it. Particularly in the RDL area of the package, structural integrity is necessary for it to function as intended. Remember, we discussed the main roles of the package where protection has been the number one responsibility for decades.

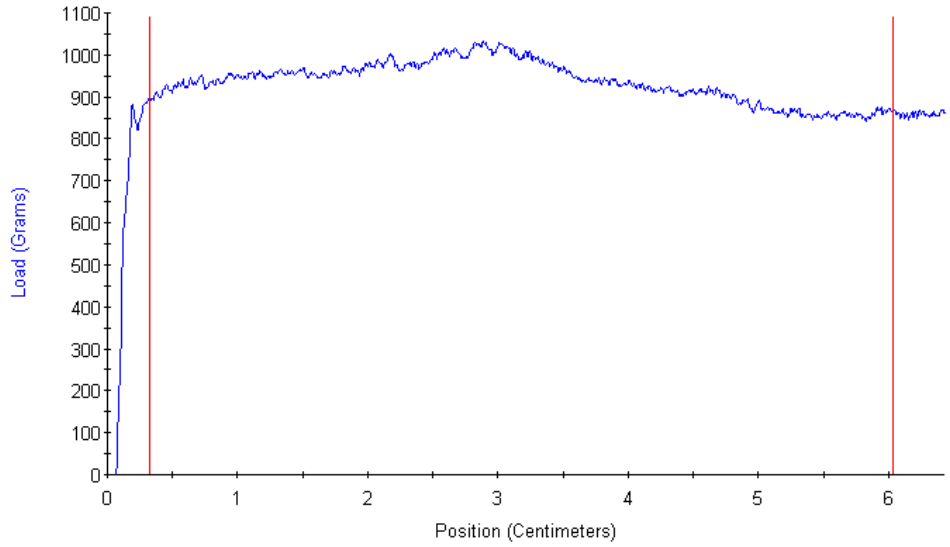


Figure 18: First peel test measured on test wafer #1.

To prove the Zaristo-700 dielectric can be utilized as an RDL stack-up material in the future for advanced packaging technologies, the JEDEC standard test of peel testing is used. Initiating the peel is done using a razor blade to get a strip of copper prepared for the peel testing to grab onto. A promising sign was the difficulty in starting a peel with the razor blade, as this already demonstrates a high adhesion strength for the Zaristo-700. Two

peel test samples of blanket copper on dielectric were measured at a 90° incline at a peel rate of 12 inches/minute. Average peel/adhesion strengths for both samples were measured at 930 and 1,074 grams respectively. Two peels were successful on wafer 1 and only one peel was measured fully on wafer 2 (*Figures 16-18).* Therefore, this validates our claim that the Zaristo-700 has high adhesion values as compared to current RDL materials such as ABF with a reported peel strength of roughly ~700 grams.

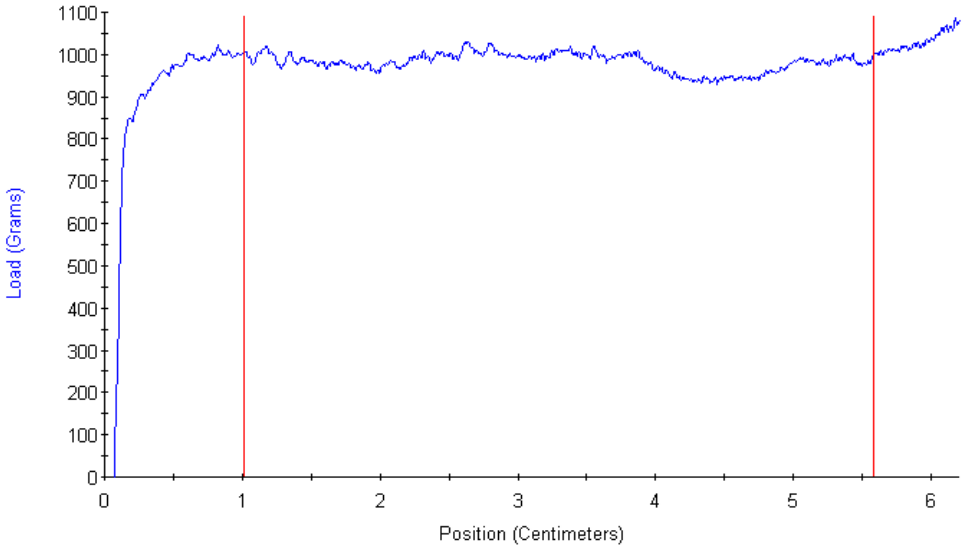


Figure 19: Second Peel test measured on test wafer #1.

Some comments on the difficulty in initiating a peel could be due to dielectric roughness before plasma treatments being around ~70 nm and after ~100 nm. Dielectric roughness can be a cause for concern with demonstrating and resolving features at small pitches. There will be more on this in the future works section of Chapter 6.

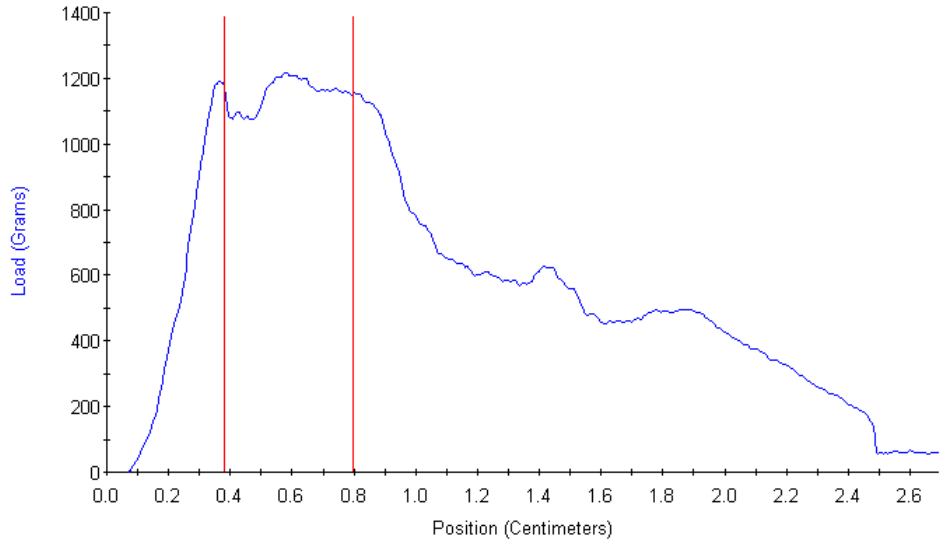


Figure 20: Third peel test measured on test wafer #2.

3.1.2 Lithography Optimization: Dose Testing

Before any true fabrication can begin, dose testing samples are created with blanket TiCu seed layer and a 15 µm thick Hitachi RY-5115 photoresist on top (*Figure 19)*. The purpose of this process is to obtain a range of stable dosages in which line-spaces (L/S) can be fully developed to create features of interest on the dielectric.

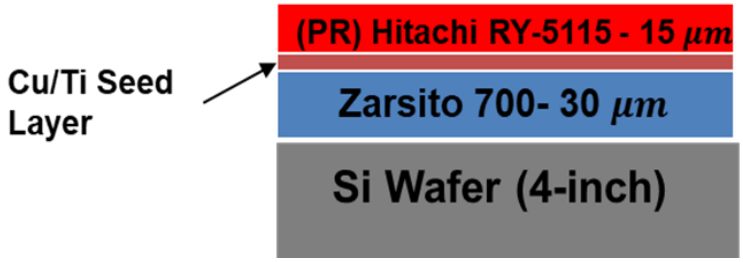


Figure 21: Schematic of Dose Test Samples.

Included in the test samples are 50, 25, 20, 15, 10, 8.0, and 5.0 µm L/S features for demonstration purposes. The first range of doses tested on the dielectric are from 50-190 mJ/cm^2 and had a critical dimension of 5.0 µm. Critical dimension (CD) is defined as the minimum feature size that can be reliably printed on a substrate. It is measured as the width of the smallest feature or pattern that can be created. *Figures 20*-24 show images of 8.0 µm being resolvable by doses of 100, 110, and 140 mJ/cm^2. As stated, the roughness of the Zaristo-700 material is quite high pre-processing at 70 nm, and post-processing (after plasma treatments) at around ~100 nm or 1.4 µm.

The purpose of a second dose test is to center the dose range for the three-layer stacks. Meaning, what is the best dose for this dielectric as successive layers are fabricated. The optimized dose result is 180 mJ/cm^2 and produces 8.0 µm L/S features as shown in *Figure 25*. MLA dose testing is deemed as necessary when applying photoresist to a new material. Being able to resolve 8.0 µm L/S on a thicker dielectric, 30 µm, may seem insignificant, but as discussed in the introductory sections “higher-κ” dielectrics tend to have poorer resolution as compared to low-κ. The Zaristo-700 is on the higher side of what the advanced packaging sector has set as the “low-κ” range for dielectric materials.

After confirmation and some discussion, the roughness values obtained matched those of Taiyo, Ink. High roughness values affect the CD of the features printable on the wafer. Multiple issues arise when the roughness of a dielectric is high such that line width variation, depth of focus variation, and inconsistent electrical performance can occur on within the package. First, line width variation is when the surface roughness of a dielectric leads to fluctuations in the width of lines or patterns. Lithography and advanced packaging have proven the importance of controlling the dielectric roughness to ensure consistent electrical performance in the lines created. Next, the depth of focus (DOF) is the range of distances over which the MLA 150 systems can maintain the specified CD which is 5.0 µm. Furthermore, with rough features on the dielectric it can appear to the lens system the some of those areas are closer or farther away from the lens. Unfortunately, 5.0 µm L/S features were unresolvable on the Zaristo-700. As they were underdeveloped and the lines collapsed in on each other, this issue was confirmed immediately after PR development on the Keyence Optical Profilometer.

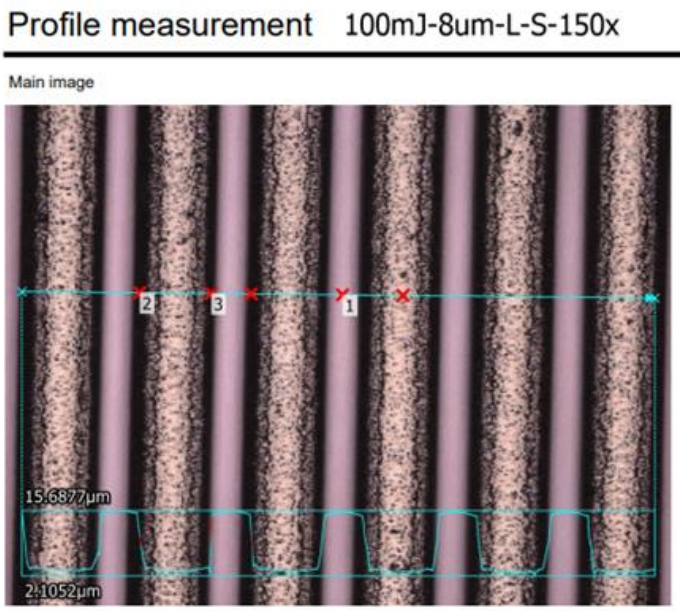


Figure 22: MLA 150 Dose 100 mJ/cm^2 resolved 8.0 um L/S features.

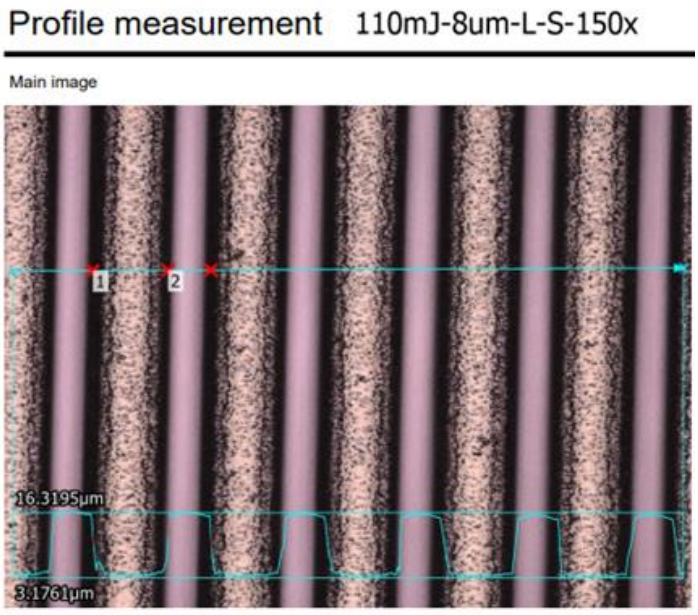


Figure 23: MLA 150 Dose 110 mJ/cm^2 resolved 8.0 µm L/S features.

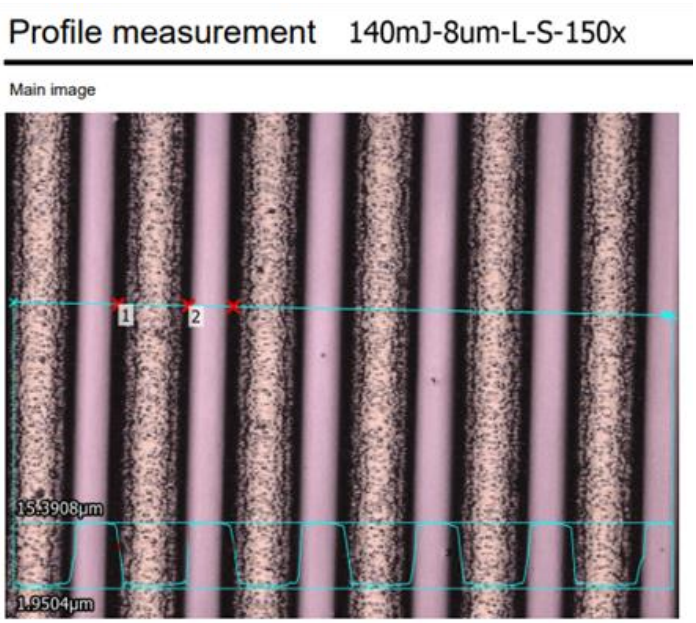


Figure 24: MLA 150 Dose 140 mJ/cm resolved 8.0 um L/S features.

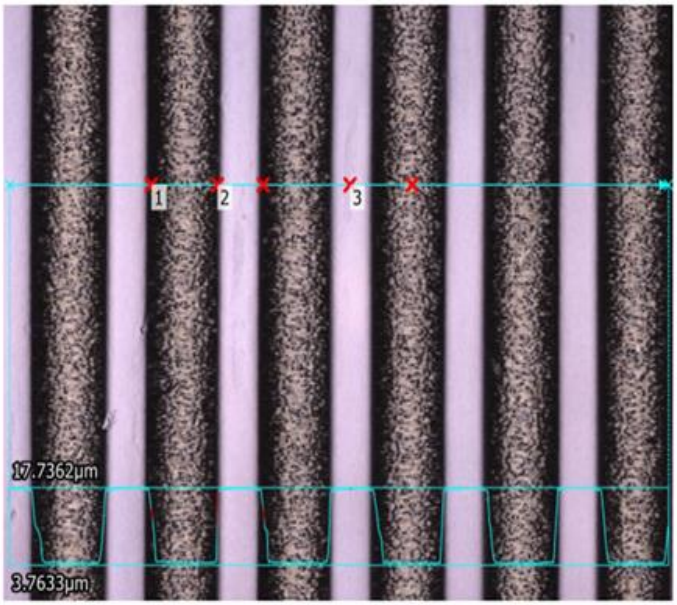
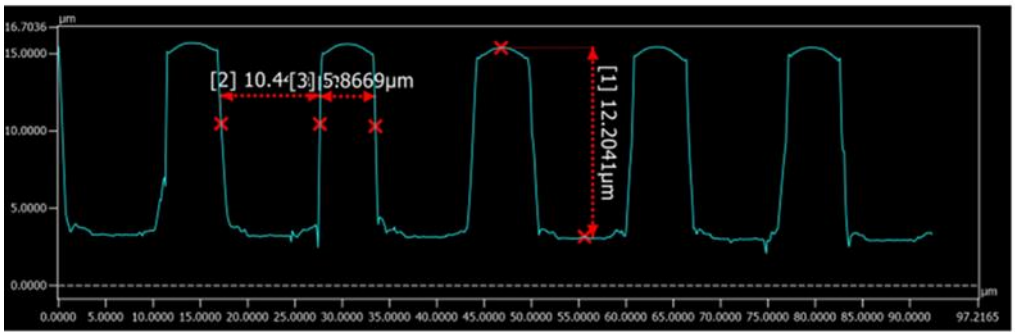
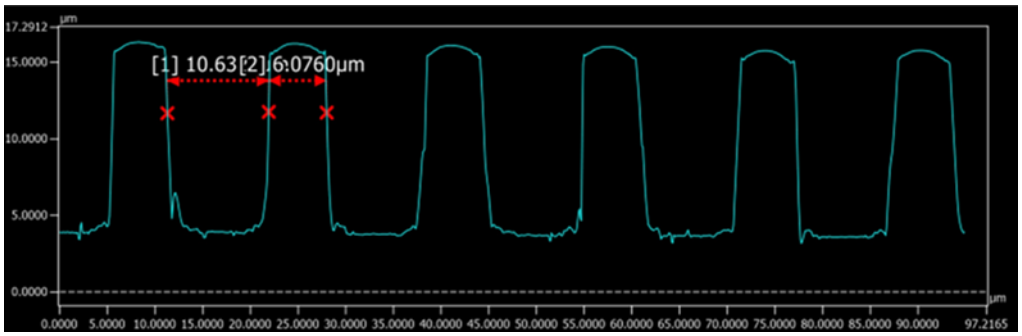


Figure 25: MLA Dose Test #2, 180 mJ/cm optimized dose for 8.0 um L/S features.





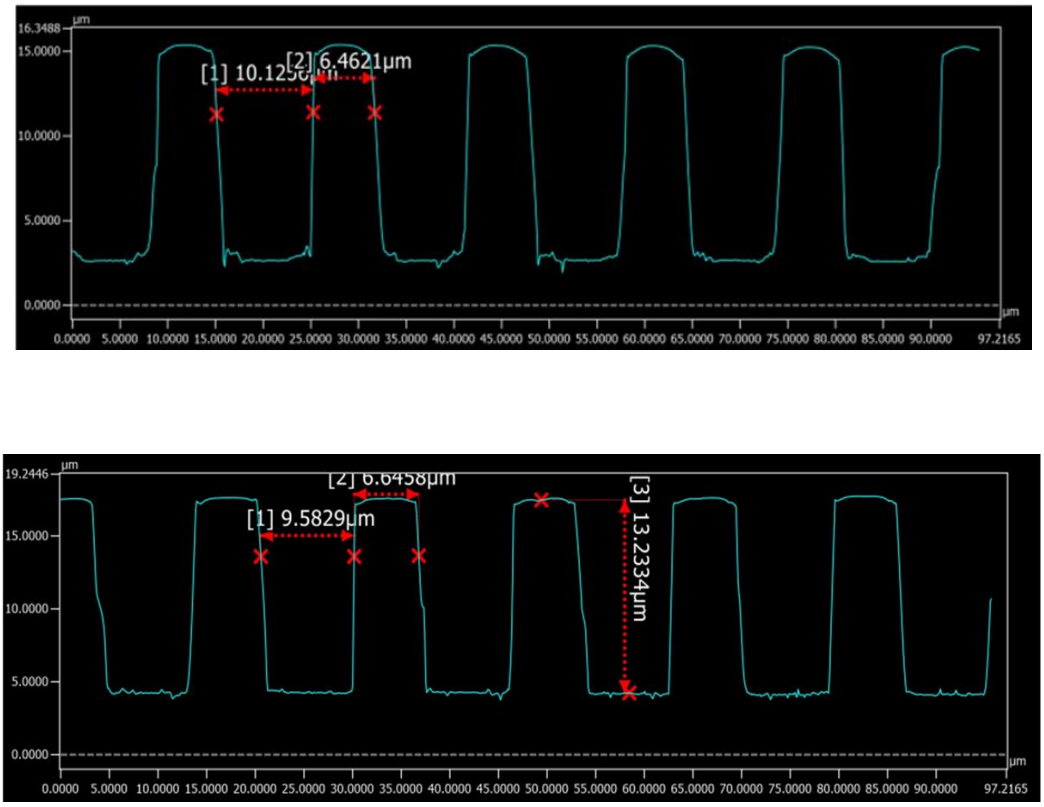


Figure 26: Line Profiles from Keyence Optical Profilometer of doses optimized for 8.0 um L/S. (a) 100 mJ/cm^2. (b) 110 mJ/cm^2. (c) 140 mJ/cm. (d) 180 mJ/cm^2.

3.1.3 Femtosecond Laser Optimization for Via Drilling

Stacked and tapered vias were designed to bridge M3-to-M2 and M2-to-M1. Using a femtosecond laser, vias of two sizes were demonstrated as stated in Chapter 2, *section 2.2.8* of 23 and 30 µm. To ensure that the femtosecond laser drilled through the dielectrics at the proper depths, the Keyence Optical Profilometer laser function is utilized to take images of the vias (*Figures 26a and 26b). Figure 27 and b* shows a test via of 40 µm in diameter with some particulate build-up due to the laser ablation. In *Figure 26b*, the same via is shown after an Ar plasma treatment, by the Oxford RIE system. This clean step is done as a pre-treatment before TiCu seed layer to ensure a more pristine dielectric surface.

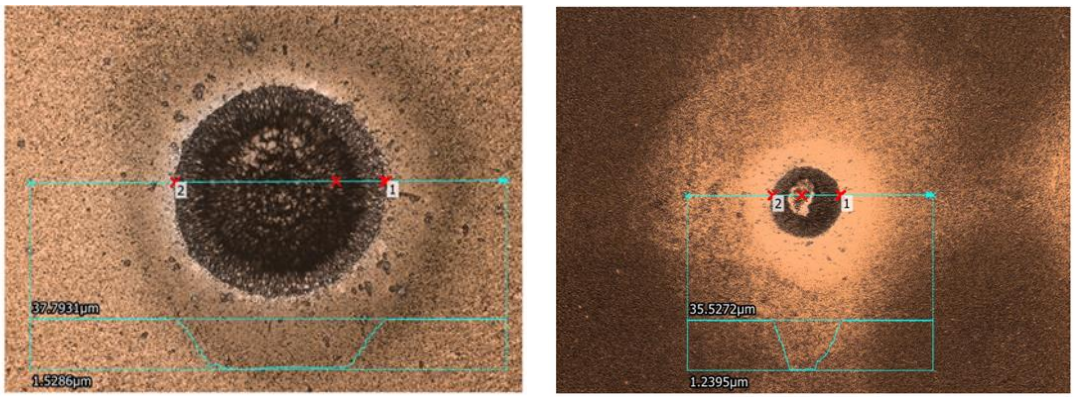


Figure 27a and 27b: (a) Debris at bottom of 40 um via after laser ablation and before Ar plasma treatment. (b) Removal of debris at bottom of 40 um via after laser ablation and after Ar plasma treatment.

CHAPTER 4. ANALYSIS OF ELECTRICAL AND SAMPLE WARPAGE MEASUREMENTS

4.1 Leakage Current after HAST

Section 2.2.9 was a discussion of the leakage current and IV characteristics of the Zaristo-700 dielectric before HAST testing. Here, we will discuss the data and characteristics of the material after it was purposefully exposed to extreme changes in environmental conditions. As stated, the Signatone Probing station inside of a controlled environment glove box was used to obtain these results.

For a reminder, there were six different aluminum pad sizes measured for their capacitances. Whereas in the case of frequency sweeps and IV curves, only between two to three pad sizes were sampled. In obtaining the capacitance and loss tangent of dielectric, 48 frequency points were swept over a range between 20.0 Hz to 1.0 MHz. As seen in Chapter 2, the curves for before HAST showed little to no change in the parameters during frequency and subsequent voltage sweeps. In *Figures 30-32b,* the current following HAST treatment held at values of ~2.0 nA which is still very low. This statement holds true for after HAST testing as well and further demonstrates the potential of Zaristo-700 as a RDL dielectric material.

In *Table 4*, the six Al electrode pads for the ITO samples are listed in increasing order of pad size. The trend of capacitance with pad area a direct relationship, whereas pad area increases so does capacitance. The reason we can clearly identify this trend is due to the mask used during electron beam evaporation, as it includes a variety of pad sizes.

Table 4: Six Aluminum pad sizes listed by increasing size to demonstrate the trend with capacitance.

Al Pad Size	Capacitance (pF)
Smallest Electrode	0.596
Second from smallest	1.14
Third from smallest	3.27
Fourth from smallest	6.74
Fifth from smallest	11.76
Largest Electrode	29.6

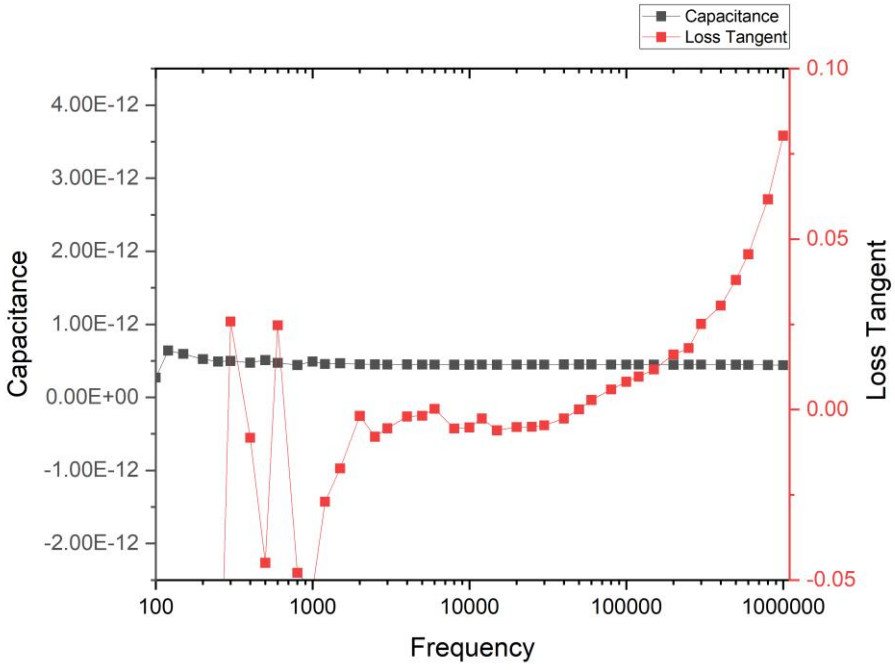


*Figure 28a: (a) S1 Frequency sweep of smallest Al pad size for ITO samples **after** HAST.*

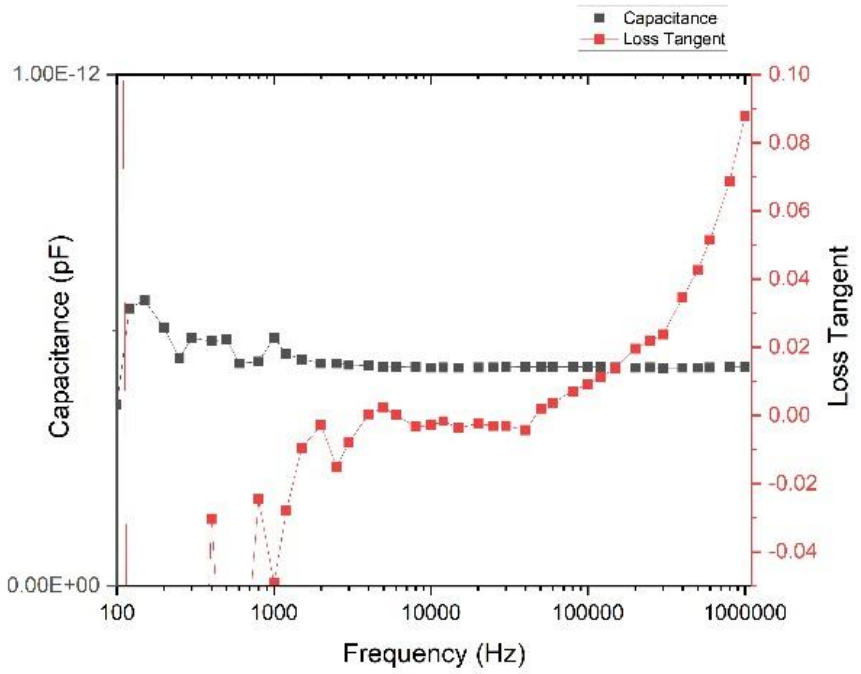


*Figure 28b: (b) S2 Frequency sweep of smallest Al pad size for ITO samples **after** HAST.*

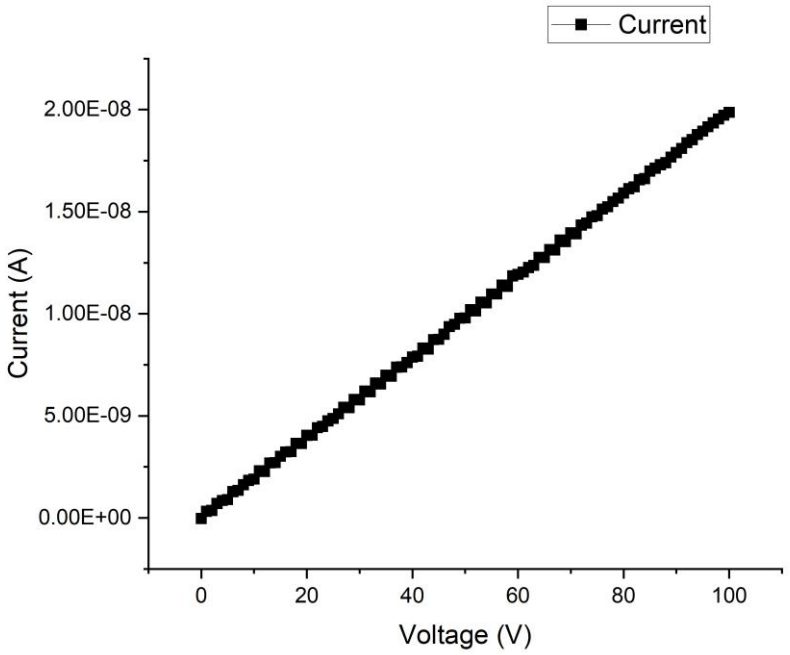


*Figure 29: S1 IV curve of the smallest Al electrode pad size with a voltage sweep from 0 to 100 V **after** HAST.*

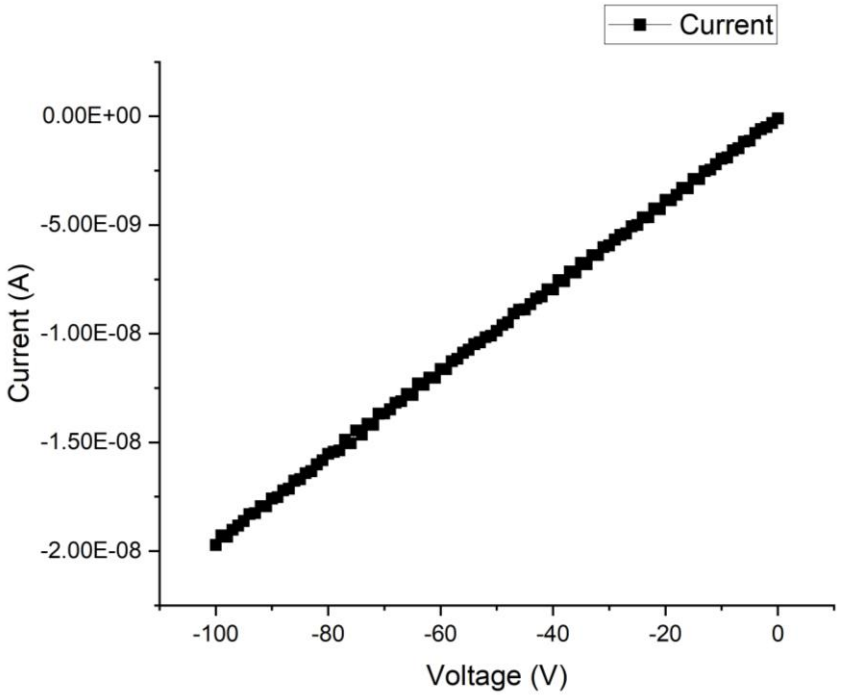


Figure 30: S1 IV curve for the smallest Al electrode pad size with a voltage sweep from 0 to (-100 V) after HAST.

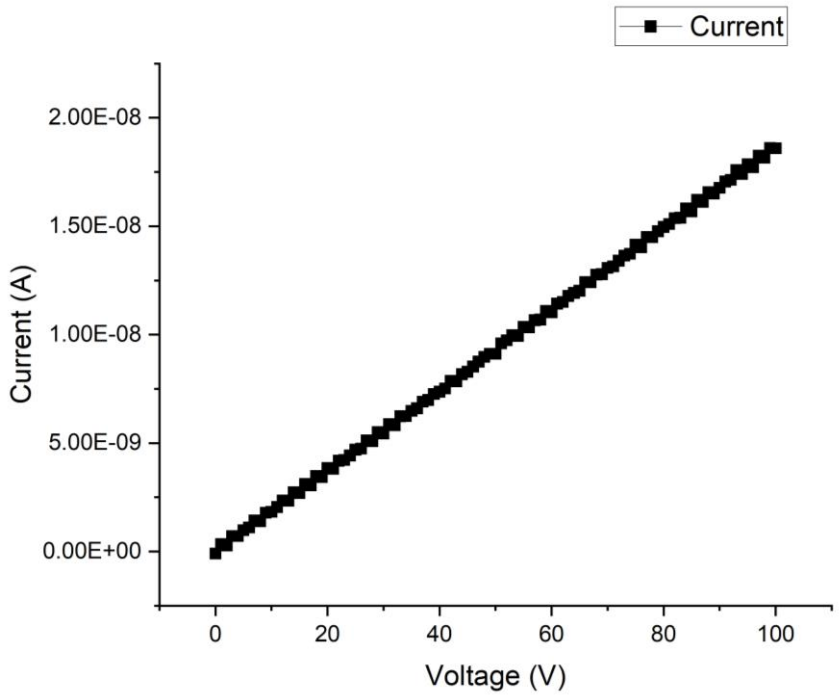


Figure 31a: S1 IV curve for the second smallest Al electrode pad size with a voltage sweep from 0 to 100 V after HAST.

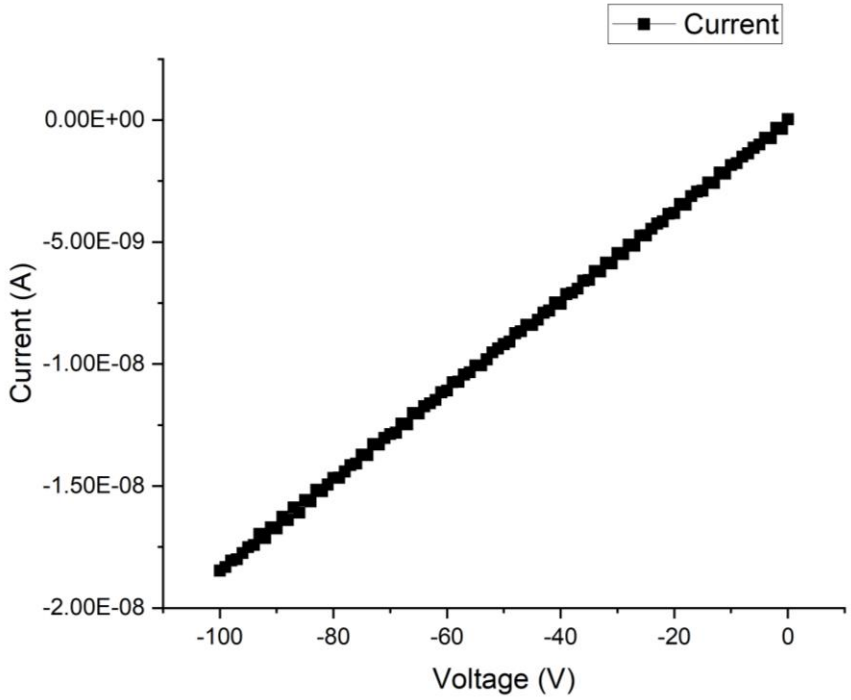


*Figure 31b: S1 IV curve for second smallest Al electrode pad size with a voltage sweep from 0 to (-100 V) **after** HAST.*

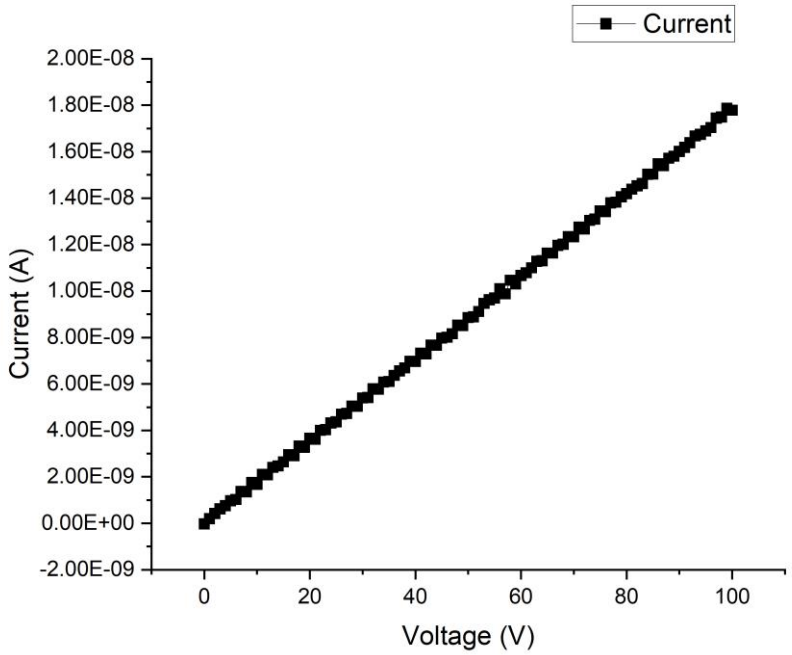


Figure 32a: S1 IV Curve for third smallest Al electrode pad size with a voltage sweep from 0 to 100 V after HAST.

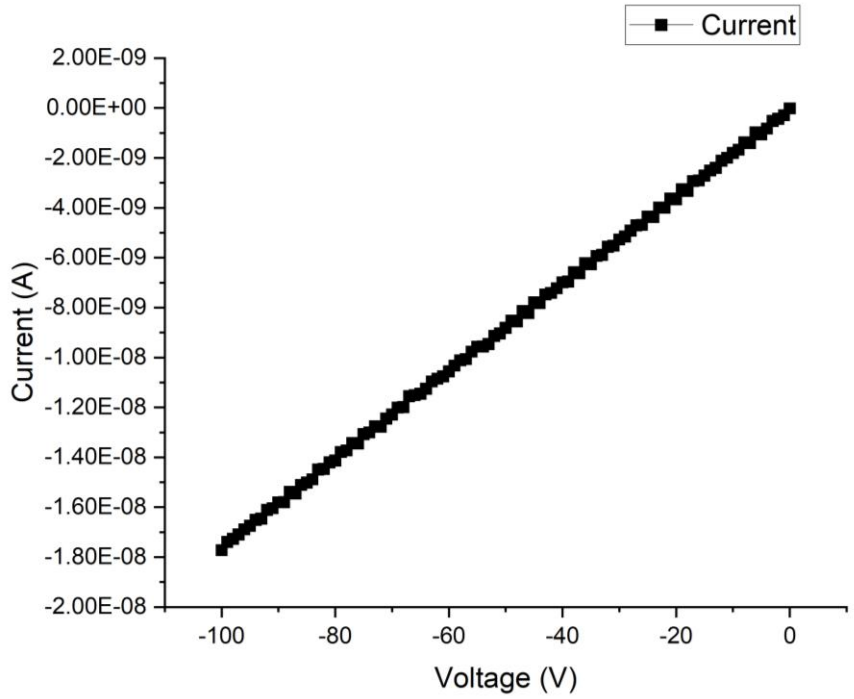


Figure 32b: S1 IV Curve for third smallest Al electrode pad size with a voltage sweep from 0 to 100 V after HAST.

4.2 Daisy-chain Resistance Measurements

In the introduction there were a few main parameters mentioned, here we will discuss the importance of them and what their effect is on this project. Resistance is a valued measurement when characterizing a new material for use in the development of a novel packaging scheme. It determines how well connected the vias are between M3-to-M2 and M2-to-M1. As a standard check, when the via diameters are large enough, then the resistances can be measured using a multimeter.

Figure 5a shows the first wafer, which had four coupons with M2-to-M1 daisy-chains that gave us measurable resistance data. The left side of each coupon contained eight M2-to-M1 daisy-chains, with the flat of the wafer on the bottom, and in *Table 5* the values are listed. They were measured in order from bottom chain to the top chain.

Table 5: Wafer 1 Daisy-chain Resistance Measurements for four working coupons in Ω's.

Coupon #	Resistance (Ω)
4th	19.7, 23.6, 9.8, 328.9, 10.4, 17.8, 44.8, 23.7
5th	2.1, 4.7, 5.4, 5.4, 4.0, 3.7, 5.5, 5.4
7th	9.4, 17.7, 10.8, 14.2, 27.3, 29.4, 15.9, 21.3
8th	5.5, 42.6, 60.9, 0, 7.2, 7.0, 7.8, 3.7

It is important to understand that this is only a surface-level picture of the connectivity of the vias in this tri-layer stack. The prober tool, such as the Signatone, should be used in DC measurement mode to establish a clearer baseline of the resistance values obtained. The two probes on a multimeter have their own resistance values and there is residual contact resistance between the copper in the daisy-chains and metal contact of the meter. It is precisely for this reason why a more sophisticated probing tool is necessary in measuring resistance values, as the previously stated issues are major contributors to error.

4.3 Capacitance Measurements (C_p)

Checking the electrical characteristics of the ITO samples is important, but to verify the data the samples must be physically analyzed for any material failure. Using the Keyence Optical Profilometer again, the optical microscope can detect if there is any delamination of the dielectric film from its ITO substrate. We found there to be no delamination of the Zaristo-700 film from the ITO surface, and there was no change in surface thickness to show peeling away of the dielectric. The only physical change that occurred was the cracking of the ITO glass slides during HAST. As we have determined, the Zaristo-700 dielectric material is one of resilience and changing its environmental conditions seems to have little to no effect on its electrical and *some* of its physical properties.

Table 5 includes the capacitance values of one layer of dielectric with Al pads on top, and those graphs indicated that HAST has very little effect on the electrical characteristics of the Zaristo-700. To be discussed in the future works section, the obtaining of leakage current measurements on the tri-layer stacks will be completed upon iteration of the design. For simplification of the first iteration of the Zaristo-700 tri-layer stack-up, a capacitor pad was placed on the upper-left hand corner of both wafers. This was done to measure the capacitance across all three layers of the dielectric, and the two values were 0.34 and 0.37 pF. Low capacitances coincide with the design as having the three dielectric layers in parallel with each other. As the number if dielectric layers in parallel increase the lower the total capacitance of the RDL build-up. Each layer of the 30.0 μm thick dielectric draws the total capacitance closer to zero. These values were obtained by the Signatone Prober in the well-controlled environment glove box.

4.4 Shadow-Moir*é*: Warpage Analysis

Shadow-moir*é* measurements employed in advanced packaging pertain to a method utilized for the meticulous evaluation of the precision and alignment of diverse strata and attributes inherent to semiconductor packages. This method involves the projection of a shadow with a regular, predetermined pattern, often comprised of grids or lines, onto the surface of the package. Subsequently, the resulting moire pattern, arising from the interaction between this shadow and the underlying structures, is subjected to rigorous analysis. This technique is instrumental in the discernment of potential misalignments, deformations, or defects during advanced packaging procedures. It thereby serves as a vital tool in ensuring the meticulous alignment and quality assurance of the distinct constituents constituting advanced semiconductor packages, such as chips, substrates, and interconnections. In *Figure 32* the shadow moire setup from Akrometrix is shown [9].

Figure 33: Akrometrix shadow moire setup in PRC with the inner sample holder/grating setup shown.

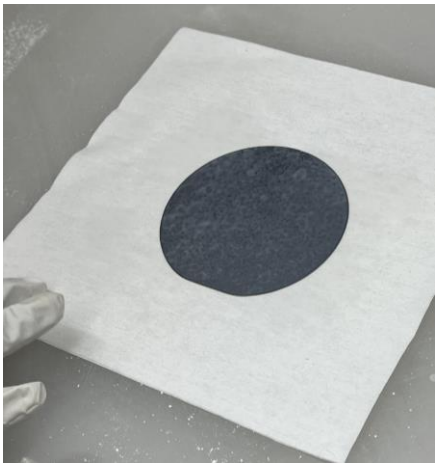


Figure 34: Thin non-reflective coating before drying on backside of Si substrate.

Before the measurement begins, a thin non-reflective coating is sprayed on the back of the wafer to create contrast for the system to pick up on and accurately measure the fringes (*Figure 33*). Two samples were analyzed: one “dummy” sample with two layers of dielectric and M1 then one full tri-layer RDL sample.

Convex warpage, in the context of advanced packaging and semiconductor technology, refers to a deformation or curvature in a package or substrate that results in its surface being curved outward or upward, resembling a convex shape. This warpage can occur due to various factors, such as differences in thermal expansion coefficients between the materials used in the package or during the manufacturing processes. Between the two samples, the warpage increases from 178 µm to 391 µm. Comparing one layer of copper and dielectric to three layers of both indicates that more RDL layers leads to larger warpage.

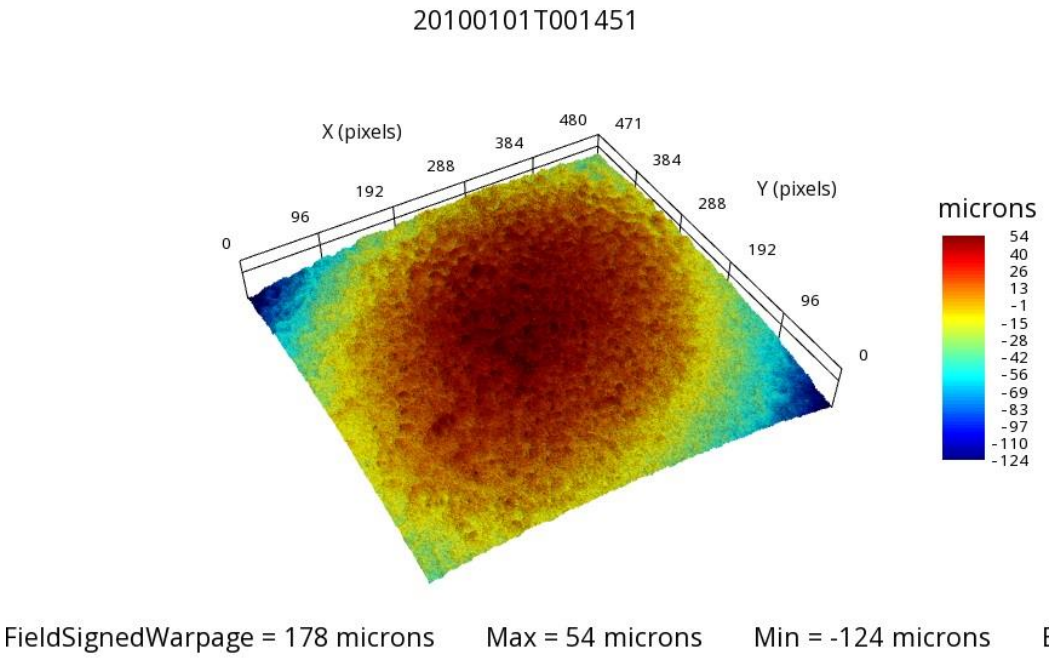


Figure 35: 3D Warpage map for Zaristo-700 dielectric double stack-up with only M1 completed.

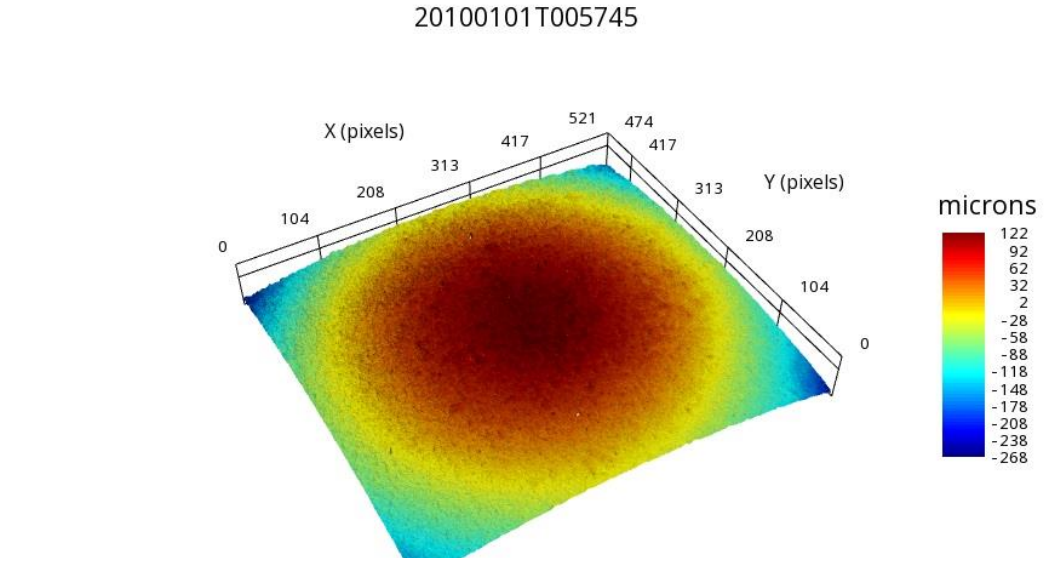


Figure 36: 3D Warpage Map for Zaristo-700 Tri-layer RDL Build-up sample.

4.4.1 Summary

In the context of shadow-moir*é* measurements, convex warpage may be a critical issue to address. When a package or substrate exhibits convex warpage, it can lead to misalignment and poor contact between various components within the package, such as the integrated circuit chips, interconnects, and substrates. This misalignment can affect the overall performance and reliability of the semiconductor device. Shadow-moir*é* measurements are employed to detect and quantify convex warpage, ensuring that the curvature of the package or substrate falls within acceptable tolerances and facilitating precise alignment and quality control in advanced packaging processes. From *Section 2.1*, the importance of CTE (coefficient of thermal expansion) was expressed as it is a major contributor to warpage of the packaging substrate. Copper has a CTE of 16.7 ppm/ºC whereas the Zaristo-700 dielectric has a reported CTE of 15-20 ppm/ºC. Even though the CTE of copper is within the range for the dielectric, any mismatch between coefficients can be pointed to as a cause for warpage. The thickness of the dielectric, at 30 µm, is a cause for concern with the warpage jumping to almost 400 µm with only three layers of dielectric. Currently, this measurement is high but acceptable for its sole purpose of demonstrating the Zaristo-700 as a RDL material. Each metal layer was fabricated without issues concerning warpage; therefore the only test is if it was put into an assembly via the solder resist on top of M3. Then we could observe if there were subsequent problems going forward in the assembly processing for advanced packaging (solder ball mounting, etc.).

CHAPTER 5. SUMMARY OF RESEARCH

5.1 Analysis of Findings

Exploring new materials for redistribution layers of advanced packaging applications has proved to be not a simple task. RDLs have been designed and in use for decades now, but even if they are well studied there is always more that can be done to further advance the field. Throughout this study we obtained more knowledge than ever on a material that has never been used in an RDL build up. Zaristo-700, 30 µm thick dielectric has proven to us that it can be implemented as an advanced packaging material for further development in applications.

First, a discussion on the issues that showed themselves during the characterization and fabrication processes. In the sections on laser via drilling and lithography dose testing high surface roughness was mentioned as a factor in not forming the most pristine and clean vias. After via drilling was completed, under the Keyence Optical Profilometer, there was debris at the bottom of the vias and onto the landing pad of the below metal layer. Previously stated, a plasma treatment of Ar is utilized to control and mitigate the amount of debris at the bottom of the vias. It has been demonstrated that this clean-step does remove the particles. The copper of M1 below a M2 via can be seen after an Ar plasma treatment, which is the same recipe as used to clean the surface before the TiCu seed layer (*Figure 26b).*

For dose testing the roughness of the material does not allow for fine lines and spaces to be developed, as only down to 8.0 µm L/S were achieved whereas the goal was at least 5.0 µm. A high surface roughness can lead to the direct write laser tool (Heidelberg MLA 150) not being able to focus completely on the surface, which leads to a variation in thickness in what the tool as measured. In *section 3.1.2*, the significantly high surface roughness has multiple effects on the processability, and fabrication methodologies used here at PRC. Therefore, it hinders the CD of the lithography capabilities onsite and limits the resolution of features within this RDL stack-up.

The connectivity issues of the vias from M3-to-M2 across the right-side of the twelve coupons could have been caused by either the via drilling or the seed-layer deposition that is done on Denton Discovery tool. It has been noted that with vias of any size, the Denton tool does not properly ensure an even coating of the TiCu seed layer on the bottom of vias. As there were issues with the Unifilm tool during the fabrication of these samples, the Denton tool allows two samples to be coated simultaneously and to continue parallel processing. Unfortunately, the recipes on the Denton does not allow for changing deposition rate where the Unifilm does. Now, in the future the Unifilm tool should be sought out for seed layer work at all costs. This can lead to issues in the copper electroplating steps, where the electroplated copper does not go through to the bottom of the via. This can be a direct cause of improper vias drilled, as maybe not all of them were connected to the metal layer below it. Despite physical checks on the Keyence if one via on all the daisy-chains was shorted then the rest of the seven in the row would read at 0.0 Ω.

5.2 Zaristo-700 Checklist

A checklist is the guide for an exploratory project such as this one, where a material that has been in production for other applications is now being researched for use in a novel manner. We have had to go through a series of characterization steps before beginning the fabrication of the tri-layer RDL demonstration on silicon. In this work there is a multitude of things that need to be completed to ensure the two samples fabricated can be further improved upon.

First, a more in-depth plasma study needs to be completed to show the effect of power, time, pressure, and flow rate have on surface roughness. Now, the roughness values were obtained on the profilometer, and an AFM (Atomic Force Microscope) should be used instead to provide a clearer picture on the material's surface condition. Not everything has been finished for this project and that is where the future works section will highlight what will come of this demonstration.

Table 6: Pros and Cons of Zariso-700 and a summary of the work completed as of this November.

Goals	Metrics	Objectives	Milestones – Nov, 2023 IAB	Challenges
First time use of Zaristo 700 as RDL material	Performance	• RDL thickness: 90 µm • High adhesion of Zaristo 700 • Obtain resistance measurements from daisy-chain structures • **Materials used for other industry applications can be studied for use in RDLs** • **Low CTE necessary for package reliability (15-20 ppm for Zaristo 700)**	• Total RDL thickness: 90 µm • Low leakage current	• Controlling warpage due to three layers of thicker dielectric • Developing fine features < 5 µm L/S
Creation and optimization of stable wiring layers using Zaristo 700	Miniaturization	• Total thickness < 400 µm • Number of metal layers 3 • Range of via sizes 23-50 µm	• Number of metal layers 3 • Completed tri-layer demonstration on Si • One or two layers of dielectric stack on **glass substrates**	

CHAPTER 6. CONCLUSION

In this body of work, we have completed an extensive characterization on the novel use of the Zaristo-700 dielectric as a future redistribution layer build-up material in advanced packaging applications. Studies on material properties, documentation of its behavior through JEDEC standard tests such as peel testing and HAST, as well as demonstrating the utilization of the dielectric in a three-metal layer stack up have all been done in the past 10 months. The data presented have more than proven that the Zaristo-700 is a great candidate for being used in multiple metal layer designs. Peel testing data has validated the claim for Taiyo, Ink. to use this dielectric as an RDL material for its incredible surface adhesion with copper and its Si substrate. Dose testing may have captured a crucial limitation on the resolution of the dielectric, but with further investigation we believe that 5.0 μm L/S features could be achieved. The shadow-moiré study on the tri-layer RDL raises some concern for future use in advanced packaging applications such as during package assembly especially if more layers are fabricated.

With further research and experimentation, this material could change the face of dielectrics that are considered "higher-κ" because they are on the higher end of the range for "low-κ's". Therefore, it would be in the best interest of Taiyo, Ink. as well as the PRC to continue pursuing the Zaristo-700 as a RDL stack-up material and to push the limits of the material to ensure it can further advance the advanced packaging technologies of today.

6.1 Future Work

Even after the accomplishment of two samples, with one of them partially working, there is still work to be done to optimize the process of integrating the Zaristo-700 material into a multi-metal layer stack. A future researcher can abide by what is listed, but a great researcher could expand upon what we could not finish. It's worthwhile for a researcher to go beyond that of the work the ones did before them. Below are some interesting ideas that have the potential to bring this demonstration to new heights if the research is continued.

1. Study the effect of Ar, O_2 or possibly a combination of the two, plasma on the Zaristo-700 through AFM, XPS, FTIR and other surface characterization techniques. There is room to explore how plasma treatments can either worsen or better the surface roughness of the dielectric.
2. Explore the use of different film deposition tools for TiCu seed layers, using surface characterization techniques such as ellipsometry to see how uniform the film is across the substrate.
3. Warpage of the Si substrate was studied through shadow moire experiments, to further examine this a researcher can utilize the temperature ramping of the tool once it is operational. This will bring a whole new set of parameters to examine and study, such as CTE.
4. A compelling argument for the Zaristo-700's use as a RDL material would be a study into the differences in CTE between the Si substrate, copper, and Zaristo-700 dielectric would be a compelling argument for its use in RDLs.

5. This project could be taken into the realm of glass. A future researcher could explore the possibility of glass wafers or panels, which calls for double sided processing, and how this thick dielectric behaves with a different material set. First, starting with one full metal layer, then a second, and finally a third.

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