

GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION
SPONSORED PROJECT INITIATION

Date: 12/14/78

Project Title: Assembly and Evaluation of Multichip Series-Connected IMPATT Diode Chips, a Feasibility Investigation

Project No: A-2300

Project Director: Mr. Charles T. Rucker

Sponsor: Microwave Associates, Inc.

Agreement Period: From 11/21/78 Until 4/20/79

Type Agreement: Standard Industrial Research Agreement, dated 11/21/78

Amount: \$15,509 (Phases I, II, and III)

Reports Required: Monthly Progress Reports; Final Report

Sponsor Contact Person (s):

Technical Matters

Contractual Matters
(thru OCA)

Dr. T. B. Ramachandran, Manager
GaAs and Transistor Products Division
Microwave Associates, Inc.
Burlington, Massachusetts 01803

Defense Priority Rating: N/A

Assigned to: ASL/SSSD (School/Laboratory)

COPIES TO:

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GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION
SPONSORED PROJECT TERMINATION

Date: July 11, 1979

Project Title: Assembly and Evaluation of Multichip Series-Connected IMPATT
Diode Chips, a Feasibility Investigation

Project No: A-2300

Project Director: Mr. Charles T. Rucker

Sponsor: Microwave Associates, Inc.

Effective Termination Date: 5/27/79

Clearance of Accounting Charges: 5/27/79

Grant/Contract Closeout Actions Remaining:

- Final Invoice and Closing Documents
- Final Fiscal Report
- Final Report of Inventions
- Govt. Property Inventory & Related Certificate
- Classified Material Certificate
- Other _____

Assigned to: Electromagnetics Laboratory/SSSD (School/Laboratory)

COPIES TO:

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Other _____

A-2300

Monthly Status Letter No. 1

(Ref. paragraph 6, Research Project Agreement)

ASSEMBLY AND EVALUATION OF MULTICHIP SERIES-CONNECTED
IMPATT DIODE CHIPS, A FEASIBILITY DEMONSTRATION

Contract Period Covered
21 November 1978 through 21 December 1978

Submitted to
Microwave Associates
Burlington, Massachusetts

by
Solid State Sciences Division
Applied Sciences Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by
C. T. Rucker

21 December 1978

GENERAL STATUS

Formal project work began on November 21, 1978. Twenty IMPATT chips, supplied earlier, have been used to proceed with Phase I tasks. Progress has been good and results to date are quite encouraging as briefly outlined below.

TECHNICAL STATUS

Chip Evaluation

Twenty chips from MA Lot No. 4819 1STPX615 have been screened in terms of V_B , leakage, capacitance and geometry (SEM). Some chips exhibit premature breakdown and/or leakage. A few exhibit plated heat sink voids. All show very close tolerance between the photoresist step (associated with heat sink electroforming) and the mesa edge. Copies of SEM photos related to these observations have been provided to R. Walline of MA.

None of the above imperfections constitutes a serious problem. Chip performance is quite uniform and the chips withstand considerable abuse.

Additional chips will be evaluated when received. Ten more chips from Lot 4819 1STPX615 were requested to insure a working supply. Higher power and/or efficiency chips should be forwarded when available.

Packaged Devices

Chip No. 2-4 was assembled and tested at 10% duty; efficiency of only 9% was obtained. Subsequent tests at 20% (after discussions with R. Walline) gave the performance noted below.

V_P (v)	I_P (A)	P_{in} (w)	P_{out} (w)	η (%)	f_o (GHz)	P.W. (μ sec)	Duty (%)
48	1.65	79.2	11.7	14.7	10.6	4	20

Additional tests with packaged chips 1-3 and 2-8 are noted below. Both operated efficiently ($\approx 15\%$) when operated at 25% duty. Data for both diodes are tabulated below.

DIODE 1-3

V	I	P	P _o	η	f _o	P.W.	Duty
51.0	1.8	92.3	11.3	12.2	10.4	4	20
51.0	1.9	97.9	14.4	14.7	10.2	2	25
50.6	1.7	88.0	13.9	15.8	10.2	4	25

DIODE 2-8

V	I	P	P _o	η	f _o	P.W.	Duty
50.0	1.9	94	11.1	11.8	10.2	4	20
47.8	1.6	75.5	12.4	16.5	10.5	4	25
46.8	1.4	67.0	12.0	17.9	10.4	4	33-1/3
45.0	1.6	70.7	12.1	17.2	10.4	4	40
44.0	1.2	53.7	9.8	18.2	10.4	4	50
CHIP FAILED DURING TUNING						1	50

MULTICHIP EXPERIMENTS

Prior to the variable duty testing of the foregoing paragraphs, a two chip unpackaged assembly using chips 1-4 and 1-10 was tested with efficiency of 11.7%. This assembly was converted to a three chip assembly by addition of chip 2-10. The device failed after much testing using P.W. = 4 μ sec, duty = 20%. Apparently both 2 and 3 chip versions would have operated more efficiently had the duty been increased. Typical data for another two chip assembly are given next.

TWO CHIP ASSEMBLY (Chips 2-1, 1-7)

V	I	P	P _o	n	f _o	P.W.	Duty
94	1.6	150.4	24.3	16.2	9.7	4	20

Apparently, this chip operated at higher temperature, giving good efficiency at duty of only 20%.

The most recent multichip diode consists of a 4 chip assembly using chips 1-8, 2-7, 2-3, and 1-9. This diode does not readily stay in the high efficiency mode but very encouraging results were achieved as noted below.

FOUR CHIP ASSEMBLY (1-8, 2-7, 2-3, 1-9)

V	I	P	P _o	n	f _o	P.W.	Duty
174	1.77	308.0	43.3	14.1	9.9	4	20
175	1.75	306.2	42.1	13.8	9.8	4	25
191	1.87	357.2	49.4	13.8	10.2	4	16
*178	1.80	320.4	45.4	14.2	10.0	4	22

* Bias oscillations not totally suppressed.

CONCLUSIONS

Single and multichip results are most encouraging. The work is continuing with tests limited to two chip assemblies.

ADMINISTRATIVE

The Engineering Experiment Station will be closed for the period December 25 through January 1.

Monthly Status Letter No. 2

(Ref. paragraph 6, Research Project Agreement)

ASSEMBLY AND EVALUATION OF MULTICHIP SERIES-CONNECTED
IMPATT DIODE CHIPS, A FEASIBILITY DEMONSTRATION

Contract Period Covered
21 December 1978 through 25 January 1979

~~IN CONFIDENCE~~

Submitted to
Microwave Associates
Burlington, Massachusetts

by
Solid State Sciences Division
Applied Sciences Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by
C. T. Rucker

26 January 1979

GENERAL STATUS

Progress has continued to be good. The initial chip lot (20 chips) is depleted. The successful completion of Phase I appears to be insured but additional chips are needed immediately to complete this phase. Five to ten chips are needed to complete Phase I and at least 20 (preferably 30 to 40) additional chips are needed for Phase II.

Phase I can be considered complete if desired because the three detailed tasks of this phase have been nominally completed. It should be noted, however, that only 20 chips have been evaluated. Phase I allowed for evaluation of approximately 50 chips. If chips having higher power and/or efficiency are now available, we recommend that some of these chips be evaluated before proceeding to Phase II. Completion of Phase I was due on 21 January 1979. Therefore, continuation of Phase I will cause a schedule slip. Phase II will require approximately two months after chips are received. Work is now stopped awaiting additional chips.

TECHNICAL STATUS

The last monthly status letter (No. 1) reported chip evaluation, tests with packaged chips and multichip experiments with two and four chips. Additional experiments, using two chips, have been performed in an attempt to ascertain whether or not stabilization capacitors are necessary with these chips.

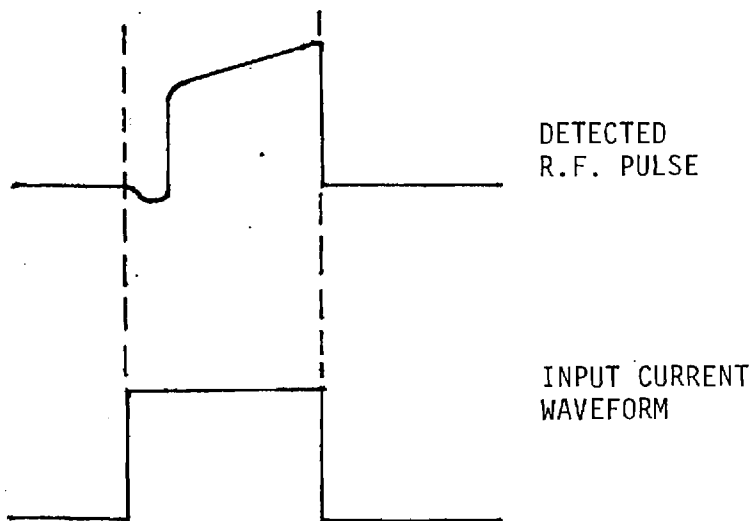
The most useful result would be obtained if two chips could be mounted on a diamond, in the standard pill package (ceramic I.D. = .050") with 3-48 stud. One two-chip assembly of this type was constructed. Results were poor as tabulated below. In general this assembly behaved poorly and was most difficult to tune.

(v)	(A)	(W)	(W)	(%)	(GHz)	(μ sec)	(%)
V	I	P	P_o	η	f_o	P.W.	Duty
100.0	1.88	188.0	18.8	10.0	9.0	2	20
Drops mode, can't tune						2	25
98.0	1.83	179.3	17.5	9.8	8.9	4	20

A two chip unpackaged assembly was next constructed with stabilization capacitors in place but unconnected. Results obtained were:

V	I	P	P_o	η	f_o	P.W.	Duty
92.0	1.62	149.0	14.1	9.5	10.3	2	20
96.0	1.95	187.2	20.1	10.7	10.2	4	25
89.0	1.82	162.0	20.5	12.7	10.0	4	33.3

Under short pulse conditions (2 μ sec) the detected output waveform showed severe turn-on problems as indicated in the sketch below.



The capacitors were connected resulting in the behavior tabulated below.

V	V	P	P _o	η	f _o	P.W.	Duty
99.0	2.02	200.0	21.2	10.6	10.2	4	25
97.0	1.81	175.6	23.3	13.3	10.0	4	33.3

These data imply that nominally similar performance is obtained with the unpackaged assembly whether or not capacitors are used. The experiment is considered to be inclusive for several reasons.

- 1) Two packaged chips exhibit very poor performance without capacitors.
- 2) Two unpackaged chips noted above behave only moderately well but equally well with and without capacitors.
- 3) The efficiency and power of all the above data do not compare well with earlier data reported in Status Letter No. 1.

Additional tests appear to be in order to resolve this problem. Statistics based on one or two assemblies are not sufficient to provide a good basis for proceeding to Phase II.

Monthly Status Letter No. 3

(Ref. Paragraph 6, Research Project Agreement)

ASSEMBLY AND EVALUATION OF MULTICHIP SERIES-CONNECTED
IMPATT DIODE CHIPS, A FEASIBILITY DEMONSTRATION

Contract Period Covered
25 January 1979 through 21 March 1979

~~CONFIDENTIAL~~

Submitted to
Microwave Associates
Burlington, Massachusetts

by
Solid State Sciences Division
Applied Sciences Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

Prepared by
C.T. Rucker

21 March 1979

PROJECT STATUS

Except for minor administrative activity, work on this task has been stopped since submission of the last Monthly Status Letter (No. 2). The work is stopped because the 20 diode chips supplied originally have been depleted.

We are presently awaiting:

- 1) Receipt of additional diode chips from Microwave Associates.
- 2) Instructions from Microwave Associates related to either continuation of Phase I or start of Phase II.

The program schedule will be reorganized upon receipt of further instructions from Microwave Associates.

Monthly Status Letter No. 4

(Ref. Paragraph 6, Research Project Agreement)

ASSEMBLY AND EVALUATION OF MULTICHIP SERIES-CONNECTED
IMPATT DIODE CHIPS, A FEASIBILITY DEMONSTRATION

Contract period covered
21 March 1979 through 15 April 1979

~~IN CONFIDENTIAL~~

Submitted to
Microwave Associates
Burlington, Massachusetts

by
Solid State Sciences Division
Applied Sciences Laboratory
Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting through
Georgia Tech Research Institute
Georgia Institute of Technology

Prepared by
C.T. Rucker

15 April 1979

PROJECT STATUS

Technical

Except for minor administrative activity, work on this task has been stopped since submission of Monthly Status Letter No. 2. This work is stopped because the 20 diode chips supplied originally have been depleted.

We are presently awaiting:

- 1) Receipt of additional diode chips from Microwave Associates.
- 2) Instructions from Microwave Associates related to either continuation of Phase I or start of Phase II.

The program schedule will be reorganized upon receipt of further instructions from Microwave Associates.

Funding

Contract funds in the amount of \$7,991.80 remain.