

**INVESTIGATION OF THERMAL PERFORMANCE OF THIN FILMS
FOR EMERGING ELECTRONIC APPLICATIONS**

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The Academic Faculty

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INVESTIGATION OF THERMAL PERFORMANCE OF THIN FILMS FOR EMERGING ELECTRONIC APPLICATIONS

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[Dedicated to my mom, dad, brother, wife and son, who are the five pillars in my life]

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS	iv
LIST OF TABLES.....	viii
LIST OF FIGURES	ix
LIST OF ABBREVIATIONS AND SYMBOLS.....	xii
SUMMARY	xvii
CHAPTER 1: INTRODUCTION.....	1
1.1. THERMAL PROPERTIES OF MATERIALS RELEVANT TO POWER ELECTRONICS AND MEMRISTORS.....	1
1.1.1. Power electronics.....	1
1.1.2. Memristors	2
1.1.3. Thermal Conductivity Measurements and Data Analysis.	3
1.2. HEAT MANAGEMENT IN PORTABLE ELECTRONICS.....	3
1.2.1. Heat spreaders.....	3
1.2.2. Bonding materials	5
1.3. MOTIVATION.....	6
1.3.1. Power Electronics	6
1.3.2. Memristors.....	7
1.3.3. Machine Learning for FDTR Data Analysis.....	8
1.3.4. Heat Management in Portable Electronics.....	8
1.3.5. Bonding Materials for Thermal Interface	10
1.4. OVERALL OBJECTIVE AND SCOPE OF THE DISSERTATION.....	10
CHAPTER 2: LITERATURE REVIEW	12
2.1. THERMAL PROPERTIES OF GALLIUM OXIDE	12
2.2. ALTERNATIVE MATERIALS FOR MEMRISTOR’S ELECTRODES	15
2.3. TDTR, FDTR, AND ML FOR DATA ANALYSIS.....	18
2.4. h-BN THERMAL PROPERTIES AND ITS TRANSFER METHODS	22
2.1.1. h-BN thermal properties.	22

2.1.2. h-BN transfer methods	23
2.5. HOPG AS A HEAT SPREADER AND ITS BONDING METHODS	26
2.6. CONTRIBUTIONS OF THE RESEARCH.....	28
CHAPTER 3: METHODS	30
3.1. TIME-DOMAIN AND FREQUENCY-DOMAIN THERMOREFLECTANCE.....	30
3.2. HOPG MECHANICAL TESTING	34
3.3. A TRANSIENT THERMAL METHOD BASED ON THE JEDEC JESD51-14 STANDARD TO ESTIMATE THE THERMAL RESISTANCE OF THE BONDED MATERIALS	35
CHAPTER 4: MEASUREMENTS AND NUMERICAL CALCULATIONS OF THERMAL CONDUCTIVITY TO EVALUATE THE QUALITY OF β-GALLIUM OXIDE THIN FILMS GROWN ON SAPPHIRE AND SILICON CARBIDE BY MOLECULAR BEAM EPITAXY.....	38
4.1. INTRODUCTION	38
4.2. DESCRIPTION OF THE Ga₂O₃ SAMPLES.....	38
4.3. THEORETICAL CALCULATIONS	41
4.4. RESULTS	44
CHAPTER 5: MACHINE LEARNING APPROACHES TO STUDY THE THERMAL CONDUCTIVITY OF MATERIALS FOR MEMRISTORS ELECTRODES	51
5.1. THERMAL CONDUCTIVITY OF MATERIALS AIMED TO IMPROVE MEMRISTORS' PERFORMANCE	51
5.2. ML MODELS FOR THE ANALYSIS OF FDTR DATA.....	53
5.3. RESULTS	55
5.3.1. Results for a two-layer model of an anisotropic material to predict three parameters simultaneously.	55
5.3.2. Results for a two-layer model of an anisotropic material to predict four parameters simultaneously.	57
5.3.3. Results for a three-layers model (thin film) anisotropic material to predict four variables at once.	58
5.4. SUMMARY.	60
CHAPTER 6: HEAT SPREADERS FOR PORTABLE ELECTRONICS.....	62
6.1. h-BN AND HOPG FOR THERMAL MANAGEMENT OF HOT SPOTS ON SILICON CHIPS USED IN MOBILE DEVICES: A SIMULATION-BASED COMPARISON	62

6.2. METHODS AND CHALLENGES TO TRANSFER h-BN ON OTHER SUBSTRATES.....	65
6.3. APPROACHES TO REDUCE THERMAL RESISTANCE WITH HEAT SPREADERS MADE OF HOPG IN MICRO-ELECTRONICS: THE ROLE OF CYTOP AND NP-Cu. 69	
6.3.1. HOPG Morphology and Shear Strength.	69
6.3.2. Fabrication Methods	71
6.3.3. Thermal assessment of HOPG bonded with CYTOP and NP-Cu.	77
CHAPTER 7: SUMMARY AND FUTURE WORK.....	85
7.1. SUMMARY OF THE DISSERTATION.....	85
7.2. FUTURE WORK.....	87
7.2.1. Thermal properties of epitaxially-grown Ga ₂ O ₃	87
7.2.2. ML methods for data analysis of FDTR experiments.....	88
7.2.3. HOPG as a heat spreader for the thermal management in mobile electronics.....	88
APPENDIX A: SUPPLEMENTARY MATERIAL FOR CHAPTER 4.....	90
A.1. DETAILS OF THE TDTR SYSTEM	90
A.2. METHODS TO CALCULATE UNCERTAINTY.....	91
A.3. CALCULATIONS OF THE LATTICE THERMAL CONDUCTIVITY IN THE (-201) DIRECTION	91
A.4. CALCULATIONS OF THE DMM MODEL.....	93
REFERENCES.....	95

LIST OF TABLES

Table 2.1. Experimental reports of in-plane thermal conductivity of h-BN	22
Table 2.2. Polymers used in handling layers for 2D materials transfer	24
Table 4.1. TBC results with the uncertainty estimate with two different methods	48
Table 5.1. Physical properties of the materials	52
Table 5.2. Thermal conductivity of measured Ti-based materials.....	52
Table 5.4. Comparison of the ML model architectures used in this work.....	54
Table 5.5. Range of the parameters to generate the training database for two-layer models with anisotropic material and with gold transducer.	55
Table 5.6 Comparison of the performance of Models A and B in the training phase for a two-layer model with anisotropic material for the prediction of three variables at once.....	56
Table 5.7. Actual (traditional fitting) and ML-predicted k_{in} , k_{out} , and G_I for sapphire.....	57
Table 5.8 Comparison of the performance of Models A and B in the training phase for a two-layer model with anisotropic material for the prediction of four variables at once.	58
Table 5.9. Actual (traditional fitting) and ML- predicted k_{in} , k_{out} , $pump\ radius$, and $Au\ thickness$ for sapphire	58
Table 5.10. Range of the parameters to generate the training database for three-layer models with anisotropic material with gold transducer.....	59
Table 5.11. Actual (traditional fitting) and ML-predicted k_{out} , k_{in} , $pump\ radius$, and $Gold\ thickness$ $Ti_2AlN\ MAX\ Phase$	60
Table 6.1 Thermal conductivity of heat spreader materials.....	63
Table 6.2. Summary of thermal resistance values for the different options of bonding material. 81	

LIST OF FIGURES

Fig. 3.1. Schematic of the TDTR system used to measure the thermal conductivity and the thermal boundary conductance (left), and typical TDTR signal and data fitting for Ga₂O₃ on SiC sample at a frequency of 3.6 MHz [147]. Copyright © 2020, IEEE..... 32

Fig. 3.2. Schematic of the FDTR system used to measure the thermal conductivity and the thermal boundary conductance (left). The acronyms M, PBS, HWP, QWP, L, ISO, PD, BP, DMLP, and OBJ stand for mirror, polarizing beam splitter, half-wave plate, quarter-wave plate, lens, isolator, photo-diode, bandpass filter, low pass dichroic mirror, and objective lens, respectively [149]. Typical FDTR signal and data fitting for Ti₂AlN-Cubic sample (right). Left figure - Copyright © 2023, IEEE..... 33

Fig. 3.3. Diagram of the shear tests performed on bonded HOPG. 35

Fig. 3.4. Cumulative structure-function: the graphic representation of the thermal RC equivalent. Reproduced with permission from Springer Nature from Lasance, Clemens JM, and András Poppe, eds. *Thermal management for LED applications*. Vol. 2. New York: Springer, 2014 [150]..... 36

Fig. 4.1. A bright-field low- and high- resolution TEM micrographs showing (a-c) Ga₂O₃ on sapphire substrate with a thickness of ~ 119.4 nm. The presence of the lattice fringes as well as FFT reflections (inset) suggests crystalline structure. There exists lattice strain field across the HRTEM micrograph. (c) HRTEM micrograph obtained from a specimen rotated normal to the substrates Z= [01 $\bar{1}$ 0] direction reveal a crystalline structure decorated with high density of 1-D defects like stacking faults and twinning dislocations within the film which are indicated by SF and T, respectively. (d) bright-field TEM show ~ 81 nm thick Ga₂O₃/SiC. In addition, (e) HRTEM and (f and g) FFT of the film and substrate show lattice fringe real images and respective low-order diffraction reflection demonstrating crystallinity in structure of Ga₂O₃ film.....40

Fig. 4.2. AFM image of the surface of a β -Ga₂O₃ sample grown on SiC for this work. The mean lateral grain size is 52 nm. The field of view of the image is 500 x 500 nm²..... 41

Fig. 4.3. (a) Comparison of published values of the thermal conductivity of thin films Ga₂O₃ with respect to their thickness. The sample for this work were grown by MBE, whereas the rest of the films were grown using PLD, MOVPE or were monocrystals [22, 23, 34, 51, 178]. (b) Variation of the thermal conductivity of Ga₂O₃ in the (-201) direction with thickness. Thermal conductivity computed using BTE is compared against the experimental results. The dashed line corresponds to the bulk thermal conductivity in the (-201) direction, as reported by [34]..... 47

Fig. 4.4. (a) Influence of gallium and oxygen vacancies on the thermal conductivity. Gallium vacancies cause a higher reduction in the thermal conductivity compared to oxygen vacancies. The linear defect density is set to zero to isolate the effect of vacancies. (b) Influence of the density of linear defects on the thermal conductivity when gallium vacancies are present for the 119 nm sample (grown on sapphire)..... 47

Fig 5.1. Schematic of the ML model architectures used in this work. 53

Fig. 6.1. Diagram of the smartphone (left) and Package on Package (right)..... 63

Fig. 6.2. Performance of h-BN heat spreader with a thickness of 0 ~ 80 μm (left) and HOPG heat spreader with a thickness of 0 ~ 30 μm (right) 65

Fig. 6.3. Schematic of the transfer process of h-BN from Cu foil to a new substrate. 66

Fig. 6.4. Qualitative comparison of the surfaces of h-BN with different handling polymer layers. (a) pristine h-BN on Cu. (b) h-BN transferred using PMMA as the handling layer. (c) h-BN transferred with PC. (d) h-BN transferred using rosin. Contamination and defects are evident in (b) and (c), whereas the sample is destroyed in (d) 67

Fig. 6.5. XPS results for a h-BN sample transferred with PMMA. The figure shows boron, nitrogen, and carbon curves and the estimated atomic composition obtained from the curves.... 68

Fig. 6.6. Cross section of HOPG shows three types of irregularities on the surface: regular roughness, valleys, and waviness. The irregularities are randomly present all over the surface.. 69

Fig. 6.7. Comparison of unbonded regions when bonded with different materials. (a) Au. (b) 2 μm CYTOP. 70

Fig. 6.8. Correlation between the copper composition in the alloy and the current density..... 73

Fig. 6.9. Comparison between an 82%Cu / 18% Zn alloy (left) and a 90% Cu / 10% Zn alloy in SEM images taken from the top. The structures on the left resemble an interconnected network of ligaments, whereas those have disappeared in the right image, which means that the sample shown on the right is "too de-alloyed." The scale bar is 200 μm 74

Fig. 6.10. Comparison between an 82%Cu / 18% Zn alloy, whose de-alloying times were ~ 1 hour (left) and 1 hour 45 minutes (right) in SEM images taken from the top. The ligaments have disappeared in the sample on the right. Both images have a magnification of ~45KX..... 74

Fig. 6.11. Problems presented during NP-Cu fabrication due to improper cleaning protocols. If the samples are not adequately cleaned, the remaining HCl will form crystals on the surface (right), whereas a too-aggressive cleaning protocol might delaminate the NP-Cu from the seed layer (right) 75

Fig. 6.12. Representation of samples used for the thermal tests. Epoxy, CYTOP, or NP-Cu are used between the Silicon and HOPG layers. Double-sided tape is used to bond the Si/bonding material/HOPG stack on the backside of a power diode. To perform the experiments, half of the samples have an extra double-sided tape layer (right) to attach the stack to the FR4 board. 77

Fig. 6.13. Comparison between delaminated samples bonded with CYTOP (left, SEM image) and NP-Cu (right, optical microscope image) taken from the top. The inset in the right figure shows a magnified area with NP-Cu and HOPG. Most of the area is covered by delaminated HOPG with

"unbonded areas" scattered on the surface of both samples. These unbonded areas are bonding defects that might affect thermal performance. The scale bar is 100 μm 77

Fig. 6.14. Comparison of the structure functions (left) and the derivative of the structure functions (right) of two power diodes, without and with an additional double-sided tape to attach the sample to the FR4 substrate and use the procedure established in the JEDEC JESD51-14 standard for the measurement of the junction-to-case thermal resistance of semiconductor devices with heat flow through a single path. The separation point indicates the value of the package's thermal resistance. The separation is more apparent in the right-side plot..... 78

Fig. 6. 15. Cross section of a sample bonded at 200 °C. The detail a. shows a fractured region where the HOPG started to separate from the NP-Cu layer. The detail b. shows a bonded region with no gaps between HOPG and NP-Cu. Detail c. shows an un-bonded region with a wide gap between the HOPG and the NP-Cu. The scale bar for the image is 5 μm , whereas that for the insets is 2 μm 82

Fig. 6.16. Schematic of the model used for the simulation..... 83

LIST OF ABBREVIATIONS AND SYMBOLS

Abbreviations

APU	Application Process Unit
ANN	Artificial Neural Networks
AFM	Atomic Force Microscopy
BP	Bandpass Filter
BTE	Boltzmann Transport Equation
BLT	Bond Line Thickness
CPU	Central Process Unit
CVD	Chemical Vapor Deposition
CW	Continuous Wave
DL	Deep Learning
DFT	Density Functional Theory
DUT	Device Under Test
DMM	Diffuse Mismatch Model
EFG	Edge-defined Film-fed Growth
E _g	Energy Gap
EDX	Energy-Dispersive X-ray Spectroscopy
EMC	Epoxy Mould Compound
FFT	Fast Fourier Transform
FEM	Finite-element-Method
FZ	Floating Zone
FIB	Focused Ion Beam

FDTR	Frequency-domain Thermoreflectance
GaN	Gallium Nitride
Ga ₂ O ₃	Gallium Oxide
GPU	Graphics Process Unit
HfO ₂	Hafnium Oxide
HWP	Half-Wave Plate
HDI	Heat Diffusion Imaging
h-BN	Hexagonal Boron Nitride
HTERM	High Resolution Transmission Electron Microscopy
HOPG	Highly Oriented Pyrolytic Graphite
IFC	Interatomic Force Constants
IQR	Interquartile Range Method
ISO	Isolator
L	Lens
DMLP	Low Pass Dichroic Mirror
LPCVD	Low-Pressure Chemical Vapor Deposition
ML	Machine Learning
MESFET	Metal Semiconductor Field Effect Transistor
MOCVD	Metal-Organic Chemical Vapor Deposition
MOVPE	Metal-Organic Chemical Vapor Phase Epitaxy
MOSFET	Metal-oxide-semiconductor Field-effect Transistor
M	Mirror
MAE	Mean Absolute Error

MAPE	Mean Absolute Percentage Error
MBE	Molecular Beam Epitaxy
NP-Cu	Nanoporous Copper
NRL	Naval Research Laboratory
OBJ	Objective
PoP	Package on Package
PBE	Perdew-Burke-Ernzerhof
PD	Photo-diode
PBS	Polarizing Beam Splitter
PC	Poly(bisphenol A carbonate)
PMMA	Poly(methyl methacrylate)
PMMA	Polymethyl methacrylate
PAW	Projector Augmented-Wave
PLD	Pulsed-Laser Deposition
QWP	Quarter-Wave Plate
RS	Resistive Switching
SEM	Scanning Electron Microscope
SAED	Selected Area Electron Diffraction
SiC	Silicon Carbide
Ta ₂ O ₅	Tantalum Oxide
TSP	Temperature-Sensitive Parameter
TBC	Thermal Boundary Conductance
TIM	Thermal Interface Material

TDTR	Time-domain Thermoreflectance
Ti ₂ AlN	Titanium Aluminum Nitride
TiN	Titanium Nitride
TiO ₂	Titanium Oxide
TMDs	Transition Metal Dichalcogenides
2D	Two-Dimensional
VASP	Vienna ab initio simulation package
XRD	X-Ray diffraction
XPS	X-Ray photoelectron spectroscopy
XRR	X-ray reflectometry

Symbols

β	Beta Phase
l	Thermal Penetration Depth
f	Frequency
D	Thermal Diffusivity
$1/\tau_{\text{anh}}$	Intrinsic Anharmonic Phonon Scattering Rate
$1/\tau_{\text{b}}$	Phonon Boundary Scattering Rate
$1/\tau_{\text{v}}$	Phonon Scattering Rate due to the Vacancies
$1/\tau_{\text{gb}}$	Phonon Scattering Rate due to Grain Boundaries
x	Density of Vacancies
M	Average Mass per Atom
M_{v}	Mass of the Missing Atom

$g(\omega)$	Phonon Density of States
G	Number of Atoms in the Crystal
$p(\omega)$	Specularity Parameter
D_{avg}^{-1}	Average Grain Size of Polycrystalline Samples
a	Lattice Parameter
v	Phonon Velocity
γ	Grunnessien's Constant
ω	Angular Frequency
N_s	Number of Linear Faults per cm
R^2	Coefficient of Determination
k_{out}	Out-of-plane (Trough plane) Thermal Conductivity
k_{in}	In-plane Thermal Conductivity
C	Volumetric heat capacity
G_1	TBC material/gold transducer
G_2	TBC material/substrate

SUMMARY

The demands for faster and more robust wireless communication systems, superior power electronics, enhanced memory, advanced neuromorphic computation, and powerful portable electronics have accelerated the evolution of electronics. Regardless of the type of electronic system, critical components like transistors and diodes must be faster, smaller, and more efficient. These devices necessitate new materials, the thermal properties of which are critical in designing effective thermal management solutions. Moreover, these new materials' fabrication and integration methods significantly impact their thermal properties. Therefore, understanding the thermal properties of materials used in power electronics, memristors, and heat spreaders is paramount. This dissertation delves into this crucial topic, offering insights and research findings that stand to contribute to the field significantly.

In this dissertation, I present a comprehensive investigation into the thermal properties of various materials pertinent to emerging electronic devices. My research initially focused on the thermal conductivity of β -Ga₂O₃ thin films grown on different substrates. I utilized techniques such as Time-Domain Thermoreflectance (TDTR), Atomic Force Microscopy (AFM), and Transmission Electron Microscopy (TEM) to investigate this aspect. This detailed analysis enabled me to estimate the defect densities (vacancies and dislocations), offering insights into the impact of different defects on thermal conductivity.

Subsequently, I explored the thermal conductivity of various Ti-containing materials, specifically those used in memristor electrodes. I discovered that Ti₂AlN (MAX Phase) could improve the performance of HfO₂-based memristors compared to traditional TiN. My research also encompassed the evaluation of machine learning models in the context of thermal conductivity analysis. By comparing two Artificial Neural Network (ANN) architectures, I found that the task

was complex and would require further work to optimize model architecture and hyperparameters to have a model with enhanced predictive power.

Moreover, I examined the feasibility of hexagonal boron nitride (h-BN) and highly oriented pyrolytic graphite (HOPG) as heat spreaders for silicon chips in mobile devices. I performed simulations to compare the thermal performance of h-BN and HOPG. I studied various h-BN transfer methods to assess their adaptability to industrial processes. I concluded that HOPG outperforms h-BN not only in terms of thermal management but also in terms of costs and current commercial availability.

Lastly, I experimented with CYTOP and nanoporous copper (NP-Cu) for bonding HOPG heat spreaders on Si substrates. While it was evident that optimal bonding conditions still need to be determined, I concluded that both strategies to reduce thermal resistance—reducing the Bond Line Thickness (BLT) using CYTOP and improving the thermal conductivity of the bonding material with NP-Cu—shows promise.

This dissertation provides a pathway for the continued development of thermal management of emerging electronic materials, offering valuable insights and strategies that may guide future research and applications in this rapidly advancing field.

CHAPTER 1: INTRODUCTION

Faster and more powerful wireless communication systems, better power electronics, improved memory, neuromorphic computation, and miniaturization of portable electronic devices are just a few of the demands required by electronic applications that are needed to handle the introduction of technologies such as renewable energies, electric mobility, neural networks, and artificial intelligence, among others. Regardless of the type of electronic systems, components of electronic circuits in these systems, such as transistors and diodes, need to be made faster and smaller, which require new materials, and the thermal properties of these new materials and their interfaces after integration into a device are needed to design an efficient thermal management solution. In addition to successfully employing these new materials in practical applications, the manufacturing methods to fabricate and integrate these materials influence their thermal properties. In this chapter I discuss the importance of studying the thermal properties of materials employed in power electronics, memristors, and heat spreaders, along with the motivation, the overall objective, and the outline of this dissertation.

1.1. THERMAL PROPERTIES OF MATERIALS RELEVANT TO POWER ELECTRONICS AND MEMRISTORS

1.1.1. *Power electronics.*

RF and power electronic devices use materials with wide bandgaps. The state-of-the-art commercial devices are made of SiC ($E_g \sim 3.25$ eV) or GaN ($E_g \sim 3.4$ eV). Nevertheless, β -Ga₂O₃ is emerging as a material that may be widely used in future devices. On the one hand, the high bandgap and critical electric field of β -Ga₂O₃ (4.8 eV and 10 MV/cm, respectively) make this material ideal for high-performance devices. On the other hand, the low thermal conductivity of β -Ga₂O₃ (10 – 30 W/m-K for single crystal specimens) represents a challenge for thermal

management. One of the advantages of β -Ga₂O₃ is that single crystal substrates can be fabricated from the melt by the floating zone (FZ) and edge-defined film-fed growth (EFG) methods [1], which can be used to produce large diameter wafers at low cost and low energy consumption. Homoepitaxy growth of β -Ga₂O₃ has produced β -Ga₂O₃-based devices (diodes, MESFETs, and MOSFETs, among others.). However, to efficiently remove heat from β -Ga₂O₃-based devices, high thermal conductivity materials should be used as substrates. Researchers in [2] simulated and compared β -Ga₂O₃ MOSFETs fabricated on crystalline β -Ga₂O₃ and 4H-SiC, respectively. They found that devices grown on 4H-SiC substrates presented a “...18% increase in the peak drain current and 15% reduction in lattice temperature.” These results indicate that fabricating β -Ga₂O₃-based devices on thermally conductive substrates might be a good strategy for thermal management.

1.1.2. Memristors.

The advent and refinement of machine learning (ML) algorithms have produced an explosion of machine learning-based applications such as natural language processing, fraud detection, image and object recognition, and image generation, among others. All these applications are limited because of the data transmission speed between the processor and the memory, known as the “memory wall” [3]. Researchers in [4] have proposed an architecture called in-memory computing, in which memristors play a vital role. Memristors can also be used for neuromorphic computing, miming the functioning of neurons and synapses. Neuromorphic computing devices are more efficient than traditional computing machines, particularly for deep learning model training tasks.[5, 6]. Researchers in [7] presented a model to describe the roles of the electric field, temperature, oxygen vacancy concentration gradient, and different material and device parameters on the change in the resistance of memristors. I am interested in the role of the

thermal phenomena, which depends on the thermal properties of the switching material, the substrate, and the electrode materials.

1.1.3. Thermal Conductivity Measurements and Data Analysis.

It is clear that estimating the thermal properties of the materials used in the next generation of electronic devices is capital, mainly when the thickness is thin because size effects can affect the thermal conductivity. Specialized techniques such as the 3ω method, time-domain thermoreflectance (TDTR), or frequency-domain thermoreflectance (FDTR) are employed for this purpose [8]. TDTR and FDTR are non-contact methods that use a pump laser to heat the sample with a periodic signal and a probe laser to detect the thermal response (by measuring the change in thermoreflectance of a transducer deposited on top of the sample). The data obtained from the experiments is the phase lag between the probe and pump signals in the time and frequency domains, respectively. The phase delay data is fitted with a theoretical model to estimate the thermal properties [9]. Depending on the complexity of the structure of the samples, the fitting process might be long and inaccurate. For this reason, different research groups [10, 11] have presented schemes for faster and more accurate data analysis based on ML algorithms.

1.2. HEAT MANAGEMENT IN PORTABLE ELECTRONICS

1.2.1. Heat spreaders

The new generation of electronic components employed in portable systems, such as smartphones and smartwatches, to mention a few, are smaller and high-power-density, which represents a significant challenge for thermal management. The power density of typical hot spots in microprocessors can range from 150 to 350 W/m² [12, 13]. Attaching a heat sink cooled by a fan to the microprocessor is not an option for portable systems because there is insufficient space. In this context, heat spreaders can provide a viable solution. Heat spreaders must be made of high

thermal conductivity material, such as metals (e.g., copper) or 2D materials (e.g., graphene or hexagonal boron nitride). Graphene and hexagonal boron nitride (h-BN) possess a layered structure of single layers arranged in a hexagonal lattice made of carbon atoms for graphene and alternating boron and nitrogen atoms for h-BN. These materials' attractive properties for thermal management are their high thermal conductivity in the basal plane (parallel to the layers). The basal plane thermal conductivity of suspended pristine graphene and h-BN is reported to be as high as ~ 5000 and 700 W/m \cdot K at room temperature, respectively [14] [15]. The thermal conductivity of transferred supported materials has been reported between 50 and 1020 W/m \cdot K for graphene [16] and between 60 and 500 W/m \cdot K for h-BN [17] [18]. The main difference between graphene and h-BN is that the latter is an electrical insulator, which would allow for efficient heat transfer without interfering with electrical components or causing short circuits. Despite their advantages, h-BN cannot be widely used yet. In the first place, the thickness of the anisotropic materials will affect the heat flow because these materials mainly transport heat laterally (the thickness of commercially available h-BN does not exceed 10 nm). In addition, the production and processing methods for high-quality h-BN can contribute to its higher cost than alternative materials. Finally, the availability and scalability of h-BN for large-scale applications can be challenging. While research and development efforts are ongoing to enhance the production and availability of h-BN, its widespread implementation in commercial electronic devices may still face limitations.

An alternative layered material that does not have the drawbacks of graphene or h-BN is highly oriented pyrolytic graphite (HOPG). HOPG is a unique form of graphite that exhibits a high degree of crystalline alignment along a specific axis. It is produced through pyrolysis, where a precursor material (usually a carbon-based compound) is heated to high temperatures in a controlled environment. The resulting HOPG material consists of thin graphite flakes stacked

together in a highly ordered manner. HOPG possesses exceptional anisotropic properties, meaning its physical and mechanical properties vary significantly depending on the direction in which they are measured. The basal plane of HOPG exhibits excellent thermal and electrical conductivity. Due to its high thermal conductivity, anisotropic properties, and availability in different thicknesses relevant to micro-electronics thermal management, HOPG can be utilized as a heat spreader to dissipate heat from electronic components and high-power devices.

1.2.2. Bonding materials

In thermal management, apart from the material used for the heat spreader, another critical factor is the thermal interface material (TIM) that connects the heat spreader to the chip's surface. Typically, TIMs like silicone grease, silicone grease pads, or thermal gel are commonly employed in electronics to establish contact between the heat spreader and the chip's surface. These conventional TIMs are usually composed of polymers with relatively low thermal conductivity. In addition to the low thermal conductivity, the typical bond line thickness (BLT) for this type of material typically ranges between approximately 50 and 150 μm [13, 14]. Despite the low thermal conductivity, one possible approach is to use highly flowable polymers that can reduce the bond line thickness by filling the air gaps between the silicon chip and the heat spreader. For example, polymers like CYTOP have been tested as bonding materials at low temperatures [17, 18]. CYTOP offers the advantage of manipulating the bond line thickness by adjusting the dilution ratio and the other processing parameters used during its deposition via spin coating.

A different approach is using thermo-compression bonding (used for metal-to-metal bonding). This process requires high bonding temperatures and pressures that might be unsuitable for semiconductor fabrication. However, using nano foams, such as nanoporous copper (NP-Cu), offers several advantages, such as achieving low-temperature sintering below 250 $^{\circ}\text{C}$.

Furthermore, these nanostructures retain much of the original high thermal conductivity associated with metals, enabling low-thermal resistance bonding. If successful, a bonding process with NP-Cu could present negligible thermal resistance between the device and the attached heat spreader.

1.3. MOTIVATION

1.3.1. Power Electronics

There is substantial literature on the fabrication of β -Ga₂O₃-based thin films and their devices. Fabrication methods include mechanical exfoliation of β -Ga₂O₃ nanomembranes, homo-epitaxy, and the hetero-epitaxy growth of β -Ga₂O₃ thin films using different growth methods [19]. The thermal conductivity of mechanically exfoliated β -Ga₂O₃ membranes (typically crystalline) ranging from \sim 200 to \sim 800 nm has been reported. However, the phonon scattering with the boundaries of the samples decreases their thermal conductivity. For example, researchers in [20] reported a decrease in thermal conductivity from 11.5 W/m-K to 4.7 W/m-K when the thickness of the sample decreased from 768 nm to 206 nm. In this work, the thermal boundary conductance (TBC) at the interface of β -Ga₂O₃ membranes and β -Ga₂O₃ single crystal substrates is measured to be 15 ± 4.5 MW/m²-K. These results coincide with [21], which measured the thermal conductivity of a 427 nm thick sample to be 8.4 ± 1.0 W/m-K and a TBC at the β -Ga₂O₃/diamond interface of $17 -1.7/+2.0$ MW/m²-K. The low TBC results from the weak Van der Waals forces between the membrane and the substrate, which will hinder the heat flow in their devices. For the case of epitaxy-grown samples, the thermal conductivity of β -Ga₂O₃ samples of thickness 100 - 500 nm, grown using pulsed laser deposition, has been reported. Representative values are 2.9 W/m-K, 5.3 W/m-K, and 12.4 W/m-K for 100 nm, 245 nm, and 500 nm thick samples, respectively [22, 23]. Nevertheless, the thermal conductivity and the thermal boundary conductance of thin films of β -Ga₂O₃ grown on high conductivity substrates, such as silicon carbide (SiC), have been

rarely reported. In conclusion, there is a need to investigate the thermal properties of β -Ga₂O₃ thin films of different thicknesses grown on foreign substrates and the link between the fabrication conditions, the structural properties of the material, and the thermal conductivity.

1.3.2. Memristors.

In its simplest form, a memristor is a two-terminal device made of a metal oxide (hafnium oxide, for example) that changes its electrical resistance based on the history of the applied voltage or current. The key mechanism behind the operation of a memristor is the movement and redistribution of ions or vacancies within its solid-state structure. When a voltage is applied across a memristor, the movement of charged species, typically ions or vacancies, occurs within the memristor's active material. This movement leads to a change in the conductive pathways or resistance of the device. Creating a conductive filament in metal oxides involves the formation of an oxygen-deficient region or a region enriched in metal atoms [24]. This formation requires breaking metal-oxygen bonds and migrating oxygen anions or vacancies. Researchers in [25, 26] studied the influence of substrate thermal conductivity on the memristors' performance by fabricating their devices on glass and flexible polyamide. They found that the devices fabricated on non-conductive substrates presented lower reset voltage, better endurance, and low switching current, among other desirable characteristics. Also, researchers in [27] used simulations to demonstrate that this concept of using low-thermal conductivity substrates can be extended to the electrodes, where devices with smaller thermal conductivity electrodes or substrates have more stable thermal switching. For this reason, studying the thermal properties of materials with a lower thermal conductivity than metals but that have significantly high electrical conductivity, such as Titanium Nitride (TiN) or Titanium Aluminum Nitride (Ti₂AlN), is important.

1.3.3. Machine Learning for FDTR Data Analysis

ML has established itself as a popular research tool in many scientific fields because it has the potential to accelerate experimental data processing. In the case of heat transfer, the phenomena are governed by complex physics, making it impractical to understand them from principles, even if the computational capabilities improve [28]. Consequently, ML algorithms can obtain computationally efficient and robust reduced-order models or determine an appropriate connection between the input parameters and the measured variables in complex experiments. In the case of TDTR and FDTR, data processing requires the iterative change of the fitting parameters until the theoretical model fits the experimental signal. Shen et al. [10] presented a novel data analysis approach for FDTR experiments using deep learning (DL) to predict the thermal properties of a sample. They developed a DL model for their experimental setup. The DL predictions can be used as initial guesses for the traditional fitting methods or rough estimates of the thermal properties.

On the other hand, Pang et al. [11] extended the ML-based approach. They developed generally applicable (i.e., valid for various experimental setups) ML models using artificial neural networks (ANNs) to process TDTR measurements. In both cases, the ML-based methods were tested with experimental data obtained from measuring bulk samples (samples with two layers: metal transducer and the bulk substrate). While it is true that ML algorithms are capable of helping in processing TDTR and FDTR analysis, their limits have yet to be tested. There is no comparison between different algorithms or clarity on the number of variables that can be accurately predicted using these techniques.

1.3.4. Heat Management in Portable Electronics

The (expected) high in-plane thermal conductivity of h-BN, combined with its electrical insulating nature, makes this material suitable for applications requiring electrical isolation, such

as near-junction heat spreading [17, 29]. However, its application as a heat spreader in other areas of the chip has yet to be explored. In addition, since the preferred method to fabricate commercially available h-BN is to grow it on a metallic substrate (copper or nickel) using chemical vapor deposition (CVD), h-BN must be transferred from its growth substrate to the substrate where it is intended to be used. The transfer methods are classified into four categories: metal etching, mechanical delamination, oxide-assisted delamination, and electrochemical delamination. Regardless of the method, a protective layer is deposited on the material to protect the 2D material and avoid damage during transfer. This material is usually a polymer and must be removed from the 2D material after the transfer. In consequence, fabricating an h-BN heat spreader is a complex process. Even if the growth conditions are ideal for obtaining high in-plane thermal conductivity, the different phases of the transfer process (protect the material, remove the metallic substrate, transfer to a new substrate, and cleaning) can introduce defects that can affect the in-plane thermal conductivity of h-BN after integration to target substrate. In short, the relation between the transfer process and the thermal conductivity must be studied, and its applicability as a heat spreader on the back side of a silicon chip. Even if the transfer process is flawless and the in-plane thermal conductivity is high, the nanometer-scale thickness of h-BN might hinder the heat flow. Fabrication methods for large-area (millimeter-scale) growth of micrometer-thick and high-quality h-BN have yet to be reported. Micrometer-thick h-BN is obtained in a research laboratory by exfoliation and cannot be adapted for large area samples. Few h-BN layers might not be good enough to spread heat in specific applications. Thus, highly oriented pyrolytic graphite (HOPG) has been considered a viable solution for heat spreaders on the backside of a chip.

1.3.5. Bonding Materials for Thermal Interface

Current solutions to bond HOPG either utilize metallization of the HOPG to use solder as the bonding material or polymer-based paste as the adhesive. In the first case, metallization of HOPG has been tested to directly bond a millimeter-thick HOPG-based heat spreader with a laser diode [30]. In the second case, since the bond line (BL) thickness is traditionally in the range of tens of microns, it could limit the heat conduction through the joint. For example, researchers in [31] used silicone-based TIM (thermal conductivity between 0.8 and 1.2 W/m-K) to bond a HOPG heat spreader to bare chips. The superior thermal properties of HOPG are not fully exploited because the material and processes used to bond the HOPG to the chip can hinder heat flow. Consequently, new bonding approaches that minimize the thermal resistance between the heat spreader and the chip are needed, based on using materials that allow for the reduction of the BLT or that have high thermal conductivity after bonding and are compatible with current industrial methods.

In summary, this dissertation is motivated by the need for faster, more powerful, and miniaturized electronic devices, which demand the exploration of new materials and efficient thermal management. Challenges include the thermal properties of materials in power electronics and memristors, heat management in portable electronics using suitable heat spreaders, and choosing appropriate bonding materials for effective thermal interfaces in TIMs. Addressing these challenges will contribute to developing advanced electronic devices with improved performance and reliability.

1.4. OVERALL OBJECTIVE AND SCOPE OF THE DISSERTATION

This dissertation focuses on the thermal performance of thin films for emerging electronics in power electronics, memristors, and heat spreaders for the thermal management of mobile

devices. I used diverse experimental and fabrications methods, such as TDTR, FDTR, thermal transient measurements, and thermo-compression, among others, depending on the material to be studied, along with Finite-element-method (FEM) simulations and ML algorithms for a complete description of the thermal behavior of the materials. The document is organized in the following sequence. Chapter 2 summarizes the literature corresponding to all materials and methods pertaining to this dissertation. The contributions of this research are summarized at the end of this chapter. Chapter 3 describes all characterization methods employed to work with the materials subject of this work. Chapter 4 studies Ga_2O_3 using TDTR and the impact of its thickness and atomic scale defects on its thermal conductivity. Chapter 5 studies TiN and Ti_2AlN using FDTR and ML algorithms. Chapter 6 analyses the suitability of using h-BN or HOPG as a heat spreader on the backside of silicon chips, along with promising bonding techniques to attach HOPG heat spreaders to silicon chips. Chapter 7 presents the conclusion of the different sections of this research and recommends areas for future work.

CHAPTER 2: LITERATURE REVIEW

In this chapter, I provide a comprehensive literature review of the key research topics explored in this dissertation. The review begins with a synopsis of research papers discussing gallium oxide's thermal properties. Subsequently, the attention shifts towards the properties of titanium nitride and titanium aluminum nitride, specifically in the context of memristor electrodes. Next, I offer a brief description of Time-Domain Thermoreflectance (TDTR) and Frequency-Domain Thermoreflectance (FDTR), with a particular emphasis on the utilization of Machine Learning (ML) for the analysis of data derived from these experiments. The following section describes the properties of hexagonal Boron Nitride (h-BN) as heat spreaders, including the methodologies employed for transferring h-BN and measuring its thermal conductivity. The fifth section delineates the current status of materials and techniques employed for bonding Highly Oriented Pyrolytic Graphite (HOPG) to diverse substrates. The chapter ends with a compilation of my contributions.

2.1. THERMAL PROPERTIES OF GALLIUM OXIDE

This section is reproduced/adapted from Vaca, Diego, et al. "Measurements and numerical calculations of thermal conductivity to evaluate the quality of β -gallium oxide thin films grown on sapphire and silicon carbide by molecular beam epitaxy." *Applied Physics Letters* 121.4 (2022) [32], with the permission of AIP Publishing.

Future applications, such as power electronics for AC/DC conversion or faster wireless networks, will require devices with superior power density and power switching capabilities. To achieve this, semiconductors such as GaAs, SiC, and GaN are commercially available and are under development to broaden their applications. On the other hand, Ga₂O₃, an ultra-wide bandgap semiconductor, is expected to show superior properties when used for power-switching devices,

according to the Baliga figure of merit, which measures the power losses in switching devices [33]. In addition, wafers of Ga₂O₃ are available and can be fabricated with high-volume commercial techniques such as the Czocharlaski method or the edge-defined film-fed crystal growth. However, one of the limitations of using Ga₂O₃ in high-frequency and high-power switching applications is its lower thermal conductivity. The maximum reported bulk thermal conductivity of Ga₂O₃ at 300 °K is around 26 W/(m·K) in (010) direction [34, 35]. The low thermal conductivity can hinder the full potential of Ga₂O₃-based devices because high temperatures will accelerate the degradation of these devices [36, 37].

Recently, many studies focused on the electro-thermal transport in Ga₂O₃ transistors [38-42]. In the case of thin-film transistors, the layers of Ga₂O₃ can be obtained using two prime methods: mechanical exfoliation of the membranes or epitaxial growth on compatible substrates. In the case of exfoliation, devices with membrane thickness in the range of tens to hundreds of nm have been presented [43-45]. Even though many studies used mechanical exfoliation of Ga₂O₃ to fabricate devices, this process cannot be scaled for industrial production because it is neither possible to control the thickness nor the lateral dimension of the membranes. In addition, the membranes and the substrate are coupled by weak Van der Waals forces, which results in low thermal boundary conductance (TBC). In general, the TBC at the membrane interface that has been transferred to a substrate is one order of magnitude lower than the TBC between thin layers grown or deposited using physical/chemical methods on a substrate [21, 46]. For the devices with epitaxial-grown thin film layers [47-49], the thickness of layers was around 200 - 600 nm. The TBC at the interface of the Ga₂O₃ thin film and substrate will depend on the growth process followed. Most of the previous work focuses on analyzing the electrical characteristics of the

devices. However, only a handful of studies investigate the TBC at the interfaces of Ga₂O₃ thin films and the effect of interfaces on the thermal conductivity of thin films [21, 23].

There are multiple methods for the epitaxial growth of Ga₂O₃ thin layers, such as low-pressure chemical vapor deposition (LPCVD), metal-organic chemical vapor deposition (MOCVD), metal-organic chemical vapor phase epitaxy (MOVPE), molecular beam epitaxy (MBE), among others. [19]. The growth of Ga₂O₃ thin films on high thermal conductivity foreign substrates can provide a pathway for developing high-power devices. An interesting alternative for heteroepitaxy growth of Ga₂O₃ thin layers is the homoepitaxy growth on a Ga₂O₃-on-SiC composite wafer [50]. LPCVD and MOCVD require less expensive equipment and can have higher growth rates. The choice of growth method influences the thermal conductivity of Ga₂O₃ thin layers and the TBC at their interfaces because different growth methods can create different types and concentrations of defects. For example, Song et al. [51] showed that there is a tradeoff between the quality of Ga₂O₃ grown on c-plane sapphire using MOVPE and the TBC. Samples grown on 6° off cut c-plane sapphire had higher thermal conductivity (10-30%) but lower TBC than those grown on 0° off cut c-plane sapphire. Sapphire has relatively lower thermal conductivity (~ 30 W/m-K), and epitaxial growth on high conductivity substrates like SiC is highly desired. Even if the quality of Ga₂O₃ on SiC is lower than the other substrates, the thermal performance of this combination can be superior because the thermal conductivity of 4H-SiC is ~ ten times higher than sapphire. MBE can be used for the heteroepitaxy growth of Ga₂O₃ and investigation of the fabrication of thin films of Ga₂O₃ on SiC.

An important aspect of analyzing Ga₂O₃ grown on foreign substrates is how the polycrystalline nature of the material (grain size), along with the formation of point defects (vacancies) and linear defects (dislocations), will affect its thermal conductivity. The influence of

vacancies in the crystal lattice of Ga_2O_3 on its thermal conductivity has been studied by incorporating the defect-induced phonon scattering rate into the solution of the Boltzmann Transport Equation (BTE) [52] and the molecular dynamic simulations [53]. However, neither the influence of linear defects nor the mean grain size of polycrystalline Ga_2O_3 has been considered in the previous studies along with vacancies.

2.2. ALTERNATIVE MATERIALS FOR MEMRISTOR'S ELECTRODES

In 1971, Leon Chua was the first researcher to predict the existence of a fourth fundamental circuit element (other than a resistor, a capacitor, and an inductor), the memristor, which means "memory resistor" [54]. In contrast, the first demonstration was presented in 2008 [55]. The resistance of a memristor can reversibly switch from a low-resistance state to a high-resistance state. Digital computers could use these characteristics to represent the on-and-off states required for their functioning [56]. Memristors are simple devices usually made of a top electrode, a resistive switching (RS) layer, and a bottom electrode. There are different switching mechanisms (for a review of all mechanisms, check [57, 58]). However, the most widely studied is the growth and fracture of conductive filaments, mainly divided into metal-ion filaments and vacancy filaments [59]. In the metal-ion filament formation case, conductive ions migrate from the top electrode and form a conductive filament that joins the top and bottom electrodes. On the other hand, in the vacancy filament formation case, defects in the lattice, such as oxygen vacancies, act as conductive particles [56]. In any case, Joule heating partially drives the formation of the conductive filament [56, 60]. Hence, the thermal properties of the materials used in memristors are important.

The following discussion on the materials for the RS layer is based on [56]. Researchers have tested different materials for the RS layer, which can be classified as oxide, 2D materials,

ferroelectrics, solid electrolytes, and other materials. Oxides such as titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), zinc oxide (ZnO), and hafnium oxide (HfO_2), among others, are the most commonly used materials for RS layers in memristors. The RS mechanism in oxides can vary depending on the electrodes and RS layers, such as oxygen vacancy accumulation or metal ion redox reactions. 2D materials have become the focus of research in various fields due to their advantages, such as excellent electrical, optical, thermal, and mechanical properties. The application of 2D materials in the field of functional materials and structural materials has shown great potential. Materials tested for the RS layer include graphene, h-BN, black phosphorus, and transition metal dichalcogenides (TMDs) such as WSe_2 and MoS_2 . The third type of material is ferroelectrics. Ferroelectrics have a spontaneous polarization that can be reversed by an external electric field, making them suitable for use in memristors. Some ferroelectrics tested include $\text{Pb}(\text{ZrTi})\text{O}_3$ (PZT), and BiFeO_3 . The next type of material is solid electrolytes. Solid electrolytes have high ionic conductivity and can create memristors with low power consumption. Some examples of solid electrolytes suitable for the RS layer are Ag_2S , Cu_2S , and Cu_2Se . In addition, other less-reported materials for the RS layer include organic materials (Cu-TCNQ , chitosan) and magnetic tunnel junction (MgO), among others.

The material for the electrode (for the oxide-based memristors) is commonly a metal. The literature reports using metals such as titanium, nickel, copper, silver, gold, and more. It is worthwhile that some nitrides (TiN) are also used for the electrodes [61]. Several reports have reported the influence of the materials chosen for the electrodes on the performance of memristors [62-64]. Some factors influenced by the electrode material include the contact resistance between the electrode and the RS layer, filament formation, dissolution kinetics, stability, and switching voltage and current levels.

Given that Joule heating influences the formation and the dissolution of the conductive filament [65, 66], another factor that impacts the memristors performance is the thermal conductivity of the material. The influence of the thermal conductivity of the substrate [25, 26], the RS layer [67], and both [27] have been presented. The researchers found that the thermal properties of the materials used in the memristor affect the reset voltage, endurance, low switching current, the memory window, the on-state to off-state conductance, the operation energy, and more. The selection of the materials for memristors must include careful thermal design engineering to enhance the performance of memristors.

In this sense, using TiN as the material for the memristors' bottom electrode (for certain RS layers such as hafnium oxide [62]) can be beneficial. The thermal conductivity of TiN is one order of magnitude lower than most of the metals tested as electrodes. On the other hand, MAX phases are a class of materials that could be used as memristors' electrodes. MAX phases are a family of ternary compounds uniquely combining metallic and ceramic properties. The name "MAX" is derived from the first letter of each constituent element: M for a transition metal, A for an element from groups 13 to 14, and X for carbon or nitrogen. The general formula for MAX phases is $M_{n+1}AX_n$, where $n = 1, 2, \text{ or } 3$ [68]. Over 70 MAX phases have been discovered and reported in the literature. Some MAX phases are Ti_3SiC_2 , Ti_3AlC_2 , Ti_3GeC_2 , V_2AlC , V_2GeC , Ti_2AlN , and more. In the context of electrode materials for memristors, MAX Phases are good electrical conductors (resistivity between ~ 0.2 and $\sim 2.5 \mu\Omega\cdot m$ at room temperature, which is around one order of magnitude higher than most metals), and their thermal conductivity is between 12 to 60 W/m-K (one order of magnitude lower than most metals), which makes them attractive for this application.

2.3. TDTR, FDTR, AND ML FOR DATA ANALYSIS

The following description of TDTR and FDTR is based on [9]. The laser-based time-domain thermorefectance (TDTR) and frequency-domain thermorefectance (FDTR) methods have emerged and advanced as highly dependable, robust, and flexible techniques for evaluating the thermal properties of various bulk materials and thin films, as well as characterizing the interfaces between them. TDTR and FDTR are methods used to investigate thermal properties by measuring thermorefectance, which refers to the change in reflection with temperature. Typically, a thin metal film that serves as a transducer coats the sample. This film's surface reflectance exhibits a linear change in response to temperature, especially when the temperature rise is relatively small. The fundamental implementation of these techniques involves a pump-probe setup. A pump laser pulse heats the sample, while a separate probe laser pulse measures the thermorefectance signal. In the case of TDTR, the time-domain thermorefectance signal is obtained by varying the time delay between the pump and probe pulses. On the contrary, FDTR evaluates the thermorefectance signal by varying the modulation frequency of the pump beam rather than observing the signal based on the delay between the arrival times of the pump and probe pulses. This approach simplifies the implementation of FDTR significantly, as it eliminates the need for a complex mechanical delay for time delay adjustment. Moreover, FDTR can utilize cost-effective continuous wave (CW) laser sources, making it more accessible and practical.

Regardless of the technique used, the experimental signal is analyzed to extract the thermal properties of the sample. Estimating thermal transport properties usually involves fine-tuning free parameters (representing the unknown thermal properties) within a thermal transport model. This iterative process aims to achieve the best possible agreement between the model's predictions and

the experimental data. The full description of the thermal transport model, its solution, and its implementation can be found elsewhere [69, 70].

The fitting of the observed data to a theoretical model generally requires using least squares fitting. In these models, unknown and known parameters are fitted to a theoretical model function, minimizing the difference from the observed data. However, if the initial starting point to begin the iterative fitting process is not good enough, difference minimization methods, such as Levenberg-Marquardt [71, 72] and trust-region techniques [73], can sometimes get stuck in local minima, despite their aim to find the global minimum. The reliability of FDTR and TDTR methods is estimated by measuring the uncertainty of the values obtained from the experiments, which is strongly linked to parameter sensitivity. This sensitivity, affected by factors such as modulation frequency, beam spot size, transducer thickness, and material properties, influences the level of uncertainty, mainly when dealing with low-sensitivity parameters. The uncertainty in these methods can be assessed through analytical methods [74] and Monte Carlo simulations [75]. Analytical methods, while fast, depend on accurate parameters, whereas Monte Carlo simulations can handle unknown parameters, albeit at a high computational cost and the need for a robust fitting approach.

On the other hand, heat transfer problems, whether they involve fundamental studies or large-scale systems, often present complex nonlinear challenges that are difficult to solve using traditional methods, even with advancements in computing power. For this reason, ML has gained popularity in heat transfer engineering. With artificial intelligence and computer hardware advancements, sophisticated ML algorithms have emerged. These algorithms enable computers to model and solve problems without explicit instructions on the solution approach. ML has the

potential to enhance researchers' and engineers' understanding of heat transfer phenomena, as well as improve system design and optimization [76].

Three main categories of machine learning approaches are supervised, unsupervised, and reinforcement learning [77]. Examples of all categories can be found in the mechanical engineering-related literature. Supervised learning resembles standard nonlinear regression models or curve-fitting. In this approach, the model receives inputs along with corresponding desired outputs (labeled data), and the objective is to find a set of parameters that accurately map the inputs to the outputs. The quality of this mapping is determined by selecting an appropriate error metric. Some examples of this approach are in [78, 79]. In the second place, unsupervised learning occurs when the model is not provided with any labeled data, and the algorithm aims to discover the underlying structure of the data independently. Applications of unsupervised learning were presented in [80, 81]. Finally, unlike supervised learning, reinforced learning algorithms do not receive a pre-labeled dataset. Instead, they actively gather information by acting and interacting with the environment. Then, before acting, the algorithm receives two forms of information: the current state of the environment and a reward value specific to the task and its associated objective. Researchers in [82, 83] presented applications of reinforcement learning related to heat transfer problems.

Most of the ML applications in heat transfer use supervised learning algorithms. Researchers in [76] summarized and described the main supervised learning algorithms. In the field of FDTR and TDTR, only a handful of researchers have applied supervised learning approaches to estimate the thermal properties of materials. In the first place, Shen et al. [10] explored the application of frequency- FDTR in probing the thermal characteristics of bulk and thin film materials. The authors emphasize that the uncertainties involved in the FDTR traditional

data analysis originate from an inaccurate selection of the initial guess for the iterative fitting. The authors introduce a new data analysis method integrating deep learning and traditional fitting algorithms to mitigate these uncertainties. The deep learning model developed can predict thermal conductivity, volumetric heat capacity, and thermal boundary conductance (three parameters) with an average error of less than 5% for coated bulk samples. In the second place, Pang et al. [11] constructed universally applicable ML models to facilitate efficient and high-volume data processing in TDTR measurements. These models can concurrently extract thermal conductivity and interface thermal conductance (two properties) from isotropic bulk materials such as silica, sapphire, silicon, and silicon carbide, and in-plane, out-of-plane thermal conductivities and interface thermal conductance (three properties) from anisotropic bulk pyrolytic graphite. Despite the authors stating that ML models possess sufficient sophistication and power to discern even the most minor characteristics of experimental signals, enabling the simultaneous extraction of multiple parameters (more than three) from a single measurement, this idea has yet to be proven. In the third place, Xiang et al. [84] introduced a method for determining depth-dependent thermal conductivities using TDTR and FDTR combined with machine learning techniques. The demonstration shows that kernel ridge regression, a supervised-learning algorithm, can reconstruct the thermal conductivity profile without needing pre-existing knowledge about the profile's functional form. In summary, these works show that adequately trained machine learning algorithms could be effective assistants in treating experimental data originated by pump-probe techniques.

2.4. h-BN THERMAL PROPERTIES AND ITS TRANSFER METHODS

2.1.1. h-BN thermal properties.

As mentioned in the introduction, there is a growing interest in using h-BN as a heat spreader for the thermal management of microelectronics. Researchers have studied two types of heat spreaders: ultra-thin heat spreaders made of large area (i.e., fabricated by CVD) mono or multilayered h-BN [17, 29, 85, 86], and thicker (μm scale) heat spreaders that use h-BN flakes (i.e., exfoliated from bulk h-BN) in a solution that is deposited on a hot spot, or as part of a composite with polymer binders [87-92]. This dissertation will focus on the first type of heat spreader.

The h-BN thermal conductivity presented in experimental reports widely varies and depends on the fabrication, measurement, and transfer methods. Table 2.1 summarizes some of the experimental values.

Table 2.1. Experimental reports of in-plane thermal conductivity of h-BN

Thickness	Fabrication method	Measurement method	Suspended or supported	Thermal conductivity (W/m-K)	Reference
4-layer	CVD	Frequency Domain magneto-optical Kerr effect	Supported	242	[93]
1-layer	Exfoliation	Raman Thermometry	Suspended	751	[15]
1-layer	CVD	Raman Thermometry	Suspended	544.6	[18]
15 μm	Exfoliation	Time Domain Thermo reflectance	Supported	550	[94]
77 nm	Atmospheric pressure CVD	Heat spreader method	Supported	77.4	[17]

2.1.2. *h*-BN transfer methods

The preferred fabrication method of large-area *h*-BN is CVD, which requires a metallic substrate (usually copper or nickel) that works as a catalyzer. Consequently, the *h*-BN must be transferred from the metallic substrate to the surface of the chip. This transferring process has four parts: protecting the *h*-BN with a "handling layer" deposited on top, separating the handling layer/*h*-BN stack from the metal substrate, transferring the stack to the desired substrate, and removing the handling layer. The main challenges of this process include the proper selection of the material for the handling layer so that it leaves as few residues as possible that can affect the thermal properties of the transferred *h*-BN and the delamination process that produces the least damage to the heat spreaders. Since most transfer methods have been developed and tested on graphene (and adopted for *h*-BN), the rest of this section will refer to graphene and *h*-BN as 2D materials.

Handling layers.

The first step when transferring a CVD-grown 2D material from its metal substrate to the desired substrate is depositing on top of it a thin layer (~ 100 nm) that gives it structural support. The material that is widely tested for this purpose is Polymethyl methacrylate (PMMA). Nevertheless, other polymers that can be removed more easily than PMMA have been reported. Finally, researchers have tested other materials, such as metals and metal oxides.

PMMA is the most popular supporting material for handling 2D materials. A solution of PMMA is prepared by dissolving the solid polymer with the appropriate solvent (acetone, for example) and spin-coated on the 2D material. After that, the stack is baked to remove the excess solvent and solidify the layer. However, because of the large adsorption energy with the surface (especially with graphene) and the low solubility with solvents, PMMA leaves residues that affect

the properties of the 2D material. Techniques to entirely remove PMMA have not been fully successful and include annealing at high temperatures (200 °C to 1050 °C) [95-97] under different atmospheres (vacuum, Ar/H₂, O₂) [98].

Because of the high temperatures needed to remove PMMA, the use of other polymers has been reported in the literature and compared with PMMA-based procedures. In general, the reports indicate that using alternative polymers requires more benign removal conditions. The properties of the 2D materials are superior to when they were transferred using PMMA if the PMMA is not removed with very high annealing temperatures. A selection of alternative polymers is presented in Table 2.2.

Table 2.2. Polymers used in handling layers for 2D materials transfer

<i>Polymer</i>	<i>Solvent</i>	<i>Removal conditions</i>	<i>Reference</i>
Formvar	Chloroform	Room temperature	[99]
Rosin	Acetone	Room temperature	[100]
Poly-vinyl alcohol	Deionized Water	Room temperature	[101]
Poly(bisphenol A carbonate)	Chloroform	Room temperature	[98]
Paraffin	Hexane	Room temperature	[102]
Thermal release tape	None	Heating @ 120 °C	[103]

Some studies have used a protective layer before depositing the polymer layer to avoid contamination of 2D materials with polymers. If graphene is intended to fabricate transistors, researchers in [104, 105] used an Al₂O₃ layer that could work as a dielectric and protect the graphene from the polymer. Because the Al₂O₃ layer protects the graphene, more aggressive conditions to remove the polymer could be used. In this case, the protective layer remains attached to graphene. On the other hand, few studies have used Ni or Co layers [106] that were removed after the transfer and MoO₃ [107], which is soluble in water.

Delamination methods

After the deposition of the handling layer, the 2D material must be detached from the metal substrate. The preferred method is the dissolution of the metallic substrate. However, other methods that attempt to preserve the substrate for future 2D material growth have been reported.

Oxide-assisted delamination consists of exposing the 2D material to water (either vapor or liquid) to promote the formation of a thin metal oxide layer (copper oxide, for example) between the 2D material and the substrate [101, 108, 109]. This exposition usually lasts 24 hours. Then, the 2D material is pulled from the substrate because the oxide layer facilitates the separation. It has been reported that this method worked well for graphene but not for h-BN [101].

Mechanical delamination is known as the dry-transfer method. The 2D material is peeled off from the substrate because the adhesion force at the interface of the handling layer/2D material is stronger than that at the 2D material/substrate. Two approaches have been reported: using Van der Waals forces between two different 2D materials (using an h-BN stamp to transfer graphene, for example) [110, 111] and using a metal layer as part of the handling stack [106].

In electrochemical delamination (bubble transfer), the stack polymer/2D material/metal substrate is used as an electrode in an electrochemical cell [112-114]. When the electrochemical cell works, H₂ bubbles form at the 2D material/substrate interface and separate them. It has been reported that the process is fast, but the conditions must be carefully controlled to avoid the mechanical damage that the bubbles could cause to the 2D material.

Finally, etching the substrate is the most common method to separate the 2D material and the substrate. The most common substrates used in CVD-grown 2D materials are Cu and Ni, and they are etched, exposing the stack to appropriate etchants such as ammonium persulfate [115] or hydrochloric acid [17], respectively. In addition, to control the damages that the random etching

process could cause, previous studies have conducted controlled etching processes in the electrochemical cells, leading to under-etching delamination [116] and directional etching [117].

2.5. HOPG AS A HEAT SPREADER AND ITS BONDING METHODS

As smartphones and tablets continue to become thinner and more powerful because of the consumer's demand for devices with better performance and durability, they often incorporate high-performance chips with power usage reaching 6W [118]. In addition, the expected power density of typical hot spots in silicon microprocessors can be 150 to 350 W/m² [12, 13]. As these devices slim down further, managing heat dissipation becomes increasingly vital due to their compact size and the absence of active cooling. Given the space limitations, various studies have proposed solutions such as thermoelectric coolers [119], piezoelectric coolers [120], phase change cooling [121], micro heat pipes [122], and heat spreaders [123] for the thermal management of microprocessors used in mobile devices.

For heat spreaders to function effectively, they need to be made from materials with high thermal conductivity, such as metals (e.g., copper) or 2D materials (e.g., graphene or hexagonal boron nitride). Both graphene and hexagonal boron nitride (h-BN) have gained attention for their thermal management capabilities in electronics because of their high thermal conductivity in the basal plane (parallel to the layers) [14, 15]. Despite the advantages, a few drawbacks are associated with using 2D materials for thermal management, such as the thickness of the commercially available multilayered 2D materials (thickness does not exceed 10 nm [124]), higher cost than alternative materials, and the availability and scalability of 2D materials for large-scale applications.

An alternative to 2D materials is highly oriented pyrolytic graphite (HOPG). HOPG is a unique form of graphite that exhibits a high degree of crystalline alignment along a specific axis.

HOPG consists of multiple graphene layers stacked together. The basal plane of HOPG exhibits excellent thermal and electrical conductivity. Due to its high thermal conductivity, anisotropic properties, and availability in different thicknesses relevant to micro-electronics thermal management, HOPG is utilized as a heat spreader to dissipate heat from electronic components and high-power devices [31, 123, 125-127].

In addition to the heat spreader material, the other key factor in thermal management is the thermal interface material (TIM) used to bond the heat spreader with the chip. Commonly, heat dissipation systems in electronics use TIMs like silicone grease, silicone grease pads, or thermal gel to establish contact between the heat spreader and the surface of the chip. Standard TIMs are typically composed of polymers whose thermal conductivity is low. For example, the thermal conductivity for a typical epoxy TIM is 1.2 W/m-K [128]. The typical bond line thickness (BLT) for this type of material is between ~ 50 and ~ 150 μm [129, 130]. To increase the thermal conductivity of polymer-based TIMs, they have been filled with inorganic fillers such as metal nanoparticles and boron nitride, among others. However, the high thermal conductivity filler particles are isolated by very low thermal conductivity polymers, leading to an overall thermal conductivity of under 5 W/m-K [131]. Another problem with using fillers is that the flowability of the TIM decreases when more fillers are added, which increases the BLT and the overall thermal resistance [129]. Despite their low thermal conductivity, using highly flowable polymers (to fill the air gaps present between the silicon chip and the heat spreader) whose BLT can be reduced could be one feasible option. For example, polymers such as BCB [132] or CYTOP have been tested as bonding materials at low temperatures [133, 134]. CYTOP has the advantage that the BLT can be manipulated by tuning the dilution ratio and the parameters employed during its deposition

using spin coating. In summary, controlling the BLT of the bonding layer is as important as controlling the thermal conductivity of the TIM.

One technology that has gained renewed attention to bond large areas in the semiconductor industry (especially for power electronics) is using metal nanostructures (either particles or nanofoams) for thermo-compression. Nanostructures are advantageous because they can be low-temperature sintered, using temperatures lower than 250 °C. In addition, the nanostructures will recover much of the original high thermal conductivity expected for metals, allowing for a low-thermal resistance bonding. One of the options is the use of nanoscale metal particles in a polymer matrix. The typical BLT of this solution is between 25 and 50 μm [135]. On the other hand, using metal nanofoams does not require a polymer matrix. Recently, researchers in [136-138] have reviewed and proposed using nanoporous metals as interconnection materials in power electronics and microelectronics. This concept could be adapted to large-area heterogeneous integration of HOPG heat spreaders with different substrates [139, 140].

2.6. CONTRIBUTIONS OF THE RESEARCH

The significant contributions of this research are listed next:

- 1) I investigated the impact of thickness and atomic scale defects on the thermal conductivity of hetero-epitaxial grown $\beta\text{-Ga}_2\text{O}_3$ and the thermal boundary conductance (TBC) at the $\beta\text{-Ga}_2\text{O}_3/\text{SiC}$ interface. I used a combination of first principles simulations with experimental results to estimate the defects in $\beta\text{-Ga}_2\text{O}_3$ thin films.
- 2) I evaluated the advantages and limits of a deep learning-based data analysis method for estimating the thermal properties of thin films measured by FDTR. I tested the application of this tool for data analysis on thin films to estimate four parameters.

- 3) Using experiments and simulations, I studied the suitability of using h-BN as a heat spreader on the backside of microchips. I assessed the compatibility of transferring h-BN thin films to substrates with industrial processes and their benefits and limitations to be used as heat spreaders in portable electronics.
- 4) I developed a technique to bond thin-film HOPG heat spreaders on the backside of silicon substrates using CYTOP and nanoporous copper. Finally, I adapted a thermal transient measurement technique based on the JEDEC JESD51-14 standard to measure the junction-to-case thermal resistance of semiconductor devices with heat flow through a single path to estimate the thermal resistance of each bonding solution.

CHAPTER 3: METHODS

This chapter covers all characterization methods employed in this work. First, I present TDTR and FDTR employed to study β -Ga₂O₃ thin films and TiN and MAX Phase Ti₂AlN. Then, I describe the characterization methods to study h-BN. Finally, I present the thermal characterization methods used with HOPG, CYTOP, and NP-Cu.

3.1. TIME-DOMAIN AND FREQUENCY-DOMAIN THERMOREFLECTANCE

TDTR is an optical technique in which a modulated laser beam, called the pump, heats a sample's surface. Concurrently, an unmodulated beam, the probe, monitors the reflectivity changes of the surface. A thin metal film, typically around 100 nm, is deposited on the sample for two purposes: to convert the photons into thermal energy and act as a temperature transducer due to its reflectivity changes with temperature, enabling surface temperature rise measurement [141, 142]

The pump and probe beams typically hit the sample surface at a right angle. This method is mainly used to measure the through-plane thermal conductivity of the material. Nevertheless, alternative methods relying on variable beam sizes and shapes are used to measure the thermal conductivity of anisotropic materials. [143, 144].

The pump beam's modulation facilitates signal measurement via a lock-in amplifier. The probe beam, slightly delayed compared to the pump beam, tracks the decline of the thermoreflectance signal. A thermal model is fitted to the experimental data to deduce the desired thermal properties. The known sample properties inform the thermal model [69, 145], while unknown properties are treated as fitting variables.

In TDTR experiments, the pump beam's modulation generates a thermal wave heating the sample. The signal's amplitude and phase are measured using a lock-in amplifier. The thermal

penetration depth (l) depends on the modulation frequency (f) and the sample's thermal diffusivity (D). This dependence is described by $l = \sqrt{D/\pi f}$ [146].

The TDTR setup and the data interpretation [147] I used for this study were described in [69, 145, 148]. In short, the two-color system consists of a Spectra Physics Ti:Sapphire ($\lambda=800$ nm, 40 nJ/pulse) laser with ~ 150 fs pulse width and a repetition rate of ~ 80 MHz. The beam is split into a probe and a pump beam. The frequency modulation of the pump beam can be controlled by an electro-optical modulator, and its values are chosen depending on the sensitivity of the values of interest to this parameter (i.e., the most sensitive, the better), and the pump pulse frequency is doubled using a BiBO crystal. On the other hand, the probe beam enters a double-pass delay stage before merging its path again with the pump beam. A 10x objective lens focuses both collinear beams on the sample. The pump radius on the sample's surface was ~ 9.95 μm , while the probe radius was ~ 6.2 μm . The material properties needed to fit the data (i.e., thermal conductivity, density, and specific heat) were measured or taken from the previous studies (see bulk material properties section). The TDTR setup used in this work has available six filters that correspond to 1.2, 2.2, 3.6, 6.3, 8.8, and 11.6 MHz for the modulation frequency. I used all filters in the measurements (i.e., each sample has six data sets). Fig 3.1 presents a schematic of the TDTR system used for the measurements and a typical signal and data fitting curve.

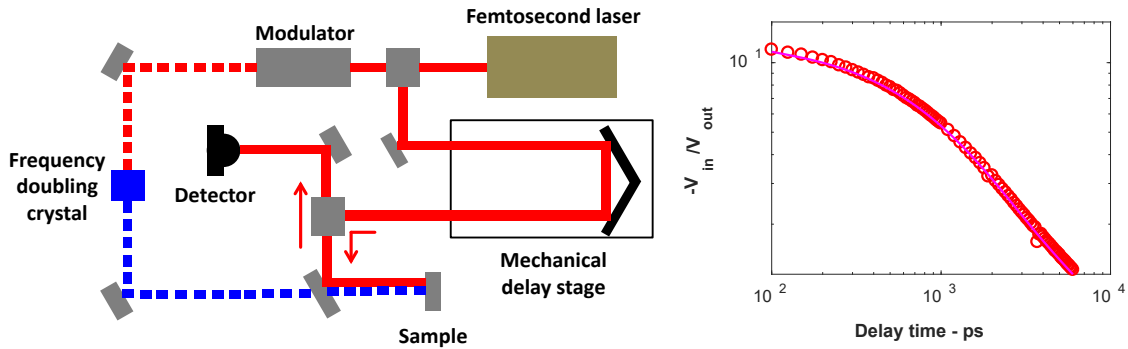


Fig. 3.1. Schematic of the TDTR system used to measure the thermal conductivity and the thermal boundary conductance (left), and typical TDTR signal and data fitting for Ga_2O_3 on SiC sample at a frequency of 3.6 MHz [147]. Copyright © 2020, IEEE

FDTR and TDTR both employ a modulated pump laser to heat the surface of a sample and use a probe beam to register the thermal response. The difference between the two methods is that FDTR collects thermal response data by altering the modulation frequency of the pump beam instead of changing the delay time via a mechanical stage. FDTR measurements can be conducted in numerous ways [70]. However, I used the setup that was implemented by Shen et al. [3]. This setup uses two continuous-wave (CW) lasers. One of these CW lasers, frequency-modulated, serves as the pump laser, while the other is used as the probe laser to detect the sample's thermal response. A photodiode-assisted lock-in amplifier captures the thermal signal. Using CW lasers is less expensive than a pulsed laser system. The methods employed to deal with several challenges for FDTR measurements, such as accurately extracting the signal's first harmonic and removing the errors in phase delay caused by cables, optics, and traveling paths, are presented in [3].

The description of the FDTR setup used in this work is adapted and reproduced from Shen, W. et al. "Temperature Dependent Thermal Properties of Thin Film Hafnium Oxide." *2023 22nd IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*. IEEE, 2023 [149]. Copyright © 2023, IEEE

The FDTR system I utilized in this work consist of a digitally modulated pump laser (488 nm) that delivers a periodic heat flux, whereas a continuous probe laser (520 nm) monitors the surface temperature variation. A lock-in amplifier (Zurich HF2LI) extracts the phase lag between the pump and probe lasers. I fitted the phase lag over a range of modulation frequencies to the theoretical model to derive parameters such as thermal conductivity and thermal boundary conductance. The lock-in amplifier in the system is equipped with a mixer of sinusoidal waves and can accurately extract the fundamental frequency signal or the first harmonic . As a result of the digital modulation of the modulated pump, the photo-diode detects a significant amount of high-order harmonic signal. It is necessary to extract the first harmonic of the signal since the fitting model only considers the first harmonic of periodic heating. Fig 3.2 presents a schematic of the FDTR system used for the measurements and a typical signal and data fitting curve.

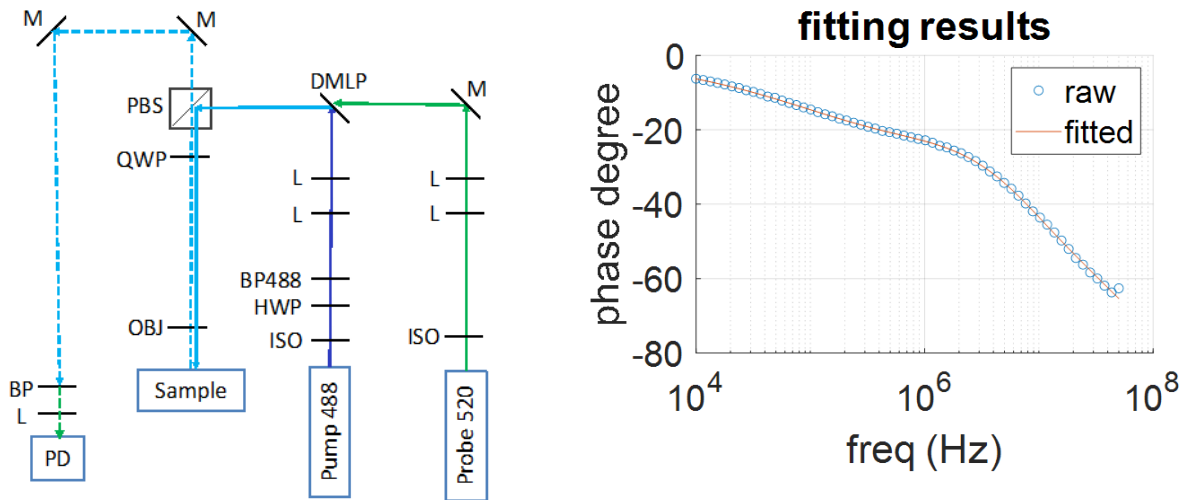


Fig. 3.2. Schematic of the FDTR system used to measure the thermal conductivity and the thermal boundary conductance (left). The acronyms M, PBS, HWP, QWP, L, ISO, PD, BP, DMLP, and OBJ stand for mirror, polarizing beam splitter, half-wave plate, quarter-wave plate, lens, isolator, photo-diode, bandpass filter, low pass dichroic mirror, and objective lens, respectively [149]. Typical FDTR signal and data fitting for Ti₂AlN-Cubic sample (right). Left figure - Copyright © 2023, IEEE

3.2. HOPG MECHANICAL TESTING

I used a commercial bond tester to compare the shear strength of the CYTOP and metallurgical bonding. However, before performing the experiment, I had to bond HOPG to Si substrates. For this purpose, I diced 5 x 5 mm² Si samples. Then, I coated the Si samples with 100 nm of Ti and 150 nm of Au or Cu, respectively. On the other hand, I coated HOPG with 100 nm of Ti and 500 nm of Au or Cu. I used electron-beam evaporation in both cases.

I bonded Au-Au and Cu-Cu using a manual flip chip bonder (by Finetech), placing the HOPG on the heating base, whereas the tool head picked the Si. In the case of Au-Au bonding, I applied ~80 newtons (~ 3.2 MPa for a 5 x 5 mm² sample) for 10 minutes at temperatures of 300, 350, and 400 °C. Before Cu-Cu bonding, I immersed the samples in formic acid to remove the native copper oxide. I bonded under a controlled atmosphere in a chamber with forming gas (5% hydrogen in nitrogen). I applied the same load and temperatures used for Au-Au bonding for Cu-Cu bonding, but I increased the time to 20 minutes. For the case of CYTOP, the details will be presented in Chapter 6.

Finally, I assessed the bonding quality of Au-Au, Cu-Cu, and CYTOP 5 x 5 mm² samples using a standard shear test with a Xyztec bond tester, using the following parameters: 1500 μm at 100 μm/second using a shear height of 50 μm. I attached the HOPG/Si stack to a FR4 substrate (HOPG side) with super glue. Fig 3.3. shows a schematic of the stack. After the shear test, I analyzed the morphology of both sides (Si side and HOPG side) using optical microscopy, scanning electron microscopy (SEM), and energy-dispersive X-ray spectroscopy (EDX) for the chemical analysis.

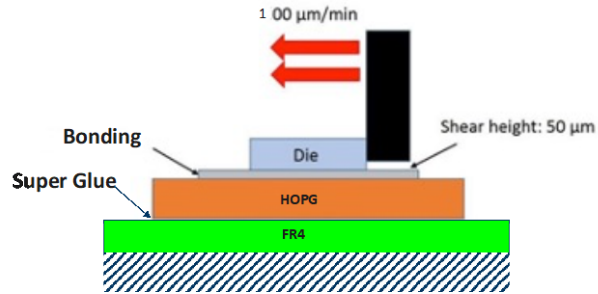


Fig. 3.3. Diagram of the shear tests performed on bonded HOPG.

3.3. A TRANSIENT THERMAL METHOD BASED ON THE JEDEC JESD51-14 STANDARD TO ESTIMATE THE THERMAL RESISTANCE OF THE BONDED MATERIALS

The thermal transient measurement method is typically employed to determine the thermal resistance of the package of semiconductor devices. The method consists of applying a pulsed heating current to the device and monitoring the transient changes of a temperature-sensitive parameter (TSP) while the device cools down (e.g., the forward voltage of a diode exhibits temperature-dependent variations). Once the transient temperature data is obtained, it is interpreted using the Cauder-ladder network model. This model correlates specific regions within the device package with parts of a thermal network model [150]. The behavior described by the model allows for identifying the heat flow paths (the central assumption is that there is a 1D heat flow from the junction to the heat sink) using a mathematical technique known as "structure functions." Structure functions are mathematical representations of the system's distributed (thermal) RC network impedances. Fig 3.4. presents a typical structure function plot with the equivalent thermal RC network.

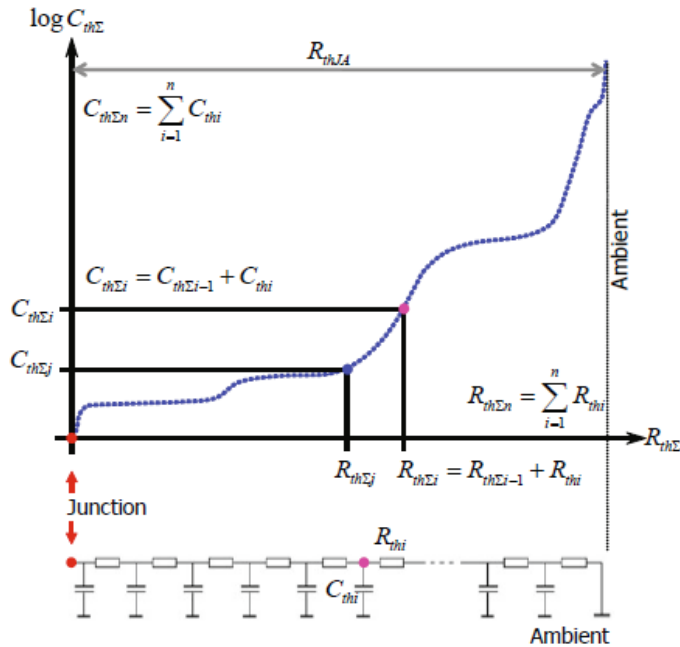


Fig. 3.4. Cumulative structure-function: the graphic representation of the thermal RC equivalent. Reproduced with permission from Springer Nature from Lasance, Clemens JM, and András Poppe, eds. *Thermal management for LED applications*. Vol. 2. New York: Springer, 2014 [150].

Using the structure functions to determine the thermal resistances along the heat flow path requires the joint analysis of the cumulative and differential structure functions [151-154]. More details on the method can be found in [150]. However, determining slope changes in the plots (indicating a new thermal resistance) might require some effort. To facilitate the analysis of the structure functions and determine the thermal resistance of each layer of the sample, I adapted the dual interface measurement principle stated in the JEDEC JESD51-14 standard for the measurement of the junction-to-case thermal resistance of semiconductor devices with heat flow through a single path. I conducted two transient measurements on the same power semiconductor device, and in both cases, the device must be in contact with a temperature-controlled heatsink. In the first measurement, no additional interface material exists between the device under test (DUT) and the cold plate. In the second measurement, I added bonding tape at the interface. The presence of additional material results in an increased interface resistance. This increased resistance ensures

a clear distinction between the measured transient curves at a particular time. The two curves diverge when the heat flow enters the additional interface layer, indicating thermal resistance. The separation point is identified by checking the difference between the derivatives of the experimental Zth curves (Zth curves are the normalized temperature variation to time) and the structure functions. More information on the method can be found in [155, 156].

I used the Simcenter Microed Powertester by Siemens to perform thermal tests on the samples. The equipment measures packaged semiconductor devices' real-time heating and cooling curves. I used that information in the Simcenter 3D Solutions software to obtain the structure functions and compare them. For the experiments, I applied a heating current of 10 A for 60 seconds and allowed the devices to cool down for 90 seconds. I kept the heat sink temperature at 25 °C, and applied a ~500 N force on top of the DUTs to keep the environmental conditions as stable as possible during all tests.

CHAPTER 4: MEASUREMENTS AND NUMERICAL CALCULATIONS OF THERMAL CONDUCTIVITY TO EVALUATE THE QUALITY OF β -GALLIUM OXIDE THIN FILMS GROWN ON SAPPHIRE AND SILICON CARBIDE BY MOLECULAR BEAM EPITAXY

This chapter presents the results used to evaluate the quality of β -Ga₂O₃ thin films by measurements and numerical calculations of its thermal conductivity [32].

4.1. INTRODUCTION

In this work, I present results on measuring the cross-plane thermal conductivity of β -Ga₂O₃ and TBC at its interfaces for films grown on c-sapphire and 4H-SiC substrates using MBE [147]. I compared the measured values with theoretical results and used this comparison to estimate the defect densities (vacancies and dislocations) that might have been created during growth. I performed the measurements using time-domain thermoreflectance (TDTR). In contrast, I used the iterative solution of the Boltzmann Transport Equation (BTE) to estimate the variation of the thermal conductivity with film thickness and the effect of defects on thermal conductivity. In order to make these estimations, I used the grain size of Ga₂O₃ measured using AFM and the linear defect density using TEM as input to the BTE simulations. The percentage of point defects is one variable that is not easy to measure, and I estimated that by comparing experimental and numerical results. In summary, I propose a method to study the effects of the different defects on the thermal conductivity of epitaxially grown Ga₂O₃, which can also be employed to study other materials. Finally, the diffuse mismatch model (DMM) was used to predict the TBC and better explain the experimental results.

4.2. DESCRIPTION OF THE Ga₂O₃ SAMPLES

Two thin films of undoped Ga₂O₃ were grown on c-sapphire and 4H-SiC by MBE at the U.S. Naval Research Laboratory (NRL). MBE is a physical-vapor epitaxial growth process in high vacuum. For Ga₂O₃ epitaxy, ultra-high pure elemental Ga and reactive oxygen were provided using

Ga effusion cell and oxygen plasma, respectively [157]. The optimized conditions used to grow Ga₂O₃ on sapphire and SiC, along with the characterization of the films, have been published in [147, 157]. More details about the growth of Ga₂O₃ by MBE can be found in [158]. Also, I used bulk samples of the substrates to measure their thermal conductivities. In both cases (bulk and thin-film samples), I deposited a thin Al transducer (97 nm and 93 nm, for bulk and thin-film samples, respectively) by e-beam evaporation. I performed the TDTR measurements using a Ti:Sapphire laser (wavelength=800 nm). The frequency modulation of the pump beam can be controlled by an electro-optical modulator and is doubled using a BiBO crystal. The pump radius on the sample's surface was ~9.95 μm, while the probe radius was ~6.2 μm. Based on the sensitivity analysis, the data obtained at modulation frequencies of 8.8 and 11.6 MHz were used for the samples grown on sapphire and SiC, respectively. Appendix A has more details of the TDTR system.

High-Resolution Transmission Electron Microscopy (HRTEM) performed on both samples revealed a thickness of 119.4 ± 2.8 and 81.3 ± 1.3 nm for Ga₂O₃ on c-sapphire and 4H-SiC substrates, respectively (see Figs. 1a and 1d). In addition, the thickness of the Ga₂O₃ layers was measured by spectroscopic ellipsometry and X-ray reflectometry (XRR). Both HRTEM and X-Ray diffraction (XRD) measurements, performed by NRL, showed β-Ga₂O₃ of orientation (-201) for both samples. Details of the structural characterization can be found in [157]. A bright-field low- and high-resolution phase contrast TEM imaging, selected area electron diffraction (SAED) imaging, and post-imaging analysis using Fast Fourier transform (FFT) show that Ga₂O₃ thin films on sapphire and 4H-SiC substrate have a crystalline structure (Figs. 4.1a to 4.1g). Defect analysis using images of phase contrast and inverse FFT lattice images revealed that both samples have 1-dimensional defects (dislocations) and zero-dimensional defects. In brief, several TEM

images are processed using the FFT to identify the regions of interest, and images of those regions are converted back using the inverse FFT. Then, the linear defects are counted, and this number is divided by the area of the region of interest. More details on the method to estimate defect density can be found in [159]. In this case, the defect density was $2.5 \times 10^{12} \text{ cm}^{-2}$ and $1.0 \times 10^{12} \text{ cm}^{-2}$ (taken from [157] as they correspond to the same sample) for the $\text{Ga}_2\text{O}_3/\text{Al}_2\text{O}_3$ and $\text{Ga}_2\text{O}_3/\text{SiC}$, respectively. The TDTR setup and the data interpretation for this study have been described in [69, 148].

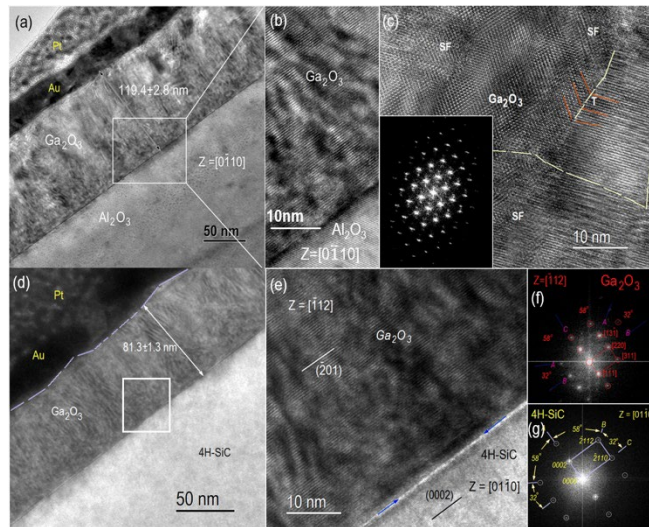


Fig. 4.1. A bright-field low- and high- resolution TEM micrographs showing (a-c) Ga_2O_3 on sapphire substrate with a thickness of ~ 119.4 nm. The presence of the lattice fringes as well as FFT reflections (inset) suggests crystalline structure. There exists lattice strain field across the HRTEM micrograph. (c) HRTEM micrograph obtained from a specimen rotated normal to the substrates $Z= [01\bar{1}0]$ direction reveal a crystalline structure decorated with high density of 1-D defects like stacking faults and twinning dislocations within the film which are indicated by SF and T, respectively. (d) bright-field TEM show ~ 81 nm thick $\text{Ga}_2\text{O}_3/\text{SiC}$. In addition, (e) HRTEM and (f and g) FFT of the film and substrate show lattice fringe real images and respective low-order diffraction reflection demonstrating crystallinity in structure of Ga_2O_3 film.

I used Atomic Force Microscopy (AFM) to scan the samples' top surface and analyze the presence of lateral grains (Fig. 4.2). These measurements revealed that the samples are

polycrystalline with a mean lateral grain size of 52 nm. I obtained this value using the intercept technique. In this technique, several random lines are drawn on the micrograph and the number of grain boundaries intersecting the lines is counted. Then, the average grain size is calculated by dividing the line length by the number of grain boundaries. I repeated this procedure for ten lines to have a representative value for the micrography. It is worth mentioning that I obtained Fig. 4.2 using the “phase” signal because this signal allows for a better contrast image that reveals the presence of grain boundaries, as opposed to the AFM image presented in [157], which used the “topographic (height)” signal, which is more suitable to measure the roughness of the sample.

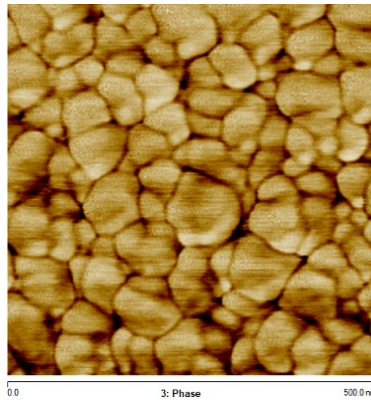


Fig. 4.2. AFM image of the surface of a β -Ga₂O₃ sample grown on SiC for this work. The mean lateral grain size is 52 nm. The field of view of the image is 500 x 500 nm²

4.3. THEORETICAL CALCULATIONS

I performed this part of the research with Matthew Barry, a former student in our group. He performed the Density functional theory calculations, and I provided the equations and experimental information for the scattering rates calculations. Density functional theory (DFT) calculations in conjunction with Boltzmann Transport Equations were used for the estimation of phonon relaxation time and thermal conductivity of Ga₂O₃ [160]. DFT calculations were performed using the Vienna *ab initio* simulation package (VASP) to compute the interatomic force constants (IFCs) of Ga₂O₃. A plane-wave basis set and the projector augmented-wave (PAW)

method were used with the Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional [161-164]. A 500 eV kinetic energy cutoff was used to optimize the structure and calculate the second-order harmonic and third-order anharmonic force constants. The convergence criteria for the energy and force were 10^{-9} eV and -0.001 eV/Å, respectively. The 20-atom β -Ga₂O₃ unit cell was optimized using a $4 \times 16 \times 8$ grid for Brillouin zone sampling. The optimized lattice parameters were $a = 12.45$ Å, $b = 3.08$ Å, and $c = 5.86$ Å, with $\beta = 103.76^\circ$, which are in good agreement with recent computational [52] and experimental results [165]. The second-order harmonic and third-order anharmonic IFCs were calculated using the finite displacement method with a $1 \times 4 \times 2$ supercell of the optimized 20-atom unit cell [166]. The finite displacement distance was 0.01 Å, and a 4th nearest neighbor cutoff was used for computing the third-order IFCs. Using the second- and third-order IFCs, the phonon relaxation times and the anisotropic thermal conductivities of bulk β -Ga₂O₃ were calculated using Fermi's golden rule [167] with the iterative solution to the BTE [168, 169]. A $5 \times 17 \times 9$ k-space sampling mesh was used for Brillouin zone sampling.

After calculating the IFCs, the linearized form of the BTE were solved using ShengBTE to obtain the thermal conductivity tensor(see Appendix A for details). The combined effects of sample size [170], oxygen or gallium vacancies, grain boundaries, and linear defects on the thermal conductivity were considered by adding the phonon boundary scattering rate, the vacancies-induced scattering rate, the grain boundary scattering rate, and the linear defect scattering rate (dislocations), respectively, to the anharmonic phonon scattering rate [171], according to the Matthiessen's rule:

$$1/\tau = 1/\tau_{anh} + 1/\tau_b + 1/\tau_v + 1/\tau_{gb} + 1/\tau_{ld} \quad (4.1)$$

Here $1/\tau_{\text{anh}}$ is the intrinsic anharmonic phonon scattering rate, $1/\tau_{\text{b}}$ is the phonon boundary scattering rate, $1/\tau_{\text{v}}$ is the phonon scattering rate due to the vacancies, $1/\tau_{\text{gb}}$ is the scattering rate due to grain boundaries, and $1/\tau_{\text{ld}}$ is linear defect scattering rate.

The phonon scattering rate caused by oxygen or gallium vacancies in the crystal can be expressed as [172, 173] :

$$1/\tau_{\text{v}} = x \left(-\frac{M_{\text{v}}}{M} - 2 \right)^2 \frac{\pi \omega^2 g(\omega)}{2G} \quad (4.2)$$

where x is the density of vacancies, M is the average mass per atom, M_{v} is the mass of the missing atom, $g(\omega)$ is the phonon density of states, and G is the number of atoms in the crystal (number of atoms in the unit cell). The grain boundary scattering rate was estimated using the Casimir model [174]:

$$1/\tau_{\text{gb}} = \frac{1-p(\omega)}{1+p(\omega)} D_{\text{avg}}^{-1} v_{g,a} \quad (4.3)$$

where $p(\omega)$ is the specular parameter, D_{avg}^{-1} is the average grain size of polycrystalline samples, and $v_{g,a}$ is the phonon group velocity along a direction. In this case, the specular parameter $p(\omega)$ was chosen to be zero, which represents diffusive scattering at grain boundaries. The linear defect scattering rate was estimated using the equation in [175]:

$$1/\tau_{\text{ld}} = 0.7 \frac{a^2}{v} \gamma^2 \omega^2 N_s \quad (4.4)$$

where a is the lattice parameter, v is the phonon velocity, γ is the Grunnessien's constant, ω is the angular frequency and N_s is the number of linear faults per cm. In contrast to the Debye-Callaway model used by other researchers [23] , using an exact iterative solution of phonon BTE is more accurate , and allowed me to obtain the thermal conductivity tensor for layers with different thickness, and calculate the thermal conductivity along different directions, following the procedure presented in [176].

For the calculation of the TBC, I used the diffusive mismatch model (DMM), considering not only the acoustic phonon branches but all branches of the materials because the complex crystalline structure leads to many optical branches and cannot be omitted in the calculations. For example, researchers in [52] demonstrated that optical phonon modes contribute significantly to the thermal conductivity of Ga_2O_3 depending on the orientation of the crystal. I implemented the qDMM model, where the integration is performed over the wave vector q [177].

4.4. RESULTS

Before determining the thermal conductivity of Ga_2O_3 and TBC at its interfaces with the substrate, I first determined the thermal properties of the sapphire and SiC substrates using 2-layered samples. The through-plane and in-plane thermal conductivities of SiC were estimated to be 301.4 ± 36.2 W/(m·K) and 387.3 ± 46.5 W/(m·K), respectively. For sapphire, the thermal conductivity was 27.3 ± 2.0 W/(m·K). These values agree with the previous studies, and I used them as constants in the 3-layer models. I used the data set with the best-fitting results to estimate the thermal conductivity and the TBC. The samples on c-sapphire (119 nm) had a thermal conductivity of 3.2 ± 0.3 W/(m·K), whereas the thermal conductivity of the sample on 4H-SiC (81 nm) was 3.1 ± 0.5 W/(m·K). The numerically estimated conductivities using BTE for the two thin film samples were 8.9 W/(m·K) (119 nm) and 7.9 W/(m·K) (81 nm), which are much higher than the measured values.

The thermal conductivity of crystalline samples of Ga_2O_3 thinner than 120 nm has hardly been reported. The thermal conductivity of thin films of Ga_2O_3 fabricated using PLD has been reported in [23]. The thermal conductivity of the samples fabricated by MBE is slightly higher than those fabricated by PLD with comparable thickness (~ 100 nm). It is lower than the film grown by MOVPE on sapphire in [51], but those films were thicker (>164 nm). A comparison of different

results is presented in Fig. 4.3a. I also compared the thermal conductivity of MBE-grown samples with single-crystal thin-film samples. For example, the study in [178] presents the thermal conductivity of monocrystalline Ga₂O₃ thin films bonded to SiC. H ions were implanted in the Ga₂O₃ crystal before the bonding process, which might have induced strain in the crystal and produced defects. For this reason, the thermal conductivity of a ~140 nm sample was 2.9 W/(m·K), which is lower than what could be expected for a single crystal sample but comparable with our results. The fabrication process and post-fabrication treatment will likely affect thermal conductivity and the TBC.

The phonon dispersion curve for Ga₂O₃ in the (-201) direction was calculated using the 2nd order harmonic force constants (IFCs) and thermal conductivity from the iterative solution of BTE using 2nd and 3rd order IFCs, obtained from the first principles simulations. When comparing the experimental and computational results, I observe that the experimental results in the (-201) direction are ~ 2 to 3 times smaller than those computed from the first principles. This could indicate the presence of unavoidable imperfections during the fabrication of the thin films of Ga₂O₃. Fig. 4.3b shows the variation of the computed thermal conductivity of Ga₂O₃ without imperfections with respect to its thickness for the (-201) direction, where it is evident that the thermal conductivity will reach a plateau, corresponding to the bulk value, similar to the results published in [23].

To explain the lower thermal conductivity measured from TDTR compared to the numerical predictions, I introduced scattering due to the vacancies of gallium and oxygen, the grain boundaries, and linear defects (stacking faults) while computing conductivities (see Eq. 4.1). The gallium vacancies had a higher impact in the reduction of the thermal conductivity because gallium is heavier than oxygen. Linear defects are first not considered to isolate the effect of

vacancies (Fig. 4.4a). Simulations with 3 % oxygen vacancies result in thermal conductivity of 4.2 W/(m·K) and 4.0 W/(m·K) for 119 nm and 81 nm samples, respectively, which is still higher than the measured conductivity and suggests the presence of Ga vacancies in our samples. I estimated that the 119 nm sample had around 3 % Ga vacancies, whereas the 81 nm sample had around 2.5 %. Through high-resolution transmission electron microscopy [179] and positron spectroscopy [180], previous studies determined that the most likely vacancies to occur during fabrication are Ga vacancies for both bulk and thin films. A high density of linear defects is also probable. For this reason, three levels of linear defects were introduced in the calculations for the 119 nm sample, in addition to Ga vacancies (Fig. 4.4b). The thermal conductivity for a sample with 1% of Ga vacancies and 10^6 linear defects/cm was 3 W/(m·K), which is close to the measured value, as opposed to 8.9 W/(m·K) for a perfect crystal (Fig. 4.4b). Also, the effects of the linear defects are more pronounced when the linear density is at least 10^6 defects/cm. The actual linear defects density is 1.5×10^6 defects/cm. I obtained this values by calculating the square root of 2.5×10^{12} linear defects/cm², that is the linear defect density per unit of area previously reported in [157].

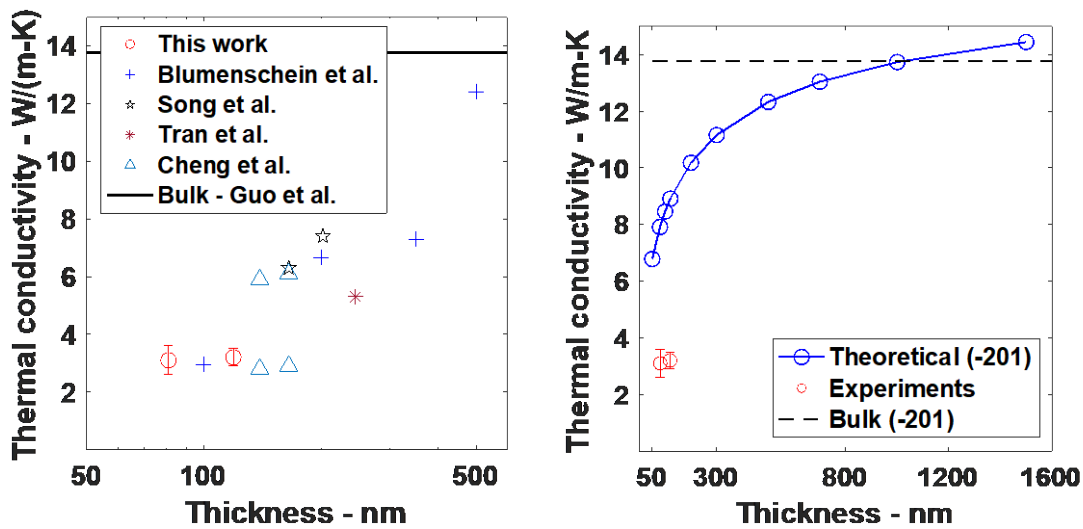


Fig. 4.3. (a) Comparison of published values of the thermal conductivity of thin films Ga_2O_3 with respect to their thickness. The sample for this work were grown by MBE, whereas the rest of the films were grown using PLD, MOVPE or were monocrystals [22, 23, 34, 51, 178]. (b) Variation of the thermal conductivity of Ga_2O_3 in the (-201) direction with thickness. Thermal conductivity computed using BTE is compared against the experimental results. The dashed line corresponds to the bulk thermal conductivity in the (-201) direction, as reported by [34].

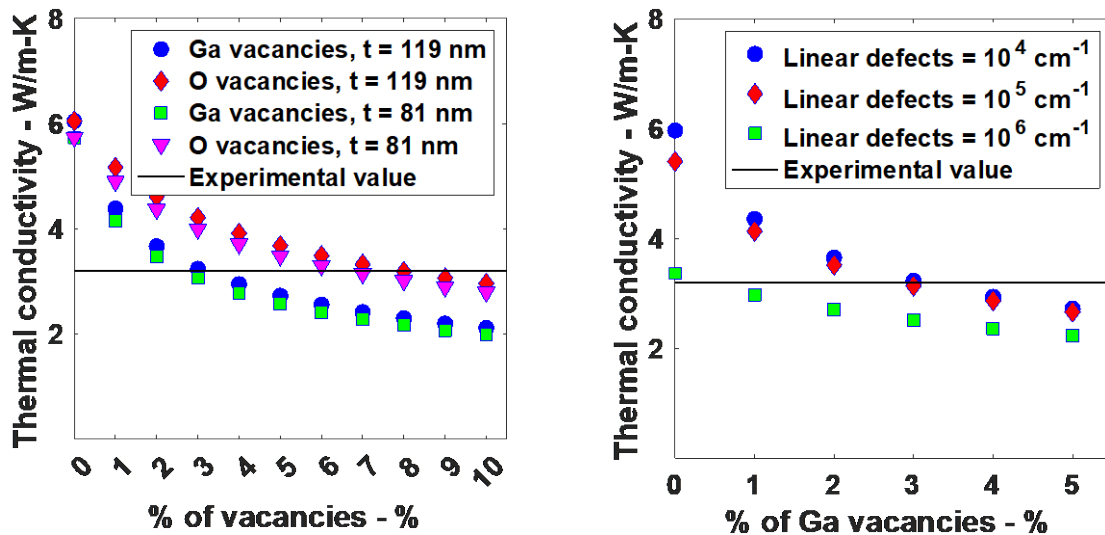


Fig. 4.4. (a) Influence of gallium and oxygen vacancies on the thermal conductivity. Gallium vacancies cause a higher reduction in the thermal conductivity compared to oxygen vacancies. The linear defect density is set to zero to isolate the effect of vacancies. (b) Influence of the density of linear defects on the thermal conductivity when gallium vacancies are present for the 119 nm sample (grown on sapphire).

I measured the TBC at the interface of Ga₂O₃ with the metal transducer and the substrates SiC and sapphire. Using TDTR, the TBC at the interface of Al/Ga₂O₃ was measured as 125.41 +15.62 / -10.66 MW/(m²·K) for the sample grown on sapphire and 158.18 +88.37 / -41.34 MW/(m²·K) for the sample grown on SiC. The results may indicate that the different imperfections that the fabrication method induces in the crystal depend on the substrate. The TBC values reported here are in the same order of magnitude as those reported in [20, 181, 182]. For the Ga₂O₃/substrate interfaces, a summary of the TBC results is presented in Table 4.1. Details on the methods to calculate the uncertainty can be found in Appendix A. Due to the low parameter sensitivity, high uncertainty in the estimation of the TBC can be observed, regardless of the calculation method. My results are comparable to those in [178] for crystalline Ga₂O₃ films bonded to SiC. The bonding of Ga₂O₃ with SiC using surface activation bonding required a thin layer of Al₂O₃ coating on Ga₂O₃. For a 30 nm thick Al₂O₃ layer, the reported TBC was ~ 70.1 +68.1/-10.4 MW/(m²·K), whereas for a 10 nm thick Al₂O₃ layer, the reported TBC was ~ 100.5 +93.8/-16.2 MW/(m²·K).

Table 4.1. TBC results with the uncertainty estimate with two different methods

Interface	Traditional Method [183]	Monte Carlo Method [75]
Ga ₂ O ₃ /sapphire TBC MW/(m ² ·K)	155.6 ± 65.3	159.6 +58.2 /-62.5
Ga ₂ O ₃ /SiC TBC MW/(m ² ·K)	141.8 ± 63.8	149.3 +57.9/-46.4

For the theoretical calculations of the TBC at the Ga₂O₃/substrate interfaces following DMM(details of these equations are in Appendix A), I used the phonon dispersion curve of Ga₂O₃ obtained from the first principles. For sapphire (orientation 001) and SiC (orientation 001), I used the dispersion curves available in the Materials Project [184, 185] in the $\Gamma \rightarrow Z$ and $\Gamma \rightarrow A$

directions, respectively. At 300 K, the calculated TBC using the DMM for the Ga₂O₃/sapphire interface was 294.3 MW/(m²·K), whereas the Ga₂O₃/SiC interface was 357.0 MW/(m²·K). When comparing the experimental and theoretical results, I can see that the experimental mean TBC values are between 2 and 2.5 times smaller than the DMM-based estimations. This difference could be attributed to the defects present at the interface of Ga₂O₃/substrate. One important detail in the estimation of the TBC using DMM to point out is the use of the full dispersion curves for the materials because of the complexity of the crystalline structures and the large number of optical phonons despite their lower phonon branch velocities. If I had only considered the acoustic phonon branches, the TBC values would have been 51.8 MW/(m²·K) for Ga₂O₃/sapphire and 57.4 MW/(m²·K) for Ga₂O₃/SiC, underestimating the TBC values. Finally, it was suggested that Ga₂O₃ could replace GaN-based devices. Studies in [186] reported TBC values of 199.8 +29.3/-30.23 MW/(m²·K) for the GaN/AlN-SiC interface and 224.41 +22.49/-23.3 MW/(m²·K) for the GaN/SiC interface. Those values are between 30% and 50% higher than those I report for Ga₂O₃/SiC but still lower than the TBC that could be expected for a perfect Ga₂O₃/SiC interface.

In summary, I report the thermal conductivity of Ga₂O₃ thin films grown by MBE with 119 nm and 81 nm thicknesses and the TBC at Ga₂O₃/sapphire and Ga₂O₃/SiC interfaces. The measured thermal conductivity is around three times smaller than the numerically calculated conductivity for pristine thin films of similar thickness with no defects. Calculations of the variation in thermal conductivity with the percentage of gallium and oxygen atom vacancies, linear defects in thin-films, and the lateral grain boundaries explain the experimental results. For example, the inclusion of grain boundary scattering, corresponding to grain sizes obtained from AFM, contributed to a reduction of 32% in thermal conductivity compared to a sample with no defects. 1% of Ga vacancies contributed to a further reduction of 28%, and the presence of 10⁶ cm⁻³

¹ linear defects reduced another 30% the thermal conductivity in the samples grown on sapphire. In all, my results provide reference values of thermal properties of thin-film Ga₂O₃ and its interfaces and suggest the level of defects present in the crystal that could be used to accelerate the design of Ga₂O₃-based electronic devices.

CHAPTER 5: MACHINE LEARNING APPROACHES TO STUDY THE THERMAL CONDUCTIVITY OF MATERIALS FOR MEMRISTORS ELECTRODES

This chapter presents the use of FDTR to measure the thermal conductivity of Ti-containing nitrides, and the application of ML models to help in the data treatment for this type of experiments.

5.1. THERMAL CONDUCTIVITY OF MATERIALS AIMED TO IMPROVE MEMRISTORS' PERFORMANCE

Hafnium oxide-based memristors are promising devices for nonvolatile memories and artificial synapses. The switching mechanism of these memristors relies on the movement of oxygen defects [187]. Researchers in [188, 189] demonstrated a TiN/Ti/HfO₂/TiN memristor with excellent switching behavior. One of the reasons is that the titanium layer attracts the oxygen in the HfO₂ layer. Given that other researchers have demonstrated the importance of reduced thermal conductivity in the electrode material, I compared the thermal conductivity of different Ti-containing materials.

I measured the thermal conductivity using FDTR of four different samples: TiN, Ti₂AlN (cubic phase), Ti₂AlN (hexagonal phase), and Ti₂AlN (MAX Phase). To determine the uncertainty of the results, I used the Monte Carlo-based method by performing 2000 fitting operations for each data set. The upper and lower bounds correspond to the 90th and 10th percentile of the normally distributed fitting results, respectively. All samples were fabricated on sapphire (through-plane thermal conductivity: 32 W/m-K; in-plane thermal conductivity: 30 W/m-K) by sputtering by Prof. Eric Vogel's group at MSE, Georgia Tech. Before performing the experiments, a ~100 nm thick gold layer (nominal thickness) was deposited on the samples to facilitate the acquisition of the reflected laser beam. The gold layer's mean thickness was 88 nm, measured using a Bruker Dimension Icon atomic force microscope. The average sheet resistance of gold was found to be

4.03E-1 Ω/sq using Signatone Four-point Probe. I used the sheet resistance to estimate the thermal conductivity using the Wiedemann-Franz Law. The value for the thermal conductivity of gold was 202 W/m-K, within the range of the values reported by other researchers [190]. The physical properties of the different materials needed to estimate the thermal conductivity are presented in Table 5.1, and the results are summarized in Table 5.2

Table 5.1. Physical properties of the materials

	Thickness (nm)	Density (kg/m³)	Specific Heat (J/kg-K)	References
Gold	88	19320	1230	[191] [192]
TiN	273	5400	604	[193] [194]
Ti ₂ AlN – cubic	242	4350	607	
Ti ₂ AlN – hexagonal	269	4350	607	[195] [196]
Ti ₂ AlN – MAX Phase	215	4350	607	

Table 5.2. Thermal conductivity of measured Ti-based materials

	Through plane thermal conductivity (W/m-K)	In-plane thermal conductivity (W/m-K)
TiN	12.1 -1.4/+6.6	12.1 -1.4/+6.6
Ti ₂ AlN – cubic	7.4 -0.8/+1.6	7.4 -0.8/+1.6
Ti ₂ AlN – hexagonal	3.6 -0.5/+1.3	4.1 -0.9/+2.9
Ti ₂ AlN – MAX Phase	8.0 -0.9/+5.6	6.7 -2.4/+8.4

The values range from 3.6 W/m-K for the Ti₂AlN – hexagonal sample to 12.1 W/m-K for the TiN sample. The thermal conductivity of the Ti₂AlN-hexagonal is the lowest because successive nano-sized layers of Ti and AlN form it. In addition, a more interesting comparison is between the TiN and Ti₂AlN-MAX phase. The thermal conductivity of the MAX phase sample is ~ 30% lower than the thermal conductivity of TiN, which means that the performance of memristors that use the Ti₂AlN MAX phase instead of TiN would be better.

5.2. ML MODELS FOR THE ANALYSIS OF FDTR DATA

Among the several algorithms available to develop ML models applied to Mechanical Engineering [197], researchers have employed artificial neural network (ANN)-based models to deal with the data obtained from TDTR or FDTR experiments. However, up to three variables have been predicted by such models. In this work, I tested two different ANN architectures. First, I used the model developed by Choi [198], inspired by the one presented by Shen et al. [10] (It will be called “Model A”). Second, researchers in [11] used a fully connected architecture but did not provide any detail on the hyperparameters. For that reason, I used the model presented in [197] (It will be called "Model B"). Fig. 5.1 and Table 5.3 summarize each model's principal parameters. Model A's architecture includes a concatenation layer following each dense layer, merging the dense layer's output with the original input features. This layer allows the network to learn advanced features while retaining access to the original input data, enhancing its ability to identify relationships between the input features and the target variables.

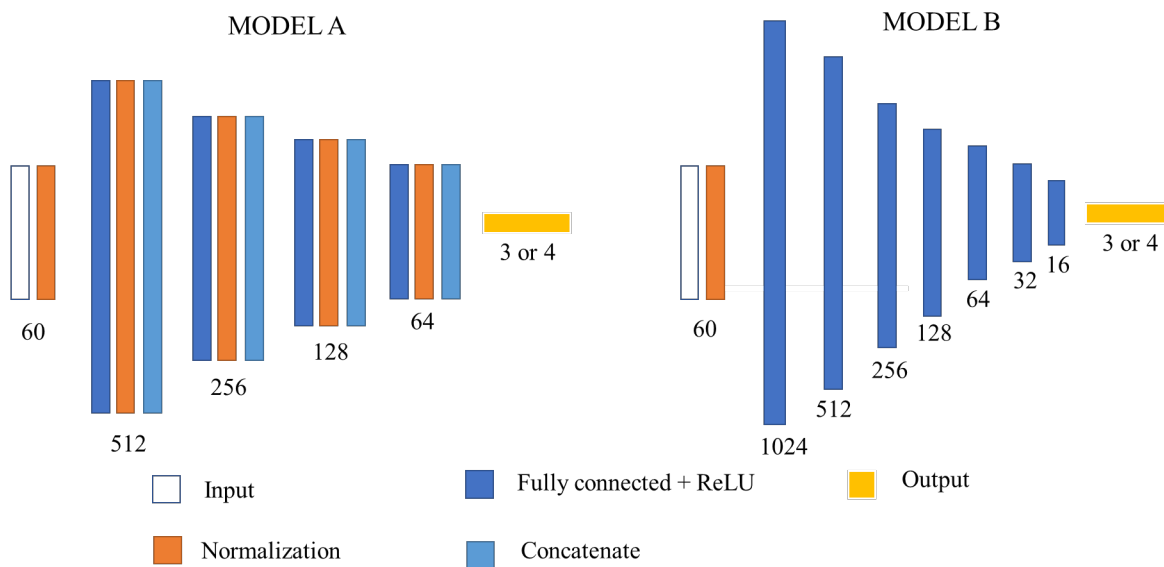


Fig 5.1. Schematic of the ML model architectures used in this work.

Table 5.3. Comparison of the ML model architectures used in this work.

	Model A	Model B
Input parameters	60	60
Output parameters	3 or 4	3 or 4
Hidden layers sizes	512, 256, 128, 64	1024, 512, 256, 128, 64, 32, 16
Hidden layers types	Fully connected, Batch Normalization, Concatenate	Fully Connected
Activation function	ReLU	ReLU

The literature dealing with the application of ML for analyzing TDTR/FDTR data has reported two strategies to obtain the training data to use in ANN. The first strategy is to use all combinations of the parameters of a model within a specific range. The advantage of this strategy is that it allows one to obtain samples from the whole data space. However, it limits the number of parameters used in the calculations. Increasing the resolution within a determined range for all variables (e.g., using 50 data points in a range [a, b] of thermal conductivity instead of 20 data points) or adding more variables (e.g., varying the gold layer thickness) increments the total number of combinations, that easily can reach billions of points. On the contrary, a second strategy uses only some combinations to produce the training data. Instead, random values from each variable space are selected and combined to obtain the training data. For this purpose, I used the Latin Hypercube Sampling (LHS) method [199] to generate 150×10^3 unique sets of phase angles. Finally, I trained the model with 80% of the data and validated it with the remaining 20%.

I used two standard metrics to assess the training performance of the models: the coefficient of determination (R^2) and the mean absolute percentage error (MAPE). In general, when the performance parameters do not meet a specific goal, the hyper-parameters of the ML model need to be modified until a well-performing ML model is obtained. However, the purpose of this work is to explore the limits of the current models that our research groups have. Consequently, fine-tuning and retraining the models is part of future research work.

Another difference concerning previous works is that I implemented a statistical method to remove the outliers from the training data set, the interquartile range method (IQR) [200]. The IQR measures the dispersion of a data set, defined as the difference between the 25th and 75th percentiles of the data set. The IQR is often used to identify outliers. The rule to determine the outliers states that any number below 1.5 IQR from the 25th percentile (i.e., $Q_{25^{th}} - 1.5 \text{ IQR}$) or above 1.5 IQR from the 75th percentile ($Q_{75^{th}} + 1.5 \text{ IQR}$) can be considered an outlier.

5.3. RESULTS

5.3.1. Results for a two-layer model of an anisotropic material to predict three parameters simultaneously.

For the first test, I trained a model to predict the through-plane thermal conductivity (k_{out}), the in-plane thermal conductivity (k_{in}), and the TBC between the material and the gold transducer (G_I) when sapphire is the substrate (this is the substrate employed to grow the materials tested for electrodes' memristors). Table 5.4 presents the range of parameters used to generate the training database.

Table 5.4. Range of the parameters to generate the training database for two-layer models with anisotropic material and with gold transducer.

	Range	Unit
Through-Plane thermal conductivity	10 – 50	W/m-K
In-Plane thermal conductivity	10 – 50	W/m-K
Volumetric Heat Capacity	$1 \times 10^6 - 4 \times 10^6$	J/kg-m ³
Thermal Boundary Conductance	40- 120	MW/m ² -K
Gold thermal conductivity	180 – 220	W/m-K
Gold thickness	85 - 100	nm

Pump beam radius	5.8 – 7	μm
Probe beam radius	1.6 – 2.2	μm

For the training phase, the results show that both models accurately predict k_{out} , k_{in} , and G_I . The maximum MAPE is 10% in all cases. Removing the outliers is critical because it allows the models to be trained only with physically actual data (i.e., it removes the values from materials that might not exist in nature). In addition, both models showed a similar performance, which means that the added complexity of model A did not significantly improve the results. Table 5.5 summarizes and compares the results of the training phase.

Table 5.5 Comparison of the performance of Models A and B in the training phase for a two-layer model with anisotropic material for the prediction of three variables at once

		R^2	MAPE
Model A	k_{out}	0.900	0.101
	k_{in}	0.902	0.098
	G_I	0.979	0.034
Model B	k_{out}	0.899	0.102
	k_{in}	0.901	0.098
	G_I	0.977	0.036

Even though both models showed encouraging behavior during the training phases, the next step was testing their performance with experimental data. Table 5.6 shows the model's performance against the traditional fitting method for sapphire. The error for the thermal conductivity in both directions does not exceed 10%, especially for model B. It is within the range of the values calculated with the traditional fitting method, which means that the ML model has similar accuracy to the conventional fitting method but is faster (around 36 milliseconds for the ML model as opposed to 3 seconds for the conventional fitting), once the model is trained. However, the difference for the TBC is significant when the ML models are compared with the mean value of G_I . Further analysis of this variable indicates that the sensitivity of the TBC is low for the model.

For this reason, the prediction capacity diminishes with the model's sensitivity to different variables.

Table 5.6. Actual (traditional fitting) and ML-predicted k_{in} , k_{out} , and G_I for sapphire

		Average	Predicted	% difference with average
Model A	k_{out} (W/m-K)	26.57 -1.78/+1.87	27.47	3.4
	k_{in} (W/m-K)	28.57 -1.84/+2.02	33.02	15.6
	G_I (MW/m ² -K)	106.45 - 5.11/+5.23	86.67	30.3
Model B	k_{out} (W/m-K)	26.57 -1.78/+1.87	29.75	7.6
	k_{in} (W/m-K)	28.57 -1.84/+2.02	29.92	10.4
	G_I (MW/m ² -K)	106.45 - 5.11/+5.23	80.34	24.9

5.3.2. Results for a two-layer model of an anisotropic material to predict four parameters simultaneously.

This work aims to test the limits of ML learning models. Previous works have tried to predict up to three variables at once. This is the first time that four variables are predicted with a ML model. One of the parameters required for the correct fitting of FDTR experiments is the transducer thickness (in this case, gold). Measuring gold thickness requires fabricating an additional sample to avoid scratching the original sample and using an atomic force microscope or a profilometer to measure the thickness. For this reason, I added the gold thickness as one of the variables to be predicted by the ML model. In addition, given that the TBC value has high uncertainty, I replaced it with the pump beam radius, a known and accurately measured variable. The training data was the same as used in section 5.3.1. Except for the gold thickness, the performance values were similar to the previous model. However, given that the gold thickness was narrow with a relatively limited range (from 85 to 100 nm), the prediction performance is expected to be reasonably accurate. A summary of the results is presented in Table 5.7

Table 5.7 Comparison of the performance of Models A and B in the training phase for a two-layer model with anisotropic material for the prediction of four variables at once.

		R^2	MAPE
Model A	k_{out}	0.899	0.101
	k_{in}	0.901	0.098
	<i>pump radius</i>	0.779	0.021
	<i>Au thickness</i>	0.582	0.037
Model B	k_{out}	0.898	0.102
	k_{in}	0.900	0.099
	<i>pump radius</i>	0.773	0.021
	<i>Au thickness</i>	0.127	0.037

The prediction capability of Model B was better than Model A. The error prediction for k_{in} , k_{out} , and *Au thickness* was within 5%. On the other hand, the k_{out} predicted by model A was too low with respect to the expected value. This indicates that model A's added complexity (which means it takes longer to train) does not help improve the model's predictive capabilities. A summary of the results is shown in Table 5.8.

Table 5.8. Actual (traditional fitting) and ML- predicted k_{in} , k_{out} , *pump radius*, and *Au thickness* for sapphire

		Average	Predicted	% difference with average
Model A	k_{out} (W/m-K)	26.57 -1.78/+1.87	19.87	25.21
	k_{in} (W/m-K)	28.57 -1.84/+2.02	34.03	19.11
	<i>pump radius</i> (μm)	6.79	6.35	6.48
	<i>Au thickness</i> (nm)	88.00	94.00	6.81
Model B	k_{out} (W/m-K)	26.57 -1.78/+1.87	29.63	0.40
	k_{in} (W/m-K)	28.57 -1.84/+2.02	33.50	11.97
	<i>pump radius</i> (μm)	6.79	6.35	6.48
	<i>Au thickness</i> (nm)	88.00	92.26	4.84

5.3.3. Results for a three-layers model (thin film) anisotropic material to predict four variables at once.

Many of the samples tested by FDTR are comprised of three layers: a metal transducer, a thin film (much thinner than the substrate), and a substrate. The fitting of these samples is more

difficult because five new variables must be added (physical properties of the thin film such as the out-of-plane thermal conductivity, the in-plane thermal conductivity, the density, the specific heat, and the thickness) plus a new TBC between the thin film and the substrate. For this reason, the training data set for this kind of sample required a new set of variables. The range of the data I used to train this new model is summarized in Table 5.9. I tailored the range for the thermal conductivity of the substrate to coincide with sapphire properties. Otherwise, using a broader set of values would have improved the model's prediction accuracy to reasonable levels.

Table 5.9. Range of the parameters to generate the training database for three-layer models with anisotropic material with gold transducer.

	Range	Unit
Substrate Through-Plane thermal conductivity	25 – 35	W/m-K
Substrate In-Plane thermal conductivity	25 – 35	W/m-K
Substrate Volumetric Heat Capacity	$1 \times 10^6 - 4 \times 10^6$	J/kg-m ³
Thermal Boundary Conductance Substrate/film	40- 120	MW/m ² -K
Thin Film Through-Plane thermal conductivity	5 – 15	W/m-K
Thin Film In-Plane thermal conductivity	5 – 15	W/m-K
Thin Film Volumetric Heat Capacity	$1 \times 10^6 - 4 \times 10^6$	J/kg-m ³
Thickness Thin Film	200 - 300	nm
Thermal Boundary Conductance film/gold	40- 120	MW/m ² -K
Gold thermal conductivity	180 – 230	W/m-K
Gold thickness	85 – 100	nm
Pump beam radius	5.8 – 7	μm
Probe beam radius	1.6 – 2.2	μm

Given that the final purpose of an ML model is to predict a set of values and that this work does not use the statistical parameters to optimize the model's hyperparameters, I will only report the prediction results of these more complex models. I used the experimental data obtained from the measurement of the Ti₂AlN MAX Phase. As expected, the prediction capabilities of a more complex model deteriorated the performance. However, the prediction capabilities must be compared to traditional fitting models. For the Ti₂AlN MAX Phase, the uncertainty of the measurements, especially for the higher end, is high (as reported in Table 5.2). I predicted k_{out} , k_{in} for the Ti₂AlN, the pump beam radius, and the gold thickness. The results are presented in Table 5.11

Table 5.10. Actual (traditional fitting) and ML-predicted k_{out} , k_{in} , pump radius, and Gold thickness Ti₂AlN MAX Phase.

	Average	Predicted	% difference with average
Model A	k_{out} (W/m-K)	8.00 -0.9/+5.6	5.28 34.00
	k_{in} (W/m-K)	6.70 -2.4/+8.4	9.99 49.10
	pump radius (μm)	6.79	6.67 1.77
	Au thickness (nm)	88.00	91.00 3.49
Model B	k_{out} (W/m-K)	8.00 -0.9/+5.6	9.72 21.5
	k_{in} (W/m-K)	6.70 -2.4/+8.4	9.70 44.77
	pump radius (μm)	6.79	6.41 5.60
	Au thickness (nm)	88.00	93.00 5.68

Although the absolute error increased with respect to the mean value, the values predicted by the ML model are within the range of the predicted values obtained with traditional fitting. This means that the ML learning model has similar accuracy to the conventional fitting method but is faster (30 milliseconds for the ML model, as opposed to 7 seconds for the traditional fitting). On the other hand, the ML model can predict known parameters with a difference lower than 6%.

5.4. SUMMARY.

I trained two ML models to predict four different properties simultaneously in two (transducer and substrate) and three-layered (transducer, material, and substrate) samples. At their current status (hyperparameters), the models are accurate enough to replace the traditional fitting model when the model is sensitive to those parameters. ML models are also much faster than traditional fitting models. Low sensitivity in traditional fitting could not be fixed using the ML models. However, the models can be improved to predict more than three variables accurately.

CHAPTER 6: HEAT SPREADERS FOR PORTABLE ELECTRONICS

This chapter compares the suitability of using h-BN and HOPG as heat spreaders as part of the packaging of a silicon chip. The first part analyzes the possibility of using h-BN and discusses the advantages and drawbacks of these materials. The second section focuses on my work on HOPG, followed by the results of using different options to bond this material with silicon substrates.

6.1. h-BN AND HOPG FOR THERMAL MANAGEMENT OF HOT SPOTS ON SILICON CHIPS USED IN MOBILE DEVICES: A SIMULATION-BASED COMPARISON

I developed the simulation model in collaboration with Dr. Wenqing Shen, a former member of the MiNDS lab.

Current smartphones' application processing unit (APU) increasingly includes more powerful CPUs, GPUs, and machine learning engines. A typical design, Package on Package (PoP), enables swift data transfer between the APU and memory by stacking the memory chip and logic chip together. However, the heat generated inside the logic chip must not exceed a critical temperature. Two solutions exist for improving thermal performance without reducing operation power. One is creating a better heat dissipation channel from the PoP to the surrounding environment, and the other is optimizing the PoP for a more uniform temperature distribution. Because of limited space, heat dissipation from the logic die is typically passive, and the memory die stacked above adds extra thermal resistance. Using a heat spreader made of h-BN or HOPG to replace the epoxy mold compound (EMC) between the logic and memory dies will help to maintain the chip's temperature below its critical point.

I created a smartphone simulation comprising a battery, motherboard, display, and back panel to assess the effectiveness of various heat spreaders of different thicknesses. The phone's dimensions were estimated based on the iPhone 11 Pro Max. The PoP configuration included a 30

μm epoxy mold compound (EMC) between the logic die and the memory substrate (see Fig. 6.1). I also investigated thicker heat spreaders; the details will be explained later. The thermal conductivity of the heat spreader is summarized in Table 6.1. For all the cases, I assume that the heat source of the logic die is located in a $3 \times 3 \text{ mm}^2$ area at the center of the $10 \times 10 \text{ mm}^2$ logic die with a power dissipation of 4W.

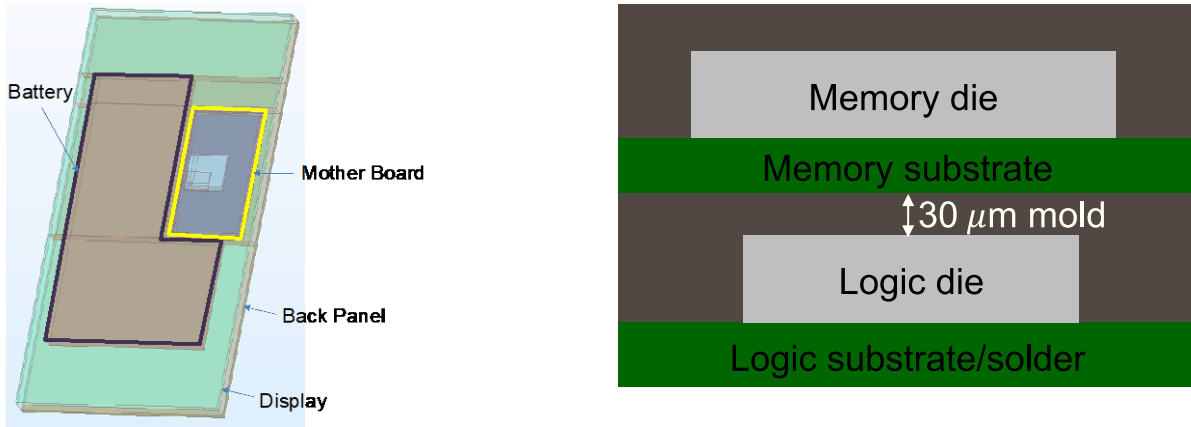


Fig. 6.1. Diagram of the smartphone (left) and Package on Package (right)

Table 6.1 Thermal conductivity of heat spreader materials

<i>Material</i>	<i>In-plane thermal conductivity</i>	<i>Cross-plane thermal conductivity</i>
	k_r (W/mK)	k_z (W/mK)
h-BN	200	20
HOPG	1500	10

I used the thermal resistance between the junction and ambient to evaluate the thermal performance of the integrated system. For both materials, the thermal resistance decreases with increasing thickness within the tested thickness range. However, there are significant differences between h-BN and HOPG.

First, for h-BN, the maximum temperature is $121.52 \text{ }^\circ\text{C}$ for the original design and $111.96 \text{ }^\circ\text{C}$ for PoP with a $30 \mu\text{m}$ h-BN heat spreader. The thermal resistance is reduced by 9.4% when

replacing the 30 μm EMC between the logic die and memory substrate with h-BN. A 10 μm h-BN reduces the thermal resistance by 4%. There are two options to apply h-BN thicker than 30 μm . The PoP can either have a thinner logic die and maintain the original PoP thickness or have a larger overall PoP thickness while keeping the original die thickness. With a thinner logic die, the thermal resistance decreases with increasing h-BN thickness. However, the decreasing trend is less sharp in the 30 - 80 μm range than in the 0 - 30 μm range. By keeping the original logic die thickness and having a thicker PoP, 70 μm h-BN results in a 16.3% reduction in thermal resistance, which is 27.9% better than having the same h-BN thickness but with a thinner logic die. For the range of thickness considered, it can be concluded that the thicker PoP is better than the thinner die for the integration of thick h-BN. This is because the Si substrate used in the logic die has high thermal conductivity, so a thicker a die can assist the heat spreading inside the die.

In the second place, I considered HOPG, which has much higher in-plane thermal conductivity. With thickness in the range of 0 ~ 30 μm , thicker HOPG results in lower thermal resistance. The thermal resistance with 30 μm HOPG is 18.5 K/W, 27.2% lower than the original PoP, and 2.9 times reduction compared with 30 μm h-BN. Although HOPG has lower cross-plane thermal conductivity than h-BN, the benefit of higher in-plane thermal conductivity makes HOPG a better heat spreader than h-BN. The result for both materials is summarized in Fig. 6.2. In short, replacing EMC between the logic die and memory with a heat spreader effectively improves the thermal performance of PoP. A thicker heat spreader results in lower thermal resistance, but there could be limitations on the maximum thickness of the heat spreader, which could be employed due to the constraints on the thickness of PoP or die. The thermal resistance is more sensitive to the in-plane thermal conductivity of the heat spreader rather than the cross-plane thermal conductivity. HOPG has the best heat-spreading performance when compared to h-BN.

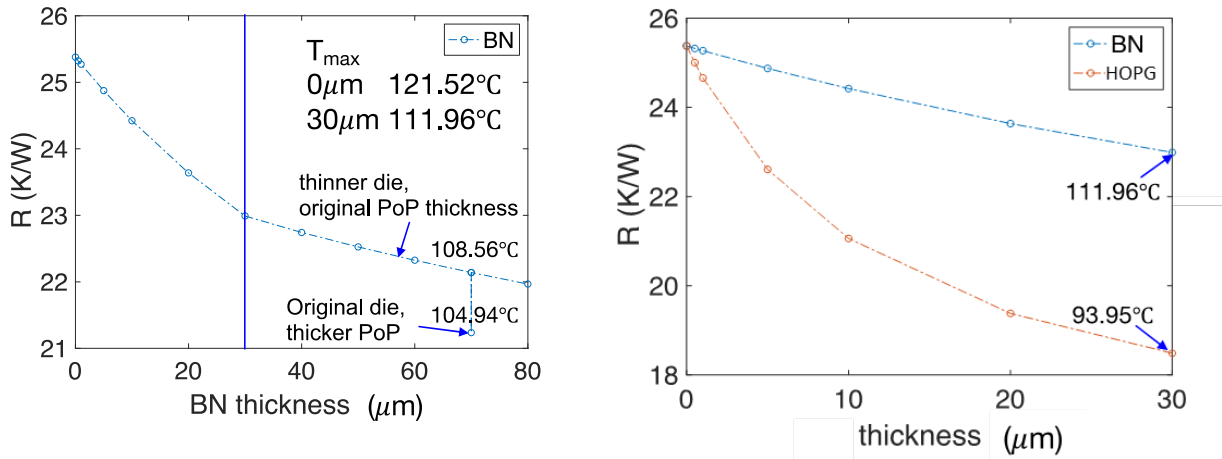


Fig. 6.2. Performance of h-BN heat spreader with a thickness of 0 ~ 80 μm (left) and HOPG heat spreader with a thickness of 0 ~ 30 μm (right)

6.2. METHODS AND CHALLENGES TO TRANSFER h-BN ON OTHER SUBSTRATES

Chemical vapor deposition (CVD) is the preferred method to fabricate large-area h-BN [100]. In this method, the substrate acts as a catalyzer for the growth of high-quality h-BN. Cu foil is the typical substrate to grow h-BN. I used CVD-grown 2 x 2 in² multilayer h-BN (provided by 2D Semiconductors) to perform the transfer experiments.

The traditional transfer process requires fabricating a handling layer on top of the h-BN to provide structural integrity to the h-BN once the Cu substrate is removed. This handling layer is generally made of a polymer and should be removed once the h-BN is transferred [201]. An illustration of this process is presented in Fig. 6.3.

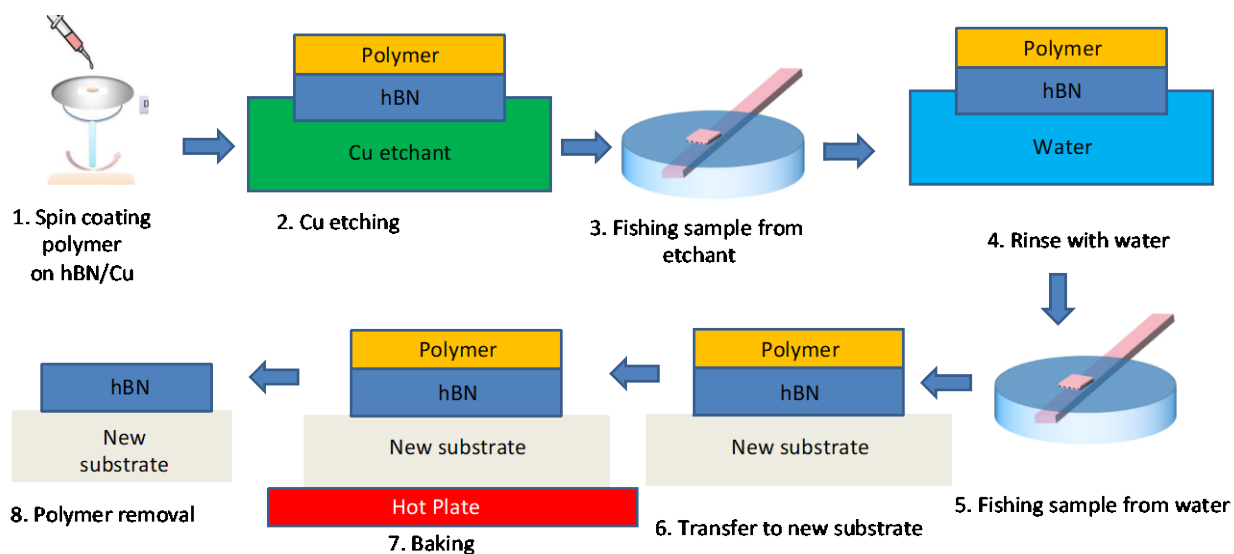


Fig. 6.3. Schematic of the transfer process of h-BN from Cu foil to a new substrate.

Most of the reported transfer processes have been tested on graphene. The selection of the polymer in the transfer process of graphene is crucial because each one will require different solvents and processing conditions to keep the graphene as clean as possible and avoid polymer residuals, which can affect the final properties of the transferred materials [98]. The same behavior (change of properties because of polymer contamination) could be expected in h-BN. For this reason, I tested three different polymers to transfer h-BN. Samples of size $\sim 10 \times 10 \text{ mm}^2$ of h-BN/Cu were spin-coated with the polymers. The first polymer I tested was Poly(methyl methacrylate) (PMMA). PMMA is used as a benchmark because it was the first polymer tested to transfer graphene. Most of the reports on transferring 2D materials used PMMA. I prepared a solution of 5% wt. of PMMA (MW $\sim 120,000$ by Sigma Aldrich) in acetone (ACS reagent $> 99.5\%$ by Sigma Aldrich) using a magnetic stirrer for about 8 hours to allow for the complete dissolution of the PMMA. I spin-coated a $\sim 500 \text{ nm}$ thick PMMA layer. The second polymer I tested was Poly(bisphenol A carbonate). I prepared a solution of 5% wt. of PC (MW $\sim 45,000$ by Sigma Aldrich) in chloroform (Sigma Aldrich) using a magnetic stirrer for about 8 hours to allow for the complete dissolution of the PC. I spin-coated a $\sim 1 \mu\text{m}$ thick PC layer. The third polymer that I

tested was rosin. I prepared a solution of 25% wt. and 50% wt. of rosin (Fischer Scientific) in ethyl lactate 97% (Fischer Scientific) using a magnetic stirrer for about 12 hours to allow for the complete dissolution of the rosin. None of the Rosin concentrations provided a strong enough polymer layer to have an acceptable transfer (i.e., the structural integrity of the samples was affected). In all cases, I removed the Cu foil by exposing the Cu/h-BN/polymer stack to a copper etchant (Ferric Chloride by Sigma Aldric) overnight. After rinsing and transferring the sample, I removed all polymers using their respective solvent baths for ~2 hours. Fig. 6.4 presents a qualitative comparison between different handling layers.

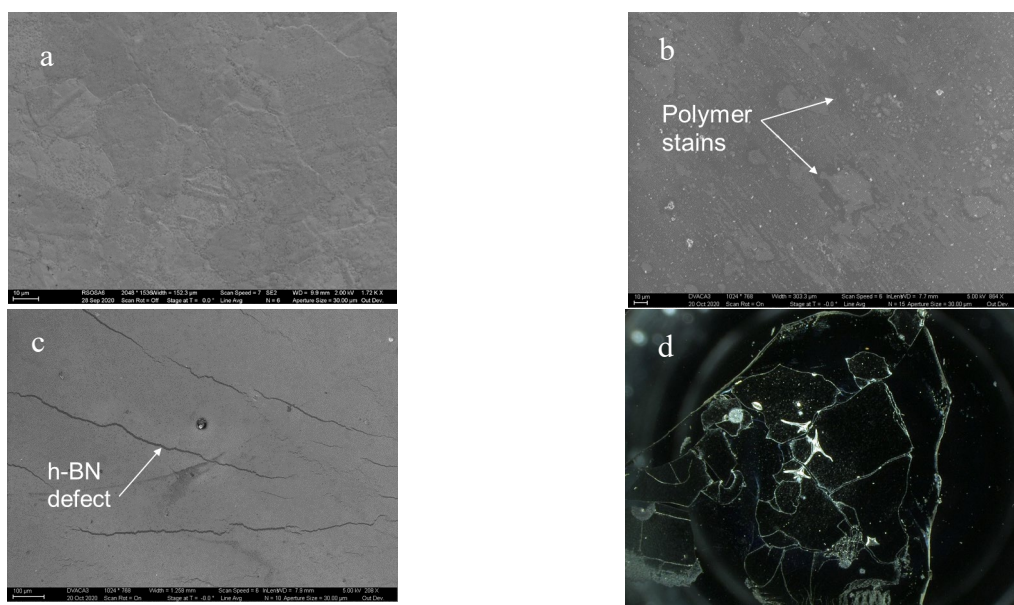


Fig. 6.4. Qualitative comparison of the surfaces of h-BN with different handling polymer layers. (a) pristine h-BN on Cu. (b) h-BN transferred using PMMA as the handling layer. (c) h-BN transferred with PC. (d) h-BN transferred using rosin. Contamination and defects are evident in (b) and (c), whereas the sample is destroyed in (d)

To complement the study on the transfer process, I used X-Ray photoelectron spectroscopy (XPS) to evaluate the atomic composition on the sample's surface. This study revealed that contamination (i.e., the presence of carbon atoms) is high in the samples. Fig. 6.5. shows typical

XPS curves for h-BN transferred using PMMA as the handling layer and the atomic composition calculated by the XPS software.

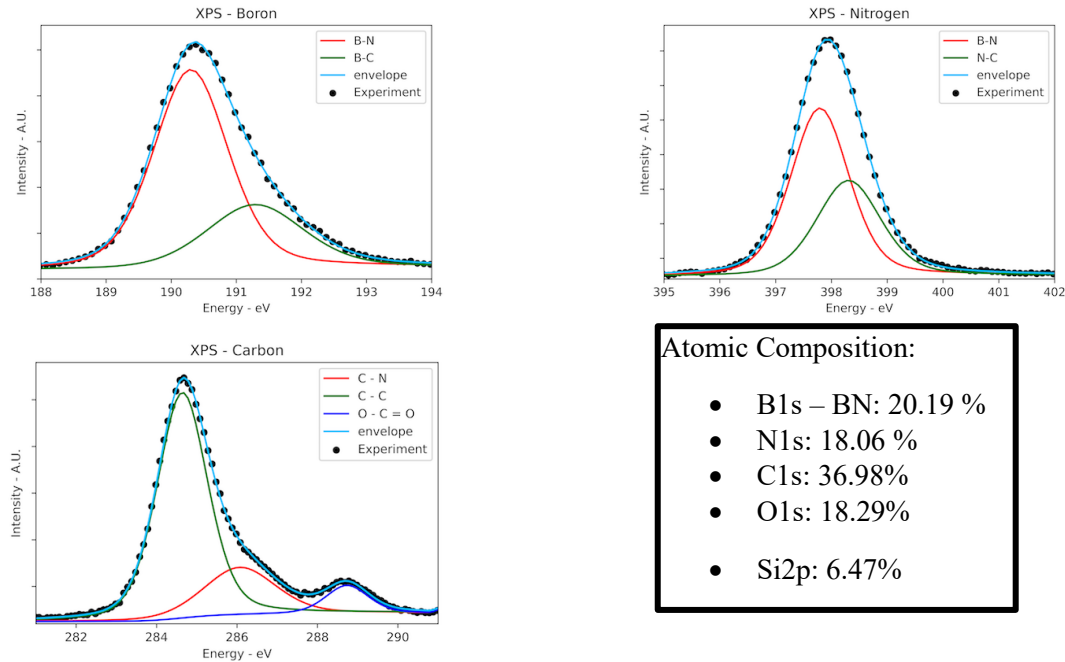


Fig. 6.5. XPS results for a h-BN sample transferred with PMMA. The figure shows boron, nitrogen, and carbon curves and the estimated atomic composition obtained from the curves.

I decided to move from h-BN to HOPG because of three main reasons. First, commercially available multilayered h-BN is not thicker than ~ 20 nm. A thicker h-BN heat spreader (in the μm order of magnitude) will require successive transfer processes to place h-BN layers one-on-top of the other, which cannot be transferred to industry because it would be costly and time-consuming. Second, even if thicker h-BN were available, simulations showed that the HOPG performance is superior when used in a chip package. Finally, although the steps seem simple, proper transfer of h-BN on Si wafer at a desired location is not a trivial task, and developing a proper in-house appropriate transfer process would have deviated from the actual purpose of this research, which is developing and testing heat spreaders.

6.3. APPROACHES TO REDUCE THERMAL RESISTANCE WITH HEAT SPREADERS MADE OF HOPG IN MICRO-ELECTRONICS: THE ROLE OF CYTOP AND NP-Cu

6.3.1. HOPG Morphology and Shear Strength.

I bonded HOPG samples (50 μm thick) to 5 x 5 mm^2 Si substrates using metal-to-metal thermocompression with Au and Cu and adhesive bonding using CYTOP to evaluate the HOPG resistance to shear forces. Before surface preparation, I evaluated HOPG using an optical profiler (Zeta-20). These measurements revealed three aspects of the HOPG surface that must be considered for bonding. The first aspect is roughness. The surface is not uniform and has a root mean square value of ~ 300 nm. I used this value as a guide to decide the thickness of the bonding material. The second aspect is that some localized regions present deep valleys of ~ 10 μm . These valleys may not be controlled during HOPG fabrication and might affect the contact between HOPG and Si. The third aspect is the "waviness" (long range deformation) of the sample. This deformation will correct itself during the thermocompression process. Fig 6.6 illustrates these affirmations.

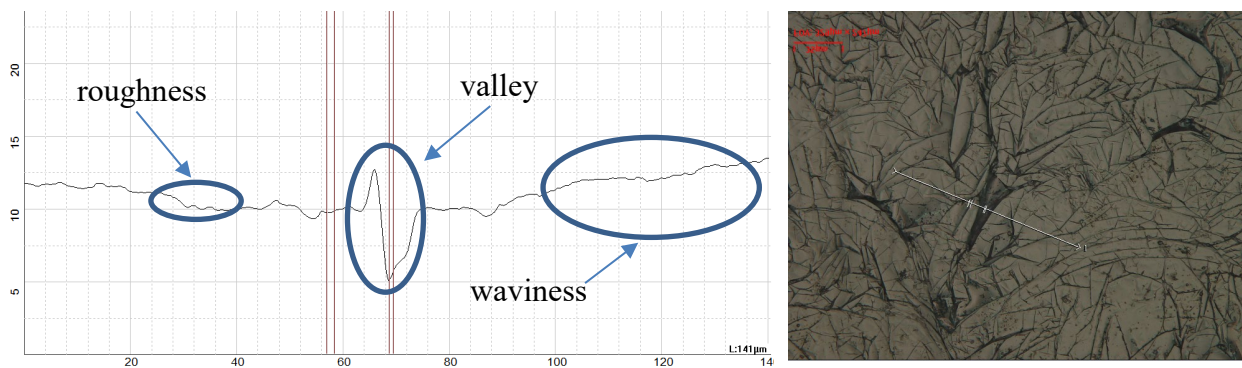


Fig. 6.6. Cross section of HOPG shows three types of irregularities on the surface: regular roughness, valleys, and waviness. The irregularities are randomly present all over the surface.

For the metal-to-metal thermocompression, I deposited 500 nm of Au or Cu on HOPG and Si using an e-beam evaporator. I bonded the parts using a manual chip bonder using ~ 80 N at 300,

350, and 400 °C for 15 minutes and 20 minutes for Au-to-Au and Cu-to-Cu samples, respectively. For the case of adhesive bonding with CYTOP, I spin-coated CYTOP on Si (1 μm and 2 μm layers) and placed the samples to evaporate the solution for ~5 minutes at 150 °C. I bonded HOPG on these substrates using a vacuum laminator set at 1 MPa and 180 °C for 15 minutes. Once the samples were ready, I used a standard shear test to assess the mechanical performance of the bonding and examined both sides of the bond to study the fracture mechanism.

Shear tests revealed that the maximum shear force for cleaving is ~1.5 kg, regardless of the bonding material. This result is counterintuitive because experiments that used metals as bonding materials were expected to have a better mechanical performance. However, further analysis of the samples under the microscope showed that HOPG delaminates. The weak Van der Waals forces that keep together the graphene layers that form HOPG are not strong enough to resist the shear force. In addition, images showed that among the delaminated HOPG, there were islands of "non-bonded" material. These non-bonded regions might affect the heat flow when HOPG is used as a heat spreader. Fig. 6.7 presents the comparison of the sizes of non-bonded regions.

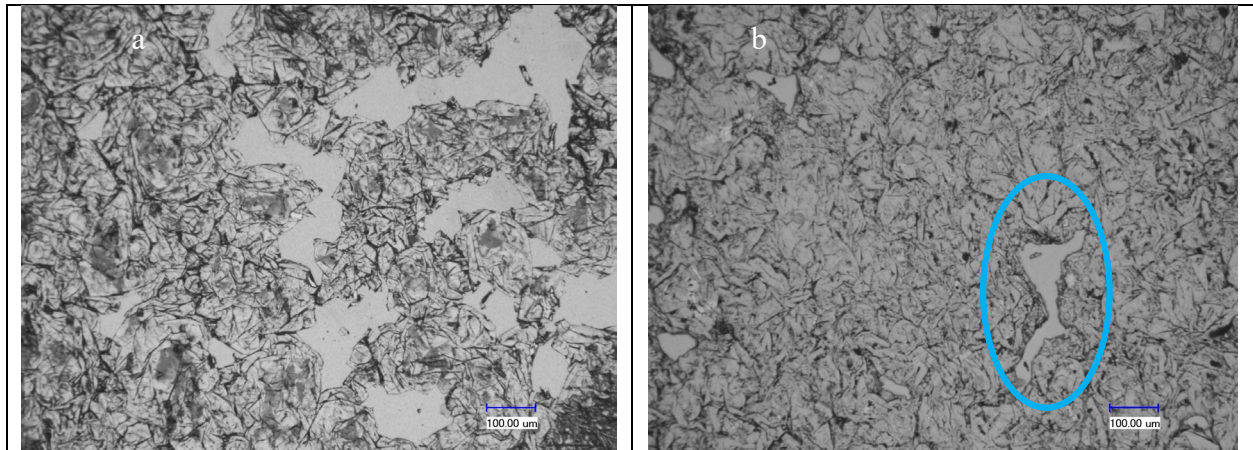


Fig. 6.7. Comparison of unbonded regions when bonded with different materials. (a) Au. (b) 2 μm CYTOP.

6.3.2. *Fabrication Methods*

I used an automatic dicing saw (DAD3360) to dice Si samples of 10 x 10 mm² from 550 μm thick 3-inch Si wafers. Then, I cut pieces of HOPG (Panasonic Pyrolytic Graphite Sheets), larger than the Si substrates, using scissors. The thickness of the HOPG was 80 μm (according to the manufacturer, the nominal thickness is 50 μm Panasonic) [202]. Before bonding, I cleaned both materials using acetone, methanol, and isopropyl alcohol and blow-dried with nitrogen.

CYTOP bonding

I diluted as-received CYTOP (9% polymer, 91% solvent, by weight) with its corresponding solvent in ~1:1 dilution ratio (by volume). I spin-coated this solution on the Si substrates (spin coating parameters: 500 rpm for 10 seconds and 1000 rpm for 20 seconds). The thickness of the films before bonding was ~1.5 μm. After spin coating, I evaporated the excess solvent by placing the samples on a hot plate at 100 °C for 2 minutes. After that, I employed a vacuum laminator (MVL300/300 by Meiki) to bond HOPG with CYTOP-coated Si substrates. I applied a pressure of 0.7 MPa at 170 °C for 15 minutes.

NP Cu fabrication

One of the options to bond HOPG with Si substrates is using NP-Cu. The fabrication of NP-Cu involves a process known as de-alloying, which is a selective dissolution method used to remove one or more components from an alloy. A general description of the fabrication process is as follows:

1. Evaporation of seed layer: I successively deposited 100 nm of titanium and 200 nm of copper on a 550 μm-thick silicon wafer using electron-beam evaporation (I used the Denton Explorer electron-beam evaporator in all evaporation processes)
2. Dicing: I diced the silicon wafers into 20 x 40 mm² rectangles using a disco dicing saw to facilitate control over the electrical parameters used during the electroplating process.

3. Electroplating / Alloy Preparation: I deposited an alloy of copper/zinc on the substrates by electroplating. The bath consisted of 0.01 M Cu, 0.15 M Zn, and 0.25 M Pyrophosphate in 3.5 liters of deionized water, using a potentiostatic process with a zinc counter electrode. More details on the chemistry of the bath can be found at [203]. I set the plating time to ~ 2 hours to obtain Cu/Zn layers between 1 and 2.5 μm . The alloy composition was maintained around 80%Cu/20% Zn and not higher than 90%Cu/10% Zn to reduce the de-alloying time (next step) and maintain a Zn content as low as possible (lower than 5%) after de-alloying.
4. Dicing: I diced the electroplated substrates using a disco dicing saw to have 10 x 10 mm^2 samples.
5. Selective Dissolution (De-alloying): The next step involves subjecting the alloy to a chemical de-alloying process. I placed the samples in diluted 0.05 M HCl for ~ 1 hour. This process dissolves most of the Zn in the alloy, creating nano-ligaments in the structure.
6. Washing and Drying: Once the de-alloying process is complete, I thoroughly washed the NP-Cu by rinsing it in two successive baths of deionized water and leaving it in the open air for drying.

The fabrication of NP-Cu with desired composition (~80 % Cu / 20% Zn) and morphology (nano-ligaments) required studying the parameters that affect these characteristics. In the first place, there is an inverse correlation between the current density and the alloy composition. A higher current density (more negative) correlates with a smaller Cu composition in the alloy. In our experiments, the average current density (not considering the first 10 minutes that takes the current to stabilize) was ~ -0.625 mA/cm^2 to obtain a ~80%Cu/20%Zn composition. Fig. 6.8. presents the correlation between the copper composition and the current density.

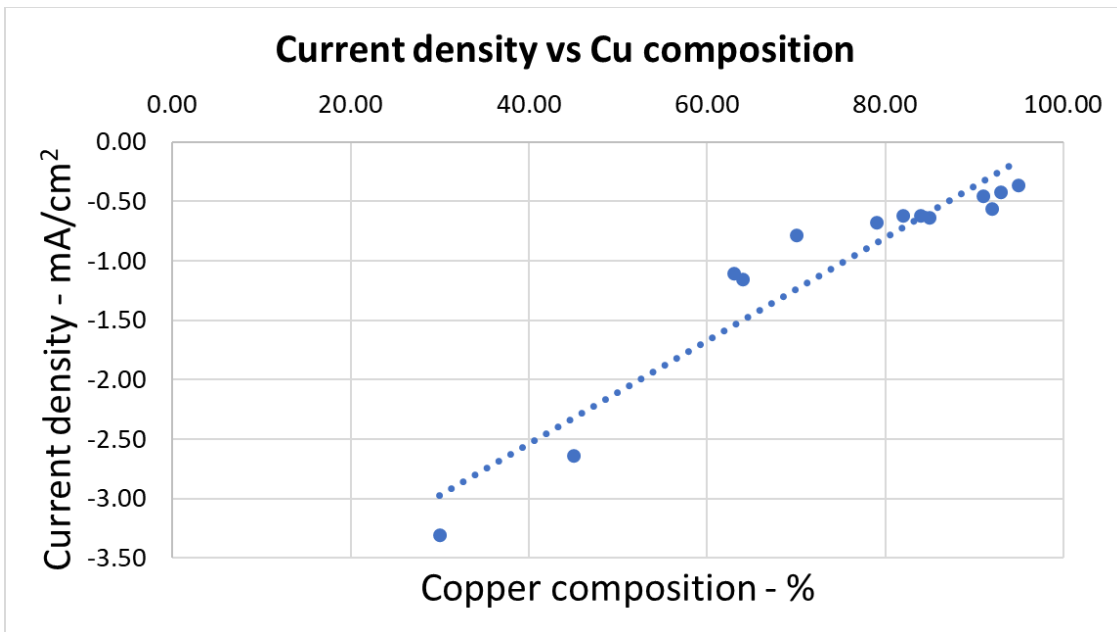


Fig. 6.8. Correlation between the copper composition in the alloy and the current density.

Once I fabricated the NP-Cu samples, I examined them using a scanning electron microscope (SEM) to assess the link between the alloy composition and the final morphology after de-alloying. The de-alloying time and the alloy's initial composition impact the final morphology of the nanostructures. Fig. 6.9 compares alloys with different compositions when the de-alloying time was ~ 1 hour, whereas Fig. 6.10 shows the de-alloying time impact on the morphology.

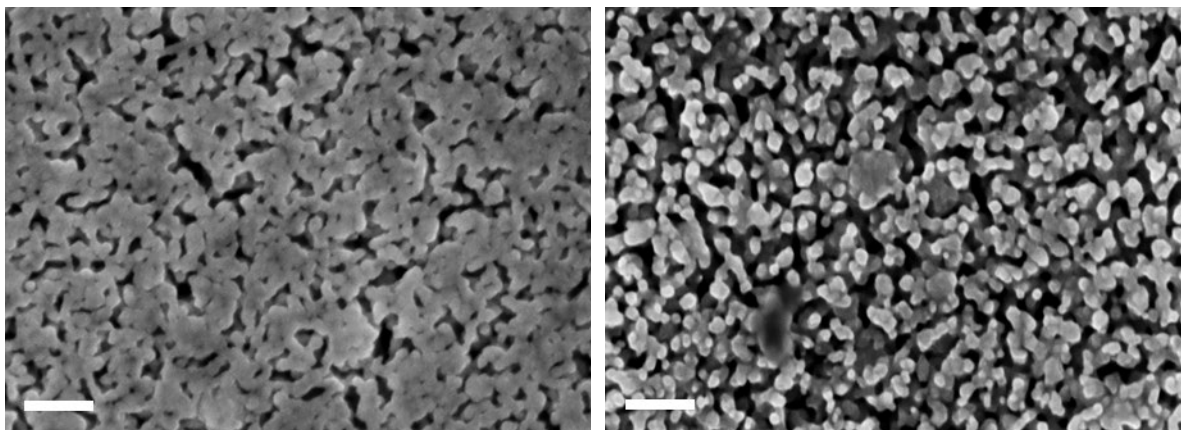


Fig. 6.9. Comparison between an 82%Cu / 18% Zn alloy (left) and a 90% Cu / 10% Zn alloy in SEM images taken from the top. The structures on the left resemble an interconnected network of ligaments, whereas those have disappeared in the right image, which means that the sample shown on the right is "too de-alloyed." The scale bar is 200 μm .

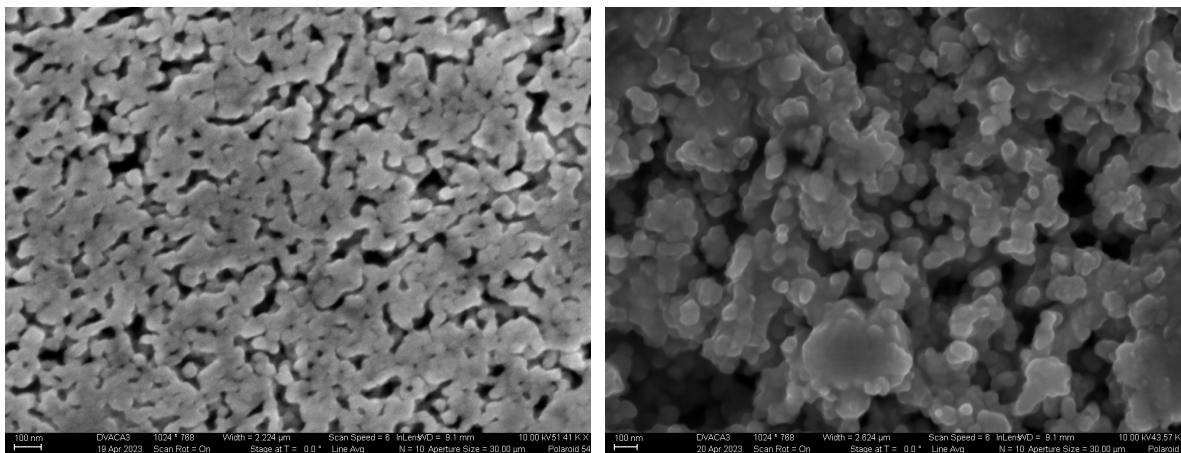


Fig. 6.10. Comparison between an 82%Cu / 18% Zn alloy, whose de-alloying times were ~ 1 hour (left) and 1 hour 45 minutes (right) in SEM images taken from the top. The ligaments have disappeared in the sample on the right. Both images have a magnification of $\sim 45\text{KX}$.

Finally, two common problems might happen during NP-Cu fabrication and be avoided with a proper cleaning protocol. The first problem is the formation of crystals on the top surface of the sample. I observed crystals, whose composition is $\sim 60\%$ Cu, 25% Cl, and 15% other elements, on the sample's surface if the HCl acid used for de-alloying remains on the sample. In this case, the sample is unusable because of the contamination. The second problem is that a too-

aggressive cleaning protocol (using pressured deionized water, for example) might delaminate the NP-Cu from the seed layer. Fig. 6.11 illustrates these problems.

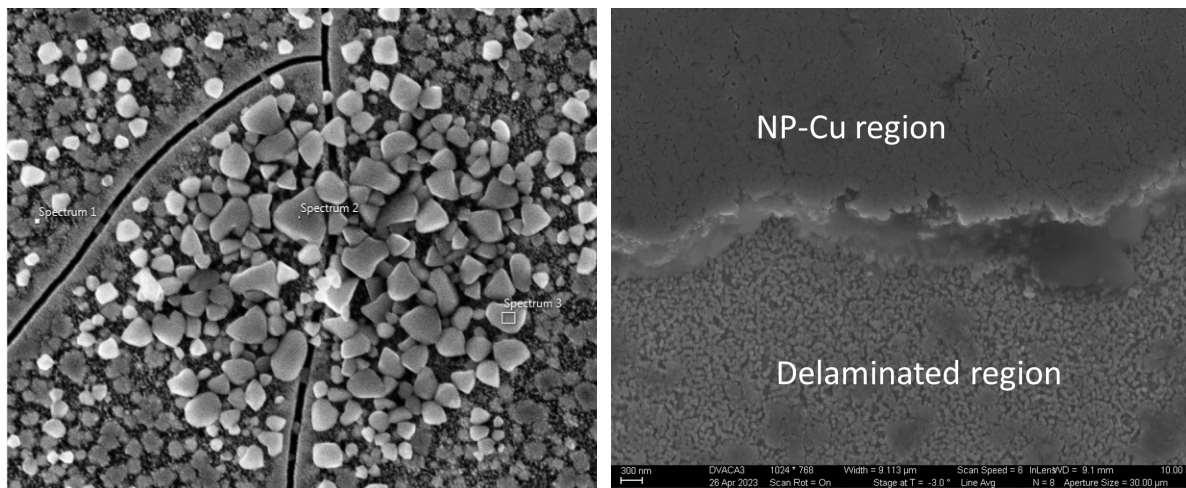


Fig. 6.11. Problems presented during NP-Cu fabrication due to improper cleaning protocols. If the samples are not adequately cleaned, the remaining HCl will form crystals on the surface (right), whereas a too-aggressive cleaning protocol might delaminate the NP-Cu from the seed layer (right)

Metallization of HOPG

To bond a silicon substrate with HOPG using NP-Cu, HOPG must have a copper seed layer for Cu-Cu bonding with the NP-Cu fabricated on the silicon substrate. For this reason, I evaporated 100 nm of Ti and 200 nm of Cu on previously cleaned (with acetone, methanol, and isopropyl alcohol) HOPG. After metallization, I cut $\sim 12 \times 12 \text{ mm}^2$ pieces with scissors.

Bonding Si/NP-Cu to metallized HOPG.

The bonding process started with the copper oxide control on the parts. It is recommended that the bonding be performed under forming gas environment. However, due to tool constraints, I emulated the process by dipping both parts in a solution containing 33% formic acid in isopropyl alcohol [203]. After that, I assembled both parts (Si/NP-Cu and HOPG with the Cu seed layer) using a C-clamp [204] that provided a force of $\sim 900 \text{ lb}$. This force is $\sim 40 \text{ MPa}$ when $10 \times 10 \text{ mm}^2$

samples are employed. The assembly was introduced in a vacuum oven and sintered at 200 °C for 30 minutes. Some experiments were performed at 250 °C and 300 °C but were unsuccessful. I speculate that higher temperatures exacerbate copper oxide formation, and the formic acid solution does not properly work at higher temperatures. On the other hand, all samples bonded at 200 °C were successful (i.e., the parts stayed bonded after the removal of the c-clamp)

HOPG bonded to Si substrates using epoxy.

After dicing 10 x 10 mm² Si substrates, I used screen printing to apply ~110 μm of epoxy TIM (8329TFS Thermally Conductive Adhesive). After that, I manually pressed pieces of HOPG on the Si/epoxy sample until both parts bonded. Finally, I cured the samples at 80 °C for 6 hours in an oven.

Fabrication of samples for thermal tests

Since the transient thermal tests require a pulsed power source, I utilized power diodes as active devices to generate heating power, allowing us to monitor the evolution of the TSP during the cooling process. I bonded the 10 x 10 mm² samples (HOPG/Si) to the backside of a power diode (RFUH5TF6S by Rohm semiconductor) using double-sided tape (Thermally Conductive Adhesive Transfer Tapes 8805 by 3M). Then, that stack was attached to a 60 x 60 mm² FR4 board to provide the electrical connections needed to perform the tests. Half of the samples had an extra double-sided tape attached to the FR4 board to perform the experiments according to the JEDEC JESD51-14 (see characterization methods section). An illustration of the samples is presented in Fig. 6.12.

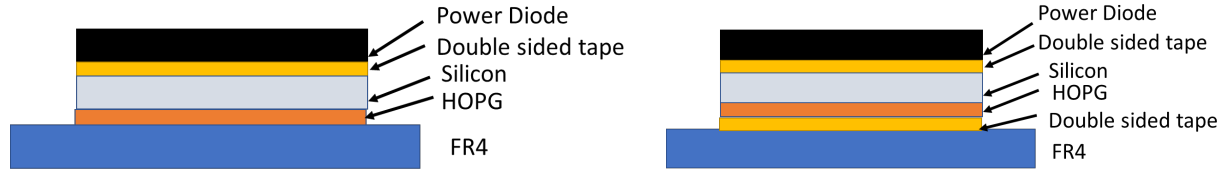


Fig. 6.12. Representation of samples used for the thermal tests. Epoxy, CYTOP, or NP-Cu are used between the Silicon and HOPG layers. Double-sided tape is used to bond the Si/bonding material/HOPG stack on the backside of a power diode. To perform the experiments, half of the samples have an extra double-sided tape layer (right) to attach the stack to the FR4 board.

6.3.3. Thermal assessment of HOPG bonded with CYTOP and NP-Cu.

Even though the purpose of this work is the thermal characterization of the samples, I performed a simple peeling test to characterize the morphology of the joint bonding materials/HOPG. The results showed mechanical failure in the HOPG, not at the interface. Being a group of graphene layers, one on top of the other, bonded by weak Van der Waals forces, HOPG delaminates. Most of the regions on the surface area of the delaminated samples presented delaminated HOPG with some "unbonded areas" where both CYTOP and NP-Cu are visible. Fig. 6.13 presents these results.

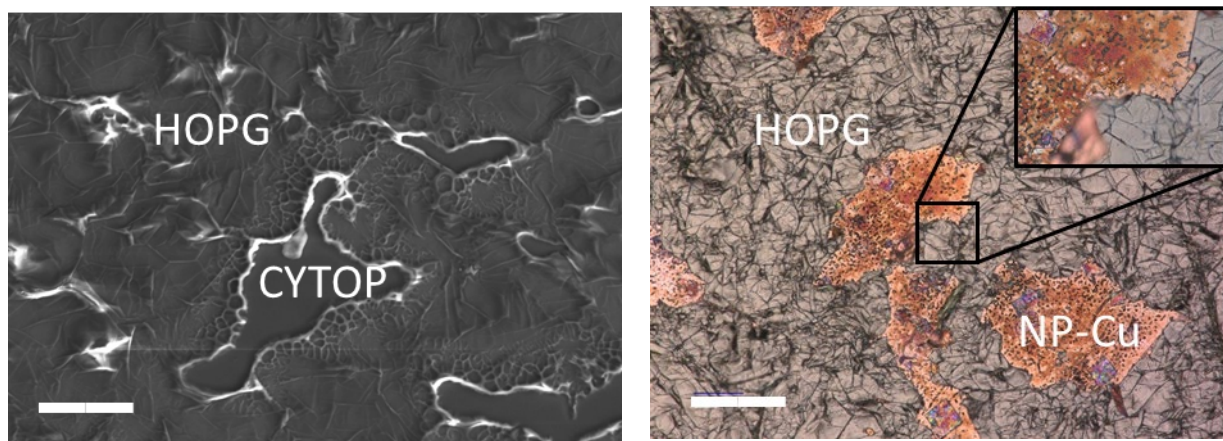


Fig. 6.13. Comparison between delaminated samples bonded with CYTOP (left, SEM image) and NP-Cu (right, optical microscope image) taken from the top. The inset in the right figure shows a magnified area with NP-Cu and HOPG. Most of the area is covered by delaminated HOPG with "unbonded areas" scattered on the surface of both samples. These unbonded areas are bonding defects that might affect thermal performance. The scale bar is 100 μm .

After describing the bonded interface's morphology, I measured the thermal performance. The first step to obtaining a thermal transient curve for an electronic component is to calibrate the device under test (DUT) with accurate thermal measurements. This calibration was achieved by applying a small constant sensor current (100 mA) to the DUT and monitoring the change in voltage with temperature. The calibration process covered a temperature range of 20°C to 60°C, resulting in a K-factor of -2.384 mV/°C. The K-factor represents the correlation between the forward voltage at a constant forward current and the junction temperature.

Once I calibrated the samples, the first experiment involved measuring the diode package to compare it with the value reported in the datasheet. The value calculated at the separation point of the two structure functions (see Figs. 10 and 11) was 2.34 K/W. In contrast, the published value is 2.5 K/W [205] (~ 6% higher than the published value). In consequence, the values calculated using these experiments can be trusted. Fig. 6.14 shows the comparison between curves with and without the additional thermal resistance using our adaptation of the method employed in the JEDEC JESD51-14 standard to determine the thermal resistance of the power diode package.

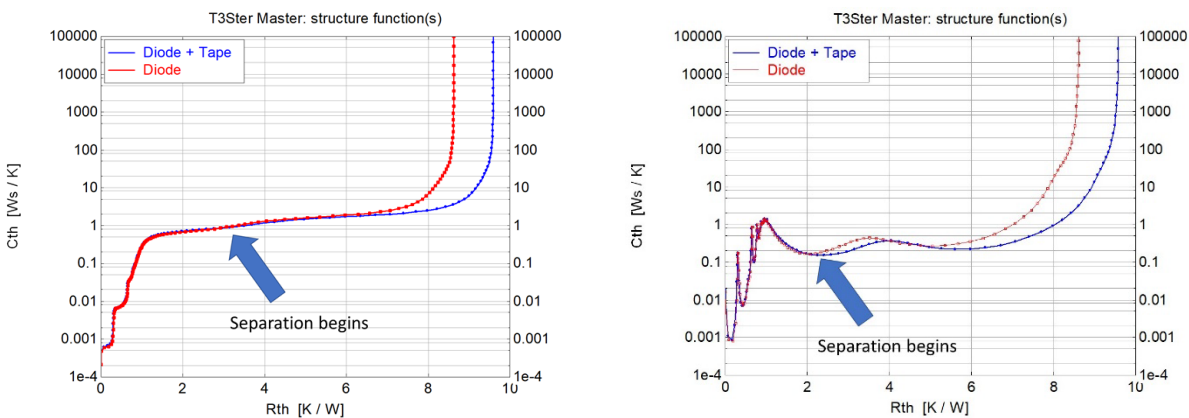


Fig. 6.14. Comparison of the structure functions (left) and the derivative of the structure functions (right) of two power diodes, without and with an additional double-sided tape to attach the sample to the FR4 substrate and use the procedure established in the JEDEC JESD51-14 standard for the measurement of the junction-to-case thermal resistance of semiconductor devices with heat flow through a single path. The separation point indicates

the value of the package's thermal resistance. The separation is more apparent in the right-side plot.

The following experiment attempted to measure the thermal resistance of the tape/silicon substrate thermal resistance. The sample comprises three layers: the power diode, the double-sided tape, and the silicon substrate (this stack will be called PD/DT/Si). The results indicate that the stack PD/DT/Si has a thermal resistance of 4.25 K/W, and given that the thermal resistance of the power diode is 2.34 K/W, the thermal resistance of the double-sided tape/silicon stack is 1.91 K/W. The thickness of the Si substrate was 500 μm , and assuming a thermal conductivity of 130 W/m-K, the theoretical thermal resistance is 0.04 K/W. In consequence, the experimental thermal resistance of the double-sided tape is 1.87 K/W. On the other hand, the theoretical thermal resistance of the double-sided tape is 2.08 K/W (thermal conductivity: 0.6 W/m-K, thickness: 0.125 mm, size: 10 x 10 mm²), which is ~10% higher than the experimental thermal resistance.

To measure the thermal resistance of the epoxy/HOPG stack, I used a sample consisting of the power diodes, the double-sided tape, the silicon substrate, the epoxy layer, and HOPG (this stack will be called PD/DT/Si/E/HOPG). The thermal resistance of the stack PD/DT/Si/E/HOPG was 5.57 K/W. Since the thermal resistance of the stack PD/DT/Si was 4.25 K/W, the thermal resistance of the stack epoxy/HOPG was 1.32 K/W. The theoretical thermal resistance attributed to the epoxy layer was 0.92 K/W (thermal conductivity: 1.2 W/m-K [128], thickness: 110 μm , size: 10 x 10 mm²), whereas the theoretical thermal resistance attributed to the HOPG was 0.11 K/W (thermal conductivity: 7.1 W/m-K [11], thickness: 80 μm , size: 10 x 10 mm²)

Given that the structure of samples that use CYTOP and NP-Cu as bonding materials is the same as the one that uses epoxy, I obtained the thermal resistance by direct comparison of the total thermal resistance presented in the structure function obtained for the epoxy sample and the structure functions obtained for the CYTOP and NP-Cu samples. The results indicated that the

total thermal resistance for the CYTOP and the NP-Cu samples were 0.15 K/W and 0.42K/W lower than the total thermal resistance for the epoxy sample. Since the thermal resistance of the stack epoxy/HOPG was 1.32 K/W, the thermal resistance was 1.17 K/W for the CYTOP/HOPG stack and 0.90 K/W for the NP-Cu/HOPG stack. In the case of CYTOP, the theoretical thermal resistance attributed to the CYTOP layer was 1.22 K/W (thermal conductivity: 0.12 W/m-K [206], thickness: 1.5 μm , size: 10 x 10 mm^2). In the case of NP-Cu, thermal conductivity has not been widely reported because it depends on the degree of sintering. However, assuming that the NP-Cu is non-sintered (worst case scenario), the theoretical thermal resistance attributed to the NP-Cu was 0.0001 K/W (thermal conductivity: 176.5 W/m-K [138], thickness: 2 μm , size: 10 x 10 mm^2)

By comparing the experimental and theoretical values of the total thermal resistances of the bi-layers bonding material/HOPG, I can estimate the contact resistance at the interface of each material. For example, the theoretical thermal resistance for HOPG is 0.11 K/W, and the theoretical thermal resistance for the CYTOP layer is 0.12 K/W. Given that the experimental thermal resistance for the stack HOPG/CYTOP is 1.17 K/W, the thermal resistance at the interface CYTOP/HOPG is 0.94 K/W ($1.17 - 0.11 - 0.12 = 0.94$ K/W). Then, the contact resistance is calculated by multiplying the thermal resistance by area, i.e., 100 mm^2 (10 x 10 mm^2). A summary of the results is presented in Table 6.2. In the case of epoxy, the thermal resistance is dominated by the material itself, whereas for CYTOP and NP-Cu, the thermal resistance is dominated by the contact resistance. The results indicate that although significant room exists to fully optimize the bonding conditions for the CYTOP and NP-Cu cases (e.g., the contact resistance is higher than when using epoxy), the total thermal resistance is lower than the current industry practice.

Table 6.2. Summary of thermal resistance values for the different options of bonding material

Stack of Materials	Thermal Resistance [K/W]	Total Equivalent Contact Resistance $\times 10^{-5}$ [m² K/W]	Contact Resistance at the interface Bonding Material/HOPG $\times 10^{-5}$ [m² K/W]	Equivalent Contact Resistance not including HOPG $\times 10^{-5}$ [m² K/W]
Epoxy/HOPG	1.32	13.20	2.90	12.10
CYTOP/HOPG	1.17	11.70	9.40	10.60
NP-Cu/HOPG	0.90	9.00	7.90	7.90

To understand the reasons why the thermal contact resistances are higher than expected, especially for the NP-Cu sample (which is the material with the most industrial interest), I cross-sectioned ($\sim 30 \mu\text{m}$ long) NP-Cu samples using a focused ion beam (FIB). I obtained images using the SEM to study the sintering and bonding quality. I studied a sample bonded at $200 \text{ }^\circ\text{C}$, whose HOPG did not de-bond during manipulation. The cross-section (Fig. 6.15) revealed that the sample has three distinctive regions: a bonded region, a fractured region (i.e., the region that might have been bonded but started to separate in the NP-Cu/HOPG interface, and a non-bonded region. It might be expected that these three regions are uniformly scattered over the whole sample surface because the HOPG remained attached to the Si substrate. However, whether the partially bonded and un-bonded regions appeared because of the peeling force applied to study the samples is unclear. Also, I noticed that NP-Cu did not fully densify, which might result from insufficient sintering time or the lack of an appropriate bonding environment (i.e., not bonded under a reducing environment). Finally, the separation between the HOPG and the Si substrate happens at the interface between the HOPG and Ti/Cu-seed layer (i.e., the seed layer remains bonded to the NP-Cu, but the seed layer separates from the HOPG. This phenomenon has been previously reported in [207-210].

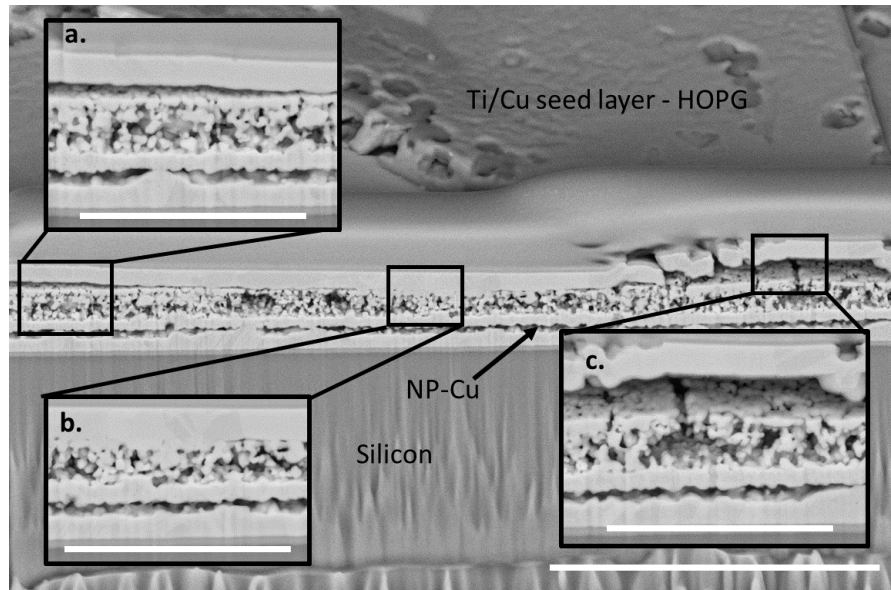


Fig. 6. 15. Cross section of a sample bonded at 200 °C. The detail a. shows a fractured region where the HOPG started to separate from the NP-Cu layer. The detail b. shows a bonded region with no gaps between HOPG and NP-Cu. Detail c. shows an un-bonded region with a wide gap between the HOPG and the NP-Cu. The scale bar for the image is 5 μm , whereas that for the insets is 2 μm .

Using the bonding solutions presented in this work, I simulated a hot spot on a silicon substrate's backside to predict the behavior of devices that might incorporate HOPG as a heat spreader. The power density was 250 W/cm². The development of this simulation model followed a similar approach outlined in [127] and [124]. The thermal contact resistance values used at the HOPG/Si substrate correspond to the "Equivalent Contact Resistance, not including HOPG" (presented in Table 6.2). This value was calculated by subtracting the theoretical HOPG thermal resistance (0.11 K/W) from the experimental HOPG/contact resistance/bonding material stack and multiplying the result by 100 mm² (10 x 10 mm²). In contrast, the thermal conductivity of the materials was as follows: in-plane HOPG: 1300 W/m-K, through-plane HOPG: 7 W/m-K, silicon: 130 W/m-K, package: 2 W/m-K. Fig. 6.16 presents the configuration for this simulation.

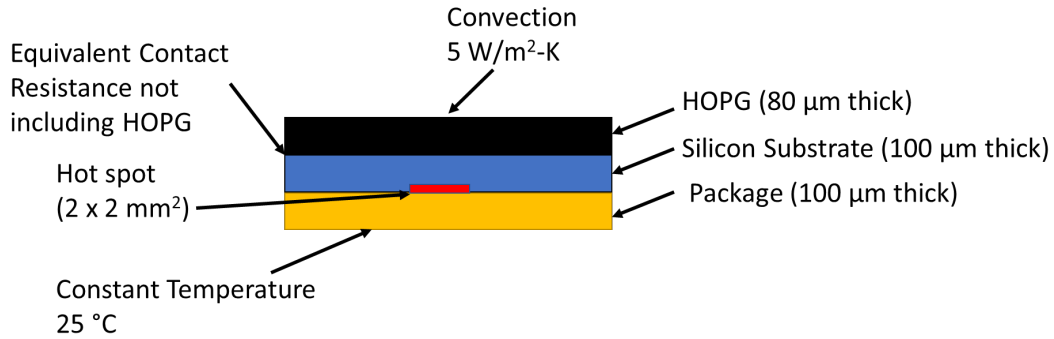


Fig. 6.16. Schematic of the model used for the simulation.

The results indicated that the hot spot temperatures were 83.2, 82.2, and 79.7 °C when using epoxy, CYTOP, and NP-Cu as bonding layers, respectively. Given that the bonding quality between HOPG and NP-Cu could be improved, a reduction in the thermal contact resistance would follow. If the thermal contact resistance between HOPG and NP-Cu reduces between five to ten times, the hot spot temperature would be 64.1 and 58.7 °C, respectively. Although the ideal bonding conditions for CYTOP and NP-Cu are yet to be found to decrease the thermal contact resistance at the interface, the temperature of the hot spot decreased with both proposed solutions, which indicates that HOPG bonded with NP-Cu to substrate could be a promising approach to develop heat spreaders for hot-spot thermal management.

In summary, I explored using h-BN and HOPG as heat spreaders for the thermal management of mobile electronic devices through simulations and experiments. First, I concluded that the development of h-BN (market availability, large-scale transferring, and other factors) is not mature enough to be considered in the short term a viable heat spreader. For this reason, I focused on comparing and developing methods to bond HOPG on silicon substrates. I used epoxy, CYTOP and NP-Cu as bonding materials and estimated the thermal resistance of the different materials. The results indicated that despite the bonding process with NP-Cu still needs

improvement, the lower thermal resistance of this material makes it a good candidate to attach HOPG to the back side of silicon microprocessors.

CHAPTER 7: SUMMARY AND FUTURE WORK

7.1. SUMMARY OF THE DISSERTATION

In this work, I studied the thermal properties of different materials for emerging electronics. Here I present a summary of the results.

(1) I studied the thermal conductivity of β -Ga₂O₃ thin films grown on sapphire and silicon carbide substrates by molecular beam epitaxy using TDTR and the iterative solution of the BTE. I used AFM and TEM to measure the grain size of β -Ga₂O₃ and the linear defect density of the samples, respectively. With that information, I compared the measured values with theoretical results and estimated the defect densities (vacancies and dislocations) that might have been created during growth. Finally, I used the DMM to predict the TBC between the material and the substrate to explain the experimental results better. The most relevant lesson from this section is that the fabrication conditions strongly affect the structure-properties relations of epitaxially grown materials. Unfortunately, the experiments to estimate the atomic scale defects might be complex, and the equipment for these experiments can be costly and not widely available. Consequently, the method proposed in this work (i.e., the combination of thermal measurements with atomic scale thermal modeling) can be used to study the effects of different types of defects on the thermal conductivity of epitaxially grown β -Ga₂O₃, which can help in accelerating the development of high quality of this material.

(2) I explored the thermal conductivity of materials used in memristors's electrodes using FDTR because of the importance of reduced thermal conductivity of the electrode material of memristors in enhancing their performance. I focused on measuring the thermal conductivity of different Ti-containing materials, including TiN, Ti₂AlN (cubic phase), Ti₂AlN (hexagonal phase), and Ti₂AlN (MAX Phase). The results indicated that replacing TiN with Ti₂AlN (MAX Phase) as

the material for HfO₂-based memristors will improve memristors' performance. In addition to the estimation of the thermal properties, these experiments showed me the versatility of the FDTR method over the TDTR method because I could estimate the in-plane thermal conductivity of the anisotropic materials with the same set of data without having to rely on modified methods (e.g., elliptical beams, beam offset measurements, and others).

(3) I used machine learning models to analyze the FDTR data and predict the thermal conductivity of materials. I tested two different ANN architectures and found that predicting four parameters simultaneously is challenging for the current ML models. Despite the models requiring further exploration and optimization of the architecture and the hyperparameters, the estimations are within the range of the values estimated using traditional fitting. This section highlights that it is difficult to create a general ML model for most materials with enough accuracy to deal with an ample range of physical properties and dimensions. Different models will be required for different applications (e.g., anisotropic materials, high thermal conductivity materials ($\sim > 500$ W/mK), low thermal conductivity materials (< 5 W/mK), among others) if high accuracy is required.

(4) I compared the suitability of using h-BN and HOPG as heat spreaders for silicon chips in mobile devices and discussed the advantages and drawbacks of these materials. For that purpose, I proposed replacing the epoxy mold compound (EMC) between the logic and memory in PoP configuration with h-BN or HOPG. I studied this alternative by FEM simulations. The results showed that HOPG outperformed h-BN for heat management. In addition, I explored different h-BN transfer methods to study the adaptability of these research laboratory methods for industrial processes. Ultimately, I concluded that HOPG is a better candidate for heat spreaders in Si chips. The main lesson learned is that the h-BN-related technology needs to be mature enough to be implemented in thermal management applications. The main drawbacks are the impossibility of

fabricating thick, high-quality h-BN and the complications of adapting the current transfer practices to industrial processes.

(5) I employed CYTOP and NP-Cu to bond HOPG heat spreaders on Si substrates and presented an adaptation of the method employed in the JEDEC JESD51-14 standard to determine the thermal resistance of the power diode package. The results indicated that, despite the best bonding conditions are yet to be found, both strategies to reduce the thermal resistance, reducing the BLT (CYTOP) and increasing the thermal conductivity of the bonding material (NP-Cu), are interesting options that require further analysis. The current use of NP-Cu in the semiconductor industry is for making copper-to-copper interconnections. To the best of my knowledge, this is the first time that a flexible material (HOPG) is bonded to a rigid substrate (Si) using a nanoporous metal (NP-Cu) and that NP-Cu is employed for large-area bonding (10 x 10 mm² samples). In consequence, this work opens a new applied research field to use nanoporous metals to bond large areas in the semiconductor industry.

7.2. FUTURE WORK

The following section presents ideas to expand the research I performed for this dissertation.

7.2.1. Thermal properties of epitaxially-grown Ga₂O₃

The quality of the Ga₂O₃ I measured was not electronic-grade because the growing conditions were not optimized. This is one of the reasons why the defects in the crystalline structure significantly decrease the thermal conductivity. It would be interesting to extend this study by exploring how varying the method and MBE growth conditions (like temperature, pressure, and deposition rate) impact the thermal conductivity of β-Ga₂O₃ using the framework I

proposed. The emphasis would be on how these variations influence defect formation and grain size and, in turn, affect the thermal properties. Such research would pave the way to the fabrication of high-quality electronic devices made with heteroepitaxial grown Ga₂O₃ that incorporates a high thermal conductivity substrate for the thermal management of the devices.

7.2.2. ML methods for data analysis of FDTR experiments

Despite its wide use, ML-based applications to solve thermal problems are still in its infancy. Specifically, even when generalized models have been presented for the analysis of data obtained by TDTR or FDTR, the performance for the prediction of more than three parameters is yet to be improved. Future research should focus on optimization of the hyperparameters and architecture, studying the relative importance of the input data provided for training (i.e., study if phase delay is enough or if more data, such as known parameters, can improve the prediction), and the implementation of methods to remove un-realistic (i.e., a combination of properties that do not exist in materials) data points from the training set. Incorporating physics-based algorithms to prepare the training data is a definite step forward. Otherwise, the models might be trained with physically unrealistic data (e.g., physical properties of materials that do not exist in nature). If progress is made in these areas, ML has the potential to become a powerful tool to estimate the thermal properties of new materials accurately.

7.2.3. HOPG as a heat spreader for the thermal management in mobile electronics

The study of the bonding process of HOPG for heat-spreading applications with CYTOP and NP-Cu highlighted the challenges and potential limitations associated with using these

materials and the need for further research and development to optimize bonding techniques. In the first place, there is a need to explore different bonding parameters such as temperature, pressure, and bonding environment to achieve reliable and uniform bonding between NP-Cu and HOPG and investigate the effect of sintering time and reducing environments on the densification of NP-Cu. In the second place, further optimizing the dealloying process to achieve precise control over the morphology and porosity of NP-Cu and scaling up this process for industrial applications is required. In third place, studying the long-term reliability and stability of the bonded HOPG and substrate assembly under various operating conditions must be tested. This can involve subjecting the assembly to thermal cycling, mechanical stress, and humidity to assess its durability and performance over time. Fourth, given the inherent HOPG interlayer weakness, studying different alternatives to improve both the interlayer strength and the Cu seed layer/HOPG bonding force to increase the mechanical reliability of the heat spreader is needed. If the bonding and HOPG mechanical properties challenges are addressed, the next natural step would be exploring the potential of integrating other functional materials or structures with HOPG for enhanced thermal management. This can include incorporating heat pipes, microchannels, or other cooling mechanisms to improve heat dissipation and temperature uniformity. Given that the current bonding technology is one of the bottlenecks for the thermal management of mobile microprocessors, the development of nanoporous metals-based bonding techniques will facilitate the incorporation of more powerful and reliable microprocessors into consumer products.

APPENDIX A: SUPPLEMENTARY MATERIAL FOR CHAPTER 4

A.1. DETAILS OF THE TDTR SYSTEM

This information has been taken from [211]. The TDTR two-color system consist of a Spectra Physics Ti:Sapphire ($\lambda=800$ nm, 40 nJ/pulse) laser with ~ 150 fs pulse width and a repetition rate of ~ 80 MHz. The beam is split in a probe and a pump beam. The frequency modulation of the pump beam can be controlled by an electro-optical modulator, and is doubled using a BiBO crystal. The probe beam enters a double-pass delay stage before merging its path again with the pump beam. Both collinear beams were focused by a 10X objective lens on the sample. On the surface of the sample, the pump radius was ~ 9.95 μm , while the probe radius was ~ 6.2 μm . The TDTR setup used in this work has available six filters that correspond to 1.2, 2.2, 3.6, 6.3, 8.8 and 11.6 MHz for the modulation frequency. Based on the sensitivity analysis, the data obtained at modulation frequencies of 8.8 and 11.6 Mhz were used for the samples grown on sapphire and SiC, respectively.

For the thermal properties of the susbtrates, I used 2-layered samples to measure these properties. In the case of SiC the through-plane and in-plane thermal conductivities were estimated to be 301.4 ± 36.2 W/m-K and 387.3 ± 46.5 W/m-K, respectively. In the case of sapphire the thermal conductivity was measured as 27.3 ± 2.0 W/m-K. These thermal conductivity values are in the range of the values published in [212, 213]. In addition, the values for the heat capacity were taken from published literature and were 778.8 J/kg-K, 669.3 J/kg-K and 484.8 J/kg-K for sapphire [214], SiC [215] and Ga₂O₃ [216], respectively. Finally, the thermal conductivity of a thin film Al transducer was estimated using the four-point collinear probe method to measure the electrical sheet resistivity and converting that to thermal conductivity using the Wiedemann-Franz Law, and it was measured as 170 W/m-K.

All measurements were performed in the Prof. Samuel Graham's laboratory by Diego Vaca and Luke Yates.

A.2. METHODS TO CALCULATE UNCERTAINTY

One of the challenges while using TDTR is the selection of the appropriate experimental conditions, considering sensitivity with respect to different parameters and how they affect the determination of unknown parameters, i.e., the thermal conductivity and the TBC for the present analysis. More details about the sensitivity analysis of TDTR can be found in our previous publication [23]. For the case of thermal conductivity, the sensitivity is high enough to conclude that the experimental conditions used in the measurements were adequate to estimate an accurate value. However, the sensitivity to TBC is low for these experimental conditions. Because of the low sensitivity of the TBC values, the uncertainty of those measurements was estimated using two methods. The first method is a traditional method which uses a mathematical expression employed in [183]. The second method was a Monte Carlo method [75], which uses a population of 1000 data sets, randomly chosen from a normal distribution. Each data set is fitted with a different group of model parameters to generate a random distribution of possible results. Once the distribution of possible results is obtained, the value that is at the 50th percentile of the distribution is taken as the mean value, whereas the values at the 5th percentile and the 95th percentile were the lower and upper bounds, respectively.

A.3. CALCULATIONS OF THE LATTICE THERMAL CONDUCTIVITY IN THE (-201) DIRECTION

The procedure to calculate the thermal conductivity is described in [176]. In summary, after calculating the IFC's, I solved the linearized form of the Boltzmann Transport Equation

(BTE) using ShengBTE [168], that requires sets of second-order and third-order force constants.

ShengBTE uses Eqs. A1a and A1b to calculate the thermal conductivity tensor

$$\kappa_l^{\alpha\beta} = \frac{1}{k_B T^2 \Omega N} \sum_{\lambda} f_o (f_o + 1) (\hbar \omega_{\lambda})^2 v_{\lambda}^{\alpha} F_{\lambda}^{\beta} \quad (\text{A1a})$$

$$F_{\lambda} = \tau_{\lambda}^0 (v_{\lambda} + \Delta_{\lambda}) \quad (\text{A1b})$$

where κ is the component of the tensor of the thermal conductivity in the cartesian direction α and β , k_B is the Boltzmann constant, T is the temperature, Ω is the volume of the unit cell, N is the number of discrete points of a regular grid in the Brillouin zone ($N = N_1 \times N_2 \times N_3$ q points with q being the wave vector), λ is the phonon mode, f_o is the equilibrium Bose-Einstein, \hbar is de modified Plank constant, ω is the frequency, v is the group velocity, F is a linearized form of the BTE, τ is the relaxation time, v is the group velocity and Δ is a term that measures how much or the population of a specific phonon mode deviates from the relaxation time approximation.

The software calculates the thermal conductivity tensor for the Ga₂O₃ crystal structure in this form:

$$\kappa_{ij} = \begin{pmatrix} \kappa_{xx} & \kappa_{xy} & \kappa_{xz} \\ \kappa_{yx} & \kappa_{yy} & \kappa_{yz} \\ \kappa_{zx} & \kappa_{zy} & \kappa_{zz} \end{pmatrix} \quad (\text{A2})$$

The directions (100) and (010) coincide with \hat{x} and \hat{y} , respectively, whereas (001) is at an angle β with respect to \hat{x} and orthogonal to \hat{y} .

For example, the tensor that I obtained for the 81 nm-thick samples was (units are W/m-K):

$$\kappa_{ij} = \begin{pmatrix} 5.94 & 0 & 0.14 \\ 0 & 12.93 & 0 \\ 14.33 & 0 & 8.06 \end{pmatrix}$$

For the calculation of the thermal conductivity in the (-201) direction I used Eq. A3

$$\kappa_{(-201)} = K_{xx} \sin^2\gamma + K_{xz} \sin 2\gamma + K_{zz} \cos^2\gamma \quad (\text{A3})$$

where $\gamma = 167.7^\circ$, that corresponds to the angle between \hat{x} and (-201)

Using Eq. A3 and the tensor for the 81 nm-thick sample, the thermal conductivity κ calculated in the (-201) direction was 7.9 W/m-K. The same approach was followed for the 119 nm-thick sample.

For the calculation of the reduced thermal conductivity as a consequence of the defects, I introduced the respective scattering rates before obtaining the thermal conductivity tensor.

A.4. CALCULATIONS OF THE DMM MODEL

For the calculation of the thermal boundary conductance for energy moving from material 1 (Ga_2O_3) to material 2 (substrate), $h_{BD}^{1 \rightarrow 2}$, I employed the approach found in [217] (Eq. A4), where the integration is done in the wave vector space.

$$h_{BD}^{1 \rightarrow 2} = \frac{1}{8\pi^2} \sum_j \int_{q_{j,1}} \hbar \omega_{j,1}(q) q_{j,1}^2 |v_{j,1}(q_{j,1})| \frac{df_o}{dT} \zeta^{1 \rightarrow 2} dq_{j,1} \quad (\text{A4})$$

Where the summation is performed over the all phonon branches, j , \hbar is de modified Plank constant, f_o is the equilibrium Bose-Einstein distribution, q is the wave vector, ω is the frequency, v is the group velocity defined as $d\omega/dq$, and $\zeta^{1 \rightarrow 2}$ is the transmission coefficient from material 1 to material 2. The transmission coefficient was calculated with Eq. A5.

$$\zeta^{1 \rightarrow 2}(T) = \frac{\sum_j \int_{q_{j,2}} \hbar \omega_{j,2}(q) q_{j,2}^2 |v_{j,2}(q_{j,2})| f_o dq_{j,2}}{\sum_j \int_{q_{j,2}} \hbar \omega_{j,2}(q) q_{j,2}^2 |v_{j,2}(q_{j,2})| f_o dq_{j,2} + \sum_j \int_{q_{j,1}} \hbar \omega_{j,1}(q) q_{j,1}^2 |v_{j,1}(q_{j,1})| f_o dq_{j,1}} \quad (\text{A5})$$

Equations A4 and A5 require the knowledge of the phonon dispersion curves of each material. These curves were obtained from first principles calculations in the case of Ga_2O_3 and from the Materials Project web site, in the case of SiC and sapphire. The discrete phonon dispersion

curves were fit to a 4th order polynomial equation for each phonon branch, and these relations were used to obtain all the inputs needed to calculate the TBC.

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