

**MILLIMETER-WAVE CIRCUIT TECHNIQUES FOR ENERGY-  
EFFICIENT POWER GENERATION FOR WIRELESS  
COMMUNICATIONS**

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**MILLIMETER-WAVE CIRCUIT TECHNIQUES FOR ENERGY-  
EFFICIENT POWER GENERATION FOR WIRELESS  
COMMUNICATIONS**

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To honesty, hard work, and dedication... and to my mom for all her unconditional love and support!

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It has been a long and wild ride, and now, the inevitable face of the future past appears to be gazing in the rearview mirror. I started my graduate studies thirteen years ago back in 2010 at the University of Florida; I was just a young graduate student figuring out my way into adulthood. My times at UF were happy times, full of discovering a brand-new world personally and professionally. Those days, I kept busy aiming to figure out the intimidating equipment found in the cleanroom and using my newfound knowledge about MEMS fabrication to create small batteries for medical applications. That was my first attempt at becoming a doctor, a PhD doctor that is, and back then becoming the first in my family to do so seemed like an honorable pursuit. Family and honor are two beliefs that keep my personal quests honest, but in its infinite wisdom, the universe found a better path for me, and my story at UF ended abruptly after four years.

After a short stint at the Army Research Lab, I moved to Atlanta to begin my PhD for the second time at the Georgia Institute of Technology. I was 33 years of age and had left behind what it seemed back then like my entire life: friends, family, and a life partner. Georgia Tech for me was not a happy beginning to a world full of possibilities, but a second chance to fulfill my dreams. It was hard, it was lonely, but choosing to attend Georgia Tech was probably one of the best decisions I ever made in my life. At Georgia Tech, I discovered a renewed passion for circuits, design, and semiconductors. I also found a sense of purpose and a clear vision for what I wanted my professional life to look like.

The road to here has been a long and winding one, from a small farm town in Venezuela to the hallways of TSRB, and the support of family, friends, colleagues, lab mates, teachers,

mentors, partners, and others made my journey possible and quite enjoyable. Therefore, I have a laundry list of people that I would like to acknowledge, but I will start from the deepest regions of my heart and soul and move outwards.

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## LIST OF SYMBOLS AND ABBREVIATIONS

ACLR	Adjacent Channel Leakage Ratio
AWG	Arbitrary Waveform Generator
BEOL	Back End of Line
CG	Common-Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CS	Common-Source
CW	Continuous-Wave
DC	Direct Current
DE	Drain Efficiency
DPD	Digital Pre-Distortion
DUT	Device Under Test
EIRP	Equivalent Isotropic Radiated Power
EVM	Error Vector Magnitude
FET	Field-Effect Transistor
FoV	Field of View
LNA	Low Noise Amplifier
Mm-Wave	Millimeter-Wave
MIMO	Multiple-Input Multiple-Output
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAE	Power Added Efficiency

PAPR Peak-to-Average Power Ratio  
PBO Power Back-Off  
PCB Printed Circuit Board  
PLL Phase-Locked Loop  
QAM Quadrature Amplitude Modulation  
RF Radio Frequency  
RX Receiver  
SOI Silicon-on-Insulator  
SRF Self-Resonant Frequency  
T-line Transmission line  
TRX Transceiver  
TS Test Structure  
TX Transmitter  
VNA Vector Network Analyzer

## SUMMARY

5 billion People are connected to a wireless network through handheld devices, computers, and wearable devices. It is envisioned that the new generation millimeter-Wave (mm-Wave) network infrastructure will deliver multi-gigabit connectivity and enough channel capacity so that the user experience will be drastically improved, particularly in highly populated areas. In addition, future 5G and 6G enabled electronics that take advantage of the mm-Wave and sub-THz frequency spectrum will provide the technology necessary to achieve the full potential of the market opportunity in some consumer electronic areas, such as virtual/augmented reality, health care monitoring, and wearables. In addition, there are plenty of mission-critical Department of Defense (DoD) applications where mm-Wave and sub-THz hardware electronics are indispensable.

New generation network infrastructure deployment targeted for 5G and 6G wireless communication is bringing new challenges to circuit and system designers that are yet to be addressed by conventional semiconductor technologies and circuit topologies. One of the main challenges is that battery energy density is not catching up to the power consumption needs of current electronic devices, particularly when the battery is constrained to a small form factor dictated by the size of consumer electronic. In addition, modern satellite constellations employ large transmitter arrays, which are exceptionally power hungry and rely on battery and solar cell power to operate. Moreover, network infrastructure such as cellphone towers and base stations, which are tethered to the electrical grid and do not have any battery constraints, often are extremely expensive to operate due to the high electricity and thermal management cost.

Power amplifiers (PA) and transceiver (TRX) blocks are the most important components for any wireless data transmission system since they dictate the overall system efficiency, communication distance, bandwidth, and data rate. In addition, more than 80% of the energy in wireless systems is consumed by power amplifiers and this number will increase as newer network generations are being adopted. Therefore, for the next-generation networks (5G, 6G, and beyond) to be successfully deployed, new circuit design techniques and circuit/system topologies will need to be reimaged. The core of my research focuses on developing innovative system and block level architectures and design techniques that drastically increase the efficiency, linearity, and overall performance of PA/TRX blocks that will support next-generation mm-Wave/sub-THz wireless networks.

First, we propose a cascadable self-similar high-order on-chip rat race hybrid coupler architecture that supports wideband operation by cancelling out the output phase imbalance and magnitude mismatch. Our proposed cascaded rat-race architecture can be further realized using a higher order implementation to extend the bandwidth of operation. Our cascaded rat-race mm-Wave implementations can support multi-band multi-standard 5G communication systems. This work was presented in the *IEEE MTT-S International Microwave Symposium in 2018* [1].

Secondly, by leveraging the block level co-design we implemented a wideband vector modulator phase shifter integrated with a power amplifier, pre-driver, and input/output Marchand balun covering a frequency range from 40GHz to 60GHz. In our proof-of-concept demonstration, the vector modulator provides a truly 0 magnitude and 40dB of dynamic range while covering 360° of phase interpolation. The vector modulator is able to deliver sufficient output power to drive the next stage electronics.

Thirdly, we present a sub-THz regenerative low power miniature 2-way radio integrated with an on-chip patch antennas array operating at 150GHz achieving a bidirectional chip-to-chip over the air link of 70cm. To achieve this level of performance, we propose an on-chip patch antenna design methodology that greatly increases radiated power and efficiency. In addition, we introduce an integrated low-loss Marchand balun-based coupling network for oscillators that enhances power generation efficiency. Our proof-of-concept achieves the highest efficiency reported of all the silicon-based sub-THz transceivers. This work was published in the *IEEE Journal of Solid-State Circuits in 2022 [2]*.

The last part of this dissertation presents a new power amplifier topology. Commercially available Power amplifiers cores were developed in the 1930s and have not changed much since then. More importantly, they already reached the maximum theoretical efficiency limit and since 2015 only small incremental improvements in efficiency and linearity have been obtained. We propose a new amplifier topology called the dual-drive PA, which increases the achievable energy efficiency, linearity, and output power previously achieved in a conventional common-source/common-gate PA. Furthermore, we implement a proof-of-concept prototype that achieves the highest reported efficiency for a 2-stage PA in silicon at mm-Wave frequencies. This work was presented in the *2021 IEEE International Solid- State Circuits Conference (ISSCC) [3]*.

## CHAPTER 1. INTRODUCTION

*“Honesty is a very expensive gift. Don’t expect it from cheap people.”*

*– Warren Buffett*

*“No legacy is so rich as honesty.”*

*– William Shakespeare*

Advances in semiconductor fabrication technology, particularly lithographic processes, have allowed for a reduction in the transistor minimum feature size. This has resulted in faster and densely packed transistors operating at lower voltage levels, which has allowed engineers to design complex mixed-signal/RF circuitry for new wireless system platforms with an unimaginable degree of integration and functionality. Furthermore, back-end-of-line (BEOL) improvements in the fabrication process is providing designers with low loss metal and dielectric layer stacks allowing the on-chip integration of radio-frequency (RF) passive structures, such as transmission lines, couplers, and antennas. As a result, in the past few decades there has been a push from industry and academia to create wireless systems for sensor networks, IoT devices, and consumer electronics that employ mm-Wave frequencies. These wireless systems are targeted towards the health care industry, manufacturing, consumer products, Department of Defense (DoD) related applications, and wireless tags, among others.

5G enabled systems and devices will create a huge impact across multiple industries, such as automotive, health care, consumer products, space, scientific, and

military. The 5G spectrum has already been licensed and portioned across the globe, and the main were allocated from bellow 6GHz for 5G FR1 and from 24 to 71GHz for 5G FR2. For 5G systems to be successfully deployed, broadband or reconfigurable hardware that operates throughout the entire 5G spectrum is needed. Some of the main advantages offered by 5G networks are the compact hardware size due to the high level of integration provided by the smaller wavelength at higher frequencies. Moreover, there are specific frequencies in which systems can operate that offer particular advantages. For example, secure over the air networks can be implemented at 60GHz due to the high oxygen absorption at this frequency. Additionally, 5G wireless networks are perfectly suited for user dense area and high Gb/s wireless communication. In the same manner, the 6G and sub-THz spectrum is opening the doors to new opportunities to create miniaturized systems on-chip with some degree of functionality that integrate on-chip network connectivity and chip-to-chip sensing capabilities.

One of the biggest challenges for new generation wireless networks and systems operating at mm-Wave and sub-THz frequencies is transmitter power and efficiency. In most transceiver designs, power amplification blocks, which includes power amplifiers and oscillators, dominate the overall system efficiency, thermal performance, and data rate. Moreover, it is extremely difficult to transmit a signal efficiently over the air at mm-Wave and sub-THz frequencies due to the higher path losses. My PhD research at Georgia Tech focuses on leveraging modern semiconductor technology nodes to explore new circuit and design techniques that will increase the efficiency, bandwidth, and level of integration that will address the beforementioned challenges of future wireless systems. The main contributions of this dissertation are summarized below.

1. We propose a cascadable self-similar high-order rat-race hybrid coupler architecture supporting wideband operation which inherently cancels the output phase imbalance and reduces the magnitude mismatch through cascading, enabling a substantial coupler bandwidth extension. Our proposed rat-race architecture exhibits a very compact size, low insertion loss, accurate phase and magnitude balance, and its mm-Wave implementations can support multi-band multi-standard 5G communication systems.
2. To increase radiated power of on-chip sub-THz systems, we propose an on-chip patch antenna array design methodology which consists of a new adaptive metal-fill placement approach that largely reduces antenna losses and detuning present in sub-THz/THz frequency antennas without the need for bulky silicon lenses.
3. We propose an integrated low-loss Marchand balun-based coupling network as a coupling mechanism for fundamental power oscillators that guarantees the correct phase synchronization without ambiguity between the coupled oscillators.
4. To demonstrate the feasibility of ultra-efficient on-chip wireless systems at sub-THz frequencies, we propose a new 150GHz regenerative low power miniature 2-way radio integrated with on-chip antennas. The low power radio is based on a reconfigurable fundamental oscillator array that can be used as a sub-THz source in the transmitter (TX) mode and as a sub-THz super-regenerative detector in the receiver (RX) mode. Our proof-of-

concept prototype achieves the highest efficiency reported of all the silicon-based sub-THz transceivers (TRX) in the 150GHz range.

5. To increase power amplifier efficiency and linearity, which are key performance metrics for next generation wireless data systems, we propose a new dual-drive PA topology. This new topology increases the achievable energy efficiency, linearity, and output power of the PA core. Our proposed dual-drive PA core architecture employs a dual-drive coupling network to drive the gate and source of the transistors that form part of the PA core, which fundamentally increases the device drain efficiency beyond that of the common-source topology. A prototype of our dual-drive PA achieves the highest reported PAE and DE for a 2-stage PA in silicon at mm-Wave frequencies.

The remainder of this dissertation is organized as follows:

Chapter 2 presents the theoretical analysis and ultra-compact on-chip implementation of a cascaded self-similar high-order rat-race hybrid coupler architecture supporting wideband operation. The theoretical analysis presented in this chapter demonstrates that our cascaded rat-race architecture inherently cancels the output phase imbalance and reduces the magnitude mismatch through cascading, enabling a substantial coupler bandwidth extension. The cascaded rat-race architecture can be extended to a higher order (nth-order) implementation. Our proposed rat-race architecture exhibits a very compact size, low insertion loss, accurate phase and magnitude balance, and its mm-Wave implementations can support multi-band multi-standard 5G communication systems.

Chapter 3 presents a vector modulator phase shifter covering a frequency range from 40GHz to 60GHz and integrated with a power amplifier and pre-driver. The vector modulator covers  $360^\circ$  of phase interpolation while providing a truly 0 magnitude and 40dB of dynamic range for phased array systems. The vector modulator is implemented with an input and output Marchand balun, pre-amplifier, vector modulator core, and a 2-stage power amplifier, which provides the desired phase interpolation while delivering sufficient output power to drive the next stage electronics.

Chapter 4 presents a regenerative low power miniature 2-way radio integrated with an on-chip patch antennas array operating at 150GHz. The sub-THz low power bidirectional radio is based on a reconfigurable fundamental oscillator array that can be used as a source in transmitter mode and as a power detector in the receiver mode. Our bidirectional transceiver supports on-off keying (OOK) modulation. Moreover, we present a novel coupling technique based on a low-loss integrated Marchand balun-based network that guarantees the correct phase synchronization between oscillators. Our proof-of-concept low-power bidirectional transceiver prototype achieves the highest efficiency reported of all the silicon-based sub-THz transceivers without using a silicon lens. Moreover, wireless chip-to-chip wireless data transferred was demonstrated at a distance of 70cm.

Chapter 5 presents a new dual-drive PA topology that increases the achievable energy efficiency, linearity, and output power previously achieved in a conventional common-source/common-gate PA. The dual-drive topology enhances the performance of the PA by driving the gate and source of the transistor out of phase, which fundamentally increases the drain efficiency and linearity of the device. Theoretical mathematical

expressions are derived for the dual-drive operation that demonstrate the efficiency enhancement due to the concurrent driving of the gate and source of the device.

Chapter 6 presents a proof-of-concept prototype of a 2-stage Dual-Drive power amplifier at 38GHz using the 45nm RFSOI process from GlobalFoundries that achieves the highest reported efficiency for a 2-stage PA in silicon at mm-Wave frequencies.

Finally, Chapter 7 summarized this dissertation.

**CHAPTER 2. A CASCADED SELF-SIMILAR HIGH-ORDER  
RAT-RACE HYBRID COUPLER ARCHITECTURE:  
THEORETICAL ANALYSIS AND A COMPACT KA-BAND  
IMPLEMENTATION IN CMOS SOI**

This chapter presents the theoretical analysis of a cascaded self-similar high-order rat-race hybrid coupler architecture supporting wideband operation and its ultra-compact fully integrated implementation. Our theoretical analysis demonstrates that our cascaded rat-race architecture inherently cancels the output phase imbalance and reduces the magnitude mismatch through cascading, enabling a substantial coupler bandwidth extension. The cascaded rat-race can be extended to a higher order (nth-order) implementation with a total of  $2^{2 \times n}$  individual rat-races ( $n = 1$  for a 2<sup>nd</sup>-order implementation). Our proposed rat-race architecture exhibits a very compact size, low insertion loss, accurate phase and magnitude balance, and its mm-Wave implementations can support multi-band multi-standard 5G communication systems.

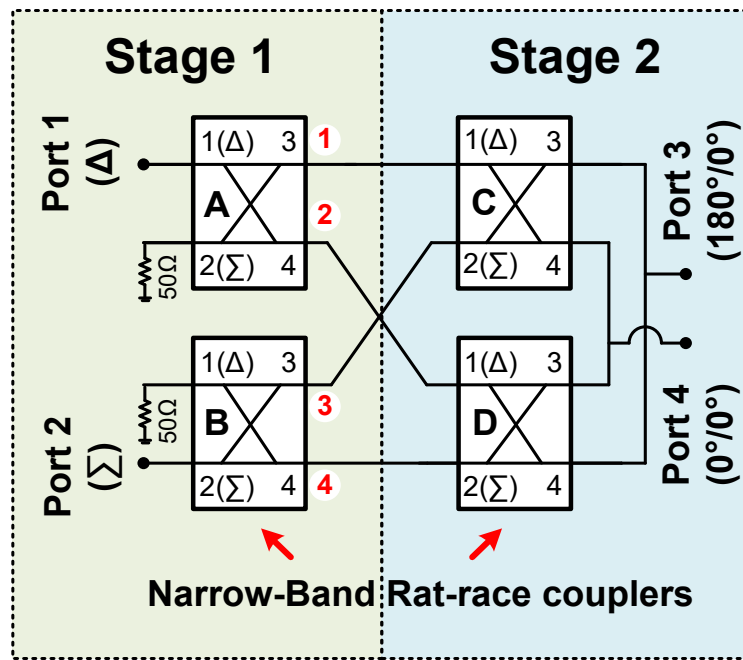
As a proof-of-concept example, we implement a 2<sup>nd</sup>-order cascaded rat-race coupler covering 22.6-43.4 GHz in the GlobalFoundries 45nm CMOS SOI process, simultaneously supporting the 24, 27, 37, and 39GHz mm-Wave 5G bands without any band-selection switches or tunable elements. Based on our measurement results, the cascaded rat-race coupler design achieves a less-than 5° phase error, less-than 1dB magnitude mismatch, an average insertion loss of only 2.5dB, and better-than -10dB input matching across the entire Ka-band.

## 2.1 Introduction

Monolithic passive networks and structures, unlike active devices, often do not benefit from the continuous node scaling in silicon fabrication processes. Over the past few decades, most performance improvements in RF/mm-Wave circuits have been related to active devices scaling by decreasing the transistor peripherals, increasing the transistor  $f_t/f_{max}$  [4]. For on-chip passive structures at mm-wave frequencies, advances in back-end-of-the-line (BEOL) processes have led to marginal performance improvements yielding low Q inductors and capacitors and lossy transformers [5]. As a result, in many RF/mm-wave integrated circuits, on-chip passives often consume large and expensive chip real-estate and limit the system-level performance, including bandwidth, gain, and energy-efficiency [6-9]. These various challenges are positioning passive network as a major technology differentiator in RF/mm-wave circuit and system designs.

Among popular passive structures,  $180^\circ$  hybrid couplers are fundamental and widely used in RF/mm-Wave systems requiring passive in-phase and differential signal generation [10]. Although various popular passive structures exist for broadband differential signal generations, e.g., Marchand balun [11] and transformer balun [12], many of them are inherently 3-port networks and cannot be used in applications requiring a true 4-port coupler such as antenna array beamforming [13-16]. In [17], a 94GHz transceiver for imaging applications is presented where a hybrid coupler is used for I/Q generation. Moreover, the Butler matrix has been widely used as part of beam forming systems where a network composed of couplers is employed to form the antenna beam in a specific direction [18-20]. Among  $180^\circ$  hybrids, the rat-race (hybrid ring) coupler is inherently compatible with coplanar fabrication technologies, making it a highly desired solution for

on-chip integration [21]. Conventionally the design of a rat-race coupler requires multiple segments of  $\lambda/4$  transmission lines (t-lines) [22]. Therefore, a traditional rat-race implemented on a CMOS chip is prohibited in terms of cost and silicon area even for many mm-Wave bands. There have been some reported compact broadband rat-race couplers yet at the expense of severely degraded insertion loss, amplitude/phase imbalance, or complex 3D fabrication processes [23-29].



**Figure 2-1 Equivalent circuit schematic of the folded-inductor cascaded rat-race coupler.**

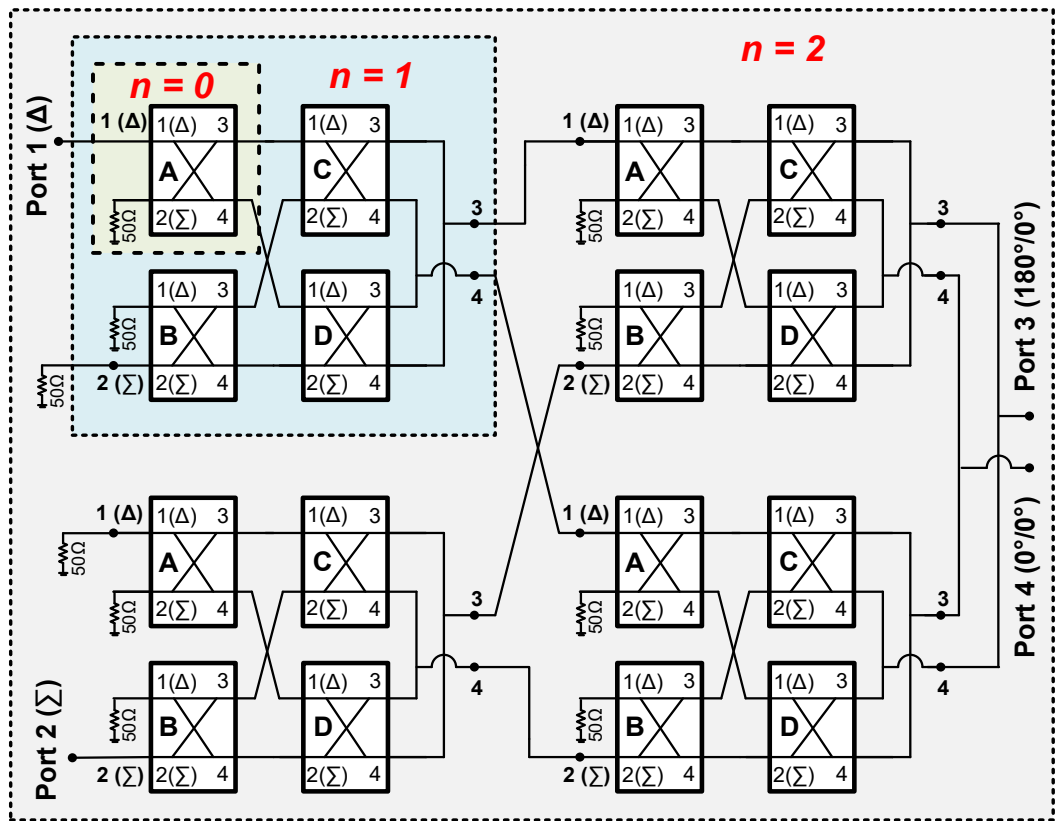
To address the above-mentioned challenges, we propose a cascaded  $180^\circ$  rat-race coupler architecture that employs narrow-band hybrid couplers as building blocks to form a high-order self-similar  $180^\circ$  coupler network. We demonstrate theoretically that our passive network topology achieves a substantial bandwidth extension by cancelling the phase imbalance and reducing the magnitude mismatch while achieving a low insertion loss and compatibility with using any narrow-band  $180^\circ$  hybrid coupler as building blocks.

As a proof-of-concept a 2<sup>nd</sup>-order cascaded 180° rat-race coupler is implemented in a 45nm SOI process based on a previously reported narrow-band folded inductor-based rat-race coupler [30]. This paper presents the passive coupler details, complete theoretical analysis and simulations on phase cancelling and magnitude reduction for cascaded rat-races of different orders, 3-D electromagnetic (EM) simulations, and measurement results of 10 independent samples to demonstrate the robustness of our proposed architecture. Our proposed cascaded rat-race coupler achieves a less-than 1dB magnitude mismatch from 19.4 to 43.4GHz, less-than 5° phase mismatch from 25.6 to 49GHz, and a minimum insertion loss of 2.3dB at 33 GHz, simultaneously covering multiple 5G mm-Wave bands of 24, 28, 37, and 41GHz for future multi-band multi-standard wireless communications.

## 2.2 Theoretical Analysis of a Cascaded Self-Similar Rat-Race Hybrid Coupler

Figure 2-1 shows the general circuit diagram of a 2<sup>nd</sup>-order design (n=1) of our proposed cascaded rat-race coupler. As a proof-of-concept, here we present a 2<sup>nd</sup>-order implementation (n=1) comprising four narrow-band 180° couplers that together form a true 4-port coupler network [1]. For this 2<sup>nd</sup>-order design, the rat-race coupler network can be divided into two stages, where each stage consists of two narrow-band rat-race couplers (Figure 2-1). For stage 1, each individual coupler has one of its input ports terminated with a 50Ω isolation resistor. To obtain the correct magnitude and phase difference at the output (0°/0° or 0°/180°), port 3 and port 4 of the individual rat-race couplers are connected to the rat-races in stage 2, as shown in Figure 2-1. It will be shown that this cascaded structures greatly suppresses the magnitude mismatch and phase imbalance across a broad bandwidth due to the high-pass or low-pass response of the different rat-race signal paths [31, 32]. Specifically, the appropriate combination of the signals from stage 1 to stage 2 inherently

cancels the phase error and reduces the magnitude. It is important to note that the phase and magnitude error cancelling effects are correlated, and thus this cancelling effect is limited in most cases by the magnitude mismatch across frequencies of each individual rat-race. Our proposed cascadable rat-race is a self-similar structure, and it can be extended to a general  $n$ th-order implementation with a total  $2^{2 \times n}$  individual rat-race blocks, as shown in Figure 2-2.



**Figure 2-2 Block diagram of a 3rd order ( $n = 2$ ) cascaded rat-race.**

### 2.2.1 Small Signal Analysis

To analyze the magnitude mismatch reduction and phase imbalance cancelling by our proposed cascaded rat-race coupler structure, we will compare the mismatch of a single

rat-race with that of a cascaded rat-race coupler. In our analysis we use the subscripts ‘s’ and ‘c’ to represent the S-parameters of a single and cascaded rat-race coupler, respectively. We assume that the four-unit rat-race couplers are identical designs with the same magnitude/phase mismatches at corresponding ports. It is important to note that this is a general analysis and can be used with any rat-race structure.

We will first consider the magnitude and phase mismatch of a single rat-race. Its magnitude and phase mismatch can be calculated using the 4-port S-parameters in (1-1)-(1-4). Additionally, we can define the Common-Mode (CM) and Differential-Mode (DM) outputs of a single stage rat-race for the  $\Delta$ -Port and  $\Sigma$ -Port using (1-5)-(1-8), as

$$|\Delta\text{-Port}_s|_{\text{mismatch}} = ||S_{31_s}| - |S_{41_s}|| \quad (1-1)$$

$$|\Sigma\text{-Port}_s|_{\text{mismatch}} = ||S_{32_s}| - |S_{42_s}|| \quad (1-2)$$

$$\angle\Delta\text{-Port}_s|_{\text{mismatch}} = |\angle(S_{31_s}) - \angle(S_{41_s})| \quad (1-3)$$

$$\angle\Sigma\text{-Port}_s|_{\text{mismatch}} = |\angle(S_{32_s}) - \angle(S_{42_s})| \quad (1-4)$$

$$\text{CM}_{\Delta_s} = \frac{1}{2}(|S_{41_s}| + |S_{31_s}|) \quad (1-5)$$

$$\text{DM}_{\Delta_s} = \frac{1}{2}(|S_{41_s}| - |S_{31_s}|) \quad (1-6)$$

$$\text{CM}_{\Sigma_s} = \frac{1}{2}(|S_{42_s}| + |S_{32_s}|) \quad (1-7)$$

$$\text{DM}_{\Sigma_s} = \frac{1}{2}(|S_{41_s}| - |S_{32_s}|) \quad (1-8)$$

Furthermore, for a single stage rat-race, equations (1-5)-(1-8) can be used to relate the 4-port S-parameters as expressed in (1-9)-(1-12), as

$$S_{41_s} = (CM_{\Delta_s} + DM_{\Delta_s})e^{j\pi} \quad (1-9)$$

$$S_{31_s} = (CM_{\Delta_s} - DM_{\Delta_s})e^{j0} \quad (1-10)$$

$$S_{42_s} = (CM_{\Sigma_s} + DM_{\Sigma_s})e^{j\pi} \quad (1-11)$$

$$S_{32_s} = (CM_{\Sigma_s} - DM_{\Sigma_s})e^{j\pi} \quad (1-12)$$

Next, we will use our proposed 2nd-order cascaded rat-race coupler as an example to analyze the magnitude and phase mismatches after cascading. Considering the losses through each signal path (Figure 2-1), we can first find the magnitude mismatch of the cascaded rat-race. For the magnitude mismatch analysis, we assume that the phase mismatch of each individual rat-race is negligibly small compared to the amplitude mismatch. The resulting analysis will aid in understanding the bandwidth extension and mismatch reduction attained by our cascaded structure. For the 2<sup>nd</sup>-order cascaded rat-race, the magnitude mismatch is given by (1-13)-(1-14), which can be further expressed using the Common-Mode and Differential-Mode output equations (1-9)-(1-12) of the single rat-race, as shown below

$$\begin{aligned} & |\Delta\text{-Port}_c|_{\text{mismatch}} \\ & = (|S_{31_s}| \times |S_{41_s}| + |S_{41_s}| \times |S_{31_s}|) \end{aligned}$$

$$\begin{aligned}
& -(|S_{31_s}| \times |S_{31_s}| + |S_{41_s}| \times |S_{41_s}|) \\
& = [2 \times (\text{CM}_{\Delta_s} - \text{DM}_{\Delta_s}) \times (\text{CM}_{\Delta_s} + \text{DM}_{\Delta_s})] \\
& - [(\text{CM}_{\Delta_s} - \text{DM}_{\Delta_s})^2 \times (\text{CM}_{\Delta_s} + \text{DM}_{\Delta_s})^2] \\
& = (2 \times \text{DM}_{\Delta_s})^2 \tag{1-13}
\end{aligned}$$

$$\begin{aligned}
& |\Sigma\text{-Port}_c|_{\text{mismatch}} \\
& = (|S_{32_s}| \times |S_{42_s}| + |S_{42_s}| \times |S_{32_s}|) \\
& - (|S_{32_s}| \times |S_{32_s}| + |S_{42_s}| \times |S_{42_s}|) \\
& = [2 \times (\text{CM}_{\Sigma_s} - \text{DM}_{\Sigma_s}) \times (\text{CM}_{\Sigma_s} + \text{DM}_{\Sigma_s})] \\
& - [(\text{CM}_{\Sigma_s} - \text{DM}_{\Sigma_s})^2 \times (\text{CM}_{\Sigma_s} + \text{DM}_{\Sigma_s})^2] \\
& = (2 \times \text{DM}_{\Sigma_s})^2 \tag{1-14}
\end{aligned}$$

Equations (1-13) and (1-14) demonstrate that the magnitude mismatch of a 2<sup>nd</sup>-order cascaded rat-race coupler will be equal to the square of the magnitude mismatch of a single rat-race. Since the magnitude mismatch of a single rat-race is already a small quantity with its magnitude less than 1 in the band of operation, there will always be a magnitude mismatch reduction by employing our proposed cascaded structure. Furthermore, it can be shown that cascading to higher-order configurations will further reduce the magnitude mismatch at the expense of total insertion loss, as

$$|\Delta - Port_c|_{mismatch} = (2 \times DM_{\Delta_s})^{2^n} \quad (1-15)$$

Figure 2-3 shows the simulated magnitude error for cascaded rat-races of different orders ( $n = 0,1,2,3$ ), where  $n = 0$  is for a single narrow-band rat-race coupler. The benefit of using a cascaded topology can be clearly seen in this figure where the magnitude error is reduced from 3dB for a single rat-race to 1 dB for  $n = 1$  and 0.1dB for  $n = 2$ .

Phase mismatch suppression in hybrid couplers is of particular interest, since phase imbalances can degrade the signal integrity along the signal path and performance in various beam-former/beam-steering systems. Similar to the amplitude mismatch analysis, we can analyze the phase imbalance of our proposed cascaded rat-race coupler using the S-parameters of a single rat-race. This will aid in comparing the phase mismatch improvements offered by the cascaded structure over any single narrow-band rat-race. We begin our analysis by assuming that the magnitude mismatch at the output ports of the single rat-race is negligibly small compared to the phase mismatch. For the  $\Delta$ -Port of a single rat-race, we can define the phase mismatch using equation (1-16) as  $2\delta$  and the arithmetic average of the output phases as  $\varepsilon$ , as shown in (1-17). Based on (1-16) and (1-17), the phase of each signal path for the single and cascaded rat-race are given as

$$\delta = \frac{1}{2}(\angle S_{41_s} - \angle S_{31_s}) \quad (1-16)$$

$$\varepsilon = \frac{1}{2}(\angle S_{41_s} + \angle S_{31_s}) \quad (1-17)$$

$$\angle S_{41_s} = \varepsilon + \delta \quad (1-18)$$

$$\angle S_{31_s} = \varepsilon - \delta \quad (1-19)$$

$$\angle(S_{31_s} \times S_{41_s}) = (\varepsilon + \delta) + (\varepsilon - \delta) = 2\varepsilon \quad (1-20)$$

$$\angle(S_{41_s} \times S_{31_s}) = (\varepsilon - \delta) + (\varepsilon + \delta) = 2\varepsilon \quad (1-21)$$

$$\angle(S_{31_s} \times S_{31_s}) = (\varepsilon - \delta) + (\varepsilon - \delta) = 2(\varepsilon - \delta) \quad (1-22)$$

$$\angle(S_{41_s} \times S_{41_s}) = (\varepsilon + \delta) + (\varepsilon + \delta) = 2(\varepsilon + \delta). \quad (1-23)$$

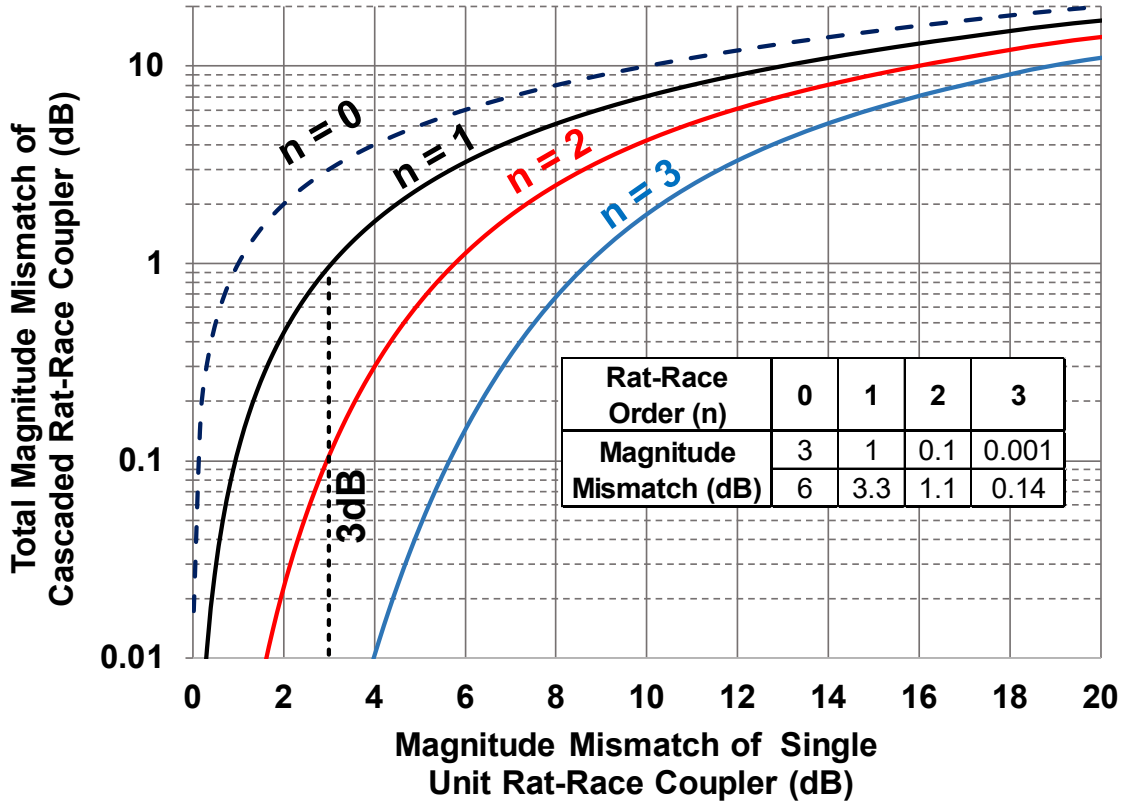
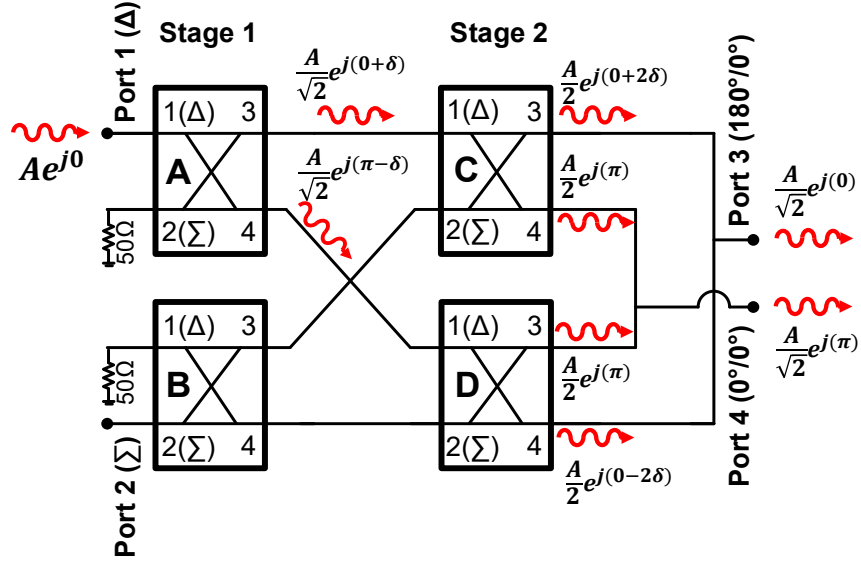


Figure 2-3 Total simulated magnitude mismatch for an nth-order cascaded rat-race coupler versus magnitude mismatch of a single unit rat-race coupler. The single unit rat-race coupler uses the folded-transformer coupler design presented in [30].



**Figure 2-4 Schematic of a 2nd order cascaded rat-race showing the phase error related to each signal path and the inherent error cancellation out the output ports.**

Next, we will investigate the phase mismatch using (1-20)-(1-23) to compute the phase error through each signal path. As shown in Figure 2-4, the input signal at the  $\Delta$ -Port passes through two single stage rat-races in the case of a 2-stage design, and then the outputs of the last stage are combined to obtain the desired phases and magnitudes. The phase mismatch at each of the outputs of the cascaded rat-race can be found as follows.

$$(\angle S_{41_c})_{mismatch}(cascaded\ rat - race)$$

$$= \tan^{-1} \left[ \frac{\sin(2\varepsilon - 2\varepsilon)}{1 + \cos(2\varepsilon - \varepsilon)} \right] = 0 \quad (1-24)$$

$$(\angle S_{31_c})_{mismatch}(cascaded\ rat - race)$$

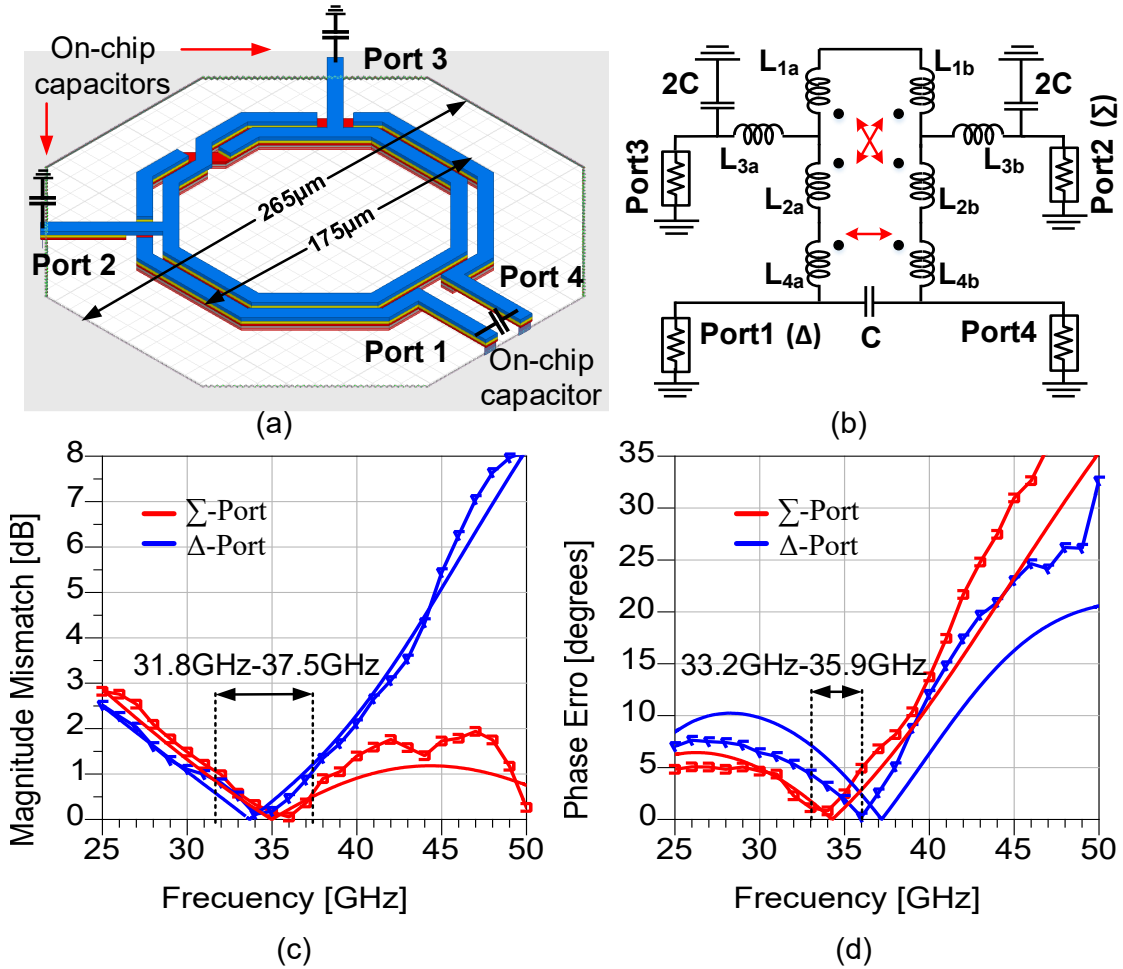
$$= \tan^{-1} \left[ \frac{\sin[2(\varepsilon - \delta) - 2(\varepsilon + \delta)]}{1 + \cos[2(\varepsilon - \delta) - (\varepsilon + \delta)]} \right] = -2\delta. \quad (1-25)$$

It is important to note that the S-parameters in (1-24)-(1-25) represent the S-parameters of a 2<sup>nd</sup>-order cascaded rat-race coupler. Then, we can compute the total phase mismatch between the outputs of ports 3 and 4 using (1-21)-(1-25) by subtraction of the output phases of port 3 and 4 as

$$\begin{aligned}
 & (\angle S_{41_c} - \angle S_{31_c})(\text{cascaded rat - race}) \\
 & = [2(\varepsilon + \delta) - 2\delta] - [2\varepsilon - 0] = 0^\circ \qquad \qquad \qquad \mathbf{(1-26)}
 \end{aligned}$$

This first order analysis shows the phase mismatch cancelling effect offered by cascading multiple rat-race couplers. The same analysis can be performed on the  $\Sigma$ -Port to yield the same zero-phase mismatch result obtained in (1-26). Note that the above equation (1-26) means that the phase mismatch of the unit rat-race couplers will cancel each other and lead to ideally zero phase error for our proposed cascaded rat-race coupler as long as the magnitude mismatch is small, and the unit rat-race couplers have identical magnitude and phase mismatches at corresponding ports. This inherent phase cancelling error can also be analyzed using Figure 2-4, where the phase error added by each stage is equal to  $\pm\delta$ . Therefore, when adding the signals correctly the total phase imbalance at the output will completely cancel out. However, magnitude mismatch in each unit rat-race couplers and process/fabrication variations among the unit rat-race couplers degrade such phase error cancellation in practice.

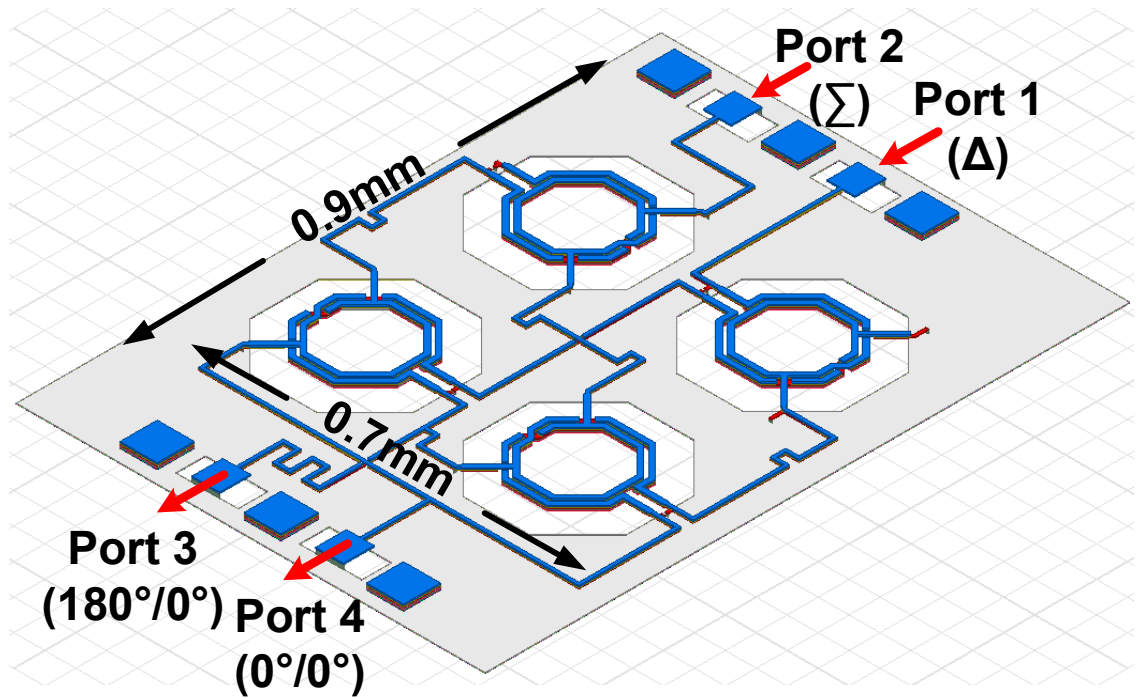
In summary, the above derivations show that cascading more rat-race stages achieves further magnitude/phase mismatch suppression and thus bandwidth extension, however, at the expense of the total insertion loss.



**Figure 2-5 (a) Single folded-inductor rat-race 3D EM model, (b) equivalent schematic, and measurement and 3D EM simulation results and measurements of (c) magnitude mismatch and (d) phase error.**

### 2.3 Folded Inductor Based Rat-Race Coupler

Conventionally, rat-race couplers are synthesized using  $\lambda/4$  and  $3\lambda/4$  t-lines, which makes conventional rat-races an area-expensive choice for on-chip implementations. To shrink the coupler size, lumped elements are employed to replace the t-line sections with either  $\Pi$  or T lumped equivalent circuits [33, 34]. In our previous research, the rat-race coupler size was decreased even further by combining the three inductors needed into one folded inductor geometry, thus creating a rat-race coupler with only one inductor footprint.

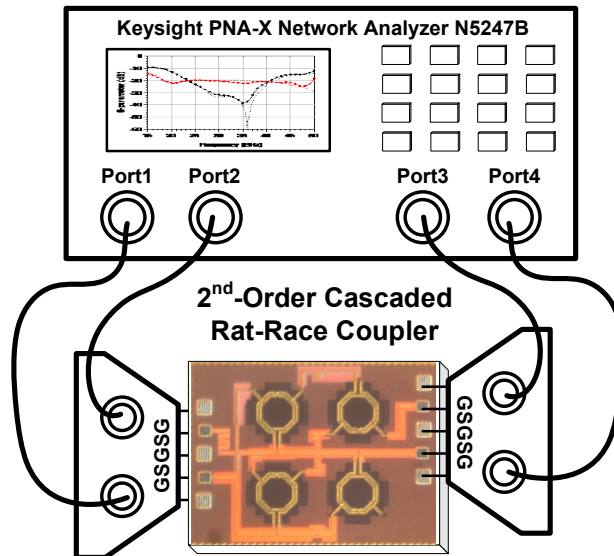


**Figure 2-6 3-D EM model of proposed 2nd order cascaded rat-race hybrid coupler implemented in the GlobalFoundries 45nm SOI CMOS process.**

This folded inductor-based coupler achieves a more than  $3\times$  size reduction compared to conventional lumped element design [33]. Figure 2-5(a) shows the 3D EM model of the rat-race coupler utilized in this paper where port 1 and port 2 are the difference and sum ports, respectively. Figure 2-5(b) shows the equivalent schematic for the folded inductor-based rat-race coupler, which differs from the classical six element lumped model (three inductors and three capacitors) due to the magnetic coupling among adjacent traces in the folded structure. Thus, this rat-race design in Figure 2-5 is used as the building block ( $n = 0$  in Figure 2-2) for our high-order self-similar  $180^\circ$  cascaded rat-race architecture. The complete circuit analysis of the rat-race shown in Figure 2-5 can be found in [30] and is not presented here for brevity. Note its low-loss nature ensures moderate insertion loss degradation when using it as unit cells in high-order cascade structures.

## 2.4 Simulation And Measurement Results

A proof-of-concept 22.6-43.4 GHz 2<sup>nd</sup>-order cascaded rat-race coupler is implemented in the GlobalFoundries 45nm CMOS SOI process. The 3-D EM HFSS model of the 2<sup>nd</sup>-order cascaded rat-race coupler used for all simulations is shown in Figure 2-6. For the folded inductor and trace routing we use the top aluminum layer (4.125 $\mu$ m) and top copper layer (3 $\mu$ m). For the ground plane we use a metal stack of multiple thin copper layers, i.e., one layer of 175nm copper and three layers of 140nm copper. In addition, we employ meander transmission lines to compensate for the phase difference that arises as a result of layout asymmetries.



**Figure 2-7 Equipment setup used to characterize the single stage and cascaded rat-race.**

In our cascaded rat-race design, the input ports are defined as ports 1 and 2 and the output ports are defined as ports 3 and 4 (Figure 2-6). Since our rat-race design is a symmetric structures ports 3 and 4 can also be used as the input. All the EM simulations

are performed using HFSS (Ansys) and all measurement were done using a 4-port vector network analyzer from Keysight (10MHz-67GHz) and GSGSG probes (Cascade Microtech). Figure 2-7 shows the measurement setup for the single stage and cascaded rat-race couplers.

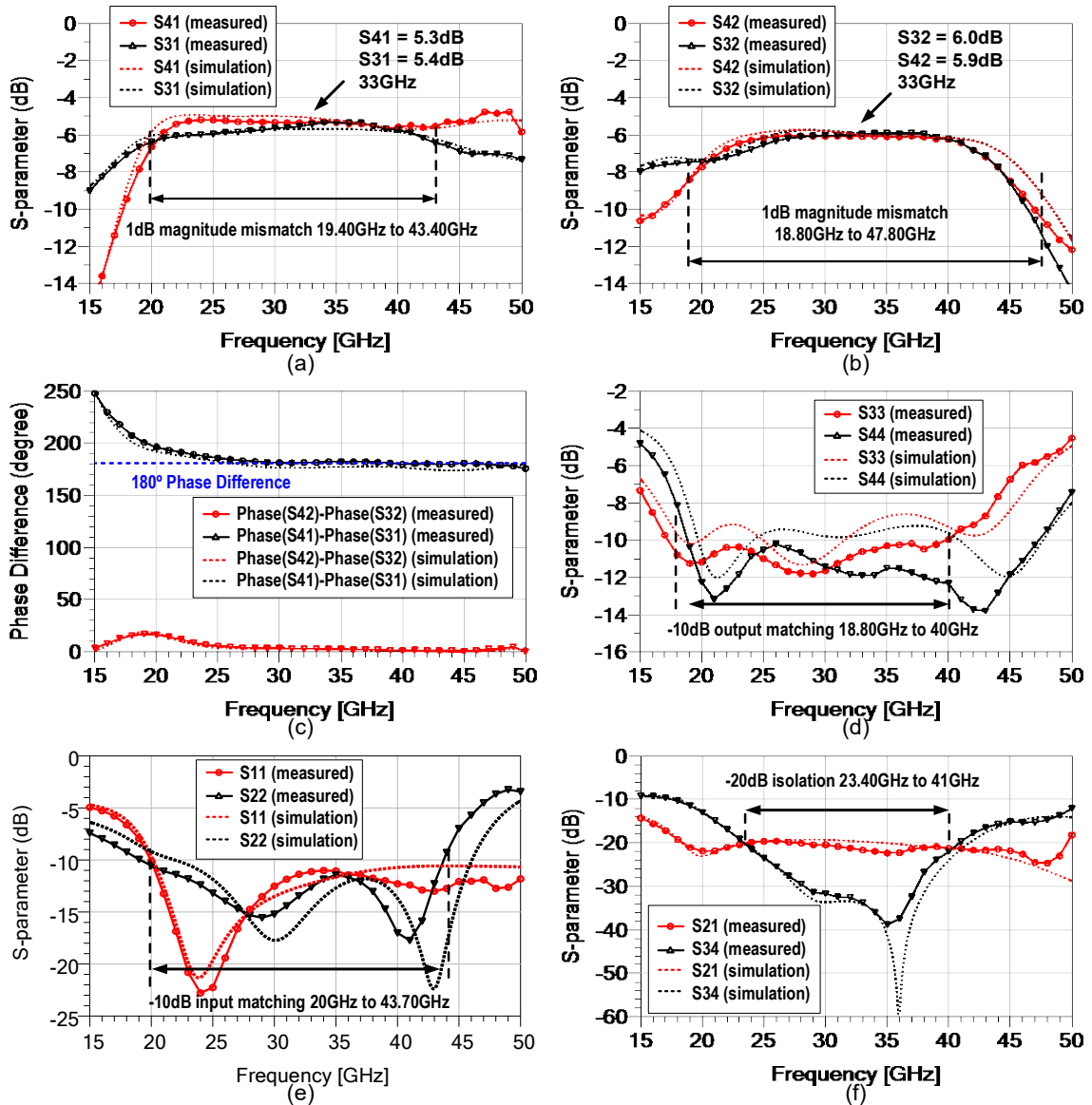


Figure 2-8 Measurement and 3D EM simulation results of the 2nd order cascade rat-race coupler: (a) magnitude response of Port1, (b) magnitude response of Port2, (c)

phase response of Ports 1 and 2, (d) output matching, (e) input matching, and (f) input and output isolation.

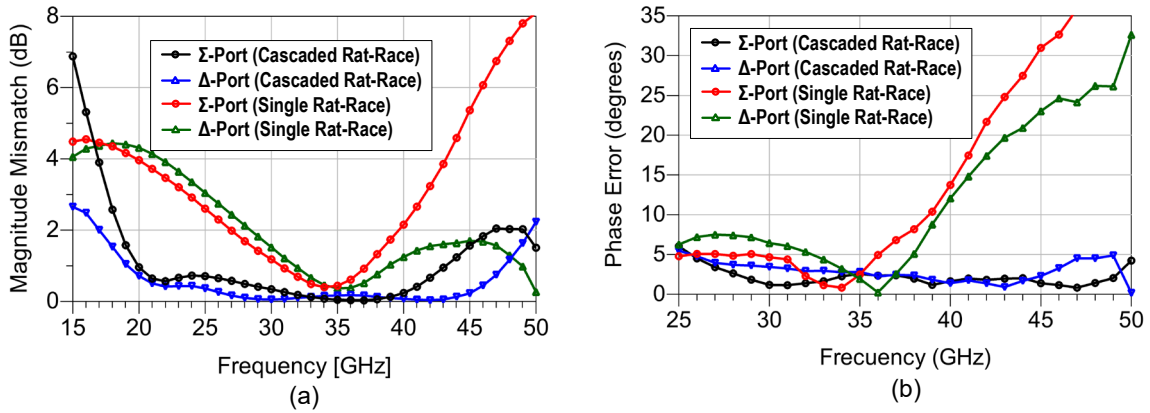


Figure 2-9 Measurement results of the (a) magnitude mismatch and (b) phase error comparison between single unit and cascaded rat-race coupler.

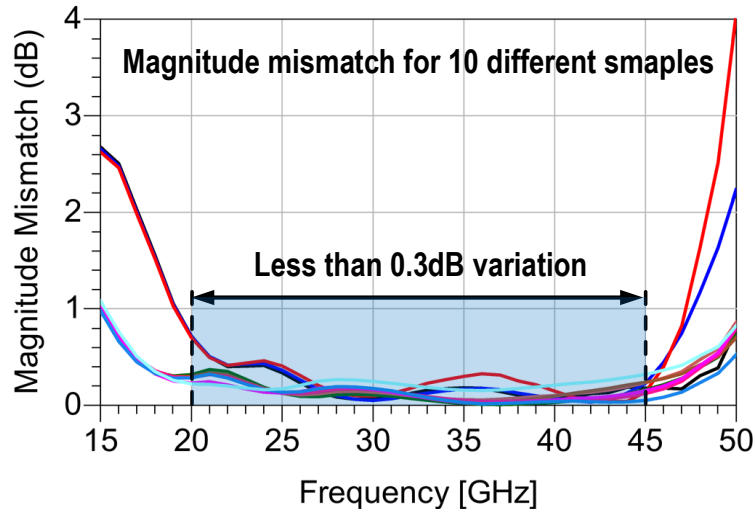
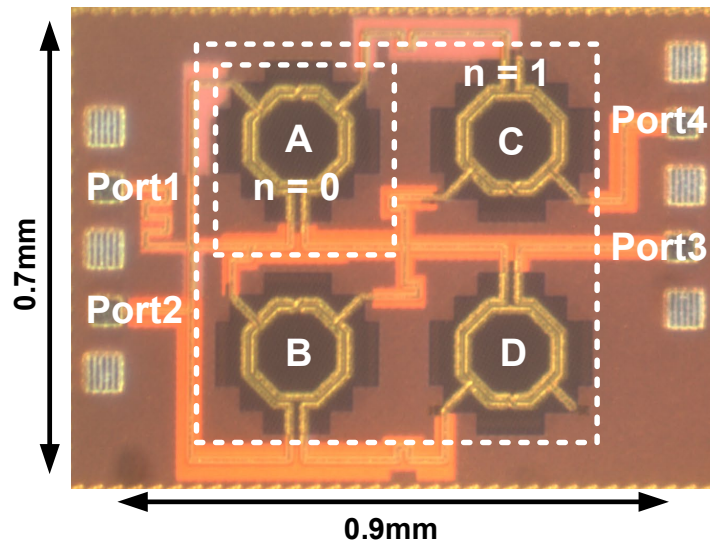


Figure 2-10 Measured magnitude response of 10 different samples of the 2nd order cascaded rat-race.

The 4-port measurement results and 3-D EM simulation results are shown in Figure 2-8. The magnitude and phase responses of port 1 show a less than 1dB magnitude mismatch from 19.40 to 43.40GHz and a phase mismatch of less than  $5^\circ$  from 26 to 45.80GHz (Figure 2-8(a) and Figure 2-8(c)). For port 2, the magnitude mismatch is less

than 1dB from 18.80 to 47.80GHz, and the phase mismatch is less than  $5^\circ$  from 25 to 47.40GHz (Figure 2-8(b) and Figure 2-8(c)). Matching for all four ports is better than -10dB throughout the frequency range of interest (Figure 2-8(d) and Figure 2-8(e)). In addition, the insertion loss between the input and output ports is between 2.2dB to 3.2dB across the 1dB bandwidth, making this design very symmetric. Figure 2-8(f) shows that the isolation between input ports ( $S_{21}$ ) and the isolation between output ports ( $S_{34}$ ) is better than -20dB from 23.40 to 41GHz.



**Figure 2-11 Chip micrograph of the proof-of-concept 2nd order cascaded rat-race coupler.**

Moreover, we measure the S-parameters across frequency of a single rat-race and compare the results with those of our cascaded rat-race, as shown in Figure 2-9. For the  $\Delta$ -Port and  $\Sigma$ -Port magnitudes, there is a 3dB reduction in the magnitude error at 20 and 45GHz (Figure 2-9(a)), demonstrating the substantial bandwidth extension of our proposed cascaded rat-race architecture. Figure 2-9(b) shows the phase imbalance cancelling properties of the cascaded rat-race, where a less than  $5^\circ$  error is observed from 25 to

50GHz, which means that the cascaded rat-race cancels the phase error by more than 40° at the higher operation frequencies.

In addition, 10 independent samples are measured to demonstrate the robustness of our 2<sup>nd</sup>-order cascaded rat-race. Figure 2-10 shows the magnitude mismatch of the 10 samples measured where the magnitude mismatch variation among the 10 samples is less than 0.3dB across the bandwidth, which can be attributed in large part to the measurement error induced by the difference in the probe landing.

These measurement results demonstrate that our 2<sup>nd</sup>-order cascaded rat-race design is a desirable candidate for implementing broadband beam-formers, full Ka-band multi-functional radars, and multi-band 5G communication systems operating at 24, 28, 37, and 41GHz. The core area of the 2nd-order Ka-band cascaded rat-race coupler occupies only 0.65mm by 0.65mm (excluding pads) in the GlobalFoundries 45nm SOI CMOS process. The chip microphotograph is shown in Figure 2-11. Table 2-1 summarizes the performance comparison with recently published mm-wave rat-race couplers full integrated in silicon processes.

**Table 2-1 Comparison of Mm-Wave Rat-Race Couplers**

	This Work	[18]	[20]	[21]	[27]	[23]	[33]
Technology	45nm SOI	BiCMOS	CMOS	GaAs	CMOS	BiCMOS	CMOS
Operating Frequency (GHz)	22-44	57 - 71	110-170	37-43	62-78	63-77	28-32
Amplitude Imbalance (dB)	1	1.2	0.5	1	1	1.4	0.5dB
Phase Imbalance	5	20°	15°	10	10	6	20
Max. Insertion Loss (dB)	2.5	3.2	1.5	5.2	1.1	2.6	2.6
Dimensions (mm <sup>2</sup> )	0.42	0.28	0.05	0.2	0.037	0.11	0.28

## 2.5 Conclusion

A new cascaded high-order rat-race coupler network architecture is proposed that achieves bandwidth extension by reducing the amplitude mismatch and cancelling of the phase imbalance. As a proof-of-concept design, a 22.6-43.4 GHz 2nd-order cascaded rat-race coupler fully integrated in the GlobalFoundries 45nm CMOS SOI process is presented. The cascaded rat-race design cancels the amplitude mismatch and phase error of a single rat-race coupler through each signal path and greatly extends the operation bandwidth. Based on our measurement results, our cascaded rat-race design achieves a less than 1dB magnitude mismatch, a less than  $5^\circ$  phase mismatch, while providing excellent input/output matching and better than -20dB isolation, throughout the entire Ka-band.

# **CHAPTER 3. A 40-60GHZ 5-BIT VECTOR MODULATOR PHASE SHIFTER INTEGRATED WITH A POWER AMPLIFIER FOR PHASED ARRAY SYSTEMS IN 45NM CMOS SOI**

This chapter presents a broadband vector modulator phase shifter integrated with a PA covering  $360^\circ$  of phase interpolation while providing a truly 0 magnitude and 40dB of dynamic range covering a frequency range from 40GHz to 60GHz for phased array systems. The transmitter path consists of an input and output Marchand balun, pre-amplifier, vector modulator core, and a 2-stage power amplifier. These three stages provide the desired phase interpolation while delivering adequate power to drive an on-chip antenna element. As a proof-of-concept design, we implemented a 3-stage phase-rotator-power-amplifier system in a 45nm CMOS SOI process with a total chip area of 2.9mm by 0.98mm. Our measurement results demonstrate that our prototype provides a maximum saturated output power of 12.5dBm at 50GHz and a small signal gain greater than 18dB throughout the entire bandwidth while providing  $360^\circ$ -degree full span phase interpolation. The Marchand baluns provide an input and output matching better than -10dB from 35GHz to 60GHz.

## **3.1 Introduction**

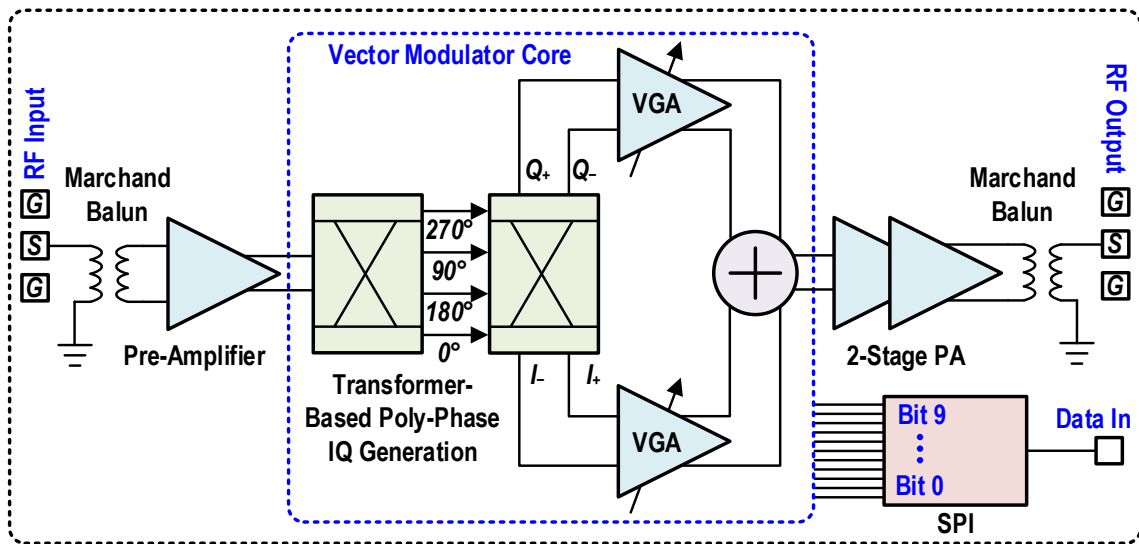
In recent years, the scaling of silicon devices and availability of the 5G mm-Wave spectrum have generated much interest from designers to implement entire phased array systems in one single silicon chip [35-37]. Phased arrays systems pose distinctive advantages over single-element transceivers, such as element dependent equivalent-

isotropic-radiated-power (EIRP), higher signal-to-noise (SNR), and beamforming used in spatial filtering. In addition, mm-Wave integrated phased-arrays systems offer superior performance over discrete implementation due to lower losses caused by longer signal routing and lossy interconnects. Moreover, transceivers based on phased arrays are finding their way into automotive radar applications, 5G consumer applications, and hyperspectral imaging, amongst other [38-40].

5G mm-Wave wireless system employing time division duplexing (TDD) might benefit from the reconfigurability that is provided by front-end-module architectures using a separate transmitter (TX) and receiver (RX) due to the data asymmetry in the upload/download channel. One of the most important components in phased-array systems is the phase rotator. This is particularly due because the beam steering and beam forming quality of the phased array depends heavily on the phase error and magnitude variation of the phase interpolation. A common approach to phase interpolation is by implementing a passive phase rotator such as the reflective type phase shifter (RTPS), which consists of a 90° quadrature hybrid and two matched tunable reflective loads [41]. The load tunability provides the ability to obtain the desired phase shifting. Nonetheless, there are two main drawbacks for reflective phase shifters. First, RTPS exhibit a direct trade-off between the phase shifting range and insertion loss (IL). Additionally, reflective phase shifters might need large silicon area since they require a  $\lambda/4$  coupler. There exist other types of passive phase shifters, such as switched filter and delay line-based phase shifters, which also suffer from similar drawbacks as RTPS such as significant passive losses.

Active phase rotators are widely employed to mitigate some of the drawbacks mentioned previously. Cartesian vector modulator-based phase rotator is a common

topology used as an active approach [42]. This type of phase rotator has the advantage of providing a dense phase interpolation range over the entire cartesian plane while delivering some degree of signal amplification. A typical active phase rotator consists of an in-phase/quadrature (I/Q) generation network, two variable gain amplifiers (VGA), and an output summing circuit. In this topology, the input RF signal is split into its I and Q components with equal amplitudes, which are then amplified independently by the appropriate gain, and finally the amplified signals are summed together to obtain the desired phase interpolation.



**Figure 3-1 Block diagram of the transmitter front end module.**

Vector modulator-based phase rotators often employ complex passive I/Q generation networks which introduce a substantial insertion loss. Additionally, for broadband designs the digital VGAs cannot provide enough gain to overcome the insertion losses introduced by the passive networks, therefore the signal amplification and output power is very limited. To overcome these challenges, we propose a transmitter (TX) composed of a low-power pre-amplifier stage, a broadband vector modulator-based phase-rotator, and a 2-

stage power-amplifier covering a frequency range from 40GHz to 60GHz while providing 360°-degree full span phase interpolation, a maximum saturated output power of 12.5dBm, and a small signal gain greater than 18dB throughout the entire bandwidth.

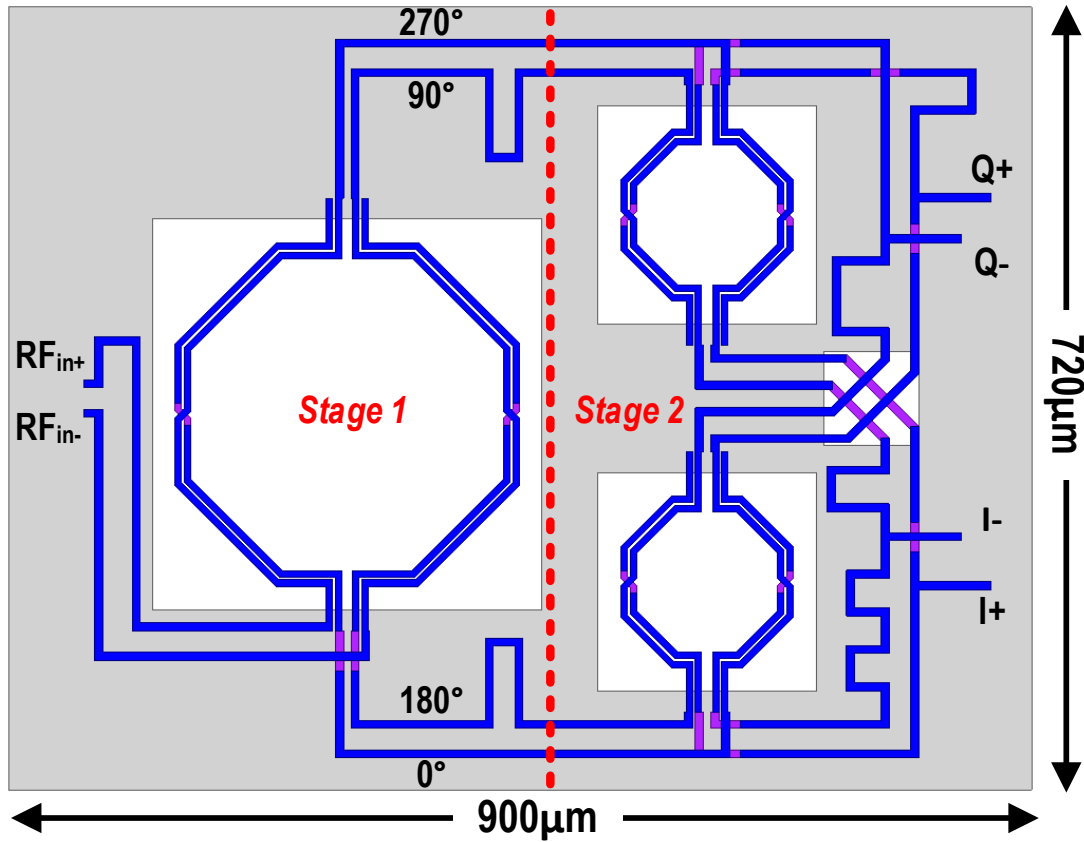
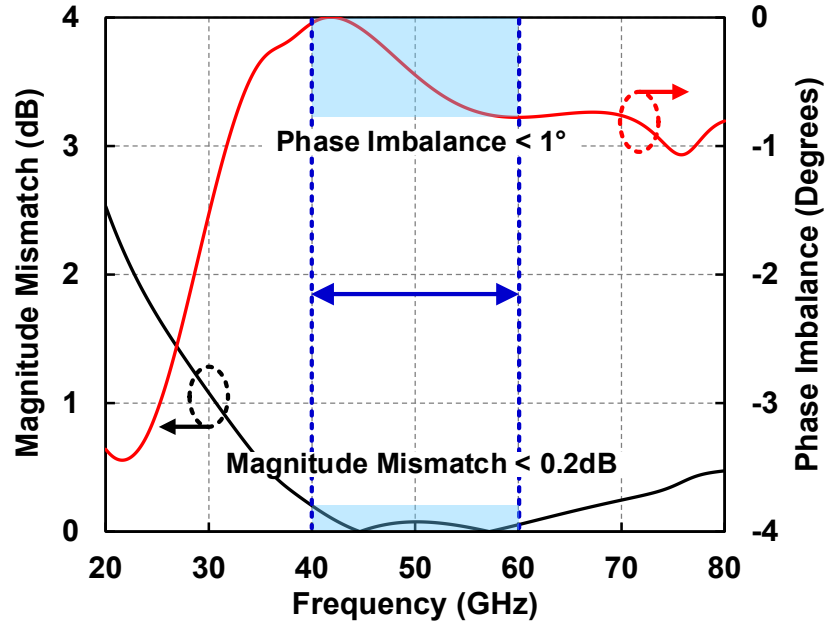


Figure 3-2 3D HFSS model of transformer-based quadrature generation network.

### 3.2 Proposed System Architecture

The top-level system architecture of the proposed TX is shown in Fig. 1. Marchand baluns are used at the input and output ports for broadband single-ended to differential conversion. The first stage is a low-power broadband pre-amplifier that consists of a differential common-source driver-stage. Neutralization capacitors are used in all gain stages to enhance stability and gain. In addition, transformer-based matching networks are

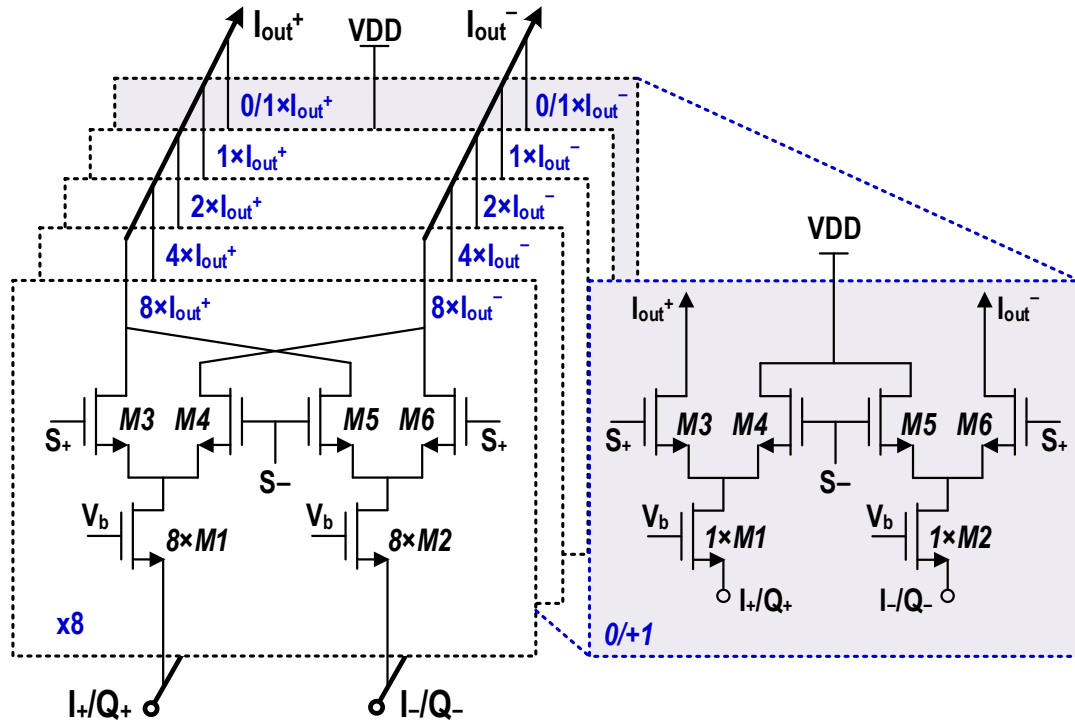
used for at the input and output of the pre-amplifier stage to provide adequate loading at the output of the pre-amplifier and for input matching. The driver-stage common-source (CS) of the 2-stage PA was reused in the pre-amplifier core.



**Figure 3-3 Magnitude mismatch and phase imbalance of IQ generation network.**

The second stage is the vector modulator core, which is composed of the I/Q generation network, VGAs, and output summing network. The I/Q generation is a 2-stage transformer-based poly-phase network design [31]. In summary, a differential transformer-based quadrature hybrid is used as the first stage to generate the differentials I/Q signals. The second stage of the poly-phase network is composed of two identical quadrature hybrid couplers, which help to increase the bandwidth of operation and partially correct the I/Q generation inaccuracies. The first stage of the I/Q generation network is primarily responsible for the overall magnitude mismatch and phase imbalance. Therefore, the second stage hybrid couplers were designed smaller to reduce the silicon area while still

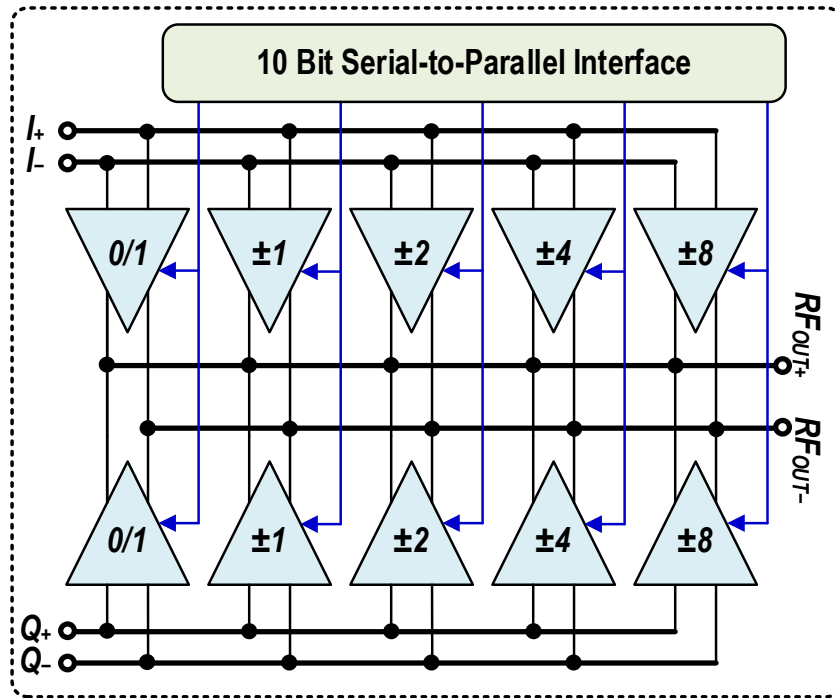
enhancing the performance. Fig. 2 shows the 3D HFSS model of the 2-stage differential transformer-based quadrature generation network. Fig. 3 shows the simulated magnitude mismatch and phase imbalance from 20 to 80GHz.



**Figure 3-4 Schematic of the binary weighted cells that make up the digital VGA.**

The differential I/Q signals coming out of the quadrature generation network are fed into two digital VGAs. The VGA is implemented using 4-bit binary weighted cells and a half-bit cell, where all the cells are connected in parallel, as shown in Fig. 4. The binary weighted cells are implemented using a differential common-gate (CG) amplifier and 4 current polarity selector switches. The CG topology is used to facilitate broadband matching between the quadrature generation network and the digital VGAs. Each VGA cells delivers a normalized output RF current amplitude of 0/+1 for the half-bit cell, and

$\pm 1, \pm 2, \pm 4, \pm 8$  for bits 1 through 4. Consequently, the polarity of each cell can be digitally controlled to produce a combined normalized output from -15 to +15. The output currents of each digital VGA are combined by an inter-stage matching transformer network. Fig. 5 shows our proposed vector modulator phase rotator core diagram.



**Figure 3-5 Schematic diagram of the proposed vector modulator phase rotator core.**

A 2-stage power amplifier is used as the final stage to provide enough gain and output power capable of driving an antenna element or the next stage in transceiver chain. The schematic of the 2-stage PA is shown in Fig. 6. Our 2-stage PA consists of a capacitively neutralized common-source driver and PA core. The input/output networks are based on transformers to provide output loading and inter-stage matching.

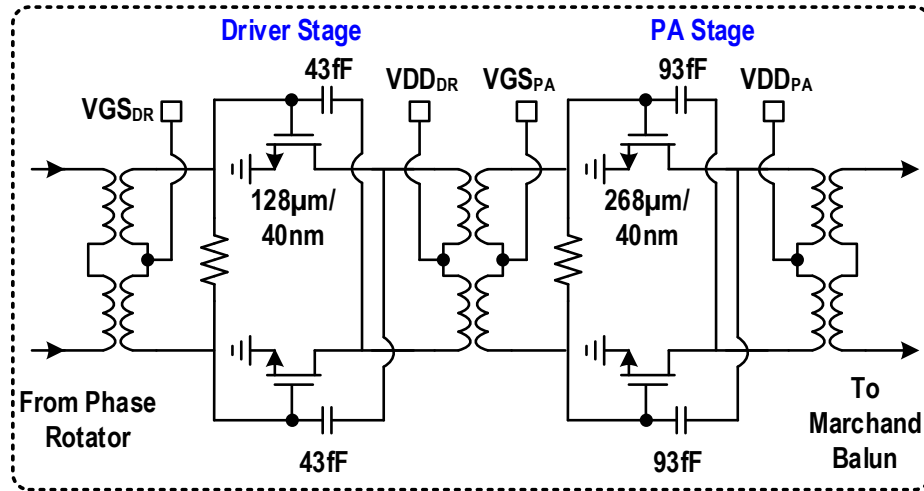


Figure 3-6 Schematic diagram of the proposed 2-stage power-amplifier.

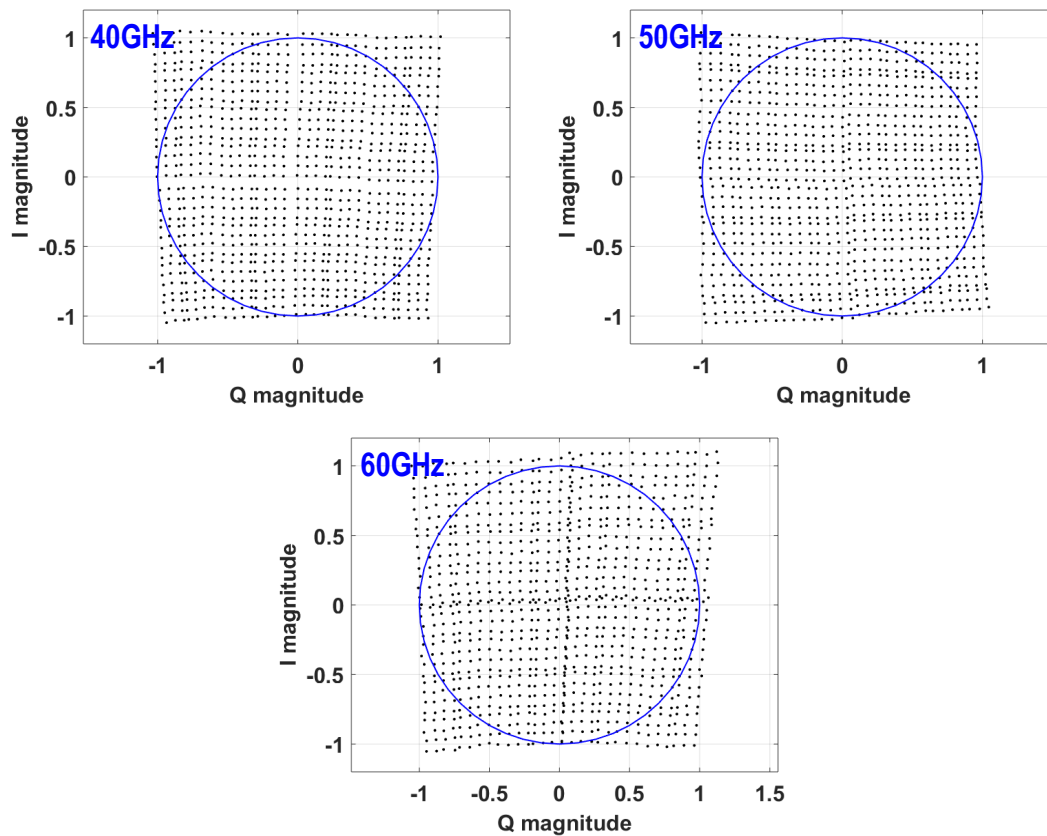
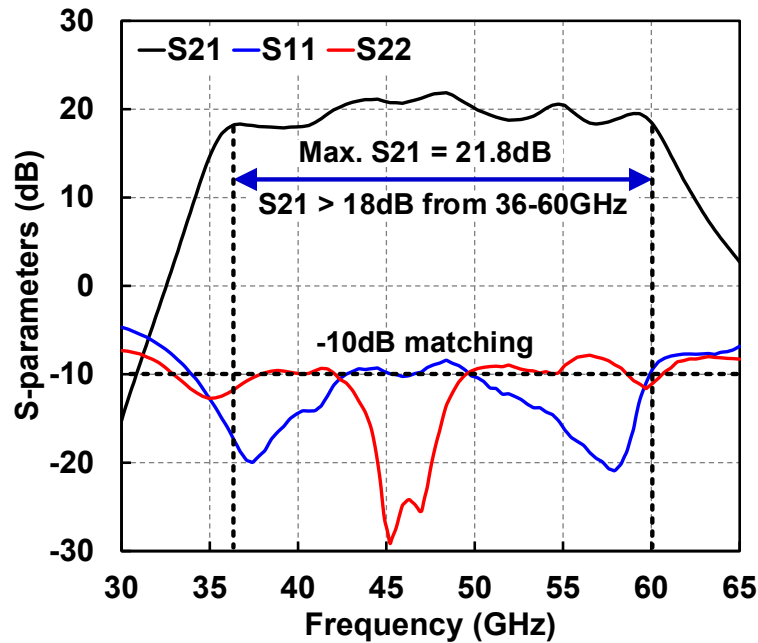


Figure 3-7 Constellation measurement of full 961 phase interpolation points in normalized I/Q coordinate at 40, 50, and 60GHz.

### 3.3 Measurement Result

As a proof of concept, the integrated phase rotator-power amplifier was implemented in the GlobalFoundries 45nm CMOS SOI process. Small-signal measurements were performed using GSG input and output probes and a vector network analyzer (Keysight PNA-X). Off-chip DACs were used to generate the 10-Bit VGA control codes.



**Figure 3-8 2-port S-parameter measurements.**

The phase rotator core consumes 33mA from a 1.8V source while the pre-amplifier and 2-stage PA consume a total of 110mA from a 1.1V source. Fig. 7 shows the measured normalized small-signal constellations at 40, 50, and 60GHz each one containing a total of 961 cartesian interpolation points, which demonstrates a minimal magnitude mismatch and phase imbalance over the frequency of operation. The small-signal gain (S21) is greater than 18dB from 40GHz to 60GHz and the matching for input and output ports is better than -10dB from 35GHz to 60GHz as shown in Fig. 8.

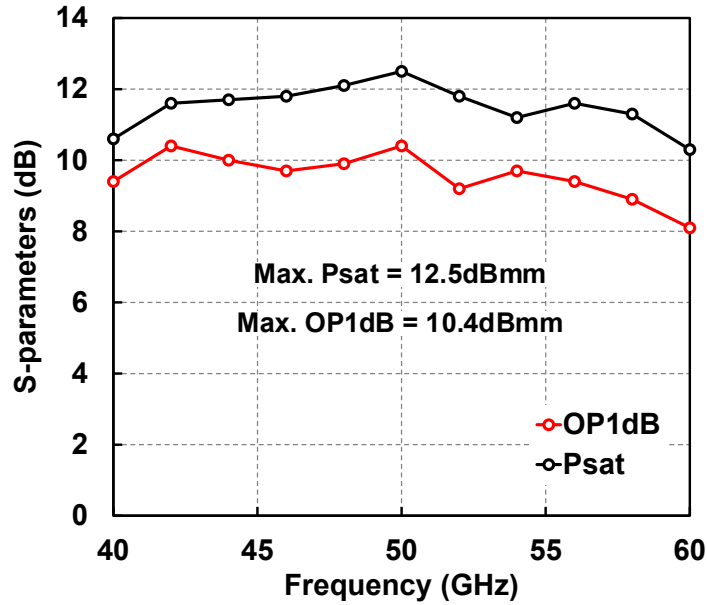


Figure 3-9 Large signal CW measurements.

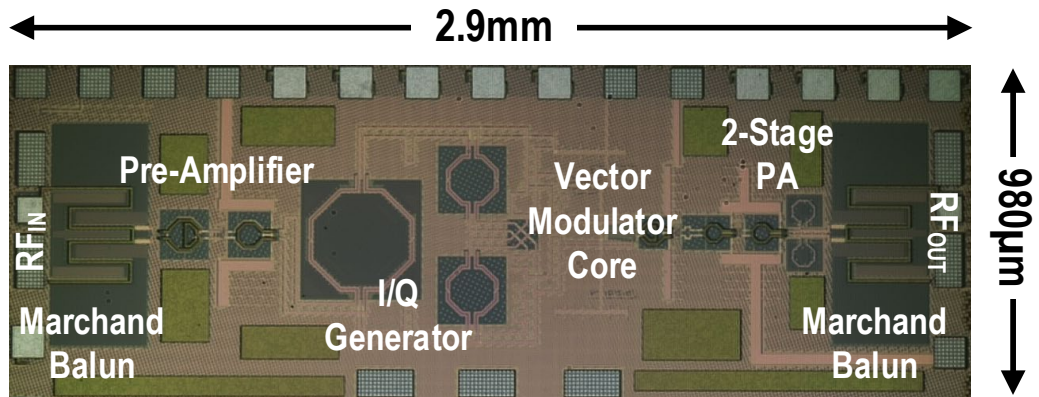


Figure 3-10 Chip micrograph.

Large-signal CW measurements were performed using a power meter and sensor (Keysight Power Meter N1914A, Power Sensor N8488A). Large-signal measurements results are shown in Fig. 9. The integrated PR-PA achieves a maximum saturated power (Psat) of 12.5dBm at 50GHz with a minimum of 10.3dBm at 60GHz. The maximum measured OP1dB is 10.4dBm at 50GHz demonstrating excellent output power capabilities.

Fig. 10 shows the chip micrograph of our prototype implemented in the GlobalFoundries 45nm CMOS SOI process. Table 1 shows the comparison with state-of-the-art phase shifters and integrated transmitters at mm-Wave frequencies.

**Table 3-1 Comparison of State-of-Art.**

	<b>This Work</b>	<b>[5]</b>	<b>[9]</b>	<b>[2]</b>	<b>[8]</b>	<b>[7]</b>
<b>Technology</b>	<b>45nm SOI</b>	65nm CMOS	65nm CMOS	45nm SOI	130nm CMOS	45nm SOI
<b>Frequency (GHz)</b>	<b>40-60</b>	2-20	62	57.5-65.5	24.5-29.4	60
<b>Integration Level</b>	<b>wPA</b>	Phase Rotator	LNA/PA	PA	Phase Rotator	Mixer/PA
<b>Power Consumption (mW)</b>	<b>180</b>	9.2	168	67 <sup>3</sup>	27	220
<b>Gain per Element (dB)</b>	<b>21.8</b>	1 <sup>1</sup>	7.7	22	7.6	20-35
<b>3-dB Bandwidth (GHz)</b>	<b>19.2</b>	19	9 <sup>2</sup>	8	5.7	8 <sup>4</sup>
<b>OP1dB per Element</b>	<b>10.4</b>	-	5 <sup>2</sup>	10	-	10.9
<b>Size (mm<sup>2</sup>)</b>	<b>2.8</b>	2.16	1.69	0.45	0.85	3.92

### 3.4 Conclusion

A new integrated vector modulator-based phase-rotator-power-amplifier architecture topology for phased array systems is proposed that achieves 360° full-span phase interpolation while providing high output power capabilities covering a frequency range from 40 to 60GHz. As a proof-of-concept, our PR-PA was implemented in the GlobalFoundries 45nm CMOS SOI and achieves a maximum Psat of 12.5dBm, a maximum gain of 22.7dB, and negligible magnitude mismatch and phase imbalance while occupying a silicon area of 2.9mm by 0.98mm. Our prototype also demonstrates excellent input/output matching.

**CHAPTER 4. A 150 GHZ LENS-FREE LARGE FOV  
REGENERATIVE 2×2 TRANSCEIVER ARRAY WITH 31% DC-  
TO-EIRP EFFICIENCY AND -70 DBM SENSITIVITY FOR A 70  
CM BIDIRECTIONAL PEER-TO-PEER LINK**

This chapter presents a 150GHz regenerative low power miniature 2-way radio integrated with on-chip antennas. The low power radio is based on a reconfigurable fundamental oscillator array that can be used as a sub-THz source in the transmitter (TX) mode and as a sub-THz super-regenerative detector in the receiver (RX) mode supporting on-off keying (OOK) modulation. The oscillators are coupled through a low-loss integrated Marchand balun-based coupling network that guarantees far-field constructive interference at the receiver side. A 2×2 on-chip patch antenna array is designed with a new adaptive metal-fill placement methodology that largely reduces antenna losses and off-tuning present in sub-THz/THz frequency antenna designs without the need for bulky silicon lenses. Our proof-of-concept prototype achieves a maximum EIRP of 8.52dBm, at a frequency of 149GHz, an RX sensitivity of -70dBm, and a DC-to-EIRP efficiency of 30.7% with no silicon lens, which is the highest efficiency reported of all the silicon-based sub-THz transceivers (TRX) in the 150GHz range.

The moderate 2×2 array size with no silicon lens offers a large Field-of-View (FoV) of  $\pm 40^\circ$ , which eases node finding and link establishment in deployment. Our miniature low-power radio prototype consumes 11.6 mW in the TX mode and 10 mW in the RX mode after duty-cycling. Wireless peer-to-peer network measurements with OOK modulation using a 10Mb/s data rate demonstrate a chip-to-chip communication distance of 70cm and a BER  $\leq 10^{-5}$  at/above -55dBm received power and a BER of  $6 \times 10^{-3}$  at -70dBm received power. The prototype chip was designed using the GlobalFoundries

45nm silicon on insulator (SOI) process and it occupies a total chip area of 2.1mm by 2.1mm, including the antenna array, making it particularly apt for ultra-miniaturized, high-security, and stealth IoT nodes for intelligent edge networks and wearable devices.

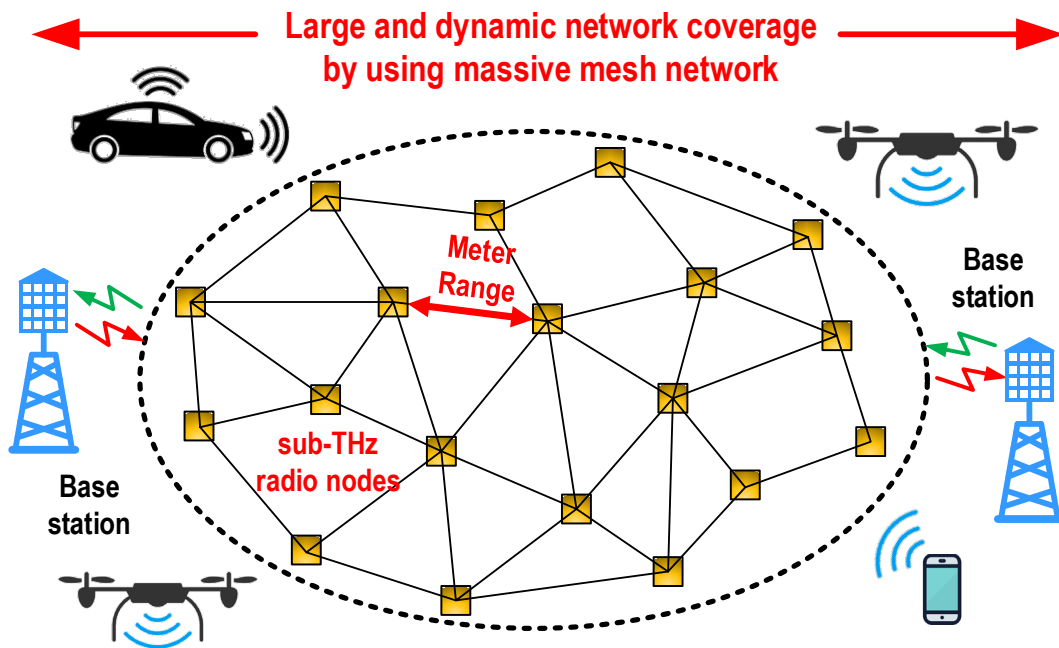
#### **4.1 Introduction**

The past few decades have witnessed a surge of smart wireless sensor networks and IoT devices targeting the health care industry, manufacturing, consumer products, and defense applications, among others [43-49]. Recently, there has been an increasing interest in silicon-based mm-Wave/THz IoT systems to explore their ultra-compact form factor and on-chip antenna integration, which will potentially lead to high-security and even “invisible” stealth sensor nodes or RFID tags [50, 51]. Conceptually, these invisible sensor nodes would gather information collaborative from their surroundings and establish neighbor-to-neighbor meter-scale mesh communication networks where they relay the information from one node to another to form long distance communication links, as shown in Figure 4-1. These edge sensor nodes could decide what is the important information that needs to be sent to the cloud, easing the computing/storage requirements.

The feasibility of functional field deployable large-scale sensor networks is dependent upon these systems being highly miniaturized, consuming low power, transmitting signals efficiently at reasonable data rates, and that are easy to manufacture in a self-contained form factor. The MHz and low GHz frequency radios achieve impressive energy efficiency [52-56]; however, their low-frequency antennas are at the centimeter range. Electrically small antennas can be used to largely reduce the overall form factor at the expense of antenna bandwidth and gain, which drastically reduces link distance and efficiency.

Frequencies at the mm-Wave are another potential candidate to create wireless systems with an intrinsic reduction in antenna size. As an example, a pad-less millimeter-

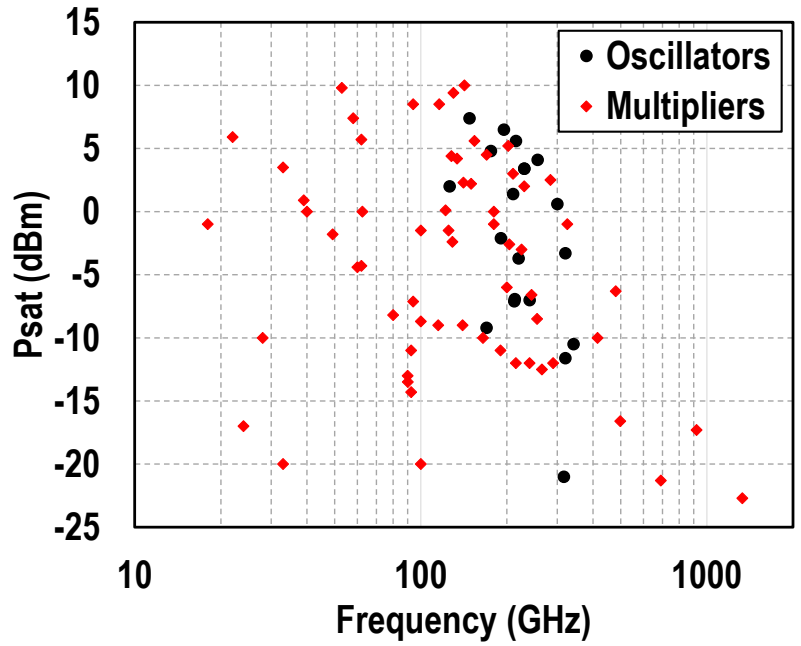
sized radio with power harvesting capabilities has been demonstrated in [57] as a possible candidate for a miniature radio for IoT applications and wireless tags. This system is a self-sufficient mm-wave miniature radio with no external equipment, two antennas operating at different frequency bands, an energy harvesting unit, and it provides a measured maximum communication distance of 50cm using an external PA and horn antenna generating an EIRP of 45dBm. Although this system leverages the mm-Wave frequency range for antenna size reduction while providing a high level of integration, there is still a need to further increase the wireless link functionality and to further decrease the size of on-chip low power radios to enable the next generation of IoT devices and deployable wireless sensor nodes [58-61].



**Figure 4-1 – Distributed peer-to-peer ultra-miniaturized mesh network based on deployable low-power 2-way sub-THz stealth radios.**

High mm-Wave/sub-THz frequencies are an excellent candidate for invisible radio nodes since antenna arrays can be easily implemented in a small form factor to increase the EIRP and communication distance [62-66]. Moreover, adequate power generation in this

part of the frequency spectrum is possible by employing fundamental/harmonic oscillators, and frequency multipliers [67-77], as shown in Figure 4-2. Nevertheless, previously reported mm-Wave/THz transceivers (TRX) often rely on large antenna arrays and off-chip silicon lenses [78-81] to boost their radiated power density, making them bulky and highly directional with very limited scan angles for viable IoT devices and sensor nodes. Note that on-chip antennas in bulk silicon typically suffer from low gain, low efficiency, and poorly defined antenna driving impedance due to the random metal fill and antenna substrate modes, necessitating the use of silicon lenses to collimate the beams.



**Figure 4-2 – Output power generation at mm-Wave and THz frequencies using fundamental and subharmonic oscillators and multipliers using CMOS and BiCMOS processes [25].**

Moreover, these systems often employ coherent receivers that require accurate frequency references and high-power consumption/complexity [82, 83]. Viable mm-Wave/sub-THz radio solutions for field deployable IoT sensor networks require aggressively miniaturized, low power, and self-contained wireless frontends with angle-

insensitive wide FoV. Most importantly, these mm-Wave/THz IoT radios should support symmetric peer-to-peer communication links to form dynamic mesh networks.

To overcome the beforementioned issues, we present a low-power lens-free angle-insensitive regenerative transceiver on a GlobalFoundries 45nm CMOS SOI process with high resistivity silicon substrate [4]. The low-power radio is based on fundamental cross-coupled Colpitts oscillators that can be reconfigured as a power oscillator-based sub-THz source in TX mode or as a sub-THz super-regenerative receiver (SSR) in RX mode [84-91], which support bidirectional OOK-based communication. Moreover, the sub-THz Colpitts oscillator core is implemented where the source terminal is used as the output port to drive the antenna. This allows the decoupling of the oscillator tank's resonant frequency from the antenna impedance, thus reducing frequency detuning due to changes in the antenna impedance related to near-field interference or fabrication variations. Additionally, we employ a unique approach to couple the two oscillators by using a Marchand balun structure, which also serves to perform differential to single-ended conversion and to provide the appropriate choke or DC path to oscillator's source terminal. Our multi-purpose Marchand balun structure allows for low-loss coupling, appropriate DC biasing, and differential to single-ended conversion.

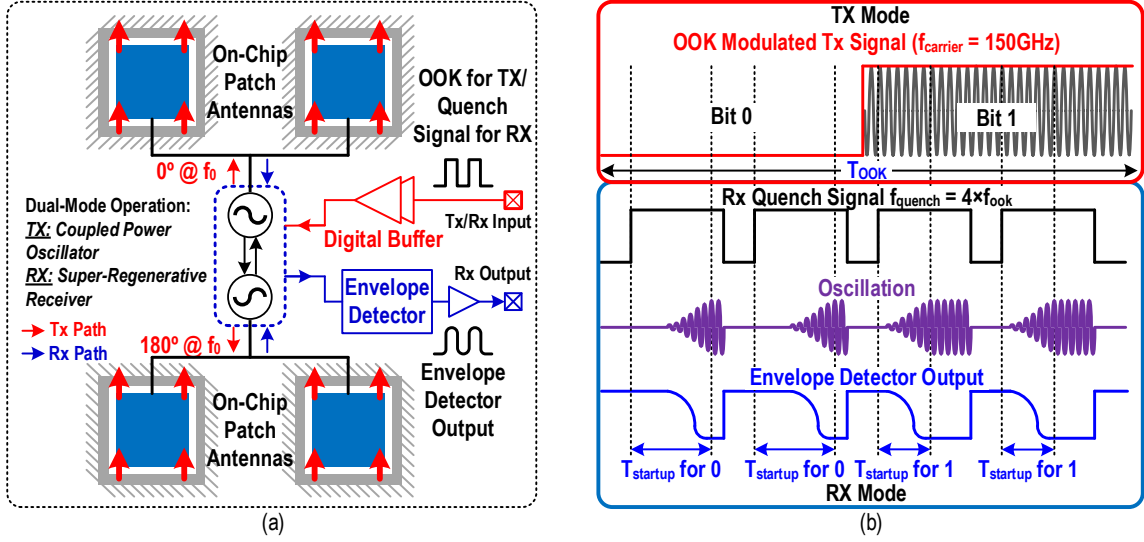
Lastly, A  $2 \times 2$  grounded coplanar patch antenna array was designed on a high-resistivity SOI substrate. The ground plane under the antenna suppresses the unwanted substrate mode and back-side radiation. To mitigate antenna losses and impedance/frequency variations, an adaptive metal fill is judiciously patterned with the metal density inversely proportional to the patch antenna near-field E-field strength. This minimizes hard to predict capacitive parasitic loading and losses due to eddy currents, which is extremely important when designing radiating elements at sub-THz and THz frequencies. Our custom metal fill avoids the need for the foundry's random metal fill placement. Our design methodologies allowed our sub-THz radio to demonstrate for the

first time a chip-to-chip wireless communications distance of 70cm while exhibiting a DC-to-EIRP efficiency of 31% without employing a silicon lens and consuming less than 10mW.

This chapter is organized as follows. Section 4.2 presents the overall proposed architecture of the sub-THz radio. Section 4.3 presents the measurement results and compares our work with the state of the art. Finally, Section 4.4 concludes this chapter.

## **4.2 Proposed Sub-THz System Overview**

The low-power 2-way sub-THz radio proposed here is based on two fundamental cross-coupled Colpitts oscillators operating at a frequency of 150GHz. The two oscillators are coupled through [92] a low-loss passive coupling structure that allows them to oscillate with a 180° phase difference to ensure that the antennas electromagnetic (EM) fields are constructively combined in the far-field. Each of the oscillator's output is connected to a 2×1 patch antenna array through a microstrip power combining/splitting structure. The patch antenna array is tuned to radiate to the oscillator's fundamental frequency of oscillation of 150GHz. The coupled oscillators can also be reconfigured as a transmitter or receiver supporting OOK modulation. In TX mode, the modulation scheme was implemented using a large tail current transistor operated in the triode region that is used to switch on and off the coupled oscillator pair. In RX mode, the injection transistor and the envelope detector are enabled while the transistor tail current is switch on and off. The start-up time of the oscillator is then measured to detect the presence of the sub-THz carrier signal. In the on-cycle the tail transistor is operated at a reduced bias to increase the sensitivity of the receiver and improve the DC power consumption. Figure 4-3 shows the system topology/timing diagram for transmitting/receiving OOK signals.



**Figure 4-3 – (a) Proposed system architecture of the 150GHz bidirectional low-power radio with on-chip patch antennas. (b) Basic operation of radio in TX and RX mode.**

#### 4.2.1 Antenna Array

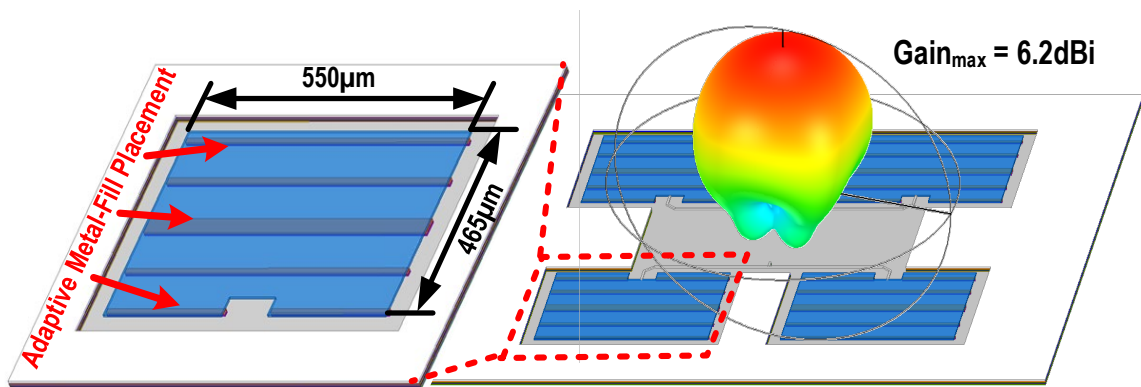
A  $2 \times 2$  on-chip coplanar patch antenna array was implemented using the top metal aluminum layer with a conductor thickness of  $4.125\mu\text{m}$  for the radiating structure and side ground, as shown in Figure 4-4. A bottom ground that enforces top-side radiation was realized using the last available thick copper layer with a conductor height of  $1.2\mu\text{m}$ . Initially, the antenna geometry was calculated using the following equations for the width and length of the patch [93]:

$$W = \frac{c}{2f_0 \sqrt{\frac{\epsilon_R + 1}{2}}} \quad (1-1)$$

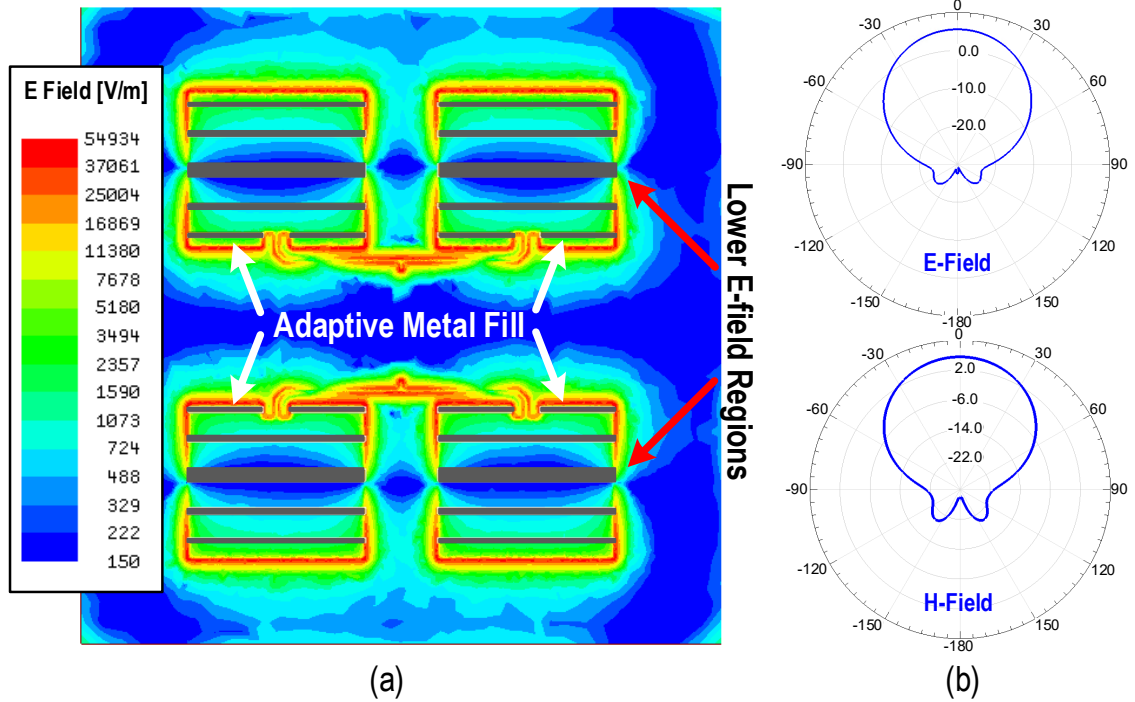
$$\epsilon_{eff} = \frac{\epsilon_R + 1}{2} + \frac{\epsilon_R - 1}{2} \left[ \frac{1}{\sqrt{1 + 12(h/W)}} \right] \quad (1-2)$$

$$L = \frac{c}{2f_0\sqrt{\epsilon_{eff}}} - 0.824h \left( \frac{(\epsilon_{eff} + 0.3)\left(\frac{W}{h} + 0.264\right)}{(\epsilon_{eff} - 0.258)\left(\frac{W}{h} + 0.8\right)} \right) \quad (1-3)$$

To mitigate antenna loss and impedance variations, a customized metal fill is judiciously patterned with the metal density inversely proportional to the patch antenna near-field E-field strength. Our custom metal fill avoids the need for the foundry's random metal fill placement, which minimizes hard to predict capacitive parasitic loading [94]. Since our custom metal fill introduces changes in the antenna resonance frequency, iterative 3D HFSS (Ansys) electromagnetic (EM) simulations are conducted to optimize the antenna size to obtain the highest gain and efficiency at 150GHz. Figure 4-5 shows the 3D HFSS EM simulations results of the E-field and radiation pattern of the final patch antenna array including the metal fill. The final width and length for the patch antennas are 550 $\mu$ m and 465  $\mu$ m, respectively. Antenna gain simulation results with different metal fill methods are shown in Figure 4-6(a).



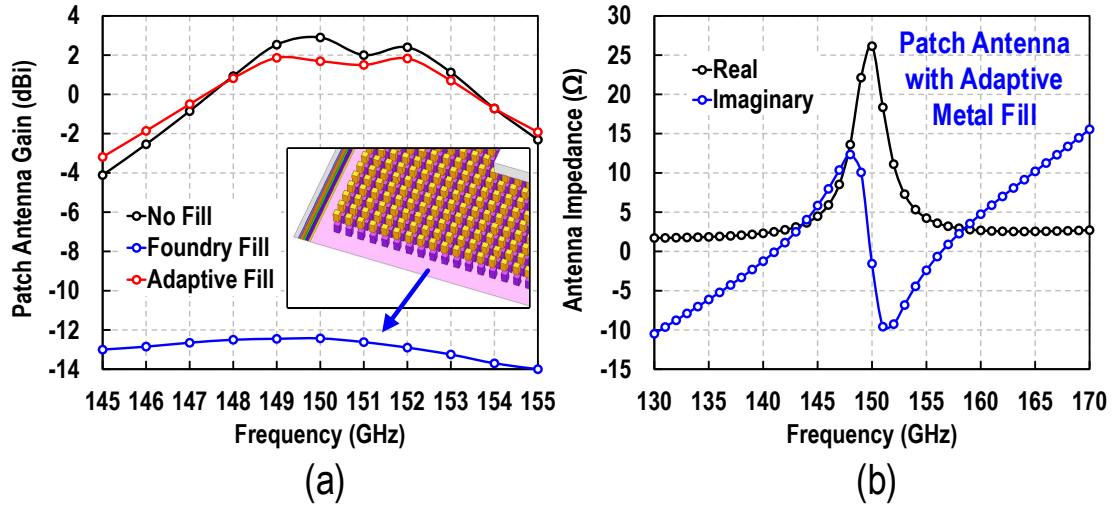
**Figure 4-4 Antenna array design with adaptive metal fill placement and 3D-EM HFSS simulation results.**



**Figure 4-5 – (a) 3D-EM HFSS simulation results of the E-field and (b) array radiation pattern with adaptive metal fill.**

Moreover, the oscillator and patch antenna array are codesigned such that the optimum load impedance needed at the oscillator output can be easily implemented by the antenna impedance without employing lossy matching networks, greatly reducing the passive losses and improving the DC-to-EIRP efficiency of the transmitter. In addition, the optimum load is constrained by a realizable characteristic impedance of a transmission line to reduce reflections and losses due to routing from the oscillator output to the patch antenna. This optimum load impedance presented at the oscillator output maximizes the power output and efficiency. The individual antenna impedance was modified by changing the width and length of the signal feed cutout. Moreover, the antenna pairs are arranged in an anti-parallel fashion. This supports a scalable array floorplan, lowers routing-based loss to the oscillator core, and provides a stronger coupling to each element. For this specific antenna configuration, it is necessary for the oscillators to drive the antenna pairs with a

180° phase difference. This allows for the electromagnetic radiation to be constructively combined in the far-field.



**Figure 4-6 – 3D-EM HFSS simulation results of (a) single patch antenna gain using different metal fill methods, and (b) patch antenna pair impedance.**

The maximum antenna array gain achieved is 6.2dBi with a radiation efficiency of 32% at the center frequency of 150GHz. The optimum real impedance obtained from the patch antenna pair was 26.1Ω, as shown in Figure 4-6(b). The optimum load is constrained by a realizable characteristic impedance of a transmission line to reduce reflections and losses due to routing from the oscillator output to the patch antenna.

#### 4.2.2 Transceiver Design

The transceiver is designed as a fundamental cross-coupled power Colpitts oscillator (PCO) that operates at a frequency of 150GHz and that can be reconfigured as TX or RX. In this architecture, the TRX employs two oscillators that are coupled differentially through a passive network that ensures a 180° phase difference at the oscillator outputs. The total transistor size was first optimized with the main goal of maximizing the DC-to-RF efficiency. Post-layout simulations of different layouts were

carried out where the number of fingers and multiplicity were varied to obtain the highest maximum oscillation frequency,  $f_{max}$ , of the transistor while maintaining reasonable inductance and capacitance values to form the resonant tank. The post-layout simulations did not include top metal layers since the parasitic of these layers were extracted using HFSS when simulating the entire oscillator core. The final total transistor width was chosen to be  $15\mu\text{m}$  with 15 fingers and a multiplicity of 2. Based on simulations this transistor achieves an  $f_{max}$  of 382GHz using a gate bias of 600mV.

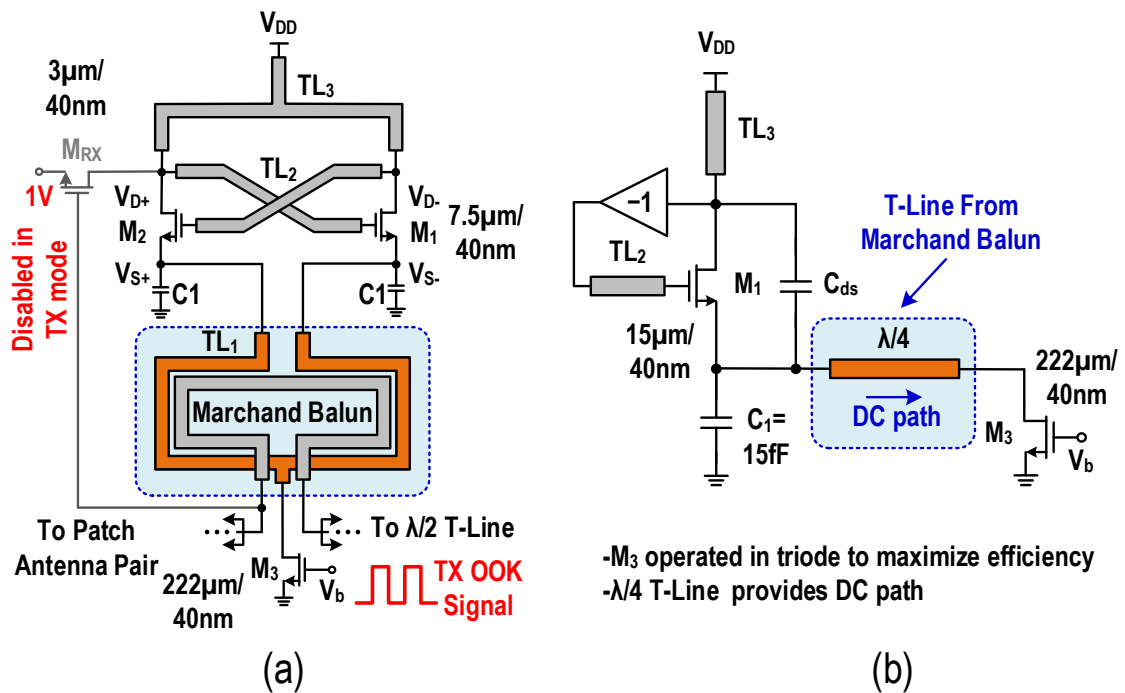
#### 4.2.3 Transmitter Mode

The design of the cross-coupled Colpitts oscillator core is shown in Figure 4-7(a). The oscillator consists of a NMOS transistor pair  $M_1$  and  $M_2$  that provides the necessary negative transconductance,  $-g_m$ , which is needed to overcome the passive losses of the resonant tank to sustain steady-state oscillation. The two capacitors that form the voltage divider and feed the signal back to the gate are  $C_1$  and the junction capacitance,  $C_{DS}$ , which together with the inductance provided by  $TL_3$  form the resonant tank structure. The initial values for the capacitor  $C_1$  and  $C_{DS}$  and inductor  $TL_3$  that form the resonant tank and that determine the fundamental frequency of oscillation are first calculated using the following Colpitts's oscillator equation:

$$EIRP = P_{IF} - G_{IF} - CL_{Mixer} - G_{Ant} + FSPL \quad (1-4)$$

The values for  $C_1$  and  $TL_3$  are chosen so that they are easily implemented with a high Q factor. In addition,  $C_{DS}$  is kept at a reasonable value so that the transistors  $M_1$  and  $M_2$  can achieve a large  $f_{max}$ . All inductances are derived from microstrip structures using the top metal layers for the signal and the bottom top metal layer for ground.  $TL_3$  also provides the appropriate DC path to  $V_{DD}$  and together with  $TL_2$  provides the gate biasing for the transistors. In addition,  $TL_2$  is used to adjust the gate to drain phase delay which is

used to obtain the maximum oscillation amplitude and efficiency [71]. Half circuit schematics of the oscillator implementation is shown in Figure 4-7(b). The DC ground path for the source is provided by  $TL_1$  which also acts as a large choke inductance at the fundamental frequency. This large choke inductor that connects both sources of  $M_1$  and  $M_2$  is tapped at the center where the large tail transistor ( $M_3$ ) operated in triode is connected and provides the path to ground.  $M_3$  also serves as the on/off switch to implement OOK modulation.



**Figure 4-7 – (a) Circuit schematic of cross-coupled Colpitts oscillator in (a) TX mode and (b) Colpitts oscillator half circuit schematic.**

In TX mode, the large tail transistor is operated in the triode region to ensure large voltage swings at the terminals of  $M_1$  and  $M_2$ . The gate of  $M_3$  is driven by a buffer which in turn is driven by a digital OOK signal. The output of the oscillators is taken differentially at the source of the transistors of  $M_1$  and  $M_2$  instead of their drain terminals. In doing so, any changes in the antenna impedance will not detune the resonant frequency of the oscillators since the source is insensitive to load variations due to its low impedance nature

( $1/g_m$ ). Moreover,  $TL_1$  together with  $C_1$  provide a low impedance path at  $2f_o$  for the sources of each transistor to ground, which offers additional second harmonic suppression at the antenna output. Due to the  $C_{DS}$  dependence on bias conditions, the oscillation frequency and output power levels can be tuned by adjusting  $V_{DD}$ . In TX mode the injection transistor  $M_{RX}$  is disabled by biasing its source to  $V_{DD}$ . When operating in TX mode the envelope detector and analog buffers are turned off to decrease the overall system DC power consumption.

Figure 4-8 shows the non-linear simulation results using the harmonic balance method to calculate the steady-state response of the oscillators in TX mode. Load-pull harmonic balance simulations were also employed to find the optimum load impedance that maximizes the DC-to-RF efficiency. The optimum real impedance from load-pull harmonic balance simulations was  $26\Omega$ . The optimum load is constrained by a realizable antenna impedance and characteristic impedance of a transmission line to reduce reflections and losses due to routing from the oscillator output to the patch antenna. These simulation results include extracted parasitics of the transistor and 3D EM HFSS models of all passive structures including patch antenna array, local interconnects, routing, and inductances. Our simulation results show a maximum DC-to-RF efficiency of 10.5% that translates to a DC-to-EIRP efficiency of 38.2%, including antenna gain and routing losses. In addition, the output power can be tuned from -3.19 to 7.49dBm by varying  $V_{DD}$  while maintaining a DC-to-RF efficiency above 8.5%. The frequency of oscillation can also be tuned from 148.8 to 150.2GHz. The DC minimum DC power consumption of the transmitter is 5.2mW, which demonstrates the viability of our sub-THz radio as a low power bidirectional sensor node.

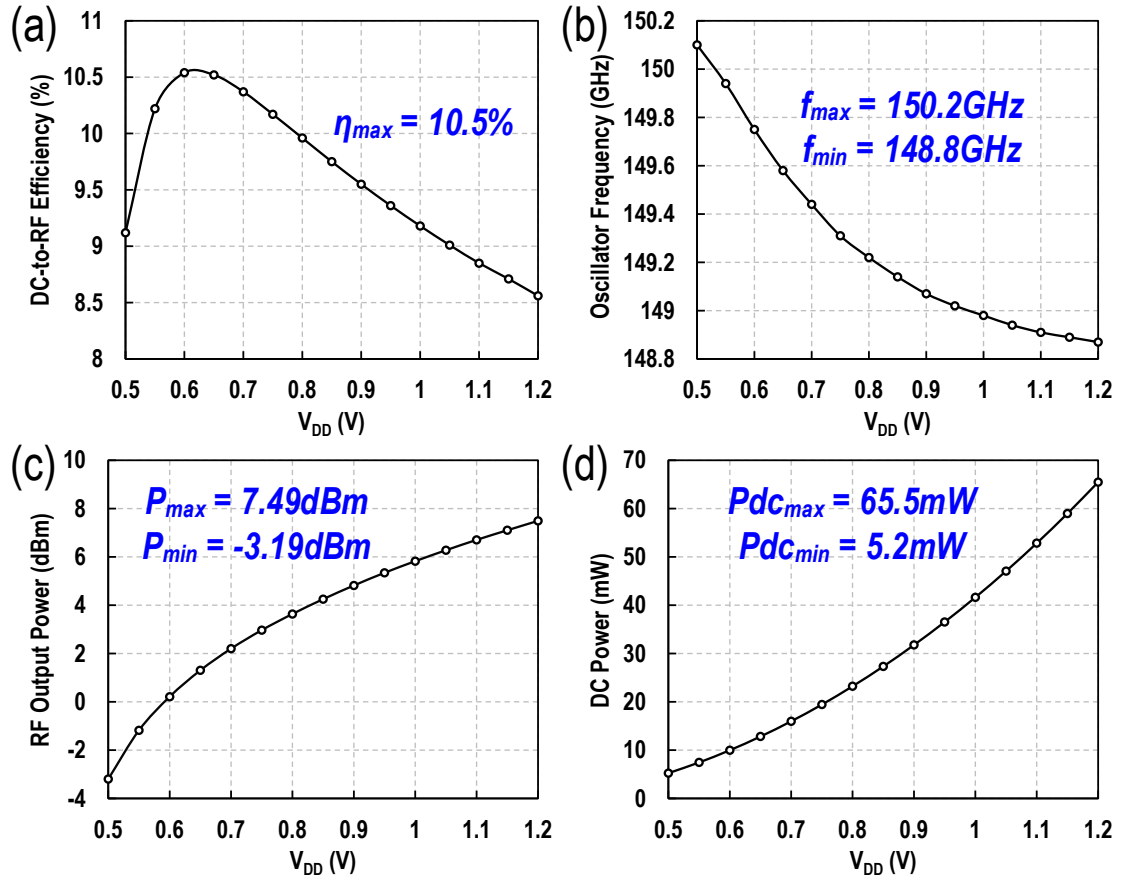


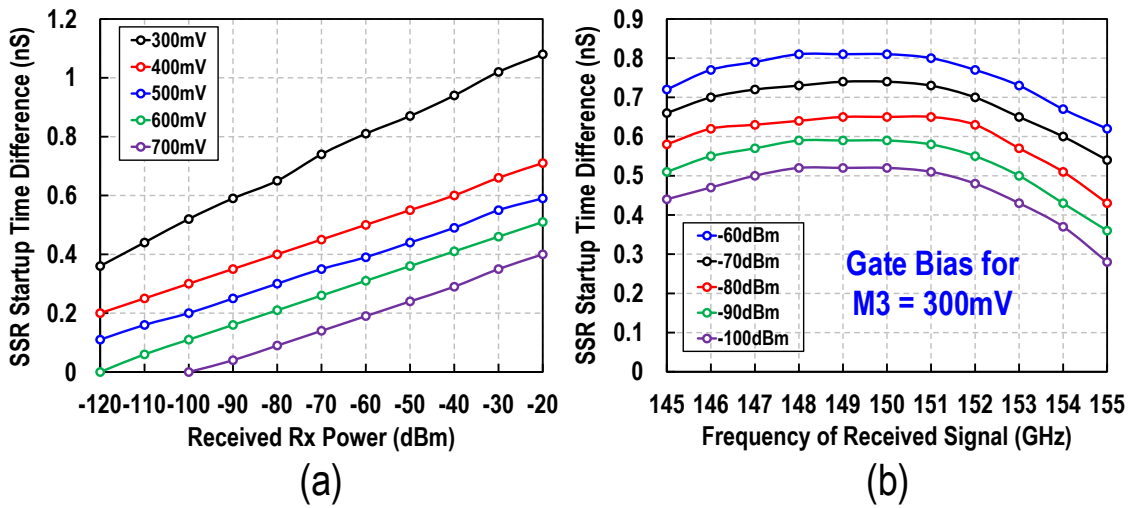
Figure 4-8 – Simulation results in TX mode of (a)DC-to-RF efficiency, (b) frequency tuning, (c) output power, and (d) DC power consumption.

#### 4.2.4 Receiver Mode

In the RX mode, the oscillator is reconfigured as a super-regenerative receiver operating at the fundamental frequency of 150GHz and supporting OOK modulation. Figure 4-9(a) shows the receiver schematic. The SRR is enabled by biasing the source of the injection transistor MRX to 0.4V; at this bias point MRX exhibits the highest gain. The operation of the SRR is explained as follows. M3 is driven by a quench signal that turns the coupled oscillator on and off. When the incoming sub-THz signal is received by the on-chip patch antennas MRX injects a small current into the resonant tank which changes the oscillation start-up time. The difference in oscillator start-up time is used to detect the



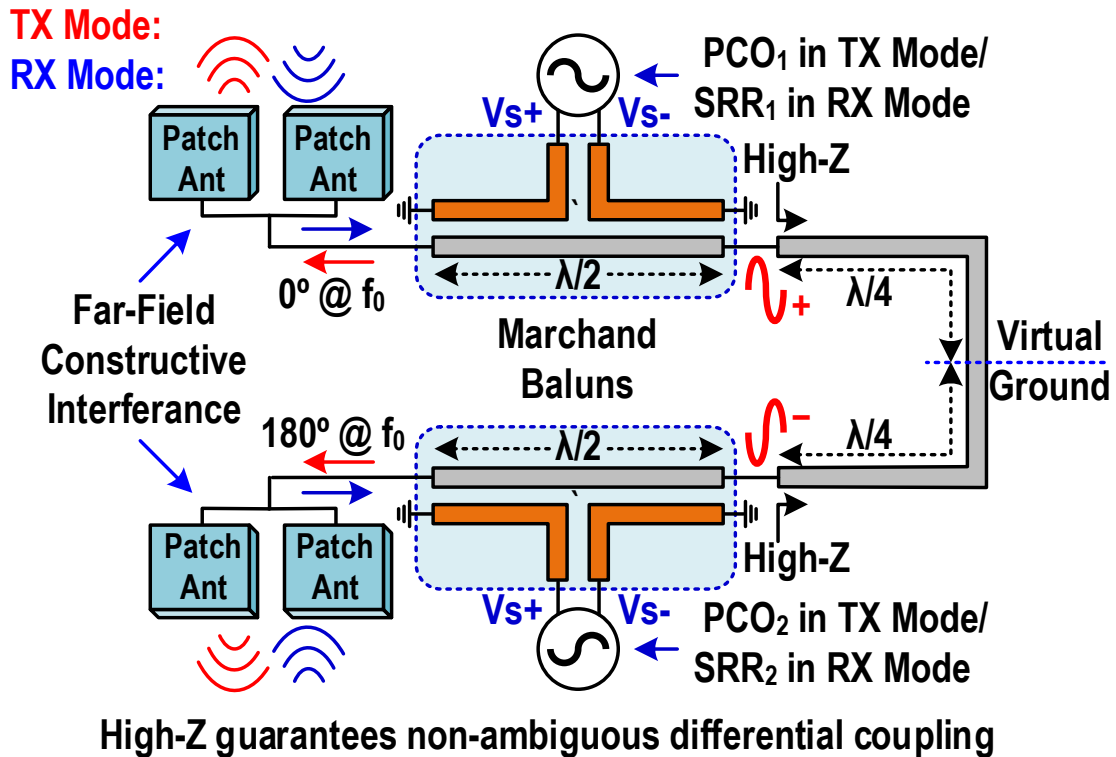
the gate biasing of M3 increases the oscillator start-up time and changes the RX sensitivity, as shown in Figure 4-10(a). Based on simulations, a biasing of 300mV maximizes the RX sensitivity and helps in reducing the RX power consumption. Moreover, the SRR shows a band-pass frequency response with respect to the received RX signal. The sensitivity increases when the frequency of the incoming RX signal is close to the resonance frequency of the oscillator, as shown in Figure 4-10(b). Simulations demonstrate that the super-regenerative receiver is an excellent candidate for a low-power bidirectional radio since it provides enough sensitivity for meter-long communication distances at 150GHz.



**Figure 4-10 – Simulation results in RX mode of SRR start-up time difference as a function of (a) received RX power under varying bias points and (b) frequencies of the received signal.**

#### 4.2.5 Coupling Network

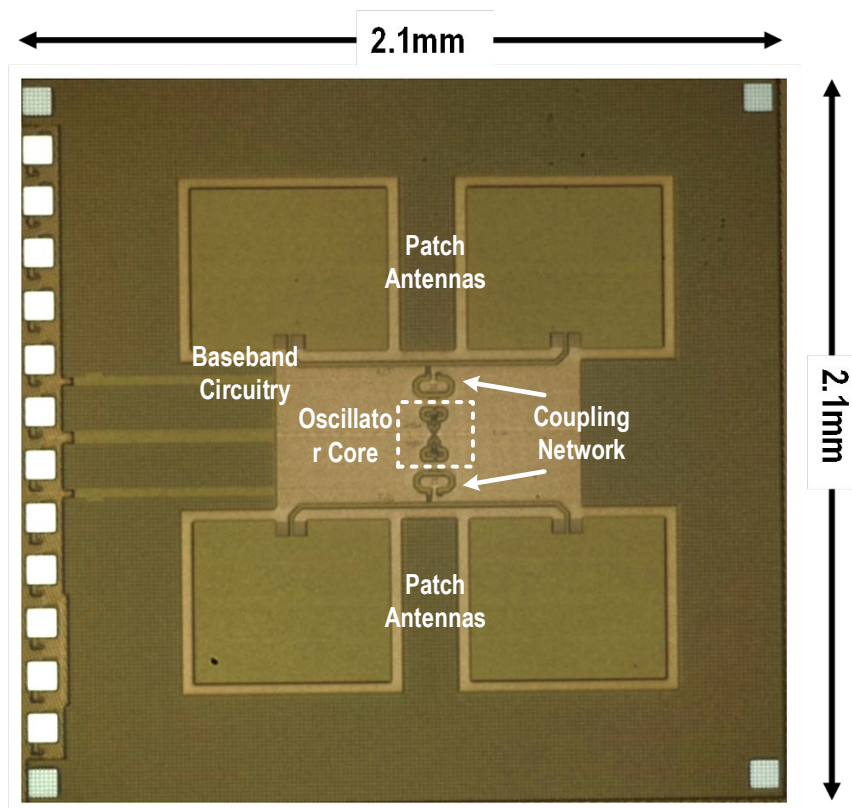
A Marchand balun is used to transition from a differential output of the oscillator ( $V_{s+}$  and  $V_{s-}$ ) to the single ended input/output of the patch antenna pair. Secondly, it serves as the core of the coupling network used to ensure that the outputs of the two oscillators are 180° out of phase, and third it is used to provide the DC path to ground for the source terminal of M<sub>1</sub> and M<sub>3</sub>. The coupling network implementation is shown in Figure 4-11.



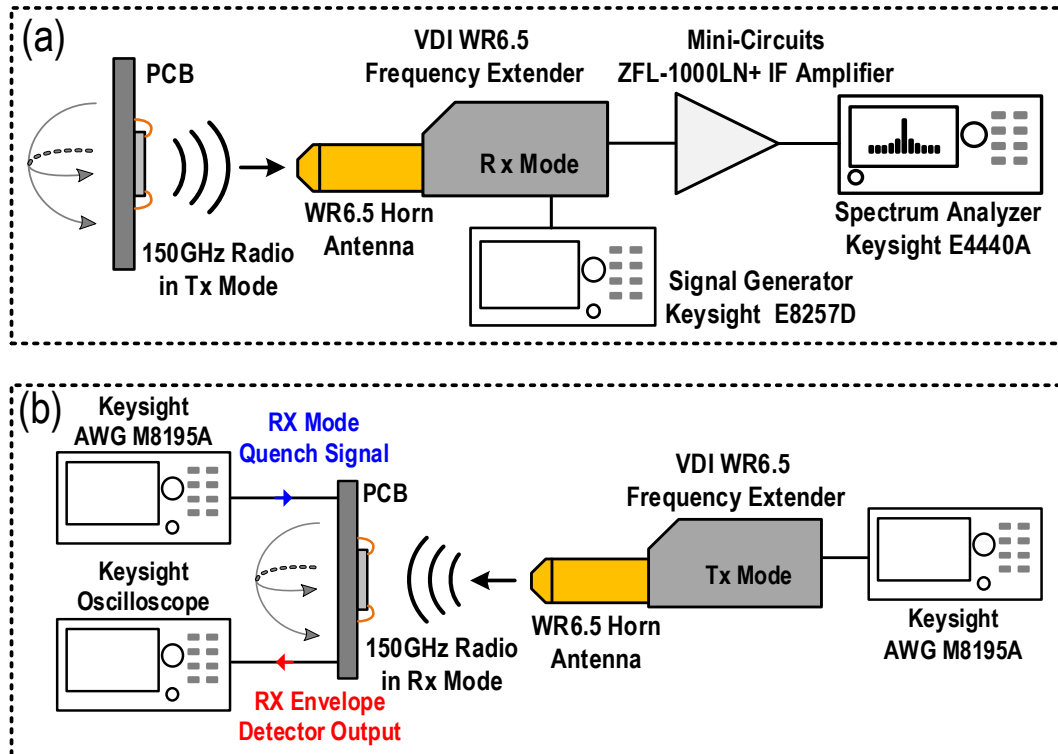
**Figure 4-11 – Proposed oscillator coupling mechanism based on Marchand baluns.**

The Marchand balun is based on a coupled-line structure where the  $TL_1$  choke inductor is also used as one of the coupled-lines that form the Marchand balun. Conventionally, one end of the second coupled-line is employed to route the power to the single-ended load while the other end is left open. The proposed coupling network presented here uses the open termination of the second coupled line to connect the two Marchand baluns together through a  $\lambda/2$  transmission line, which guarantees non-ambiguous differential coupling. When the oscillators are locked differentially, an artificial ground is formed at the center of the  $\lambda/2$  transmission line providing  $\lambda/4$  impedance transformation from a low impedance to the high impedance needed for the Marchand balun to work properly. In addition, the  $\lambda/2$  transmission line also provides the adequate electrical length needed for a differential coupling. Since the  $\lambda/2$  transmission line provides a high impedance path, ideally very little power is dissipated into the coupling structure.

To summarize, our sub-THz transceiver achieves high DC-to-RF efficiency by implementing a Colpitts oscillator where the source terminal is used as the output port. This allows the decoupling of the oscillator tank's resonant frequency from the antenna impedance and allows for a high-Q resonant tank at the drain which increases the voltage swing at the drain and gate of the transistors. These high voltage swings maximize the oscillator's DC-to-RF efficiency. Moreover, we employ a unique approach to couple the two oscillators by using a low-loss Marchand balun-based coupling structure, which also serves to perform differential to single-ended conversion and to provide the appropriate choke or DC path to the oscillator's source terminal. In doing so, the power wasted in oscillator coupling is minimized, which also maximizes the DC-to-RF efficiency.



**Figure 4-12 – Chip micrograph of the prototype low-power bidirectional TRX with a total area of 2.1mm×2.1mm.**



**Figure 4-13 – (a) CW TX measurement characterization setup, (b) RX measurement setup used to measure oscillator startup time, and (c) measurement setup image.**

### 4.3 Measurement Results

A prototype of our 150 GHz miniature low-power radio is implemented in the GlobalFoundries 45nm SOI CMOS process and occupies an area of 2.1mm×2.1mm including on-chip antennas and DC pads. Our chip prototype is attached and wire-bonded to a PCB to provide the appropriate DC connections and biasing. The chip micrograph is shown in Figure 4-12. Two different measurement setups are used to characterize the TX and RX performance, as shown in Figure 4-13. In addition, chip-to-chip wireless measurements are performed to demonstrate the bidirectional communication capabilities of our prototype. All over-the-air measurements are performed without a silicon lens, as shown in Figure 4-14.

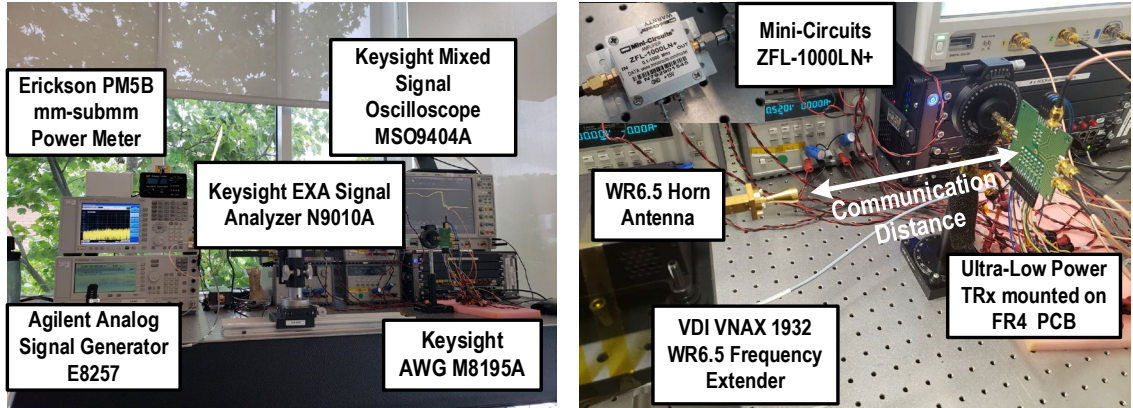


Figure 4-14 – Transceiver measurement setup.

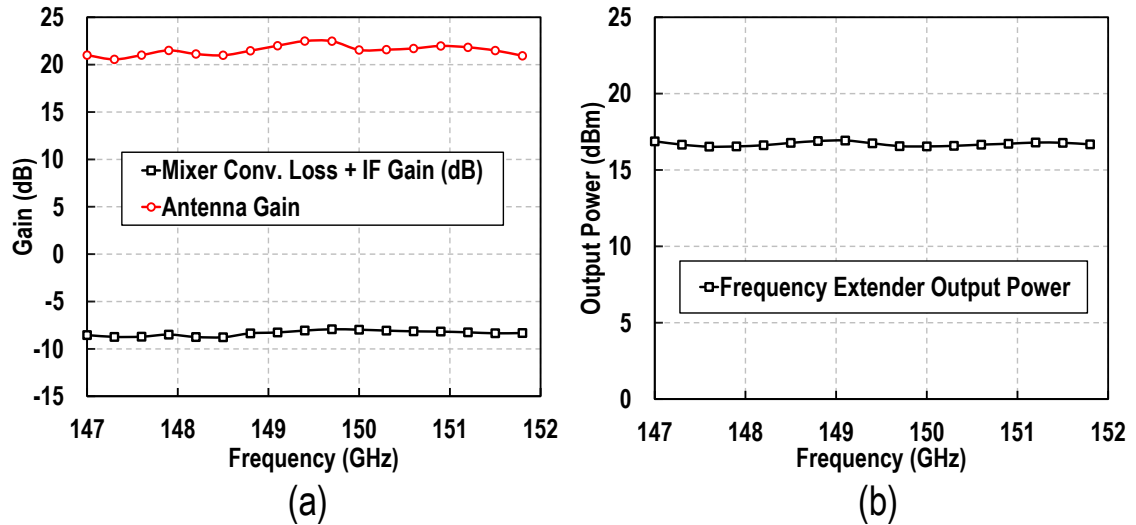


Figure 4-15 – (a) Measured antenna gain and mixer conversion loss plus IF power amplifier gain. (b) Measured frequency extender output power.

A VDI WR6.5 frequency extender is used as a downconversion mixer for TX characterization measurements and as a sub-THz power source for RX measurements. In addition, a conical WR6.5 horn antenna is attached to the frequency extender for all wireless measurements. Conversion gain and power output of the frequency extender/IF amplifier and horn antenna gain are carefully measured prior to chip characterization to de-embed the measurement equipment from the results. Sub-THz power calibration are

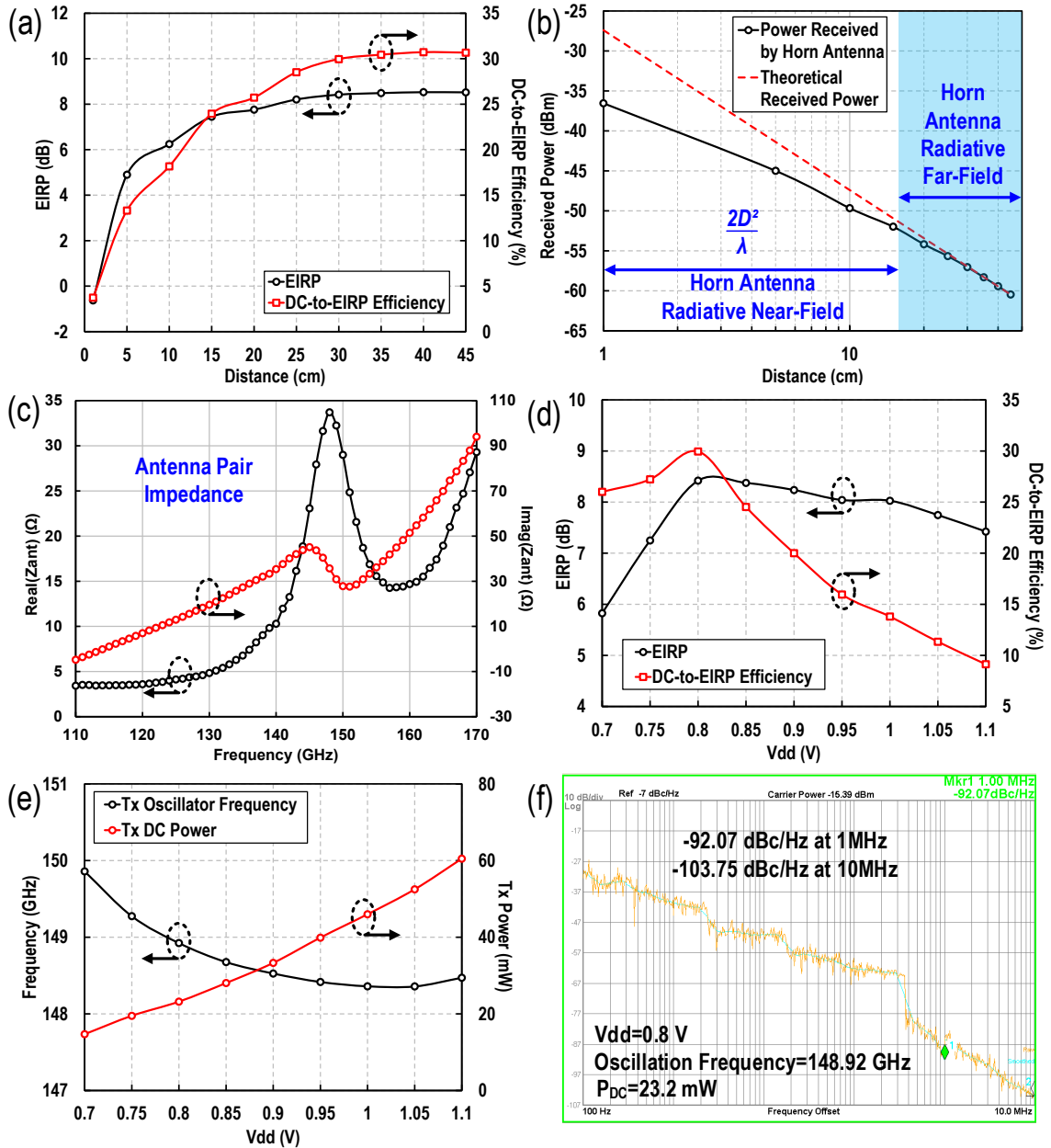
performed using an Erickson PM5B power meter. The calibration data is shown in Figure 4-15. For all wireless measurements, the PCB and the frequency extender are mounted on a movable stage to control the distance and angle between the device under test (DUT) and the horn antenna/frequency extender. This section presents all measurement results for the continuous wave (CW) TX characterization, RX performance, and chip-to-chip communication link.

#### 4.3.1 TX Mode

A VDI WR6.5 frequency extender is used to downconvert the incoming radiated signal to 500MHz from the DUT. A conical WR6.5 horn antenna with a gain,  $G_{Ant}$ , of 21.5dB is connected to the output of the frequency extender to receive the incoming signal. An Agilent Analog Signal Generator E8257 is connected to the frequency extender to generate the appropriate LO signal to downconvert the incoming 150GHz carrier from the DUT. In addition, a Mini-Circuits ZFL-1000LN+ was used as the IF Amplifier. To measure the EIRP of the TX the IF power,  $P_{IF}$ , was measured using a Keysight E4440A Spectrum Analyzer. Then, the TX EIRP was calculated by using the following equation:

$$EIRP = P_{IF} - G_{IF} - CL_{Mixer} - G_{Ant} + FSPL \quad (1-5)$$

where  $CL_{Mixer}$  is the conversion loss of the mixer,  $G_{IF}$  is the gain of the IF amplifier, and  $FSPL$  is the free-space path loss [95]. The IF power was then measured as the DUT to horn antenna/frequency extender distance was increased from 1cm to 45cm. Figure 4-16 shows the complete CW TX measurement results. The TX exhibits an EIRP of 8.52dBm with a DC-to-EIRP efficiency 30.7% at a distance of 45cm. It can be seen from our measurements that the EIRP increases as the distance is increased due to changes from near-field to far-field propagation due to the horn antenna radiative near-field as shown in Figure 4-16(b).



**Figure 4-16 – Transmitter CW measurement results of (a) EIRP, DC-to-EIRP efficiency, and (b) received power as a function of TX-to-RX distance. (c) Measured patch antenna pair impedance. d) EIRP, DC-to-EIRP efficiency, and (e) received power by horn antenna as a function of V<sub>DD</sub>. (f) Oscillator phase noise measurement.**

To demonstrate the tunability of the TX, the DUT was characterized for different values of V<sub>DD</sub> voltages while maintaining a fixed TX-to-RX far-field distance of 30cm.

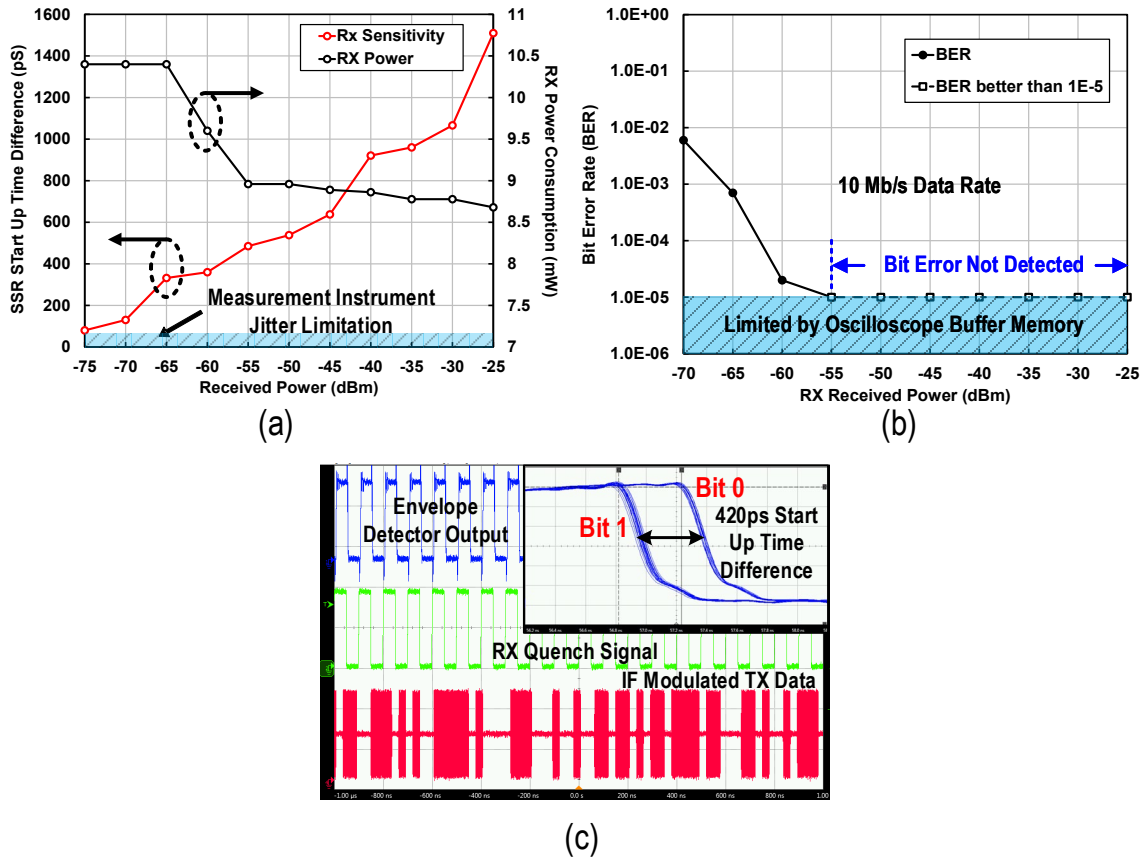
The highest DC-to-EIRP efficiency was achieved for a VDD of 800mV (Figure 4-16(d)). By varying the supply voltage, the transmitter achieves a 1.34% frequency tuning range from 149 to 151GHz (Figure 4-16(e)). The minimum phase noise obtained was -92.07 dBc/Hz at 1MHz offset while using a VDD of 800mV (Figure 4-16(f)).

A separate patch antenna structure is also implemented to verify the effectiveness of our adaptive metal fill and antenna design methodology. For the antenna test structure, 1-port S-parameter measurements were performed from 110 to 170GHz. A GSG high frequency probe (MPI Corporation) and a Keysight PNA-X 5247B are used for the testing. The probe and cables were first calibrated using the MPI AC-2 calibration substrate prior to the measurement. A clear resonance at 149GHz can be seen from the measurements shown in Figure 4-16(c). Furthermore, a measured antenna impedance of  $28.9\Omega$  was obtained at 150GHz, which is very close from the  $26.1\Omega$  obtained from our HFSS 3D EM simulations, demonstrating the robustness of our adaptive metal fill and design methodology.

#### 4.3.2 *RX Mode*

The RX sensitivity is characterized by measuring the difference in the oscillator start-up time when a 150GHz signal is present at different received power levels. The frequency extender (VDI WR6.5) together with the horn antenna are used as the sub-THz transmitter for all measurements. A 10Mb/s OOK modulated signal is generated using an arbitrary waveform generator (AWG) (Keysight M8195A) and applied to the frequency extender for upconversion to the desired sub-THz frequency. The AWG is also used to generate the quench signal at  $4 \times f_{\text{OOK}}$ . The oscillator start-up time is measured by connecting the output of the envelope detector buffer to a high-speed sampling oscilloscope (Keysight Mixed Signal Oscilloscope MSO9404A). The measured output power of the frequency extender, horn antenna gain, and the free-space path loss are used to calculate

the RX received power at the patch antenna plane. The transmission distance is kept at 30 cm for initial RX characterization. The RX measurement setup is shown in Figure 4-13(b).



**Figure 4-17 – Measurement results of the (a) oscillator startup time for different received power, (b) BER for different received power, and (c) oscilloscope screen capture of the envelope detector output, RX quench signal, and the IF modulated signal connected to the frequency extender used as the TX.**

The overall RX performance shows a maximum sensitivity of -70dBm, including the antenna array gain. The difference between simulations and measurements results for the RX minimum detectable signal is mostly due to the frequency and bias sensitivity of the super-regenerative reiver and the frequency response of the patch antennas. Our simulation results show how the SRR startup time changes as a function of the frequency of the received signal (Figure 4-10(b)) which shows a bandpass behavior; the closer the frequency of the incoming RX signal is to the resonant oscillator frequency, the higher the

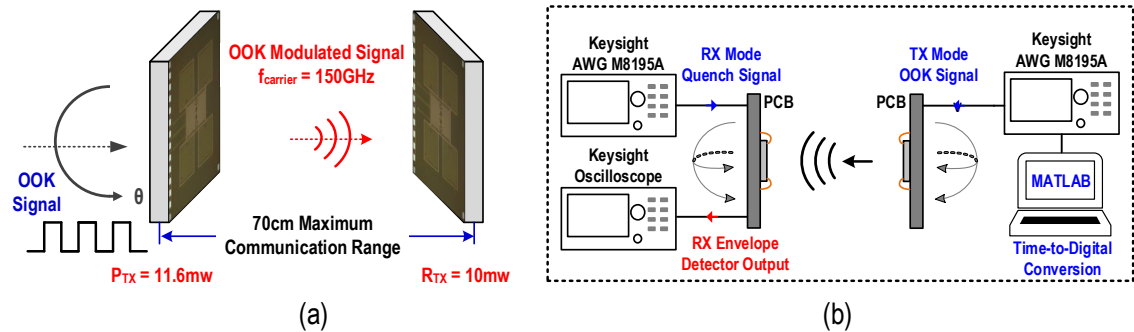
sensitivity. Moreover, the patch antenna frequency response also affects the sensitivity of the receiver since the ability of the incoming signal to propagate through the SRR dependence on the impedance matching between the patch antenna and the Marchand balun.

The minimum oscillator start-up time difference measured when the TX is switched on and off is 130ps, which is limited by the total equipment jitter. The maximum start-up difference is 1.5ns when the received power is -25dBm. The RX power changes from 8.7 to 10.4mW mainly because we adjust VDD to tune the frequency of the RX coupled-oscillators to compensate for any detuning caused by the decrease in received power (Figure 4-17(a)). To further evaluate the RX performance, OOK modulation is performed and the BER is evaluated by saving the envelope detector output waveform for long periods of time on the oscilloscope and comparing it to the original digital data. A MATLAB (MathWorks) script is used to perform the time-to-digital conversion of the envelope detector output. The following equation was used to calculate the test time required for a 95% confidence level in our BER results:

$$Time(seconds) = \frac{-\ln(1 - CL)}{bitrate \times BER} \approx 30ms \quad (1-6)$$

The buffer memory of the oscilloscope restricts our measurements to a BER of  $10^{-5}$  and also the minimum data rate that we can achieve while measuring an acceptable BER. Moreover, the maximum data rate is limited by how fast we can quench the SRR. In our simulations we obtained that it takes close to 5ns to turn on the SRR and 2.5ns to fully quench the oscillation. In measurements we were able to obtain a maximum detectable data rate of 10Mb/s. The variation in simulated and measured data rates is due to the additional time it takes to quench all the remaining small signal oscillations inside the oscillator nodes, which desensitizes the SRR's ability to detect an incoming RF signal.

In summary, the startup time of the SRR is limited by the small-signal gain of the oscillator and the passive loss of the resonant tank, which limits the sensitivity and how fast the oscillator can reach a minimum oscillation amplitude that can be detected by the envelope detector. Moreover, the oscillator turn-off time is limited by the passive losses associated with the resonant tank and all the passive structures that form the Colpitts oscillator. Therefore, the Q factor and transistor gain found in this frequency range is the main limiting factor for the achievable data rate. The degraded sensitivity and response time are inherent tradeoffs for the low power operation of the SRR architecture. A BER lower than  $10^{-5}$  means no error is observed in the data downloaded from the oscilloscope memory. Based on our measurements, the super-regenerative RX achieves a  $BER \leq 10^{-5}$  at/above  $-55\text{dBm}$  received power, and a BER of  $6 \times 10^{-3}$  at the  $-70\text{dBm}$  equipment-limited RX sensitivity (Figure 4-17(b)). Figure 4-17(c) shows the oscilloscope screen capture of the envelope detector output from the TRX test chip configured on RX mode, the RX quench signal applied to the chip configured in RX mode, and the IF modulated signal applied to the frequency extender that was used as the TX to verify the performance of the TRX chip in RX mode.



**Figure 4-18 – (a) Conceptual illustration of chip-to-chip Wireless link measurement demonstration and (b) corresponding wireless link measurement setup using a low-power bidirectional radio chip as a transmitter and a second low-power bidirectional radio chip as a receiver.**

### 4.3.3 Chip-to-Chip Communication Measurement

To demonstrate the suitability of our design as a low-power sensor node, chip-to-chip communication measurements are performed. A 10Mb/s OOK modulated signal is generated using an arbitrary waveform generator (AWG) (Keysight M8195A) and applied to the transceiver in TX mode. The AWG is also used to generate the quench signal at  $4 \times f_{OOK}$ , which is applied to the transceiver in RX mode. The oscillator start-up time is measured by connecting the output of the envelope detector buffer to a high-speed sampling oscilloscope (Keysight Mixed Signal Oscilloscope MSO9404A). The Bit error rate (BER) measurements are performed by saving the envelope detector output waveform on the oscilloscope and comparing it to the original digital data using a MATLAB (MathWorks) script, which is used to perform the time-to-digital conversion of the envelope detector output. Figure 4-18 shows chip-to-chip communication setup. Our measurements demonstrate a  $BER \leq 10^{-5}$  up to 50cm and a BER of  $10^{-3}$  at 70cm chip-to-chip distance.

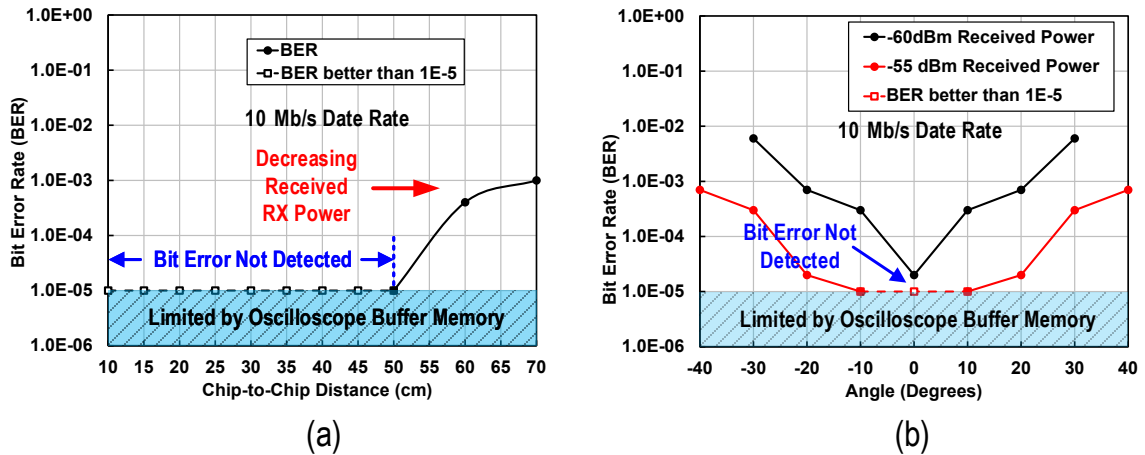


Figure 4-19 – Chip-to-chip wireless measurement results: (a) BER for different chip-to-chip distances and (b) BER at different RX angles.

**Table 4-1 Prior-Art Comparison Table for Sub-THz And THz Transceiver Arrays**

	This Work	ISSCC 2015 [38]	ISSCC 2020 [37]	JSSC 2019 [40]	JSSC 2014 [56]	JSSCC 2019 [33]	CICC 2017 [55]	JSSC 2015 [15]	JSSC 2015 [54]
Freq (GHz)	150	317	668	344	120	530	320	60(TX) / 24(RX)	240
TX,RX,TRX	TRX	TX	TX	TX	TX	TX	TRX	TRX	RX
Chip-to-Chip Measurement	Yes	No	No	No	No	No	No	No	No
Area(mm <sup>2</sup> )	4.41	2.1	0.86	1.2	3.6	2.5	0.57	4.44	2
Array Size	2x2	4x4	4x2	2x2	1x1	1x4	1x1	1x1	1x1
Lens Used	No	Yes	Yes	No	No	No	No	No	No
TX EIRP (dBm)	8.52	22.5	7.4	4.9	NA	2.3	-11.6	-3	NA
Peak Radiated Power(dBm)	2.9	5.2	-16.1	-6.8	NA	-12	NA	NA	NA
RX Sensitivity (dBm)	-70	NA	NA	NA	NA	NA	-89	-10.5	NF=15
DC Power Consumption (mW)	11.6(TX) / 10 (RX)	610	99.7	450	220	260	18.2(TX) / 31.1(RX)	NA	260
DC to EIRP Efficiency(%)	30.7	29.1	5.5	0.69	NA	0.65	0.19	NA	NA
DC to RF Efficiency(%)	8.5	0.54	0.025	0.046	NA	0.02	NA	NA	NA
Phase Noise @1MHz (dBc/Hz)	-92.07	-79	-69	-93.1 (10MHz)	NA	NA	NA	NA	NA
Frequency Tuning Range(%)	1.33	NA	2.36	15.1	NA	0.9	1.25	3.33	NA
Max Communication Distance (cm)	70	9	20	4	18	NA	50	50	2
Modulation Scheme	OOK	NA	NA	NA	QPSK	NA	OOK	M-PMM	QPSK/BPSK
Data Rate (Mb/s)	10	NA	NA	NA	2GB/s	NA	4.4	12	10Gb/s
BER	< 10 <sup>-5</sup>	NA	NA	NA	10 <sup>-11</sup>	NA	10 <sup>-6</sup>	10 <sup>-3</sup>	10 <sup>-6</sup>
Antenna	Patch	Folded Slot	Slotline	Patch	Bondwire Dipole	Patch	Slot	Folded Dipole	Slotted Loop
Architecture	Coupled Colpitts	Harmonic Oscillator	Harmonic Oscillator	Coupled Oscillator	Quadrature PA	ILO Chain	Harmonic Oscillator	VCO/PA	Direct-Conversion
Technology	45nm SOI CMOS	130nm SiGe BiCMOS	40nm CMOS	0.13um SiGe BiCMOS	45nm LP CMOS	40nm Bulk CMOS	45nm CMOS SI	65nm CMOS	65nm CMOS

**Table 4-2 Prior-Art Comparison Table for GHz Transceivers**

	This Work	[4]	[7]	[10]
Freq (GHz)	150	4.15/ 278	2.48	2.44
TX,RX,TRX	TRX	TRX	TRX	TRX
Chip-to-Chip Measurement	Yes	No	No	No
Area(mm <sup>2</sup> )	4.41	5.28	8.4	1.9
Array Size	2x2	1x1	1x1	No On-chip Antenna
Off-chip components	No	2cmx2cm PCB loop antenna - External PA -	31dBm Reader/Antenna	No
TX EIRP (dBm)	8.52	NA	-60	3 (Pout)
Peak Radiated Power(dBm)	2.9	NA	NA	NA
RX Sensitivity (dBm)	-70	-81	NA	-95
DC Power Consumption (mW)	11.6(TX) / 10 (RX)	1.87	0.00128	6.5
DC to EIRP Efficiency(%)	30.7	NA	NA	NA
DC to RF Efficiency(%)	8.5	NA	NA	27
Phase Noise @1MHz (dBc/Hz)	-92.07	NA	NA	-92 @ 5MHz
Frequency Tuning Range(%)	1.33	NA	NA	NA
Max Communication Distance (cm)	70	1	4.5	NA
Modulation Scheme	OOK	OOK	PWM/2-PPM	GFSK
Data Rate (Mb/s)	10	2.5	2Kb/s	1
BER	< 10 <sup>-5</sup>	NA	< 10 <sup>-4</sup>	NA
Antenna	Patch	On-Chip Dipole - Off-chip Loop	Off-chip loop antenna	NA
Architecture	Coupled Colpitts	Power Oscillator	Back-scattering	PA/ADPLL
Technology	45nm SOI CMOS	130nm CMOS	180nm CMOS	28nm CMOS

To further characterize the functionality of the wireless link, we keep the TX chip location and orientation fixed and rotate the RX chip in the azimuthal plane. Thanks to the wide beamwidth of the 2x2 patch antenna array and no use of silicon lens, we demonstrate a BER of <10<sup>-3</sup> from -40° to +40° for a TRX distance of 30cm and an input power up to -55dBm and a of BER of <10<sup>-2</sup> from -30° to +30° for a TRX distance of 50cm. The low

power transceiver prototype consumes 11.6 mW and 10 mW after duty-cycling for the TX and RX, respectively. Due to the low power nature of this design, the sensitivity of the receiver is lower than conventional downconversion transceivers since we do not employ a power hungry LNA at the front-end. These link BER measurements and large FoV demonstrate that our low-power radio prototype can support reliable peer-to-peer bidirectional wireless links. Our measurement results are shown in Figure 4-19.

Table 4-1 compares this work with the state-of-the-art silicon based mm-Wave to THz transceivers. The TRX implementation presented here achieves the highest DC-to-EIRP efficiency and lowest power consumption. Moreover, our antenna design methodology allowed for this TRX implementation to perform very close from the simulated results. To the best of the author's knowledge, this work is one of the first to demonstrate low-power sub-THz communication over both a 70cm distance and  $-40^\circ$  to  $40^\circ$  scan angle with no phase-shifting and without the need of silicon lenses.

Moreover, Table 4-2 provides a comparison of our work with transceivers at GHz frequencies. Although GHz transceivers achieve ultra-low power, our proof-of-concept can achieve a fully integrated chip-to-chip communication platform without the need for external power-hungry PAs or bulky antennas.

#### **4.4 Conclusion**

This chapter presents a lens-free and low-power sub-THz 2-way radio with on-chip antennas supporting 10Mb/s OOK chip-to-chip communication. The TRX is based on a differential Colpitts oscillator that can be reconfigured as a sub-THz power source (TX mode) and as a super-regenerative receiver (RX mode). An on-chip patch antenna array is implemented with an adaptive metal fill that ensures accurate modeling of the antenna impedance and gain, avoiding the need for bulky silicon lenses. As a proof-of-concept, a sub-THz TRX is implemented in the GlobalFoundries 45nm CMOS SOI process

occupying an area of  $2.1\text{mm}\times 2.1\text{mm}$  and achieves a maximum EIRP of  $8.52\text{dBm}$  with a DC-to-EIRP efficiency of  $30.7\%$  with no silicon lens. By varying the supply voltage, the chip achieves a  $1.34\%$  tuning range and minimum phase noise of  $-92.07\text{ dBc/Hz}$  at  $1\text{MHz}$  offset. The super-regenerative RX achieves a sensitivity of  $-70\text{dBm}$  limited by the equipment jitter and a maximum chip-to-chip communication distance of  $70\text{cm}$ .

The moderate  $2\times 2$  array size with no silicon lens offers an ample FoV of  $\pm 40^\circ$ , which eases node finding and link establishment in deployment. This work achieves the highest DC-to-EIRP efficiency with no lens among the integrated mm-Wave/sub-THz transceivers and oscillators. Our ultra-compact design, large FoV, and demonstrated meter-range peer-to-peer communication distance makes our prototype ideal as a stealth sensor node for distributed mesh networks.

## **CHAPTER 5. THE DUAL-DRIVE POWER AMPLIFIER: THE NEXT FRONTIER IN POWER AMPLIFICATION**

Power amplifier (PA) efficiency and linearity are key performance metrics for the deployment of next generation wireless data systems. This chapter presents a new dual-drive PA topology targeted at wireless communication applications. This new topology increases the achievable energy efficiency, linearity, and output power of the PA core. Our proposed 2-stage proof-of-concept consists of an input and output transformer-based balun, a common-source (CS) driver (DR), and a cascode dual-drive PA for the 2nd stage. Our new dual-drive PA core architecture employs a dual-drive coupling network to drive the gate and source of the transistors that form part of the PA core, which fundamentally increases the device drain efficiency (DE) beyond that of the CS topology.

### **5.1 INTRODUCTION**

The 5G mm-wave spectrum is opening new opportunities to create over the air systems that operate at high-Gb/s data rates. This next generation network is poised to create a huge impact across multiple industries, such as automotive, health care, consumer products, space, scientific, and military, etc. Most government agencies across the globe have already partitioned and licensed the 5G mm-Wave spectrum, and the main bands were allocated from 24 to 71GHz, with some frequency gaps in between. Therefore, broadband or reconfigurable hardware that operates throughout the entire 5G spectrum is needed for a global 5G network. Some of the advantages that 5G transceivers provide are the compact hardware size, especially the antenna elements. In addition, some mm-wave bands offer specific advantages; for example, at 60GHz oxygen absorption is very high which can be used to create secure communication networks. Moreover, the increasing demand for high Gb/s data rates and service quality in user dense areas is pushing network operators to

deploy infrastructure supporting 5G wireless networks that operate in the mm-Wave portion of the available spectrum. These 5G mm-Wave wireless networks rely on large array-based systems where the RF front-end modules (FEM) with beam forming capabilities, containing low noise amplifiers (LNAs), power amplifiers (PAs), and switches, are being integrated on a single silicon chip [96-106].

In addition, 5G mm-Wave communication systems are required to support Gb/s modulated signals with high spectral efficiency, such as quadrature amplitude modulation (QAM) implemented with large constellation sizes. Furthermore, the 5G New Radio (NR) standard employs orthogonal frequency division multiplexing (OFDM), which increases the peak-to-average power ratio (PAPR) of the corresponding high-order QAM signal. To accommodate 5G NR modulation, average output power requirements, and array size [107-109], PAs must exhibit excellent linearity and high efficiency over a wide output power range [110-114] to ease power and thermal management requirements. Therefore, high performance PAs are critical for the successful and rapid adoption of commercial mm-Wave communication networks since they dominate the overall transceiver power efficiency, thermal management requirements, and overall channel performance.

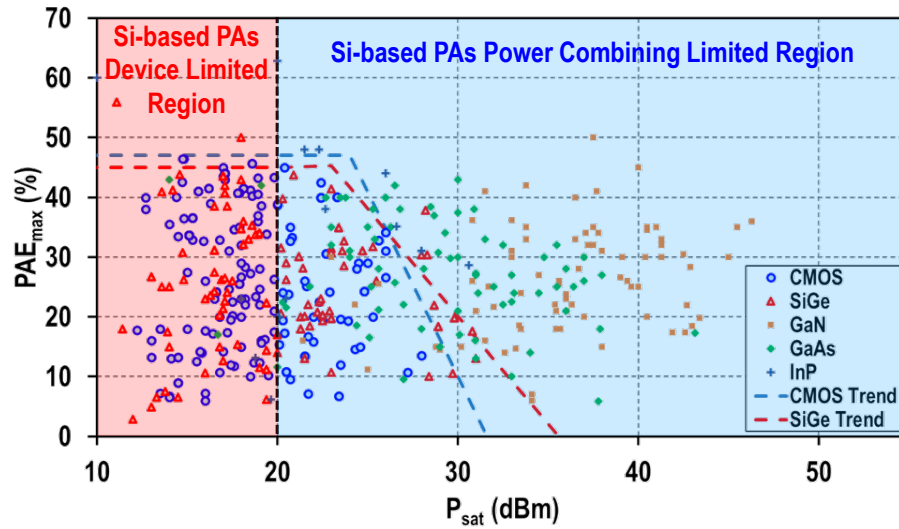
The demand for more efficient and linear mm-Wave PAs for 5G communication networks has produced extensive research to improve the performance at the device level, for example increasing the  $f_{max}/ft$  of the transistor [115-118]. In addition, improvements in back end of the line processes such as thicker and lower loss top metal layers have increased the performance of passive components, which has allowed a further increase in efficiency and output power [4]. With regards to circuit topology improvements, to this date, almost all PA designs rely on common-source or common-gate topologies and are mainly focused on increasing the peak/power-back-off (PBO) PAE and maximum output power ( $P_{out}$ ) by presenting multi-harmonic terminations to the output of the PA, such as the class-F, Class-J, and their inverse and continues mode operation [119-126]. A topology

that has gained popularity in recent years is the harmonic-tuned PA and its different variations. This topology takes advantage of adding load terminations at the fundamental frequency and at some of the harmonics to increase the maximum PAE of the amplifier. Most modern technology nodes exhibit an  $F_{\max}$  and  $F_t$  between 100 to 200GHz, therefore at mm-Wave the harmonic content is not substantial enough to make a significant improvement in efficiency. Furthermore, the efficiency improvement is only possible when the PA exhibits large non-linearities near the saturation power ( $P_{\text{sat}}$ ), which makes it very hard to modulate a signal efficiently. Additionally, passive networks that can provide harmonic tuning tend to be complex and lossy, further reducing the efficiency enhancement [127]. Even though this technique shows low to moderate efficiency improvements, the beforementioned drawbacks hinder its adoption into commercial applications [128].

Recent efforts have also been focused on further improving the efficiency of existing topologies that can support complex modulation methods, such as stacked, outphasing, mixed-signal, reconfigurable, and Doherty PAs [114, 129-133]. However, in modern silicon processes with nanometer sized technology nodes that employ supply voltages of less than 1V per stacked transistor, these reported techniques see diminishing returns on PAE and  $P_{\text{out}}$  since the transistor knee voltage,  $V_{\text{knee}}$ , becomes a significant portion of the supply voltage [134]. Moreover, extra reduction in supply voltage is often observed in practical deployment to ensure device reliability. This is especially relevant for mm-Wave array operations, where array element couplings result in substantial antenna impedance mismatches (VSWR) and undesired large PA output voltage/current swings [135]. Although the reported techniques have improved overall PA efficiency at mm-Wave, their operation principles are incapable of theoretically surpassing the linear mode operation PA core efficiency of the class B CS PA topology without resorting to lower conduction angle or harmonic shaping. To overcome the aforementioned issues, in this

manuscript we present an improved version of the dual-drive power amplifier topology [3] on a GlobalFoundries 45nm CMOS SOI process with high resistivity silicon substrate.

This chapter is organized as follows. Section 5.2 presents the overall proposed architecture of the dual-drive PA. Section 5.3 presents the measurement results and compares our work with the state of the art. Finally, Section 5.4 concludes this article.



**Figure 5-1** Survey of published PAs from 20 to 50GHz showing PAE versus saturated power for different transistor technologies [67].

## 5.2 Efficiency Considerations for Power Amplifiers

Figure 5-1 shows  $P_{\text{sat}}$  vs  $\text{PAE}_{\text{max}}$  for previously published PAs covering the frequency range between 20 to 50GHz [67]. From the survey plot we can see that there is an inherent tradeoff between  $P_{\text{sat}}$  and  $\text{PAE}_{\text{max}}$ . In addition, there exist two distinctive power/efficiency regions for PAs delimited by  $P_{\text{sat}}$ . In the red region, called the device limited regime, the efficiency is limited by the technology or device performance characteristics and to some extent by the design topology. In the blue region, called the circuits/combiner limited regime, the increase in power is attained by employing different

power combining techniques and therefore the efficiency is limited by the losses of the output combiner network. This shows a clear tradeoff between saturated output power and maximum efficiency.

Moreover, when considering energy efficiency in power amplifiers, PAE can be characterized by the four independent factors [136] shown in the following equations:

$$PAE = F_{Vmin} \times F_{Gain} \times F_{Matching} \times F_{Waveform} \quad (5-1)$$

$$F_{Vmin} \sim 1 - \frac{V_{min}}{V_{DD}} \quad (5-2)$$

$$F_{Gain} = 1 - \frac{1}{G} \quad (5-3)$$

$$F_{Matching} \sim \frac{Q_{ind}}{Q_{ind} + Q_{transformation}} \quad (5-4)$$

$$F_{Waveform} = 0.5 \sim 0.78 \quad (5-5)$$

where the first factor  $F_{Vmin}$  is associated with the maximum allowed output voltage swing which is determined by the knee voltage of the device and the supply voltage, the second factor  $F_{Gain}$  is related to the gain of the device or the necessary driving power needed to saturate the PA, the third factor  $F_{Matching}$  relates to the passive efficiency of the output network, and the last factor  $F_{Waveform}$  is a constant that depends on the gate biasing of the PA. From these previous definitions we can conclude the following. The first two factors,  $F_{Vmin}$  and  $F_{Gain}$ , are limited by the device choice while the last two factors,  $F_{Matching}$  and  $F_{Waveform}$ , are limited by design choices. Previous topologies aimed at improving the maximum efficiency of the PA were limited to only increasing  $F_{Matching}$  and  $F_{Waveform}$  through design choices. In this manuscript we will further demonstrate that our new dual-

drive topology enables designers additional design freedom in improving the PA performance by artificially reducing the knee voltage of the device, increasing the factor  $F_{Vmin}$  and in turn increasing the overall  $PAE_{max}$  of the PA.

### 5.2.1 Class-B PA Theoretical Efficiency Review

To fully understand the proposed dual drive architecture, we begin with deriving the maximum theoretical drain efficiency of a class-B amplifier. In class-B operation, the transistor is biased at the threshold voltage ( $V_{TH}$ ) and will only conduct current during half of the cycle. When the device is on, the drain current will be proportional to  $(V_{in} - V_{TH})$ . Therefore, the drain current can be modeled as a half-wave rectified sine wave. Although the transistor drain current has a large frequency content, the passive output network ensures that only the fundamental tone reaches the load. Using Fourier series analysis, we can define the maximum output power as:

$$P_{out} = \frac{V_{peak} \times I_{max}}{2} \quad (5-6)$$

The peak voltage swing at the load,  $V_{peak}$ , can be described in terms of the supply voltage,  $V_{DD}$ , and the knee voltage,  $V_{knee}$ , to include the effects of the device choice:

$$V_{peak} = V_{DD} - V_{knee} \quad (5-7)$$

The DC power dissipation of the transistor can be expressed using the maximum current going through the load,  $I_{max}$ , as shown in the following equations:

$$I_{DC} = \frac{2 \times I_{max}}{\pi} \quad (5-8)$$

$$P_{DC} = 2 \times V_{DD} \times I_{DC} \quad (5-9)$$

Finally, the maximum theoretical drain efficiency of an amplifier operating in class-B mode can be expressed by combining equations (5-6) through (5-9), as shown in (5-10)-(5-13).

$$\eta_{class-B} = \frac{P_{out}}{P_{DC}} = \frac{V_{peak} \times I_{max}}{2 \times V_{DD} \times I_{DC}} \quad (5-10)$$

$$\eta_{class-B} = \frac{(V_{DD} - V_{knee}) \times I_{max}}{2 \times V_{DD} \times \left(\frac{2 \times I_{max}}{\pi}\right)} \quad (5-11)$$

$$\eta_{class-B} = \frac{(V_{DD} - V_{knee})}{2 \times V_{DD} \times \left(\frac{2}{\pi}\right)} = \frac{\pi}{4} \left(\frac{(V_{DD} - V_{knee})}{V_{DD}}\right) \quad (5-12)$$

$$\eta_{class-B} = \frac{\pi}{4} \left(1 - \frac{V_{knee}}{V_{DD}}\right) \quad (5-13)$$

Equation (5-13) shows the canonical class-B maximum efficiency of 78.5% when the  $V_{knee}$  is zero. In addition, (5-13) also establishes the relationship between  $V_{knee}$  and the drain efficiency,  $\eta_{class-B}$ , as previously shown using the proportionality constant  $F_{Vmin}$  in (5-1).

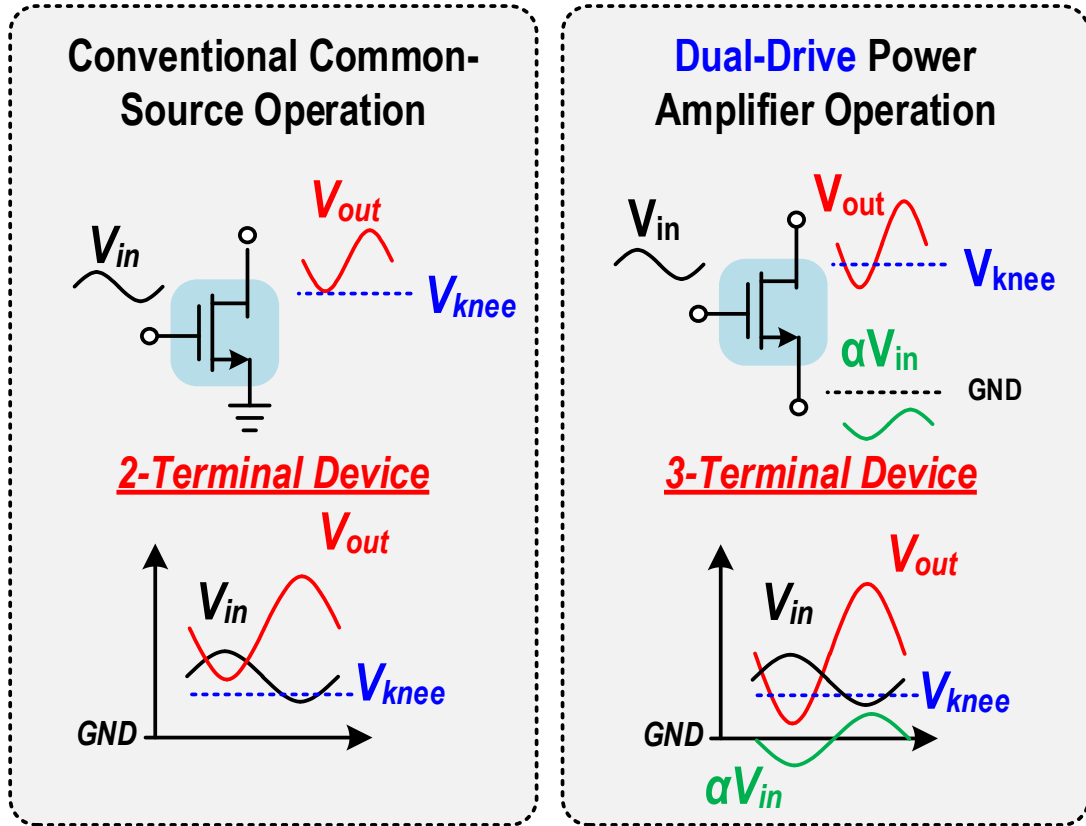


Figure 5-2 Conventional common-source PA topology and proposed dual-drive topology showing gate, drain, and source transient waveforms.

### 5.3 Proposed Dual-Drive Power Amplifier

Most existing PA topologies view the power transistor only as a two-terminal device (i.e., a gate/drain or source/drain configuration), which forms the basis for most analysis of classic PA operation and thus establishes their theoretical efficiency limitations. Inspired by recent research on leveraging the transistor multi-terminal nature for efficient harmonic generation [71], we propose a new dual-drive PA core architecture that exploits the simultaneous driving of the gate and source of the transistor as well as the waveform shaping of the three-terminals (gate, source, and drain), which fundamentally increases the device drain efficiency beyond its two-terminal CS PA counter-part at the same conduction angle and without the need for any harmonically tuned output network. Figure 5-2 shows

the gate, source, and drain waveforms of our proposed dual-drive topology and the conventional CS operation.

When a transistor is only driven at the gate, the device maximum efficiency is dictated by the device conduction angle and the technology specific  $V_{knee}$ , which reduces the peak output voltage swing and restricts the drain efficiency particularly for lower  $V_{DD}$  values, as shown in (5-1) and (5-13). In our proposed topology, we exploit the transistor being a three-terminal device and drive both the gate and the source terminals with out-of-phase inputs  $V_{in}$  and  $\alpha V_{in}$  ( $0 < \alpha < 1$ ), respectively. In our analysis the dual-drive coupling constant,  $\alpha$ , is defined as the voltage ratio between the source and the gate,

$$\alpha = \frac{V_S}{V_G} \quad (5-14)$$

Assuming short terminations for all harmonics at the drain node, the source voltage now swings below ground while having an in-phase relationship with the drain voltage, increasing the maximum drain output voltage swing by  $\alpha V_{in}$ . This increase in the output voltage swing can be attained without having to increase the supply voltage. It will be shown in the next subsection, that the theoretical class-B drain efficiency is increased in the dual-drive topology by a factor greater than 1. This demonstrates that the maximum theoretical efficiency of a PA can be fundamentally increased beyond that of any particular CS PA class, Class-b in this particular example.

### 5.3.1 Dual-Drive PA Theoretical Efficiency Derivation

The maximum drain efficiency of the dual-drive PA can be derived following the same analysis developed for the class-B mode of operation and by adding the term  $\alpha V_{in}$  to  $V_{peak}$ , which represents the additional voltage swing at the source terminal of the transistor as shown in (5-15)

$$V_{peak} = V_{DD} + \alpha V_{in} - V_{knee} \quad (5-15)$$

$$I_{DC} = \frac{2 \times I_{max}}{\pi} \quad (5-16)$$

By inserting (5-15) and (6-16) into equation (5-10) we can derive the maximum drain efficiency of the transistor when it's driven at the gate and source terminals with out-of-phase inputs, which is the foundation of the dual-drive PA topology

$$\eta_{Dual-Drive} = \frac{P_{out}}{P_{DC}} = \frac{V_{peak} \times I_{max}}{2 \times V_{DD} \times I_{DC}} \quad (5-17)$$

$$\eta_{Dual-Drive} = \frac{P_{out}}{P_{DC}} = \frac{(V_{DD} + \alpha V_{in} - V_{knee}) \times I_{max}}{2 \times V_{DD} \times \left(\frac{2 \times I_{max}}{\pi}\right)} \quad (5-18)$$

$$\eta_{Dual-Drive} = \frac{(V_{DD} + \alpha V_{in} - V_{knee})}{2 \times V_{DD} \times \left(\frac{2}{\pi}\right)} = \frac{\pi}{4} \left( \frac{(V_{DD} + \alpha V_{in} - V_{knee})}{V_{DD}} \right) \quad (5-19)$$

$$\begin{aligned} \eta_{Dual-Drive} &= \frac{\pi}{4} \left( 1 - \frac{V_{knee}}{V_{DD}} + \frac{\alpha V_{in}}{V_{DD}} \right) \\ &= \frac{\pi}{4} \left( 1 - \frac{V_{knee}}{V_{DD}} \right) \left( 1 + \frac{\alpha V_{in}}{V_{DD}} \left( 1 - \frac{V_{knee}}{V_{DD}} \right)^{-1} \right) \end{aligned} \quad (5-20)$$

$$\eta_{Dual-Drive} = \frac{\pi}{4} \left( 1 - \frac{V_{knee}}{V_{DD}} \right) \left( 1 + \frac{\alpha V_{in}}{V_{DD}} \left( \frac{V_{DD} - V_{knee}}{V_{DD}} \right)^{-1} \right) \quad (5-21)$$

$$\eta_{Dual-Drive} = \frac{\pi}{4} \left( 1 - \frac{V_{knee}}{V_{DD}} \right) \left( 1 + \frac{\alpha V_{in}}{V_{DD}} \left( \frac{V_{DD}}{V_{DD} - V_{knee}} \right) \right) \quad (5-22)$$

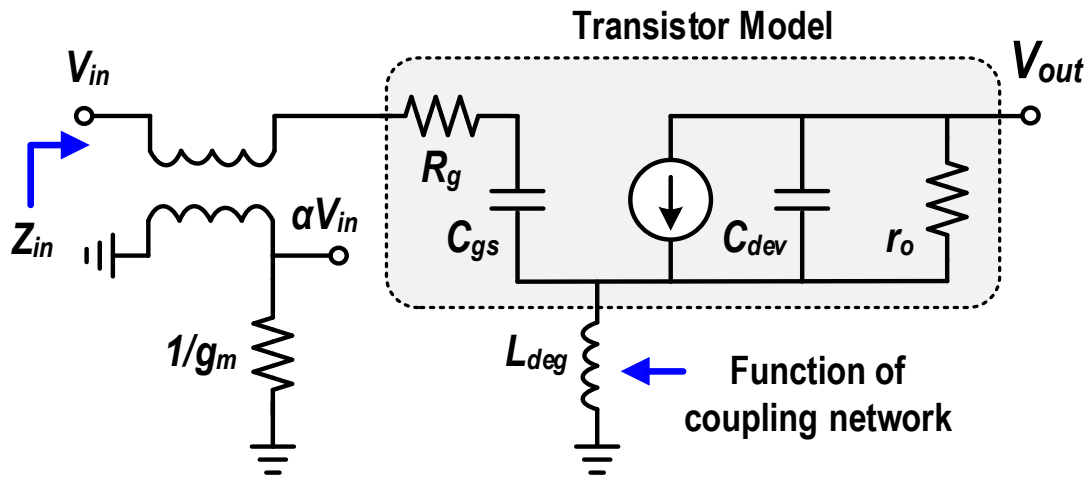
$$\eta_{Dual-Drive} = \frac{\pi}{4} \left( 1 - \frac{V_{knee}}{V_{DD}} \right) \left( 1 + \left( \frac{\alpha V_{in}}{V_{DD} - V_{knee}} \right) \right) \quad (5-23)$$

$$\eta_{Dual-Drive} = \eta_{class-B} \left( 1 + \left( \frac{\alpha V_{in}}{V_{DD} - V_{knee}} \right) \right) \quad (5-24)$$

$$\eta_{Dual-Drive}(\alpha V_{in} = V_{knee}) = \frac{\pi}{4} \quad (5-25)$$

When the maximum voltage swing at the source is equal to the knee voltage of the transistor ( $\alpha V_{in} = V_{knee}$ ), the theoretical maximum drain efficiency for the dual-drive power amplifier will reach the maximum theoretical efficiency of the class-B power amplifier,  $\pi/4$ , as shown in equation (5-25). The strength of the source swing will depend on  $\alpha$ , which is a design constant that can be adjusted. These results show that by employing the dual-drive architecture, we can recover the efficiency lost by the  $V_{knee}$  of the transistor. In addition, our analysis of the dual-drive PA is in line with equation (5-1).

Although input source-gate capacitive coupling is utilized in RF LNAs [137], its purpose is for small-signal gain boosting, and the large-signal behavior and energy efficiency enhancement in PAs has not been explored. Additionally, it should be emphasized that our dual-drive PA topology is different from stacked PAs, since the source of the bottom stacked device is tied to ground, which critically determines the total device output voltage swing [114].



**Figure 5-3 Small signal dual-drive transistor model which includes dual-drive coupling network and inductive degeneration.**

### 5.3.2 Benefits of the Dual-Drive PA

The benefits of the dual-drive PA topology are summarized as follows. First, increasing the source coupling coefficient,  $\alpha$ , can fundamentally increase the PA core drain efficiency beyond that of the CS topology at the same conduction angle (class-A, B, or C biasing). Second, higher drain efficiency can be maintained even at reduced  $V_{DD}$  voltages since the effect of  $V_{knee}$  under a lower  $V_{DD}$  can be mitigated. Third, the  $P_{sat}$  can be increased while reducing the device AM-PM and AM-AM distortion, since the active device spends more time in its saturation region and less in triode.

Furthermore, the parallel input resistance of the transistor is reduced since the device gate impedance is combined in parallel with its low source impedance, which also can be engineered by the source coupling,  $\alpha$ , to ease in the design of broadband and low-loss inter-stage matching networks without the need to implement de-Qing resistors. Figure 5-3 shows the small signal dual-drive transistor model that is used to derive the input impedance, which includes dual-drive coupling network and inductive degeneration. The input impedance of the dual-drive PA core can be expressed using the following equations:

$$Z_{in} = Z_{C_{gs}} \parallel R_p \parallel \frac{1}{\alpha^2 g_m} \quad (5-26)$$

$$Z_{in} = \left( \frac{1}{Z_{C_{gs}}} + \frac{1}{R_p} + \alpha^2 g_m \right)^{-1} \quad (5-27)$$

$$Z_{in} = \left( \frac{1}{\frac{1}{j\omega C_{gs}}} + \frac{1}{R_p} + \alpha^2 g_m \right)^{-1} = \left( j\omega C_{gs} + \frac{1}{R_p} + \alpha^2 g_m \right)^{-1} \quad (5-28)$$

$$Z_{in} = \left( \frac{1 + \alpha^2 R_p g_m + j\omega R_p C_{gs}}{R_p} \right)^{-1} = \frac{R_p}{1 + \alpha^2 R_p g_m + j\omega R_p C_{gs}} \quad (5-29)$$

$$Z_{in} = \frac{R_p \times (1 + \alpha^2 R_p g_m - j\omega R_p C_{gs})}{(1 + \alpha^2 R_p g_m + j\omega R_p C_{gs}) \times (1 + \alpha^2 R_p g_m - j\omega R_p C_{gs})} \quad (5-30)$$

$$Z_{in} = \frac{R_p \times (1 + \alpha^2 R_p g_m) - j\omega R_p^2 C_{gs}}{(1 + \alpha^2 R_p g_m)^2 + (\omega R_p C_{gs})^2} \quad (5-31)$$

$$\text{Real}(Z_{in}) = \frac{R_p \times (1 + \alpha^2 R_p g_m)}{(1 + \alpha^2 R_p g_m)^2 + (\omega R_p C_{gs})^2} \quad (5-32)$$

$$Z_{in} = R_p \parallel \frac{1}{\alpha^2 g_m} \quad (5-33)$$

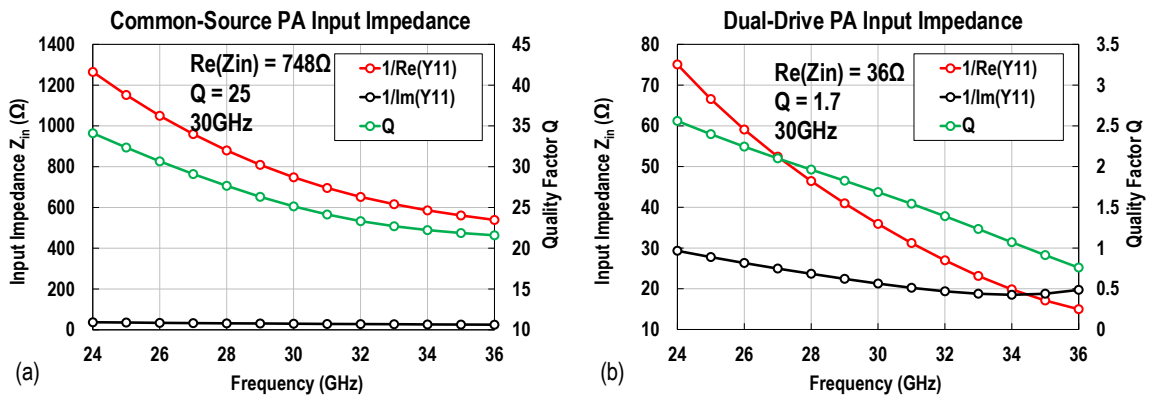
$$Z_{in} = \left( \frac{1}{R_p} + \alpha^2 g_m \right)^{-1} = \left( \frac{1 + \alpha^2 R_p g_m}{R_p} \right)^{-1} = \frac{R_p}{1 + \alpha^2 R_p g_m} \quad (5-34)$$

$$R_{g_{deg}} = g_m X_{C_{gs}} X_{L_{deg}}(\alpha) + R_g \quad (5-35)$$

$$Q_{deg} = \frac{X_{C_{gs}}}{R_{g_{deg}}}; R_p = (1 + Q_{deg}^2)R_{g_{deg}} \quad (5-36)$$

Where  $R_p$  is the parallel representation of the degenerated gate resistance due to the source inductance added by the dual-drive coupling network. The real part of the input impedance,  $Z_{in}$ , will be dominated by the term  $\frac{1}{\alpha^2 g_m}$  as it is the smallest term. Furthermore, the input impedance becomes a design choice and can be easily adjusted by changing the coupling between the source and the gate, as shown in (5-25). Figure 5-4(a) shows the input impedance of a CS PA and Figure 5-4(b) shows the input impedance of a dual-drive with a  $\alpha$  of 0.3.

Finally, the dual-drive PA can mitigate the reliability issues of voltage peaking in complex harmonic-shaping PAs (class-J or continuous-mode class-F PAs). Therefore, our dual-drive PA topology is particularly suitable for high-reliability commercial/defense applications that mandate low supply voltages.



**Figure 5-4** Input impedance of a (a) common-source PA core and (b) dual-drive PA core with an input coupling of 0.3.

## CHAPTER 6. DUAL-DRIVE POWER AMPLIFIER: 38GHZ PA IMPLEMENTATION

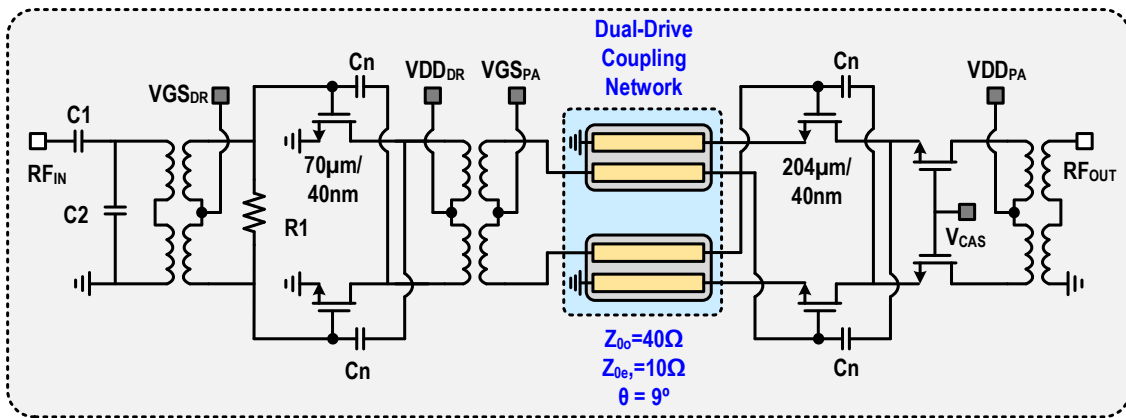
A prototype of a 38GHz dual-drive PA is implemented in the 45nm SOI CMOS process from GlobalFoundries and occupies a total area of  $1.3 \times 1.5 \text{mm}^2$ . The CW measurement results of the dual-drive PA show a maximum  $OP_{1\text{dB}}$  of 18.02dBm at 38GHz and less than 1dB variation from 32 to 41GHz. The dual-drive PA achieves a  $PAE_{\text{max}}$  of 45.32% and a  $DE_{\text{max}}$  of 53.71% at 39GHz for a 1.9V supply, which is 95% of the rated supply voltage. Our PA achieves the highest reported PAE and DE for a 2-stage PA in silicon at mm-Wave frequencies. From 33 to 42GHz the PA also maintains a  $PAE_{\text{max}} \geq 40\%$ . The  $OP_{1\text{dB}}$  and  $P_{\text{sat}}$  are within 1dB throughout the bandwidth with a maximum  $PAE_{OP_{1\text{dB}}}$  of 41.85% at 39GHz. The highest measured  $P_{\text{avg}}$  and  $PAE_{\text{avg}}$  is 12.8dBm and 25.06% for a 250MSym/s 64-QAM signal with -25dB rmsEVM at 38GHz with a 1.8V supply. Other modulation schemes or data rates could not be measured due to equipment limitations.

The schematic of our proof of concept of our 38GHz dual-drive PA is shown in Figure 6-1(a). Our dual-drive PA consists of 2 stages: a CS driver and a dual-drive PA core. Neutralization capacitors are used in both stages to enhance stability and gain. The dual-drive PA core consists of a cascode differential pair composed of transistors  $M_1$  and  $M_2$  as the PA core and a dual-drive coupling network, which provides the coupling between the gate and the source.

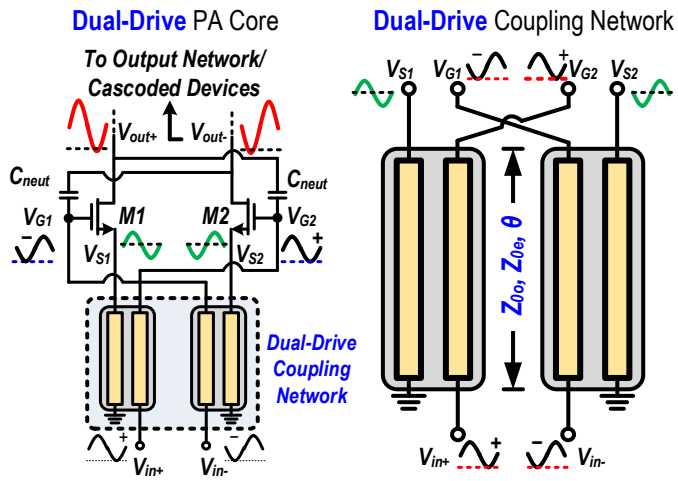
### 6.1.1 Dual-Drive Coupling Network

In summary, the dual-drive PA core shown in Figure 6-1(b) works as follows. The differential input signal,  $V_{\text{in}}$ , is coupled from the gate of  $M_1$  to the source of  $M_2$  and from

the gate of  $M_2$  to the source of  $M_1$ . Providing the appropriate phase relationship and driving strength between gate and source. The coupling network is realized with two identical transmission-line (T-line)-based couplers, where the source driving strength is adjusted in the design flow by modifying the even and odd mode impedances of the coupled lines ( $Z_{0e}$ ,  $Z_{0o}$ ) (Figure 6-1(c)). The impedance seen by the coupled line couplers is equal to the transistor's gate impedance, which differs from  $50\Omega$ , therefore, the coupler's coupling coefficient,  $c$ , and  $\alpha$  are not the same.



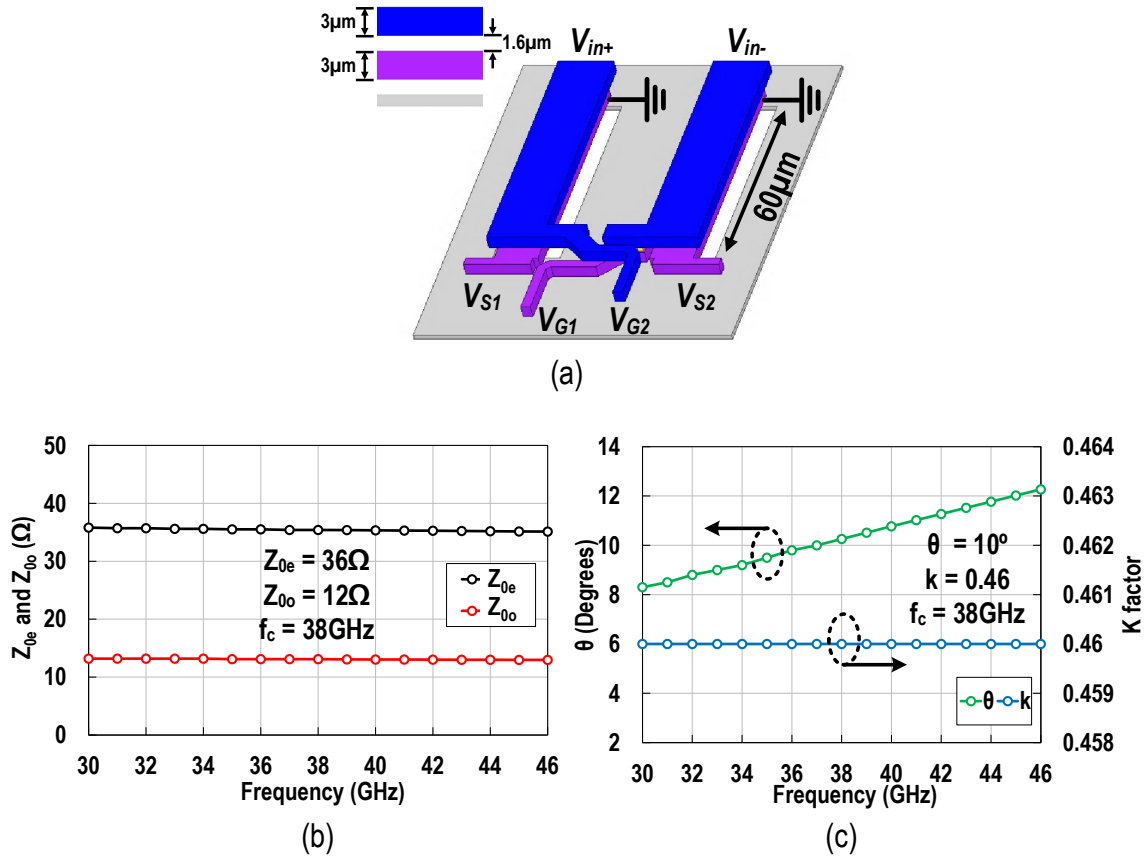
(a)



(b)

(c)

**Figure 6-1 (a) Proposed dual-drive coupling network, (b) dual-drive PA core schematic, and (c) complete 2-stage dual-drive power amplifier.**



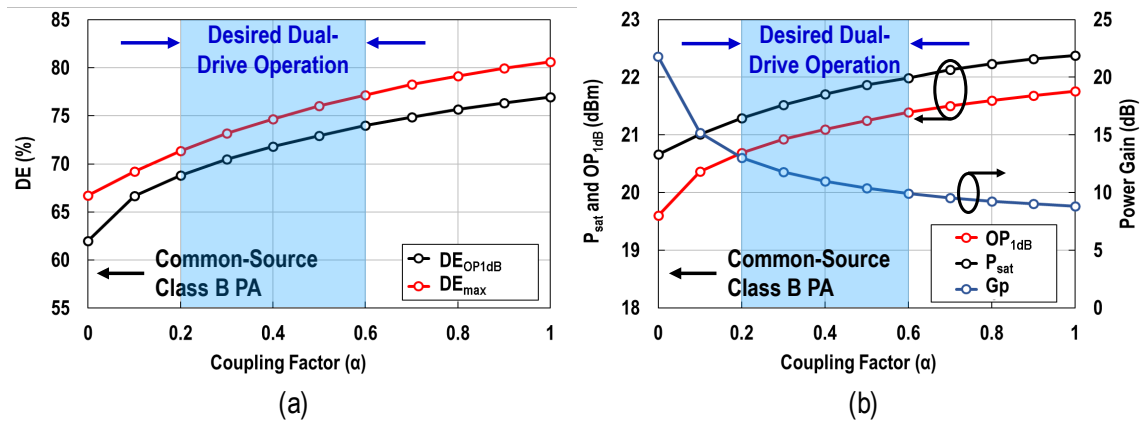
**Figure 6-2 (a) 3D HFSS electromagnetic model of the input dual-drive network. Simulation results of the (b) even and odd mode impedance and (c) electrical length and coupling factor of the input dual-drive network.**

Compared to conventional capacitive coupling networks, the Dual-Drive coupling network accounts for all routing parasitics and can be optimized for the desired amplitude/phase coupling with flexibility. Moreover, the input coupling network naturally offers the appropriate DC biasing for each device terminals, ground for the source and  $V_{gs}$  for the gate, without the need to employ any additional passives. This assumes that the interstage matching transformer between the driver and PA core provides the DC gate biasing through its center-tap. The 3D EM HFSS model is shown in Figure 6-2(a). Moreover, the dual-drive coupling network introduces inductive source degeneration due to the transmission lines' electrical length. The source inductive degeneration lowers the overall device power gain. To counteract this effect, the inductive reactance is minimized

by choosing low values for  $Z_{0o}$  and  $Z_{0e}$  while still maintaining the desired coupling coefficient. Figure 6-2(b) and (c) show simulation results of the even and odd mode impedance, electrical length, and coupling factor of the dual-drive network.

### 6.1.2 Passive Networks for Impedance Matching

The input and output matching networks are based on transformer baluns to provide single-ended input and outputs while utilizing differential PA cores. The input matching network is realized with additional capacitors and a gate de-Qing resistive termination for broadband  $S_{11}$  matching. The inter-stage matching network only uses one transformer without the need to employ gate de-Qing resistors due to the lower real parallel impedance at the dual-drive PA core input ( $748\Omega$  for CS and  $36\Omega$  for dual-drive PAs).

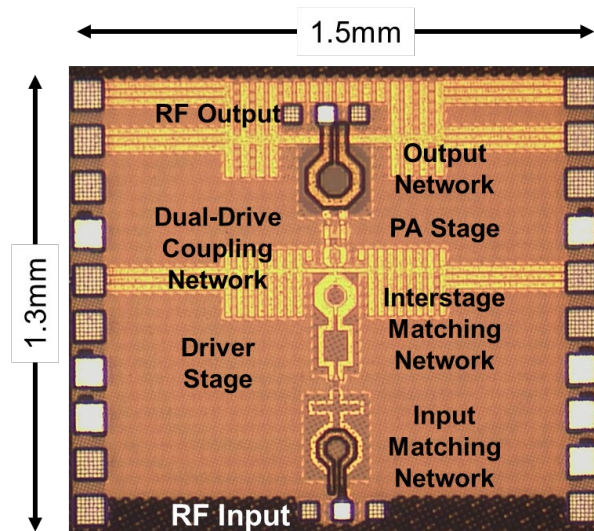


**Figure 6-3 Large signal CW load-pull simulation results using foundry transistor model for different coupling coefficient of the (c) drain efficiency and (d)  $P_{sat}$ ,  $OP_{1dB}$ , and Power Gain.**

### 6.1.3 Constant Wave Large Signal Simulations

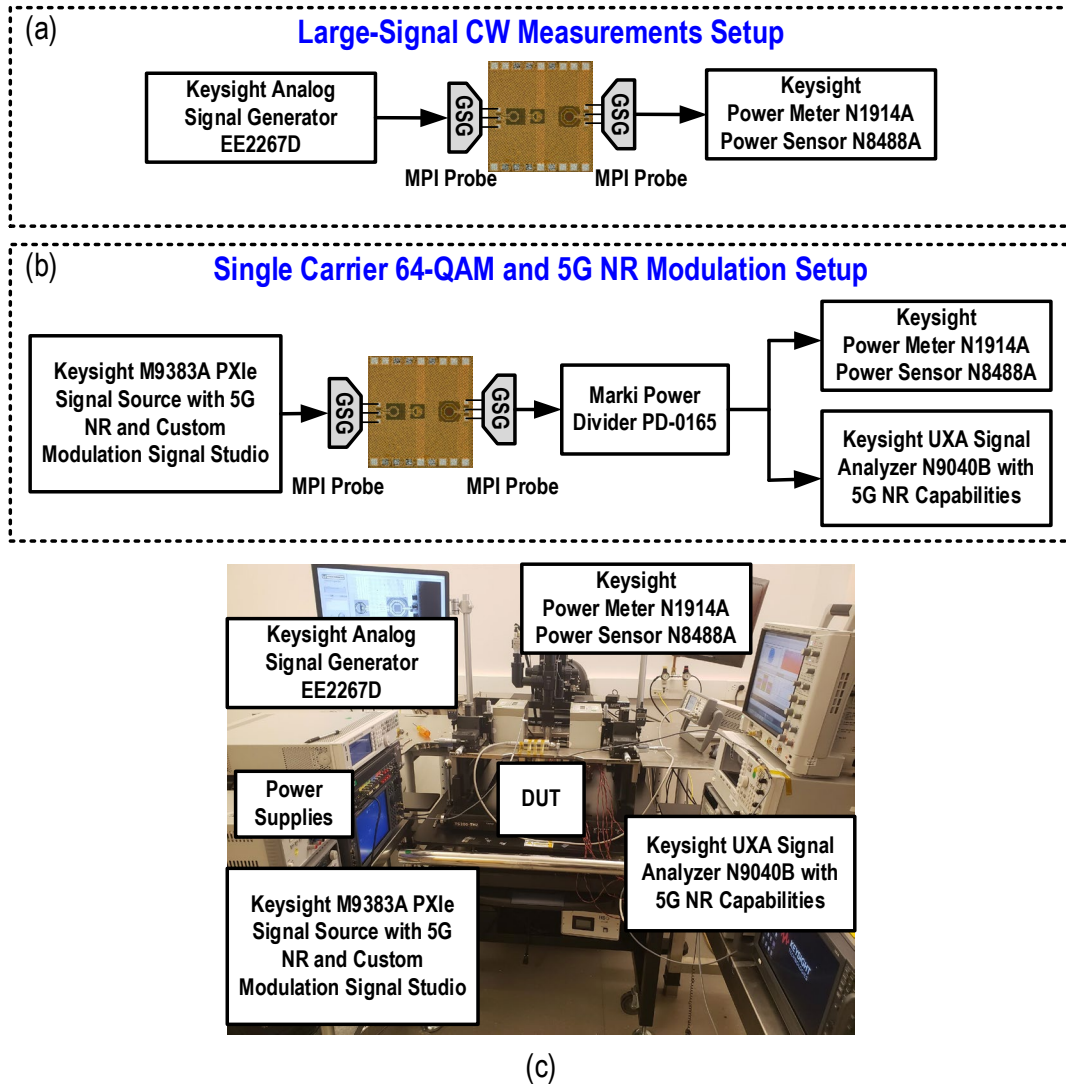
To demonstrate the advantages of the dual-drive topology, we performed large-signal load-pull simulation using the transistor foundry model in addition to the layout dependent extracted parasitics. The results are shown in Figure 6-3. From these results, it

can be observed that as the dual-drive coefficient,  $\alpha$ , increases DE,  $OP_{1dB}$ , and  $P_{sat}$  also increase. The improvement in efficiency and increased output power is due to the larger output voltage swing resulting from driving the source terminal as the coupling coefficient increases. Conversely, as  $\alpha$  increases, the power gain ( $G_p$ ) decreases. The impedance reduction can be understood by looking at the input impedance of the PA core as  $\alpha$  is increased. From (19), the input impedance of the PA,  $Z_{in}$ , is reduced, therefore reducing the voltage gain which in turn reduces the overall power gain. To a lesser extent, in a real implementation the gain is also reduced due to the source inductive degeneration created by the dual-drive coupling network.



**Figure 6-4 Photograph of our proposed 38GHz 2-stage dual-drive PA.**

Based on this analysis, there exists an optimum dual-drive operation/design region where the gain is sufficient to maintain the overall PAE of a 2-stage PA implementation. Moreover, decreases in the PA core gain is offset by the lower loss inter-stage matching network required for the dual-drive PA core since the driver is being matched to a low-impedance node. For our 2-stage PA at 38GHz the design target is to have a gain close to 20dB, which is adequate for any transmitter system, therefore  $\alpha$  was chosen to be 0.4.



**Figure 6-5** Diagram of measurement setup for (a) large-signal CW measurements and (b) modulation measurements. (c) Picture of measurement setup.

## 6.2 Measurement Results

As a proof of concept, our dual-drive PA prototype is implemented in the 45nm SOI CMOS process from GlobalFoundries and occupies a total area of  $1.3 \times 1.5 \text{mm}^2$  with a core area of  $0.25 \text{mm}^2$ . Our chip is attached via silver epoxy and wire-bonded to a PCB to provide the appropriate DC connections and biasing. The chip micrograph is shown in

Figure 6-4. Two different measurement setups are employed to fully characterize the CW and modulation performance of the dual-drive PA, as shown in Figure 6-5.

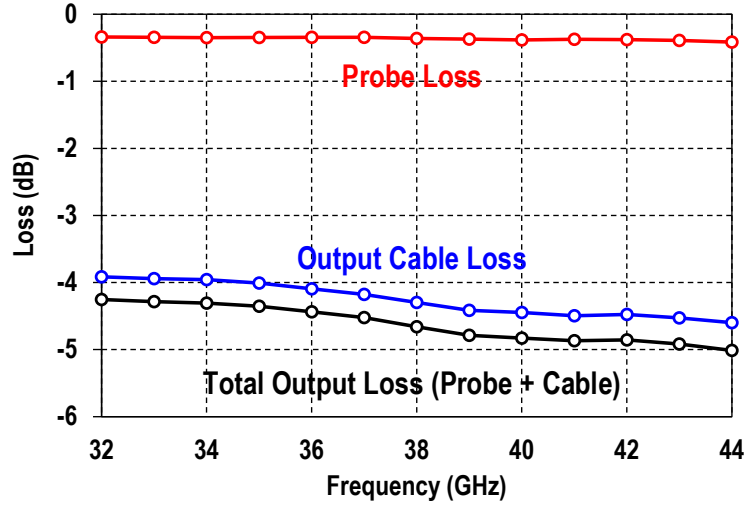


Figure 6-6 Picture of measurement setup and calibration data used in the measurements.

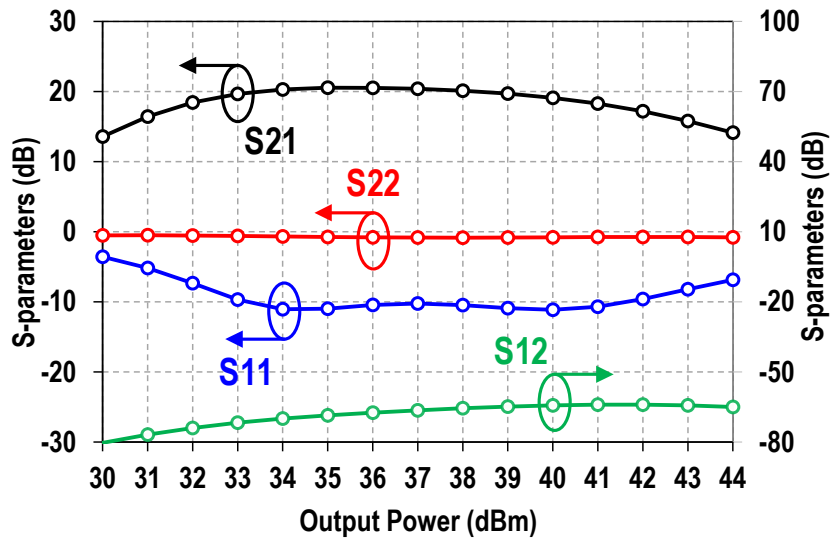
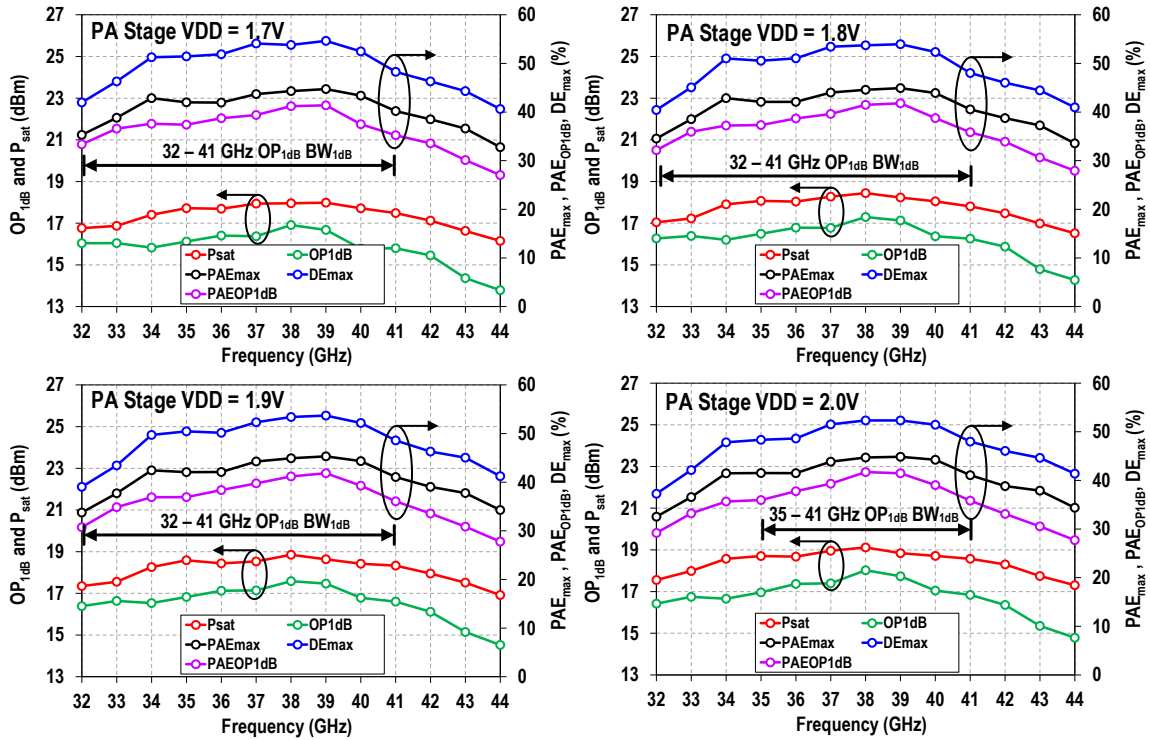


Figure 6-7 Small signal simulation results of the 2-stage dual-drive PA.

All measurements are performed using GSG probes (MPI Corporation) to access the RF input and output on-chip pads. GSG Probes, RF cables, and connector losses are

carefully measured at each frequency point before chip characterization to de-embed the measurement setup from the results. Moreover, the output power of the signal generator is carefully measured for power correction. The calibration data is shown in Figure 6-6. This section presents all measurement results for the continuous wave characterization and modulation performance of the dual-drive power amplifier.

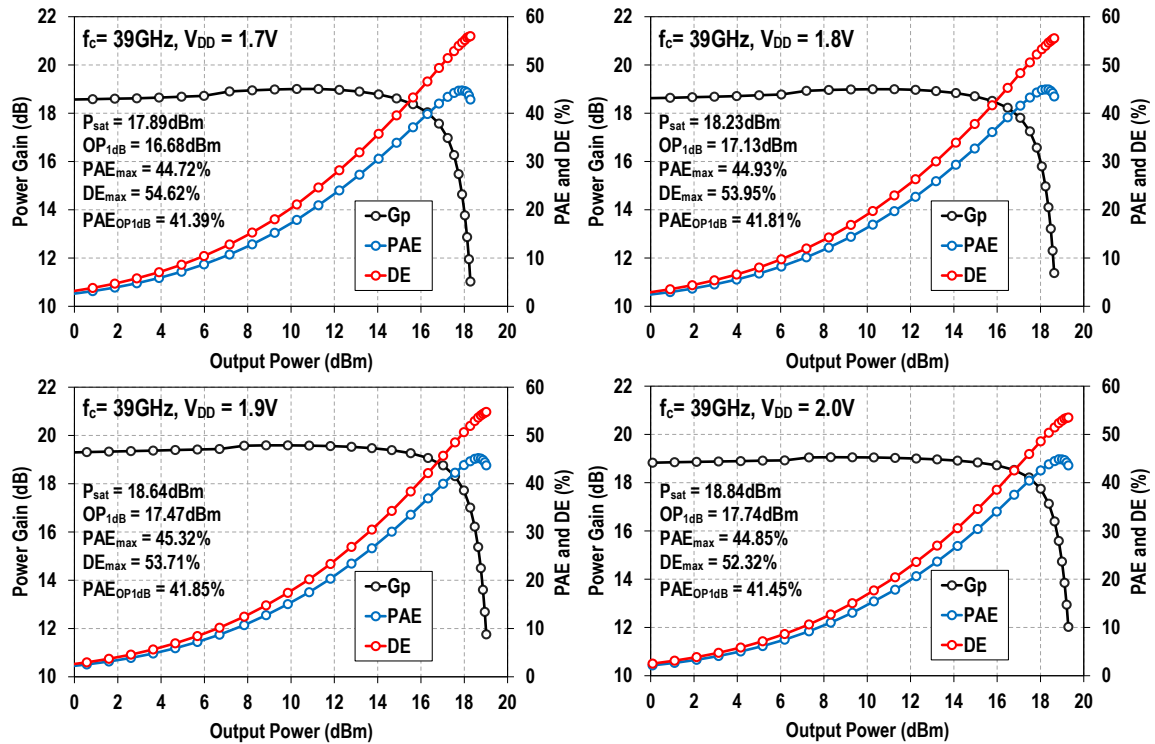


**Figure 6-8 Large signal CW measurement results of the 2-stage dual-drive PA operated at 1.7V, 1.8V, 1.9V, and 2.0V.**

### 6.2.1 Continuous-Wave Measurements

Conventionally, 2-port small-signal S-parameter measurements are performed using a vector network analyzer such as the PNAX vector network analyzer from Keysight (10MHz-67GHz) and GSG probes. Due to equipment availability, Figure 6-7 shows the S-parameter simulation results from 30 to 44GHz. The simulated S<sub>21</sub> is 20.54dB with a 3-

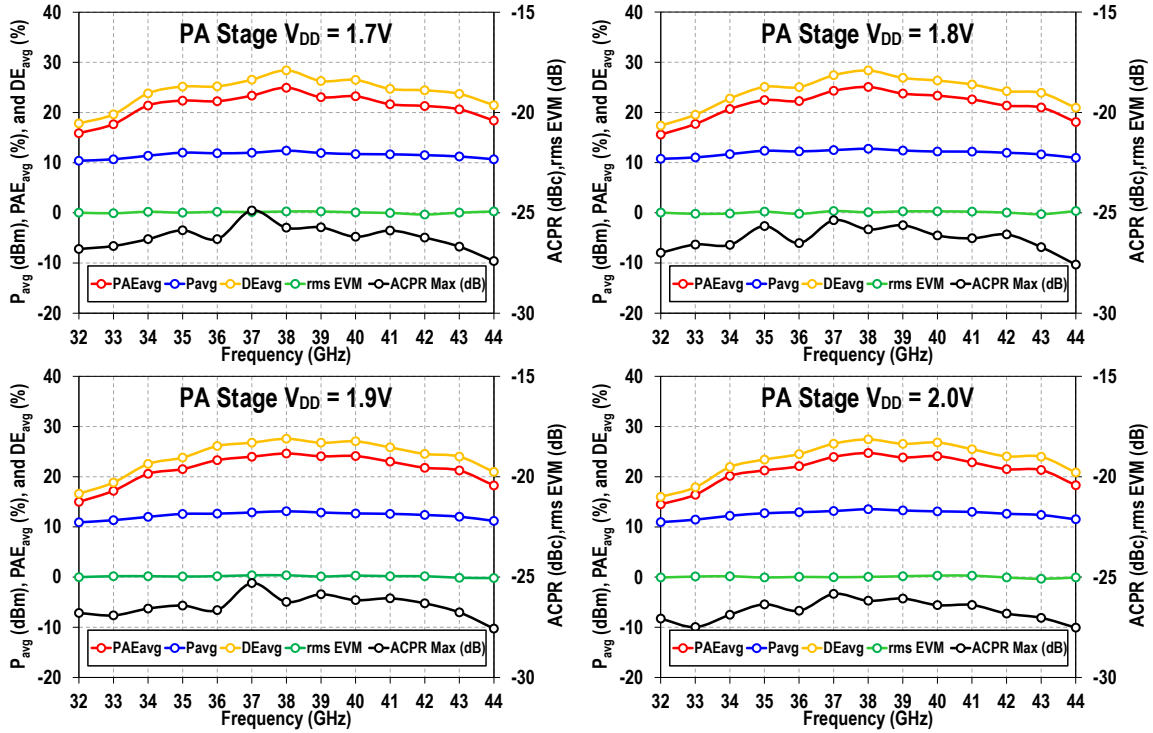
dB bandwidth from 31 to 42GHz. In addition,  $S_{11}$  results show an input matching less than -10dB from 33 to 42GHz.



**Figure 6-9 Large signal CW measurement results of the 2-stage dual-drive PA operated at 1.7V, 1.8V, 1.9V, and 2.0V.**

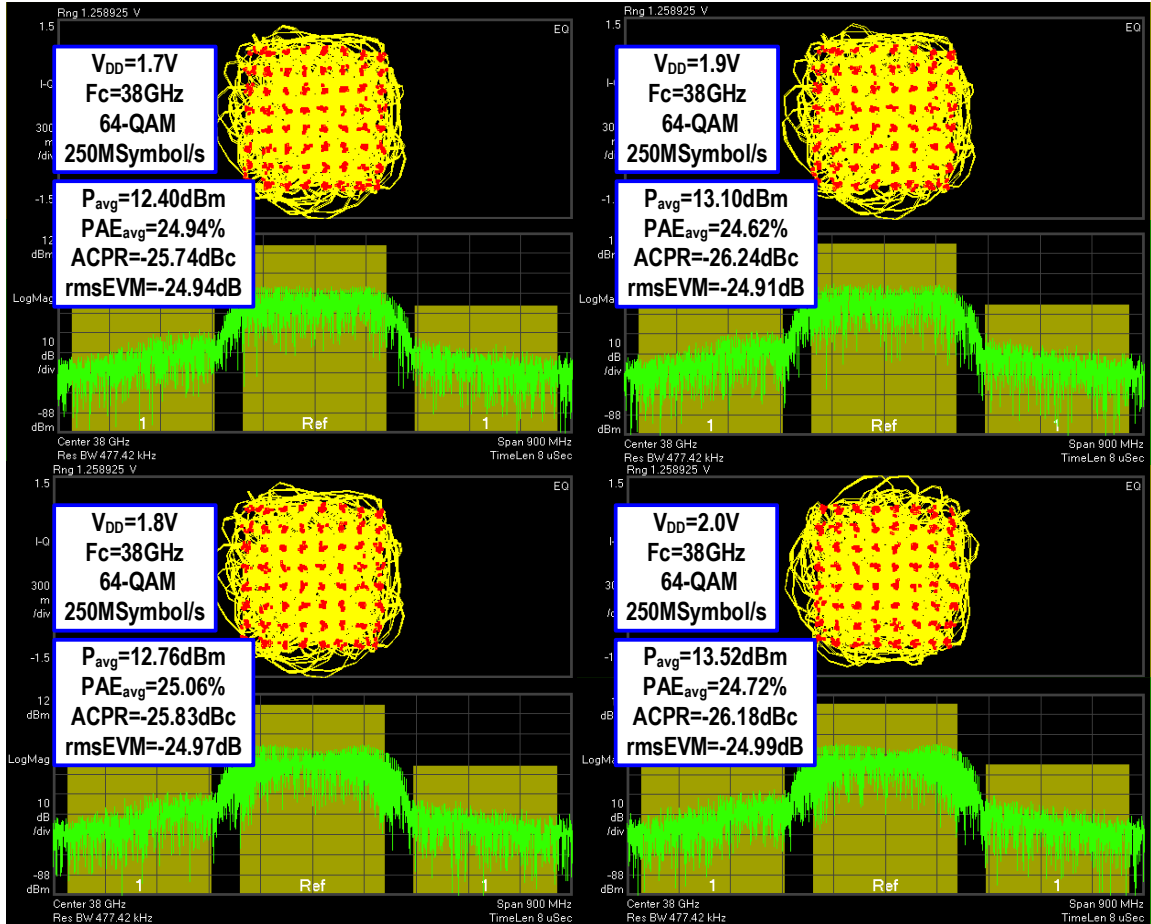
The dual-drive PA is further characterized using large-signal CW measurements (Figure 6-5(a)). These measurements are carried out using an analog signal generator (Keysight EE2267D) to drive the PA and a power meter (Keysight N1914A) and power sensor (Keysight N8488A) connected to the output RF pad through GSG probes to measure the output power. Moreover, measurements were carried out for different supply voltages from 1.7V to 2.0V with 0.1V increments to demonstrate the efficiency enhancements capabilities at lower supply voltages. The summary of the large-signal CW performance from 23-36 GHz is shown in Figure 6-8 and Figure 6-9. In summary, our dual-drive PA achieves a maximum  $OP_{1\text{dB}}$  of 18.02dBm at 38GHz and displays less than 1dB variation from 32 to 41GHz. Also, a maximum PAE of 45.32% and maximum drain efficiency of

53.71% is achieved at 39GHz, which is the highest reported PAE and DE for a 2-stage PA in silicon. The drain efficiency only accounts for the efficiency of the PA core, while the PAE accounts for all stages.



**Figure 6-10 Single-carrier 64-QAM modulation measurement results of the 2-stage dual-drive PA operated at 1.7V, 1.8V, 1.9V, and 2.0V.**

From 33 to 42GHz the PA also maintains a  $PAE_{max}$  larger than 40%. The  $OP_{1dB}$  and  $P_{sat}$  are within 1dB throughout the bandwidth with a maximum PAE at  $OP_{1dB}$  of 41.85% at 39GHz. Moreover, the dual-drive PA is measured under different supply voltages. Figure 6-8 and Figure 6-9 also shows the large-signal CW measurement summary under different supply voltages at 39GHz. Our PA achieves a maximum PAE from 44.72 to 45.31% when varying the supply voltage from 1.7 to 2V, which demonstrates the superior performance of our PA under lower  $V_{DD}$  values for increased reliability.



**Figure 6-11 Single-carrier 64-QAM modulation measurement results of the 2-stage dual-drive PA operated at 1.7V, 1.8V, 1.9V, and 2.0V.**

### 6.2.2 Modulation Measurements

For modulation characterization, we employ a signal source with 5G NR and custom modulation capabilities (Keysight M9383A PXIe Signal Source with 5G NR and Custom Modulation Signal Studio) to drive the input of the PA. The output of the PA is split into two signals using a power divider (Marki Power Divider PD-0165). One of the outputs of the power divider is connected to a signal analyzer (Keysight UXA N9040B) with 5G NR Capabilities. The other output of the power divider was connected to the power sensor to measure the average power.

Figure 6-10 and Figure 6-11 shows the measured modulation results using a single-carrier 64QAM signal (data source: PRBS 29–1) without using any digital predistortion (DPD) from 32 to 44GHz. For all measurements a data rate of 250MSymbols/s was used while maintaining a minimum rmsEVM of -25dB. Linear equalization is performed for every measurement, which does not correct the non-linearity of the PA. Linear equalization only corrects the measurement setup’s linear frequency response and the additional linear impairments introduced when the PA is in place [14]. The highest measured performance for average output power and PAE is 12.76dBm and 25.06% while maintaining a minimum rms EVM of -25dB at 38GHz for a 1.8V supply. In addition, based on our measurement results, the modulation performance variation for different supply voltages is very minor as can be seen in the summary plots (Figure 6-10).

**Table 6-1 Performance summary and comparison to recently reported mm-wave PAs**

	This Work		Huang ISSCC 21	Li TMITT 19	Vigilante JSSCC 18	Wang ISSCC 20					Mannem ISSCC 20
Technology	45nm SOI CMOS		45nm SOI CMOS	45nm SOI CMOS	28nm CMOS	45nm SOI CMOS					45nm SOI CMOS
Architecture	Dual-Drive PA Core		Continuous coupler-Doherty-power-amplifier	Continuous Mode Hybrid Class-F/F <sup>-1</sup>	Transformer-based High Order Network	Compensated Distributed Balun					Coupler-based reconfigurable Series/Parallel Doherty
Supply (V)	1.7	1.9	2	2	0.9	2					2
Gain (dB)	18.5	19.2	14	15.6	20.8	20.5					13.2
Bandwidth(GHz)	32 to 44	32 to 44	26 to 60	55.10%	32.30%	51%					38.5 to 47
Freq (GHz)	39	39	37.5	39	40	24	28	37	39	42	39
Psat (dBm)	17.89	18.64	21.8	18.9	15.9	20	20.4	20	19.1	17.9	20.8
OP1dB (dBm)	16.68	17.47	20*	17.4	11.1	19.6	19.1	18.9	18	15.7	20.2
DE <sub>max</sub> (%)	54.62	53.71	NA	NA	NA	NA	NA	NA	NA	NA	NA
PAE <sub>max</sub> (%)	44.72	45.32	32.5	36	18.4	38.9	45	38.7	38.6	35	33.3
PAE <sub>OP1dB</sub> (%)	41.39	41.85	27*	NA	7.5	38.9	38.9	42.5	37.7	37.3	30.4
Modulation Scheme	64-QAM	64-QAM	64-QAM	34-QAM	64-QAM	5G NR FR2 64-QAM 2-CC OFDM					64-QAM
Freq (GHz)	38	38	40	39	34	24	24	28	37	39	42
Data Rate (Gb/s)	0.25	0.25	3	3	1.5	800 MHz	800 MHz	800 MHz	800 MHz	800 MHz	0.6
EVM (dB)	-25	-24.91	-25.2	-28.1	-25	-25.1	-25.1	-25.1	-25.1	-25.1	-23.8
ACPR (dB)	-25.74	-26.24	-27.2	-28	-32.1	-25.2	-25.6	-27.9	-26.1	-26.4	-36.5
P <sub>avg</sub>	12.4	13.1	12.6	11	10.1	10.9	11.3	10.2	10.2	8.4	13.8
PAE <sub>avg</sub>	24.94	24.62	15.2	10.2	5.8	14.2	16.6	13.6	13.4	10.3	19
Area (mm <sup>2</sup> )	0.18mm <sup>2</sup> (Core Area)	0.18mm <sup>2</sup> (Core Area)	0.62mm <sup>2</sup> (Core Area)	0.21mm <sup>2</sup> (Core Area)	0.16mm <sup>2</sup> (Core Size)	1.35					2.86

Our dual-drive proof-of-concept performance summary and comparison with recently reported state-of-the-art mm-Wave PAs is presented in Table 6-1. The dual-drive PA achieves the highest reported PAE and Drain Efficiency for a 2-stage PA in silicon while maintaining a reasonable bandwidth of operation. This performance is achieved even at a lower supply voltage of 1.7V. Furthermore, it achieves the highest reported average PAE for a 64 QAM modulated signal and a data rate of 250MSym/s. In addition, we were able to demonstrate state-of-the-art modulation results for 5G NR signals. Amongst the

reported mm-Wave PAs, our dual-drive PA presents a new topology and region of operation and achieves the highest efficiency ever reported at 38GHz.

### **6.3 Conclusion**

This article presents new dual-drive power amplifier topology for mm-Wave applications. The dual-drive PA exploits the 3-terminal device nature of the transistor by driving the gate and the source at the same time with an out-of-phase signal. In doing so, the drain efficiency becomes proportional to the driving strength of the source terminal. The dual-drive topology increases the overall maximum PAE of the PA, eases the interstate matching network requirements, and mitigates reliability issues since the PA can be used with lower supply voltages. As a proof-of-concept, a dual-drive 2-stage power amplifier is implemented in the GlobalFoundries 45nm CMOS SOI process occupying an area of 1.04mm×1.28mm and achieves a  $PAE_{max}$  of 45.32% and  $DE_{max}$  of 53.71% at 39GHz at 1.8V supply. This work also achieves the highest average PAE and DE under complex modulation among mm-Wave 2-stage PAs. Our new dual-drive prototype is ideal for highly reliable wireless communications the employ complex modulation schemes.

## CHAPTER 7. CONCLUSIONS

### 7.1 Research Summary

The main challenge for future generation networks and systems operating beyond mm-Wave frequencies is power efficiency. Electronic devices targeted to 5G/6G and beyond wireless networks employ phased array transmitter architectures, which limits the overall system energy efficiency, thermal performance, and data rate. Moreover, multipath propagation and higher path losses makes extremely challenging to transmit signals efficiently at mm-Wave and sub-THz frequencies. In this dissertation, we presented new on-chip TRX/PA design approaches and circuit architectures to address challenges regarding the energy efficiency, linearity, and bandwidth of future 5G/6G enabled systems.

First, in Chapter 2 we propose a design method for cascading multiple rat-race hybrid couplers that increases the bandwidth of operation. Our high-order rat-race architecture reduces the amplitude mismatch and cancels the phase imbalance at the output ports. In addition, we present a 2<sup>nd</sup>-order proof-of-concept on-chip implementation that operates from 22.6 to 43.4GHz using a GlobalFoundries 45nm CMOS SOI platform. Our measurement results demonstrate that our proposed cascaded rat-race architecture achieves a less than 5° phase mismatch, less than 1dB magnitude mismatch, better than -10dB input/output matching, and better than -20dB isolation throughout the entire bandwidth.

In Chapter 3, we explore further methods of increasing the operational bandwidth of other TRX building blocks. We presented on on-chip cartesian vector-modulator integrated with input/output Marchand balun, driver, and a 2-stage power amplifier. Our

proposed proof-of-concept achieves  $360^\circ$  full-span phase interpolation while providing high output power capabilities covering a frequency range from 40 to 60GHz.

In Chapter 4, we present low-power sub-THz TRX integrated with on-chip patch antenna array supporting 10Mb/s OOK chip-to-chip communication at a chip-to-chip distance of 70cm and without employing a silicon lens. The sub-THz TRX presented in this chapter is based on two coupled differential Colpitts oscillator. The two oscillators can be reconfigured as a sub-THz power source (TX mode) and as a super-regenerative receiver (RX mode). In addition, we present an adaptive metal fill placement methodology for the design of the on-chip patch antenna that ensures accurate modeling of the antenna impedance and gain, which avoids the need for bulky silicon lenses. We demonstrate a proof-of-concept in the GlobalFoundries 45nm CMOS SOI process and occupies a silicon area of  $2.1\text{mm}\times 2.1\text{mm}$ . Our prototype achieves a maximum EIRP of 8.52dBm with a DC-to-EIRP efficiency of 30.7% with no silicon lens.

The last part of this dissertation, Chapter 5, we present a new power amplifier topology that we call the dual-drive PA. In our new dual-drive PA topology, we drive the gate and the source of the transistor simultaneously with an out-of-phase signal. We demonstrate in our theoretical analysis of the dual-drive PA that the drain efficiency becomes proportional to the driving strength of the source terminal. Moreover, the dual-drive topology increases the overall maximum PAE of the PA, eases the interstate matching network requirements, and mitigates reliability issues since the PA can be used with lower supply voltages. We implement a proof-of-concept, 2-stage dual-drive power amplifier in the GlobalFoundries 45nm CMOS SOI process. Our prototype occupies an area of  $1.3\text{mm}\times 1.5\text{mm}$ , achieves a  $\text{PAE}_{\text{max}}$  of 45.32%,  $\text{DE}_{\text{max}}$  of 53.71% at 39GHz at 1.9V supply. This work also achieves the highest average PAE and DE under complex modulation among mm-Wave 2-stage PAs.

## 7.2 Key Research Contributions

1. Self-similar high-order rat-race hybrid coupler architecture supporting wideband operation.
2. On-chip patch antenna array design methodology which consists of a new adaptive metal-fill placement approach.
3. Integrated low-loss Marchand balun-based coupling network as a coupling mechanism for fundamental power oscillators.
4. 150GHz regenerative low power miniature 2-way radio integrated with on-chip antennas. Our proof-of-concept prototype achieves the highest efficiency reported of all the silicon-based sub-THz transceivers (TRX) in the 150GHz range.
5. New dual-drive PA topology. A prototype of our dual-drive PA achieves the highest reported PAE and DE for a 2-stage PA in silicon at mm-Wave frequencies.

## 7.3 Future Work

As the world moves toward more connected devices, users, and data rates, there is a massive need for improving the energy efficiency at higher frequencies of transmitters, more specifically, large-signal generator circuits such as power amplifiers and power oscillators. This subsection presents relevant future work that could be carried out to fully implement the ideas presented here in commercial applications.

First, to evaluate the device operation conditions/limits and costs/tradeoffs between commercially available semiconductor platforms, namely bulk silicon (Si), silicon-on-

insulator (SOI), gallium arsenide (GaAs), and gallium nitride (GaN), to understand which technology platform is most amenable and maximizes the superior value proposition of the dual-drive power amplifier over existing topologies on similar semiconductor platforms. For example, GaN offers exceptional power density, efficiency, and improved radiation-hardening tolerance, making it an ideal candidate for future space applications. Additional high power/voltage semiconductor manufacturing processes should be explored, such as Gallium-Arsenide and LDMOS/EDMOS on silicon.

Furthermore, performance characteristics degradation due to packaging materials of the dual-drive power amplifier should be evaluated and appropriate design changes should also be explored to compensate for packaging parasitics and losses. In addition, adequate chip packaging materials should be explored to ensure hermetically sealed enclosures and radiation-hardened robustness for LEO space applications. There are considerable technical efforts that are needed to bring this technology to market.

#### **7.4 Research Publications**

1. D. Munzer, N. S. Mannem, **E. F. Garay** and H. Wang, "Single-Ended Quadrature Coupler-Based VSWR Resilient Joint mmWave True Power Detector and Impedance Sensor," in IEEE Transactions on Microwave Theory and Techniques.
2. **E. F. Garay**, D. J. Munzer and H. Wang, "A 150 GHz Lens-Free Large FoV Regenerative 2 x 2 Transceiver Array With 31% DC-to-EIRP Efficiency and -70 dBm Sensitivity for a 70 cm Bidirectional Peer-to-Peer Link," in IEEE Journal of Solid-State Circuits.

3. A. Mirbeik-Sabzevari, S. Li, **E. Garay**, H. Nguyen, H. Wang and N. Tavassolian, "W-Band Micromachined Antipodal Vivaldi Antenna Using SIW and CPW Structures," in IEEE Transactions on Antennas and Propagation, vol. 66, no. 11, pp. 6352-6357, Nov. 2018.
4. A. Mirbeik-Sabzevari, S. Li, **E. Garay**, H. Nguyen, H. Wang and N. Tavassolian, "Synthetic UltraHigh-Resolution Millimeter-Wave Imaging for Skin Cancer Detection," in IEEE Transactions on Biomedical Engineering.
5. **E. F. Garay** and R. Bashirullah, "Biofluid Activated Microbattery for Disposable Microsystems," in Journal of Microelectromechanical Systems, vol. 24, no. 1, pp. 70-79, Feb. 2015.
- D. J. Munzer, N. S. Mannem, **E. Garay** and H. Wang, "A Broadband Mm-Wave VSWR-Resilient Joint True-Power Detector and Impedance Sensor Supporting Single-Ended Antenna Interfaces," 2022 IEEE International Solid- State Circuits Conference (ISSCC), 2022, pp. 1-3.
6. **E. Garay**, D. Munzer, and H. Wang, "A Mm-Wave Power Amplifier for 5G Communication Using a Dual-Drive Topology Exhibiting a Maximum PAE of 50% and Maximum DE of 60% at 30GHz" accepted and to appear in IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, Feb. 2021.
7. **E. Garay**, M. Huang, and H. Wang, "A Cascaded Self-Similar Rat-Race Hybrid Coupler Architecture and its Compact Fully Integrated Ka-band Implementation," 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, PA, 2018, pp. 79-82.

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