UNDERSTANDING AND ADVANCING SEMICONDUCTOR NANOWIRE SYNTHESIS

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UNDERSTANDING AND ADVANCING SEMICONDUCTOR NANOWIRE SYNTHESIS

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LIST OF SYMBOLS AND ABBREVIATIONS

NW	Nanowire
NWs	Nanowires
VLS	Vapor-liquid-solid
VL	Vapor-liquid
LS	Liquid-solid
VS	Vapor-solid
SLV	Solid-liquid-vapor
CNTs	Carbon nanotubes
FETs	Field effect transistors
LSPR	Localized surface plasmon resonance
TEM	Transmission electron microscope
SEM	Scanning electron microscope
AFM	Atomic force microscope
RIE	Reactive ion etching
EBL	Electron beam lithography
MaCE	Metal-assisted chemical etching
SLS	Solution-liquid-solid
SFLL	Supercritical fluid-liquid-liquid
SFSS	Supercritical fluid-solid-solid
SVG	Solvent vapor growth
VSS	Vapor-solid-solid
UHV	Ultra-high vacuum
CVD	Chemical vapor deposition

TMT	Tetramethyltin
TMSi	Trimethylsilane
EELS	Electron energy loss spectroscopy

SUMMARY

Semiconductor nanowires (NWs) have become an indispensable nanoscale platform for a broad range of electronic, photonic, and energy conversion applications. Among all growth technique, the bottom-up vapor-liquid-solid (VLS) nanowire (NW) fabrication technique offers the ability to encode material functionalities along the length of a NW in a user programmable manner. A robust control of VLS growth requires understanding of multiple heterogeneous chemical processes: (1) transportation of semiconductor molecules/atoms from vapor to liquid droplets or vice versa at the vapor-liquid (VL) interface, (2) crystallization and dissolution of semiconductor atoms at the liquid-solid (LS) interface, and (3) the conformal deposition of precursor molecules onto the nanowire sidewall at the vapor-solid (VS) interface. However, the ability to rationally engineer NWs for advanced semiconductor devices is critically impaired by limited understanding of these chemical processes at the heterogeneous interfaces.

In this thesis, we first focus on the heterogeneous chemical reactions at the VL interface. In Chapter 3, we demonstrate a novel solid-liquid-vapor (SLV) process to remove the semiconductor atoms from the NW, which has been theoretically discussed for decades with no definitive evidence. We use a dicarbonyl species, 2,3-butanedione, to *in-situ* etch <111> grown Ge nanowires selectively in the growth direction with the help of a metal catalyst uniformly across a large area.

In Chapter 4, we connect the SLV etching at the VL interface to the LS interface. We propose that this top-down NW etching process operates by dissolving Ge atoms from the NW crystal into the eutectic catalyst through the LS interface. Subsequently, a volatile etch product at the VL interface removes Ge atoms in the eutectic catalyst. Also, we proposed and substantiated a kinetic model to describe this selective nanowire etching removal process. The kinetic model is validated by the experimental data and can be used as a theoretical tool to predict the etch rate for a wide range of experimental conditions.

In Chapter 5, we leverage the surface chemistry knowledge gained from the previous projects to engineer defect-free Si/Ge nanowire heterostructures. We recognize that the monolayer of hydrogen atoms at the VS interface may be critical for stable NW growth. Often, imperfections in NW heterostructures synthesis potentially come from the growth instability by losing the hydrogen layer at the VS interface when switching to different precursor gasses at different temperatures. Here, we use trisilane – a highly reactive precursor for Si – to maintain monolayer hydrogen coverage at the VS interface while still supplying enough semiconductor atoms for Si segment growth at low temperature. Low-temperature environment maintains the hydrogen layer at the VS interface. Thus, an array of Si/Ge heterostructure NWs is synthesized without defects at the hetero-junction. Finally, we leverage the technique to form a Si nano-disk embed in two Ge segments. The apprehension of the heterogeneous chemical processes derived over the course of our studies has set the stage for the robust VLS NW synthesis and enabled future development of NW applications.

CHAPTER 1. INTRODUCTION & BACKGROUND

1.1 Overview

One-dimensional nanomaterial systems have received considerable attention in the past two decades. That primary research focuses on the 1D-nanostructure is triggered perhaps by the facile synthesis first of carbon nanotubes (CNTs), and later by graphene.[1] Since the 1990s, CNTs have been recognized as both excellent prototypic systems and as potential building blocks for the next generation of electronic nanodevices. Nevertheless, further development of CNTs in manufacturing applications is hindered by technical difficulties such as the production of CNTs with uniform properties because actual properties strongly depend on their symmetry, the electronic structure of graphene, and variations in exact structural folding angle.[2] 1D-Nanowires (NWs), on the other hand, can be synthesized with excellent uniformity, as opposed to CNTs, and thus may serve as an attractive alternative in probing novel properties at the nanoscale. Sine their initial synthesis and description, 1D-NWs have been continuously adopted by others for various applications including field effect transistors (FETs) [1-3], lithium-ion batteries [4-6], computing devices [7-9], photovoltaics [10-12], lasers [13-15], chemical and biological sensors and drug delivery [16-18], and nanoelectromechanical systems [19-21].

The technological and commercial potential of NWs has shifted from minimizing device features to discovery and implementation of emerging applications. These applications are derived from and made possible by modern NW synthesis advancement. For example, radial NW heterostructures control carrier transfer direction due to a band offset at abrupt interfaces.[24] Kinked NWs with a p-n junction as a sensor contacts with biological systems can be easily fabricated more intimately, enabling ultra-high sensitivity and reproducibility.[19,25] Intentional defect introduction and diameter modulation in NWs alter thermal conductivity due to changes in ordered crystal structure and subsequently the number of scattering centers along the primary NW growth direction.[26-27] However, these revolutionary applications, derived from novel properties, may not be applicable for large-scale manufacturing because a complete understanding of uniform and reproducible NW synthesis is currently lacking.

Understanding of fundamental NW synthesis is the key to promoting NW applications through better understanding of the structure-property-application relationship. New knowledge in synthesis can advance our capability of uniformly manipulating NW structures. Enhanced NW uniformity directly impacts product yield - and thus costs control- in manufacturing. On the other hand, structural modulation techniques can allow one to observe novel properties, leading toward more innovative NW applications. Thus, the background information provided in Chapter 1 will revisit current NW novel properties, methodologies, and applications, as well as synthesis capability for each type of current structural modulations. During the discussion of synthesis capability, both top-down and bottom-up methods are introduced with a focus on the group IV-NW formation, especially via the vapor–liquid–solid (VLS) mechanism. The final portion of Chapter 1 discusses our current synthesis challenges, and promotes the urgency in understanding functional and reproducible NW synthesis.

1.2 Semiconductor Nanowire Properties and Applications

1.2.1 Electrical Properties and Electronic Applications

If cells are the building blocks of life, transistors are certainly the building blocks of digital devices. Transistors at the nanoscale could use semiconducting NWs as potential alternatives for post-Moore electronics. For instance, single-crystal doped Si NWs have been successfully integrated into FETs.[28-31] The doped NWs are deposited on an insulating substrate surface. Subsequently, at both ends of the NWs, metal contacts are deposited before configuring either a bottom or top gate electrode. Performance from the doped NW-based FET exceeds that of planar Si devices after thermal annealing and oxide passivation.[3] Also, Ge NWs inherently have higher intrinsic electron and hole mobility for superior electrical performance compared to their planar counterparts.[32-33] To further improve device performance, core-shell Ge/Si doped NWs can become a conductive channel for FETs.[34] The energy band offset at the heterojunction generates an internal field to redistribute charge-carriers, thus enabling higher mobility devices. However, the dopant impurities in NWs also can serve as scattering centers to simultaneously retard charge transport.

Therefore, intrinsic Si [35] and core-shell Ge/Si NWs [36-38] remain as the popular choices by possessing additional benefits. For example, core-shell Ge/Si heterostructure FETs could even detect a single charge transport because of charge accumulation at the hetero-interface.[37] Improved performances can be achieved by using high-κ dielectrics in a top-gate geometry because it lowers electrical resistance between the NWs and electrode contacts.[36, 38] Resistance can be further reduced using non-metal contacts such as a metal silicide [39], doped thin film [40] and conducting oxide contacts [41]. Moreover, NW-based FETs can be assembled to generate memory cells [42], logic gate [9, 43], switches [44], complementary circuits [45-47], programmable circuits [11], and three-dimensional nanoelectric networks [48]. Table 1 shows the performance from various NW-based FETs.

Table1.1. Performance of Different Types of NW Based FETs

FET Type	*Impurity Dopant*	*Transconductance (nS)*	*Charge Mobility ($cm^2V^{-1}s^{-1}$)*
n-type Si NW[31]	phosphine	900 ±100 (peak: 1500)	95 (peak: 270)
p-type Si NW[49]	diborane	45-800 (peak: 2000)	30-560 (peak: 1350)
p- and n-type Ge NW[32]	phosphine and diborane	2800 (peak: 4900)	100 (peak: 70)
p-type Ge NW[33]	diborane	2100	600
Undoped Si NW[50]	None	\	650 (inversion) 330 (accumulation)
Undoped Ge/Si NW[38]	None	2600	730
Undoped Ge/Si NW[36]	None	7800-9100	\

1.2.2 Optical Properties and Photonic Applications

In the 21st century, humankind faces a significant challenge to stabilize the carbon dioxide–induced component of climate change. Arguably, the most efficient way to reduce carbon dioxide emissions while retaining economic growth is to replace fossil-based electricity with sustainable energy sources such as solar energy.[51-52] The energy from the sun striking the Earth in 1 hour generates more than all the energy consumed globally in one year. However, high efficiency solar cells come with a high price tag, preventing it from becoming a genuinely comprehensive and primary power source.[53] On the other hand, NW-based solar cells offer advantages such as broadband anti-reflection [13, 54-57], excellent light trapping [58-60], flexible band gap tunability [61-64], facile strain relaxation [65-68], increased defect tolerance [69-70], and easy integration with low-cost substrates [22-25]. The unique NW geometry relaxes fabrication requirements necessary to approach maximum power conversion efficiency, potentially representing opportunities for a cost-effective energy source.

Notably, IV-NW can further reduce capital costs by being compatible with the existing Si-based microelectronic industry. They have been demonstrated as a key component for a solar cell.[12,14,55,58, 74-77] For example, coaxial-doped Si-NW solar cells generate a maximum power output up to 200 pW as shown in Figure 1.1a [12], which sufficiently powers nanosystems such as the nano-circuit system shown in Figure 1.1b.[78-80] These IV-NW based solar cells could also couple with other chemical or material systems such as organic and polymer molecules [81-83], and nanoparticles [84-85] to improve light absorption efficiency. More interestingly, the NW platform can induce localized surface plasmon resonance (LSPR) via heavy doping [86-87], which could further enhance light absorption[26-27] and light trapping [90-91].

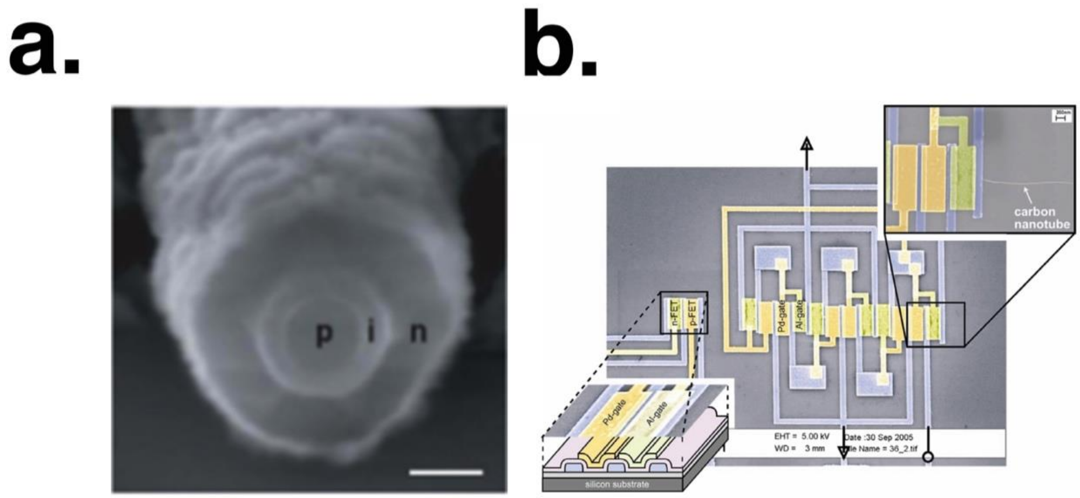

Figure 1.1. (a) A representative SEM image of coaxial silicon nanowire solar cell as the nanoelectronic power sources. Scale bar, 50 nm. Adapted from 12 and reprinted with permission. (b) A SEM image of a five-stage carbon nanotube ring oscillator circuit. Adapted from 78 and reprinted with permission.

In photovoltaics, essential steps required for converting light to electricity involve photon absorption, exciton formation, and charge separation and collection.[92] Each step is associated with multiple sources of energy loss; however, these losses can effectively be minimized by controlling NW morphologies to potentially achieve higher power conversion efficiency. In photon absorption, high reflection and transmission are the primary mechanisms for these losses because not all of the energy from light contributes to electron excitation. Fortunately, the physical shape of NWs naturally suppresses reflection and transmission, traps, and/or light concentration in a broadband, angle independent fashion.[11, 25, 28-38] Reflection and transmission can be dramatically modified at certain wavelengths by the length and diameter of the NWs. [11, 28-33] In addition, superior antireflective characteristics from the mid-infrared (IR) to Thz frequency regions are observed from a tapered NW structure, acting as a nanoantenna with a gradual change in refractive index across the NW and air interface.[56-57]

On the other hand, the light could be trapped more efficiently via the resonant effect, which is affected by the NW cross section geometry (cylindrical vs. hexagonal vs. rectangular), as computationally predicted by the Lorenz–Mie theory[97]; an experimental evidence confirms this prediction via photocurrent measurements[93]. In the exciton formation, the excited electrons above the conduction band edge could be stabilized to a lower energy state in the valence band via either direct or indirect carrier relaxation by emitting or dissipating energy as light or heat with the assistance of phonons. Therefore, increasing the band gap via multiple methods such as quantum confinement[99] and strain introduction[100-101] in NWs could minimize this exciton loss.

In charge separation and collection, electrons and holes first must be separated and then diffused to their respective electrodes, and subsequently be extracted for useful work. However, in the charge diffusion process, electrons can lose energy via bulk recombination before carrier collection. To avoid substantial bulk recombination, NW systems with an axial and coaxial p–i–n junction must provide a smaller carrier collection distance[10, 12, 39-40], as compared to its planar counterpart. Particularly, coaxial core-shell NWs separate the carriers oppositely in the radial direction, making the carrier collection distance smaller or comparable to the carrier diffusion length.[10, 39-40] Furthermore, by applying strains in different regions along a NW, an induced spatial elongation between the highest occupied molecular orbitals and the lowest unoccupied molecular orbitals form a type-II homojunction to facilitate the charge separation.[41-43]

1.2.3 Mechanical Properties and Sensing Applications

Semiconducting NW-based FETs are not only recognized as a building block for next generation nanoelectronics, but also for next generation ultrasensitive nanosensors with a direct sensing and label-free capability. The NW-FET–configured sensors use source and drain terminals to emit and collect charges, as shown in Figure 1.2a.[106] They modulate electric conductance by an individual analyte binding. The analyte acts as an external voltage source via the gate terminal to effectively modulate the carrier transport rate. The binding event occurs by forming a selective linkage between the analyte and groups of NW receptors at the surface of a NW "bulk" channel. Since the analytes, especially in (bio)chemical systems, have comparable sizes to the NW, the binding connection naturally forms a tighter junction as compared to 2-D planar sensors, enabling ultra-high sensitivity without the help of fluorescent labeling dyes. In addition, the small junction gap allows for detection with minimal local perturbation, converting it into a charge with electrical conductivity. This exquisite sensitivity facilitates fundamental (bio)molecular studies, which accelerates the development of disease diagnosis and drug discovery. The ultrasensitivity and low detection limits have been demonstrated with hydrogen and metal ions[16, 44-45], nucleic acids[46-60], tissue[124-125], proteins[16, 61-73], cells[74-78] and even a single virus[143]. Surprisingly, the NW-sensors can be fabricated on non-semiconductor substrates such as flexible plastic substrates[144-146], and can even be liberated from a substrate for detection, as shown in Figure 1.2b[25]. NW- sensors have rapidly moved into an exciting stage of development over the past five years and become the subject of several comprehensive reviews.[147-150]

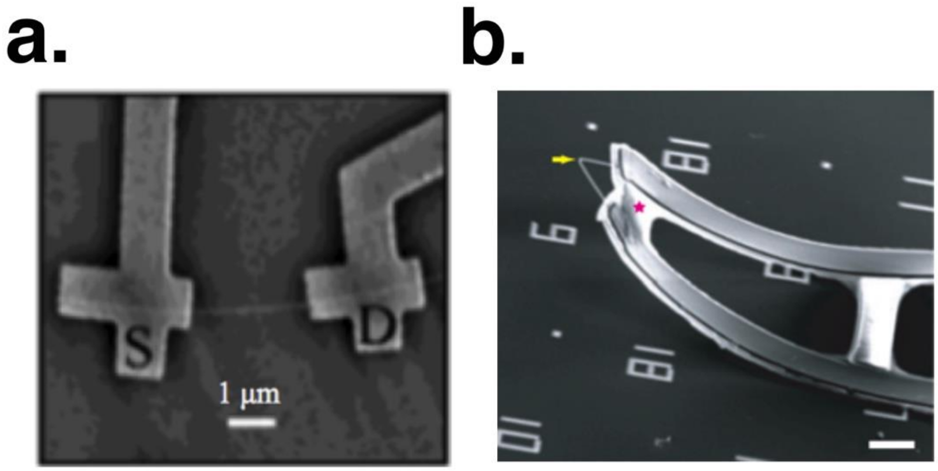

Figure 1.2. (a) A representative SEM image of silicon nanowire device with source and drain terminals. Scale bar, 1 μm. Adapted from 106 and reprinted with permission. (b) A representative of SEM image of an as-made device. The yellow arrow and pink star mark the nanoscale FET and SU-8. Scale bar, 5 μm. Adapted from 25 and reprinted with permission.

To fabricate NW devices such as FETs and (bio) chemical sensors, NWs can be expected to experience unavoidable induced strains and external stresses resulting from fabrication processes at multiple temperatures and pressures. These strains and stresses serve as sources of crack formation and propagation and related material property alternations such as changes to charge mobility. Therefore, the operation and reliability of these NW-based devices strongly depends on mechanical properties such as elasticity (the ability to absorb external forces), and strength (the ability to resist forces without deformation). These mechanical properties have deviated from those of their bulk counterparts due to their high surface-to-volume ratio.

Experimentally, these mechanical properties are extracted mainly via resonance techniques using transmission and/or scanning electron microscopes (TEM; SEM)[151-154], bending based techniques[155-159], or nano-indentation techniques using an atomic force microscope (AFM) in either TEM/SEM[160-161] under various loading and/or preparation methods. Computationally, these mechanical properties can be quantified mostly via first-principles[162-166], atomic simulations[167-171], or empirical atomistic potentials and continuum methods[79-83] with various initial NW configurations. Not surprisingly, the experimental data show significant discrepancy with these simulation results; however, the mechanical properties can still form a general connection with the NW structure or material components.

For elasticity, the elastic modulus (ε), which is defined as the work done on NWs per unit volume, becomes smaller as the diameter of IV NWs diameter decreases.[80-81, 84-85] The ε also shows strong crystallographic orientation dependence because the NW growth in different orientations is confined by cross sections with unique sidewall facets.[165, 173] Each unique sidewall facet poses various numbers of surface bonds with incompatible binding energy to give different degrees of their contributions to the overall mechanical properties.[163] Additionally, the concentration of a component in the NW could alter ε; for example, the ε of Si_xGe_{1-x} NWs goes down as the Ge content increases.[176] For strength, the fracture strength, defined as the maximum strength applied to NWs before breaking, monotonically increases as the diameter of the NWs increases. The fracture strength has both the same orientation and component dependence for the same reasons as discussed above.[176] Distinctively, NWs with defects or twin planes significantly lower the fracture strength, but are relatively less sensitive to ε, which could potentially cause discrepancies seen between simulations and experimental results.[171, 177]

1.3 Semiconductor Nanowire Synthesis: Top-down vs. Bottom-up

1.3.1 Top-down: Reactive Ion Etching

Taking advantage of existing Si-based manufacturing capability, top-down synthetic methods such as reactive ion etching (RIE) can fabricate a large area of highly uniform NWs. RIE includes two steps: rapid plasma etching, and chemical passivation.[86-97] For plasma etching, the fluorine-based plasma generated from gases (e.g. SF_6) removes semiconductor materials (e.g., Si) to carve isotropic structures. To prevent lateral etching, a chemical passivating layer such as SiO_2 must be used to protect the NW sidewall. It can be deposited onto the sidewall either by thermal treatment[92, 96] or chemical deposition[86, 88, 97]. This sequence of alternating steps can be optimized through control parameters such as pressure, RF-bias voltage, and plasma-gas ratio to further increase the resulting aspect ratio.[181, 187] However, the lateral feature size is also controlled by the size of the etching-resistant mask before the RIE process. In order to fabricate NWs, the nanoscale mask is defined by expensive photolithographic techniques such as electron beam lithography (EBL).[180, 184] As nanofabrication techniques evolve, the nanoscale mask can also be fabricated by low-cost common techniques such as nanosphere lithography[96, 98-100], diblock copolymer lithography[101-102], and nanoparticle self-assembly[94, 102]. A study has demonstrated that RIE can fabricate Si NWs of ~60 nm in diameter.[186] Nevertheless, the etch rate is significantly reduced as the aspect ratio increases due to the bottling effect, putting a limit on NW length.[195] High-density plasma, on the other hand, induces ion damage to the sidewall.[196-198] The induced damage creates additional surface states, increasing the non-radiative recombination rates while lowering carrier mobility. Additionally, isotropic etching steps often undercut the NW sidewall, creating unintentional but unavoidable diameter modulation or tapering.[86-93, 97].

1.3.2 Top-down: Metal-assisted Chemical Etching

In contrast to RIE, metal-assisted chemical etching (MaCE) alternatively offers a low-cost and straightforward synthetic method at low temperatures for high-aspect-ratio NWs. In MaCE, a semiconductor substrate (e.g., Si) is first covered by a noble metal such as Au, Pt, or Ag. Subsequently, the metal-covered substrate is immersed into an etchant-oxidizer mixed solution, inducing local oxidation-reduction reactions. The noble metal acts as a cathode to catalyze the reduction reaction of the oxidizer (e.g., H_2O_2), producing holes locally. The holes are then injected into the adjacent semiconductor substrate to activate the oxidation reaction. The oxidized semiconductor surface (e.g., SiO_2) layer is later etched by the etchant (e.g., HF). More discussions about the MaCE mechanisms can be found in other reviews.[199-200] As an example, Figure 1.3a shows a Si array produced via MaCE.[201] The resultant NW structures can be controlled via experimental parameters such as volumetric ratio of etchant and oxidizer, temperature, etch time, amount of noble metal, and even noble metal or oxidizer choices.[201-208] The noble metal can be deposited on the semiconductor substrate via various methods such as thermal evaporation, electron beam evaporation, sputtering, or electroless deposition.[103-109] With template methods such as an anodic aluminum oxide membrane, high-density Si NWs can be formed with 8 nm in diameter. However, similarly to the RIE, the MaCE often introduces unavoidable rough NW sidewalls.[106, 109-111] Additionally, the NW growth direction frequently cannot be modulated during MaCE because the etch direction depends on the crystallographic orientation of a semiconductor substrate.

1.3.3 Bottom-up: Solution Phase Synthesis

Solution-phase NW synthesis has exploited various solvents via a metal catalyst in different temperature and pressure regimes; it has been considered a low-cost, high-throughput method to grow NWs. The various solution-phase techniques can be separated into four categories: Solution-Liquid-Solid (SLS), Supercritical Fluid-Liquid-Liquid (SFLL) or Supercritical Fluid-Solid-Solid (SFSS), and Solvent Vapor Growth (SVG); the differences among them are primarily in growth medium. This topic is explored in more depth (e.g. growth conditions and catalyst choices) in another review.[213] For SLS growth, high temperatures are required to nucleate Si or Ge NW formation due to their high thermal stability. Thus, SLS growth uses high boiling point solvents such as squalane and squalene.[214-217] Additionally, SLS synthesis has been also demonstrated in a continuous flow system.[218] To relax solvent restrictions, high-pressurized supercritical fluids such as benzene, hexane, and toluene can be used to synthesize Si and Ge NWs at low temperatures.[219-223] The SFLL and SFSS techniques depend on only the thermodynamic phase of the metal catalyst during growth. A SFLL growth technique has been used by

Holmes et al. to synthesize small diameter Si NWs (4-5 nm), as shown in Figure 1.3b.[220] Moreover, in contrast to the SFLL/SLSS growth, the SVG method synthesizes Si, Ge and Si/Ge heterostructure NWs in the vapor phase of a glass reactor.[224-226] Thus, NW formation in the vapor phase can incorporate different substrates during growth. Nevertheless, solution-phase synthesis faces challenges in controlling uniform crystal growth direction, defect introduction, doping incorporation, and compositional modulation during growth.

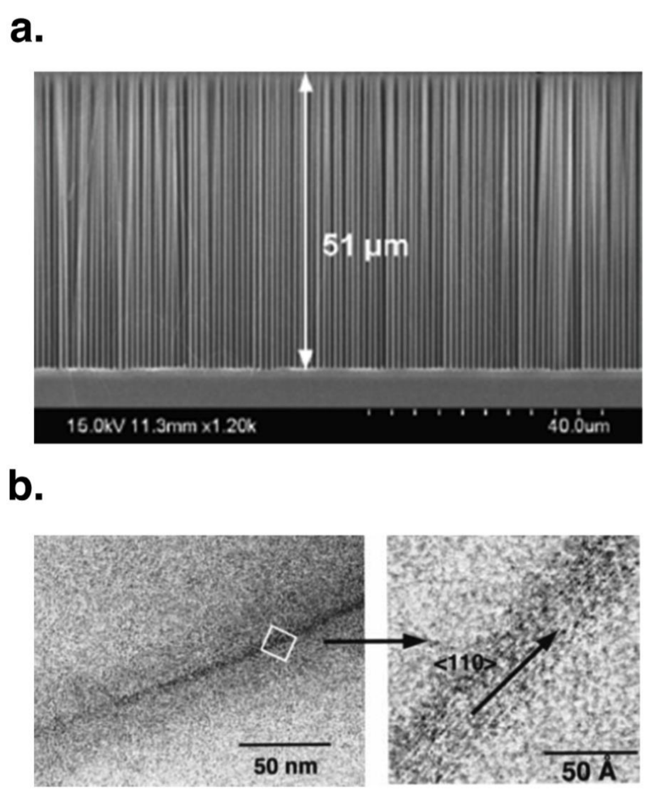

Figure 1.3. (a) Demonstration of vertical high aspect ratio nanopillars without supercritical drying. Cross-sectional SEM image of p+ nanopillars etched for 20 min. Scale bar, 40 μm. Adapted from 201 and reprinted with permission. (b) TEM images of Si nanowires synthesized at 500 °C in hexane at pressures of 270 bar. Scale bar, 50 nm and 50Å. Adapted from 220 and reprinted with permission.

1.3.4 Bottom-up: Laser Ablation

Laser ablation has also been used to synthesize ultrathin NWs with a high aspect ratio.[227-235] In laser ablation, semiconductor materials with a metal catalyst are compressed together as a mixed target for subsequent synthesis. A high-power laser pulse ablates the target in a furnace tube while an inert gas purges through at high temperature. The ablated material vapor is condensed to liquid droplets when colliding with the relatively cold inert gas stream. Then, the liquid droplets continuously absorb semiconductor atoms from the gas, following the VLS mechanism as described in detail in a later section. Once the liquid droplets achieve supersaturation, a new layer of semiconductor material is incorporated into the droplets to form NWs. Morales et al. first demonstrated Si and Ge NW growth with Fe, Ni, and Au metal catalysts as seen in Figure 1.4a by the laser ablation as small as 6 and 9 nm, respectively.[229] Fukata et al. have further shown that growth parameters such as temperature, laser power, inert gas choices and metal content percentage in a mixed target can affect the resultant NW diameter.[112-114] Furthermore, NWs can be synthesized without the help of metal catalysts during laser ablation. Multiple studies of laser ablation demonstrate an ability to form NWs from oxides.[236-240] Oxide-assisted growth relies on phase separation of semiconductor material and its oxide at a high temperature. Nevertheless, the NWs synthesized via the laser ablation method suffer from a high density of defects or kinking[115-118], lack of a sophisticated doping/heterostructure capability[232], and the expensive cost of the required laser apparatus.

1.3.5 *Molecular Beam Epitaxy*

In order to explore a doping/heterostructures synthetic capability, molecular beam epitaxy (MBE) has been introduced to directly modify the composition profile during NW growth.[242-245] In MBE, a thin metal film is first deposited on a substrate. The thin film subsequently breaks into metal seed droplets after annealing. However, the metal droplets do not act as catalysts for cracking precursor molecules. Instead, these droplets only serve as absorption sites during growth. Later, high-purity solid semiconductor sources are heated to generate an impinging flux of atomic species onto the metal seed particles as well as the substrate for semiconductor deposition. In order to maximize the atomic impingement rate and minimize surface contamination, MBE often requires ultra-high vacuum (UHV) conditions coupled with reflection high-energy electron diffraction to analyze surface quality during growth. Thus, one can expect the growth surface after the thermal treatment could have negligible amounts of adsorbates under UHV conditions. This relatively clean surface enables NWs to grow predominantly via diffusion of adsorbed atomic species between the metal seeds.

Multiple studies demonstrate successful Si and Ge NW synthesis in a layer-by-layer fashion similar to the VLS mechanism shown in Figure 1.4b.[246-249] Furthermore, Werner et al. and Schubent et al. show that initial Au thin layer thickness, growth temperature, and impinging Si flux can alter Si NW morphologies.[248-249] However, in MBE synthesis studies for IV and III-V NWs, NWs cannot be formed with diameters less than 30nm.[242-249] The UHV requirements also inherently impose another constraint on the NW growth rate.

1.3.6 Chemical Vapor Deposition

Although chemical vapor deposition (CVD) originally was developed for high quality thin film deposition, it can also be utilized as a NW synthetic method; it is perhaps one of the more widely used methods due to its great flexibility. In CVD, a reactive semiconductor gaseous precursor (e.g., silane, trichlorosilane or silicon tetrachloride) serves as the semiconductor source. Source molecules in the vapor are provided with enough thermal energies and subsequently can be dissociated into their constituents. The constituents are carried to and react with a substrate to deposit semiconductor atoms. Deposition can occur in a wide range of operating temperatures (e.g., 250-1100 °C for Si NWs)[250-251] and pressures (e.g., 10^{-8} to 700 Torr for Si NWs)[252-253] with a possibility to use plasma assistance[254-256] from choices of both semiconductor sources and catalytic materials. In particular, UHV operating conditions for the CVD allows for integration with TEM, opening a new avenue to study the fundamental physics for NW synthesis during growth, as illustrated in Figure 1.4c.[257] Also, intentional doping and compositional modulation can be achieved by simply adding other doping (e.g., PH_3)/semiconductor source (e.g., GeH_4) precursors, offering an opportunity for axial and radial p-n junction formation within a NW.[34, 258] However, during the CVD growth, crystallographic direction of a substrate and diameter of a catalytic metal (if the growth mechanism requires) often induce non-vertical NW growth from the substrate.[259-260] This non-verticality can be solved by using a template[261-262] or appropriate choice of the substrates and operating conditions.[263]

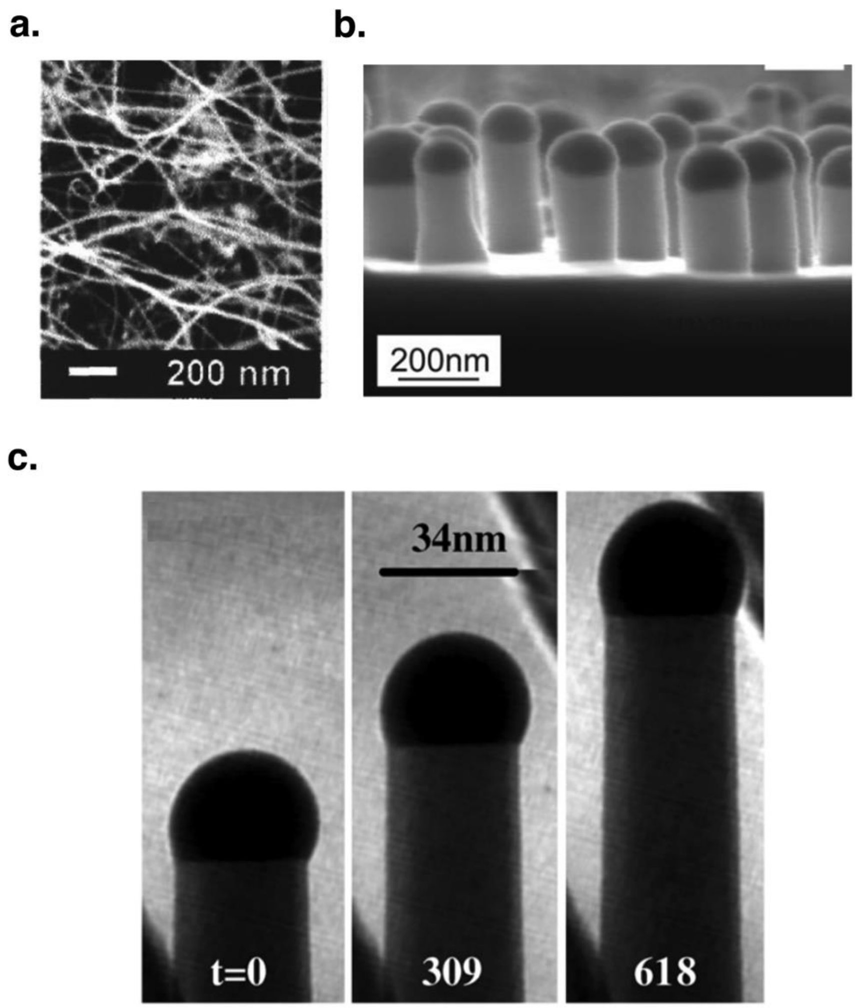

Figure 1.4. (a) Representative SEM image, TEM image, and high-resolution TEM image of Si nanowires synthesized by using $Si_{0.99}Ni_{0.01}$. Adapted from 229 and reprinted with permission. (b) SEM cross section image of Si whiskers grown in <111> Si substrate at 0.5 Å/s for 120 min growth time at 525 °C. Scale bar, 200 nm. Adapted from 246 and reprinted with permission. (c) Ge Nanowire growth from a AuGe liquid droplet at 340 °C and 4.6×10^{-6} Torr Ge_2H_6 with a rate of 0.11 nm/s. The time is shown in seconds since the first image. Adapted from 257 and reprinted with permission.

1.3.7 Vapor-Liquid-Solid Mechanism

The VLS growth mechanism was first proposed by Wagner and Ellis in 1964 for Si micro-wires using Au as a catalyst.[264] However, not until the 1990s did CVD NW synthesis via the VLS mechanism become one of the more dominant methods to synthesize NWs. In the VLS mechanism, metal catalysts on a substrate are heated to/above their eutectic temperature to form catalytic alloy droplets. The droplets catalyze chemical dissociation of semiconductor reactive molecules such (e.g., silane SiH_4) in the vapor (V) in Figure 1.5a. Then, semiconductor atoms (e.g., Si) are absorbed into the liquefied droplets (L) as shown in Figure 1.5b. The continuous incorporation of semiconductor atoms supersaturates the droplet. The further incorporation of these atoms after supersaturation nucleates a new solid nucleus at the edge[265]; subsequently, a solid layer propagates rapidly from the nucleus to form a new solid layer (S), a so called “ledge flow”. These steps occur cyclically during growth to facilitate NW formation, as illustrated in Figure 1.5c. During growth, semiconductor/dopant gaseous sources can be turned on or off to modulate the composition profile. When co-flowing a dopant source (PH_3) with SiH_4 at high temperature, vapor-solid deposition occurs at a higher rate, generating the core-shell structure. When co-flowing a dopant source (PH_3) with SiH_4 at a low temperature, the VLS NW growth rate is at a higher rate than the vapor-solid deposition, creating axial heterostructures. Analogous to the VLS mechanism, the VSS mechanism of growth occurs through these repeated steps, but the catalyst droplets remain in the solid phase during growth via alloying or choices of the catalytic metal.[266-267] In-situ TEM observations reveal that both VLS and VSS mechanisms from NWs via the “ledge flow” layer-by-layer fashion.[268-270]

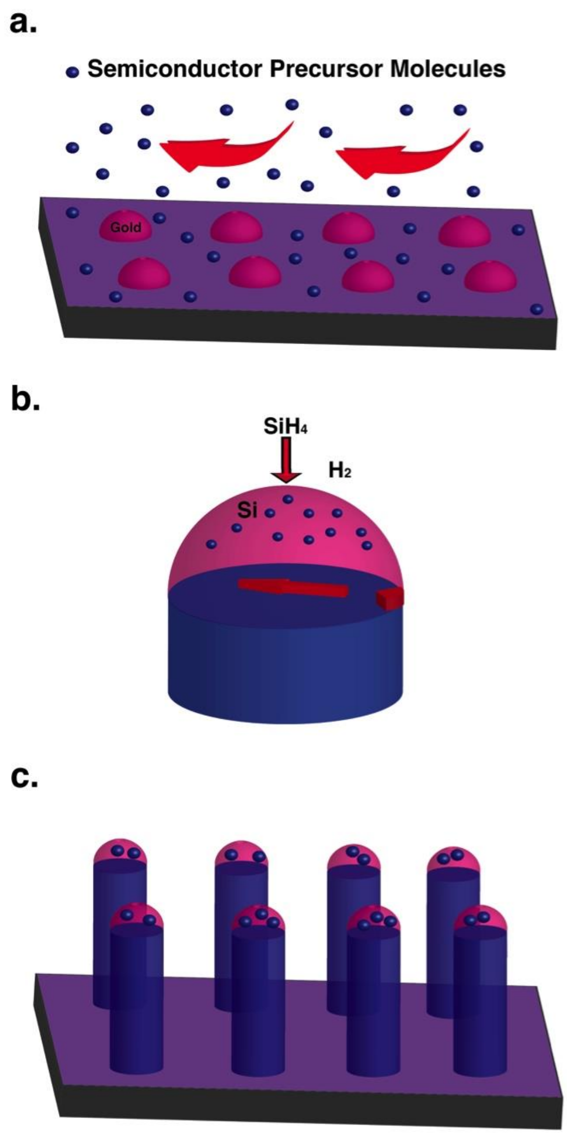

Figure 1.5. General illustration of VLS nanowire growth via chemical vapor deposition (a) At the beginning of nanowire growth, metal catalyst is deposited at selective areas while semiconductor precursor molecules are introduced at or above the eutectic temperature. (b) With the help of the catalyst, semiconductor molecules are dissociated into the liquid catalyst through the vapor-liquid interface. The continuous dissociation of semiconductor molecules saturates the catalyst, favoring a nucleation event at the edge of liquid-solid interface. Once the nucleation occurs, a bi-layer of semiconductor material is quickly formed across the liquid-solid interface. (c) The layer-by-layer growth occurs repeatedly on the areas covered by the metal catalyst to form arrays of semiconductor nanowires across a substrate.

1.3.8 Force Balance at the Triple-Phase Line

Although fundamental thermodynamics generally governs supersaturation and the thermodynamic phase of the catalytic droplets, NW growth is controlled by kinetic events such as sidewall adsorption, semiconductor incorporation, adsorbate diffusion, and droplet dynamics at the LS interface. Among them, the droplet dynamics at the interface can be observed easily by *in-situ* TEM to provide more insights at the triple-phase line, where the vapor, liquid, and solid meet. For example, after each nucleation step, Gamalski et al. used in-situ characterization to observe the cyclic destabilization and partial dissolution of the Ge NWs, as shown in Figure 1.6a-e.[271] This triple-phase boundary dynamic provides strong evidence that the NW growth via the VLS mechanism is kinetic-derived.

During NW growth, catalytic droplets remain at the growth front because the mechanical forces at the triple-phase line are in balance. Figure 1.6a reveals the equilibrium contact angle (θ_c) with three interfacial forces acting on the triple-phase line: liquid-vapor interfacial energy (γ_{lv}), liquid-solid interfacial energy (γ_{ls}), and vapor-solid interfacial energy (γ_{vs}).[271] These interfacial energies with the change in supersaturation ($\Delta\mu$) can guide the rational modulations of NW structures such as kinking. For example, Teroff et al. uses a continuum model to predict NW structures by changing interfacial energies.[272] However, their model assumes that droplets can instantaneously relax to their equilibrium, and these forces are always maintained in balance at the triple-phase line. If the droplets are not at equilibrium, they can diffuse to sidewalls or substrates, as observed by Hannon et al. from an *in-situ* TEM study.[273] Thus, any changes in these three interfacial energies and supersaturation could dramatically change the resultant NW structures.

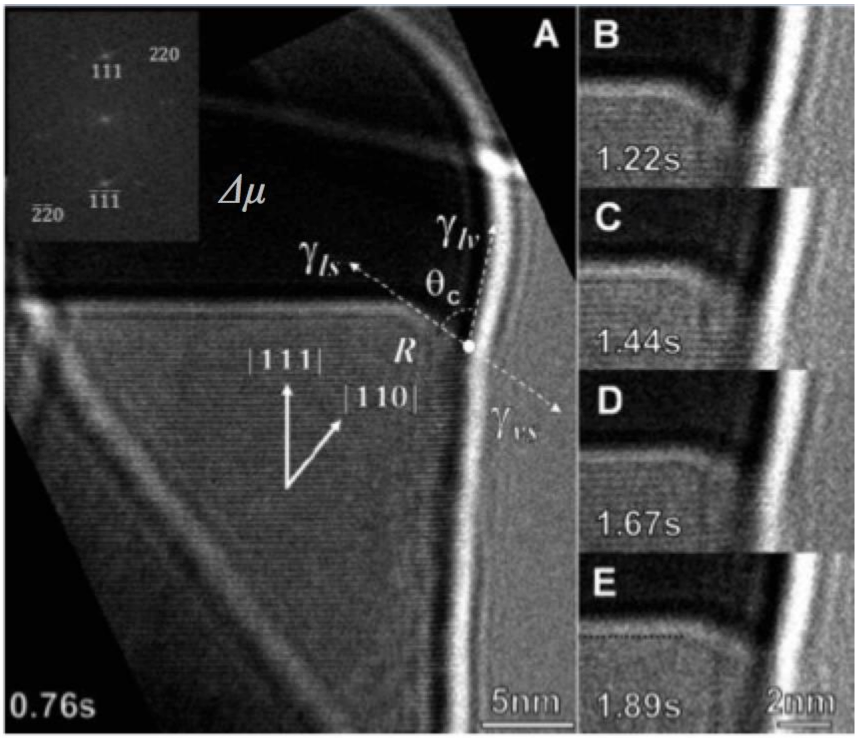

Figure 1.6. Bright field ETEM image sequence of the catalyst interface around the TPB of a growing Ge nanowire at ≈ 310 °C in Ge_2H_6 (30% in He) at ≈ 4 × 10^{-3} mbar. The total times indicated in (A)-(E). In (A) the atomically rough surface is denoted by R, the wetting angle by θ_c, and γ_{lv}, γ_{ls}, and γ_{vs} are the surface energy differences between the liquid-vapor, liquid-solid, and vapor-solid surfaces, respectively. The inset shows a selected area FFT of the Ge nanowire. In(E) the original (111) solid-liquid interface is traced with a dotted black line to highlight the advancement of the growth interface. Adapted from 271 and reprinted with permission.

1.4 Synthetic Advantages in Semiconductor Nanowires via VLS Mechanism

1.4.1 Diameter Modulation

Diameter modulation has received much less attention since its first observation. However, the ability to modulate NW diameters can still enable novel properties. In terms of electrical properties, computational studies show that varying the diameter of a NW can vary its energy band structure and resulting confinement of electrons for quantum wires.[274-275] Experiments demonstrate that the diameter of a NW can alter both resistivity and mobility of electrons, subsequently producing diameter-dependent conductance.[276-279]

In terms of optical properties, modulating the NW diameter changes light scattering, absorption, and reflectance behaviors.[13, 280-281] Also, diameter-modulated segments within a NW show similar changes for potentially broadband photonic applications.[282-283] Surprisingly, periodic diameter-modulated NWs can construct a grating along the sidewall to enable the detection of surface optical phonons.[284]

In terms of thermal properties, diameter-modulated NWs reduce phonon group velocities. Notably, the reduction of acoustic phonons decreases the lattice heat conduction.[285-287] Also, 1D-NW geometries offers enhancements of the Seebeck coefficient for thermoelectric applications.[288-290] Thus, many studies suggest that diameter-modulated 1D NWs are one of the potential candidates to approach Carnot thermoelectric efficiencies.[119-122]

NW diameters can be altered via compositional changes during hetero-interface formation.[294-298] To form a hetero-interface, one needs to switch the gaseous sources. In response to species change in the vapor, contact angle and/or metal catalyst droplet volume can be modified during growth. For contact angle, different gaseous species can alter the mechanical force balance at the triple-phase line (where the vapor, liquid, and solid phases meet) by changing the interfacial energies. Consequently, the contact angles could be modified because the catalyst droplet could then wet or dewet the NW sidewall. For example, Hocevar and his colleagues synthesized GaP/Si NW heterostructures with a larger diameter in the GaP segment, as shown in Figure 1.7a.[296] They suggest that the diameter expansion is attributed to differences in the contact angle between the Au/Ga alloy on GaP and Si surfaces. Although the contact angle can be changed by formation of defects such as twin planes and stacking faults for III-V NW systems, the defects often alter the crystal structures, forming a more complicated system for a diameter modulation study.[299-301] For droplet volume, the droplet can accommodate new gaseous of atoms during the gas-phase switching due to differing solubilities. If the droplet uptakes more new atoms, it can increase the volume of the droplet, expanding the NW cross-section, as suggested by others.[294]

NW diameter can also be modulated via manipulating growth process conditions such as partial pressure of the reactive species and temperature for homogeneous IV-NWs. The changes in both pressure and temperature alter the number of atoms in the metal-catalyst droplet (via absorption) as well as on the NW sidewall (via adsorption). Subsequently, the mechanical force balance (as discussed in the NW kinking section) acting on the triple-phase line should be changed. Crawford and his colleagues showed theoretically that changes in interfacial energies can lead to a larger contact angle[302], especially for the faceted solid-liquid interfaces commonly observed or predicted for IV-NW systems.[303-305] Also, only changing the growth temperature can both increase or decrease the droplet volume, as noted by Sutter and his colleagues for Ge NWs, as shown in Figures 1.7b and 1.7c.[306] They suggest that the change in temperature can manipulate supersaturation in the droplet, putting different numbers of Ge atoms into the droplet.

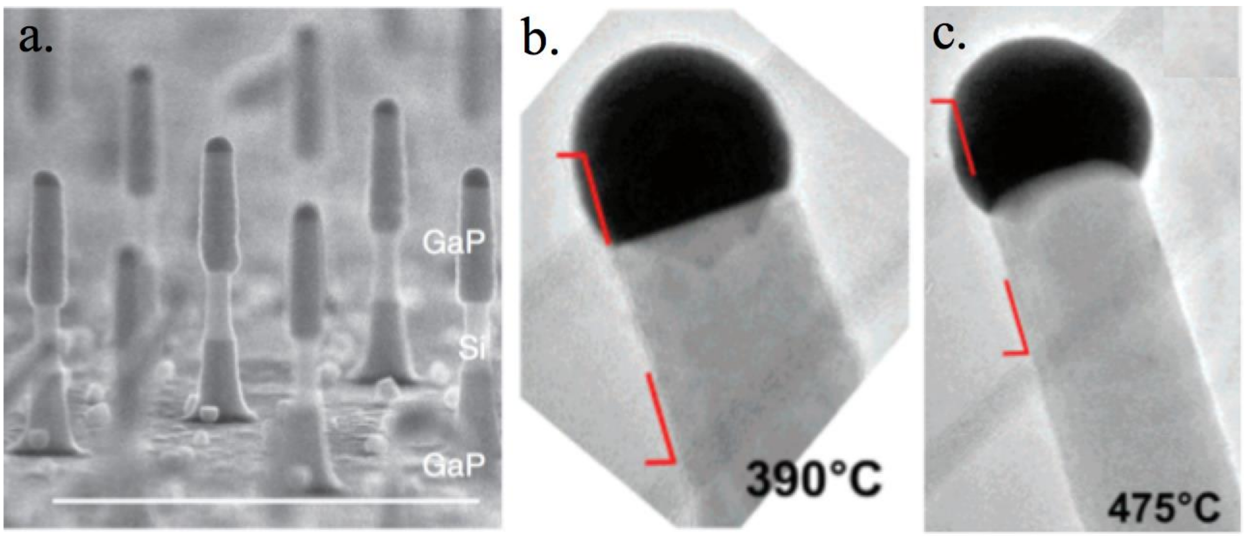

Figure 1.7. (a) SEM image of an array of 60 nm-diameter GaP–Si–GaP nanowires with GaP, Si and GaP segment lengths of 180, 150 and 270 nm, respectively. Tilt angle = 80°, scale bar, 1 μm. Adapted from 296 and reprinted with permission. (b-c) Exchange of material across the Ge NW/liquid drop interface after melting of the alloy Au-Ge nanoparticle at 368 °C. The marker delineates the surface of the Ge NW and provides a reference for the temperature dependent location of the Au-Ge/Ge interface. Adapted from 306 and reprinted with permission.

Diameter modulation can be rationally achieved via surface passivation. The surface passivation method can allow one to independently change only the NW cross-section, not the NW crystal structure or composition. Several studies have investigated chemical passivation of NW sidewalls in solutions.[307-309] Similarly, gaseous chemical species can adsorb at the CVD-grown NW's sidewall, passivizing the surface's dangling bonds as a "molecular resist." Thus, gas-phase semiconductor atoms cannot find an available dangling bond to bond with, dramatically decreasing the V-S deposition rate. A difference in the V-S deposition rate between a passivized segment and a non-passivized segment enables the possibility of intentionally modulating the NW cross-section along a NW. Our group elaborated the "molecular resist" idea and identified two chemical species (tetramethyl tin (TMT) and trimethyl silane (TMSi)) for the diameter modulation, as seen in Figures 1.8a-e.[310-311] Kim and his colleagues used acetylene to grow a carbon sheath for the same purpose, as seen in Figure 1.8f, although the authors suggest that the carbon incorporation path is through the surface of Au droplets.[312]

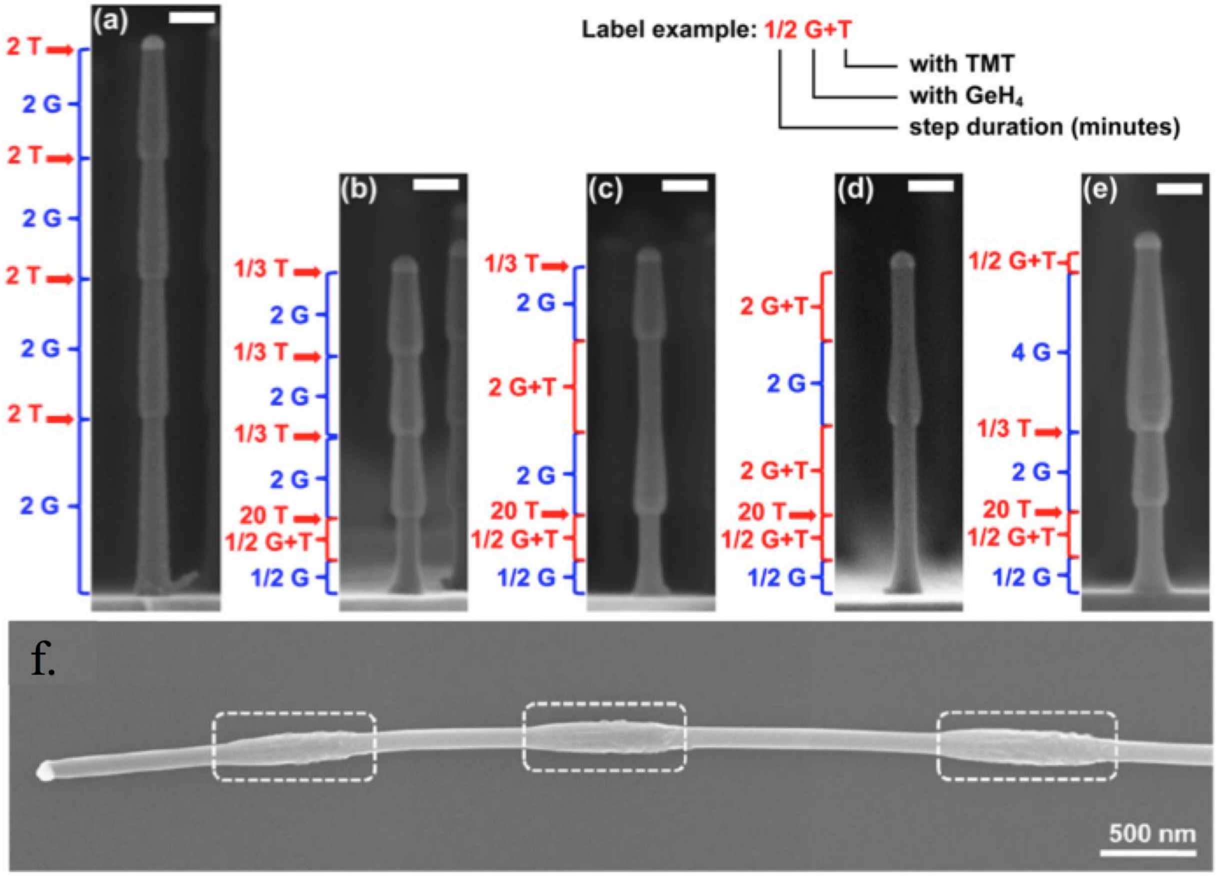

Figure 1.8. (a)-(e) User-programmable diameter-modulated Ge nanowire superstructures fabricated from 20 nm Au colloid on a Ge(111) wafer via combinations of different flow conditions at 350 °C. The sequence of growth conditions utilized for each superstructure is shown to the left of each image. G refers to 15 sccm GeH_4 and 110 sccm H_2 at 2.2 Torr total pressure (i.e., GeH_4 only), T refers to 20 sccm Ar bubbled through TMT and 105 sccm H_2 at 2.2 Torr total pressure (i.e., TMT only), and (3) G + T refers to 15 sccm GeH_4, 20 sccm Ar bubbled through TMT, and 90 sccm H_2 at 2.2 Torr total pressure (i.e., co-flow of GeH_4 and TMT). The number preceding each flow designation represents the time in minutes that each condition was applied. Scale bars, 50 nm. Adapted from 310 and reprinted with permission. (f) A series of SEM images of a single Ge NW with three elliptic fragments induced by a repeated carbon gas, "on-off" process. It clearly shows the effect of the carbon sheath on preventing the uncatalyzed vapor deposition during the NW growth process. Adapted from 312 and reprinted with permission.

1.4.2 Doping Incorporation

Incorporation of dopant impurities is one of the essential synthetic techniques in the fabrication of semiconductor structures and integrated devices. For dopant incorporation, dopant atoms can either sit between crystal atoms (interstitial doping) or replace the host crystal atom (substitutional doping), injecting free carriers into a host material system to modify conductivity. The free carrier injection gives additional flexibility to alter the band gap of the host system. Semiconductors can be doped with either donor or acceptor impurities. The donor impurities create extra free electrons; acceptor impurities provide additional holes to the semiconductor crystalline lattice.

Analogous to semiconductors, semiconducting NWs follow the same doping principles and have been demonstrated to be effective dopants. For example, IV-NWs can be doped with boron, phosphorous, arsenic, antimony or manganese[313-319] while III-V NWs can be incorporated with magnesium, silicon, sulfur, and zinc.[320-325] Dopant incorporation in the NWs alters their electrical, optical, magnetic and thermal properties[123-132], and these novel properties enable applications in devices such as field effect transistors,[1-2, 133-134] logic gate/circuits,[7,135-136] tunnel diodes,[137-139] photodetectors,[337-338] (bio)chemical sensors, [339-341] and thermoelectrics.[342-343] Recently, it has also been demonstrated, for the first time, doping-induced localized surface plasmon resonance (LSPR) in highly phosphorous-doped Si NWs.[140-142] The LSPR can be tuned by the dopant concentration in NWs, promoting novel usages such as NW-based high-speed optical interconnects.[345]

VLS-mediated incorporation is used as a standard method to modulate doping concentration axially and radially.[1, 127, 133, 135, 137-138, 140-145] In VLS-medicated doping, it is generally accepted that there are two primary incorporation paths: dopant incorporation via a metal catalyst (VL interface), or non-catalytic conformal VS growth (VS interface).[346-354] For the VLS-grown III-V NWs, dopant atoms can be incorporated into the lattice structure at element III or V sites, complicating the doping incorporation mechanism. To fundamentally understand doping incorporation, IV-NWs serve as an ideal system to investigate dopant incorporation paths as well as the subsequent alteration of their properties. The core-shell (conformal V-L growth) doping NWs were first demonstrated by Lauhon et al.; they first grew the intrinsic Si core and subsequently deposited silicon shells with boron dopant, as shown in Figures 1.9a-b.[34] The CVD shell deposition process in their study is analogous to the doping CVD process for semiconductors that has been discussed in many studies.[355-358]

The focus then turns to the axial doping-modulated NWs. As an example of the axially doped NWs, Figure 1.9c shows a p-i-n Si NW synthesized by Kempa et al.[14] The doped segments are exposed after a selective etching process, showing the possibility of doping the NWs via a repeated VLS mechanism.

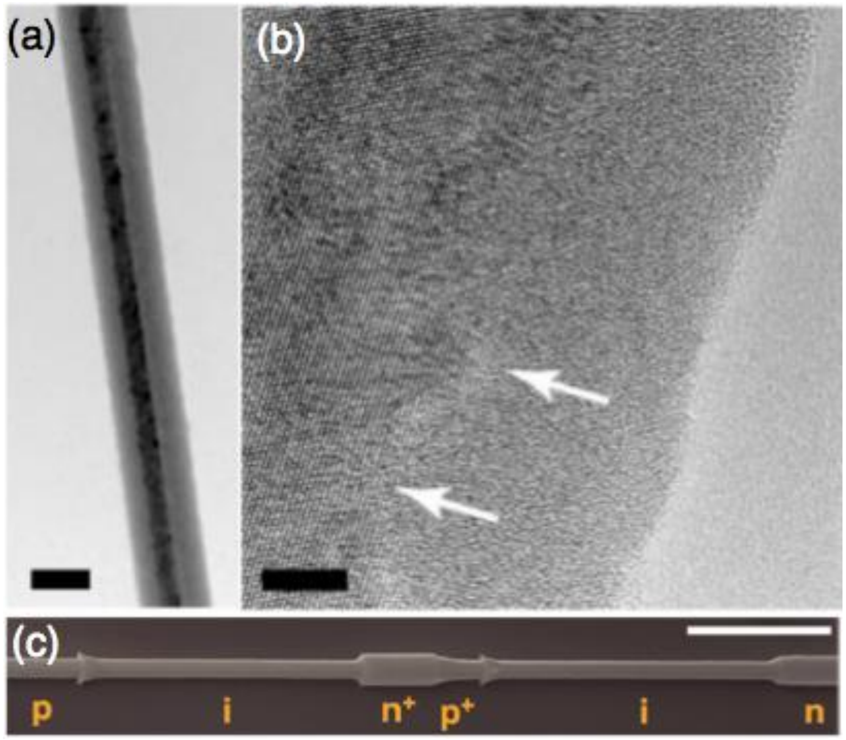

Figure 1.9. (a)-(b) Diffraction contrast and high-resolution TEM images, respectively, of an unannealed intrinsic silicon core and p-type silicon shell nanowire grown at 450 ^{o}C. Crystal facets in the high-resolution TEM image designated by arrows indicate initially epitaxial shell growth at low temperature. Scale bars are 50 nm and 5 nm, respectively. Adapted from 34 and reprinted with permission. (c) SEM images of a selectively etched tandem p-i-n+-p+-i-n SiNW; scale bar is 1 μm. Adapted from 14 and reprinted with permission.

1.4.3 Nanowire Heterostructures

The most exciting fundamental physics and electronic and optical applications often do not come from a single material, but from a two or multi-material system. Traditionally, many materials can grow on top of another to form planar heterostructures. If these materials were highly lattice-mismatched, strain would be accumulated at a heterointerface.[359-361] When the accumulated stress reaches a critical value, dislocations or/and defects can be generated at this interface. However, the unique NW geometry relaxes the elastic strain laterally, offering an ideal platform to formulate defect-free heterostructures and greater flexibility to incorporate different highly mismatched materials both axially and radially within a NW.[362-365] These NW heterostructures can introduce a band offset and subsequently generate an electrostatic potential difference at the hetero-interface. This potential difference can either accelerate or prevent free carriers from transporting across the hetero-interface, giving an additional degree of freedom (or hindrance) to internal manipulation of the carrier charge transportation for electrical and photonic devices.[366-367] Thus, device performance in all applications will depend on the quality of the hetero-interface: compositional abruptness and structural perfection. For III-V NW heterostructures, a defect-free and atomically-abrupt hetero-interface can be realized in many experimental demonstrations such as GaAs/GaP, InAs/InP, and InAs/InSb NWs, which have been the focus of other reviews.[368-369] Radial and axial IV-NW heterostructures, on the other hand, are advantageous in the device applications due to their compatibility with existing microelectronics structures. Notably, the radial IV-NW heterostructures face synthetic challenges similar to those encountered in thin film heterostructures, which also have been described in many studies.[370-372]

Many early studies have shown the formation of axial IV-NW heterostructures. Wu and his colleagues first demonstrated a novel method of synthesizing the axial Si/SiGe superlattice NWs via a combination of laser ablation and CVD.[232] The Si segments were synthesized by flowing $SiCl_4$ and H_2 at a temperature above 850 °C, while the SiGe segments were synthesized by evaporating a Ge target via a programmed laser pulse with the continuous $SiCl_4$ flow. The single-crystalline axial Si/SiGe superlattice was shown to hae a graded transition. Later, Gudiksen and his colleagues synthesized GaAs/GaP junctions in a NW via a similar laser assisted-CVD at 700-850 °C with a graded interface.[258]

Since then, the synthetic focus has shifted to CVD at a relatively low temperature to create a better interface compositional profile. To extend the range of applications for NW heterostructures, these NW heterostructures should be realized not only within group IV elements, but also within a combination of group IV and III-V materials. Dick et al. utilized the same model to describe the NW heterostructures with different combinations of III-V and IV materials, as tabulated in Table 1.2.[373] They observed NW heterostructures being formed without defects with large lattice mismatch.[373] For example, a straight double heterostructure could be formed between GaP and InAs with 11.14% lattice mismatch. Many future exciting opportunities can be realized if future synthesis techniques can permit ideal multiple-component heterostructures in a single NW. The possibilities include ballistic carrier transport, precise band-to-band carrier tunneling, and phonon transfer confinement, truly enabling a new path toward sophisticated nanodevices.

Table 1.2. Lattice Constants, Lattice Mismatch, and Heterostructure Nanowire Morphology for 13 Material Combinations. Adapted from 257 and reprinted with permission.

material A	material B	material A lattice constant (Å)	material B lattice constant (Å)	morphology: B on A[a]	morphology: A on B	mismatch[b] (%)
AlAs	GaAs	5.6605	5.6533	kinked	straight	−0.13
AlAs	GaP	5.6605	5.4512	kinked	straight	−3.70
AlAs	InAs	5.6605	6.0584	kinked	straight	7.03
AlAs	InP	5.6605	5.8686	kinked	straight	3.68
GaAs	GaP	5.6533	5.4512	straight	straight	−3.57
GaAs	InAs	5.6533	6.0584	kinked	straight	7.17
GaAs	InP	5.6533	5.8686	kinked	straight	3.81
GaAs	Si	5.6533	5.4310	kinked	straight	−3.93
GaP	InAs	5.4512	6.0584	kinked	straight	11.14
GaP	InP	5.4512	5.8686	kinked	straight	7.66
GaP	Ge	5.4512	5.6461	kinked		3.58
GaP	Si	5.4512	5.4310	kinked	straight	−0.37
InAs	InP	6.0584	5.8686	straight	kinked/straight[c]	−3.13

a Note that "straight" refers to continuation of growth in the same crystallographic direction, while "kinked" refers to a change of growth direction.
b Mismatch % is calculated with respect to material A, according to the formula mismatch = (aB-aA)/aA. Therefore, a positive value of mismatch indicates that the lattice constant of material B is larger than that of material A.
c The morphology type for InAs grown on InP depends on the growth condition.

1.4.4 *Growth Direction Modulation*

One of the advantages of 1D and 2D nanomaterial systems is to incorporate them as a building block for 3-D nanostructures. These structures such as nano-helixes, nano-springs, nano-rings, and nano spirals have been demonstrated in many nanomaterial systems.[374-378] Among them, to exploit 3-D nanostructure-based device applications, IV-NWs are especially attractive due to their compatibility with existing microelectronic infrastructure. As a first step toward 3-D nanostructures utilizing NW, the NW growth direction must be precisely controlled during creation. For the VLS mechanism, NWs can be disturbed during growth to alter the growth path, called "kinking." Kinked NWs have been applied as ultra-sensitive biological sensors, recording intracellular activities.[17, 78, 146-148] Also, kinked NWs exhibit unique mechanical and thermal properties, leading toward future nano-mechanical and thermoelectric applications.[382-384]

Growth direction modulation has frequently been observed in the literature due to changes in experimental conditions during growth. Wagner and Doherty first showed micro-Si wires could be kinked from one <111> to another <111> growth direction if a local temperature gradient was introduced.[385] Since then, many studies have demonstrated that temperature or pressure changes can induce kinking.[385-392] As an example, Figures 1.10a-c, from the study of Madras et al. shows that Si NW kinking from [111] to either another [111] or [112] is observed as either the temperature decreases or the pressure increases.[392] Tian et al., on the other hand, interrupted the Si NW growth process by purging the semiconductor reactants from the growth chamber during growth to trigger the kinking, as shown in Figure 1.10d.[393] There is also another approach to control kinking: surface chemistry. As the experimental conditions change during growth, controlling the number of adsorbed atoms/molecules on NW sidewalls to induce kinking can be instituted.[263, 394] Studies show that hydride and methyl group chemistries can be used for kinking nanowires, as illustrated in Figures 1.10e[263] and 1.11[394].

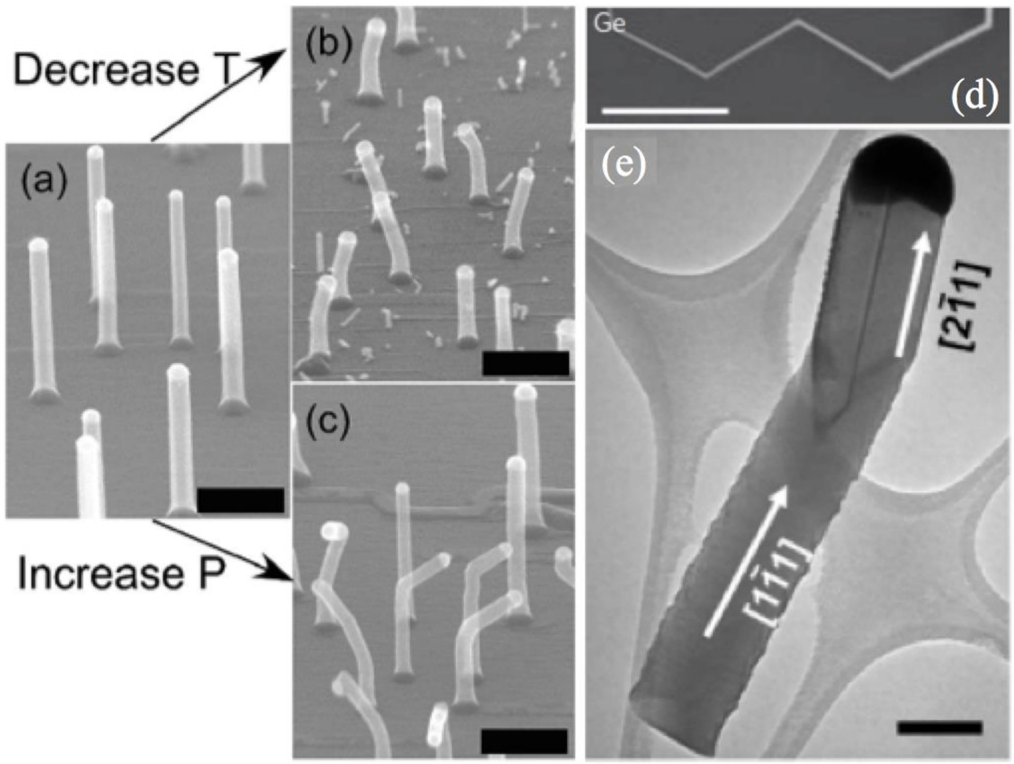

Figure 1.10. (a)-(c) SEM images showing Si nanowires grown from 100 nm diameter Au/Si(111) seeds for different disilane pressures, P, and substrate temperatures, T. (a) T) 500 °C, P) 0.7 mtorr, (b) T = 400 °C, P = 0.7 mtorr, and (c) T = 500 °C, P = 10 mtorr. Samples were imaged 60° away from normal toward [112]. All scale bars are 500 nm. Adapted from 392 and reprinted with permission. (d) SEM image of one multiply kinked germanium nanowire. Scale bar, 1 mm. Adapted from 393 and reprinted with permission. (e) Bright-field TEM image of a representative Si NW grown for 60 min with 5×10^{-5} Torr Si_2H_6 at 490 °C followed by the addition of 1×10^{-4} Torr H_2, at the same Si_2H_6 pressure, with the W filament on for another 120 min (180 min total). Scale bar, 200 nm. Adapted from 263 and reprinted with permission.

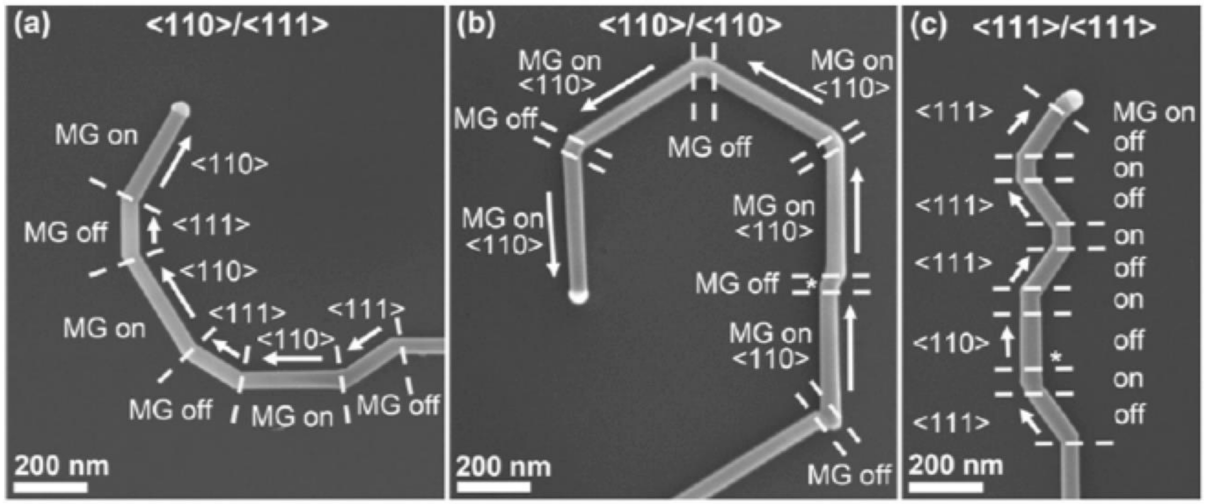

Figure 1.11. Ge nanowire kinking superstructures fabricated at 325 °C by introducing GeH_3CH_3 at user-defined points during VLS growth. Segments without GeH_3CH_3 are grown with 0.44 Torr of GeH_4 and 8.81 Torr of H_2 while those with GeH_3CH_3 are grown with 0.44 Torr of GeH_4, 0.21 Torr of MG, and 8.81 Torr of H_2. SEM images of (a) ⟨111⟩/⟨110⟩, (b) ⟨110⟩/⟨110⟩, and (c) ⟨111⟩/⟨111⟩ superstructures where GeH_3CH_3 is cycled on for 1 min and off for 1 min, on for 1.5 min and off for 15 s, and on for 10 s and off for 1 min, respectively. Dashed lines show where GeH_3CH_3 flow was initiated or terminated. An asterisk denotes "defect" locations where transition does not occur as desired. Adapted from 394 and reprinted with permission.

1.5 Summary and Perspective

Semiconductor NWs have become an indispensable nanoscale platform for a broad range of electronic, photonic, and energy conversion applications. The bottom-up vapor-liquid-solid (VLS) NW fabrication technique offers the ability to encode material functionalities along the length of a NW in a user programmable manner. However, robust control of VLS growth requires understanding of multiple heterogeneous chemical processes: (1) transportation of semiconductor molecules/atoms from vapor to liquid droplets or vice versa at the vapor-liquid (VL) interface, (2) crystallization and dissolution of semiconductor atoms at the liquid-solid (LS) interface, and (3) the conformal deposition of precursor molecules onto the NW sidewall at the vapor-solid (VS) interface. The ability to rationally engineer NWs for advanced semiconductor devices is critically impaired by limited understanding of these chemical processes.

In this thesis, we first focus on heterogeneous chemical reactions at the VL interface. In Chapter 3, we demonstrate a novel solid-liquid-vapor (SLV) process to remove the semiconductor atoms from the NW, which has been theoretically discussed for decades with no definitive experimental conclusions. We use a dicarbonyl species, 2,3-butanedione, to *in-situ* etch <111>-grown Ge NWs selectively in the growth direction with the help of a metal catalyst spread uniformly across a large area.

In Chapter 4, we connect SLV etching at the VL interface to the LS interface. We propose that this top-down NW etching process operates by dissolving Ge atoms from the NW crystal into the eutectic catalyst through the LS interface. Subsequently, a volatile etch product at the VL interface removes Ge atoms in the eutectic catalyst. Also, we propose and substantiate a kinetic model to describe this selective NW etching removal process. The kinetic model is then validated by the experimental data and can be used as a theoretical tool to predict the etch rate for a wide range of experimental conditions.

In Chapter 5, we leverage surface chemistry knowledge gained from previous projects to engineer defect-free Si-Ge NW heterostructures. We recognize that a monolayer of hydrogen atoms at VS interface may be critical for stable NW growth. Often, imperfections in NW heterostructures synthesis potentially come from the growth instability by losing the hydrogen layer at the VS interface when switching to different precursor gasses at different temperatures. Here, we use trisilane (Si_3H_8) – a highly reactive precursor for Si – to maintain monolayer hydrogen coverage at the VS interface while still supplying enough semiconductor atoms for Si segment growth at low temperatures. The low-temperature environment helps maintain a hydrogen layer at the VS interface. Thus, an array of Si/Ge heterostructure NWs is synthesized without defects at the hetero-junction. Finally, we leverage the technique to form a Si nano-disk which is embed in two Ge segments. The apprehension of the heterogeneous chemical processes derived over the course of my studies has set the stage for robust VLS NW synthesis and potentially enables future development of NWapplications.

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CHAPTER 2. EXPERIMENTAL METHODS

2.1 Chemical Vapor Deposition

2.1.1 Kinetic Theory of Gases

The kinetic theory of gasses is central to understanding heterogeneous reactions at different interfaces via CVD. It illustrates the microscopic behavior of gas molecules and their interaction for creating further dissociations or reactions. In this theory, all gas molecules act like ideal gasses, randomly moving in all directions and interacting with each other via only elastic collisions while maintaining the shape and size of the molecules. The theory shows this relationship between mean free path (λ) and reactor pressure in Eq. 2.1.[1] The λ is the average distance between gas phase molecule collisions:

$$\lambda = \frac{k_B T}{\sqrt{2}\sigma P} \tag{2.1}$$

where k_b is Boltzmann's constant and T is the gas temperature, σ is collision cross section of the molecule, and P is pressure. When two gas molecules collide with each other, their valance electrons can be rearranged in overcoming the energy barrier (minimum energy requirement for reactions) until achieving the most stable form as a final product. Additionally, gas molecules cannot travel with the same speed; thus, as shown in Eq. 2.2, a Maxwell distribution is used to describe a molecule's traveling speed in one direction at a given temperature:

$$f(v_x) = \sqrt{\frac{m}{2\pi k_B T}} e^{\frac{-mv_x^2}{2k_B T}} \tag{2.2}$$

where *m* is the mass of the gas molecule, and v_x is the speed of the gas molecules traveling in only x direction, as an example. For low pressure (LP)-CVD NW growth in our studies, the pressure is around 2-7 Torr; associated mean free path is on the order of 10-100 meters. Similarly, for ultra-high (UHV)-CVD NW growth in our studies, the pressure is ~10^{-9}-10^{-10}Torr; associated mean free path is on the order of 1000 meters. In both cases, one can safely assume that gas molecules have no or minimum intermolecular collision in the gas phase. Thus, reactions only occur after gas molecules collide with the liquid catalyst and NW sidewalls at the VL and VS interfaces, respectively. The reaction rate is proportional to the impinging rate of gas molecules at these interfaces. The impinging rate, which is defined in Eq. 2.3, depends on reaction pressure and temperature:

$$\frac{dN_{imp}}{dt} = \frac{P}{\sqrt{2\pi m k_b T}} \tag{2.3}$$

where *m* is the mass of the gas molecule, and t is time. With the same gas molecule at the same temperature, the impinging rate in the LP-CVD process is > 10000 times higher than the UHV-CVD, since reaction pressure is different by more than four orders of magnitude. Thus, the NW growth rate in the LP-CVD process is significantly higher. In general, the LP-CVD can be used to study the growth phenomena at the VL and LS interfaces. However, the high heterogeneous reaction rates may prevent researchers from performing surface-sensitive measurements at the NW sidewalls (VS interface). Instead, due to the slow kinetic rates, UHV-CVD processes become an alternative technique to understand and correlate the growth phenomena to surface reaction and its adsorbent. With these two techniques combined together, the heterogeneous reactions at these three interfaces can be studied qualitatively and quantitatively.

2.1.2 Chemical Vapor Deposition Theory

The semiconductor NW growth via vapor-liquid-solid mechanism is essentially a catalytic chemical vapor deposition on selective areas to form a 1D structure. In the fabrication of microelectronic and optical devices, chemical vapor deposition has been the most sophisticated chemical process for depositing thin films with selective properties. In traditional CVD processes, semiconductor precursors such as silane are dissociated into by-products and silicon is subsequently deposited onto a semiconductor surface. There are many forms of CVD techniques: ultra-high vacuum CVD[2-3], plasma-enhanced CVD[4-5], remote plasma CVD[6-7], rapid thermal process CVD[8-9], low-pressure CVD[10-11], and even atmospheric pressure CVD[12-13]. Their differences are mainly the reaction pressure, and heating mechanism for energy supply. However, the underlying chemical reaction is basically pyrolysis of semiconductor precursors such as silane as exemplified in Eq. 2.4. Extensive literature studies have been conducted to understand the kinetic mechanism of this reaction. Kinetic understanding is essential because in thermodynamics, a typical chemical vapor deposition process does not depend on the free energy change of the reaction. All CVD reactors are a continuous flow reactor in that fresh semiconductor precursors are constantly supplied while pumping out by-products and unreacted precursor molecules. The reaction is inherently not at equilibrium, and mainly driven by kinetic theory considerations used to determine the film properties and deposition rate. Thus, understanding the kinetics of the traditional film deposition theory is also critical for NW growth.

Although the overall deposition reaction mechanism in CVD is relatively simple, as seen in Eq. 2.4, diverse elementary reactions also occur at the semiconductor surface. Extensive studies via different surface and optical measurement techniques have been done to understand adsorption and decomposition pathways of silane.[14] One of these possible reaction full mechanisms for Si film growth on Si substrates is in the following:

$$
\begin{aligned}
&SiH_4(g) + 2* \rightarrow H* + SiH_3* \\
&SiH_3* + * \rightarrow H* + SiH_2* \\
&2SiH_2 \rightarrow H_2(g) + 2SiH* \\
&2SiH \rightarrow H_2(g) + 2*
\end{aligned}
\tag{2.4}
$$

where "*" represents an active site on the Si substrate and the "SiH*" corresponds to a surface-bound reactive intermediate. One may notice that intermediate adsorbents on a surface can drastically affect the overall reaction rate in Eq. 2.4. For example, SiH4 molecules cannot adsorb on the surface if the surface sites are occupied by other surface intermediates. However, the lifetime of surface intermediates can be modulated as a function of temperature.[14] Thus, the CVD process can easily transit from kinetic-limited due to the surface inhibition to mass-transfer limited due to insufficient precursor supply. Similar, NW sidewalls can be treated as semiconductor surfaces in that adsorption and decomposition can constantly occur during NW growth. The only difference between traditional CVD for film deposition and catalytic CVD for NW synthesis is the use of a metal catalyst. The metal drastically lowers the energy barrier for precursor dissociation, and offers an alternative reaction path for controlled deposition of a semiconductor layer via nucleation by the catalyst. The additional pathway not only helps incorporate different functionalities within NWs, but may also lower the thermal budget for NW synthesis. Also, NW growth only occurs in the area covered by the metal catalyst, so the metal catalyst precisely defines NW growth locations across a semiconductor wafer.

2.2 Low-pressure Chemical Vapor Deposition

2.2.1 Introduction

One of the major challenges with semiconductor film deposition is to form an abrupt compositional interface by doping. However, the interface is graded in traditional semiconductor film deposition because of molecular diffusion dependent on the thermal budget being employed. The molecular diffusion can be minimized by lowering the growth temperature, but the low temperature keeps more hydrogen atoms on surface. The hydrogen atoms are later incorporated in a new layer, inducing defects such as stacking fault. However, a study has shown that a low-pressure environment can reduce the adsorption of hydrogen on a surface.[15]

For NW growth, the reduction of hydrogen adsorption can be an advantage. NW sidewalls are just semiconductor surfaces that hydrogen atoms can constantly adsorb and desorb from. Fewer hydrogen atoms on the sidewalls allows semiconductor atoms to deposit onto empty surface sites. Intentional tapering in Chapter 3 can be used as a NW ruler or morphological maker for in-situ calibration with the help of other chemicals such as trimethyl silane.[16] Also, as compared to UHV-CVD, more semiconductor and test chemical precursor molecules can be introduced into the reactor. More semiconductor molecules can accelerate the nucleation at each layer while chemical modification from the test chemical precursor could be amplified. In both cases, we can shorten our growth time and easily characterize the NW morphology via ex-suit microscopic techniques.

2.2.2 Low-pressure Chemical Vapor Deposition Reactor

FirstNano EasyTube 3000 LP-CVD reactor was designed to handle a wide range of temperatures and pressure in a programmable fashion for the group IV semiconductor NW synthesis. The LP-CVD reactor is connected with Silane (SiH_4, 99.999%, Air Products) and germane (GeH_4, 99.999%, Matheson Tri-Gas) gases are used as silicon and germanium precursors, respectively. Other carrier and chemical gases include: hydrogen (H_2, 99.999%, AirGas),argon (Ar, 99.997%, Air Products), methylgermane (GeH_3CH_3, 97%, Gelest), trimethylsilane ($SiH(CH_3)_3$, 99.99%, Voltaix). Figure 2.1 shows a schematic illustration for all gas lines connected to the LP-CVD reactor.

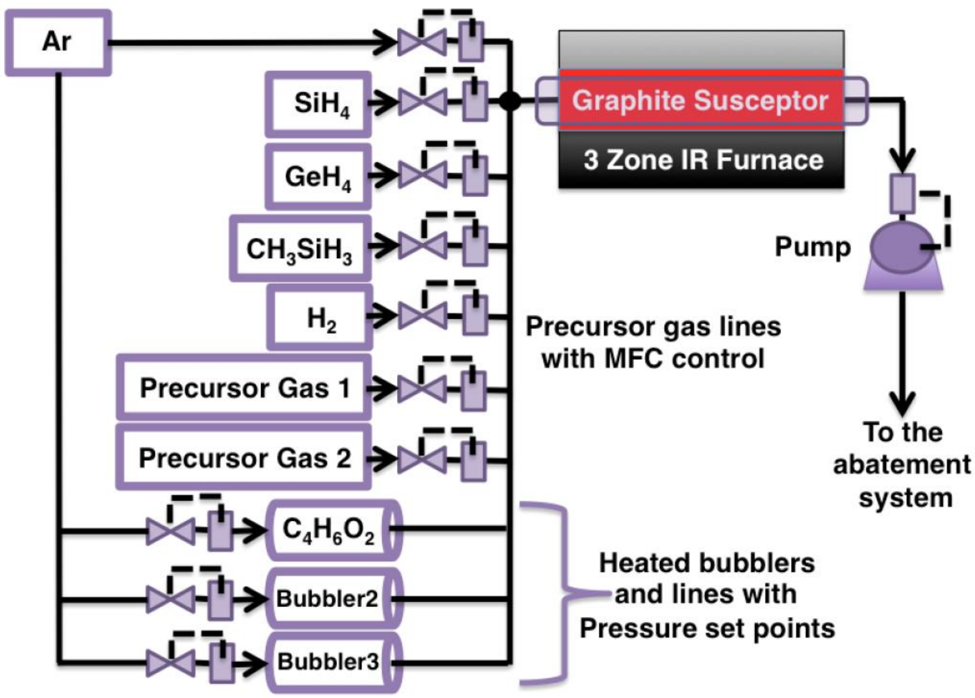

Figure 2.1. Schematic illustration of all process lines in the LP-CVD furnace. The triangular boxes are precursor gas cylinders connected with the LP-CVD reactor. The cylindrical boxes at the bottom are liquid precursor bubblers flowed with Ar gas to inject the liquid precursor into the LP-CVD reactor.

The gas cylinders are stored one floor below the LP-CVD reactor. They are connected via 316L seamless stainless steel lines with submicron stainless steel filters. The minimum operating line pressure is 8 psig. For each gas precursor line, there is a dictated mass flow controller (MFC) connected with an individual Ar purge line. All MFCs are calibrated by manufacturer specifications based on heat capacity and density of the precursors. The Ar flow rate is controlled by a pneumatic valve. All pneumatic valves with mounted solenoids can switch between open and closed states for only 0.005 s. The valve operation can be programmed such that if the pneumatic valves from gas cylinder to MFC and MFC to reaction chamber are open, the precursor molecules can be delivered to the LP-CVD reactor for NW synthesis. Otherwise, the line pressure and gas flow can be stabilized when the pneumatic valve is open from MFC to the vent line, bypassing the reactor. Moreover, multiple liquid precursors can be used by flowing Ar gas through the bubblers. A liquid precursor is stored in a stainless steel bubbler. The bubbler can be heated up to 130 ^{o}C. The bubbler temperature is monitored by a thermocouple in a stainless steel sheath embedded at the bottom of the bubbler with an electric heating strip. Additionally, the bubbler is enclosed by a thick rubber sheet for thermal insulation. Figure 2.2 shows the physical images of different components of the LP-CVD reactor.

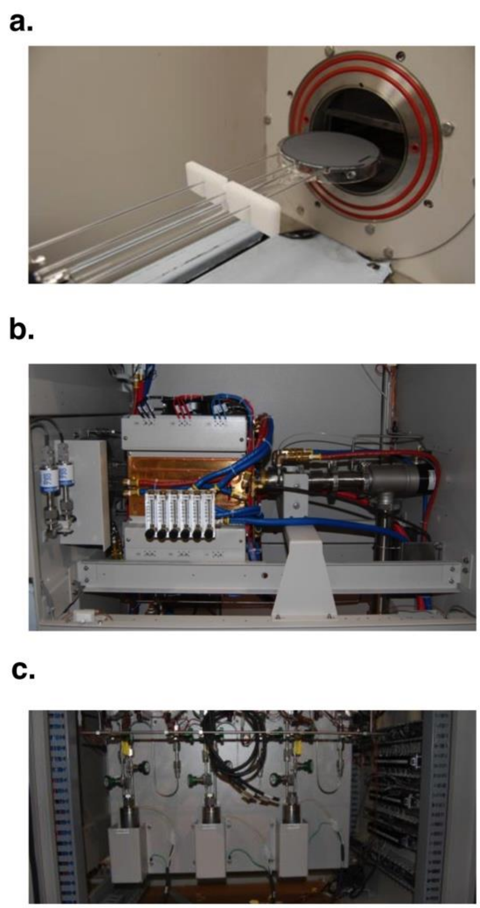

Figure 2.2. Photographs of different components in the LP-CVD furnace. (a). graphite susceptor, (b) infrared heating chamber with cooling water lines, (c) liquid precursor bubblers.

2.2.3 Reaction Parameter Controls

The pressure in the LP-CVD reactor can be controlled from 0.001 to 1000 Torr by two capacitance manometers in the feedback loop to a variable speed dry vacuum pump (Busch BA100 70 CFM). The reactor chamber seal is differentially pumped between two Viton O-rings with a secondary pump to ensure the vacuum level. The leak up rate at base pressure is below 0.001 Torr per minute and is checked before every growth process. The partial pressure of a precursor is calculated as the follow:

$$P_{prec.} = P_{total} \frac{f_{prec.}}{f_{total}} \tag{2.5}$$

where $P_{prec.}$ is the partial pressure of precursor, P_{total} is the controlled total pressure of the chamber, $f_{prec.}$ is the flow rate of the precursor, and f_{total} is the total flow rate of all gases through the chamber.

Infrared heating lamps are mounted at the top and bottom of the LP-CVD reactor for cold wall heating of the graphite susceptor. The 4-inch diameter susceptor has three embedded K-type thermocouples across the length. A feedback control is implemented to maintain the temperature in the three zones of infrared lamps for ±3 °C temperature uniformity across the length. Thus, additional PID controller tuning is often required to optimize the uniformity. The proportional gain is optimized, followed by the introduction of integral gain in the PID tuning. Finally, the derivative gain is included to minimize the overall temperature variation across the susceptor. The lamps are capable of heating and cooling the susceptor up to ±10 °C/s.

2.2.4 *Substrate Preparation*

10% HF is initially used to remove the native oxide of single side polished Si(111) (El-Cat, CZ) or Ge(111) (MTI Corporation, CZ) surfaces. In the process of oxide removal, H atoms are also adsorbed on surfaces. The hydrogen-terminated surfaces can temporarily lower the semiconductor oxidation rate. Subsequently, the semiconductor wafer is immersed into Au colloid solution (unconjugated, BBI, 20-50 nm) mixed with 0.1M HF for 5 minutes.[17] The negatively charged citrate ion from the stabilized gold nanoparticles becomes neutral in the slight acidic environment. Thus, the Au nanoparticles can deposit onto the hydrogen-terminated substrate.[18] Finally, the wafer is quickly rinsed with DI-water before loading to the low-pressure chemical vapor deposition reactor for NW growth.

2.3 Ultra-high Vacuum Chemical Vapor Deposition

2.3.1 *Introduction*

UHV-CVD has been used to study kinetic mechanism and properties of the Si and other semiconductor epitaxial films. In transitional CVD, uniformly strained epitaxial semiconductor films can be achieved via UHV-CVD.[2-3] The key differences between the UHV-CVD and other high-pressure CVD processes are the absence of hydrodynamic boundary layer effect and gas phase chemical reactions between precursor molecules before any surface reactions. In UHV-CVD, a hydrodynamic boundary layer cannot form because material transport is mainly driven by molecular flow. Additionally, the molecular mean free path is much larger than the reactor dimension, so the precursor molecules cannot react with each other via side reactions. Thus, the film growth rate only depends on the surface deposition rate of the precursor molecules. Although the surface dominant reaction condition can be achieved via other CVD processes by careful optimization of the reaction temperature, pressure, and pumping rate, the UHV-CVD serves as a simply alternative to study surface-driven growth process in a much cleaner environment.

For NW growth, hydride semiconductor precursors such as silane or germane constantly deposit semiconductor and hydrogen atoms at the NW sidewalls. The UHV-CVD can eliminate other gas phase side reactions, and allow researchers to focus on the surface reactions. Thus, the relationship between surface reactions and NW synthesis can be studied *in-situ* when coupling with other optical characterization techniques such as infrared (IR) spectroscopy. Similarly, one can assume that every dissociation event at the VL interface can deliver one semiconductor atom to the liquid catalyst without gas phase side reactions. Due to the low reaction pressure ($< \sim 10^{-4}$ Torr), the NW growth rate is inherently slow. Because of this slow growth rate, the sequential nucleation event is also slow for researchers to study other growth phenomena such as the origin of defect formation and kinking direction.

2.3.2 Ultra-high Chemical Vapor Deposition Reactor

The heterostructure study in Chapter 5 was conducted in a custom-built ultra-high vacuum chamber equipped with a Fourier Transform Infrared spectrometer. The small semiconductor wafer is loaded from a load lock chamber to a main chamber. Later, the NW growth occurs in a 12 inch-diameter spherical main chamber (McAllister Technical Services). The physical images of the main chamber are shown in Figure 2.3a while that of the load lock chambers are shown in Figure 2.3b.

a.

b.

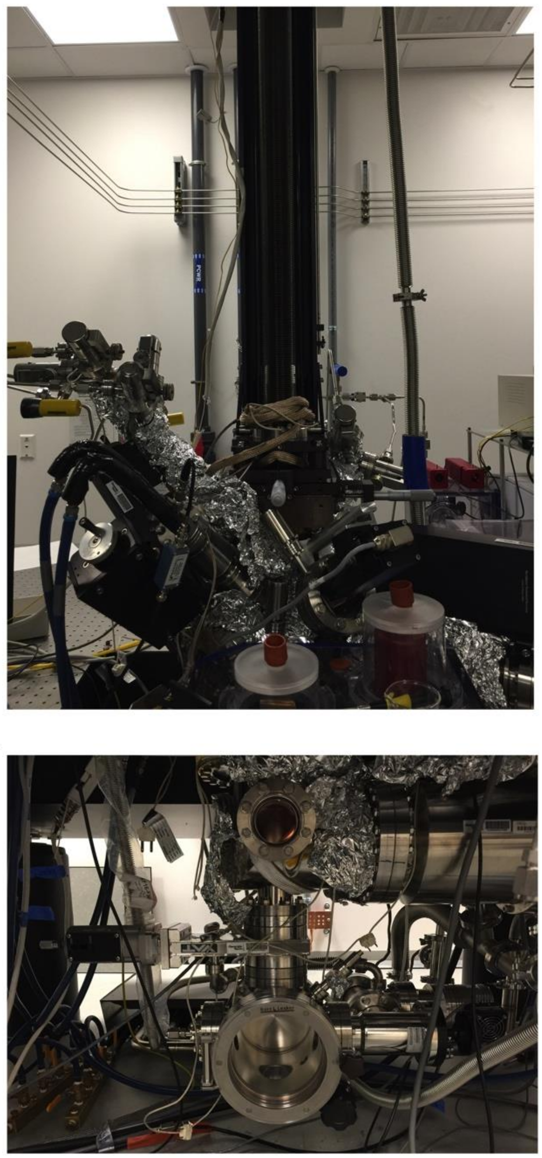

Figure 2.3. Photographs of the UHV-CVD furnace. (a). main chamber component, (b) load lock chamber component.

A 650 L/s magnetic levitation turbomolecular pump (Edwards, STP 603C) is connected with the main chamber to have a base pressure of 3×10^{-10} Torr while a 60 L/s turbomolecular pump (Edwards, EXT75DX) is connected with the load lock chamber to have a base pressure of 5.0×10^{-8} Torr. Both turbomolecuar pumps are backed by rotary vane mechanical pumps (Oerlikeon Leybold, and Edwards). A molybdenum (Mo) sample holder is used to secure and heat a small substrate above 1200 ^{o}C. A thermal evaporator (SVT Associate) deposits Au metal onto the pre-cut substrate. The metal film thickness is measured via a quartz crystal microbalance (Inficon). Two stainless dosers with variable leak valves deliver different precursors into the main chamber. Common precursors include Ge_2H_6 (Voltaix, 20% in He), Si_2H_6 (Voltaix, 99.998%), GeH_3CH_3 (Gelest, 97%), and H_2 (Airgas, 99.999%). All precursors are used without further purification.

2.3.3 Reaction Parameter Controls

Heating is achieved via direct resistive heating by flowing current. Substrate temperature is monitored by an infrared pyrometer (Mikron) focused on the back of the substrate. The pyrometer temperature measurement is calibrated by temperature programmed desorption (TPD) of an atomic hydrogen-saturated Ge(100) and Si(100) surface using a quadruple mass spectrometer (Hiden, HAL/3F 301 RC) and temperature dependent shifts of a Si-O peak position. The main and load lock chamber pressure is measured with two different ionization gauges (Duniway Stockroom) with a pressure measurement range from ~10^{-11} to 10^{-3} Torr. However, the NW growth pressure could be varied from ~10^{-5} to 10^{-2} Torr. Thus, the ionization gauge is turned off during NW growth after stabilizing the main chamber pressure to prevent filament damage. Similarly, pressure in the process lines with precursors is measured by convection gauges (Duniway Stockroom) with a pressure measurement range from ~10^{-3} to 10^{3} Torr.

2.3.4 *Substrate Preparation*

Initially, undoped and double side polished Ge (111) (MTI Corp. CZ) wafers are cut to prepare small substrates (0.6 cm × 2.4 mm). In order to eliminate contaminants and particles on the surface of the small substrates, they are chemically cleaned using a chemical procedure.[19] In the procedure, a layer of oxide is grown on the small substrate in 3 wt.% H_2O_2 (JT Baker, ACS Grade) for 1 minute followed by oxide layer strip in 9 wt.% HCl (JT Baker, CMOS Grade) for 30 seconds. Then, the substrate is rinsed by DI water and dried with N_2 gas. This procedure is repeatedly performed for at least 5 times. Finally, the substrate is immersed in 1:2:20 NH_4OH (Sigma-Aldrich, ACS Grade):H_2O_2: H2O solution for 1 minute to grow a thick oxide layer for protection followed by DI water rise and N2 gas dry.

After the wet treatment, the small substrate is loaded into the ultra-high vacuum CVD reactor. The substrate is then annealed to 485 °C for 35 min. At this high temperature, the thick oxide layer is desorbed from the substrate. The substrate is then cooled to room temperature followed by Ge thin film deposition at 305 °C with $P_{Ge2H6} = 2 \times 10^{-5}$ Torr. The thin film deposition can smooth and terminate the Ge surface with hydrogen atoms. Finally, high temperature annealing at temperature > 1000 °C to desorb the hydrogen atoms is followed by Au evaporation via electron-beam evaporation.

2.4 Semiconductor Nanowire Characterization

2.4.1 Scanning Electron Microscopy

SEM uses a packet of electrons to focus on the semiconductor wafer. The electrons carry significant energy with high velocity. Thus, due to the collision between the electrons and substrate, momentum can transfer from the electrons to eject electrons and release x-ray from the substrate. Detectors in SEM can collect these X-rays, backscattered electrons and secondary electrons as an input to reconstruct the surface topography on a screen. Generally, the small substrate with NWs are cloven in the center of the sample using a diamond scribe, mounted on SEM stubs via adhesive carbon tape, and characterized down the <110> zone axis in SEM.

2.4.2 Transmission Electron Microscopy

Similarly, TEM also uses a packet of electrons to focus on the semiconductor wafer. However, instead of diffracting the electrons during the collision, these electrons pass through a thin sample and are stopped by lattice bars in the TEM grid. These electrons can be collected as elastically scattered electrons, unscattered electrons, and inelastically scattered electrons. On the way though the thin sample, these electrons can be stopped or deflected, corresponding with the dark region on the image. When the electrons are unscattered, the region on the image would be brighter. NW structures are analyzed with a FEI Tecnai F20 transmission electron microscope (TEM). For the (S)TEM-based measurements, NWs are transferred to carbon-coated grids (Ted Pella) by a direct mechanical transfer method.[20] HRTEM images are obtained with a 0.19 nm point-to-point resolution at 200 keV.

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CHAPTER 3. SOLID-LIQUID-VAPOR ETCHING OF SEMICONDUCTOR NANOWIRES

3.1 Introduction

Selective chemical etch processes leverage crystal structure- and/or composition-dependent etch rates to create a range of micro- and nano-scale structures.[1-5] The addition of metals to semiconductor surfaces is a common method of inducing etch selectivity. Metal-assisted chemical etching (MACE), whereby the rapid oxidation (and subsequent etch) of atoms at metal/semiconductor interfaces results in NWs, is one of the most well-known techniques.[6, 7] Several decades earlier Wagner demonstrated an analogous, yet chemically distinct, process to create low aspect ratio holes on Au-decorated Ge substrates with gaseous HCl.[8] The process was proposed to occur via a solid-vapor-liquid (SLV) mechanism. HCl removes Ge from the AuGe eutectic catalyst droplet, undersaturating the catalyst and driving dissolution of Ge atoms from the substrate. More recently, Wallentin *et al.* and O'Toole *et al.* reported analogous processes where HCl and Cl_2 etched Au-decorated InP and Si substrates, respectively.[9, 10]

Vapor-liquid-solid (VLS) synthesis takes advantage of selective precursor decomposition at a metal catalyst droplet to enable the bottom-up fabrication of semiconductor NWs. These materials show promise as a building block for next generation electronic, photonic, and energy conversion devices.[11-15] The catalyst state is central to VLS NW growth. Controlling catalyst droplet composition, by adding atoms of various types, can influence growth rate, crystal structure, and/or dopant profile.[16-20] A reverse process, the scavenging of atoms from the catalyst droplet, has also been hypothesized. While such a process has been suggested as an explanation for diameter-dependent NW growth[21] and as a route to suppress the reservoir effect,[22] a definitive observation is still lacking.

Here, we use a dicarbonyl, specifically 2,3-butanedione (BD), to induce the *anisotropic chemical* etching of Ge NWs via a SLV mechanism.[23] The term “anisotropic” etching is used since our process acts only in the axial direction and does not impact the NW sidewall. We describe the process as “chemical” since precursors react with and remove Ge atoms from the catalyst droplet, which is quite distinct from reports of NW dissolution via evaporation at high temperature.[24, 25] The well-known ability of dicarbonyls to chelate a range of metal atoms, including beryllium, zinc, and copper,[26-28] informed the selection of BD as a precursor potentially capable of binding to and removing atoms from the catalyst.

3.2 Experiment Details

Ge NWs are synthesized with Au nanoparticle catalyst seeds in a cold wall chemical vapor deposition reactor (FirstNano, Easy Tube 3000) described previously.[29] Single-side polished Ge(111) wafers (MTI Corporation, CZ, 42-64 Ω-cm) are cleaned via immersion into 10% HF (J.T. Baker). The substrates are subsequently dipped into a citrate-stabilized Au colloid suspension (Ted Pella) containing 0.1 M HF.[30] Colloid diameters of 30, 40, 50, 60, and 80 nm are used in this work. The substrate is removed after 5 min, rinsed with 10% HF and deionized water, dried with nitrogen, and immediately transferred to the growth reactor. Susceptor temperature is calibrated with a

K-type thermocouple embedded in a Si wafer (Thermo Electric). Germane (GeH_4, 99.999%, Matheson Tri-Gas), trimethylsilane (TMS, 99.99%, Voltaix), argon (Ar, 99.999%, Air Products) are used without further purification and are delivered with the flow rates indicated in the text. 2,3-Butanedione (BD, 99.0%, Fisher Scientific) is purified via multiple freeze-pump-thaw cycles and delivered via Ar bubbling. BD flow rate refers to that of the Ar carrier gas. The total reactor pressure is fixed at 7 Torr for all experiments. NW morphology is analyzed with a Hitachi SU-8230 field emission scanning electron microscope (SEM). Each data point results from measurements of 50 individual NWs to obtain meaningful statistics. All error bars indicate one standard deviation from the mean.

3.3 Results and Discussion

We quantify etch rate as described below and as illustrated in Figures 3.1a-d. Ge NWs containing two identical, tapered segments, each with a length L_{ref}, are initially grown. The first segment (i.e., closest to the substrate) serves as a reference from which to accurately measure the length of the second segment (i.e., closest to the catalyst droplet) that remains after etching, L_{post}. Etch length, L_{etch}, can then be readily determined via $L_{etch} = L_{ref} - L_{post}$. A similar procedure has been used by our group to determine NW growth rate.[31] A short base segment is initially grown at 370 °C with 25 sccm GeH_4 and 625 sccm Ar for 2 min (Figure 3.1a). The base sidewall is passivated to suppress subsequent vapor-solid deposition, as previously reported, by flowing TMS at 8 sccm and Ar at 642 sccm for 2 min at the same temperature in the absence of GeH_4. The first tapered segment is elongated with 25 sccm GeH_4 and 625 sccm Ar for 5 mins (Figure 3.1b). Elongation temperatures are either 360, 370, or 380 °C and are selected to match the subsequent etch temperature. After passivating the sidewall of the first segment with TMS, using the same precursor flow rates as the base, a second tapered segment is grown (Figure 3.1c). The TMS exposure induces a diameter expansion upward and downward from the liquid-solid interface, creating a sharp corner as a morphological maker in Figure 3.2. NW etching is initiated by introducing BD immediately after growing the second segment, at the same substrate temperature, and without an intervening TMS introduction (Figure 3.1d). While the lengths of the two tapered segments are identical within the error of measuring length via SEM images in Figure 3.3, any uncertainty in initial segment lengths is substantially less than the etched length. While surface roughening is observed on the first segment (i.e., closest to the substrate) after growth of the second, an effect we attribute to the imperfect passivation of the sidewall by TMS,[30] it is unlikely to impact Ge atom removal at the catalyst droplet (*vide infra*).

Figure 3.1e shows a representative Ge NW array etched for 120 s with 8 sccm BD, 5 sccm GeH_4, and 637 sccm Ar at 370 °C. NW etching occurs only at the catalyst-NW interface, only in the <111> direction, and is uniform across large substrate areas. The crystal direction selectivity observed here is quite distinct from previous reports of metal-catalyzed etching of semiconductor substrates with HCl and Cl_2, where etching occurs in multiple degenerate crystal directions simultaneously.[9, 10] A comparison of Figures 3.1e, 3.2b and 3.3 shows that the sidewall morphology is unaffected by BD. We rarely observe NWs where the catalyst droplet unpins from the top-facet during etching. The observation of a flat top facet and a catalyst droplet that no longer extends to the NW sidewalls, as shown in the inset of Figure 3.1e, is also interesting. It suggests, within the limitations of an *ex situ*, post-growth structure measurement, that the catalyst droplet migrates on the top facet at a rate faster than the etch rate. Indeed, rapid movements of the catalyst droplet have recently been observed with *in situ* transmission electron microscopy.[32]

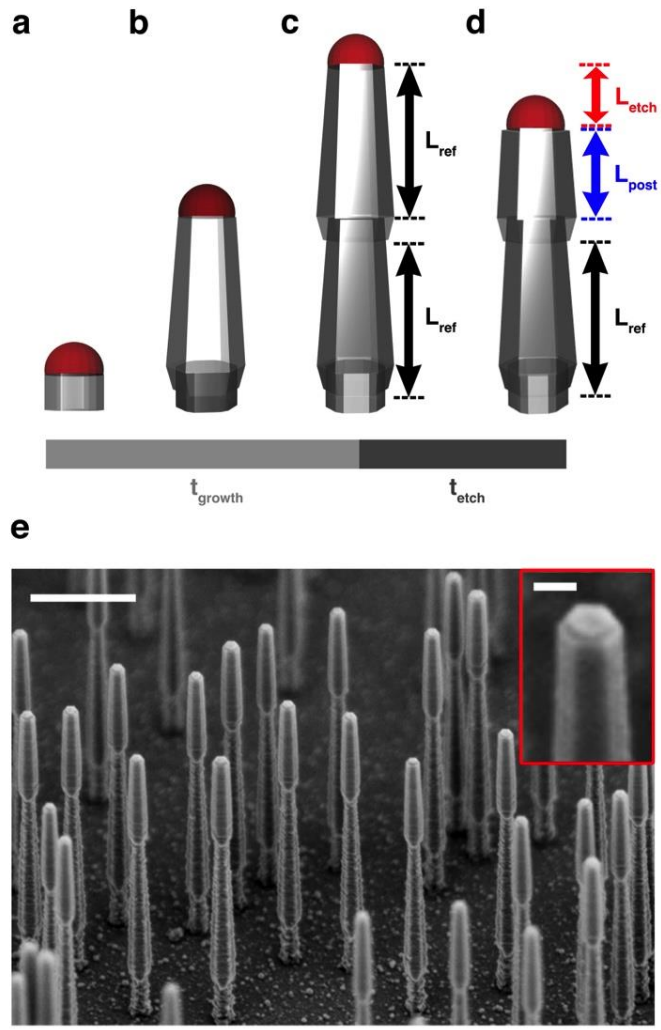

Figure 3.1. Schematic illustration of nanowire synthesis and subsequent etching procedure. (a) A short base is initially grown and passivated via TMS exposure. (b) The first of two identical tapered segments, used as an internal reference, is then grown and also passivated with TMS. (c) The second tapered segment, which will be subsequently etched, is then grown with the same conditions as the first. (d) BD exposure results in nanowire etching. L_{ref} and L_{post} are measured as indicated to determine $L_{etch} = L_{ref} - L_{post}$. (e) SEM images of a representative Ge nanowire array etched with 8 sccm BD, 5 sccm GeH_4, and 637 sccm Ar at 370 °C for 120 s. Scale bar, 500 nm. Inset: SEM image of the near-catalyst region. Scale bar, 50 nm.

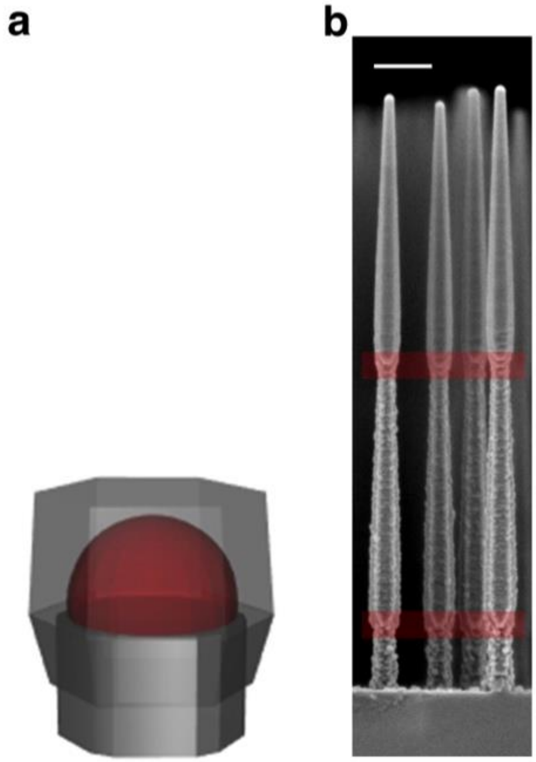

Figure 3.2. (a). TMSH induces a diameter expansion upward and downward from the liquid-solid interface, creating a sharp corner as a morphological maker. The location of the sharp morphological marker is the same as that of the red Au liquid catalyst at the growth front before NW elongation. (b). The diameter expansion occurs at the base of the reference and pre-etch segments where the TMSH is induced during growth. Scale bars, 200 nm.

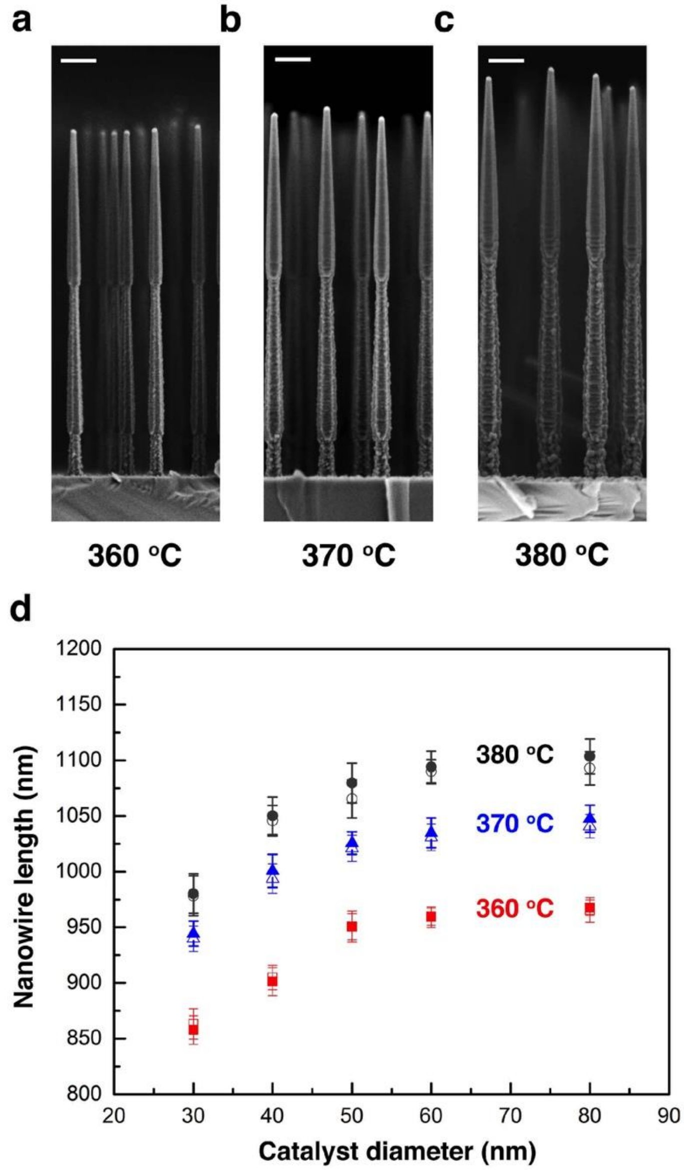

Figure 3.3. Cross-sectional SEM images of representative Ge nanowires grown at (a) 360 ºC, (b) 370 ºC, and (c) 380 ºC prior to BD introduction. Scale bars, 200 nm. (d) Comparison of initial bottom (i.e., reference, open symbols) and top (i.e., subsequently etched, solid symbols) segments lengths as a function of catalyst diameter and growth temperature.

Figure 3.4a shows the time-dependence of Ge NW etching for 8 sccm BD, 5 sccm GeH_4, and 637 sccm Ar at 370 °C. The SEM images clearly show that as time increases, the value of L_{etch} (= L_{ref} - L_{post}) increases. Figure 3.4b reveals that the dependence of L_{etch} on time is non-linear. Since the NW diameter increases away from the catalyst (i.e., due to the intentional sidewall taper), more Ge atoms must be removed per etched bilayer as the etch proceeds. We account for this effect by treating the tapered segment as a frustum and calculating the etched volume or, equivalently, the number of Ge atoms removed (volumetric density = 44.12 atoms/nm^3 for diamond cubic Ge). To permit this calculation, we use SEM to determine L_{etch} as well as NW diameter at the catalyst-NW interface, bottom of the first segment, and bottom of the second segment after etching. The result is plotted in Figure 3.4b and shows that the number of Ge atoms (ΔN_{Ge}) etched increases linearly with time. The etch rate can be determined from the slope and is ~3.40 × 10^5 Ge atoms/s for this etch condition.

Etching experiments as a function of catalyst droplet diameter, BD flow rate, and substrate temperature provide insight into the etch mechanism. Figure 3.5a shows that L_{etch} increases as a function of catalyst diameter when flowing BD for 60 s at the same conditions used in Figure 3.4a. Figure 3.5b shows a linear dependence of etch rate on the catalyst diameter squared, consistent with the etching model presented below. Figure 3.6 shows how varying the flow rate of the BD impacts etch rate. The etch rate is linear with BD flow rate for flow rates below ~25 sccm. At higher BD flow rates, the etch rate begins to plateau. This trend is consistent with an Eley-Rideal mechanism[33-35] whereby BD removes Ge atoms via reaction at the VL interface. At low to moderate flow rates, increasing the VL interface coverage of BD molecules leads to more rapid etching. Since the VL interface can only accept a finite number of BD molecules, the interface coverage of BD and thus etch rate must eventually plateau. Figures 3.5 and 3.6 hint that an inverse relationship between etch rate and temperature may be present. While this behavior is sometimes observed for gas-phase etch processes,[36, 37] the error in our measurement prevents any definitive conclusions to be drawn at the present time.

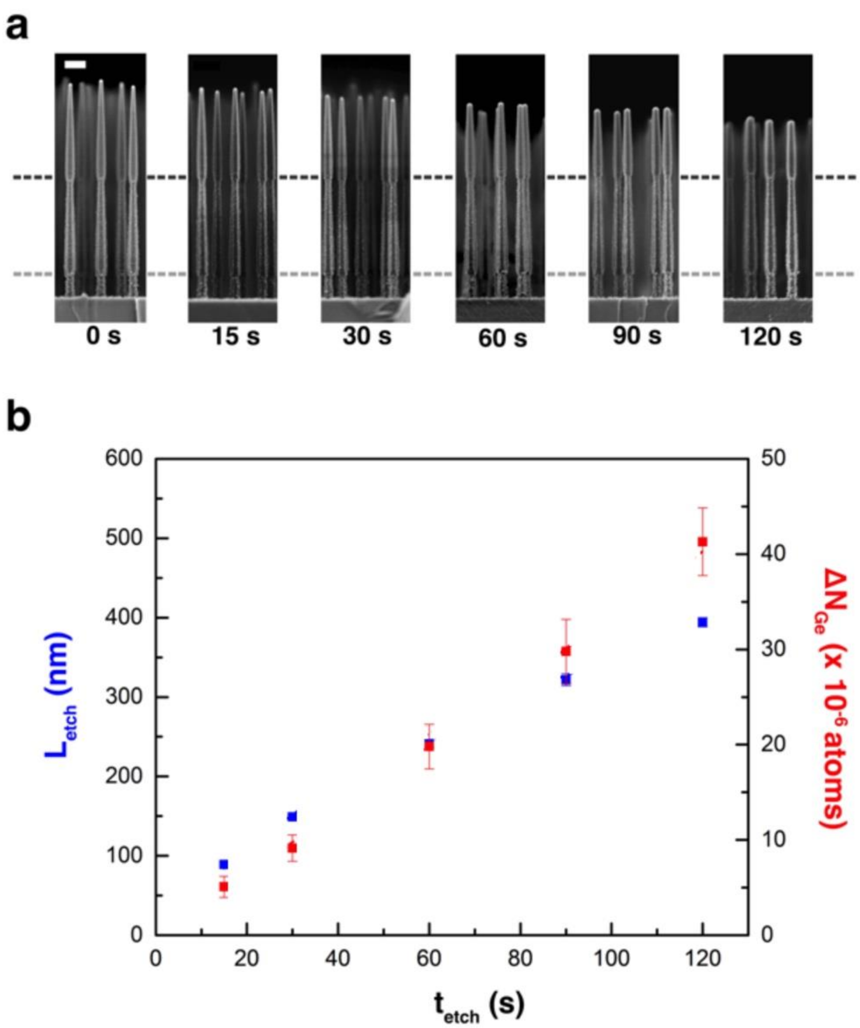

Figure 3.4. (a) Cross sectional SEM images of representative Ge nanowire arrays etched with 8 sccm BD, 5 sccm GeH_4, and 637 sccm Ar at 370 °C for 0, 15, 30, 60, 90, and 120 s. Scale bar, 200 nm. (b) Etch length (L_{etch}, left) and number of Ge atoms removed from the nanowire (ΔN_{Ge}, right) plotted as a function of etch time. The dashed lines are a least squares fit to the data.

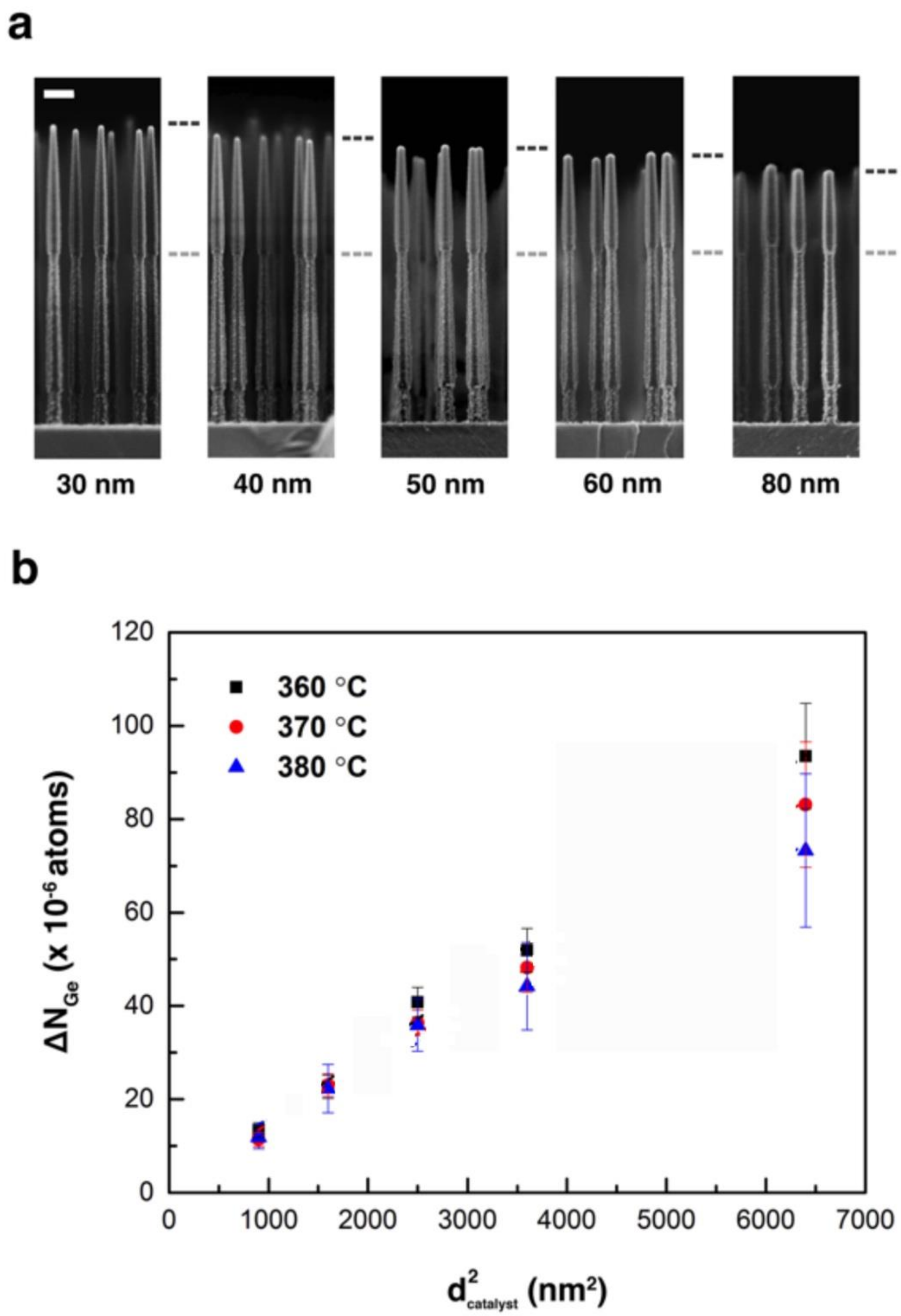

Figure 3.5. (a) Cross sectional SEM images of representative Ge nanowire arrays grown with different Au nanoparticle diameters and etched with 8 sccm BD, 5 sccm GeH_4, and 637 sccm Ar at 370 °C for 60 s. Scale bar, 200 nm. (b) Number of Ge atoms removed from the nanowire (ΔN_{Ge}) as a function of initial nanoparticle diameter squared at 360, 370, and 380 °C.

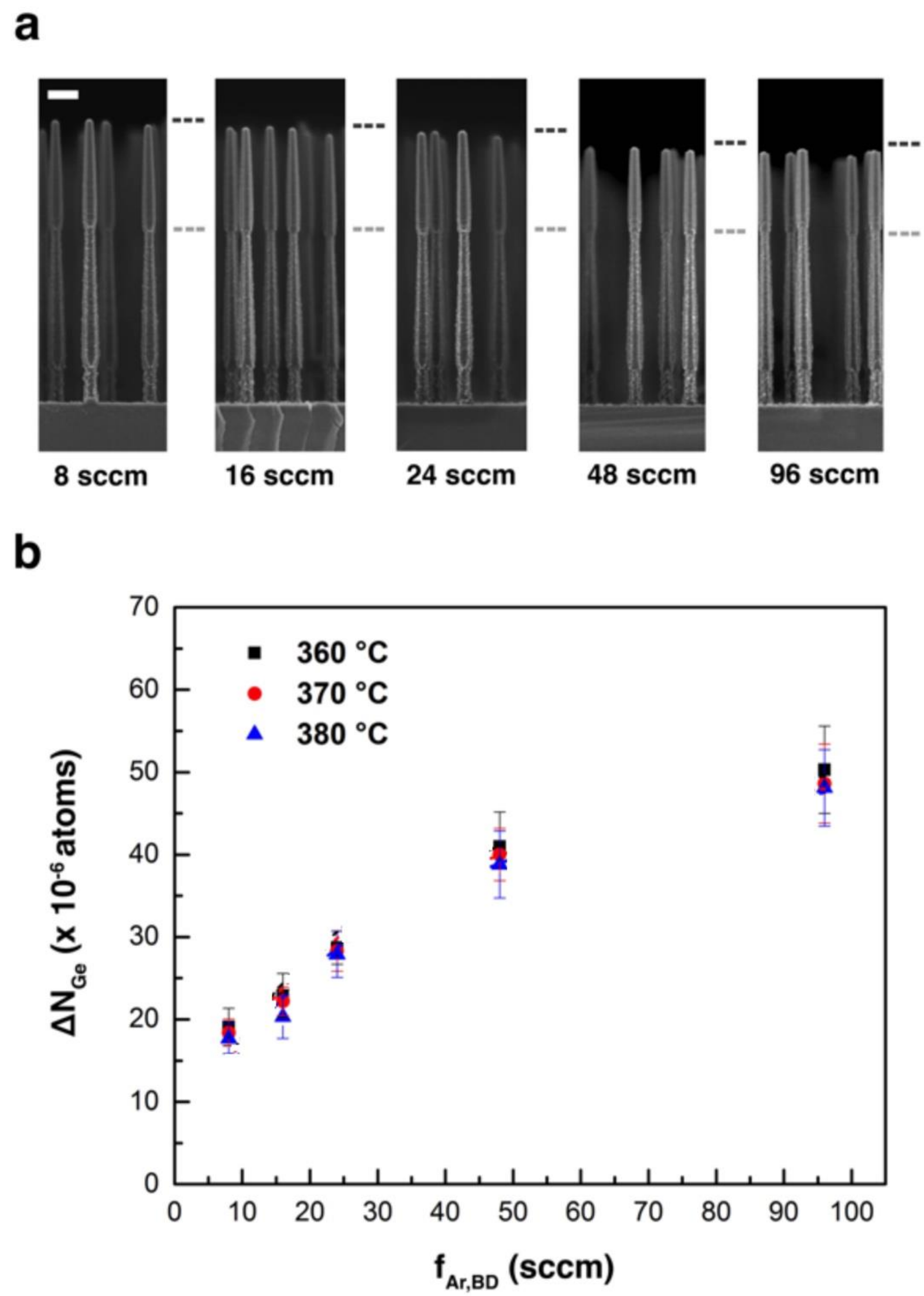

Figure 3.6. (a) Cross sectional SEM images of representative Ge nanowire arrays grown with 30 nm Au nanoparticles and etched with 5 sccm GeH_4, 637 sccm Ar, and the indicated flow rates of Ar through the BD bubbler at 370 °C for 60 s. Scale bar, 200 nm. (b) Number of Ge atoms removed from the nanowire (ΔN_{Ge}) as a function Ar flow rate through the BD bubbler ($f_{Ar,BD}$) at 360, 370, and 380 °C.

3.4 Conclusion

Semiconductor NWs synthesized by bottom-up techniques are promising materials for next generation electronic, photonic, and energy conversion devices because one can add multiple functionalities along the NW length. To achieve this, however, temperature and gas phase composition must be modulated multiple times during growth. These changes frequently result in graded composition profiles that are undesirable in many applications. Here, we demonstrate anisotropic *in situ* etching of semiconductor NWs, a process that permits the removal of these transition regions. Ge NWs are first synthesized via the vapor-liquid-solid technique with a eutectic Au-Ge catalyst at 370 ^{o}C and a GeH_4 partial pressure of 0.27 Torr. An intentional diameter expansion near the NW base serves as an internal reference point to accurately measure etch rate. The introduction of BD at a partial pressure of 0.0035 Torr initiates etching selectively from the eutectic catalyst. We find that the atomic etch rate is constant regardless of sidewall taper. Furthermore, we study this etching behavior as a function of temperature, BD partial pressure, and NW diameter. In conclusion, we demonstrate and quantitatively characterize the anisotropic etching of semiconductor NWs. Our data supports an etching process with BD-induced Ge atom removal. The SEM characterization clearly shows that Ge atoms are removed along the NW. The NW sidewall morphology has not been modified after the etching.

Our demonstration confirms a long-term speculation about gas-phase etching without plasma in semiconductor NWs. However, these interfacial reactions underneath the chemical etching are so complex that additional kinetic analysis is required. The analysis helps researchers establish a rational reaction path about the atomic/molecular interaction and movement. Here, the experimental data from Chapter 3 serves as the essential basis for the analysis that will be presented in Chapter 4.

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CHAPTER 4. KINETIC MODEL OF SELECTIVE SOLID-LIQUID-VAPOR ETCHING OF SEMICONDUCTOR NANOWIRES

4.1 Introduction

The synthesis of complex, functional objects, at any length scale, requires the synergistic combination of additive, subtractive, and patterning “process” steps. Tremendous effort has been devoted to the additive (i.e., bottom-up) processing of nanoscale structures, but their directed subtraction and patterning remain largely unexplored. Previously, we demonstrate a new process for the former – the selective removal of atoms from semiconductor NWs. 2,3-butanedione selectively extracts Ge atoms from the eutectic catalyst droplet, which results in undersaturation and dissolution of Ge from the solid NW. Experiments as a function of substrate temperature, etchant flow rate, and NW diameter support a SLV mechanism. We proposed a model to describe the mechanism with macroscopic process path and microscopic reaction scheme at VL, LS, and VS interfaces. The model of the process with reaction at the LV interface as the rate-limiting step is consistent with our experiments. These findings show how subtractive techniques can tune the structure of semiconductor NWs and also indicate a new route to enable atomically abrupt dopant profiles and heterointerfaces.

4.2 Kinetic Model, Results and Discussion

Our experiments support a SLV etch process. We now develop material balances, based on the inputs and outputs shown in Figure 4.1a, to model NW etch rate as a function of process parameters. We assume that BD only removes Ge atoms (i.e., no Au atoms), the catalyst droplet's curvature does not impact the etch process (i.e., there is no Gibbs contribution),[1] and that Ge atom crystallization and dissolution are continuous processes. For this situation, the number of Ge atoms in the catalyst droplet can decrease via crystallization at the LS interface, increase via dissolution of the NW at the LS interface, or decrease via BD-driven removal at the VL interface:

$$\frac{dn_{Ge,cat}}{dt} = -k_c(C_{Ge} - C_{Ge,e})A_{LS} + k_d(C_{Ge,e} - C_{Ge})A_{LS} + R_{removal}A_{VL} \quad (4.1)$$

where $n_{Ge,cat}$ is the number of moles of Ge in the catalyst droplet, k_c is the crystallization rate constant, k_d is the dissolution rate constant, $C_{Ge,e}$ is the equilibrium concentration of Ge in the catalyst droplet, C_{Ge} is the concentration of Ge in the catalyst droplet, A_{LS} is the

LS interfacial area, A_{VL} is the VL interfacial area, $R_{removal}$ is the rate of BD-driven Ge atom removal at the VL interface, and t is time. Ge atoms can be added to or removed from the NW via crystallization or dissolution at the LS interface, respectively:

$$\frac{dn_{Ge,NW}}{dt} = k_c(C_{Ge} - C_{Ge,e})A_{LS} - k_d(C_{Ge,e} - C_{Ge})A_{LS} \quad (4.2)$$

where $n_{Ge,NW}$ is the number of moles of Ge in the NW. Combining Eqs. 4.21 and 4.22, assuming the number of moles of Ge atoms in the catalyst droplet is constant, yields:

$$\frac{dn_{Ge,NW}}{dt} = R_{removal} A_{VL} \tag{4.3}$$

The kinetic rate law for Ge removal at the VL interface, $R_{removal}$, must be known before solving for the NW etch rate. Figure 4.1b illustrates a Eley-Rideal mechanism consisting of the following elementary steps: (i) reversible BD adsorption to create an interface-bound intermediate (BD*); (ii) irreversible reaction of BD* with Ge atoms in the catalyst droplet to form an interface-bound etch product (BD-Ge*); and (iii) reversible desorption of the final etch product (BD-Ge). The constituent chemical reactions can be written as follows:

$$BD(g) + * \underset{k_{-1}}{\overset{k_1}{\rightleftarrows}} BD* \tag{4.4}$$

$$BD* + Ge(l) \xrightarrow{k_2} BD - Ge* \tag{4.5}$$

$$BD - Ge* \underset{k_{-3}}{\overset{k_3}{\rightleftarrows}} BD - Ge(g) + * \tag{4.6}$$

where k_1 and k_{-1} are the rate constants for BD adsorption and desorption at the VL interface, respectively; k_2 is the rate constant for BD-Ge* formation; k_3 and k_{-3} are the rate constants for BD-Ge desorption and adsorption at the VL interface, respectively. * denotes an open site at the VL interface. For this situation, the overall Ge removal rate is:

$$R_{removal} = -k_2 C_{BD*} C_{Ge} \tag{4.7}$$

where C_{BD*} is the concentration of adsorbed BD molecules at the VL interface and C_{Ge} is the concentration of Ge atoms in the catalyst droplet. Eq. 4.7 assumes that Eq. 4.5 is irreversible and rate-limiting. From Eq. 4.4, assuming equilibrium, the concentration of BD* at the VL interface (C_{BD*}) is:

$$C_{BD*} = \frac{K_1 P_{BD} C_*}{RT} \tag{4.8}$$

where $K_1 = k_1/k_{-1}$, C_* is the concentration of surface sites, P_{BD} is the partial pressure of BD, R is the universal gas constant, and T is the absolute temperature. Analogously, we can express the concentration of the etch product bound to the VL interface ($C_{BD\text{-}Ge*}$), using Eq. 4.6, as:

$$C_{BD-Ge*} = \frac{P_{BD-Ge} C_*}{K_3 RT} \tag{4.9}$$

where $K_3 = k_3/k_{-3}$ and $P_{BD\text{-}Ge}$ is the partial pressure of BD-Ge. A site balance on the VL interface yields:

$$C_{*,0} = C_* + C_{BD*} + C_{BD-Ge*} \tag{4.10}$$

where $C_{*,o}$ is the total number of surface sites. Substituting Eqs. 4.8 and 4.9 into 4.10 and rearranging yields:

$$C_* = \frac{C_{*,0}}{\left(1 + \frac{K_1 P_{BD}}{RT} + \frac{P_{BD-Ge}}{K_3 RT}\right)} \tag{4.11}$$

The final rate equation is obtained by combining Eqs. 4.7, 4.8, and 4.11:

$$R_{removal} = -\frac{K_1 k_2 P_{BD} C_{Ge} C_{*,0}}{RT\left(1 + \frac{K_1 P_{BD}}{RT} + \frac{P_{BD-Ge}}{K_3 RT}\right)} \tag{4.12}$$

where $K_1 = k_1/k_{-1}$, $C_{*,0}$ is the total number of VL interface sites, P_{BD} is the partial pressure of BD, $P_{BD\text{-}Ge}$ is the partial pressure of the BD-Ge etch product, R is the universal gas constant, and T is the absolute reaction temperature.

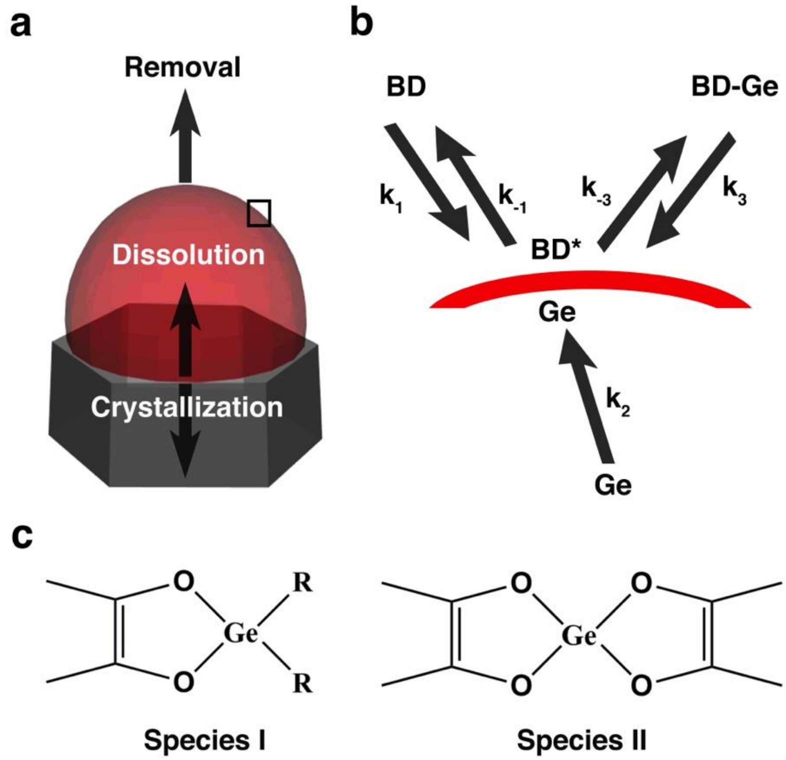

Figure 4.1. (a) Overview of the key processes in the etch model: crystallization and dissolution of Ge atoms at the liquid-solid (LS) interface as well as Ge atom removal at the vapor-liquid (VL) interface. (b) Illustration of the elementary VL interface reactions: (1) reversible adsorption of BD, (2) irreversible reaction of BD with Ge atoms in the catalyst droplet, and (3) reversible desorption of the etch product into the gas phase. (c) Chemical structures of two potential etch products.

The number of moles of Ge atoms removed from the NW as a function of time can be determined by assuming the catalyst droplet is a hemispherical cap and inserting Eq. 4.12 into Eq. 4.3:

$$\frac{dn_{Ge,NW}}{dt} = -\frac{K_1 k_2 P_{BD} C_{Ge}\ C_{*,0}\left(\frac{\pi d^2}{2}\right)}{RT\left(1 + \frac{K_1 P_{BD}}{RT} + \frac{P_{BD-Ge}}{K_3 RT}\right)} \tag{4.13}$$

where d is the diameter of the catalyst droplet. The partial pressure of BD can be written in terms of the flow rate of Ar through the BD bubbler as:

$$P_{BD} = \frac{\eta f_{Ar,BD}}{f_{total}} P_{total} \tag{4.14}$$

where η is the efficiency of BD vaporization per unit of Ar mass flow, $f_{Ar,BD}$ is the mass flow rate of Ar through the BD bubbler, f_{total} is the total mass flow rate, and P_{total} is the total pressure. Substituting Eq. 4.14 into Eq. 4.13, integrating over time, and converting to atomic units yields the number of Ge atoms etched from the NW, $\Delta N_{Ge,NW}$:

$$\Delta N_{Ge,NW} = -\frac{N_A K_1 k_2 \eta f_{Ar,BD} P_{total} C_{Ge} C_{*,0}\left(\frac{\pi d^2}{2}\right)}{RTf_{total}\left(1 + \frac{K_1 P_{BD}}{RT} + \frac{P_{BD-Ge}}{K_3 RT}\right)} t_{etch} \tag{4.15}$$

where N_A is Avogadro's number and t_{etch} is the etch time. Assuming the partial pressure of BD-Ge is low due to its continuous removal via the pump, Eq. 4.15 simplifies to:

$$\Delta N_{Ge,NW} = -\frac{A f_{Ar,BD} t_{etch} d^2}{\left(1 + B f_{Ar,BD}\right)} \tag{4.16}$$

where A and B are constants defined as:

$$A = \frac{N_A K_1 k_2 \eta P_{total} C_{Ge} C_{*,0} \left(\frac{\pi}{2} \right)}{f_{total} RT} \tag{4.17}$$

$$B = \frac{K_1 \eta P_{total}}{f_{total} RT} \tag{4.18}$$

A and B are determined by fitting the data in Figure 4.2. Table 4.1 tabulates these values at each temperature. Excellent agreement between the model and experiment is observed in Figures 4.3-4.4. Figure 4.5a shows NW etch rate for any combination of d and $f_{Ar,BD}$ values at 370 °C.

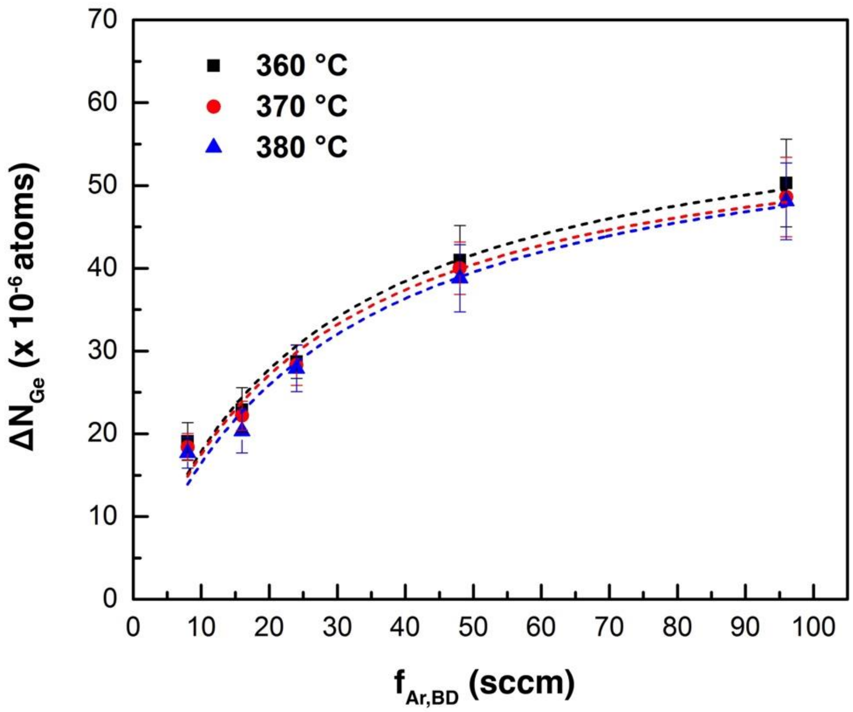

Figure 4.2. Number of Ge atoms removed from the nanowire (ΔN_{Ge}) as a function of Ar flow rate through the BD bubbler ($f_{Ar,BD}$) at 360, 370, and 380 °C. The dashed lines are fits to our etch model.

Table 4.1. Values of Constants *A* and *B* in the Etch Model

Reaction Temperature (°C)	A ($\times 10^{-5} \frac{atoms}{nm^2 sccm}$)	B ($\times 10^{-2}\, sccm^{-1}$)
360	4.64	3.72
370	4.57	3.43
380	4.17	3.32

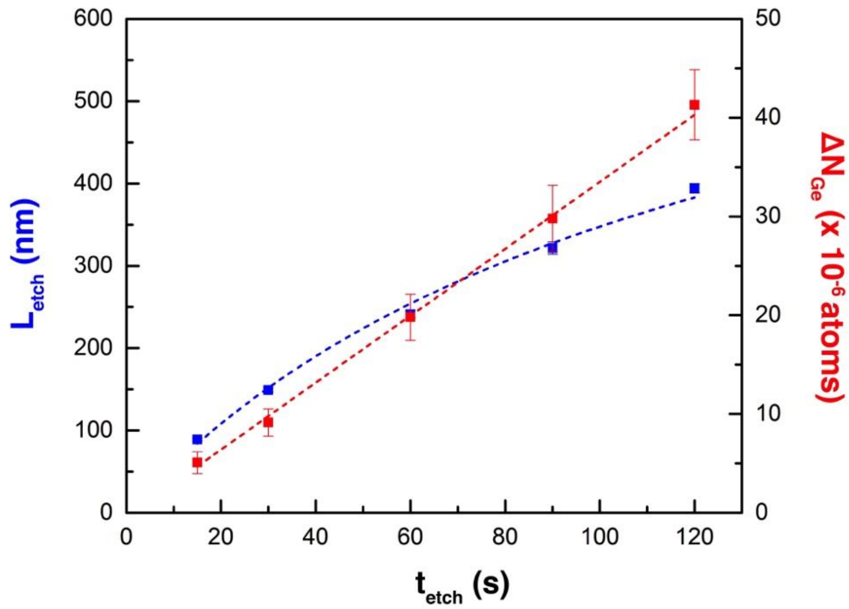

Figure 4.3. Etch length (L_{etch}, left) and number of Ge atoms removed from the nanowire (ΔN_{Ge}, right) plotted as a function of etch time. The dashed lines are fits to our etch model.

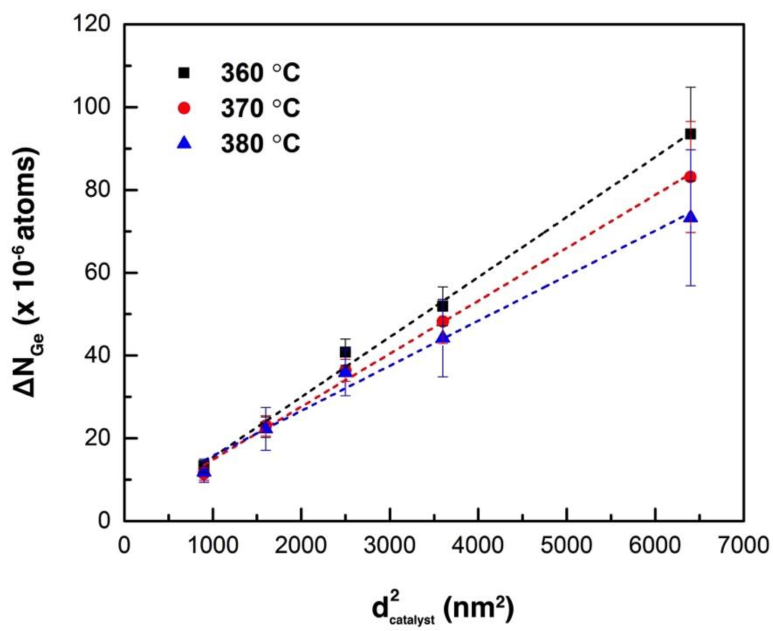

Figure 4.4. Number of Ge atoms removed from the nanowire (ΔN_{Ge}) as a function of initial nanoparticle diameter squared at 360, 370, and 380 °C. The dashed lines are fits to our etch model.

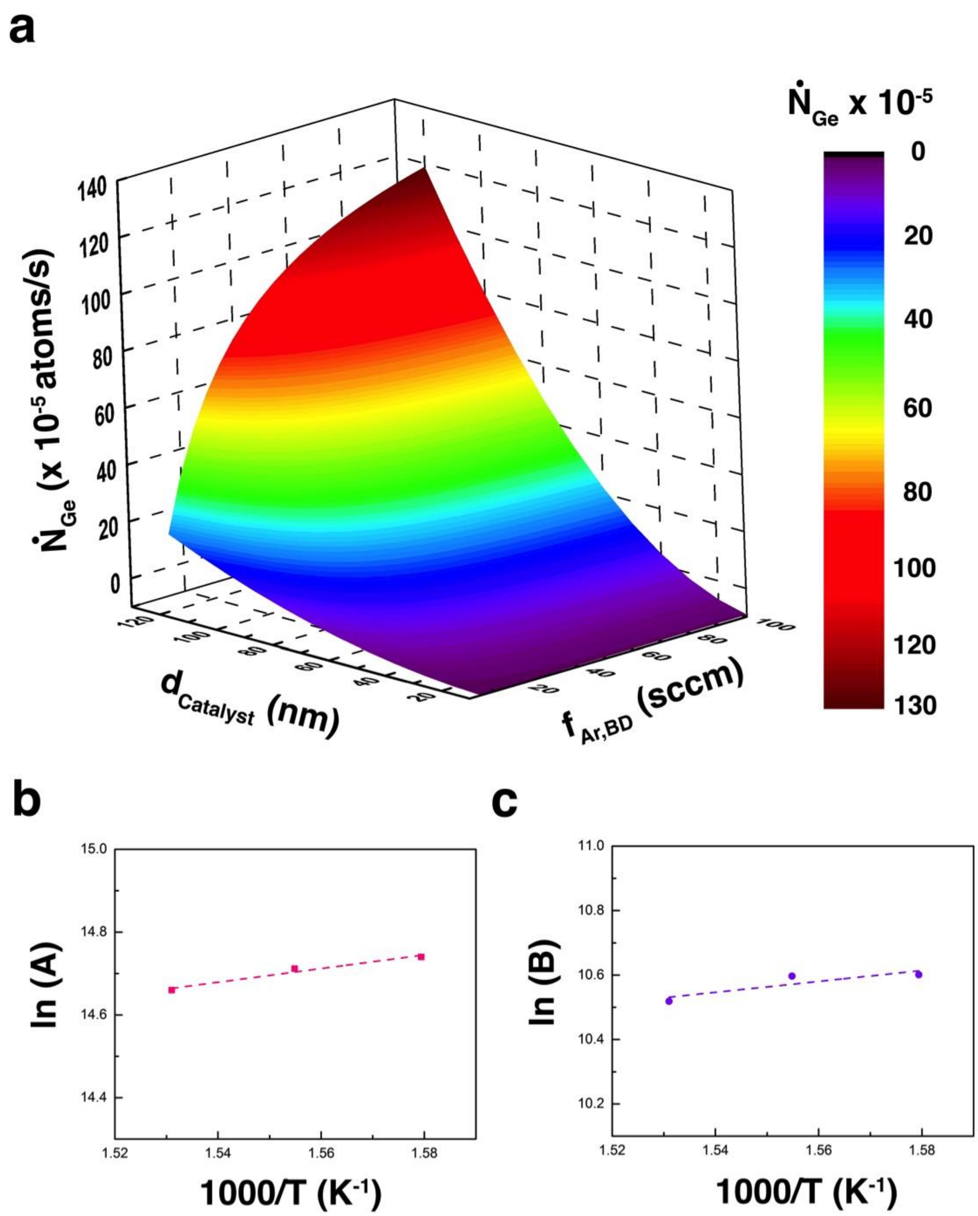

Figure 4.5. (a) Nanowire etch rate predicted from the full model as a function of *d* and $f_{Ar,BD}$ at 370 °C. (b,c) Arrhenius plots allowing apparent activation energies for the constants A and B to be extracted. The data for these plots comes from Table 4.1.

Our kinetic analysis also provides valuable insight into the observed temperature dependence and elementary reactions. Foremost, the constant A is proportional to the following collection of elementary rate constants:

$$A \propto \frac{k_1 k_2}{k_{-1}} \tag{4.19}$$

Assuming each elementary rate constant exhibits an Arrhenius dependence, an apparent activation energy, $E_{A,app}$, can be extracted:

$$E_{A,app} = E_1 - E_{-1} + E_2 \tag{4.20}$$

where E_1 is the activation energy for BD adsorption to the VL interface, E_{-1} is the activation energy for BD desorption from the VL interface, and E_2 is the activation energy for the BD-Ge* formation reaction. An analogous apparent activation energy, $E_{B,app}$, can be extracted from the constant B:

$$E_{B,app} = E_1 - E_{-1} \tag{4.21}$$

We find, as determined via the Arrhenius plots in Figures 4.5b and 4.5c, that the values of $E_{A,app}$ and $E_{B,app}$ are -3.28 and -3.36 kcal/mol, respectively. Negative apparent activation energies are consistent with the inverse temperature dependence seen in Figures 4.2 and 4.4. This result also implies that the value of E_2 is near zero, which indicates that nearly all collisions between Ge atoms and BD* with the correct orientation will result in BD-Ge* formation. This step can still be rate limiting, despite its low activation barrier, since the concentration of BD at the VL interface, C_{BD*}, is low (Eq. 4.7).

We propose that the etch product (BD-Ge) is one of the chelated species shown in Figure 4.1c. One or two BD molecules may react with a Ge atom to yield product I or II, respectively. A dicarbonyl species similar to BD, hexafluoroacetylacetone, is known to etch Cu films and a similar chelation reaction has been hypothesized.[2] The formation of at least two Ge-O bonds, each with a bond strength of ~14-17 kcal/mol,[3] supports the assumption that the interface reaction is irreversible. A number of factors support Species I as the etch product. Foremost, continuous NW etching requires a GeH_4 coflow. If GeH_4 flow is terminated immediately after tapered segment growth, the etch process begins but quickly ceases in Figure 4.6. (For this reason, we maintained a GeH_4 flow rate of 5 sccm in all of the above-described etching experiments.) We hypothesize that hydrogen atoms from the heterogeneous decomposition of GeH_4 combine with a Ge atom and BD to form species I. The lower molecular weight of this species (i.e., relative to II) and thus higher vapor pressure would also offer a higher etch rate. Additionally, the etch rate decreases linearly as a function of GeH_4 flow rate in Figure 4.7, a situation we attribute to a reduced degree of catalyst droplet undersaturation with Ge addition.

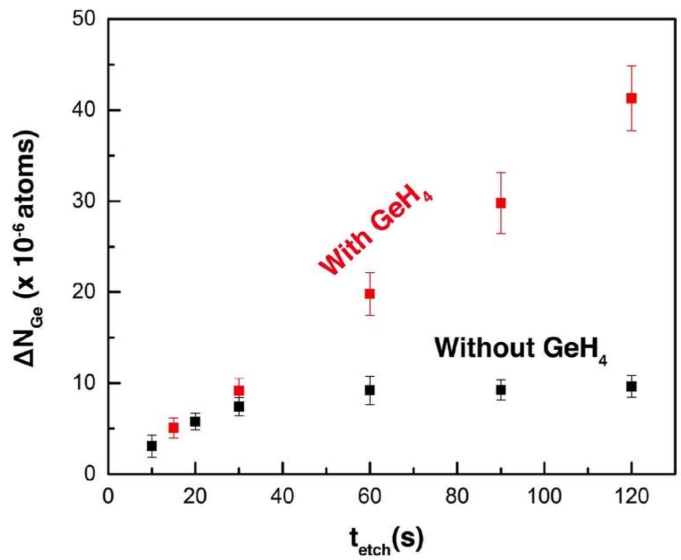

Figure 4.6. Number of Ge atoms removed from the nanowire (ΔN_{Ge}) as a function of etch time with and without coflowing 5 sccm GeH_4 during etching. The etch terminates in the absence of GeH_4.

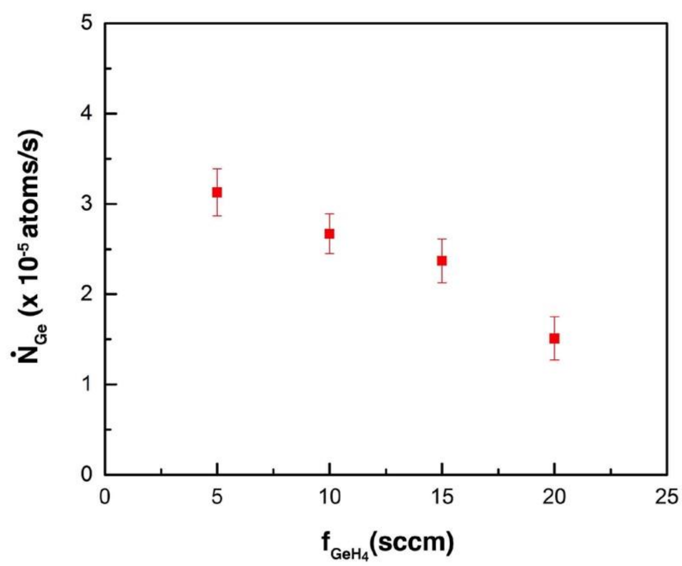

Figure 4.7. Nanowire etch rate as a function of GeH_4 coflow rate during etching.

4.3 Conclusion

In conclusion, our data supports a solid-liquid-vapor (SLV) etch process with BD-induced Ge atom removal at the VL interface. Despite treating Ge atom dissolution as continuous in our model, it is well known that bilayer crystallization at the LS interface occurs via a cyclic nucleation and ledge-flow mechanism.[4, 5] Thus, dissolution could very well occur via "reverse" ledge-flow since the removal of a single atom from an atomically flat top-facet is likely rate limiting.

While *in situ* control of catalyst droplet composition is possible by adding elements,[6-10] our experiments confirm that the reverse process is also possible with appropriately designed precursors. It also highlights, along with recent reports of selective sidewall etching,[11-13] new opportunities to tune the morphology of semiconductor NWs via subtractive techniques. First, the so-called "reservoir effect" – where atoms remaining in the catalyst droplet after cessation of precursor flow continue to be injected into the elongating NW – often results in compositionally graded dopant profiles and heterostructures.[14, 15] Atomically abrupt Si/Ge heterostructures may be possible, without modifying global process parameters[166-167] or without changes to catalyst phase,[10,16] by removing Si/Ge atoms upon Ge/Si atom addition (and vice versa). The development of selective chemistries that target one species, but not another, and vice versa, will be critical here. Second, the demonstrated etch process creates new opportunities to remove structural defects, such as twin planes and/or stacking faults, followed by a regrowth to 'heal' NWs. Lastly, the judicious placement of Au nanoparticles on the NW sidewall may enable etching at arbitrary angles that, after regrowth, could yield novel kinked morphologies and/or tree-like structures.

4.4. References

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CHAPTER 5. AXIAL SI/GE NANOWIRE HETEROSTRUCTURES GROWN VIA THE SUBEUTECTIC VAPOR-LIQUID-SOLID MECHANISM

5.1 Introduction

Control of composition at the nanoscale is central to the construction and operation of devices ranging from field effect transistors to solar cells.[1-2] It is also critical for advanced materials where the arrangement of nanoscale constituent elements gives rise to exotic properties.[3-6] The vapor-liquid-solid (VLS) mechanism, which permits the encoding of different materials and/or compositions along the length of semiconductor NWs, provides one route to programmable compositional heterogeneity.[7-9] Group III-V NWs due to the low solubility of group V atoms in the catalyst droplet, as well as the wide parameter space offered by the use of two precursors (i.e., for delivering group III and V atoms), currently offer the best control of axial heterostructure.[10-12] Axially embedded quantum dots can be fabricated with heights ranging from a single (< 2 nm) to several (< 20 nm) bilayers.[13-15]

Axial heterostructure formation remains difficult for group IV materials. Yet, the promise of group IV heterostructures in applications including large-area integrated circuits and thermoelectrics, where low cost, low toxicity, and thermal stability are paramount,[16-18] continues to motivate work in this area. The majority of axial Si/Ge heterostructure syntheses can be categorized in one of two ways: (1) those that can achieve clean morphologies, but with rapid growth rates that prevent the encoding of quantum-confined structures[19-20] and (2) those with growth rates more suitable for achieving confinement, but which yield poor morphologies,[21-22] catalyst atom diffusion,[23] sidewall deposition,[24] kinking,[25-26] and/or crystallographic defects.[27]

Rapid changes to the NW sidewall's surface termination when switching between Si- and Ge-containing precursors are a likely source of the unwanted structural motifs described above. We have previously shown that the sidewalls of NWs grown with hydride precursors (e.g., Si_2H_6 and Ge_2H_6) are often decorated with covalently-bonded hydrogen atoms.[28-30] Surface hydrogen atoms, of their several roles, help to pin the catalyst droplet at the NW tip by lowering the vapor-solid interface energy. Surface coverage, being dependent on the relative rate of H atom delivery (from precursor decomposition) and H_2 desorption, is a function of temperature and precursor partial pressure. Importantly, the desorption of hydrogen atoms (as H_2) from bare Si and Ge surfaces begins near ~350 and 230 °C, respectively.[31-33] This difference translates into significantly different H_2 desorption rates at any given temperature, which is problematic when growing Si/Ge heterostructures. Consider the introduction of Ge atoms (e.g., from Ge_2H_6 decomposition) after the growth of a Si domain (e.g., with Si_2H_6) under conditions where the sidewall is largely terminated with hydrogen atoms. Once Ge atoms are present on an otherwise Si sidewall, either from direct precursor adsorption on the vapor-solid interface or nucleation of a new bilayer at the liquid-solid interface, the rate of H_2 desorption from the sidewall will increase. A small coverage of Ge atoms on a Si surface is sufficient to yield Ge-like H_2 desorption behavior.[34-36] Dangling bonds created from the loss of surface hydrogen atoms, in turn, increase the vapor-solid interface energy and perturb the droplet. This situation likely causes kinking, [28, 37]defect formation,[37-38] and/or catalyst solidification.[29] Reduced hydrogen atom coverage also permits non-catalyzed precursor decomposition on the sidewall further away from the tri-junction, yielding tapered structures and unwanted radial heterointerfaces.[24, 30]

Figure 5.1 illustrates that the use of a single precursor for group IV materials intimately couples NW growth rate and sidewall termination,[30] making it difficult to maintain a high sidewall hydrogen atom coverage when switching between Si/Ge precursors. Increasing precursor partial pressure, which will deliver additional hydrogen atoms to the sidewall, offers one route to compensate for increased H_2 desorption rates. This approach, however, will also increase axial growth rate and preclude the formation of highly confined structures. Decreasing substrate temperature will also increase sidewall hydrogen coverage by reducing the rate of H_2 desorption, but it is challenging to lower it far enough. Complications often arise from crossing the eutectic temperature (T_e ~ 360 °C). Moreover, the adsorption of commonly used Si-containing precursors (e.g., SiH_4, Si_2H_6) slows below ~400 °C, which would also act to reduce sidewall hydrogen coverage. In summary, it is unlikely that judicious control of substrate temperature and the partial pressure of *conventional* hydride precursors will provide sufficient control of Si/Ge heterostructure growth with the VLS mechanism.

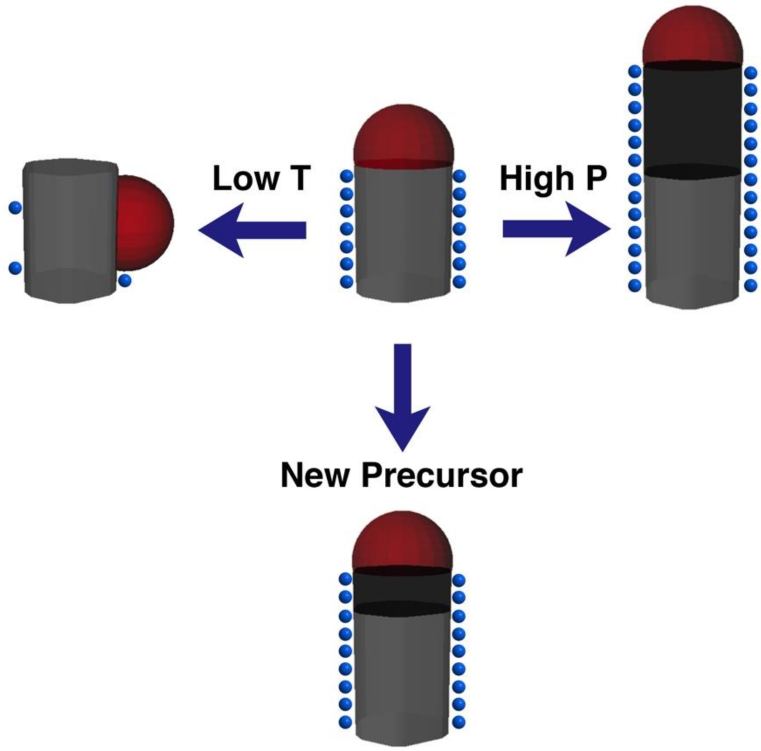

Figure 5.1. Schematic illustration of Ge/Si nanowire heterostrcuture synthesis at different process conditions with low and high adsorbent coverage. The Ge base segment initially is grown. During precursor switching, process conditions such as temperature (T) and partial pressure of the precursor (P) can strongly affect the heterostructure morphology. At low T, the adsorbent coverage is low due to low dissociation rate of the conventional hydride precursor, inducing Au diffusion. At High P, the adsorbent coverage is high but growth rate is rapidly increased to pose challenges in nano-scale synthetic control. A new hydride precursor is required to maintain high adsorbent coverage at low T while the growth is precisely controlled.

Vapor-solid-solid (VSS) growth, with an alloyed catalyst (e.g., Au/Al, Au/Ag) but conventional precursors, offers one route to high quality axial Si/Ge heterostructure NWs. [15, 39] It is difficult to perturb solid catalysts, even when the vapor-solid interface energy rises, which minimizes kinking or defect formation. The low solubility of semiconductor atoms in a solid catalyst also improves heterointerfacial abruptness. However, the alloys used in prior demonstrations required substrate temperatures higher than normal, which can reduce the coverage of hydrogen atoms on the NW sidewall (i.e., due to H_2 desorption). Even in the absence of wholesale catalyst depinning, metal catalyst atoms (e.g., Al, Au, etc.) can diffuse along the sidewall.[40] Direct adsorption of semiconductor atoms (e.g., Si, Ge, etc.) onto the sidewall can also create unwanted radial heterostructures, a situation that is exacerbated as the number of heterointerfaces in any given NW increases (i.e., while growing superlattices).

VLS growth with conventional catalysts such as Au, on the other hand, has some successes in NW heterostructures formation with unconventional precursors. The unconventional precursors such as HCl can be co-flowed with conventional hydride precursors during precursor switching.[41-42] Halogen and H atoms from the unconventional precursor provide additional sources of adsorbents on sidewalls, increasing the adsorbent coverage. Thus, the high adsorbent coverage can be maintained to stabilize catalyst droplets similar to the situation when flowing conventional hydride precursors at high partial pressure. However, adding different types of adsorbents into the VLS growth increases complexity of the NW structural control. Halogen adsorbents near the triple-phase line can affect the interfacial energies differently than the hydride adsorbents. Computational calculations previously predicated that even small changes in the interfacial energies cause structural imperfections.[43] Similarly, experimental studies observed structural changes such as kinking and twin planes during growth when sidewalls are passivated with adsorbents other than hydrides.[44-45] In addition, halogen atoms could react with IV- and III-V semiconductor surfaces to create rough surfaces or even remove atoms from the surfaces.[46-48] Ideally, an *unconventional* hydride precursor is required to maintain high adsorbent coverage at low temperature while still delivering semiconductors to the catalyst. The low temperature environment minimizes the unwanted conformal deposition and semiconductor delivery rate to achieve judicious control of the heterostructure formation during growth.

Here, we demonstrate high quality arrays of axial Si/Ge heterostructure NWs with clean sidewall morphologies and purely axial composition profiles.[49] We use a new precursor, trisilane (Si_3H_8), as the Si source and a conventional Au catalyst. Trisilane is highly reactive, enabling homoepitaxy at substrate temperatures as low as 300 °C.[50] The desorption rate of H_2 is slow at these temperatures, even in the presence of Ge atoms, and promises NWs whose sidewalls are well-passivated at all times. This precursor chemistry prevents unwanted catalyst perturbations when transitioning from Ge to Si segment growth, thus opening a new route to quantum-confined axial structures and/or superlattices in group IV NWs.

5.2 Experiment Details

5.2.1 Nanowire Synthesis

All NWs are synthesized in a custom-built ultra-high vacuum (UHV) chamber with a base pressure of 3×10^{-10} Torr (McAllister Technical Services). A description of the chamber and substrate preparation methods are included in prior studies.[28, 30] Briefly, substrates are cut into rectangles (6 mm × 24 mm) from a double-side polished Ge (111) wafer (MTI Corp., CZ, 500 μm, 42-64 Ω-cm). Each substrate is repeatedly oxidized in 3 wt% H_2O_2 (JT Baker, 30 wt%, ACS grade), etched with 9 wt% HCl (JT Baker, CMOS grade), cleaned with dionized water, and dried with N_2 gas. The substrate is then immersed in a 1:2:20 NH_4OH (Sigma-Aldrich, 28-30 wt%, ACS grade):H_2O_2:H_2O solution, rinsed with dionized water, and dried with N_2 gas. Upon insertion into the UHV chamber, the substrate is heated to 485 °C to desorb the chemical oxide from the previous wet chemical treatment, followed by epitaxial Ge film deposition at 305 °C with a Ge_2H_6 (Air Liquide, 20% in He) partial pressure of 2×10^{-5} Torr. Finally, a thin layer of Au (< 0.5 nm) is deposited onto the substrate at room temperature via thermal evaporation (SVT Associates). The substrate temperature is monitored throughout the NW growth by a calibrated infrared pyrometer (Mikron) focused on the backside of the substrate.

NW synthesis begins by introducing a Ge_2H_6 partial pressure of 1×10^{-4} Torr with the substrate at room temperature. The substrate is then heated to 485 °C at a rate of 10 °C/s, held for 30 s, and cooled to 305 °C at a rate of 3 ºC/s. A short Ge NW "stub" results from growth at these conditions for 5 min. While maintaining the Ge_2H_6 partial pressure, the substrate temperature is lowered to 290 °C and the remainder of the Ge segment is grown over the course of 30 min with a growth rate of 10.6 nm/min. Si segment growth is initiated by flowing Si_3H_8 followed by termination of Ge_2H_6 flow. The Si segment is elongated at either 290, 310, or 330 °C with Si_3H_8 (Air Liquide, 99.99%) at a partial pressure of 1×10^{-4} Torr for 30 min. Growth is terminated by rapidly reducing substrate temperature, after which Si_3H_8 is evacuated from the chamber.

5.2.2 Nanowire Characterization

NW structure is analyzed with a Hitachi SU-8230 scanning electron microscopy (SEM) and a FEI Tecnai F20 transmission electron microscope (TEM). For the (S)TEM-based measurements, NWs are transferred to carbon-coated grids (Ted Pella) by a direct mechanical transfer method.[59] HRTEM images are obtained with a 0.19 nm point-to-point resolution at 200 keV with an embedded Gatan image filter for EELS analyses. For the compositional maps and profiles, we combined scanning TEM (STEM) with electron energy loss spectroscopy (EELS) in the same FEI Tecnai F20 TEM.

5.2.3 Strain Determination

Heterointerfacial strain is analyzed by the geometric phase analysis (GPA) method.[60] The GPA algorithm performs an analysis based on the amplitude and phase of the lattice fringes as a function of position in the HRTEM images at different Bragg reflection angles. The cosine type mask with the radius previously optimized is employed around the (1 -1 -1) growth plane for all NW samples.

5.3 Results and Discussion

Arrays of epitaxial Si/Ge NWs are synthesized in an ultrahigh vacuum chamber described previously.[28, 30] A detailed experimental procedure is described in the Methods.

Briefly, Ge NWs are initially grown on a Ge(111) wafer with a Au catalyst at a Ge_2H_6 partial pressure of 1.0×10^{-4} and substrate temperature of 290 °C for 30 min. A Si segment is subsequently grown with a Si_3H_8 partial pressure of 1.0×10^{-4} at either 290, 310, and 330 °C for another 30 min. NWs are analyzed post-growth with scanning electron microscopy (SEM) and (scanning) transmission electron microscopy ((S)TEM).

Figures 5.3a and 5.3b show representative SEM images of Si/Ge NW arrays where the Si segment is grown at 290 and 330 °C, respectively. Si segment growth at 310 °C yields a similar morphology in Figure 5.4. NW morphology and cross-array uniformity is excellent (> 98% verticality) for all temperatures in Figure 5.5. Kinking or catalyst depinning at the hetero-interface is rarely observed. Nearly all NWs exhibit an epitaxial orientation relative to the Ge(111) substrate, indicating their growth is in the <111> direction. As anticipated for a Si/Ge heterostructure, the images in the Figures 5.3a,b and 5.4 insets show a bright segment (Ge) below a dark (Si) segment. The growth rate of the initial Ge segment is ~10.58 nm/min, as expected for growth at 290 °C.[30] The Si segment growth rate is far lower at ~0.45, 0.96, and 1.64 nm/min for 290, 310, and 330 °C, respectively. Despite the slow Si segment growth rates, to our knowledge, this is the first report of subeutectic Si segment growth with an Au catalyst and a gas phase hydride precursor.

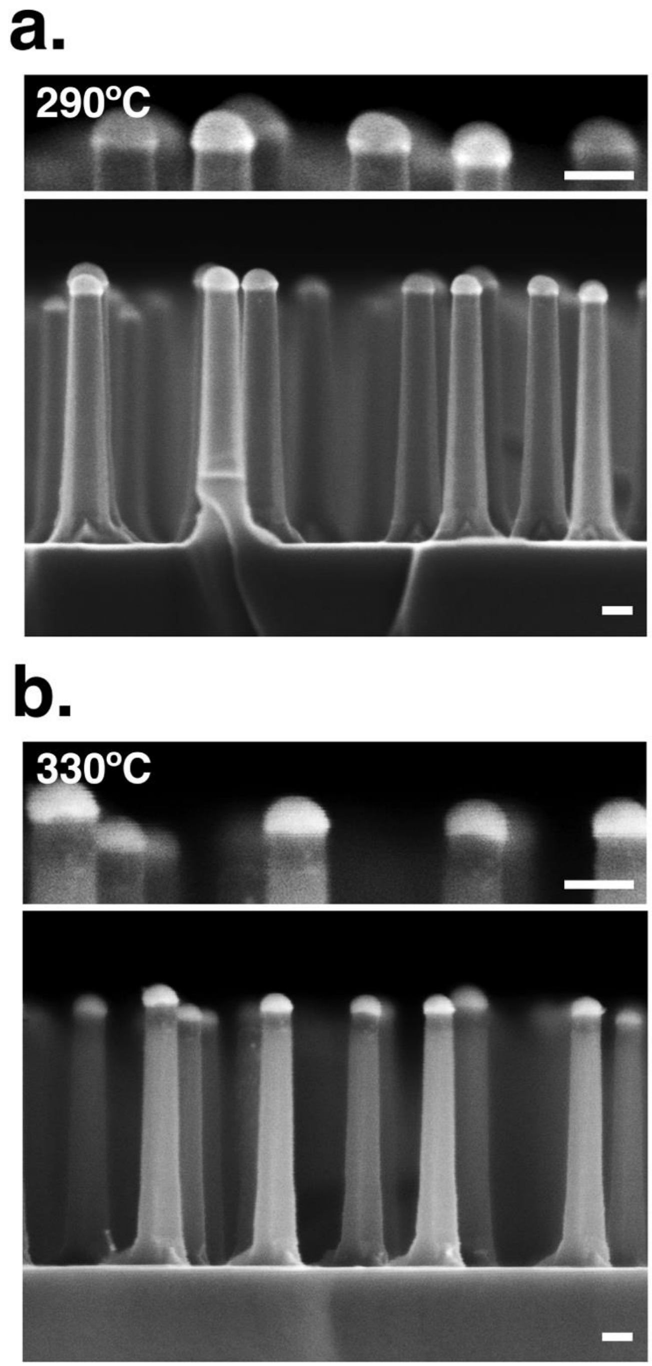

Figure 5.2. Representative cross-sectional SEM images of Si/Ge heterostructure nanowires where the Si segment is grown at (a) 290 °C and (b) 330 °C for 30 minutes. Scale bars, 50 nm.

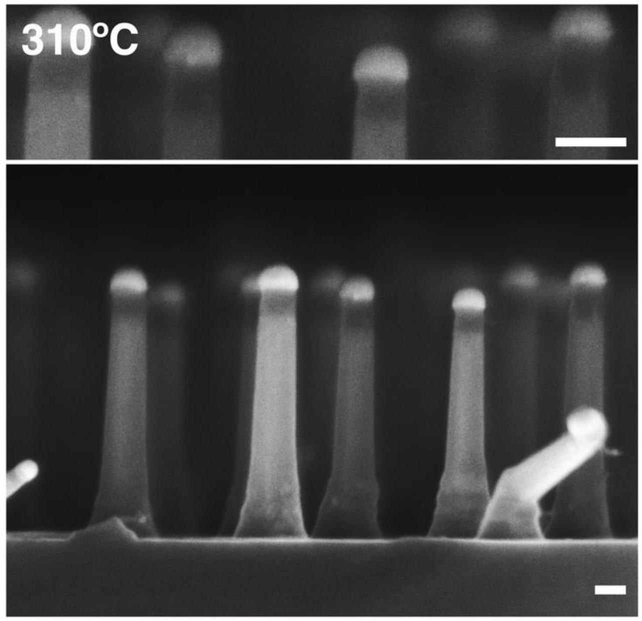

Figure 5.3. Representative cross-sectional SEM images of Si/Ge heterostructure nanowires where the Si segment is grown at 310 °C. Scale bars, 50 nm.

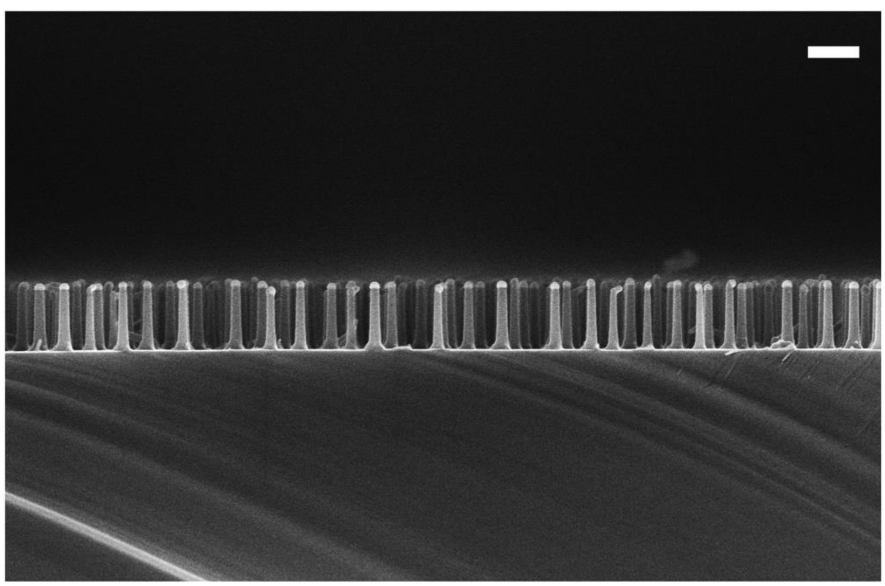

Figure 5.4. Representative cross-sectional SEM image of a Si/Ge heterostructure nanowire array. The Si segment is grown at 330 °C. Excellent epitaxy and clean sidewall morphologies are achieved across large areas. Scale bar, 300 nm.

Detailed structural analysis confirms the single-crystallinity and growth direction of the Si/Ge heterostructure NWs. Figure 5.6a shows a representative bright field TEM image of a Si/Ge heterostructure NW in the near-catalyst region with a Si segment grown at 290 °C. Lattice fringes are clearly visible, demonstrating that the NW remains single-crystalline across the Si/Ge heterointerface. Figures 5.6b,c and 5.6d,e show high-resolution TEM images along the [1-12] zone axis and associated Fast Fourier Transform (FFT) power spectra for the nominally Si (blue box) and Ge (red box) segments, respectively. Both segments grow along the <111> direction.

Electron energy loss spectroscopy (EELS) measurements confirm the chemical identity of the Si and Ge segments. Figure 5.7a shows a representative dark-field STEM image of a NW containing Si/Ge NWs with the Si segment grown at 290 °C. A contrast change near the catalyst is observed similar to that seen in Figure 5.3. The dark field images show no gold diffusion on sidewalls since the sidewalls are well passivated based on our recent work.[29] EELS maps of Si (blue) and Ge (red) are also show in Figure 5.6a and definitively confirm the presence of Si and Ge segments. The top of each map is the liquid-solid interface.

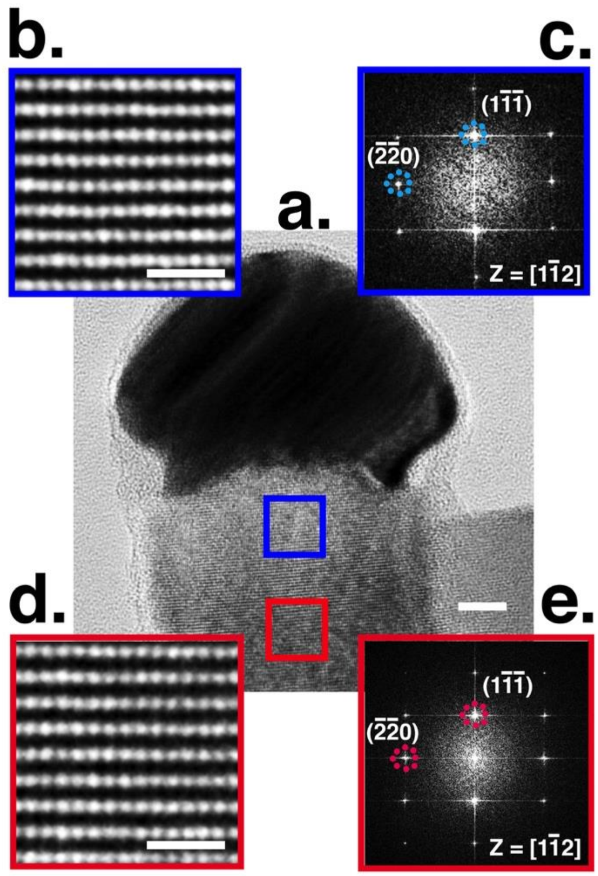

Figure 5.5. HRTEM characterization of the Si/Ge heterointerface. (a) HRTEM image of a nanowire with the Si and Ge segments grown at 290 °C. Scale bar, 5 nm. (b) High resolution TEM image of the Si segment. Scale bar, 1 nm. (c) FFT of the image in (b) showing growth along the <111> direction. (d) High resolution TEM image of the Ge segment. Scale bar, 1 nm. (e) FFT of the image in (d) showing growth along the <111> direction.

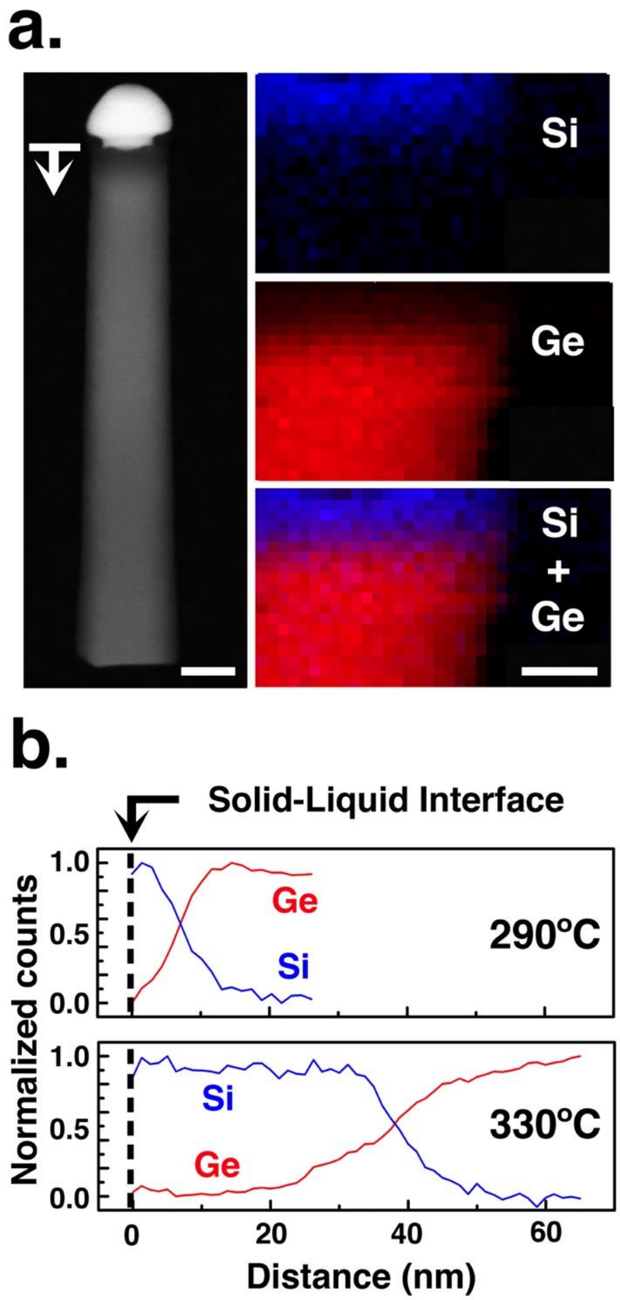

Figure 5.6. Compositional analysis of the Si/Ge heterointerface. (a) Representative high angle annular dark field (HAADF) scanning TEM (STEM) image of a Si/Ge heterostructure nanowire grown entirely at 290 °C. Scale bar, 30 nm. White line denotes the liquid-solid interface. Electron energy loss spectroscopy (EELS) maps of Si, Ge, and Si + Ge are also shown. Scale bar, 10 nm. (b) Axial EELS composition profiles starting at the liquid-solid interface and crossing the Si/Ge heterointerface for nanowires with the Si segment grown at 290 and 330 °C.

EELS composition profiles along the Si/Ge interface are displayed in Figure 5.7b and provide additional chemical insight. Foremost, Si is undetectable on the sidewall of the Ge segment in Figure 5.8, providing additional support that the NW sidewall is well passivated (likely by hydrogen) and the as-synthesized heterostructures are purely axial. The axial Si/Ge heterointerface is compositionally graded along the axial direction for all temperatures studied here. A transition width of approximately 10 and 20 nm is observed for Si segment growth at 290 and 330 °C, respectively, and is considerably less than the NW diameter.[19-20] Graded composition profiles are frequently observed for axial heterointerfaces and attributed to the so-called “reservoir effect”.[51-52] The solubility of semiconductor atoms in a liquid catalyst is non-negligible, which results in the continued injection of atoms into the elongating NW even after the termination of precursor flow. Here, upon switching from Ge_2H_6 to Si_3H_8, Ge atoms continue to be injected into the NW while the concentration of Si atoms rises in the catalyst. While graded heterointerfaces are usually undesirable, this observation provides strong evidence that growth occurs via the subeutectic VLS mechanism.

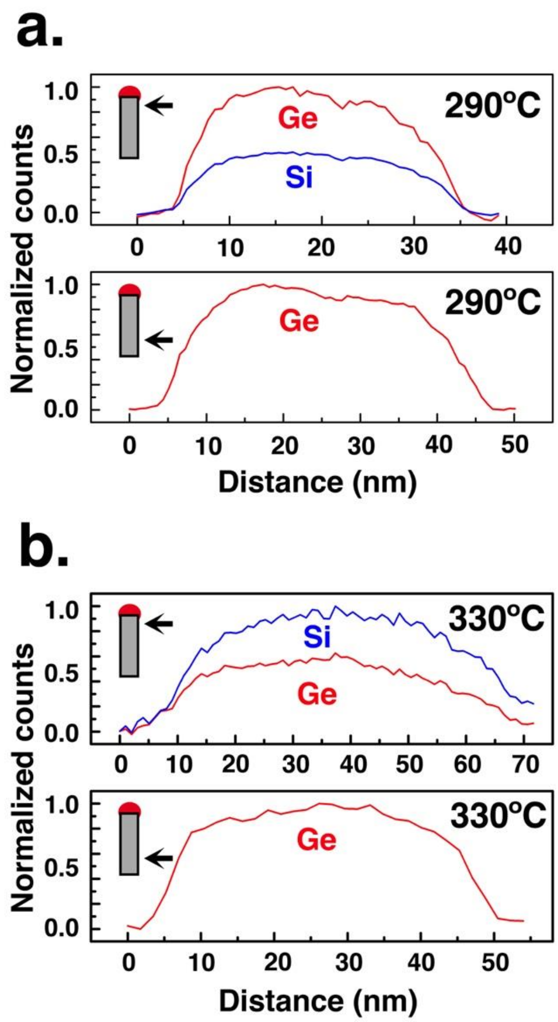

Figure 5.7. Radial EELS composition profiles for nanowires with the Si segment grown at (a) 290 and (b) 330 °C. Profiles are shown for locations near to (top) and far from (bottom) the Si/Ge heterointerface.

Identification of a root cause for the temperature-dependent transition width seen here is still under investigation, but is most likely of kinetic origin. Since the solubility of semiconductor atoms in the catalyst droplet changes only a few percent over the temperature range studied here, thermodynamics cannot fully explain the 50% change in transition width over 40 °C in Figure 5.7b.[53] Recent work has shown that atomic species (e.g., Ge) present in the catalyst droplet upon termination of precursor (e.g. Ge_2H_6) flow can be removed via a back reaction to the gas phase.[54-55] This kinetic pathway is consistent with the present data. A smaller transition width is observed at lower temperature, where the stability of the gas phase product species (e.g. GeH_x) would be higher.

We quantify heterointerfacial strain, as shown in Figure 5.9, with HRTEM combined with geometric phase analysis (GPA). The GPA maps in Figure 5.9 (left column), show the presence of a greenish transition area in between the reddish one corresponding to the pure Ge and the blueish, which corresponds to the relaxed pure Si tip. The greenish transition area is in good agreement with the presence of a graded heterointerface as visualized by EELS in Figure 5.7. This latest result indicates that the reservoir effect is not only influencing the composition at the transition interface, but also the cell parameter, which also takes a gradation in accordance with the composition, as observed recently in III-V axial heterostructures.[56-57] In addition, the strain measurements performed on the growth plane clearly at the Ge and Si regions (far from the transition graded heterointerface) show values close to the different *d* spacing of Ge and Si (a_{Si} = 5.4286 Å; a_{Ge} = 5.6580 Å). The expected theoretical mismatch between both species in a perfectly relaxed bulk heterointerface should be around -4%. Note that the calculated values, -3.7% and -3.9% for the Si segments grown at 290 and 330ºC, respectively, are close to the theoretical mismatch values, indicating an almost total relaxation of the two lattices involved. The highest discrepancy in the case of the segment grown at 290ºC, is due to the fact that the Si segment is shorter and thus remains slightly strained, suffering a tensile stress of about 0.3%.

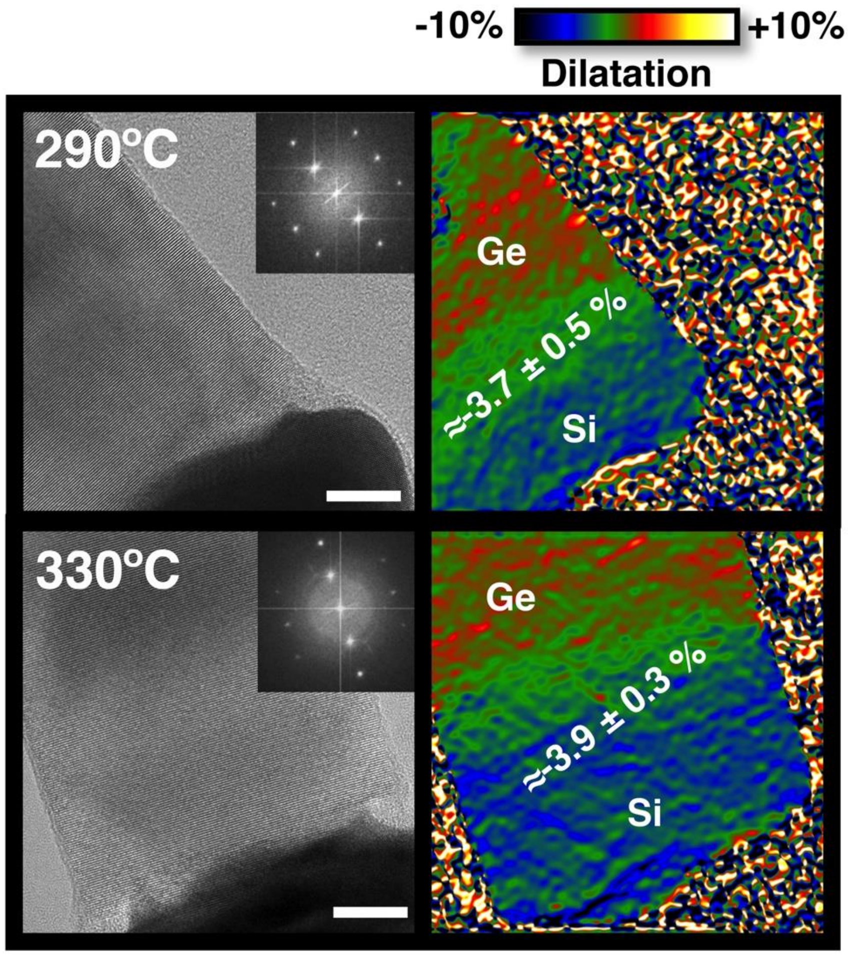

Figure 5.8. HAADF-STEM images of Si/Ge heterostructure nanowires with the Si segment grown at 290 and 330 °C, respectively. Dilatation map after applying GPA to the (1 -1 -1) Si and Ge growth planes at the same heterointerface region. The color scale in the GPA maps is following the temperature scale shown on the top right (from -10 to 10 % lattice expansion). Scale bars on the HRTEM images, 10 nm.

Arrays of epitaxial Ge/Si/Ge NWs are also synthesized. Figure 5.10a shows a representative HAADF STEM image containing Ge/Si/Ge NWs with each segment grown at 290 °C for 30 min. It definitively confirms the presence of Si (blue) and Ge (red) segments. The top of the map is the liquid-solid interface. Figure 5.10b confirms that the NW remains single-crystalline in HRTEM images along the [1-12] zone axis. Additionally, the EELS composition profile in Figure 5.10c shows similar graded interface at the first transition from the Ge to Si growth. Surprisingly, the interface at the second transition from Si to Ge segment growth is abrupt. The abruptness may come from catalyst solidification during the Si_3H_8 introduction because the growth rate of the second Ge segment is much slower than that of the first Ge segment with the same growth time. We also believe that the catalyst solidification prevents the Si elongation. Nevertheless, the change of the catalyst state is not the focus of our study here, and will be addressed in a future study. Despite incomplete understanding of the crystal state, our Ge/Si/Ge NW heterostructures alone present a new means to embed quantum structure within NWs. This ability could open many opportunities to tune novel properties for a wide range of applications.

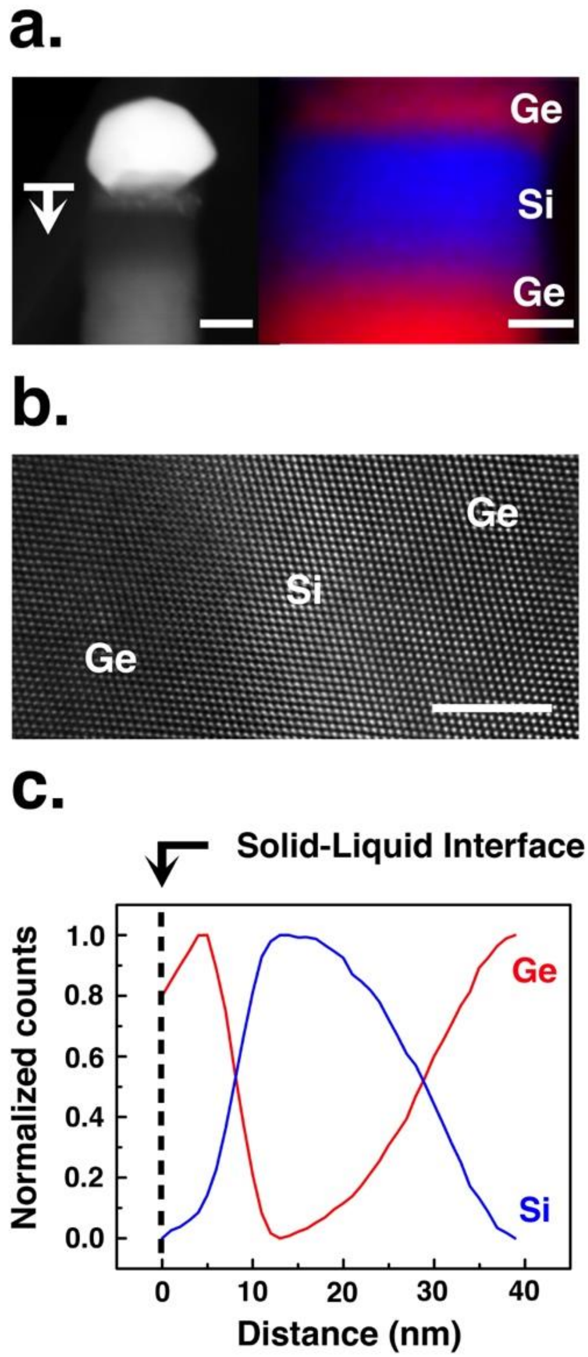

Figure 5.9. Compositional analysis of the Ge/Si/Ge heterointerface. (a) Representative HAADF-STEM image of a Ge/Si/Ge heterostructure nanowire grown entirely at 290 °C. Scale bar, 10 nm. White line denotes the liquid-solid interface. EELS maps of Ge + Si + Ge is also shown. Scale bar, 20 nm. (b) High resolution TEM image of the Ge-Si-Ge segments. Scale bar, 5 nm. (c) Axial EELS composition profiles starting at the liquid-solid interface and crossing the Ge/Si/Ge heterointerfaces for nanowires with each Ge and Si segments grown at 290 °C for 30 min.

5.5 Conclusion

In conclusion, we demonstrate the growth of axial Si/Ge heterostructures via the subeutectic VLS mechanism. The low decomposition temperature of both Si_3H_8 and Ge_2H_6 enables heterostructure formation without large changes in substrate temperature, resulting in large-area arrays of epitaxial NWs with clean morphologies and purely axial composition profiles. The lack of Au atoms on the NW sidewall indicates that the hydrogen atom coverage remains high during the Ge to Si transition, and prevents the catalyst perturbations that result in undesirable phase change, defects, and/or kinks.[27-28, 38,57] Additional work is required to improve heterointerface abruptness, but our experiments identify a new path to achieve the controlled growth of NWs with highly confined axial Si/Ge segments.

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CHAPTER 6. CONCLUDING REMARKS

6.1 Conclusions

Throughout this thesis, we have presented information, data and results showing how heterogeneous reactions at different interfaces are capable of tuning semiconductor NW structures. We have chosen group-IV materials (e.g. Si, Ge) with Au catalyst as the model system for NW synthesis. My studies focus on NW synthesis under a wide range of growth conditions (Pressure: UHV- and LP-CVD; Temperature: 260- 400 °C) in two chamber systems. Structural analysis on NWs utilized microscopic measurement techniques such as SEM and TEM with *in situ* IR spectroscopy to observe short-lived species. Along with the comprehensive analytical techniques, we create a kinetic model to elucidate the connections between different hetero-interfaces and NW growth.

Chapter 3 describes work~~s~~ that experimentally confirms long-standing speculation in NW synthesis - that semiconductor atoms can be removed from NWs through a catalyst.[1] We intentionally created a tapered segment as the morphological marker, and subsequently used 2,3-Butanedione to remove Ge atoms from Ge NWs. After etching, the volume of Ge NWs decreases only along the NW length. The NW sidewall is unaffected in the etching. The etching selectivity may have originated from the catalytic properties of the Au droplets. They accelerate the heterogeneous reaction to form stable etching by-products for atom removal at the VL interface. Finally, we quantified the etch rate as a function of temperature, pressure, and etchant flow rate. The kinetic data from the experiments are used to validate the model presented in Chapter 4.

In Chapter 4, the proposed model based on existing theory describes atom removal paths across both VL and LS interfaces.[1] In the theorized etching mechanism, Ge atoms in the droplets first bind with ~~the~~ etchant molecules to form stable etching by-products at the VL interface. The highly volatile molecules at the VL interface pour the Ge atoms from the droplet into the gaseous phase. The removal of continuous atoms undersaturates the droplet, introducing Ge dissolution from Ge solid NWs into droplets at the LS interface. Without the catalytic droplet, the heterogeneous reaction that forms etch by-products at the VL interface is minimized. Thus, atom removal only occurs along the NW growth direction. This model fits well with the experimental data from Chapter 3, suggesting its generalizability across a wide range of experimental conditions.

In Chapter 5, we reveal a novel synthesis of arrays of Si/Ge NW heterostructures that eliminates defects at low temperature in the absence of plasma.[2] Previous study shows a monolayer of adsorbents at the SV interface helps stabilize the NW growth.[3] However, lifetimes of the absorbent heavily depend on temperature. The low temperature environment increases their lifetime, but also lowers the dissociation rate of semiconductor sources at the VL interface. The slow dissociation cannot support supersaturation during NW growth, hence, growth cannot continue. To counter this undesirable effect, we selected a highly reactive species, trisilane, for Si segment growth in the heterostructures. It not only dissociates well at low temperature, but also is capable of supporting supersaturation of the growth while the low temperature environment maximizes the adsorbent's lifetime to suppress defect formation.

6.2 Outlook

Our studies reinforce, through theoretical and experimental endeavor, the important roles of heterogeneous reactions at different interfaces. By leveraging understanding of the chemistry at the interfaces, we succeeded in creating a set of novel techniques for structure tuning in NW growth, driving the development of next-generation NW-based applications. At the VL and LS interfaces, we present a new etching chemistry to remove atoms. From experiments and modeling, we propose that having a ring structure for the etch byproducts is required for stabilization on the droplet surface.[1] However, the etch rate can potentially be influenced by structural changes in the ring structure such as having different functional groups (e.g. dicarbonyl vs. diamino groups) or numbers of the members (4- vs. 5- member ring structures). Thus, in future studies, a series of potential etchants should be chosen to study how changes in the functional groups or ring structure impact etching behavior at the VL and LS interfaces. Additionally, etching chemistry selection could apply to other NW material systems such as III-V and II-VI NWs, selectively removing the atoms along the NW length without plasma.

At the VS interface, we observed how adsorbates such as hydrogen atoms affect the NW growth stability reported in a prior study.[3] However, semiconductor surface studies indicate that hydrogen atoms are desorbed at relatively low temperature. Thus, they may not be robust enough to modify/stabilize NW structures in a wide range of growth windows. New precursors are required to put down adsorbates and increase their lifetimes at the VS interface in different growth windows. For example, adsorbates such as O and S atoms have completely different adsorption characteristics and rates than hydrogen as a function of temperature at the VS interface.[4-5] Therefore, designing appropriate precursors for the molecular adsorption at the VS interface, in conjunction to exploring growth regimes that maximizes the adsorbate coverage, open the door to a robust chemical control of NW synthesis. Moreover, it may be possible to study the relationship between NW growth stability/structure and adsorbate coverage as a function of temperature and pressure via real-time IR spectroscopy. This technique could be used to can measure vibration spectra of adsorbates at the VS interface. The adsorbates with different functional groups and surface coverage can be detected and then speciated. Along with post-imaging techniques such as SEM, we can correlate the NW growth stability/structure with the interaction between the adsorbates at the VS interface and the catalytic droplet at the triple phase line. This valuable correlation could be further developed and generalized as design rules for engineering NW materials on different semiconductor surfaces.

For NW heterostructures, understanding that low temperature growth environments can increase the lifetimes of adsorbates at the VS interface is crucial to formation of defect-free Si/Ge NW heterostructures. We can potentially leverage our understanding of controlling NW heterostructures for doping and dopant profile control. Doping in NWs, on the other hand, is very attractive because the most exciting applications of semiconductor NWs often do not come from intrinsic materials. For example, semiconductor NWs with highly-doped segments have been considered as an alternative and flexible class of plasmonic materials, leading to sensitivity enhancement in chemical detection,[7] catalytic reactions,[8] and even biomolecular interaction detection.[9] However, defects often form in doped-NWs. For example, boron-doped Si NWs might suffer from uncontrollable kinking, diameter modulation, twin planes, and/or stacking faults.[10-12] In these studies, hydride-based precursors (e.g., Silane) were used to grow Si NWs above 500°C, which is well above the desorption temperature of hydrogen adsorbates at the VS interface. Similar to the NW heteorstructures, the absence of adsorbates in high temperature environments could destabilize the droplet at the growth front, inducing these crystal defects. In contrast to the silane precursor, Si NW growth with trisilane in a low temperature environment can maintain the hydrogen adsorbate layer to stabilize the droplet while co-flowing the dopant precursors. This additional support to the droplet could minimize defect formation as we show for NW heterostructures. Additionally, during doping processes, dopant precursors co-flow with the semiconductor precursor. If the adsorbates desorb from the VS interface, the empty spaces at the exposed NW sidewalls can react with the dopant precursor in a similar fashion as traditional semiconductor film doping. As a result, NWs could have an undesirable doped shell. Alternatively, the low temperature environment with trisilane maximize the lifetimes of adsorbates at the VL interface, preventing any significant chemical interaction between the dopant precursors and the semiconductor surface underneath the adsorbate layer. Thus, the doping profile can be precisely controlled by the user.

6.3 References

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