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Citation: Appl. Phys. Lett. 91, 092114 (2007); doi: 10.1063/1.2778472
View online: http://dx.doi.org/10.1063/1.2778472
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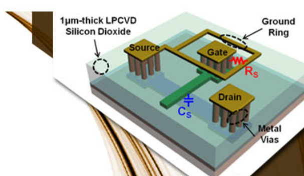

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High-performance and electrically stable C_{60} organic field-effect transistors

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(Received 26 July 2007; accepted 9 August 2007; published online 27 August 2007)

The authors report on high-performance C_{60} organic field-effect transistors fabricated by physical vapor deposition. Electron mobility ranging from 2.7 to 5.0 $cm^2/V\,s$ was achieved when treating the gate dielectric with divinyltetramethyldisiloxane bis(benzocyclobutene) and depositing C_{60} at room temperature. The transistors combine threshold voltages near zero, low subthreshold slopes (<0.7 V/decade), on/off current ratios larger than 10^6, excellent reproducibility, and good electrical stability under prolonged continuous dc bias stress. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2778472]

Thin-film field-effect transistors fabricated from organic semiconductors that can be processed onto various substrates at low temperature are of great interest. To enable the design of complementary circuits and take advantage of their intrinsic features such as low power consumption, *n*-channel and *p*-channel organic transistors with comparable performance are desirable. To date, more interest was given to the fabrication of *p*-channel transistors from hole transport organic materials, while electron transport organic semiconductors were given less attention.[1–4] Among electron transport organic semiconductors, fullerenes hold great promise for high-mobility *n*-channel organic field-effect transistors (OFETs). Since the first report by Haddon *et al.*[5] in 1995, improvements in the processing of C_{60} have led to the demonstration of the highest electron mobility of 6 $cm^2/V\,s$ by Anthopoulos *et al.*[2] in C_{60} films deposited by hot wall epitaxy at an elevated temperature of 250 °C. By modifying the properties of the C_{60}/SiO_2 interface using pentacene, Itaka *et al.*[6] obtained an electron mobility of 4.9 $cm^2/V\,s$ in devices processed at 50 °C and tested in high vacuum, and the devices exhibited an ambipolar property due to the presence of the pentacene wetting layer. Hence, it is highly desirable to achieve high-performance *n*-channel OFETs with large electron mobility, low threshold voltage, low subthreshold slope, and large on/off current ratio, and that can be processed at room temperature using standard physical vapor deposition. Furthermore, the transistors should show good stability when subjected to multiple testing cycles and under continuous electrical bias.

Here, we report on high-performance C_{60}-based OFET devices that were fabricated by standard physical vapor deposition at room temperature. Devices with various geometries were fabricated and tested in nitrogen at ambient pressure. These devices exhibit high electron field-effect mobility values that range from 2.7 to 5.0 $cm^2/V\,s$, depending on the device geometry. In addition to high-mobility values, these devices simultaneously exhibit threshold voltages near zero ($|V_T|<1$ V), low subthreshold slopes (<0.7 V/decade), and on/off current ratios larger than 10^6. By modifying the surface at the gate oxide with different organic dielectric materials, devices with excellent reproducibility and good electrical stability under multiple test cycles and continuous electrical stress could be demonstrated. The best combination of high-performance and good electrical stability could be achieved by using divinyltetramethyldisiloxane bis(benzocyclobutene)[7] (BCB) at the semiconductor/gate dielectric interface.

Transistors were fabricated on heavily *n*-doped silicon substrates (n^+-Si, as the gate electrode) with 200-nm-thick thermally grown SiO_2 as the gate dielectric ($\varepsilon_r=3.9$). To better control the interfacial properties at the dielectric and C_{60} interface, the SiO_2 dielectric surface was passivated with different thin buffer layers of polymers or with a self-assembled monolayer (SAM). Three hydroxyl-free polymers: BCB (Cyclotene™, Dow Chemicals), polystyrene (PS), and poly(methyl methacrylate) (PMMA) were used to coat the SiO_2 surface. The thin films from diluted Cyclotene™ BCB were cross-linked at 250 °C on a hot plate for 1 h in a N_2-filled glovebox. PS or PMMA films were spin coated from a 4 mg/ml solution in toluene and annealed at 130 °C on a hot plate for 1 h. Octadecyltrichlorosilane (OTS) SAM with a long alkyl chain, known as a good tunnel barrier to silanol groups on SiO_2 surface, was formed by soaking the substrates in a 5 mM toluene solution of OTS for 15 h in a dry N_2-filled glovebox right after the substrates were oxygen-plasma treated for 2 min. The thickness of the OTS layer was 2.25 nm, as measured by ellipsometry. The root-mean-square (rms) surface roughness of both polymer-coated and OTS-treated 200-nm-thick SiO_2 was below 5 Å, as measured by atomic force microscopy (AFM). The capacitance density C_{ox} (nF/cm^2) was measured from parallel-plate capacitors with 12 varying contact areas. The buffer layer on SiO_2 reduced C_{ox} from 16.6 to 16.2 nF/cm^2 with OTS, 15.5 nF/cm^2 with BCB, 15.3 nF/cm^2 with PS, and 15.8 nF/cm^2 with PMMA. The results on rms and C_{ox} are listed in Table I and will be used to calculated OFET electrical parameters.

OFETs were fabricated with a top-contact geometry, as shown in Fig. 1(a). For convenience, the transistors with BCB, PS, PMMA, and OTS as a buffer layer are referred to as devices T1, T2, T3, and T4, respectively. All transistors, for which data are reported here, underwent the same processing, measurement, and analysis steps. The devices were completed by evaporating a 50-nm-thick film of purified C_{60} at room temperature followed by the shadow mask deposition of the patterned 150-nm-thick Al as top source/drain electrodes. The electrical measurements were performed in a

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TABLE I. Summary of the electrical parameters for C_{60} transistors T1, T2, T3, and T4. rms, root-mean-square roughness (of the gate dielectrics), C_{ox}, capacitance density; μ, field-effect mobility; V_T, threshold voltage; V_{TO}, turn-on voltage; S, subthreshold slope, $I_{on/off}$, on/off current ratio. T1: BCB/SiO_2/n^+-Si; T2: PS/SiO_2/n^+-Si; T3: PMMA/SiO_2/n^+-Si; T4: OTS/SiO_2/n^+-Si.

	rms (Å)	C_{ox} (nF/cm^2)	μ (cm^2/V s)	V_{TO} (V)	V_T (V)	S (V/decade)	$I_{on/off}$
T1	3.2	15.5	3.1±0.2	−1.5±0.3	−0.1±0.4	0.5±0.1	1×10^7
T2	2.9	15.3	2.1±0.1	−0.1±1.4	1.2±1.3	0.5±0.2	6×10^6
T3	3.1	15.8	1.1±0.1	1.4±0.3	2.1±0.4	0.4±0.0	6×10^6
T4	4.1	16.6	1.2±0.1	−0.8±0.3	1.8±0.6	0.6±0.1	2×10^6

N_2-filled glove box (O_2, $H_2O<0.1$ ppm) at normal pressure (1 atm) in the dark using an Agilent E5272A source/monitor unit.

To explore the influence of the different dielectrics on device performance, the electrical characteristics of transistors T1, T2, T3, and T4 with the same channel length $L=100$ μm and the same channel width $W=1000$ μm are compared in Figs. 1 and 2. Figures 1(b)–1(e) show the representative transfer characteristics (I_{DS} vs V_{GS} plotted on a semi-logarithmic scale and $\sqrt{I_{DS}}$ vs V_{GS}, at V_{DS}=30 V) for both forward and reverse gate bias scans. Figure 1(f) compares the representative output characteristics (I_{DS} vs V_{DS}) of all four types of transistors at V_{GS}=30 V. Field-effect mobilities μ and threshold voltages V_T were calculated in the saturation regime defined by standard metal-oxide-semiconductor field-effect transistor models by fitting the $\sqrt{I_{DS}}$ vs V_{GS} data to the square law. Also extracted from the transfer characteristics are turn-on voltage (V_{TO}) and on/off current ratio ($I_{on/off}$). For each type of transistors, four devices with identical geometry were measured to obtain the mean value with its standard deviation (SD). The extracted electrical parameters (μ, V_{TO}, V_T, S, and $I_{on/off}$) (calculated from forward bias scans) are summarized and compared in Table I, along with rms and C_{ox} previously obtained. As seen from AFM height images in the insets of Figs. 1(b)–1(e), C_{60} films generally exhibit similar morphology and microstructure with small grains, regardless of the dielectric surface modification. This structure is characteristic to that observed previously in C_{60} films deposited at low temperature.[8,9] Even with small grains in C_{60} films, all transistors presented a mobility μ higher than 1 cm^2/V s, a threshold voltage V_T less than 2.5 V, a subthreshold slope S steeper than 1 V/decade, and $I_{on/off}$ ratios larger than 10^6. Note that among them, T1 (BCB) showed the highest mobility of 3.1 ± 0.2 cm^2/V s.

Also shown in Figs. 1(b)–1(e) is the influence of the surface dielectric properties on the hysteresis observed sometimes in the transfer characteristics. Here, the threshold voltage shift $\Delta V_T=\Delta V_T^R$ (reverse scan) $-\Delta V_T^F$ (forward scan) was used as a metric to quantify the hysteresis and bias stress effects. A value of ΔV_T=2.9 V due to hysteresis was observed in T4 with an OTS SAM, as shown in Fig. 1(e). However, the hysteresis behavior was strongly suppressed in transistors T1, T2, and T3 where the SiO_2 surface was passivated with hydroxyl-free polymers such as BCB, PS, or

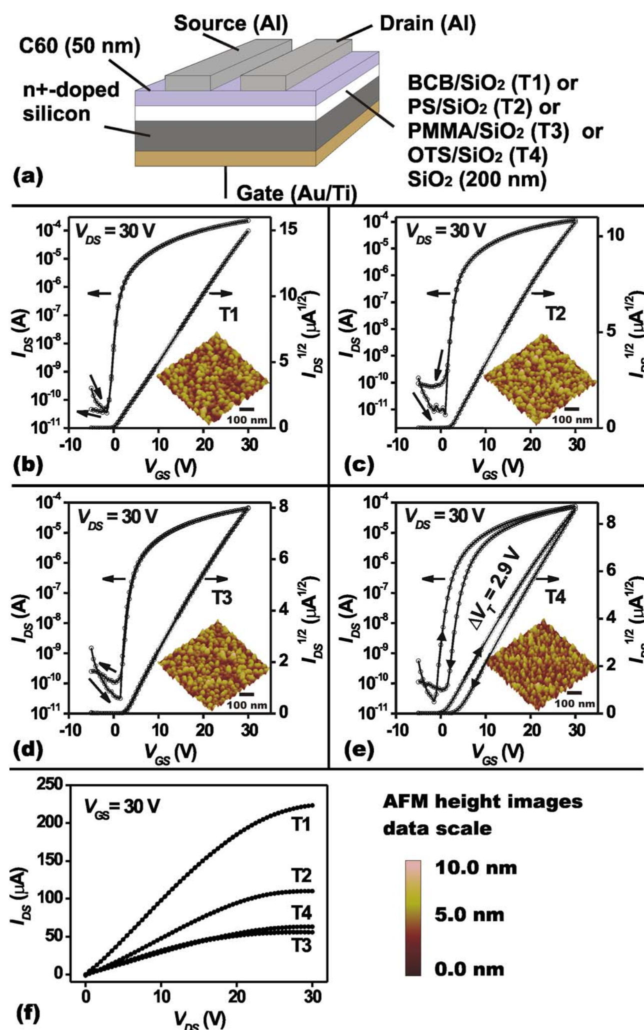

FIG. 1. (Color online) (a) Diagram of the OFET device geometries for transistors T1–T4. [(b)–(e)] Transfer characteristics at V_{DS}=30 V for both forward and reverse gate bias scans with corresponding AFM height images of C_{60} films (insets) for transistors T1–T4, respectively. (f) Output characteristics at V_{GS}=30 V for all four types of transistors.

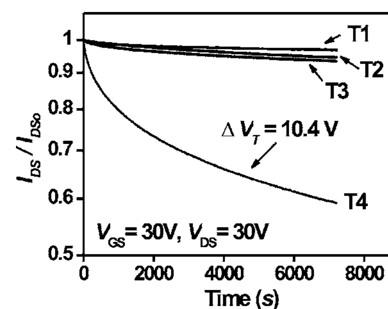

FIG. 2. Time-dependent decay of I_{DS} of C_{60} OFETs for transistors T1–T4 with different buffer layers under continuous dc voltage biases of $V_{GS}=V_{DS}$=30 V for 2 h.

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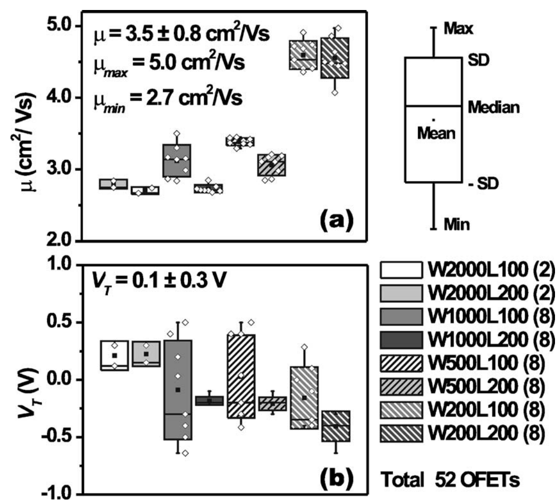

FIG. 3. Statistical analysis of the electrical characteristics: (a) mobility and (b) threshold voltage of 52 C_{60} OFETs obtained from two substrates fabricated within the same batch.

PMMA. The same trend was also found when conducting dc bias stress tests. No degradation was observed in transistors other than T4 (OTS) when the devices were repeatedly stressed by measuring transfer characteristics in the saturation regime 100 times with a 2 s waiting time between scans. Figure 2 shows the time-dependent decay of I_{DS} of C_{60} OFETs with different buffer layers under continuous dc voltage biases of $V_{GS}=V_{DS}=30$ V for 2 h. The C_{60} OFETs with polymers as a buffer dielectric (T1, T2, and T3) show negligible degradation with 3.1%, 5.4%, and 6.6% decrease in I_{DS}, respectively. In contrast, T4 (OTS) devices show a steep decay with a 40% decrease in I_{DS} and a large V_T shift of 10.6 V. Hydroxyl-free polymers used with C_{60} as gate dielectrics are shown to significantly improve the device stability. These observations are in agreement with the findings of Chua *et al.*[4] that hydroxyl groups (e.g., silanol) can lead to the electrochemical trapping of electrons that in turn can induce a gradual change in gate threshold over time when the transistor is under continuous bias. The electrical instability observed from T4 transistors treated with OTS confirms that surface silanol groups cannot be fully passivated by siloxane-based SAMs,[10] as previously shown by Chua *et al.*[4] in *n*-channel transistors fabricated from various conjugated polymers.

In view of the best combination of performance and stability obtained in T1 devices, a set of 52 OFETs devices with channel width ranging from 200 to 2000 μm and channel length of 100 or 200 μm was fabricated on two separate substrates that were processed identically within the same batch. The distribution and uniformity of device parameters (μ, V_T) measured in the 52 devices are shown in Fig. 3 in the form of box plots. The on/off current ratios for the 52 devices range from 10^6 to 10^8 where the resolution of the off current (10^{-11} A) is a limiting factor. As shown in Fig. 3(a), the mobility values measured in the 52 devices range from a minimum value of 2.7 $cm^2/V\,s$ to a maximum value of 5.0 $cm^2/V\,s$ with a mean value of 3.5 $cm^2/V\,s$ and a SD of 0.8 $cm^2/V\,s$. Devices with the lowest W/L ratio ($W=L=200$ μm) showed the highest mobility where geometry effects such as fringing currents may lead to larger effective field-effect mobilities. All the devices have a V_T near zero [0.1 ± 0.3 V see Fig. 3(b)] and a subthreshold slope S smaller than 1 (0.5 ± 0.1 V/decade).

In conclusion, we have demonstrated electrically stable, high-performance top-contact C_{60}-based *n*-channel OFETs in which BCB was inserted at the semiconductor gate dielectric interface. Studies of electrical degradation under dc bias stress performed on devices with different gate dielectric materials have shown that hydroxyl-free polymers such as BCB, PS, and PMMA can lead to devices with superior lifetime in which interface charge trapping effects are minimized. Current devices were fabricated using standard physical vapor deposition with substrates held at room temperature during the C_{60} deposition demonstrating ease of processing over large area. Testing was performed in inert atmosphere at normal pressure. Future work will focus on passivating these transistors using atomic layer deposition which provides good encapsulation, as demonstrated recently with pentacene/C_{60} solar cells.[11]

This material is based upon work supported in part by the STC Program of the National Science Foundation under Agreement No. DMR-0120967 and by the Office of Naval Research. This work was performed in part at the Microelectronics Research Center at Georgia Institute of Technology, a member of the National Nanotechnology Infrastructure Network, which is supported by NSF (Grant No. ECS-03-35765).

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