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Top-gate hybrid complementary inverters using pentacene and amorphous InGaZnO thin-film transistors with high operational stability

J. B. Kim, C. Fuentes-Hernandez, D. K. Hwang, W. J. Potscavage Jr., and B. Kippelen[a]
Center for Organic Photonics and Electronics (COPE), School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332, USA

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We report on the operational stability of low-voltage hybrid organic-inorganic complementary inverters with a top-gate bottom source-drain geometry. The inverters are comprised of *p*-channel pentacene and *n*-channel amorphous InGaZnO thin-film transistors (TFTs) with bi-layer gate dielectrics formed from an amorphous layer of a fluoropolymer (CYTOP) and a high-k layer of Al_2O_3. The *p*- and *n*- channel TFTs show saturation mobility values of 0.1 ± 0.01 and 5.0 ± 0.5 cm^2/Vs, respectively. The individual transistors show high electrical stability with less than 6% drain-to-source current variations after 1 h direct current (DC) bias stress. Complementary inverters yield hysteresis-free voltage transfer characteristics for forward and reverse input biases with static DC gain values larger than 45 V/V at 8 V before and after being subjected to different conditions of electrical stress. Small and reversible variations of the switching threshold voltage of the inverters during these stress tests are compatible with the observed stability of the individual TFTs. *Copyright 2012 Author(s). This article is distributed under a Creative Commons Attribution 3.0 Unported License.* [doi:10.1063/1.3684635]

Organic and metal-oxide thin-film transistors (TFT) are attractive because they can be processed at low-temperature, on large-area flexible substrates.[1,2] Practical electronic circuits are expected to use both *p*- and *n*-channel TFTs to build complementary inverters that operate with low power consumption, high gain values, and high and balanced noise margins. To maximize the inverter performance, the *p*- and *n*-channel TFTs should yield comparable output characteristics despite of differences in the properties of the materials used. Organic semiconductors provide a good framework for the development of complementary technologies, since *n*-channel or *p*-channel TFTs can readily be fabricated. However, *n*-channel TFTs tend to be more susceptible to degradation in air and show lower mobility values than metal-oxide semiconductors. On the other hand, metal-oxide semiconductor TFTs that can be processed at low temperatures and yield high mobility values, with a few exceptions,[3] operate mainly as *n*-channel TFTs.[2,4] Metal-oxide TFTs that are stable under continuous bias stress typically require annealing at temperatures higher than 300 °C, however, strategies are emerging to reduce its processing temperatures, making them more suitable to flexible substrates.[5,6] Therefore, *n*-channel metal-oxide TFTs combined with *p*-channel organic TFTs could be used to realize complementary circuit designs that benefit from the intrinsic advantages of these two classes of semiconductors.

Hybrid TFT-based complementary inverters with high gain values have been demonstrated using horizontally distributed *n*- and *p*-channel semiconductor layers with a bottom-gate geometry.[7,8] Unfortunately, the operational stability of hybrid inverters after electrical bias stress has been overlooked and only a few studies exist that explore the operational stability of all-organic inverters.[9,10]

[a]Author to whom correspondence should be addressed; electronic mail: Kippelen@ece.gatech.edu.

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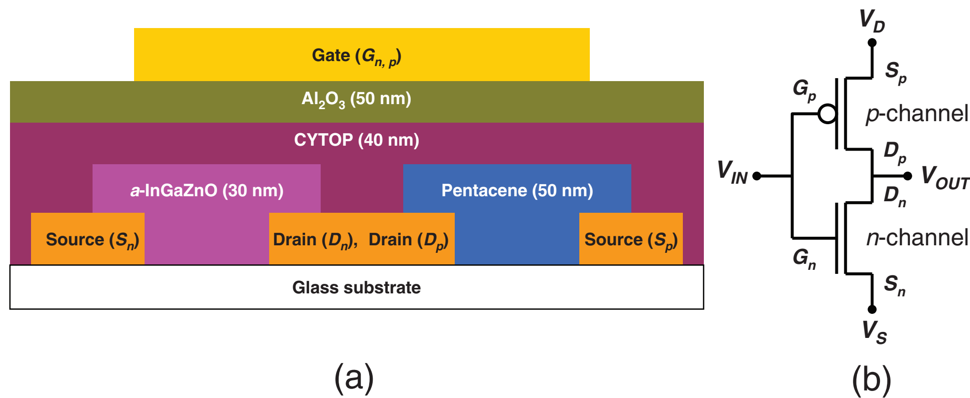

FIG. 1. (a) Schematics of the organic-inorganic hybrid complementary inverters comprised of *p*-channel pentacene and *n*-channel *a*-IGZO TFTs. (b) Complementary inverter circuit diagram.

This is in part because achieving long-term operational stability is a major challenge faced by many TFT technologies incorporating either organic[11,12] or metal-oxide[13,14] semiconductors. The degradation of the performance of a TFT during operation is reflected by changes of its current characteristics that can result from changes of mobility, threshold voltage or variations of the capacitance density. Recently we developed 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) and poly(triarylamine) (PTAA) blend *p*-channel TFTs using a top-gate bi-layer gate insulator comprised of CYTOP and a high-*k* metal-oxide layer of Al_2O_3 fabricated by atomic layer deposition (ALD).[15] The use of a CYTOP/Al_2O_3 bi-layer gate dielectric yielded TFTs with low voltage operation and remarkable long-term environmental and operational stabilities. However, the operational stability of metal-oxide TFTs and hybrid complementary inverters with this bi-layer top-gate geometry has not been study.

In this work, we report on the operational stability of top-gate *p*-channel pentacene and *n*-channel amorphous InGaZnO (*a*-IGZO) TFTs and inverters that use a CYTOP/Al_2O_3 bi-layer as gate dielectric. We show that individual TFTs yield hysteresis-free current voltage characteristics with high saturation mobility values and large on-off current ratios at low operating voltages. We also demonstrate that both types of TFTs show good electrical stability with negligible variations under continuous multiple scans up to 500 cycles and less than 6 % variations after continuous direct current (DC) bias stress for 1 hour. We demonstrate that these TFTs yield stable inverters with hysteresis-free voltage transfer characteristics that show small and reversible shifts of the switching threshold voltage under different bias-stress conditions. Finally, we discuss strategies for improving the electrical stability of inverters in view of the behavior of individual TFTs during dc bias stress tests.

We fabricated organic-inorganic hybrid complementary inverters with a top gate and bottom-contact source and drain electrode geometry, as shown in Fig. 1(a). First, Ti/Au (6 nm/50 nm) electrodes were deposited using electron-beam (e-beam) evaporation at room temperature on a glass substrate through a shadow mask to define the source and drain electrodes. Non-overlapping pentacene (hole transport) and *a*-IGZO (electron transport) channels horizontally distributed with different aspect ratios were fabricated on top of the source/drain electrodes. A 30 nm-thick *a*-IGZO (Ga_2O_3:In_2O_3:ZnO = 1:1:1 mol %) active layer was deposited at room temperature by rf-sputtering through a shadow mask using a power of 125 W at a working pressure of 3 mTorr in an O_2/Ar (2%/98%) atmosphere. These structures were annealed at 300 °C for 30 minutes in air. Then, a 50 nm-thick layer of pentacene was deposited through a shadow mask using thermal evaporation with a substrate temperature of 25 °C and an initial pressure of 2 x 10^{-8} Torr. Prior to thermal evaporation, pentacene was purified using gradient zone sublimation. A CYTOP/Al_2O_3 bi-layer was then used as a top gate dielectric. A CYTOP solution (CTL-809M) with a concentration of 9 wt. % was purchased from Asahi Glass and diluted to 2 wt. % with a fluorinated solvent (CT-solv.180). The diluted solution was spin casted at 3000 rpm for 60 sec to yield 40-nm-thick CYTOP layers. The

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CYTOP film was annealed at 100 °C for 20 min. All spin-coating and annealing processes were carried out in a N_2-filled dry box. After that, a Savannah100 ALD system from Cambridge Nanotech Inc. was used to deposit a 50 nm-thick Al_2O_3 layer. The Al_2O_3 films were deposited at 110 °C using alternating exposures of tri-methyl-aluminum ($Al(CH_3)_3$) and H_2O vapor at a deposition rate of approximately 0.1 nm per cycle. The capacitance density of the bi-layer gate dielectric was measured to be 34.8 nF/cm^2. Finally, a 50 nm-thick Al electrode was fabricated by thermal evaporation through a shadow mask to serve as gate electrode. Complementary inverter circuits, as shown in Fig. 1(b), were constructed using *p*-channel pentacene and *n*-channel *a*-IGZO TFTs with a similar channel length of L = 180 μm and different channel widths of W_p = 4000 μm and W_n = 400 μm, respectively. The channel width ratio of W_p/W_n = 10 was selected to compensate for differences in electron and hole mobility and differences in the threshold voltage.

The current-voltage characteristics of independent *p*-channel and *n*-channel TFTs, fabricated on the same substrate with the same channel aspect ratio as those used in the complementary inverters, are shown in Fig. 2. The transfer (Figs. 2(a) and 2(c)) and output characteristics (Inset of Fig. 2(b)) of all TFTs were measured using an Agilent E5272A medium-power source/monitor unit connected to a probe station. Pristine *p*-channel pentacene and *n*-channel *a*-IGZO TFTs showed hysteresis-free current voltage characteristics with saturation mobility values of 0.1 ± 0.01 and 5.0 ± 0.5 cm^2/Vs and threshold voltage (V_{TH}) values of -1.6 ± 0.1 and 2.6 ± 0.1 V, respectively. Bias stress tests were then conducted to investigate the electrical stability of both TFTs by first using multiple V_{GS} scans, up to 500 cycles, and then 1 hr DC bias stress at $V_{GS} = V_{DS} = \pm$ 8 V (this is, at a total TFT sheet resistance of 58 MΩ/□ and 1 MΩ/□ for the *p*-channel pentacene and *n*-channel *a*-IGZO TFTs, respectively). As shown in Fig. 2, the transfer and output characteristics of both TFTs remain unchanged after the cycling test. Figure 2(b) shows the temporal evolution of the drain-to-source current (I_{DS}) during the DC bias stress. Remarkably, the maximum changes observed at the end of 1 hr corresponded to less than +3 % and -6 % variations of pentacene and *a*-IGZO TFTs, respectively. A 10% current decay lifetime, $\tau_{10\%}$,[16] of 1.4×10^4 s is extrapolated from stretch exponential fits to the data measured on the *a*-IGZO TFTs. For the pentacene TFTs, an estimation of the $\tau_{10\%}$ value results difficult given the initial rise of I_{DS}. For top-gate TIPS-pentacene TFTs with the same bi-layer gate dielectric geometry and similar electrical characteristics $\tau_{10\%}$ values in the range from 5×10^5 to 1×10^6 s can be extrapolated.[15] The inset of Fig. 2(b) shows the output characteristics measured before and after this DC bias stress test. To summarize, Fig. 2(c) shows a comparison of the transfer characteristics measured on pristine TFTs and those measured after the different bias stress tests.

As shown in Fig. 2(c), the small variations of I_{DS} observed are related primarily to small changes of V_{TH}. To understand the origin of these small changes and their differences in sign, let us discuss the main mechanisms that can lead to operational instabilities: (i) the formation of charge traps at the semiconductor/dielectric interface or in the semiconductor itself; (ii) a field-induced dipolar increase in polarization of the gate dielectric; (iii) the displacement of mobile charged impurities inside the gate dielectric; and (iv) the injection of charges from the gate electrode into the gate dielectric.[8,15,17] These different mechanisms can lead to either an increase (mechanism (ii), (iii) and (iv)) or a decrease (mechanism (i)) of the source and drain current (I_{DS}). As we previously reported, the bi-layer gate dielectric geometry allows for a combination of compensating mechanisms that stabilize the operation of TFTs.[15] In this context, we can attribute the gradual increase of I_{DS} exhibit by pentacene TFT, to a dominant mechanism of the type (ii), (iii) or (iv) in which the field-induced orientation of hydroxyl groups in the Al_2O_3 layer, remnant from the ALD deposition, leads to an increase in polarization and consequently an increase in capacitance density and a positive shift of V_{TH}. This mechanism dominates over the mechanism of type (i) in which charges get trapped at the semiconductor/dielectric interface or in the semiconductor itself. On the other hand, the opposite is true on the *a*-IGZO TFTs where a more dominant mechanism and the type (i), leads to a small, but gradual decrease in I_{DS}. This reflects differences in the concentration of surface defects and density of deep traps between the two semiconductor channels. We note that in *a*-IGZO TFTs, the annealing conditions have a profound effect over the density of trapping sites leading to mechanism (i). This is because annealing promotes the diffusion of oxygen into the oxide layer and consequently, filling of oxygen vacancies which act as traps under continuous electrical bias. Although diffusion is a thermally promoted process, it is also affected by the porosity and the path-length for the gas to

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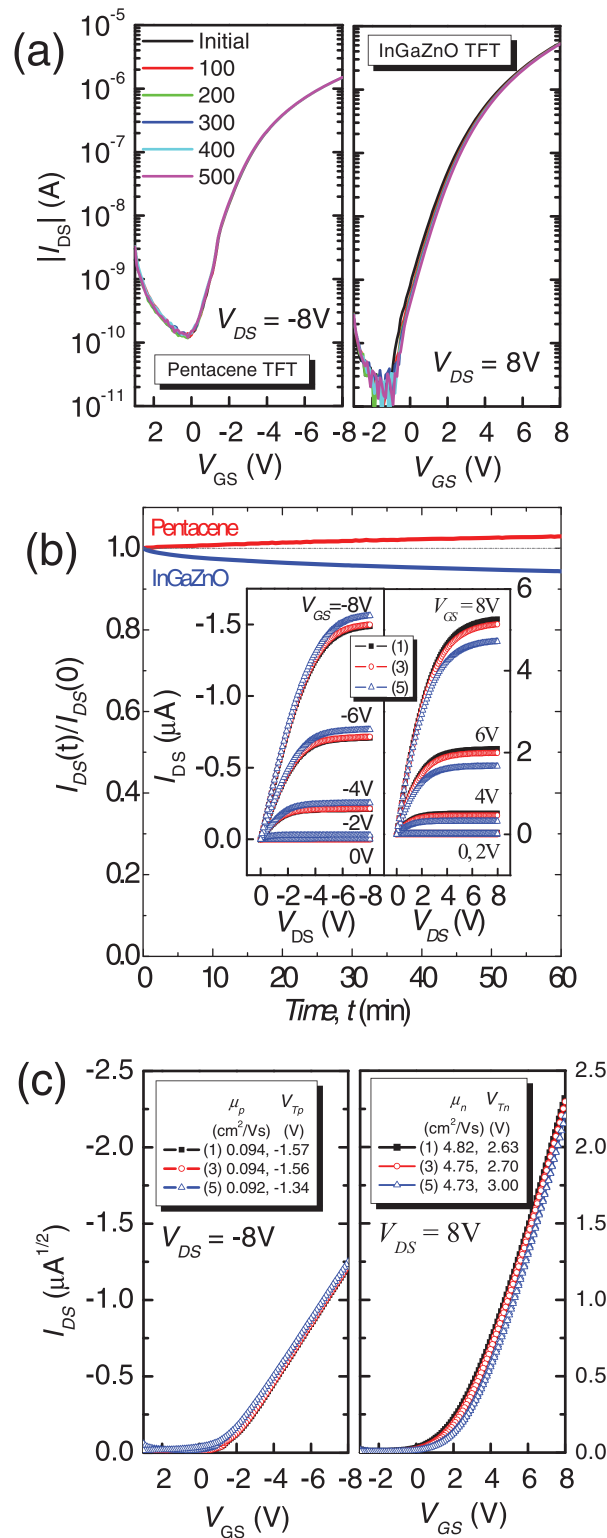

FIG. 2. (a) 500 multiple cycles of transfer characteristics of *p*-channel pentacene and *n*-channel *a*-IGZO TFTs at $V_{DS} = \pm 8$V. (b) I_{DS} of pentacene and *a*-IGZO TFTs with 1 h DC bias stress at $V_{GS} = V_{DS} = \pm 8$ V. (Inset: Representative output characteristics of pentacene and *a*-IGZO TFTs before stress and after 500 multiple cycles of transfer curves and after 1 h DC bias stress.) (c) Representative hysteresis transfer characteristics of pentacene and *a*-IGZO TFTs before stress and after 500 multiple cycles of transfer curves and after 1 h DC bias stress.

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diffuse into the solid film. Reductions of the annealing temperatures for the *a*-IGZO TFTs could be possible if the protocols for annealing and depositing the *a*-IGZO films (i.e. film thickness, annealing atmosphere, etc.) are optimize. Detailed studies concerning the effects of annealing conditions on the performance of *a*-IGZO TFTs are underway but are also outside the scope of the present work so they will be publish elsewhere.

The static performance of an inverter is evaluated by its static gain and noise margin values, both extracted from the measured voltage transfer characteristics (*VTC*s).[18] Achieving high and balanced noise margin values is necessary for reliable circuit operation in complex logic circuits such as ring oscillators. The noise margin is defined by two values, the noise margin low ($N_{\mathrm{ML}} = V_{\mathrm{IL}} - V_{\mathrm{OL}}$) and the noise margin high ($N_{\mathrm{MH}} = V_{\mathrm{OH}} - V_{\mathrm{IH}}$), where V_{IH}, V_{IL}, V_{OH}, and V_{OL} are input (V_{IN}) and output (V_{OUT}) voltages at the high and low levels of a given inverter *VTC*s. The noise margin is limited by the steepness ($\Delta V_{IN} = V_{\mathrm{IH}}$ - V_{IL}) of the transition, where ΔV_{IN} is the difference of input voltages at high and low levels, and by the position of the switching threshold voltage ($V_M = V_{IN} = V_{OUT}$). High and balanced noise margins are found when the ideal condition $V_M = 0.5V_D$ is met, hence when $V_M = V_{IN} = 0.5V_D = V_{OUT}$. However, the value of V_{IN} at which this transition occurs is generally not $0.5V_D$. The actual value of V_M depends on the range of $V_{D.}$ The *VTC*s and static DC gains of the complementary inverters shown in Fig. 3(a) and 3(b) were evaluated at $V_D = 8$ V after the following steps: (1) before stress; (2) after 500 continuous scans of the transfer characteristic of only the *p*-channel TFT; (3) after 500 continuous scans of the transfer characteristic of only the *n*-channel TFT; (4) after 1 h DC bias stress of only *p*-channel TFT; and (5) after 1 h DC bias stress of *n*-channel TFT. Before and after bias stress, the inverters yielded hysteresis-free voltage transfer characteristics for forward and reverse input biases due to the hysteresis-free current voltage characteristics with static DC gain values higher than 45 V/V. Before the stress tests, the inverter showed a V_M value of 3.3 V at 8 V and noise margins low of $N_{\mathrm{HL}} = 1.95$ V and high of $N_{\mathrm{MH}} = 3.65$ V, corresponding to 49 % and 91 % of their theoretical maximum. The V_M was 3.4 V after the cycling tests (1-3) and 3.7 V, after all stress tests (1-5), a cumulative variation smaller than 12% from its original value, with N_{ML} and N_{MH} values of 2.49 V and 3.33 V, respectively. This variation increases the N_{ML} by 14 %, moving V_M closer to its ideal value without compromising the steepness of the transition. The shift of V_M is consistent to differences in the sign of the variations of I_{DS} during DC bias stress. The inset of Fig. 3 shows that as I_{DS} increases on the *p*-channel TFTs, the resistance of this channel is reduced while a decrease of I_{DS} increases the resistance of the *n*-channel TFTs, thereby causing V_M to shift closer to its ideal value and increasing the noise margins of the inverter.

Finally, Fig. 3(c) shows selected *VTC* characteristics for an inverter subjected to 200 continuous forward and backward *VTC* cycles during a period of 6 h. Consistent with our prior observations, the *VTC* characteristics exhibited a positive shift of the V_M without a serious change of steepness or dc gain value. As shown on the inset of Fig. 3(c), during this time, V_M did not follow a monotonic increase but rather seem to be asymptotic in nature, with progressively smaller changes as the inverter undergo more stress cycles. This shift of V_M increases the overall noise margin of the inverter, reaching maximum values of N_{ML} and N_{MH} for the 200$^{\mathrm{th}}$ forward and backward *VTC* cycles. Interestingly, as shown in Fig. 3(c), upon disconnecting the inverter for 20 h, the *VTC* characteristics of the inverter recovered and became close to their original values. After recovery of the *VTC* characteristics, threshold voltage and mobility values of *p*- and *n*-channel TFTs are comparable to their initial values. We should note, that the variations of the *VTC* characteristics under continuous inverter operation described here are small, particularly considering that gain and noise margins are the most important performance parameters of an inverter. However, from these experiments it is clear that to improve the operational stability of V_M further, the rate of change of I_{DS} (magnitude and sign) during DC bias stress test of both transistors would have to be better matched. Further optimization of the processing conditions and the widths and lengths of the TFTs could allow V_M to be closer to $0.5V_D$, the ideal value, and to achieve high and balanced noise margins. As we have shown,[15] in top-gate transistors with the proposed geometry, control over the rate of change of I_{DS} can easily be achieved by varying the thickness ratio between CYTOP and Al_2O_3 in the bi-layer geometry to improve the stability of the inverter.

In summary, we demonstrated top-gate pentacene and amorphous InGaZnO TFTs and complementary inverters that use an amorphous fluoropolymer (CYTOP) and high-k (Al_2O_3) bi-layer

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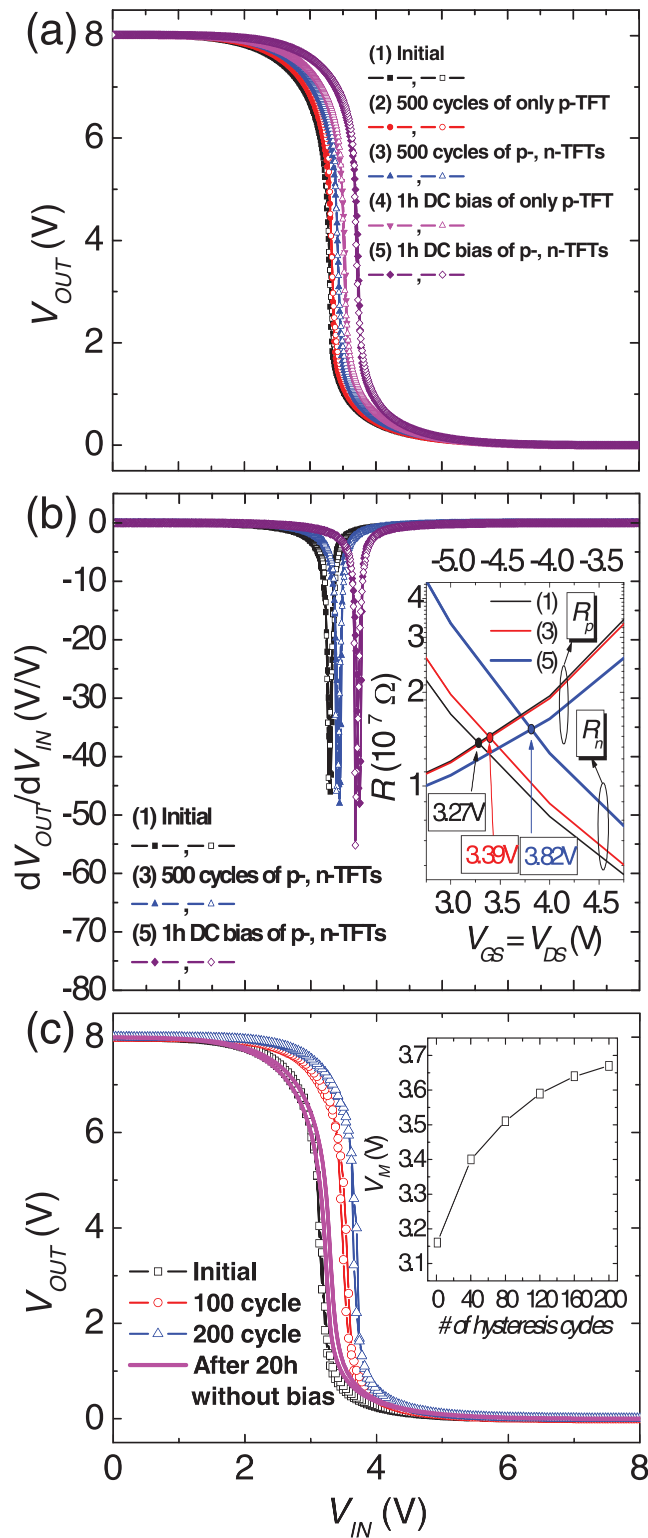

FIG. 3. (a) and (b) Voltage transfer characteristics and static gains of the hybrid complementary inverter before stress and after 500 multiple cycles of transfer curves and after 1 h DC bias stress of *p*- and *n*-channel TFTs. (Inset: Resistances of *p*- and *n*-channel TFTs before stress and after 500 multiple cycles of transfer curves and after 1 h DC bias stress.) (c) Voltage transfer characteristics during 200 times continuous hysteresis cycles of the hybrid complementary inverters.

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gate dielectric layer to achieve good operational stability. The *p*-channel pentacene and *n*-channel *a*-IGZO TFTs showed hysteresis-free current voltage characteristics and high electrical stability with very small variations under continuous multiple scans up to 500 cycles and after continuous DC bias stress for 1 h at gate-to-source and drain-to-source voltages of 8 V. The inverters yielded hysteresis-free voltage transfer characteristics with static DC gain values larger of -45 V/V and switching threshold voltages of 3.3 V at a supply voltage of 8 V. Although the small changes in the channel resistance of the TFTs upon the different conditions of bias stress had additive effects, due to the differences in the sign of change of I_{DS}, the switching threshold voltage varied less than 12% after all the different bias stress tests were conducted. Therefore, the use of bi-layer gate dielectrics in top-gate TFT geometries seems to be a promising way to realize hybrid complementary inverters that operate at low voltages with high operational stability.

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