

**Modeling of Simultaneous Switching Noise in On-Chip and
Package Power Distribution Networks Using Conformal
Mapping, Finite Difference Time Domain and Cavity
Resonator Methods**

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**Modeling of Simultaneous Switching Noise in On-Chip and
Package Power Distribution Networks Using Conformal
Mapping, Finite Difference Time Domain and Cavity
Resonator Methods**

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Dedicated to
献给

my father, Liming Mao
我的父亲, 毛黎明

my mother, Zujuan Zhu
我的母亲, 朱祖娟

my sister, Yanling Mao
我的妹妹, 毛燕凌

for their love and support
为了他们对我的爱和支持

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CHAPTER I

INTRODUCTION

The rapid advance in semiconductor technology is pushing high-performance electronic systems toward higher operating frequency, higher power dissipation, and lower supply voltage, which pose tremendous challenges for designers. The number of failures caused by signal and power integrity problems is on the rise because existing design tools and methodologies cannot address these issues effectively. Signal integrity refers to a broad set of interconnect design issues, such as impedance mismatch, crosstalk noise, differential transmission lines, etc. On the other hand, power integrity refers to a set of power supply design issues, such as resonance, IR voltage drop, electromigration, simultaneous switching noise (SSN), etc. Analyzing signal and power integrity problems is important for meeting the design specifications since incorporating signal and power integrity analysis into the system design flow has become a necessity. In fact, the 2002 international technology roadmap for semiconductors (ITRS) lists power noise management as one of the key challenges facing the semiconductor industry in the future [1]. A typical power distribution network (PDN) for a high speed electronic system contains voltage regulator modules (VRM), decoupling capacitors, printed circuit boards (PCBs), packages and on-chip power grids, as shown in Fig. 1. The topic of this thesis is on modeling and simulation of simultaneous switching noise in packages as well as integrated circuits (ICs) and the focus is mainly on the latter.

According to R. Senthinathan and J. L. Prince [2], simultaneous switching noise (also known as delta-I noise or ground bounce) is “a voltage glitch induced at the chip-package power distribution connections, due to an inductively induced voltage drop, when internal gates and/or output drivers switch simultaneously.” For high-speed design, SSN has certain deleterious effects on circuit performance. It can destroy the digital information carried by the node in the circuit, result in incorrect state stored in a latch, and ultimately affect digital functionality. When noise acts simultaneously with a switching node, this leads to a change

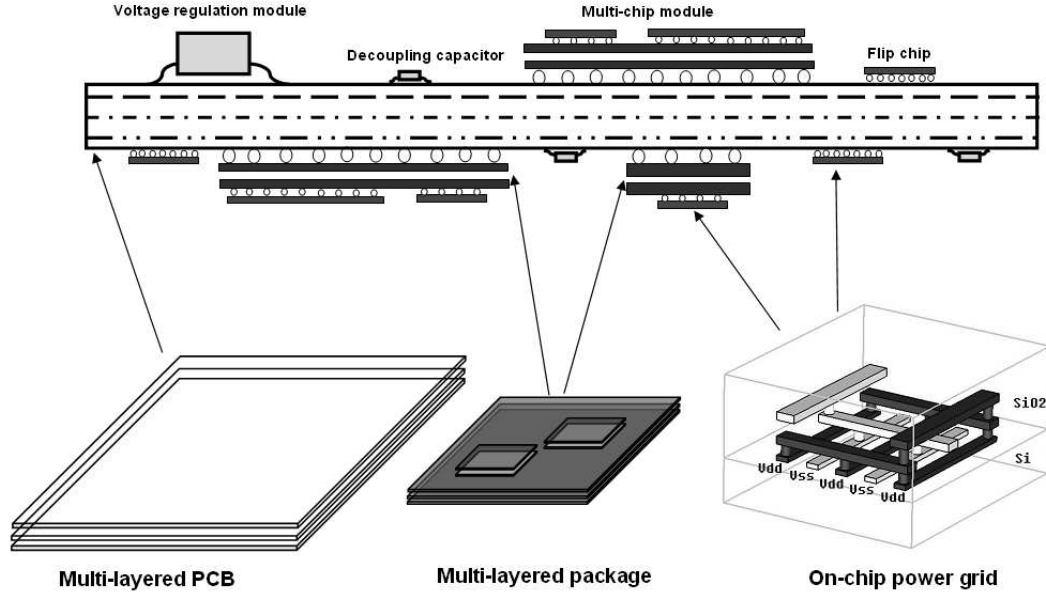


Figure 1: Power distribution network of electronic systems

in the timing of the transient signal, which causes large delay and skew variations. In mixed-signal integrated circuits, the noise injected into the substrate or common power network can deteriorate the performance of sensitive analog parts, such as RF circuits. Nowadays, in deep submicron circuits, in order to manage the power distribution and achieve a sound and robust quality design, accurate techniques and efficient methodologies for modeling power distribution networks are required for analyzing power supply noise.

1.1 Available methods for modeling power distribution networks

In the literature, different methodologies have been adopted for analyzing SSN by various authors. Several important approaches are illustrated in Fig. 2.

Measurement-based techniques verify the soundness of the system by directly measuring the device-under-test (DUT) in the frequency domain or time domain or both. Equipment such as network analyzer (NA) and time domain reflectometry (TDR) have been used for power distribution measurements in [3]. The measurement data has been processed to extract the model of DUT and has been correlated with the simulation results to validate

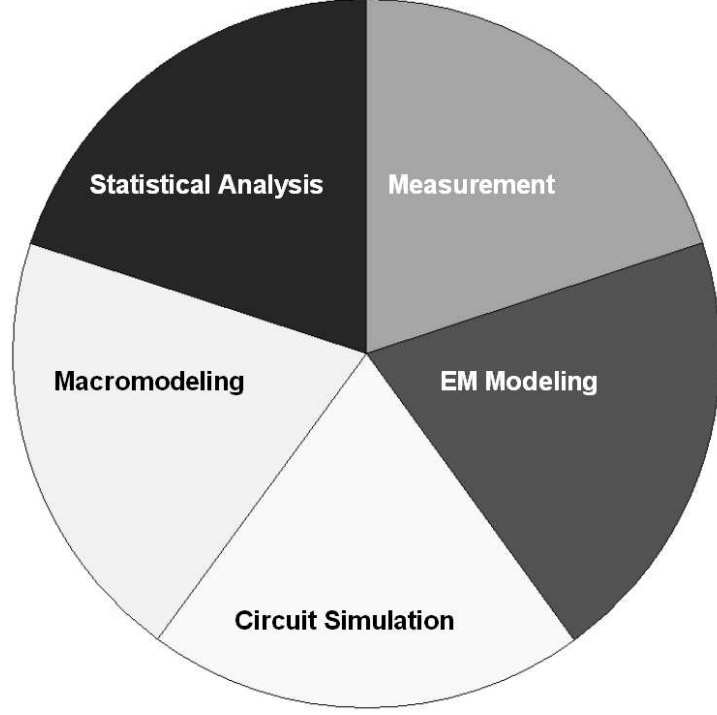


Figure 2: Different methods used for power integrity analysis

the design.

Statistical analysis explores the relation between noise performance and design variations, for which a parametric diagnosis methodology has been developed [4]. It has been successfully applied on high-speed digital systems as well as embedded RF passive circuits.

Macromodeling denotes a black-box representation of the frequency response of distributed networks, which captures the behavior of the passive structure at the input/output ports [5]. The macromodel can be constructed using two methods. One method is to construct the macromodel from the moments that are the characteristics of the circuit. In [6]–[8], explicit or implicit moment-matching techniques have been used to construct the macromodel by generating and matching the moments using Padé approximation. The other method is to capture the frequency dependent data using a macromodel after extracting the port behavior of the circuit either from an electromagnetic simulator or from measurements. In [9]–[14], the macromodel has been constructed by capturing measured or simulated frequency data using least squares approximation [9]–[11] and vector fitting [12]–[14].

Recently, the multiport passivity formulae have been derived and band division method has been developed by S. H. Min to construct passive and broadband macromodels [5], which have been realized into a software named Broadband Efficient Macromodeling Program (BEMP).

Circuit simulation plays a crucial role in power/signal integrity analysis. In high-speed digital systems, parameters such as delay and peak-to-peak noise magnitude, are the key criteria to evaluate the design. Hence, time domain simulation algorithms and methodologies have been a topic of intense research for many years. A critical issue in circuit simulation is the solution of large size networks, which can contain millions of nodes. Thus, efficient algorithms have been studied to solve this problem, such as finite difference time domain (FDTD) method [23].

Electromagnetic (EM) modeling of the power distribution networks is one of the most challenging tasks in microelectronics package design. Though the physics of the electromagnetism has been well defined, there are various practical modeling strategies required for different power distribution structures. At the same time, to reduce the design cycle for high speed electronic products, faster and more accurate EM modeling tools are required. Therefore, different numerical methods, such as finite element method (FEM) [114], and analytical techniques, such as spectral domain approach (SDA) [70], have been used for EM modeling.

The aforementioned methods are not isolated from each other. In fact, in the practical design phase, they are used together to accomplish the design goal. For example, the frequency response of a power distribution network from EM modeling can be fed into a macromodeling tool, which provides a circuit representation for simulation. Afterwards, the time domain waveform can be correlated with the measurement data from Time-Domain Reflectometry (TDR). The discrepancy between measurement and design can be used to diagnose the manufacturing and operational variations, which can be tuned to increase the yield and significantly reduce design iteration cycles. Each of the approaches mentioned above for solving the power integrity problem is of similar importance. This dissertation addresses mainly the EM modeling and time domain simulation of SSN in packages and

PCBs as well as ICs. First, the modeling of multilayered planar structures in PCBs/packages is discussed in Section 1.2, and then the modeling of on-chip power distribution network is discussed in Section 1.3.

1.2 Modeling of multilayered power and ground planes

PCBs and MCMs use stacked multilayered planes to provide power to ICs. Since power supply noise is increasingly becoming one of the dominant limitations to system performance and cost, characterization of such a multilayered structure has been a topic of intense research since the 1980s [15], drawing the attention of both the industry [16]– [20] and research institutions [21]– [23].

A simple expression has been used to explain and estimate SSN [2] given by:

$$V_{\Delta I} = N L_{eff} \frac{di}{dt}$$

where di/dt denotes the current slew rate of a single driver; N denotes the number of drivers that switch simultaneously; L_{eff} denotes the effective inductance of the power distribution system which accounts for the entire inductance of the current loop in the package as well as PCB. Nevertheless, as the operating frequency goes higher, a single inductance can no longer represent the complex packaging structure. Hence, different methodologies and algorithms [2]– [51] have been proposed and applied for modeling the power distribution of high speed systems. Each of the following methods is briefly described in the successive subsections, namely, inductor network method [2]– [26], transmission line method [27]– [32], transmission matrix method [36]– [40], finite difference time domain method [33]– [34], and cavity resonator method [41]– [51].

1.2.1 Inductor network method

In the early 1990s, University of Arizona led by Professor John Prince developed methods for the modeling of power/ground planes using an inductor network [24]– [26]. The inductances were calculated using the following steps:

1. Electric potential ϕ was calculated by solving Laplace’s equation (1.1a) inside the power plane with the boundary condition (1.1b) enforced at the plane peripheries.

2. Current density J and magnetic vector potential A were calculated from ϕ using the expressions (1.1c) and (1.1d),
3. Resistance R and inductance L were calculated from (1.1e) and (1.1f).

The critical equations used by University of Arizona can be written as:

$$\nabla^2 \phi = 0 \quad (1.1a)$$

$$\frac{\partial \phi}{\partial n} = 0 \quad (1.1b)$$

$$J = -\sigma \nabla \phi \quad (1.1c)$$

$$A = \mu \int_v J(r') G(r|r') dv' \quad (1.1d)$$

$$R|I_{tot}|^2 = \frac{1}{\sigma} \int_v J^* \cdot J dv \quad (1.1e)$$

$$L|I_{tot}|^2 = \text{Re} \frac{1}{\sigma} \int_v J^* \cdot A dv \quad (1.1f)$$

where σ is the conductivity of the plane, J^* denotes the complex conjugate of the current density J and $G(r|r')$ denotes the free-space Green's function given by

$$G(r|r') = \frac{1}{4\pi |r - r'|} \quad (1.2)$$

This method has been applied on both solid and perforated planes. A copper plane with area of 3 cm \times 3 cm and thickness of 0.05 cm has been modeled in [2]. The source at the center of this plane was represented as a single port and eight sink ports were placed around the source point, as shown in Fig. 3. The inductances calculated using the method described above is given by:

$$[L'_{ij}] = \begin{pmatrix} 14.07 & 7.10 & 5.74 & 4.85 & 4.71 & 4.85 & 5.74 & 7.10 \\ & 12.28 & 7.10 & 5.47 & 4.85 & 4.55 & 4.85 & 5.47 \\ & & 14.07 & 7.10 & 5.74 & 4.85 & 4.71 & 4.85 \\ & & & 12.28 & 7.10 & 5.47 & 4.85 & 4.55 \\ & & & & 14.07 & 7.10 & 5.74 & 4.85 \\ & & & & & 12.28 & 7.10 & 5.47 \\ & & & & & & 14.07 & 7.10 \\ & & & & & & & 12.28 \end{pmatrix} (nH) \quad (1.3)$$

Since the system was reciprocal and the inductance matrix was symmetric, only half of the matrix is shown. The identical plane with the perforation as shown in Fig. 4 has been modeled to study the effects of perforation on inductor network. The elements of inductor network for the perforated plane are given in (1.4). It can be observed that the self and mutual inductances are larger in (1.4) than those in (1.3), which is attributed to the perturbation of current distribution on the plane caused by perforations.

$$[L_{ij}] = \begin{pmatrix} 15.01 & 8.59 & 6.18 & 4.93 & 4.94 & 5.04 & 6.01 & 7.53 \\ & 14.62 & 8.54 & 6.17 & 5.72 & 5.00 & 5.28 & 6.12 \\ & & 14.95 & 7.50 & 6.44 & 4.90 & 4.54 & 4.83 \\ & & & 12.58 & 7.81 & 5.05 & 4.41 & 4.28 \\ & & & & 15.93 & 6.29 & 5.31 & 4.65 \\ & & & & & 12.61 & 7.34 & 5.62 \\ & & & & & & 14.00 & 7.15 \\ & & & & & & & 12.41 \end{pmatrix} (nH) \quad (1.4)$$

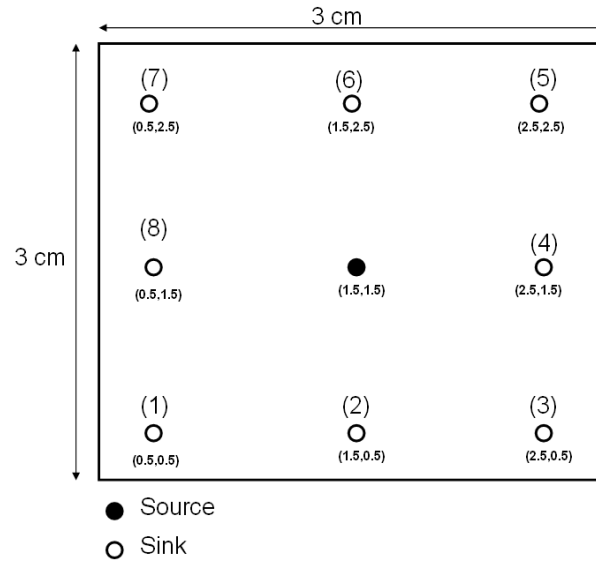


Figure 3: Solid plane with eight sink ports

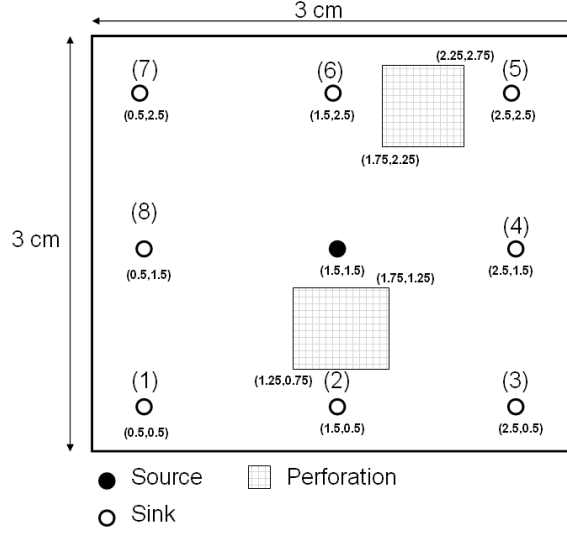


Figure 4: Perforated plane with eight sink ports

This method is quite efficient and easy for implementation. However, due to the assumptions made during the derivation, there are several deficiencies in this method which can be listed as:

- The elements of inductor network are constant over the entire frequency range, because skin effect is assumed to be negligible. Hence, there is no frequency dependent inductance in the result, which limits the application of this method at high frequency, where frequency dependent parameters are essential for the accuracy of analysis.
- The property of the material between power and ground planes is not included in the derivation, and therefore dielectric loss is not included in the model.
- Since the construction of inductor network is based on the solution of Laplace's equation, which is a quasi-static approximation of the full-wave phenomenon, it cannot capture the behavior of multi pole-zero system response and plane resonances in packages.

1.2.2 Transmission line method

Power planes have been modeled using lumped elements in the previous subsection. However, this method can only be applied on the system in which the rise-time of digital signal is much longer than the propagation time across the plane. To overcome this limitation, transmission line (TL) method was proposed in [27], which used a two-dimensional array of transmission lines for approximating a plane pair, as shown in Fig. 5. The characteristic impedance Z_0 , propagation velocity V_0 and propagation constant γ_0 of each transmission line are calculated using the following expressions:

$$Z_0 = \sqrt{2 * L / C} \quad (1.5a)$$

$$V_0 = \sqrt{2 / (L * C)} \quad (1.5b)$$

$$\gamma_0 = \varpi / V_0 \quad (1.5c)$$

$$L = \mu d \quad (1.5d)$$

$$C = \varepsilon \frac{l^2}{d} \quad (1.5e)$$

where ε , ϖ , l and d are permittivity of dielectric, angular frequency, side dimension of the cell, and thickness of dielectric, respectively. The factor of two is added in the equations in order to compensate for the double counting of the plane capacitance C in the array of the transmission lines.

Transmission line method can be used for modeling rectangular and arbitrarily shaped planes. The transmission line model of a rectangular plane pair has a uniform layout as shown in Fig. 6(a), while the model of an arbitrarily shaped plane pair has a sawtooth-like approximation, as shown in Fig. 6(b).

A test vehicle with a thick-film substrate as show in Fig. 7 was fabricated and measured [27]. Two planes are separated by alumina with thickness of $280 \mu m$ in Fig. 7. The relative dielectric constant was 9.6 and sheet resistivity of the metal plane was $1.6 \times 10^{-3} \Omega/\text{square}$. Frequency response from 50 MHz to 20 GHz was measured for this test vehicle using a vector network analyzer (HP8510C). The transmission line model similar to Fig. 6(a) was fed into a SPICE-like simulator which generated S-parameter at two measurement ports, as shown in Fig. 7.

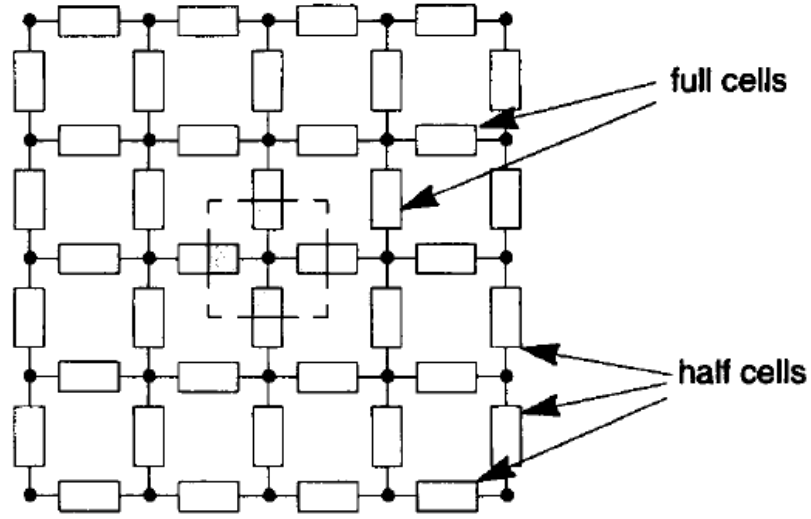
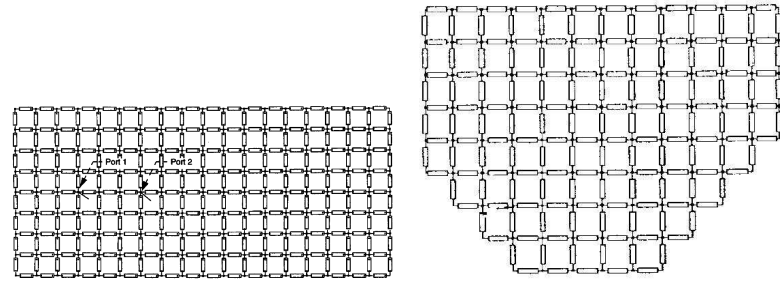


Figure 5: Transmission line model for power planes



(a) TL model of a rectangular plane (b) TL model of an arbitrarily plane

Figure 6: Transmission line model of (a)a rectangular plane, (b)an arbitrarily plane

The S-parameter, S_{11} and S_{12} , from transmission line model and measurement are correlated in Fig. 8. It is evident that simulation matches measurement very well up to 10 GHz. The discrepancy between two curves above 10 GHz is due to the negligence of frequency dependent property of conductors and dielectric losses in the transmission line model.

Transmission line method has been modified to improve its accuracy in [28]. Instead of lossless transmission line, lossy transmission line is used as unit cell of the two-dimensional

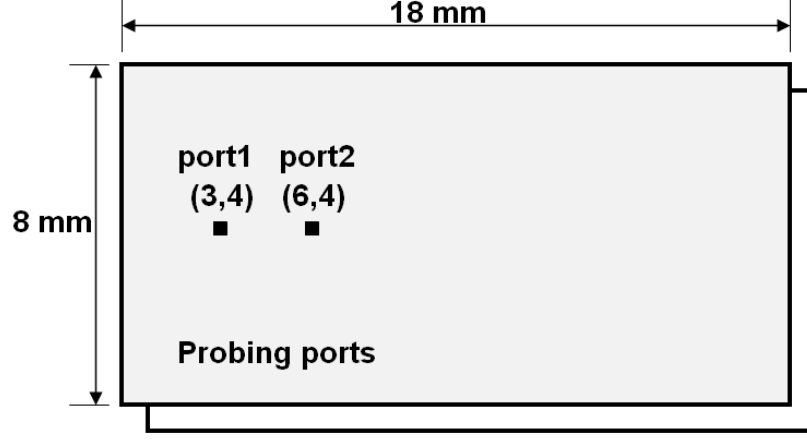


Figure 7: Test vehicle of transmission line method

array. The parameters of a lossy transmission line are calculated using the follows expressions:

$$Z_0 = \sqrt{2Z_l/Y_c} \quad (1.6a)$$

$$\gamma_0 = \sqrt{Z_l Y_c/2} \quad (1.6b)$$

$$Z_l = R_s + j(\omega L + X_s) \quad (1.6c)$$

$$Y_c = G_d + j\omega C \quad (1.6d)$$

where G_d is the shunt conductance of the dielectric layer. Z_0 is complex characteristic impedance and γ_0 is complex propagation constant, which include both conductor loss and dielectric loss. The terms R_s and X_s are given by:

$$R_s = R_{hf} * (1 - e^{-A} * (\cos(A) - \sin(A))) / den \quad (1.7a)$$

$$X_s = R_{hf} * (1 - e^{-A} * (\cos(A) + \sin(A))) / den \quad (1.7b)$$

$$den = 1 - 2 * e^{-A} * \cos(A) + e^{-2A} \quad (1.7c)$$

$$A = t/\delta \quad (1.7d)$$

$$R_{hf} = 2l/(\sigma * \delta * w) \quad (1.7e)$$

$$\delta = 1/\sqrt{\pi f \mu_0 \sigma} \quad (1.7f)$$

where σ , t , l , w , δ , and A denote conductivity, thickness of the plane, length of the unit,

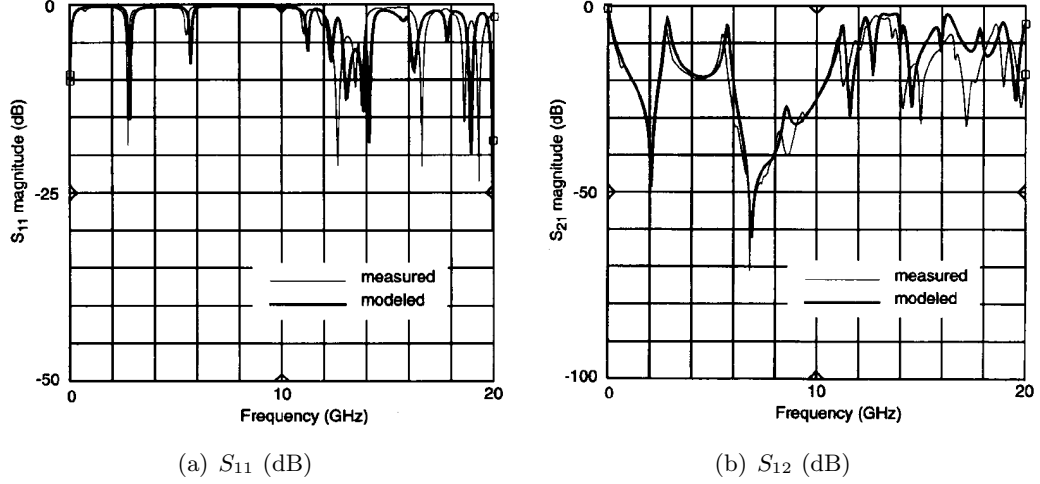


Figure 8: Measurement and TL model correlation (a) S_{11} , (b) S_{12}

width of the unit, skin depth and ratio of metal thickness to skin depth.

Including conductor and dielectric loss in the lossy transmission line, the modified transmission line model provides more accurate S-parameters for the test vehicle in Fig. 7 and the S-parameter matched the measurement very well up to 20GHz [28].

Transmission line model is able to predict the dominant TEM mode, and resonance frequency of the power and ground planes. It has advantages such as 1) compatibility with general SPICE-like circuit solvers, and 2) easy to incorporate decoupling capacitor and other active devices. Nevertheless, this approach also has several shortcomings which can be listed as:

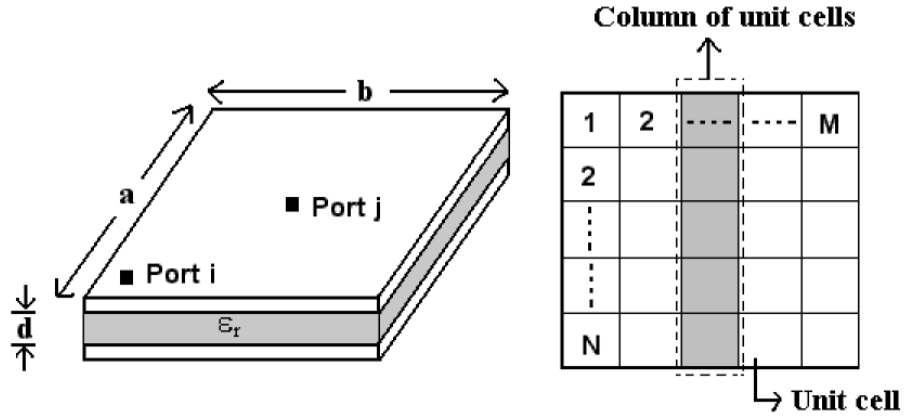
- Non-TEM mode at high frequency is neglected in the model, especially at the peripheries and corners of the planes. Hence, the application of transmission line method is limited by the spectrum of the switching signal.
- Radiation from the edges of power planes is neglected in the model. Therefore, the transmission line method is not suitable for modeling the electromagnetic interference (EMI), such as the noise coupled among different power supplies in a mixed-signal environment.
- The ports for measurement can be chosen only at the discrete junctions where the

transmission lines meet. Though this problem can be partially solved by using a nonuniform discretization technique, the cost of increased complexity is high.

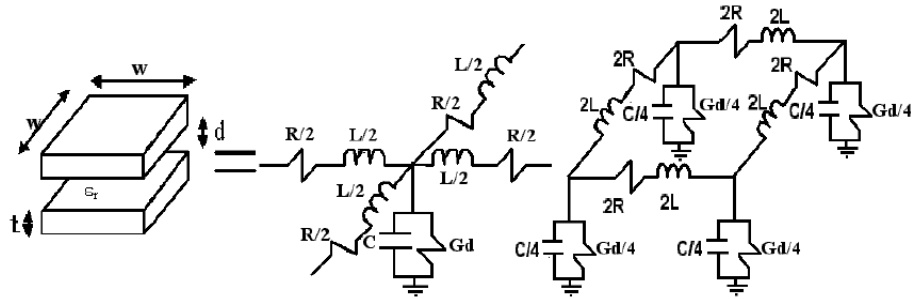
- Transmission line model is not very efficient for simulation, because a SPICE-like simulator takes more computational resources to solve transmission line than lumped elements. This approach can lead to long simulation time for a large array of transmission lines.

1.2.3 Transmission matrix method

Proposed in [35]– [40], transmission matrix method (TMM) is an efficient approach for analyzing arbitrarily shaped, electrically large power distribution networks. In this method,



(a) Plane pair and unit cell



(b) Unit cell with T and Π model

Figure 9: TMM model (a) Plane pair and unit cell, (b) T model and Π model

power/ground planes are divided into unit cells, each of which can be represented by an

equivalent circuit with R, L, C, and G elements. Every unit cell can be represented by either a T or Π model as shown in Fig. 9(b).

Provided the dielectric thickness d is much less than the size of a plane, a and b , the value of elements in a unit cell can be obtained from the following expressions:

$$C = \epsilon_0 \epsilon_r \frac{w^2}{d} \quad (1.8a)$$

$$L = \mu_0 d \quad (1.8b)$$

$$R_{dc} = \frac{2}{\sigma t} \quad (1.8c)$$

$$R_{ac} = 2\sqrt{\frac{\pi f \mu_0}{\sigma}}(1 + j) \quad (1.8d)$$

$$G_d = \varpi C \tan(\delta) \quad (1.8e)$$

where w , d , ϵ , $\tan(\delta)$, t , σ denote the lateral dimension of a unit cell, separation between planes, dielectric constant, loss tangent of dielectric, thickness and conductivity of metal planes. The parameter R_{dc} is the resistance of power and ground planes at DC, for which uniform cross-section is assumed. The AC resistance R_{ac} accounts for the skin effect on both metal planes and the shunt conductance G_d represents the dielectric loss. Using SPICE-like simulator to solve a large network containing hundreds of cells is time consuming. Instead, TMM suggests an efficient alternative, which is based on a multi-input/multi-output (MIMO) transfer function.

A column of cells ($N \times 1$ unit cells) among the $N \times M$ unit cells for a rectangular plane, as shown in Fig. 9, can be represented by a $2N \times 2N$ matrix, representing a subsystem with N input ports and N output ports. The MIMO schematic is shown in Fig. 10, where the input and output ports are indexed from 1 to N on the left side and from $N + 1$ to $2N$ on the right side, respectively. The relationship between node voltages and port currents of a $2N$ -port subsystem is given by:

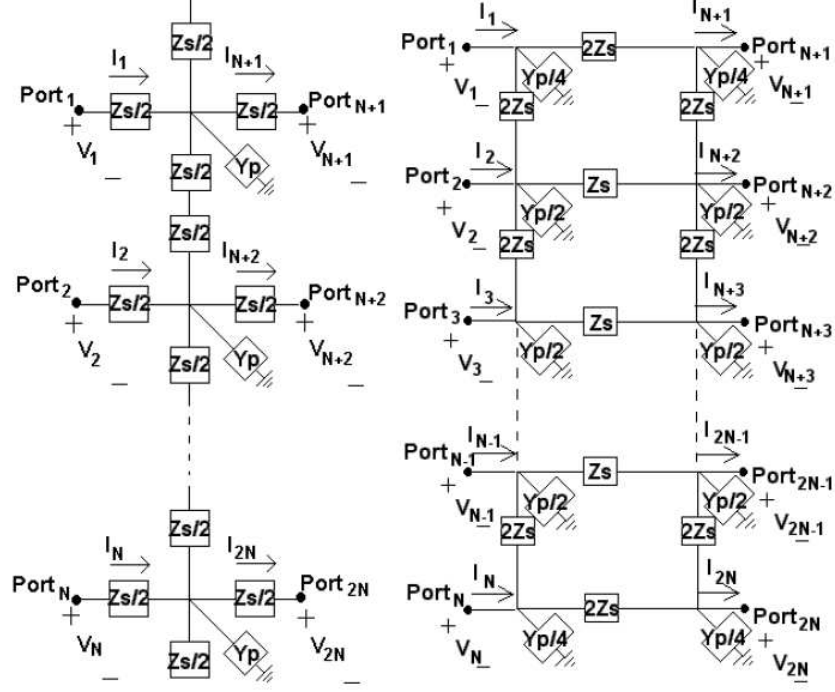


Figure 10: Equivalent circuit for a column of unit cells

$$[h] \begin{bmatrix} V_1 \\ \vdots \\ V_N \\ \dots \\ I_1 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} T_{1,1} & \dots & T_{1,N} & \vdots & T_{1,N+1} & \dots & T_{1,2N} \\ \vdots & & \vdots & \vdots & \vdots & & \vdots \\ T_{N,1} & \dots & T_{N,N} & \vdots & T_{N,N+1} & \dots & T_{N,2N} \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ T_{N+1,1} & \dots & T_{N+1,N} & \vdots & T_{N+1,N+1} & \dots & T_{N+1,2N} \\ \vdots & & \vdots & \vdots & \vdots & & \vdots \\ T_{2N,1} & \dots & T_{2N,N} & \vdots & T_{2N,N+1} & \dots & T_{2N,2N} \end{bmatrix} \begin{bmatrix} V_{N+1} \\ \vdots \\ V_{2N} \\ \dots \\ I_{N+1} \\ \vdots \\ I_{2N} \end{bmatrix} \quad (1.9)$$

The representation for a power plane, which is modeled as a cascade of M subsystems, is obtained by multiplying the matrices of all the columns, generating a $2N \times 2N$ matrix as well [35]. Since the matrices for every column of unit cells are same, the size and sparsity of the matrix are retained. The cascading process is shown in Fig. 11 and the matrix multiplication is given by:

$$[T'] = [T_l] [T_m] [T_n] \quad (1.10)$$

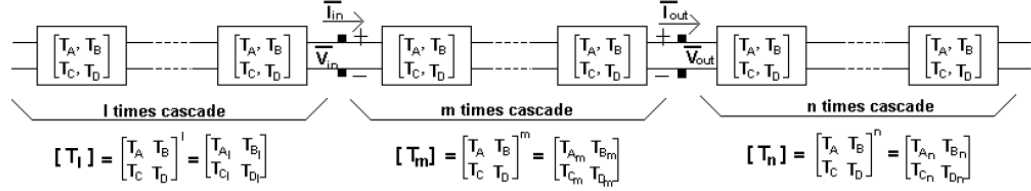


Figure 11: Cascading of columns of cells

Once the transfer matrix of entire network is computed, it can be converted into scattering matrix $[S]$, admittance matrix $[Y]$, or impedance matrix $[Z]$ by performing certain matrix operations.

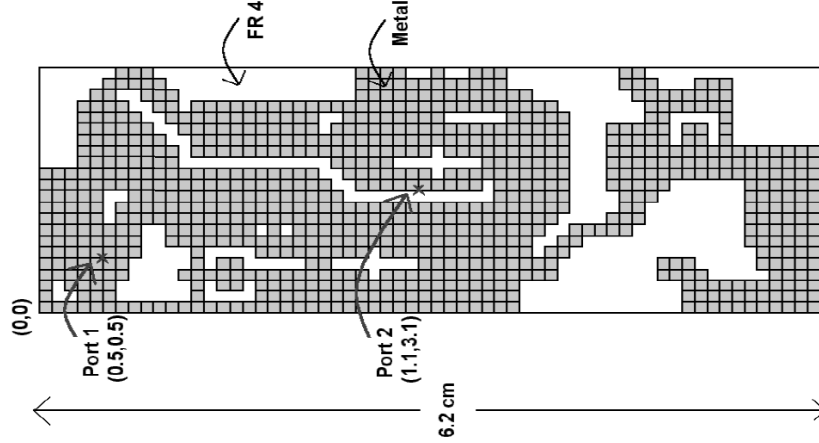


Figure 12: Top view of Motorola Bravo Plus pager power plane

TMM has been applied on different applications such as multilayered planes and irregular shaped planes. A Motorola Bravo Plus pager was selected as an example of irregular geometry [35] whose top view is shown in Fig. 12. The system consists of 20 mm thick copper planes with conductivity $\sigma = 5.8 \times 10^7$ S/m and 200 mm thick FR-4 with a relative dielectric constant of 4. The dielectric loss tangent, $\tan(\delta)$, is 0.02 at 5 GHz. Port 1 and 2 are chosen at (0.5cm, 0.5 cm) and (1.1 cm, 3.1 cm), respectively, with the origin defined at the bottom left corner. Unit cell of size 0.1cm \times 0.1cm was used in TMM and the self and transfer impedance are shown in Fig. 13.

The advantages of TMM method are flexibility and efficiency which can be described as

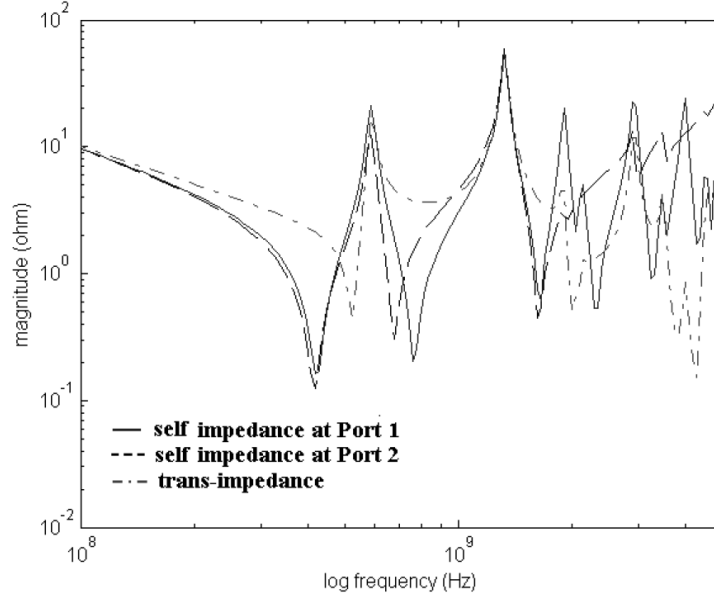


Figure 13: Impedance of Motorola pager

follows:

- It builds the frequency domain MIMO model of the plane pair without doing tedious electromagnetic simulation, for which closed-form expressions of elements and efficient matrix operations are used.
- With macromodeling technique, TMM can be used for time domain simulation with ease [35].
- TMM requires less memory and less CPU time than SPICE-based simulators. In fact, a speedup in the range of $7\times$ – $13\times$ has been reported by using TMM [35].

The imperfection in TMM is that the model of cells at the plane boundary does not include higher modes of the EM wave. Hence, the reflection and the loss due to radiation are ignored in TMM. Including all the effects of discontinuity on the power plane in the TMM model could improve its accuracy and make it more practical.

1.2.4 Modeling the power planes with FDTD method

Applying the finite difference approximation to Maxwell's equation can be traced back to 1966 [62] when K. S. Yee used it to solve the electromagnetic problem in isotropic

media. Since then, tremendous modifications and improvements have been made to FDTD algorithm with appropriate absorbing boundary conditions [65]. The applications of FDTD are broad, such as antennas and wireless and microwave circuit components. Using FDTD to solve the power plane problem [33]– [34] is simply an application of a general solver on the special geometry and boundary conditions, though the algorithm has been modified to be more adaptive to the arbitrary shape of planar structures [33].

The advantage of FDTD is that the propagation of power supply noise can be observed in 3-D space, which provides designers an intuitive cognition of the noise distribution versus the location. The essential drawback of FDTD is computational inefficiency, because the unknowns E_x, E_y, E_z, H_x, H_y and H_z are distributed in the entire domain of the problem, which are updated at each time step. In order to obtain the frequency domain response from FDTD simulation using Fast Fourier Transform (FFT), the simulation has to be carried out for sufficient time so that the error introduced by truncating the waveform is limited. For a power distribution system which resonates, it takes very long time (many time steps) for the field to arrive at a steady state. Besides, since the variables in the circuit simulator are V and I , the interface between FDTD method and the circuit simulator is relatively complex.

1.2.5 Cavity resonator method

Cavity resonator method (CRM), as indicated by its name, captures the resonance of a cavity formed by power and ground planes in PCBs/packages [41]– [50]. It is based on the analytical solution of the impedance at the ports on regular plane pairs, which has been represented as a sum of an infinite number of propagation modes [21].

A typical rectangular plane pair is shown in Fig. 14, which consists of two planes of dimensions $a \times b$, separated by a dielectric of thickness d and permittivity ε . Under the condition that $d \ll a, b$ and $d \ll \lambda$ (wavelength), the major field components are E_z, H_x and H_y and the other field components, H_z, E_x and E_y , are assumed to be zero. Therefore, Maxwell's equations are simplified as a two-dimensional wave equation–Helmholtz equation

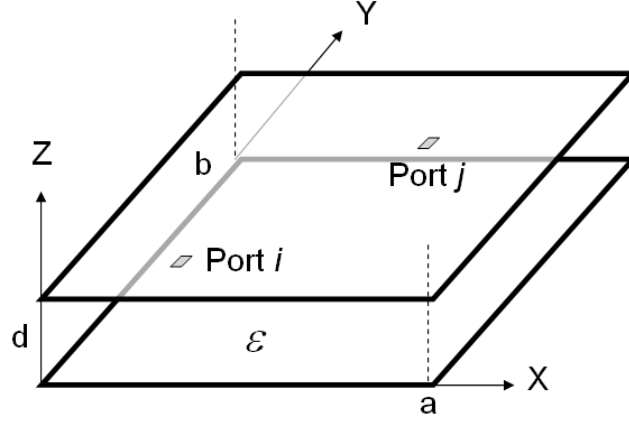


Figure 14: Plane pair structure

[41]:

$$(\nabla^2 + k^2)E_z = 0, \nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \quad (1.11)$$

In Eq. (1.11), the wave number k is a complex value such that $k = k' - jk''$ where $k' = \varpi\sqrt{\mu\epsilon}$ and $k'' = \varpi\sqrt{\mu\epsilon}(\tan\delta + r/d)/2$. The parameters ω , μ , δ and σ denote the angular frequency, permeability of the dielectric, loss angle of the dielectric, and conductivity of the metallization, respectively. Parameter $r = \sqrt{2/\varpi\mu\sigma}$ denotes the skin depth of the conductor. The complex wave number accounts both the conductor and dielectric losses. Along the periphery of the plane pair, it is assumed that the electric field is perpendicular to the metal, which is a magnetic wall for E_z given by,

$$\frac{\partial E_z}{\partial n} = \frac{\partial V}{\partial n} = 0 \quad (1.12)$$

Equations (1.11) and (1.12) constitute an eigenvalue problem. For a rectangle plane pair, the eigenvalues have two sets of infinite discrete values: $K_x = \frac{m\pi}{a}, K_y = \frac{n\pi}{b}$, where (m, n) is the index of propagating modes in the cavity. The corresponding eigenfunctions

are

$$\phi_{mn}(x, y) = \frac{\varepsilon_m \varepsilon_n}{\sqrt{ab}} \cos \frac{m\pi x}{a} \cos \frac{n\pi y}{b} \quad (1.13a)$$

$$\varepsilon_m = \begin{cases} 1, m = 0 \\ \sqrt{2}, m \neq 0 \end{cases} \quad (1.13b)$$

$$\varepsilon_n = \begin{cases} 1, n = 0 \\ \sqrt{2}, n \neq 0 \end{cases} \quad (1.13c)$$

Using the above eigenvalues and eigenfunctions, the impedance between ports i and j can be represented as:

$$Z_{ij} = j\varpi\mu T \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{(k_{mn}^2 - k^2)ab} f(x_i, y_i) f(x_j, y_j) \quad (1.14a)$$

$$f(x_i, y_i) = \cos \frac{m\pi x_i}{a} \sin c \frac{m\pi t_{xi}}{2a} \cos \frac{n\pi y_i}{b} \sin c \frac{n\pi t_{yi}}{2b} \quad (1.14b)$$

where (x_i, y_i) and (x_j, y_j) are the coordinates of the port locations and (t_{xi}, t_{yi}) and (t_{xj}, t_{yj}) are the dimensions of the ports. In Eq. (1.14), $k_{mn}^2 = (m\pi/a)^2 + (n\pi/b)^2$ determines the poles and resonant frequency of the system. The expression (1.14) captures the behavior of radial waves between the plane pair, based on which the following work has been carried out:

- A technique which reduces the order of resonator modes from infinity to minimum – model order reduction (MOR) – has been developed [21]. This technique preserves the passivity of the network.
- Based on MOR, the equivalent circuit for plane pair has been extracted [21].
- Decoupling capacitors have been incorporated into the above equivalent circuit and the selection and placement of decoupling capacitors have been carefully studied for reducing SSN [23].
- Using segmentation technique, irregular shaped planes have been modeled [21].
- The effect of vias on switching noise has been quantified [22].
- A split plane with a transmission line has been modeled [22].

- The result from cavity resonator method has been correlated with measurement for a 20-layer functioning board [22]. The curves of SSN from modeling and measurement are shown in Fig. 15.

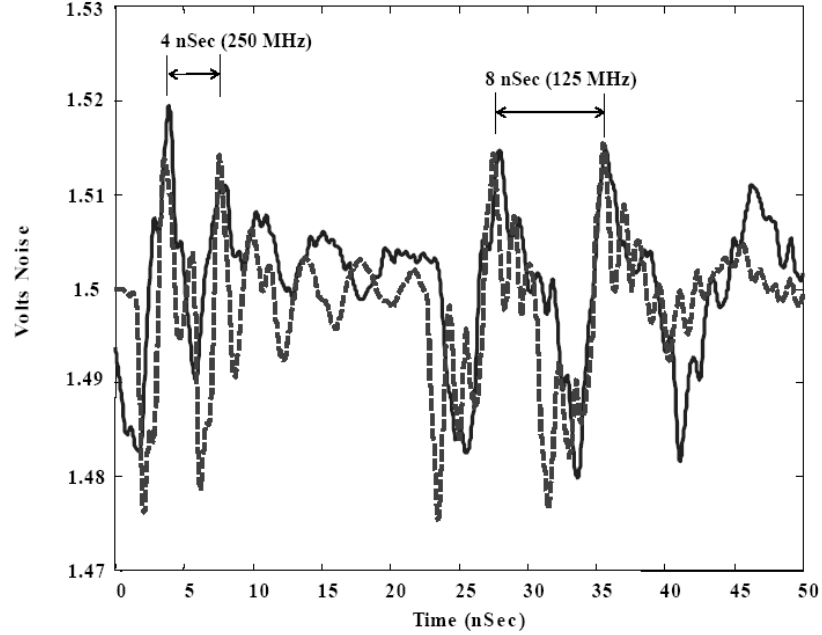


Figure 15: Modeling to hardware correlation for a functioning board

The pros and cons of this approach are as follows: 1) Analytical expressions for power planes have been obtained with clear physical insight. Using these expressions, it is easy to calculate the resonance mode of plane pair with a simple shape, such as rectangle, but it is relatively difficult for irregular shapes. 2) Due to the continuity of analytical solutions, ports can be placed at arbitrary locations on the plane and it does not require extra computational resources (memory and CPU time). 3) The equivalent circuit of cavity resonator method is compatible with general circuit simulators and it is quite easy to attach different devices to the equivalent circuit, such as transmission lines, I/O drivers, etc.

1.3 Modeling of on-chip power grid

Power distribution for very large scale integrated circuits (VLSI) has been investigated for many years [52]– [55]. As system-on-chip (SOC), deep submicron (DSM) technology, and

mixed-signal technique are being developed, designing and analyzing the power distribution network in ICs becomes a challenging task. A robust power network is essential to ensure the ICs operate reliably at the guaranteed level of performance. Switching activity of high-speed CMOS circuits produces large transient currents, which may generate large potential drops/surges owing to the parasitics of on-chip PDN. A poorly designed power network along with large switching currents may degrade IC performance and reliability.

The challenges of on-chip power grid analysis can be grouped into two categories: 1) on-chip interconnect modeling and 2) full chip power grid analysis, which is essentially a large network simulation problem. These two parts will be discussed in the following subsections.

1.3.1 Modeling of on-chip interconnect

Instead of planes, an on-chip power distribution system uses a metal grid to distribute power, which has a side view as shown in Fig. 16. The equivalent circuit of an entire grid is based on the accurate model of individual line.

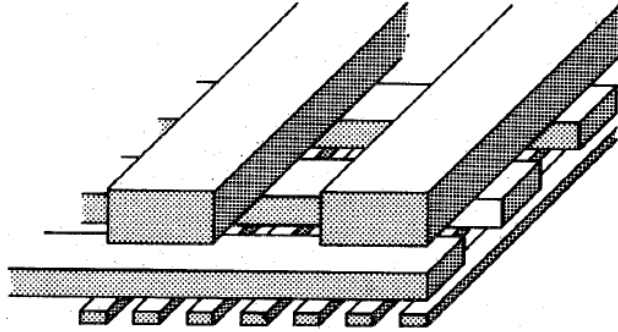


Figure 16: Side view of on-chip power grid

The modeling techniques of on-chip interconnect has followed in the steps of the semiconductor process and gate feature size. Historically, the gate parasitic impedances of transistors has been much larger than the interconnect parasitic impedance, since the gate geometries were quite large. This resulted in ignoring interconnect impedance and modeling it as a short circuit, as shown in Fig. 17(a). With the scaling of the gate feature size, interconnect capacitances became comparable to the gate capacitance, requiring the

interconnect to be modeled as a lumped capacitor that was added to the gate capacitor, as shown in Fig. 17(b). With the continuous increase in device densities, the interconnect density has also correspondingly increased. The cross-sectional area of interconnects was reduced to provide more interconnect per unit area. Simultaneously, the global wires connecting modules across an integrated circuit has increased in length. Both the decreased cross-sectional area and the increased wire length caused the global wire resistances to dramatically increase. As shown in Fig. 17(c), the resistance of the interconnect was then included in interconnect model–RC model, which had greatly complicated the analysis of circuits. While represented as a short-circuit or a capacitive model, the interconnect could be modeled as a single node, nevertheless, by including the series resistance, the interconnect was composed of multiple nodes and, thus, the size of the network expanded significantly. Due to the shorter signal rise time and changing inductance/resistance ratio imposed by technology scaling, the RC model became inadequate and on-chip inductive elements had to be taken into account, leading to the RLC model, as shown in Fig. 17(d). The transition of the on-chip interconnect model from R to RLC changed all aspects of the design and analysis of integrated circuits [89].

To extract the RLC model of on-chip traces, finite difference [115] and finite element methods [114] have been applied to the governing Maxwell’s equations. These two approaches generate a global 3-D mesh for all parts of the analyzed structure and for surrounding space, which causes a large amount of unknowns leading to a large linear system. Solving this large linear system requires excessive memory and consumes long CPU time, which makes on-chip interconnect parasitics extraction using FEM or finite difference method impractical. As an alternative, various methods were proposed, among which partial element equivalent circuit method (PEEC) [102], spectral domain approach (SDA) [70] and complex image technique (CIT) [71] will be briefly discussed.

1.3.1.1 *Partial element equivalent circuit method*

The integral formulations of PEEC have been derived by assuming magnetoquasistatic assumption such that the displacement current $j\omega D$ is negligible [119]. Given this, the

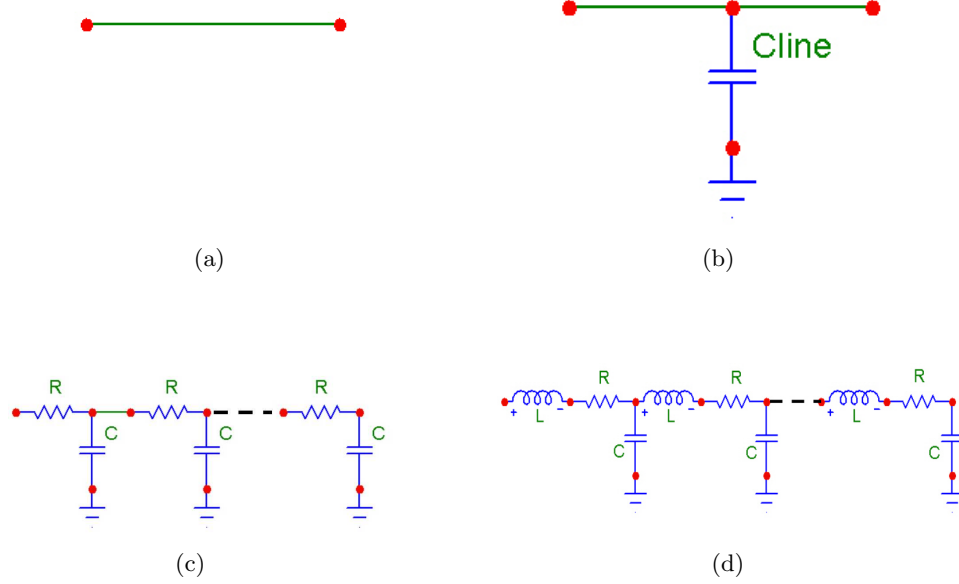


Figure 17: Transition of the interconnect model (a) Short circuit , (b) Capacitor model, (c) RC model, and (d) RLC model

vector potential, A , can be related to the current, J , by

$$A(r) = \frac{\mu}{4\pi} \int_{V'} \frac{J(r')}{|r - r'|} dv' \quad (1.15)$$

where V' is the volume of all conductors, r' is the source point and r is the field point vector. The electric field E is related to vector potential A and scalar potential Φ by

$$E = -j\omega A - \nabla\Phi \quad (1.16)$$

Assuming the ideal conductor constitution relation, $J = \sigma E$, and combining this relation with (1.15) and (1.16) results in

$$\frac{J(r)}{\sigma} + \frac{j\omega\mu}{4\pi} \int_{V'} \frac{J(r')}{|r - r'|} dv' = -\nabla\Phi(r) \quad (1.17)$$

By discretizing the above integral equation (1.17), a dense system of equations can be generated. This system can be solved iteratively for the volume of current in the conductors for a given terminal voltage. The process can be repeated for each terminal to get its corresponding impedances, and thus the inductance and the resistance of the whole interconnect system can be extracted.

Using PEEC, mesh is generated only in the volume of the conductors. Thus, the PEEC method produces fewer number of unknowns than finite element and finite difference methods. Enhanced by multipole-accelerated algorithm, it has been reported that this method is two orders of magnitude faster than direct factorization when used to extract the inductance matrix for realistic packaging examples [119]. On the other hand, the effect of substrate is not included in the PEEC analysis, since the PEEC method partitions only the volume of conductors and there is no unknown assigned in the silicon substrate.

1.3.1.2 Spectral domain approach (SDA)

Accurate analysis of the interconnect on Si-SiO₂ substrate is crucial for on-chip power grid modeling. The propagation characteristics of a microstrip over silicon substrate depend on the frequency and the conductivity of the silicon, which are characterized by three modes: quasi-TEM, slow-wave, and skin-effect modes [69]. Thus, the distributed transmission line parameters have a significant frequency dependence. In [70], spectral domain approach has been applied to calculate the frequency dependent distributed inductance $L(\varpi)$ and resistance $R(\varpi)$.

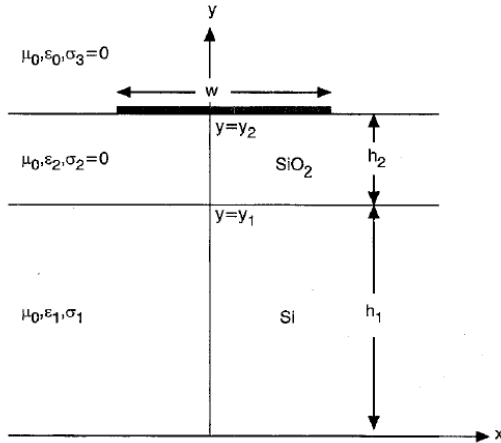


Figure 18: Microstrip over Si-SiO₂ substrate

The governing equations for magnetic vector potential A_z in a multilayered media, as

shown in Fig. 18, are

$$\nabla^2 A_z(x, y) = \begin{cases} -\mu_0 \delta(x - x') \delta(y - y'), & \text{lossless dielectric, unit current source} \\ j\omega \mu_0 \sigma A_z(x, y), & \text{lossy dielectric, no current source} \end{cases} \quad (1.18)$$

where σ is the conductivity of the lossy dielectric. In addition, at the interface of the i th and $(i + 1)$ th layers, on which the perfect conductor of zero thickness is located, the vector potentials A_i and A_{i+1} satisfy the boundary conditions given by:

$$\frac{\partial A_{i+1}(x, y)}{\partial y} - \frac{\partial A_i(x, y)}{\partial y} = \begin{cases} \mu_0 J, \text{ on strip} \\ 0, \text{ otherwise} \end{cases} \quad (1.19)$$

$$\frac{\partial A_{i+1}(x, y)}{\partial x} - \frac{\partial A_i(x, y)}{\partial x} = 0 \quad (1.20)$$

$$\frac{\partial A_i(x, y = y_i)}{\partial x} = 0, \text{ on strip} \quad (1.21)$$

Taking Fourier transform of (1.18)–(1.21) with respect to x , the original differential equations and boundary conditions are transformed into spectral domain. For example, the vector potential can be written as:

$$\tilde{A}(\alpha, y) = \int_{-\infty}^{\infty} A(x, y) e^{j\alpha x} dx \quad (1.22)$$

Using Galerkin method in Fourier transform domain, the current density on the microstrip can be expanded in terms of basis functions. The coefficients of these basis functions can be obtained from the solution of a set of algebraic equations. From the current distribution, frequency dependent inductance and resistance can be calculated. It has been reported that the inductance and resistance calculated using SDA approach are in good agreement with those from the full wave solver [70].

SDA is basically an integral equation method carried out in Fourier-transform domain. By construction, it consists of a system of algebraic equations instead of integral equations, which makes SDA simpler in the numerical computation and more efficient than other methods. However, as a numerical algorithm, it is too time-consuming to be a viable solution for computer-aided design (CAD) of on-chip PDN. Therefore, analytical solutions have been explored, which are discussed in the next subsection.

1.3.1.3 Complex image technique (CIT)

Closed-form expressions for the characteristics of on-chip interconnects are very desirable for fast simulation and CAD. Closed-form expressions for various kinds of transmission line on lossless substrates are readily available for microwave integrated circuit design. These expressions, however, are not applicable to the interconnects on silicon substrate due to the lossy nature of the substrate. To model the interconnects on lossy silicon substrate using closed-form expressions, complex image technique has been proposed, which has been applied on single microstrip as well as coupled microstrips [71].

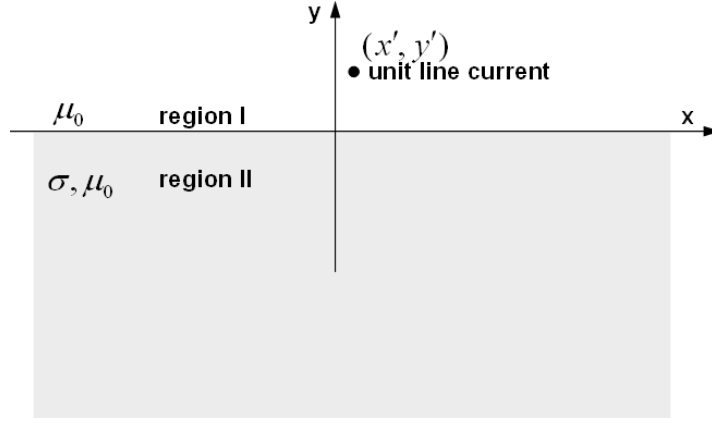


Figure 19: Current source over a semi-infinite lossy substrate.

The derivation of complex image for the microstrip-type interconnects over infinite substrate is as follows. The magnetic vector potential in different regions of Fig. 19 satisfies the following equation:

$$\begin{aligned} \nabla^2 A_z(x, y) &= -\mu_0 \delta(x) \delta(y - y') & \text{for } y > 0 \\ \nabla^2 A_z(x, y) &= j\varpi \mu_0 \sigma A_z(x, y) & \text{for } y < 0 \end{aligned} \quad (1.23)$$

In region I, the Green's function is given by

$$G_1(x, y | x' = 0, y') = \frac{\mu_0}{2\pi} \int_0^\infty \left[\frac{e^{-k|y-y'|}}{k} - \frac{q-k}{q+k} \frac{e^{-k(y+y')}}{k} \right] \cos(kx) dk \quad (1.24)$$

where $\gamma = \sqrt{j\varpi\mu_0\sigma}$ and $q = \sqrt{k^2 + \gamma^2}$. Expanding the term $(q - k)/(q + k)$ into a Taylor

series about $k = 0$, and neglecting its high-order terms, the Green's function in region I can be approximated as

$$G_1(x, y|x' = 0, y') \approx \frac{\mu_0}{2\pi} \int_0^\infty \left[\frac{e^{-k|y-y'|}}{k} - \frac{e^{-k(y+(y'+2/\gamma))}}{k} \right] \cos(kx) dk \quad (1.25)$$

In (1.25), the first term in the integral is due to the current source located at $(x' = 0, y')$. The second item indicates an image current located at a complex location $(x' = 0, -(y' + d))$, where $d = 2/\gamma = \frac{2}{\sqrt{j\omega\mu_0\sigma}} = (1-j)\delta$, and $\delta = 1/\sqrt{\pi f\mu_0\sigma}$ is the skin depth of the conducting substrate. This image current represents the eddy current distributed in the silicon substrate, which largely depends on the frequency and the conductivity of the substrate. The magnitude of image current is -1 , indicating that it flows in an opposite direction to the current source. The entire system is neutral due to the cancellation of the forward and return current. As an alternative to the complex image current, the effect of lossy substrate can be modeled as a virtual ground plane centered between the source and image current, which is at a complex distance $h_{eff} = h + (1-j)\delta/2$ from the current source, as shown in Fig. 20.

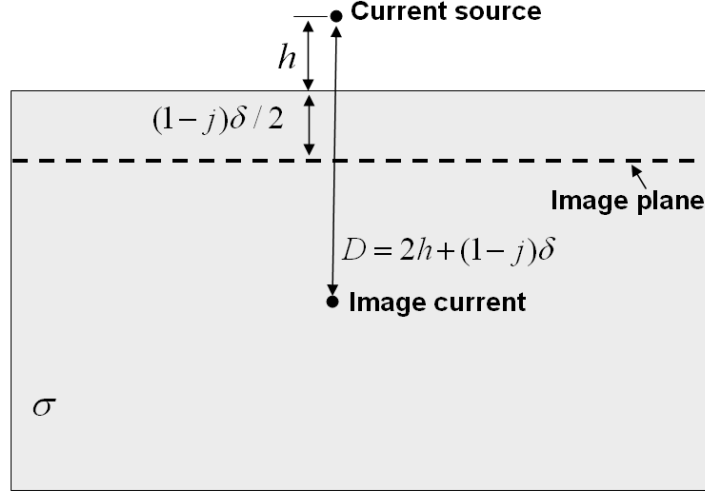


Figure 20: Virtual ground plane of current source over lossy substrate.

Following the same steps, the virtual ground plane for a lossy substrate with a backside ground plane, as shown in Fig. 21, is away from the source current with a complex distance

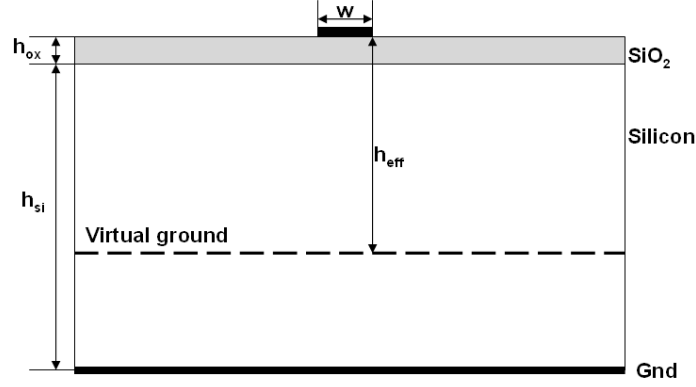


Figure 21: Complex image model of source over substrate with ground plane.

given by:

$$h_{eff} = h_{ox} + \frac{(1-j)}{2} \delta \tanh[(1+j)h_{si}/\sigma] \quad (1.26)$$

where $\delta = 1/\sqrt{\pi f \mu_0 \sigma}$ is the skin depth of the bulk silicon. Closed-form expression for inductance of a lossless microstrip has been given by Wheeler in [107] as:

$$L(w/h) = \frac{\mu_0}{4\pi} \ln \left\{ 1 + 32 \left(\frac{h}{w} \right)^2 \left[1 + \sqrt{1 + \left(\frac{\pi w}{8h} \right)^2} \right] \right\} \quad (1.27)$$

Substituting h by h_{eff} in $L(w/h)$, per-unit-length inductance $L(\omega)$ and resistance $R(\omega)$ of a microstrip over lossy substrate can be obtained from the real and imaginary part of $L(w/h_{eff})$ given by:

$$L(\varpi) = \text{Re}\{L(w/h_{eff})\} \quad (1.28a)$$

$$R(\varpi) = -\varpi \text{Im}\{L(w/h_{eff})\} \quad (1.28b)$$

Regarding the parameters of shunt admittance, C and G , formulas have been derived based on the corresponding equivalent circuit in the low and high frequency limits. The equivalent circuit for the shunt admittance of an interconnect over lossy substrate is shown in Fig. 22 and closed-form expressions for $C(\varpi)$ and $G(\varpi)$ are given by

$$G(\varpi) = \frac{\varpi^2 G C_{ox}^2}{G^2 + \varpi^2 (C_{si} + C_{ox})^2} \quad (1.29a)$$

$$C(\varpi) = \frac{\varpi^2 C_{si} C_{ox} (C_{si} + C_{ox}) + C_{ox} G^2}{G^2 + \varpi^2 (C_{si} + C_{ox})^2} \quad (1.29b)$$

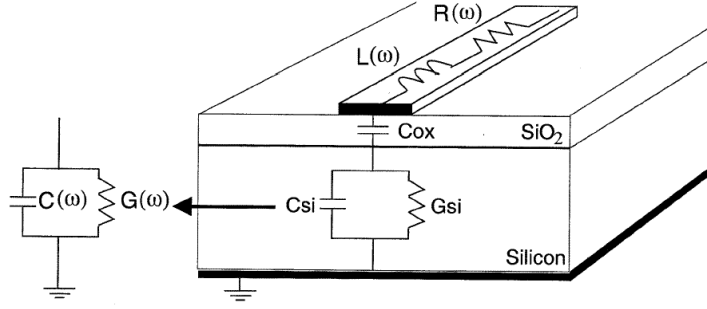


Figure 22: $C(\omega)$ and $G(\omega)$ of a microstrip on silicon substrate.

where C_{ox} is the capacitance of a microstrip of height h_{ox} , for which SiO_2 is used as dielectric. The parameters C_{si} and G_{si} are the shunt admittance of the lossy substrate.

The accuracy of complex image technique has been verified by comparing the RLCG parameters from CIT with those from quasi-static solvers, as shown in Fig. 23. The per-unit-length RLCG parameters have been illustrated as functions of substrate conductivity as well as frequency.

Complex image technique has also been applied on multi-conductor transmission lines. For N coupled transmission lines, CIT generates $N \times N$ matrices, in which the off-diagonal entries denote the coupling. The mutual inductance L_{ij} has been evaluated by extrapolating the formulas for partial self/mutual inductance of conductors with finite length [109]. However, the inductance PUL is increasing with the length of the conductor l due to a divergent term in the formula [98]. For example, the partial inductance L_{11}^p of a conductor with length l , width w , and thickness t is given by

$$\frac{L_{11}^p}{l} = \frac{\mu_0}{2\pi} \left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} - f(w, t) \right] \quad (1.30)$$

which has a divergent term $\ln(\frac{2l}{w+t})$.

1.3.2 Chip level simulation

At the early stage, the on-chip power grid has been analyzed as a resistive network connected to a power supply through the model of the package [52]. Therefore, IR-drop analysis has been carried out to obtain patterns that produce maximum instantaneous current and

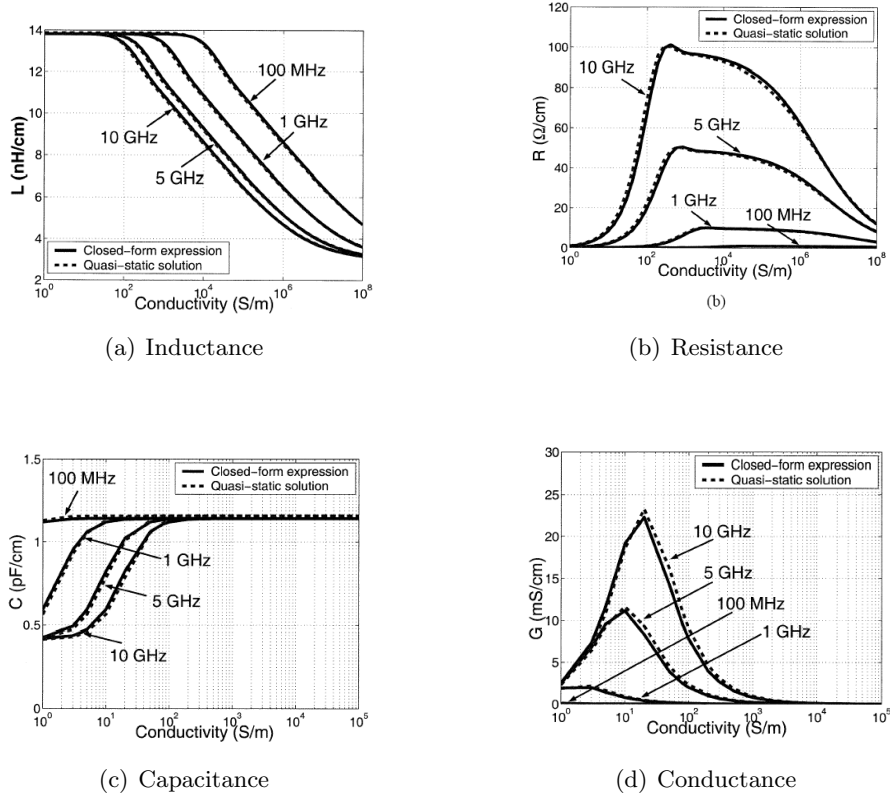


Figure 23: RLGC parameter for microstrip over lossy substrate (a) inductance, (b) resistance, (c) capacitance and (d) conductance

patterns that produce large sustained currents, to prevent problems caused by electromigration [120]. Due to the shorter rise time of digital signal and scaling technology, the resistive model becomes inadequate to represent the on-chip power grid. In stead, transmission line model has been used for constructing a complex network for the on-chip power grid [64].

A critical issue for simulating this complex network is its large size which makes it infeasible to use general purpose circuit simulators, such as SPICE, which will take a long time for simulation. To solve this problem, authors of [64] proposed a unit cell approach. The basic idea behind this approach is the use of iso-potential area for each functional block within the chip. The chip is first divided into many iso-potential areas, and an equivalent circuit is generated for each area. Afterwards, this equivalent circuit is repeatedly assigned to each of the areas and connected at the corresponding nodes. This simple method creates an artificial boundary between functional blocks and is constructed upon the assumption

that the noise is uniform within an iso-potential area, which can lead to erroneous results for large chips operating at high frequencies. Besides the above approach, more efficient algorithms and methodologies, such as hierarchical approach [88], multigrid method [58], latency insertion method (LIM) [63] and circuit-based FDTD [68], have been proposed. Each of them will be discussed briefly in the following subsections.

1.3.3 Hierarchical analysis of on-chip power distribution networks

Traditionally, the large size problem has been addressed by using sparse-matrix techniques for linear systems, which have two categories: 1) direct method such as Cholesky factorization [90] and 2) iterative method such as conjugate gradient technique with preconditioners [90]. According to the authors of [88], these methods are non-hierarchical or flat methods, which stand for solving the problem directly without a graded/ranked series analysis. As a result, there is a serious limitation on the size of the problem that they can handle, which is imposed by the amount of available memory. To overcome the limitations of traditional approaches, a hierarchical analysis was proposed in [88]. This approach consists of the following steps:

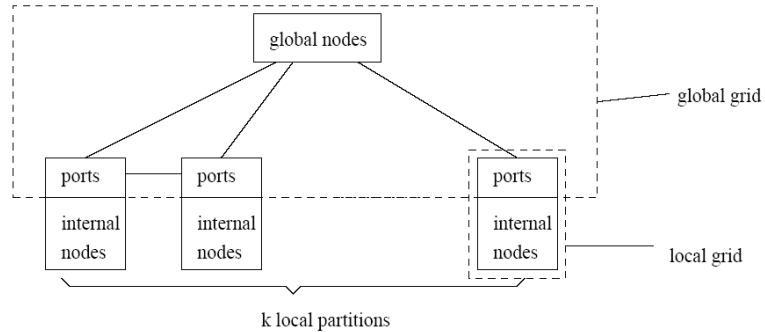


Figure 24: Partition for hierarchical analysis

1. Partitioning and macromodeling: As shown in Fig. 24, the power grid is first divided into k local partitions and a global partition which connects the local partitions through ports. Each of the k local grids is represented as a multi-port linear subsystem with a macromodel $I = AV + S$, where I and V are the vectors of port current

and voltage, A is the admittance matrix and S is a vector of current sources connected between each port and the reference node.

2. Global grid solution: Once macromodels of all the local grids are generated, the entire network can be abstracted as a cluster of macromodels connected at the ports. Inserting every macromodel into the nodal equations of global grid builds a system level model for the entire power grid, and it is considerably smaller than the model from non-hierarchical method. However, the admittance matrix A is usually dense, which is undesirable, since the number of floating point operations for solving a linear system increases with the density of the matrix. Hence, it is important to sparsify the matrix while preserving the positive definiteness of the system. The hierarchical approach includes a numerical process that sparsify the coefficient matrix A , which keeps the error introduced by this process below a chosen criterion.
3. Local grids solution: After obtaining the result of the global grid, vectors of port current I and voltage V can be used to calculate the voltages at the internal nodes of each partition.

Matrices A, S and vectors V, I are the data transferred among the local partition and global partition. The flow of the data is illustrated in Fig. 25.

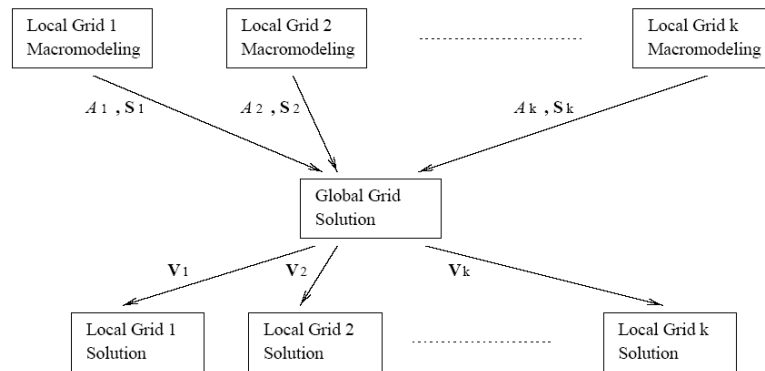


Figure 25: Data flow for hierarchial analysis

The memory requirement of the hierarchical approach is much smaller than that of non-hierarchical approaches, which is a strong advantage of the hierarchical approach and makes it very practical for engineering application. In spite of that, two main processes of the hierarchical approach limit its application, namely, 1) matrix sparsification and 2) partitioning. The sparsification procedure has significant influence on the performance of the approach. Therefore, it has to be carried out carefully for maintaining both acceptable level of accuracy and passivity of each partition. As for partition strategy, the key concept is to identify a subnetwork with an interface boundary, such that the number of nodes at the interface is much smaller than the number of internal nodes. The current solution has used a simple manual inspection for checking every circuit block or a group of blocks placed next to each other for meeting the above criteria. Thus, it involves a lot of user intervention, which is not convenient for design automation and may not achieve the optimal partition.

1.3.4 Multigrid method

Multigrid method was initially used for solving partial differential equations (PDEs), and its application on power supply network was first proposed in [57], then refined in [58]. The terminology “grid” here means a set of discrete points in the domain of the problem, which is different from the “grid” in power grid. In general, the multigrid method belongs to the category of iterative solvers, such as Gauss-Seidel algorithm, as opposed to direct solvers like Gaussian elimination.

Defined as the difference between the exact and the approximate solutions, the error of an iterative solution has the components of low-frequency and high-frequency Fourier modes [59]. Classic iterative methods start from an initial guess and attempt to converge to the real solution by eliminating the error. However, they all suffer from the so-called smoothing property, which means they can quickly remove the high-frequency components, but as iteration continues, the rate of eliminating low-frequency components becomes very slow [58]. The procedure of a general multigrid method has two basic operations, namely: 1) relaxation (smoothing) which reduces the high-frequency error components and 2) coarse grid correction which reduces the low frequency error components. The multigrid method

for on-chip PDN analysis has two corresponding operations, namely: 1) coarsen the network until the problem becomes small enough to be solved exactly using a direct approach, and 2) map the solution back to the original fine network.

The steps of the multigrid method for on-chip power grid analysis are listed below:

1. Grid reduction: The objective of this step is to remove as many nodes/buses as possible, thus the large grid is coarsened and the number of variables is significantly reduced. As an example, a refinement of a power grid is shown in Fig. 26.
2. Interpolation: Operator P is defined to map the original grid to the coarsened grid. This operator relates the voltages on the removed nodes to those on the coarsened grid, thereby allowing the solution of the coarsened grid to accurately reflect that of the original grid.
3. Solving coarsened grid: The reduced grid is then solved exactly by using a direct/iterative solver.
4. Back-mapping process.: The solution of the reduced grid is mapped back to the fine grid, by applying the interpolation operator P obtained in step 2. A back-mapping process is shown in Fig. 27.

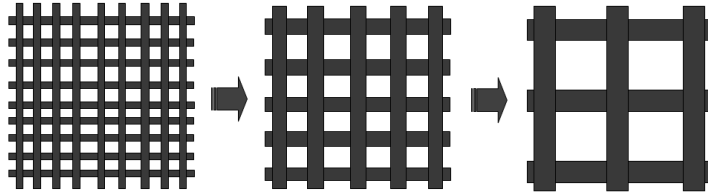


Figure 26: Grid reduction

The main advantage of multigrid technique for power grid analysis is efficiency. It has been reported that multigrid technique shows speedups of one to two orders of magnitude over other methods (direct and iterative methods) for both DC and transient analysis [58]. Its performance is attributed to the rapid convergence of the iterative solver, because the

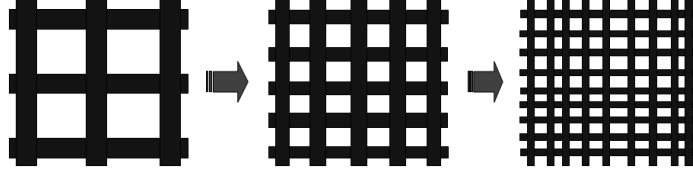


Figure 27: Back-mapping process

solution on a coarse grid typically provides a good initial guess for the iteration on the fine grid. On the other hand, the efficiency of this method relies heavily on the choice of the multigrid operations: the relaxation operator (coarsening procedure) and the interpolation operator, which are not well defined and optimized. From the viewpoint of EM modeling, coarsening power grid dramatically changes the response of the on-chip interconnects and their transmission line parameters. Therefore, the relaxation procedure may introduce error into every level of the iteration, from low-frequency components to high-frequency components.

1.3.5 Latency insertion method and circuit based FDTD

Latency insertion method (LIM) was introduced by the authors of [63] for the simulation of large networks. In [63], finite difference has been used to generate updating expressions for the voltage and current in the circuit. LIM is analogous to the full-wave FDTD method [62], which generates solutions in both time and space from the updating equations for E and H field. The common feature of traditional full-wave FDTD and LIM is that they both use finite difference as an approximation for differential operator, but full-wave FDTD has three spatial differential operators ($\partial/\partial x, \partial/\partial y, \partial/\partial z$) and one temporal operator ($\partial/\partial t$), while LIM only has one time domain operator (d/dt) on circuit variables. Hence, the terminology – circuit based FDTD – has been adopted by J. Choi [67] to signify the resemblance. In the rest of the text, LIM and circuit based FDTD are used as interchangeable terms.

To use LIM, the following requirements for the circuit topology have to be met:

- Each branch of the network must contain an inductance; otherwise, a small inductance is inserted into the branch to generate the latency.

- Each node of the network must provide a capacitive path to ground; otherwise, a small shunt capacitor is added to generate latency at that node.

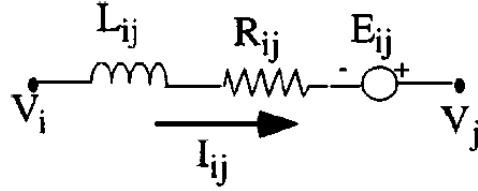


Figure 28: Branch equation derivation

Consider a circuit branch consisting of a voltage source, an inductor and a resistor in series, as shown in Fig. 28, The discrete time equation can be written as:

$$I_{ij}^{n+1} = I_{ij}^n + \frac{\Delta t}{L_{ij}}(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij}I_{ij}^n + E_{ij}^{n+1/2}) \quad (1.31)$$

where Δt is the time step.

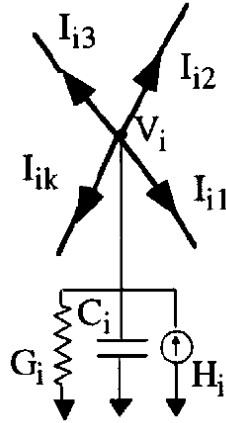


Figure 29: Node equation derivation

On the other hand, each node is modeled as a parallel combination of a current source, a conductance, and a capacitor to ground, as shown in Fig. 29. The discrete equation is given by:

$$V_i^{n+1/2} = \frac{C_i V_i^{n-1/2} + H_i^n - \sum_{k=1}^{M_i} I_{ik}^n}{C_i/\Delta t + G_i} \quad (1.32)$$

At each time step, (1.31) is performed over all branches of the power grid to update the current and (1.32) is performed over all nodes to update the voltage. Computations of branch currents and node voltages alternate as time progresses, which is similar to the updating of H and E field in full-wave FDTD method. According to [63], the condition for numerical stability of circuit based FDTD can be written as

$$\Delta t < \sqrt{L_k C_k} \quad (1.33)$$

where L_k and C_k are the inductance and capacitance of the unit cell k . Eq. (1.33) is analogous to the Courant-Friedrichs-Lewy (CFL) criterion for full wave FDTD method [63].

Circuit based FDTD has been improved in several ways in [66], [67] and [68] which can be listed as follows:

- A modified latency insertion method has been presented for the simulation of large networks with low-latency sections [66]. This method isolates sections with low latency and processes them separately. Using this approach, computational speed is increased and memory usage is reduced.
- For multilayered on-chip power grids, a branch capacitor model has been proposed [67], which is different from the companion model used in the original LIM. The use of companion model attributes to erroneous results due to its incompatibility with the finite difference operator. On the contrary, the method in [67] keeps the compatibility and gives a much better model of the branch capacitor.
- A method for including CMOS inverter characteristics into the circuit based FDTD has been presented in [68]. It has been applied on the on-chip clock distribution to compute the power supply noise across an entire chip. The effect of non-linearity of active circuits on power supply noise has been demonstrated.

Circuit based FDTD method has been applied on large problems, such as an on-chip power distribution network containing around 2 million passive elements [23]. Its algorithm exhibits linear computational complexity and comparisons with SPICE have shown speedups of several orders of magnitude [63]. However, the extraction of inductance, resistance and capacitance of each unit cell depends heavily on the time consuming EM 2-D or 3-D solvers. At the same time, frequency dependence of the RLGC elements in on-chip PDN has been ignored.

1.4 Completed research

The objective of this dissertation is the development of efficient and accurate methods for modeling the coupling due to SSN in multi-layered planes arising in electronic packages, extraction of the power grid parasitics in integrated circuits and simulation of the power supply noise arising in on-chip power distribution networks. Different methods have been developed for various elements of the power distribution hierarchy. Since each level has a distinct power distribution structure, it imposes different kinds of challenges for modeling and simulation. At the PCB and package level, cavity resonator method has been used to model the coupled noise. At the chip level, conformal mapping has been used for extracting the parasitics of the power grid. Using circuit models constructed from the extracted parameters, Finite Difference Time Domain (FDTD) method has been used to simulate power supply noise. The hierarchical power distribution network and the methods developed for modeling and simulation are shown in Fig. 30.

The following research has been completed in this dissertation:

1. Field penetration through planes:

A modeling method is discussed for capturing the field penetrating through power/ground planes. The method is an extension to the cavity resonator model, and uses a perturbational solution to capture the field penetration effect. The results have been compared with measurements and used to analyze its effect on a switching microprocessor.

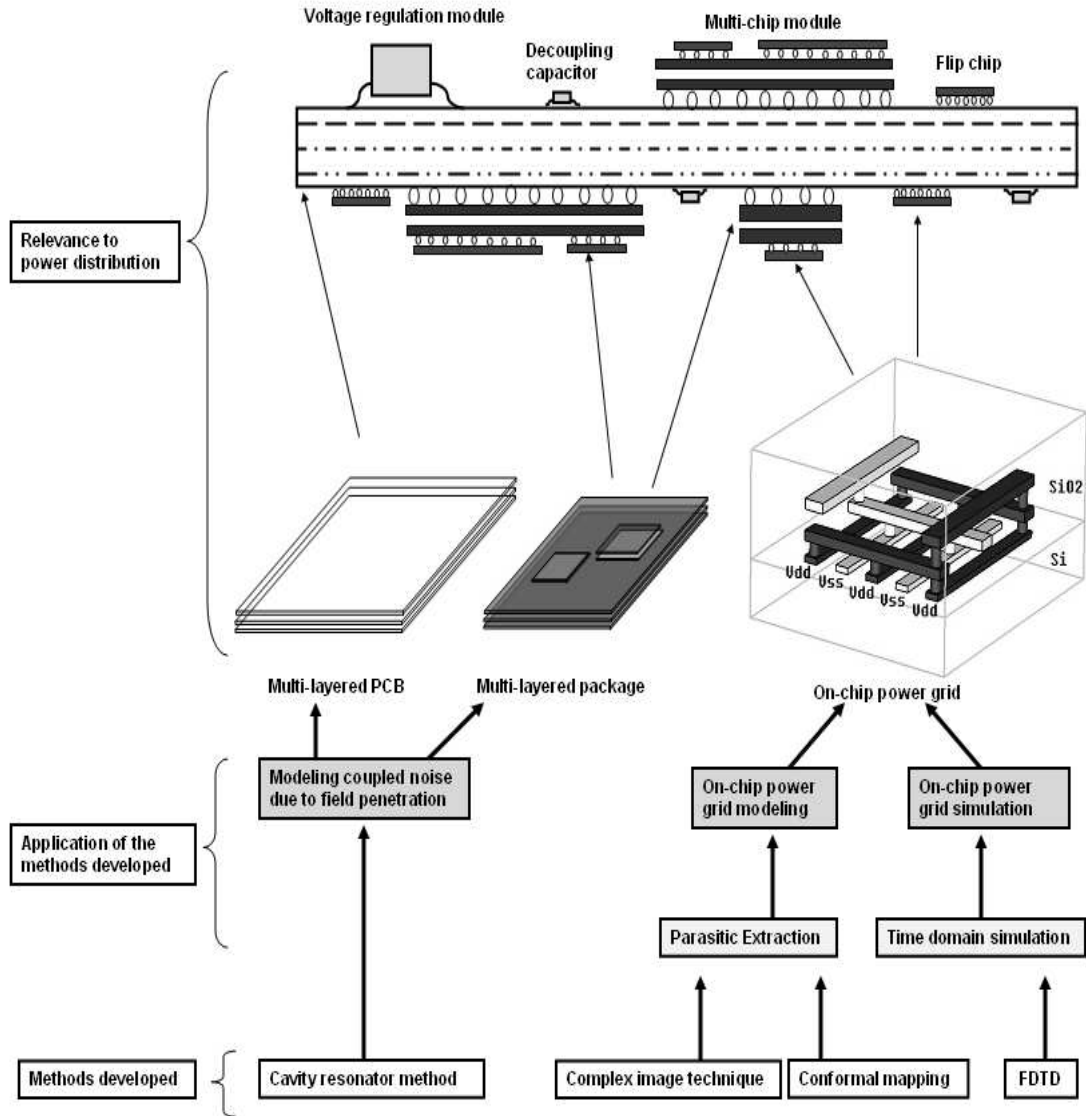


Figure 30: Modeling and simulation methods developed and their relevance to power distribution

2. Modeling of substrate resistivity and its effect on switching noise:

Effect of substrate loss on simultaneous switching noise in on-chip power distribution network has been studied. Complex image technique is used to capture the loss due to eddy current in the conductive substrate and conformal mapping technique is used to model the periodic power grid. The combination of the two techniques enables the modeling of power grid by taking into account the geometry as well as dielectric loss. Through this method, frequency dependent RLGC line parameters have been extracted.

3. Debye approximation and FDTD simulation of on-chip PDN:

For simulating frequency dependent RLGC parameters, first-order Debye rational approximation has been used. Circuit based FDTD method has been modified to include the first order Debye circuit model.

4. Crossover capacitor modeling:

Analytical expressions for crossover capacitance using conformal mapping have been derived. For modeling the crossover capacitance, two issues are studied: 1) the effect of neighboring interconnects on the crossover capacitance and 2) the fringing distance of the electric field for calculating the capacitance. The results of the analytical expressions have been verified by comparing with those from finite element method.

5. Extraction of line parameters in the presence of adjacent metal layers:

Line parameters of the interconnects on a layer are extracted in the presence of adjacent layers using analytical expressions. The analytical expressions generate partial element circuit models for multi-conductor transmission lines which are converted to the equivalent RLGC parameters of a single transmission line. The accuracy of the analytical expressions has been verified by comparing the result with finite element method.

6. Performance of irregular/non-periodic power grid:

In order to explore the different designs of on-chip PDNs, irregular power grid has been studied to analyze the effect of non-periodic layout on SSN. Transmission line

parameters have been extracted using analytical expressions and the power grid with non-periodic layout has been simulated using modified FDTD method. This research was done in collaboration with the first author of [134].

7. Design automation for on-chip power grid analysis:

A software program was developed in C++ language to generate the on-chip power grid model automatically, which takes the geometry of the layout and the property of the material as input. The outputs of the program are a group of text files which are either in the form of SPICETM netlist or in a format readable by FDTD code.

8. Power distribution for 3-D IC:

Three-dimensional (3-D) silicon integration is a promising solution that is being pursued for enhancing the performance of the integrated circuits. Analytical expressions have been derived to characterize the interconnects used in 3-D integration by extending the complex image technique to stripline-type structure. The extra loss due to the eddy current in the stack-up substrates has been captured. SSN in 3-D ICs has been simulated in the time domain and the effect of 3-D integration on noise performance has been studied.

1.5 Dissertation Outline

The remainder of this thesis is organized as follows. Chapter 2 presents the method for modeling noise coupling due to field penetrating through power/ground planes. Chapter 3 describes the effect of substrate loss on simultaneous switching noise in on-chip power distribution networks. Conformal mapping and first-order Debye approximation based FDTD is used for model extraction and simulation with frequency dependent parameters, respectively in Chapter 3. Chapter 4 presents the effects of neighboring layers on power grid modeling, which includes the crossover capacitor calculation and line parameter extraction in the presence of adjacent layers. In Chapter 5, a method for extracting parameters for power grid in 3-D integrated chips is presented. Finally, Chapter 6 discusses the conclusion and future work .

CHAPTER II

MODELING OF FIELD PENETRATION THROUGH PLANES IN MULTILAYERED PACKAGES

The power distribution network includes the chip, package and board where each level in the system hierarchy contributes to the system response. A commonly used power distribution structure in high performance packages are multilayered power and ground planes, such as in printed wiring boards, multi-chip modules and single-chip modules. A major concern in the design of such modules is power supply noise which appears as a voltage fluctuation on the power distribution network when groups of circuits switch simultaneously. In the previous chapter, various methods adopted by researchers in the packaging community to model power/ground pairs have been discussed, such as inductance network [24], two dimensional discrete transmission line model [27], transmission matrix method [35], FDTD method [33], and cavity resonator method [21].

In all the methods that have been used for analyzing multilayered power distribution networks containing planes, the plane pairs have always been assumed to be isolated from each other. For example, in [21] the effect of conductor loss is included in the solution by changing the wave number k to a complex number. For a single plane pair, the skin effect is then assumed to be dominant and the solution is extended to multilayered structures by assuming zero coupling between the plane layers. However, in the steady state, when the planes resonate, substantial coupling between the plane layers can occur through the magnetic fields penetrating the solid conductor where the level of penetration depends on the conductor thickness and conductivity of the planes. In the past, the clock frequency was much smaller than the package resonant frequency due to which isolation between the plane layers could be assumed. With the increase in clock frequency for present and future microprocessors, the package resonance frequency can overlap with the clock frequency causing coupling between the layers. This effect is a steady state effect which can cause

a problem when the microprocessor performs an operation continuously over many clock cycles. The modeling and analysis of the field penetrating through power/ground planes is the subject of this chapter.

This chapter begins with the modeling of voltage coupling between neighboring planes and the extension of the modeling technique to multiple layers. Then, the modeling method has been applied to a test structure and compared with measurements. Later, the effect of field penetration for a switching microprocessor has been discussed using frequency and time domain simulation. Two important parameters, namely, the metal thickness and metal conductivity of the planes are optimized to suppress the field penetration effect. Finally, a summary is provided at the end of the chapter.

2.1 Modeling of field penetration through planes in multi-layered packages

The modeling method to be discussed in this section is an extension to the cavity resonator model [21] [22], where a perturbational solution has been used to capture the field penetration effect. The cavity resonator model for a plane pair has been described in detail in this section.

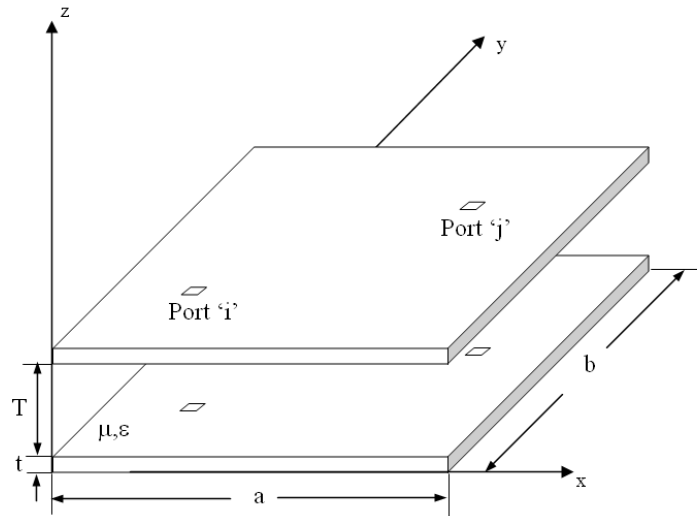


Figure 31: Plane pair structure

In Fig. 31, two planes of dimension $a \times b$ separated by a distance T have been analyzed as a cavity resonator. The figure shows two ports, namely, port i , and port j . Each port consists of two regions, one on the top plane and the other on the bottom plane. Each region represents a metal surface, with the two surfaces separated by the dielectric thickness T . The area of these surfaces at the port location is small and can be viewed as a pad where measurements can be made. Using the cavity modes, the impedance between ports i and j , Z_{ij} , can be written in the form

$$Z_{ij} = j\varpi\mu T \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{(k_{mn}^2 - k^2)ab} f(x_i, y_i) f(x_j, y_j) \quad (2.1)$$

where

$$f(x_i, y_i) = \cos \frac{2m\pi x_i}{2a} \sin c \frac{m\pi t_{xi}}{2a} \cos \frac{2n\pi y_i}{2b} \sin c \frac{n\pi t_{yi}}{2b},$$

and

$$\varepsilon_m, \varepsilon_n = \begin{cases} 1, & \text{for } m, n=0 \\ \sqrt{2}, & \text{otherwise} \end{cases}$$

$(x_i, y_i), (x_j, y_j)$, coordinates of the port locations,

$(t_{xi}, t_{yi}), (t_{xj}, t_{yj})$, dimensions of the ports,

$k_{mn}^2 = (\frac{m\pi}{2})^2 + (\frac{n\pi}{2})^2$, m, n being propagating modes in the cavity,

$k = k' - jk'', k'' = \varpi\sqrt{\mu\varepsilon}(\frac{\tan(\delta)}{2} + \frac{r}{2T})$, complex wave number,

$r = \sqrt{2/\varpi\mu\sigma}$, skin depth,

$\tan(\delta)$, loss tangent of the dielectric ,

μ , permeability of the medium,

ε , permittivity of the medium,

σ , conductivity of the metallization,

ϖ , angular frequency.

Expression (2.1) has been derived directly by solving Maxwell's equations and assuming magnetic wall at the edges. This analytical solution captures the propagation and reflection of radial waves between the power planes [45]. Efficient methods for reducing the model complexity and for stacking planes have also been described in [21] and [48]. In [49], this method has been applied to develop SPICE models for simulating the noise generated by output drivers switching simultaneously.

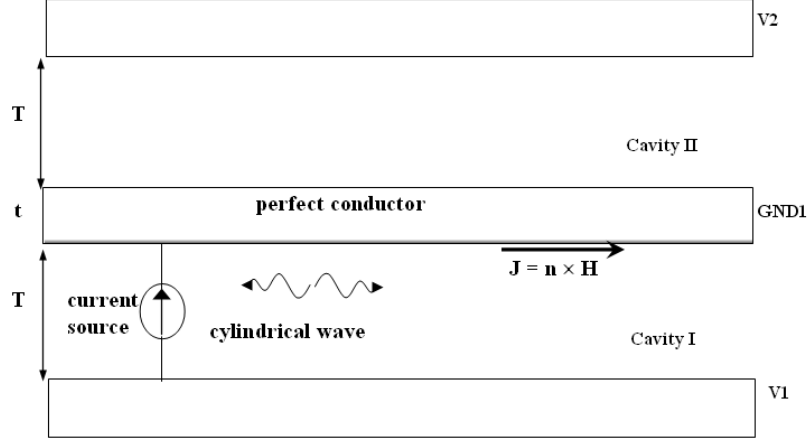


Figure 32: Three-layer package planes constructed with high conductivity metal (perfect conductor)

The modeling methods in [21], [45], [48] and [49] are based on the assumption that skin effect is dominant and hence the field cannot penetrate the solid planes. The plane pairs are therefore assumed to be completely isolated from each other since the skin depth is a small fraction of the metal thickness at high frequencies, as shown in Fig. 32. Though this assumption is valid for thick planes with high conductivity metallization, thin planes with low conductivity metallization are sometimes used to supply power to the chip. When this happens, magnetic fields can penetrate through solid conductors. Since a plane pair acts as a cavity resonator with high quality factor Q (low loss), a small amount of energy leaking into the cavity can take a long time to decay. Hence, over time, a switching microprocessor can couple a significant amount of energy into the layers above/below. The maximum coupling of energy occurs at resonance, as will be shown in Sec. 2.2 of this chapter.

To enable the magnetic field to penetrate the solid conductor, the analytical solution in (2.1) has been modified. The solution procedure starts with the computation of the electrical field in cavity I composed of plane V1 and GND1 as shown in Fig. 32. The electric field can be described in cavity I as [41]

$$E_{cav1,z} = \frac{j\varpi\mu J_s}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_{mn}^2 - k^2} \cos \frac{m\pi x_i}{a} \cos \frac{n\pi y_i}{b} \cos \frac{m\pi x_j}{a} \cos \frac{n\pi y_j}{b} \quad (2.2a)$$

$$E_{cav1,x} = E_{cav1,y} = 0 \quad (2.2b)$$

where only a vertical z-directional electric field is assumed to exist in the cavity due to the small dielectric thickness T . In Eq. (2.2), a vertical delta current source J_s is assumed to excite the cavity to mimic a switching circuit [21]. By evaluating the curl of the electric field in Eq. (2.2), the magnetic field in cavity I can be expressed as

$$H_{cav1,x} = \frac{J_s}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_{mn}^2 - k^2} \frac{n\pi}{b} \cos \frac{m\pi x_i}{a} \sin \frac{n\pi y_i}{b} \cos \frac{m\pi x_j}{a} \cos \frac{n\pi y_j}{b} \quad (2.3a)$$

$$H_{cav1,y} = \frac{J_s}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_{mn}^2 - k^2} \left(-\frac{m\pi}{a}\right) \sin \frac{m\pi x_i}{a} \cos \frac{n\pi y_i}{b} \cos \frac{m\pi x_j}{a} \cos \frac{n\pi y_j}{b} \quad (2.3b)$$

In Eq. (2.3), the magnetic fields are along the transverse direction. Assuming initially that the ground plane GND1 is a perfect conductor, the current density at the bottom of plane GND1 can be computed as

$$J_{per_GND1,x} = \frac{J_s}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_{mn}^2 - k^2} \left(-\frac{m\pi}{a}\right) \sin \frac{m\pi x_i}{a} \cos \frac{n\pi y_i}{b} \cos \frac{m\pi x_j}{a} \cos \frac{n\pi y_j}{b} \quad (2.4a)$$

$$J_{per_GND1,y} = \frac{J_s}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_{mn}^2 - k^2} \left(-\frac{n\pi}{b}\right) \cos \frac{m\pi x_i}{a} \sin \frac{n\pi y_i}{b} \cos \frac{m\pi x_j}{a} \cos \frac{n\pi y_j}{b} \quad (2.4b)$$

$$J_{per_GND1,z} = 0 \quad (2.4c)$$

where the currents in Eq. (2.4) are obtained from Eq. (2.3) through the boundary condition $\vec{J}_{per_GND1} = \hat{n} \times \vec{H}_{cav1}$ with \hat{n} being the unit outward vector normal to the surface of plane GND1. Since the magnetic fields are in the transverse direction, the induced currents at the bottom of plane GND1 flow in the transverse direction. The current computed in Eq. (2.4) is a surface current which cannot penetrate the conductor, since the conductor is assumed to be perfect with infinite conductivity.

If the center conductor plane GND1 in Fig. 33 is assumed to have a finite conductivity, the current through the cross section of the conductor has the form

$$\vec{J}_{non_GND1}(z) = \vec{J}_0 e^{-\gamma z} \quad (2.5)$$

where \vec{J}_{non_GND1} is the distribution of the current across the cross section of non-ideal conductor and the parameter γ is related to the metal conductivity and frequency through

$$\gamma = (1 + j) \sqrt{\frac{\omega \mu_0 \sigma_c}{2}} \quad (2.6)$$

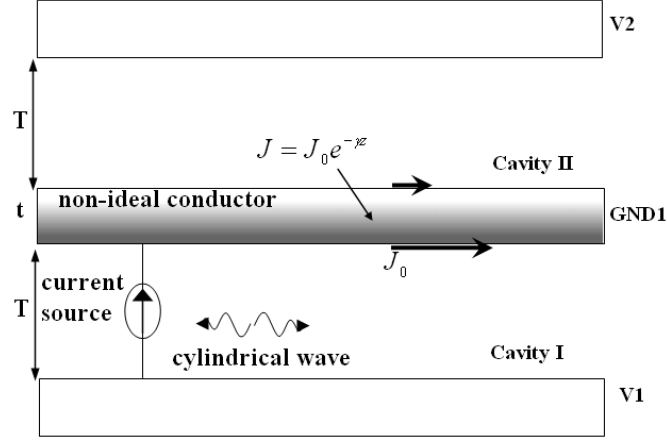


Figure 33: Three-layer package planes constructed with non-ideal conductor

where σ_c is the metal conductivity and ϖ is the angular frequency. In Eq. (2.5), the unknown constant \vec{J}_0 can be computed by assuming that the total volume of current in the non-ideal conductor GND1 is equal to that in the perfect conductor. This assumption which is a perturbational solution can be represented in the form

$$\int_0^t \vec{J}_{non_GND1} dz = \vec{J}_{per_GND1} \quad (2.7)$$

where t is the thickness of the plane GND1. By combining Eq. (2.5) and Eq. (2.7), the constant \vec{J}_0 can be derived as

$$\vec{J}_0 = \frac{\gamma}{1 - e^{-\gamma t}} \vec{J}_{per_GND1} \quad (2.8)$$

Hence, for a thickness t , the current density at the top of plane GND1 can be obtained by combining Eq. (2.5) and Eq. (2.8) as

$$\vec{J}_{GND1,top} = \frac{\gamma e^{-\gamma t}}{1 - e^{-\gamma t}} \vec{J}_{per_GND1} \quad (2.9)$$

The current designated by Eq. (2.9) flowing at the top of the plane GND1 acts as the source of coupled noise in the quiet cavity II composed of planes V2 and GND1 in Fig. 33. Since the current and electric field in a conductor are related by

$$\vec{J} = \sigma_c \vec{E} \quad (2.10)$$

the electric field at the top of plane GND1 can be computed as

$$\vec{E}_{GND1_top} = \frac{\nu}{\sigma_c} \vec{J}_{per_GND1} \quad (2.11)$$

where the constant $\nu = (\gamma e^{-\gamma t}) / (1 - e^{-\gamma t})$.

In Eq. (2.11), since the current is in the transverse direction on the plane, the electric field is along the transverse direction. Using the boundary condition that the tangential electric field is continuous at an interface, the electric field computed in Eq. (2.11) is the field at the bottom surface of cavity II.

Since the field distribution in cavity II is not known, the variation of the electric field in cavity II can be described as

$$\vec{E}_{cav2} = \frac{\nu}{\sigma_c} \vec{J}_{per_GND1} f_{mn}(z) \quad (2.12)$$

where $f_{mn}(z)$ is an arbitrary function with a maximum of 1 at the bottom surface of cavity II and a minimum of 0 at the top surface of cavity II. This is based on the assumption that the electric field decays to zero at the top of cavity II. It can be extended to n cavities in a multilayered structure where the function $f_{mn}(z)$ is assumed to be zero at the top surface of the n th cavity, which is equivalent to the electric field decaying to zero at the top of the n th cavity. It is important to note that Eq. (2.12) is a perturbational solution to the electric field which is a good approximation, as will be justified later through measurement.

Since the fields in cavity II have to satisfy the wave equation, substitution of Eq. (2.12) into the wave equation leads to

$$(\frac{\partial^2}{\partial z^2} + C_{mn}^2) f_{mn}(z) = 0 \quad (2.13a)$$

$$C_{mn}^2 = k^2 - (\frac{m\pi}{a})^2 - (\frac{n\pi}{b})^2 \quad (2.13b)$$

$$f_{mn}(z) = \begin{cases} 1; & \text{for } z = 0 \\ 0; & \text{for } z = T \end{cases} \quad (2.13c)$$

For two plane pairs, as shown in Fig. 33, the solution of Eq. (2.13) is

$$f_{mn}(z) = \frac{-\sin[C_{mn}(z - T)]}{\sin(C_{mn}T)} \quad (2.14)$$

Applying $\nabla \cdot \vec{E} = 0$ in the source free region (cavity II), and integrating over the thickness of the cavity, the voltage fluctuation in cavity II can be derived as

$$V_{cav2} = \frac{J_s \nu}{ab \sigma_c} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{-\varepsilon_m^2 \varepsilon_n^2 k_{mn}^2}{(k^2 - k_{mn}^2)^2} \cos \frac{m\pi x_i}{a} \cos \frac{n\pi y_i}{b} \cos \frac{m\pi x_j}{a} \cos \frac{n\pi y_j}{b} \quad (2.15)$$

which leads to the transfer impedance between port i in cavity I and port j in cavity II as

$$Z_{ij} = \frac{A}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{-\varepsilon_m^2 \varepsilon_n^2 k_{mn}^2}{(k^2 - k_{mn}^2)^2} \cos \frac{m\pi x_i}{a} \cos \frac{n\pi y_i}{b} \cos \frac{m\pi x_j}{a} \cos \frac{n\pi y_j}{b} \quad (2.16)$$

In (2.16), (x_i, y_i) and (x_j, y_j) denote the coordinates of excitation port in cavity I and the port in cavity II at which the field is to be computed, respectively. The parameter A is a function of the metal thickness t and conductivity σ_c of plane GND1 given by $A = \frac{\nu}{\sigma_c}$. The parameter $k_{mn}^2/(k^2 - k_{mn}^2)^2$ is a frequency dependent factor that determines the poles of the system. The primary difference between Eq. (2.1) and Eq. (2.16) is that the latter equation contains second order poles which give rise to sharper peak response at the resonant frequencies of the structure.

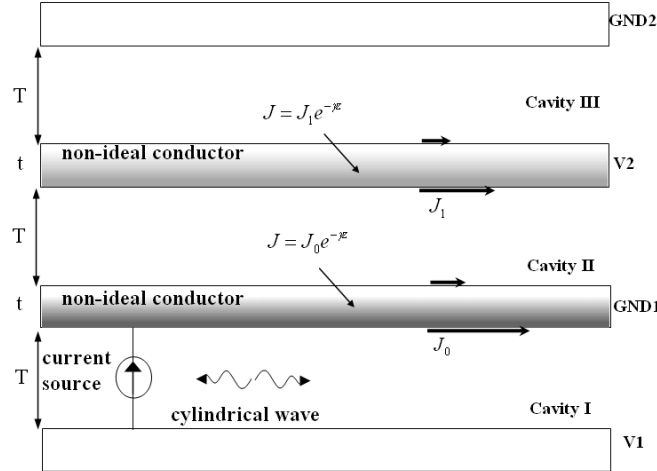


Figure 34: Four-layer package with non-ideal conductor

Through a similar procedure, the method can be extended to multiple plane pairs containing more than two cavities. As an example, consider a three plane pairs structure containing a homogeneous dielectric as shown in Fig. 34. Assuming a current excitation in cavity I, the transfer impedance between the excitation port i in cavity I and the measured

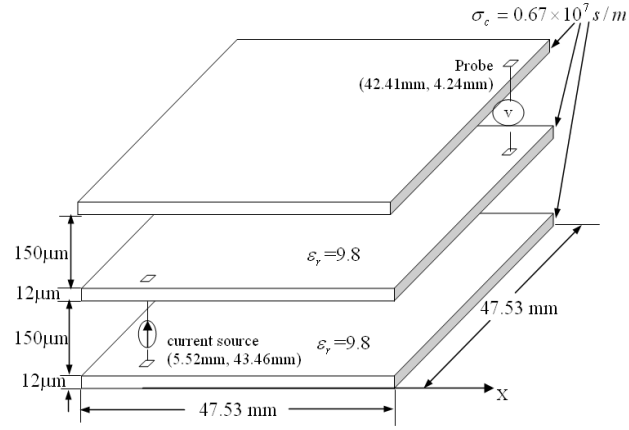
port j in cavity III can be computed as

$$Z_{ij} = \frac{1}{j\omega\mu} \frac{A^2}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{-\varepsilon_m^2 \varepsilon_n^2 k_{mn}^2}{(k^2 - k_{mn}^2)^{5/2}} \frac{k^2}{\sin(C_{mn}T)} \cos \frac{m\pi x_i}{a} \cos \frac{n\pi y_i}{b} \cos \frac{m\pi x_j}{a} \cos \frac{n\pi y_j}{b} \quad (2.17)$$

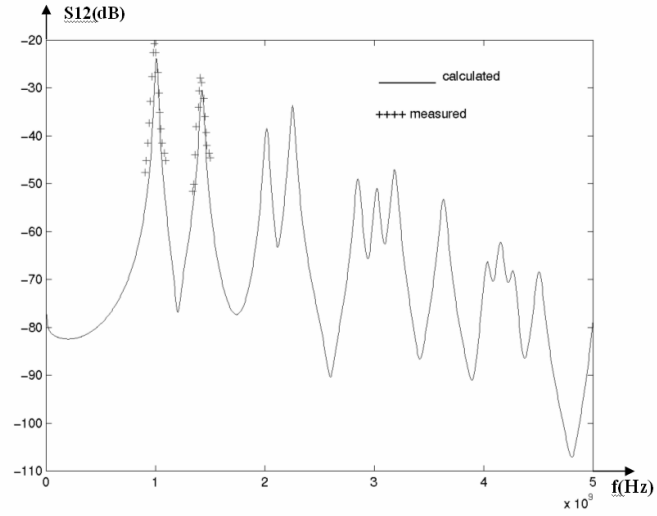
The coupled voltage beyond the second cavity is typically small due to the factor A^2 . Therefore, the leakage of energy beyond one plane pair can be ignored in most realistic structures.

2.2 Model to measurement correlation

The model for the impedance derived in Eq. (2.16) was compared with measurement on a test vehicle. The test vehicle consists of three planes as in Fig. 35(a). with lateral dimensions of $a = 47.53mm$ and $b = 47.53mm$. Tungsten metallization was used with thickness $t = 12\mu m$ and conductivity $\sigma_c = 0.67 \times 10^7 s/m$. The dielectric medium is homogeneous with relative permittivity $\varepsilon_r = 9.8$ and thickness $T = 150\mu m$. The source port and coupling port were located at $x_1 = 5.52mm$, $y_1 = 43.46mm$ and $x_2 = 42.41mm$, $y_2 = 4.24mm$, respectively. The scattering parameter S_{12} , which denotes the transmission and coupling of energy between the ports, was measured using a network analyzer-HP8510B. The correlation between the model and measurement is shown in Fig. 35(b). As can be seen, substantial coupling (-20 to -30 dB) occurs at the resonant frequency of the structure with the first two resonant peaks coupling the maximum voltage. As expected, the amplitude of the coupled energy between the plane pairs decreases as the frequency increases, which can be attributed to skin effect that reduces the amplitude of the current penetrating the conductor. The effect of resonance on the distribution of current can be illustrated by plotting Eq. (2.5) as a function of the metal thickness. The current distribution in the center conductor in Fig. 35 is shown in Fig. 36 at two frequencies, namely, a frequency far from resonance ($f = 0.4$ GHz) and a frequency at resonance ($f = 2$ GHz). In Fig. 36(a), the current density across the cross section of the center conductor is minimum. However, in Fig. 36(b) substantial current density exists across the cross section of the conductor. In addition, the current density shows a standing wave pattern with maximum penetration at specific points along the surface of the center conductor.

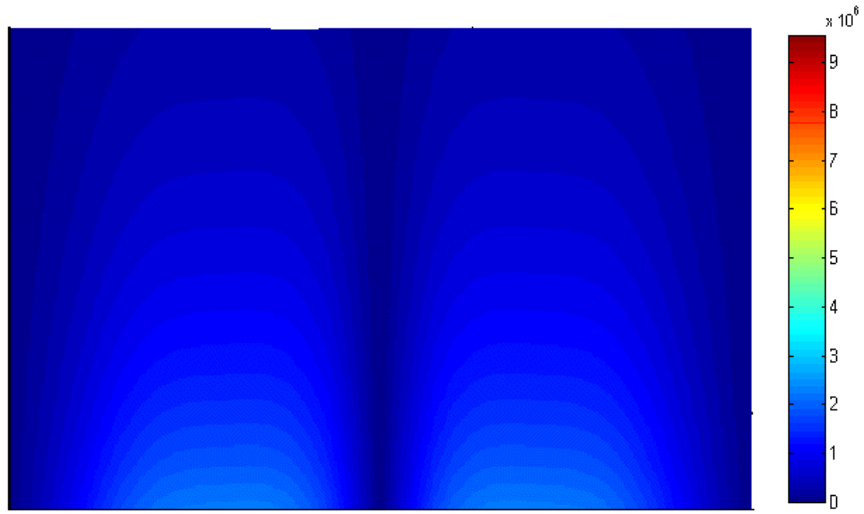


(a)

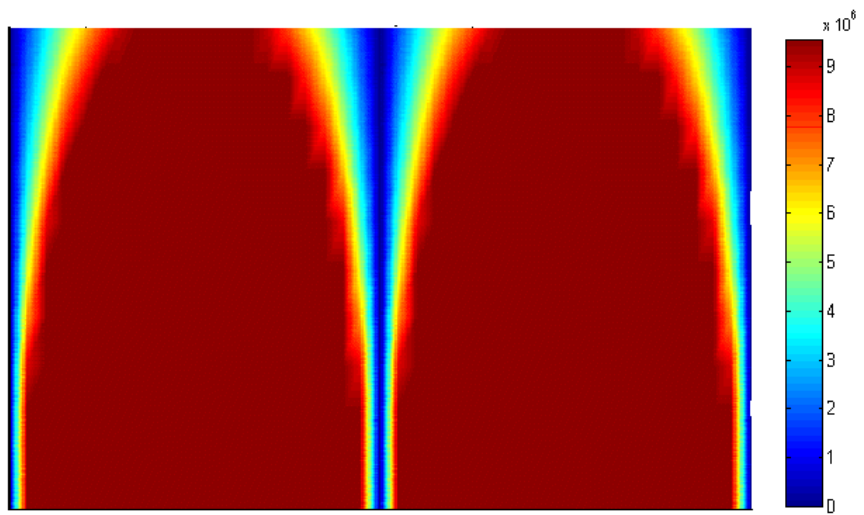


(b)

Figure 35: Measurement to model correlation (a)Cross section of test vehicle, (b)Comparison between simulation and measurement data

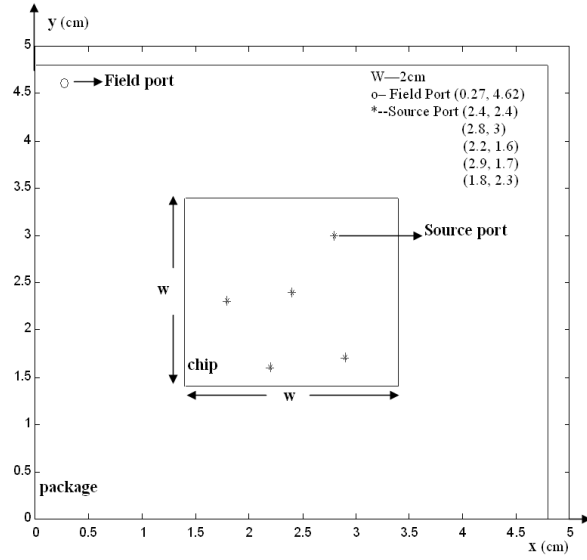


(a)

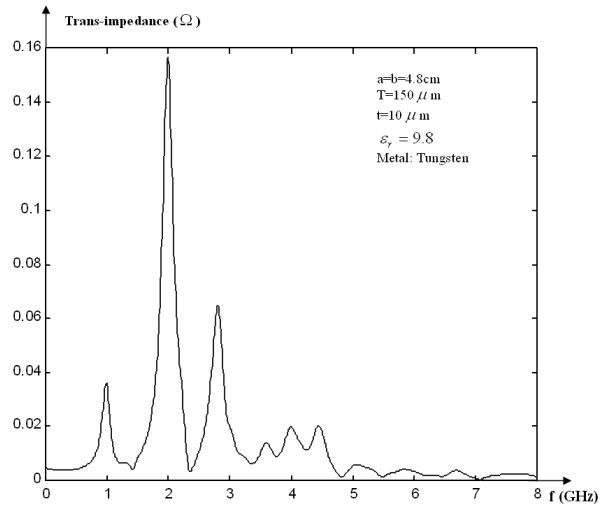


(b)

Figure 36: Current distribution in the cross section of GND1 plane: (a) $f = 0.4$ GHz, (b) $f = 2.0$ GHz



(a)



(b)

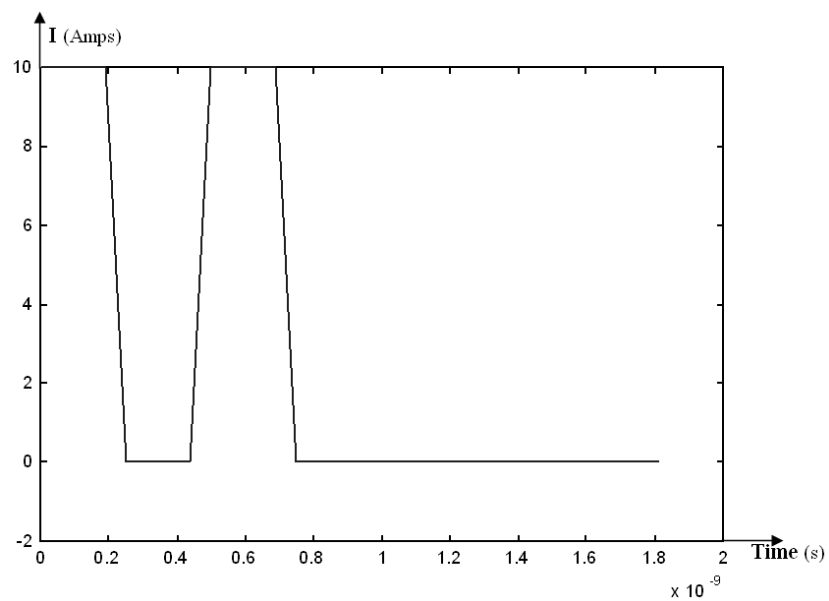
Figure 37: Microprocessor package: (a) top view of the single chip module and (b) trans-impedance V_s frequency.

2.3 Simulation of a switching microprocessor in high speed computer applications

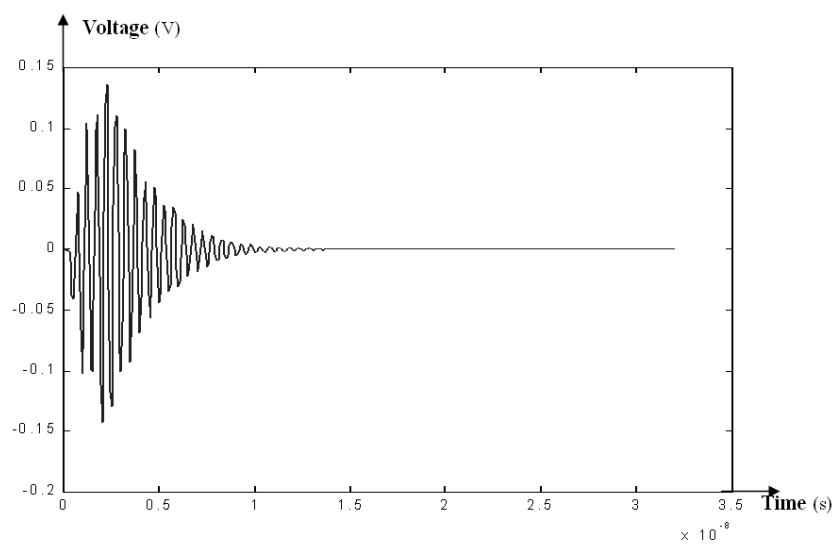
In this section, the effect of coupling between plane pairs for a gigahertz microprocessor application is discussed. Consider the test case of a single chip module shown in Fig. 37(a). The chip measures $2\text{cm} \times 2\text{cm}$ and is mounted on a package of size $4.8\text{cm} \times 4.8\text{cm}$. Three planes are used to supply power to the chip which is similar in cross section to Fig. 35(a) where the top plane is the voltage plane for the core and the bottom plane is the voltage plane for the input/output (I/O). The center plane serves as the common ground for the voltage plane $V1$ and $V2$. The separation between the planes is $T = 150\mu\text{m}$ and the plane thickness is $t = 10\mu\text{m}$. Tungsten was used as the metallization with conductivity $\sigma = 0.67 \times 10^7$ (s/m). The space between the planes was filled with a dielectric with relative permittivity $\varepsilon = 9.8\varepsilon_0$.

Consider groups of circuits within the microprocessor core switching simultaneously. They are powered by the top two planes in the package. These circuits are represented as “*” in Fig. 37(a) where each group of circuits is a 10 A current source, for a total of 50 A for the microprocessor. A field point is also shown in Fig. 37(a) between the center and bottom plane at which the coupled noise is measured. The coupling between the five sources and the field point is shown in Fig. 37(b), which was computed using (2.16). In Fig. 37(b), superposition has been used whereby the individual response from the five sources have been computed and added together. As can be seen in Fig. 37(b), maximum coupling occurs at 2 GHz.

Consider next a switching frequency of 2 GHz for the microprocessor core which translates to a period of 0.5 ns with rise time and fall time of 62.5 ps, as shown in Fig. 38(a). When the microprocessor core switches for two cycles, it couples energy into the I/O power supply as shown in Fig. 38(b). This was computed using the frequency response in Fig. 37(b) with the source current defined in Fig. 38(a). From Fig. 38(b), the maximum coupled noise for two switching cycles is ± 100 mV. However, when the core switches for 30 cycles as shown in Fig. 39(a), more coupled noise can be generated in the system. The coupled energy in Fig. 39(b) gradually increases during the initial 5 ns, reaches a steady state and



(a)



(b)

Figure 38: Excitation and voltage fluctuation for two switching cycles: (a)source waveform, (b)coupled voltage.

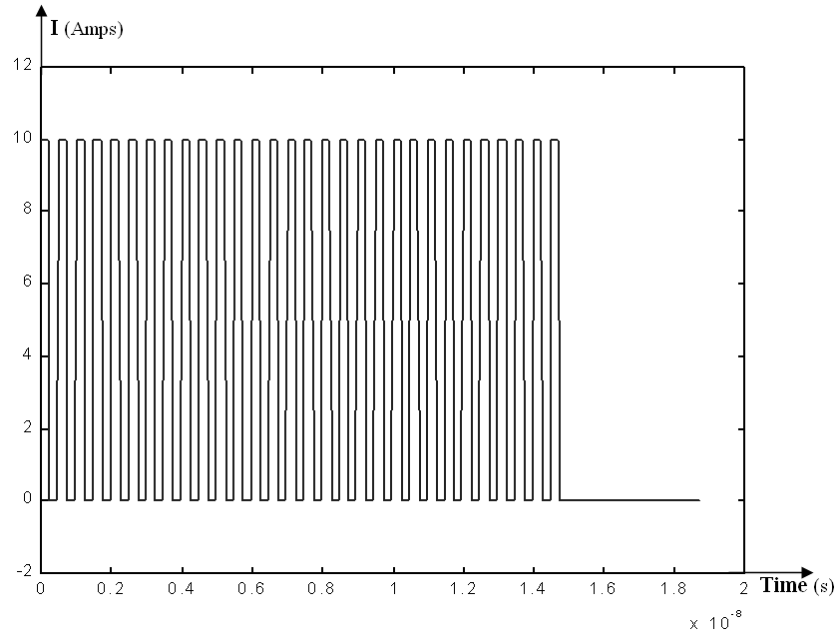
gradually decreases after the core stops switching. It is interesting to note that the I/O power supply bounces ± 400 mV in the steady state which is large and therefore cannot be ignored. Moreover, the coupled energy lasts for 5 ns even after the core has stopped switching due to the high quality factor of the cavity. Both these effects can deteriorate the functioning of future microprocessors operating at gigahertz frequencies. In addition, the interconnect I/Os in the package operating at high frequencies can also cause coupling between plane layers.

Fig. 40 shows a plot of the trans-impedance at 2 GHz between the source and field points, as the position of the field point is varied. From Fig. 40, it is apparent that the field penetration phenomenon induces varying magnitudes of disturbance voltage at different positions of the field point. The coupled voltage exhibits a standing wave pattern across the plane surface consisting of peaks and nulls. The peaks located at the center and corner of the power planes lead to the maximum coupling of energy resulting in large voltage fluctuations.

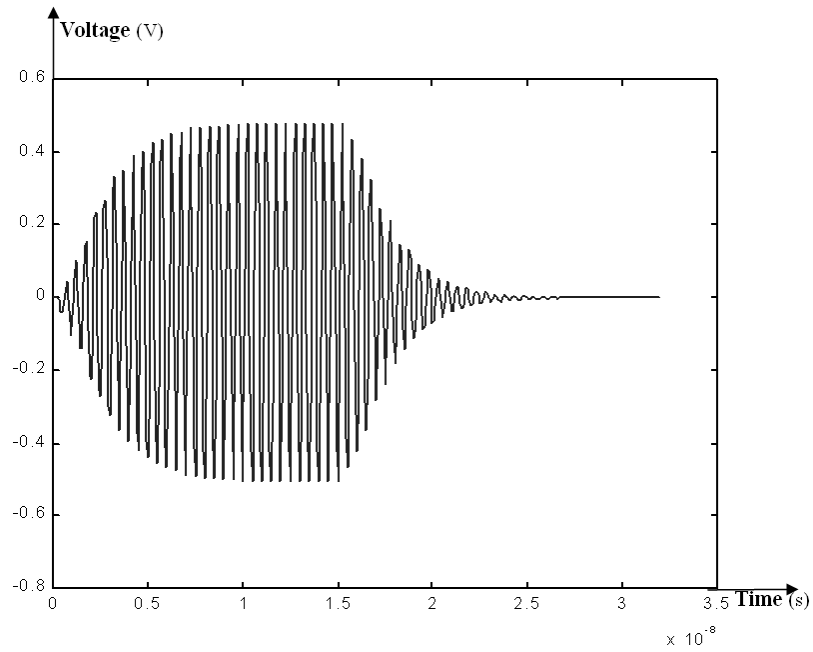
2.4 *Suppression of power plane coupling between layers*

The coupled noise between plane pairs discussed above is undesired and needs to be suppressed. In [45] and [50], optimization methods have been proposed to minimize the impedance between ports by varying the position of the excitation and coupled ports. Since Eq. (2.1) and (2.16) contain similar cosine factors that capture the position of the ports, these optimization methods can be applied to minimize the coupling between power planes.

An alternate method for minimizing coupling is by varying the metal conductivity σ_c and metal thickness t which occur in Eq. (2.16). To show the effect of conductivity on coupling, the structure in Fig. 37(a) was simulated with two different metallizations, tungsten ($\sigma_c = 0.67 \times 10^7$ s/m) and copper ($\sigma_c = 5.81 \times 10^7$ s/m). It can be observed from the comparison in Fig. 41 that the plane with copper metallization has much smaller trans-impedance as compared to the plane with tungsten metallization. Since the conductivity is at the denominator of Eq. (2.16), the scaling factor would be smaller for higher conductivity metal. Since copper has higher conductivity, the attenuation constant $\alpha = \sqrt{\pi f \mu \sigma_c}$ (real



(a)



(b)

Figure 39: Excitation and voltage fluctuation for 30 switching cycles: (a)source waveform, (b)coupled voltage.

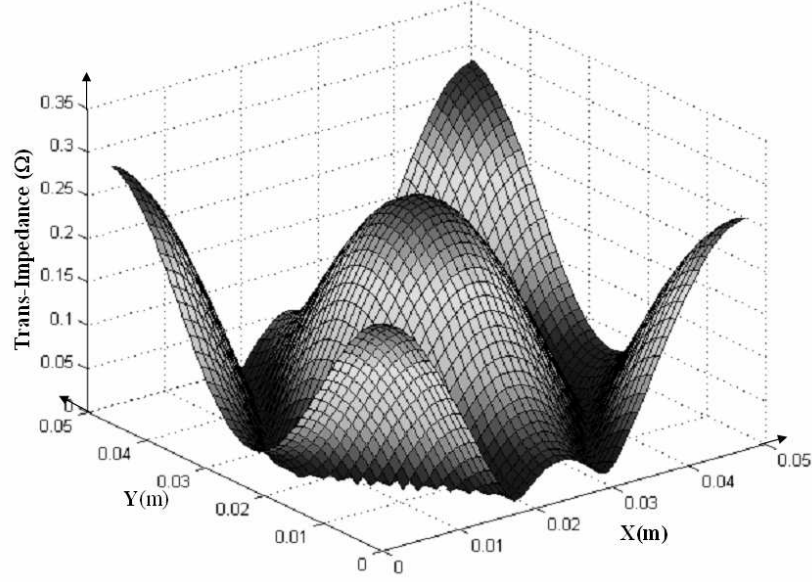


Figure 40: Coupling as a function of location

part of γ) is larger which results in a smaller depth of penetration of the magnetic field and current in the center plane.

Another important parameter in the scaling factor in Eq. (2.16) is the thickness of the metal plane t . To demonstrate its effect, the structure in Fig. 37(a) was simulated with varying thickness by assuming tungsten as the metallization. The results are shown in Fig. 42 where a larger metal thickness results in better isolation between plane pairs.

The coupled noise can also be suppressed by reducing the quality factor Q of the cavity. This can be achieved by reducing the dielectric thickness between the planes or by increasing the loss tangent of the dielectric material.

An alternate method which is not related to the impedance in Eq. (2.16) is to use decoupling capacitors to reduce the impedance of the planes [50].

2.5 Summary

This chapter discussed a method for modeling the effect of field penetration through planes in package power distribution networks. The correlation between measurement and computation demonstrates the validity of the approach. The effects of penetrating fields have

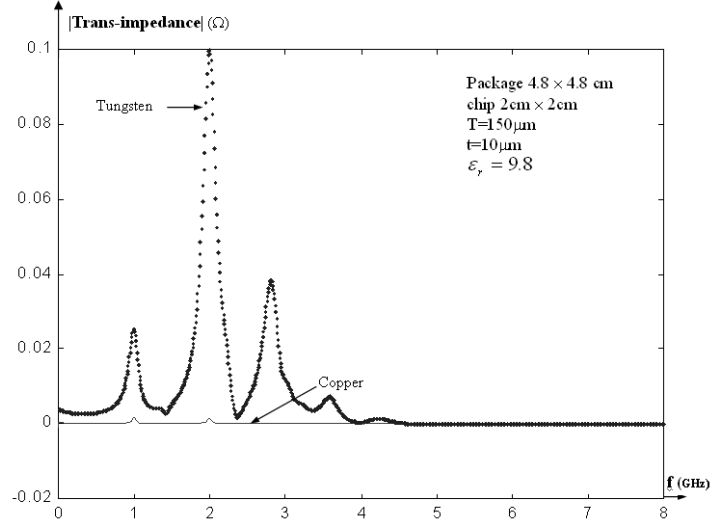


Figure 41: Effect of metal conductivity on trans-impedance

been computed both in the frequency and time domain, for a microprocessor that switches continuously over many cycles. Based on the analysis, large coupled noise was generated in the system due to the coupling between the plane layers, in the steady state. Methods to reduce this noise were suggested by using thick planes with high conductivity metal.

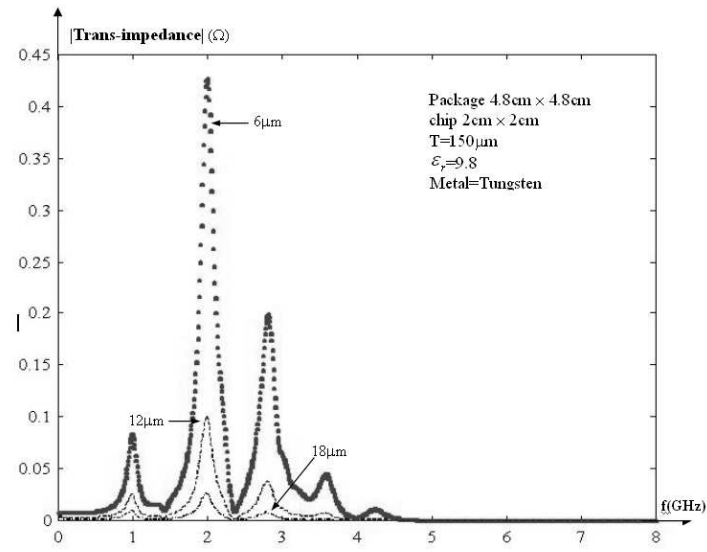


Figure 42: Effect of metal thickness on trans-impedance

Since the modeling method is an extension of the cavity resonator method for a single plane pair, the solution retains its analytical representation. Hence, multiple plane layers can be analyzed using this method.

The rapidly changing world is in constant pursuit of faster electronics. In the past, isolation between the plane layers could be assumed due to the smaller clock frequency compared with the package resonance frequency. As clock frequency for microprocessors increases, it coincides with package resonance frequency, and causes coupling between the layers. Thus, the modeling method developed in this chapter can be used for pre-layout power integrity analysis and methods for reducing coupled noise can be used as a guideline for package design.

CHAPTER III

MODELING OF ON-CHIP POWER GRID ON LOSSY SILICON SUBSTRATE

In the system hierarchy of a power distribution network, the design of on-chip power grid and analysis of its impact on the timing and noise characteristics are important. The deep sub-micron trend in semiconductor products is requiring enhanced modeling and simulation techniques for on-chip power distribution networks. This chapter presents a methodology for modeling the power grid over a lossy silicon substrate, as shown in Fig. 43. A combination of conformal mapping and complex image techniques (CIT) have been used for the electromagnetic modeling of the power grid. Using a first-order Debye approximation, the power supply noise has been simulated using the Finite Difference Time Domain (FDTD) method.

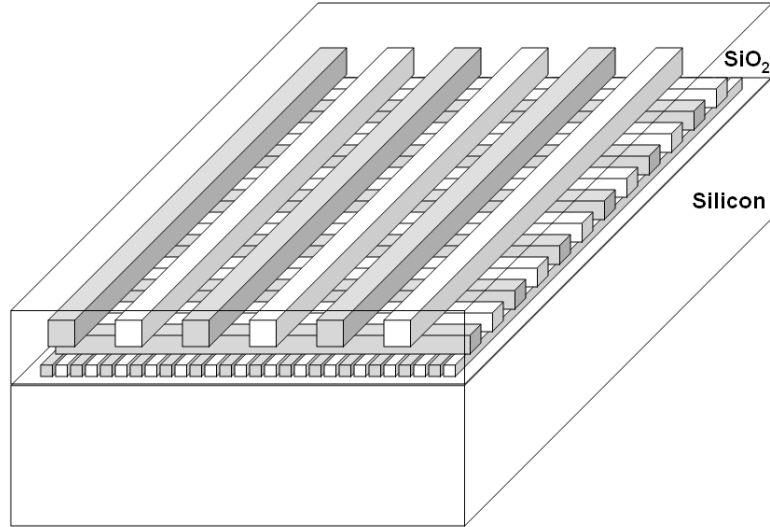


Figure 43: Multilayered on-chip power grid

This chapter is organized as follows. In Section 3.1, the combination of conformal

mapping and CIT is introduced to model coplanar waveguide (CPW) on a lossy silicon substrate. In Section 3.2, a conformal mapping technique has been developed for modeling the on-chip power grid, which provides closed-form expressions for extracting frequency dependent RLGC parameters of the periodic power/ground buses over lossy silicon substrate. Also in Section 3.2, the effect of oxide thickness on substrate loss is quantified. Then first-order Debye approximation of impedance and admittance parameters and its FDTD implementation are discussed in Section 3.3. Finally, examples are provided to demonstrate the effect of substrate resistivity on switching noise in on-chip power distribution network in Section 3.4 followed by the summary in Section 3.6.

3.1 Modeling of CPW on lossy silicon substrate

An accurate model of the interconnects forming the power grid on silicon substrate is essential for on-chip power grid analysis. The propagation characteristics of the transmission line on the conductive silicon substrate are characterized by three modes, namely, quasi-TEM, slow-wave and skin-effect modes [69]. The modal characteristics and the distributed transmission line parameters exhibit a significant frequency dependence. Though different numerical methods such as PEEC [103] or measurement-based methods such as the non-physical RLGC model from TDR measurement [3] can be used for extracting these characteristics, it is very desirable to develop analytical models for the computer-aided-design (CAD) of the power distribution network. The model from analytical expressions gives an alternative for characterizing the transmission line and provides a strong physical insight into dispersion and loss mechanism of transmission line over a conductive substrate.

3.1.1 Relationship between CPW and on-chip power grid

A side view of a typical power grid layout is illustrated in Fig. 44. Parallel and alternating power (Vdd) and ground (Vss) buses form an array of transmission lines. The buses on neighboring layers are orthogonal to each other, and buses of the same potential are tied together with vias at crossover points. The distance between adjacent power buses or ground buses in a layer (pitch) is relatively large at the chip-package interface and it shrinks gradually as the power buses get closer to active circuits on the silicon. The power grid is

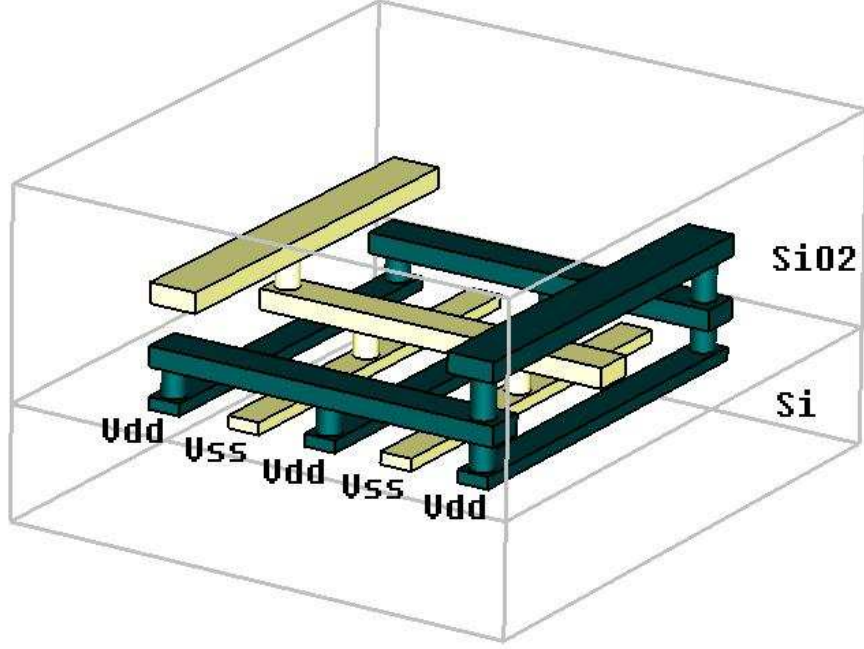


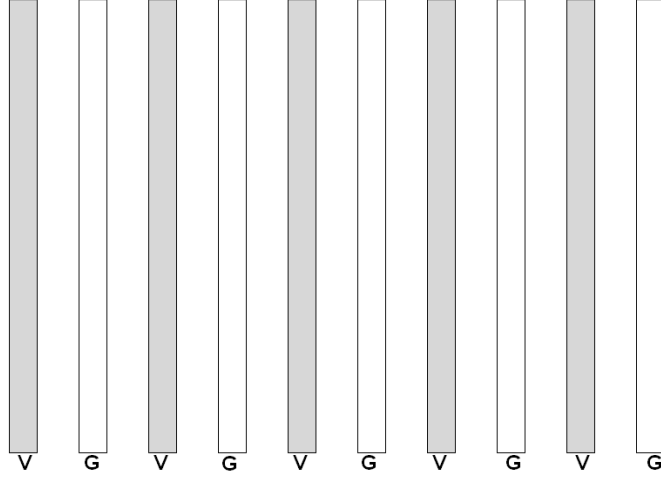
Figure 44: Side view of on-chip grid

embedded in SiO_2 and is present over a silicon substrate, as shown in Fig. 44.

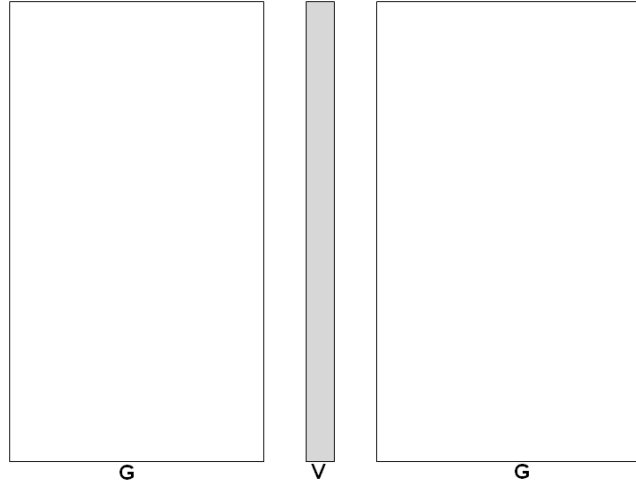
The interdigitated Vdd and Gnd buses on the same layer of an on-chip power grid, as shown in Fig. 45(a), have a uniform and periodic distribution. The alternating potential configuration of the buses shows similarity to a coplanar waveguide where three neighboring buses form a G-V-G pattern, which is the same as the CPW transmission line as shown in Fig. 45(b). Based on the principle that similar geometry may possess similar electrical properties, CPW on silicon substrate has been studied in this section for capturing the electrical characteristics of the on-chip power grid. The difference between the on-chip buses and CPW is attributed to the symmetry of the field distribution and the distribution of the return current, which has been studied in Section 3.2.1.

3.1.2 Field pattern of CPW on silicon substrate

The electric field distribution of CPW over silicon substrate is shown in Fig. 46. The electric field distribution was obtained using FEMLABTM which uses finite element method to solve differential equations of electric potential in the dielectric under certain boundary conditions [113]. The boundary conditions were set up as follows: the electric potential at



(a)



(b)

Figure 45: Top view of (a) Interdigitated on-chip buses, and (b) CPW

the center trace (signal trace) was 1 V and those at the sides and bottom ground plane was 0 V. The gaps between signal trace and left/right ground plane were set up as perfect magnetic surfaces, for which the explanation is discussed in Section 3.1.3. The silicon has a relative permittivity of 11 and conductivity of $100 \Omega\text{-cm}$. It can be observed from Fig. 46 that CPW has a symmetric electric field distribution around the center of the signal trace.

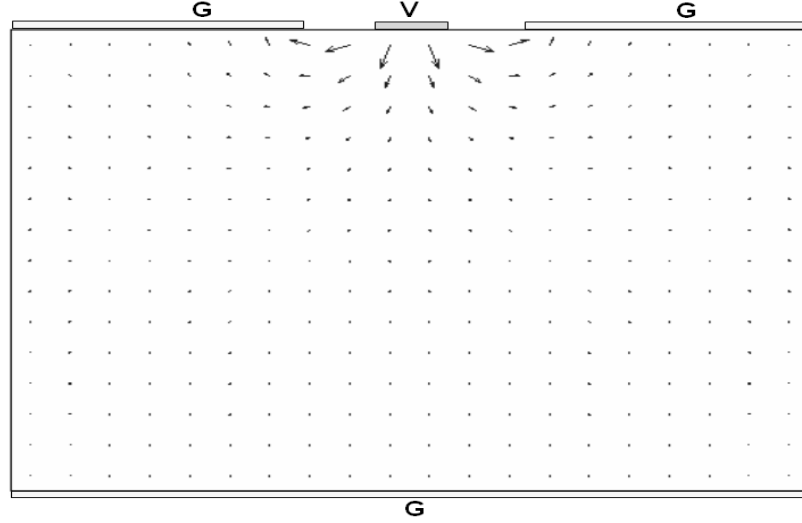


Figure 46: Field distribution of CPW

3.1.3 Parasitic extraction of CPW over lossless substrate

In this subsection, an analytical model for CPW fabricated on a lossless substrate is described. In the next subsection, complex image technique is used with the analytical model to develop a complete model for CPW on a silicon substrate.

A modeling method for lossy CPW has been discussed in [75], where CPW is modeled as a coplanar coupled three-line system, which generates a 3×3 matrix as the solution. The methodology proposed in this section uses an analytical solution for CPW, which provides a much simpler model than the coupled line approach [130].

Using the quasi-static approximation, effective permittivity ε_{eff} , characteristic impedance Z and propagation constant γ of a transmission line can be calculated as

$$\varepsilon_{eff} = \frac{C_{line}}{C_0} \quad (3.1a)$$

$$Z = \frac{1}{cC_0\sqrt{\varepsilon_{eff}}} \quad (3.1b)$$

$$\gamma = j\omega\sqrt{\mu_0\varepsilon_0\varepsilon_{eff}} \quad (3.1c)$$

where c is the speed of light, C_{line} is the line capacitance of the transmission line, and C_0 is the line capacitance when no dielectrics exist. In Eq. (3.1), parameters C_{line} and C_0 have to be found first in order to obtain other parameters. For coplanar waveguide with a lower

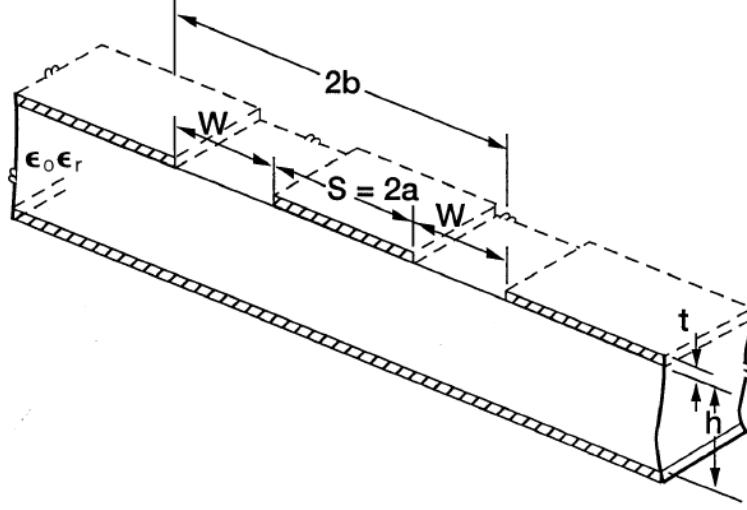


Figure 47: Conductor backed coplanar waveguide

ground plane as shown in Fig. 47, the line parameters have been derived in [80] as

$$\varepsilon_{eff} = C_{CPW}/C_0 = (1 + \varepsilon_r \frac{K(k')}{K(k)} \frac{K(k_3)}{K(k'_3)}) / (1 + \frac{K(k')}{K(k)} \frac{K(k_3)}{K(k'_3)}) \quad (3.2a)$$

$$Z = \frac{60\pi}{\sqrt{\varepsilon_{eff}}} \times 1 / (\frac{K(k)}{K(k')} + \frac{K(k_3)}{K(k'_3)}) \quad (3.2b)$$

where

$$k = a/b$$

$$k_3 = \tanh(\pi a/2h) / \tanh(\pi b/2h)$$

$$k' = \sqrt{1.0 - k^2}$$

$$k'_3 = \sqrt{1.0 - k_3^2}$$

and $K(k)$ is the complete elliptic integral of the first kind.

The derivation of the above analytical expression follows an approximate conformal mapping technique, which is based on the assumption that the gap between signal and ground, W , can be represented as a perfect magnetic surface – that is, by enforcing Neumann boundary conditions. This assumption leads to excellent results even for fairly large gaps [79]. According to this hypothesis and neglecting the thickness of the conductors, the line capacitor is obtained by summing up the upper half-space capacitance with twice the capacitance of the section shown in Fig. 48(a). The detailed derivation is provided in [80]

and only a picturised representation of the conformal mapping method, as shown in Fig. 48, has been used to discuss the method in this section.

Conformal mapping transforms the original geometry into a regular shape but still maintains the boundary conditions, orthogonality of the field, and the capacitance. The first conformal mapping used in C_{CPW} calculation transforms the field inside the strip in x -plane into an open space and the boundary is converted into the x coordinate axis of the t -plane. The second conformal mapping closes the boundary into a rectangle in the w -plane.

3.1.4 Effect of lossy silicon substrate on CPW characteristics

The previous section provides simple analytical expressions for ε_{eff} and Z as a function of the geometry, yet it is derived under the condition that the dielectric is lossless. To take into account the loss due to eddy currents in the silicon substrate, complex image technique is adopted. As shown in Fig. 49, the lossy substrate is approximately replaced by a virtual conducting image plane located at a complex distance h_{eff} from Vdd. The effective height h_{eff} obtained from complex image technique [71] is a function of frequency and substrate resistivity, which can be written as:

$$h_{eff} = h_{ox} + \frac{(1-j)}{2} \delta \tanh[(1+j)h_{si}/\sigma] \quad (3.3)$$

where $\delta = 1/\sqrt{\pi f \mu_0 \sigma}$ is the skin depth of the bulk silicon. By substituting h with h_{eff} in the analytical expressions for $\varepsilon_{eff}(a, b, h)$ and $Z_0(a, b, h)$ for conductor-backed CPW, the final model provides an analytical model of the CPW which takes into account the geometry as well as the substrate loss. To compare the results of this approach with those of other methods including measurement, one more step has been used to convert the interconnect parameters, ε_{eff} and Z , to S-parameters using the following expressions [99]:

$$[S] = \frac{1}{D_s} \begin{bmatrix} (Z^2 - Z_0^2) \sinh(\gamma l) & 2ZZ_0 \\ 2ZZ_0 & (Z^2 - Z_0^2) \sinh(\gamma l) \end{bmatrix} \quad (3.4)$$

where $D_s = 2ZZ_0 \cosh(\gamma l) + (Z^2 + Z_0^2) \sinh(\gamma l)$. In Eq. (3.4), parameter l is the length of the CPW and $Z_0 = 50\Omega$ is the reference impedance of the measurement system.

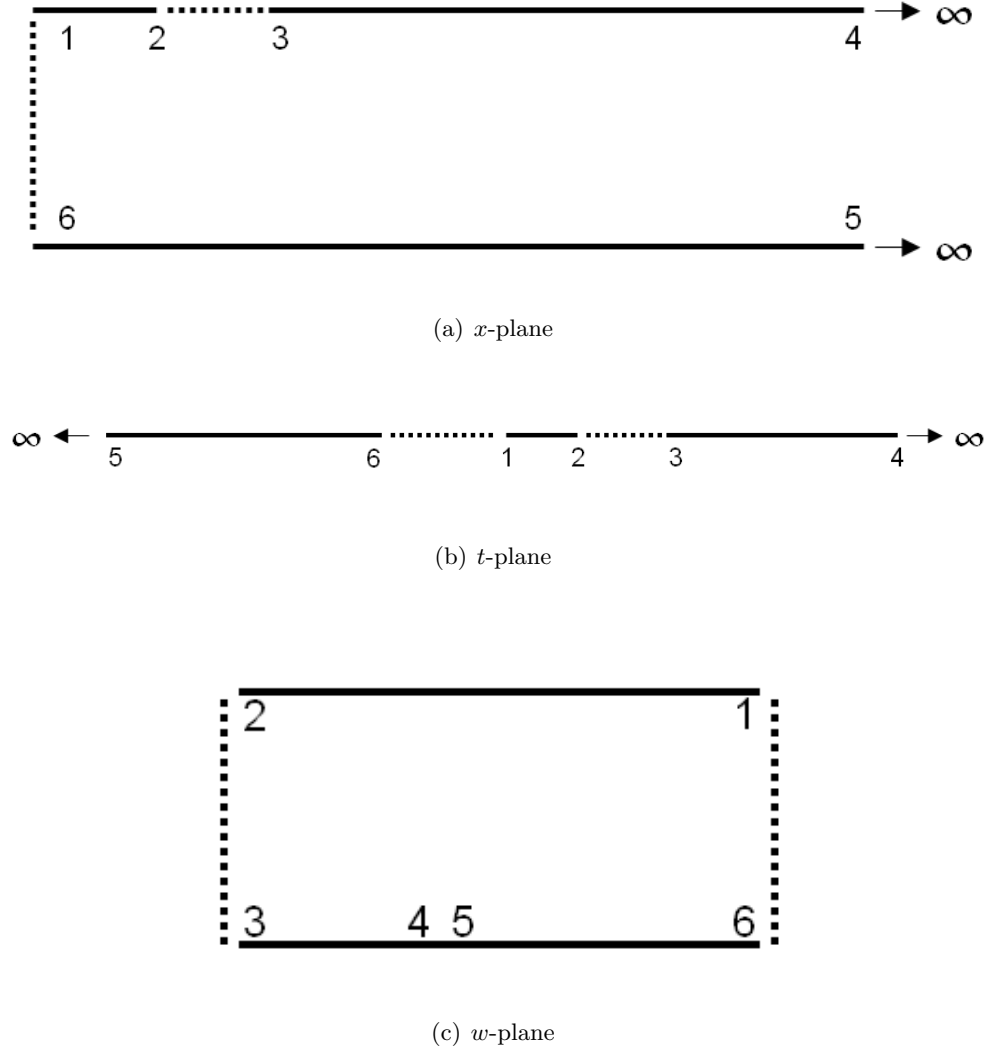


Figure 48: Conformal mapping for calculating C_{CPW} (a) coplanar waveguide lower right quadrant, (b) intermediate transformed quadrant in t -plane (c) final transformed geometry in w -plane

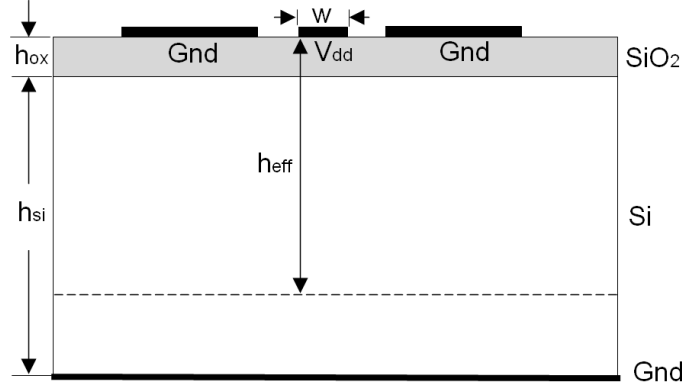


Figure 49: Conductor backed coplanar waveguide

3.1.5 Model to measurement correlation

To verify the accuracy of Eq. (3.2), several types of coplanar waveguide were designed and fabricated on silicon wafers at the Packaging Research Center at Georgia Institute of Technology [129]. The fabrication process used the following parameters: $h_{ox} = 1\mu m$, $h_{si} = 0.5mm$, $w = 25\mu m$, $l = 1.5mm$, $\epsilon_{si} = 11.9\epsilon_0$ and $\epsilon_{sio_2} = 3.5\epsilon_0$. The silicon substrates had two different resistivities, namely, high resistivity $\rho = 2000\Omega\text{-}cm$ and low resistivity $\rho = 100\Omega\text{-}cm$. The numerical results from the closed form expressions of CPW showed good agreement with measurement data from a vector network analyzer (VNA) – AgilentTM 8720ES – as shown in Fig. 50 and Fig. 51 for high resistivity and low resistivity wafers, respectively.

3.2 Parasitic extraction for coplanar multi-conductor lines in on-chip power grid networks

In this section, the combination of complex image and conformal mapping technique is applied for modeling the on-chip power grid. The terminology “Coplanar Multi-conductor (CMC)” structure has been introduced here to describe the interdigitated Vdd and Gnd buses on the first layer of an on-chip power grid (M1 layer), which has the periodic structure as shown in Fig. 52. In Fig. 52, parameters w and s denote the width of the traces and the distance between neighboring traces, respectively. Parameters h_{ox} and h_{si} denote the

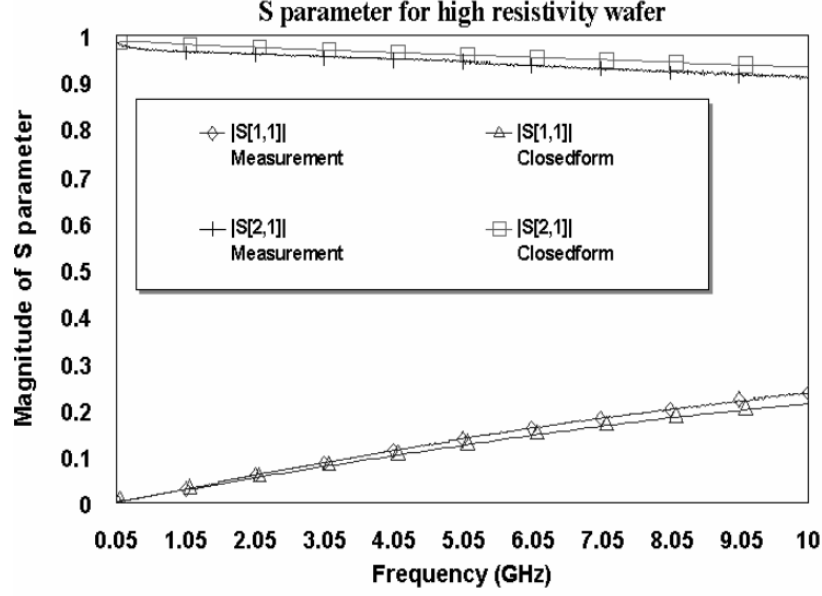


Figure 50: Measurement vs. analytical model for high resistivity wafer

thickness of SiO_2 and the thickness of silicon substrate, respectively.

3.2.1 Field distribution on M1 layer

The electric field distribution of CMC structure calculated using FEMLABTM [113] is shown in Fig. 53(a). The boundary conditions were set up as follows: the electric potential on Vdd traces was 1 V and those on Gnd traces and bottom ground plane was 0 V. The gaps between Vdd and Gnd traces were set up as perfect magnetic surfaces since there is no electric field normal to the line connecting Vdd and Gnd traces [79] [80]. The silicon has a relative permittivity of 11 and conductivity of $100 \Omega\text{-cm}$. Compared with Fig. 47, it can be observed that CPW and CMC structure share the common feature that the neighboring interconnections contain opposite potentials. However, the CMC structure has two distinct features, namely, 1) Its uniform topology causes symmetric field around the center of each wire, and 2) The return current distribution is changed since Gnd traces have the same dimension as Vdd traces.

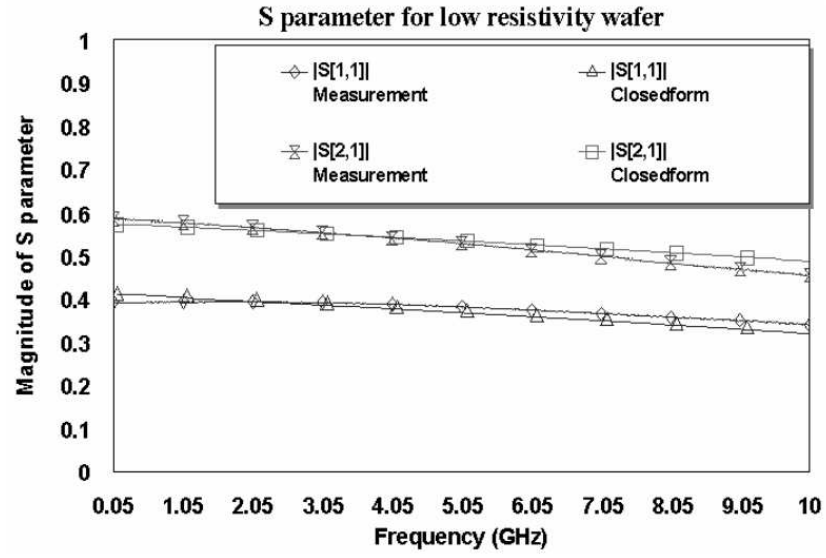


Figure 51: Measurement vs. analytical model for low resistivity wafer

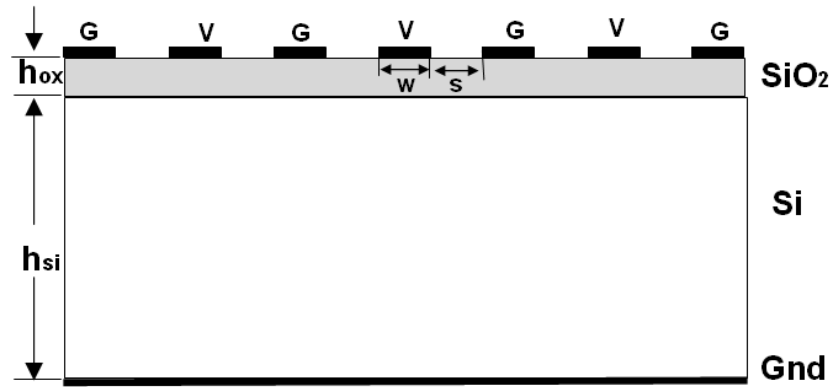
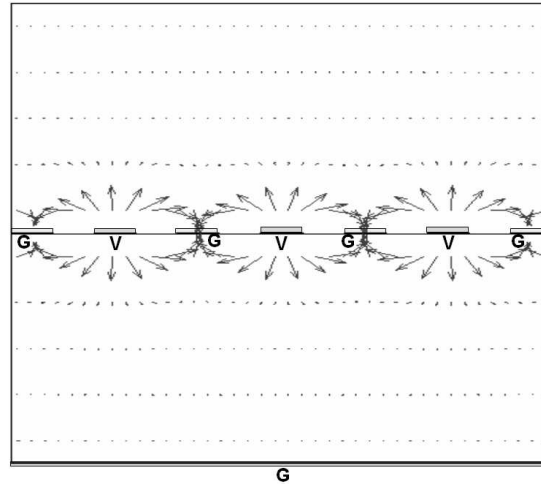
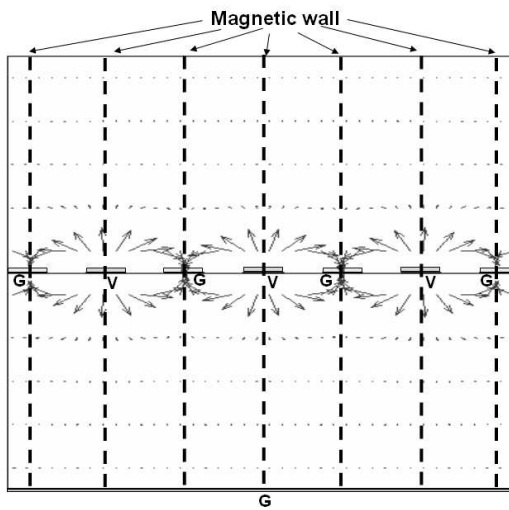


Figure 52: Cross section of first layer on-chip power bus (M1 layer)



(a)



(b)

Figure 53: CMC lines (a) Electric field of CMC, and (b) Magnetic walls at the center of all buses

Due to the periodic topology and symmetric field distribution in a CMC structure, imposing magnetic walls at the center of Vdd and Gnd traces, as shown in Fig.53(b), does not change the field distribution because there is no electric field normal to the line perpendicular to the center of each wire. This property has been utilized in the next section to extract the parasitics of the CMC lines.

3.2.2 Parasitic extraction

The similarity and difference between CPW and CMC structure has been used to develop the modeling approach for the CMC structure in this section. The combination of CIT with quasi-static approximation has been applied for modeling the CMC structure. However, the method described earlier has been modified to extract the effective permittivity of the CMC structure, namely, $\varepsilon_{eff} = C_{CMC}/C_0$. The key issue in this approach is an efficient way to compute the capacitance C_{CMC} .

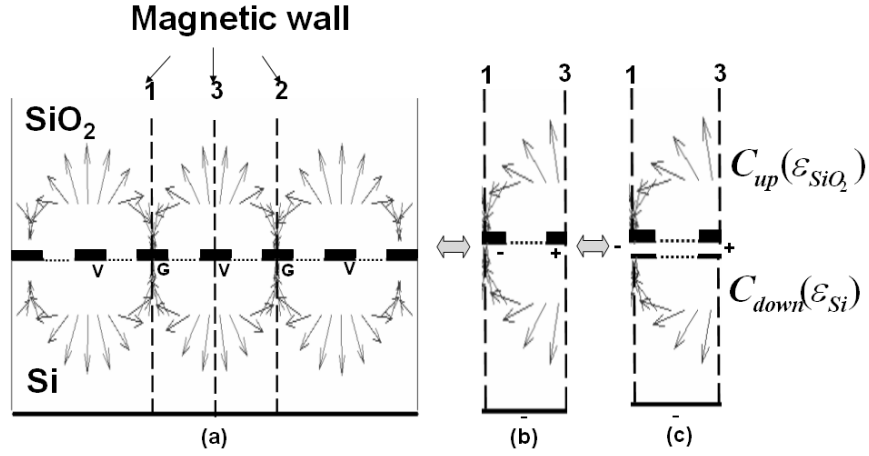


Figure 54: Electric field of CMC structure and capacitor calculation

To calculate the capacitance C_{CMC} , magnetic walls No. 1,2 and 3 are imposed at the center of a Vdd bus and two neighboring Gnd buses as shown in Fig. 54(a). The field confined by magnetic walls No. 1 and 2 contributes to the line capacitor C_{CMC} . It is efficient to calculate electric field only on one side of the magnetic wall No. 3 to reduce the computation complexity since the electric field is symmetric around the magnetic

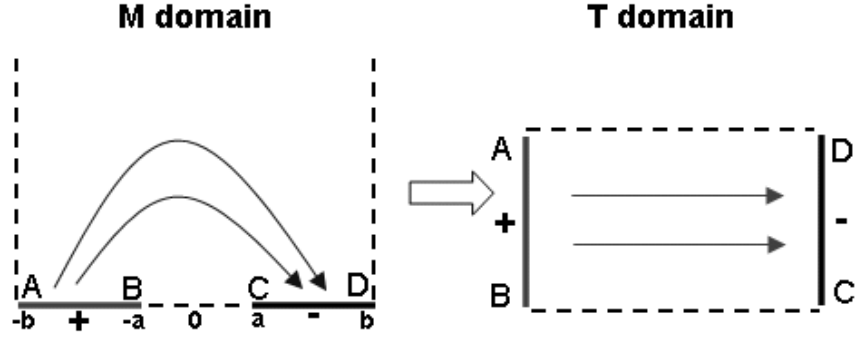


Figure 55: Conformal mapping of C_{up}

wall No. 3, as shown in Fig. 54(b). Furthermore, as shown in Fig. 54(c), C_{CMC} is calculated by doubling the summation of $C_{up}(\varepsilon_{SiO_2})$ and $C_{down}(\varepsilon_{Si})$, such that $C_{CMC}/2 = C_{up}(\varepsilon_{SiO_2}) + C_{Down}(\varepsilon_{Si})$. The quantities $C_{up}(\varepsilon_{SiO_2})$ and $C_{down}(\varepsilon_{Si})$ are obtained through the conformal mapping procedures described in this section.

In Fig. 55, $C_{up}(\varepsilon_{SiO_2})$ is determined by using Schwarz-Christoffel mapping derived in (3.5). The solid lines denote the perfect electric conductor (PEC) and the dotted lines denote the perfect magnetic conductor (PMC) or magnetic wall. This mapping transforms the original open geometry into a closed rectangle, in which the electric line of force has a canonical pattern with parameters as follows:

$$T = \int_{-b}^M \frac{dt}{\sqrt{t^2 - a^2}}, \quad (3.5a)$$

$$W = \int_{-b}^{-a} \frac{dt}{\sqrt{t^2 - a^2}}, \quad (3.5b)$$

$$d = \frac{1}{j} \int_{-a}^a \frac{dt}{\sqrt{t^2 - a^2}}, \quad (3.5c)$$

$$C_{up}(\varepsilon_{SiO_2}) = \frac{\varepsilon_0 \varepsilon_{SiO_2} W}{d} \quad (3.5d)$$

In Fig. 56, Capacitor $C_{down}(\varepsilon_{si})$ is obtained by going through two successive Schwarz-Christoffel mappings, which are derived in (3.6) and (3.7). In the first conformal mapping, the electric field inside the rectangle is mapped to the open space while the boundary of the box is transformed to the real axis. The second conformal mapping closes the real axis to

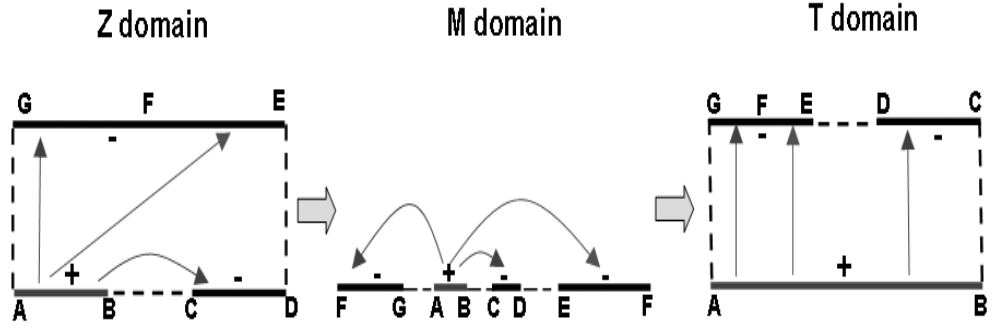


Figure 56: Conformal mapping of C_{down}

form a rectangle, where the boundary conditions are different from the original rectangle.

The resulting parameters are as shown below:

$$Z = \frac{b}{k} \int_0^M \frac{dt}{\sqrt{(1-t^2)(1-k^2t^2)}}, \quad (3.6a)$$

$$\frac{K}{K'} = \frac{b}{h}, \quad (3.6b)$$

$$K = \int_0^1 \frac{dt}{\sqrt{(1-t^2)(1-k^2t^2)}}, \quad (3.6c)$$

$$x = sn\left(\frac{aK}{b}, k\right) \quad (3.6d)$$

$$T = \int_{-1}^M \frac{dt}{\sqrt{(t + 1/k)(t + 1)(t^2 - x^2)}} \quad (3.7a)$$

$$W = \int_{-1}^{-x} \frac{dt}{\sqrt{(t + 1/k)(t + 1)(t^2 - x^2)}}, \quad (3.7b)$$

$$W_1 = \int_x^1 \frac{dt}{\sqrt{(t + 1/k)(t + 1)(t^2 - x^2)}} \quad (3.7c)$$

$$W_2 = \int_{-\infty}^{-1/k} \frac{dt}{\sqrt{(t + 1/k)(t + 1)(t^2 - x^2)}} + \int_{1/k}^{\infty} \frac{dt}{\sqrt{(t + 1/k)(t + 1)(t^2 - x^2)}} \quad (3.7d)$$

$$d = \frac{1}{j} \int_{-x}^x \frac{dt}{\sqrt{(t + 1/k)(t + 1)(t^2 - x^2)}}, \quad (3.7e)$$

$$C_{down}(\varepsilon_{si}) = \frac{\varepsilon_0 \varepsilon_{si} (W + W_1 + W_2)}{2d} \quad (3.7f)$$

where sn is the Jacobi elliptic function.

The above expressions provide a simple analytical solution for C_{CMC} from which ε_{eff} and Z can be obtained. To include the loss due to eddy currents in the silicon substrate, complex image technique is applied to the expressions by replacing the height of silicon h with complex distance h_{eff} given by (4.10), similar to the method described in Section 3.1. As a result, the effective permittivity ε_{eff} , characteristic impedance Z , and propagation constant γ can be obtained using the following expressions:

$$\varepsilon_{eff} = \frac{C_{CMC}}{C_0} \quad (3.8a)$$

$$Z = \frac{1}{cC_0\sqrt{\varepsilon_{eff}}} \quad (3.8b)$$

$$\gamma = j\varpi\sqrt{\mu_0\varepsilon_0\varepsilon_{eff}} \quad (3.8c)$$

To utilize the extracted model of CMC structure in SPICE-like simulator or circuit FDTD algorithm, lumped element representation of the on-chip buses is required. Hence, the following expressions (3.9) are used to extract RLGC transmission line parameters from

characteristic impedance Z , and propagation constant γ [99].

$$R = \text{Re}\{\gamma Z\} \quad (3.9a)$$

$$L = \text{Im}\{\gamma Z\}/\varpi \quad (3.9b)$$

$$C = \text{Im}\{\gamma/Z\}/\varpi \quad (3.9c)$$

$$G = \text{Re}\{\gamma/Z\} \quad (3.9d)$$

where Re and Im are the operators for extracting the real and imaginary part from a complex entity and ϖ is the angular frequency.

3.2.3 Accuracy of the extracted model

A simple test structure as shown in Fig. 57 was modeled to verify the accuracy of the derived analytical expressions. The capacitance calculated using conformal mapping was compared with that from FEMLABTM [113] as shown in Table 1. From Table 1, it is apparent that conformal mapping provides accurate analytical capacitance value for coplanar multi-conductor structures arising in on-chip power grids.

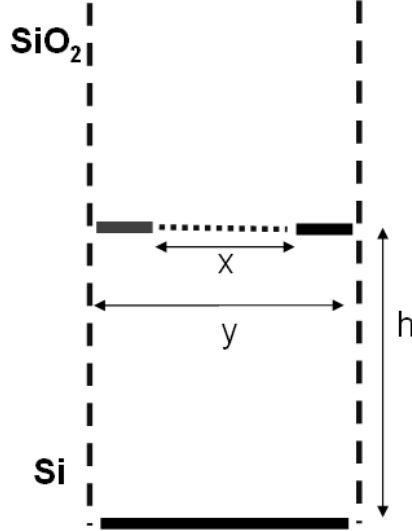


Figure 57: Test case of half CMC structure: $x = 5\mu m$, $y = 10\mu m$, $h = 250\mu m$, $\epsilon_{si} = 11.9\epsilon_0$ and $\epsilon_{sio_2} = 3.5\epsilon_0$

Table 1: Capacitance result from conformal mapping and FEM

Quantity	Conformal mapping	FEM (FEMLAB™)	error %
Capacitance (pF/m)	67.243	69.379	3.17
ε_{eff}	8.130	8.389	3.09

3.2.4 Comparison between CMC and CPW structure

The RLGC parameters for CMC structure in an on-chip power grid are frequency dependent and the simulation of frequency dependent parameters are therefore required, which has been discussed in Section 3.3. In this section, the RLGC parameters of a CPW and CMC structure over low resistivity substrate are compared using Fig. 58 to illustrate their difference. The CPW and CMC structure are configured to have the same geometry, namely $w = 25\mu m$, $h_{ox} = 1\mu m$, $h_{si} = 500\mu m$, except for the width of the ground wire, Vss, which is $300\mu m$ for CPW and $25\mu m$ for CMC structure.

The accuracy of a power grid model depends on the precise circuit representation of the individual power bus. Among the different types of planar transmission lines, CPW has the configuration that is closest to the layout of on-chip power grid, as explained earlier. Yet the discrepancy between the RLGC parameters of CPW and CMC invalidate the application of the CPW models for representing the periodic coplanar buses for the on-chip power grid. The difference in the series impedance parameters, R and L , can be explained by the different return current distribution of CPW and CMC lines. Since the return current is forced to flow on narrower Gnd traces of CMC lines rather than wide Gnd lines of CPW, higher inductance and resistance are obtained for CMC lines. Regarding shunt admittance parameters, C and G , the difference can be attributed to the positions of the two magnetic walls: The two side ground planes of an ideal CPW are infinite wide, for which two magnetic walls can be placed at \pm infinity without affecting the characteristics of CPW. Hence the distance between two magnetic walls for CPW is infinity. For CMC structure, as shown in from Fig. 54, the distance between two magnetic walls is the pitch of M1 layer. The closeness of magnetic walls of the latter force electric field to penetrate deeper into the silicon substrate, which leads to stronger frequency dependence due to the effect of lossy substrate, especially for the conductance parameter.

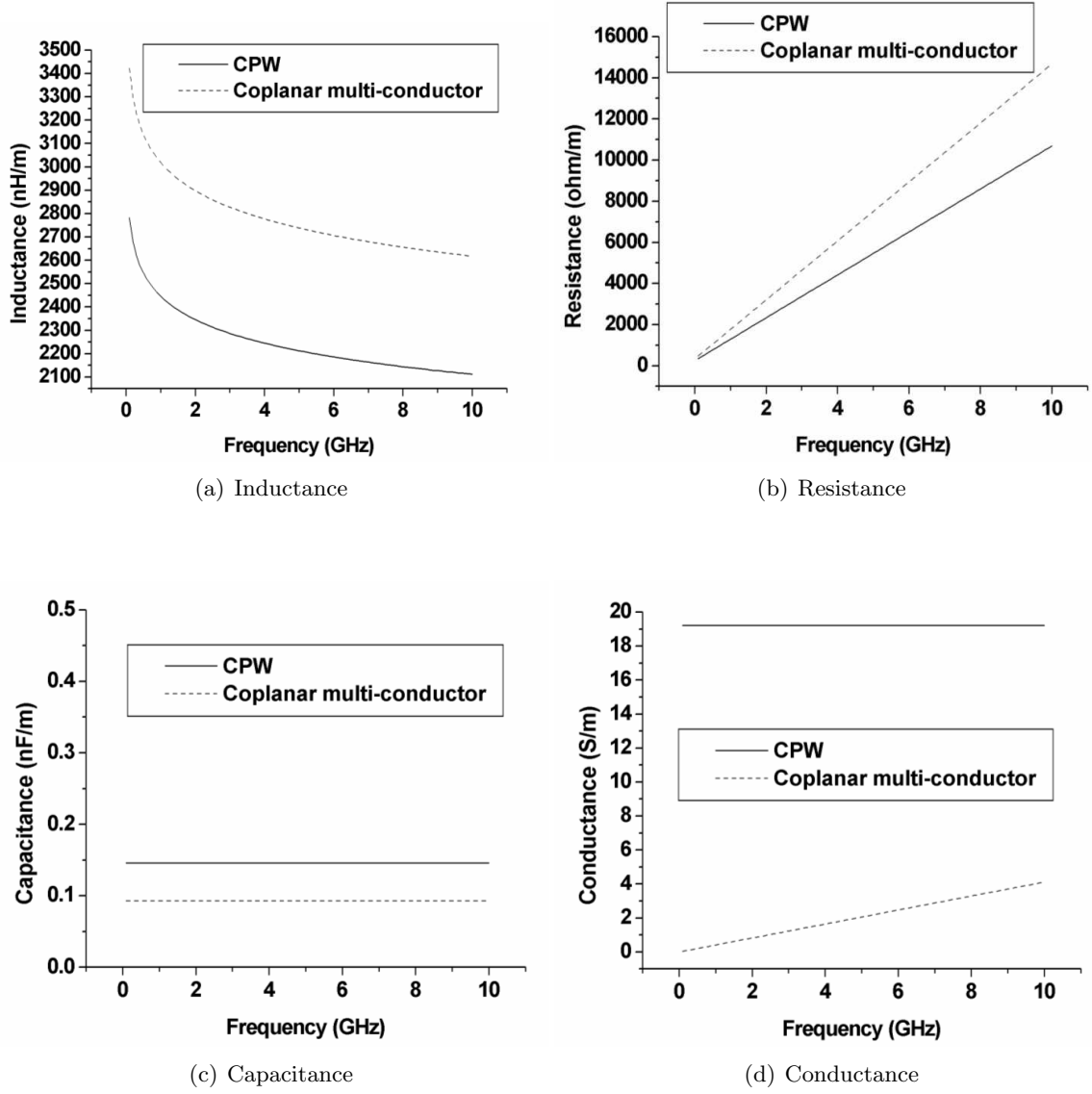


Figure 58: Comparison of parameters for CPW and CMC structure, (a) inductance, (b) resistance, (c) capacitance and (d) conductance

3.2.5 Effect of SiO₂ thickness

The eddy current in the silicon substrate serves as the return current for the on-chip power buses and it contributes to the conductance element G of the transmission line. The attenuation of on-chip simultaneous switching noise is directly related to the value of G , which determines the energy dissipation in the lossy substrate. The parameter G is a function of the conductivity of the substrate as well as the thickness of the SiO₂, which is the insulation layer between the metal and silicon substrate. In integrated circuit (IC) design, once the process is decided by the foundry technology, the conductivity of the semiconductor wafer is fixed. Thus, besides the decoupling capacitor, it leaves the chip designer only the freedom of changing the geometry of the power grid to maintain the power integrity.

The thickness of SiO₂, h_{ox} , has been studied in this section for its effect on the conductance element G . As an extension of the asymptotic solution for shunt admittance parameters, the parameter G is derived as a function of oxide thickness h_{ox} , which is given by,

$$G(h_{ox}, \varepsilon_{si}, \varepsilon_{sio_2}, \dots) = 4\pi^2 f^2 \sigma_{si} \varepsilon_{si}^2 \varepsilon_{sio_2}^3 w^3 C_\infty / (\varepsilon_0 h_{ox}^3 (\frac{\varepsilon_{si} \varepsilon_{sio_2} w}{h_{ox}} - C_\infty) (\frac{\sigma_{si}^2 \varepsilon_{sio_2}^2 w^2 C_\infty^2}{\varepsilon_0^2 h_{ox}^2 (\frac{\varepsilon_{si} \varepsilon_{sio_2} w}{h_{ox}} - C_\infty)^2} + 4\pi^2 f^2 (\frac{\varepsilon_{si} \varepsilon_{sio_2} w C_\infty}{h_{ox} (\frac{\varepsilon_{si} \varepsilon_{sio_2} w}{h_{ox}} - C_\infty)} + \frac{\varepsilon_{si} \varepsilon_{sio_2} w}{h_{ox}})^2)) \quad (3.10)$$

where ε_{si} , ε_{sio_2} , σ_{si} and w are the permittivity of silicon, permittivity of SiO₂, conductivity of silicon and the width of power buses, respectively. In Eq. (3.10), C_∞ is a constant which is the capacitance in the high frequency limit, as defined in [71].

Fig. 59. shows the conductance versus h_{ox} for a test case with $w = 4\mu m$, $h_{si} = 500\mu m$ and $f = 5$ GHz. It can be observed that as the thickness of the SiO₂ increases, the substrate loss G decreases, since eddy current in the substrate becomes weak as the sources move away from the silicon substrate. This result provides two advices to the on-chip power grid designer, namely, 1) Small h_{ox} leads to large loss and helps reduce switching noise, and 2) Silicon substrate has little effect on the conductance parameter G of the transmission line model for the interconnects far away from the substrate, such as the buses on the M3 layer and above. In the above example, if the interconnects of a power grid are larger than $5\mu m$ over the silicon, the G element is negligible. Thus, for the interconnect lines on higher

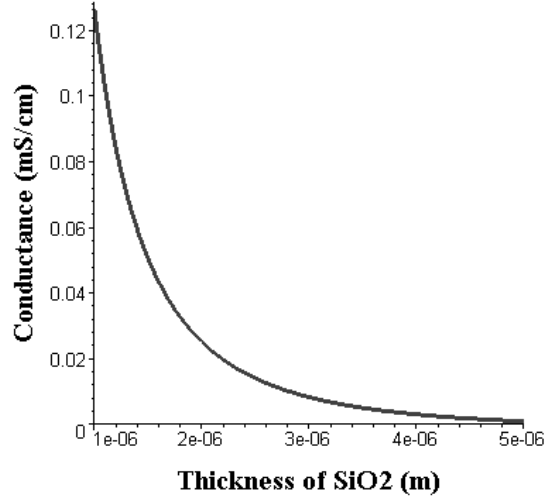


Figure 59: Conductance vs. SiO₂ thickness

layers, the modeling of the power bus can be simplified by ignoring the dielectric loss.

3.3 FDTD simulation for the on-chip power grid

In general, the RLGC parameters of the on-chip power grid are frequency dependent, especially for the M1 and M2 layers. When high-speed digital signal propagates on such a line, its waveform is altered owing to the frequency dependent nature of the dispersive transmission line. The time domain algorithms at present for the chip level simulation, such as hierarchical analysis [88] and multi-grid method [57] [58], do not take the frequency dependence into account. Neither does the LIM [63] and circuit based FDTD method [68]. In this section, a modified FDTD algorithm with the first-order Debye approximation is used to simulate the frequency dependent circuit model of the on-chip power grid.

3.3.1 Representing an on-chip power grid using constant RLGC parameters

A standard way to deal with the frequency domain function in the time domain is through convolution and Fourier transforms. However, they are not suitable for an on-chip power distribution network with millions of branches, each of which has frequency dependent RLGC elements. Hence, various approximations are usually used. One such approximation which is largely used is the constant RLGC model. In the on-chip power grid model as

shown in Fig. 60, each segment has a constant RLGC representation and the segments of one bus are serially connected. For the orthogonal buses with the same potential on the neighboring layers, they are tied together with vias at crossover points, which have a representation of serially connected resistor and inductor. In this circuit model, the capacitive coupling between neighboring layers due to crossover capacitor is not included, which has been studied in Chapter 4.

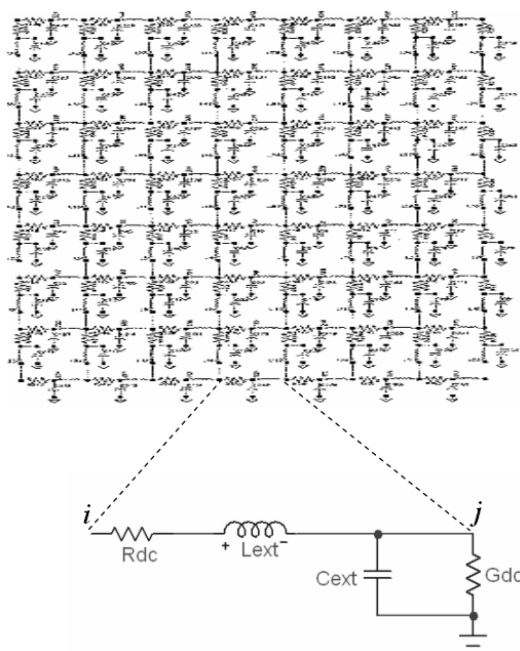


Figure 60: On-chip power grid with constant RLGC representation

Since during parameter extraction, shunt elements C and G are referred to the ground plane at the bottom of silicon substrate as shown in Fig. 52, that plane is modeled as a global ground node (node 0 in a SPICE netlist) for the circuit model representation of the entire on-chip power grid, as shown in Fig. 61. The updating equations of the FDTD method for solving a circuit with constant elements are discussed in the next subsection.

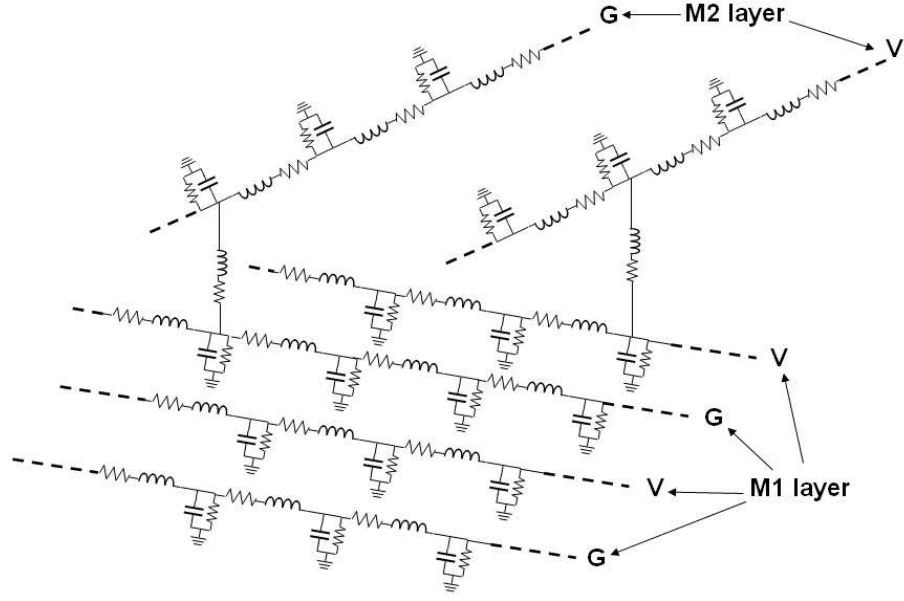


Figure 61: Constant RLGC representation of M1 and M2 layers

3.3.2 Implementation of FDTD for constant RLGC circuit model of on-chip power grid

The implementation of FDTD for a constant RLGC circuit model of the on-chip power grid uses the algorithm based on LIM [63], where the updating equations can be written as:

$$V_j^{n+1/2} = \frac{C_{ext}V_j^{n-1/2} - \sum_{k=1}^{M_i} I_{ik}^n}{C_{ext}/\Delta t + G_{dc}} \quad (3.11)$$

$$I^{n+1} = I^n + \frac{\Delta t}{L_{ext}}(V_i^{n+1/2} - V_j^{n+1/2} - R_{dc}I^n) \quad (3.12)$$

where parameters R_{dc} and L_{ext} are the constant resistance and inductance, G_{dc} and C_{ext} are the constant conductance and capacitance. In Eq. (3.11) and (3.12), Δt is the time step.

The procedure for time domain simulation follow the steps described below:

1. At time $T=0$, initial values $I_j(0)$ and $V_j(0)$ are assigned to each branch current and node voltage, respectively;

2. The node voltages $V_j, j = 1, 2, \dots$ are updated using expression (3.11), and the switching current is updated in each alternate time step separated by half a time step;
 3. The voltages $V_{dd}(=1)$ and $G_{nd}(=0)$ are enforced at appropriate nodes, to which DC supply is connected;
 4. The branch currents $I_j, j = 1, 2, \dots$ are updated using expression (3.12);
 5. The time step is advanced, $T=T+\Delta t$,
- if** ($T < T_{stop}$) , goes to step 2, where T_{stop} is the time limit to end simulation;
else quit and output.

3.3.3 Debye approximation for inclusion of frequency dependent RLGC circuit model

Being independent of frequency, the constant RLGC circuit model discussed in the previous subsection is an approximation at low frequency which does not take into account frequency dependence. Therefore, a better modeling technique– Debye rational approximation– has been used to approximate the frequency dependent RLGC parameters [84]. The advantage of Debye rational function approximation is that it can approximate the smooth behavior of RLGC parameters with a relatively small number of poles. The equivalent circuit representation of Debye model is obtained by replacing the standard transmission line model with a group of parallel and serially connected elements.

The parallel network represented in Fig. 62(a) corresponds to a model where only frequency dependent resistance R and inductance L of the transmission line are considered. Its Debye rational function is given by:

$$Z = R_{dc} + j\omega L_{ext} + j\omega \sum_{i=1}^N \frac{L_i}{1 + j\omega L_i/R_i} \quad (3.13)$$

where R_{dc} and L_{ext} denote the DC resistance and low frequency inductance of the line.

The series network represented in Fig. 62(b) corresponds to a model where only frequency dependent capacitance C and conductance G are considered. Its Debye rational

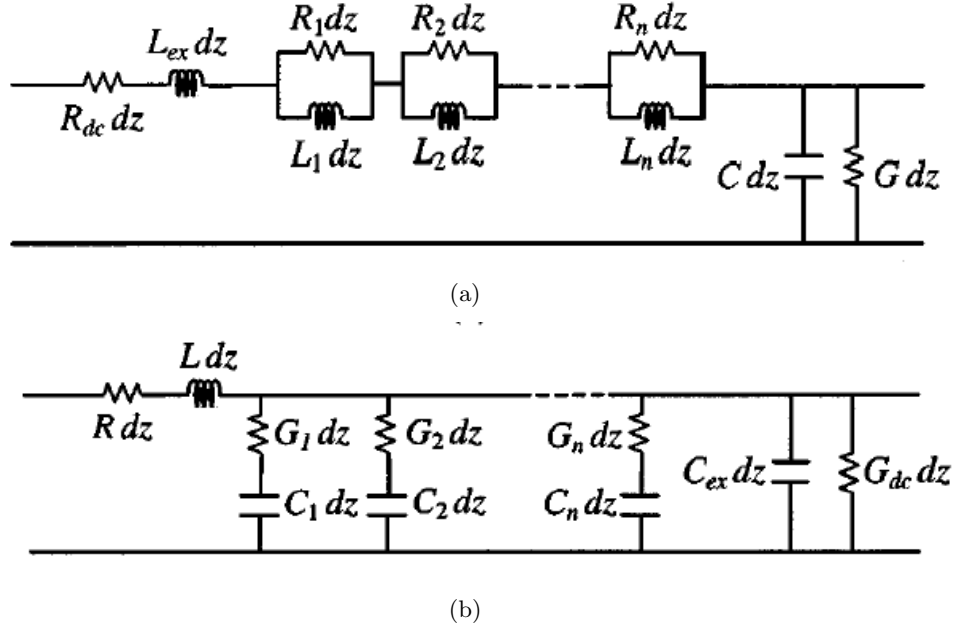


Figure 62: Equivalent circuit of unit length transmission line (a) Debye model for series R and L , (b) Debye model for shunt G and C

function can be written as:

$$Y = G_{dc} + j\varpi C_{ext} + j\varpi \sum_{i=1}^N \frac{C_i}{1 + j\varpi C_i/G_i} \quad (3.14)$$

where G_{dc} and C_{ext} denote the DC conductance and low frequency capacitance of the line.

During the approximation, the number of poles N must be chosen and then the corresponding R_i , L_i , G_i , and C_i can be determined by an optimization procedure, such as minimum least square technique suggested in [84]. It has been reported that a good matching over a frequency range reaching a few gigahertz can be obtained using no more than three or four Debye terms. While higher-order rational function approximations are possible, the relatively few number of terms provides an extremely simple model, such as the first order Debye circuit with $N = 1$, as shown in Fig. 63.

A simple test circuit as shown in Fig. 64 has been constructed to illustrate the effect of first order Debye model. It is an on-chip driver connected to a dispersive interconnect with the frequency dependent $R(\varpi)$, $L(\varpi)$, $G(\varpi)$, $C(\varpi)$ parameters as shown in Fig. 65. The value of each element in the first order Debye approximation is listed in Table 2. The

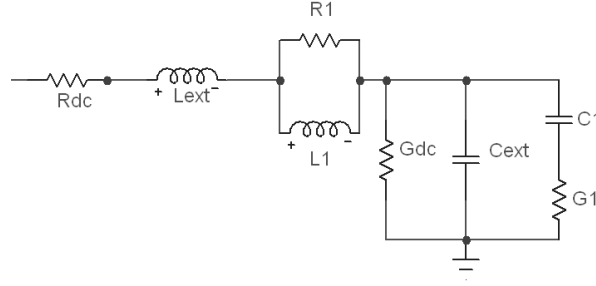


Figure 63: Circuit of first order Debye approximation

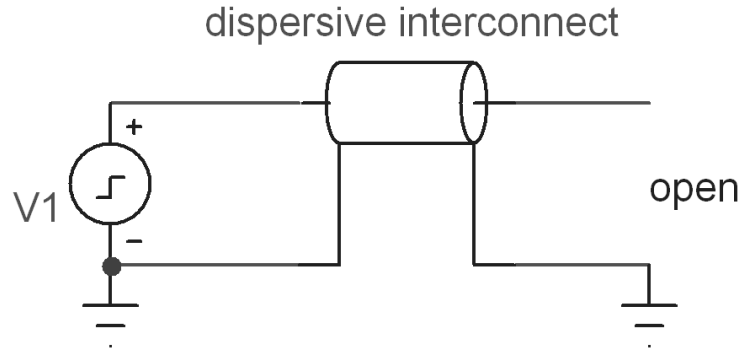


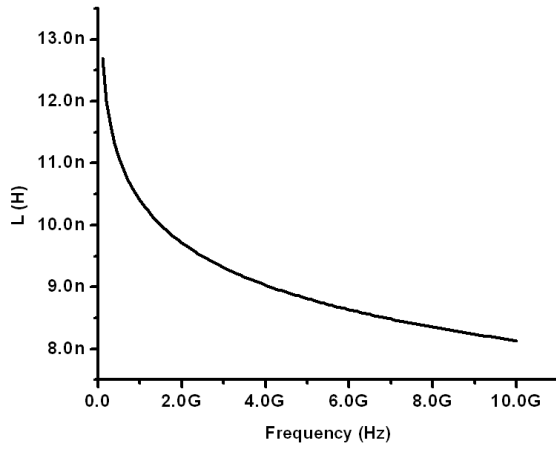
Figure 64: Example of using first order Debye model

approximated impedance and admittance parameters are correlated with those obtained from $Z(\varpi) = R(\varpi) + j\varpi L(\varpi)$ and $Y(\varpi) = G(\varpi) + j\varpi C(\varpi)$ in Fig. 66.

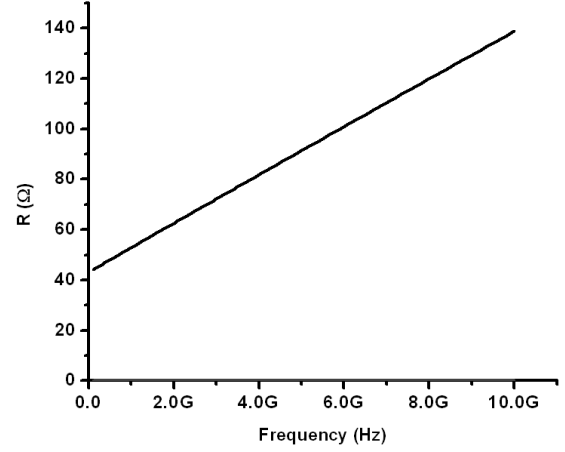
Table 2: Circuit elements in the first order Debye approximation

Impedance				Admittance			
R_{dc} (Ω)	R_1 (Ω)	L_{ext} (nH)	L_1 (nH)	C_{ext} (pF)	C_1 (pF)	G_{dc} (S)	G_1 (S)
45.8534	201.5576	6.3596	3.5367	0.37958	0.86351	1e-8	25.0254

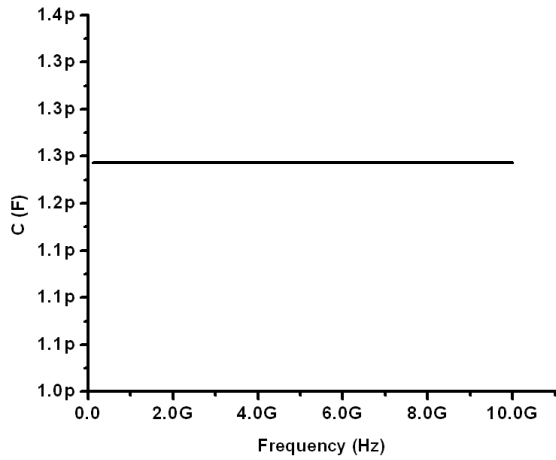
To illustrate the importance of including frequency dependent RLGC parameters in the time domain simulation, the test circuit has been simulated twice using SPICETM; one with constant RLGC parameters and the other with first-order Debye model using the parameters listed in Table 2. The voltage output of the driver is a trapezoid waveform, as shown in Fig. 67. The response of the circuit is observed at the far end of the transmission line. The results of constant RLGC model and first order rational approximation are shown in Fig. 67. It can be deduced that constant RLGC model cannot predict the correct propagation



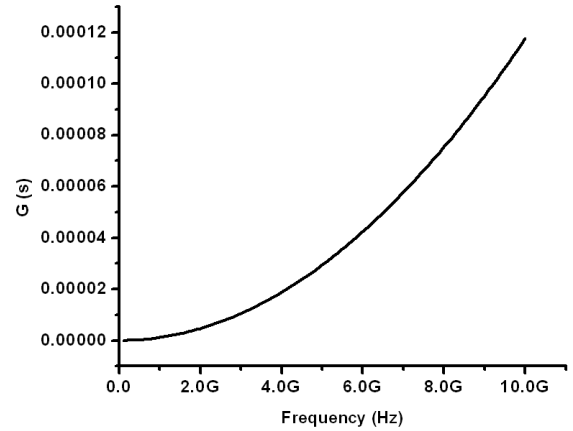
(a) Inductance



(b) Resistance



(c) Capacitance



(d) Conductance

Figure 65: Parameters of the test structure, (a) inductance, (b) resistance, (c) capacitance and (d) conductance

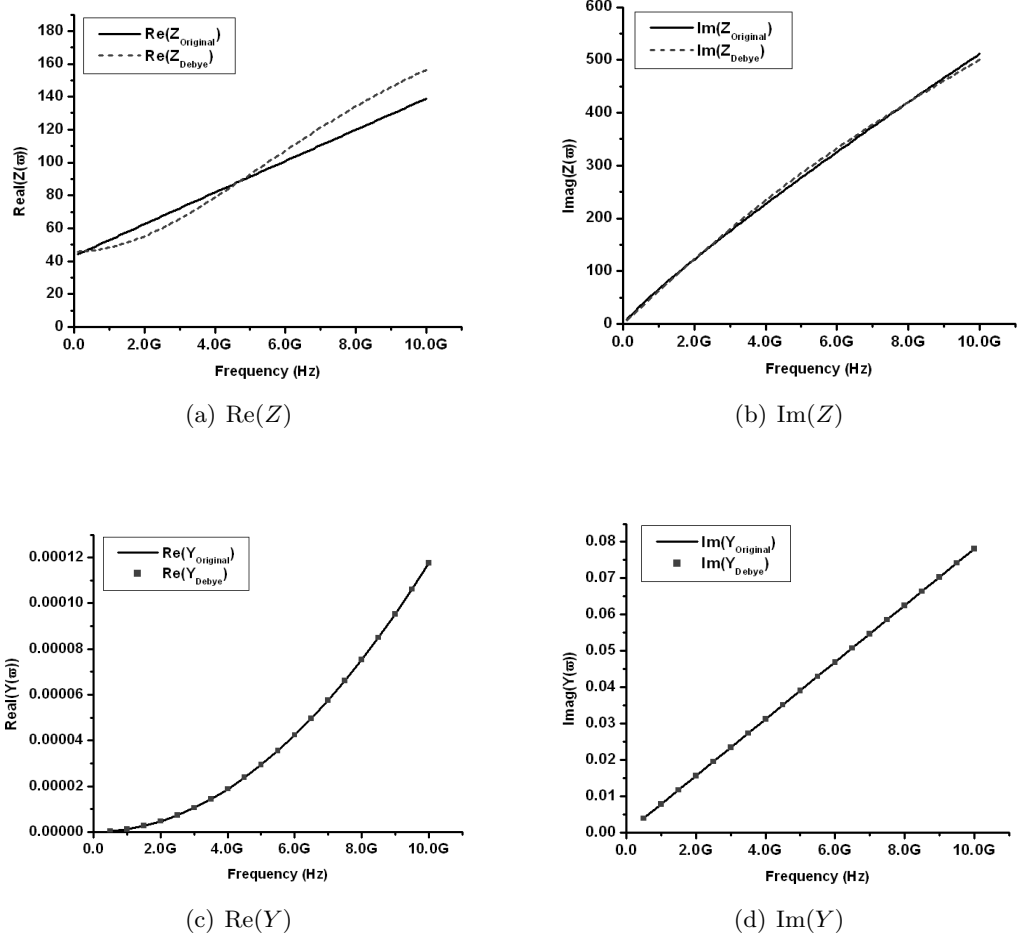


Figure 66: First order Debye approximation of frequency dependent impedance and admittance (a) $\text{Re}(Z)$, (b) $\text{Im}(Z)$, (c) $\text{Re}(Y)$, (d) $\text{Im}(Y)$

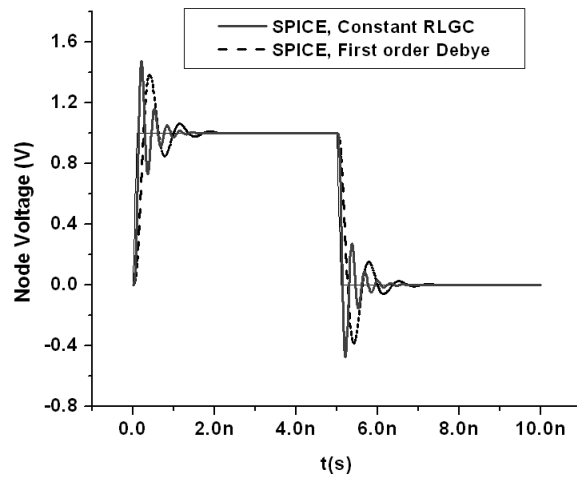


Figure 67: Comparison between constant RLGC model and first order Debye

delay and magnitude of the noise transmitted on a frequency dependent on-chip power grid. On the contrary, first order Debye circuit provides an extremely simple model to characterize the frequency dependent interconnects forming the on-chip power grid.

3.3.4 Implementation of Debye model in FDTD algorithm

The implementation of first-order Debye model in FDTD algorithm and its accuracy are discussed in this subsection. It is shown that once the first-order Debye model is extracted, it takes only a slight modification to the standard FDTD equations to incorporate this circuit model.

The updating equations for series impedance are introduced in [84], which focuses mainly on the frequency dependent R and L parameters. These equations are repeated below to provide a complete description of the problem. On the other hand, the FDTD equations for shunt admittance are derived in this section.

The set of updating equations of Debye series impedance are

$$b(k)^{n+1} = b(k)^n - \frac{\Delta t}{L_{ext}\Delta z} [v(k+1)^{n+1/2} - v(k)^{n+1/2}] \quad (3.15a)$$

$$d(k)^{n+1} = \frac{1}{AQ-1} [Q \cdot RS1 - RS2] \quad (3.15b)$$

$$m(k)^{n+1} = \frac{1}{AQ-1} [A \cdot RS2 - RS1] \quad (3.15c)$$

$$i(k)^{n+1} = b(k)^{n+1} - d(k)^{n+1} - m(k)^{n+1} \quad (3.15d)$$

where $A, Q, RS1, RS2$ are the intermediate variables:

$$A = \frac{2L_{ext}}{R_{dc}\Delta t} + 1$$

$$Q = \frac{2L_{ext}}{R_1\Delta t} + \frac{L_{ext}}{L_1} + 1$$

$$RS1 = b(k)^{n+1} + b(k)^n + [\frac{2L_{ext}}{R_{dc}\Delta t} - 1]d(k)^n - m(k)^n$$

$$RS2 = b(k)^{n+1} + b(k)^n + [\frac{2L_{ext}}{R_1\Delta t} - \frac{L_{ext}}{L_1} - 1]m(k)^n - d(k)^n$$

The corresponding updating equations of Debye shunt admittance are derived as shown

below:

$$b_s(k)^{n+1} = b_s(k)^n - \frac{\Delta t}{C_{ext}\Delta z} [i(k+1)^{n+1/2} - i(k)^{n+1/2}] \quad (3.16a)$$

$$d_s(k)^{n+1} = \frac{1}{A_s Q_s - 1} [Q_s \cdot RS1_s - RS2_s] \quad (3.16b)$$

$$m_s(k)^{n+1} = \frac{1}{A_s Q_s - 1} [A_s \cdot RS2_s - RS1_s] \quad (3.16c)$$

$$v(k)^{n+1} = b_s(k)^{n+1} - d_s(k)^{n+1} - m_s(k)^{n+1} \quad (3.16d)$$

where $A_s, Q_s, RS1_s, RS2_s$ are the intermediate variables:

$$A_s = \frac{2C_{ext}}{G_{dc}\Delta t} + 1$$

$$Q_s = \frac{2C_{ext}}{G_1\Delta t} + \frac{C_{ext}}{C_1} + 1$$

$$RS1_s = b_s(k)^{n+1} + b_s(k)^n + [\frac{2C_{ext}}{G_{dc}\Delta t} - 1]d_s(k)^n - m_s(k)^n$$

$$RS2_s = b_s(k)^{n+1} + b_s(k)^n + [\frac{2C_{ext}}{G_1\Delta t} - \frac{C_{ext}}{C_1} - 1]m_s(k)^n - d_s(k)^n$$

The Eq. (3.15) and (3.16) update the current in the branches and voltage at nodes as functions of the current and voltage values at the previous time step and circuit elements, and they are very similar to the updating equations (1.31) and (1.32) for LIM [63]. The advantage of Debye updating equations is that the frequency dependency of the interconnects are explicitly included through the parameters R_1, L_1, C_1, G_1 . The cost of this algorithm is that extra memory has to be allocated for the intermediate variables and extra floating point operations and CPU time have to be used in calculating these variables.

To check the accuracy of the above updating equations of first-order Debye model, the test circuit in the previous subsection was simulated using SPICETM and modified FDTD algorithm. Fig. 68 shows the match between the SPICETM simulation and FDTD algorithm for the same first order Debye model. The FDTD algorithm uses the updating equations in (3.15) and (3.16) and no matrix inversion is required.

3.4 *Full-chip power supply simulation*

The extraction of frequency dependent interconnect parameters and their Debye model are discussed in Section 3.2 and 3.3 respectively, which lay the foundation for full-chip power supply noise simulation. In this section, the capacitive coupling between neighboring layers

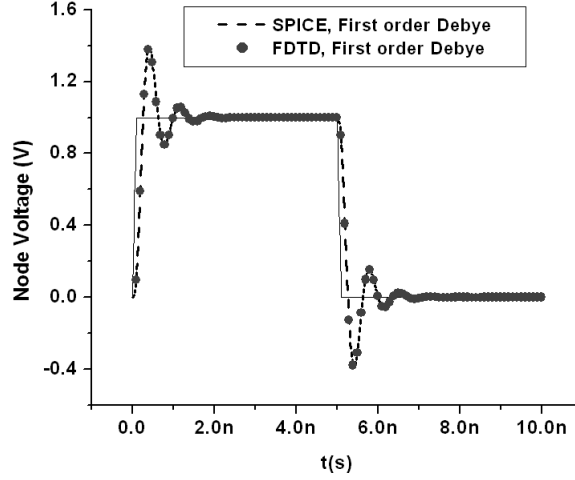


Figure 68: Correlation between SPICE and modified FDTD for first-order Debye model

due to crossover capacitor is not included in the circuit model, which has been studied in Chapter 4. The model of the on-chip power grid is composed of a large number of sub-circuits, which are serially connected at the same layer and tied to other sub-circuits at the neighboring layer through vias. Each sub-circuit represents a piece of power/ground bus whose RLGC parameters are extracted and approximated by the first order Debye circuit model using the method described in Section 3.2 and Section 3.3.3. Its schematic is shown in Fig. 69 and Fig. 70.

In each sub-circuit of the Debye model, the shunt elements are connected to the global ground node (node 0 in the SPICETM netlist), which is referenced to the plane at the bottom of a silicon substrate, as shown in Fig. 71.

The large network obtained above has been simulated using circuit FDTD algorithm with the updating equations defined in (3.15) and (3.16). After that, different aspects of the on-chip switching noise can be observed, such as its propagation pattern and time domain signature.

Fig. 72 shows the DC voltage distribution of a three-layer on-chip power grid and Fig. 73 shows the propagation pattern on the bottom metal layer. The propagation pattern is a snapshot of the voltage distribution on the bottom layer of power grid under the excitation of a group of circuits switching at the center of the chip. A dotted line has been

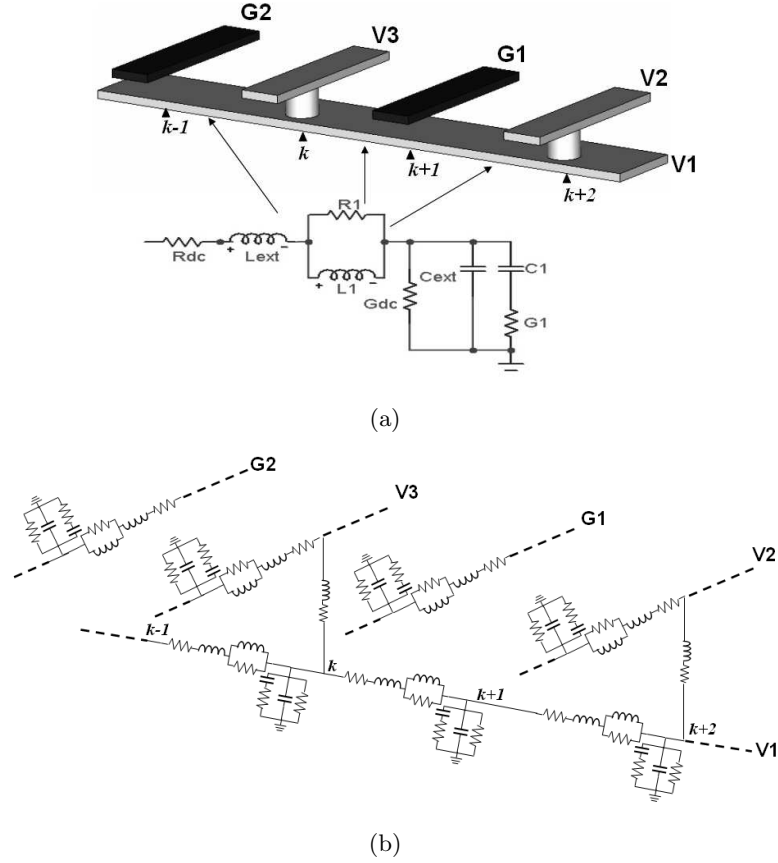


Figure 69: Power grid model (a) Debye model for each segment of the power/ground buses, and (b) the connection of M1 and M2 layers

drawn to connect the points where noise has the same magnitude (equipotential line). The corresponding concept in the electromagnetics is wavefront, which is defined as a surface on which the propagating fields have a constant phase. In a homogeneous dielectric, every point on the wavefront of the propagating fields has the same distance from the source. For instance, the wavefront forms a sphere for a point source launched in 3-D space filled with a homogeneous medium. In rectangular power planes used in PCBs and MCMs, the wavefront of switching noise has a circular shape [21]. In on-chip power grid analysis, the equipotential line denotes the positions at which noise has the same magnitude and phase. As shown in Fig. 73, the equipotential line has an elliptical shape, which can be explained as follows: The propagating noise is guided by the power buses in the homogeneous media, SiO_2 . Given the same amount of time, the noise propagates the same distance from the source, which is

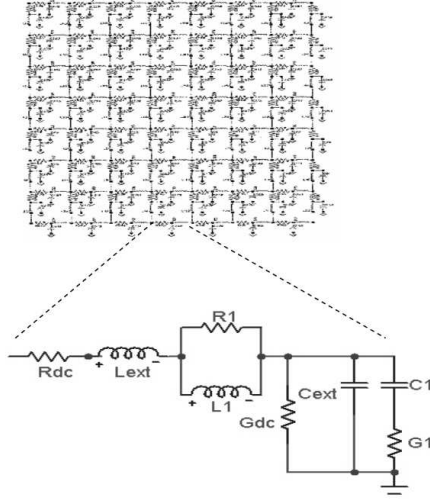


Figure 70: Full-chip power model and Debye approximation

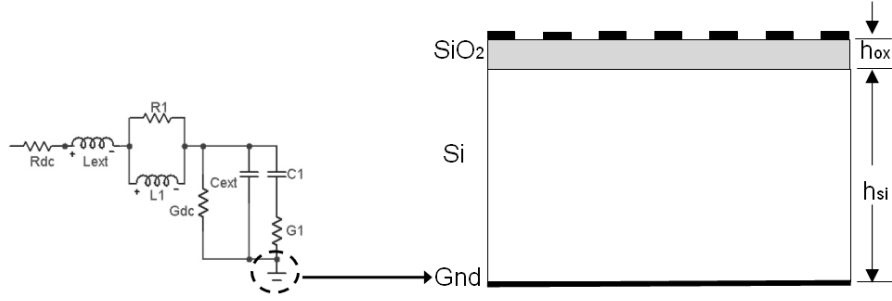


Figure 71: Ground node of an on-chip power grid

the length of the path along the power buses taken by the noise. There is noise propagating along the buses on M1 layer, and there is noise propagating to M2 layer through the via and coming back to M1 layer, as shown in Fig. 74. In Fig. 74, the length of the solid arrow is identical to the summation of the length of all dotted segments. Hence, connecting the tips of the arrows forms the equipotential line, which forms an ellipse. This diagnosis is based on the condition that switching noise is propagating only along the metal interconnections (buses and vias) and the paths of displacement current due to crossover capacitor is not included in the diagnosis. The capacitive coupling due to crossover capacitance between orthogonal buses is explored in Chapter 4.

The propagation pattern helps to observe the noise versus location at a certain time step.

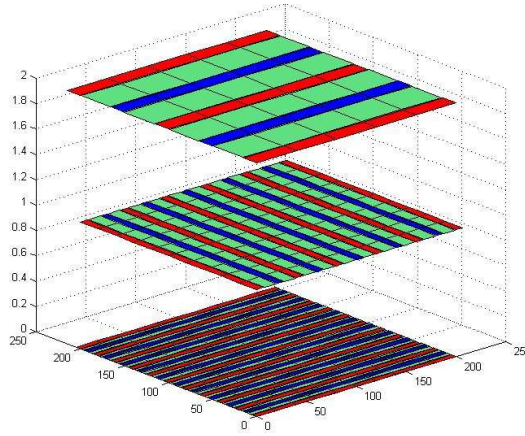


Figure 72: Steady state (DC) of on-chip power distribution

The noise signature can also be observed at a certain location as a function of time. Both are important to the on-chip power integrity analysis and diagnosis. By observing the noise signature of the power grid over substrate with different resistivity, the impact of substrate on switching noise of on-chip power distribution network is studied. As mentioned earlier, the resistivity of the substrate is defined by the foundry technology and by chip designers at the early stage of a design flow. The substrate affects the power grid in two ways. First, the substrate reduces the distribution network's DC voltage drop. Second, the voltage swing is reduced due to the conductance and the decoupling effect of parasitic capacitor between power buses and substrate. Consequently, a power distribution analysis without the substrate effect can lead to an over-designed distribution network and result in wastage of chip resources. The effect of substrate resistivity on SSN is demonstrated through a simple test vehicle, which is a $4mm \times 4mm$ chip with a three-layer power supply and the pitches of each layer are $20\mu m$, $40\mu m$, and $80\mu m$. The width of power bus is $5\mu m$ and the thickness is $1\mu m$. Switching current is modeled as a triangular current pulse with 10ps rise time, 20ps fall time and 200ps as period. The supply voltage is 1 V and the power density at the center of the chip is $300mw/(mm^2)$. Two simulations are done for the chip with the same physical setup but different substrates, namely, high resistivity with $\rho = 100\Omega\text{-}cm$ and low resistivity with $\rho = 5\Omega\text{-}cm$. The voltage of a node $1mm$ away from the chip center

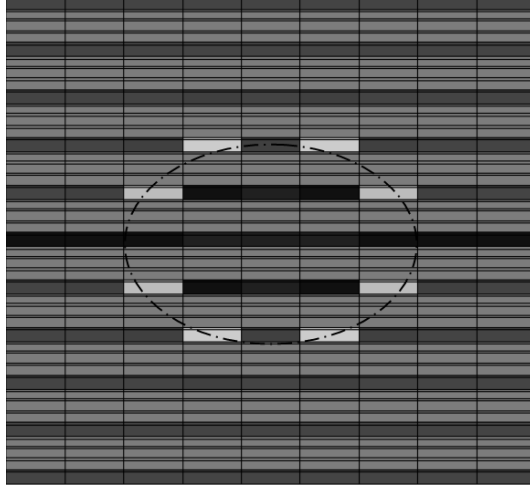


Figure 73: Elliptical pattern of the switching noise

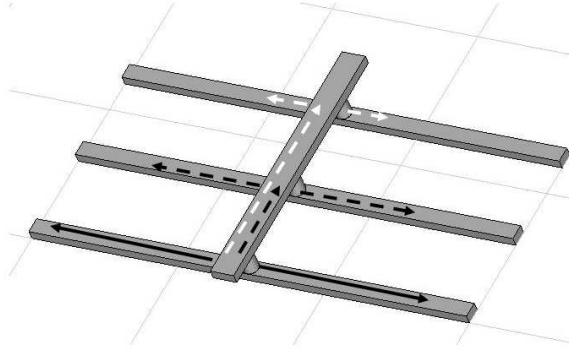


Figure 74: Physical explanation of elliptical pattern of switching noise

at the bottom layer is recorded. The waveforms of both are compared in Fig. 75. It can be clearly seen that lossy substrate helps attenuate the on-chip simultaneous switching noise by reducing the peak-to-peak value and accelerating the damping of the voltage swing.

3.5 Simulation for on-chip power grid with various power densities

In the previous section, simulation has been carried out for an on-chip power grid with the switching circuit located at the center of bottom layer, which is useful for analyzing the switching noise generated by a localized noise source. This section discusses the realistic

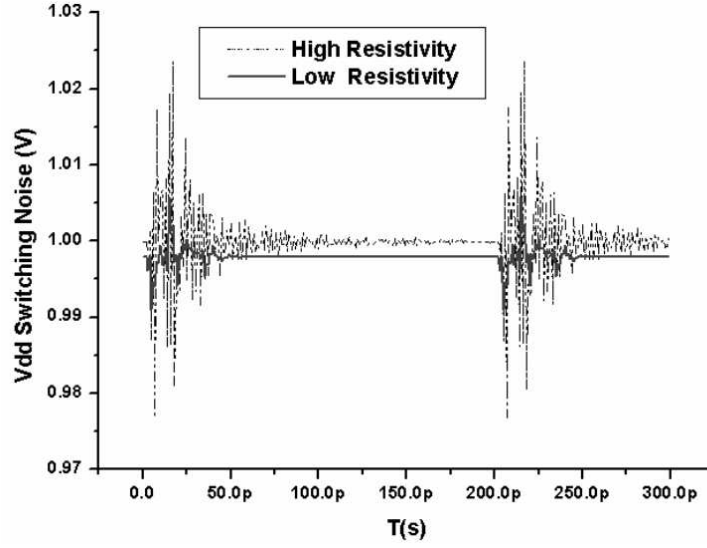


Figure 75: Switching noise on wafers with different resistivity

situation where switching circuits are distributed across the entire chip.

In the design of an IC, circuits are grouped together according to their function, such as logic, fast storage buffer (cache memory) and I/O. The logic circuits are further divided into different partitions, such as arithmetic and logical unit (ALU) and control unit as determined by computer architecture. This design results in various blocks on the layout of the IC, which consume different amount of power and draw different volume of current from the power supply. Since the switching activity is a random process, the parameter used to describe the power consumption of a block is power density $P_{density}$, which is the power requirement of a block averaged in time. Having the unit of mW/mm^2 , the power density needs to be multiplied by the area of the block A_{area} to obtain the actual power consumption. The power consumption is divided by the DC supply V_{DC} to obtain the average current drawn by the block during the switching $I_{average}$, which is given by,

$$I_{average} = \frac{P_{density} \times A_{area}}{V_{DC}} \quad (3.17)$$

The peak current I_{peak} is calculated as two times of the average current $I_{average}$ [64], which can be written as:

$$I_{peak} = 2 \times I_{average} \quad (3.18)$$

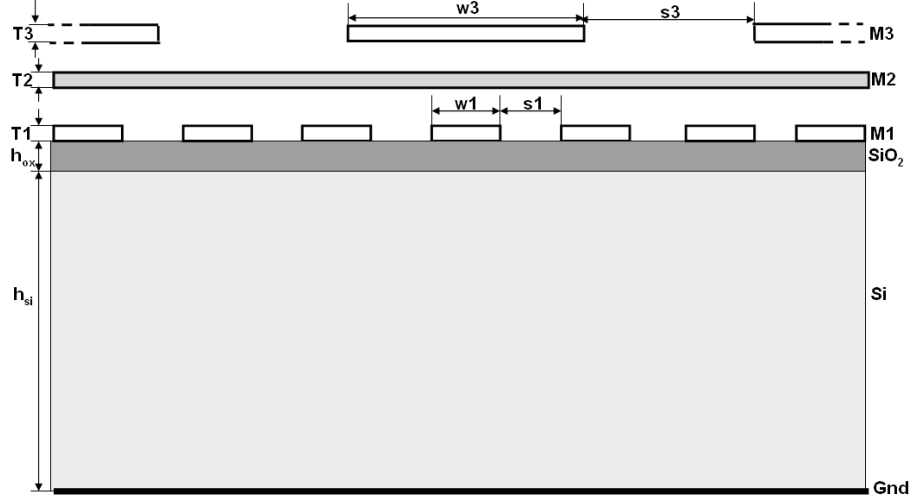


Figure 76: Cross section of three layer power grid with the following parameters: $w1 = 0.36\mu m$, $s1 = 6.72\mu m$, $T1 = 0.31\mu m$, $w2 = 2.8\mu m$, $s2 = 53.76\mu m$, $T2 = 0.31\mu m$, $w3 = 75.24\mu m$, $s3 = 806.4\mu m$, $T3 = 0.54\mu m$, $h_{ox} = 2\mu m$, $h_{si} = 500\mu m$, $\epsilon_{sio2} = 4\epsilon_0$, and $\epsilon_{si} = 11\epsilon_0$, and $\rho_{si} = 0.01 \Omega\text{-cm}$

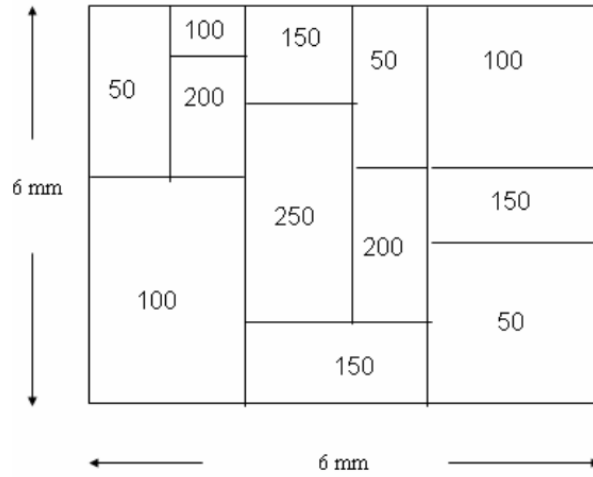
A $6\text{mm} \times 6\text{mm}$ chip with three layers of power grid as shown in Fig. 76 was simulated with different power densities. The chip was divided into twelve blocks and the power densities of the blocks had a value from 50 to 250 mW/mm^2 . The top view of the block and their power density is shown in Fig. 77. The coordinates of the bottom-left and top-right corners of each block are listed in Table 3. The DC voltage supply was 1.5V and the period of noise source was $T = 4\text{ns}$. The simulation was carried out from $t = 0\text{ns}$ to $t = 2T$ and the average voltage drop from Vdd to Gnd was calculated, which can be written as:

$$V_{average} = \frac{1}{2T} \int_0^{2T} (V_{Vdd} - V_{Gnd}) dt \quad (3.19)$$

The top view and side view of average voltage fluctuation are plotted respectively in Fig. 78 and Fig. 79 using MATLABTM. In Fig. 78 and Fig. 79, the area with blue color has the minimum voltage, which indicates that higher power density block draws more current from power supply and has more voltage drop. On the other hand, the area with red color has the maximum voltage, which indicates that lower power density block draws less current from power supply and has less voltage drop.

Table 3: Coordinates of the blocks with different power density

	Bottom-left corner		Top-right corner		Power density (mW/mm ²)
	x (mm)	y (mm)	x (mm)	y (mm)	
Area1	0	0	2	3	100
Area2	2	0	4	1	150
Area3	4	0	6	2	50
Area4	2	1	3	4	250
Area5	3	1	4	3	200
Area6	4	2	6	3	150
Area7	0	3	1	6	50
Area8	1	3	2	5	200
Area9	1	5	2	6	100
Area10	2	4	3	6	150
Area11	3	3	4	6	50
Area12	4	3	6	6	100

**Figure 77:** Chip divided in to twelve blocks with various power density (unit= mW/mm^2)

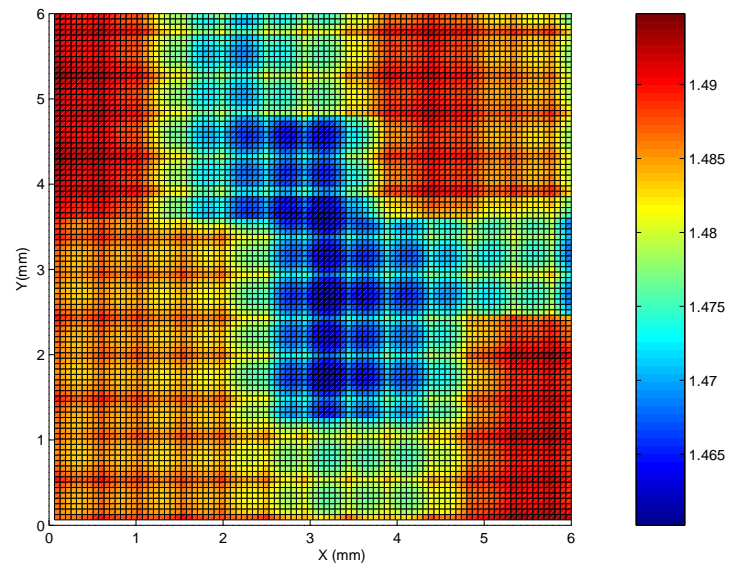


Figure 78: Top view of voltage fluctuation

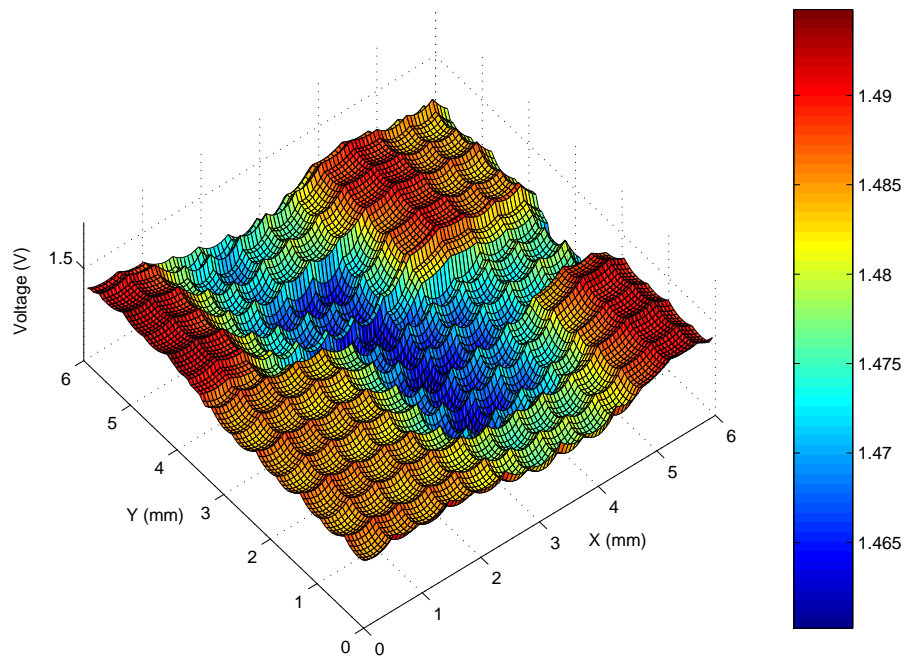


Figure 79: Side view of voltage fluctuation

3.6 Summary

This chapter discussed the modeling and simulation of on-chip power grid. First, complex image technique is applied for modeling the dispersive interconnect on lossy silicon substrate. The closed form analytical model for CPW is used together with complex image technique, which results in an accurate model which was correlated with measurement data. The similarity and dissimilarity between CPW and coplanar multi-conductor structure was studied, which enabled the analytical modeling of CMC structure. Analytical expressions for CMC structure were derived using conformal mapping technique. The procedure of extracting the frequency dependent RLGC parameters was discussed by using the combination of complex image and conformal mapping techniques.

Secondly, the Debye rational approximation was applied on the extracted RLGC parameters to simulate the frequency dependent elements in the time domain. The model of the entire chip power grid was constructed using the first order Debye approximation for each segment of the power/ground buses. The simulation of the entire network of the full-chip power grid was carried out using the modified FDTD updating equations. The on-chip simultaneous switching noise was observed as a function of location as well as a function of time. The effect of substrate loss on switching noise in on-chip power distribution network was quantified by comparing the SSN on substrates with different resistivity.

Due to the efficiency of the analytical expressions and easy implementation of the Debye updating equations, the proposed approach can easily be incorporated into CAD tools for chip and system power integrity design.

CHAPTER IV

MODELING OF MULTILAYERED ON-CHIP POWER DISTRIBUTION NETWORKS

In the previous chapter, a methodology was formulated for characterizing the regular on-chip power grid, which includes the extraction of frequency dependent RLGC parameters for periodic power buses and time domain simulation of an entire on-chip power distribution network consisting of three layers. Though the modified FDTD algorithm has universal practical applications, the application of the modeling procedure is limited by the assumption used in the development. The assumption is that the layout of power/ground buses on each layer has a uniform periodic pattern, which may not be true for a generic power grid. Besides, the mutual coupling between the buses on different layers has been ignored and thus no effects from buses on neighboring layers are included. In other words, the modeling procedure in the previous chapter is developed under ideal conditions and is limited to three layers.

In this chapter, the modeling method is improved to be of practical use for a generic on-chip power grid. As shown in Fig. 80, several topics are covered in this chapter which includes: 1) Incorporating the capacitive coupling between adjacent layers into the power grid analysis, 2) Parameter extraction of the general on-chip multi-conductor transmission lines, 3) Including the thickness of the conductor in the transmission line model, 4) Studying the effect of adjacent layers on the circuit model of on-chip power buses, 5) Studying the noise performance of irregular power grid, and 6) Generating the circuit model automatically from the layout information of an on-chip power grid.

4.1 Crossover capacitance of power buses

In Fig. 81, two buses with the same potential crossing each other are connected by a via. However, the crossover of two interconnects of opposite potential results in a capacitor,

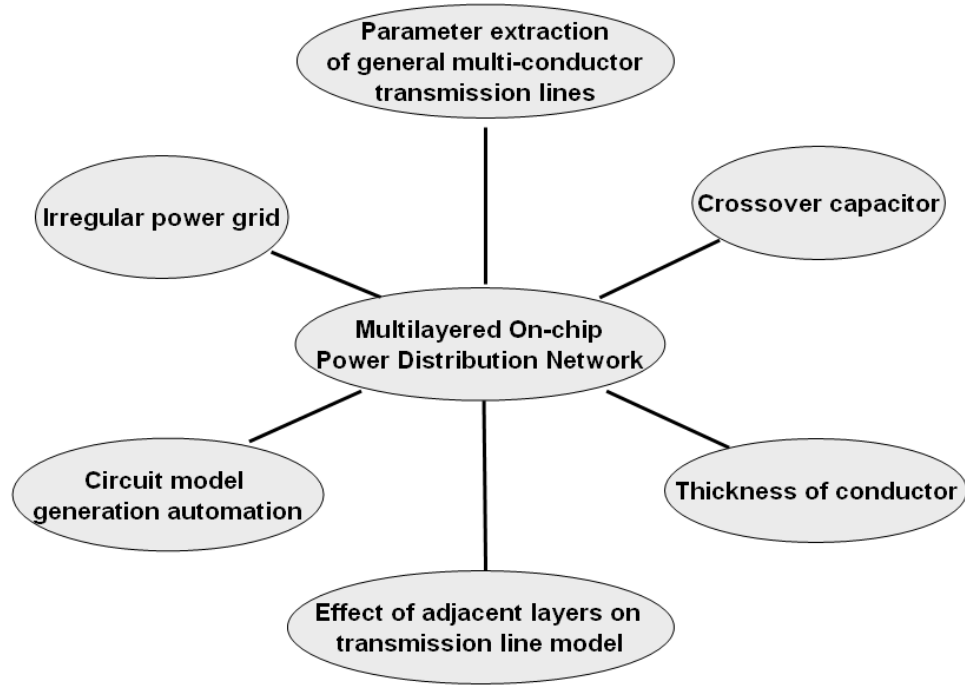


Figure 80: Various topics covered in Chapter IV

which induces coupling between neighboring layers. Various numerical methods have been used in the past to extract crossover capacitance formed by the orthogonal interconnects in a multilayered structure. These methods can be generally classified into two categories, namely, integral-equation methods and differential-equation methods. The differential-equation method, such as finite-element method (FEM) [114] and finite-difference method (FDM) [115] divide the problem space into meshes that lead to a large-size sparse matrix. The integral-equation method, such as the method of moments (MoM) [116], and the boundary-element method (BEM) [117], divide the surfaces of conductors and the interfaces of dielectric layers into meshes that lead to a relatively smaller, but full matrix. Instead of numerical methods that are often time consuming, analytical expressions of crossover capacitance are derived in this section using conformal mapping technique, which give accurate results and are more efficient.

For characterizing the crossover capacitance, two issues need to be studied first, namely, 1) the effect of neighboring interconnects on the crossover capacitance, and 2) the fringing

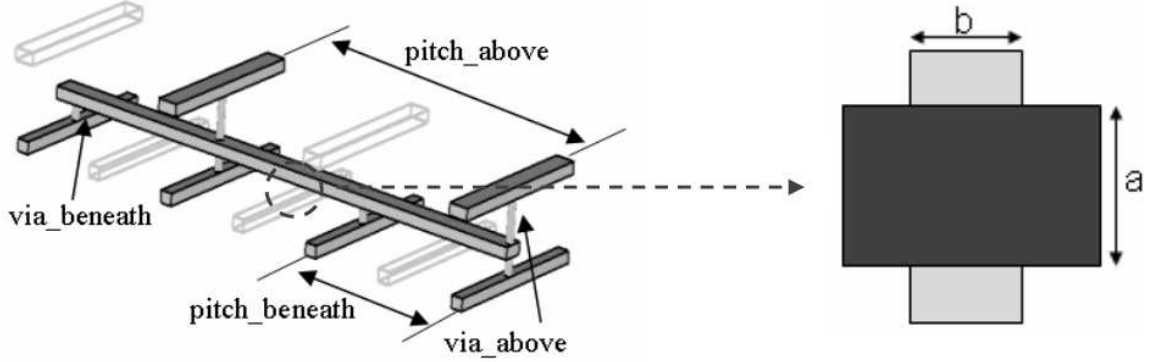


Figure 81: Crossover capacitor formed by buses with opposite potential

distance of the electric field of the crossover structure.

4.1.1 Effect of coplanar neighboring interconnects

A crossover formed by V1 and G2 and its neighboring interconnect, G1, is shown in Fig. 82. The effect of the neighboring interconnects on the crossover capacitance has been studied as a ratio of capacitances using EM Studio which is an electrostatic solver based on finite integration technique [118]. The ratio of capacitances is $C_{parallel} / (C_{parallel} + C_{crossover})$, where $C_{parallel}$ denotes the mutual capacitance between V1 and G1 and $C_{crossover}$ denotes the crossover capacitance between V1 and G2. The capacitance ratio calculated as a function of l/d is shown in Fig. 83, where l is the distance between V1 and G1 and d is the thickness of the SiO_2 between V1 and G2.

The capacitance ratio decreases rapidly as l/d increases and the value of $C_{parallel}$ is very small compared to the total capacitance for very large l/d ratio. When the distance l is ten times greater than the SiO_2 thickness, the effect of neighboring interconnects on crossover capacitance can be ignored. This approximation is used for calculating the crossover capacitance between interconnects on adjacent layers in the following sections.

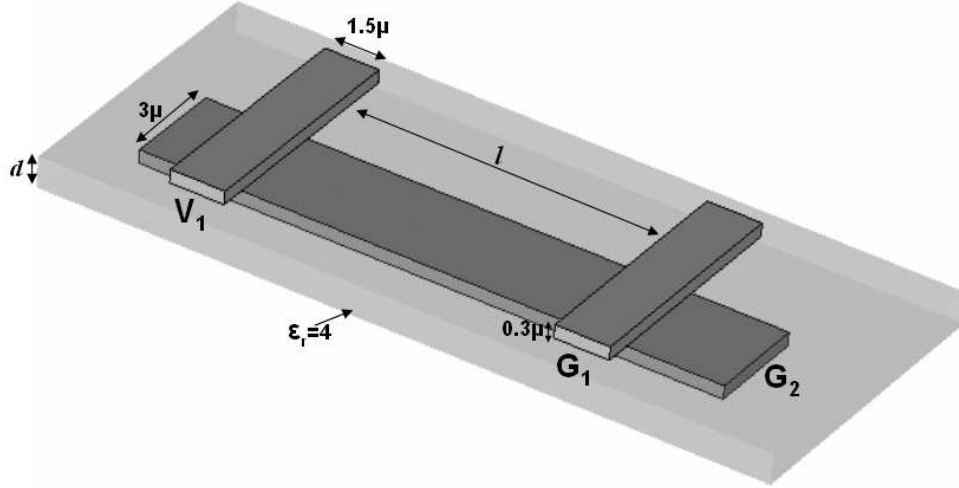


Figure 82: Effect of neighboring interconnects

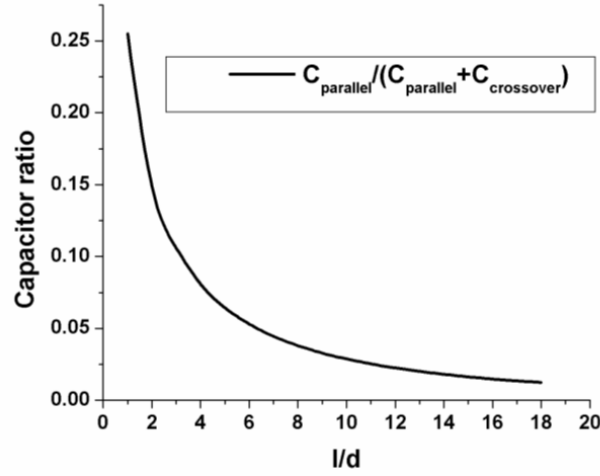
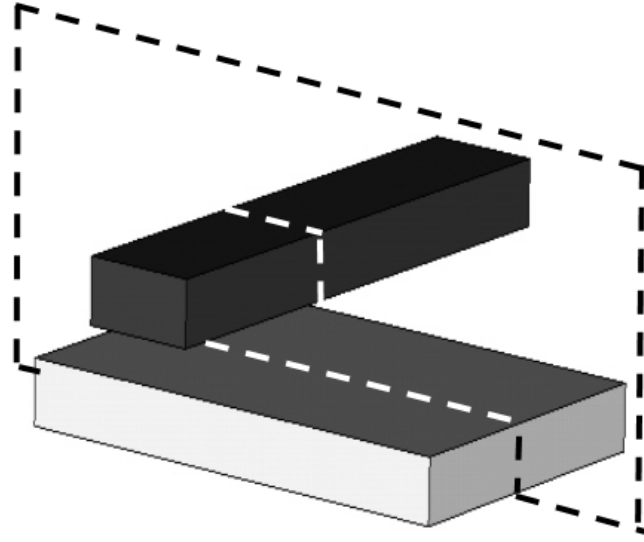


Figure 83: Capacitance ratio

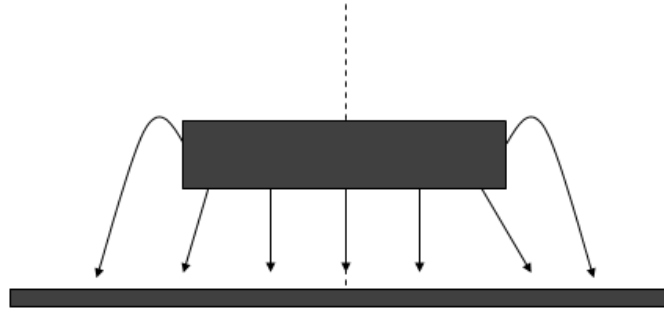
4.1.2 Fringing distance

In Fig. 82, the electric field is not confined within the cuboidal volume formed between two orthogonal strips. Instead, it extends beyond the volume due to the fringing field. To balance the accuracy and computational complexity of the problem, two interconnects need to be truncated at a finite distance away from the cuboidal volume. The distance of the fringing field or fringing distance is quantified in this section.

Fig. 84 shows a plane cutting the crossover structure and the cross section obtained consequently. Because of the symmetry of the cross section, only half of the cross section



(a)



(b)

Figure 84: Crossover structure (a) Cutting plane, (b) Cross section

and its electric field distribution at the right side are studied for determining the fringing field. The fringing distance is investigated here by studying the relationship between the magnitude of electric field intensity and the ratio x/d , where x is the distance between the point of observation and the edge of cuboid, as shown in Fig. 85.

The fringing electric field E in Fig. 85 has been calculated using FEM as well as the conformal mapping technique in this chapter, which is described in this section. Maxwell's transformation $Z = d/\pi(1 + W + e^W)$ [77] maps the complex variable $W = u + iv$ into $Z = x + iy$ as shown in Fig. 86. The line $u = K_u = \text{constant}$, is mapped to the arc as

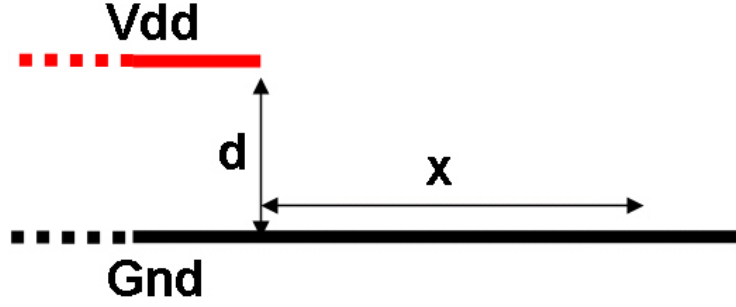


Figure 85: Fringing distance

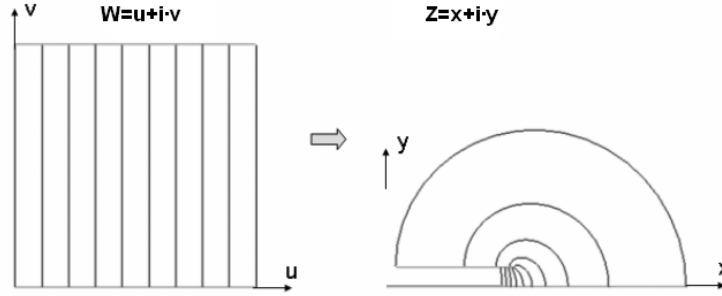


Figure 86: Maxwell's transformation

the electric field line at the edge of two parallel plates in the Z domain. Its parametric equations can be expressed as:

$$x = f(u = K_u, v) = \frac{d}{\pi}(1 + K_u + e^{K_u} \cos(v)) \quad (4.1a)$$

$$y = g(u = K_u, v) = \frac{d}{\pi}(v + e^{K_u} \sin(v)) \quad (4.1b)$$

where d is the thickness of the dielectric. Once the potential difference between two plates V is set, the magnitude of electric field intensity $|E|$ is inversely proportional to the length of the arc, according to $|V| = |E \cdot l_{arc}| = |E| |l_{arc}|$. The formula (4.2) can be used to compute the length of an arc $|l_{arc}|$ in Cartesian coordinate from the above parametric equations [121], which can be written as:

$$l_{arc} = \int_{\alpha}^{\beta} \sqrt{f'^2(v) + g'^2(v)} dv \quad (4.2)$$

The magnitude of electric field, $|E|$, normalized to the value of $|E_{x=0}|$, is plotted along

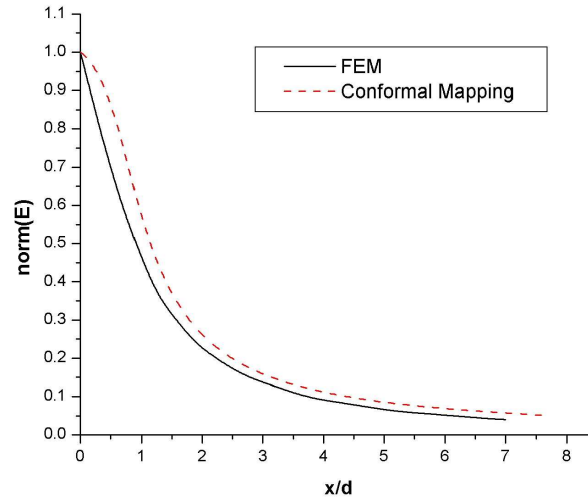


Figure 87: Correlation between FEM and conformal mapping for fringing field

the Gnd for $x \geq 0$ in Fig. 87, in which the result from conformal mapping matches well with the result from FEMLABTM. It can be observed that the electric field attenuates quickly beyond the edge of the cuboid. At a distance that is four times the SiO₂ thickness away from the edge, its magnitude is less than ten percent of the value at the origin. Since the electric energy density and corresponding capacitance is proportional to the square of $|E|$, the contribution from the field beyond the distance $4 \times d$ can be neglected. Hence, two orthogonal interconnects can be truncated at a distance of four times SiO₂ thickness d away from the overlapping area, based on which further crossover capacitance calculations can be carried out.

4.1.3 Conformal mapping for calculating crossover capacitance

After applying the fringing distance criterion and truncating the orthogonal interconnects, the crossover structure has the shape as shown in Fig. 88. The coupling capacitance can be extracted using numerical methods such as FEM [114]. However, in this subsection, analytical expressions for calculating the crossover capacitance are derived using conformal mapping, which can yield accurate capacitance and allow for physical understanding of the capacitance.

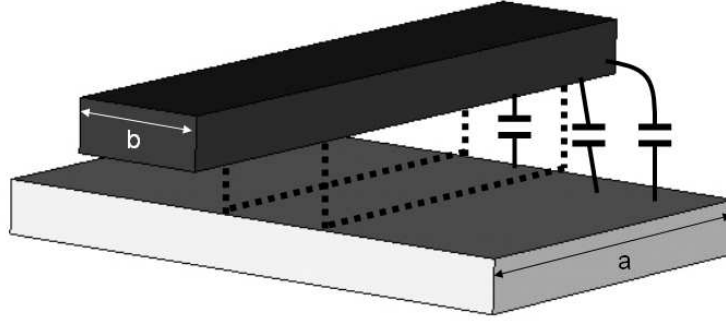


Figure 88: Crossover capacitor

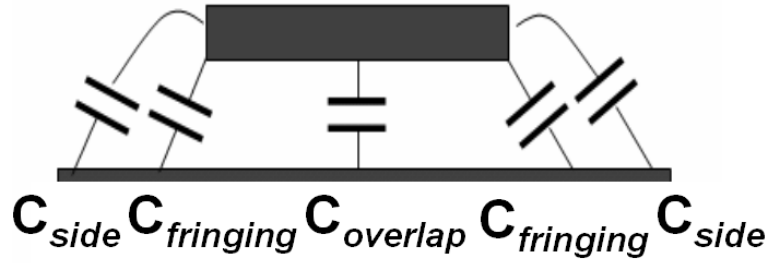
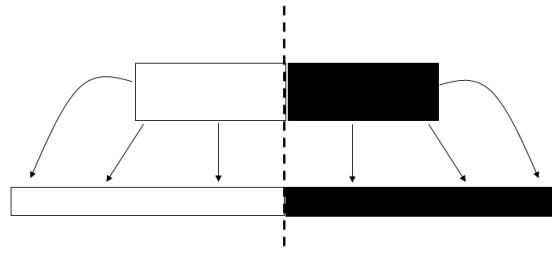


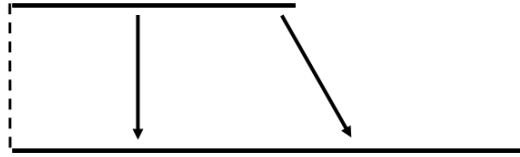
Figure 89: Schematic representation

The total crossover capacitance can be approximately divided into three major components as shown in Fig. 89. Capacitance $C_{overlap}$ stems from the field confined within the center cube and can be simply calculated as $C_{overlap} = \epsilon_{\text{siO}_2}(a \cdot b)/d$. Capacitance $C_{fringing}$ denotes the contribution from the fringing field, which is derived under the assumption that two conductors have zero thickness. The effect of the conductor thickness is considered in capacitance C_{side} .

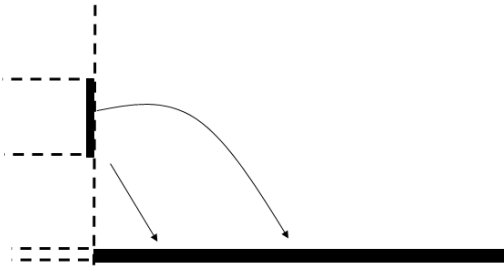
Due to symmetry, only half of the electric field needs to be evaluated after imposing the magnetic wall along the center line as shown in Fig. 90(a). Furthermore, the capacitance per unit length of the half cross section can be approximated by the summation of two capacitances, which are related to $C_{fringing}$ and C_{side} as shown in Fig. 90(b) and Fig. 90(c), respectively.



(a)



(b)



(c)

Figure 90: Capacitance decomposition (a) Symmetric field, (b) $C_{fringing}$, (c) C_{side}

The capacitance per-unit-length $C_{fringing_pul}$ is determined by going through two conformal mappings shown in Fig. 91. The expressions of this conformal mapping are given by

$$T(z) = \sin\left(\frac{\pi}{d}z\right) \quad (4.3a)$$

$$W(t) = \int_a^t \frac{dt}{\sqrt{(t-a)(t-b)(t^2-1)}} \quad (4.3b)$$

$$l_1 = \int_a^{-1} \frac{dt}{\sqrt{(t-a)(t-b)(t^2-1)}} \quad (4.3c)$$

$$l_2 = \int_{-1}^1 \frac{dt}{\sqrt{(t-a)(t-b)(t^2-1)}} \quad (4.3d)$$

$$C_{half} = \frac{\varepsilon \cdot l_1}{l_2} \quad (4.3e)$$

$$C_{fringing_pul} = C_{half} - \frac{\varepsilon \cdot w_1}{d} \quad (4.3f)$$

In Fig. 91, the variable in the Z domain is transformed to the T domain using Eq. 4.3a. The electric field inside the strip is mapped to the open space while the boundary of the strip is transformed to the real axis. The second conformal mapping transforms the variable in the T domain to the W domain using Eq. 4.3b, which closes the real axis to form a rectangle. The nodes A-B-C-D on the boundary have the values as shown in Table 4, where $a = \sin[\frac{\pi}{d}(-d/2 + i * w_1)]$, $b = \sin[\frac{\pi}{d}(d/2 + i * w_2)]$ and l_1, l_2 are calculated using (4.3c) and (4.3d).

Table 4: Nodes on the boundary for calculating $C_{fringing}$

Nodes	Z domain	T domain	W domain
A	$-d/2 + i * w_1$	a	$-l_2/2 + i * l_1$
B	$-d/2$	-1	$-l_2/2$
C	$d/2$	1	$l_2/2$
D	$d/2 + i * w_2$	b	$l_2/2 + i * l_1$

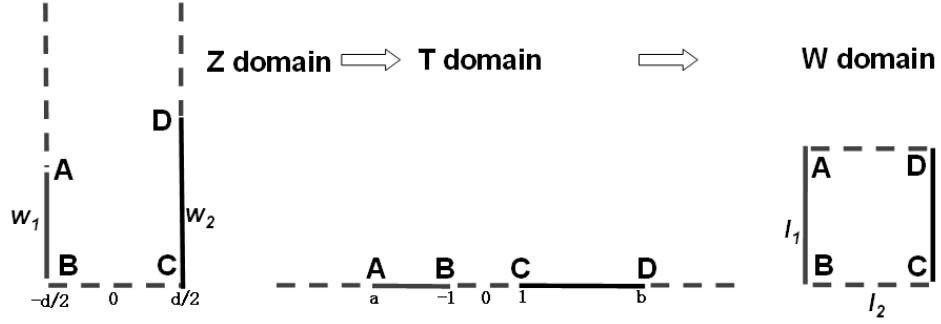


Figure 91: Conformal mapping for $C_{fringing_pul}$

The capacitance per-unit-length C_{side_pul} is determined by going through two conformal mappings shown in Fig. 92. The expressions of conformal mapping are given by

$$T(z) = z^2 \quad (4.4a)$$

$$W(t) = \int^t \frac{dt}{\sqrt{(t-A)(t-B)t(t-D)}} \quad (4.4b)$$

$$l_1 = \int_A^B \frac{dt}{\sqrt{(t-A)(t-B)t(t-D)}} \quad (4.4c)$$

$$l_2 = \int_B^0 \frac{dt}{\sqrt{(t-A)(t-B)t(t-D)}} \quad (4.4d)$$

$$C_{side_pul} = \frac{\varepsilon \cdot l_1}{l_2} \quad (4.4e)$$

Table 5: Nodes on the boundary for calculating C_{side_pul}

Nodes	Z domain	T domain	W domain
A	$i * (h + w_2)$	a	$-l_2 + i * l_1$
B	$i * h$	b	$-l_2$
C	0	0	0
D	w_1	d	$i * l_1$

In Fig. 92, the variable in the Z domain is transformed to the T domain using Eq. 4.4a. The electric field inside the first quadrant is mapped to the open space while the boundary of first quadrant is transformed to the real axis. The second conformal mapping transforms the variable in the T domain to the W domain using Eq. 4.4b, which closes the real axis to form a rectangle. The nodes A-B-C-D on the boundary have the values as shown in Table 5, where $a = [i * (h + w_2)]^2$, $b = (i * h)^2$, $d = w_1^2$ and l_1, l_2 are calculated using (4.4c) and

(4.4d).

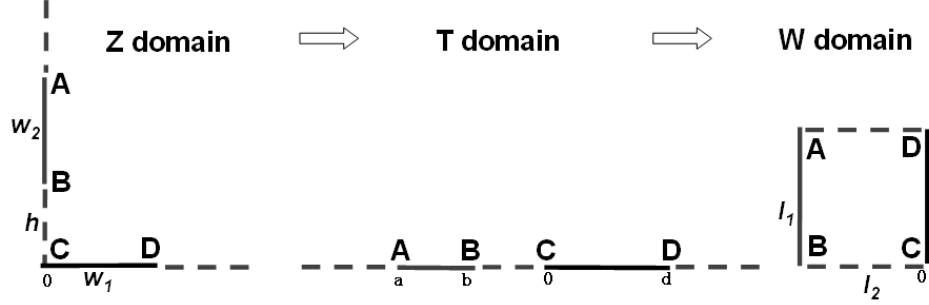


Figure 92: Conformal mapping for $C_{side-pul}$

To achieve the actual value, the values of $C_{fringing-pul}$ and $C_{side-pul}$ are doubled to account for the other half cross section and are multiplied by the width of the strip.

4.1.4 Capacitor results

To validate the accuracy of the approach proposed above, results for two crossover structures obtained by using conformal mapping are compared with those computed by using FEMLABTM, which is based on finite element method. In the examples, two conductors of thickness $0.3\mu m$ are present in a homogeneous dielectric (SiO_2) with $\epsilon_r = 4$. The dielectric distance between two interconnects is $1\mu m$ and the calculated capacitances are shown in Table 6. It can be seen that conformal mapping provides accurate capacitance for interconnects crossing each other.

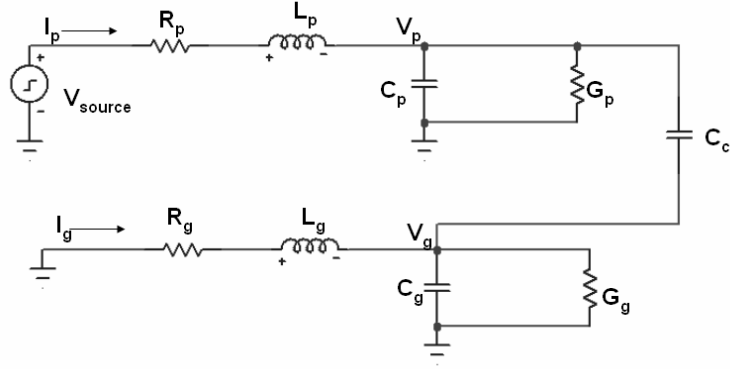
Table 6: Crossover capacitance comparison

Crossover geometry (μm)	C(fF)		Error (%)
	FEM	Conformal mapping	
a=10, b=20	10.0059	9.9312	0.75
a=5, b=15	4.6594	4.5449	2.5

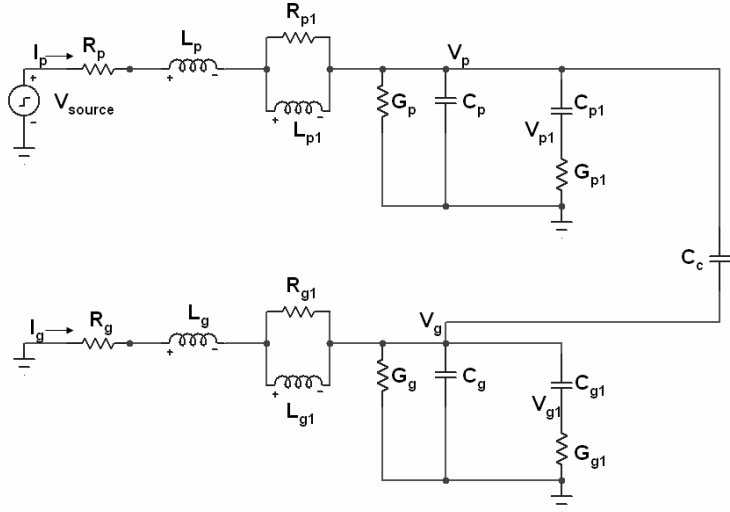
4.1.5 FDTD implementation with crossover capacitance

To include the crossover capacitor in the FDTD algorithm, the finite difference expressions are derived based on Kirchoff's current law (KCL), as described in this section.

An example of two buses – one power, one ground bus – with crossover capacitor C_c is shown in Fig. 93. The buses in Fig. 93(a) contain the frequency independent parameters, while those in Fig. 93(b) contain first order Debye model for frequency dependent parameters. Subscript p and g are used to denote the power and ground parameters, while $p1$ and $g1$ are used to denote the parameters of first order Debye model.



(a)



(b)

Figure 93: Crossover capacitor between two transmission lines (a) Frequency independent parameters, (b) First order Debye model for frequency dependent parameters

From KCL, the summation of the current at node V_p and V_g in Fig. 93(a) should be

zero, which results in

$$C_p \frac{dV_p}{dt} + G_p V_p + C_c \frac{d(V_p - V_g)}{dt} - I_p = 0 \quad (4.5a)$$

$$C_g \frac{dV_g}{dt} + G_g V_g - C_c \frac{d(V_p - V_g)}{dt} - I_g = 0 \quad (4.5b)$$

Replacing the differential operator by finite difference, the above expressions can be written as:

$$\begin{aligned} & \left\{ \frac{1}{\Delta t} \begin{bmatrix} C_p + C_c & -C_c \\ -C_c & C_g + C_c \end{bmatrix} + \begin{bmatrix} G_p & \\ & G_g \end{bmatrix} \right\} \begin{bmatrix} V_p^{n+1} \\ V_g^{n+1} \end{bmatrix} \\ &= \begin{bmatrix} I_p^n \\ I_g^n \end{bmatrix} + \frac{1}{\Delta t} \begin{bmatrix} C_p + C_c & -C_c \\ -C_c & C_g + C_c \end{bmatrix} \begin{bmatrix} V_p^n \\ V_g^n \end{bmatrix} \end{aligned} \quad (4.6)$$

In (4.6), a 2×2 matrix inversion is necessary for finding the voltage at V_p and V_g at each time step. Eq. (4.6) updates the voltage in the circuit. On the other hand, Eq. (4.7) from LIM is used for updating the current, which is given by,

$$I_p^{n+1} = I_p^n + \frac{\Delta t}{L_p} (V_{source}^{n+1/2} - V_p^{n+1/2} - R_p I_p^n) \quad (4.7a)$$

$$I_g^{n+1} = I_g^n + \frac{\Delta t}{L_g} (0 - V_g^{n+1/2} - R_g I_g^n) \quad (4.7b)$$

where Δt is the time step.

The above expressions have been tested for simulating a circuit with the following parameters: $R_p = R_g = 45.8534\Omega$, $L_p = L_g = 6.3596nH$, $G_p = G_g = 0.001S$, $C_p = C_g = 1.2pF$ and $C_c = 0.6pF$. The excitation is a voltage pulse as shown in Fig. 93 with the following parameters: $V_{peak} = 1V$, $T_{rise} = 0.1ns$, $T_{fall} = 0.1ns$ and $T_{peak} = 5ns$. The voltages at node V_p and V_g are compared with SPICETM in Fig. 94 and 95. It can be observed that (4.6) predicts the voltage on both the aggressor and victim transmission lines accurately.

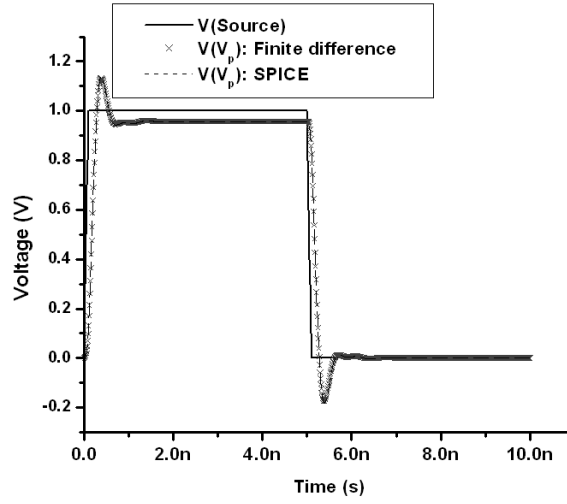


Figure 94: Voltage at node V_p

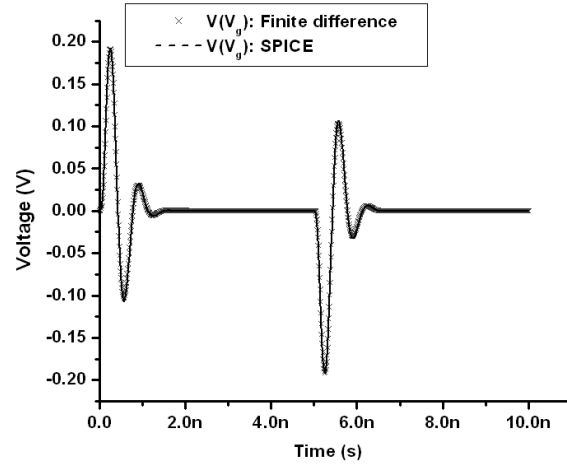


Figure 95: Voltage at node V_g

For the frequency dependent example, the same concept has been applied which results

in the following modification for updating the voltages:

$$\begin{aligned}
& \left\{ \frac{1}{\Delta t} \begin{bmatrix} C_p + C_{p1} + C_c & -C_{p1} & -C_c & \\ & -C_{p1} & C_{p1} & \\ & -C_c & & C_g + C_{g1} + C_c & -C_{g1} \\ & & & -C_{g1} & C_{g1} \end{bmatrix} + \begin{bmatrix} G_p & & & \\ & G_{p1} & & \\ & & G_g & \\ & & & G_{g1} \end{bmatrix} \right\} \begin{bmatrix} V_p^{n+1} \\ V_{p1}^{n+1} \\ V_g^{n+1} \\ V_{g1}^{n+1} \end{bmatrix} \\
&= \begin{bmatrix} I_p^n \\ I_g^n \end{bmatrix} + \frac{1}{\Delta t} \begin{bmatrix} C_p + C_{p1} + C_c & -C_{p1} & -C_c & \\ & -C_{p1} & C_{p1} & \\ & -C_c & & C_g + C_{g1} + C_c & -C_{g1} \\ & & & -C_{g1} & C_{g1} \end{bmatrix} \begin{bmatrix} V_p^n \\ V_{p1}^n \\ V_g^n \\ V_{g1}^n \end{bmatrix} \quad (4.8)
\end{aligned}$$

In (4.8), a 4×4 matrix inversion is necessary for finding the voltage at V_p , V_{p1} , V_g and V_{g1} . The expressions have been tested for simulating the circuit with the following parameters: $R_p = R_g = 45.8534\Omega$, $R_{p1} = R_{g1} = 201.5576\Omega$, $L_p = L_g = 6.3596nH$, $L_{p1} = L_{g1} = 3.5376nH$, $G_p = G_g = 10^{-6}S$, $G_{p1} = G_{g1} = 25.0254S$, $C_p = C_g = 0.37958pF$, $C_{p1} = C_{g1} = 0.86351pF$ and $C_c = 0.1pF$. The excitation is a voltage pulse with the following parameters: $V_{peak} = 1V$, $T_{rise} = 0.1ns$, $T_{fall} = 0.1ns$ and $T_{peak} = 5ns$. The voltages at node V_p and V_g are compared with SPICETM in Fig. 96 and 97, respectively. It can be seen that accurate voltages can be predicted by using (4.8) on both the aggressor and victim transmission lines containing first order Debye model for frequency dependent parameters.

4.1.6 Power grid simulation with crossover capacitance

In order to observe the effect of crossover capacitance on the SSN, a corner of a two-layer power grid was set up, which had three Vdd and two Gnd buses on the first layer and two Vdd and one Gnd bus on the second layer. The top view and cross section of the two-layer power grid are shown in Fig. 98 and Fig. 99, respectively. In Fig. 98, \otimes and \odot denote the vias connecting the Vdd buses and Gnd buses, and \triangle denotes the crossover capacitor formed by orthogonal Vdd and Gnd buses. The segment of the first layer and second layer buses has the RLGC parameters as shown in Table. 7. The core switching current I_1 and I_2 was injected into the power grid at the bottom left corner and voltage fluctuations were

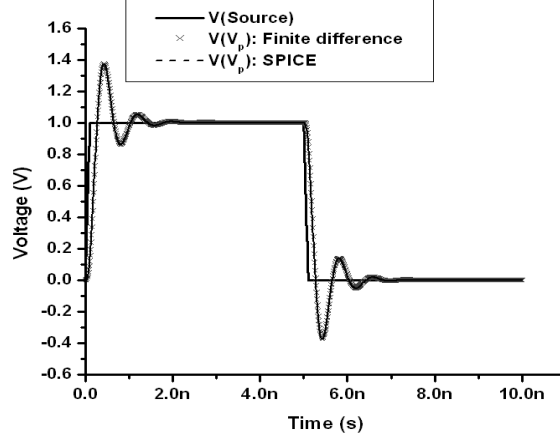


Figure 96: Voltage at node V_p

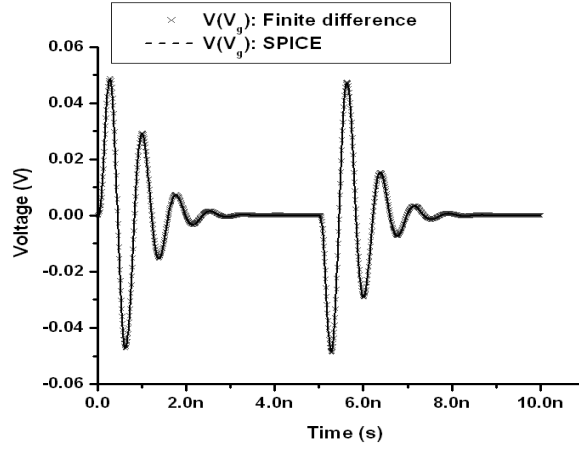


Figure 97: Voltage at node V_g

observed at two selected locations V_1 and G_1 . In Fig. 98, I_1 and I_2 are the oppositely directed currents such that $I_2 = -I_1 = I_{switching}$, where

$$I_2 = -I_1 = \begin{cases} I_{peak}(t - T_{rise}), & (0 < t \leq T_{rise}) \\ I_{peak}(T_{rise} + T_{fall} - t), & (T_{rise} < t < T_{rise} + T_{fall}) \\ 0, & (\text{otherwise}) \end{cases} \quad (4.9)$$

and $I_{peak} = 0.1mA$, $T_{rise} = 1ps$ and $T_{fall} = 2ps$.

Three simulations were carried out for the above structure with the following specifications, namely: 1) *Full-coupled*: All the crossover capacitance was included and I_1 and I_2 were both present, 2) *Uncoupled*: None of the crossover capacitance was included and I_1

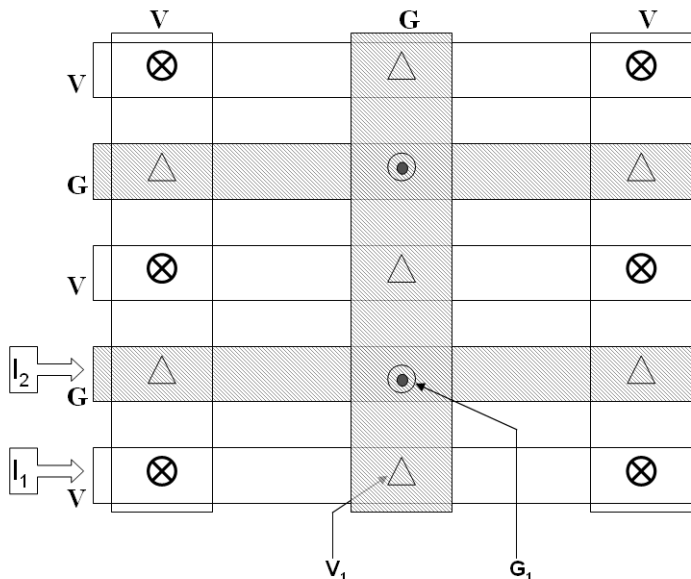


Figure 98: A corner of two-layer power grid

Table 7: Parameters of a two-layer power grid

	R (Ω)	L (pH)	C (fF)	G (mS)
First layer	0.18	11.993	2.69467	0.644456
Second layer	0.12	26	7.8262	0.015268
Crossover	\times	\times	0.17531	\times

and I_2 were both present, 3) *Vdd-coupled*: All the crossover capacitance was included but $I_2 = 0$. Though the third specification is not consistent with the actual switching activity, it was designed for observing the SSN initiated solely from Vdd buses.

The voltage fluctuation at Vdd bus V_1 for *Full-coupled* and *Uncoupled* cases are plotted in Fig. 100. The waveform of *Uncoupled* case is the voltage response due to the conducting current flowing along the Vdd buses, while the waveform of *Full-coupled* is attributed to the conducting current as well as the displacement current in the form of capacitive coupling $I_{displacement} = C_{crossover} \frac{dV}{dt}$. Since the crossover capacitances are distributed across the entire chip uniformly, the Vdd and Gnd buses are tightly coupled to each other. It is important to include crossover capacitance in the equivalent circuit of on-chip power grid to model the structure correctly and get accurate results.

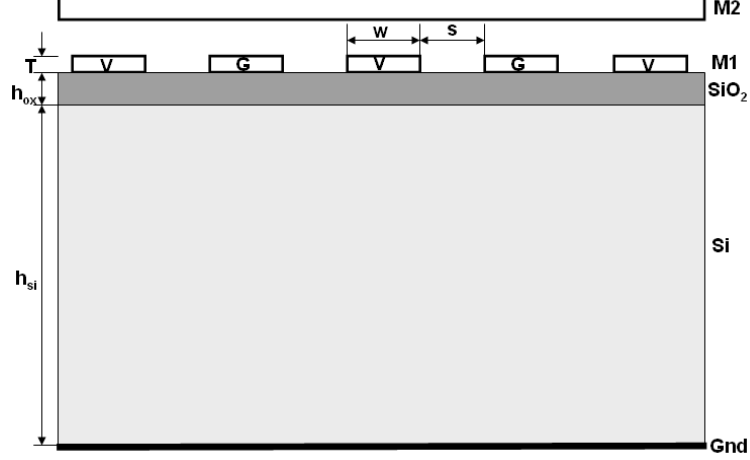


Figure 99: Cross section of two-layer power grid with the following parameters: $w = 4\mu m$, $s = 4\mu m$, $T = 0.1\mu m$, $h_{ox} = 2\mu m$, $h_{si} = 500\mu m$, $\epsilon_{siO_2} = 4$, and $\rho_{si} = 0.01 \Omega\text{-cm}$

To further demonstrate the coupling between Vdd and Gnd buses, the voltage fluctuation on node G_1 was analyzed. In the *Uncoupled* case, the noise at G_1 can be attributed solely to the noise source I_2 , since the noise on Vdd bus does not have any effect on it. On the other hand, in the *Vdd-coupled* case, the noise at G_1 can be attributed solely to the noise source I_1 through the capacitive coupling. In Fig. 101, two waveforms are shown: one is the summation of voltage fluctuation at G_1 in *Uncoupled* and *Vdd-coupled* case; the other one is the voltage fluctuation in *Full-coupled* case. Since the principle of superposition is valid in the SSN analysis for linear sources, the switching noise on Vdd/Gnd buses can be attributed to the summation of noise due to conducting current on Vdd/Gnd buses and the noise due to the coupling between Gnd/Vdd buses. From Fig. 101, it is apparent that the summation of noise on node G_1 of *Uncoupled* and *Vdd-coupled* matches that of *Full-coupled*, which satisfies the principle of superposition.

4.2 Parameter extraction for generic on-chip layout

In Chapter III, the analytical expressions were derived for a regular power grid with uniform periodic layout. On the other hand, the irregular power grid has practical applications in the chip design such as in Field Programmable Gate Arrays (FPGAs). Instead of maintaining the periodicity and uniformity, irregular layout has less restriction on the placement of

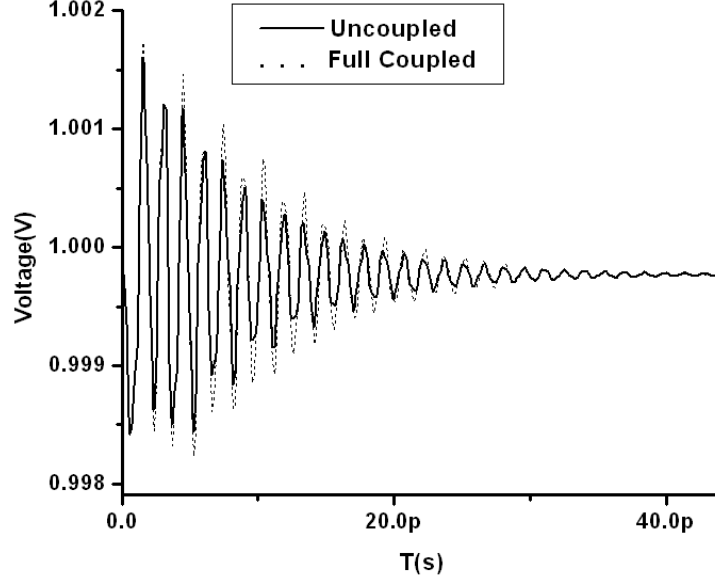


Figure 100: Comparison between switching noises on V_1

parallel conductors. It is common that power and ground buses are arranged aperiodically in a realistic IC. This section discusses the extraction of parameters of multi-conductor transmission lines with generic layout over lossy silicon substrate.

For a single transmission line over a lossy substrate, per-unit-length (pul) inductance and resistance can be obtained from the real and imaginary part of $L(w/h_{eff})$, which is a closed form expression for the inductance of a microstrip over a ground plane with the complex distance h_{eff} calculated from complex image technique. The height h_{eff} can be written as:

$$h_{eff} = h_{ox} + \frac{(1-j)}{2} \delta \tanh[(1+j)h_{si}/\sigma] \quad (4.10)$$

In [71], it has been reported that using this method, pul inductance and pul resistance extracted for a microstrip shown in Fig. 102 have good correlation with quasi-static and full-wave solution, as shown in Fig. 103. In Fig. 103, the full-wave solution is obtained by using MomentumTM, which is an electromagnetic solver for planar structures based on Method of Moment (MOM) [72].

The same analysis can be applied on multi-conductor transmission lines. The off-diagonal entries L_{ij} , which denote the mutual inductance, have been evaluated by extrapolating the formulas for partial mutual inductances of finite length conductors [109].

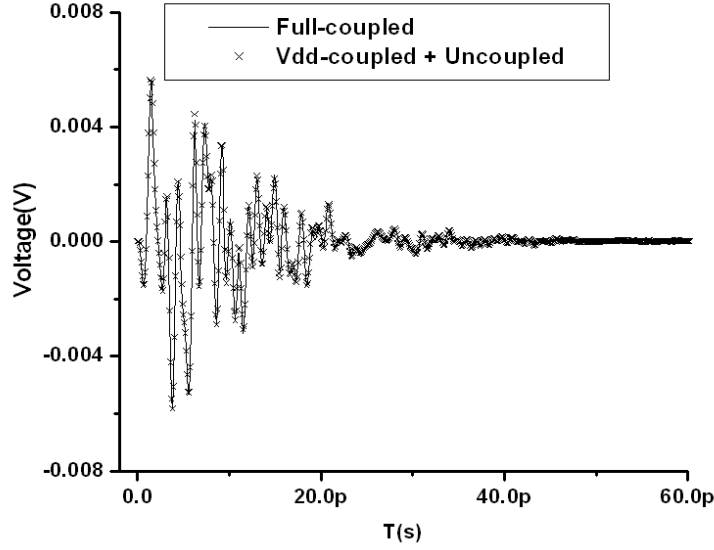


Figure 101: Comparison between switching noises on G_1

However, the pul inductance is increasing with the length of the conductor l due to a divergent term in the formula [98]. In this section, stable analytic formulae as shown in Eq. (4.11) from [110] have been used to calculate the self- and mutual inductance and resistance, which can be written as:

$$L_{ii}(h^e) = \frac{\mu}{2\pi} \ln\left(\frac{2h^e}{r_i^e} + 1\right), i = 1, 2, \dots \quad (4.11a)$$

$$L_{ij}(h^e) = \frac{\mu}{4\pi} \ln\left(\frac{(s^e + r_i^e + r_j^e)^2 + (2r_i^e + r_j^e + d^e + 2h^e)^2}{(s^e + r_i^e + r_j^e)^2 + (2r_i^e + r_j^e + d^e)^2}\right) \quad (4.11b)$$

where parameters r_i^e , r_j^e denote equivalent radius of the conductors, i and j . Parameters s^e , d^e are equivalent horizontal and vertical distance between conductors, and h^e is the equivalent height of the conductor over ground plane, as shown in Fig. 104. Their expressions are given as follows:

$$r_i^e = (W_i + T_i)/4 \quad (4.12a)$$

$$h^e = h + (T_i - W_i)/4 \quad (4.12b)$$

$$d^e = d + (T_i - W_i)/4 + (T_j - W_j)/4 \quad (4.12c)$$

$$s^e = s + (W_i - T_i)/4 + (W_j - T_j)/4 \quad (4.12d)$$

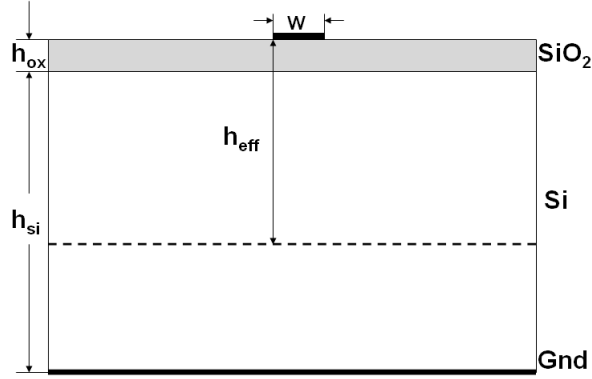


Figure 102: Microstrip on silicon substrate with $w = 4\mu m$, $h_{ox} = 2\mu m$ and $h_{si} = 500\mu m$

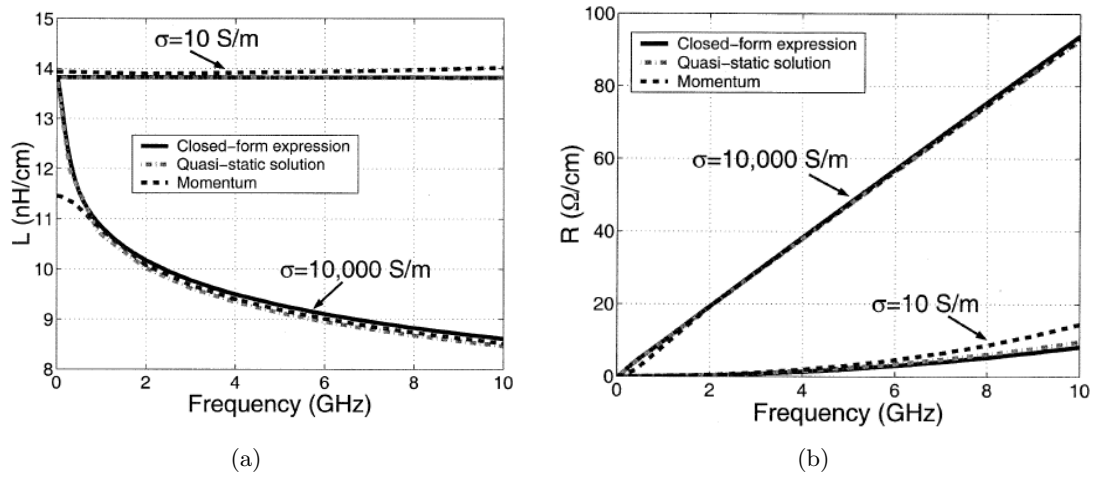


Figure 103: Frequency dependent impedance (a) inductance and (b) resistance

Since the formulae for self- and mutual inductance given in Eq. (4.11) are not functions of the conductor length l , they do not pose divergent problem by nature and thus are suitable for engineering applications. The complex inductance is readily obtainable by replacing h^e with h_{eff} given by Eq. (4.10). Afterwards, inductance and resistance can be obtained from the real and imaginary parts of $L_{ii}(h_{eff})$ and $L_{ij}(h_{eff})$.

The evaluation of the frequency dependent admittance parameters, $C(\omega)$ and $G(\omega)$, follows the asymptotic solution approach described in [71], which is based on the electric behavior of the lossy substrate and the corresponding equivalent circuit. This approach has been introduced in Section 1.3.1.3 and details are referred to [71], while some important

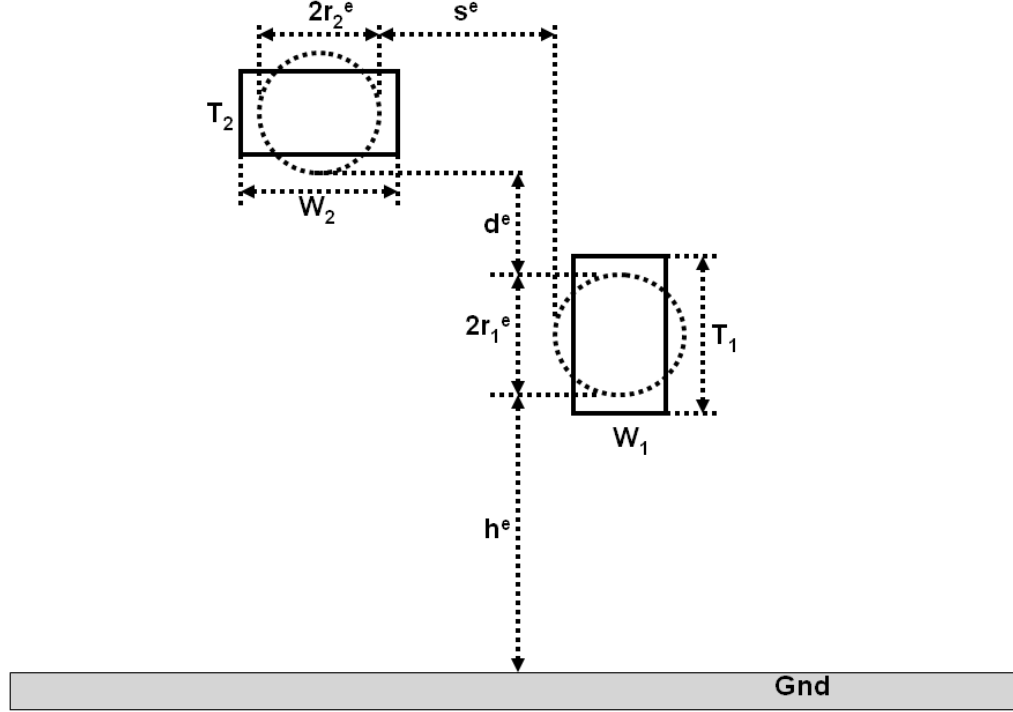


Figure 104: Coupled interconnects and definition of r^e , s^e , d^e and h^e

points are discussed below:

- For a single interconnect, $C(\omega)$ and $G(\omega)$ are functions of C_{ox} and C_{∞} , which can be determined by using analytical expressions. For example, in [71], the C_{ox} for a microstrip line was determined using analytical expressions from R. E. Collin's book [73].
- For coupled interconnects, $C(\omega)$ and $G(\omega)$ are the closed form functions of C_{ox} , C_m , C_{Si} , C_{Sim} , as shown in Fig. 105. As stated in [71], closed form expressions for the self- and mutual capacitance for coupled interconnects with general configuration may not be as readily available as for a single interconnect. As an alternative, these capacitances can be calculated using a 2-D static capacitance solver [125].

The above procedures are valid for parallel rectangular conductors and there is no restriction on the placement of adjacent conductors. The conductors can be placed aperiodically on the same layer or even be placed on different layers. In fact, these expressions are used

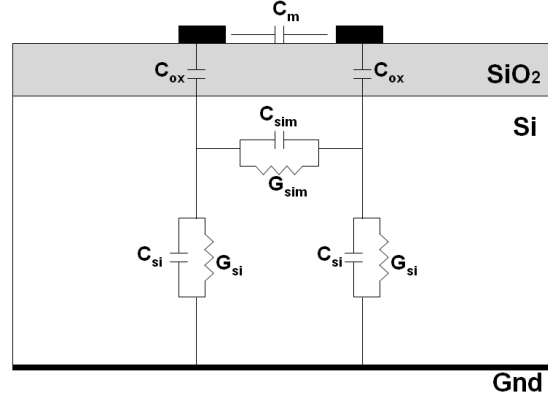


Figure 105: Equivalent circuit for coupled interconnects on silicon substrate

in Section 4.3 for studying the effect of every alternate layer below or above on the the interconnects being analyzed and in Section 4.4 for studying the effect of irregular layout. Hence it is a general solution for modeling on-chip multi-conductor interconnects. The results from these expressions are $N \times N$ RLGC matrices for a N-conductor configuration. To use these matrices in the circuit simulation, two factors have to be considered, namely, 1) acquiring the equivalent parameters from $N \times N$ matrices, and 2) including the thickness of the conductors in the model. These factors are discussed in the following two subsections, respectively.

4.2.1 Acquiring the equivalent parameters from $N \times N$ matrices

In order to reduce the complexity of the time domain simulation and capture the global effect of multi-conductor lines, the $N \times N$ matrices are reduced to 1×1 matrices. In other words, the multi-conductor traces are modeled as a single transmission line.

The schematics of equivalent loop inductance and equivalent capacitance are illustrated in Fig. 106 and Fig. 107. The detailed derivation of equivalent quantities from matrices is referred to [112] and only the expressions for a three-conductor configuration are shown in Eq. (4.13) and Eq. (4.14). It is important to note that the effect of return current in the substrate has been included in the entries L_{ii} due to h_{eff} , so that there is no term in Eq. (4.13) for that entity.

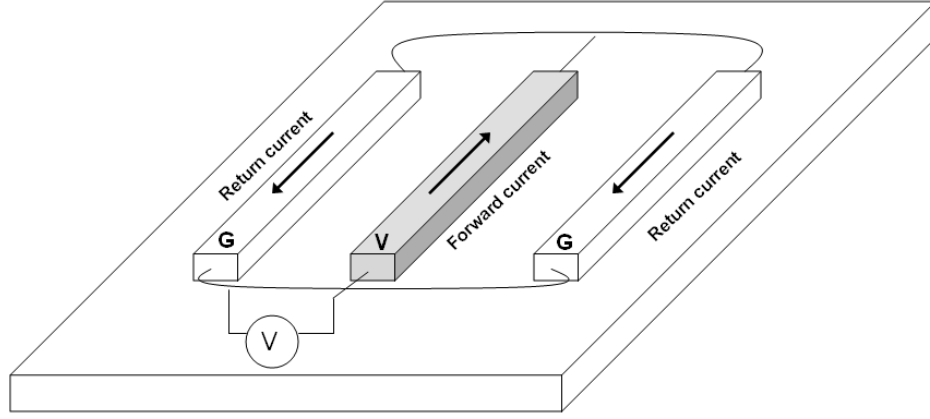


Figure 106: Equivalent loop inductance

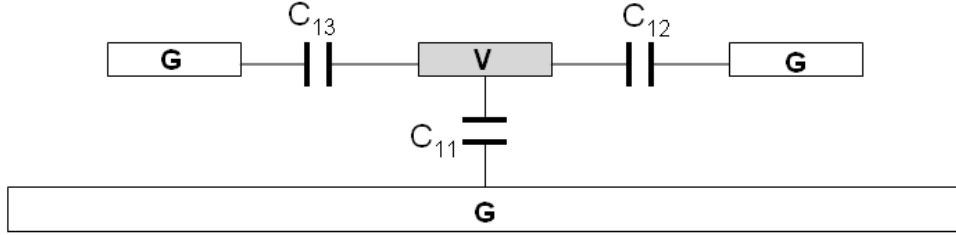


Figure 107: Equivalent capacitance

$$L_{eq} = \frac{3}{2}L_{11} - L_{12} + \frac{1}{2}L_{23} + \frac{1}{2}L_{23} - L_{13} - \frac{1}{2} \frac{(L_{11} - L_{23})(L_{12} - L_{13})^2 \varpi^2}{R_{11}^2 + (L_{11} - L_{23})^2 \varpi^2} \quad (4.13a)$$

$$R_{eq} = \frac{3}{2}R_{11} + \frac{1}{2} \frac{(L_{12} - L_{13})^2 R_{11} \varpi^2}{R_{11}^2 + (L_{11} - L_{23})^2 \varpi^2} \quad (4.13b)$$

$$C_{eq} \approx C_{11} + \sum_{k=2}^3 2C_{1k} \quad (4.14a)$$

$$G_{eq} \approx G_{11} + \sum_{k=2}^3 2G_{1k} \quad (4.14b)$$

It can be observed that if the three-conductor system is symmetric around the center conductor such that $L_{12} = L_{13}$, which holds true for regular power grids, the equivalent

inductance can be simplified by removing the term containing $(L_{12} - L_{13})^2$ given by

$$L_{eq} = L_{loop} = \frac{3}{2}L_{11} - L_{12} + \frac{1}{2}L_{23} - L_{13} \quad (4.15)$$

4.2.2 Inclusion of conductor thickness

The above expressions are derived under the assumption that the current flows only on the surface of the conductor which ignores the thickness of the conductor. In other words, the inductance model does not include the internal inductance and the resistance model does not include the DC resistance.

To find the solution of a generic power grid and improve the precision of the model, the following procedures are used to include the thickness of the conductor.

- a) DC resistance: The general expression for DC resistance is added as an augment to the equivalent resistance, given by

$$R_{DC} = \frac{l}{\sigma \cdot t \cdot w} \quad (4.16)$$

where t , w and $t \cdot w$ are the thickness, width and area of the cross section of the conductor. l is the length of the conductor, which is set as unit length for calculating the resistance per-unit-length.

- b) Internal inductance: The internal inductance is part of the total inductance which is caused by the magnetic flux in the conductor. Derived in [122], it is computed from the internal reactance as

$$L_{internal} = \frac{l}{w} \left(\mu \frac{d}{2} \right) \quad (4.17)$$

where $d = \frac{1}{\sqrt{\pi f \mu_0 \sigma}}$ is the skin depth. The internal inductance is added as an augment to the equivalent inductance.

4.2.3 Parasitic extraction result

To validate the above modeling approaches, the frequency dependent RLGC matrices of a multi-conductor structure in Fig. 108 was extracted and post-processed using Eq. (4.13) and Eq. (4.14). Lines $G1$ and $G2$ were modeled as the conductors assuming return current

for $V1$, while lines $G2$ and $G3$ were modeled as the conductors assuming return current for $V2$, so were lines $G3$ and $G4$ and $V3$. In Fig. 109, the equivalent RLGC parasitics calculated for a set of transmission lines ($G2$, $V2$, $G3$) are compared with those from electromagnetic solver MomentumTM. It can be observed that the results from the closed-form expressions of the generic layout are in good agreement with those from the full wave solver. Therefore, the analysis described provides the IC designer with choices in the design flow. For example, to design power grid with spatially regular geometry, closed-form expressions for regular periodic layout in Chapter III could be used to generate quick results. Otherwise, the expressions for a generic layout can be applied to the irregular power grid structure to generate equivalent transmission line parameters.

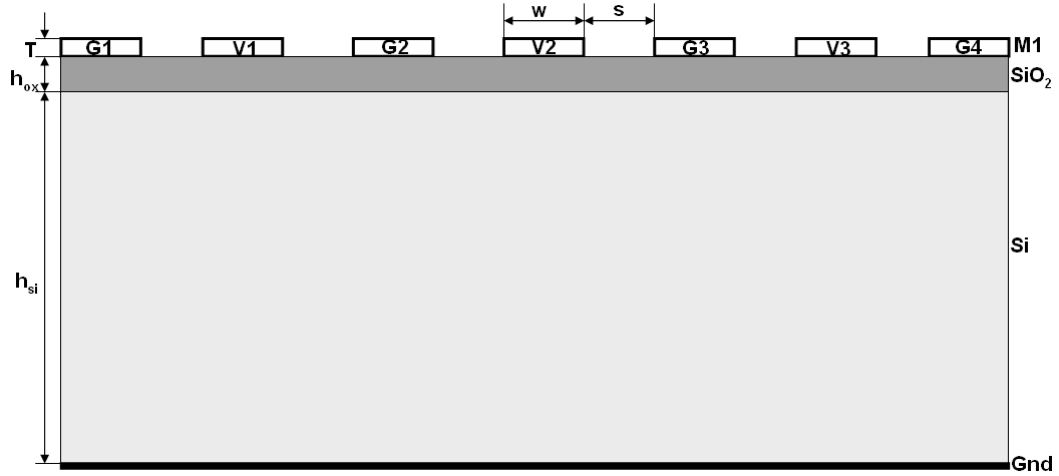
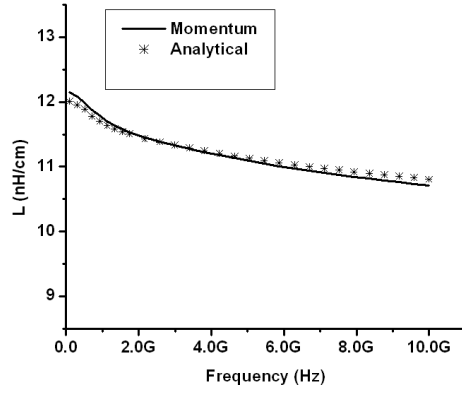
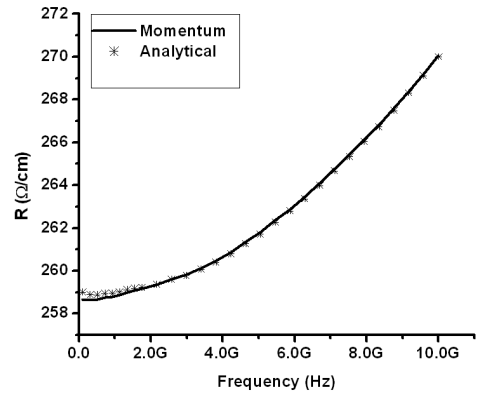


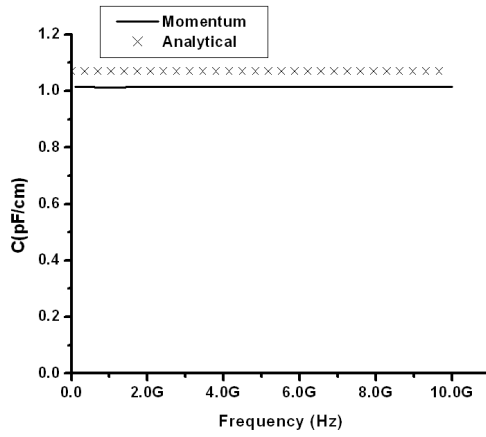
Figure 108: Power grid with the following parameters: $w = 2\mu m$, $s = 2\mu m$, $T = 0.5\mu m$, $h_{ox} = 2\mu m$, $h_{si} = 500\mu m$, $\epsilon_{sio_2} = 4$, and $\rho_{si} = 0.01 \Omega\text{-cm}$



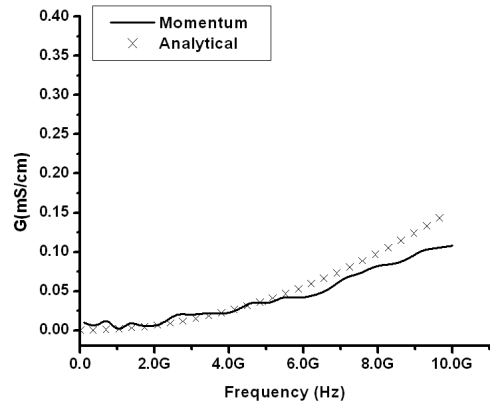
(a) Inductance



(b) Resistance



(c) Capacitance



(d) Conductance

Figure 109: Frequency dependence of line parameters of on-chip line on silicon substrate, (a) inductance, (b) resistance, (c) capacitance and (d) conductance

4.3 *Effect of adjacent layers in parasitic extraction*

The task of modeling the power grid consists of analyzing the interconnects on the same layer and the coupling between different layers as well. The inductive coupling between two neighboring layers is negligible, because orthogonal lines have no magnetic linkage and thus have zero mutual inductance. The capacitive coupling between two neighboring layers is characterized by evaluating the crossover capacitance formed by the buses with the opposite potential, for which the closed-form expressions were developed in Section 4.1. For a multilayered on-chip power grid, M_i is used to denote the i th metal layer. In this section, the effect of alternate metal layers, on either side of the multi-conductor transmission lines has been studied. First, the effect of M3 on the parasitics of the interconnects on M1 layer is discussed, and then the parasitics of buses on M3 are extracted with the M1 and M5 layers present.

4.3.1 **Effect of M3 on the parasitics of interconnects on M1**

The model obtained in Chapter III takes into account the effect of coplanar neighboring buses on M1 and silicon substrate. As an extension, the effect of M3 on the parasitics of buses on M1 is analyzed in this section. The schematics of equivalent loop inductance and equivalent capacitance for one Vdd bus surrounded by substrate and neighboring Gnd buses on M1 and M3 layers are illustrated in Fig. 110.

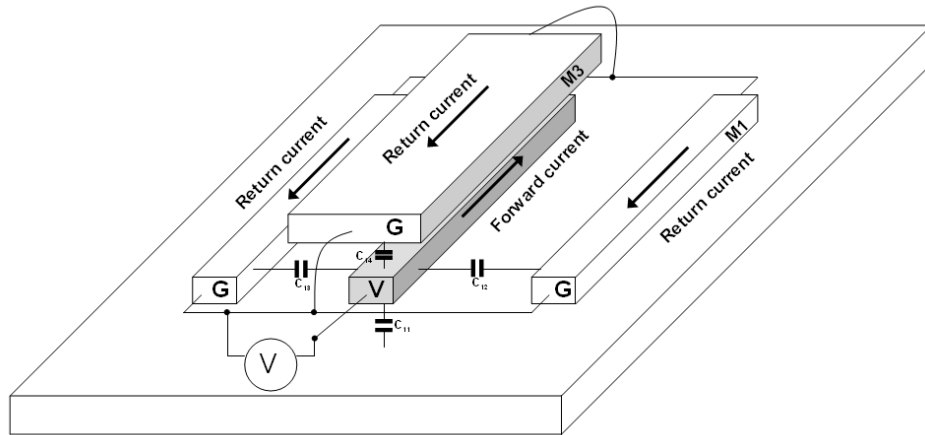


Figure 110: Equivalent/loop inductance for M1 and M3

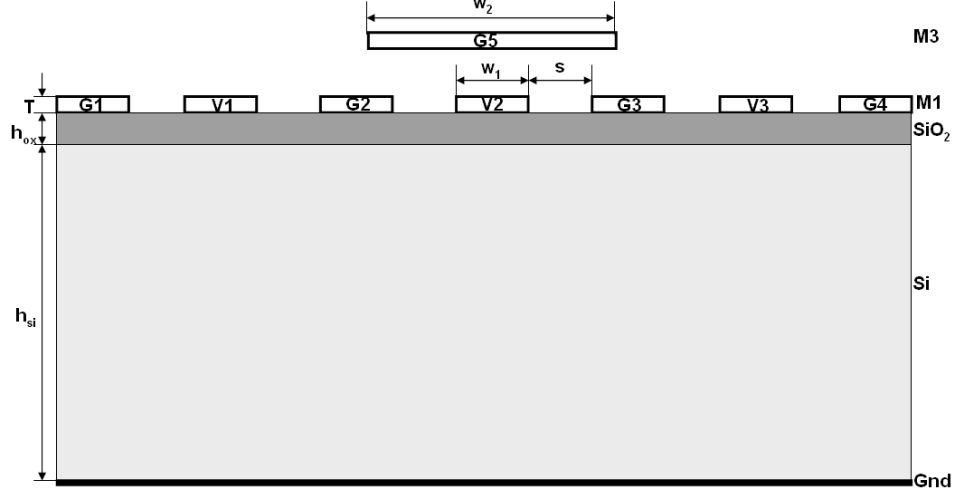


Figure 111: Power grid with the following parameters: $w_1 = 2\mu m$, $w_2 = 8\mu m$, $s = 2\mu m$, $T = 0.5\mu m$, $h_{ox} = 2\mu m$, $h_{si} = 500\mu m$, $\epsilon_{sio_2} = 4$, and $\rho_{si} = 0.01 \Omega\text{-cm}$

Using the expressions derived for the generic layout of a power grid in Section 4.2, the RLGC matrices can be calculated and further reduction can be carried out to obtain the single transmission line RLGC parameters using Eq. (4.13) and Eq. (4.14). This process has been conducted for a structure which contains buses on M1, M3 layers presented over a silicon substrate, as shown in Fig. 111. The results obtained for a set of transmission lines (G2, V2, G3, G5) are compared with the results of the structure without M3 in Fig. 112.

4.3.2 Parasitic extraction for M3 layer

The above subsection discussed the modeling procedure for buses on M1 layer by including the effect of the substrate and neighboring buses on M1 and M3 layers. The modeling procedure for buses on M2 layer assumes the same steps except that the buses on M1 and M3 layers are replaced by the buses on M2 and M4 layers. For the buses on higher layers above M2, a different modeling method is discussed in this subsection.

Silicon substrate has less effect on the parasitics of interconnects on M3 layer and above due to the following two reasons. First, as discussed in subsection 3.2.5, the substrate loss G is very small when the interconnects are far away from the silicon substrate, because eddy current in the substrate is weak. Secondly, since the buses on lower layer are densely routed, the lower layer shields higher layers from the eddy currents in the lossy substrate.

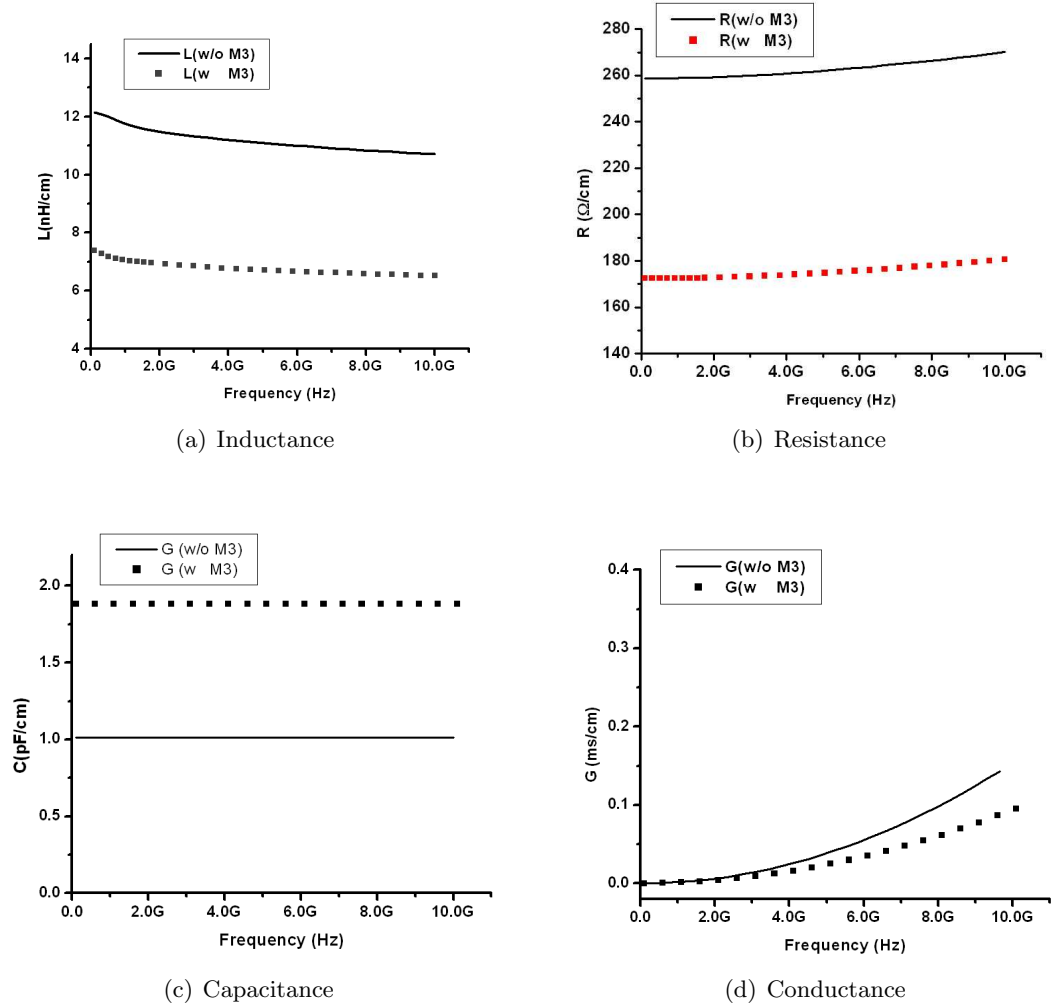
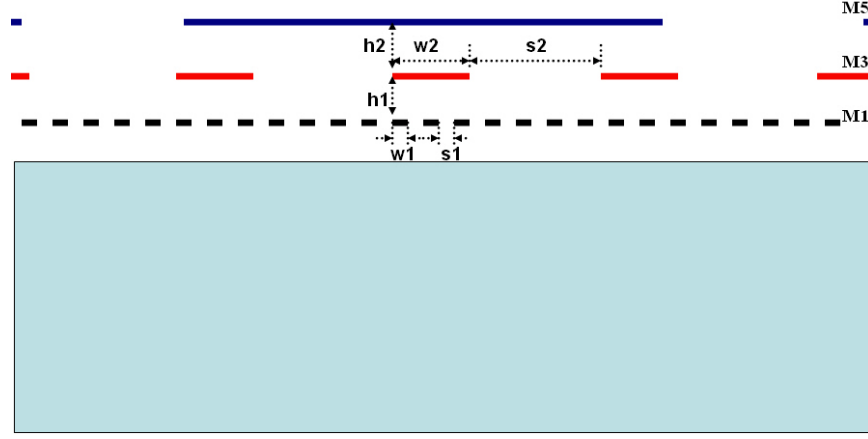
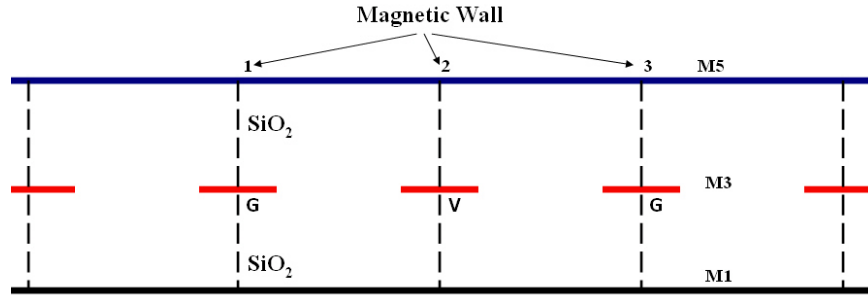


Figure 112: Comparison of RLGC parameters for M1 with and without M3 Layer, (a) inductance, (b) resistance, (c) capacitance and (d) conductance



(a) Cross section of M1, M3, M5



(b) Approximation of M1 and M5 layers using solid plane

Figure 113: Modeling M3 in the presence of M1 and M5 layers (a) Power grid with $w_1=s_1=2\mu m$, $h_1=h_2=2\mu m$, $w_2=8\mu m$, $s_2=32\mu m$, (b) Replacing M1 and M5 as solid plane

Due to this effect, a different model is used for buses on higher layers.

Consider M3 in the presence of the adjacent layers, Layers M1 and M5 function as the carrier of the return current for M3, while the orthogonal layers, M2 and M4, cannot support the return current. The pitch of M1 layer is very small and the power buses on M1 are densely distributed in the manufacturing process. At the same time, the width of buses in the higher layer, M5, usually is much larger than that of buses in the lower layer, M3. According to this analysis, a simplified model is proposed here for extracting the parameters of buses in M3 by approximating M1 and M5 as solid planes, as shown in Fig. 113.

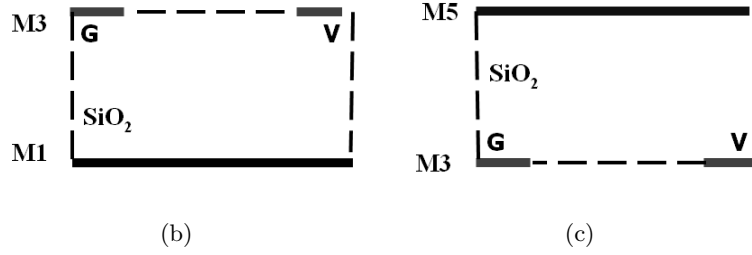
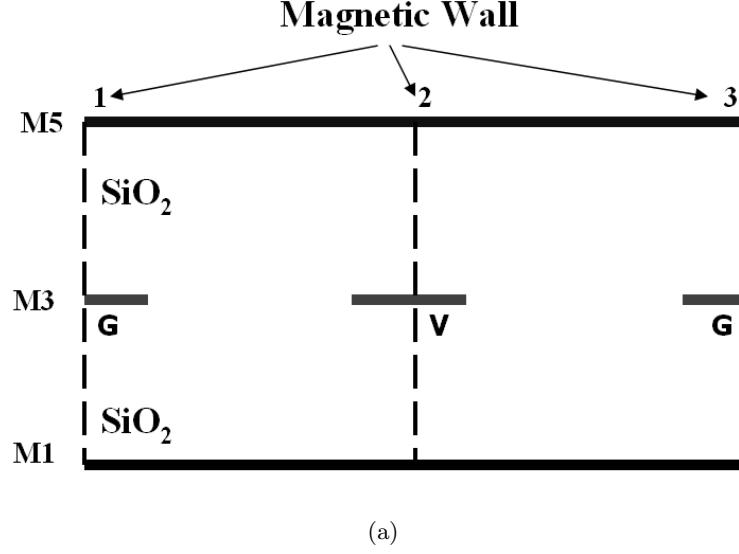


Figure 114: Three-layer structure (a) Cross section of M1, M3, M5 (b) M1 and M3 (c) M3 and M5

For buses in M3 with a regular layout, the same principle described in Section. 3.2 can be applied. Because of the symmetry of the system, the magnetic walls can be imposed at the center of each strip. The configuration of one bus is shown in Fig. 114(a), which is similar to Fig. 54 in Subsection 3.2, except for two differences: 1) In Fig. 54, the top is an open boundary, which is replaced by a perfect electric conductor (PEC) in Fig. 114(a), and 2) In Fig. 54, the dielectric has an inhomogeneous distribution of Si and SiO₂, while it is replaced by homogeneous SiO₂ in Fig. 114(a). Furthermore, the original structure can be decomposed into smaller divisions as shown in Fig. 114(b) and Fig. 114(c) using the symmetry of the field distribution. The capacitance of each division can be analyzed individually and the results can be combined together using the principle of superposition.

It is important to note that the geometries in Fig. 114(b) and Fig. 114(c) are same

but with different orientation, which have the same configuration of C_{down} as shown in Fig. 56. Therefore, the conformal mapping and its expressions derived for C_{down} can be used to calculate the line capacitance. In this section, only the conformal mapping is repeated here for convenience in Fig. 115. If the system is symmetric, in which M3 is at the center between M1 and M5, the capacitance can be calculated only once and duplicated accordingly.

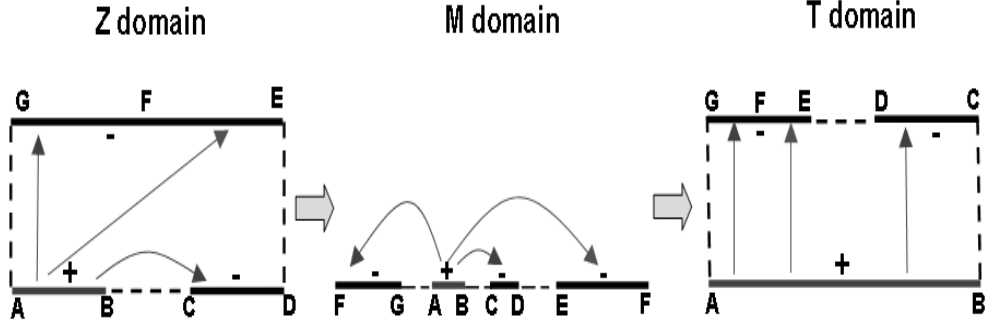


Figure 115: Conformal mapping of $C_{M1,M3}$

The validity of the solid-plane approximation has been quantified by comparing the extracted parameters with the results from FEM [113] in Table 8. The width of strips in M3 is $8 \mu m$, and the pitch of M3 is $40 \mu m$. M1 and M5 are located $4 \mu m$ away from M1. The analytical solutions are found to be within acceptable range. Since M3 is embedded in lossless dielectric SiO_2 , conductance G is negligible. With this approximation, the densely routed M1 layer is modeled as a metal screen, which virtually shields M3 from the eddy currents in the lossy substrate. In addition, the thickness of the conductor is not considered during the conformal mapping. To complete the model, the internal inductance needs to be included to take into account the sheet thickness and skin effect of the conductor, as mentioned before in Subsection 4.2.2.

Table 8: Inductance and capacitance of M3 layer

Quantity	Method		Error
	FEM	Analytical	
Inductance (nH/cm)	2.178	2.1769	0.051%
Capacitance (pF/cm)	2.018	2.0416	1.17%

4.4 Irregular power grid

Besides the regular layout, the irregular power grid also has practical applications in the design of ICs such as Field Programmable Gate Arrays (FPGAs). The irregularity of the power grid contains the variation of the following items, namely, 1) width, 2) pitch, 3) shape, and 4) alignment of the strips. The performance of the power grid are affected by different kinds of irregularity, which can be isolated and characterized individually. This section focuses on studying the effect of the aperiodic layout.

A simple case has been considered to study the effect of non-periodic buses. The buses on M1 has a layout similar to that of the example used in Section 4.3. However, the following modification was made: odd numbered power/ground buses were removed from M1 as shown in Fig. 116. For calculating equivalent loop inductance, lines $G0$ and $G1$ were modeled as the conductors supporting return current for $V1$, while lines $G1$ and $G2$ were modeled as the conductors assuming return current for $V2$. The frequency dependent RLGC matrices were extracted using Eq. (103) and post-processed by Eq. (4.13) and Eq. (4.14). The transmission line parameters obtained are plotted along with those of the regular layout in Fig. 117 [134].

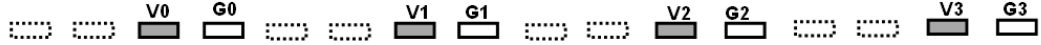


Figure 116: Irregular layout with missing Vdd and Gnd strip on M1 layer

To observe the effect of non-periodic layout in the time domain, comparison has been carried out between power grid with regular and irregular layout on M1 layer. A $4.48 \text{ mm} \times 4.48 \text{ mm}$ chip with a six-layer power supply, as shown in Fig. 118, is used to demonstrate the effect of irregular layout on the switching noise. The thickness of power bus is $0.5 \mu\text{m}$. The widths of each layer are 2, 4, 8, 16, 32 and $64 \mu\text{m}$ while the pitches of each layer are 20, 40, 80, 160, 320 and $640 \mu\text{m}$. The frequency dependent RLGC models of all the layers are listed in Table 9 and 10. Switching current at the center of the chip is modeled

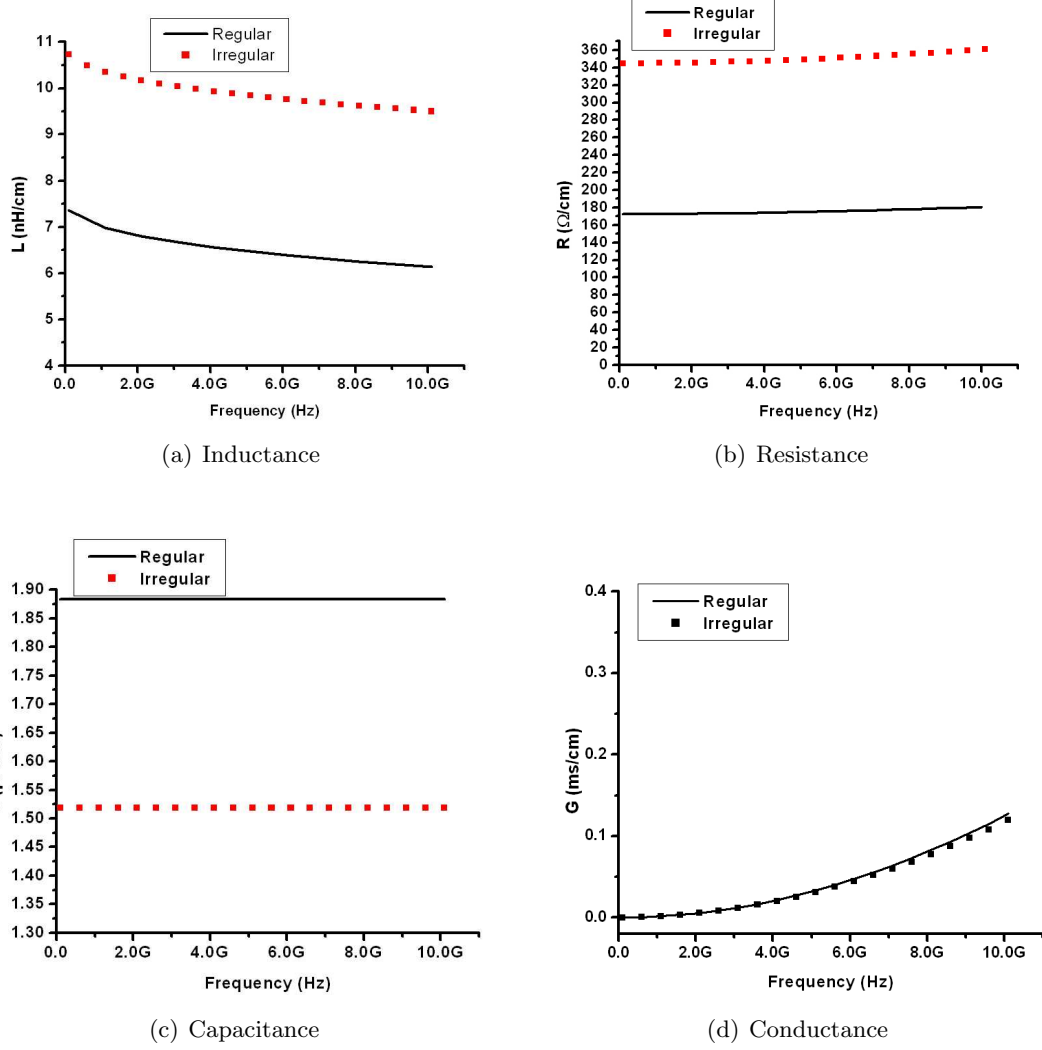


Figure 117: Parameters of regular and irregular M1 layer, (a) inductance, (b) resistance, (c) capacitance and (d) conductance

as a triangular pulse with 1ps rise time, 2ps fall time and peak magnitude of 3mA. The supply voltage is 1V. The waveform on a node 1 mm away from the switching source at the M1 layer is observed. The waveform of irregular layout is compared with the waveform of regular layout in Fig. 119. Because of the missing power/ground buses on M1 layer which induces larger loop inductance, the switching noise has a larger peak-to-peak value. Hence, more noise control and power management need to be taken for irregular power grid of non-periodic layout.

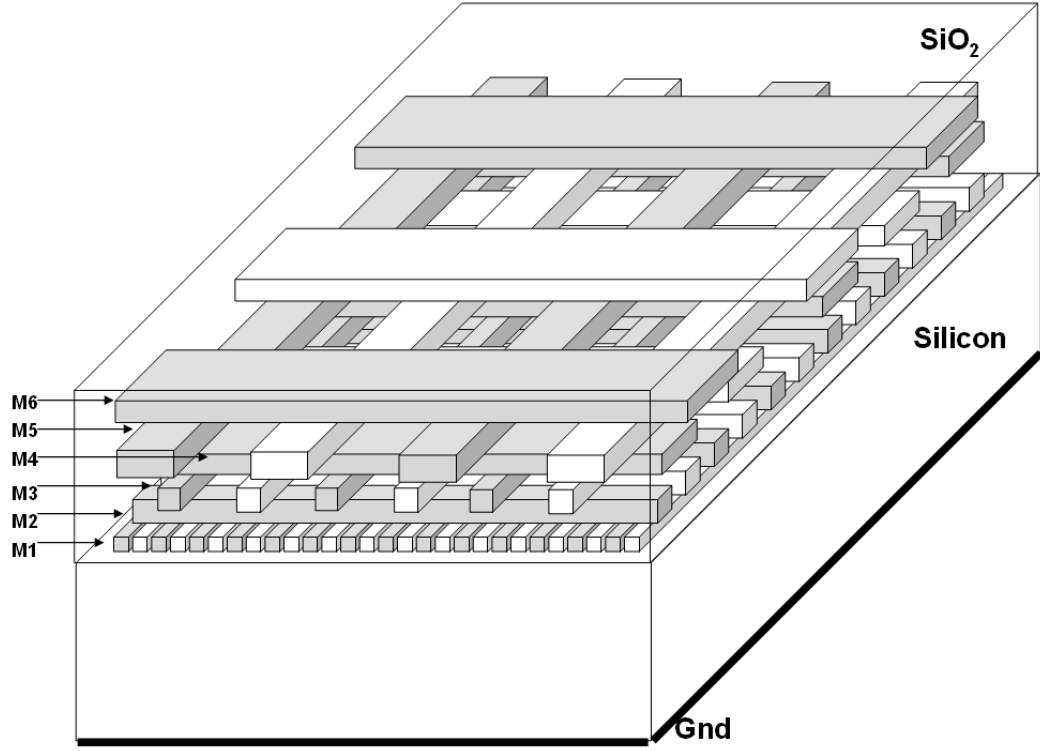


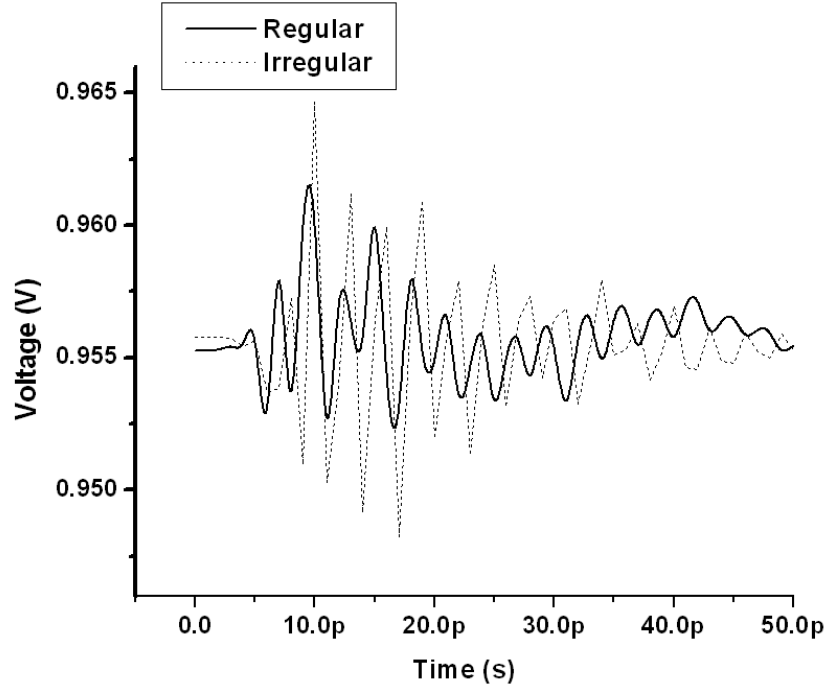
Figure 118: Side view of a six-layer power grid

Table 9: Impedance parameters of a six-layer power grid

	$R_{dc}(\Omega/m)$	$L_{ext}(H/m)$	$R_1(\Omega/m)$	$L_1(H/m)$
M1(Regular)	2.5741×10^4	6.9715×10^{-7}	1.10×10^2	1.3000×10^{-5}
M1(Irregular)	5.1928×10^4	1.0175×10^{-6}	2.219038×10^2	1.8973×10^{-5}
M2	1.3059×10^4	6.2247×10^{-7}	3.41×10^2	1.5890×10^{-5}
M3	7.2609×10^3	4.3902×10^{-7}	2.5291×10^2	1.2810×10^{-5}
M4	3.3233×10^3	3.0020×10^{-7}	4.3570×10^1	2.4271×10^{-5}
M5	1.6564×10^3	2.7514×10^{-7}	3.12600×10^1	2.3579×10^{-5}
M6	1.3174	1.8301×10^{-7}	5.387×10^{-1}	5.8249×10^{-5}

Table 10: Admittance parameters of a six-layer power grid

	$C_{ext}(F/m)$	$G_{dc}(s/m)$	$C_1(F/m)$	$G_1(s/m)$
M1(Regular)	2.47×10^{-10}	5.20×10^{-1}	8.6351×10^{-11}	1.00×10^{-1}
M1(Irregular)	2.0077×10^{-10}	5.20×10^{-1}	7.0188×10^{-11}	1.01×10^{-1}
M2	$1.9916474 \times 10^{-10}$	8.033×10^{-1}	7.2434×10^{-11}	2.56×10^{-1}
M3	$2.1763371 \times 10^{-10}$	1.1497279×10^{-4}	3.4328×10^{-11}	3.3589×10^{-5}
M4	$4.2339151 \times 10^{-10}$	1.040208×10^{-4}	7.0695×10^{-11}	4.2313×10^{-6}
M5	$4.0638975 \times 10^{-10}$	1.0604936×10^{-4}	6.6893×10^{-11}	2.8125×10^{-6}
M6	$8.0890936 \times 10^{-10}$	3.3568409×10^{-4}	4.7895×10^{-11}	1.3675×10^{-6}

**Figure 119:** Time domain waveform of regular and irregular power grid

4.5 *Model generation and automation*

In order to reduce the time for building the equivalent circuit for entire on-chip power grid, which is time consuming for organizing millions of nodes and elements manually, a software program was developed in C++ language to generate the power grid model automatically. The program takes the following data as input: 1) size of the chip, 2) number of power grid layers, 3) permittivity of the SiO₂, 4) pitch, width, thickness, sheet resistance and conductivity of each power layer. The output of the program contains two types of text files which are either compatible with SPICE syntax or readable by parameter extraction tools.

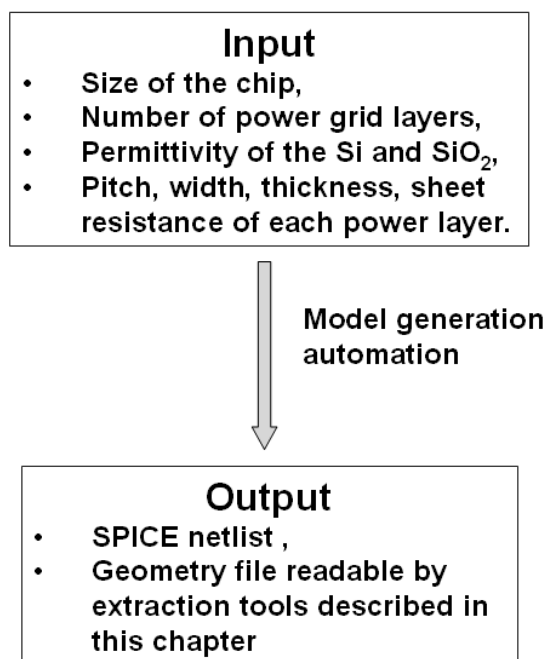


Figure 120: Model generation automation for on-chip power grid analysis

Some terms are defined here to ease further discussions:

1. “via_beneath” and “via_above”: via used to connect current layer to the layer beneath and above it, respectively,
2. “pitch_beneath” and “pitch_above”: distance between two via_beneaths and two via_aboves,

which is the pitch of the layer beneath and above the current layer,

3. “pitch_current”: pitch of current layer,
4. “chip_size”: the length of the chip edge, assuming the chip has a square shape.

Each Vdd/Gnd metal bus can be split into several sections, each of which has the length of “pitch_above”. One section can be divided into several segments, each of which has the length of “pitch_beneath”. The side view and top view of a piece of power grid are shown in Fig. 121 and Fig. 122 to illustrate these terminologies, while graphical representation of the sections and segments is shown in Fig. 123.

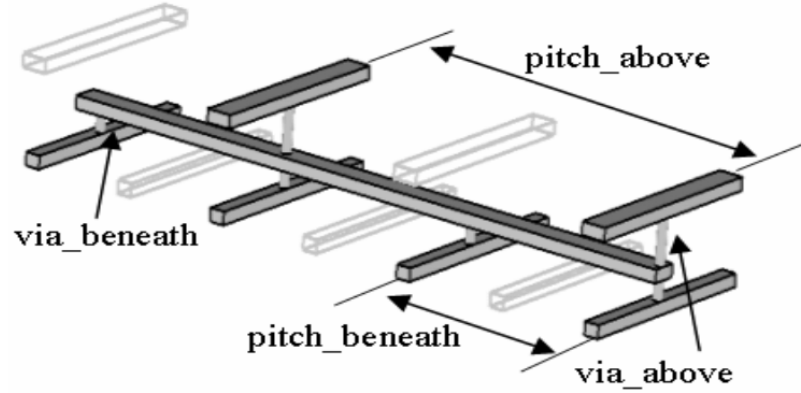


Figure 121: On-chip power bus connections

The feature of on-chip power grid leads to the following procedure for constructing circuit models as follows:

1. At each layer, the number of Vdd/Gnd buses is determined by $\text{chip_size}/\text{pitch_current}$.
2. The number of sections along each bus is determined by $\text{chip_size}/\text{pitch_above}$.
3. The number of segments within every section is determined by $\text{pitch_above}/\text{pitch_beneath}$.
4. Via_beneath and via_above are distributed along Vdd/Gnd buses with the period of pitch_beneath and pitch_above, respectively.

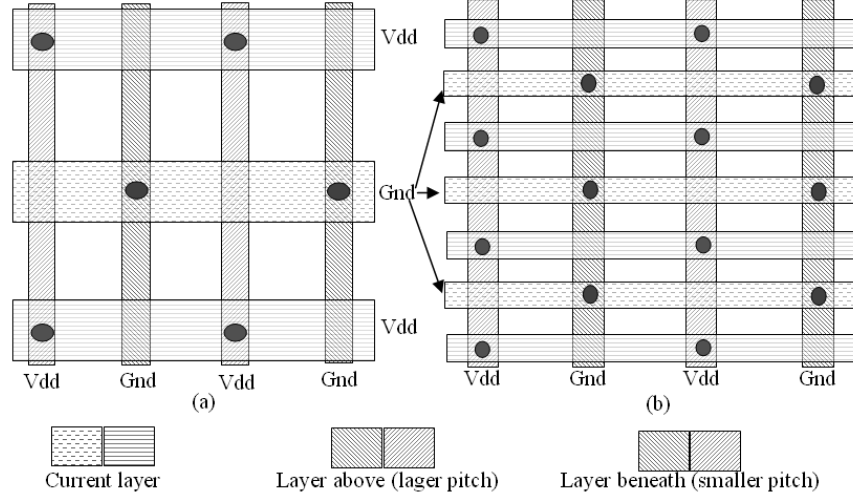


Figure 122: Two layers of power grid (a) current layer and layer above, (b) current layer and layer beneath

5. The top layer uses `pitch_current` as “pitch_above” and the bottom layer uses the `pitch_current` as “pitch_below”.

The program developed significantly reduces the time for building large size equivalent circuits from the layout, based on which simulations can be quickly carried out for power grid with different geometries and dielectrics.

4.6 Summary

This chapter discusses the modeling and simulation of generic on-chip power distribution networks. Firstly, the capacitive coupling between adjacent layers of on-chip power grid is captured by incorporating the crossover capacitance into circuit based FDTD algorithm. The crossover capacitance is evaluated using analytical model derived using conformal mapping technique. Secondly, the analytical model is used to extract parameters of on-chip multi-conductor transmission lines, which guarantees the stability and is applicable to general distribution of multi-conductor transmission lines. The obtained data from the analytical model are $N \times N$ matrices, which are reduced to RLGC parameters of a single transmission line. The effect of the thickness of the conductor is included as an augment to the RLGC parameters. Afterwards, the effect of alternate layers on the model of on-chip

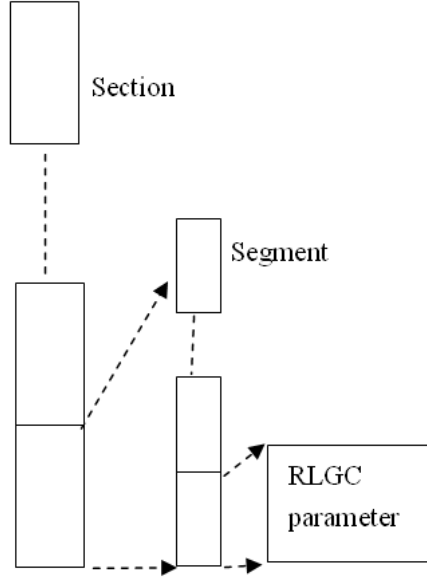


Figure 123: Section and segment of on-chip power bus

buses is investigated and the noise performance of irregular power grid was studied. Finally, computer aided model generation was discussed, which constructs the power grid model for an entire chip from the layout automatically.

The research done in this chapter explores different aspects of the on-chip power grid modeling and simulation. A solution has been provided to construct models for a generic on-chip power grid, which takes into account the mutual coupling, thickness of the conductor and basic irregularity of the power grid. The solution contains the closed form expressions whose accuracy has been verified. An algorithm was developed to construct the model for an entire chip automatically. Thus, the proposed approach can be readily incorporated into computer-aided-design or electronic-design-automation tools for chip power integrity design and diagnosis.

CHAPTER V

PRELIMINARY MODELING OF POWER GRIDS IN THREE DIMENSIONAL INTEGRATED CIRCUITS

In 2-D integrated circuits as described in the previous chapters, chip size is continually increasing despite reductions in feature size made possible by advances in IC technology due to Moore's law. At the same time, three-dimensional (3-D) integration provides a promising solution that can reduce the chip size while significantly enhancing the performance of the integrated circuit [105]. It can reduce the interconnect delay, ease noise isolation in mixed-signal environment, reduce the complexity of heterogeneous integration of different technologies, shrink chip size and increase packaging density [105] [106]. All of these are possible since different functional blocks can be placed on separate semiconductor layers, which are stacked on top of each other, as shown in Fig. 124. The 3D integration offers an extra degree of freedom to the chip designer and exploits the vertical dimension for alleviating the interconnect related problems, which increases the functionality and reduces size.

A comprehensive treatment of 3-D ICs has been presented in [105] and it has been shown that by simply dividing a planar chip into separate blocks, each occupying a separate physical level interconnected by short and vertical inter-layer interconnects, significant improvement in performance and reduction in chip area can be achieved. In [105], the power problems of 3-D ICs have been discussed from the angle of thermo-mechanical analysis, using heat sink technology for heat dissipation. However, rigorous research has not been done in characterizing the electrical performance of the power grid in 3-D ICs. To predict the potential power integrity problem in 3-D ICs, this chapter discusses a methodology for modeling and simulating the power grid in 3-D ICs.

The content of this chapter is organized as follows. At first, the complex image technique is extended from microstrip-type interconnects to stripline-type interconnects. Macromodel

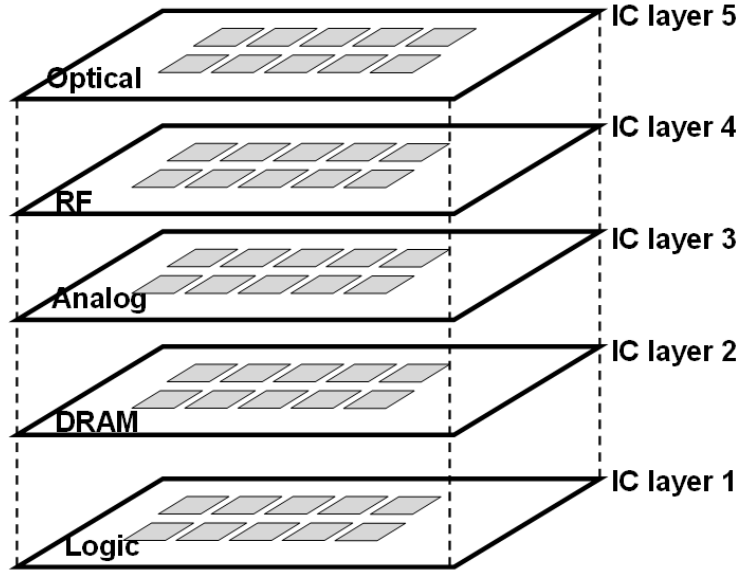


Figure 124: Side view of 3D integration

images are used to capture the loss mechanism of the multiple conductive substrates. Secondly, the macromodel images are applied on a single strip-line as well as coupled strip-line interconnects. Afterwards, the model of power grid of 3-D IC is constructed based on the circuit representation of coupled strip-line interconnects, which has been simulated using circuit based FDTD algorithm.

5.1 Complex image for dual conductive substrate

Along with multiple advantages such as high packaging density, 3-D architectures also provides new challenges to the traditional computer-aided-design tools. A major problem is the interconnect characterization for power integrity analysis. This section focuses on modeling power distribution network in 3-D integrated circuits, which has the cross section shown in Fig. 125. In Fig. 125, the power grid for a single IC layer contains four layers of orthogonal buses, which is embedded in SiO_2 and sandwiched between two silicon substrates. The simplest unit of the 3-D power grid in 3-D ICs is an interconnect embedded in SiO_2 and sandwiched between two silicon substrates, as shown in Fig. 126. The difference between the interconnects in 2-D and 3-D ICs is that there are two or multiple conductive substrates on

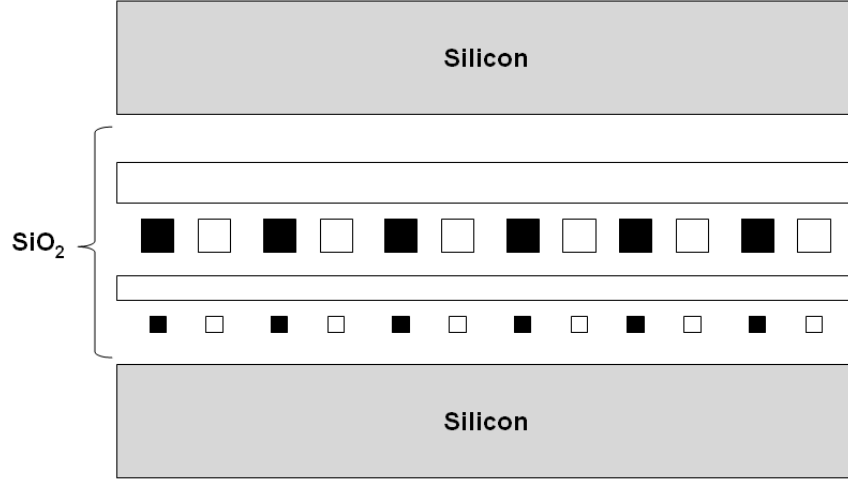


Figure 125: Cross section of power grid in 3-D ICs for a single IC layer

either side of the interconnect for 3-D ICs. Complex image technique has been successfully applied for modeling the interconnects in 2-D ICs in Chapter III and IV, which has been extended to the interconnects in 3-D ICs in the following sections.

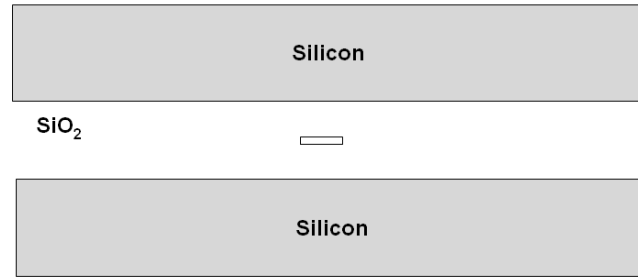


Figure 126: Cross section of single interconnect in 3-D IC

5.1.1 Complex image technique for modeling 2-D interconnects

The derivation of the complex image technique for a microstrip-type on-chip interconnect, as shown in Fig. 127, is briefly reviewed in this section and has been extended to 3-D interconnects in subsection 5.1.2. This review is not a simple duplication of subsection 1.3.1.3 in the first chapter, but provides a deeper insight into the nature of complex image

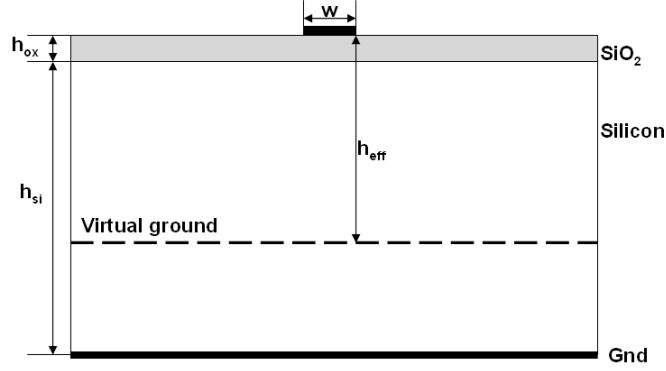


Figure 127: Complex image for an on-chip microstrip line

in the conductive substrate.

For the on-chip microstrip, the Green's function satisfies the partial differential equations of magnetic vector potential (1.23), which is given by:

$$G(x, y|x', y') = \frac{\mu_0}{2\pi} \int_0^\infty \frac{Kernel}{m} \cos(mx) dm \quad (5.1)$$

$$Kernel = e^{-m|y-h|} + a \cdot e^{md} e^{-m(y+h+d)}$$

where $a = -(q-m)/(q+m)$, $q = \sqrt{m^2 + \gamma^2}$ and $\gamma = \sqrt{j\omega\mu_0\sigma}$. In Eq. (5.1), a is calculated as a reflection coefficient, which determines the magnitude of the image current. It can be observed from the kernel of Green's function that the second term represents an image current located at complex distance $h+d$ below the dielectric interface. The first order approximation of the magnitude of image current, $a \cdot e^{md}$, is given by:

$$a \cdot e^{md} = -1 - (d - \frac{2}{\gamma})m + O(m^2) \quad (5.2)$$

where $O(m^2)$ is the error in the approximation. This error is proportional to m^2 and can be ignored, which can be written as

$$a \cdot e^{md} \approx -1 - (d - \frac{2}{\gamma})m = -1 \Big|_{d=\frac{2}{\gamma}} \quad (5.3)$$

The approximation of the magnitude of image current, $a \cdot e^{md}$ becomes -1 under the condition $d = 2/\gamma$, which means that an image current with the same volume as the source current flows in a direction opposite to the source current. Thus, the system is neutral due to the cancellation of the forward and return current.

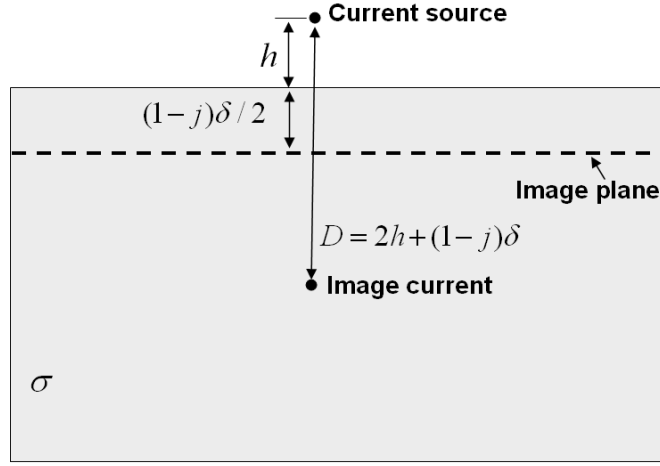


Figure 128: Complex image for a microstrip over a semi-infinite lossy substrate

The image current is placed at a complex depth below the microstrip line. As an alternative to the complex image current representation, the effect of the lossy substrate can be modeled as a virtual ground plane centered between the source and image current, as shown in Fig. 128, which is at a complex distance h_{eff} from the current source. The complex depth h_{eff} of a microstrip over a semi-infinite lossy substrate is given by

$$h_{eff} = h_{ox} + (1-j)\delta/2 \quad (5.4)$$

where $\delta = 1/\sqrt{\pi f \mu_0 \sigma}$ is the skin depth of the bulk silicon of the lossy substrate [71]. The neutrality principle will be used to develop complex image current for 3-D ICs and expressions similar to (5.2) and (5.3) will be derived in the following subsections.

5.1.2 Complex image technique for modeling interconnects in 3-D ICs

The same concept of virtual ground plane and complex distance can be applied on interconnects in 3-D integrated circuits. Since return current will be distributed in the lower as well as upper substrates, two virtual ground planes are needed to model this cross section. Fig. 129 shows a single strip with two virtual ground planes in a multilayered structure composed of SiO_2 and two silicon substrates. Since ground planes are present beneath and above the signal line, stripline model has been developed for modeling interconnects in 3-D

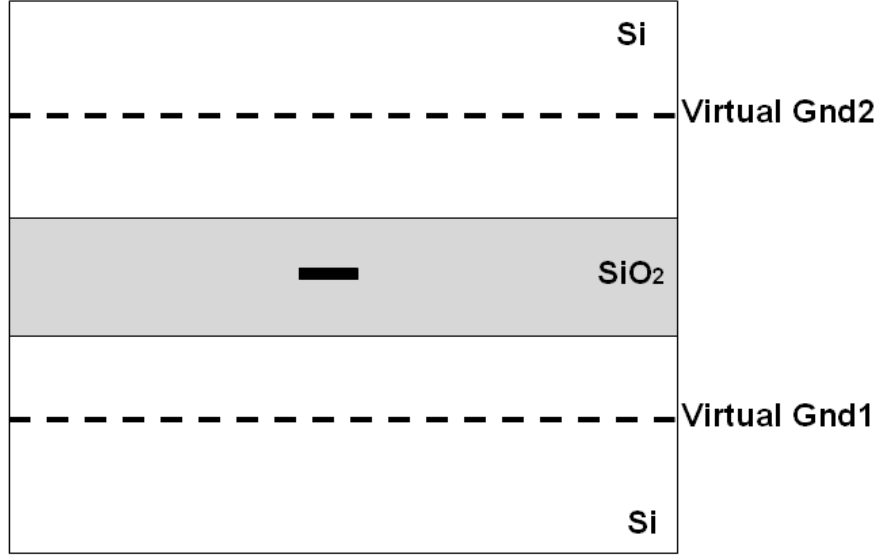


Figure 129: Embedded interconnect with two virtual ground planes

ICs.

Though the difference between microstrip-type and stripline-type transmission lines is the absence or presence of a ground plane, the number of image currents varies substantially (from one to infinity), due to multi-reflections. As shown in Fig. 130(a), the entire image current consist of two groups, elements of which are denoted by $1\star$ and $2\star$, where \star is a used to identify the sequence of image current. The first element of group No.1, 1a, is the image of the current source referred to ground plane Gnd1. The second element 1b, is the image of 1a referred to ground plane Gnd2. The rest of the elements are the images of previous elements referred to the appropriate ground planes. The formation of elements in group No.2 is similar except that the first element is the image of current source referred to ground plane Gnd2. Eventually, the distribution of the image current is the superposition of two groups as shown in Fig. 130(b). In Fig. 130(b), \odot and \otimes denote the alternating direction of the current, and filled/unfilled circles are used to distinguish the two groups in Fig. 130.

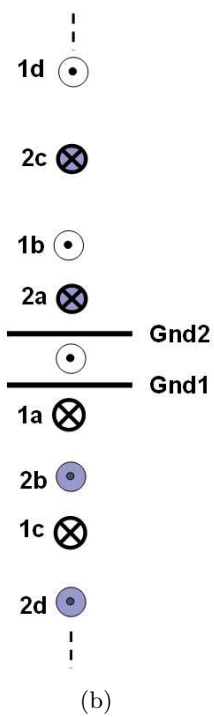
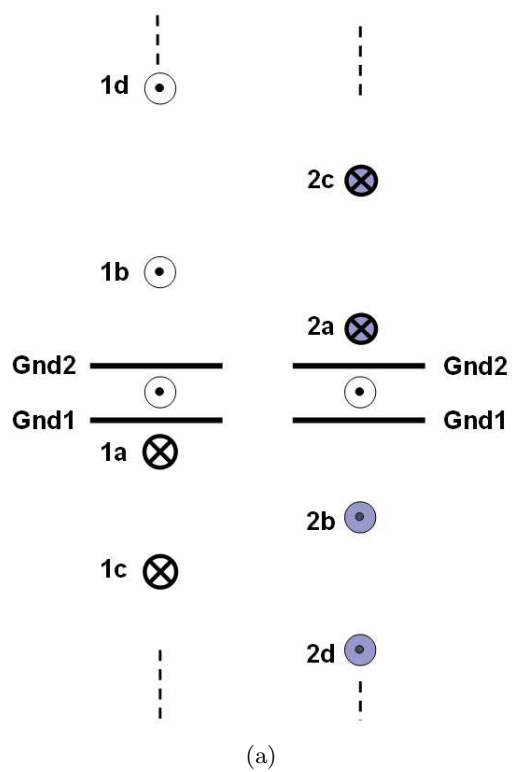


Figure 130: Image currents of strip line (a) Infinite images of group No. 1 and No. 2, (b) Total infinite images for strip line

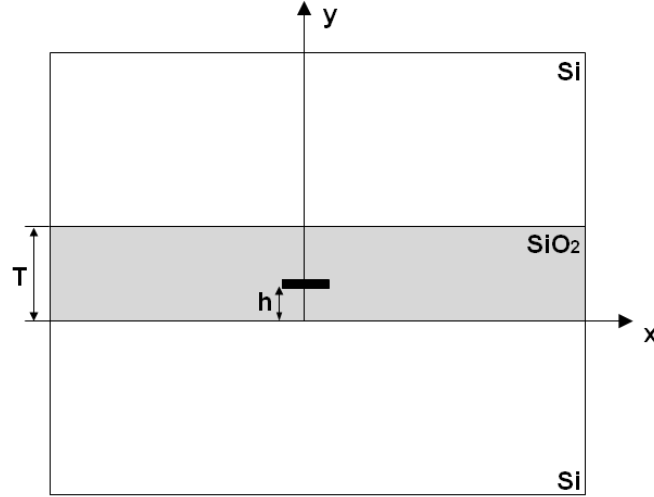


Figure 131: Coordinate of embedded interconnect

The mathematical model of infinite image currents is an infinite series, which is not convenient for engineering applications. One way to solve this problem is to truncate the infinite series to finite terms, which requires the estimation of truncation error to determine the number of terms to retain in the infinite series. In the following sections, a simplified model is proposed which replaces the infinite images by two macromodel images. No truncation is made to the infinite series in forming the macromodel images, so that the macromodel represents the entire series and captures the effect of multi-reflection between two ground planes. The macromodel image current is derived in the next paragraph for infinite substrate and finite substrate with ground planes.

5.1.2.1 Complex image for infinite substrate

The solution of Green's function for infinite substrate is derived as follows. The back and forth reflection of the image current is characterized by the increasing order of the reflection coefficient $a^n = [-(q-m)/(q+m)]^n$, and increasing distance between image and its original source $|y \pm (nT \pm h)|$, where n is the integer number, T and h denotes the distance, as shown in Fig. 131. In Fig. 131, $T = 2h$ holds true for symmetric system, while $T \neq 2h$ is valid for asymmetric system. The total effect of the infinite images can be expressed as a summation,

which can be written as:

$$\begin{aligned}
& Kernel_{\text{inf}} \\
&= e^{-m|y-h|} \\
&+ \{ae^{-m(y+h)} + a^2e^{-m(-y+2T+h)} + a^3e^{-m(y+2T+h)} + a^4e^{-m(-y+4T+h)} \dots\} \\
&+ \{ae^{-m(-y+2T-h)} + a^2e^{-m(y+2T-h)} + a^3e^{-m(-y+4T-h)} + a^4e^{-m(y+4T-h)} + \dots\}
\end{aligned} \tag{5.5}$$

In Eq. 5.5, the first term $e^{-m|y-h|}$ represents the contribution from the source located at $y = h$. The terms in the first curly parenthesis represent the image currents of group No. 1. The magnitude of each term is denoted as a^N , where N is increased by 1 after each reflection. The location of each image current is calculated as $(y + (N-1) \times T + h)$ for N as an odd number, and $(-y + N \times T + h)$ for N as an even number. The terms in the second curly parenthesis represent the image currents of group No. 2. The location of each image current is calculated as $(-y + (N+1) \times T - h)$ for N as an odd number, and $(y + N \times T - h)$ for N as an even number.

The infinite geometric series has been used to calculate the summation of image currents, which is given by:

$$S = \sum_{n=1}^{\infty} b \cdot q^{n-1} = \frac{b}{1-q}, (|q| < 1) \tag{5.6}$$

where b is the first term of infinite geometric series and q is the ratio between two successive elements in the series. After substituting Eq. (5.6) into Eq. (5.5), a simplified three-term summation is obtained in Eq. (5.7). During the substitution, the condition of $|q| = |a^2e^{-m(2T)}| < 1$ is satisfied which guarantees convergence. The physical explanation of $|q| < 1$ is that the magnitude of image current shrinks after each reflection. Due to Eq. (5.6), the contribution from all of the infinite image currents can be written as:

$$\begin{aligned}
& Kernel_{\text{inf}} \\
&= e^{-m|y-h|} \\
&+ \frac{e^{m \cdot d_{\text{down}}}}{1 - a^2e^{-m \cdot 2T}} [a^{-mh} + a^2e^{-m(2T-h)}] e^{-m(y+d_{\text{down}})} \\
&+ \frac{e^{m \cdot d_{\text{up}}}}{1 - a^2e^{-m \cdot 2T}} [a^2e^{-m(T+h)} + ae^{-m(T-h)}] e^{-m(-y+T+d_{\text{up}})} \\
&= e^{-m|y-h|} + f_{\text{down}}(m, \gamma, d_{\text{down}}) e^{-m(y+d_{\text{down}})} + f_{\text{up}}(m, \gamma, d_{\text{up}}) e^{-m(-y+T+d_{\text{up}})}
\end{aligned} \tag{5.7}$$

Compared with Eq. (5.1), it can be observed that the kernel of Green's function in Eq. (5.7) contains three currents: source current at $y = h$ and two macromodel images

at $y = -d_{down}$ and $y = T + d_{up}$, respectively. These two image currents have different magnitudes which are denoted by $f_{down}(m, \gamma, d_{down})$ and $f_{up}(m, \gamma, d_{up})$ in Eq. (5.7). To determine the value of $d_{up/down}$ and $f_{up/down}$, neutral condition can be applied on Eq. (5.7). To accomplish this, the first order approximation of $f_{down}(m, \gamma, d_{down})$ and $f_{up}(m, \gamma, d_{up})$ has been used. These quantities, under the condition that d_{down} and d_{up} assume the value of $1/\gamma$, is given in Eq. (5.8) as:

$$f_{down}(m, \gamma, d_{down}) = -\frac{\gamma T - h\gamma + 1}{\gamma T + 2} + O(m^2) \big|_{d_{down}=1/\gamma} \quad (5.8a)$$

$$f_{up}(m, \gamma, d_{up}) = -\frac{h\gamma + 1}{\gamma T + 2} + O(m^2) \big|_{d_{up}=1/\gamma} \quad (5.8b)$$

where $O(m^2)$ is the error in the approximation, which is proportional to m^2 and can be ignored.

The summation of the volume of two image currents can be written as:

$$-\frac{\gamma T - \gamma h + 1}{\gamma T + 2} - \frac{\gamma h + 1}{\gamma T + 2} = -1 \quad (5.9)$$

where the first term $-\frac{\gamma T - \gamma h + 1}{\gamma T + 2}$ denotes the magnitude of the image current in the lower substrate, and the second term $-\frac{\gamma h + 1}{\gamma T + 2}$ denotes the magnitude of the image current in the upper substrate. The summation of the volume is -1, which means that the entire image current has the same magnitude as the source current and flows in a direction opposite to the source current. Thus, the system is neutral due to the cancellation of the forward and return currents.

In short, the complex image for two (top and bottom) infinite substrates has been summarized in Eq. (5.10) and shown pictorially in Fig. 132.

$$G_{inf}(x, y|x', y') = \frac{\mu_0}{2\pi} \int_0^\infty \frac{Kernel_{inf}}{m} \cos(mx) dm \quad (5.10)$$

$$Kernel_{inf} \approx e^{-m|y-h|} - \frac{\gamma T - h\gamma + 1}{\gamma T + 2} e^{-m(y+1/\gamma)} - \frac{h\gamma + 1}{\gamma T + 2} e^{-m(-y+T+1/\gamma)}$$

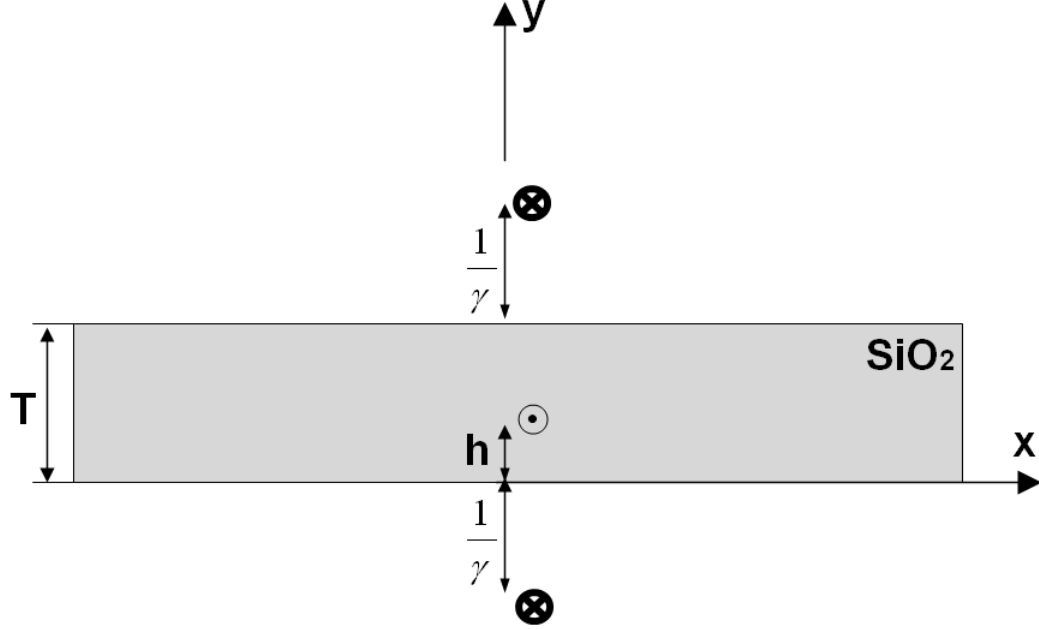


Figure 132: Embedded interconnect with two macromodel images

5.1.2.2 Complex image for ground-backed substrate

For the interconnect sandwiched between two ground-backed substrates (GBS) as shown in Fig. 133, the magnitude and location of complex image can be derived in a way similar to the previous subsection. However, based on transmission line theory, the summation of infinite geometric series can be avoided. It is observed that the symbol q in reflection coefficient of infinite substrate $a = -(q - m)/(q + m)$ represents the input impedance of an infinite long transmission line. For the same reason, the ground-backed substrate corresponds to a finite transmission line with a short circuit at the far end, for which the input impedance can be found as $p = q \cdot \coth(q \cdot h_{Si})$ [98], where h_{Si} is the thickness of the silicon substrate. Thus, the kernel of Green's function of ground-backed substrate assumes the same form as Eq. (5.7) except that the reflection coefficient needs to be changed to $a = -(p - m)/(p + m)$,

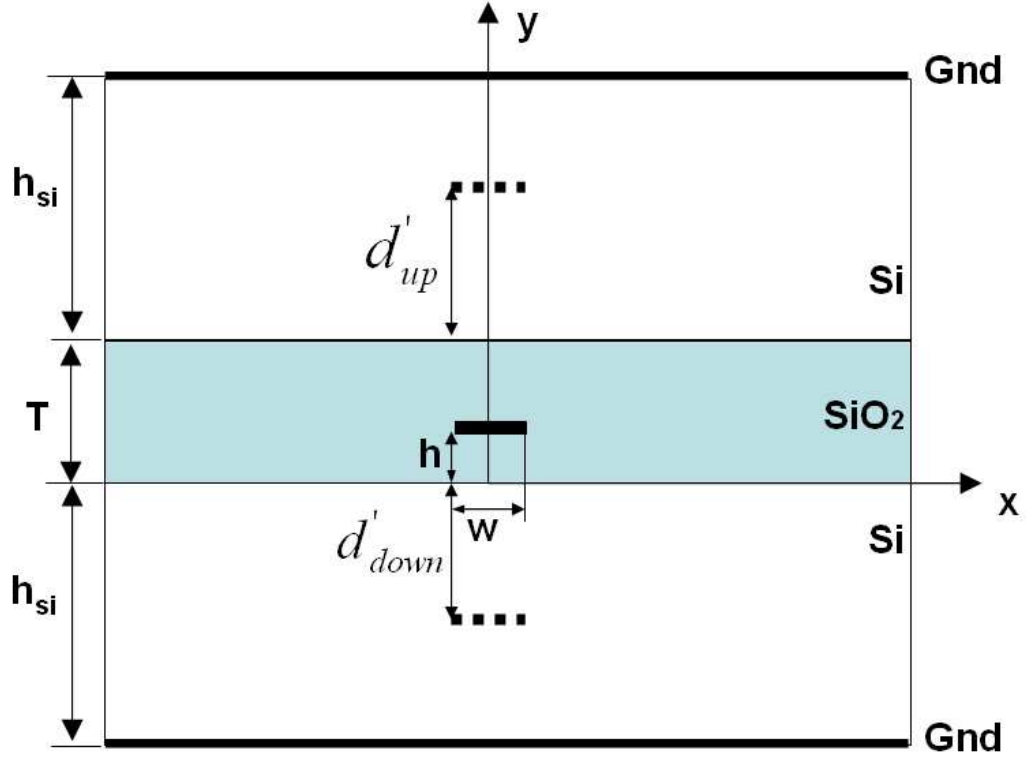


Figure 133: Grounded substrate with two macromodel images

which is given below:

$$\begin{aligned}
 & Kernel_{GBS} \\
 &= Kernel_{inf} \Big|_{a=-\frac{p-m}{p+m}} \\
 &= e^{-m|y-h|} + f_{down}(m, \gamma, d'_{down})e^{-m(y+d'_{down})} + f_{up}(m, \gamma, d'_{up})e^{-m(-y+T+d'_{up})}
 \end{aligned} \tag{5.11}$$

where $f_{down}(m, \gamma, d'_{down})$ and $f_{up}(m, \gamma, d'_{up})$ denotes the magnitude of two image currents. Their first order approximation is given in Eq. (5.12a) and (5.13a), under the condition that d'_{down} and d'_{up} assume the values in Eq. (5.12b) and (5.13b), respectively.

$$f_{down}(m, \gamma, d'_{down}) = -\frac{1 + \gamma(T-h) \coth(h_{si} \cdot \gamma)}{2 + \gamma T \coth(h_{si} \cdot \gamma)} + O(m^2) \tag{5.12a}$$

$$d'_{down} = \frac{\gamma(2h - 3T) + \gamma^2(h - T)T \coth(h_{si} \cdot \gamma) - 2 \tanh(h_{si} \cdot \gamma)}{-2\gamma + \gamma^2(2h - 3T) \coth(h_{si} \cdot \gamma) + \gamma^3(h - T)T \coth(h_{si} \cdot \gamma)^2} \tag{5.12b}$$

$$f_{up}(m, \gamma, d'_{up}) = -\frac{1 + \gamma h \coth(h_{si} \cdot \gamma)}{2 + \gamma T \coth(h_{si} \cdot \gamma)} + O(m^2) \quad (5.13a)$$

$$d'_{up} = \frac{\gamma(2b + T) + h\gamma^2 T \coth(h_{si} \cdot \gamma) + 2 \tanh(h_{si} \cdot \gamma)}{2\gamma + \gamma^2(2h + T) \coth(h_{si} \cdot \gamma) + h\gamma^3 T \coth(h_{si} \cdot \gamma)^2} \quad (5.13b)$$

There are several physical explanations for the properties of Eq. 5.12 and 5.13. These are as follows:

- 1) The system stays neutral, since the total volume of the return current cancels the source current, given by:

$$-\frac{1 + \gamma(T - h) \coth(h_{si} \cdot \gamma)}{2 + \gamma T \coth(h_{si} \cdot \gamma)} - \frac{1 + \gamma h \coth(h_{si} \cdot \gamma)}{2 + \gamma T \coth(h_{si} \cdot \gamma)} = -1 \quad (5.14)$$

- 2) The macromodel image current is symmetric for symmetric stripline trace, and hence

$$d'_{down} |_{T=2h} = d'_{up} |_{T=2h} \quad (5.15)$$

- 3) The system is consistent with the previous macromodel, such that d'_{down} and d'_{up} are the same as those for infinite substrate, under the limit that the thickness of silicon approaches infinity, given by:

$$\lim_{h_{si} \rightarrow \infty} d'_{down} = \lim_{h_{si} \rightarrow \infty} d'_{up} = \frac{1}{\gamma} = d_{down} = d_{up} \quad (5.16)$$

The physical explanation of the above equation is that the short-circuit termination at the far end of an infinite transmission line does not affect the characteristic of the infinite transmission line.

5.2 *Extraction of transmission line parameters for interconnects in 3-D ICs*

Due to the analogy between the cross section of transmission line in 3-D ICs and that of stripline waveguides, expressions for striplines derived earlier has been adopted for modeling the 3-D transmission lines. Different layouts of interconnects in 3-D ICs and corresponding stripline models will be discussed in the following subsections, which include symmetric, asymmetric and coupled 3-D interconnects.

5.2.1 Transmission line parameter extraction for symmetric interconnects in 3-D ICs

A symmetric 3-D interconnect, in which the conductor is located in the middle of the SiO₂ ($T = 2h$), has been modeled as a symmetric stripline. The series inductance and resistance parameters can be determined from the closed-form expressions for symmetric stripline by applying the macromodel complex image derived in Eq. 5.12 and 5.13 for grounded substrate. The closed-form expression of inductance for a lossless stripline is readily available from Wheeler's publication [108], which can be written as:

$$L_{stripline}(h, w) = \frac{\mu_0}{4\pi} \ln \left\{ 1 + \frac{1}{2} \left(\frac{16h}{\pi w} \right) \left[\frac{16h}{\pi w} + \sqrt{\left(\frac{16h}{\pi w} \right)^2 + 6.27} \right] \right\} \quad (5.17)$$

After applying the macromodel image and replacing the ' h ' with ' h_{eff} ' in Eq. (5.17), the series inductance and resistance parameters can be determined from the real and imaginary part of the $L_{stripline}(h_{eff}, w)$ as:

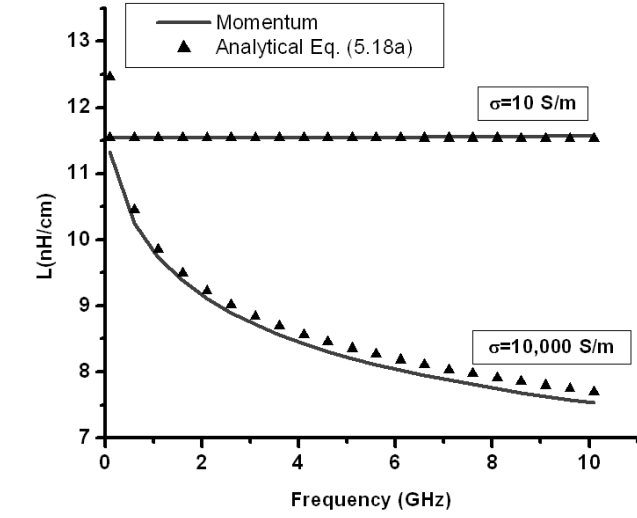
$$L(\varpi) = \text{Re}[L_{stripline}(h_{eff}, w)] \quad (5.18a)$$

$$R(\varpi) = -\varpi \text{Im}[L_{stripline}(h_{eff}, w)] \quad (5.18b)$$

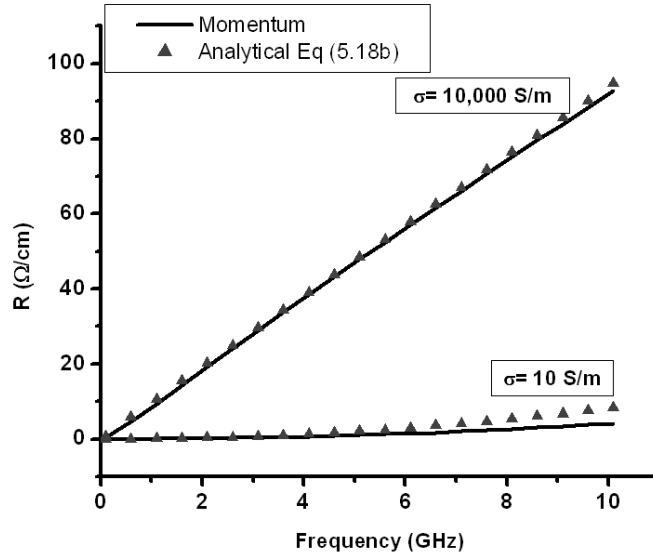
where h_{eff} is the complex distance between the source and virtual ground, which is located in the center of the source and macromodel image.

To verify the accuracy of the combination of Wheeler's expression and macromodel image, the structure shown in Fig. 133 with the following parameters has been modeled: $w = 4\mu m$, $h = 2\mu m$, $T = 4\mu m$, $h_{si} = 500\mu m$. Per unit length (pul) inductance (L) and resistance (R) are calculated for the cases where the substrates have two different conductivity, namely, $\sigma = 10,000$ S/m and $\sigma = 10$ S/m. Firstly, R and L are extracted assuming that the conductor has zero thickness. After that, the effect of thickness of the conductor is taken into account as described in section 4.2.2.

The extracted ' R ' and ' L ' parameters for zero thickness conductor have been compared with MomentumTM in Fig. 134.



(a)



(b)

Figure 134: Series impedance of zero thickness 3-D interconnect (a) Inductance, (b)Resistance

Fig. 134 demonstrates significant frequency dependence in ' R ' and ' L ' parameters for substrate with high conductivity, or in other words, the R and L are more sensitive to the change of frequency for substrate with high conductivity. The physical interpretation is that the depth of eddy current in the substrate with high conductivity shows stronger frequency dependence than that in the substrate with low conductivity. The absolute value of ' h_{eff} ' is plotted for the above cases in Fig. 135, showing the variation of ' h_{eff} ' with frequency.

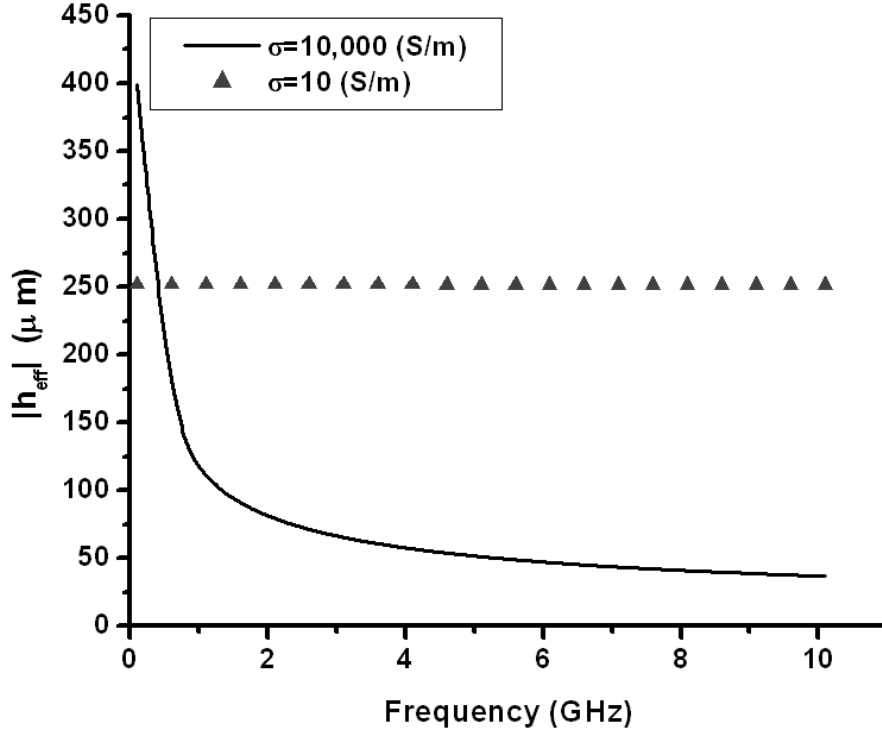
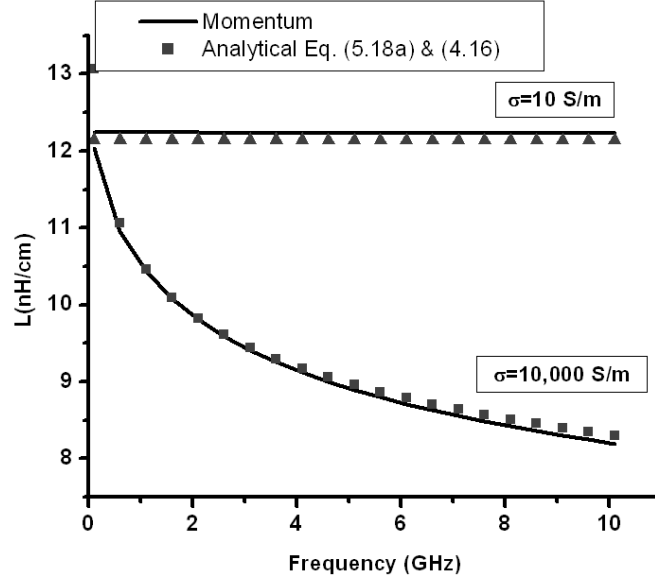


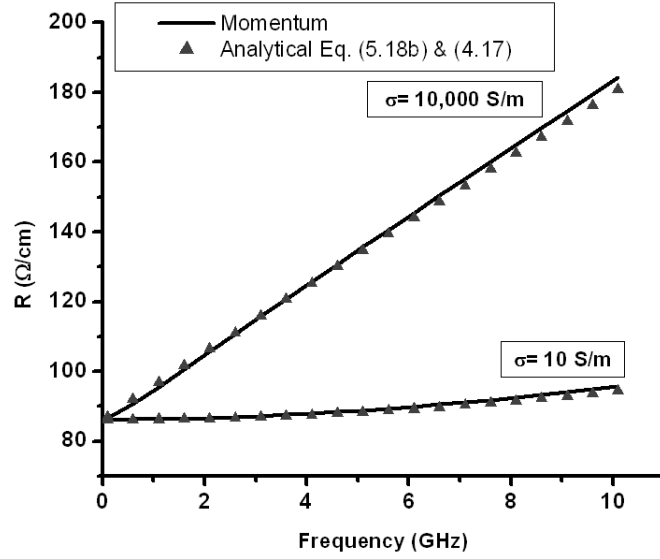
Figure 135: Comparison of $|h_{eff}|$

To account for conductor thickness, Eq. (4.16) and (4.17) in Section 4.2.2 are applied on the same stripline with a conductor whose thickness is $0.5\mu m$. The updated ‘ R ’ and ‘ L ’ values are plotted in Fig. 136.

The shunt capacitance and conductance of 3-D interconnect can be obtained by following the asymptotic solution approach described in Section 4.2. A circuit model for the shunt admittance of a symmetric 3-D interconnect is shown in Fig. 137(a). At sufficiently low frequency, the displacement current in the substrate is negligible compared with the conduction current and thus the lossy substrate behaves as a ground plane. At higher frequencies, the conduction current and displacement current coexist in the lossy substrate, which can be represented by the circuit model with parallel connected capacitance (C_{si}) and conductance (G_{si}) parameters. Due to the symmetry of the stripline, its model can be simplified as a microstrip with the elements shown in Fig. 137(b). The resulting capacitance



(a)



(b)

Figure 136: Series impedance of finite thickness ($0.5\mu\text{m}$) interconnect in 3-D ICs (a) Inductance, (b) Resistance

C_{ox}^{eq} is that of a stripline with SiO₂ as dielectric substrate medium, which can be obtained from the analytical expression for the capacitance of a symmetric strip line [123], given by:

$$C_{ox} = \frac{1.41\epsilon_r}{\ln\left[\frac{3.81h}{0.8w+t}\right]} \quad (5.19)$$

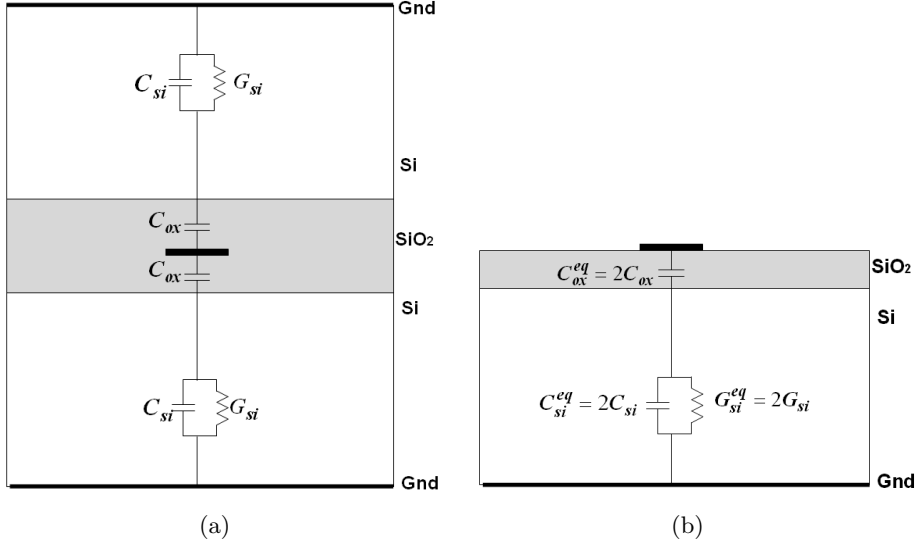
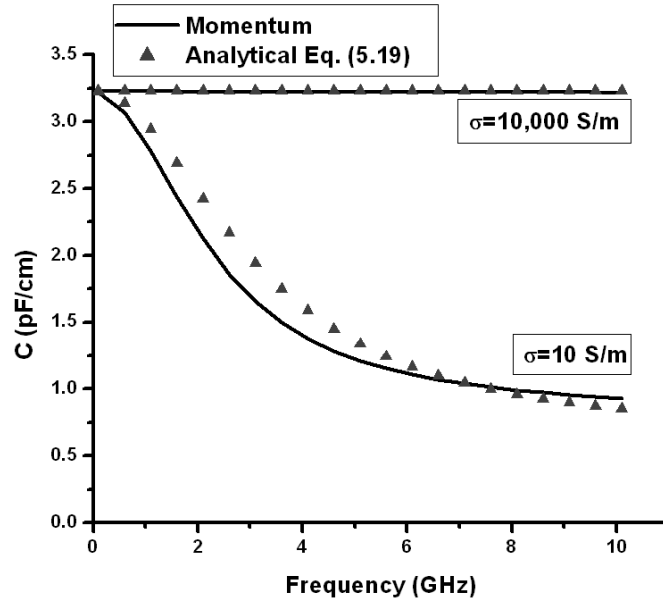


Figure 137: Shunt admittance (a) Circuit model of stripline, (b) Equivalent microstrip model

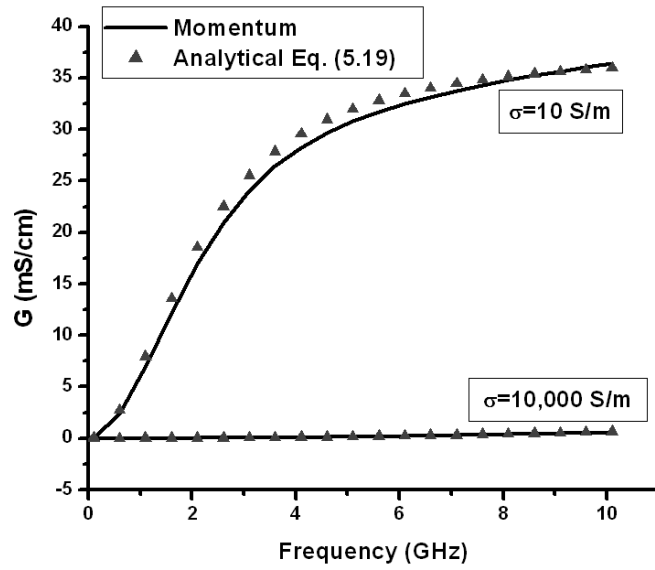
Using the above circuit model, the C and G parameters have been extracted for 3-D interconnect embedded in the substrate with conductivity of $\sigma = 10,000$ S/m and $\sigma = 10$ S/m and correlated with the results from MomentumTM, as shown in Fig. 138.

Fig. 138 demonstrates that C and G parameters for substrate with high conductivity are less sensitive to the change of frequency than the C and G parameters for substrate with low conductivity, which is opposite to the characteristics of L and R parameters. This can be interpreted by using the circuit model in Fig. 137(b). In the substrate with high conductivity, the conduction current dominates the displacement current so that $G_{si}^{eq} \gg j\omega C_{si}^{eq}$ and $G_{si}^{eq} \gg j\omega C_{ox}^{eq}$. The total admittance can be written as:

$$(G_{si}^{eq} + j\omega C_{si}^{eq}) // j\omega C_{ox}^{eq} \approx G_{si}^{eq} // j\omega C_{ox}^{eq} \approx j\omega C_{ox}^{eq} \quad (5.20)$$



(a)



(b)

Figure 138: Shunt admittance of 3-D interconnect (a) Capacitance, (b) Conductance

where $//$ symbolizes an operation defined as $a//b = (a \times b)/(a + b)$. Hence, the G pul parameter, which is the real part of admittance, can be written as:

$$G_{pul} = \text{Re}[(G_{si}^{eq} + j\varpi C_{si}^{eq})//j\varpi C_{ox}^{eq}] \approx \text{Re}(j\varpi C_{ox}^{eq}) = 0 \quad (5.21)$$

The C pul parameter, which is obtained from the imaginary part of the admittance, can be written as:

$$C_{pul} = \text{Im}[(G_{si}^{eq} + j\varpi C_{si}^{eq})//j\varpi C_{ox}^{eq}]/\varpi \approx \varpi C_{ox}^{eq}/\varpi = C_{ox}^{eq} \quad (5.22)$$

From Eq. (5.22), it can be seen that C_{pul} is almost completely determined by the oxide capacitances and thus remains constant over the entire frequency range of interest. From Eq. (5.21), it can be seen that the G_{pul} parameter is negligibly small for 3-D interconnects embedded in substrates with high conductivity. For 3-D interconnects embedded in the substrate with low conductivity, C and G pul parameters show significant frequency dependence, because displacement current is comparable to conduction current in the substrate and both are included in the calculation of total admittance.

5.2.2 Parameter extraction for asymmetric transmission lines in 3-D ICs

The same methodology can be applied on asymmetric 3-D interconnects, as described in this section. Thus the expression for H (5.23a) from [123] and expression for C_{ox} (5.23b) from Institute of Interconnecting and Packaging Electronic Circuits (IPC) [124] can be used, where:

$$H(w, H, H_1) = \frac{80}{c} \ln\left(\frac{1.9(2H+t)}{0.8w+t}\right)\left(1 - \frac{H}{4H_1}\right) \quad (5.23a)$$

$$C_{ox} = \frac{1.06\epsilon_r}{\ln\left(\frac{1.9(2H+t)}{0.8w+t}\right)\left(1 - \frac{H}{4H_1}\right)} \quad (5.23b)$$

In Eq. (5.23a), H , H_1 are the parameters defined in Fig. 139 and c is the velocity of light in vacuum.

To verify the accuracy of the above approach for modeling the asymmetric 3-D interconnects, a strip line shown in Fig. 140 with the following parameters are modeled: $w = 4\mu m$, $h_1 = 20\mu m$, $h_2 = 10\mu m$, $h_{si} = 500\mu m$. The $RLCG$ transmission line parameters are calculated for the cases where the substrates have two different conductivities, namely, $\sigma_{si} = 10,000 S/m$ and $\sigma_{si} = 10 S/m$, as shown in Fig. 141.

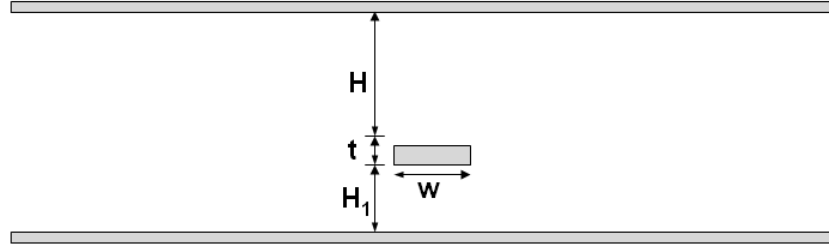


Figure 139: Cross section of asymmetric stripline

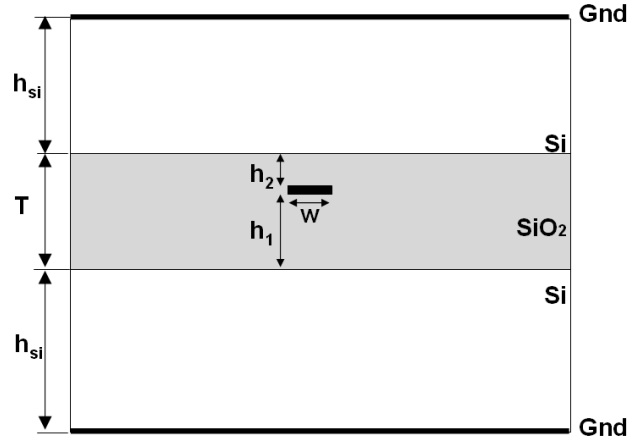


Figure 140: Cross section of asymmetric 3-D interconnect

In Fig. 141, the results obtained using analytical expressions are seen to be in good agreement with the results from MomentumTM. Fig. 141(a) and 141(b) demonstrate the significant frequency dependence in L and R parameters for substrate with high conductivity, which can be attributed to the frequency dependent depth of eddy current in the substrate with high conductivity, as discussed in Section 5.2.1.

The shunt admittance parameters, C and G , remain constant over the frequency range for substrate with high conductivity, as shown in Fig. 141(c) and 141(d). This can be explained using Eq. (5.21) and (5.22), which stem from the analysis that conduction current dominates displacement current in the substrate with high conductivity.

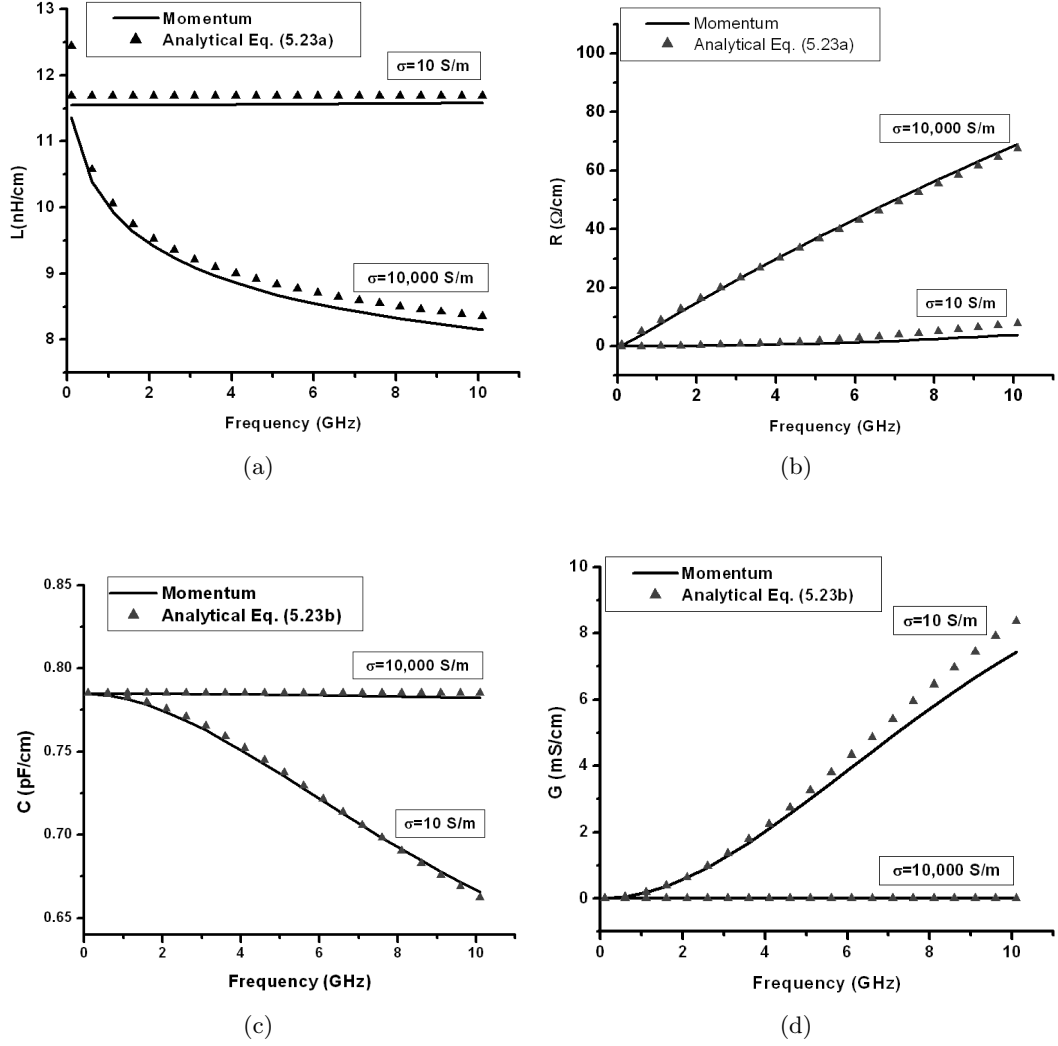


Figure 141: Parameters of an asymmetric 3-D interconnect (a) Inductance, (b) Resistance, (c) Capacitance, (d) Conductance

5.2.3 Parameter extraction for coupled transmission lines in 3-D ICs

It is important to extend the methodology described in previous sections to coupled 3-D interconnects, as shown in Fig. 142, because the power grid in 3-D ICs contains multi-conductor transmission lines, which can be arranged on the same or adjacent layer(s). However, the analytical expressions for general coupled striplines are not readily available. To overcome this problem, the following approach is proposed. The loss mechanism in the bottom silicon substrate is modeled as a virtual ground plane while eddy currents in the top silicon substrate are represented by complex images. The schematic of this modeling

approach is illustrated in Fig. 143 with the coupled strips and their images numbered.

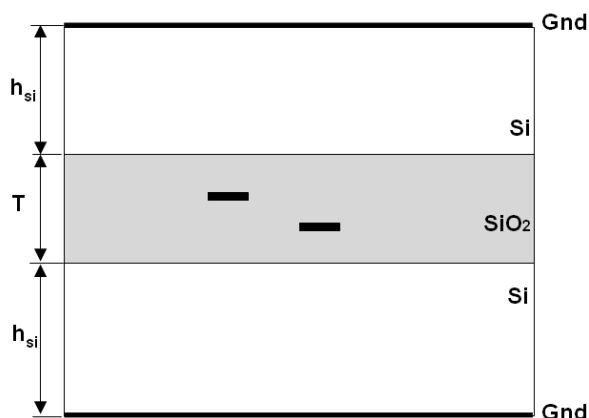


Figure 142: Cross section of coupled 3-D interconnects

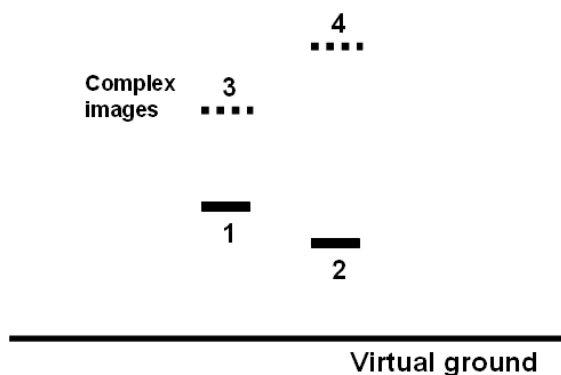


Figure 143: Modeling of coupled 3-D interconnects

It is apparent that after the above procedure is applied, the two coupled-stripline system is now transformed as a four coupled-microstrip system. For the coupled microstrip configuration, the general solution has been fully explored in section 4.2. Therefore, the modeling of N 3-D interconnects/coupled striplines can be transformed as $2N$ coupled microstrips whose solution is readily available. The solution is in the form of $2N \times 2N$ matrices. In order to obtain the $N \times N$ matrices for N transmission lines, one more step has been used to map the $2N \times 2N$ matrices to $N \times N$ matrices, which was originally presented in [71].

Using two coupled striplines in Fig. 143 as an example, a 4×4 inductance matrix can be obtained after applying the above transformation step, which contains the partial inductance element $L_{11}, L_{12}, \dots, L_{44}$. The equivalent 2×2 inductance matrix can be expressed as:

$$[L] = \begin{bmatrix} L_{11} - L_{13} & L_{12} - L_{14} \\ L_{12} - L_{23} & L_{22} - L_{24} \end{bmatrix} \quad (5.24)$$

A simple explanation for forming the elements of the above inductance matrix is provided below:

$$\begin{aligned} V_1 &= sL_{11}I_1 + sL_{12}I_2 + sL_{13}I_3 + sL_{14}I_4 \\ V_2 &= sL_{12}I_1 + sL_{22}I_2 + sL_{23}I_3 + sL_{24}I_4 \end{aligned} \quad (5.25)$$

The voltage V_i across the unit length of coupled transmission lines is expressed in Eq. (5.25), where s is the Laplace's operator and I_i is the individual current. By applying the following conditions:

$$\begin{aligned} I_3 &= -I_1 \\ I_4 &= -I_2 \end{aligned} \quad (5.26)$$

the voltage V_i has the form in Eq. (5.27), which provides the elements of the inductance matrix in Eq. (5.24).

$$\begin{aligned} V_1 &= s(L_{11} - L_{13})I_1 + s(L_{12} - L_{14})I_2 \\ V_2 &= s(L_{12} - L_{23})I_1 + s(L_{22} - L_{24})I_2 \end{aligned} \quad (5.27)$$

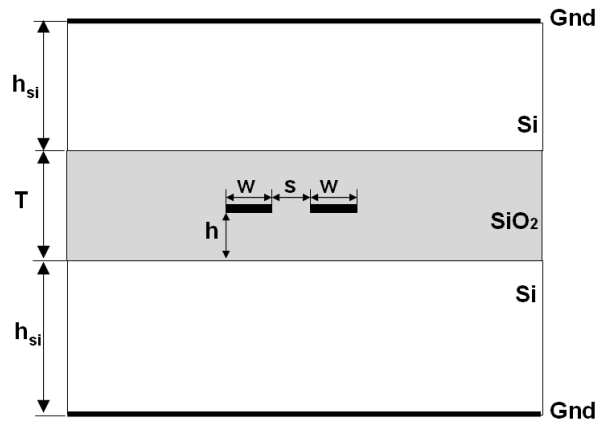


Figure 144: Test case for coupled 3-D interconnects

To verify the accuracy of the above approach for modeling coupled 3-D interconnects, a structure shown in Fig. 144 with the following parameters are modeled: $w = 4\mu m$, $h = 2\mu m$, $s = 2\mu m$, $T = 4\mu m$, $h_{si} = 500\mu m$ and $\sigma_{si} = 10s/m$. The $RLCG$ parameters were calculated and are shown in Fig. 145. The C and G parameters are calculated by following the procedures in Section 4.2, where the mutual capacitance is calculated using a 2-D static capacitance solver [125], since the analytical solution for mutual capacitance between general planar conductors is not readily available.

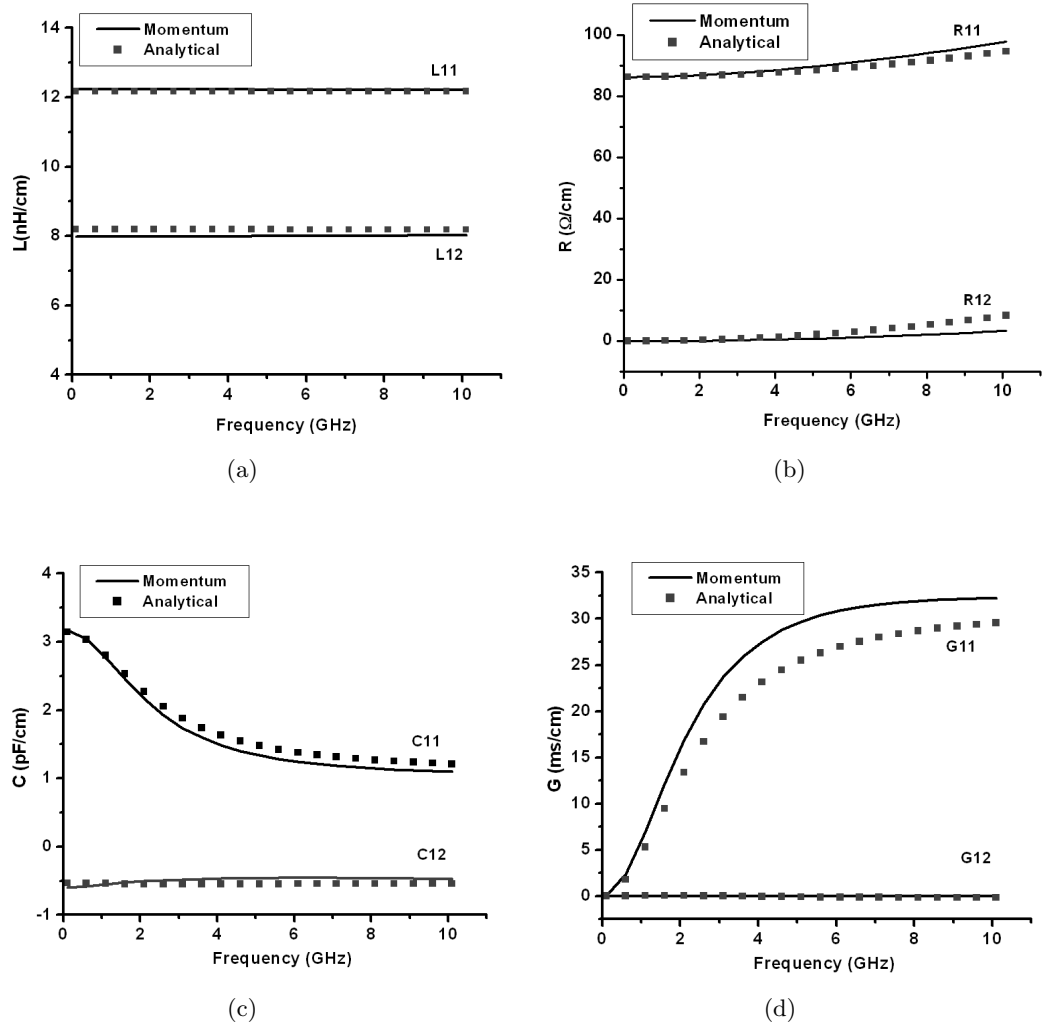


Figure 145: Parameters of two coupled 3-D interconnects (a) Inductance, (b) Resistance, (c) Capacitance, (d) Conductance

The closed-form expressions for *RLGC* parameters are in good agreement with the electromagnetic solutions, as can be seen from the comparison with MomentumTM. In Fig. 145, the self and mutual inductance and resistance do not show strong frequency dependence, because the depth of image current in the substrate remains constant, as discussed in Section 5.2.1. While there is significant frequency dependence in self capacitance and conductance, mutual capacitance and conductance, C_{12} and G_{12} , remain constant over the frequency range, because the electric field contributing to these two elements is mainly distributed in SiO₂, which is not affected by the silicon substrates.

5.2.4 Effect of M3 metal layer on M1 metal layer parasitics in 3-D ICs

The effect of adjacent layers in parasitic extraction of power grid in 3-D ICs is discussed in this section. The calculation of crossover capacitance between M1 and M2 has been discussed in Section 4.3 using closed-form expressions. This section focuses on studying the effect of M3 on the parasitics of interconnects on M1 layer.

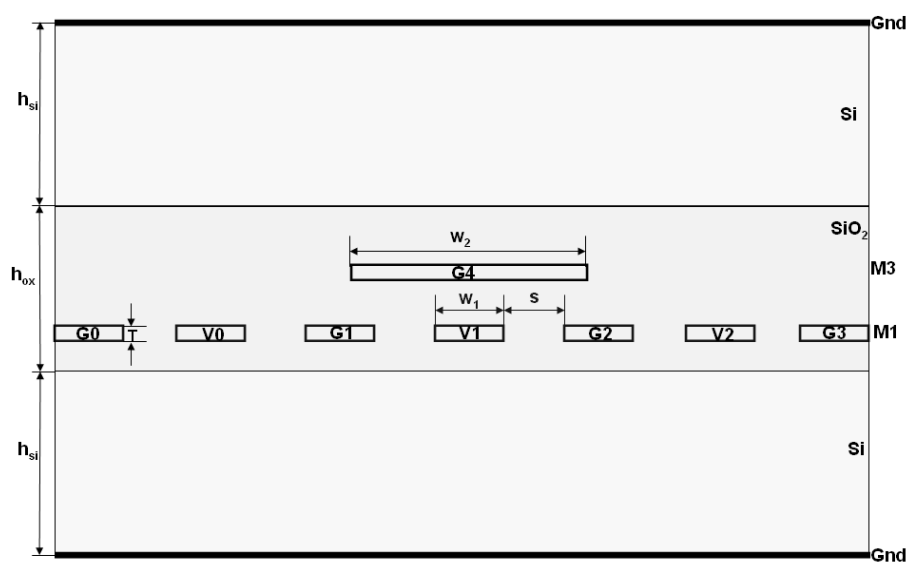


Figure 146: 3-D power grid with the following parameters: $w_1 = 4\mu m$, $w_2 = 16\mu m$, $s = 2\mu m$, $T = 0.5\mu m$, $h_{ox} = 7\mu m$, $h_{si} = 500\mu m$, $\epsilon_{siO_2} = 4$, and $\rho_{si} = 0.01 \Omega\text{-cm}$

Using the method described in Section 5.2.3, the RLGC matrices have been calculated and reduction has been carried out to obtain the single transmission line RLGC parameters

for a set of transmission lines (G1, V1, G2, G4), as shown in Fig. 146. The results obtained are compared with those of the structure without the M3 metal layer in Fig. 147.

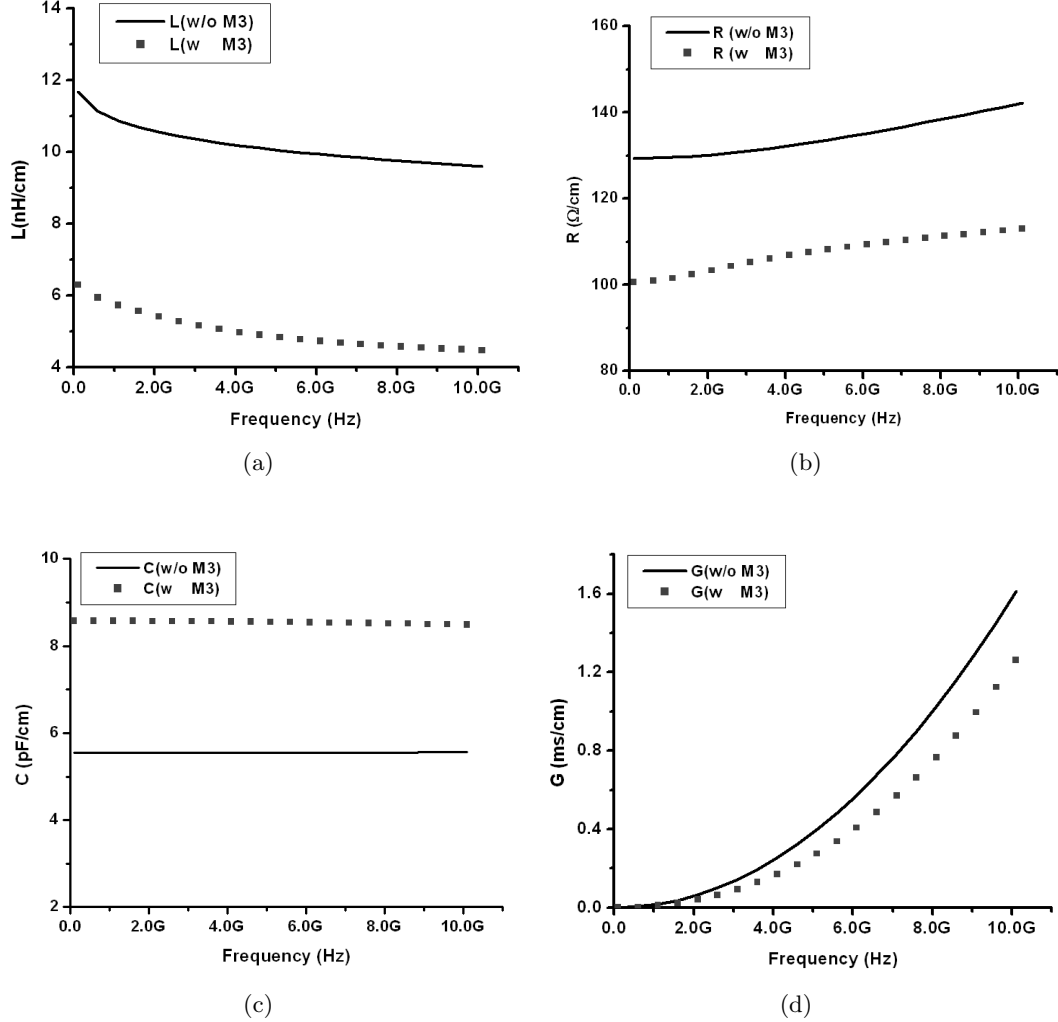


Figure 147: Parasitics of interconnects on M1 metal layer in the presence of M3 metal layer (a) Inductance, (b) Resistance, (c) Capacitance, (d) Conductance

5.3 Simulation of power grid of 3-D IC

To understand the effect of 3-D integration on switching noise and power integrity, the proposed modeling methodology has been applied to an on-chip power grid. A 4 mm \times 4 mm chip with a three-layer power distribution, as shown in Fig. 148, was modeled. The pitch of M1, M2 and M3 layer are 20 μm , 40 μm , and 80 μm , respectively. The thickness

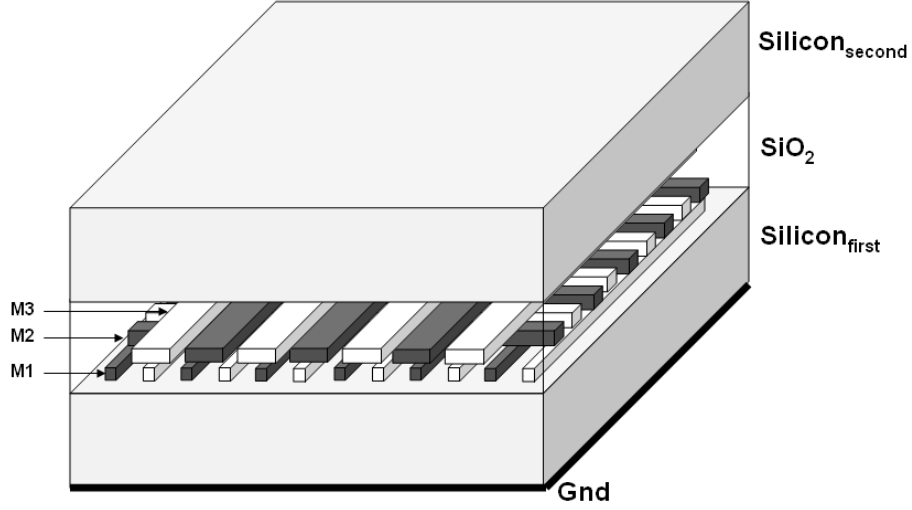


Figure 148: A three layer 3-D power grid

of power bus was $0.5\mu\text{m}$ and width of M1, M2 and M3 layer was $2\mu\text{m}$, $4\mu\text{m}$ and $8\mu\text{m}$, respectively. The power grid is embedded in SiO_2 and sandwiched between two silicon substrates, $\text{Silicon}_{\text{first}}$ and $\text{Silicon}_{\text{second}}$. The thickness of the SiO_2 is $10\mu\text{m}$. The thickness of $\text{Silicon}_{\text{first}}$ and $\text{Silicon}_{\text{second}}$ is $500\mu\text{m}$ and $10\mu\text{m}$, respectively. The $RLGC$ parameters of each metal layer have been extracted using the methods described before. The equivalent loop inductance and equivalent capacitance for multi-conductor traces have been calculated using Eq. (5.24), (4.13) and (4.14). The conductor thickness has been included in the transmission line parameters using Eq. (4.16) and (4.17). The effect of M3 metal layer has been included in the parameter extraction of M1 metal layer and vice versa using the method described in Section 4.3.1 and 4.3.2. The extracted impedance parameters for M1, M2 and M3 metal layers are listed in Table 11, in which R_{dc} and L_{ext} denote the DC resistance and low-frequency loop inductance, and $R_1 L_1$ denote the first order Debye approximation of serial impedance. The extracted admittance parameters and crossover capacitance are listed in Table 12, where G_{dc} and C_{ext} denote the DC conductance and low-frequency capacitance, and $C_1 G_1$ denote the first order Debye approximation of serial admittance. Switching current was modeled as a triangular pulse with 1ps rise time and 2ps fall time. The supply voltage was 1 V and the power density at the center of the chip

was 300 mw/mm^2 . The conductivity of the substrate was $\rho=10 \text{ } \Omega\text{-cm}$. The construction of the model for entire chip power grid follows the procedures discussed in Chapter IV, which generates the equivalent circuit automatically for FDTD simulation. The schematic of the equivalent circuit is shown in Fig. 149.

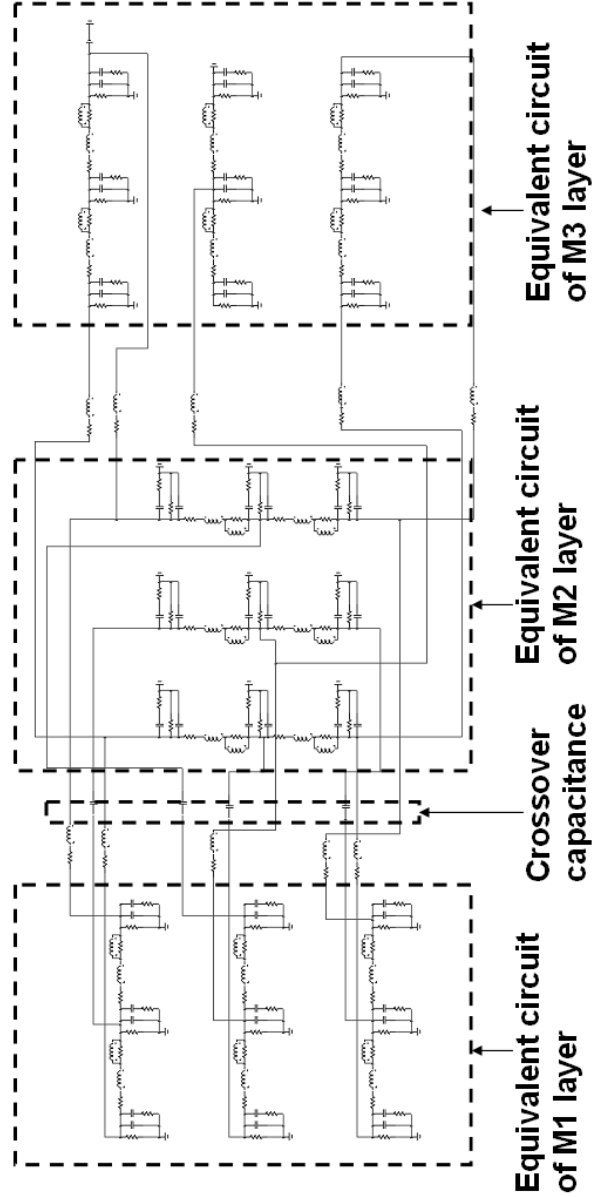


Figure 149: Equivalent circuit of a three-layer power grid

Table 11: Impedance parameters of a three-layer 3-D power grid

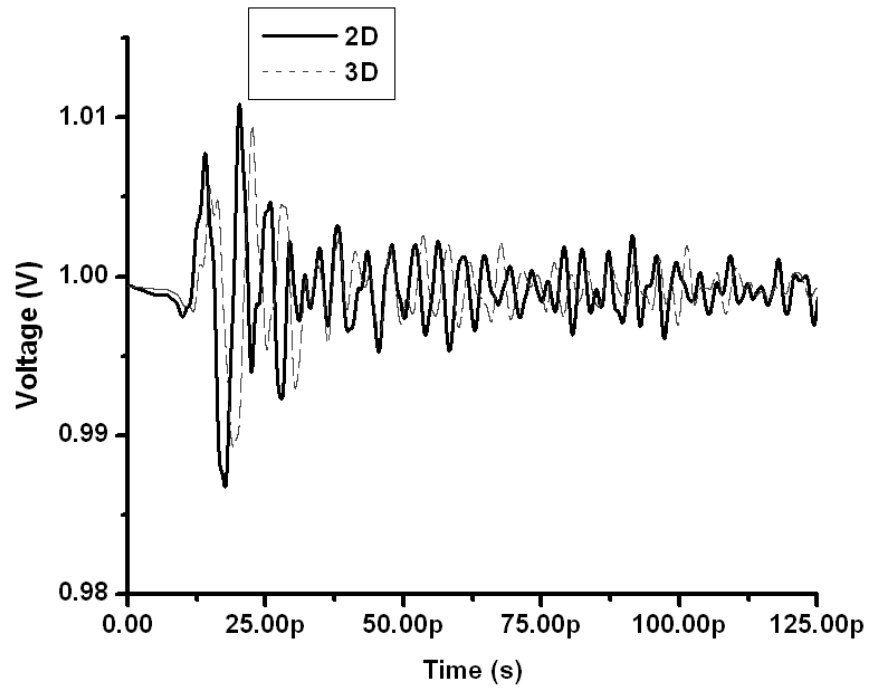
	$R_{dc}(\Omega/m)$	$L_{ext}(H/m)$	$R_1(\Omega/m)$	$L_1(H/m)$
M1	2.5610×10^4	6.6238×10^{-7}	1.0587×10^2	1.2849×10^{-5}
M2	1.2980×10^4	5.8990×10^{-7}	3.2747×10^2	1.1790×10^{-5}
M3	3.0867×10^1	4.3336×10^{-7}	1.6920×10^1	1.7890×10^{-5}

Table 12: Admittance parameters of a three-layer 3-D power grid

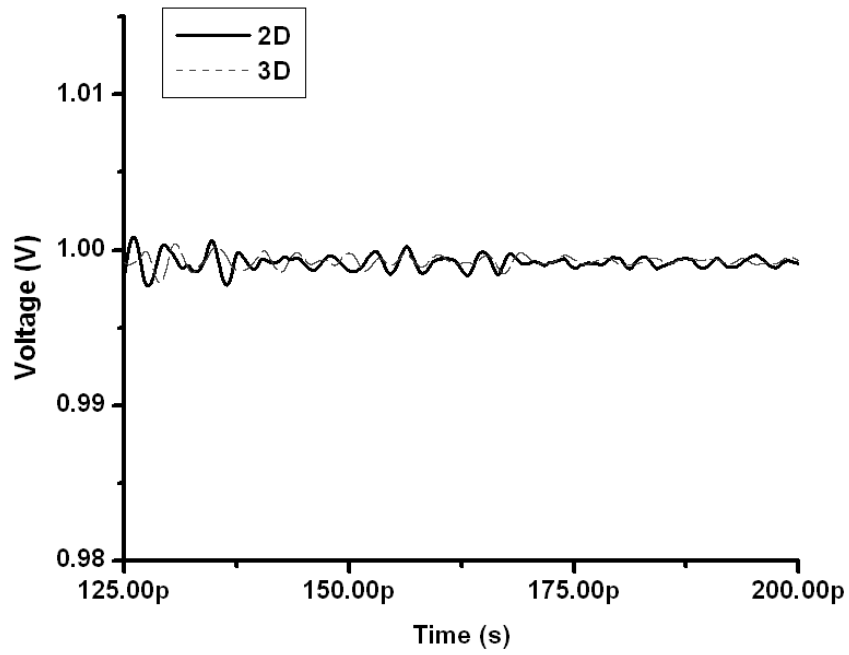
	$C_{ext}(F/m)$	$G_{dc}(s/m)$	$C_1(F/m)$	$G_1(s/m)$	$C_{crossover}^{To_next_layer}(F)$
M1	2.5098×10^{-10}	6.254×10^1	8.7163×10^{-11}	1.383×10^{-1}	0.75419×10^{-15}
M2	2.6689×10^{-10}	8.289×10^1	7.423×10^{-11}	2.61×10^{-1}	2.6418×10^{-15}
M3	2.5789×10^{-10}	9.346×10^1	3.8692×10^{-11}	3.65×10^{-1}	N/A

The waveform on a node 1 mm away from the switching source at the bottom layer has been observed. The simulation result has been compared between 2-D and 3-D power grid with the same geometry in Fig. 150, yet the upper silicon substrate, Silicon_{second}, is absent in 2-D power grid. The frequency dependent RLGC models of 3-D power grid for all the layer are listed in Table 11 and 12. The discrepancy of the noise shown in Fig. 150 indicates the noise performance of 3-D integration. Since the top substrate of 3-D ICs introduces one more virtual ground over the interconnect than 2-D configuration, it has relatively larger capacitance, which delays the switching noise. At the same time, the smaller peak-to-peak noise magnitude of 3-D integration is attributed to two factors: 1) 3-D integration provides less loop/equivalent inductance and, 2) the eddy current in the top lossy substrate causes larger attenuation.

The above analysis has been extended to a 3-D power grid with 6 metal layers and three silicon substrates, as shown in Fig. 151. In Fig. 151, M1, M2 and M3 layers have the same size as Fig. 148. The pitch of M4, M5, M6 layers are 160, 320, 640 μm and the width of them are 16, 32 and 64 μm , respectively. The frequency dependent RLCG models of M4, M5, M6 layer are listed in Table 13 and Table 14. The schematic of the equivalent circuit is shown in Fig. 152.



(a)



(b)

Figure 150: Time domain waveform of 3D Integration (a) Comparison from 0 to 125ps (b) Comparison from 125ps to 200ps

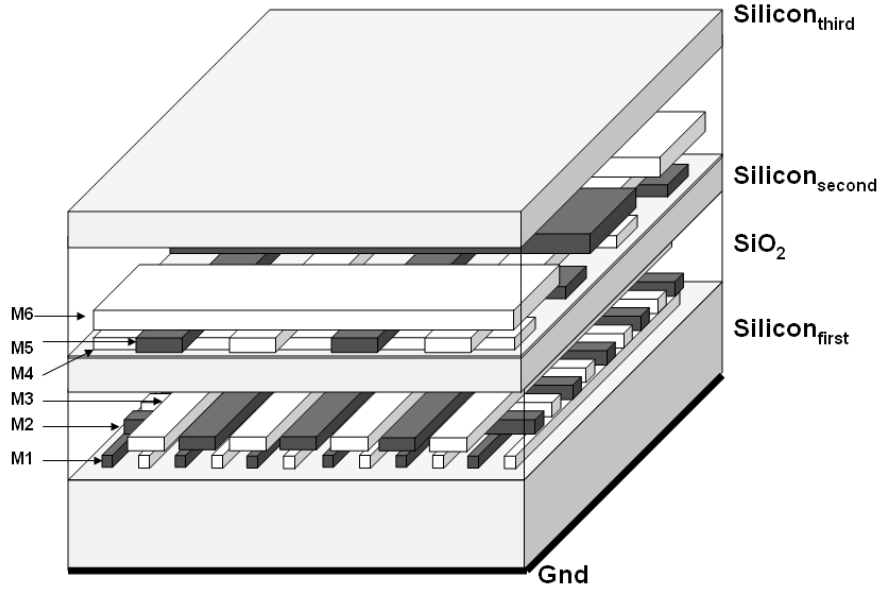


Figure 151: 3-D six layer power grid

Table 13: Impedance parameters of M4, M5, and M6 metal layer

	$R_{dc}(\Omega/m)$	$L_{ext}(H/m)$	$R_1(\Omega/m)$	$L_1(H/m)$
M4	3.3463×10^3	3.8161×10^{-7}	0.43123×10^2	2.4890×10^{-5}
M5	1.8151×10^3	4.0849×10^{-7}	0.37641×10^2	2.7541×10^{-5}
M6	0.8345×10^3	2.2484×10^{-7}	0.0655×10^1	5.5462×10^{-5}

Table 14: Admittance parameters of M4, M5, and M6 metal layer

	$C_{ext}(F/m)$	$G_{dc}(s/m)$	$C_1(F/m)$	$G_1(s/m)$	$C_{crossover}^{To_next_layer}(F)$
M4	4.2323×10^{-10}	0.2104×10^1	8.9875×10^{-11}	4.8732×10^{-6}	42.27×10^{-15}
M5	4.0765×10^{-10}	0.2524×10^1	6.7275×10^{-11}	2.1346×10^{-6}	169.08×10^{-15}
M6	8.0563×10^{-10}	0.23356×10^1	4.7649×10^{-11}	1.4567×10^{-6}	N/A

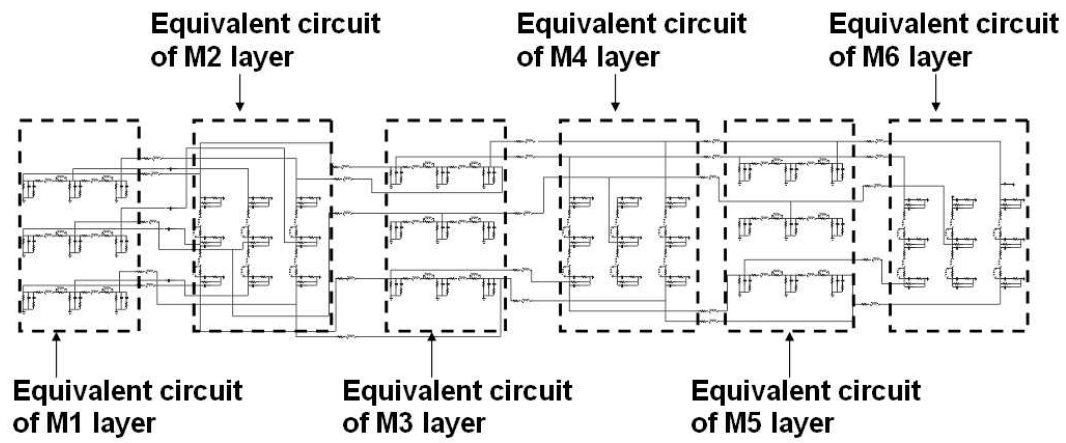


Figure 152: Equivalent circuit of a six-layer power grid

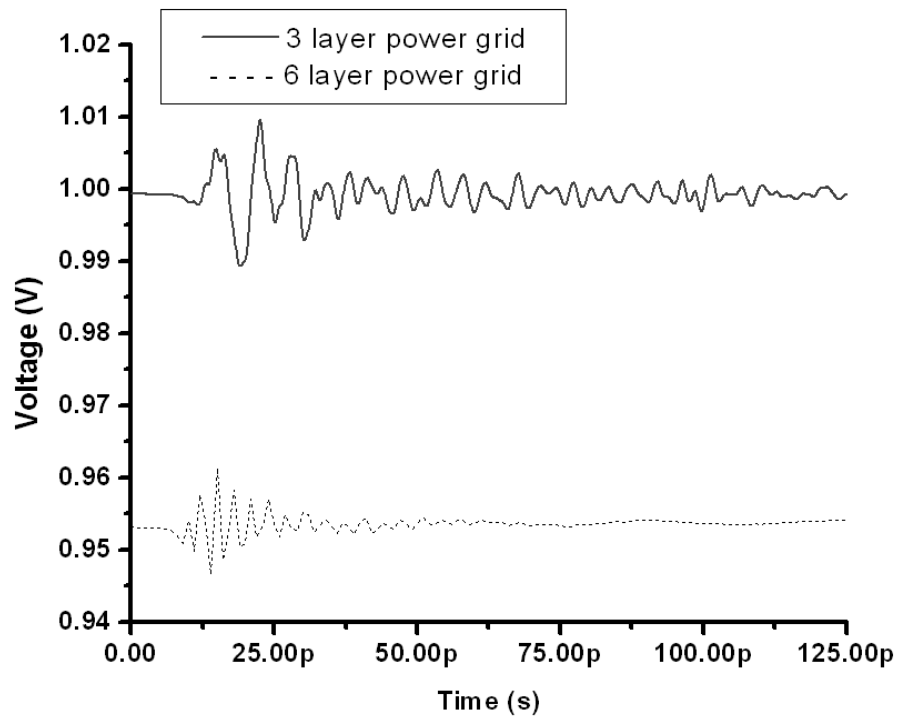


Figure 153: Noise waveform comparison between three and six layer power grid in 3-D IC

The waveform on a node 1 mm away from the switching source at the bottom layer has been observed. The simulation result has been compared between three-layer and six-layer power grid in 3-D ICs, as shown in Fig. 153. The shift of DC voltage of the six-layer power grid is attributed to the IR drop on the top three layers. The smaller peak-to-peak noise magnitude of the six-layer power grid is attributed to the damping effect on the top three layers due to the eddy current in the silicon substrates, Silicon_{second} and Silicon_{third}.

5.4 *Simulation of power grid of 3-D IC with various power densities*

In the previous section, simulation has been carried out for the on-chip power grid of 3-D IC with single noise source. To analyze the realistic IC which has circuits switching simultaneously at different parts of the IC, the power grid of 3-D IC with various power densities has been simulated in this section.

As introduced in Section 3.5, power density $P_{density}$ is a parameter to describe average power consumption of different blocks on the chip. The average current $I_{average}$ drawn by the block during the switching and the peak current I_{peak} can be calculated from power density, which are given by,

$$I_{average} = \frac{P_{density} \times A_{area}}{V_{DC}} \quad (5.28a)$$

$$I_{peak} = 2 \times I_{average} \quad (5.28b)$$

where A_{area} is the area of the block, V_{DC} is the DC supply.

The power grid of 3-D IC as shown in Fig. 151 was simulated with different power densities. The first layer of the chip was divided into thirteen blocks and the top view of the block and their power density is shown in Fig. 154. The coordinates of the bottom-left and top-right corners of each block are listed in Table 15.

The DC voltage supply was 1.0 V and the period of noise source was $T = 4ns$. The simulation was carried out from $t = 0ns$ to $t = 2T$ and the average voltage drop from Vdd to Gnd was calculated using Eq. (3.19). The top view and side view of average voltage fluctuation are plotted in Fig. 155 and Fig. 156 using MATLABTM, respectively. In Fig. 155 and Fig. 156, the area with blue color has the minimum voltage, which indicates that

higher power density block draws more current from power supply and has more voltage drop. On the other hand, the area with red color has the maximum voltage, which indicates that lower power density block draws less current from power supply and has less voltage drop.

Table 15: Coordinates of the blocks with different power density in 3-D IC

	Bottom-left corner		Top-right corner		Power density (mW/mm ²)
	x (mm)	y (mm)	x (mm)	y (mm)	
Area1	0	0	0.8	0.8	90
Area2	0.8	0	1.6	1.6	210
Area3	1.6	0	2.4	1.6	150
Area4	0	0.8	0.8	2.4	250
Area5	2.4	0	4	0.8	70
Area6	2.4	0.8	4	1.6	130
Area7	0.8	1.6	2.4	2.4	50
Area8	0	2.4	0.8	4	230
Area9	0.8	2.4	2.4	3.2	190
Area10	0.8	3.2	1.6	4	110
Area11	1.6	3.2	3.2	4	170
Area12	2.4	1.6	3.2	3.2	210
Area13	3.2	1.6	4	4	90

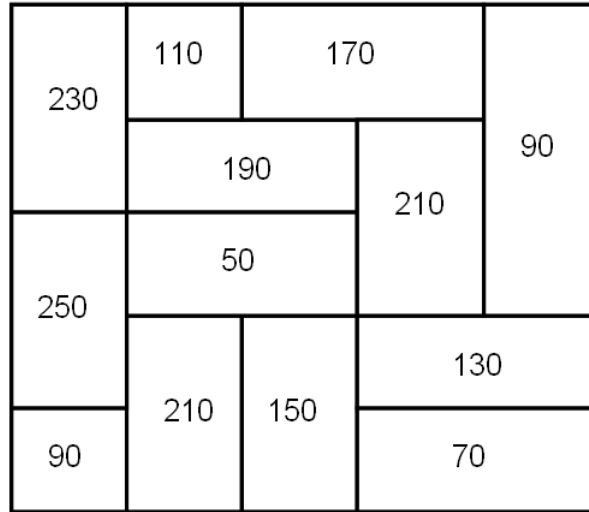


Figure 154: Chip divided in to thirteen blocks with various power density (unit= mW/mm^2)

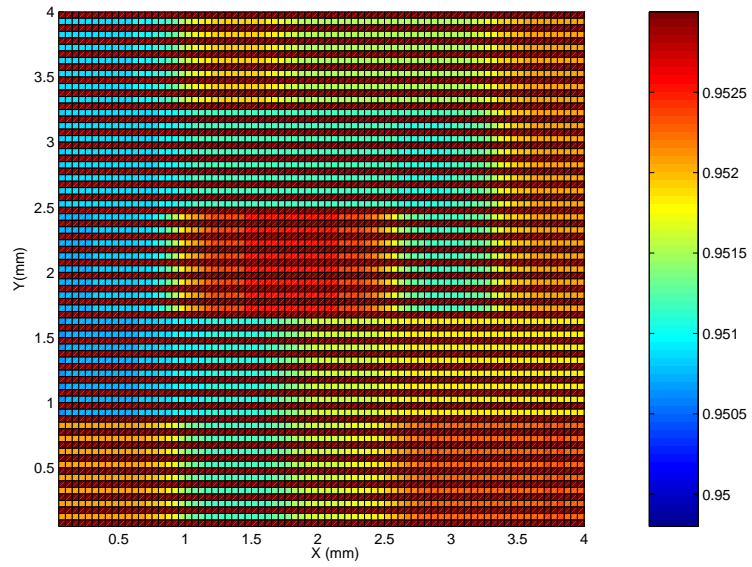


Figure 155: Top view of voltage fluctuation on power grid of 3-D IC

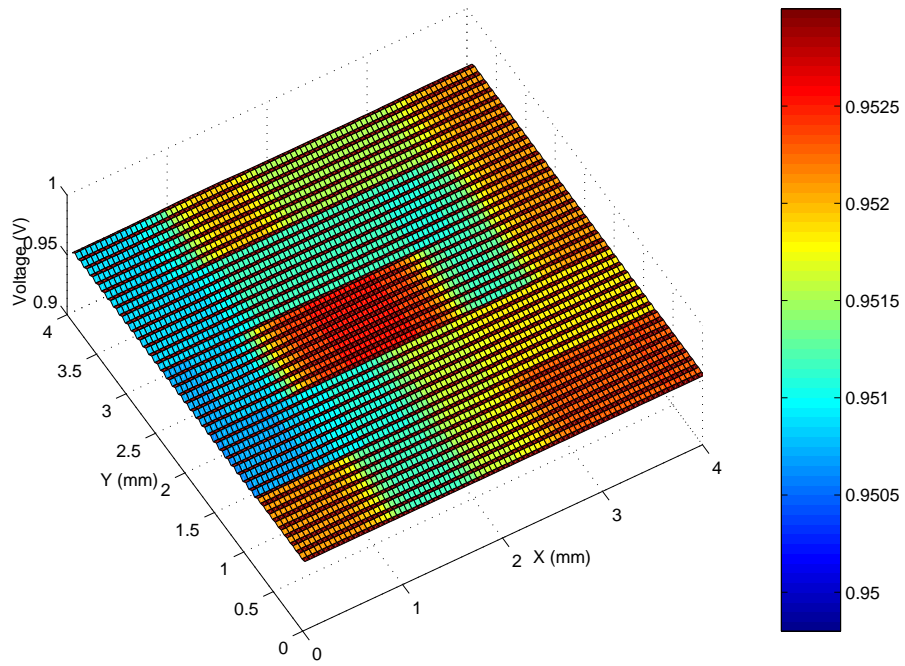


Figure 156: Side view of voltage fluctuation on power grid of 3-D IC

5.5 *Summary*

This chapter discusses the modeling and simulation of 3-D on-chip power distribution networks. Firstly, the complex image technique has been extended from microstrip-type interconnects to stripline-type interconnects. Macromodel images are derived with close form expressions to capture the loss mechanism of the dual conductive substrates. Secondly, the macromodel images are applied on symmetric 3-D interconnect as well as asymmetric 3-D interconnects, for which symmetric stripline and asymmetric stripline models are used. Analytical solutions are achieved by combining lossless stripline model with complex image techniques for 3-D integration. Afterwards, the coupled N 3-D interconnects have been modeled as $2N$ coupled microstrips with the complex distance between the interconnects and their images. Equivalent $N \times N$ matrices are obtained from $2N \times 2N$ matrices by going through a matrix reduction procedure. Finally, the effect of 3-D integration on the switching noise and power grid is illustrated from the result of a time domain simulation.

The research done in this chapter explores electrical performance of the on-chip power grid for 3-D integration. It provides electromagnetic models for power/ground buses, which takes into account the effect of multiple lossy substrates and layout information, such as symmetric/asymmetric single interconnect and coupled interconnects. The solution contains the closed form expressions whose accuracy has been verified. Thus, the proposed approach can be readily incorporated into the pre-layout design for 3-D integrated chips with the focus on power integrity analysis and diagnosis.

CHAPTER VI

CONCLUSION AND FUTURE WORK

6.1 Conclusions

In this dissertation, efficient methodologies are presented for characterizing the coupling mechanism in multilayered electronic package and characterizing the electromagnetic behavior of the on-chip power grid. With the proposed techniques, simultaneous switching noise at different levels of the power distribution network can be efficiently analyzed. As a result, the electrical performance of the power distribution system in a high speed electronic product can be predicted before the design is finalized. In other words, power integrity can be checked at the pre-layout design stage. Consequently, the electronic product can be designed with these methodologies to satisfy the power integrity specifications which leads to a shorter design cycle and rapid time-to-market.

The model developed for field penetration in Chapter II captures the effect of the magnetic field penetrating through planes in multilayered packages. It is an extension of the cavity resonator model based on the perturbational solution described in Chapter II. The effects of penetrating fields have been computed both in the frequency and time domain. The correlation between measurement and computation demonstrates the validity of the approach. It has been illustrated that large amount of switching noise can be coupled in the steady state. Methods to reduce this noise are illustrated by investigating the effect of the thickness of planes as well as the conductivity of the metal. The model developed has an analytical representation, and hence can be applied on multiple plane pairs with relative ease.

Analytical model for the extraction of the interconnect parasitics for a regular on-chip power grid has been presented. Complex image technique has been applied for modeling the dispersive interconnect on lossy silicon substrate. The combination of CIT and the closed form expressions generates an accurate model for coplanar waveguide, which has

been correlated with measurement data. The same modeling procedure has been extended to coplanar multi-conductor lines over silicon substrate and analytical expressions have been derived for CMC structure using conformal mapping technique. The procedure for extracting the frequency dependent RLGC parameters has been explained in Chapter III.

The Debye rational approximation has been used to approximate the RLGC parameters in order to simulate the frequency dependent elements in the time domain. The model of the entire chip power grid has been constructed using first order Debye approximation for each segment of the power/ground buses. The simulation of the entire network of the full-chip power grid has been carried out using the modified FDTD expressions. The on-chip simultaneous switching noise was simulated as a function of location and time. The effect of substrate loss on switching noise in on-chip power distribution network has been quantified by comparing the SSN on the substrates with different resistivity.

Several aspects of characterizing the generic on-chip power distribution network have been presented. The capacitive coupling between adjacent layers of an on-chip power grid has been captured by incorporating the crossover capacitance with the other parts of the power grid model. The crossover capacitance has been evaluated using analytical model derived from conformal mapping, for which the effect of neighboring interconnects and fringing distance are studied for efficiently evaluating the crossover capacitance. An analytical model has been proposed to extract parameters of on-chip multi-conductor transmission lines, which guarantees the stability and is applicable to general distribution of multi-conductor transmission lines. It generates self- and mutual circuit elements in the form of $N \times N$ matrices, for which reduction is used to achieve the equivalent RLGC parameters. The effect of the thickness of the conductor is included as an augment to the R and L parameters. Using the analytical model for general layout, the effects of every alternate layer on the model of on-chip bus as well as the noise performance of irregular power grid have been investigated. The above modeling procedures have been incorporated into a computer program, which generates the power grid model from the layout of chip power distribution networks automatically.

Regarding the research on 3-D on-chip power distribution networks, the complex image

technique has been extended from microstrip-type interconnects to stripline-type interconnects. Macromodel images have been derived with closed form expressions to capture the loss mechanism of the multiple conductive substrates. They have been applied on symmetric 3-D interconnect as well as asymmetric 3-D interconnects. Analytical solutions are achieved by combining lossless stripline model with complex image technique. The N coupled 3-D interconnects have been modeled as coupled microstrips by replacing the top virtual ground plane with N image of the interconnect so that the number of lines is changed from N to $2N$. Equivalent $N \times N$ matrices are obtained from $2N \times 2N$ matrices by going through a reduction procedure. The effect of 3-D integration on switching noise has been illustrated in the time domain using examples.

Based on the work presented in Chapter 2 – 5, the contributions of this research can be listed as follows:

1. Developed an efficient model to characterize the mechanism of field penetrating through power/ground planes.
2. Developed analytical model for regular power grid. This model includes the effect of substrate loss and periodic geometry by using complex image and conformal mapping techniques.
3. Adopted first-order Debye rational approximation for modeling and simulating frequency dependent transmission line parameters. Circuit based FDTD has been modified to include the first order Debye circuit model for entire on-chip power grid simulation.
4. Developed analytical expressions for evaluating crossover capacitance using conformal mapping technique. The effect of neighboring interconnects on the crossover capacitance and the fringing distance have been investigated.
5. Developed analytical expressions for extracting transmission line parameters of generic power grid with non-periodic layout.

6. Developed analytical model for on-chip power bus which includes the effect of alternate metal layers on either side of the multi-conductor transmission lines.
7. Investigated and illustrated the effect of simple non-periodic layout of power grid on simultaneous switching noise.
8. Developed a software program to generate the on-chip power grid model automatically from the layout information.
9. Developed analytical expressions to characterize different kinds of interconnects used in 3-D integration by extending the complex image technique to stripline-type structures. The effect of 3-D integration on noise performance has been illustrated.

6.2 Publication

The following publications have resulted from this research:

- J. Mao, J. Srinivasan, J. Choi, N. Do, and M. Swaminathan, "Computation and effect of field penetration through planes in multi-layered package power distribution networks for giga-processors," IEEE 9th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 43–46, Oct. 2000.
- J. Mao, J. Srinivasan, J. Choi, N. Do and M, Swaminathan, "Modeling of field penetration through planes in multi-layered packages," IEEE Trans. Advanced Packaging, vol. 24, pp. 326–333, Aug. 2001.
- J. Choi, J. Kim, J. Mao, J. Choi, S. Chun and M. Swaminathan, "Enabling reliable systems through ground bounce predictions," 2001 Mixed Signal Integrity Workshop, Atlanta, April. 2001.
- W. Kim, R. Madhavan, J. Mao, S. Choi, D. Ravi, V. Sundaram, S. Sankaravaman, P. Gupta, Z. Zhang, M.Lyer, G.lo, M. Swaminathan, R. Tummala, C. P. Wong, M. Rotaru and A Tay, "Electrical design of wafer level package on board for gigabit data transmission," Proc. of 5th Electronics Packaging Technology Conference, pp. 150–159, Singapore, Dec. 2003.

- J. Mao, M. Swaminathan, J. Libous and D. O'Connor, "Effect of substrate resistivity on switching noise in on-chip power distribution networks," IEEE 12th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 33–36, Oct. 2003.
- J. Mao, W. Kim, S. Choi, M. Swaminathan, J. Libous and D. O'Connor, "Electromagnetic modeling of switching noise in on-chip power distribution networks," Proc. 8th International Conference on Electromagnetic Interference and Compatibility, pp. 47–52, India, Dec. 2003.
- J. Mao, M. Swaminathan, J. Libous and D. O'Connor, "Electromagnetic modeling of on-chip power distribution networks," Proc. 20th Annual Review of Progress in Applied Computational Electromagnetics, April 2004.
- J. Mao, M. Swaminathan and J. Libous, "Distributed modeling of on-chip power distribution networks using conformal mapping and FDTD method", Proc. International Symposium on Electromagnetic Compatibility, Japan, June 2004.
- S. N. Lalgudi, J. Mao and M. Swaminathan, "Modeling and simulation of on-chip power distribution networks," Submitted to 16th International Zurich Symposium on Electromagnetic Compatibility, February, 2005.
- J. Mao, W. Kim, S. Choi, M. Swaminathan, J. Libous and D. O'Connor, "Electromagnetic modelling of switching noise in on-chip power distribution networks," To be published in the Electromagnetic Compatibility Society Newsletter, 2004

6.3 *Future work*

As an extension to the methods described in this dissertation, the following research needs to be investigated:

1. **Including on-chip decoupling capacitor:** The extraction and simulation of the on-chip power grid in this dissertation is carried out without considering the decoupling capacitors. The model for on-chip decoupling capacitor and its effect on transmission line parameters affect the integrity of the model. Hence, on-chip decoupling capacitor

needs to be incorporated with the available model to complete the power integrity analysis.

2. **Exploring totally irregular on-chip power grid:** A simple irregular power grid is studied in this dissertation. However, the irregularity of the power grid can be complex. The power grid for a FPGA IC can be designed without any predictable patterns. Hence, general modeling and simulation methodology is required for totally irregular on-chip power grid.
3. **Including the effect of substrate noise:** The extracted model of power grid takes into account the effect of lossy substrate. However, the propagation of the noise in the substrate or substrate noise is not captured. The substrate noise will be very important in the design of mixed-signal system-on-chip. Therefore, the entire SSN analysis needs to take into consideration the effect of substrate noise.
4. **Including macromodel of on-chip non-linear circuit:** In this dissertation, the switching activity of the active circuits is modeled as a linear current source. It is a simplified model for the non-linear circuits such as core logic gates and I/O drivers. In order to represent the non-linear feature of the active circuits and study the saturation phenomenon of switching noise, the macromodel of non-linear circuit needs to be included as part of the on-chip power integrity diagnosis.
5. **Exploring IC package co-design and co-simulation:** The dissertation breaks down the design of power distribution networks into two separate parts, package and IC, respectively. However, the relentless pressure to quickly deliver designs to market demand a new co-design approach. The biggest challenge in this approach is to make sure the IC-to-package and package-to-board interfaces are designed in consideration of one another. To solve this problem, the co-design of IC, package and board must be performed by firmly linking their distinct design and simulation processes.
6. **Adopting more efficient circuit simulation algorithm:** The circuit based FDTD is adopted in this thesis as a basic simulation algorithm for on-chip power integrity

analysis. Nevertheless, it has its own limitations such as being inefficient at handling coupling elements. Thus, more efficient circuit simulation algorithms need to be considered and adopted.

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