

**HIGH PERFORMANCE RADIO-FREQUENCY AND
MILLIMETER-WAVE FRONT-END INTEGRATED CIRCUITS
DESIGN IN SILICON-BASED TECHNOLOGIES**

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Presented to
The Academic Faculty

by

Jihwan Kim

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Approved by:

Dr. Kevin T. Kornegay, Advisor
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Emmanouil M. Tentzeris
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Chang-Ho Lee
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Geoffrey Ye Li
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Paul A. Kohl
School of Chemical and Biomolecular
Engineering
Georgia Institute of Technology

Date Approved: April 18, 2011

To my wife and two sons

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LIST OF SYMBOLS AND ABBREVIATIONS

AGC	automatic gain control
AM-AM	amplitude-to-amplitude
AM-PM	amplitude-to-phase
BEOL	back-end-of-line
BiCMOS	bipolar and CMOS
BV	breakdown voltage
BV_{CBO}	breakdown voltage when the emitter is open-circuited
BV_{CEO}	breakdown voltage when the base is open-circuited
CDMA	code division multiple access
CG	common gate
CMOS	complementary metal oxide semiconductor
CPW	coplanar waveguide
CS	common source
DA	driver amplifier
DE	drain efficiency
DSB	double-side band
EBR	efficiency back-off ratio
EBR_{achieved}	achieved EBR
EER	efficiency enhancement ratio
EM	electro-magnetic
EVM	error vector magnitude
FCC	Federal Communications Commission
FGCPW	finite ground-plane coplanar waveguide

f_{max}	maximum unity power-gain frequency
FMCW	frequency modulated continuous wave
f_T	maximum transit frequency
GaAs	gallium arsenide
GSM	global system for mobile
HBT	hetero-junction bipolar transistor
HEMT	high electron mobility transistor
HP	high-power
IC	integrated circuit
IF	intermediate frequency
IIP ₂	input-referred second-order intercept point
IIP ₃	input-referred third-order intercept point
IL	insertion loss
IMD ₃	third order inter-modulation distortion
InGaP	indium gallium phosphide
InP	indium phosphide
ISM	industrial, scientific, and medical
LNA	low-noise amplifier
LO	local oscillator
LP	low-power
LPF	low pass filter
LTE	long term evolution
MIM	metal-insulator-metal
MMW	millimeter-wave
MOSFET	metal oxide semiconductor field effect transistor

MP	medium-power
NF_{\min}	minimum noise figure
NF	noise figure
OFDM	orthogonal frequency division multiplexing
$P_{1\text{dB}}$	output referred 1-dB compression point
$P_{1\text{dB_in}}$	input referred 1-dB compression point
PA	power amplifier
PAE	power added efficiency
PAPR	peak-to-average power ratio
PCB	printed circuit board
PCT	parallel-combining transformer
PGS	patterned ground shield
P_{sat}	saturated (peak) output power level
PSCT	parallel-series combining transformer
Q	quality-factor
QAM	quadrature amplitude modulation
RF	radio frequency
SCT	series-combining transformer
SiGe	silicon germanium
SNR	signal-to-noise ratio
SRF	self-resonant frequency
SSB	single-side band
VCO	voltage-controlled oscillator
VNA	vector network analyzer
WCDMA	wideband CDMA

WiMAX	worldwide interoperability for microwave access
WLAN	wireless local area network
WPAN	wireless personal area network

SUMMARY

The wireless communication market has been explosively growing while being fueled by innovative advancements in digital communication/processing technologies along with revolutionary progression in integrated circuit (IC) technologies, manifested both in the speed of the transistors and the complexity of IC systems. The silicon-based process technologies such as complementary metal oxide semiconductor (CMOS) and silicon-germanium (SiGe) are the key driver in the wireless communication IC industry that can enable implementations of fully integrated single-chip transceivers and hence true one-chip systems of mobile terminal devices at low cost. However, developments of high-performance IC blocks and systems overcoming intrinsic vulnerabilities of the silicon-based technologies have been difficult and laborious tasks.

The objective of this research is to explore limitations and challenges of radio frequency (RF) and millimeter-wave (MMW) front-end IC designs using the silicon-based technologies, and to develop effective circuit topologies and design techniques to improve the target performance of the ICs. CMOS power amplifiers (PAs) for high data-rate mobile communications (e.g., WiMAX) and SiGe receiver front-end circuits and systems for 90 to 94 GHz (W-band) long-range wireless accesses are aimed for exploration in this research.

Detailed contents presented in this dissertation are categorized as following:

1. Fundamental limitations of active and passive devices of the silicon-based technologies (silicon CMOS and SiGe) are discussed from the perspective of transceiver IC designs.

2. The design methodology for a multi-mode linear PA fabricated in a 0.18 μm CMOS technology with enhanced low-power efficiency is presented along with thorough analysis on the novel power combining structure. The design technique and procedure to implement a multi-mode (low-power, medium-power, and high-power modes) multi-standard (WLAN and WiMAX) class-AB CMOS PA is discussed. The PA performance at various operation modes is optimized by employing a novel load impedance modulation technique using varactor-based tunable matching networks. These research works will be published in IEEE Journal of Solid-State Circuits (JSSC) in May 2011 [Publication 1]. A part of the research works has been presented in IEEE Radio Frequency Integrated Circuits (RFIC) Symposium in 2010 [Publication 2].

3. A new type of power combining transformer, which is appropriate for high-power (i.e., greater than 33-dBm output power) PA applications, is introduced. The proposed transformer performs the parallel (current) combining and the series (voltage) combining simultaneously in a single structure, supplementing drawbacks of conventional types of power combining transformers. The class-AB PA with the proposed combining transformer is implemented in a 0.18 μm CMOS technology, achieving a $P_{1\text{dB}}$ of 31.5 dBm and a P_{sat} of 34 dB with a peak PAE of 34.9%. Measurement results show the effectiveness of the proposed PA structure for high-data rate wireless communication standards such as WiMAX. The result of this research work is submitted to IEEE Journal of Solid-State Circuits (JSSC) and is under review [Publication 3].

4. The design methodologies for W-band (90 to 94 GHz) receiver building blocks such as a low-noise amplifier (LNA), a balun (balanced-to-unbalanced), a mixer using a SiGe technology is presented focusing on performance optimization techniques. Detailed design procedures for individual circuits are discussed with supportive simulation and measurement results. An integrated receiver system is also implemented in a 200-GHz- f_T SiGe technology, achieving a maximum conversion gain of 36.3 dB and a minimum noise figure of 10 dB at 91 GHz. The designed receiver demonstrated the highest conversion gain among recently reported receivers built in silicon-based technologies operating beyond 90 GHz. These research works have been presented in IEEE Radio Frequency Integrated Circuits (RFIC) Symposium in 2008 [Publication 4], and published in Electronics Letters in 2009 [Publication 5].

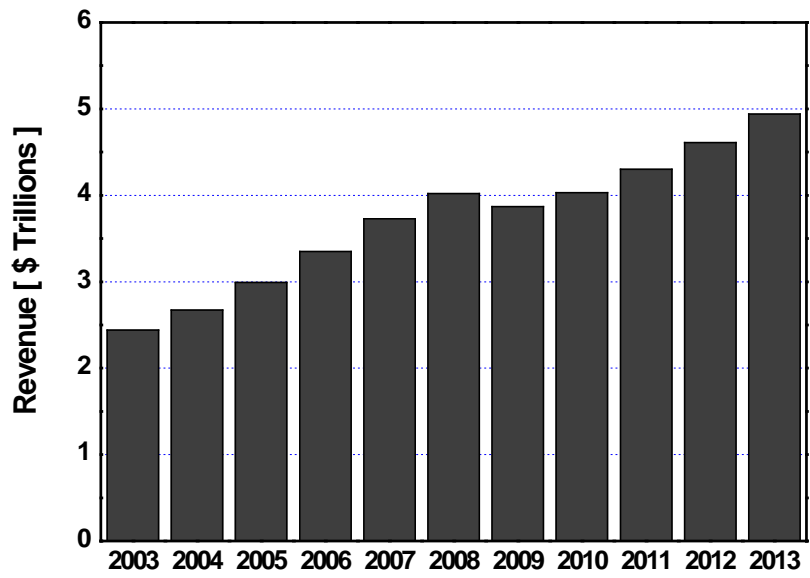
CHAPTER 1

INTRODUCTION

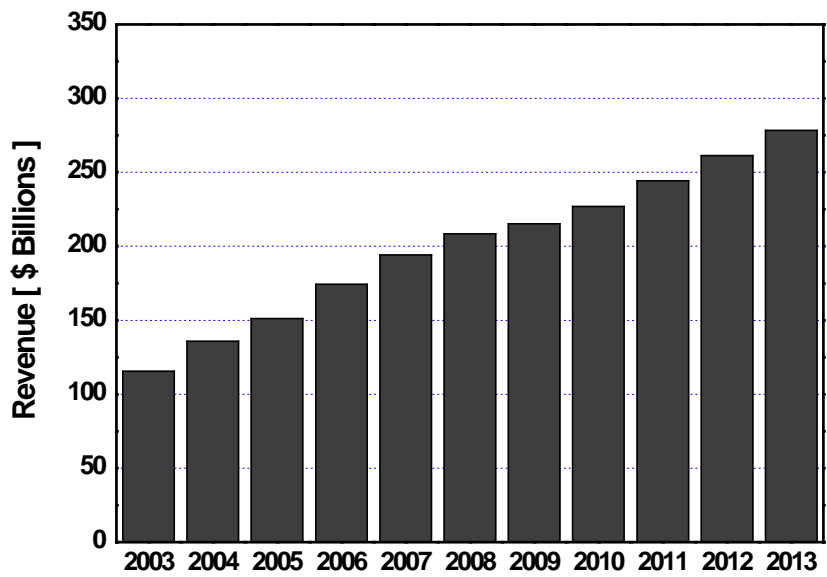
1.1. Wireless Communications

The global telecommunication market has been rapidly growing thanks to advancements in communication theories, digital signal processing, and integrated circuits (ICs) technologies. The revenue for the telecommunication industry is expected to reach \$ 4.94 trillion worldwide and \$ 278.4 billion in the United States by 2013 (Figure 1) [1]. The trend of this remarkable expansion of the wireless communication market is also observed from the fact that the number of wireless subscribers in the United States has become over 90% of the population in 2010 and will grow further to over 95% of the population by 2013 [1]. Undoubtedly, the wireless market is the mainspring of the growing telecommunication industry.

Meanwhile, ever-increasing demands from consumers for broadband wireless communications has accelerated developments of smart mobile devices that adopt various forms of wireless communication standards at radio frequency (RF) bands. Evolved from early generations of wireless communication standards such as global system for mobile (GSM) or code division multiple access (CDMA), more advanced mobile communication standards such as IEEE 802.11a/b/g wireless local area network (WLAN), wideband CDMA (WCDMA), worldwide interoperability for microwave access (WiMAX), and/or long term evolution (LTE) have become available to terminal users for accommodation of high speed data communications. As shown in the graph of Figure 2, data communications will account for about 44% (\$ 93 billion) of overall services spending in



(a)



(b)

Figure 1. Revenue for the telecommunication market. (a) Worldwide. (b) In the United States.

2013 [1]. Inevitably, developments of faster and more reliable mobile communication technologies are desired for manufacturers more than ever to meet the demands of consumers.

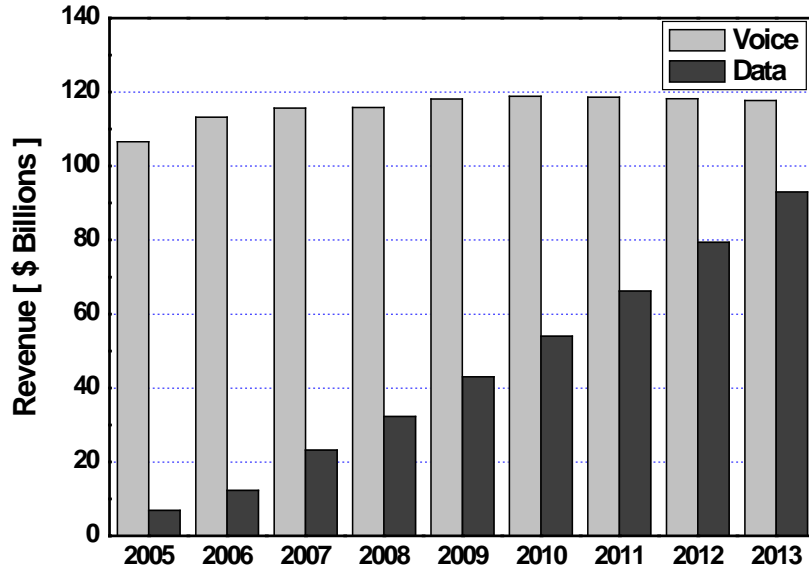


Figure 2. Wireless services revenue by category in the United States.

As frequency resources are being exhausted by competing communication standards at the RF bands, millimeter-wave (MMW) bands (greater than 20 GHz) are getting increasing interests in the telecommunication industry as a breakthrough. Much wider channel bandwidths can potentially realize Gb/s data throughput with a relaxed requirement on spectral efficiency. Promising frequency bands for the broadband next-generation wireless accesses are 59 to 64 GHz in the V-band (50 to 75 GHz), 77 to 79 GHz and 94 GHz in the W-band (75 to 110 GHz). The Federal Communications Commission (FCC) has assigned a spectrum of 59 to 64 GHz, which is called industrial,

scientific, and medical (ISM) band, for general unlicensed purposes [2]. The IEEE 802.15.3.c broadband wireless personal area network (WPAN) [3] and the WirelessHD™ [4] are good examples of emerging applications in the 59 to 64 GHz band. However, the path loss is particularly large at this frequency band due to the absorption lines of the oxygen (e.g., the attenuation of the path is about 20 dB/km at 60 GHz). Therefore, a wireless communication range is limited within a few tens of meters. In contrast, the propagation attenuation is not problematic in the W-band (75 to 110 GHz). Thus, more reliable long-range wireless accesses can be realized. Automotive radars for collision avoidance (77 to 79 GHz), passive imaging for astronomy, defense, or security purposes (94 GHz), and extremely wideband communications (110 to 120 GHz) are potential applications in this MMW frequency range. Various applications at different frequency bands with available process technologies are graphically summarized in Figure 3 [1].

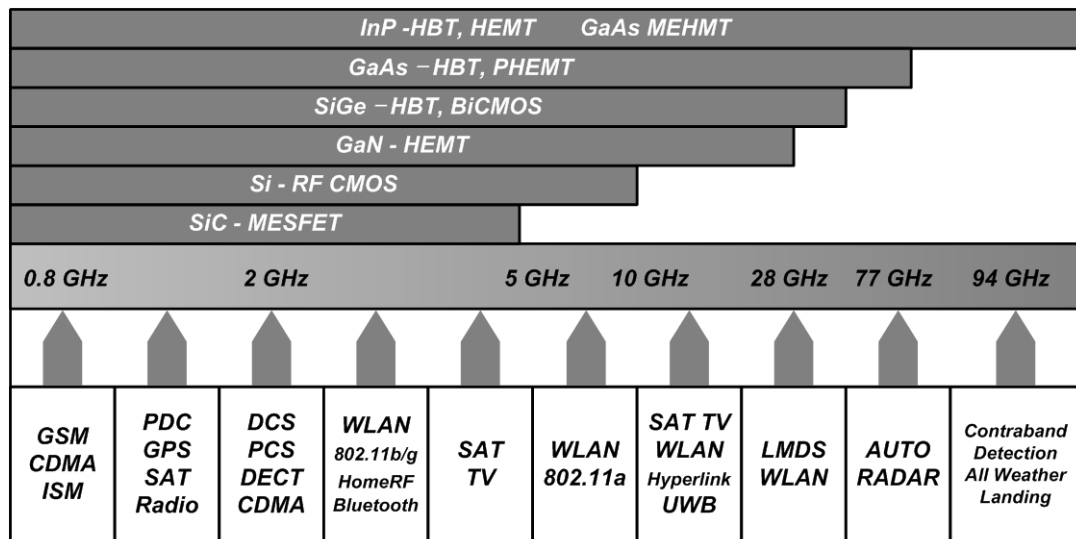


Figure 3. Frequency spectrum and various applications.

1.2. RF and MMW Transceivers

In a mobile communication device, a transceiver (transmitter and receiver) front-end system is the most essential component which is interfacing with physical channels. Although there are diverse digital modulation schemes for various applications invented in recent years, the transceiver architecture has not been fundamentally changed for decades. In a generic homodyne transceiver system, as illustrated in Figure 4, a received signal from an antenna is amplified by a low-noise amplifier (LNA) preserving the signal-to-noise ratio (SNR) as much as possible. Down-conversion is then performed by a mixer to shift down the frequency of the signal to the baseband using a frequency synthesizer as a local oscillator (LO) source. The signal is amplified again by automatic gain control (AGC) blocks and filtered by a low pass filter (LPF) before reaching a

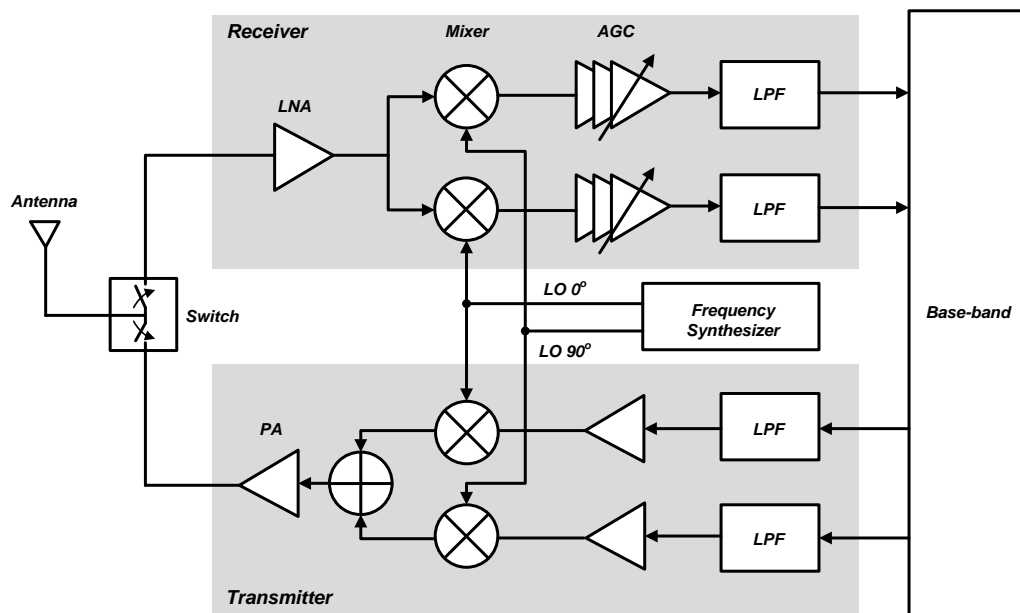


Figure 4. Block diagram of a typical direct-conversion transceiver system.

digital processing unit. The transmitter side consists of almost same functional blocks except for a power amplifier (PA) that transmits the up-converted signal to the antenna at required power level. This structure, so called a direct-conversion transceiver, has been widely adopted to implement RF and MMW wireless communication systems.

1.3. Silicon-Based Technologies for RF and MMW ICs

Full integration of digital, analog, and RF functional blocks has been the ultimate goal of the wireless communication industry for minimization of the manufacturing cost. A true single-chip transceiver implemented in silicon-based process technologies can enable a total integration of all the sub-systems within a mobile terminal device. Complementary metal oxide semiconductor (CMOS) or silicon germanium (SiGe) BiCMOS (bipolar and CMOS) technologies may be great solutions for the full integration of the radio terminal thanks to their low-cost material and good versatility [5]. The silicon wafer costs less than one-fiftieth of that of III-V compound semiconductor technologies such as gallium arsenide (GaAs), indium phosphide (InP), or indium gallium phosphide (InGaP).

Vigorous research and industrial activities to realize the fully integrated CMOS RF front-end systems for various applications have been made in recent years [6]-[8]. Nonetheless, the PA is still left as the biggest bottleneck toward the realization of the single-chip transceiver in a CMOS technology since intrinsic weakness of metal oxide semiconductor field effect transistors (MOSFETs) in terms of linearity and reliability makes the design of CMOS PAs for high-power and high-data-rate applications very challenging [9]-[14]. Therefore, despite of great exertions on improving performances of

the CMOS PAs, III-V compound hetero-junction bipolar transistors (HBTs) or high electron mobility transistors (HEMTs) have been dominating technologies of choice in the PA market as observed from the Table 1 which lists recent PA products for the fourth generation (4G) wireless communication standards such as WiMAX or LTE.

Table 1. Commercial PA products for WiMAX/LTE applications.

Vendor	Model	Freq (GHz)	Gain (dB)	P_{1dB}^* (dBm)	EVM**	Power Supply (V)	Technology
Analog Devices [15]	ADL5571	2.5-2.7	29	29	3% @25dBm	3.3	GaAs HBT
Anadigics [16]	AWM6422	2.3-2.4	30	30	2.5% @22dBm 4% @23.5dBm	3.3	InGaP HBT
SiGe Semicon [17].	SE7262L	2.5-2.7	34	-	-	3.3	SiGe HBT
RFMD [18]	SZM-3066Z	3.3-3.8	33	33.5	2.5% @26dBm	5	InGaP HBT
RFMD [18]	SZA-3044Z	2.7-3.8	-	31	2.5% @24dBm	5	InGaP HBT
TriQuint [19]	TGA2702 SM	2.3-2.8	-	29.8	2.5% @23dBm	6	InGaP HBT
Skyworks Solutions [20]	SKY77441	2.3-2.5	-	-	3.5% @27dBm	3.5	InGaP HBT

* P_{1dB} : output referred 1-dB compression point

** EVM: error vector magnitude

The MMW transceiver front-end circuits and systems have been also developed typically using the III-V compound semiconductor technologies [21]-[26]. With comparative advantages, the III-V technologies have demonstrated their appropriateness in implementations of MMW ICs. In terms of device performances such as a maximum transit frequency (f_T), a maximum unity power-gain frequency (f_{max}), a breakdown

voltage, and the availability of high quality-factor (Q) passives, GaAs/InP/InGaP HBTs/HEMTs are far superior to traditional MOSFETs and/or early generations of SiGe HBTs. However, due to the considerable cost effectiveness and a higher level of integration, the silicon-based technologies have also started attract the MMW IC industry. Along with continuous down-scaling of the technology node, bringing advancements in the speed of transistors, a deep sub-micrometer CMOS or advanced generations of SiGe technologies are becoming plausible options to implement the MMW front-end circuit components as well as the integrated transceivers (Figure 5). With incorporation of innovative design and layout techniques to compensate for the inherent drawbacks and limitations of the silicon substrate and active/passive devices, performances of CMOS/SiGe MMW transceivers and composing circuits are becoming comparable to III-V counterparts [27]-[41].

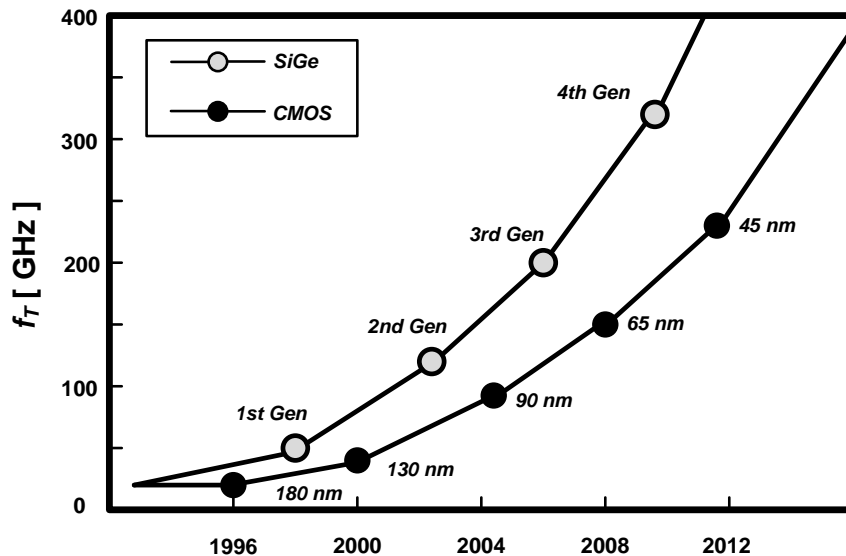


Figure 5. Evolution of CMOS and SiGe technology nodes.

1.4. Motivation

Obviously, the silicon-based technologies are advantageous for the reduced production cost and the higher level of integration of wireless communication systems as mentioned in the previous section. However, many difficulties in designing RF and MMW ICs using CMOS or SiGe technologies, which will be discussed in Chapter 2, still makes III-V compound technologies more suitable for the implementation of high performance front-end circuits. For example, a significantly low breakdown voltage of the MOSFETs and SiGe HBTs compared to GaAs/InP/InGaP HBTs/HEMTs is the most critical obstacle in designing PAs targeting for generation of watt-level output power. Furthermore, a bias-dependent input/output capacitance of the MOSFET is the fundamental drawback which severely limits linearity performance of the circuits. Lossy silicon substrate is also a big design hurdle that constrains implementation of high-quality passive components such as inductors, capacitors, or transmission lines. In the MMW operating frequencies (e.g., in the W-band), these issues become more challenging, and must be effectively handled.

The objective of the research in this dissertation is to explore limitations and challenges of RF and MMW front-end IC designs using the silicon-based technologies, and to investigate effective design techniques to improve the circuit performances. As illustrated in the research outline of Figure 6, the RF band of 2.4 to 2.5 GHz and the MMW W-band of 90 to 94 GHz are aimed for the research.

In the RF band, the PA, the most intricate building block in a transceiver system, is particularly focused to betterment its performance for next-generation wireless communications standards. To accommodate multiple standards and various power

Silicon-based Technologies			
Technologies	<table border="1"> <tr> <td>CMOS</td> <td>SiGe</td> </tr> </table>	CMOS	SiGe
CMOS	SiGe		
Frequencies	<table border="1"> <tr> <td>RF (2.4-2.5 GHz)</td> <td>MMW – W-band (90-94 GHz)</td> </tr> </table>	RF (2.4-2.5 GHz)	MMW – W-band (90-94 GHz)
RF (2.4-2.5 GHz)	MMW – W-band (90-94 GHz)		
Circuits	<table border="1"> <tr> <td>PA, Transformer</td> <td>LNA, Mixer, Balun Integrated Receiver</td> </tr> </table>	PA, Transformer	LNA, Mixer, Balun Integrated Receiver
PA, Transformer	LNA, Mixer, Balun Integrated Receiver		
Features	<table border="1"> <tr> <td> WLAN/WiMAX Dual Standards Multi-Power Mode High-power Linear Applications </td> <td> Highest Conversion Gain among Silicon-Based W-Band Receivers Port-to-Port Isolation </td> </tr> </table>	WLAN/WiMAX Dual Standards Multi-Power Mode High-power Linear Applications	Highest Conversion Gain among Silicon-Based W-Band Receivers Port-to-Port Isolation
WLAN/WiMAX Dual Standards Multi-Power Mode High-power Linear Applications	Highest Conversion Gain among Silicon-Based W-Band Receivers Port-to-Port Isolation		

Figure 6. Research outline.

modes, the PA must support flexible operation conditions with optimized performance. Specifically, a low-efficiency characteristic of the PA at lower output power levels (backed-off power levels from the peak output power level) must be resolved by innovative approaches with a structural view-point. Thus, fully integrated CMOS PAs with a novel combining structure that enables the efficiency optimization in various operation modes are implemented. Thorough investigations and analyses on monolithic transformers are performed as a primary part of the performance enhancement for the PA. Furthermore, a novel power combining transformer, which is suitable for the generation of output power of greater than 33 dBm, is proposed and designed. To demonstrate the effectiveness of the proposed power combining transformer, a fully-integrated high-power (31.5-dBm P_{1dB} and 34-dBm P_{sat}) linear CMOS PA is implemented. This research

attempts to elevate potential appropriateness of a CMOS technology for high-end PA designs (i.e., CMOS PAs for the WiMAX application).

The receiver building blocks; an LNA, a mixer, and a passive balun (balanced-to-unbalanced) for the W-band applications are designed using 200-GHz- f_T SiGe technology. Critical passive structures are electro-magnetically (EM) characterized for an accurate modeling. The integrated W-band receiver chain achieves a very high conversion gain (greater than 36 dB) due to the effective design and layout techniques, which successfully demonstrate the suitability of SiGe technology for the high-performance MMW front-end ICs. Various design hurdles originated from the inherent drawbacks of the silicon-based technology are handled by innovative design techniques with well-optimized design procedures.

1.5. Organization

Based on the motivation described in the previous section, this dissertation is organized for the best presentation of the research achievements as following.

Chapter 2 discusses various issues and challenges of the silicon-based technologies for RF and MMW IC designs. Substrate-related constraints and limitations of passive devices such as inductors, capacitors, and transmission lines are explained. Moreover, intrinsic characteristics of MOSFETs and SiGe HBTs are reviewed from the perspective of front-end circuit designs.

Chapter 3 presents a new power combining and a discrete resizing technique using an on-chip transformer to implement a multi-mode PA in a 0.18 μm CMOS technology. A novel combining structure that maximizes the efficiency of the PA at

lower power modes are introduced with theoretical analysis and experimental data. A load impedance modulation technique to optimize the PA performance at different power modes is also explored.

Chapter 4 introduces a novel power combining transformer structure: a parallel-series combining transformer (PSCT). Using the proposed power combining transformer proposed, a high-power linear PA is implemented in a 0.18 μm CMOS technology. Characteristics and advantages of the proposed transformer comparing to conventional types of monolithic power combining transformers are discussed.

Chapter 5 presents the design methodology of W-band front-end building blocks such as an LNA, a balun, and a mixer using 200-GHz- f_T SiGe technology. Detailed design procedures of MMW circuits to maximize the performance of individual circuit components and an integrated receiver chain are described followed by supporting simulation and measurement results.

Finally, the summary of the dissertation and conclusions is followed in Chapter 6. Future works and directions are also proposed.

CHAPTER 2

CHALLENGES AND ISSUES OF TRANSCEIVER FRONT-END IC DESIGNS IN SILICON-BASED TECHNOLOGIES

2.1. Introduction

The design of RF and MMW transceiver front-end ICs using silicon-based technologies accompanies various challenges and design issues: (1) The conductive substrate raises isolation problems between closely placed active and passive devices, (2) a high quality-factor (Q) for monolithic inductors and transmission lines is not achievable, (3) accurate device models are required as wavelengths of AC signals become comparable to physical dimensions of the devices, (4) parasitic components of active and passive devices must be well-extracted and properly included in actual circuit designs, and (5) constraints on device reliabilities must be carefully considered. Therefore, thorough awareness of limitations of active and passive devices and understanding of parasitic effects on circuit performances at high operating frequencies are strongly required in RF and MMW IC designs using silicon-based technologies. The design procedure becomes an amalgamation of utilizations of various design tools such as schematic simulators for transient or harmonic balance analyses and parasitic extractors or EM simulators for a modeling of secondary parasitic effects on active/passive devices as illustrated in Figure 7.

This chapter introduces typical limitations of silicon-based process technologies from the perspective of RF and MMW IC designs. Isolation issues due to the conductive silicon substrate are discussed in Section 2.2, and constraints of passive components for

high-frequency applications are explained in Section 2.3. Section 2.4 deals with characteristics and intrinsic limitations of active devices (MOSFETs and SiGe HBTs). The conclusion follows in Section 2.5.

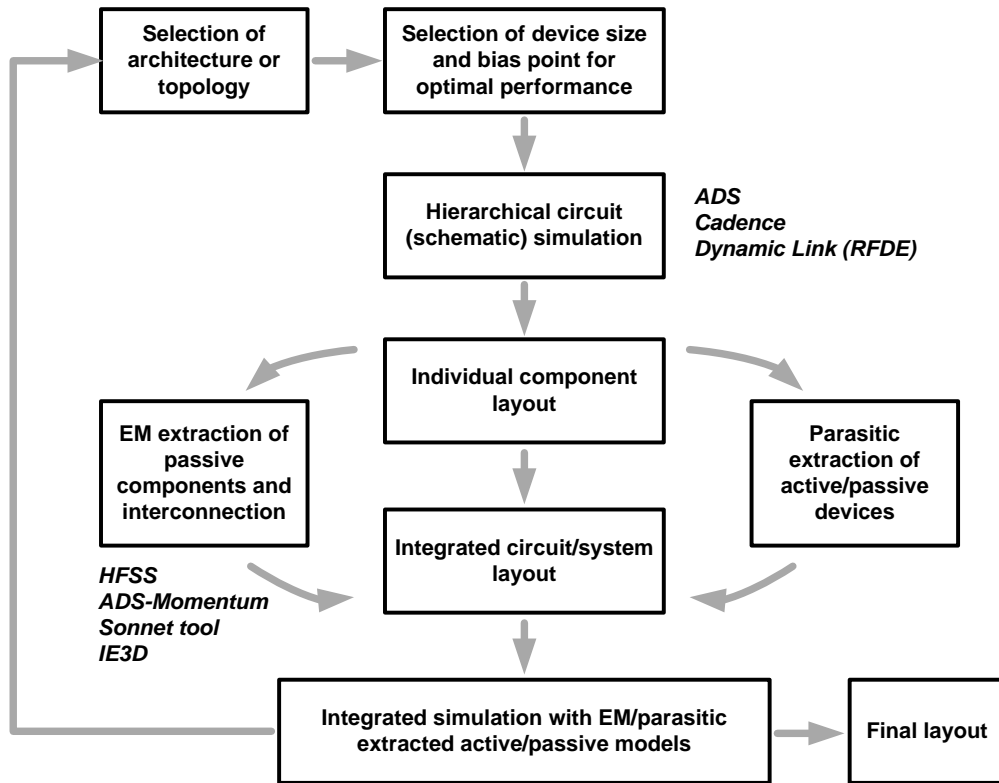


Figure 7. Parasitic-aware design procedure of RF and MMW ICs.

2.2. Issues of Silicon Substrate

A major superiority of III-V compound process technologies such as GaAs or InP to silicon-based technologies such as CMOS or SiGe is their highly resistive low-loss substrate. Due to small dimensions of modern process technologies and a high level of integration, active and passive devices that perform completely different functions are placed very close to each other in state-of-the-art integrated systems. Inevitably, cross-

talks between adjacent functional blocks become critical issues in RF and MMW system designs in which individual building blocks must be well isolated from one another. As presented in the simplified diagram of the silicon substrate in Figure 8, a finite resistance (about $10 \Omega\text{-cm}$) through the p -type silicon substrate associated with oxide and diffusion capacitors introduces non-negligible conductive paths between adjacent active or passive devices. Because of these unwanted signal paths, a serious signal coupling or a noise injection may occur in a highly integrated system that has thousands of transistors acting as critical noise sources. Moreover, large signal swings coming from transceiver front-end blocks such as PAs can be coupled to other critical blocks (e.g., frequency synthesizers or LNAs) that must be absolutely isolated because of their high sensitivity to the noise. In addition, a low resistivity of the silicon substrate provides the RF signals with conductive paths to ground attenuating strength and quality of the signal.

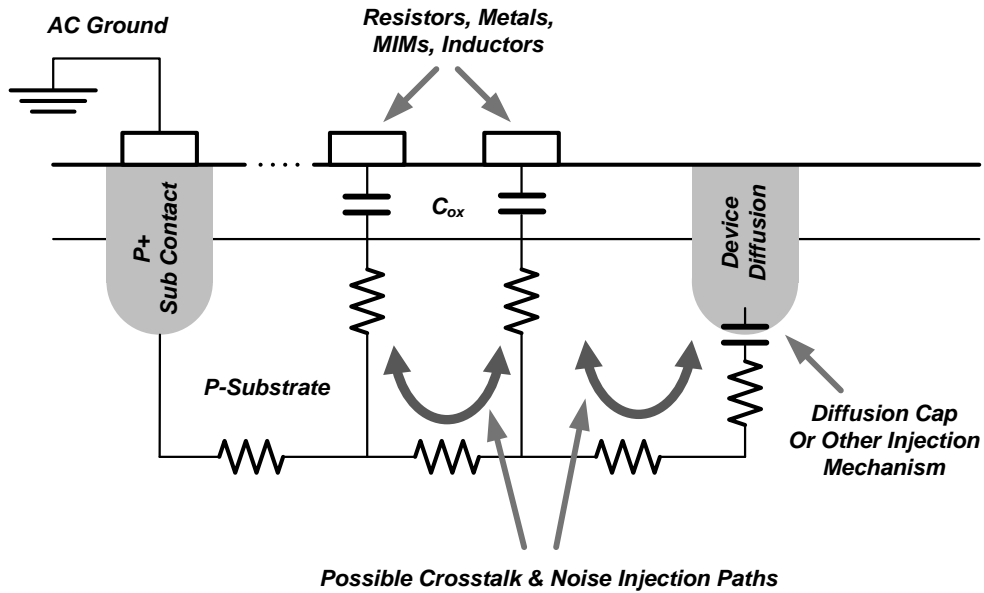


Figure 8. Signal coupling and noise injection in the silicon substrate.

Various techniques can be employed to minimize the unwanted signal coupling and the noise injection through the conductive silicon substrate. For example, guard-rings and deep N -wells in a triple well CMOS process are widely utilized to suppress the cross-talk and improve the signal integrity [42], [43]. Similarly, deep trench (vertical wall) techniques in a SiGe process can effectively enhance the inter-device isolations. In addition, extensive use of substrate contacts that tie up the silicon substrate with ground enables bypassing of the coupled noise to ground with a little penalty of the signal attenuation [44]. However, despite of these attempts, the perfect isolation and the zero signal/noise coupling between adjacent blocks are impossible to achieve. To consider various effects caused by conductive substrate, accurate schematic models of a substrate resistance and a capacitance must be properly included in simulations.

2.3. Limitations of Passive Components

At high frequencies, performances of circuits and systems are strongly affected by limitations of passive components that are functioning critical roles. The most frequently used passive components in RF and MMW designs are spiral inductors, capacitors, and transmission lines. Because of the conductive silicon substrate, complicated loss mechanisms inevitably degrade qualities of the passive components. The quality-factor, Q , of the passive components is defined as the ratio of the amount of energy stored in the component to the amount of energy dissipated per a cycle. Therefore, an expression of the Q can be given as [45]

$$Q = \frac{E_{\text{stored}}}{E_{\text{dissipated}}} = 2\pi \left(\frac{W_m + W_e}{P_e \times T} \right) = \omega \left(\frac{W_m + W_e}{P_e} \right), \quad (1)$$

where W_m is the magnetically stored energy, W_e is the electrically stored energy, P_e is the electrically dissipated energy, and T is the time period of the excited sinusoidal input. As indicated in the (1), the Q of the passive structures is reduced as the magnetic and electrical energy stored within the structure is decreased. In silicon-based process technologies, considerable amount of the EM energy leaks through the lossy substrate, which degrades the Q of the passive components.

2.3.1. Inductors

2.3.1.1. Eddy current

For monolithic spiral inductors, the substrate loss is a critical source of performance degradation [46]. The substrate loss is mainly categorized as a capacitive loss and a magnetic loss. The capacitive loss is due to a voltage difference between the conductor and the grounded substrate that gives rise to a capacitive coupling between them. The magnetic loss is generated by induced currents from penetrating magnetic fields of the conductor into the substrate that cause an extra resistive loss. The substrate eddy current is a dominant source of the substrate loss. As illustrated in Figure 9 [46], a secondary AC current, so called the eddy current, is induced in the substrate in an opposite direction to the conductor AC current. The eddy current, which tends to have a higher current density as the distance between the conductor and the substrate is decreased, generates a negative mutual inductance and reduces the magnetic field of the conductor. Thus, an overall inductance (reactance) of the conductor is reduced, which consequently reduces the Q the inductor. If the substrate has a high conductivity (or a

small resistivity) as in the silicon substrate, a substantial amount of the eddy current is produced and degradation of the inductor's Q becomes a serious issue.

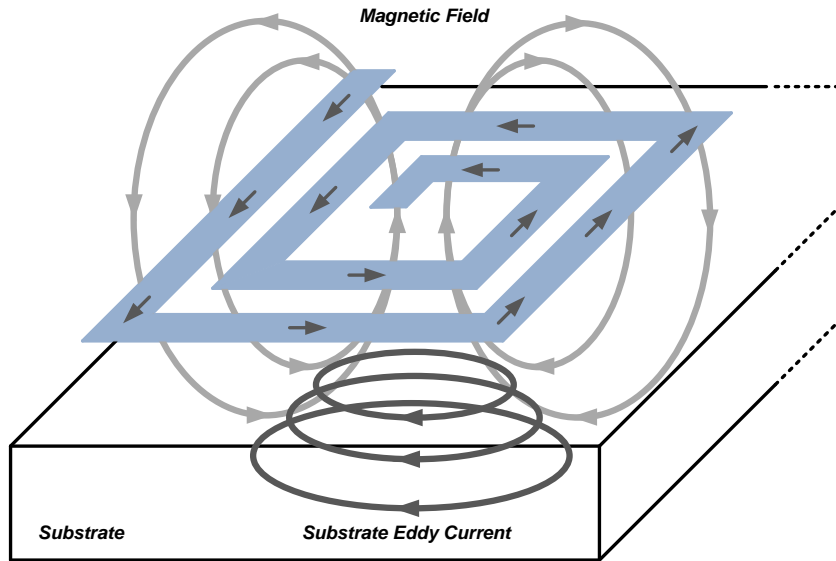


Figure 9. Substrate eddy current generation in the silicon substrate.

The eddy current also introduces an uneven redistribution of the AC current density in metal conductors for monolithic spiral inductors. Figure 10 represents the mechanism of the current density redistribution in a spiral inductor caused by the eddy currents [46]. The time-varying magnetic field produced by outer metal traces (B_{coil}) partially impedes inner metal traces and generates a secondary magnetic field inside the conductor (B_{eddy}) in such a way that both magnetic fields cancel out each other. This secondary magnetic field becomes a source of the circular eddy current in the metal conductor. The inner side of the conductor will have the eddy current that has a same direction as the conductor's AC current, and the current density will be increased. On the

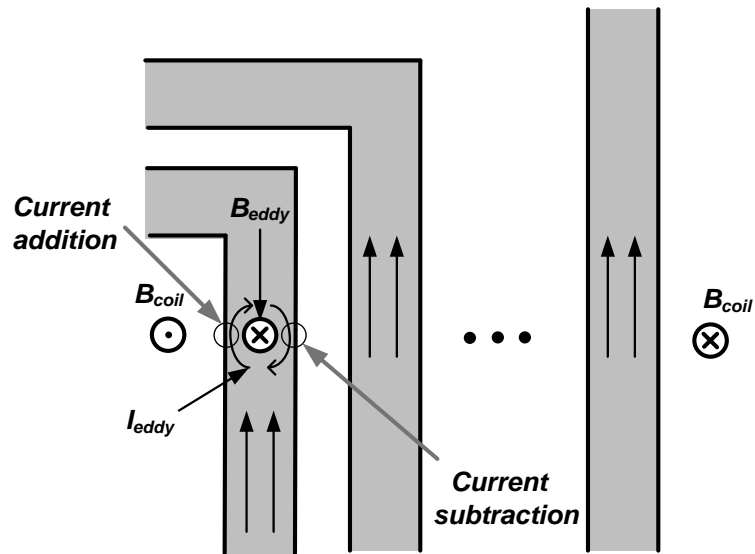


Figure 10. Uneven current redistribution of AC current due to eddy current in a spiral inductor.

other hand, the opposite side of the conductor will have the eddy current with an opposite direction to the conductor's AC current, which reduces the effective current density. Therefore, the current density within a single conductor will be redistributed unevenly enlarging the AC resistance (or RF resistance) of the conductor at high frequencies. This uneven current redistribution puts limitations on implementing on-chip spiral inductors with a large number of turns. Thus, a large effective inductance with a high Q value is not realizable.

2.3.1.2. Proximity effect and skin effect

The proximity effect and the skin effect [47] also introduce AC current density redistributions to the metal conductors. The proximity effect occurs when conductors are placed very close to each other. Neighboring magnetic fields from adjacent conductors interact with the self-magnetic field of the conductor canceling the mutual inductance.

Therefore, a uniform current distribution is disturbed and the effective AC resistance of the conductor is increased. The skin effect is caused by time-varying magnetic fields of the conductor that raises the electric field that impedes the current flowing on the inner side of the conductor. Thus, the surface of the conductor will have a higher AC current density than that of the core of the conductor, and the AC resistance of the conductor is enlarged. The depth below the surface at which the AC current density decays to 1/e (about 0.37) of the current density of the infinitely thick plane conductor is called “*skin depth*”, and is expressed as

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}}, \quad (2)$$

where δ (m) is the skin depth, ρ (C/m³) is charge density, and μ (H/m) is the permeability. To reduce the skin effect, the thickness, the width, and the conductivity of the metal traces must be controlled to minimize the AC resistance. The skin depths of typical metal conductors at the frequency of 10 GHz are summarized in Table 2.

Table 2. Conductivity, resistivity, and skin depth values of commonly-used metals at 10 GHz.

Metals	Conductivity (10 ⁵ s/cm)	Resistivity (10 ⁻⁶ Ω/cm)	Skin Depth (μm)
Aluminum	3.8	2.6	0.817
Copper	5.8	1.7	0.660
Gold	4.1	2.4	0.786
Silver	6.2	1.6	0.640

2.3.1.3. Techniques for inductor Q enhancement

Considering diverse EM effects on the monolithic spiral inductors, the AC resistance (RF resistance) of inductors can be expressed as

$$R_{rf} = \frac{l}{w\rho\delta(1-e^{-t/\delta})}, \quad (3)$$

where l , w , and t are the length, the width, and the thickness of the metal trace, ρ is the conductivity of the metal, and δ is the skin depth as in the (2). In a CMOS technology, various techniques have been utilized to enhance the inductor's Q by minimizing the AC resistance. To reduce the effect of the substrate eddy current, a patterned ground shield (PGS) underneath the metal conductors can be employed as illustrated in Figure 11 [48]. The metal slots in a 90° -shifted to the direction of AC current on the metal traces reduce the eddy current generation in the ground plane and effectively increase the Q of the

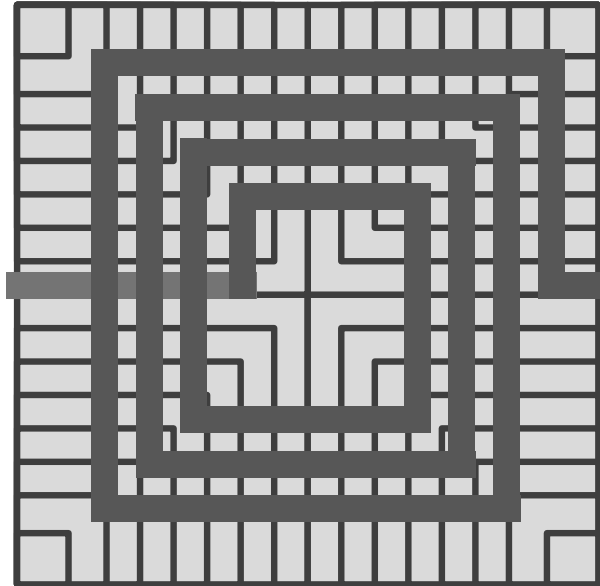


Figure 11. Spiral inductor employing patterned ground shield (PGS).

inductor. However, this technique is not appropriate for high frequency applications because a substantial parasitic capacitance is generated between the conductor and the ground plane, which lowers a self-resonant frequency (SRF) of the inductor.

The uneven redistribution of the AC current density caused by time-varying magnetic fields within a spiral inductor can be mitigated if the inductor has varying widths for metal traces [49]. A strong coupling of the magnetic field from the outer trace to the inner trace will be reduced by relatively narrower widths of the inner metal traces (Figure 12). Multi-stacked spiral inductor is another way to implement high- Q on-chip

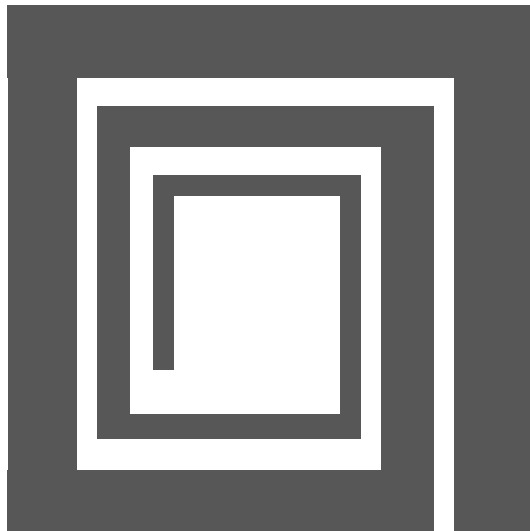


Figure 12. Spiral inductor with varying widths of metal traces.

spiral inductors with a large inductance values as shown in Figure 13 [50]. For example, two spiral inductors on different metal layers can be connected in series such that the AC current can flow in a same direction in two inductors. Thus, the total inductance of the connected inductor becomes

$$L_T = L_1 + L_2 + 2M, \quad (4)$$

where L_1 and L_2 are self inductance of two spiral inductors, respectively, and M is the mutual inductance between two inductors. The coupling coefficient is given as

$$k = \frac{M}{\sqrt{L_1 L_2}}, \quad (5)$$

and the total inductance will be $4L$ if we assume that $k=1$ and $L_1=L_2=L$. In general, a n -stacked inductor can have an inductance of n^2L in an ideal case. However, most of standard CMOS processes do not support multiple thick-metal layers, which limits the usage of this approach.

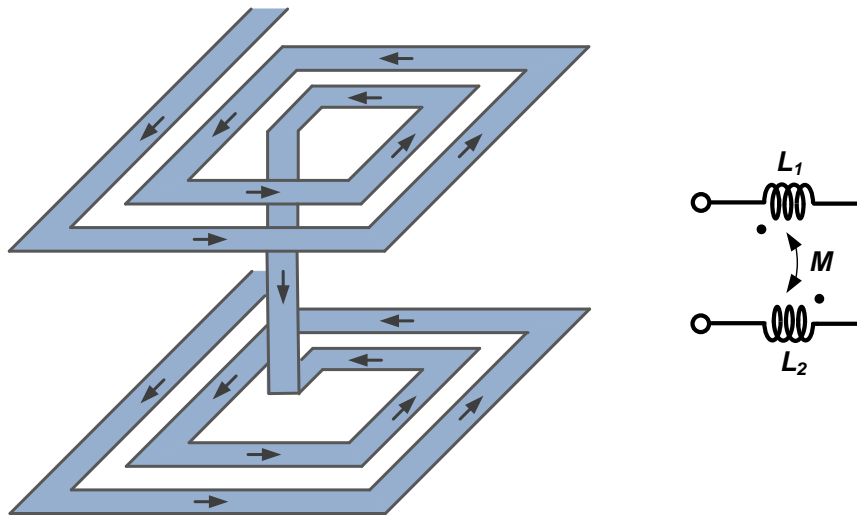


Figure 13. Double-stacked inductor.

2.3.1.4. Inductor model

To reflect various EM effects on inductor performance into the circuit simulation, an accurate equivalent model of the inductor can be used to reduce simulation time and

cost. A commonly used inductor model for the silicon-based process technologies is presented in Figure 14. The model exhibits ohmic resistances and parasitic capacitances. L_S , R_S , and C_S are the self inductance, the series resistance and the capacitance, respectively. C_S accounts for the metal-to-metal capacitance between two input terminals of the inductor that is caused by fringing field between separate metal layers. C_{ox} represents the parasitic oxide capacitance between the conductor metal and the substrate. R_{si} and C_{si} are the series resistance inside the silicon substrate due to finite resistivity. R_{se} accounts for an additional ohmic loss due to the eddy current caused by the magnetic coupling between the spiral inductor metal trace and the low-resistivity silicon substrate. To use the equivalent model of the inductors adequately, experimental verifications are required to determine the appropriate values of each components of the model.

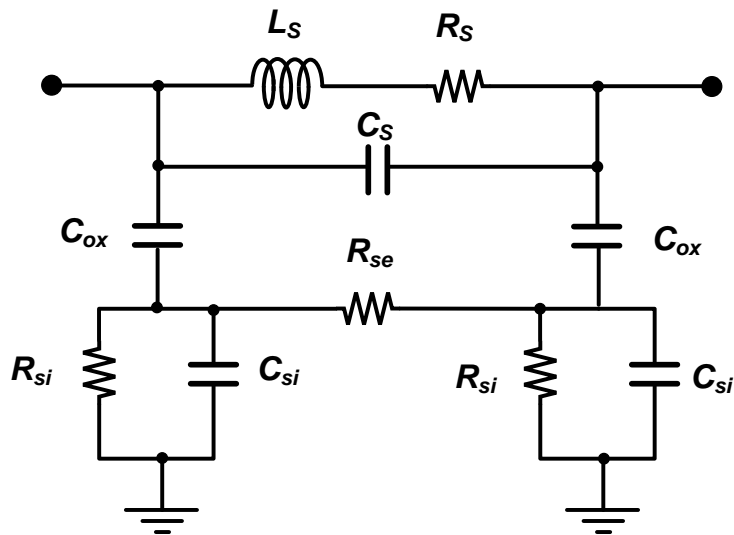


Figure 14. Commonly used equivalent model of a monolithic spiral inductor.

2.3.2. Capacitors

2.3.2.1. Metal-insulator-metal (MIM) capacitor

Monolithic capacitors are mainly classified into three kinds: microstrip capacitors, interdigital capacitors, and metal-insulator-metal (MIM) capacitors. Open-stub microstrip transmission lines can be used to realize a capacitance at MMW frequencies. The interdigital capacitors have applications where moderate capacitance values are needed. The MIM capacitors are the most widely used for RF and MMW IC designs, but they require multi-level process because the effective capacitance is generated between parallel metal planes (or electrodes). All capacitors exhibit a parasitic inductance due to their finite size and series resistance due to contact/electrode resistance. The cross section and the equivalent model of the MIM capacitor in multi-level CMOS/SiGe processes are presented in Figure 15. The parasitic inductance (L_s) associated with the series

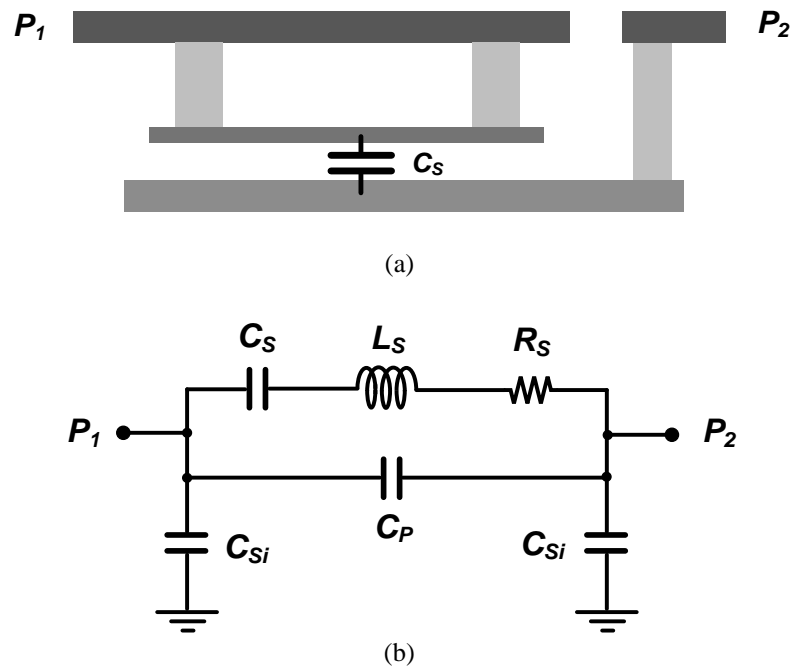


Figure 15. MIM capacitor. (a) Cross section. (b) Equivalent model.

capacitance (C_s), the parasitic parallel capacitance (C_p), and the parasitic capacitance to ground (C_{si}) may form the SRF of the capacitor below the operating frequency, so the size of the MIM capacitor must be carefully determined for high frequency applications.

2.3.2.2. Parasitic extraction of MIM capacitor

Accurate models of the MIM capacitors can be obtained by parasitic extractions or EM simulations. For MMW applications, small capacitance values (a few hundreds of fF) are often required. Thus, a parasitic resistance due to metal contacts and vias may contribute to the insertion loss (IL), substantially degrading the Q of the capacitor. This effect becomes critical if the operating frequency of the application is beyond 60 GHz, where the Q of the capacitor is comparable to that of the inductors. Figure 16 shows difference between a schematic model and a parasitic-extracted model of 100- fF MIM capacitor (IBM 8HP BiCMOS) up to frequency of 110 GHz. For large MIM capacitors,

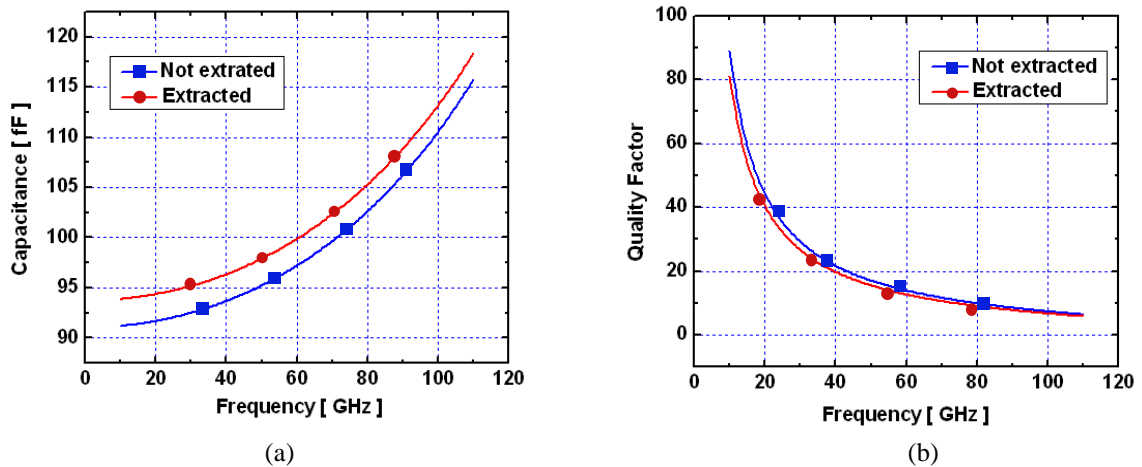


Figure 16. Comparison of MIM capacitor models (100 fF) (a) Capacitance values. (b) Q of capacitors.

long inter-connections also act as inductive transmission lines, and must be EM extracted to be accurately accounted in simulations.

2.3.3. Transmission lines

2.3.3.1. Hybrid-type transmission line

Conventional microstrip transmission lines are widely used for MMW applications. However, absence of ground shields at the top layer complicates an analysis and an accurate modeling of EM characteristics. To take advantages of side ground shields, we can implement a hybrid-type transmission line that is similar to finite ground-plane coplanar waveguide (FGCPW) transmission lines except for the existence of via connections between the side ground shields and the bottom ground plane. The cross section of the hybrid-type transmission line is presented in Figure 17, where W is the width of the top conductor, S is the gap between the conductor and the side ground shield, and H is the distance between the top conductor and the bottom ground plane. Due to the via connections, same potential around all ground shields is ensured. Comparing to the

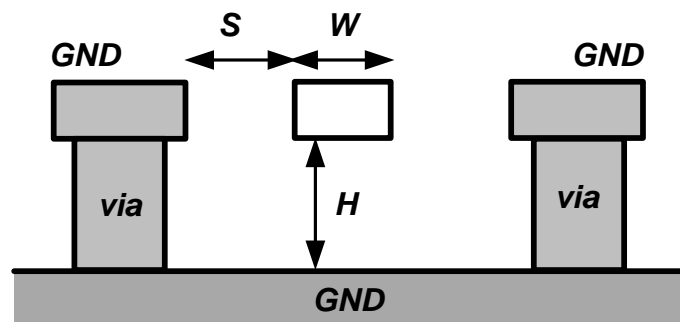


Figure 17. Hybrid-type transmission line.

conventional microstrip transmission lines, the hybrid-type lines support well-confined electric and magnetic fields, so more accurate analyses and computer-aided simulations are possible. These transmission lines can be used for interconnections between active circuits including matching networks, enhancing signal isolations by providing well-defined ground return paths and minimizing an unwanted EM coupling to adjacent structures. Furthermore, they can be easily integrated with active circuits without entailing any parasitic discontinuities in the ground plane.

2.3.3.2. Characteristic impedance

Given geometric parameters, the characteristic impedance of conventional coplanar waveguide (CPW) lines can be calculated letting $a=W$ and $b=W+2S$ as [51]

$$Z_o = \frac{60\pi}{\sqrt{\epsilon_{eff}}} \cdot \frac{1}{\frac{K(k)}{K(k')} + \frac{K(kl)}{K(kl')}}}, \quad (6)$$

where

$$k = \frac{a}{b} \quad (7)$$

$$k' = \sqrt{1-k^2} \quad (8)$$

$$kl' = \sqrt{1-kl^2} \quad (9)$$

$$kl = \frac{\tanh(a\pi / 4H)}{\tanh(b\pi / 4H)} \quad (10)$$

$$\epsilon_{eff} = \frac{1 + \epsilon_r \frac{K(k')K(kl)}{K(k)K(kl')}}{1 + \frac{K(k')K(kl)}{K(k)K(kl')}}}, \quad (11)$$

and $K(k)$ is elliptic integrals of the first kind. Because of the foundry process, H will be fixed parameter ($9.25 \mu\text{m}$ in IBM 8HP BiCMOS technology), whereas other parameters can be chosen arbitrarily. A few examples of characteristic impedances of the CPW lines calculated with varying W and S are presented in Figure 18. Although this calculation is very well approximating the trend of the characteristic impedance with various dimensions, actual characteristic impedance of the hybrid-type transmission line will be different since it has additional vias between the top ground shields and the bottom plane.

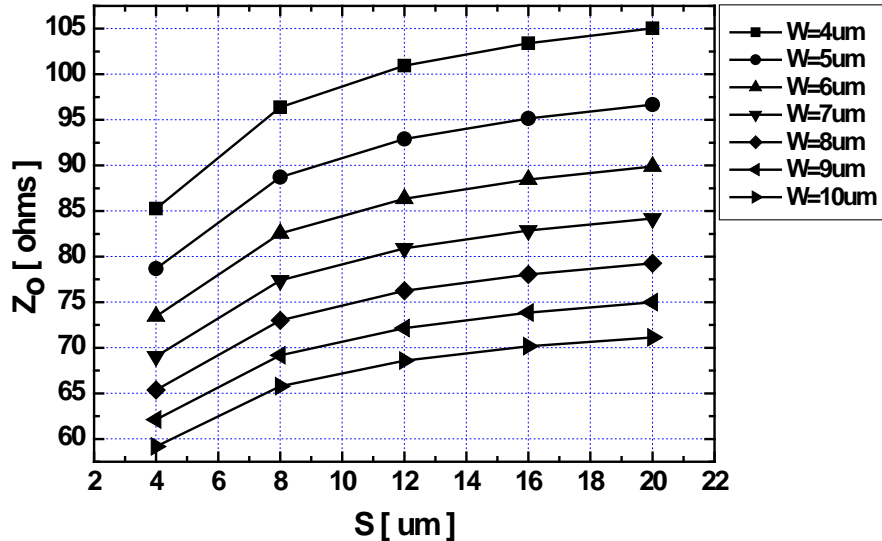


Figure 18. Characteristic impedances of conventional CPW transmission lines ($H=9.25 \mu\text{m}$).

The IBM 8HP BiCMOS process technology provides the hybrid-type transmission line models up to 200 GHz. This process features seven back-end-of-line (BEOL) metal layers with $4\text{-}\mu\text{m}$ -thickness top aluminum metallization. The cross section of the hybrid-type transmission line built on the IBM 8HP BiCMOS process is presented in Figure 19. The design-kit also provides a characteristic impedance calculator.

Characteristic impedances of the transmission lines with various dimensions are obtained using the embedded impedance calculator and are plotted in Figure 20. As observed from the Figure 18 and Figure 20, there is significant difference in calculated characteristic

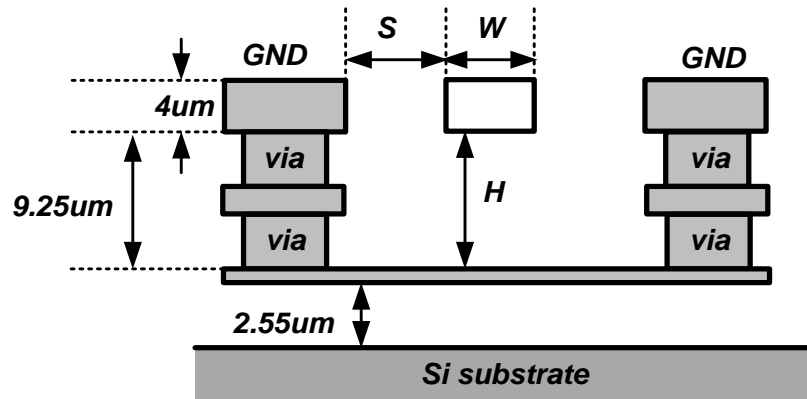


Figure 19. Cross-section of the hybrid-type transmission line in IBM BiCMOS 8HP process.

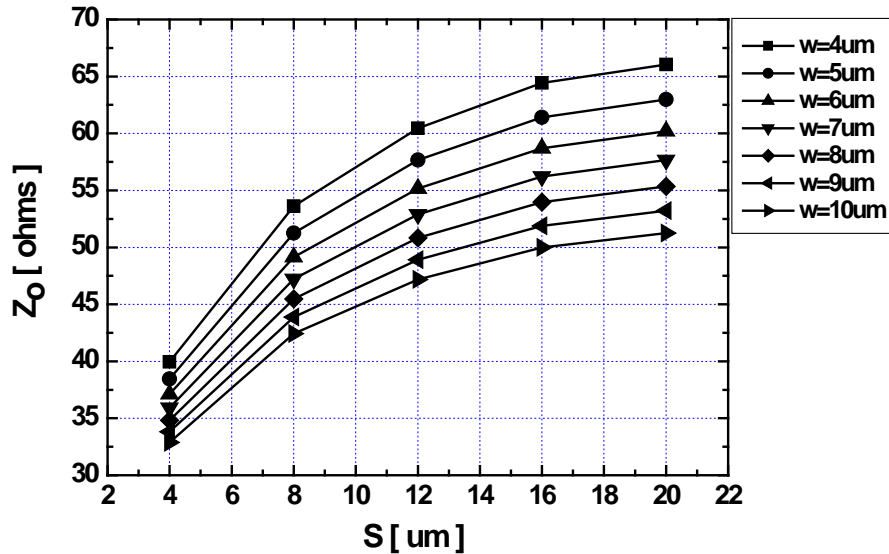


Figure 20. Characteristic impedances of the hybrid-type transmission lines obtained by embedded impedance calculator in the IBM 8HP design kit ($H=9.25 \mu\text{m}$).

impedances even though we consider that Figure 18 is for the conventional CPW transmission lines which do not employ side vias. Therefore, EM simulations are necessary to verify the transmission line models.

The ADS Momentum was used to simulate EM characteristics of the quarter-wavelength hybrid-type transmission line. The line features $W=5 \mu\text{m}$ and $L=300 \mu\text{m}$. The values of S were varied from $4 \mu\text{m}$ to $20 \mu\text{m}$ with a step of $4 \mu\text{m}$. With EM simulated data, characteristic impedance of the transmission line was obtained from S-parameters. As shown in Figure 21, the transmission line with a length of L applied by two ports at each side has two different modes of excitation that are considered. First, in the even-mode case, total signal leaving the port₁ is given by

$$S_e = S_{11} + S_{12} = \frac{z \cdot \coth(\gamma l) - 1}{z \cdot \coth(\gamma l) + 1}, \quad (12)$$

where $l=L/2$, $\gamma=\alpha+j\beta$ (α is attenuation constant and β is a propagation constant), and $z=Z/Z_0$. Therefore, we can have

$$z \cdot \coth(\gamma) = \frac{1 + S_e}{1 - S_e}. \quad (13)$$

Similarly, in the odd-mode case, total signal leaving the port₁ can be expressed as

$$S_o = S_{11} - S_{12} = \frac{z \cdot \tanh(\gamma l) - 1}{z \cdot \tanh(\gamma l) + 1}, \quad (14)$$

and we can obtain

$$z \cdot \tanh(\gamma l) = \frac{1 + S_o}{1 - S_o} \quad (15)$$

Thus, by the (13) and the (15), the complex propagation constant and the characteristic impedance can be calculated as

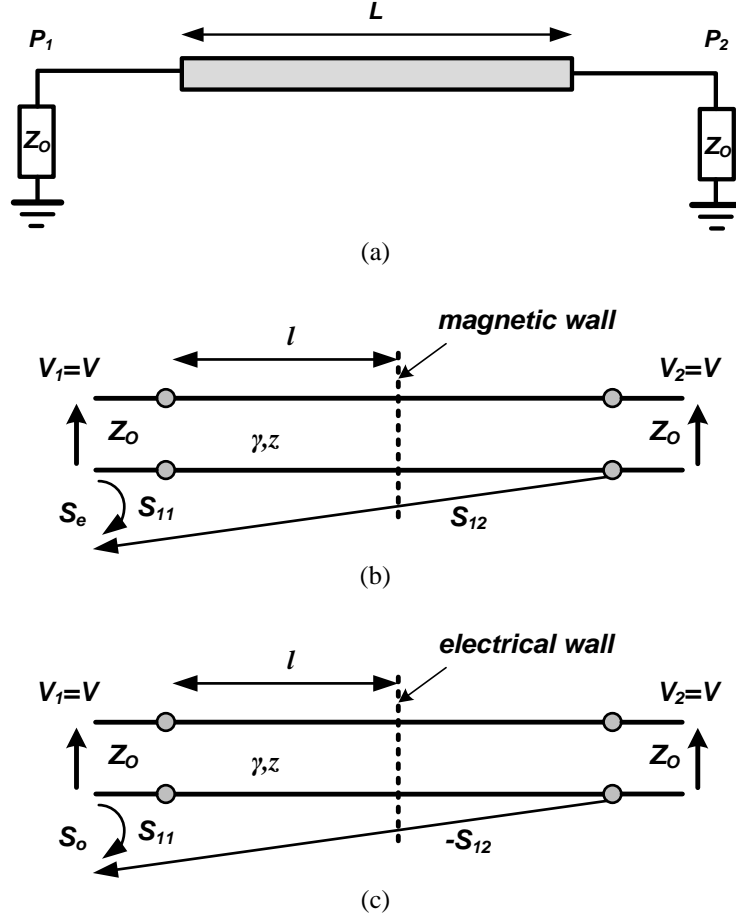


Figure 21. Calculation of the characteristic impedance. (a) A transmission line with length of L . (b) A transmission line in the even-mode. (c) A transmission line in the odd-mode.

$$\tanh^2(\gamma l) = \frac{(1 + S_o)/(1 - S_e)}{(1 + S_e)/(1 - S_o)} \quad (16)$$

$$z^2 = \left(\frac{1 + S_e}{1 - S_e} \right) \left(\frac{1 + S_o}{1 - S_o} \right). \quad (17)$$

Based on these equations, the characteristic impedances of the hybrid-type transmission line models with a length of $300 \mu\text{m}$ (as shown in Figure 22) are calculated and plotted in Figure 23. Because of the side ground shields, the characteristic

impedances for all various dimension parameters have smaller values compared to ones for the conventional CPW transmission lines. The EM model has smaller characteristic impedances for all different values of the distance between the top conductor and the side ground shields. However, this data for the EM model is still different from the data for the model provided by the design-kit. This is because the EM simulator accounts for a fringing capacitance between the signal line and the bottom ground plane to more extent than the impedance calculator in the design-kit does.



Figure 22. 3-D structure of the hybrid-type transmission line in IBM 8HP design-kit.

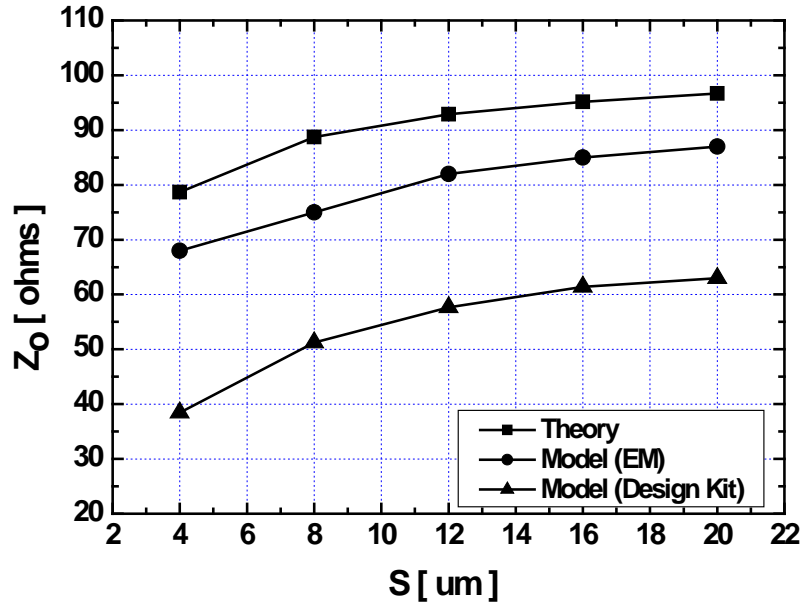


Figure 23. Characteristic impedances of the hybrid-type transmission lines ($L=300 \mu\text{m}$, $W=5 \mu\text{m}$, $H=9.25 \mu\text{m}$).

The scattering parameters (S-parameters) are also simulated to compare two models: the EM simulated model and a model from IBM 8HP design-kit. The quarter-wavelength transmission line is supposed to transform the zero impedance (shorted to ground) to the infinite impedance (open) at the design frequency. As shown in Figure 24, The EM simulated model features a smaller quarter-wavelength frequency compared to the design-kit model. Beyond the quarter-wavelength frequency, the function of the transmission line is changed from the inductive one to the capacitive one as illustrated in Figure 25. We can observe that resistance and inductance values of two models change their polarities at 89 GHz (EM model) and 94 GHz (design-kit model), respectively. It must be considered that the design-kit model shows a more optimistic characteristic in terms of the resistive loss.

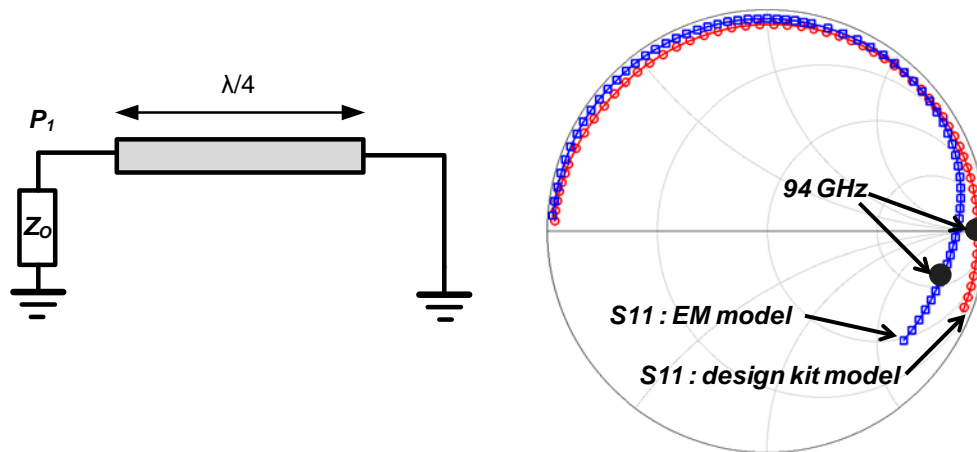


Figure 24. S_{11} of the quarter-wavelength transmission line with ground termination.

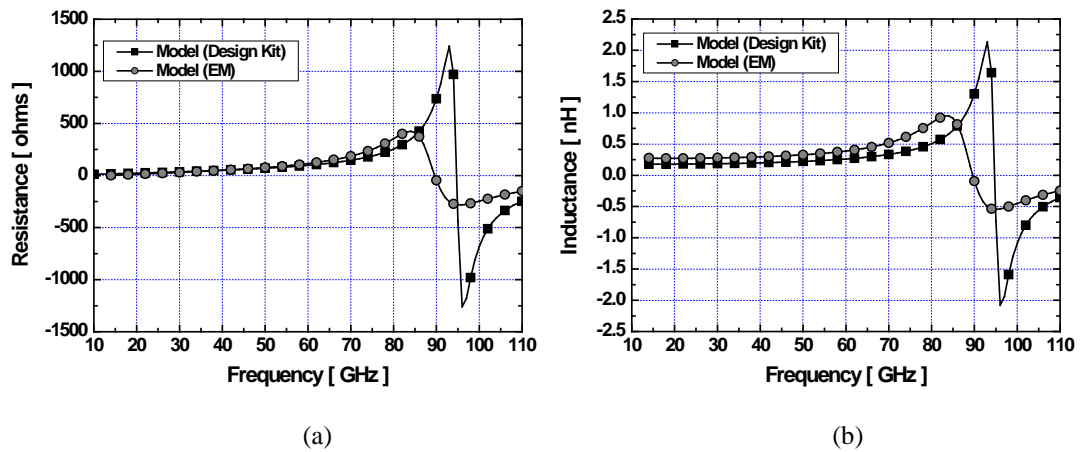


Figure 25. Resistance and inductance of the quarter-wavelength hybrid-type transmission line. (a) Resistance. (b) Inductance.

2.4. Limitations of Active Components

Active devices, or transistors, are the most critical components in circuit blocks. They consume a DC current from external power supplies and perform necessary functions. Important figure-of-merits of active devices includes a transconductance (g_m), a noise factor, a maximum transit frequency (f_T), and a maximum unity power-gain

frequency (f_{max}). Reliability and linearity of the active devices are also important characteristics to be carefully considered for optimal circuit designs. In this section, MOSFETs are reviewed from the perspective of the transconductance, reliability, and linearity characteristics, and SiGe HBTs are discussed in terms of a noise, a speed, and reliability characteristics. Circuit designers must thoroughly understand these characteristics and limitations of different active devices to appropriately determine right design environment for specific target applications.

2.4.1. MOSFETs

2.4.1.1. Transconductance

The fundamental function of active devices is amplifying the signal with a finite gain. The transconductance, or g_m , which is the ratio of the input voltage to the output current, for MOSFET device is given as

$$g_m = \frac{2I_{DC}}{V_{GS} - V_t}, \quad (18)$$

where V_{GS} is the gate-source voltage, V_t is the threshold voltage of the transistor, and I_{DC} is the DC current flowing through the transistor. The g_m of BJT device has relation of

$$g_m = \frac{qI_{DC}}{kT}. \quad (19)$$

Typically, the g_m of MOSFET is lower than that of BJT at a room temperature due to lower value of q/kT as compared to $V_{GS} - V_t$ in common process technologies. The higher g_m is always desired in analog and RF circuit designs to achieve a high gain. Moreover, higher g_m is also necessary to minimize the input-referred noise contribution from each noise source of transistors in order to enhance the performance of the LNAs and down-

conversion mixers. In RF PA designs, a low g_m necessitates the use of large device cells to accommodate required power capability, which results in a large power consumption. A low power-gain due to a low g_m also requires high driving input power for the PA, consequently reducing the power added efficiency (PAE). In short, a low g_m of MOSFETs is a big challenge in RF PA designs in terms of the load impedance matching and power efficiency [52].

2.4.1.2. Device reliability

A low breakdown voltage of MOSFET devices is one of key challenges in RF and MMW IC designs. Generally, PAs in transmitters deal with large swings of AC signals, and the device reliability is the most important factor for robust performance of the circuit. When the transistor is under the condition of high voltage stress, excessive electric fields cause the breakdown of the gate-oxide dielectric. This gate-oxide breakdown, especially in between the drain and gate terminals of the MOSFET device, is the biggest problem because it may destruct the device. The drain-to-substrate junction breakdown is also critical problem even though it is not as devastating to the transistor as the drain-to-gate oxide breakdown. The junction breakdown occurs when the high reverse-biased voltage is applied across the pn -junction. Excessive charge due to the high reverse-biased voltage causes the avalanche breakdown in the pn -junctions. The channel breakdown (between the drain and the source) due to the impact ionization or the gate leakage current, along with the hot-carriers-degradation effect, is another mechanism that is also destructive to the device. These breakdown effects on the MOSFET devices limit

the maximum voltage swing that the device can handle, bringing serious design hurdles to the large-signal circuit designs.

2.4.1.3. Linearity

Every circuit blocks in the transceiver system needs to operate as linearly as possible regardless of the signal strength they deal with. The linearity of active devices is obviously the key factor that determines overall linearity of circuits and systems. Inherently, the MOSFET device has various intrinsic sources of non-linearity. These are the gate-source junction capacitance, the gate-source transconductance, the gate-drain transconductance, and the drain-body junction diodes. These parameters with other parasitic components of an n -type MOSFET transistor are depicted in Figure 26. The gate-source junction capacitance (C_{gs}) may be the most dominant factor in non-linearity of a device, which seriously causes the phase distortion in the circuits. For example, a sensitive dependence of C_{gs} on the gate bias voltage introduces time-varying input reactance of a common source CMOS amplifier, originating the memory effect and amplitude-to-phase (AM-PM) distortion. In addition, non-vanishing third order term of the gate-source transconductance of which magnitude is also dependent on the gate bias voltage generates the third order inter-modulation distortion (IMD_3) and harmonic distortion, severely limiting the linearity performance of the CMOS amplifiers.

There have been efforts to analyze the effects of these dominant factors among other components [53]. However, most of researches are focused on the small signal analysis although critical linearity issues are raised from large signal operations. The RF

and MMW IC designers must adopt proper design techniques that compensates for non-linearity of active devices to achieve best performance of circuits and systems.

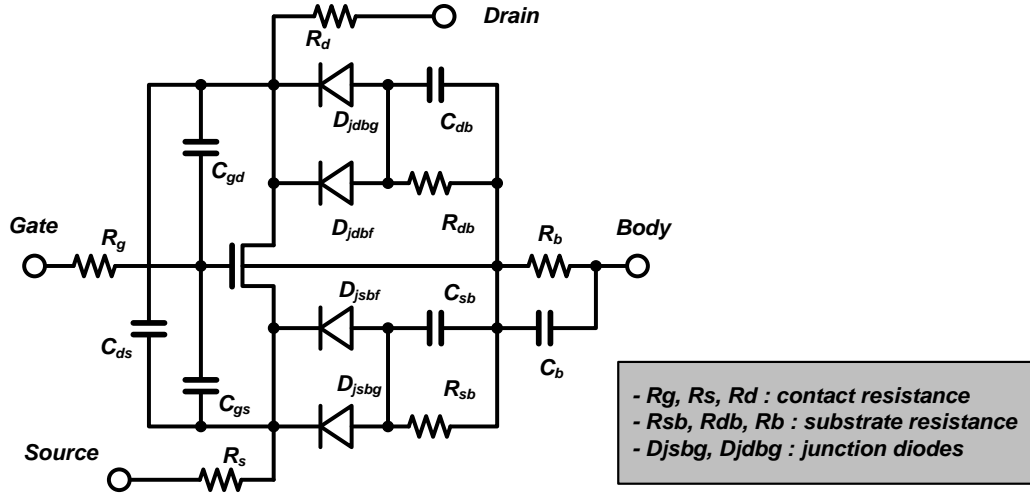


Figure 26. Equivalent NMOS transistor model.

2.4.2. SiGe HBTs

2.4.2.1. Speed consideration

One of key parameters of active device for RF and MMW applications are the f_T and the f_{max} . These parameters are strongly associated with gain/noise characteristics of the transistors. The equivalent circuit model of a general SiGe HBT is presented in Figure 27 [54]. From the transistor model, the f_T can be derived as

$$\frac{1}{2\pi f_T} = \tau_B + \tau_C + \frac{kT}{q} (C_{je} + C_{cb}) + (R_{ex} + R_c)C_{cb}, \quad (20)$$

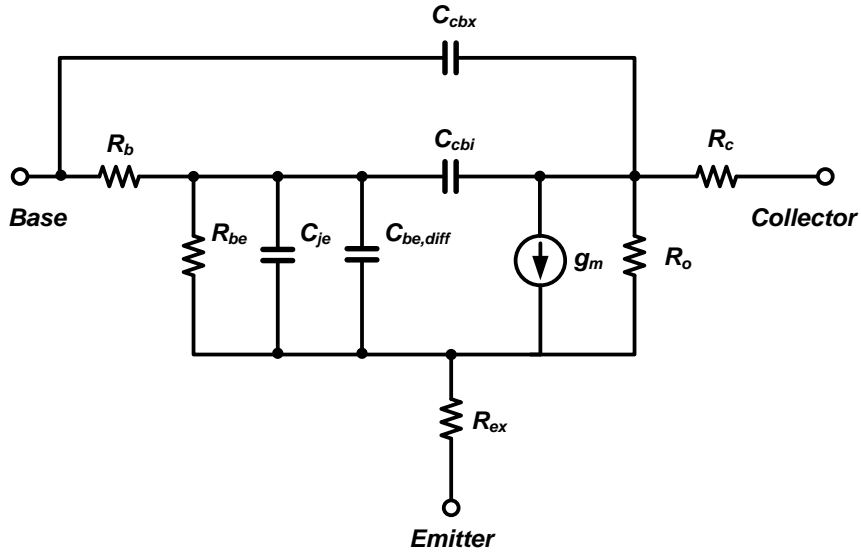


Figure 27. Equivalent SiGe HBT model.

where τ_B and τ_C are the base and collector transit time, respectively, C_{je} is the emitter-base junction capacitance, C_{cb} is the collector-base junction capacitance, and R_{ex} and R_c are the parasitic emitter and collector resistances, respectively. As seen in the (21), the f_T is dominated by the base and collector transit time with other secondary effects originated from the parasitic components. The f_{max} can be obtained from the f_T with relation of

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_b C_b}}, \quad (21)$$

where R_b and C_b are the base resistance and the base capacitance, respectively.

As a rule of thumb in MMW IC designs, the f_T and the f_{max} are required to be greater than twice of the operating frequency of circuits. Therefore, the implementation of the transceiver circuit blocks operating beyond tens of GHz requires highly advanced process technology with very high f_T and f_{max} .

2.4.2.2. Noise-gain trade-off

The noise performances of active devices are critical in LNAs and down-conversion mixers. Considering intrinsic parasitic parameters of active devices, minimum noise factor (F_{min}) of SiGe HBT can be simplified as [55]

$$F_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m R_b} \sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2}, \quad (22)$$

where $g_m R_b$ is assumed to be greater than 0.5. The associated gain, which is defined as the highest power gain achievable when the transistor source is noise matched for the minimum noise figure, is given by

$$G_a = \frac{1}{\omega^2 C_{bc} C_i R_b} \sqrt{\frac{g_m R_b + 1/2}{2} \frac{g_m^2}{\beta} + \frac{(\omega C_i)^2}{2} g_m R_b}, \quad (23)$$

where $C_i = C_{be} + C_{bc}$. As seen in the (21), F_{min} is minimized with a high DC current gain (β), a high f_T , and a low R_b . Due to the advanced band-gap engineering in the SiGe technology, a high β , a high f_T , and a low R_b can be simultaneously achieved for active devices, which makes SiGe devices as the optimal solution for low noise circuit designs. However, the associated gain, as expressed in the (22), is decreased as the β becomes higher, implying that the trade-off between the low noise characteristic and the high gain performance exists even in a single transistor. The low gain of active devices for low noise performance limits the overall gain and the dynamic range of the receiver system.

2.4.2.3. Device breakdown

The other key issue of active devices is the breakdown of the transistor, which is a big obstacle in implementation of large signal circuits in the transmitter system such as

PAs. For the SiGe HBTs, the breakdown issue is determined by effects of high electric fields that lead the device to fail. The avalanche multiplication in the collector-base region is the fundamental source of the breakdown of bipolar devices, and collector-emitter breakdown is also problematic [54]. The low breakdown voltage (BV) of the transistors makes design of circuits that handle large voltage swings very intricate. Furthermore, the breakdown voltage has trade-off relation to the f_T of the transistor as known as Johnson limit [56]. The Johnson limit describes that the product of the breakdown voltage and the f_T is always material-related constant. Therefore, extending $BV \cdot f_T$ product for enhancing the performance of RF and MMW circuits has been key challenges for many years.

The HBT breakdown voltages are characterized by the collector-emitter breakdown voltage when the emitter is open-circuited (BV_{CBO}) or when the base is open-circuited (BV_{CEO}). The BV_{CBO} is normally greater than BV_{CEO} because of the current gain in the emitter-base region. The relation of the two breakdown voltages can be given as [54]

$$BV_{CEO} \approx \frac{BV_{CBO}}{\beta^{1/n}} \quad (24)$$

where the β normally varies between 2 and 5.

2.5. Conclusion

Various challenges and issues of passive and active components for RF and MMW IC designs using silicon-based process technologies were discussed. Monolithic inductors, capacitors, and transmission lines were reviewed with particular focus on EM characteristics that determines performances of the components. Limitations and issues of

MOSFETs and SiGe HBTs for RF and MMW circuit designs were also discussed. These characteristics of passive and active devices must be carefully considered for accurate and optimal designs of each circuit blocks in the transceiver system.

CHAPTER 3

DESIGN OF MULTI-MODE CMOS POWER AMPLIFIERS FOR HIGH DATA-RATE WIRELESS COMMUNICATIONS

3.1. Introduction

With explosively growing demands on developments of true single-chip radio transceivers for mobile wireless communication devices at low cost, advances in research have led to successful implementations of CMOS PAs for various applications [57]-[61]. However, significant challenges in implementing CMOS PAs, such as low break-down voltages of transistors and lossy passive components on the highly conductive substrates, have necessitated the use of sophisticated design techniques to compensate for PA performance limitations.

Dealing with RF signals modulated with high complexity, PAs must simultaneously achieve high output power, high peak-power efficiency, and good linearity. In addition, advanced modulation schemes for high data-rate mobile wireless communications require PAs to operate at backed-off power levels to support high peak-to-average power ratio (PAPR). The PAPRs of common modulation schemes that are widely used in these days are summarized in Table 3. Because the PAs exhibits high power efficiency only near its peak output power level (P_{sat}), where transmitted signals are highly distorted, efficiency enhancement techniques at backed-off power levels (linear operation region) is strongly desired. Furthermore, enhanced efficiency at the lower output power levels extends the battery lifetime of mobile devices because the average efficiency of the PA is dominated by a probability distribution function in which

most of the transmission power is concentrated at much lower power levels than the peak output power [62].

Table 3. PAPRs of various modulation schemes.

	Peak magnitude	RMS value	Crest factor	PAPR (dB)
QPSK	1	1	1	0
64-QAM	1	$\sqrt{3/7}$	$\sqrt{7/3}$	3.7
WCDMA	1	-	-	10.6
OFDM	1	-	-	~12

In this chapter, design techniques to implement a fully-integrated watt-level linear CMOS PAs for advanced mobile communications are discussed. Section 3.2 introduces a novel power combining and discrete resizing technique to implement a multi-power mode operation with enhanced low-power efficiencies. Measured results verify the effectiveness of the proposed structure for WiMAX and WLAN multi-standards. Section 3.3 introduces a new figure-of-merit for multi-mode PAs that takes into account efficiency enhancement at power back-offs. The conclusion is followed in Section 3.4.

3.2. Linear Multi-Mode CMOS Power Amplifier

To design CMOS PAs with high output power and good efficiency/linearity, parallel-combining (or, parallel-amplification) techniques, as illustrated in Figure 28, can

be an attractive solution. By assembling multiple sub-PAs in parallel using output combining networks, the entire PA system can possibly transmit high output power while relaxing a linearity burden on individual sub-PAs. Moreover, the parallel combining structure can easily adopt a discrete power-control scheme to realize the necessary power back-offs by adequately resizing PA cells (i.e., disabling parts of parallel amplifier paths), thereby achieving enhanced low-power efficiency by reducing power consumption.

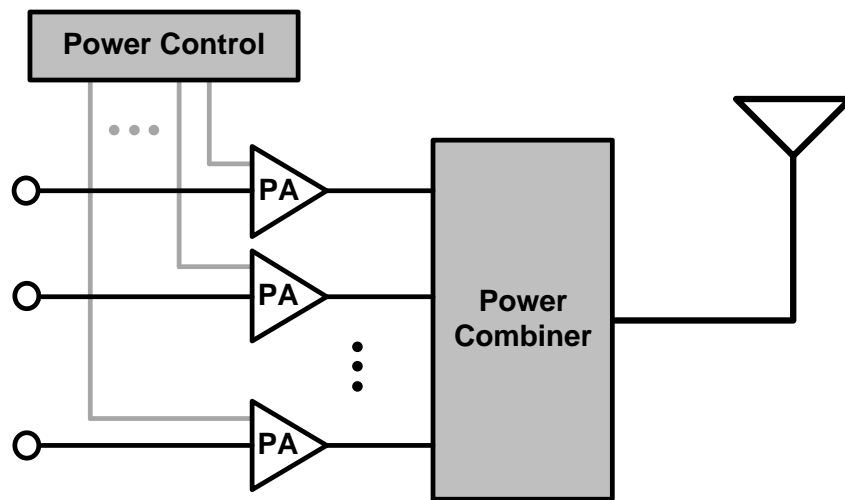


Figure 28. Block diagram of a parallel-combining PA with discrete power-control.

The transformer-based parallel combining technique is a practical way to realize fully-integrated parallel-combining multi-mode CMOS PAs. They are superior to transmission-line based parallel combining structures [63] in terms of integration ability and design simplicity. They also have wider operating bandwidth and less optimization issues than the LC-based network exploited in [64]. Two different ways of using the transformer-type power combiners associated with linear CMOS PAs have been

demonstrated thus far [65]-[68]. In one approach, the transformer is used as a current combiner [65]. The other approach uses the transformer to add up voltages at the output [66]-[68]. Integrated within PA systems, both structures were used to combine output power of individual PAs and support the control of the transmitted power levels in a discrete manner (Figure 29). However, by simply turning off each amplifier path to save power, these approaches neglected degradation effects in the transformer efficiency due to inactive primary inductors that create a leakage path back from the secondary inductor. Hence, there is room to further improve the efficiency characteristics in the lower-power modes of the PAs if the leakage is minimized.

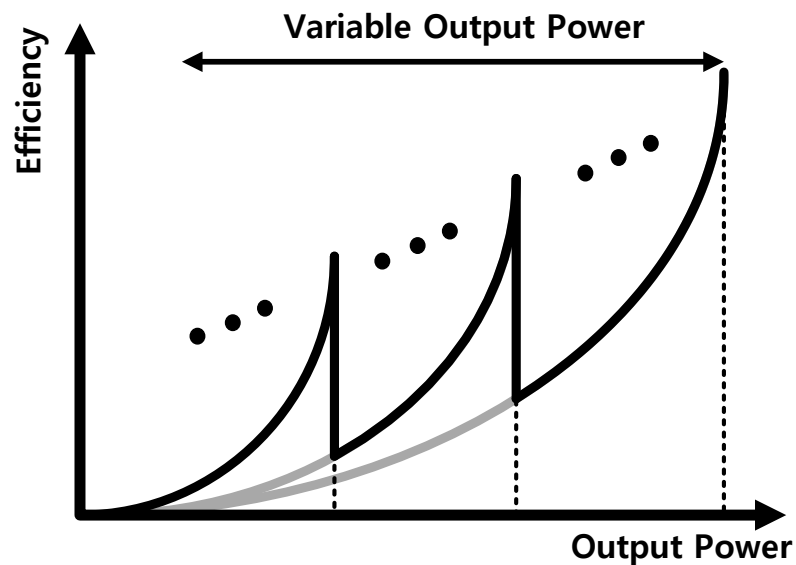


Figure 29. Operation of a multi-power mode PA.

In this section, we analyze the efficiency degradation effects of the multi-input-single-output transformers of which some of the inputs are disabled. Furthermore, a

design technique using varactor-based tunable matching networks to further improve the PA performance is introduced.

3.2.1. Power combining transformer

3.2.1.1. Transformers as power combiners

Power combining transformers can be mainly categorized as parallel-combining transformers (PCTs) that combine currents or series-combining transformers (SCTs) that aggregate voltages. Both combining transformers together with parallel PAs are illustrated in Figure 30. The number of turns of primary windings and secondary windings are denoted as N_1 and N_2 , respectively. For the PCT, the secondary winding is shared by multiple primary windings and sums all AC currents induced by each primary winding. For the SCT, multiple secondary windings are connected in series, each of which is correspondingly coupled to individual primary windings. All AC voltages across

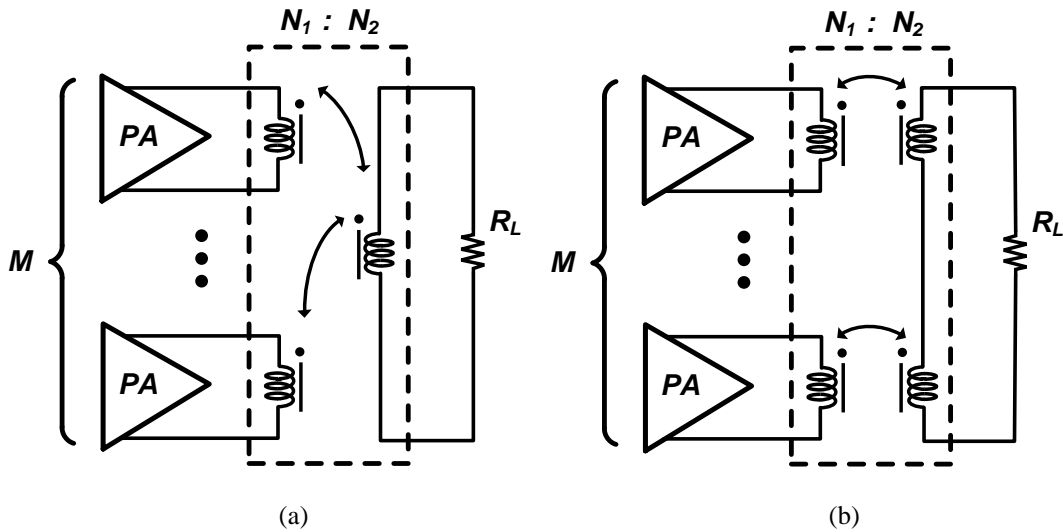


Figure 30. Two types of power combining transformers. (a) PCT. (b) SCT.

each secondary winding are summed at the top of the secondary node. With the multi-input nature of these transformers, it is also possible to enable/disable some of the inputs in a discrete manner, which is very attractive feature when they are integrated within a PA system.

3.2.1.2. Efficiency of power combining transformers

The efficiencies of both PCTs and SCTs have been analyzed in [69] ignoring coupling losses and assuming ideal mutual inductance. The transformer efficiency, which is the ratio of the transferred power at the load to the total input power, for both combining transformers can be expressed as

$$\eta_{transformer} = \frac{P_{Load}}{P_{In_total}} \quad (25)$$

$$\eta_{PCT} = \frac{R_L}{(R_1 n^2) / M + R_2 + R_L} \quad (26)$$

$$\eta_{SCT} = \frac{R_L}{MR_1 n^2 + MR_2 + R_L}, \quad (27)$$

where M is the number of combining paths, n is the turn ratio between the primary and the secondary windings (i.e., $n=N_2/N_1$), R_1 and R_2 are respective series resistances of the primary and the secondary windings, and R_L is the load impedance.

More elaboration to formulate the efficiencies of both transformers can be made including the finite coupling effect between the primary and the secondary windings. Replacing each single transformer with the T-equivalent circuit as shown in Figure 31(a) and 31(b) [70], the PCT and the SCT can be also equivalently modeled as presented in Figure 31(c) and 31(d), respectively (single-ended configurations are considered for

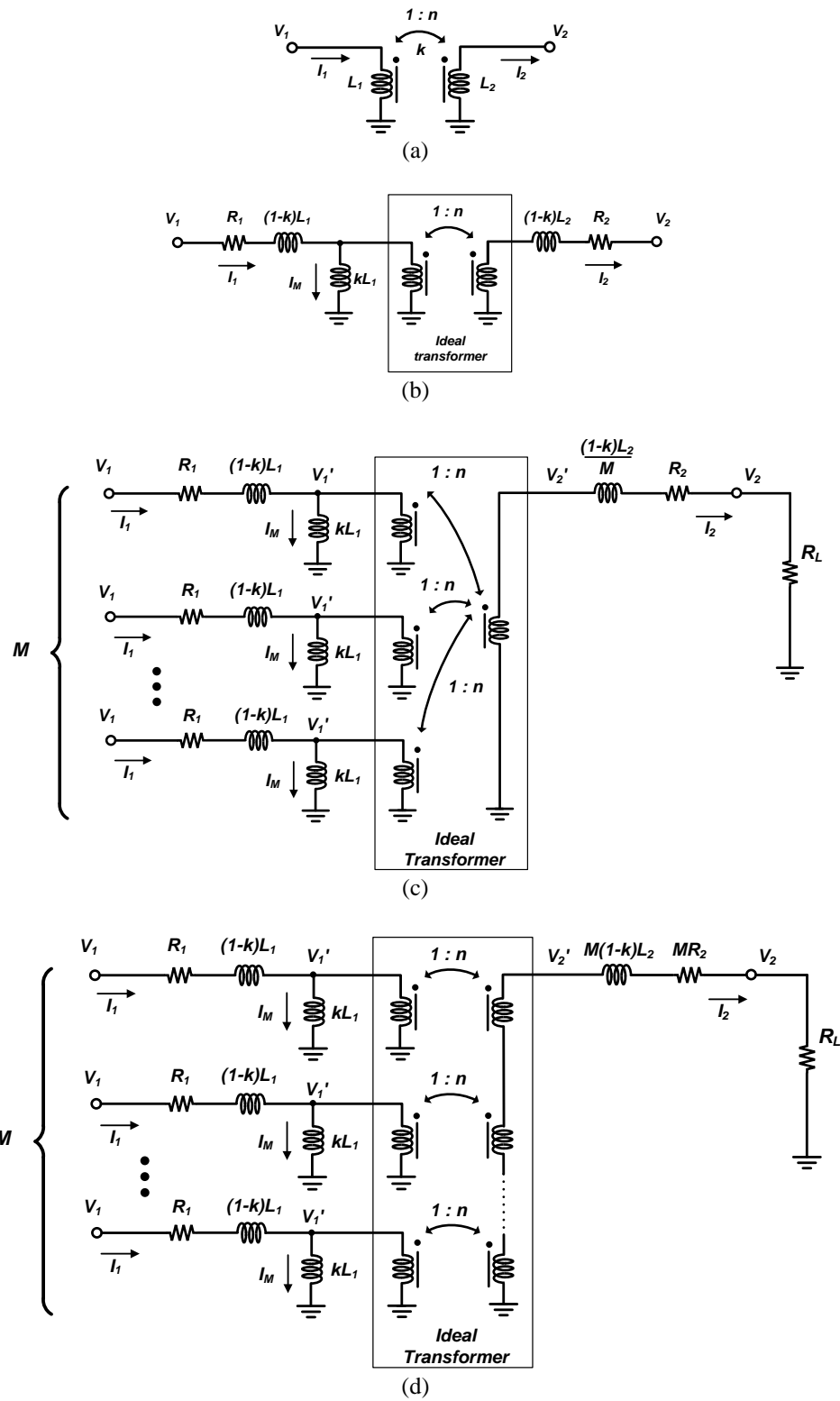


Figure 31. Equivalent transformer models. (a) Single $1:n$ transformer. (b) Equivalent model of a single $1:n$ transformer. (c) Equivalent model of an M -primary PCT. (d) Equivalent model of an M -primary SCT.

simple analysis). Due to the finite coupling coefficient, k (< 1), between the primary winding (L_1) and the secondary winding (L_2), leakage inductance will exist on both sides. For the PCT, the secondary leakage inductance will be formed in a parallel manner, and the effective inductance seen by total induced current at the secondary side becomes $(1-k)L_2/M$. In contrast, the effective secondary leakage inductance of the SCT is $M(1-k)L_2$ because all the secondary windings are connected in series.

In Figure 4(c), assuming that the current at the secondary winding is equally attributed from the primary windings, relations describing the currents and the voltages at each node are

$$M(I_1 - I_M) = nI_2 \quad (28)$$

$$nV_1' = V_2' \quad (29)$$

$$I_M = \frac{X}{j\omega k L_1 n} I_2 \quad (30)$$

$$I_1 = I_2 \left(\frac{n}{M} + \frac{X}{j\omega k L_1 n} \right) \quad (31)$$

$$V_1 = I_2 \left((R_1 + j\omega(1-k)L_1) \left(\frac{n}{M} + \frac{X}{j\omega k L_1 n} \right) + \frac{X}{n} \right), \quad (32)$$

where

$$X = j\omega \frac{(1-k)}{M} L_2 + R_2 + R_L. \quad (33)$$

Therefore, the efficiency of the PCT can be derived as

$$\eta_{PCT} \equiv \frac{P_{Load}}{P_{In_total}} = \frac{Re(I_2 V_2^*)}{M \times Re(I_1 V_1^*)} = \frac{R_L}{M \times Re \left(A \left((R_1 + j\omega(1-k)L_1 A) + \frac{X}{n} \right)^* \right)}, \quad (34)$$

where

$$A = \frac{n}{M} + \frac{X}{j\omega k L_1 n}. \quad (35)$$

Assuming ideal coupling ($k=1$) and ignoring mutual inductance ($I_M=0$), the (34) becomes equal to the (26) as derived in [69].

For the SCT, a similar flow can be taken to formulate the efficiency. In Figure 31(d), the current and the voltage relations are derived as

$$I_1 - I_M = nI_2 \quad (36)$$

$$MnV_1' = V_2' \quad (37)$$

$$I_M = \frac{Y}{j\omega k L_1 Mn} I_2 \quad (38)$$

$$I_1 = I_2 \left(n + \frac{Y}{j\omega k L_1 Mn} \right) \quad (39)$$

$$V_1 = I_2 \left((R_1 + j\omega(1-k)L_1) \left(n + \frac{Y}{j\omega k L_1 Mn} \right) + \frac{Y}{Mn} \right), \quad (40)$$

where

$$Y = j\omega M(1-k)L_2 + MR_2 + R_L. \quad (41)$$

Hence, the efficiency of the SCT can be represented as

$$\eta_{SCT} = \frac{R_L}{M \times Re \left(B \left((R_1 + j\omega(1-k)L_1) B + \frac{Y}{Mn} \right)^* \right)}, \quad (42)$$

where

$$B = n + \frac{Y}{j\omega k L_1 Mn}. \quad (43)$$

Note that the (42) also becomes equal to the (27) when ideal coupling ($k=1$) is assumed and mutual inductance is ignored ($I_M=0$).

3.2.2. Analysis on efficiency degradation of transformers

To determine the efficiencies of combining transformers described in the previous section, we only considered the case when all primary inputs participate in power combining. However, some of the primary inputs must be de-activated to realize discrete power back-offs. Although the overall power efficiency of the entire PA system appears to be increased at backed-off power levels at a first glance, substantial enhancement on the efficiency is difficult to achieve due to reverse-induced current from the secondary windings back to the idle primary windings that will inevitably dissipate power. This occurrence is illustrated in Figure 32. There is a de-activated PA among multiple PAs assembled in parallel using a combining transformer. Each active primary winding of the transformer induces AC currents at the secondary winding, and the secondary current induces another AC current at the idle primary windings with the same coupling coefficient. This reverse-induced current causes non-negligible power leakage through the idle primary sides of the transformer, degrading overall transformer efficiency. Depending on the input terminations of the idle primary windings (e.g., open-circuited, shorted to ground, and loaded by a capacitor), various frequency responses in the transformer efficiency characteristic may be obtained.

Using the approach taken in the previous section, the efficiency of the multi-primary-single-secondary transformers with some of the inputs disabled can be also derived. In Figure 33, the transformers have N idle primary inputs among M total primary

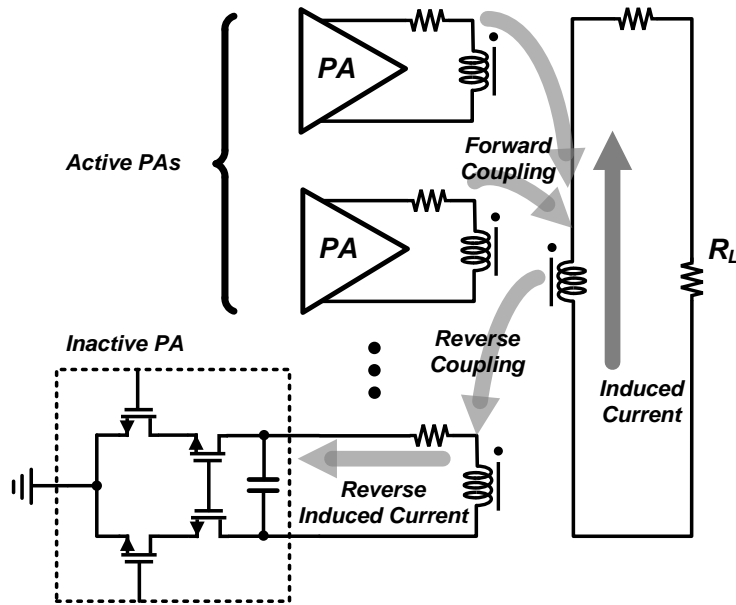


Figure 32. Diagram of a parallel-combining PA using a PCT in case when one of PAs is disabled.

inputs. Therefore, the number of active primary inputs becomes $M-N$. Each single transformer with an 1:n turn ratio can be replaced by the equivalent T-model as shown in Figure 31(b). Three different idle input terminations are considered: open-circuited, shorted to ground, and loaded by a capacitor. First, we define the impedance looking from the ideal transformer back to the idle primary input (excluding the mutual inductance) as Z_R . Therefore, Z_R is infinity for the open-circuited case, $R_1 + j\omega(1-k)L_1$ for the case when the idle primary side is shorted to ground, and $R_1 + j\omega(1-k)L_1 + 1/(j\omega C_R)$ for the case when the idle primary side is terminated by a series capacitor, C_R . The reverse-induced current and voltage from the secondary current (I_2) are denoted as I_R and V_R , respectively. Since the active primary windings serve as current sources to the secondary winding in the PCT (Figure 33(a)), we recognize that $M-N$ of active primary currents (I_1 -

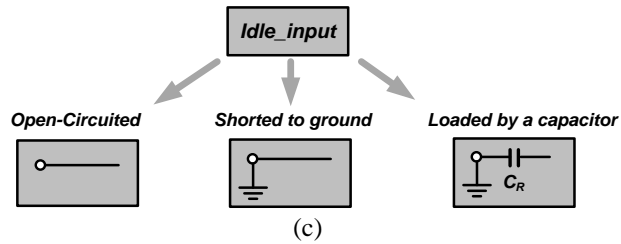
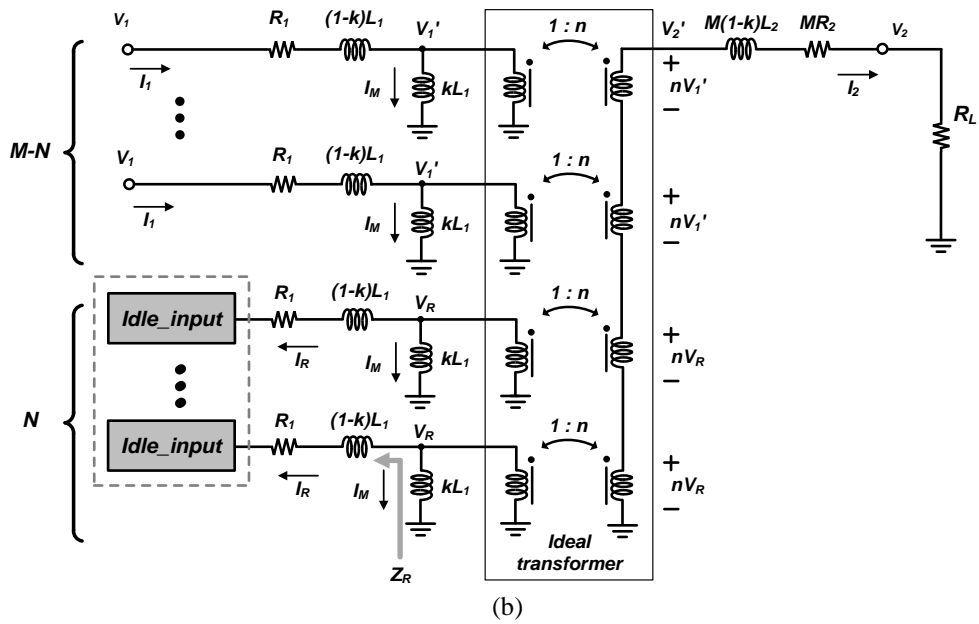
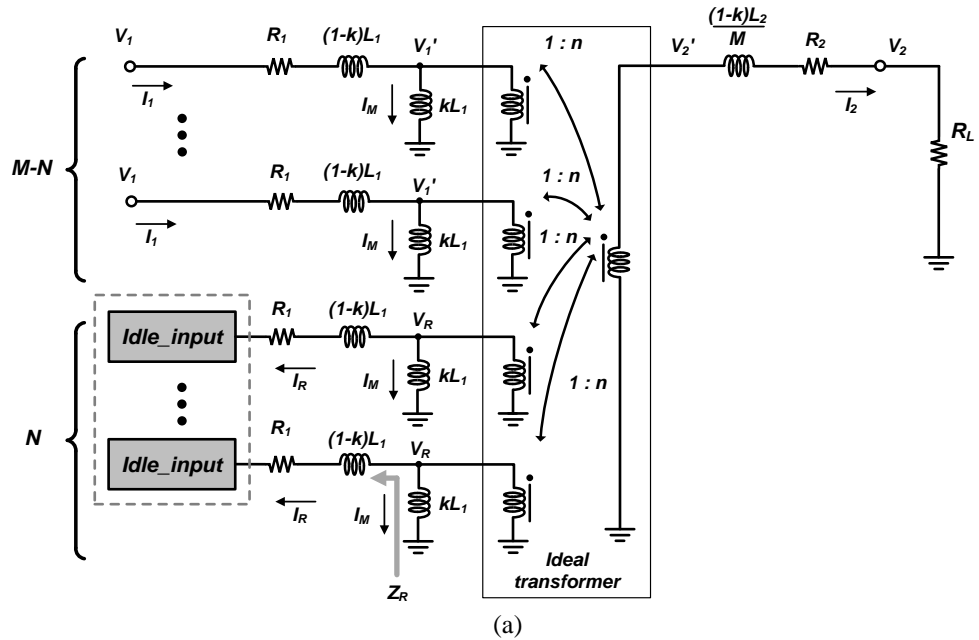


Figure 33. Equivalent circuit models of M -primary PCT and SCT with N -idle inputs. (a) PCT. (b) SCT. (c) Three different cases of idle primary input terminations.

I_M) induce the secondary current, $(I_1 - I_M)/n$, while some of the secondary current leak through the idle primary windings via reverse-induced current. Therefore, relations of the currents and the voltages at each node can be obtained as

$$(M - N)(I_1 - I_M) = nI_2 + N(I_R + I_M) \quad (44)$$

$$I_M = \frac{X}{j\omega k L_1 n} I_2 \quad (45)$$

$$I_R = \frac{X}{nZ_R} I_2 \quad (46)$$

$$I_1 = \frac{I_2}{M - N} \left(n + \frac{NX}{nZ_R} + \frac{MX}{j\omega k L_1 n} \right) \quad (47)$$

$$V_1 = I_2 \left(\frac{(R_1 + j\omega(1-k)L_1)C}{M - N} + \frac{X}{n} \right), \quad (48)$$

where X is the same as the (33) and

$$C = n + \frac{NX}{nZ_R} + \frac{MX}{j\omega k L_1 n}. \quad (49)$$

Therefore, the efficiency of the M -primary PCT with N -idle primary windings becomes

$$\eta_{PCT_N-idle} = \frac{Re(I_2 V_2^*)}{(M - N) \times Re(I_1 V_1^*)} = \frac{R_L}{Re \left(C \left(\frac{R_1 + j\omega(1-k)L_1}{M - N} C + \frac{X}{n} \right)^* \right)}. \quad (50)$$

On the other hand, for the SCT in Figure 33(b), the active primary winding should be regarded as a voltage source. The AC voltages across each secondary winding that are induced by the corresponding active primary windings are aggregated at the very top of the secondary node. The secondary current, $(I_1 - I_M)/n$, induced by the primary current, $I_1 - I_M$, flows through all the serially-connected secondary windings, subsequently inducing the AC current, nI_2 , at the idle primary windings and generating induced voltage, V_R . As

a result, the reverse-induced current, I_R , is produced. The currents and the voltages relations can be given as

$$I_1 - I_M = nI_2 \quad (51)$$

$$V_1' = \frac{V_2' - NnV_R}{(M - N)n} \quad (52)$$

$$V_R = -nI_2 \frac{Z_R j\omega k L_1}{Z_R + j\omega k L_1} \quad (53)$$

$$V_2 = \frac{R_L}{Y} V_2' \quad (54)$$

$$I_1 = V_2 \left(\frac{D}{j\omega k L_1 n (M - N)} + \frac{n}{R_L} \right) \quad (55)$$

$$V_1 = \frac{V_2}{(M - N)n} D + I_1 (R_1 + j\omega(1 - k)L_1), \quad (56)$$

where Y is the same as the (41) and

$$D = \frac{Y}{R_L} + \frac{Nn^2 Z_R j\omega k L_1}{R_L (Z_R + j\omega k L_1)}. \quad (57)$$

As a result, the efficiency of the M-primary SCT with N -idle primary sides can be derived as

$$\eta_{SCT_N-idle} = \frac{Re(I_2 V_2^*)}{(M - N) \times Re(I_1 V_1^*)} = \frac{R_L}{Re \left(E \left(\frac{D}{n} + E (R_1 + j\omega(1 - k)L_1) (M - N) \right)^* \right)}, \quad (58)$$

where

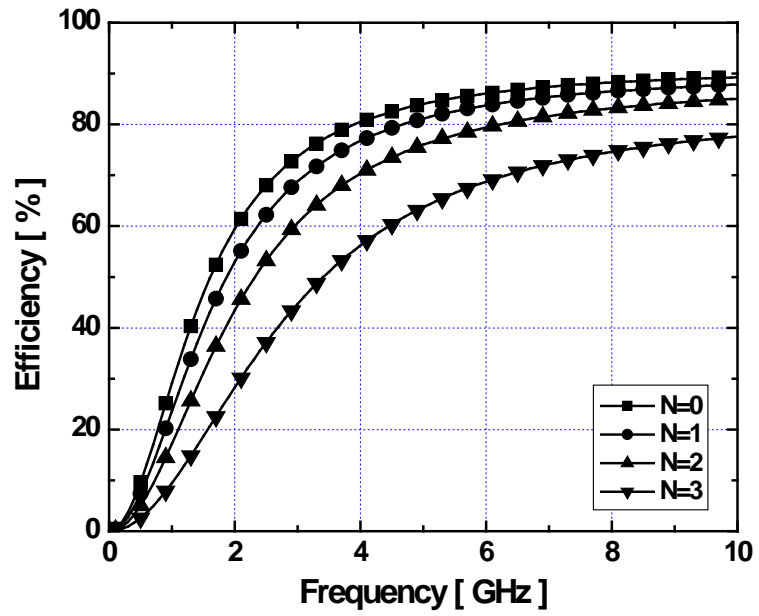
$$E = \frac{R_L D}{j\omega k L_1 n (M - N)} + n. \quad (59)$$

As observed from the (50) and the (58), the efficiencies of the M -primary PCT and SCT

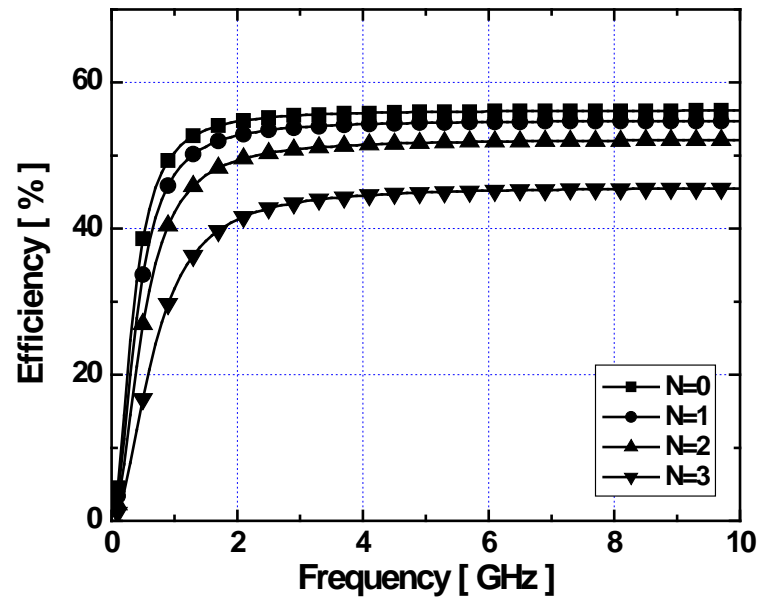
is a function of not only the number of combining inputs (M), but also the number of idle primary sides (N) and the impedance looking toward the idle primary input (Z_R). Note that if Z_R is very close to zero at specific frequencies, which is the case for LC resonance when the idle primary side is loaded by a capacitor, the denominators of the (50) and the (58) are radically increased and the efficiencies accordingly approach zero.

The analyzed efficiencies of both M -primary PCT and SCT having N -idle primary inputs with three different idle primary terminations are plotted in Figure 34, 35, and 36. A turn ratio of $n=2$ is considered. The self-inductance values of the primary and the secondary windings are set as $L_1=1$ nH and $L_2=n^2 \cdot L_1$ nH. The series resistance values, R_1 and R_2 , are 0.8Ω and $n^2 \cdot R_1 \Omega$, respectively. The quality-factor (Q) of spiral inductors and the coupling coefficient (k) are assumed to be 15 and 0.7 at 2.5 GHz, respectively. For both the PCT and the SCT, zero N represents that all primary inputs are enabled, and the efficiencies in this case are the maximum limit of the transformers. It is clearly observed that the overall efficiency is noticeably degraded as N increases. When the idle primary sides are perfectly open-circuited, the amount of efficiency degradation is minimal among all different cases. For the case when the idle primary sides are shorted to ground, the efficiency is reduced substantially across the entire frequency range. Furthermore, the resonant characteristic in the efficiency versus frequency plot is clearly seen in the case when the idle primary inputs are terminated by a capacitor (e.g., 4 pF in this analysis) for both transformers.

The transformer efficiency based on the calculation of maximum available gain [71] can be obtained in simulations. Example implementations of a two-primary PCT (Figure 37(a)) and an SCT (Figure 37(b)) with a turn ratio of 1:2 were electro-

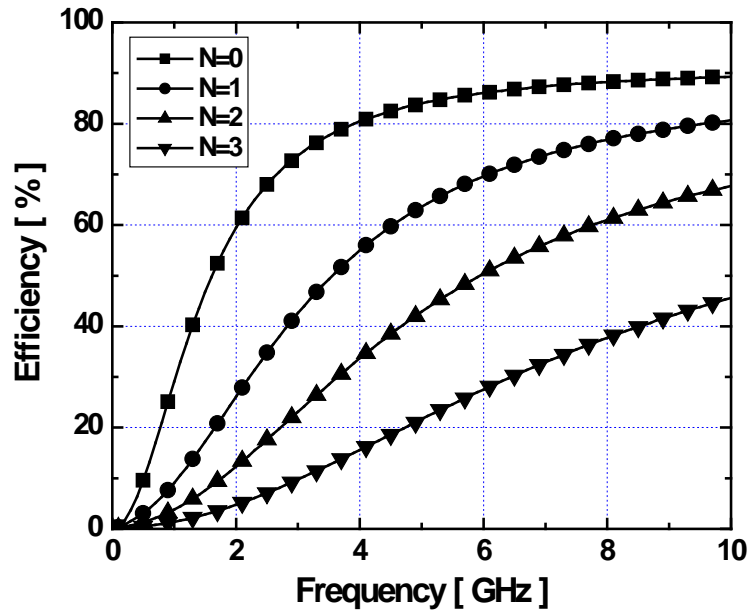


(a)

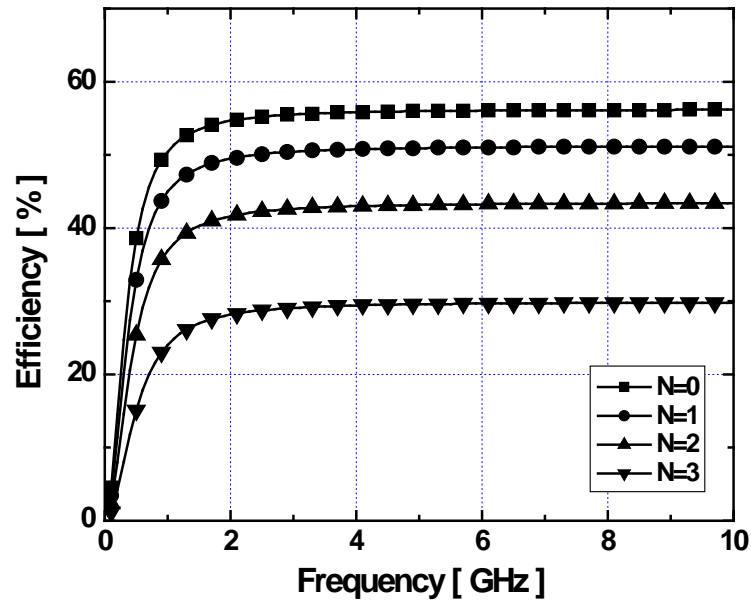


(b)

Figure 34. Analyzed efficiencies of 4-primary 1:2 transformers. (a) PCT with N -idle primary inputs that are open-circuited. (b) SCT with N -idle primary inputs that are open-circuited.

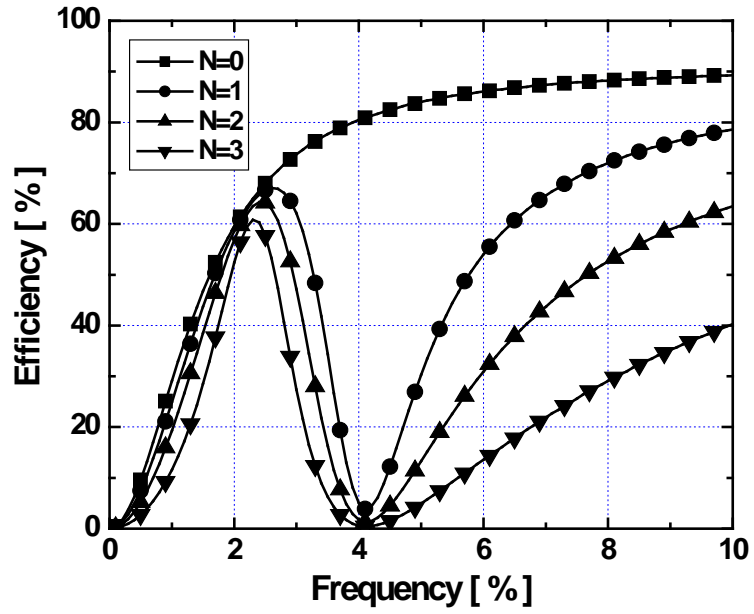


(a)

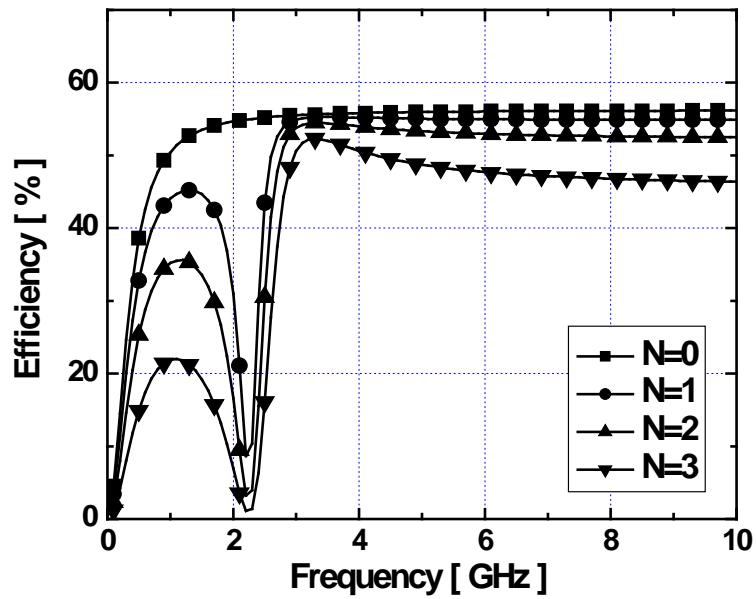


(b)

Figure 35. Analyzed efficiencies of 4-primary 1:2 transformers. (a) PCT with N -idle primary inputs that are shorted to ground. (b) SCT with N -idle primary inputs that are shorted to ground.



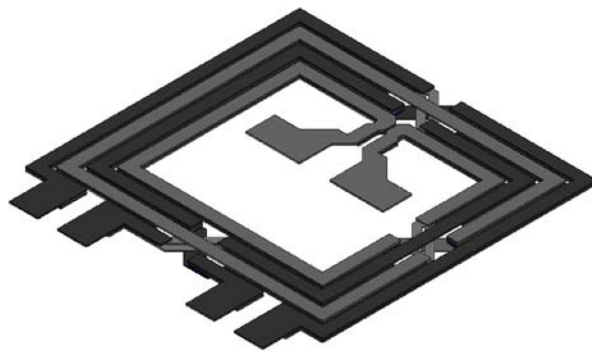
(a)



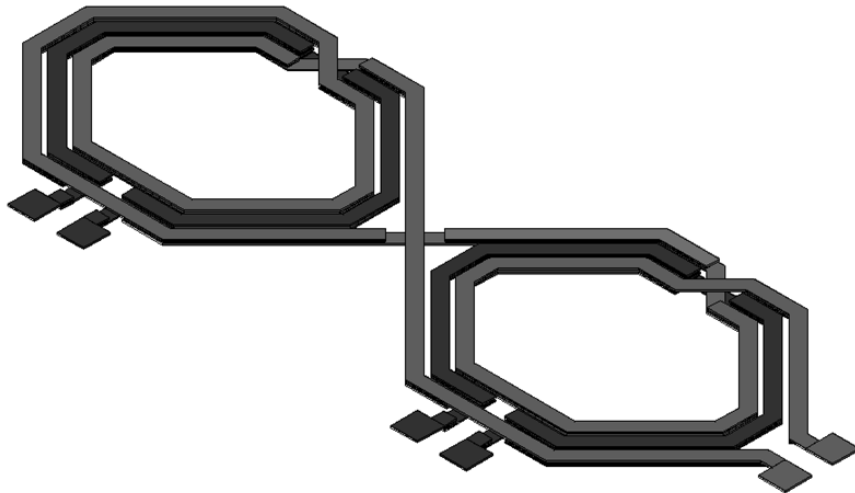
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Figure 36. Analyzed efficiencies of 4-primary 1:2 transformers. (a) PCT with N -idle primary inputs that are loaded by a capacitor. (b) SCT with N -idle primary inputs that are loaded by a capacitor.

magnetically modeled using Ansoft-HFSS and embedded into the simulations. As presented in Figure 38(b) and 38(c), maximum efficiencies across the entire frequency range were obtained only when all the primary inputs are transferring power, which coincides with derived results in the analysis above. When one of the primary inputs was disconnected from the power source with an open termination, about 10% efficiency drop

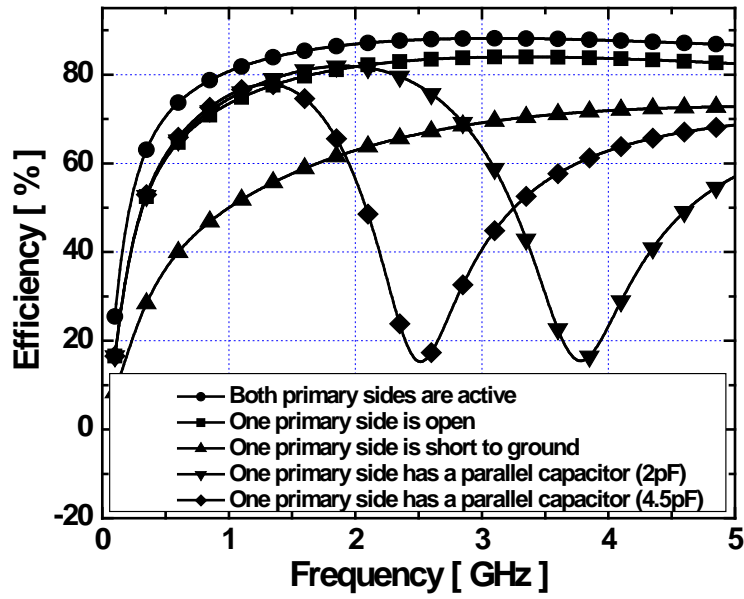


(a)

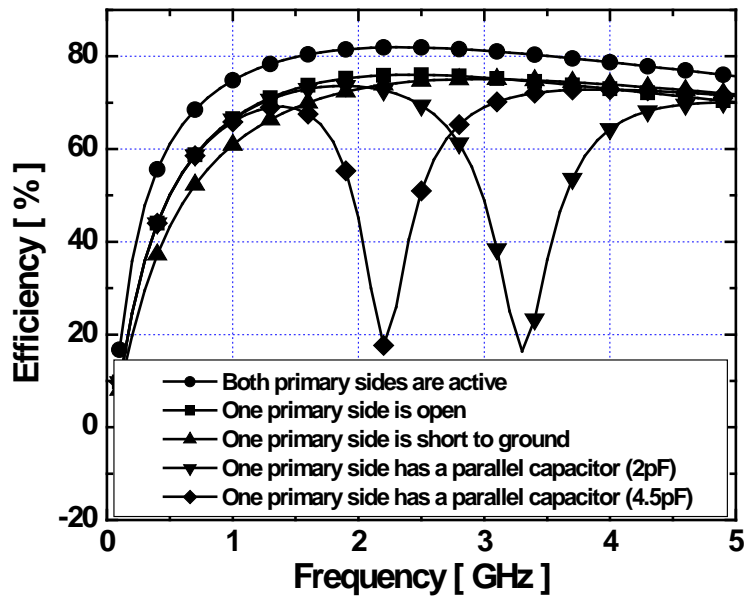


(b)

Figure 37. 3-D structures of two-primary 1:2 transformers. (a) PCT. (b) SCT.



(a)



(b)

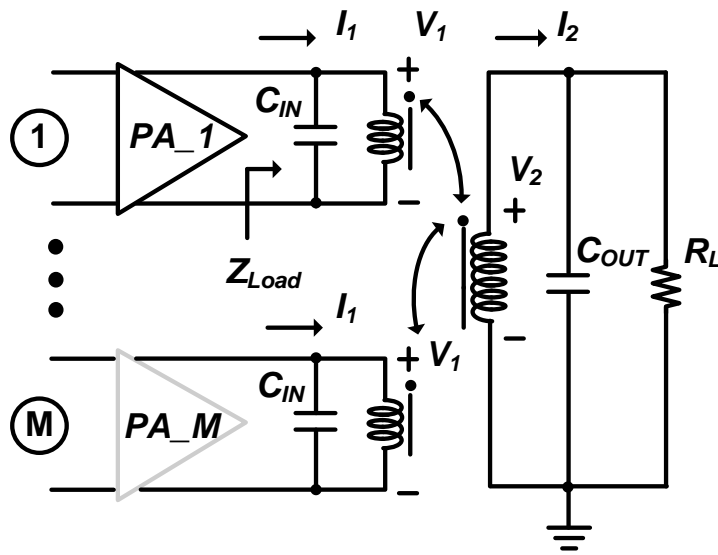
Figure 38. Simulated maximum available efficiencies of two-primary 1:2 transformers with EM-simulated models. (a) PCT. (b) SCT.

was observed. There was more significant efficiency degradation when one of the input ports was shorted to ground. Moreover, severe efficiency reduction occurred at resonances when one of the primary input ports had an additional capacitive load (2-pF and 4.5-pF capacitors were used in the simulation).

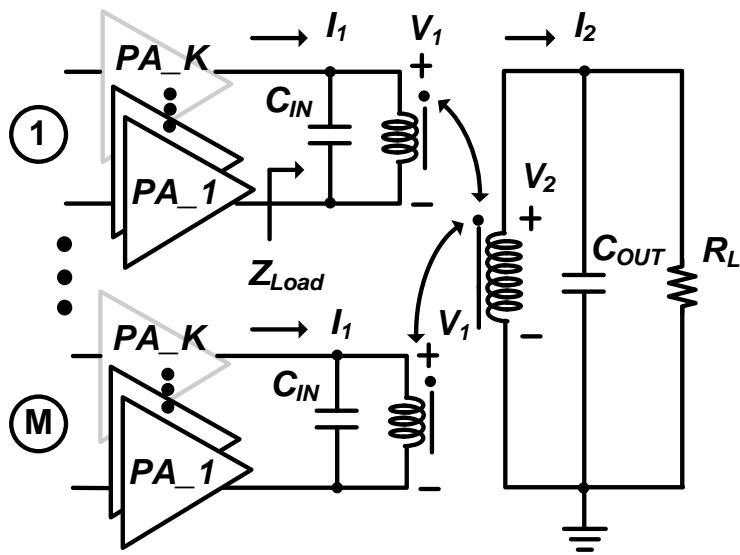
3.2.3. Design of a linear CMOS PA

3.2.3.1. Concurrent resizing and combining technique

As examined in above sections, all the primary inputs of the combining transformer must be active in order to utilize the transformer efficiency maximally. In a parallel-combining PA structure, instead of turning off each power-cell one at a time as shown in the structure in Figure 39(a), we can split each power-cell into multiple sub-cells and discretely enable/disable some of them in a concurrent manner. The idea is illustrated in Figure 39(b). There are several PA stages in parallel to be combined by the transformer at the output. Each PA stage consists of multiple sub-cells (i.e., PA_1 to PA_K) that are selectively combined in a concurrent way, meaning that only PA_1s in each PA path are combined when the lowest output power is needed, and all the sub-cells in each PA path are enabled and combined when the maximum output power is required. The number of enabled sub-power-cells may vary gradually depending on changes of required output power levels. Hence, all the primary inputs of the transformer can participate in power combining in every operation modes, preventing power losses due to idle primary inputs of the transformer. Although the idea is exemplified using a PCT in Figure 39, the SCT can be also used for the implementation.



(a)



(b)

Figure 39. Structures of parallel-combining PAs with discrete power-control using a PCT. (a) Conventional combining structure. (b) Concurrent combining structure.

Additionally, the concurrent combining scheme has another advantage over the conventional technique particularly when the PCT is used. The combining structure in

Figure 39(a) has a tendency to decrease input load impedance at the output node of each PA when some PAs are turned off [65], thereby resulting in a reduction in the voltage gain and power efficiency. The optimal load impedance of a smaller power cell should be greater than that of a larger power cell because the load-line changes in accordance with changes in the current level that the power cell can sustain [52]. Although the variation of the load impedance can be compensated with additional matching circuitry, excessive variation of the load impedance must be avoided for ease of design. In Fig. 39, the load impedance, which is a ratio of the output voltage (V_1) to the output current (I_1), becomes

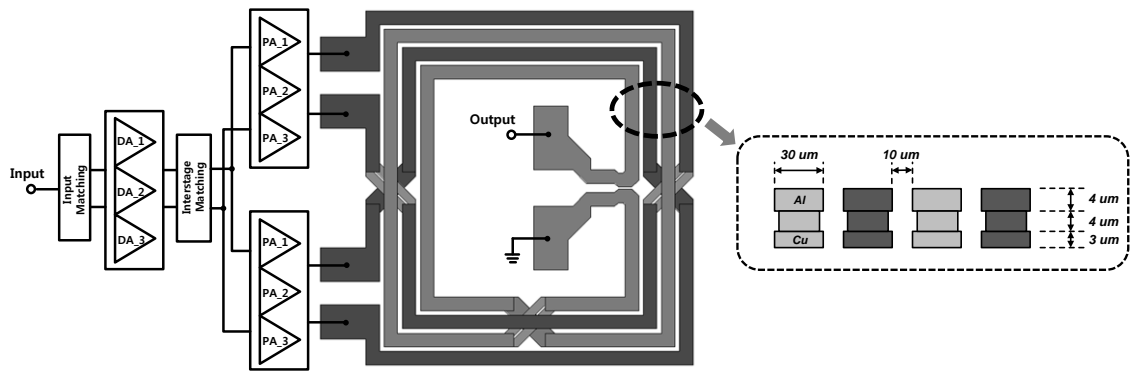
$$Z_{Load} = \frac{V_1}{I_1} = \frac{\frac{1}{n}V_2}{\frac{n}{M-N}I_2} = \frac{(M-N)V_2}{n^2I_2} = \frac{M-N}{n^2}R_L, \quad (62)$$

where M is the total number of parallel PA paths and N is the number of disabled PA paths. Thus, Z_{Load} in the conventional structure is decreased as N is increased to realize power back-offs, whereas it remains constant in the concurrent combining structure as long as equally-sized sub-power-cells in each path are enabled and combined (i.e., N is always zero in this structure). Without severely disturbing the optimal load impedance, improved efficiency characteristics in the lower-power modes can be achieved as compared to the conventional combining scheme using the PCT. However, additional tuning of the load impedance in such a way that each PA has increased load impedance when its size is reduced may be necessary to further improve the PA efficiency. This idea will be discussed later in this section.

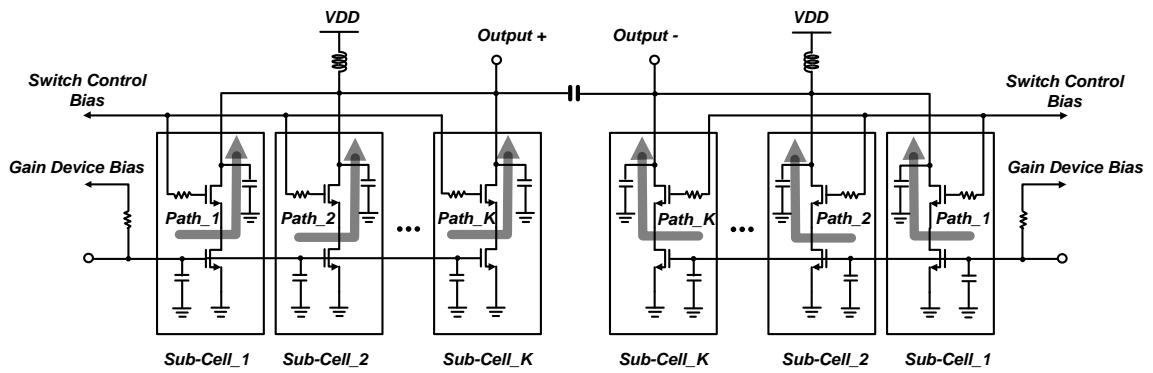
3.2.3.2. Design and implementation

A fully-integrated multi-mode PA has been fabricated in IBM 1P6M 0.18- μm CMOS technology. The diagram of designed two-stage PA is shown in Figure 40(a). The PA consists of an input balun with matching circuits, a driver stage, an inter-stage matching network, two parallel power stages, and a two-primary 1:2 PCT ($M=2$ and $N=0$) as a power combiner. The driver and each of power stages are divided into three sub-cells ($K=3$) for discrete resizing and combining. The PCT was chosen for this implementation because of its superiority in size as compared to the SCT. Due to the serially-connected secondary windings, the outer dimension of the SCT is approximately twice of that of the PCT as illustrated in Figure 37. Generalized schematic of each driver/power stage is shown in Figure 40(b). Although $K=3$ was chosen for this design, higher number of K (number of parallel driver/power stages) is also realizable to enable more continuous selections of the power mode. Operation conditions for designed PA are graphically presented in Figure 40(c). As required output power is increased, more parallel driver/power stages can be enabled with different bias conditions. At the maximum output power level that the PA can achieve, higher gate bias voltage is applied to operate the PA in clean class-A condition. For smaller power generation, relatively lower gate bias voltages are applied to enhance the overall efficiencies.

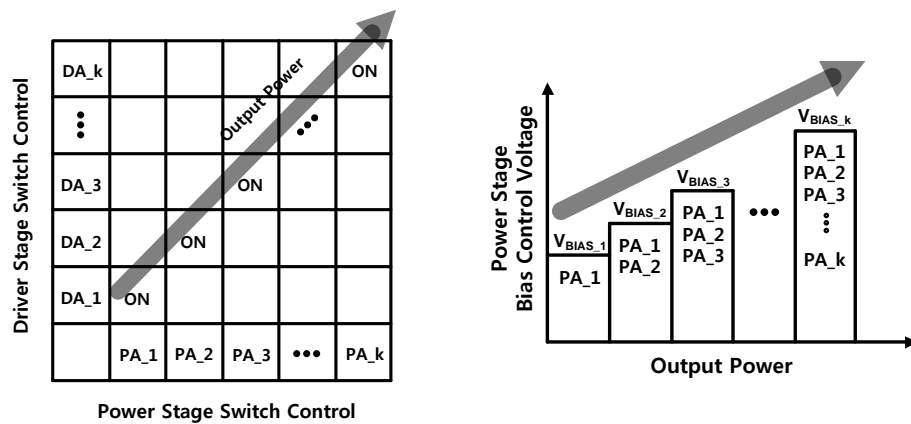
A simplified schematic of the entire PA is shown in Figure 41. Individual driver/power stages have pseudo-differential configuration to reduce the source degeneration effect by bonding wires. In addition, the differential topology minimizes self-mixing of even-order harmonics with the fundamental signal, thus reducing IMD_3 . Each sub-cell has a cascode configuration with thick gate-oxide transistors for the common gate (CG) devices, which not only relaxes voltage stress on the individual



(a)



(b)



(c)

Figure 40. Implementation of a concurrent combining PA. (a) Diagram of a PA with an integrated two-primary 1:2 PCT. (b) Generalized schematic of each driver and power stage. (c) Operation conditions of the PA.

transistors, but also eases the implementation for discrete power control. That is, by applying adequately low bias voltage to the gate of the CG devices, the signal paths through the devices are switched off and do not participate in the power combining. The common source (CS) devices in each path are always biased to operate in the saturation mode, thus overall input capacitance of driver/power stages remains constant. In contrast, there is finite change in the total output capacitance value depending on the number of enabled sub-cells because the CG devices in each stage are transitioned from the cut-off region (turned off) to the saturation region (turned on). This variation in the output capacitance should also be considered for the optimal matching, and will be effectively absorbed into the variable output matching circuitry.

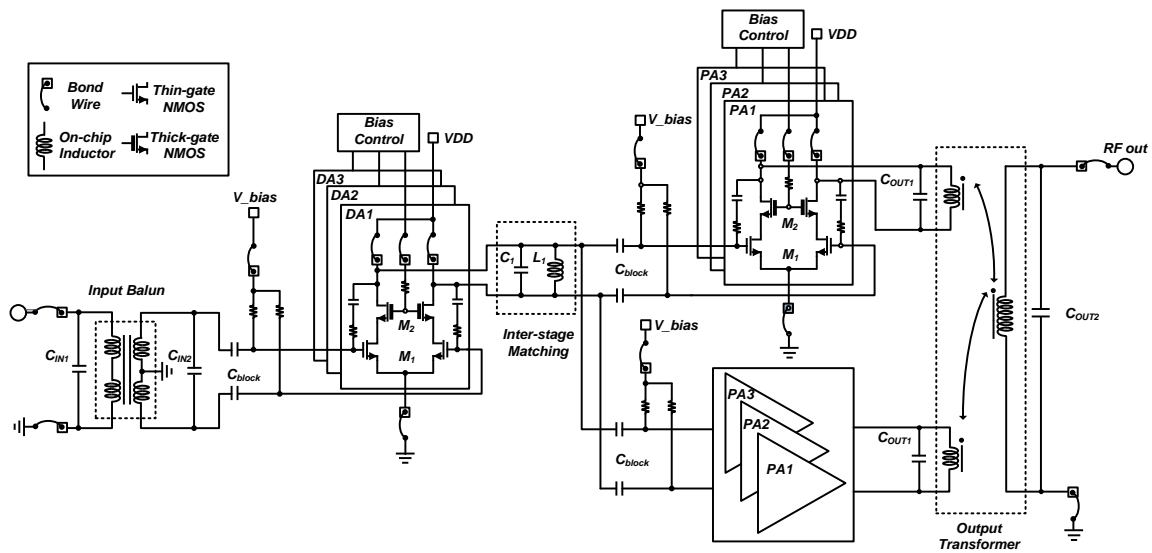


Figure 41. Simplified schematic of designed PA.

Both the driver and the power stages are biased at class-AB compromising efficiency and linearity. The driver stage is biased a little close to class-B so that it has the gain expansion to compensate for the compression of the power stage gain. An RC feedback is also employed for the individual cells to achieve better stability as well as a flatter gain response, or amplitude-to-amplitude (AM-AM) response. Three different operation modes are available with respect to required output power levels although more diverse combinations of individual sub-cells are also implementable. For maximum output power generation, all sub-cells in the driver stage ($DA_1 + DA_2 + DA_3$) and the power stages ($PA_1 + PA_2 + PA_3$) are enabled, and the PA operates in the high-power (HP) mode. By disabling the largest cells in each stage (i.e., enabling $DA_1 + DA_2$ and $PA_1 + PA_2$) the medium-power (MP) mode operation is realized with adequate power back-off. For the low-power (LP) mode operation, only the smallest sub-cells in each stage (DA_1 and PA_1) are operational for the power generation. Device sizes and configurations of each transistor in both stages are summarized in Table 4.

Design of the combining transformer is also critical because its power loss may dominate the overall power efficiency of the PA system even though the PA itself is well optimized. The outer dimension (size) of the transformer and widths of metal traces determine the self-inductance values and the quality factors of the primary and the secondary winding inductors. The spacing between two adjacent metal traces affects the effective coupling between the primary and the secondary windings as well as SRF of the transformer. Therefore, careful considerations should be taken to choose appropriate design parameters for the transformer while iteratively verifying with EM simulations. A turn ratio, $n=2$, was chosen because around $15\text{-}\Omega$ load impedance is required for

Table 4. Summary of device sizes.

	Common Source (M_{D1}/M_{P1})		Common Gate (M_{D2}/M_{P2})	
	W/L ($\mu\text{m}/\mu\text{m}$)	No. of fingers*	W/L ($\mu\text{m}/\mu\text{m}$)	No. of fingers*
DA_1	304/0.18	38	400/0.4	50
DA_2	304/0.18	38	400/0.4	50
DA_3	608/0.18	76	800/0.4	100
PA_1	512/0.18	64	656/0.4	82
PA_2	512/0.18	64	656/0.4	82
PA_3	2048/0.18	256	2624/0.4	328

* Unit finger-width is $8 \mu\text{m}$

individual power stages to generate maximum power (this value was obtained by load-pull simulations using ADS). The $30\text{-}\mu\text{m}$ width and $10\text{-}\mu\text{m}$ spacing for the windings were chosen in this design. The PCT with a size of $780 \times 800 \mu\text{m}^2$ has the primary and the secondary self-inductance of 1.5 nH and 4.2 nH at 2.5 GHz , respectively. The quality factor of each winding is greater than 12 (peak of 16) below 3 GHz , and the effective coupling coefficient is 0.72. The maximum available gain of designed PCT is -0.63 dB at 2.5 GHz . The transformer was implemented using a stack of two thick-metals connected through whole via trace as presented in Figure 40(a), which helps to achieve relatively high quality factor and coupling coefficient.

The characteristics of the PCT were obtained from EM simulations using Ansoft-HFSS. Figure 42 shows the simulation setup for the PCT. There are perfect-conductor leads for port excitations since the distance between the ground wall of the boundary box

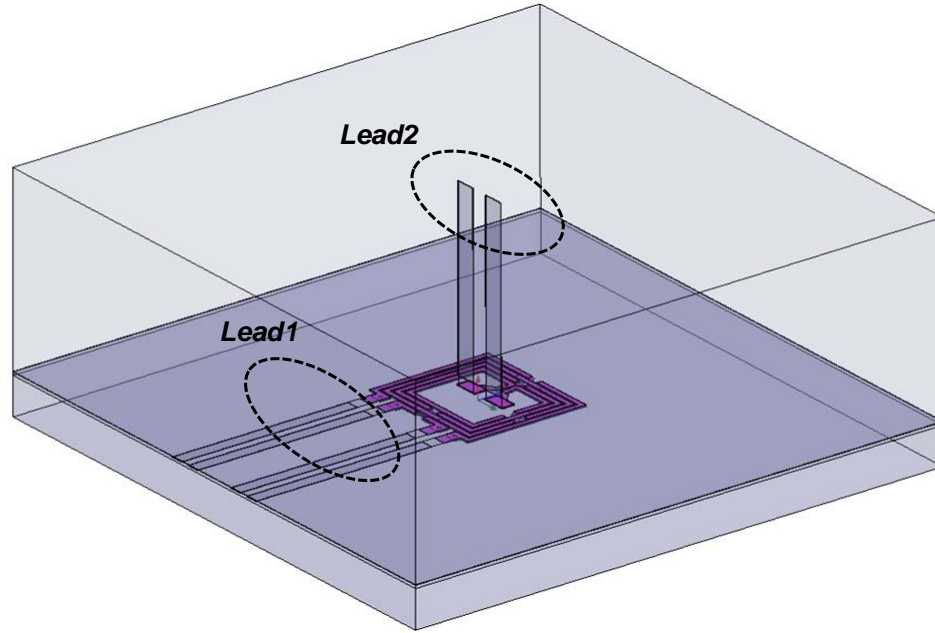


Figure 42. EM simulation setup of the two-primary PCT using HFSS.

and excitation ports is quite significant. This lead inductance must be obtained from independent simulations and effectively de-embedded from the overall inductance of the transformer. The separate EM simulation was performed for the conductor leads: Lead1 and Lead2. Then, the inductance of individual lead (L_{Lead}) is calculated from the setup presented in Figure 43 using equations

$$L_{Lead1} = \frac{Im(Z_{in})}{2\pi f} \quad (61)$$

$$L_{Lead2} = \frac{1}{2} \cdot \frac{Im(Z_{in})}{2\pi f}. \quad (62)$$

Negative values of these lead inductances must be added to the overall transformer inductance to obtain actual self inductance. Simulation results of the PCT are presented in Figure 44.

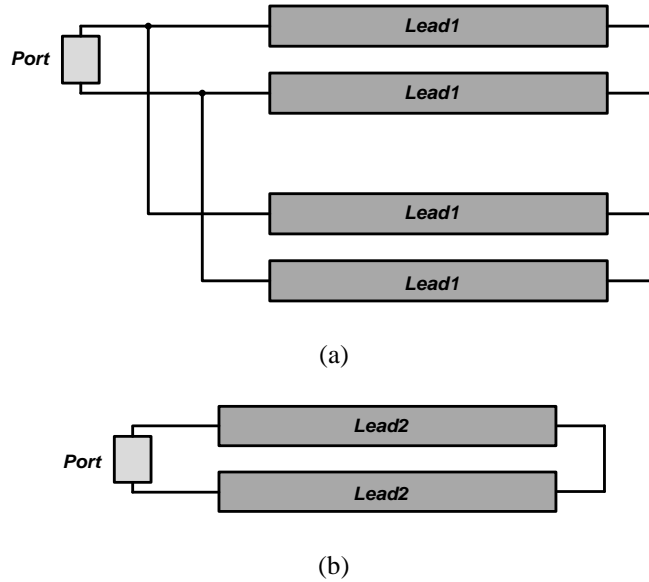


Figure 43. Lead inductance de-embedding setup. (a) For lead1. (b) For lead2.

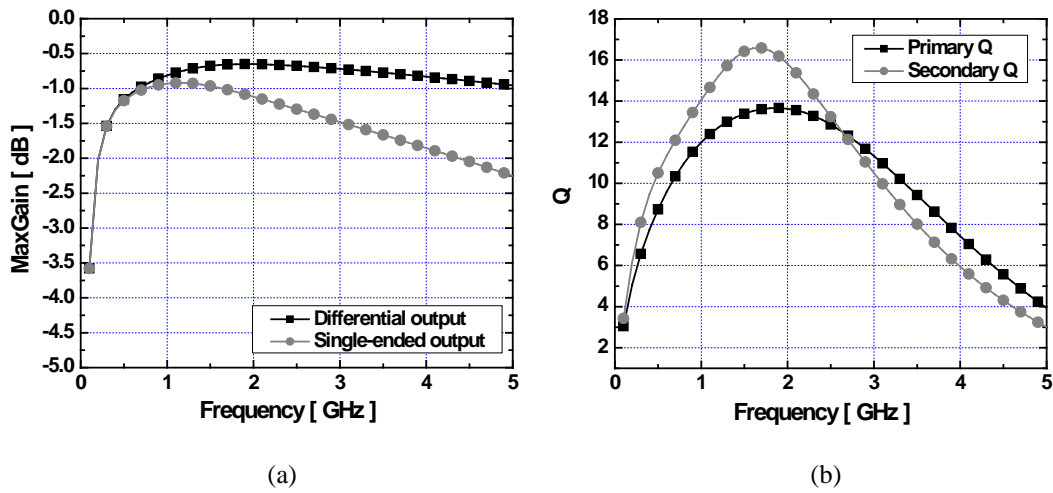


Figure 44. EM simulation results of two-primary PCT. (a) Maximum available gain. (b) Q .

3.2.3.3. Measurement results

A micro-photograph of designed PA is presented in Figure 45. A printed circuit board (PCB) was used for measurements, and the loss of signal lines in the PCB was de-embedded. Due to bond-wire effects in the matching networks, optimal operating frequency was a little shifted down from the desired frequency. One-tone power sweep

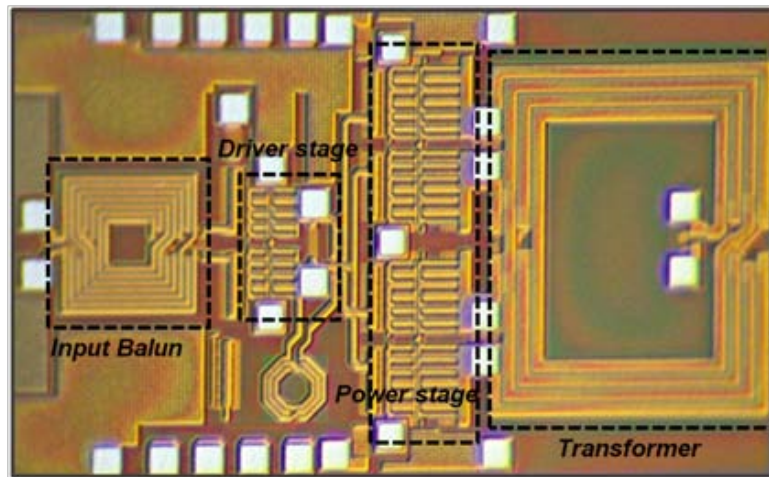


Figure 45. A Chip micro-photo of the concurrent combining multi-mode PA.

with continuous-wave signal at the RF frequency of 2.1 GHz was performed, and the measurement results are presented in Figure 46, 47, and 48. V_{DD} was 3.3 V and, the gate bias voltages for the low power (LP), the medium power (MP), and the high power (HP) modes were set at 0.5 V, 0.55 V and 0.6 V, respectively. Measured P_{sat}/P_{1dB} are 30.7/27.5 dBm with PAE of 35.8/20% for the HP mode, 25/21.8 dBm with PAE of 19.8/13% for the MP mode (6-dB back-off) and 19/16.5 dBm with PAE of 10.5/9.8% for the LP mode (12-dB back-off). Although we observed that 7% of efficiency enhancement was achieved at 17-dBm P_{out} , this is not as significant enhancement as anticipated in the

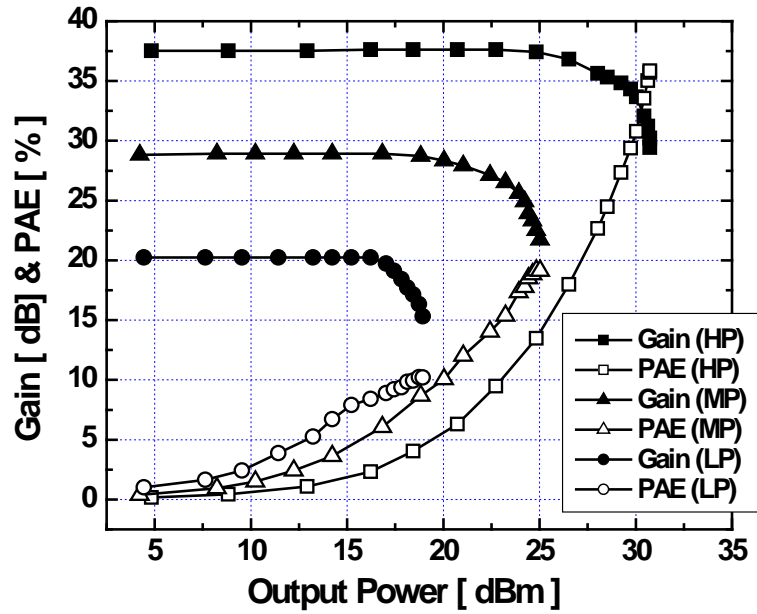


Figure 46. Measurement results of multi-mode linear CMOS PA: gain and PAE (at 2.1 GHz).

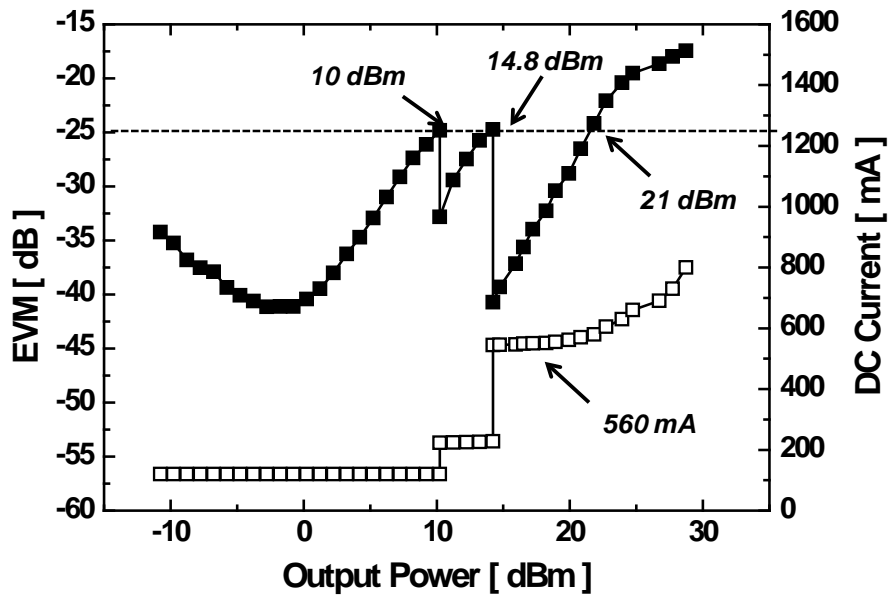
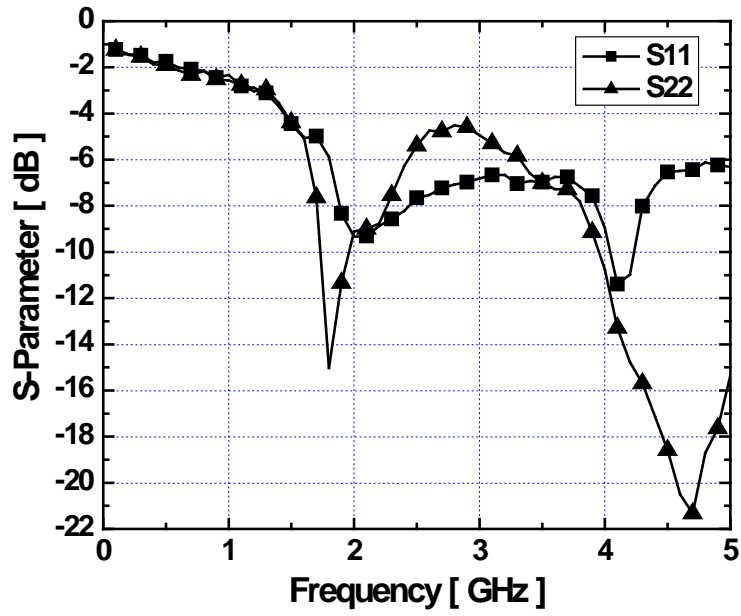
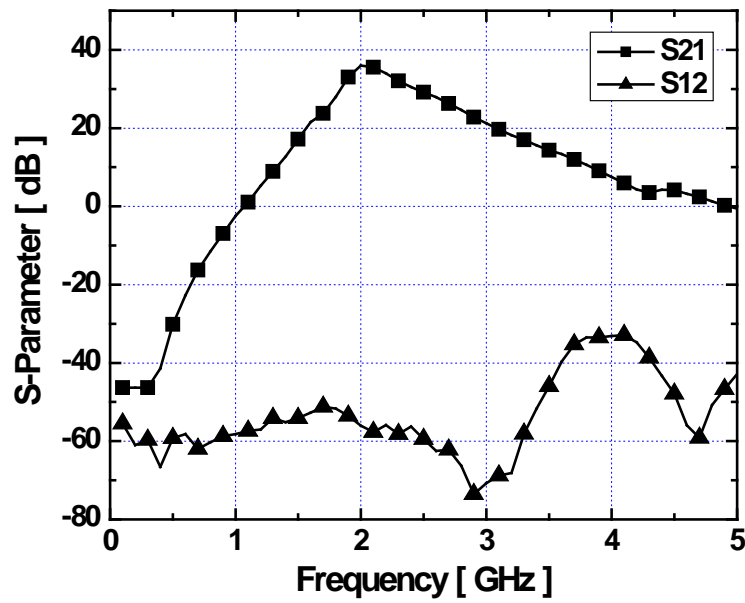


Figure 47. Measurement results of multi-mode linear CMOS PA: EVM (at 2.1 GHz).



(a)



(b)

Figure 48. Measurement results of multi-mode linear CMOS PA: S-parameters. (a) S_{11} and S_{22} . (b) S_{21} and S_{12} .

simulation. We believe that the optimal performance was limited at some point by the fixed matching network. We can improve the performance by adapting tunable capacitors in the output matching. For linearity test, 802.11g WLAN modulated signal was used to evaluate EVM. With 54 Mbps 64 QAM OFDM signal, -25-dB EVM specification was satisfied at output powers of 21 dBm (HP), 14.8 dBm (MP), and 10 dBm (LP), consuming DC quiescent current of 560 mA (HP), 200 mA (MP), and 100 mA (LP). We could verify that the linearity of designed PA is comparable to the conventional PA with enhanced low-power efficiency.

3.2.4. Load impedance modulation

To further optimize the PA performance in the lower-power modes, the load impedance seen by individual power stages must be tuned by variable matching circuitry. As the PA changes its operation mode (e.g., from HP mode to LP mode) the effective size of the power cell changes accordingly, requiring different values for the load impedance (Figure 49). Although the transformer has a fixed impedance transformation

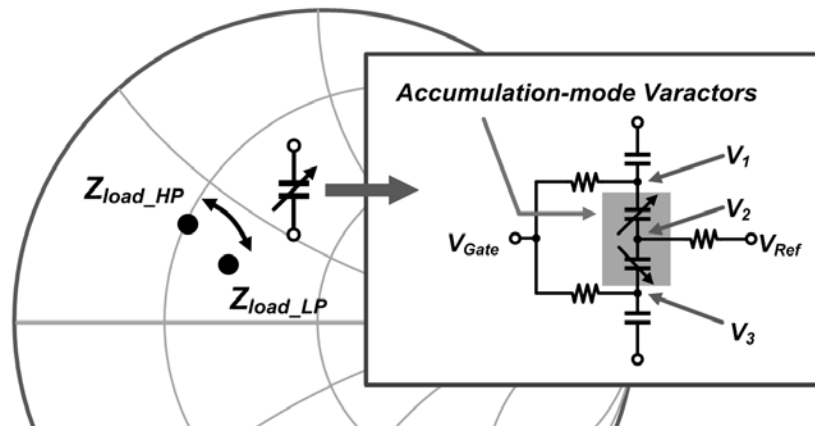


Figure 49. A varactor-based tunable capacitive matching circuit for load impedance modulation.

ratio due to its physical turn ratio, the transformed impedance value can still be adjusted (or, modulated) by adding a variable shunt capacitor to the output node of the power stages. Moreover, as fore-mentioned, the variation in the effective drain capacitance in accordance with the change in the cell size should also be taken into account. Absorbing this variation into the output capacitance, required capacitance values for the HP mode and the LP mode power stages are found to be 2.8 pF and 1.2 pF, respectively including device parasitic capacitances. The required capacitance for the MP mode power stage is not greatly different from the one for the LP mode, thus 1.2-pF capacitance was chosen for the necessary value covering the LP and MP modes.

This tunable capacitor was implemented using accumulation-mode (A-mode) MOS varactors. As presented in Figure 49, two varactors are connected symmetrically and embraced by fixed MIM capacitors on top and bottom. The A-mode varactor is an NMOS transistor on *N*-well of which the drain (D) and the source (S) are tied together. As the varactor changes its state from the depletion to the accumulation by adequate DC biasing which is applied through large resistors, different capacitance values can be achieved. When the biasing voltage difference between the gate and the source/drain is negative (e.g., $V_G = -1.5$ V and $V_{D/S} = 0$ V), the varactor is in depletion mode having smaller effective capacitance (the oxide capacitance in series with the depletion capacitance). On the other hand, the varactor exhibits larger capacitance (the oxide capacitance only) when the biasing voltage difference between the gate and the source/drain is positive (e.g., $V_G = 1.5$ V and $V_{D/S} = 0$ V) as the varactor is in the accumulation mode.

Because the reliability is the critical concern when using the varactors, a stacked

structure was exploited to relax the voltage stress on the gate-source/drain oxides by dividing applied voltage across the entire tunable matching circuit. The amplitude of the voltage swing across the gate-source/drain should be maintained within a few volts not to cause gate-oxide break-down. This was verified with simulated waveforms. As presented in Figure 50, when the PA is transmitting at almost saturated output power (with RF input power of -3 dBm), the voltage swing at the drain of each power stage remains under 11 V

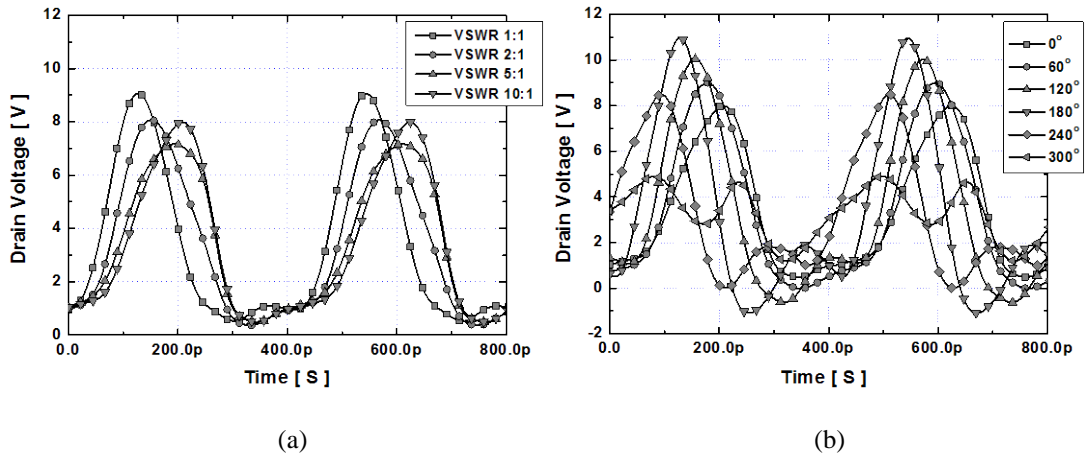


Figure 50. Simulated voltage swings at the drain of each power stage when RF input power is -3 dBm. (a) For different VSWRs with same angle (0°). (b) For VSWR of 10:1 and different angles.

even in various load mismatch conditions (9 V in the optimal load condition). In this case, a maximum 4.2-Vpp (3.7-Vpp in the optimal load condition) swing is applied across the gate-source/drain of individual varactors (V_1 - V_2 and V_3 - V_2 in Figure 49). On the other hand, less than 1-Vpp swing is applied across the varactor when the PA is operating in the LP mode. Therefore, with the stacking approach, the varactors operate under safe conditions.

It should be also noted that a large voltage swing across the varactors when the

PA is transmitting near saturated output power levels may modulate the instantaneous capacitance value during the signal period. However, the average capacitance value is still determined by applied gate voltage of the varactors, and the linearity performance of the PA in terms of the EVM and harmonics are negligibly affected by the varactors because the PA operates at backed-off power levels in most of the times. The varactor-based tunable matching circuit was used to implement C_{OUT1} and C_I in Figure 41.

The tunable matching circuit has Q of greater than 35 in the HP mode and 25 in the LP mode (Figure 51). Compared to much lower Q of the on-chip transformer, the effect of the varactor-based matching circuit on the overall Q of the output matching network is negligible. In the simulation, only 0.5-dB difference in the gain performance, and 1-% difference in the efficiency performance were seen (Figure 52). The entire schematic of the linear multi-mode CMOS PA with load impedance modulation technique is presented in Figure 53.

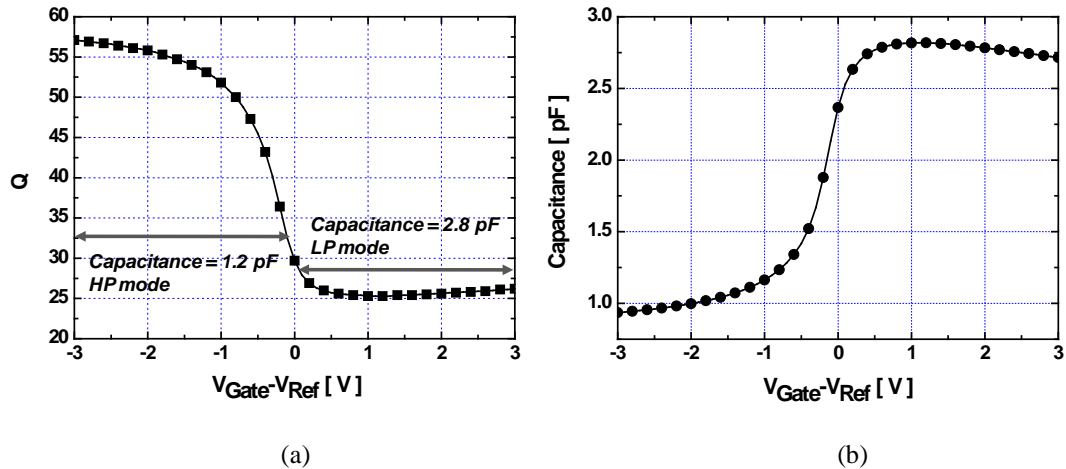


Figure 51. Simulation results of the varactor-based matching circuit. (a) Q . (b) Capacitance.

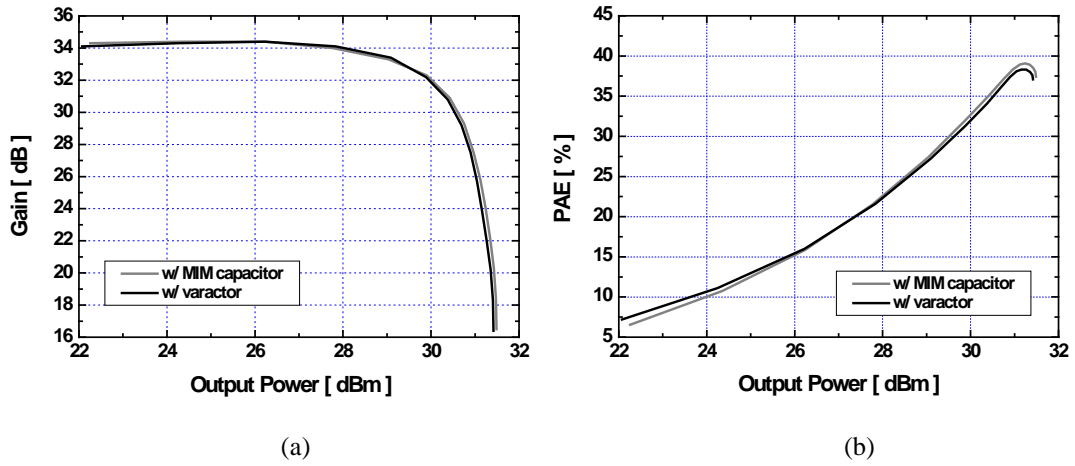


Figure 52. Simulation results of the PA with the varactor-based matching circuit. (a) Gain. (b) PAE.

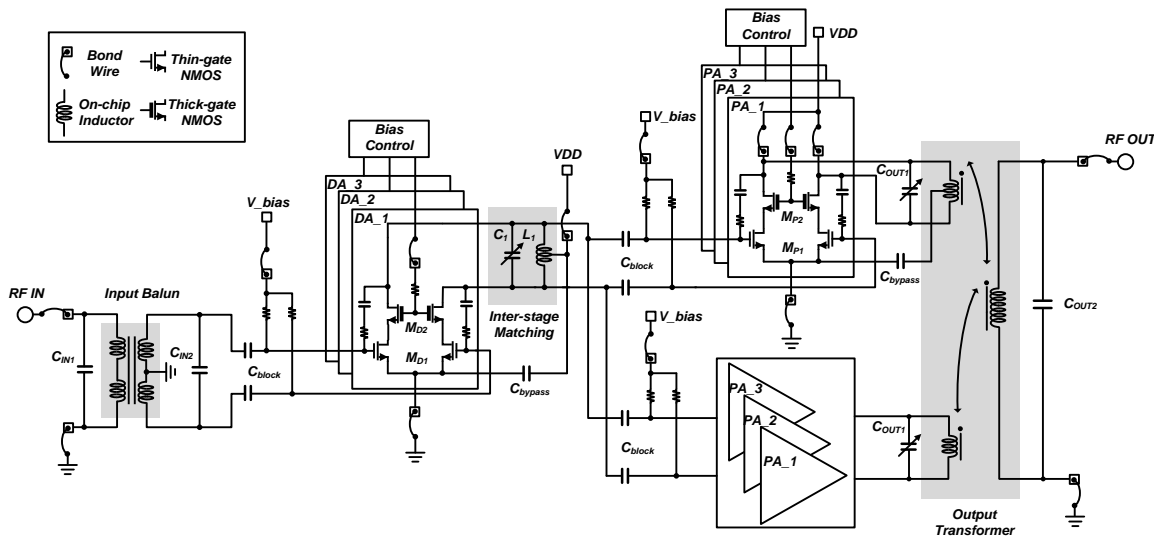


Figure 53. Entire schematic of designed linear multi-mode CMOS PA with load impedance modulation technique.

3.2.5. Measurement results of a multi-mode CMOS PA with load impedance modulation

The PA chip was mounted on the FR-4 printed circuit board (PCB) for measurements. The micro-photograph of the PA is presented in Figure 54. The PCB line loss was de-embedded, but the loss due to bonding-wires is included in the experimental

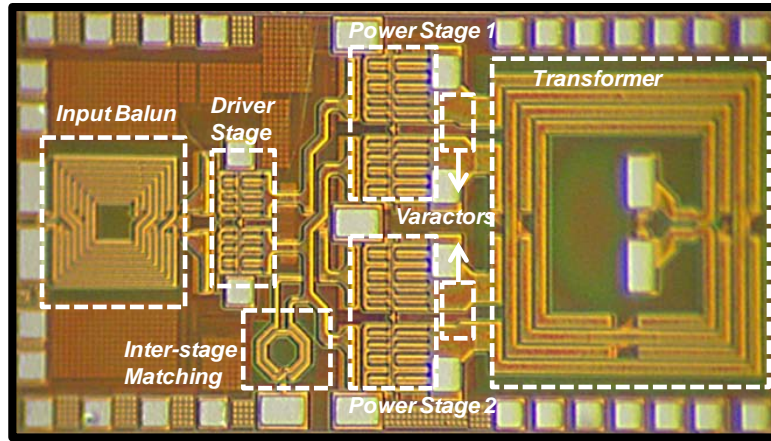


Figure 54. Micro-photograph of designed multi-mode linear CMOS PA with load impedance modulation technique ($1.1 \times 1.8 \text{ mm}^2$).

results. A single-tone continuous-wave signal with the frequency of 2.5 GHz was applied to the PA to measure the gain, $P_{1\text{dB}}$, P_{sat} , and PAE in three different operation modes. The measured results are plotted in Figure 55. Power back-offs are realized by concurrently resizing the driver and the power-cells. When all sub-cells in the driver and the power stages were enabled for the HP mode operation, gain of 31.3 dB, P_{sat} of 31 dBm, $P_{1\text{dB}}$ of 28 dBm, and peak PAE of 34.8% were achieved. For the MP and the LP mode operations, two different cases were tested. First, only discrete resizing and concurrent power combining were exploited to implement power back-offs. Next, the inter-stage and the

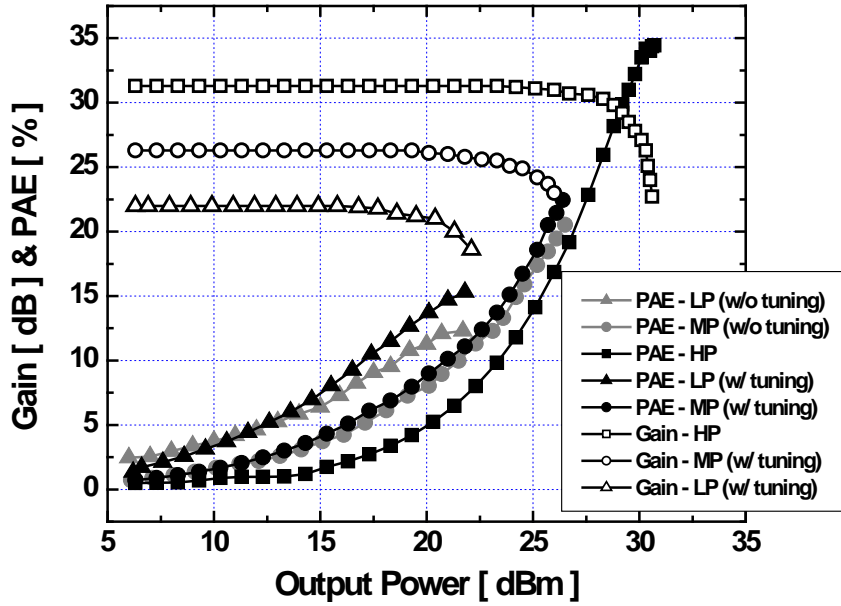


Figure 55. Measurement results of multi-mode PA with load impedance modulation in three operation modes: gain and PAE (at 2.5 GHz).

output matching circuits were additionally tuned by adjusting the varactor biasing voltage (bias voltages were applied externally). By only disabling the largest cells in the driver and the power stages, a power back-off of about 5 dB was realized (MP mode), achieving 26.5 dB, 26 dBm, 22.5 dBm, and 20.2% for the gain, P_{sat} , $P_{1\text{dB}}$, and peak PAE, respectively. With additional tuning of matching networks, gain expansion was obtained with boosted peak PAE. The small-signal gain did not have noticeable change, but the $P_{1\text{dB}}$ and the peak PAE were increased to 23.8 dBm and to 22.5%, respectively. For the LP mode operation, only the smallest cells in the driver and the power stages were enabled. The P_{sat} was backed-off by about 3 dB more from the one for the MP mode. An achieved gain, P_{sat} , $P_{1\text{dB}}$, and peak PAE with additional tuning of the matching networks were 22.4 dB, 22.3 dBm, 20.5 dBm, and 15%, respectively. The peak PAE in the LP

mode without tuning of the matching networks was only 12%. As clearly indicated in Figure 55, by employing the proposed multi-mode scheme, 9-% point increase in the PAE at the output power of 20 dBm (from 5% to 14% at 11-dB back-off from P_{sat}) and 5-% point increase at the output power of 25 dBm (from 14% to 19% at 6-dB back-off from P_{sat}) were achieved as compared to the case when the PA is operating solely in the HP mode. The measured DC currents and S-parameters of designed PA in three operation modes is plotted in Figure 56 and 57. In the HP, MP, and LP modes, designed PA consumes idle DC current of 590 mA, 225 mA, and 105 mA, respectively at a 3.3 V power supply. The gate biasing voltages for the HP, MP, and LP modes were 0.58 V, 0.54 V, and 0.5 V, respectively for the power stages and 0.56 V, 0.52 V, and 0.5 V, respectively for the driver stage. Relatively high gate biasing voltages were applied in the

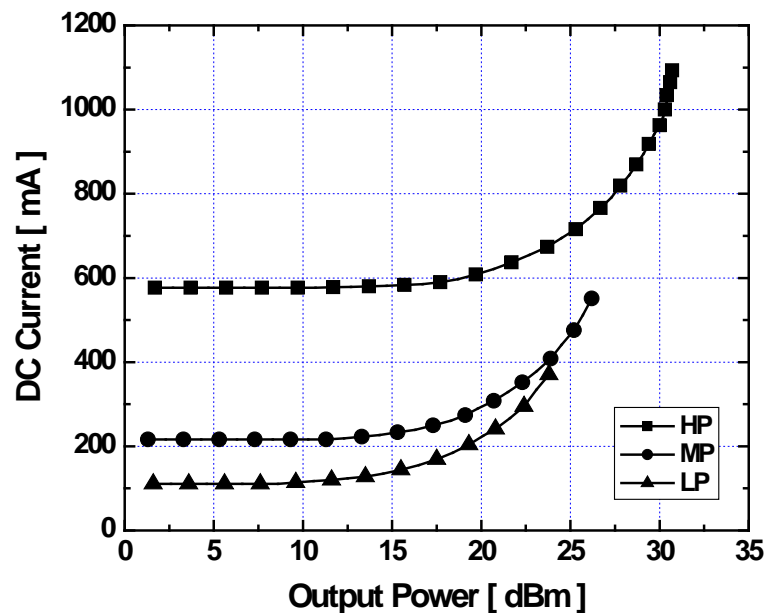
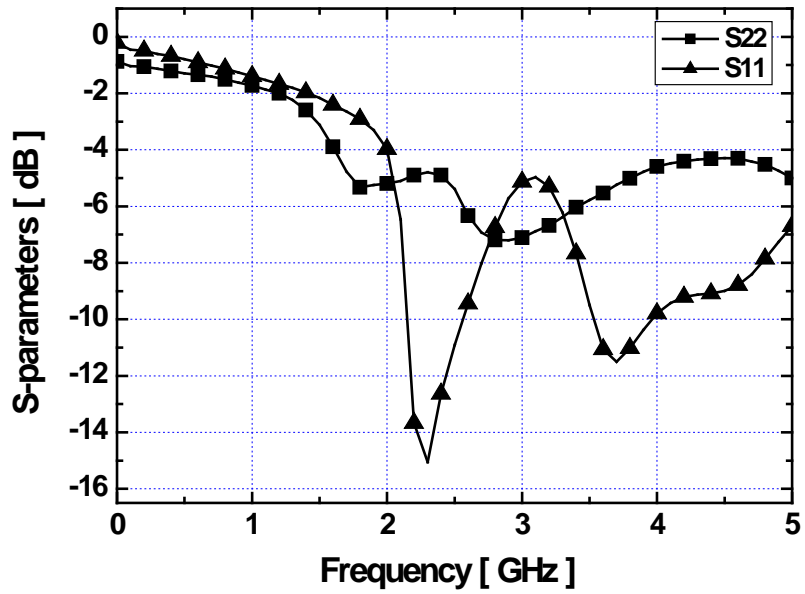
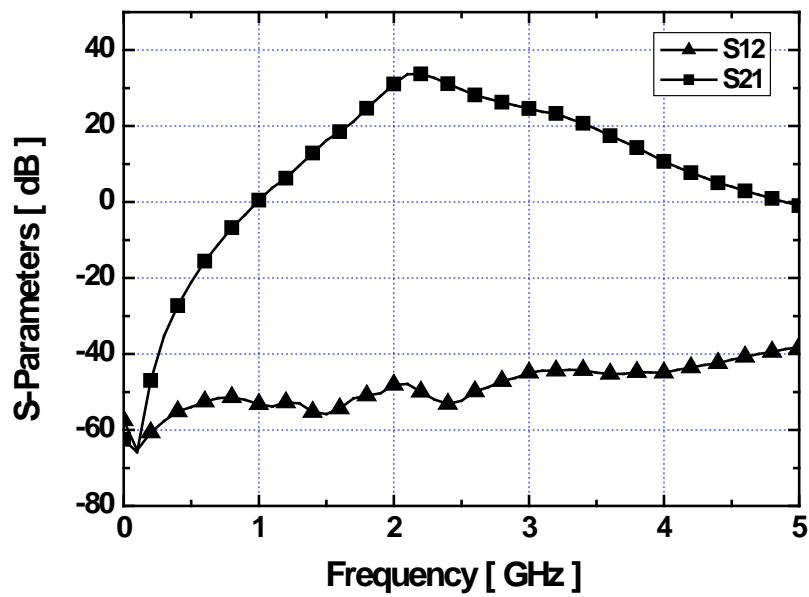


Figure 56. Measurement results of multi-mode linear PA with load impedance modulation in three operation modes: DC current (at 2.5 GHz).



(a)

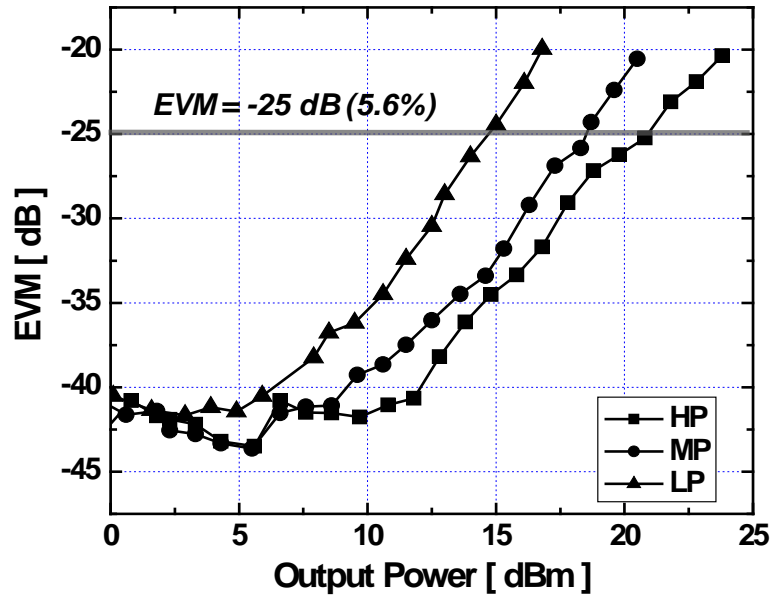


(b)

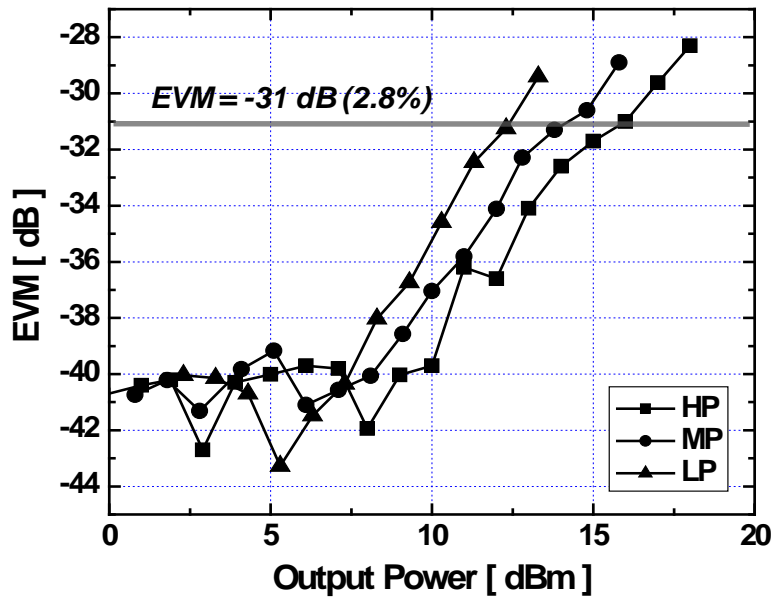
Figure 57. Measurement results of multi-mode linear PA with load impedance modulation: S-parameters. (a) S_{11} and S_{22} . (b) S_{21} and S_{12} .

HP mode operation concerning linearity as the output power level approaches P_{1dB} . The gate of CG devices of the driver stage and the power stages were biased at 3.3 V and 3 V, respectively for all measurements. The PA achieves small signal gain of 31-dB. S_{11} and S_{22} are less than -12 dB and -5 dB at 2.5 GHz, respectively.

The EVM was measured to determine the linearity of designed PA with the IEEE 802.11g WLAN OFDM 64-QAM and 802.16e WiMAX OFDM 64-QAM modulated signals at 2.5 GHz. Measured EVM for all three operation modes with two different modulated signals is presented in Figure 58(a) and (b). With WLAN 54-Mbps 64-QAM modulated signal applied, the PA meets the linearity requirement (EVM of -25 dB or 5.6%) at the output power of 21 dBm, 18 dBm, and 14.5 dBm for the HP, MP, and LP modes, respectively. For WiMAX 54-Mbps 64-QAM modulated signal (10 MHz channel band-width), the measured EVM exceeds -31-dB (2.8%) limit at the output power of 17 dBm (HP), 14.5 dBm (MP), and 12 dBm (LP). Note that the PAE of the LP mode PA at the linear output power for the WLAN 64-QAM modulated signal (P_{Linear} of 15 dBm) is about 8% with the proposed multi-mode operation scheme, while the PAE in the HP mode at the same output power is less than 4%. Therefore, the designed PA shows potential operability for WLAN/WiMAX multi-standards multi-mode applications that can support multiple modulation schemes with varying output power levels. The incorporation of proposed combining structure with discrete resizing technique using the 2-primary PCT effectively achieved optimization of the PA performance at lower power levels. Although demonstrated PA employed the PCT, other combining transformers such as SCT also can be utilized in the proposed structure. Measured constellation and output spectrum of the HP mode PA with two modulated signals are presented in Figure 59.



(a)



(b)

Figure 58. Measurement results of multi-mode linear PA with load impedance modulation in three operation modes: EVM (at 2.5 GHz). (a) For WLAN OFDM 64-QAM signal. (b) For WiMAX OFDM 64-QAM signal.

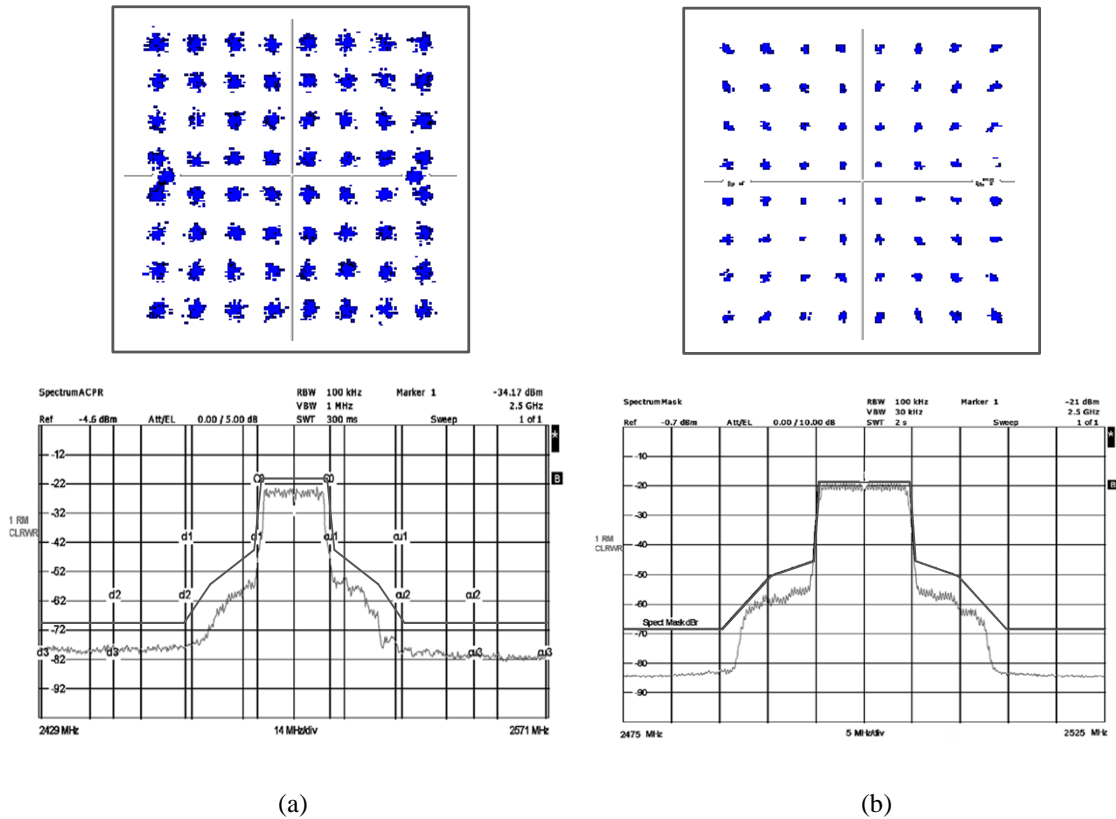


Figure 59. Measurement results of multi-mode linear PA with load impedance modulation in the high power mode: constellation and spectrum (at 2.5 GHz) (a) For WLAN OFDM 64-QAM modulated signal ($P_{out}=20.5$ dBm). (b) For WiMAX OFDM 64-QAM modulated signal ($P_{out}=16$ dBm).

3.3. Efficiency Figure-of-Merit

An indication number as a measure of efficiency enhancement at specific power back-offs can be used. Assuming that the optimal load impedance condition is preserved, we can theoretically calculate an efficiency back-off ratio (EBR) by a ratio of the efficiency at the backed-off power level to the peak efficiency as [52], [72]

$$EBR = \frac{1}{2\sqrt{10^{BO/10}}} \cdot \left(\frac{\alpha_{BO} - \sin(\alpha_{BO})}{2\sin(\alpha_{BO}/2) - \alpha_{BO}\cos(\alpha_{BO}/2)} \right) = \frac{1}{\sqrt{10^{BO/10}}}, \quad (63)$$

$$\frac{1}{2} \cdot \left(\frac{\alpha_{peak} - \sin(\alpha_{peak})}{2\sin(\alpha_{peak}/2) - \alpha_{peak}\cos(\alpha_{peak}/2)} \right)$$

where BO is the amount of power back-off in dB, α_{BO} and α_{peak} are the current conduction angles at the backed-off power and the peak output power, respectively, and the bias condition is assumed to be unchanged as the output power is reduced. This EBR represents how much low-power efficiency can be obtained with respect to the peak efficiency in a single mode PA when the amount of power back-off is specified. We can also define and obtain an achieved EBR ($EBR_{achieved}$) at the same power back-offs as

$$EBR_{achieved} = \frac{\eta_{BO}}{\eta_{peak}} \times \frac{\eta_{BO_EET}}{\eta_{BO}} = \frac{\eta_{BO_EET}}{\eta_{peak}}, \quad (64)$$

where η_{peak} is achieved (or, measured) peak efficiency, η_{BO} is achieved back-off efficiency without employing efficiency enhancement techniques, and η_{BO_EET} is achieved back-off efficiency with efficiency enhancement techniques employed. Thus, we can define the efficiency enhancement ratio at power back-offs (EER_{BO}) as

$$EER_{BO} = \frac{EBR_{achieved}}{EBR} = \sqrt{10^{BO/10}} \cdot \left(\frac{\eta_{BO_EET}}{\eta_{peak}} \right). \quad (65)$$

By using the (65) rather than using a ratio of η_{BO_EET}/η_{BO} as EER_{BO} , it is possible to reflect appropriate weighting for the amount of power back-offs and avoid exaggeration of the amount of efficiency enhancement in a case when η_{BO} is excessively lower than η_{BO_EET} .

3.4. Conclusion

The efficiency degradation effects of the power combining transformers due to idle primary inputs (in cases of open-circuited, shorted to ground, and terminated by a capacitor) are fully analyzed. To avoid efficiency degradation in lower-power modes, a concurrent resizing and combining technique has been exploited in combination with tunable matching networks to implement a fully-integrated multi-mode class-AB CMOS PA. Load impedance modulation technique using the tunable matching networks improves the performance of designed PA when operating modes of the PA changes. The measured results validate that the proposed technique can be effectively employed as a solution for multi-mode multi-standard linear CMOS PA applications. The performance comparison of state-of-the-art watt-level linear CMOS PAs is shown in Table 5.

Table 5. Performance comparison of watt-level linear CMOS PAs.

Ref.	[65]		[68]	[73]	[74]	This work		
Freq [GHz]	2.4		2.4	2.45	2.5	2.5		
Gain [dB]	37		28	32	18	31.3		
P_{1dB}/P_{sat} [dBm/dBm/]	27/31		27.7/30.1	27.5/31.5	29.5/32	28/31		
$P_{out@-25\text{-dB EVM}}$ [dBm]	22		22.7	25.5	25	21		
Peak PAE [%]	27		33	25	48	34.8		
Linearization Technique	No		Yes	Yes	Yes	No		
Multi Power Mode w/ EET	Yes		Yes	No	No	Yes		
Power Back-off [dB]	6	11	12	10	10	6	11	
PAE@ Back-off [%]	w/o EET	12	4	6	5	14.5	14	5
	w/ EET	15	6	10.4	N/A	N/A	19	14
EER_{BO}	1.11	0.79	1.25	0.63	0.96	1.09	1.43	
Supply [V]	3.3		3.3	3.3	3.3	3.3		
Size [mm ²]	2		4.32	2.7	2.25	1.98		
Technology	180 nm CMOS		90 nm CMOS	65 nm CMOS	90 nm CMOS	180 nm CMOS		

CHAPTER 4

DESIGN OF HIGH-POWER LINEAR CMOS PA WITH NOVEL POWER COMBINING TRANSFORMER

4.1. Introduction

CMOS PAs have been gaining increasing interests from the wireless communication IC industry due to their low development cost and high integration levels as mentioned in Chapter 1. From early generations of cellular applications (e.g., GSM/GPRS) to high data-rate applications with moderate transmission power levels (e.g., IEEE 802.11 a/g/n WLAN), the territory of applications for CMOS PAs has been rapidly expanded with help of novel design techniques overcoming diverse issues and challenges of silicon CMOS technologies [61], [65]-[69]. Recently, CMOS PAs have even demonstrated their suitability for more advanced wireless communication standards such as WiMAX with good achievements in output power, efficiency, and linearity performances [73]-[75]. However, it is still challenging for CMOS PAs to compete with their counterparts implemented in III-V compound semiconductor technologies (e.g., GaAs/InP/InGaP), thus more sophisticated design techniques are required to further improve performances of CMOS PAs for adaptation to next generation wireless communications.

Although linearity is one of the important performance metric of PAs, generation of high output power with good power efficiency is a more fundamental requirement for mobile applications. Due to high PAPR of OFDM-based modulation schemes that are commonly used for high data-rate communications, average output power levels for PAs

must be backed off from the peak output power level by a significant amount. With considerations of non-ideality of CMOS PAs in terms of amplitude and phase distortion, the required amount of power back-off becomes at least 8 to 9 dB for tolerable data transmission [68]. Therefore, a flat gain-response for a PA up to 30 to 31 dBm (i.e., output referred P_{1dB} of greater than 30 dBm) is required to meet a linearity specification at the average output power levels of around 22 dBm in a long-range mobile communication environment such as WiMAX. If a margin for additional loss due to a front-end switch with an antenna is taken into account, the required output power level is further increased (i.e., P_{1dB} of greater than 31 dBm).

To implement such high-power PAs in a CMOS technology with good power efficiency, transistor stacking and/or output power combining techniques have been frequently employed to overcome design issues caused by low breakdown voltage of

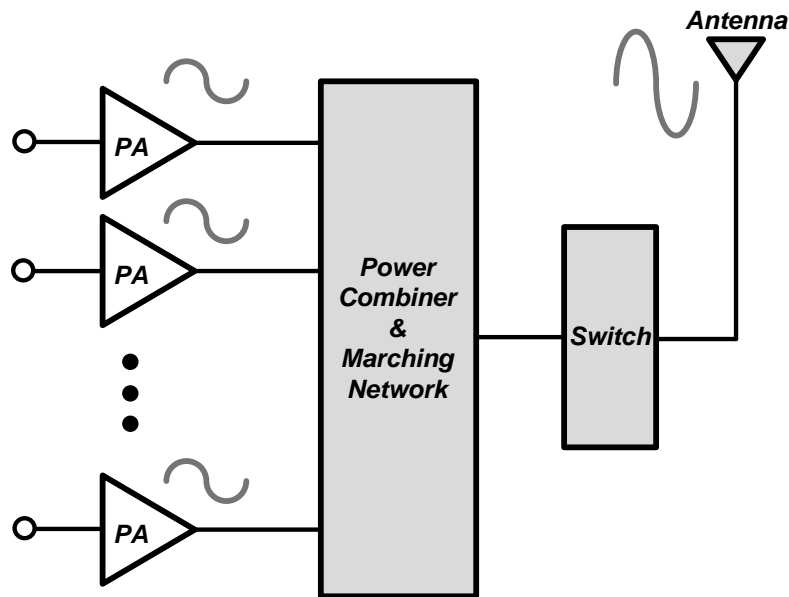


Figure 60. Output power combining technique for high-power PA applications.

MOSFET devices (Figure 60). By parallel combining of multiple PAs using an output power combining network, the requirement on the voltage swing for individual PAs can be alleviated, which results in improvements in overall linearity and efficiency. Moreover, the excessively small load impedance value that is needed to be seen by a single large PA cell can be avoided by assembling smaller sub-PA cells in parallel, so the amount of loss at the output matching networks (or the power combiner) is reduced because of lower impedance transformation ratio. The key issue is then how we can implement the low-loss monolithic power combiner in a small form-factor that can be easily integrated with the PAs in CMOS technologies.

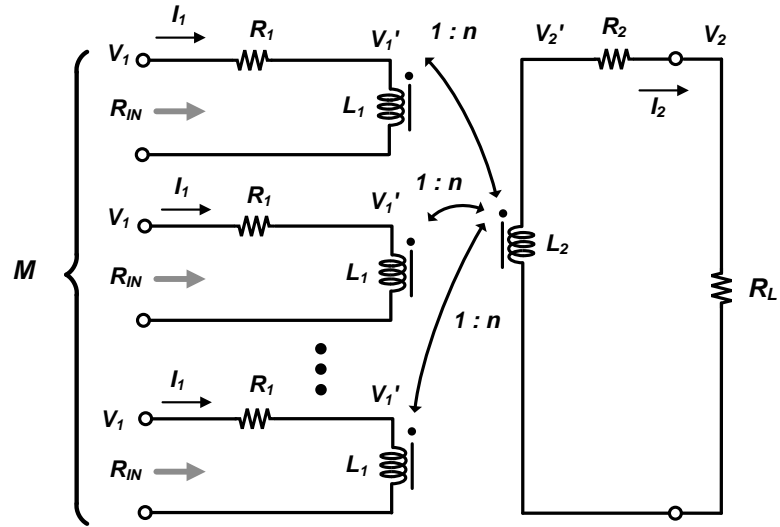
In recent years, transformer-based power combiners have attained particular attention for implementations of single-chip high-power CMOS PAs generating watt-level output power [65]-[69]. Two different types of monolithic power combining transformers: parallel-combining transformers (PCTs) and series-combining transformers (SCTs) have been successfully used thus far (These transformers are also explained in Chapter 3). Although reported high-power CMOS PAs using these transformers achieved good performance, there are still design issues and limitations in terms of feasibility of implementation and intrinsic characteristics of the transformers (e.g., efficiency and impedance transformation ratio) especially when they are incorporated to combine more than three parallel PAs to generate higher output power.

In this Chapter, we investigate characteristics of the PCT and the SCT focusing on the efficiency and transformed impedance levels at each input terminal with varying numbers of combining inputs. To overcome limitations of the PCT and the SCT, we propose a novel monolithic power combining transformer that is appropriate for

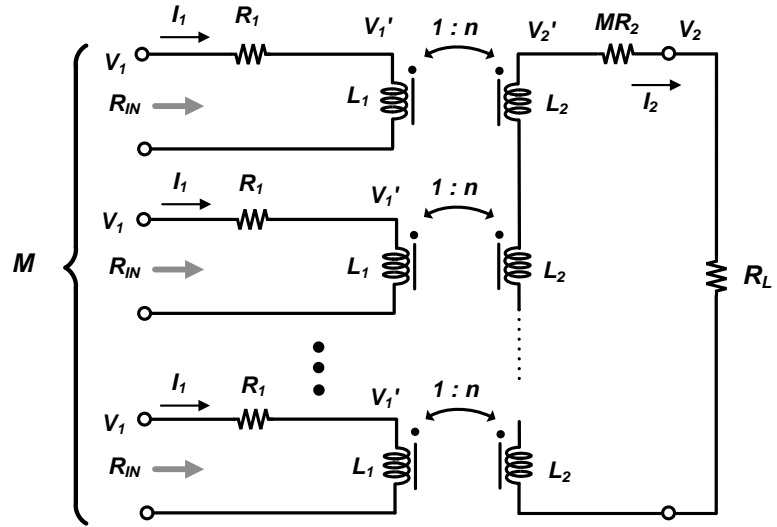
generation of output power level of greater than 33 dBm (2 W). The proposed transformer performs parallel and series combining simultaneously in a single structure to combine four sub-PAs, exhibiting an insertion loss of 0.73 dB at 2.4 GHz. Using the proposed transformer, a two-stage class-AB CMOS high-power PA for WiMAX applications is designed and demonstrated. This Chapter is organized as follows. In Section 4.2, conventional power combining transformers are characterized and compared from the perspective of high-power PA designs. Then, a new combining transformer, parallel-series combining transformer (PSCT), is introduced in Section 4.3 along with analysis and comparison to other types of combining transformers. Section 4.4 presents design example of PSCT-based CMOS PA in detail, while the measurements results and conclusions are presented in Section 4.5 and 4.6, respectively.

4.2. Conventional Power Combining Transformers: PCTs and SCTs

Schematic diagrams of conventional power combining transformers: the PCT and the SCT are illustrated in Figure 61. The transformers are composed of sub-transformers with a primary winding (L_1) and a secondary winding (L_2) that are coupled to each other. These sub-transformers are connected in parallel (PCT) or in series (SCT) to form entire combining transformers. The schematic diagrams in Figure 61 include series parasitic resistances of each primary winding (R_1) and the secondary winding (R_2). Since the SCT has secondary windings connected in series according to the number of combining inputs (M), the total series resistance at the secondary side becomes MR_2 . In contrast, the parasitic resistance at the secondary side of the PCT comes from a single secondary winding that is shared by all primary windings. I_1 and I_2 respectively represent the



(a)



(b)

Figure 61. Conventional power combining transformers. (a) PCT. (b) SCT.

primary and the secondary AC currents. V_1 is the AC voltage applied at each input terminal of the primary winding, and V_1' is the actual voltage across the primary winding, which is smaller than V_1 due to the voltage drop through the series parasitic resistance, R_1 . On the secondary side, V_2' represents the induced AC voltage across the actual secondary winding, and V_2 represents the voltage at the load, R_L . These transformers can

be used as a power combiner to implement monolithic high-power PAs. From excited input power at each input terminal at the primary side of the transformers, the output power is generated by combining the secondary AC currents (in the PCT) or the AC voltages (in the SCT). Multiple PAs can be assembled in parallel such that their outputs are combined by the transformers to effectively increase the output power level delivered to the load. These transformers also serve as an impedance transforming network with a physical turn ratio (n) between the primary and the secondary winding to step down the load impedance (50Ω) to required impedance level seen by individual PAs at the input terminals.

To characterize the power combining transformers, the efficiency and the input impedance of the transformers must be quantified. The transformer efficiency represents a ratio of the amount of delivered power at the load to the total amount of input power excited to the transformer as described in the (26) in Chapter 3. The input impedance is defined as the ratio of the input voltage to the input current at each input terminal (i.e., $R_{IN}=V_I/I_I$). While the transformer efficiency simply indicates how much power is dissipated or lost through the transformer out of transferred power to the load, the effect of the input impedance of the transformer must be considered in conjunction with sub-PA cells under specific matching conditions. Based on required output power level (accordingly, the size of the sub-PA cells and current capability), optimal load impedance value (R_{opt}) for individual sub-PA cells is determined. If the input impedance of the combining transformer is largely varied from the required value for optimal load-line matching of the sub-PA cell, the entire PA performance such as output power and efficiency will be significantly degraded.

Ignoring the finite coupling effect and the mutual inductance, the efficiency and the input impedance, R_{IN} , of both the PCT and the SCT in Figure 61 can be expressed as [69]

$$\eta_{PCT} = \frac{1}{1 + \left(\frac{n^2}{M} R_1 + R_2 \right) / R_L} \quad (66)$$

$$\eta_{SCT} = \frac{1}{1 + (Mn^2 R_1 + MR_2) / R_L} \quad (67)$$

$$R_{IN_PCT} = R_1 + \frac{M}{n^2} (R_2 + R_L) \quad (68)$$

$$R_{IN_SCT} = R_1 + \frac{1}{Mn^2} (MR_2 + R_L) \quad (69)$$

These quantities can be calculated using realistic values for R_1 and R_2 (1 Ω) assuming that the inductance of the primary winding is 1 nH with a quality-factor (Q) of 15, which is reasonable assumption based on simulated EM characteristics of the transformer. With varying n and M , calculated input impedance and efficiency for both transformers are summarized in Table 6 and graphically presented in Figure 62 and 63.

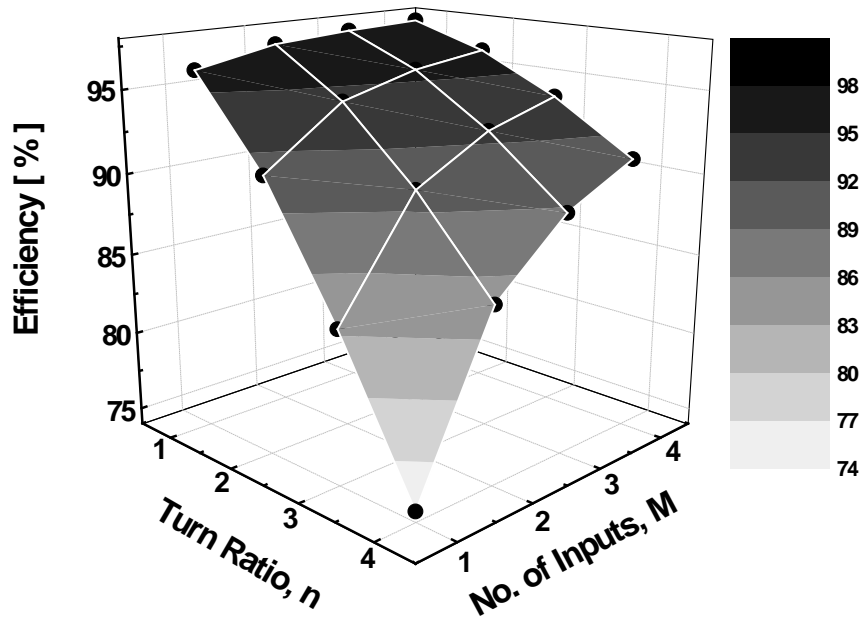
As indicated in equations above and observed from plotted graph in Figure 62 and 63, the input impedance and the efficiency of the PCT is directly proportional to the number of combining inputs, M , whereas those of the SCT is inversely proportional to M (Note that these values do not account for power leakage due to non-ideal electromagnetic (EM) coupling between the primary and the secondary winding inductors). These relations imply that the PCT may be superior to the SCT in terms of the efficiency especially when a large M is required. This is because the SCT has a larger series resistance at the secondary side, which is a critical factor for the efficiency degradation.

Table 6. Calculated input impedances and efficiencies of the combining transformers.

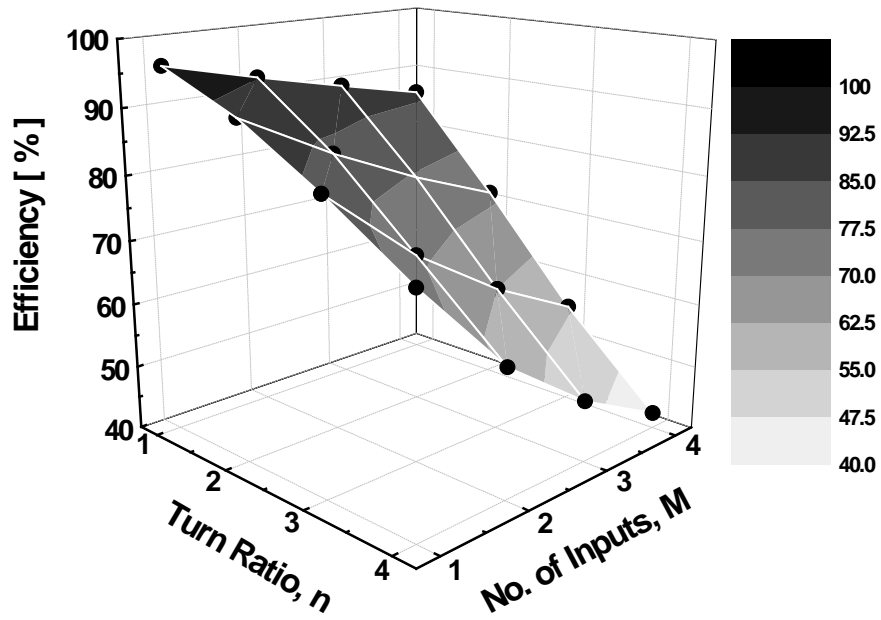
Turn ratio, n	No. of inputs, M	Efficiency (%)		$R_{IN} (\Omega)$	
		PCT	SCT	PCT	SCT
1	1	96.2	96.2	52	52
1	2	97.1	92.6	103	27
1	3	97.4	89.3	154	18.7
1	4	97.6	86.2	205	14.5
2	1	90.9	90.9	13.75	13.8
2	2	94.3	83.3	26.5	7.5
2	3	95.5	76.9	39.25	5.4
2	4	96.2	71.4	52	4.4
3	1	83.3	83.3	6.7	6.7
3	2	90.1	71.4	12.3	3.9
3	3	92.6	62.5	18	3
3	4	93.9	55.5	23.7	2.5
4	1	74.6	74.6	4.2	4.2
4	2	84.7	59.5	7.4	2.6
4	3	88.8	49.5	10.6	2.1
4	4	90.9	42.4	13.8	1.8

The amount of the secondary series resistance of the SCT is proportionally increased as the number of combining inputs, M , is increased, significantly degrading the transformer efficiency. In contrast, the secondary winding of the PCT is equally shared by all primary windings, and the number of the secondary windings does not need to be increased for larger M (i.e., there is only one secondary winding with fixed physical size). This superiority of the PCT becomes more apparent when higher turn ratios are used since multi-turn windings have longer physical lengths and larger series resistance.

However, it is not practical to choose the PCT to combine more than three PAs for two reasons. The first reason is the difficulty in physical implementation of the PCT with a large M . For the parallel combining using planar inductors, multiple primary

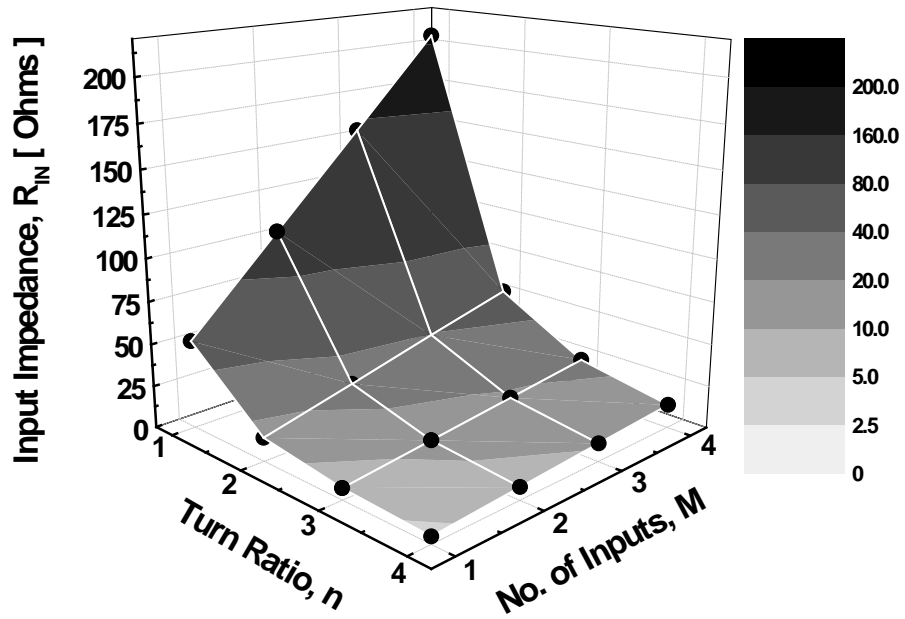


(a)

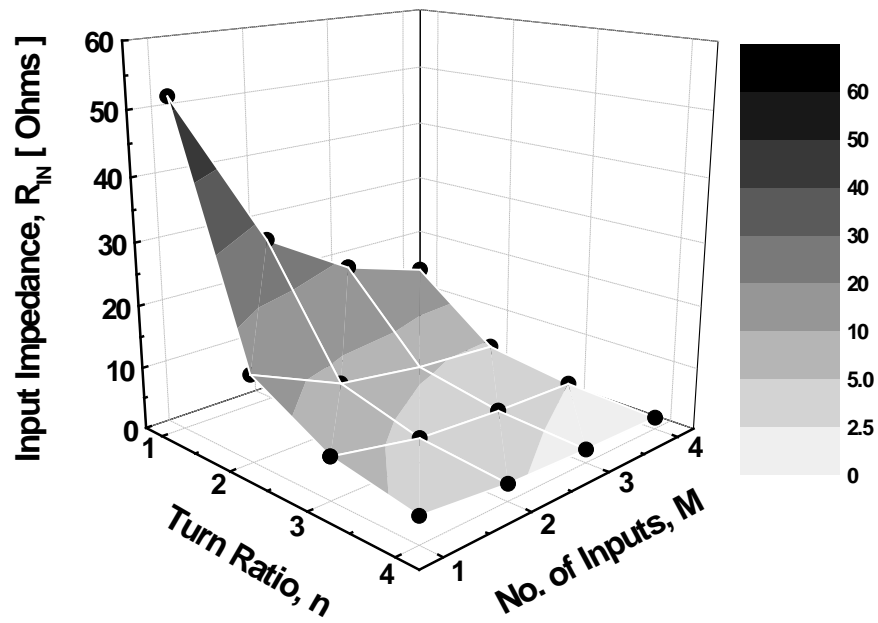


(b)

Figure 62. Calculated efficiencies of the power combining transformers with varying turn ratio (n) and the number of combining inputs (M). (a) For the PCT. (b) For the SCT.



(a)



(b)

Figure 63. Calculated input impedances of the power combining transformers with varying turn ratio (n) and the number of combining inputs (M). (a) For the PCT. (b) For the SCT.

windings must be evenly interwoven with the secondary winding to achieve equal coupling coefficient preserving equal self-inductances of the primary windings. An unequal coupling coefficient and winding inductances will cause mismatches between distributed RF signals in each combining path, consequently generating distortion at the output signal. Even distribution and placement of more than three primary windings coupled to one secondary winding in a planar structure is difficult to implement. If higher turn ratios are required, implementation of the transformer becomes more challenging. Secondly, the PCT with $M > 3$ has an excessively large input impedance transformed from the load impedance (50Ω), which is undesirable for PA designs. For example, the PCT with $M=4$ and $n=1$ exhibits very large input impedance (205Ω), thus additional matching network must be employed to down-transform the impedance to an acceptable level. However, overall loss at the output matching network will be substantially large due to such a high impedance transformation ratio. Although the excessively large input impedance value of the PCT with large M can be lowered by choosing larger value of the turn ratio ($n > 3$), the PCT with larger turn ratio is not realizable as fore-mentioned.

Therefore, the SCT seems to be a more appropriate option to implement a high-power PA combining more than three sub-PAs. For example, the SCT with $M=4$ and $n=1$ has the input impedance close to the optimal load impedance value for the individual sub-PAs (i.e., the sub-PA cell for 28-dBm output power under 3.3-V supply requires around $15\text{-}\Omega R_{opt}$, and the SCT with $M=4$ and $n=1$ exhibits R_{IN} of 14.5Ω). However, the large series resistance of the secondary winding, which is proportionally increased with increasing number of combining inputs, severely degrades the transformer efficiency. The large physical size of the SCT with large M is another design hurdle toward the

implementation of compact single-chip PAs (e.g., the SCT with $M=4$ requires four primary windings placed side by side and four serially connected secondary windings coupled to all primary windings [66]).

In short, both the PCT and the SCT are not practical solutions to implement a single-chip high-power CMOS PA combining more than three sub-PAs. Although the SCT with $n=1$ is a plausible choice to implement a high-power PA by combining four PAs, its limited efficiency and large size must be further improved.

4.3. Parallel-Series Combining Transformer (PSCT)

To resolve the contradiction in the characteristics between the PCT and the SCT, a novel approach to implement compact and efficient power combining transformer is proposed. The proposed transformer is a combination of the PCT and the SCT, and performs parallel (current) combining and series (voltage) combining at the same time. This parallel-series combining transformer, or PSCT, can generate adequate input impedance levels independent of the number of combining inputs when the numbers of parallel-combining and series-combining are preserved to be same, which is advantageous as compared to the conventional combining transformers that have varying input impedance values with a varying M . In addition, the PSCT effectively halves the number of secondary windings as compared to the SCT for the same number of total combining inputs, which leads to improved efficiency and reduced overall transformer size.

4.3.1. Characteristics of the PSCT

The structure of proposed PSCT is presented in Figure 64. There are N_P -primary windings that are coupled to one secondary winding (i.e., N_P -parallel-combining) and N_S -sets of N_P -parallel combining transformers connected in series via multiple secondary windings (i.e., N_S -series-combining). Thus, proposed transformer performs N_P -parallel-combining and N_S -series-combining simultaneously in a single structure, and effective

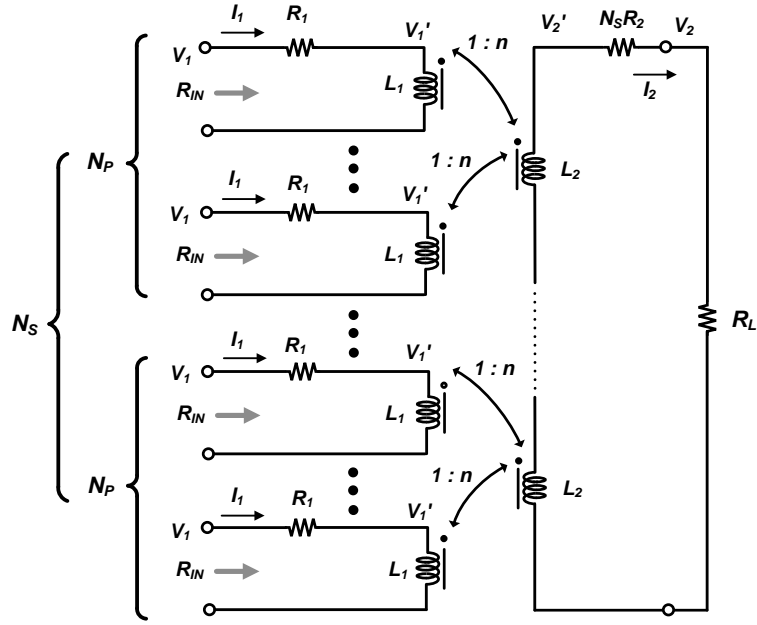


Figure 64. Schematic diagram of proposed PSCT.

number of combining inputs becomes $M=N_P N_S$. Ignoring the non-ideal coupling effect, relations for voltages and currents at each node in Figure 64 can be obtained as

$$nN_S V_1' = V_2' \quad (70)$$

$$V_1' = V_1 - I_1 R_1 \quad (71)$$

$$V_2 = V_2' - I_2 N_S R_2 \quad (72)$$

$$nI_2 = N_P I_1 \quad (73)$$

$$R_L = \frac{V_2}{I_2}, \quad (74)$$

and the efficiency of the transformer and the transformed input impedance at each input terminal can be derived as

$$\eta_{PSCT} = \frac{1}{N_p N_s} \frac{I_2 V_2}{I_1 V_1} = \frac{1}{1 + \left(\frac{N_s}{N_p} n^2 R_1 + N_s R_2 \right) / R_L} \quad (75)$$

$$R_{IN_PSCT} = \frac{V_1}{I_1} = R_1 + \frac{N_p}{N_s} \frac{1}{n^2} (R_L + N_s R_2). \quad (76)$$

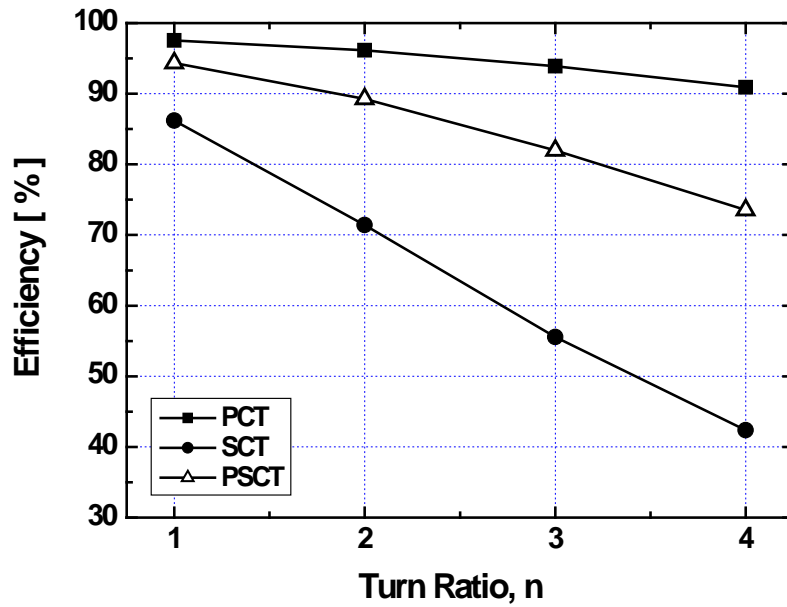
It is observed that the efficiency of the PSCT is less sensitive to the series resistance of the primary winding (R_1) when N_p equals N_s . In contrast to the PCT or the SCT, the effect of R_1 on the efficiency of the PSCT becomes independent of the number of combining inputs in this case (i.e., $N_p=N_s$). However, the secondary series resistance (R_2) still dominantly affects the efficiency in accordance with the number of series combining inputs (N_s) as in the SCT, but its effect is mitigated due to the reduced number of series combining inputs for the same number of total combining inputs (i.e., $M=2N_s$ if $N_p=N_s$). We can expect that the efficiency of the PSCT will be lower than that of the PCT because of the series combining parts, but higher than that of the SCT if the inductances of primary and secondary windings are assumed to be same for both transformers.

Unlikely for the conventional combining transformers, the input impedance of the PSCT can also be independent of the number of combining inputs when N_p becomes equal to N_s . In other words, for any number of combining inputs with equal N_p and N_s , the PSCT exhibits almost constant input impedance that is only dominantly dependent on the turn ratio, n . In an ideal case, the input impedance is simply expressed as

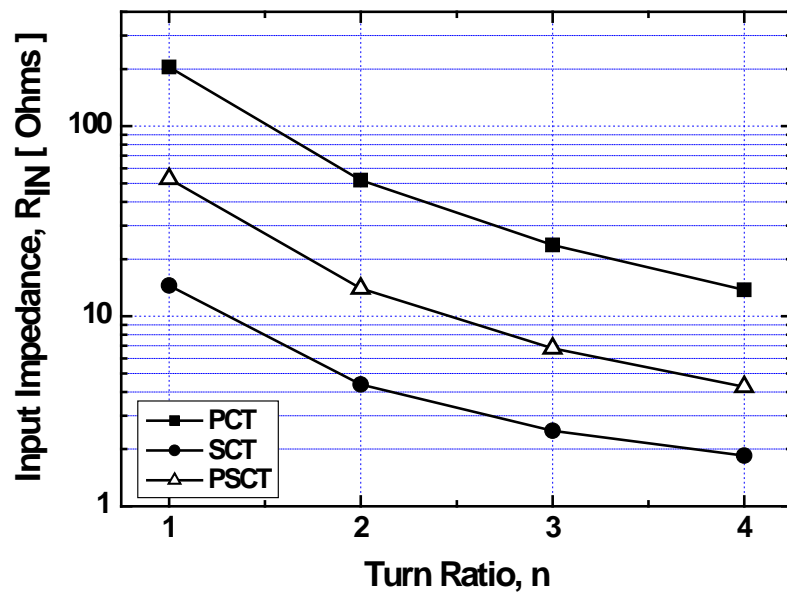
$$R_{IN_PSCT} = \frac{R_L}{n^2}. \quad (77)$$

Thus, we can implement the combining transformer that realizes required input impedance by only determining the turn ratio of parallel combining part. Avoiding the effect of the number of combining inputs on the input impedance, the proposed transformer can have more degrees of freedom in designing PAs. The efficiency and input impedance of three power combining transformers: PCT, SCT, and PSCT with four combining inputs ($M=4$) are calculated and compared in Figure 65. For the case of $n=2$, the PSCT has an R_{IN} of 14Ω with an efficiency of 89.3 %, while the SCT with $M=4$ and $n=2$ shows an R_{IN} of 4.4Ω with an efficiency of 71.4 %. It is more reasonable to compare the PSCT with $M=4$ and $n=2$ to the SCT with $M=4$ with $n=1$ considering their comparable input impedance values (i.e., R_{IN} of 14Ω for the PSCT and 14.5Ω for the SCT). Even in this comparison, the PSCT has a higher efficiency than that of the SCT (86.2 %).

A more realistic equation for the efficiency of the PSCT with N_p -parallel-combining and N_s -series-combining can be derived including non-ideal coupling effect between the primary and the secondary windings (i.e. considering finite coupling coefficient and mutual inductance between L_1 and L_2). Each transformer can be replaced with a T-equivalent model [70] as presented in Figure 66. Due to finite coupling coefficient ($k < 1$), there exists leakage inductance at each primary and the secondary side. At the secondary side, the leakage inductance of a single secondary winding is magnified by series-combining part and distributed by parallel-combining part to form an effective leakage inductance of $N_s(1-k)L_2/N_p$. First, we define the overall impedance at the secondary side excluding the ideal transformer as



(a)



(b)

Figure 65. Calculated efficiencies and input impedances of three power combining transformers: PCT, SCT, and PSCT with four combining inputs ($M=4$). (a) Efficiencies. (b) Input impedances.

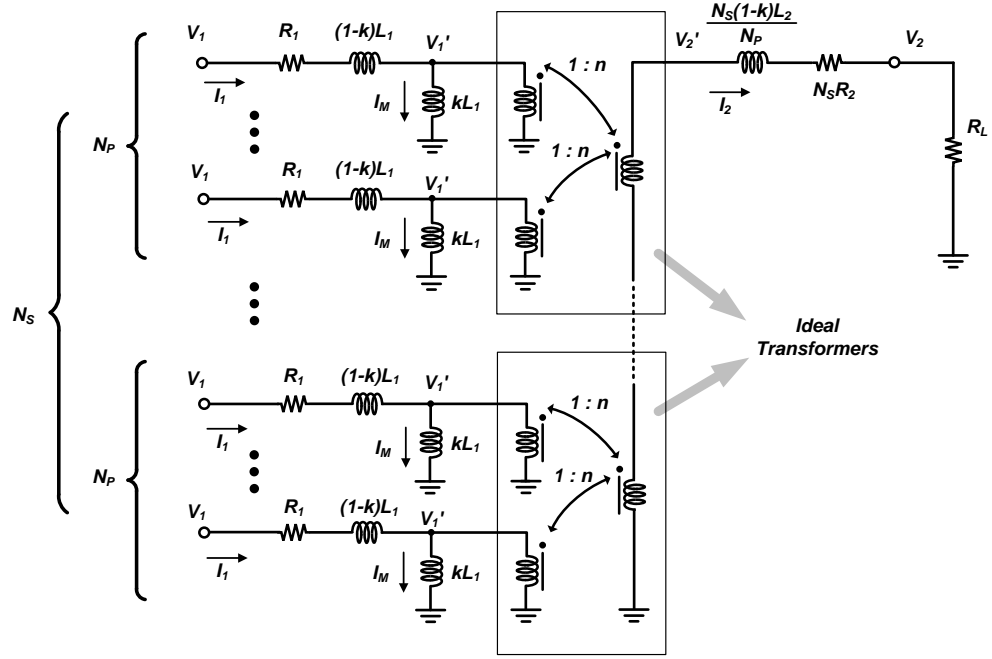


Figure 66. Schematic diagram of proposed PSCT with T-equivalent transformer model to account for non-ideal coupling effect.

$$Z_2 = j\omega \frac{N_S}{N_P} (1-k)L_2 + N_S R_2 + R_L. \quad (78)$$

From voltages and currents at each node, we can obtain following relations:

$$N_S n V_1' = V_2' \quad (79)$$

$$I_M = \frac{V_2'}{j\omega k L_1 N_S} = \frac{I_2 Z_2}{j\omega k L_1 N_S} \quad (80)$$

$$I_1 = \frac{n I_2}{N_P} + I_M = \frac{n I_2}{N_P} + \frac{I_2 Z_2}{j\omega k L_1 N_S} = I_2 \left(\frac{n}{N_P} + \frac{Z_2}{j\omega k L_1 N_S} \right). \quad (81)$$

We can define a current transfer factor, F , as

$$\frac{1}{F} = \frac{n}{N_P} + \frac{Z_2}{j\omega k L_1 N_S}, \quad (82)$$

thus the secondary current, I_2 , is expressed as a function of the primary current, I_1 , as

$$I_2 = F \cdot I_1. \quad (83)$$

The input voltage, V_1 , is then derived as

$$V_1 = I_1 (R_1 + j\omega(1-k)L_1) + \frac{I_2 Z_2}{nN_s} = I_2 \left(\frac{1}{F} (R_1 + j\omega(1-k)L_1) + \frac{Z_2}{nN_s} \right), \quad (84)$$

and the efficiency of the PSCT can be obtained as

$$\eta_{PSCT} = \frac{1}{N_s N_p} \left(\frac{\text{Re}(I_2 V_2^*)}{\text{Re}(I_1 V_1^*)} \right) = \frac{1}{N_s N_p} \cdot \frac{R_L}{\text{Re} \left(\frac{1}{F} \left(\frac{R_1 + j\omega(1-k)L_1}{F} + \frac{Z_2}{nN_s} \right)^* \right)}. \quad (85)$$

4.3.2. Implementation of the PSCT

As observed from the previous section, the PSCT can supplement drawbacks of the conventional on-chip power combining transformers for high-power PA designs. We can legitimize the utilization of the PSCT for the following reasons:

1. To implement a high-power PA with greater than 33-dBm output power, it is practical to have four sub-PAs with 28-dBm individual output power ($R_{opt}=14 \Omega$), assuming about 1-dB insertion loss at the power combiner.
2. The PCT with four primary inputs is not a plausible option due to difficulty in physical implementation.
3. The 4-primary 1:1 SCT (i.e., $M=4$ and $n=1$) is suitable to use in terms of transformed input impedance ($R_{IN}=14.5 \Omega$), but its size is excessively large due to serially connected secondary windings.
4. The PSCT with two parallel combining inputs ($N_p=2$) and two series combining inputs ($N_s=2$) having $n=2$ for parallel combining parts exhibits appropriate input impedance ($R_{IN}=14 \Omega$). In addition, its size is approximately

half of the 4-primary 1:1 SCT because the number of series-combining is halved, which results in higher or comparable efficiency (depending on the actual dimension of implemented transformer).

Therefore, we propose a 4-primary 1:2 PSCT (i.e., $M=4$ and $n=2$) as illustrated in Figure 67. There are four primary inputs that are supposed to be connected to the outputs of

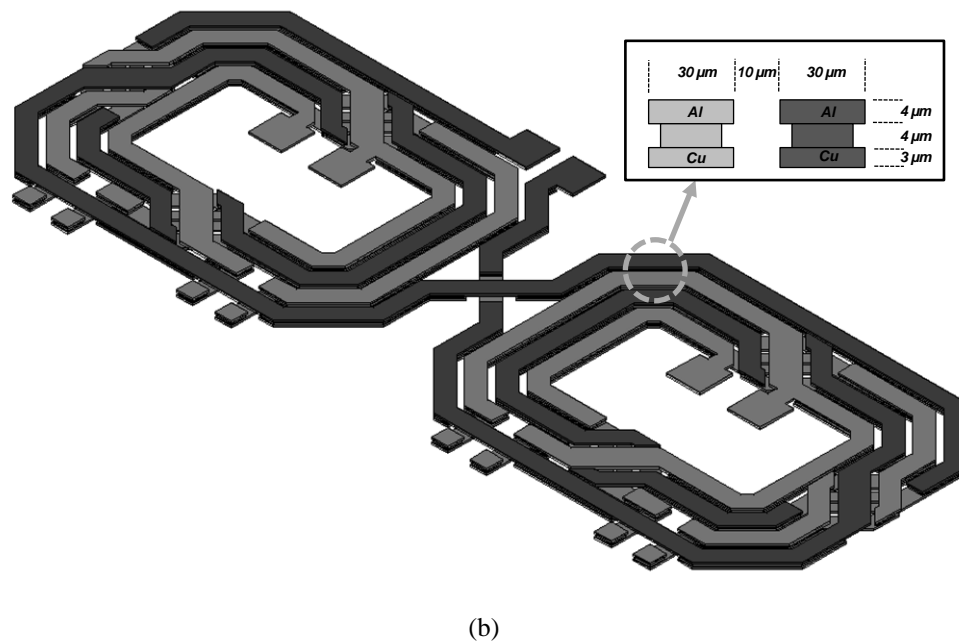
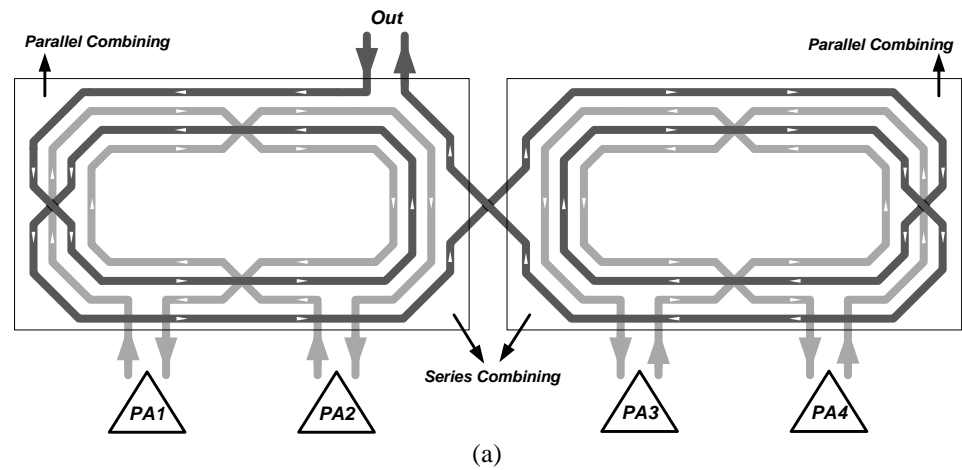


Figure 67. Implementation of proposed 4-primary 1:2 PSCT (a) Conceptual diagram. (b) Actual layout.

individual PAs. Two PCTs are composed of two primary windings that are interwoven with each other to achieve equal coupling effects to the secondary winding with a turn ratio of $n=2$, and are connected in series. Thus, the transformer performs a series-combining of two parallel-combining parts (i.e., $N_P=N_S=2$). The turn ratio of $n=2$ was chosen to realize the impedance transformation ratio of 1:4 based on the (77). The size of winding inductors must be carefully decided based on iterative EM simulations because it affects the optimal operating frequency and the bandwidth of the transformer in terms of the efficiency. The primary inductance of 1 nH was selected for this design. Since the transformer was implemented using two thick metals (4- μm thick aluminum and 3- μm thick copper) that are connected through whole via trace as presented in Figure 67(b), high- Q winding inductors can be realized. The width of windings and the spacing between adjacent windings are 30 μm and 10 μm , respectively. EM simulations using Ansoft HFSS were performed to characterize the PSCT. The simulation setup is shown in Figure 68. Because the PSCT is the series connection of two PCTs, only half-section of the PSCT, which is the 1:2 PCT with two primary inputs, can be simulated to characterize the self-inductance of the primary and the secondary windings (L_1 and L_2), the mutual inductance (M) and the coupling coefficient (k) between the primary and the secondary winding, the quality factors of the primary and secondary winding (Q_1 and Q_2), and the effective turn ratio (n). These parameters can be obtained with following equations:

$$L_{1,2} = \frac{\text{Im}(Z_{11} + Z_{22} - 2Z_{12})}{\omega} \quad (86)$$

$$Q_{1,2} = \frac{\text{Im}(1/Y_{11})}{\text{Re}(1/Y_{11})} \quad (87)$$

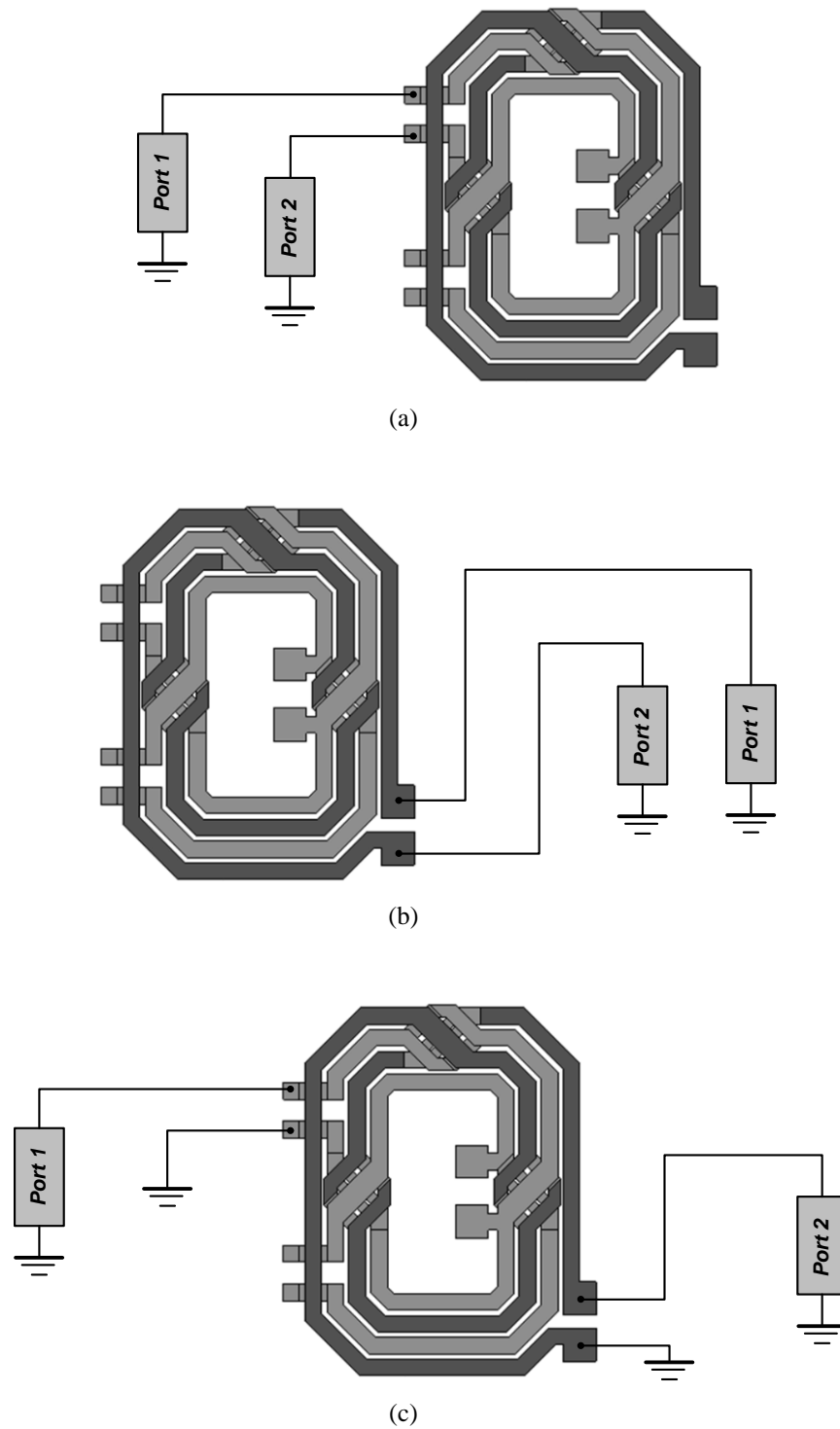


Figure 68. Simulation setup for characterization of half-section PSCT. (a) For the primary winding. (b) For the secondary winding. (c) For the coupling effect and the mutual inductance.

$$M = \frac{Im(Z_{12})}{\omega} \quad (88)$$

$$k = \frac{M}{\sqrt{L_1 L_2}} \quad (89)$$

$$n = \sqrt{\frac{L_2}{L_1}} \quad (90)$$

The transformer efficiency based on the calculation of maximum available gain is given by

$$\eta = 10^{\frac{MaxGain(dB)}{10}} \times 100 \quad (91)$$

Table 7 summarizes the EM characteristics of the half-section PSCT. The efficiency of the entire PSCT structure was also obtained from the EM simulation. the PSCT achieves a maximum available efficiency of 84% at 2.4 GHz (i.e., insertion loss of 0.73 dB) when it has differential configuration and 73.5% when it has single-ended configuration.

Table 7. EM characteristic of the half-section of the PSCT (at 2.4 GHz).

L_1	0.925 nH
L_2	3.17 nH
R_1	1.125 Ω
R_2	2.634 Ω
Q_1	13.2
Q_2	17.9
M	1.045 nH
k	0.65
n	1.85
<i>Efficiency</i>	88%

The conventional 4-primary 1:1 SCT was also implemented and simulated to compare its performance to the proposed structure. Layout of the PSCT and the SCT with 4-primary inputs are illustrated in Figure 69. As mentioned in the previous section, the size of the SCT ($2.72 \times 0.55 \text{ mm}^2$) is almost twice of the size of the PSCT ($1.43 \times 0.58 \text{ mm}^2$). The simulated insertion losses and transformed input impedance of these two

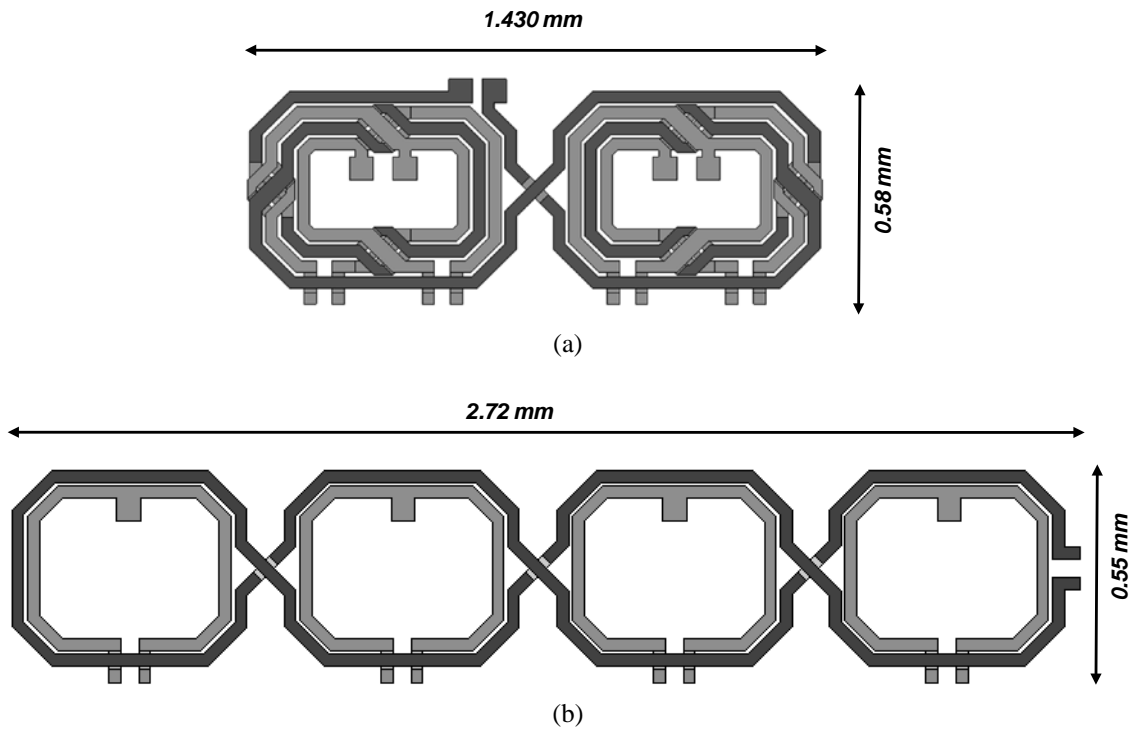
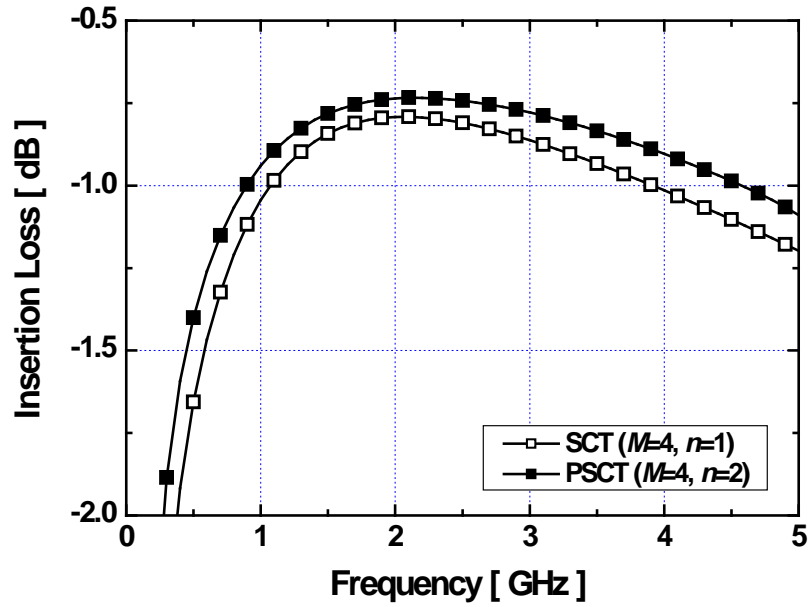
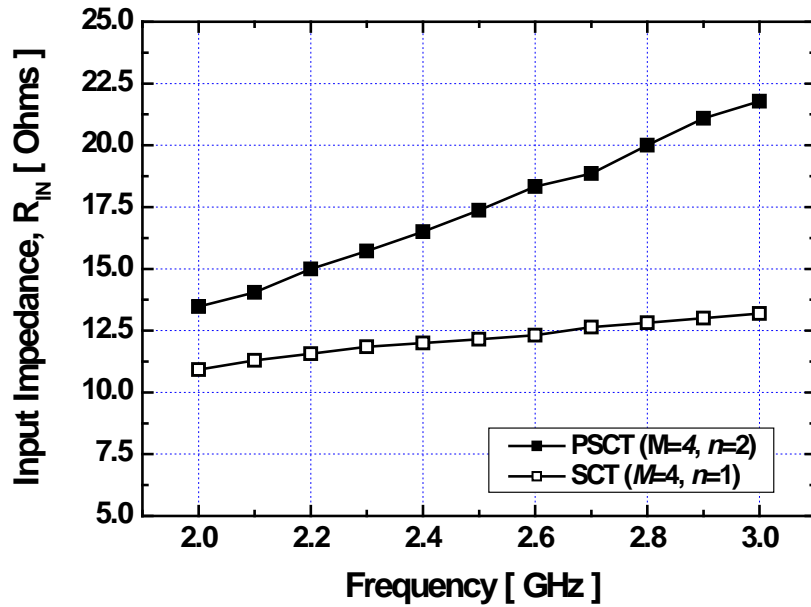


Figure 69. Size comparison between the proposed PSCT and SCT. (a) proposed PSCT ($M=4, n=2$). (b) SCT ($M=4, n=1$).

transformers are compared in Figure 70. While the SCT exhibits an insertion loss of 0.85 dB at 2.4 GHz, the PSCT achieves a lower insertion loss of 0.73 dB due to the reduced number of series combining parts. The input impedance of the PSCT is 16.5Ω at 2.4 GHz, which is very close to the required load impedance for individual PAs (R_{opt}) to generate targeted output power. The SCT has relatively lower input impedance levels



(a)



(b)

Figure 70. Simulated performances of the proposed PSCT ($M=4, n=2$) and SCT ($M=4, n=2$). (a) Insertion loss. (b) Input impedance.

because the secondary winding is surrounding the primary windings on the outer side, which results in larger secondary self-inductance of each coupled part leading to a higher effective turn ratio. Additional inductance at the cross-section area of the adjacent primary windings also increases the effective turn ratio, lowering transformed input impedance.

4.4. Design of a PSCT-based High-Power CMOS PA

4.4.1. Structure of the PSCT-based CMOS PA

Using the proposed PSCT, a fully-integrated PA is implemented in CMOS technology. The diagram of the proposed PA structure is presented in Figure 71. There are four PA branches that are combined by the PSCT at the output. Adjacent two PA branches are combined in parallel (i.e., output AC currents are combined), and two sets of

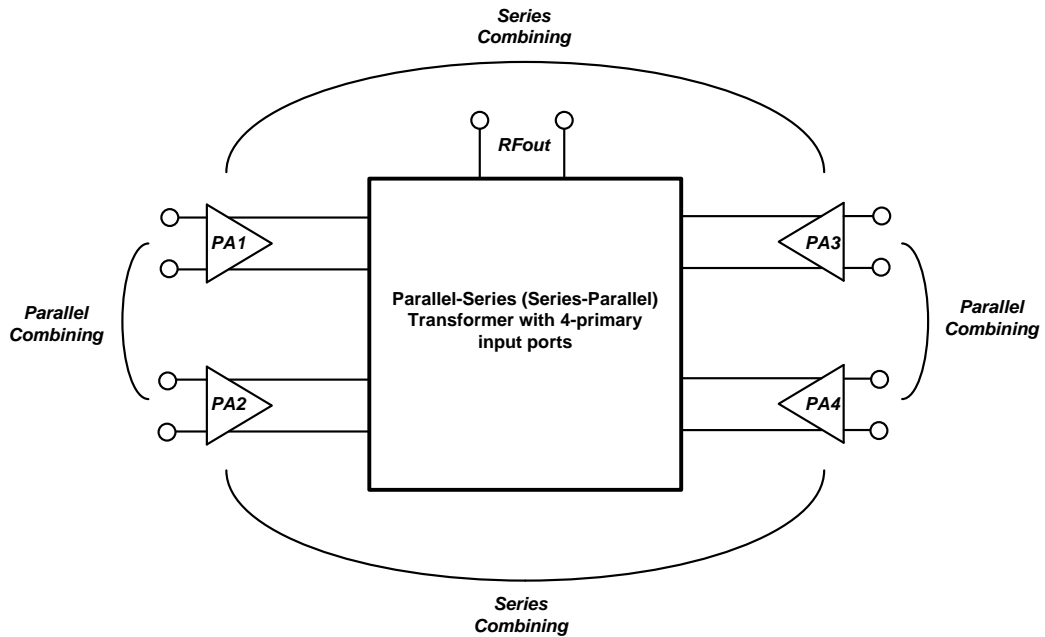


Figure 71. Diagram of proposed PSCT-based high-power linear PA.

parallel combinations are connected in series (i.e., output AC voltages are combined). The PSCT performs not only the power combining but also the impedance down-transformation that is realized by the turn ratio between the primary and the secondary windings. Thus, additional output matching networks are unnecessary (except for shunt capacitors to tune out the reactive component at the drain node of sub-PAs). The entire PA system consists of a driver stage and a combined power stage that are interconnected by LC matching network. An on-chip transformer as an input balun is used along with capacitive matching network to convert a single-ended external signal to a differential internal signal. The schematic diagram of proposed PA is presented in Figure 72.

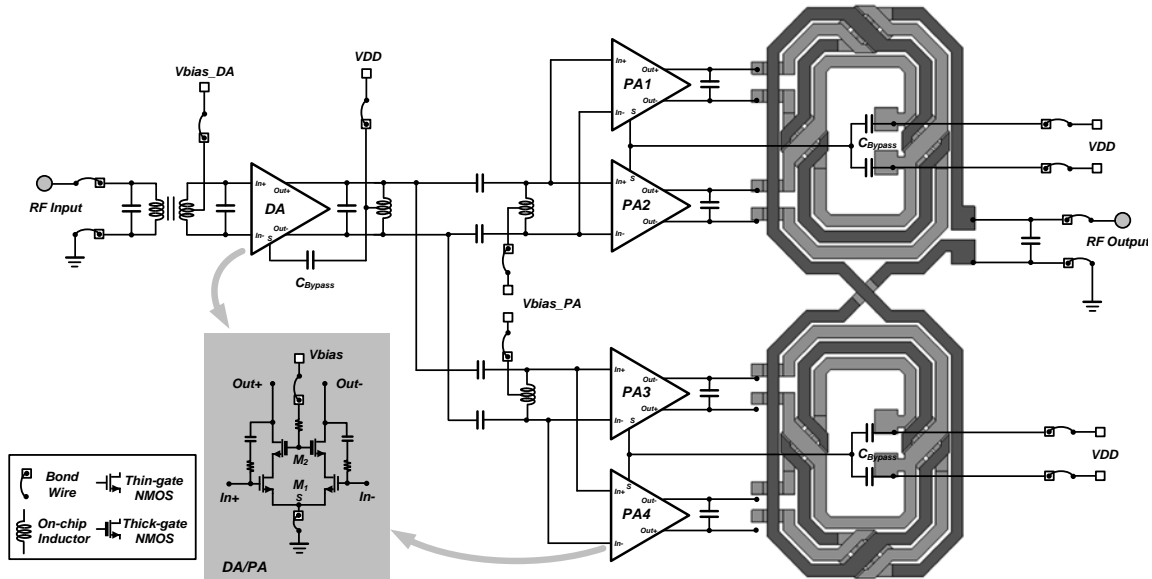


Figure 72. Schematic diagram of designed CMOS PA using the PSCT as a power combiner.

4.4.2. Circuit Design

The driver and power stage amplifiers are pseudo differential amplifiers with cascode configuration. The thick gate-oxide transistors ($L=0.4 \mu\text{m}$) are used for the

common gate (CG) devices (M_2) in the driver and power stage amplifiers to avoid the device breakdown issues. The width of common source (CS) devices (M_1) in the power stage amplifiers is $3072 \mu\text{m}$ (384 fingers with the unit finger width of $8 \mu\text{m}$). This device size was determined through the load-pull simulation in the Agilent ADS in such a way that each power-cell can generate the maximum output power of 28 dBm with reasonable efficiency. The size of the CG devices in the power stage amplifiers is $3936 \mu\text{m}$ (492 fingers with the unit finger width of $8 \mu\text{m}$). Because four power-cells are combined in parallel, effective cell size of the entire power stage becomes 12.288 mm ($3072 \mu\text{m} \times 4$). The cell size of the driver stage is determined in such a way that the output power of the driver stage amplifier is not compressed until the output power of the entire power stage begins to compress. Considering the gain of the combined power stage, a minimum $P_{1\text{dB}}$ level of the driver stage amplifier can be obtained, and the size of one-fifth of the entire power stage ($2560 \mu\text{m}$, 321 fingers with the unit finger width of $8 \mu\text{m}$) was chosen for this design. Multiple bonding-wires are used to ground the source of the driver and power stages amplifiers to minimize the effect of wire inductance and resistance. To reduce the second-order distortions, large bypass capacitors (C_{bypass}) are used to connect the center-tab of the primary windings of the PSCT to source of each power stage amplifiers. While the stability of the entire PA system may be degraded with excessively large C_{bypass} , a small capacitance may reduce the gain of the PA system. Therefore, the size of the bypass capacitor must be carefully chosen compromising the gain and the stability of the PA. 12-pF for C_{bypass} was chosen for this design. Each cascode differential amplifier has a resistive feedback network from the drain of the CG transistors to the gate of the CS transistors to improve AM-AM characteristic and stability. DC supply currents for the

driver and power stage are fed through the center-tab of the differential inductor or the transformer. Since no bonding-wires are included in the matching network, accurate frequency matching can be realized. The CS transistors are biased by external voltage source applied to the gate through large resistors. The power stage amplifiers are biased for class-AB operation for good efficiency and linearity. The driver stage is biased to act more like a class-B (i.e., deep class-AB) amplifier to maximize the efficiency. The deep class-AB operation also expands the gain of the driver stage amplifier and compensates for the gain compression of the power stage amplifiers. Expanded gain (or better AM-AM characteristic) is beneficial to achieve better EVM performance for the entire PA system.

4.4.3. Measurement Results

The high-power linear CMOS PA has been fabricated in 0.18- μm CMOS (IBM 1P6M) technology. A micro-photograph of fabricated PA is presented in Figure 73. The PA has the size of 2.1 x 1.64 mm². The PA chip was mounted on the FR-4 PCB for measurements. The PCB line loss (0.3 dB) was de-embedded to obtain actual PA performances. However, the effect of bonding-wires is included in the measurement results. The gain, $P_{1\text{dB}}$, P_{sat} , and PAE were measured with single-tone continuous wave signal. The gate bias voltages for the driver and power stages amplifiers are 0.43 V and 0.46 V, respectively, at which the overall PA has the highest $P_{1\text{dB}}$ with small gain variation. The gate bias voltages for the CG devices in the driver and power stage amplifiers are chosen to be 3.3 V and 3.2 V, respectively. Relatively higher bias voltage for CG devices improves AM-AM performance of the PA with small penalty in the

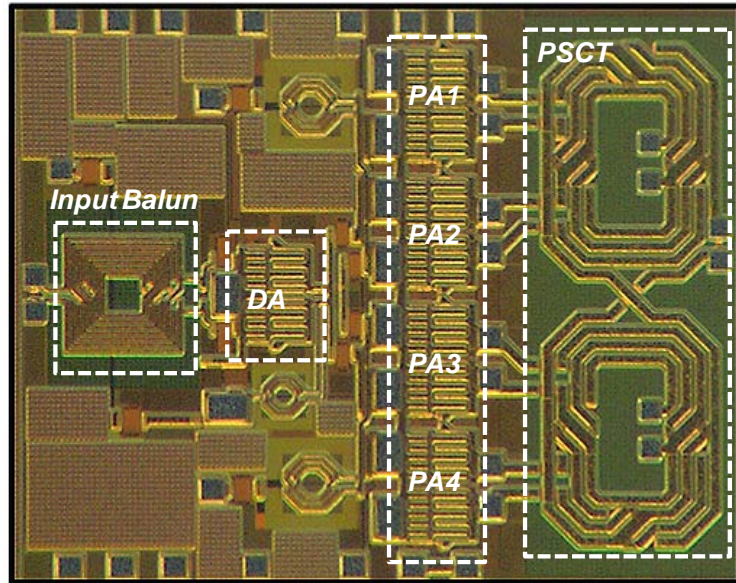
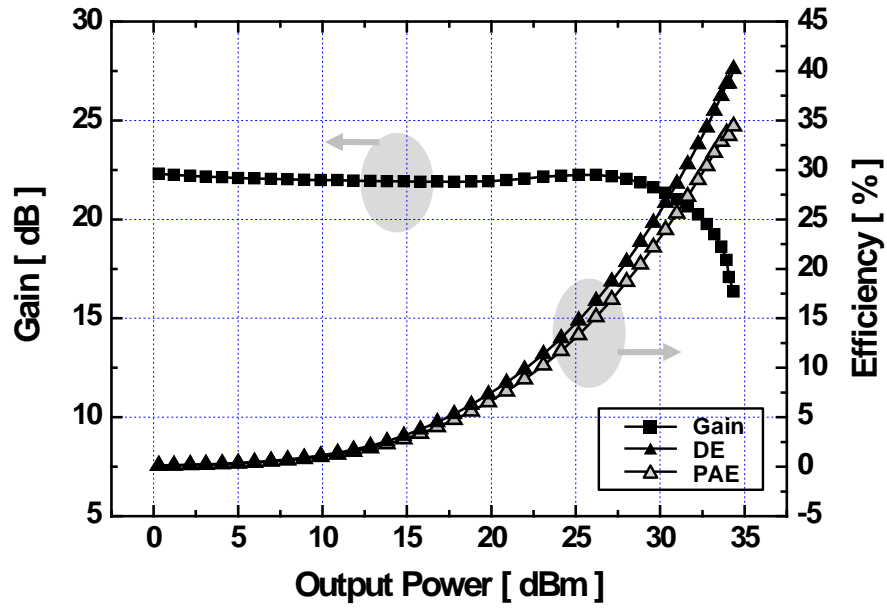


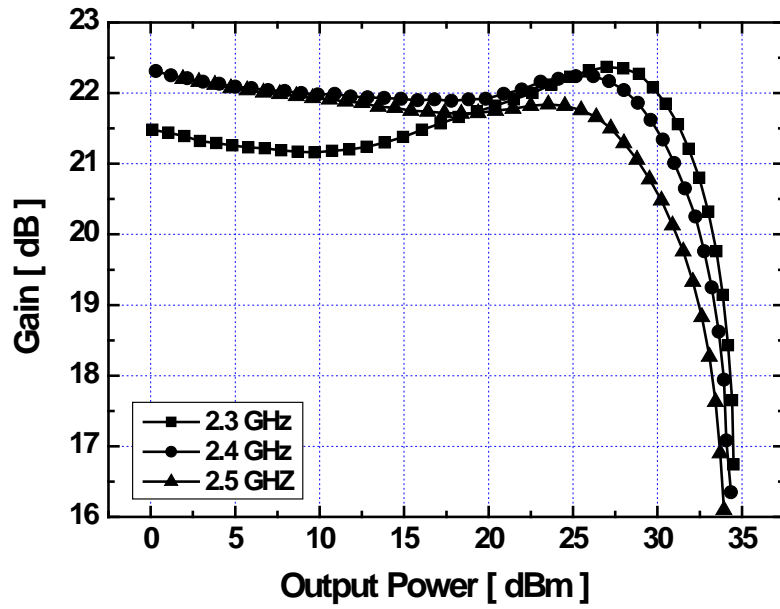
Figure 73. Micro-photograph of fabricated PA (2.1 x 1.64 mm²).

efficiency. The measured gain and efficiency of designed PA at the operating frequency of 2.4 GHz is presented in Figure 74(a). The PA achieves a gain of 22 dB, a P_{1dB} of 31.5 dBm, a P_{sat} of 34 dBm, a peak PAE of 34.9%, and a peak drain efficiency (DE) of 41%. The gain variation is less than 0.5 dB. The measured gain/ P_{1dB} at 2.3 GHz and 2.5 GHz are 21.5 dB/32.5 dBm and 22 dB/29 dBm, respectively, as shown in Figure 74(b).

The measured S-parameters are plotted in Figure 75. The input and output return losses (S_{11} and S_{22}) are better than 15 dB at 2.4 GHz. The small signal gain (S_{21}) of the PA is greater than 19 dB from 1.8 to 3.2 GHz (i.e., 3-dB bandwidth is 1.4 GHz). The EVM was also measured to observe the linearity of designed PA using the IEEE 802.11g WLAN OFDM 64-QAM (channel bandwidth is 20 MHz) and 802.16e WiMAX OFDM 64-QAM (channel bandwidth is 24 MHz) modulated signals at 2.4 GHz. The PA satisfies WLAN EVM specification (-25 dB or 5.6%) up to 23.5-dBm output power, and WiMAX

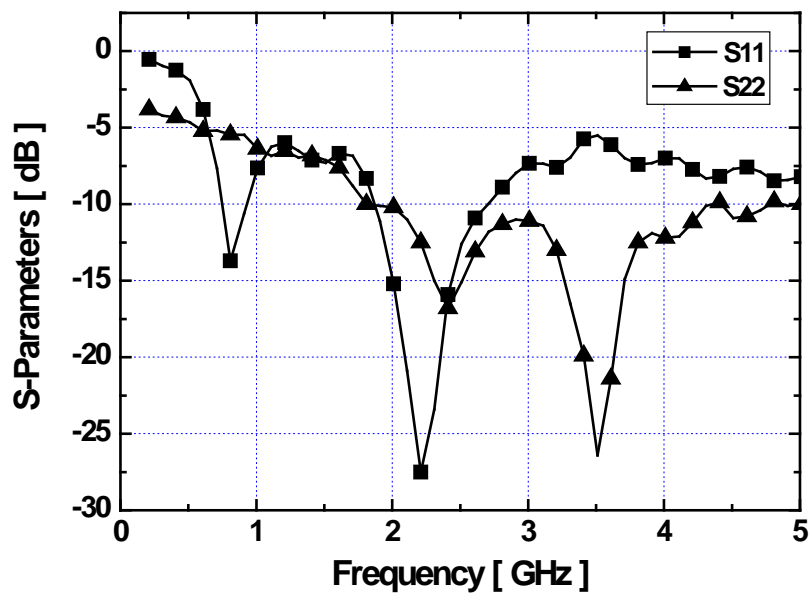


(a)

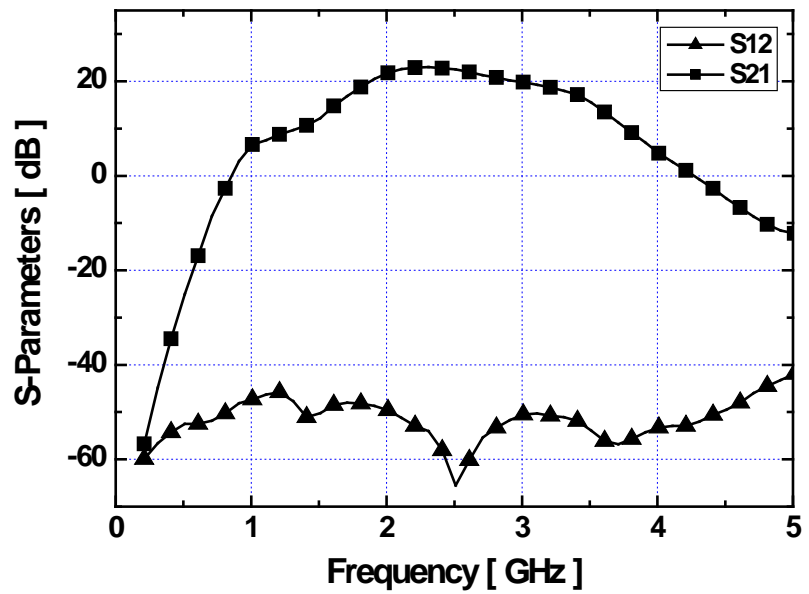


(b)

Figure 74. Measured results of designed PA. (a) Gain, DE, and PAE. (b) Gain versus P_{out} at different frequencies.

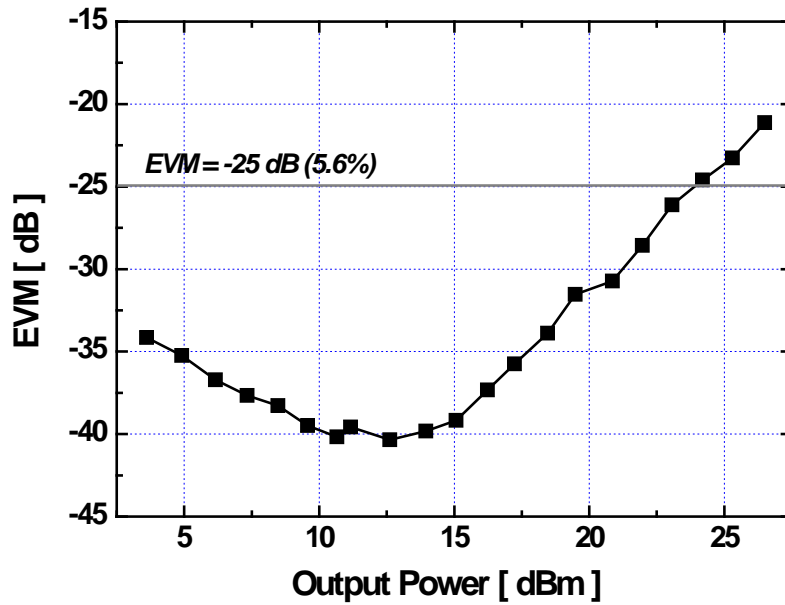


(a)

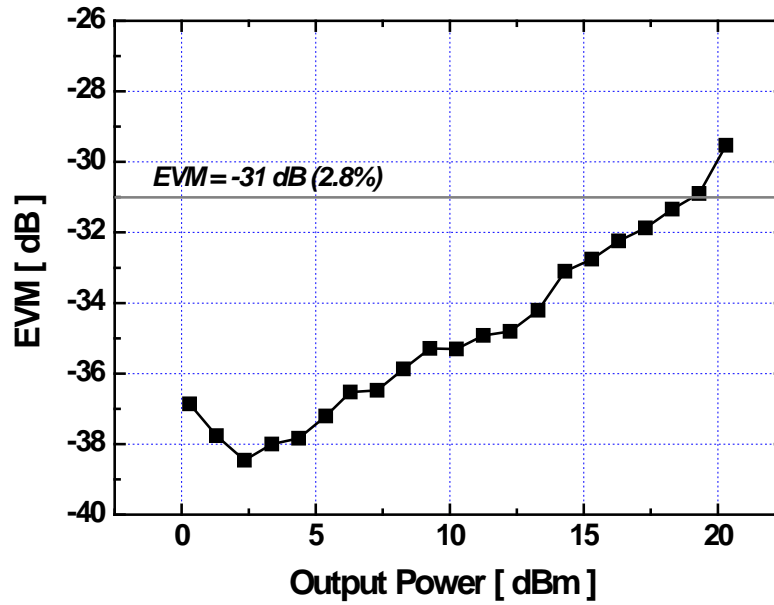


(b)

Figure 75. Measurement results of the PSCT-based high-power linear PA: S-parameters. (a) S_{11} and S_{22} . (b) S_{21} and S_{12} .



(a)



(b)

Figure 76. Measurement results of designed PA: EVM. (a) For WLAN 54 Mbps 64-QAM signal. (b) For WiMAX 54 Mbps 64-QAM signal.

EVM specification (-31 dB or 2.8%) up to 19.5-dBm output power (Figure 76). Measured spectrums and constellations for WLAN and WiMAX signals are presented in Figure 77. The PA consumes an idle DC current of 270 mA (30 mA for the driver stage amplifier and 60 mA for each of power stage amplifier) from 3.3 V supply. The performance of designed PA is compared to other state-of-the-art linear CMOS PAs in Table 8.

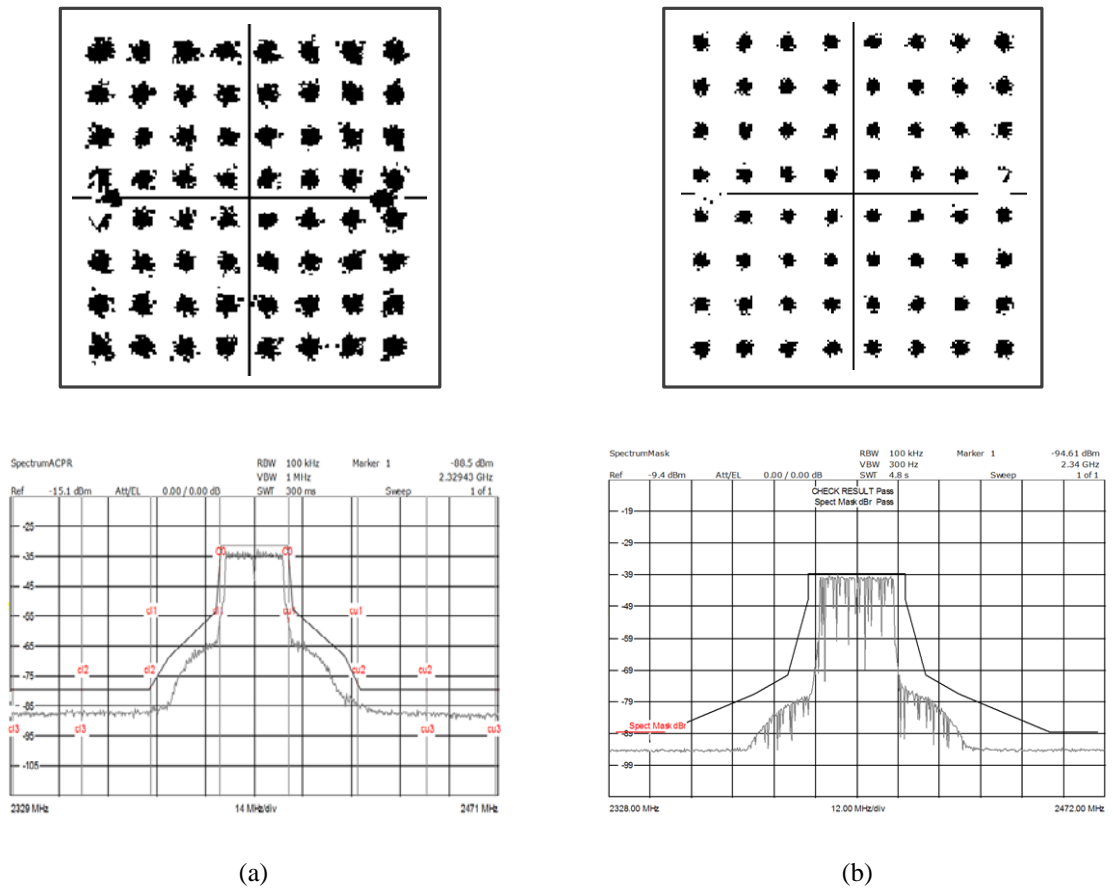


Figure 77. Measurement results of the PSCT-based high-power linear PA: constellation and spectrum (at 2.4 GHz). (a) For WLAN OFDM 64-QAM signal ($P_{out}=23$ dBm). (b) For WiMAX OFDM 64-QAM signal ($P_{out}=19$ dBm).

Table 8. Performance comparison of high-power linear CMOS PAs

Ref	[73]	[74]	[68]	[65]	This work
Freq [GHz]	2.45	2.5	2.4	2.4	2.4
Gain [dB]	32	18	28	37	22
P_{1dB} [dBm]	27.5	29.5	27.7	27	31.5
P_{sat} [dBm]	31.5	32	30.1	31	34
Pout@-25-dB EVM [dBm]	25.5	25	22.7	22	23.5
Peak PAE [%]	25	48	33	27	34.9
Linearization Technique	Yes	Yes	Yes	No	No
Supply [V]	3.3	3.3	3.3	3.3	3.3
Size [mm ²]	2.7	2.25	4.32	2	3.44
Technology	65nm CMOS	90nm CMOS	90nm CMOS	180nm CMOS	180nm CMOS

4.5. Conclusion

A novel power combining transformer, parallel-series combining transformer (PSCT), was proposed to implement a single-chip high-power linear CMOS PA. The PA has been fabricated in a standard CMOS technology and achieved a high P_{1dB} (31.5 dBm), a high P_{sat} (34 dBm), and a high peak PAE (34.9%) with a gain of 22 dB at the frequency of 2.4 GHz. While meeting the EVM specifications for WLAN and WiMAX OFDM 64-QAM signals at 23.5 dBm and 19.5 dBm, respectively, the designed PA demonstrated the highest P_{1dB} and P_{sat} with good efficiency among reported CMOS linear PAs. The effectiveness of proposed transformer, PSCT, as a power combiner for implementations

of high-power linear CMOS PAs has been successfully validated. However, the linearity performance of the PA can be further improved by employing other linearization techniques.

CHAPTER 5

DESIGN OF W-BAND (91 GHZ) RECEIVER FRONT-END ICS USING SIGE TECHNOLOGY

5.1. Introduction

The most auspicious frequency bands in the MMW range for the next-generation broadband wireless communications are the V-band (50 to 75 GHz) and the W-band (75 to 110 GHz). The V-band has been vigorously exploited to develop applications of short-range high data-rate (> 1 Gb/s) wireless accesses such as WPAN or WirelessHD™. The W-band provides more available frequency resources without severe propagation attenuation problem. With abundant spectral bandwidth available, the W-band range is being actively utilized for many commercial (e.g., automotive cruise control systems), and military (e.g., aerospace/satellite smart radar systems and missile control systems) applications [32]-[36].

The structure of the receiver systems for MMW applications also adopts conventional topologies that are widely used for RF applications. The direct down-conversion receiver illustrated in Figure 78 is perhaps the most commonly used architecture. There is no need for an image rejection filter and the second down-conversion step as in the heterodyne receiver system because the signal in the carrier frequency is directly down-converted to the baseband. Therefore, more compact implementation of the system with reduced power consumption is realizable, which is the biggest advantage for many MMW applications.

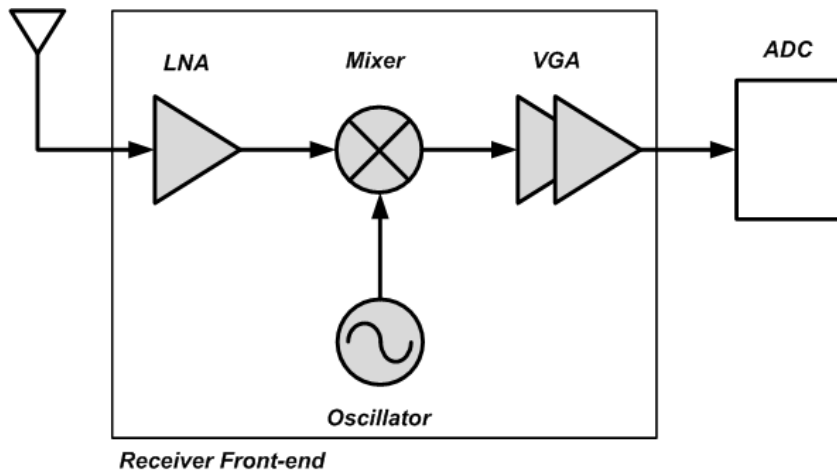


Figure 78. Diagram of a direct down-conversion receiver system.

The most successful implementation of the V-Band direct down-conversion receiver system using SiGe technology has been demonstrated in [30]. The block diagram of this V-Band receiver is presented in Figure 79, where shaded region indicates actually integrated receiver. This receiver consists of an LNA with single-ended-input and differential-output (working as an active balun), two down-conversion mixers that are based on conventional Gilbert-cell multipliers, a frequency tripler to generate the LO input, a differential branch-line directional coupler, and buffers. The novelty in this structure is the integration of the directional coupler to generate 90° -phase-shifted signals, which was implemented using quarter-wavelength transmission lines. The measured performance of critical circuit blocks is also summarized in Figure 79, where the down-converter includes the mixer and the buffer. Although the measurement data for the entire receiver chain was not reported, mathematical calculation of cascaded system shows 5.8-dB noise figure (NF), 31-dB gain, -22-dBm input-referred intercept point (IIP_3), and -32-dBm input referred P_{1dB} (P_{1dB_in}).

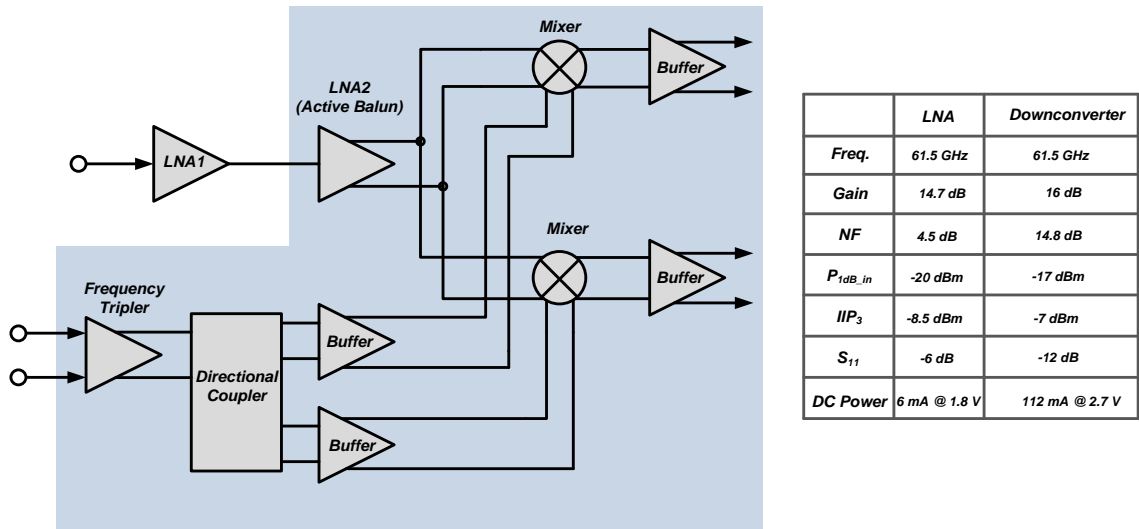


Figure 79. Diagram of the 60 GHz receiver in SiGe demonstrated in [30].

In the W-Band, integrated receiver systems using SiGe technology have been implemented employing relatively simple architectures [35], [36]. The diagrams of these W-Band receivers are presented in Figure 80. Applications in the W-band frequencies (e.g., automotive control systems, passive imagers, etc) do not exploit advanced modulation schemes, thus separation of I/Q signal paths within the receiver chain is not necessary. For the automotive radar application in 77 GHz, the demonstrated receiver in [35] achieved 30-dB conversion gain, 11.5-dB NF, -26-dBm P_{1dB_in} , and -21.6-dBm IIP₃, consuming 440 mW from 5.5 V supply. This W-Band receiver features a single-stage cascode LNA, an active balun, and a Gilbert-cell-based double balanced mixer with an LO balun. The LO balun was implemented using LC passive networks of which inductive components were realized by transmission lines. Another W-Band SiGe receiver that integrated a two-stage differential cascode LNA with a double-balanced mixer and a voltage-controlled oscillator (VCO) has been reported in [36]. This receiver achieved 40-dB conversion gain, 8-dB NF, -38-dBm P_{1dB_in} at 77 GHz, consuming 195 mW.

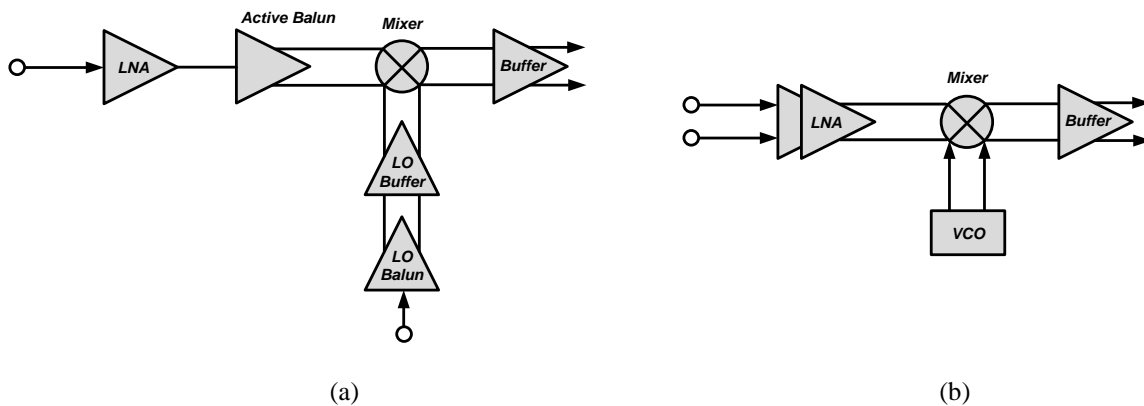


Figure 80. Diagrams of reported W-Band SiGe receivers. (a) In [35]. (b) In [36].

As a next step toward higher operating frequencies, we are motivated to explore potential usability of advanced SiGe technology to build a high-dynamic-range receiver front-end system operating at 90 to 94 GHz. This frequency band is suitable for long-range high-resolution frequency modulated continuous wave (FMCW) radar applications [76]-[78]. Proposed structure of a W-band (94 GHz) receiver is illustrated in Figure 81. The receiver adopts the direct down-conversion topology. The balun transforms single-ended signals that are amplified by an LNA to differential signals to be down-converted by a mixer. The balun also performs conversion of single-ended reference clock signal from the external oscillator to differential LO signal for the mixer input. Double-balanced mixer can improve linearity and dynamic range of the receiver system.

This chapter presents the design procedures and implementation issues of circuit blocks essential to a W-band receiver front-end system: a balun, an LNA, and a mixer. Considering diverse design challenges for active and passive circuits operating at such a high frequency (94 GHz), careful characterizations and optimizations of individual functional blocks are performed. Section 4.2 briefly describes SiGe HBT BiCMOS

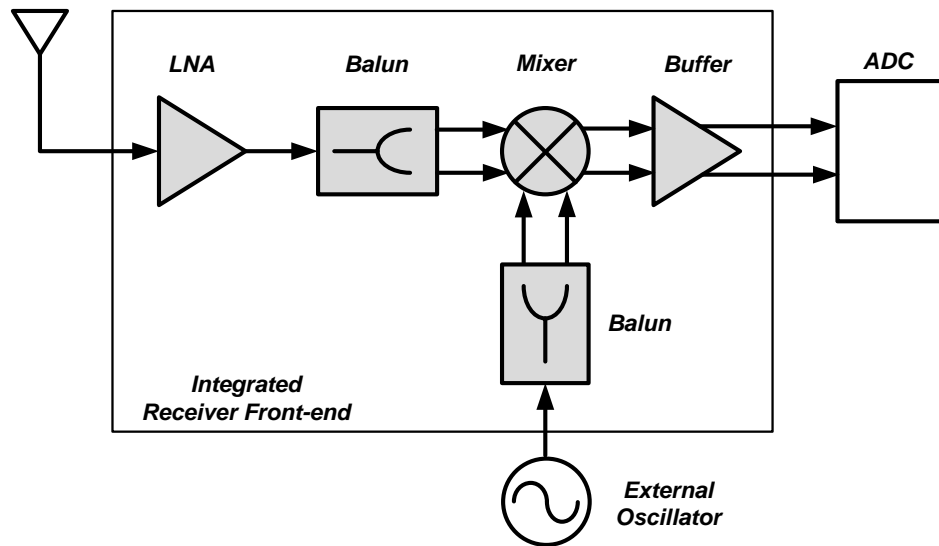


Figure 81. Diagram of proposed W-band (94 GHz) receiver front-end system.

technology that was used to fabricate the circuits. The design of the planar-type Marchand balun is introduced in Section 4.3. Section 4.4 and 4.5 present design issues and methodologies of the LNA and the down-conversion mixer along with simulation and measurement results, respectively. Implementation of an integrated W-band receiver is presented in Section 4.6. The conclusion follows in Section 4.7.

5.2. SiGe Technology

Although III-V technologies (GaAs and/or InP) provide significant performance advantages, silicon-based technologies may be preferred to be used to reduce the development cost and ease the integration with baseband digital circuitries. An advanced generation (third or fourth generation as in Figure 5) SiGe BiCMOS technology can be a good solution to implement high performance MMW circuit components since it

provides improved performance of active/passive components with advantages of the low-cost silicon substrate. A 0.12- μm -emitter-width IBM 8HP SiGe BiCMOS technology was chosen to fabricate the W-band receiver front-end circuits. The technology supports SiGe HBTs with peak f_T/f_{max} of 200/280 GHz with 0.13- μm 1.2-V Si CMOS transistors and passive elements including MIM capacitors, thin-film resistors, on-chip inductors, and transmission lines. Seven levels of metallization are available: two top aluminum layers and five copper bottom layers. The top aluminum metal features 4- μm thickness that enables implementations of high- Q inductors and transmission lines.

The advancements in SiGe HBT performance is mainly achieved by smaller base-collector capacitance (C_{BC}) which is realized by eliminating out-diffusion of the extrinsic base [54]. Employment of laterally scaled emitter width minimizes base resistance (R_b) and improves frequency/noise characteristics. Thus, high speed, low noise, and high gain devices are realizable in this technology, which is a great advantage for MMW circuit designs. The cross section of the SiGe HBT is presented in Figure 82 [54].

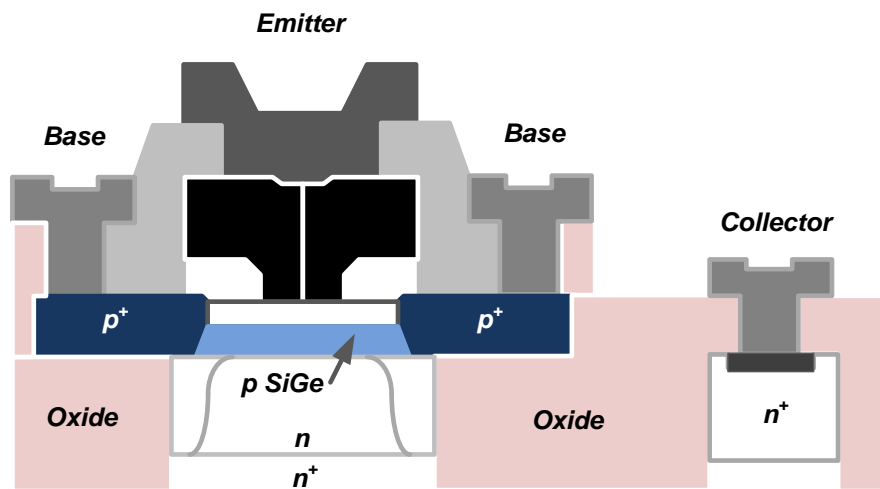


Figure 82. Cross section of SiGe HBT.

5.3. Design of a W-band balun

Differential functionality of circuits operating at high frequencies is strongly desired because it reduces common mode noise and improves linearity and dynamic range. Although single-ended (or unbalanced) signals are inevitably generated by antennas or other preceding functional blocks, a conversion to differential (or balanced) signals is still realizable using an additional circuit block.

A balanced-to-unbalanced (balun) signal conversion can be realized using active or passive circuits. Active baluns normally employ differential amplifiers of which only one side of input or output terminals is taken for applying or extracting the signals. The active baluns are advantageous in terms of generating extra gain in addition to converting signals, but have critical drawbacks. The biggest problem is amplitude/phase mismatch issue that is raised by unbalanced differential functionality of the amplifier especially when the operating frequency of the circuit is very high (as in MMW frequency range) [79]. Additional nonlinearity caused by the active balun also degrades overall linearity performance of the receiver system. Moreover, the active baluns also consume power which is commonly comparable amount to power consumed by other critical functional blocks. For these reasons, passive baluns with various configurations have been widely used for applications in MMW integrated circuits [80]-[81]. Among them, the planar-type of the Marchand balun [84] is perhaps one of the most attractive solutions due to its wideband performance and ease of design. The planar Marchand balun consists of two coupled quarter-wavelength ($\lambda/4$) transmission lines, which can be realized using microstrip lines, CPW lines, or spiral coils. The schematic representation of the planar Marchand balun is shown in Figure 83. One of each coupled lines has ground termination

at the input side, and opposite coupled lines are shorted together at the output side. An unbalanced input port and balanced output ports of the balun are terminated by impedance Z_S and Z_L , respectively.

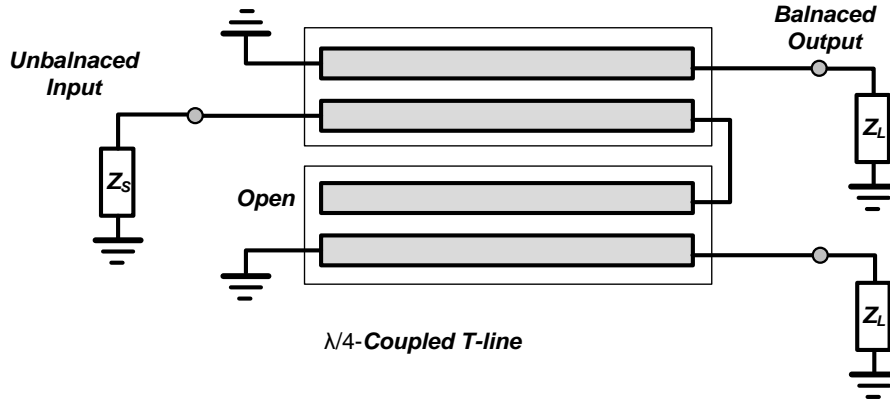


Figure 83. Schematic of a planar-type Marchand balun.

5.3.1. Quarter-wavelength coupled line

To understand how the balun works, it is necessary to review characteristics of a coupled quarter-wavelength transmission line which is illustrated in Fig. 84. The coupled line is composed of two closely placed straight transmission lines, and the coupling coefficient between two lines is denoted as k . When terminal impedances of the individual lines are chosen to be equal to the characteristic impedance of the lines (i.e., $Z_S=Z_L=Z_0$), the S-parameters of the four port network can be represented as [85]

$$[S]_{coupler} = \begin{bmatrix} 0 & -j\sqrt{1-k^2} & k & 0 \\ -j\sqrt{1-k^2} & 0 & 0 & k \\ k & 0 & 0 & -j\sqrt{1-k^2} \\ 0 & k & -j\sqrt{1-k^2} & 0 \end{bmatrix} \quad (92)$$

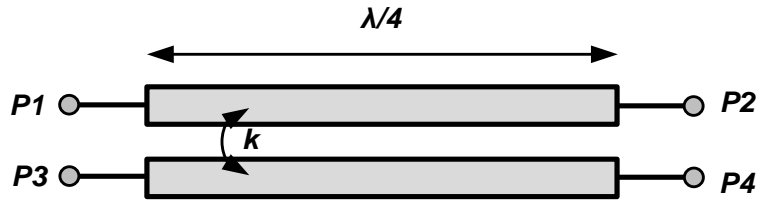


Figure 84. Coupled quarter-wavelength transmission line.

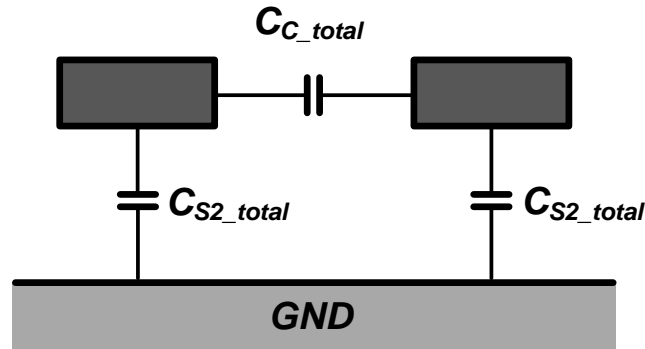


Figure 85. Total capacitance in a coupled line.

The coupling coefficient can be calculated from effective capacitance of unit length of coupled lines using the equation given by

$$k = \frac{C_{C_total}}{\sqrt{(C_{S1_total} + C_{C_total})(C_{S2_total} + C_{C_total})}}, \quad (93)$$

where C_{C_total} denotes the total equivalent coupling capacitance between two lines and C_{S1_total} and C_{S2_total} are the total equivalent capacitances between the conductors and ground plane as presented in Figure 85. As can be anticipated, the coupling coefficient is increased if C_{C_total} is large as in a case when two lines are placed very closely. The coupling coefficient is also inversely proportional to C_{S1_total} and C_{S2_total} implying that large distance between the conductors and ground-plane is desired for higher coupling.

The coupled line supports two types of excitations: the even mode, where the currents in the conductors are equal in amplitude and in the same direction, and the odd mode, where the currents in the strip conductors are equal in amplitude but in opposite directions. The characteristic impedances in each excitation modes ($Z_{O,e}$ and $Z_{O,o}$) can be derived as [84]

$$Z_{O,e} = \sqrt{Z_S Z_L} \cdot \sqrt{\frac{1+k}{1-k}} \quad (94)$$

$$Z_{O,o} = \sqrt{Z_S Z_L} \cdot \sqrt{\frac{1-k}{1+k}}, \quad (95)$$

Therefore, we can get relations between the characteristic impedance and the coupling coefficient, k , as

$$\frac{Z_{O,e}}{Z_{O,o}} = \frac{1+k}{1-k} \quad (96)$$

$$k = \frac{Z_{O,e} - Z_{O,o}}{Z_{O,e} + Z_{O,o}}. \quad (97)$$

For better performance in terms of the bandwidth, the ratio of $Z_{O,e}/Z_{O,o}$ of the coupled line must be maximized [82], so higher coupling between two lines is desired.

The hybrid-type coupled transmission line has been simulated using IBM 8HP design-kit model. The length of each conductor line is $300 \mu\text{m}$ which is a quarter-wavelength at 94 GHz. The width of signal conductor is $5 \mu\text{m}$ to feature the characteristic impedance of 65Ω (same structure as one explained in Chapter 2). This value was chosen since the balun will be loaded by output impedance of the preceding LNA and input impedance of following mixer that have higher impedances than 50Ω . The cross section of the hybrid-type quarter-wavelength transmission line is shown in Figure 86.

The simulated coupling coefficient as a function of the distance between two conductor lines (D) is plotted in Figure 87.

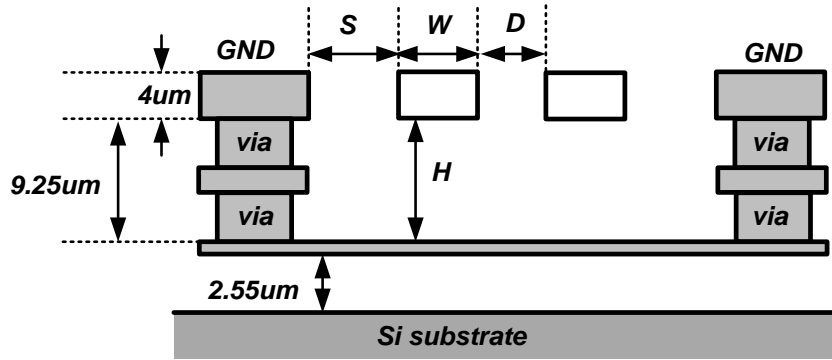


Figure 86. Cross-section of the hybrid-type coupled transmission line.

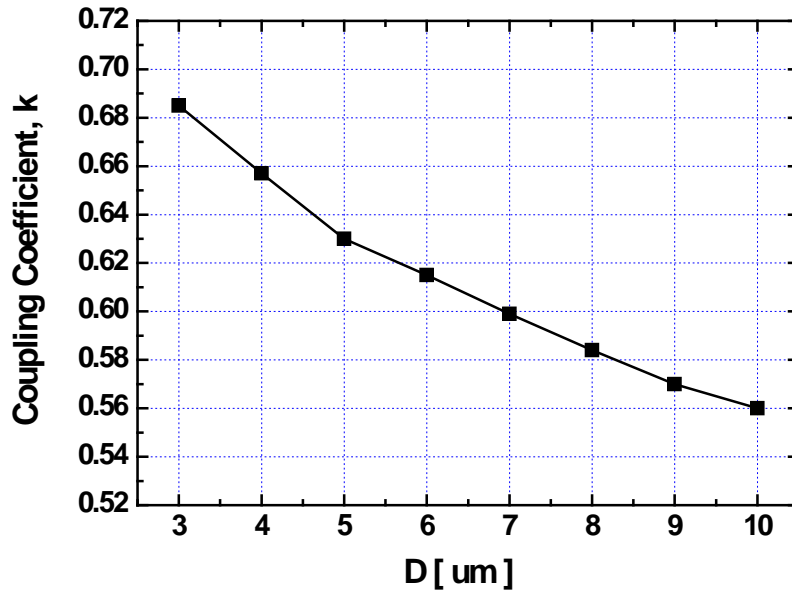


Figure 87. Simulated coupling coefficient of the hybrid-type coupled transmission line ($W=5 \mu\text{m}$, $S=20 \mu\text{m}$).

The characteristics of the hybrid-type coupled quarter-wavelength transmission line ($L=300\ \mu\text{m}$, $W=5\ \mu\text{m}$, $S=20\ \mu\text{m}$, and $D=5\ \mu\text{m}$) are compared between the design-kit model and the EM simulated model. The structure of the coupled transmission line for EM simulation is illustrated in Figure 88. The four-port S-parameters are obtained from



Figure 88. 3-D structure of the hybrid-type coupled quarter-wavelength transmission line ($W=5\ \mu\text{m}$, $S=20\ \mu\text{m}$, $D=5\ \mu\text{m}$).

the simulation to observe characteristics of the coupled line (through, coupling, and isolation). The comparison is presented in Figure 89. The EM model has slightly higher insertion loss (2.1 dB at 94 GHz) than the design-kit model (1.2 dB at 94 GHz). The coupling of the EM model is better than that of the design-kit model (k of the EM model and the design-kit model is 0.67 and 0.625 at 94 GHz, respectively). The isolations for both models are greater than 18 dB at 94 GHz. The design-kit model features relatively optimistic characteristics in terms of the line loss (resistance and inductance as shown in Figure 25 in Chapter 2), but the coupling and isolation characteristics for both models are relatively close.

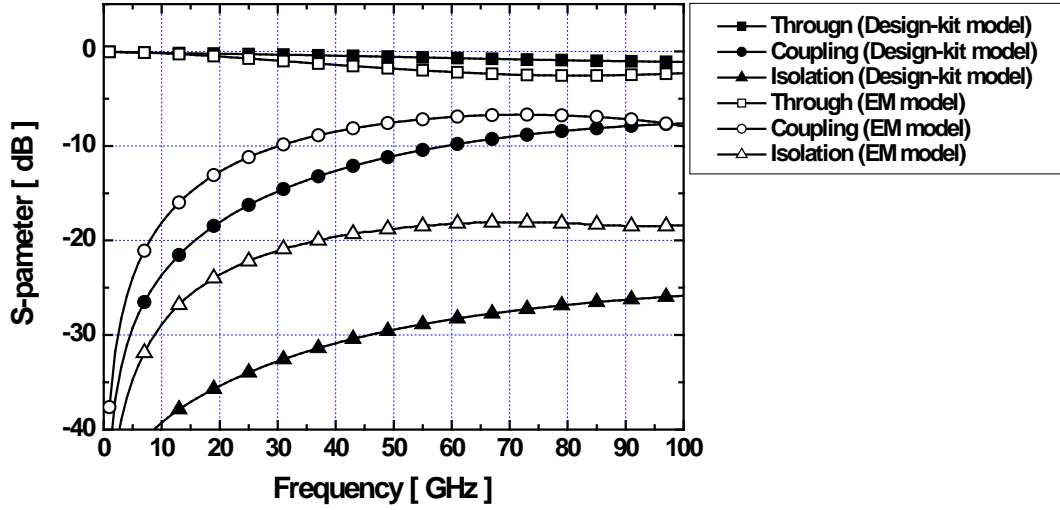


Figure 89. Simulated characteristics of the hybrid-type coupled quarter-wavelength transmission line.

The quarter-wavelength coupled transmission line itself can be used to implement the balun function. One of two terminals at one side is loaded by the input port that has impedance of Z_s , while the other terminal is open circuited for full reflection (it may be shorted to ground as well). Two terminals at the opposite side are loaded by output ports that have impedance of Z_L (this configuration is presented in Figure 90). Two output ports will have signals with the phase difference of 180° and the amplitude imbalance of [86]

$$\frac{S_{31}}{S_{21}} = \frac{Z_{O,e} - Z_{O,o}}{Z_{O,e} + Z_{O,o}} = k, \quad (98)$$

where Z_s and Z_L are assumed to be matched to the characteristic impedance of the line. Calculated amplitude imbalance of the quarter-wavelength coupled transmission line with $Z_{O,o}$ of 35Ω as a function of $Z_{O,e}$ is plotted in Figure 91. As observed, very high $Z_{O,e}$ is

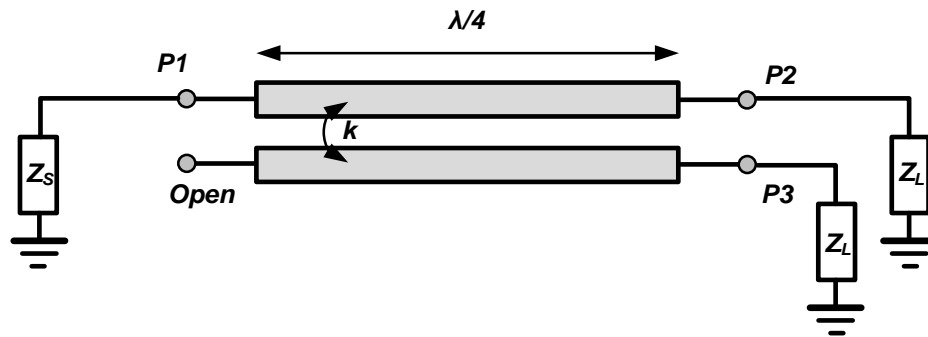


Figure 90. Configuration of a coupled quarter-wavelength transmission line as a balun.

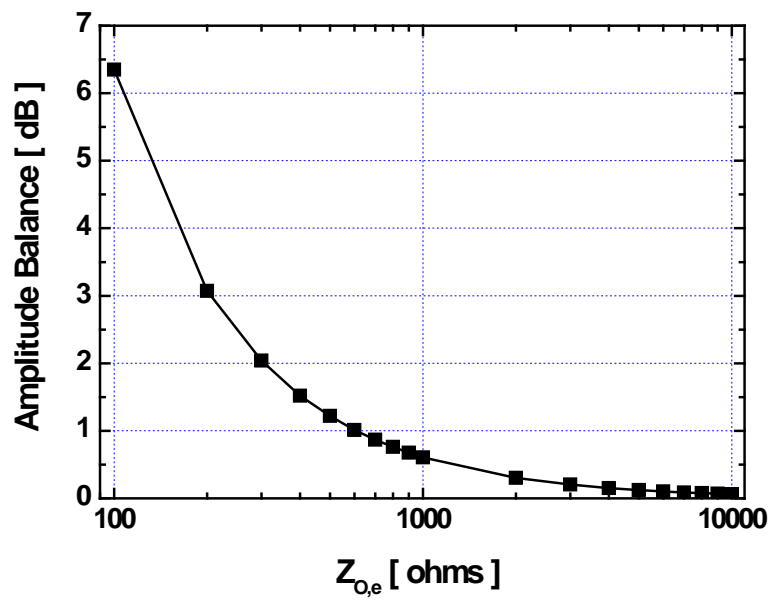


Figure 91. Simulated amplitude balance of a coupled quarter-wavelength transmission line.

required to achieve reasonable amplitude balance, which is the reason why the single section of a quarter-wavelength coupled transmission line is not widely used as a balun.

When the coupled transmission line has side ground plane (ground shields) with unequal widths, the ratio of the even-mode characteristic impedance to the odd-mode characteristic impedance ($Z_{O,e}/Z_{O,o}$) is not preserved as it is for the coupled line with equal ground plane widths [87]. The ratio of $Z_{O,e}/Z_{O,o}$ is maximized when the widths of side ground planes are equal (i.e., symmetric structure has the maximum $Z_{O,e}/Z_{O,o}$). The asymmetric structure of the coupled transmission line is illustrated in Figure 92. If the ratio of B_2/B_1 is enlarged, $Z_{O,e}/Z_{O,o}$ is decreased, which results in smaller coupling

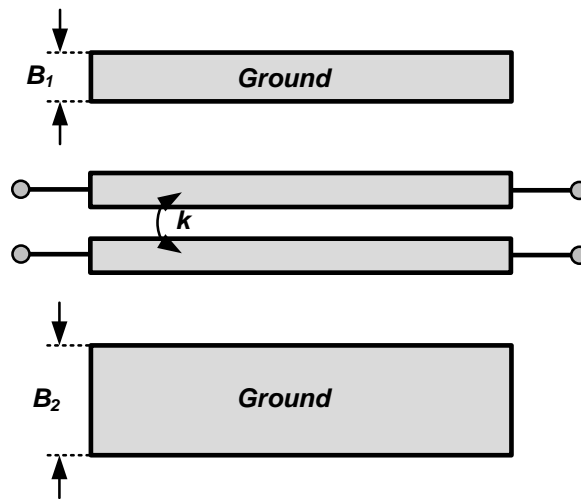


Figure 92. Coupled transmission line with unequal ground-plane widths.

coefficient between two conductors and narrower operating bandwidth. However, this effect is mitigated if the distance between the conductor and the side ground-plane is much larger than the width of the conductor line because the transmission line acts more like a microstrip line rather than a CPW line (i.e., most of the magnetic field from the AC current in the conductor is diminished before it reaches the side ground shield). With different values of B_2/B_1 , the coupling coefficients of the structure are obtained from EM

simulations and presented in Figure 93. There is no significant variation in the values of the coupling coefficient as the difference between widths of two side ground shields is increased. That is, the coupling coefficient is changed from 0.625 for the case of $B_2/B_1=1$ to 0.616 for the case of $B_2/B_1=16$. It was verified with simulations that this amount of variation in the coupling coefficient does not critically deviate the characteristic of the coupled transmission line (e.g., the characteristic impedance).

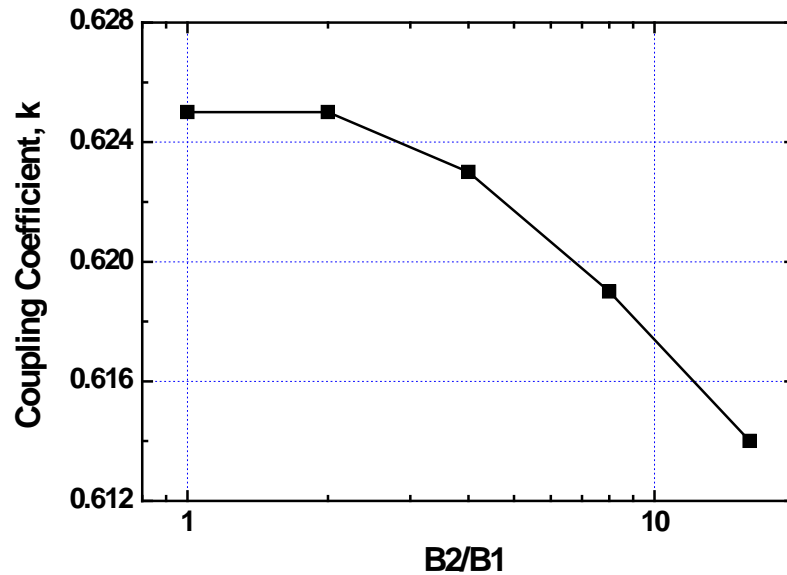


Figure 93. Coupling coefficient of coupled transmission line with unequal ground-plane widths.

5.3.2. W-band Marchand balun

By cascading S-parameters of two coupled lines configured as shown in Figure 94 and assuming the source and load impedance are matched, overall S-parameters of the three-port balun can be obtained as



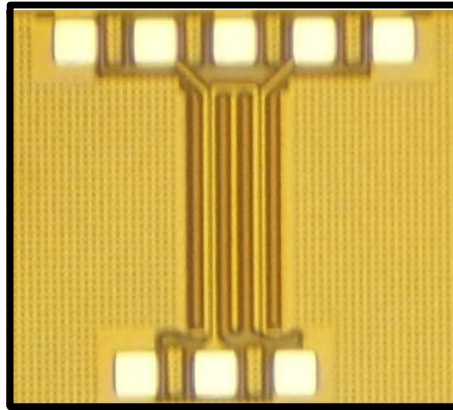
Figure 94. 3-D structure of designed W-band planar-type Marchand balun.

$$[S]_{balun} = \begin{bmatrix} \frac{1-3k^2}{1+k^2} & j\frac{2k\sqrt{1-k^2}}{1+k^2} & -j\frac{2k\sqrt{1-k^2}}{1+k^2} \\ j\frac{2k\sqrt{1-k^2}}{1+k^2} & \frac{1-k^2}{1+k^2} & \frac{2k^2}{1+k^2} \\ -j\frac{2k\sqrt{1-k^2}}{1+k^2} & \frac{2k^2}{1+k^2} & \frac{1-k^2}{1+k^2} \end{bmatrix}, \quad (99)$$

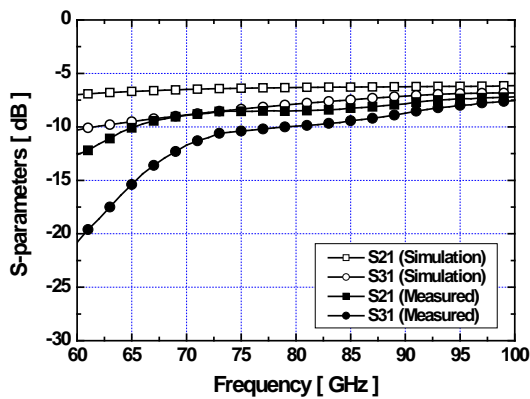
where k is same parameter as for the single coupled lines. If we engineer k so that it minimizes input reflection of the balun (i.e., $k=0.567$ and $S_{11}=0$), we can have

$$[S]_{balun} = \begin{bmatrix} 0 & \frac{j}{\sqrt{2}} & \frac{-j}{\sqrt{2}} \\ \frac{j}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \\ \frac{-j}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}. \quad (100)$$

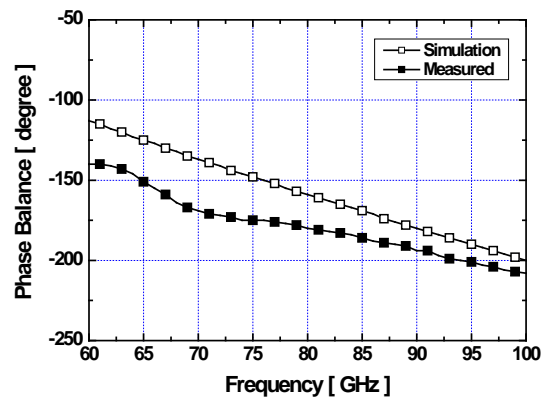
It is noticed that the coupling coefficient, $k=1/\sqrt{3}$, for the best of input return loss causes relatively poor output matching and narrow operating bandwidth (note that higher k will help the balun to have flatter amplitude balance over a wide bandwidth). Thus, some compromise is necessary to select appropriate value for k to have balanced performance of the balun. According to simulated data in Figure 87, k of 0.625 can be achieved if D of the coupled line is selected to be $5\ \mu\text{m}$. Instead of having k of 0.567,



(a)



(b)



(c)

Figure 95. Performance of designed W-band planar-type Marchand balun. (a) Micro-photo of the fabricated balun. (b) Amplitude balance. (c) Phase balance.

higher k was chosen for this design to have wider operating bandwidth with a little penalty of return loss. The EM simulation was performed using ADS Momentum. Measured performance of the balun with EM simulation results is presented in Figure 95. The balun achieved about -8-dB S_{21} and -9.5-dB S_{31} at 94 GHz. The phase imbalance between two output ports is about 20° at 94 GHz.

5.4. Design of a W-band Low-Noise Amplifier

An LNA is the most critical building block among other components in a receiver chain. Because its noise performance determines the overall noise figure of the receiver, considerably low noise characteristic is required for the LNA. In addition, maximized gain and linearity performances are desired for a high dynamic range of the system particularly when the receiver exploits a direct down-conversion topology. Good input and output return losses are important as well to be effectively integrated with preceding/following components, and low power dissipation is demanded due to limited power budget.

5.4.1. Noise characteristics of a SiGe HBT

Primary noise sources in an HBT are: 1) base thermal noise, 2) base shot noise, and 3) collector shot noise. These noise sources compose equivalent noise voltage (v_n^2) and noise current (i_n^2) with cross-correlation factor (γ) in an HBT as shown in Figure 96 [88]. A noise resistance (R_n), an optimal source admittance for minimum noise ($Y_{S,opt}$), and a minimum noise factor (F_{min}) for the HBT can be expressed as

$$R_n = \frac{v_n^2}{4kT\Delta f} \quad (101)$$

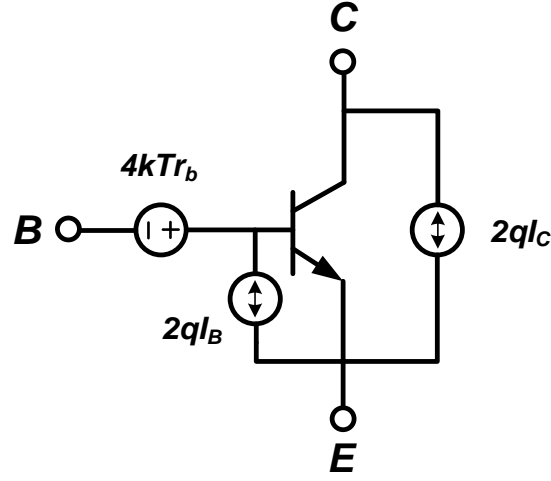


Figure 96. Primary noise sources in an HBT.

$$Y_{S,opt} = G_{S,opt} + jB_{S,opt} = \left(\sqrt{1 - \gamma_i^2} - j\gamma_i \right)^{-1} \cdot \frac{i_n}{v_n} \quad (102)$$

$$F_{min} = 1 + \frac{v_n i_n}{2kT\Delta f} \left(\gamma_r + \sqrt{1 - \gamma_i^2} \right). \quad (103)$$

If we consider the HBT as a two-port network, we can express the noise parameters of the HBT as [89], [90]

$$R_n = r_b + \frac{1}{2g_m} \quad (104)$$

$$G_{S,opt} = \sqrt{\frac{g_m}{2R_n\beta} + \frac{(\omega C_i)^2}{2g_m R_n} \left(1 - \frac{1}{2g_m R_n} \right)}, \quad (105)$$

where r_b is the base resistance, g_m is the transconductance, β is the DC current gain, C_i is total input capacitance (i.e., $C_i = C_{be} + C_{bc}$). Then, the noise factor (F) is determined as

$$F = F_{min} + \frac{G_n}{R_S} \left| Z_S - Z_{S,opt} \right|^2, \quad (106)$$

where G_n is the noise conductance and R_S is the real part of the source resistance. The optimal source impedance, $Z_{S,opt}$ reflects specific matching point of the input at which the device has a minimum noise factor (i.e., $F=F_{min}$). The real part of $Z_{S,opt}$ is obtained as

$$R_{S,opt} = 50 \cdot Re \left(\frac{1 - \Gamma_{opt}}{1 + \Gamma_{opt}} \right), \quad (107)$$

where Γ_{opt} is the optimal input reflection coefficient of the device for minimum noise normalized to 50Ω . Given the operating frequency (f), dimension of the device, and collector bias current (I_C), we can obtain $R_{S,opt}$ as

$$R_{S,opt} = \frac{f_T}{f} \sqrt{\frac{2r_b kT}{I_C q}}, \quad (108)$$

which is inversely proportional to the physical size (emitter length) of the device.

5.4.2. Circuit design

The LNA design starts with investigating the optimal bias point of the device in terms of low F_{min} and high gain. Within a power budget, the device can be biased at specific collector current level (I_C) in such a way that the device has reasonable gain and F_{min} . Once desired bias current density level (J_C) is found, physical size of the device can be determined to have $R_{S,opt}$ very close to 50Ω (assuming that impedance of preceding component such as an antenna or a switch is 50Ω). The imaginary part (reactance component) of $Z_{S,opt}$ can be compensated by an input matching network. The conjugate output matching can be implemented to have higher gain. The available gain of the amplifier with noise-matched input and conjugate-matched output is called an associate gain (G_a).

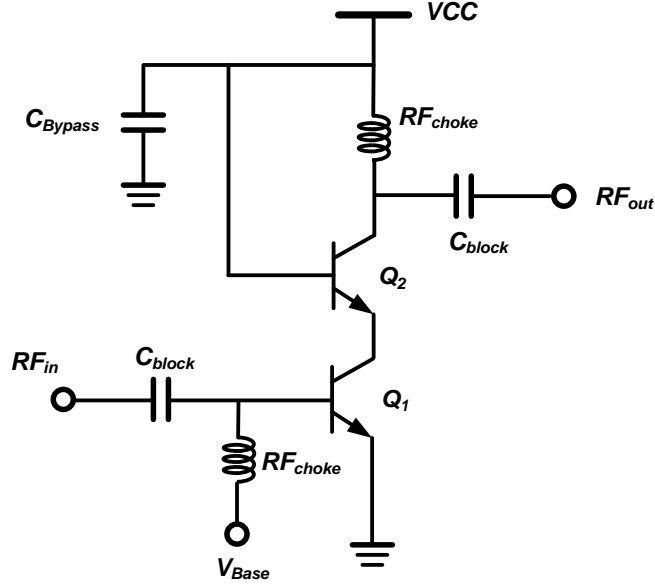


Figure 97. Cascode structure for the W-band LNA.

Figure 97 presents a unit cascode structure for the W-band LNA. The cascode configuration provides better immunity from the Miller effect, hence better isolation between input and output of the LNA can be achieved [90]. Moreover, improved isolation brings better stability over wide operating bandwidth. We selected emitter length (L_E) of transistors Q_1 and Q_2 as $4 \mu\text{m}$ and $2.5 \mu\text{m}$, respectively. Multiplicity of two for the transistors was chosen. Therefore, effective emitter area (A_E) becomes $0.96 \mu\text{m}^2$ for Q_1 and $0.6 \mu\text{m}^2$ for Q_2 . Simulated noise and gain characteristics of the cascode unit structure are shown in Figure 98. Depending on values of J_C , different maximum cut-off frequency (f_T) and NF_{min} can be achieved with opposite tendencies. To have high f_T and low NF_{min} , J_C of $3.8 \text{ mA}/\mu\text{m}^2$ was selected as a bias point (Figure 98(a)). This value of J_C provides about 15-dB associate gain at 94 GHz (Figure 98(b)). The

multiplicity of two for the transistors was chosen to have $R_{S,opt}$ of about 50Ω (Figure 98(c)). Selected size of the transistors and bias current level enable well-compromised noise and gain characteristics of the input stage of the LNA. Figure 98(d) presents Γ_{opt} of the cascode structure for different values of J_C at 94 GHz.

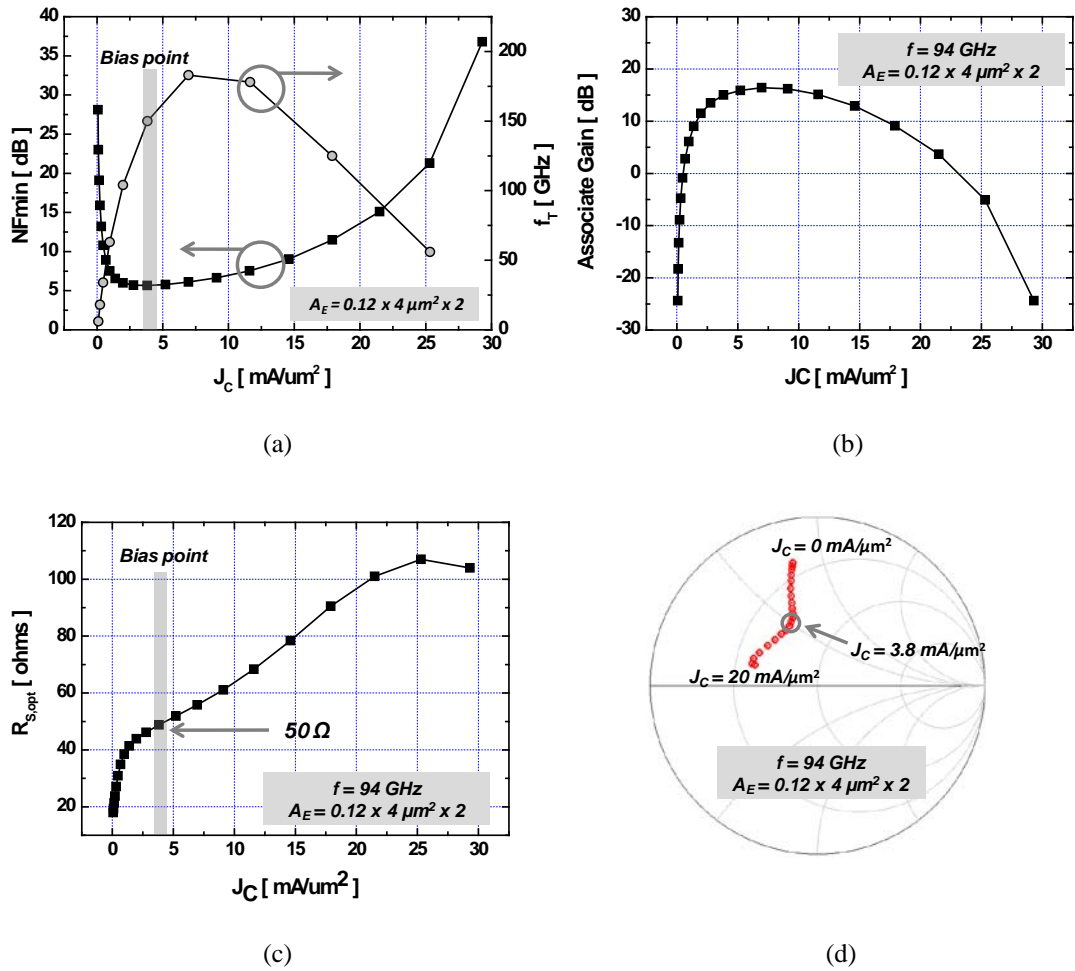


Figure 98. Simulated characteristics of the cascode structure as a function of J_C . (a) f_T and NF_{min} . (b) Associate gain. (c) $R_{S,opt}$. (d) Γ_{opt} .

The schematic of designed LNA and simulation results are presented in Figure 99 and 100, The W-band LNA exploits two stages to achieve higher gain enough to compensate the loss at the following stage (the passive balun). The second stage has identical transistor sizes as the first stage with the same bias condition. Base currents for

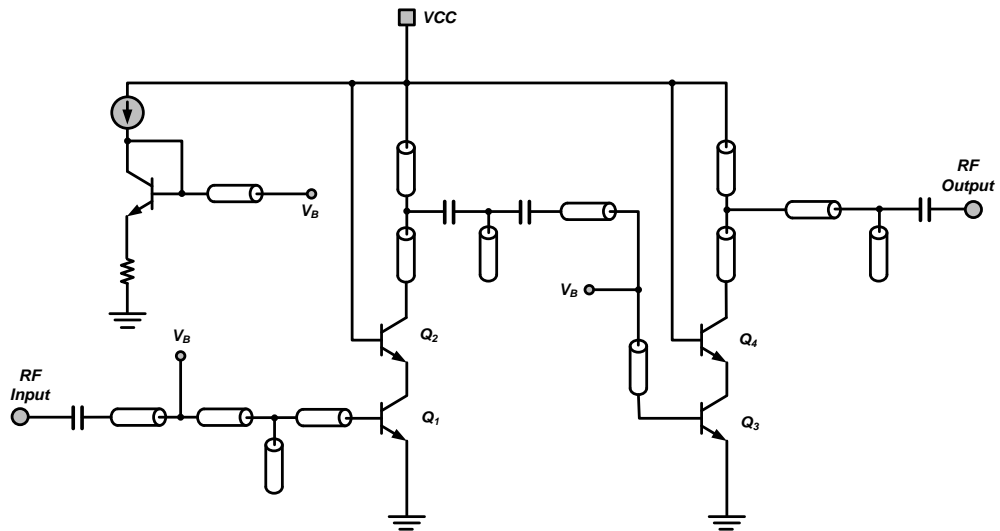


Figure 99. Schematic of designed W-band LNA.

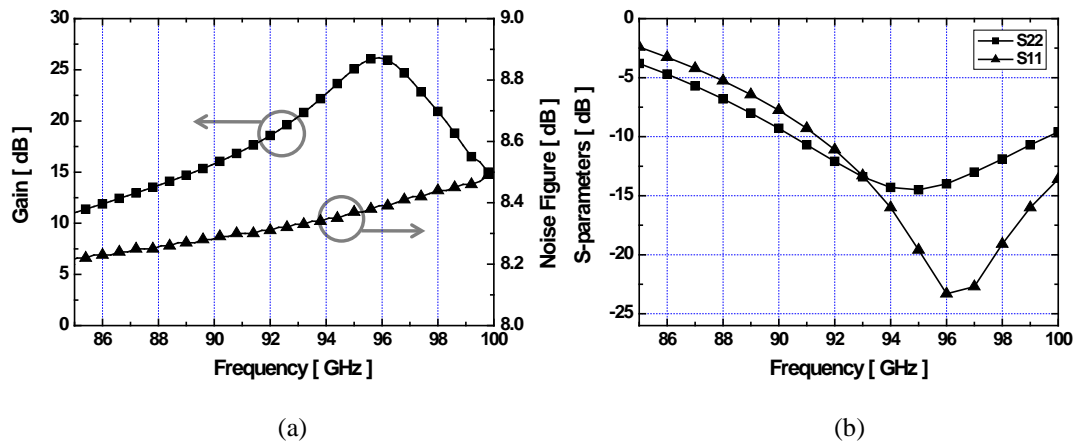


Figure 100. Simulation results of designed W-band LNA.

both stages are fed through quarter-wavelength transmission lines which are part of matching networks. The inter-stage matching network transforms the input impedance of the second stage to the conjugate value of the output impedance of the first stage. The output matching network also performs conjugate matching to the input impedance of the balun. Simulated gain and noise figure of the LNA are 26-dB and 8.4 dB around 96 GHz, respectively. The 3-dB bandwidth is 4 GHz. Input and output return losses are better than 13 dB at the operating bandwidth.

5.5. Design of a W-band Down-Conversion Mixer

For the implementation of transceiver systems in MMW frequency bands, direct up/down-conversion techniques have been widely utilized due to their design simplicity and low power consumption. However, these homodyne structures, especially the receiver side, suffer from critical drawbacks such as vulnerability to even-order distortions and LO self-mixing [92]. In order to mitigate these problems, a fully differential operation is desired for a mixer within a receiver chain. In addition, high noise-floor level at the LO output in the W-band requires better common-mode noise rejection at the mixer input, which also necessitates the use of a double-balanced topology in the W-band mixers. Critical performance metrics of the mixer are voltage conversion gain, noise figure, linearity, and power consumption. The voltage conversion gain is determined as the ratio of *rms* voltage amplitude of the down-converted signal to that of the RF input signal. The noise figure of the mixer indicates how much SNR of the down-converted signal is degraded as the signal passes through the mixer. Depending on the type of LO injection, two different definitions of the noise figure can be considered: 1)

single-side band (SSB) noise figure and 2) double-side band (DSB) noise figure (Figure 101). If the LO frequency is chosen lower or higher than the RF frequency, DSB noise figure is appropriate to measure the noise performance of the mixer. The linearity of the mixer is mainly measured by P_{1dB_in} and IIP_3 . The linearity characteristic of the mixer

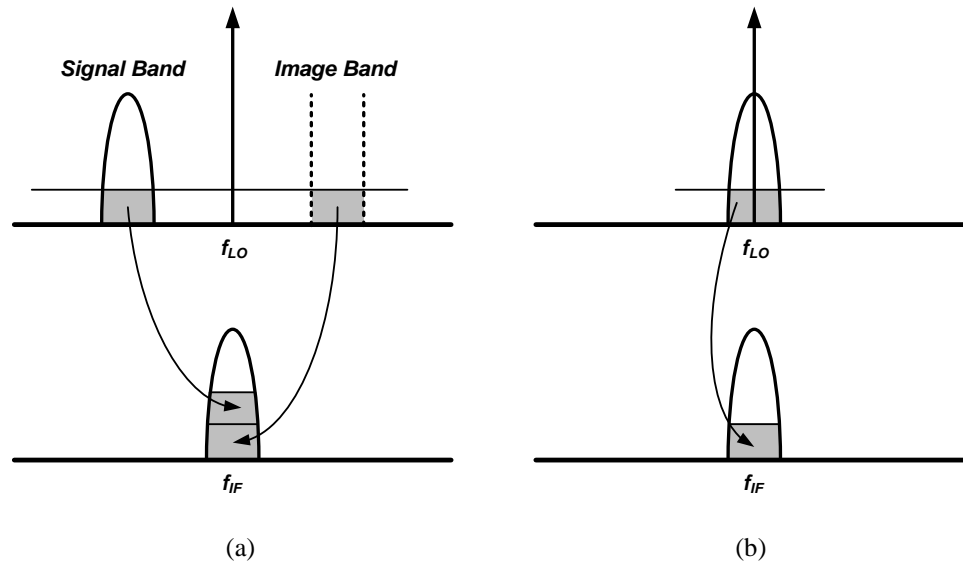


Figure 101. Noise figure in the mixer. (a) Single-side band (SSB) noise figure. (b) Double-side band noise figure.

dominates the linearity performance of entire receiver front-end system. Moreover, because the mixer is followed by baseband circuitries, second-order linearity characteristic is also important. If the mixer generates significant second-order distortions, which is normally evaluated by input-referred second-order intercept point (IIP_2), considerable DC offset is produced, which will desensitize the baseband amplifiers. If the receiver features the direct down-conversion architecture, the DC offset problem becomes tremendously critical since the total gain (or dynamic range) of the baseband blocks is large [92].

5.5.1. Double-balanced mixer topology

The mixer down-converts (in a receiver) or up-converts (in a transmitter) the input signals to necessary frequency bands. In a direct down-conversion receiver, the mixer is required to provide a high gain to maximize the dynamic range of the system while the noise performance is less important (i.e., noise figure of the entire receiver is dominated by the LNA). Furthermore, fully differential operation is required to minimize the second-order distortion. Hence, a double-balanced topology based on a Gilbert-cell multiplier, presented in Figure 102, is commonly adopted for mixers for MMW

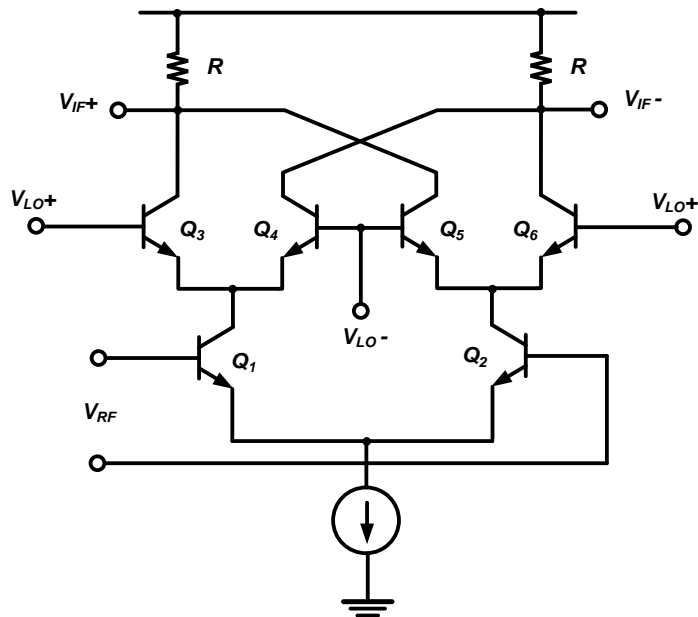


Figure 102. Double-balanced mixer topology.

applications [93]-[98]. The RF input signal in a voltage domain is converted to a current domain by a transconductance stage (Q_1 and Q_2). A switching pairs (Q_3 through Q_6) that

are excited by a high LO swing perform a signal multiplication between the RF signal and the LO signal. This multiplication of two signals results in a frequency translation of the RF signal to an intermediate frequency (IF) band. If the frequency of the LO signal is chosen to be same (or sufficiently close) as the frequency of the RF signal, the IF signal will be at DC or a very low frequency band. The IF signal is finally converted to a voltage domain by load resistors. The mixer operation is graphically illustrated in Figure 103. The RF and LO signals can be expressed as

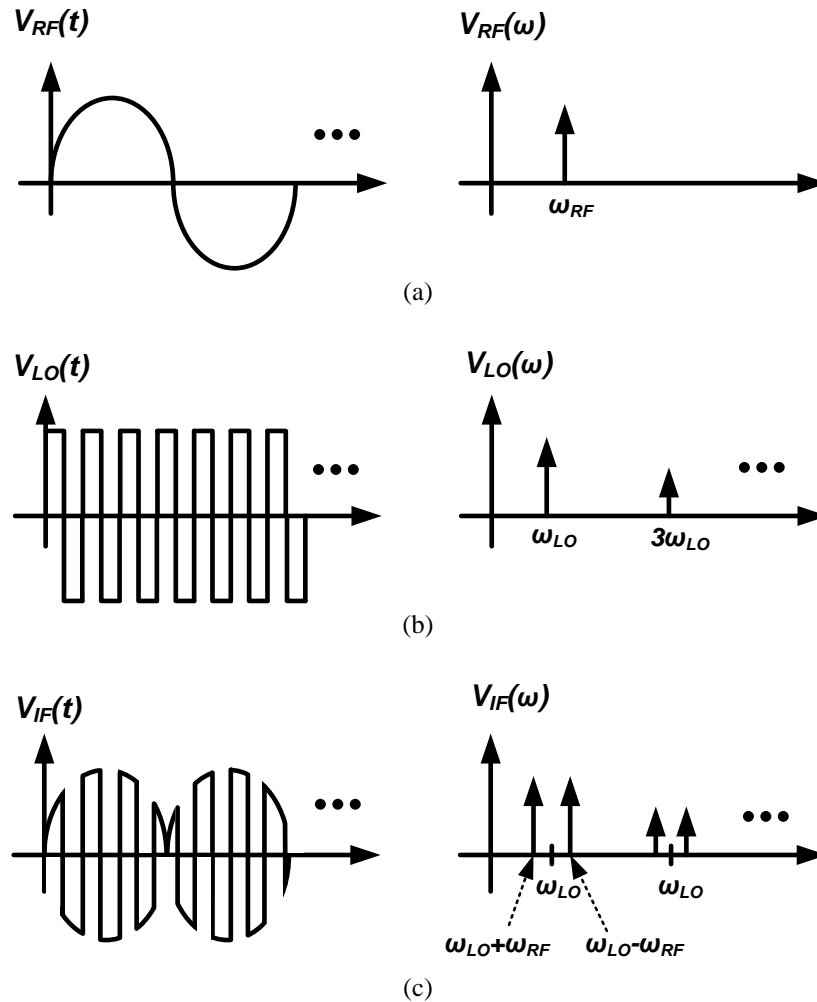


Figure 103. Signal waveforms. (a) RF signal. (b) LO signal. (c) IF signal.

$$V_{RF}(t) = V_1 \cos(\omega_{RF}t) \quad (109)$$

$$V_{LO}(t) = V_2 \sum_{n=1, odd}^{\infty} A_n \cos(n\omega_{LO}t), \quad (110)$$

where A_n represents coefficients for voltage amplitudes at odd-harmonics of the LO frequency. Thus, converted IF signal which is multiplication of the RF and the LO signals is expressed as

$$\begin{aligned} V_{IF}(t) &= k \sum_{n=1}^{\infty} A_n V_{RF} \cos(\omega_{RF}t) \cos(\omega_{LO}t) \\ &= k \sum_{n=1}^{\infty} \frac{A_n V_{RF}}{2} \left(\cos((n\omega_{LO} + \omega_{RF})t) + \cos((n\omega_{LO} - \omega_{RF})t) \right), \end{aligned} \quad (111)$$

and the voltage conversion gain is given by

$$G_c = \frac{kA_1}{V_1} = \frac{2}{\pi} g_m R, \quad (112)$$

where g_m is the transconductance of a gain stage (Q_1 and Q_2) and R is the load resistance. This is the upper limit of the voltage conversion gain when the LO swing is high enough to fully switch Q_3 through Q_6 without causing current leakage by simultaneously turned-on the switching pair (i.e., if two transistors in the switching pair are both turned on for a short period of time, converted RF current is wasted by common-mode amplification by a switching differential pair). Therefore, high LO signal swing is desired for a maximum voltage conversion gain as well as minimum noise contribution from the switching transistors.

5.5.2. Circuit design

As shown in the circuit schematic in Figure 104, the Gilbert-cell-based double-balanced mixer mainly consists of RF transconductance transistors (Q_1 and Q_2) and LO

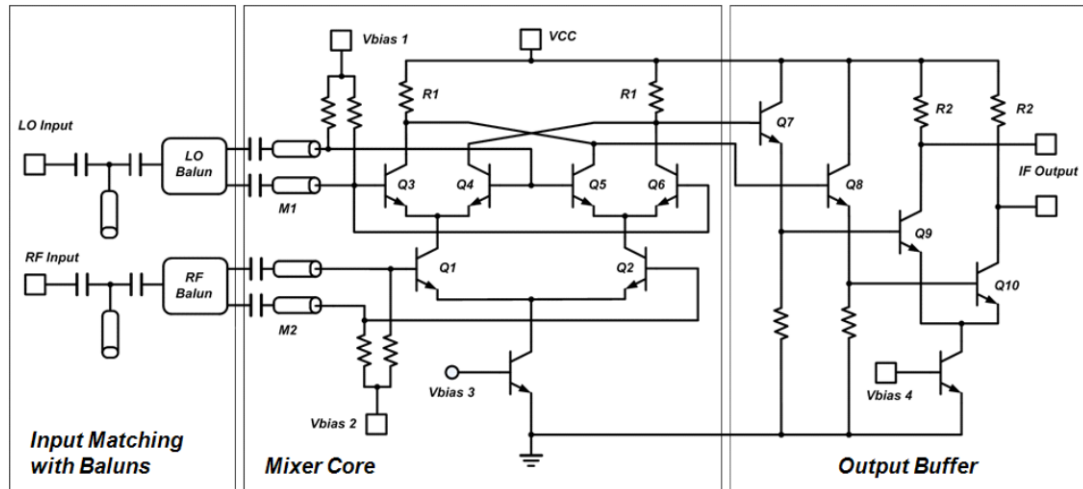


Figure 104. Schematic of designed W-band mixer.

switching transistors (Q_3 through Q_6). Q_1 and Q_2 dominantly determine overall circuit performances. That is, the linearity of the mixer heavily depends on these transistors (i.e., it is improved as the size of Q_1 and Q_2 increases with constant collector current density). However, the shot noise of these transistors, which is the main source of noise in the mixer, is also increased as their size and resulting DC current density are increased. Therefore, the device size and the bias current level of Q_1 and Q_2 should be carefully optimized so that they have maximum transconductance as well as a reasonable noise factor and linearity at the operation point. We chose a $12\text{-}\mu\text{m}$ emitter length ($6\ \mu\text{m} \times 2$) and 5.7-mA bias current for this design. This is equivalent to J_C of $3.96\ \text{mA}/\mu\text{m}^2$ and the transconductance stage has maximum available gain (G_{max}) of $16\ \text{dB}$ and NF_{min} of $5.7\ \text{dB}$ at $94\ \text{GHz}$. After selecting the bias current level, sizing of the Q_3 to Q_6 and load resistors (R_1) is followed. Since immediate and complete switching maximizes the conversion gain and minimizes the noise figure, the switching transistors must be properly sized and biased at a peak f_T current density level. While small transistors having large input

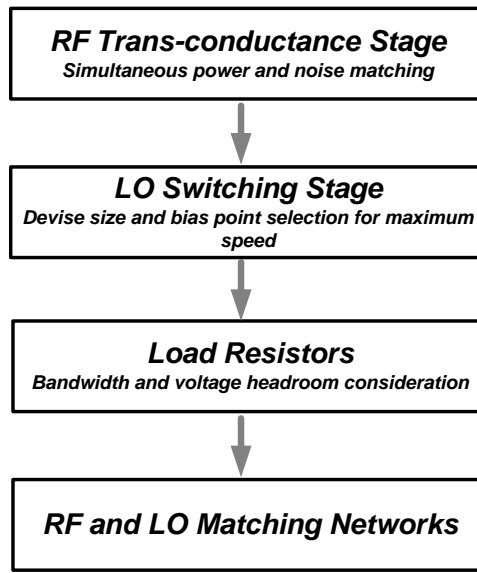


Figure 105. Design flow for the W-band mixer.

impedance are desirable for a large LO swing, a large base resistance of excessively small transistors would contribute more noise to the output. By compromising the conversion gain and the noise figure, we chose 2- μm emitter lengths for Q_3 to Q_6 , which results in J_C of 9.6 mA/ μm^2 for the switching transistors. The transistors biased at selected J_C achieves maximum f_T . The value of R_I was selected to maximize the voltage swing at the output node maintaining the bandwidth higher than IF of 500 MHz. Total extracted capacitance at the collector node of switching transistors was 170 fF, and the load resistor values was chosen to be 75 Ω . The buffer, consisting of an emitter follower and a differential amplifier was also included. The emitter follower acts as a level shifter and has small size (1.2 μm) to minimize the loading effect. The differential amplifier was designed to have unity voltage gain with 50- Ω loads and not to degrade linearity of the mixer core. The emitter length of Q_9 and Q_{10} is 8 μm and the value of R_2 is 300 Ω . The two-stage buffer draws 16.6 mA from a 3.3 V supply. Matching networks for the RF and

the LO inputs were realized with the hybrid-type transmission lines ($W=5 \mu\text{m}$ and $S=20 \mu\text{m}$) in combination with designed Marchand baluns. Long metal inter-connections (about $120 \mu\text{m}$) from the mixer core to input baluns were also modeled using the transmission lines (M_1 and M_2). A design flow of the W-band mixer is summarized in Figure 105.

5.5.3. Measurement results

The micro-photo of the mixer with input baluns is shown in Figure 106. All measurements were done on-wafer using GSG and GSSG probes. To measure the conversion gain, we used two W-band source modules (Agilent 83558A and OML S10MS) for RF and LO signal generations. An IF output port delivers down-converted signal to a spectrum analyzer through a DC blocking capacitor. The single-ended output

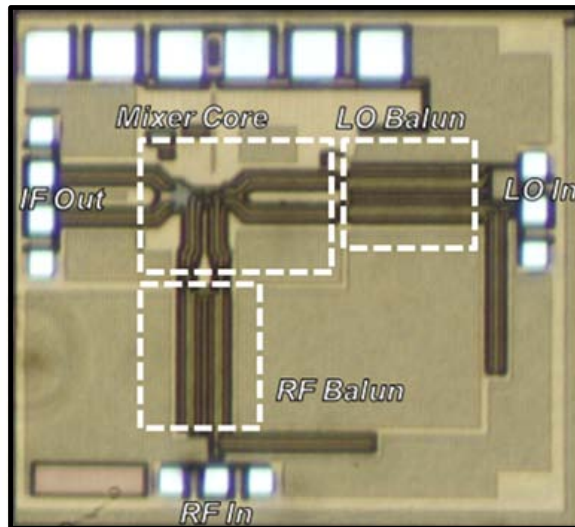
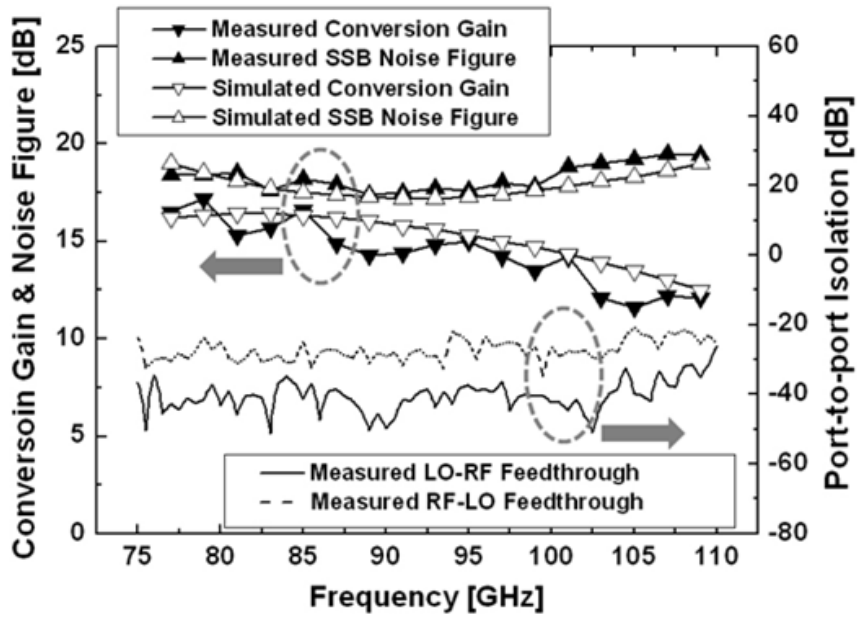
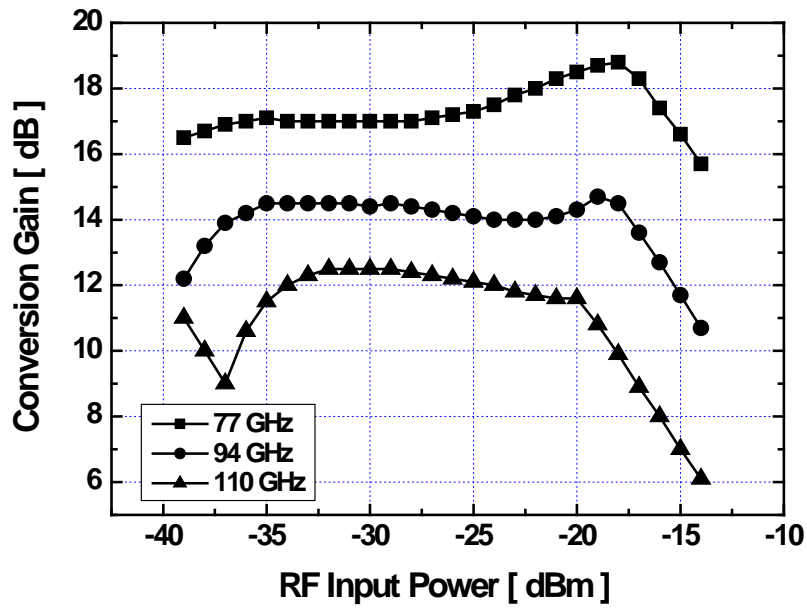


Figure 106. Micro-photograph of designed W-band mixer.



(a)



(b)

Figure 107. Measurement results of designed W-band mixer. (a) Conversion gain, noise figure, and port-to-port isolations. (b) $P_{1dB,in}$ with LO power of 0 dBm.

was measured and adjusted by 3 dB to obtain the differential output power level. Figure 107 presents measurement results of designed W-band mixer. The measured conversion gain varies from 14.5 dB to 17.2 dB depending on operating frequencies. The low-side LO injection was used for the down-conversion, and the IF was fixed at 500 MHz for all measurements. Measured conversion gain, SSB noise, port-to-port isolations, and input-referred 1-dB gain compression points (P_{1dB_in}) at three different RF frequencies are also plotted in Figure 107. The measured P_{1dB_in} at three different input frequencies are -15, -16, and -18 dBm at 77, 94, and 110 GHz, respectively. At the LO power level of 3 dBm, the conversion gains start to saturate at all three input frequencies. For the noise figure measurement, we used a combination of a W-band noise source (QNS-FB12LW), a wave-guide mixer, and external amplifiers for down-conversion of the noise. The measured minimum and maximum SSB noise figures are 17.4 dB and 19.5 dB, respectively. The port-to-port isolations were measured using a 110 GHz vector network

Table 9. Performance comparison of W-band down-conversion mixers in SiGe technologies.

Ref.	[93]	[94]	[95]	[96]	[97]	[98]	[98]	This work
Freq (GHz)	65-90.8	75-78	75-79	75-85	75-79	70-80	89-97	75-110
CG (dB)	> 24	> 10	> 11	> 15	> 13.5	20	15	> 12
NF (dB)	< 18	18.4	< 16.5	< 16.5	< 12.5	< 13.4	< 16.6	< 19.5
P_{1dB_in} (dBm)	-30	-12	-0.3	-3	2.5	-14.7	-10.8	-15
DC power	60mA, -5V	39mA, 4.5V	75mA, 5.5V	34mA, 5.5V	61mA, 5.5V	120mA, 3V	120mA, 3V	28mA, 3.3V
Size (mm ²)	0.247	0.275	0.63	0.533	0.679	3.63	3.63	0.81

analyzer (VNA). The LO-to-RF isolation, which is critical in homodyne receiver architectures, is better than 30 dB across the entire W-band. The mixer consumes 28 mA from a 3.3 V supply. The size of fabricated chip is 0.81 mm². The performance of designed W-band mixer is compared with other SiGe W-band mixers in Table 9.

5.6. Design of an Integrated W-Band Receiver

5.6.1. Receiver structure

Individual building blocks (the LNA, the Marchand balun as RF and LO inputs, and the mixer) were integrated to implement a W-band receiver chain. The diagram of the receiver and micro-photograph of the fabricated chip are presented in Figure 108. The LNA features two-stage cascode topologies with single-ended input and output. The balun integrated with input matching network of the mixer converts the single-ended input signal to differential signal. Another balun at the LO input also converts the single-ended LO signal from the external signal generator to the differential signal to perform down-conversion in the mixer. In order to minimize unwanted feed-through problems (or maximize the isolation), substrate contacts were densely placed surrounding critical active core blocks and interconnecting transmission lines to tie the substrate to ground and effectively reduce signal couplings. The output matching network of the LNA and the input matching network of the mixer/balun combination were modified to consider actual input/output impedances of preceding/following blocks. (i.e., a stand-alone LNA and a mixer had been matched to 50 Ω).

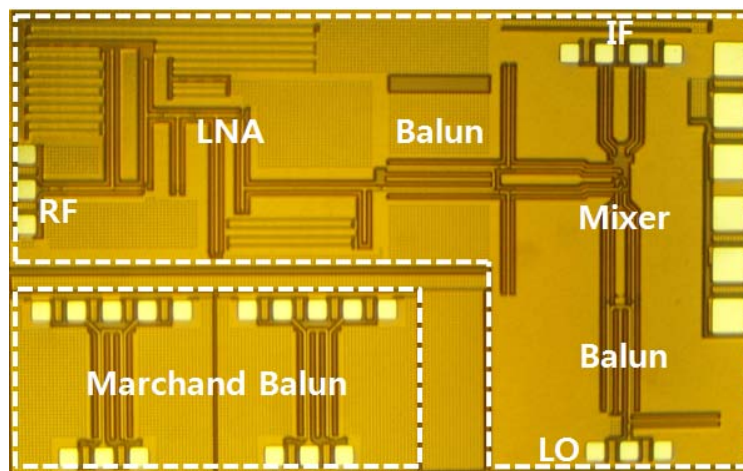
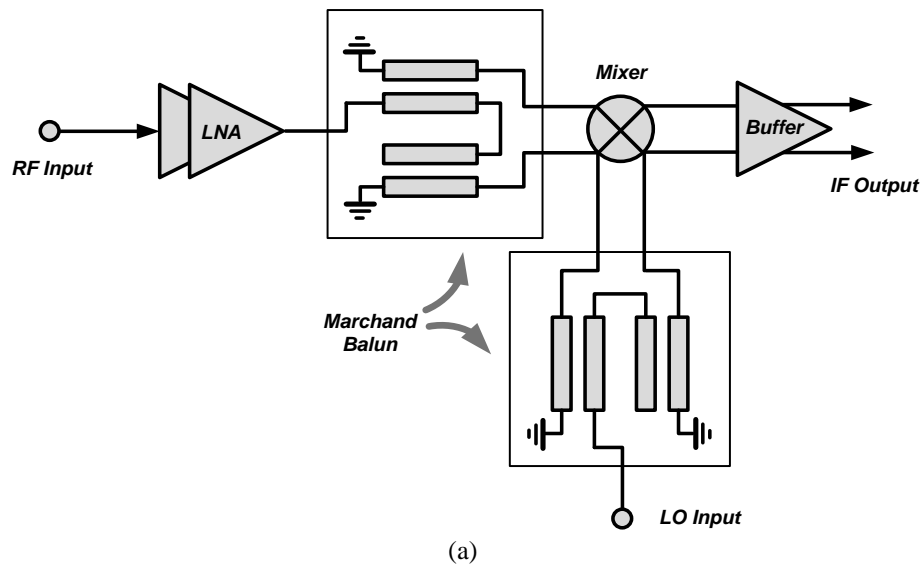
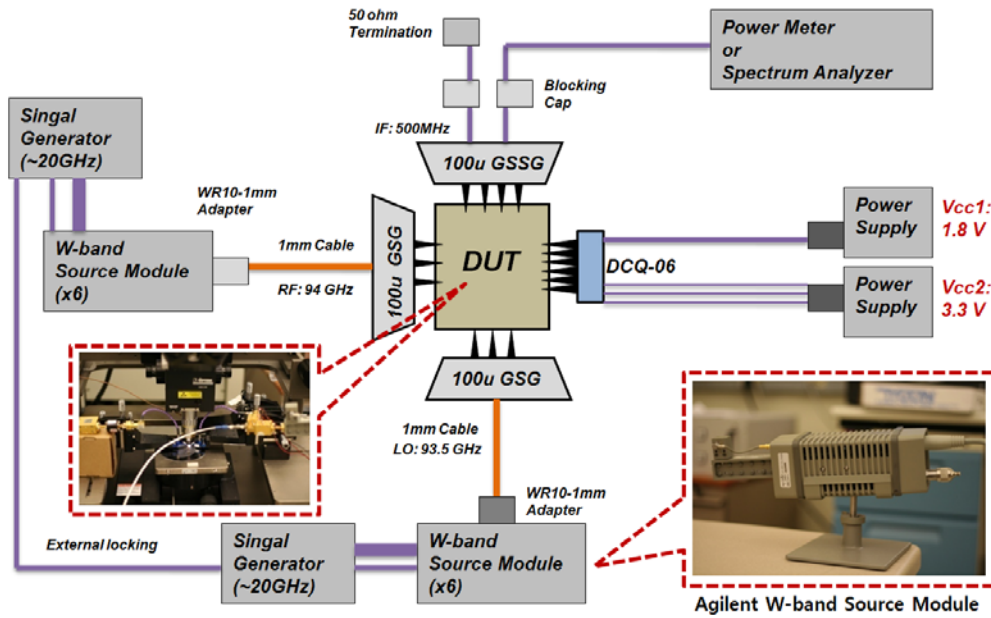


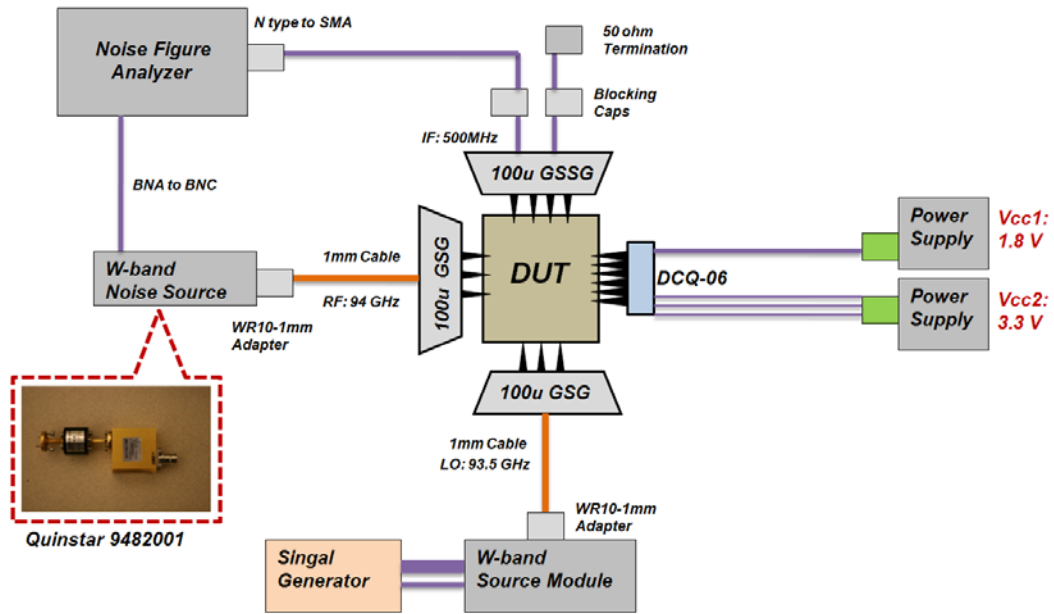
Figure 108. Designed W-band receiver. (a) Diagram of the receiver. (b) Chip micro-photograph of fabricated W-band receiver (the size is 1.82 mm²).

5.6.2. Measurement results

The measurement for the W-Band circuits is also intricate work. The limitation in the highest available frequency of signal sources necessitates the incorporation of other external measurement devices such as up-conversion harmonic mixers, wave-guide



(a)

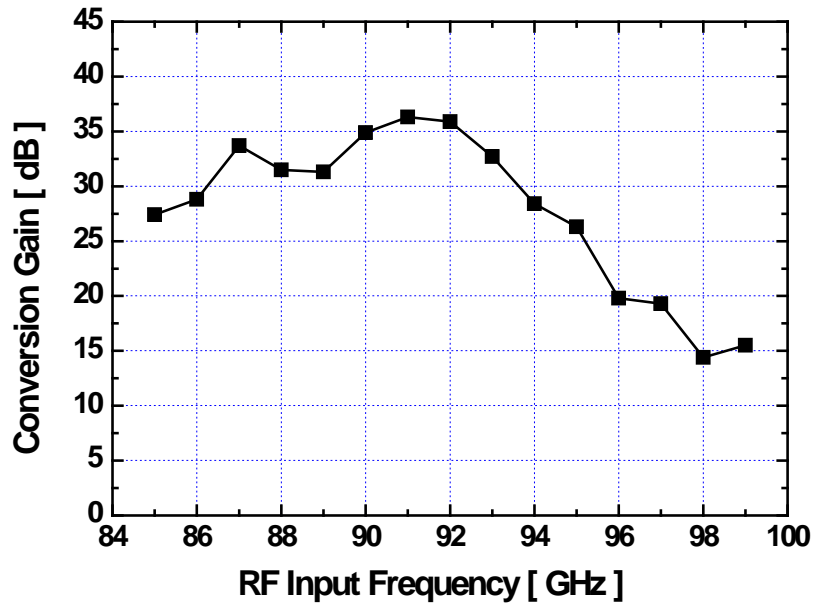


(b)

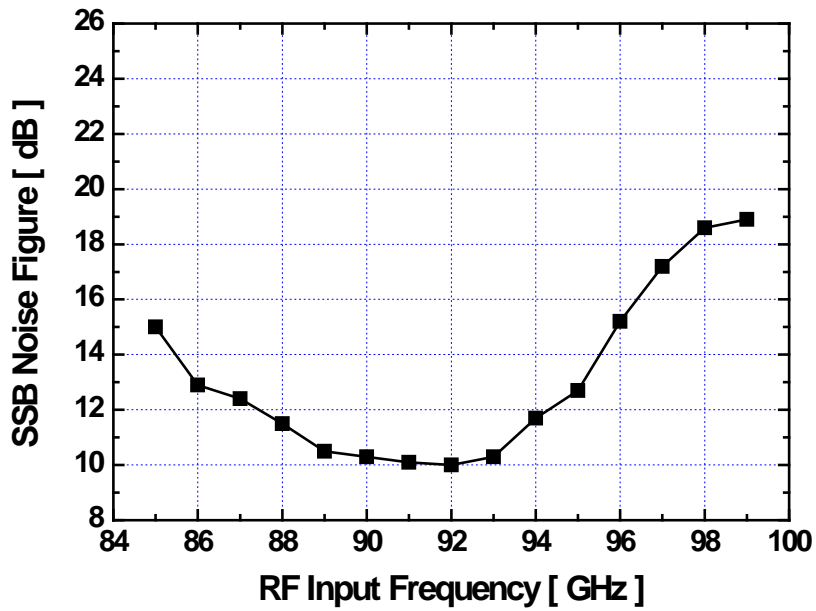
Figure 109. Measurement setup for the W-band receiver. (a) For a conversion gain. (b) For a noise figure.

mixers, external amplifiers, etc. The measurement setups for a conversion gain and a noise figure are presented in Figure 109. On-wafer measurements using GSG probes for RF and LO input were performed. A GSSG probe was used for the IF output. To generate 85 to 100 GHz external signals, two MMW source modules, the OML S10MS and the Agilent 83558A, were used in combination with Hewlett Packard 20 GHz signal generators (83622B). Using the Agilent W-band power sensor (W8486A) and the power meter (E4419B) a reference power level table was made through the frequency range of interest to de-embed all possible losses due to RF cables and wave-guide adapters. The minimum power level that can be generated from the signal source was around -60 dBm. The RF power level of -50 dBm was chosen to observe the variation of the conversion gain while sweeping RF input frequency or applied LO power level. In all cases, the IF output frequency was fixed at 500 MHz. The single-side band (SSB) noise figure was measured using the Quinstar Technology W-band noise source (QNS-FB12LW) and the Agilent noise figure analyzer (N8972A). Careful calibration was performed with the W-band noise source in combination with a wave-guide mixer (QMB-FBFBWS), an LNA (QLW-75B05015-I1) and a PA (QPW-75B01315-I1) before measuring the actual noise figure.

The measured performances of the W-band receiver are presented in Figure 110 and 111 with comparison to simulation results. A maximum conversion gain of 36.3 dB was achieved with 2-dBm LO power level at 91 GHz. In the frequency range of 87 to 93 GHz, the conversion gain is greater than 32 dB. The measured minimum SSB noise figure is 10 dB at 92 GHz. From 85 to 96 GHz, the SSB noise figure is less than 15 dB. The peak-gain frequency was shifted by 3 GHz compared to the simulation result in



(a)



(b)

Figure 110. Measurement results of designed W-band receiver. (a) Conversion gain vs RF input frequency. (b) Noise figure vs RF input frequency.

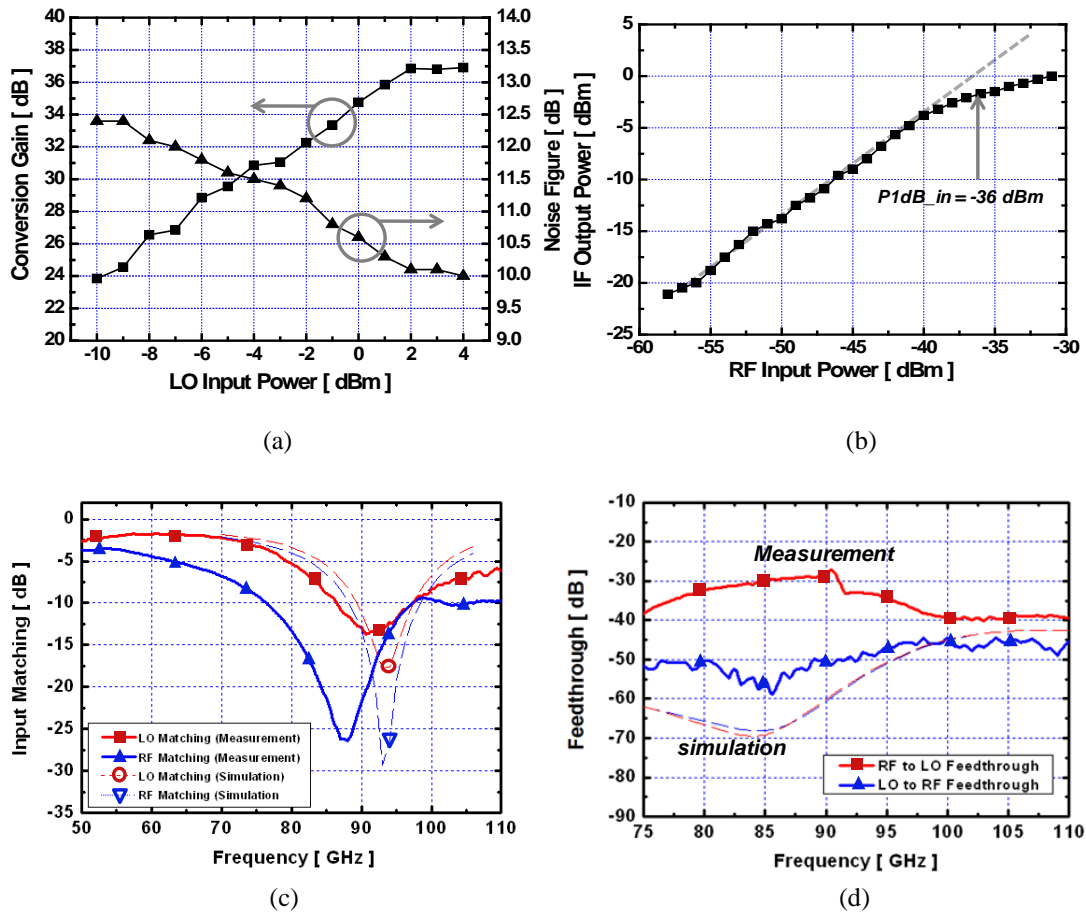


Figure 111. Measurement results of designed W-band receiver. (a) Conversion gain and noise figure vs LO input power. (b) IF output power vs RF input power. (c) RF and LO input matching. (d) Port-to-port isolations.

which the transmission line models in the design-kit (transmission lines with smaller characteristic impedance) are used. With input/output matching networks in which EM model of transmission lines are used, the conversion gain versus frequency plot is shifted down by 3 dB, which is coincident with measurement result. The measured P_{1dB_in} is -36 dBm. The RF frequency and LO power were fixed at 91 GHz and 2 dBm, respectively. The S-parameters were measured from 20 to 110 GHz using Agilent 8510C VNA. The return losses for RF and LO ports are better than 10 dB in the range of 87 to 94 GHz.

The RF to LO and the LO to RF isolation are better than 28 dB. The integrated W-band receiver performance is summarized in Table 10 with comparison to other SiGe W-band receivers.

5.7. Conclusion

The issues and design methodologies for W-band receiver building blocks: a balun, an LNA, a down-conversion mixer were presented in detail. Individual circuit components implemented using SiGe BiCMOS technology with f_T of 200 GHz. The planar-type Marchand balun was designed using hybrid-type coupled transmission lines achieving -8 dB and -9.5 dB for S_{21} and S_{31} , respectively. The two-stage LNA with cascode structure was designed showing a gain of 26 dB and a noise figure of 8.4 dB at 96 GHz. The double-balanced down-conversion mixer was also implemented with integration of the Marchand balun for RF and LO inputs. The fabricated stand-alone mixer achieved a conversion gain of greater than 12 dB and a SSB noise figure of less than 19.5 dB across the entire W-band (75 to 110 GHz) demonstrating very wideband performance. Finally, integrated W-band receiver chain was implemented. Achieved maximum conversion gain is 36.3 dB (at 91 GHz) and minimum SSB noise figure is 10 dB (at 92 GHz).

Table 10. Performance comparison of W-band receivers in SiGe technologies.

Ref.	[35]	[36]	This work
Freq (GHz)	77	77	91
CG (dB)	30	40	36.3
NF (dB)	11.5	8	10
P1dB _{in} (dBm)	-26	-38	-36
IIP ₃ (dBm)	-21.6	-26	-26
DC power (mW)	440	195	109.7

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

7.1. Contributions to the Field

In this dissertation, various approaches with novel design techniques were employed to implement high-performance transceiver front-end ICs operating at RF (2.4 GHz) and MMW (90 to 94 GHz) bands using silicon-based technologies. In Chapter 2, fundamental limitations of silicon-based technology for high-frequency IC designs were reviewed. Implantation issues for RF PAs using CMOS technology were explored in Chapter 3 and 4. Design methodologies and techniques to develop MMW receiver front-end ICs using SiGe technology were discussed in Chapter 5.

To meet increasing demand from modern wireless transceiver industry, adaptation of multi-standards and multi-modes operation schemes to PAs is strongly desired. Inherent difficulties of implementing multi-standards multi-mode PAs for high-data rate applications using CMOS technologies includes low power-efficiency, poor linearity, and limited output power capability. Effective techniques to improve the performance of linear CMOS PA in terms of efficiency optimization for multi-mode operation and maximization of the output power capability were proposed and demonstrated. Employed techniques are:

1. A novel discrete resizing and concurrent power combining structure for minimization of reverse-induced current leakage through disabled combining transformer inputs.
2. A varactor-based tunable matching network to implement the load impedance optimization.
3. A novel parallel-series combining transformer (PSCT) as an output power combiner which overcomes limitations of conventional combining transformers

such as the parallel-combining transformer (PCT) or the series-combining transformer (SCT).

Theoretical analysis and EM simulations were performed to investigate proposed passive structures verifying the effectiveness of them in applications of high-end CMOS PA designs. With these achievements, potential appropriateness of CMOS technologies to develop RF PAs for advanced wireless communications standards such as WiMAX and LTE have been demonstrated, which is the biggest contribution to the related field.

W-band receiver building blocks (an LNA, a balun, and a mixer) and integrated receiver were implemented using SiGe BiCMOS technology with f_T of 200 GHz. Optimization of the circuit performance using well-defined design methodologies were thoroughly performed to demonstrate the usability of SiGe technology for W-band applications (90 to 94 GHz). The operating frequency of designed circuits is almost half of f_T of the process technology. The implementation of receiver building blocks in such a high frequency is an amalgamation of careful EM simulations, parasitic extractions, circuit simulations, and layout optimizations. Given limited design resources including accurate models for active and passive devices, first-time success of the circuit demonstration is not easy. However, implemented circuit blocks and integrated receiver achieved good performances which well coincides with simulation results, verifying effectiveness of proposed structure and design methodology. The performance of the integrated W-band receiver showed highest conversion gain with reasonable SSB noise figure among reported W-band receivers operating beyond 90 GHz.

7.2. Future Research Directions

Although a part of this research focused on efficiency and power improvement techniques for RF CMOS PAs, linearity performance of CMOS PAs is also important for advanced wireless communications. To implement CMOS PAs that completely satisfy

specifications of high data-rate wireless communication standards, sophisticated design techniques with a device/structure view point must be incorporated to improve the linearity performance as well. In addition, the load-sensitivity problem of CMOS PAs is another issue to be overcome as a future research.

For the part of the research on the W-band SiGe IC designs, more accurate modeling of passive devices such as transmission lines must be performed. In addition, various topologies and techniques that have been utilized for applications in RF bands can be employed to enhance the linearity and noise performance of the receiver.

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VITA

JIHWAN KIM

Jihwan Kim was born in Suwon, Korea in 1978. He received his B.S. degree in electrical and computer engineering from Hanyang University, Seoul, Korea in 2005. In 2007, he received his M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, where he is currently pursuing his Ph.D. degree. His major research interests are designing RF and mm-wave front-end integrated circuits including power amplifiers (PAs), mixers, low-noise amplifiers (LNAs), and voltage-controlled oscillators (VCOs) using CMOS/SiGe technologies.

He has worked as an intern at Samsung Design Center, Atlanta, GA, in 2008 designing CMOS LNAs for GSM/GPRS applications and at RF Micro Devices (RFMD), Torrance, CA, in 2009 designing high performance GaAs pHEMT LNAs and PAs for millimeter-wave applications.