

NOVEL PROCESSING OF SOLAR CELLS WITH POROUS SILICON TEXTURING

R. Lüdemann^{1,2}, B.M. Damiani¹, A. Rohatgi¹

¹Georgia Institute of Technology, University Center of Excellence for Photovoltaic Research,
777 Atlantic Drive, Atlanta, GA 30332-0250

²Fraunhofer Institute for Solar Energy Systems ISE, Oltmannsstr. 5, D-79100 Freiburg, Germany

ABSTRACT

A simple porous silicon texturing technique that is applicable to various kinds of silicon material, including multicrystalline and ribbon Si, of any doping type and level is used to fabricate solar cells. Acidic etching of Si leads to a homogeneous porous silicon (PS) surface layer with reflectance as low as 9%. Phosphorus diffusion and thermal oxidation are shown to produce very low emitter saturation current density, 128 fA/cm^2 , which is only slightly higher than values obtained on planar surfaces, but still capable of giving open-circuit voltages in excess of 650 mV. The dopant oxide solid source (DOSS) solar cell process with its simultaneous formation of phosphorus emitter and *in-situ* surface oxide leads to an excellent surface passivation, while maintaining low reflectance on PS-textured wafers. The fabricated solar cells show efficiencies of up to 14.9% using the PS layer as an anti-reflection coating (ARC) and surface passivation. This is the highest reported value with this kind of texturing and without any additional ARC. The simplicity of the process makes it a very promising technology and easily transferable into industrial production.

INTRODUCTION

Surface texturing is an important tool to improve the conversion efficiency of silicon solar cells. In addition to reduced reflection of the incoming light, light-trapping of long wavelength light is also desirable, which becomes even more important for thinner wafers or ribbon materials. While monocrystalline silicon can easily be textured by alkaline solutions etching preferably in $\langle 111 \rangle$ direction, texturing of multicrystalline (mc) Si consisting of grains with different orientation is still a challenge. A promising technique is the formation of porous silicon (PS): Etching of silicon wafers in diluted nitric and hydrofluoric acid at room temperature leads to an appropriate porous surface layer, which gives the wafer a blue-to-purple look in order to minimize reflection.

Several groups are working on the application of PS layers to silicon solar cells (a review is given in [1]). The common objective is to form an antireflective (AR) "coating" and simultaneously etch back the emitter by forming PS on finished cells. Since the metallization acts as an etch mask, a selective emitter is formed. However, this method has several draw-backs: The metallization is attacked by the etching, leading to inhomogeneity and, most

important, to a degradation in fill factor [2]. In addition, the etch solution is contaminated with metal, which limits its usability and re-usability and demands expensive waste management. Moreover, another wet-chemical step does not fit well into an industrial fabrication sequence and holds the risk of carrying off chemicals (especially since porous surfaces tend to soak liquids). Therefore, we focus on the formation of PS during the normal cleaning sequence at the beginning of the solar cell process.

ACIDIC SURFACE TEXTURING

Porous Silicon Formation

Porous silicon is typically formed using the electrochemical process for uniformity reasons and controllability [3]ADDIN. A more simple, pure chemical technique is the so-called stain etching in a HNO_3/HF . This etching strongly depends on the type and doping level of the silicon material, since the reaction is actually a localized electrochemical etching [4]. Therefore, lower resistivity wafers etch faster. However, we have succeeded in forming PS on different float zone (FZ), Czochralski (Cz), multicrystalline (mc) silicon, and even ribbon material like EFG and String Ribbon of different resistivities using the acidic etch or stain etching process. Even high resistivity n-type FZ can be etched.

The stability of the porous silicon texture against subsequent processing, particularly other chemical etching steps, is one of the most challenging technological problems of this technique [5]. The PS layer formed by our process, though, is the final step in the cleaning process and is subsequently dried and loaded into the furnace. A thin PS layer was found to maintain anti-reflection qualities over a 60 min. diffusion followed by a 15 min. oxidation at 925°C . If the PS layer is too thick, the optical qualities are not maintained during the diffusion cycle. However, removal of the phosphosilicate glass (PSG) removes the PS texturing at least partly.

Optical Properties of Porous Silicon

The diffuse reflectance (Fig. 1) of PS-textured silicon shows a minimum at about 600 nm, reflecting its color after etching. The weighted reflectance (R_w), that is the integral reflectance between 400 and 1100 nm weighted with the AM 1.5 global spectrum, is as low as 9% for low-resistivity p-type FZ and mc-Si and 15% for high-

resistivity n-type FZ-Si, respectively, compared to 35 % of a planar surface. The higher reflectance of high-resistivity silicon is due to the slower etching resulting in a thinner PS layer that does not minimize the reflectance.

It is interesting to note, that above 500 nm the reflectance characteristic of PS texturing is similar to that of a SiN_x antireflective (AR) coating. This might indicate, that the porosity of the PS layer is low, so that above 500 nm it acts like a virtual dielectric layer resembling SiN_x with n=2 and 780 nm thick layer. The weighted reflectance, though, is still more than 0.5 % absolute lower than that of an SiN_x AR coating.

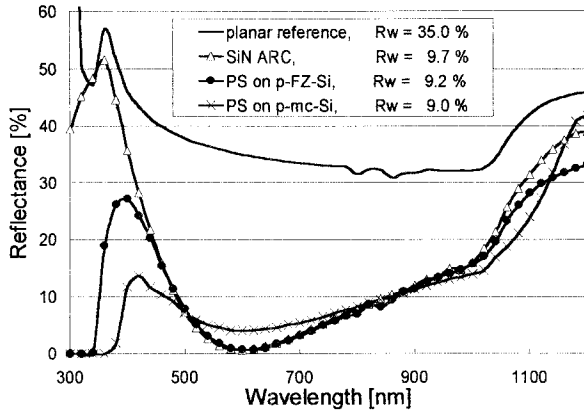


Fig. 1. Reflectance of planar silicon, silicon with SiN AR coating, and with porous silicon texturing, respectively.

Electrical properties of porous silicon emitter

The good reflectance comes with a rough surface that leads to high surface recombination velocities (SRV), on the order of 10^5 cm/s if not passivated. In addition to the above mentioned problem, the porous silicon texture could be removed by the PSG etching after diffusion. This calls for a special emitter formation process, that includes surface passivation but no PSG removal. We have therefore applied the dopant oxide solid source (DOSS) diffusion method [6] described in more detail below. This process simultaneously forms a phosphorus emitter and an *in-situ* surface oxide leading to excellent surface passivation, while maintaining low reflectance on PS-textured wafers.

The phosphorus source used for diffusion in this process yields a sheet resistivity range of 6-600 Ω /sq. at 925°C, and can be tailored to the desired sheet resistivity by selecting the proper concentration of P₂O₅. For a diffusion cycle that gave a 40 Ω /sq. emitter on a planar surface, an emitter saturation current J_{oe} of 500 fA/cm² is obtained. A PS textured sample diffused during the same furnace process gave a J_{oe} of 128 fA/cm², which could give open-circuit voltage V_{oc} values in excess of 650 mV.

Due to the porous structure the sheet resistivity on textured samples is not measurable by the four-point probe method directly. After removing the PS layer by a 4 min. oxide etch (BOE) to expose a bare silicon surface, a

sheet resistivity of approx. 250 Ω /sq. is measured. However, the doped porous silicon surface layer might contribute to the lateral current transport, so the actual sheet resistance could be lower than 250 Ω /sq. An alternate way of extracting a realistic value can be done from using the J_{oe} dependency on the sheet resistance: Fig.2 shows a graph of values obtained on planar samples using the DOSS diffusion method. The corresponding emitter sheet resistivity to a J_{oe} value of 128 fA/cm² as measured for a PS textured sample is around 100 Ω /sq. In contrast, a 250 Ω /sq. planar sample has an emitter saturation current as low as ~75 fA/cm².

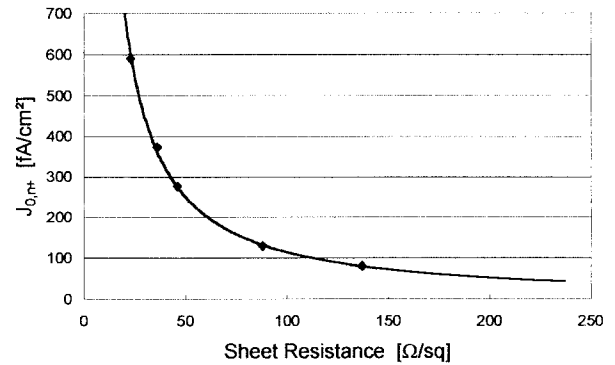


Fig. 2. Emitter saturation currents for planar samples diffused using the STAR process. PS had a 128 fA/cm² J_{oe} for an approximate 250 Ω /sq. diffusion under the PS layer.

So, by forming the PS layer before furnace diffusion and in-situ oxidation, the emitter saturation current density, J_{oe} , that results from a DOSS diffusion is comparable to planar values which now enables us to implement this texturing scheme in a high-efficiency solar cell process.

POROUS SILICON TEXTURED SOLAR CELLS

DOSS solar cell processing

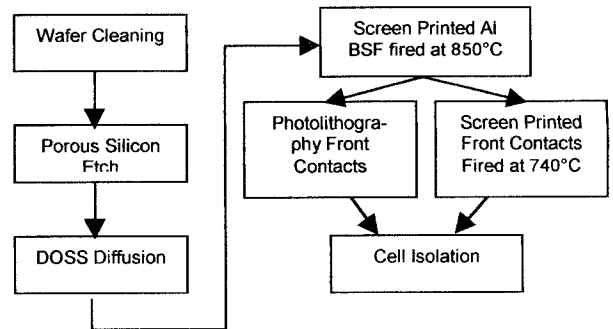


Fig. 3. Process Flow Chart

Using the dopant oxide solid source (DOSS) diffusion method [6], porous silicon textured solar cells with a screen printed Al BSF have been fabricated from 0.6 Ω -cm

FZ-Si (Shin Etsu), 0.7-1.3 $\Omega\cdot\text{cm}$ Cz-silicon (Bayer) and 0.2 $\Omega\cdot\text{cm}$ mc-Si (Eurosolare). The process sequence is shown in Fig. 3. The diffusion of phosphorus has been performed by using source wafers with spin-on dopant applied to both sides, which have been introduced to the furnace together with the samples so that every sample is stacked in front of one source wafer for emitter formation. Phosphorus is released from the source wafers at 925 $^{\circ}\text{C}$, diffuses into the samples to form the emitter. By offering oxygen, an in-situ oxidation is achieved. The actual diffusion time has been one hour, followed by an oxidation step for 15 min to obtain the *in-situ* oxide. This one step furnace process leads to diffused, textured, *in-situ* oxide passivated, and AR-coated solar cells using a porous silicon layer. It has to be noted, that no PSG removal is included in this process. Thus, the DOSS method is a perfect match for PS texturing.

By stacking high resistivity ($>100 \Omega\cdot\text{cm}$) n-type float zone silicon wafers between two phosphorus source wafers, samples to measure the lifetime and dark saturation current density with n^+n^+ structure have also been fabricated.

The phosphorus dopant is a limited diffusion source and can be tailored to obtain any desired sheet resistivity for a given process by changing the concentration of P_2O_5 contained in the spin-on glass. This is an important consideration for porous silicon textured samples. The porous silicon layer acts somewhat as a diffusion barrier by limiting the phosphorus dopant implanted into the bulk silicon region for junction formation. Thus a much heavier concentration of P_2O_5 is required to obtain the desired sheet resistivity as would be necessary for a planar sample or even a random pyramid textured sample. The overall thickness of the PS layer contributes to whether or not the PS layer is completely oxidized during the furnace step.

DOSS solar cell results

Table 1. Best porous silicon solar cell results for photolithography (PL) and screen printed porous silicon solar cells. **Confirmed at Sandia National Labs.

Material	Voc(mV)	Jsc(mA/cm ²)	FF	Eff(%)
**0.6 Ωcm FZ	629	29.32	0.807	14.9 (PL)
1.0 Ωcm Cz	618	27.61	0.785	13.4 (PL)
0.2 Ωcm mc	615	27.07	0.762	12.7 (PL)
0.6 Ωcm FZ	627	28.91	0.759	13.8 (SP)
1.0 Ωcm Cz	613	27.05	0.768	12.7 (SP)
0.2 Ωcm mc	602	26.70	0.741	11.9 (SP)

The PS layer has been formed prior to emitter diffusion and metal contact formation. The solar cells have

been fabricated using a diffusion process that yields 20 Ω/sq . on a planar surface. This ensures a sufficiently heavy diffusion on the PS textured samples. Table 1 shows results obtained for both photolithography front contacts and screen printed front contacts. For the photolithography process metal contact has been made by re-

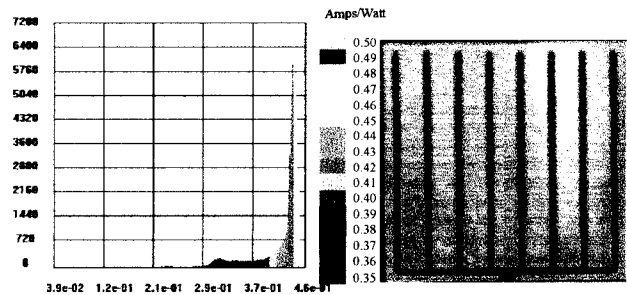


Fig. 4. LBIC map of 0.6 Ω/cm FZ 4 cm^2 sample with a Porous Silicon anti-reflection coating.

moving the in-situ oxide and PS layer below the area to be covered by metal. Screen printed front contacts were simply added directly to the PS surface. Initial results show excellent potential for further development including the highest confirmed efficiency reported to date at 14.9 %. Excellent open circuit voltages and fill factors in excess of 80 % are demonstrated for photolithography cells. A 29.3 mA/cm^2 short circuit current is obtained for a AM1.5 global weighted reflectance of 17 %. Since PS layers with a 9% AM1.5 global weighted reflectance are already demonstrated (see Fig. 1), there is potential for even higher current collection. Further optimization of the starting sheet resistance and lower reflectance can result in much higher cell efficiency.

As is apparent from the open circuit voltage the surface passivation is sufficient to maintain good V_{oc} values. The reduced efficiency results from the decreased current collection due to the non-optimal PS layer.

The potential for increase performance is supported by the following two graphs. Fig. 4 and Fig. 5 show the uniformity of the PS as a anti-reflection coating as well as a good internal quantum efficiency, IQE. The uniformity of the PS layer as an anti-reflection coating is shown in the LBIC map in Fig. 4. This demonstrates that the reflectivity of the solar cells can be tightly controlled allowing for maximum current collection when coupled with the good IQE shown in Fig. 5. The non-uniformity of PS can be avoided through a more thorough understanding of PS formation via a stain etching method. A 0.6 Ω/cm FZ sample is used to focus on any artifacts that may arise in the use of a PS layer for the IQE measurement.

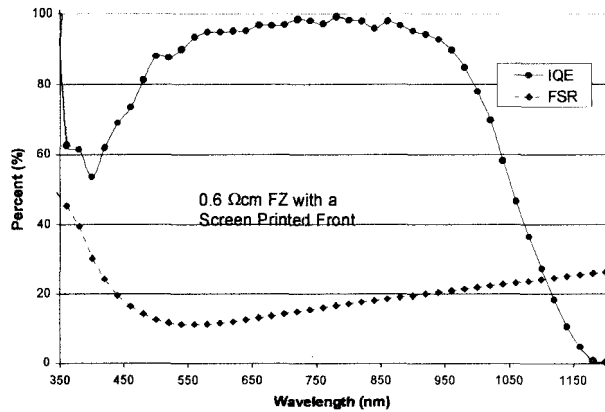


Figure 5. Internal Quantum Efficiency and Front Surface Reflectance for Porous Silicon textured FZ sample

CONCLUSIONS

Porous silicon etching is a very simple technique to texture multicrystalline silicon. Low reflectance and very good surface passivation is possible. The DOSS solar cell process is able to take full advantage of this kind of surface texturing. The diffusion from a limited source can be tailored to obtain the desired sheet resistivity underneath the PS layer that will maximize the solar cell performance and has demonstrated excellent fill factors. Poor fill factors have been a problem in the past for further development of PS textured solar cells. This problem is completely overcome in this study which resulted in a 0.807 fill factor. The *in-situ* oxidation appears to completely oxidize the PS layer to obtain excellent surface passivation, and because the process does not require the removal of the phosphorus silicate glass after diffusion, which would remove the texturing, low reflection can be maintained. The simplicity of the whole process can make the transfer into production easy and fast, leading to commercially available high efficiency multicrystalline silicon solar cells. Cell fabrication needs to be optimized, though, in order to realize the full potential of PS texturing.

Acknowledgements

The authors would like to thank Vijay Yelundur, Jed Brody, Mohammed Hilali, and Martin Schnell for fruitful discussions.

REFERENCES

- [1] R.R. Bilyalov, L. Stalmans, L. Schirone, et al., "Use of porous silicon antireflection coating in multicrystalline silicon solar cell processing", *IEEE Trans. Electron Devices* **46**, 1999, pp. 2035-2040.
- [2] M. Schnell, R. Lüdemann and S. Schaefer, "Stain Etched Porous Silicon - A Simple Method for the Simultaneous Formation of Selective Emitter and ARC", *Proc. 16th EU PVSEC*, 2000, pp. in print.

- [3] L. Canham, *Properties of Porous Silicon*, UK INSPEC 1997, p.405.
- [4] S. Shih, K.H. Jung, T.Y. Hsieh, et al., "Photoluminescence and formation mechanism of chemically etched silicon", *Appl. Phys. Lett.* **60**, 1992, pp. 1863-1865.
- [5] R. Einhaus, E. Vazsonyi, F. Duerickx, et al., "Recent Progress with Acidic Texturing Solutions on Different Multicrystalline Silicon Materials including Ribbons", *Proc. 2nd WCPEC*, 1998, pp. 1630 - 1633.
- [6] T. Krygowski and A. Rohatgi, "A simultaneously diffused, textured, in situ oxide AR-coated solar cell process (STAR process) for high-efficiency silicon solar cells", *IEEE Trans. Electron Devices* **45**, 1998, pp. 194-199.