

Modeling of Integrated Circuit Interconnect Dielectric Reliability Based on the Physical Design Characteristics

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Modeling of Integrated Circuit Interconnect Dielectric Reliability Based on the Physical Design Characteristics

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To my family

who

I know have waited this moment so long

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SUMMARY

The objective of the research is to model the reliability and breakdown mechanism of back-end dielectrics in integrated circuits and to investigate the impact of physical design characteristics on the back-end dielectric reliability. As design and process complexities continue to increase, the reliability of the back-end dielectrics becomes marginal. This is mainly because the power supply voltage is not scaled at a rate comparable to feature size, which results in exponentially increasing electric fields among interconnect lines. Therefore, it is strongly desirable to be able to predict reliability or to detect design weaknesses to reliability failure during the pre-silicon verification stage.

It is desirable to enable pre-silicon verification of back-end dielectric reliability based on physical design characteristics. In this research, it is shown that dielectric reliability can be modeled as a function of the critical circuit area based on the yield models. Defect clustering is taken into account by using the negative binomial statistics. The physical design characteristics will be investigated for their impact on back-end dielectric reliability.

These characteristics include such factors as layout geometry, pattern density, pattern orientation, and via placement. The physical breakdown mechanism for porous back-end dielectric films is also to be investigated using Monte Carlo simulation. It is shown that the electric field is enhanced by porosity in ultra-low- k dielectric films. The electric field enhancement caused by the porosity is shown to accelerate the charge transport.

CHAPTER 1

INTRODUCTION

1.1 Background

1.1.1 Recent Trends in Device Scaling and Signal Delay

Figure 1.1 shows the recent trend of device scaling. Even if this figure only shows the device scaling trend and projection for the near future for transistor critical dimension, back-end interconnect feature sizes also have been scaled accordingly to match the front-end trend. The purpose of this aggressive scaling is twofold. One is to save the silicon area and the other is to improve circuit performance.

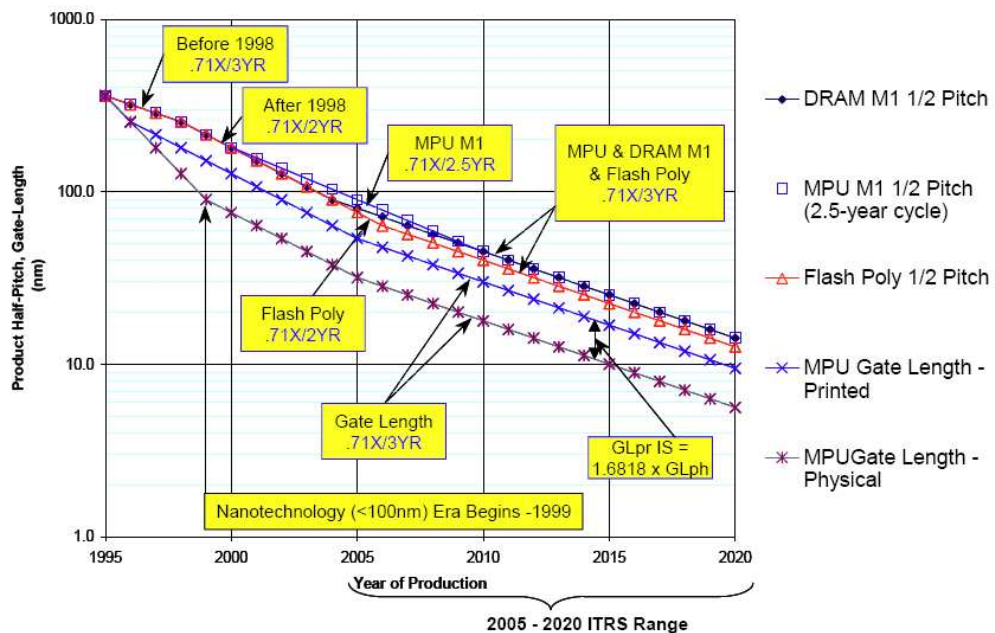


Figure 1.1: Device scaling projection shown in terms of gate length (half pitch) in various product types [1].

Approximately up to about the $0.25\mu\text{m}$ technology generation, device scaling has served these two purposes very well. As the critical dimensions of devices were scaled down to a smaller size, we could pack more devices in a fixed silicon area while

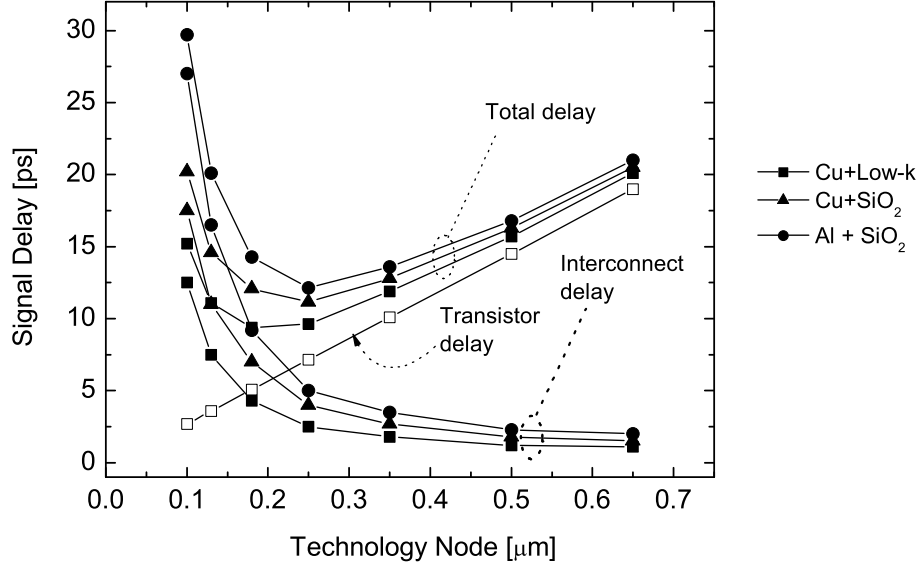


Figure 1.2: Signal delay trend as a function of device scaling. It is shown that the rapid increase in interconnect delay plays a major role in total signal delay as the device feature size gets smaller.

achieving improvement in circuit speed at the same time. However, below the $0.25\mu\text{m}$ technology node, scaling down the device size resulted in the increased signal delay, which was unexpected considering the previous trend. Figure 1.2 demonstrates this reversal in the signal delay trend.

This happens because, unlike transistors, the interconnect miniaturization causes the components in RC delay product, which is the product of interconnect resistance (R) and dielectric capacitance (C), to grow. Actually there seemed to be no reason to worry about the signal delay contribution from the interconnect RC component because interconnect itself was a very good conductor and the spacing between the adjacent interconnects was far enough to keep the RC product at a negligibly low level. However, reduced interconnect cross-sections make the interconnect resistance higher while the decreased spacing between neighboring interconnects makes the capacitance between them bigger. Therefore, at the $0.25\mu\text{m}$ technology node and below, the speed improvement benefit from front-end transistor scaling is overwhelmed by the

compensating RC delay increase resulting from back-end miniaturization.

1.1.2 Solution for Signal Delay: Copper and Low- k Back-end Process

Copper and low- k dielectric materials have been introduced as a solution for reducing RC delay for technologies 0.18 μm node and below [2]. Copper is one of the best electrical conductors available having very low resistivity that is approximately 60% of aluminum. Another important advantage of copper over the conventional interconnect material, aluminum, is that copper is more electromigration-resistant. Usually, resistance to electromigration of a metal can be estimated with its melting point. A higher melting point means stronger bonds between atoms and, in turn, it means less chance for the atoms to be displaced by the momentum transfer from colliding electrons. The melting point of copper is significantly higher than that of aluminum, and it is 1084.6°C, while that of aluminum is 660.25°C.

Copper's higher resistance to electromigration allows higher current density compared with the conventional aluminum interconnect. By allowing higher current to flow through the interconnects, the circuit speed can be improved accordingly. Or, if the priority is in integration, we can use smaller interconnects with the same current density as before.

While copper is used to achieve a reduced interconnect resistance (R), low- k dielectric material was introduced to make the capacitance (C) of the inter-metal dielectric smaller. The reduction in RC signal delay by using these new materials is displayed in Fig. 1.2. Many schemes have been developed to lower the dielectric constant of the inter-metal dielectric (IMD) and these can be categorized into two groups. One is to decrease the polarization by using materials with less polar bonds, and the other is to decrease the density of the material by introducing porosity. Examples of the first kind include certain low- k materials, where some of the Si-O bonds in silica have been replaced with less polar bonds, such as Si-F or Si-C. A more fundamental reduction

can be achieved by using virtually all non-polar bonds, for example C-C or C-H, as in materials like organic polymers [3].

Because there is a limit in lowering the dielectric constant by manipulating the polarizability of the bonds, it seems inevitable that the material density will be reduced to achieve an even lower dielectric constant, as required in the international technology roadmap for semiconductors [4]. The point in the idea of reducing the material density is to remove the source of polarization of any kind. A certain material can be polarized in one or more of the following three ways: electronic, distortion, or orientation polarization. Electronic polarization is due to the displacement of electrons in the atomic structure; displacement of ions is responsible for distortion polarization, while orientation polarization is caused by rearrangement of molecules in the direction of the applied electric field. Therefore, by reducing material density or removing part of the material, the overall polarization will be decreased accordingly, resulting in a lower dielectric constant. The ultimate goal in this case will be to replace the entire dielectric with air whose k value is the lowest possible.

1.1.3 Back-end Reliability Issues

The newly adopted materials introduced in § 1.1.2 are known to be beneficial for circuit performance, but it could be detrimental in terms of reliability. It is partly because of the poor breakdown resistance of the low- k dielectrics and copper drift issue also contributes to the emerging back-end reliability problem.

The fact that the power supply voltage is not scaled at a rate comparable to feature size scaling, which results in exponentially increasing electric fields among interconnect lines as shown in Fig. 1.3 makes the situation even worse.

In this section, we will review the reliability issues originating from the newly introduced materials such as copper and low- k dielectrics.

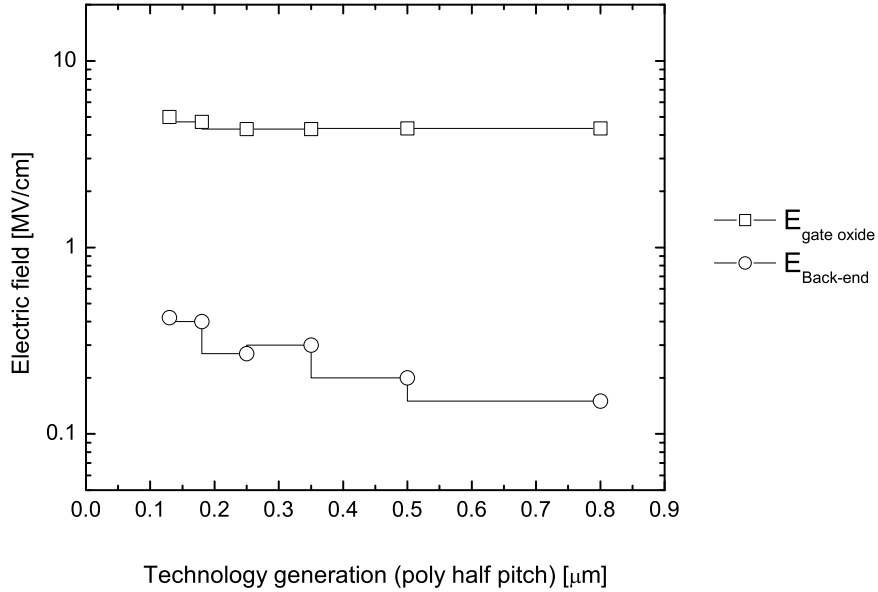


Figure 1.3: Electric field trends in gate oxide and back-end dielectric film. It is shown that the electric field in the back-end increases exponentially, while the electric field in the gate is being restricted to remain almost constant. Reproduced from [5]

1.1.3.1 Copper-related Problems

Copper diffusion: Although copper has many attractive properties as an interconnect material, several reliability issues need to be addressed, especially due to copper diffusion into the dielectric film.

It has been reported that copper can migrate quickly into the low- k dielectric film especially under the influence of an electric field, acting as a charged impurity and degrading the insulating properties [5, 6, 7]. Cu ions are initially injected from the positively biased electrode (anode) through the localized surface defects, drift toward the ground electrode (cathode) under the bias field and temperature, and accumulate near the cathode surface interface.

Time-dependent-dielectric-breakdown tests have been conducted on copper-contaminated SiO_2 Metal-Oxide-Silicon (MOS) capacitors and the result is shown in Fig. 1.6 [6].

The dielectric lifetime dependence as a function of Cu contamination allows us to understand the role of Cu in degrading the dielectric insulating properties. Cu-enhanced electron trap generation occurs continuously during stress, and this leads to an increasing electronic current (electron flow through TEOS mainly by Poole-Frenkel mechanisms which are controlled by the amount of traps [8], as shown in Fig. 1.4).

According to some studies, thermal diffusion of Cu into oxide is negligible at metallization process temperatures ($<400^{\circ}\text{C}$) [7]. It is clear from the fact that the C-V behavior is unaffected by the thermal cycles if no bias is applied. However, in the presence of an electric field at temperatures as low as 150°C , positive Cu ions (Cu^+ or Cu^{2+}) drift rapidly through oxide to degrade field isolation, induce dielectric leakage, and even degrade active devices [9].

There is about five orders of magnitude difference in the lifetimes for a dielectric film with contact to copper relative to the one with contact to aluminum. A field acceleration factor reported in [10] is 7 decades/(MV/cm). This factor is larger than what is typically observed in intrinsic gate oxide reliability cases indicating that the failure mode may be driven by the extrinsic degradation of the dielectric with copper diffusion into the insulator.

The Cu-ion polarity is verified by considering BTS results under negative gate bias [7]. For the Cu-gate capacitors, a positive gate voltage (V_{gate}) shifts the C-V curve horizontally in the negative V_{gate} direction; the longer the applied stress is maintained, the larger the shift as shown in Fig. 1.5 [9]. Since Al does not drift into oxide, the C-V characteristics of corresponding Al-gate capacitors does not change after BTS. The Cu gate serves as a reservoir of Cu^+ ions that can potentially be injected into the underlying dielectric when an electric field is applied.

Because of its quick diffusion through SiO_2 and Si, where it forms impurity levels within the forbidden band gap, Cu needs a suitable diffusion/drift barrier. Figure 1.7 shows the effectiveness of different barrier layers. From this, it is clear that the

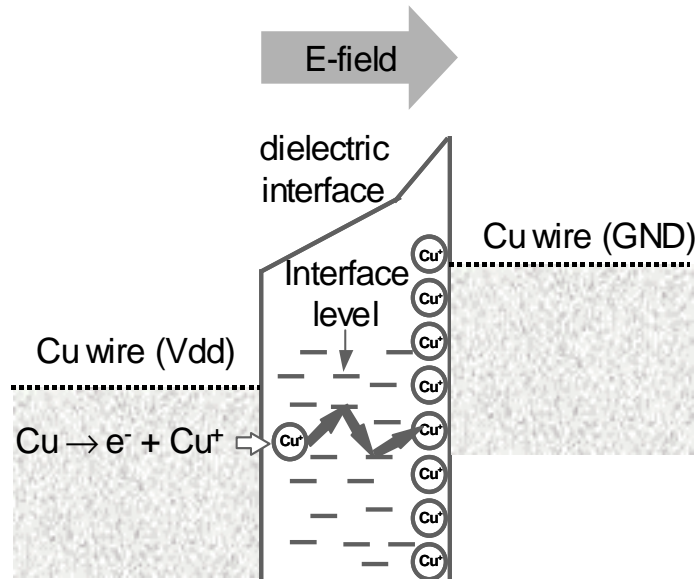


Figure 1.4: Breakdown mechanism of dielectric films in a copper interconnect structure due to copper migration. An explanation about the field enhancement at the cathode can be found in § 2.1. Reproduced from [11].

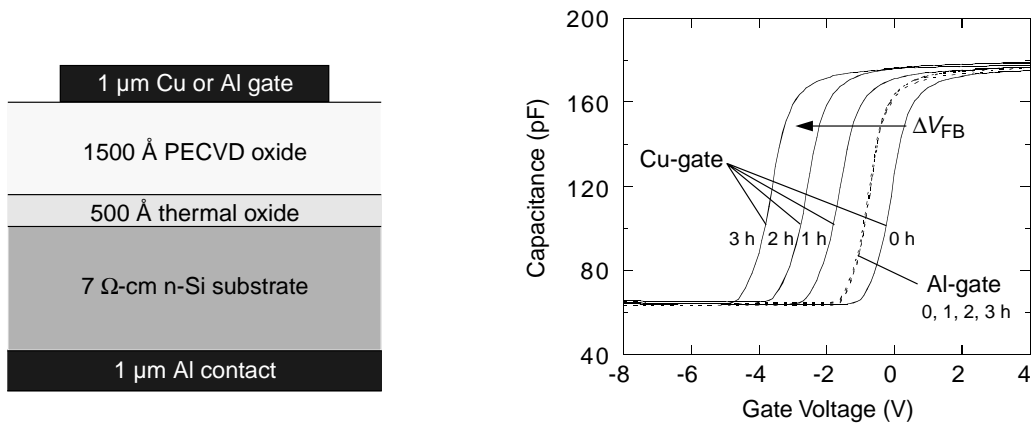


Figure 1.5: A metal-insulator-semiconductor (MIS) test structure to characterize the metal ion drift in a dielectric film (left) and the C-V plot showing ΔV_{FB} (flat band voltage shift) as a function of metal electrode and the duration of stress (right) [9].

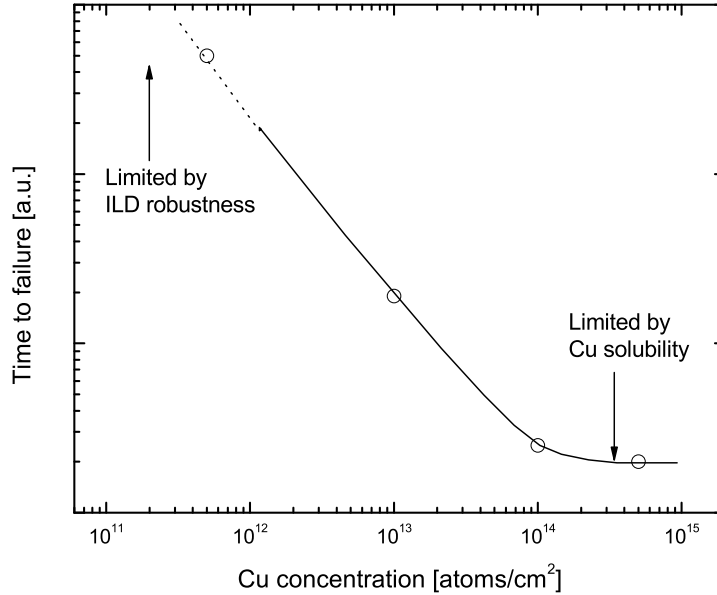


Figure 1.6: Dielectric lifetime as a function of copper concentration. In this experiment, the dielectrics were intentionally doped with copper to see its impact on dielectric lifetime. Reproduced from [6].

presence of a barrier to diffusion improves the dielectric reliability distinguishably.

However a good diffusion barrier does not absolutely ensures against the presence of Cu in the dielectric [6]. Localized surface defects such as a damaged or partly missing Ta barrier layer at the nitride-BCB interface were responsible for the leakage current failures as shown in Fig. 1.8 [12].

Moisture trapped underneath the nitride passivation layer or absorbed in the oxide, which enhances Cu ion diffusion during the B-T stress is also know to be responsible for early failure of the dielectric film [12]. Due to the damascene architecture, some critical steps, such as via etching, could re-sputter Cu atoms on the dielectric side-walls and, if the following cleaning steps are not effective enough, traces of Cu can be left behind the barrier [6]. It was found that the TDDB characteristics strongly depended on the surface condition of Cu and pTEOS before capping with pSiN. NH₃-plasma treatment prior to Cap-pSiN deposition and modification of the

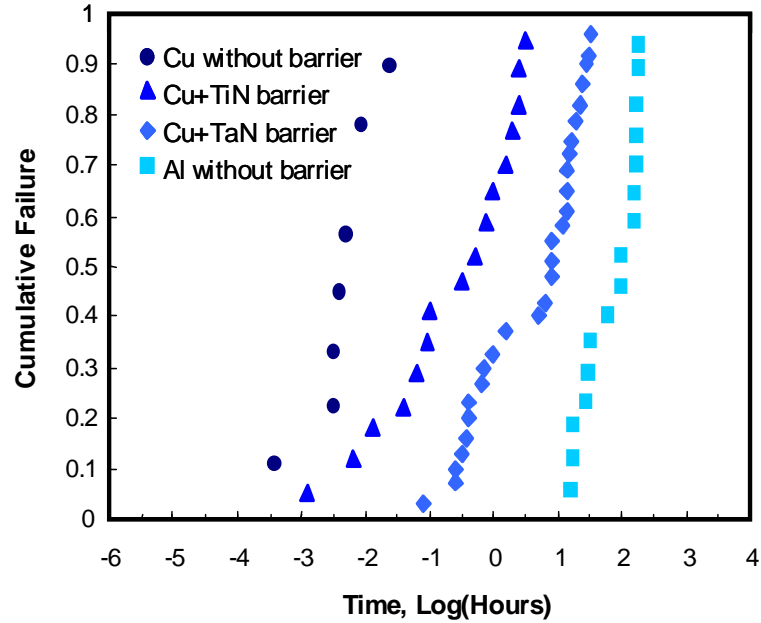


Figure 1.7: Impact of barrier metals on dielectric breakdown. The result shows the role of barrier metal in blocking copper diffusion into the dielectric film. Reproduced from [10].

Cu CMP process improved TDDB lifetime between Cu interconnects [13].

Absence of stable surface oxide: There are two characteristics of copper that make it a concern in terms of reliability. One is the highly diffusing characteristics of copper, and the other is the absence of stable surface oxide. The copper diffusion problem was described in the previous paragraph and in this paragraph, the absence of stable surface oxide will be described.

Stable surface oxide can be an inherent diffusion barrier to diffusing ions. This is why aluminum shows superior reliability to copper even without a diffusion barrier as shown in Fig. 1.7. Once a layer of stable oxide is formed at the surface, it becomes a very effective barrier for diffusing species. But in the case of copper, there is no such stable surface oxide and the copper ions can keep diffusing through the dielectric, leading to a premature dielectric breakdown.

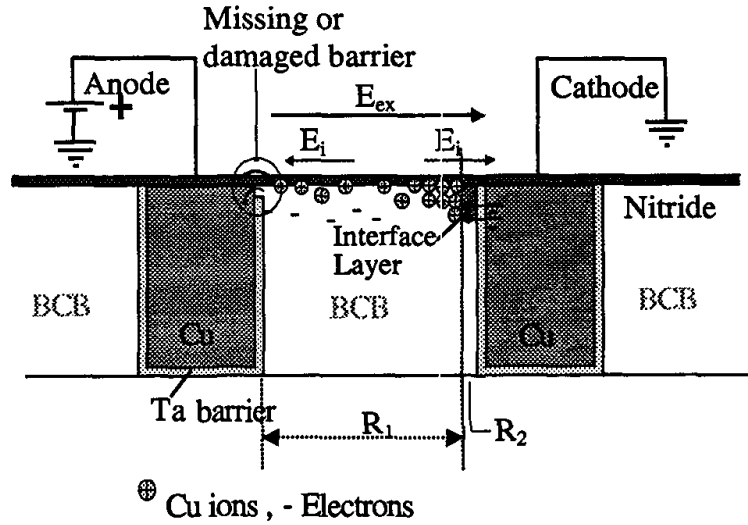


Figure 1.8: A proposed leakage current degradation mechanism between interconnects [12]. In this model, the dielectric surface is shown as the most probable leakage path.

1.1.3.2 Low- k -related Problems

Leaky property: Many researchers reported the inherently leaky property of low- k dielectrics [5, 14, 15]. Figure 1.9 shows the Cu^+ ion drift rates in various dielectrics, and from this it is clear that the ions drift much faster in low- k dielectrics (SiLK or BCB) than in the conventional oxides. Figure 1.10 shows this more clearly by comparing the leakage current as a function of electric field for several low- k dielectrics with a conventional pTEOS oxide. Low- k dielectrics show leakage current levels several orders higher than conventional pTEOS oxide.

Thermal conductivity: Low- k materials are known to be inherently poor thermal conductors. The trend of increasing the number of transistors in circuits means more total power consumption which in turn means more generation of heat. The generated heat should be somehow removed from the circuit to prevent burning out of the circuits, and the poor thermal conductivity of the dielectrics surrounding the interconnects block the efficient flow of heat out of the interconnects to the heat sink

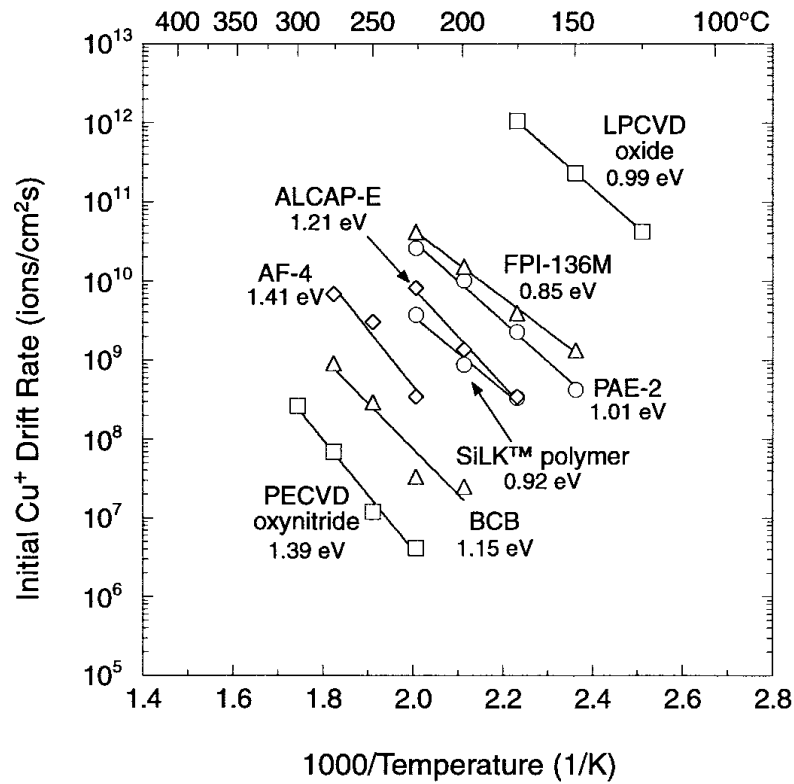


Figure 1.9: Arrhenius plot of initial Cu^+ drift rates in various dielectrics [9].

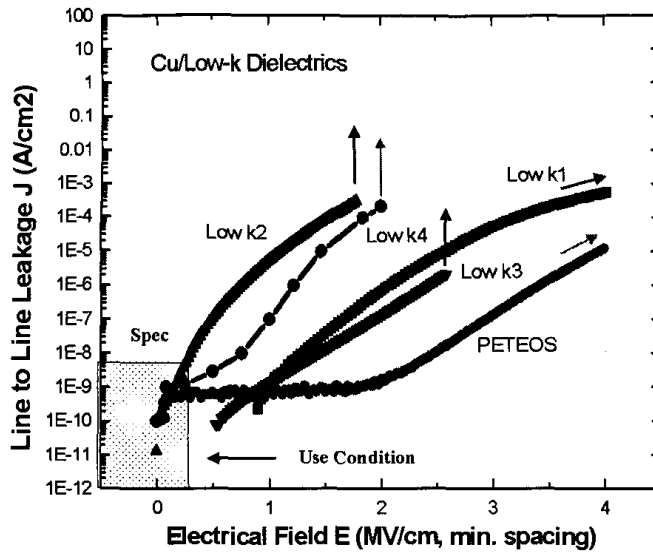


Figure 1.10: Leakage and breakdown characteristics of several low- k dielectrics [5].

connected to the outside atmosphere.

As a result, in a circuit with low- k dielectrics, it is expected that the operating temperature will be higher than in a circuit with conventional oxide dielectrics. High operating temperatures affect circuit performance and reliability. It was reported that an increased DC thermal impedance, by at least 10%, has been found in case of interconnect lines with low- k insulators [16]. From the perspective of reliability, higher temperature means higher probability of circuit failure from electromigration because electromigration lifetime of an interconnect is a strong function of circuit temperature.

Thermal expansion coefficient: Table 1.1 shows the mechanical properties of the materials used in Cu/low- k interconnect structures. The coefficient of thermal expansion (CTE) of low- k materials is shown to be much higher than that of other materials in the same structure. It means that there can be a very big mismatch among the amounts of thermal expansion from several interfacing materials. As a result, the CTE mismatch among the materials can lead to delamination at the interfaces or crack of weaker materials.

Mechanical strength: Back-end dielectrics should have enough mechanical strength to resist the pressure from back-end processes, such as CMP planarization and packaging. Table 1.1 shows the Young's moduli of low- k materials (BCB and SiLK) along with that of copper and other conventional dielectric materials. It is clear that the low- k dielectrics have very poor mechanical strength. This can lead to cracking of the dielectric film during the CMP or packaging.

Recently, the industry is testing the possibility of achieving even lower dielectric constant by using porous materials. On the downside, porous materials will exhibit even poorer mechanical and thermal characteristics, which will directly affect the reliability of the entire circuit negatively. On top of this, the presence of free volumes

Table 1.1: Thermal and mechanical properties of the materials comprising Cu/low- k interconnect structure.

Material	CTE [ppm/°C]	Young's Modulus [GPa]	Poisson Ratio
Si(100)	2.61	131.0	0.278
TiN	7.4	285.0	0.2
SiN	3.2	221.0	0.27
Cu	17.7	117.0	0.343
TEOS	1.0	59.0	0.24
BCB	63.6	2.5	0.34
SiLK	70~90	2.7	-

in the dielectric film was shown to facilitate the conduction process of the charged particles through a series of simulations, and the details will be discussed in Chapter 5.

1.2 *Research Objectives*

The objective of this research is to investigate the impact of physical design characteristics on back-end dielectric reliability. As design and process complexities continue to increase, there is a growing class of reliability problems and reliability marginalities. It is especially true for back-end structures because of the exponentially increasing electric fields among interconnect lines. Therefore, it is strongly desirable to be able to predict reliability or to detect design weaknesses to reliability failure during the pre-silicon verification stage.

In this research, a new method for modeling the reliability of the back-end dielectrics in integrated circuits is demonstrated. Defect clustering is taken into account by using negative binomial statistics. The new model gives a better estimation of integrated circuit reliability based on critical circuit area. Other physical design characteristics are also investigated for their impact on back-end dielectric reliability.

These characteristics include such factors as layout geometry, pattern density, and vias.

1.3 Thesis Overview

This report is organized as follows. Chapter 2 will focus on reliability modeling as a function of the critical circuit area. This chapter will establish the basis for the discussions in the next chapters. In Chapters 3, 4 and 5, the impact of the physical design characteristics on back-end dielectrics and process integration issues will be discussed, respectively. The conclusions and plan for future work will be explained in Chapter 6.

CHAPTER 2

AREA SCALING MODELING OF INTEGRATED CIRCUIT BACK-END DIELECTRIC RELIABILITY

2.1 Review of Dielectric Breakdown Models

2.1.1 Dielectric Breakdown Models

Impact Ionization Model. Early models of electrical breakdown in a metal-covered SiO₂ layer on Si lean heavily on the electronic mechanism of impact ionization, and subsequent electron avalanche, as the vital initiating process [17]. Nevertheless, direct evidence for such a mechanism in materials with band-gaps of 4 to 5eV upward, does not exist. The breakdown field associated with impact ionization and avalanche can be estimated, using simple energy-momentum balance equations, for low-gap semiconductors and for high-gap insulators. Reasonable agreement can be obtained in the former case, but estimated fields in the latter case turn out to be nearly an order of magnitude higher than those observed. This suggests that mechanisms other than avalanche are responsible for breakdown in insulators. Some calculations show that if avalanching is responsible, the breakdown field will be on the order of 10⁸ V/cm. Since typical breakdown fields are in the range of 10⁶ ~ 10⁷ V/cm, this suggests that other mechanisms may be more effective. This model is almost obsolete today. It is introduced here to provide an evolutionary perspective relating to the development of breakdown theories.

Ion-induced Breakdown Model. This early model was originally proposed to overcome what the avalanche breakdown model based on impact ionization in the SiO₂ cannot explain. In reality, avalanche breakdown is not likely to happen in SiO₂ films because the band gap for SiO₂ is too big for avalanche breakdown to take place. This model suggests a mechanism for SiO₂ films, based on Fowler-Nordheim injection from a cathodic protuberance, filamentary Joule heating, and activation of mobile positive ions, such as Na⁺, which enhance the injecting field leading to oxide breakdown [18].

Like other models, the essential element of the breakdown process in this model is F-N injection. The F-N injection is probably initiated at a cathodic protuberance where the local field is enhanced, and the Joule heating associated with the transit of the injected electrons through the oxide film activates mobile positive ions inside SiO₂ film. The heating, plus the observed mobility and activation of positive ions, points to the strong possibility of another basic element, the positive feedback afforded by the activation and drift of positive ions to the cathode where they enhance the local field and induce further injection. This concept of positive feedback due to negative resistance is similar to that used in the *hole trapping model* that will be mentioned later. The overall mechanism is depicted in Fig. 2.1.

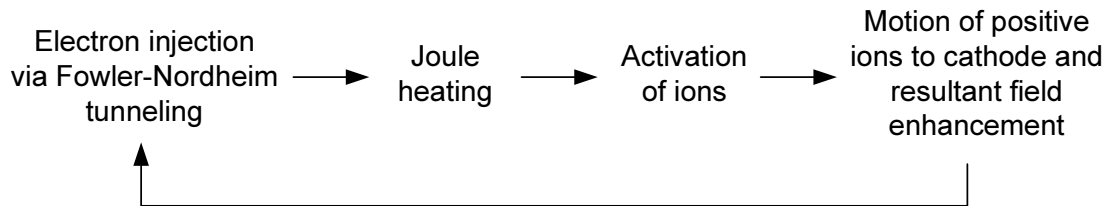


Figure 2.1: Field enhancement feedback mechanism caused by activation and accumulation of mobile ions.

The most common ions which are found as impurities in SiO₂ films are thought to be sodium, Na⁺, and a hydrogen species, H⁺. Probably the parent contaminant in the former case is NaCl, and in the latter case is H₂O. Water contamination makes

it probable that the hydrogen species is more likely to be the hydronium ion, H_3O^+ . The anions Cl^- , H^- , and OH^- appear to be immobile. Both species are highly mobile in the temperature range of 150°C and higher. The activation energy governing the mobility of Na^+ is in the range of $0.7 \sim 1.0\text{eV}$ decreasing with increasing sodium concentration. A mechanism for electrical breakdown in SiO_2 films which involves the motion of positive ions can be conceived along the following lines. This model is also almost obsolete today in explaining breakdown of thin insulator films like SiO_2 . It's because the modern semiconductor processing environment is clean enough to allow the inclusion of very few impurities. But there's some possibility for this model to be applied to thick back end insulator breakdown.

Thermodynamic Model. This oxide breakdown model, which is also called the “E-model”, proposed by many researchers and mathematically shaped by McPherson is basically a theoretical model unlike other physical or empirical models mentioned somewhere else in this report. In this model, time dependent dielectric breakdown characteristics have been analyzed using an Eyring model based on thermodynamic free energy considerations [19]. The model describes well the following features of the data : (1) an apparent activation energy which is a function of the stressing electric field and (2) a field acceleration parameter that is a function of temperature.

The assumption is that the time at which oxide capacitors breakdown may be approximated by a reaction rate constant k , where k is described by the Eyring model:

$$k \propto \exp\left(-\frac{\Delta G^*}{k_B T}\right) \quad (2.1)$$

Here, ΔG^* represents the free energy of activation associated with the breakdown process. Therefore, the mean time to failure (MTTF) can be expressed as follows.

$$MTTF \propto \frac{1}{k} \propto \exp\left(\frac{\Delta G^*}{k_B T}\right) \quad (2.2)$$

At breakdown, the dielectric undergoes an irreversible phase transition in which the material is transformed from an insulating phase to a conductive phase. While the driving force for this breakdown is a free energy difference between the two phases, the rate at which this breakdown reaction occurs is controlled by the free energy of activation associated with the growth of the conductive poly filament. The free energy of activation ΔG^* can be written as,

$$\Delta G^* = \Delta H_0^* + k_B T \sum_m \sum_n C_{mn} \frac{(E_B^n - E_S^n)}{T^m} \mu^{m-n} \quad (2.3)$$

where ΔH_0^* is the change in enthalpy required to activate the poly filament growth at breakdown. By taking only linear terms,

$$\begin{aligned} \Delta G^* &= \Delta H_0^* + k_B T \left[\frac{C_{01}}{\mu} + \frac{C_{11}}{T} \right] S \\ &= \Delta H_0^* + k_B T \left[B + \frac{C}{T} \right] S \end{aligned} \quad (2.4)$$

where B and C are constants and $S = E_B - E_S$, the MTTF becomes

$$MTTF = A \exp\left(\frac{\Delta H_0^*}{k_B T}\right) \exp[\gamma(T)S] \quad (2.5)$$

The *thermodynamic model* is the most widely used to predict device lifetime in industry today. But this model does not give any insight into the physical phenomenon which is actually happening during the breakdown process.

Hole Trapping Model. This physical model, which is usually referred to as the “1/E model”, employs impact ionization as an initiating mechanism for oxide breakdown [20]. In this model, the physical breakdown mechanism is explained with localized field enhancement at the cathode interface due to hole trapping [21, 22] as shown in Fig. 2.2. The source of these holes is believed to be impact ionization in the SiO₂.

Electrons are injected from the cathode into the SiO₂ via Fowler-Nordheim tunneling. Some of these electrons gain sufficient energy to cause impact ionization in the SiO₂. A fraction of the generated holes in the SiO₂ are then driven by the field

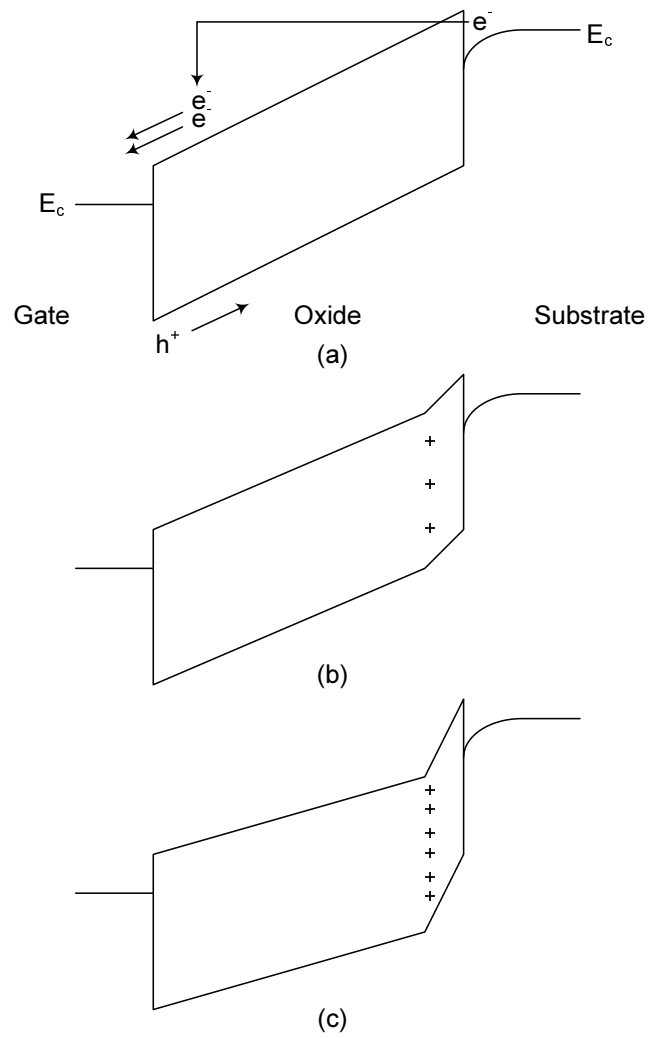


Figure 2.2: Field enhancement caused by hole trapping. Reproduced from [23].

back toward the cathode, where some are trapped. A localized component of trapped holes results in localized field enhancement and conduction, which further accelerates the local hole trapping and eventually results in breakdown and thermal destruction when the localized current density reaches a critical value.

Conceptually, the time-dependent dielectric breakdown process is divided into two stages. During the first, the buildup stage, localized high-field/current-density regions are formed as a result of charge trapping. Eventually, when the local current density or field reaches a critical value, the rapid runaway stage begins during which additional runaway electrical and or thermal processes result in breakdown. The runaway stage, once reached, is completed in a very short period of time. Hence the time necessary to reach the runaway stage determines the lifetime of the oxide. The time necessary to complete the buildup stage can be reduced considerably when defects are present. For example, Na^+ contamination can greatly accelerate the breakdown process. In addition, traps are believed to be generated as a result of the high-field stress. Essentially, in this model the breakdown process is a result of a current instability due to cathode field enhancement resulting from holes generated in the oxide via impact ionization (negative resistance or a positive feedback mechanism) [23, 24].

From other considerations about the charge trapped at the cathode interface, it is concluded that the substrate injection conduction following stressing and annealing is localized in a very small fraction of the oxide area. Because of the strong dependence of J on E_c , this localized component dominates over the current flowing in the remainder of the oxide area where the field enhancement is much smaller [25, 26]. So the oxide area is divided into two types of oxide areas, the weak area and the robust area [27, 28]. The localized weak area is very small in size and highly susceptible to hole trapping near the cathode. The area ratio of weak area to robust area is on the order of 10^{-6} . The breakdown process is dominated by the weak area characteristics.

The lifetime is expressed as follows

$$t_{BD} = A \exp\left(\frac{B}{E}\right) \quad (2.6)$$

where A and B are constants.

Based on this model, oxide wearout performance might be improved by process changes that reduce interface hole trapping, such as radiation-hard processing, in addition to the reduction of particulate contamination and crystal defects [29, 30, 31]. The $1/E$ model is a kind of *modified impact ionization model* because it employs impact ionization as a initiating process for the onset of breakdown. This model gives some insight into the actual oxide breakdown process due to its empirical nature and inclusion of some assumptions about the breakdown process.

Percolation model. It is well known that broken and strained bonds are manifest electronically as traps. Therefore, generation of such traps is the generation of physical-damage sites in the oxide [32]. Electrons can accelerate to energies high enough to break bonds, and this damage is heavier at the anode interface [33] as shown in Fig. 2.3. The concept of the physical damage model is that the oxide suffers dielectric breakdown when physical damage due to broken bonds forms a defect-filled filamentary path in the oxide that conducts excessive current [33, 34, 35].

The trap generation rate is found to be proportional to the flux of the injected charge and to increase exponentially with the oxide electric field [36, 37]. At high oxide field only a small fraction of the newly generated traps are occupied; consequently, the measured oxide charge buildup does not reflect the actual increase in the density of generated traps. The density of the generated traps reaches high values on the order of 10^{20} cm⁻³. It is claimed that these high values of oxide traps may be the cause of SiO₂ “wear out” type breakdown, through the formation of new paths of conductance by electron tunneling between closely spaced generated traps.

Trap generation occurs at the interfaces as well as in the bulk, but interfacial

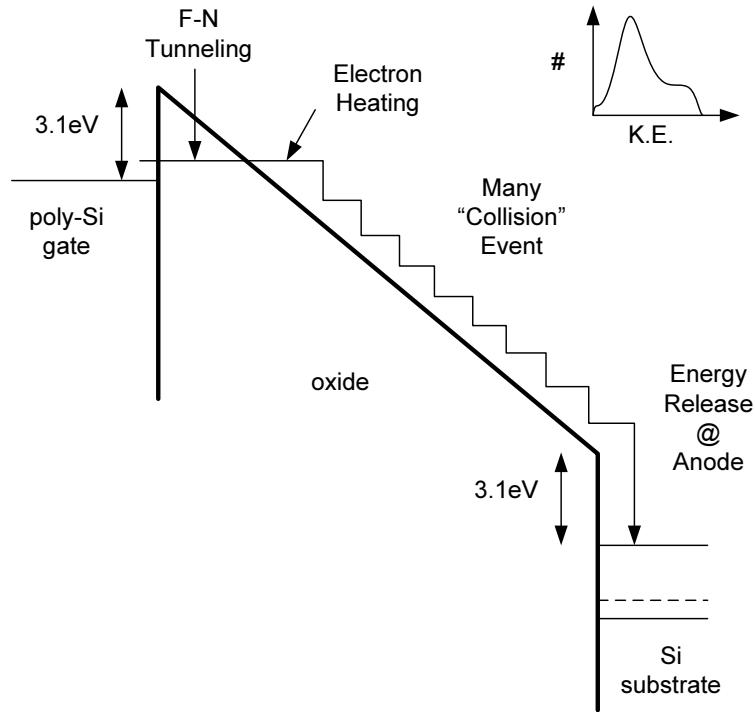


Figure 2.3: Electronic transport in the oxide conduction band. Reproduced from [32].

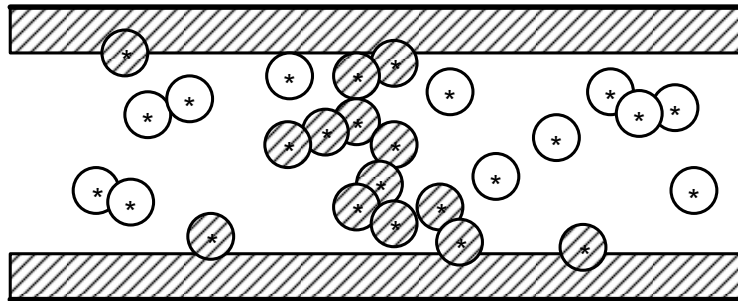


Figure 2.4: Schematic illustration of the spheres model for intrinsic oxide breakdown simulation based on trap generation and conduction via traps. A breakdown path is indicated by the shaded spheres. Reproduced from [33].

trap generation at the collecting interface (anode) is particularly severe due to the large amount of energy imparted by the electrons to weak interfacial bonds. At breakdown, the heavier damage at the anode links up with islands of bulk damage to create a filamentary path that enables excessive conduction. The physical-damage model proposes that it is the filamentary path that loses its dielectric properties, since this path is highly disordered and defect-filled, and thus, structurally different from the bulk of the oxide. Such paths have been observed visually in other dielectrics, such as polymethylmethacrylate (PMMA), but the precise nature of these paths in SiO₂ is not clear from this model. Charge to breakdown (Q_{bd}) is proportional to the inverse of the net trap-generation rate, and this behavior is independent of the polarity of the generated traps. The relationship can be mathematically stated as

$$Q_{bd} = 0.382 \times \left(\frac{dV_s}{dQ_{inj}} \right)^{-0.89} \quad (2.7)$$

Some researchers reportedly claim that it is proven that the critical density of neutral electron traps corresponds to a critical hole fluence, since a unique relationship between electron trap generation and hole fluence is found to be independent of stress field and oxide thickness. They claim that the holes are necessary for trap generation.

As the thickness of the gate oxides gets thinner, the *percolation model* draws more attention from researchers these days. According to this model, nitrided oxide (oxinitride) can be a solution for the oxide breakdown problem because the incorporation of nitrogen strengthens the weaker bonds in the dielectric, since nitrogen atoms segregate preferentially to the interface. It seems most of the recent publications about ultrathin oxide breakdown are centered around this model.

2.1.2 Applicability to Back-end Dielectrics

In the models overviewed above, some early models are not applicable to today's ultra thin and high quality gate oxides but can give some insight into the breakdown mechanism of back-end dielectrics.

The *impact ionization model*, the *1/E model* and the *physical damage model* seem unlikely to be applicable to the thick back-end interlayer dielectric case because (1) impact ionization is not a probable process to take place in thick dielectrics because the electric field in the thick dielectrics is too low, (2) the time to build a link between adjacent traps inside the thick oxide to bridge between two neighboring metal lines is much longer unless we assume a very high level of inherent physical imperfections inside the dielectrics such as impurities, trap sites, and geometrical irregularities. The most probable theories to predict the lifetime of thick back-end dielectrics are the *thermodynamic model* based on the free energy difference driven phase transition and the *impurity ion-induced breakdown model*.

Besides, when we apply the breakdown models introduced above to the back-end dielectric case, we have to be aware of the differences between front-end gate oxide and back-end dielectrics.

First, unlike the front-end gate oxide, the back-end dielectric layer undergoes complex process steps, such as chemical mechanical polishing (CMP) and photoresist strip/ashing. These process steps can leave micro and macro damage at the surface such that they can be used as trap sites in the trap-assisted conduction process.

Second, the electric field in the back-end dielectric film is not uniform as in the front-end gate oxide case. It can be easily understood recalling the fact that the interconnects are used to connect the components scattered across a chip and various geometrical shapes are used to minimize the total path length or to achieve efficient routing. In some geometrical shapes, the electric field lines converge and this sometimes causes highly enhanced electric field at that point. This enhanced electric field can accelerate the breakdown process of the dielectric because the conduction or drift of charged particles is driven by the electric field in the dielectric film. This also means that, when dealing with the back-end dielectric breakdown, the various geometrical components in the interconnect layouts should be properly taken into account.

Third, the complexity of back-end dielectric stack should be considered. Unlike the simple planar stack structure of front-end gate oxide, the back-end dielectric stack consists of many dissimilar materials such as silicon nitride, the dielectric itself, the etch stop layer and so on. This complex vertical structure makes the electric field distribution non-uniform and can make the modeling of the breakdown process more difficult than in the gate oxide case.

Fourth, the hybrid nature of the dielectric breakdown mechanism is suspected to exist. Because the back-end dielectric film is usually deposited using chemical vapor deposition (CVD), the quality of the film is usually much poorer than the gate oxide which is thermally grown and, as a result, the dielectric film contains many different kinds of defects. This makes us consider the impurity ion-induced breakdown as a primary breakdown mechanism. However as the device scaling gets into the nanoscale regime, we also have to take into account the other breakdown mechanisms that were originally conceived for the thin gate oxide case. Therefore we have to first be able to tell if the breakdown is driven by a hybrid mechanism.

2.2 Mathematical Modeling

2.2.1 Previous Work

Based on the assumption that failure occurs at a uniformly random position on a circuit, yield-area and reliability-area relationships have been modeled using Poisson statistics. However, many researchers have reported the clustering of failure-causing defects [38, 39, 40]. Defect clustering results in a correlation between the numbers of defects that occur on integrated circuit chips located adjacent to one another [40]. Defect clustering, in turn, implies a deviation from a uniform random distribution of defects resulting in a population made up of several subgroups mixed at random in various proportions, which makes the fundamental assumption for the Poisson statistics not applicable. Figure 2.5 depicts these distributions.

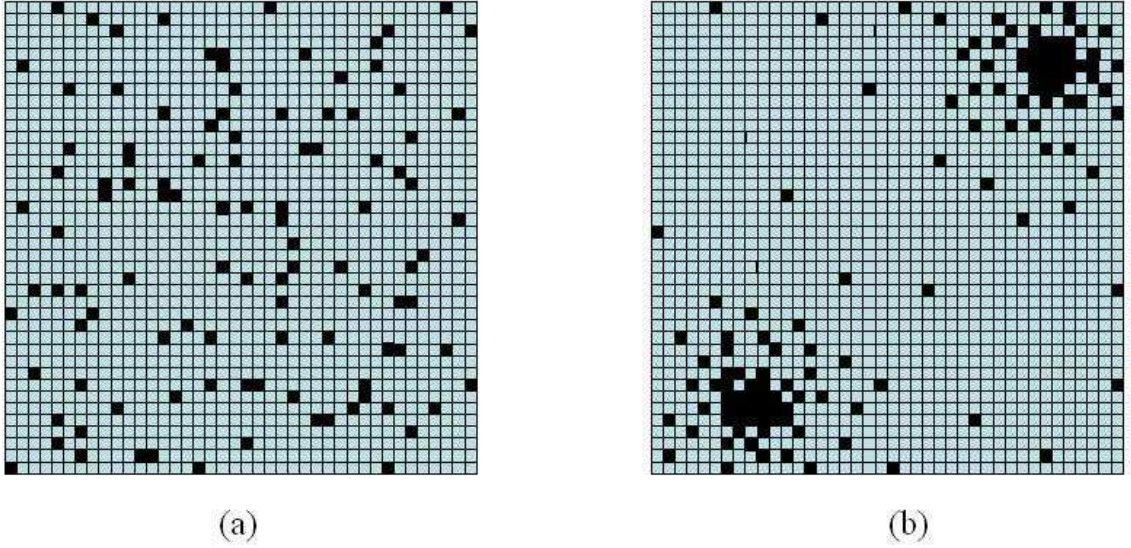


Figure 2.5: The difference of the two models relating to the assumption about the defect distribution. In the Poisson model(a), the defects are assumed to distribute randomly and uniformly across the circuit area, while in Negative Binomial model(b), it is assumed that the defects are clustering locally.

Greenwood-Yule, and Polya-Eggenberger independently discovered what is generally known as a contagious distribution or compound Poisson distribution. The origin of the contagion can be either an inhomogeneity of the population or the fact that each event affects the probability of future events [41]. In its early days, the compound Poisson distribution found applications mostly in entomology, bacteriology, accident statistics, and risk theory when a population is composed of several subpopulations with distinct parameters that cannot be described by a single Poisson distribution. It can provide the simplest description of the mechanism behind many observed distributions in the areas stated above and integrated circuit yield as well, especially when the data exhibit more variability than can be attributed by a simple Poisson distribution. The compound Poisson distribution can be used to describe the probability of getting x fatal defects on an integrated circuit with area A as shown below [41]:

$$Prob(X = x) = \int_0^\infty \frac{e^{-AD}(AD)^x}{x!} f(D)dD \quad (2.8)$$

where D is the defect density and $f(D)$ is a mixing function. It was shown that a gamma distribution can be used as the mixing function in Eq. (2.8) to model the defect densities on an integrated circuit by Stapper [42] and it can be expressed as

$$f(D) = \frac{1}{\Gamma(\alpha)\lambda^\alpha} D^{\alpha-1} e^{-D/\lambda} \quad (2.9)$$

where α and λ are the shape parameter and the inverse of scale parameter for the gamma distribution, respectively. Equation (2.8) can be re-written as follows by introducing Eq. (2.9) [43].

$$Prob(X = x) = \frac{\Gamma(x + \alpha)}{x! \Gamma(\alpha)} \frac{(A\lambda)^x}{(A\lambda + 1)^{x+\alpha}} \quad (2.10)$$

Equation (2.10) is called the negative binomial distribution. Like the Poisson, the negative binomial distribution can be used in modeling count data, but the negative binomial distribution is more general than the Poisson distribution. This is because the negative binomial has a variance that is greater than its mean, often making it a better fit for data that do not satisfy the assumptions of the Poisson distribution.

The shape parameter of a gamma distribution, α , is usually called the clustering parameter when appearing in yield or reliability models because it represents the degree of defect clustering in a physical sense. Figure 2.6 demonstrates the effect of variation on the shape of distribution. From the figure, it is clear that the skewness of the distribution increases as α decreases. In the opposite extreme, as α increases to infinity, the negative binomial distribution asymptotically approaches the Poisson distribution.

By means of negative binomial statistics, Stapper successfully introduced defect clustering into yield formula and suggested the negative binomial yield model [43]. Figure 2.7 shows the negative binomial yield model with several variations in degree of defect clustering in comparison to the Poisson yield model. The negative binomial yield model has been successful in explaining actual yield data [43, 44, 45]. If reliability is viewed as time dependent yield, the same principle regarding a defect

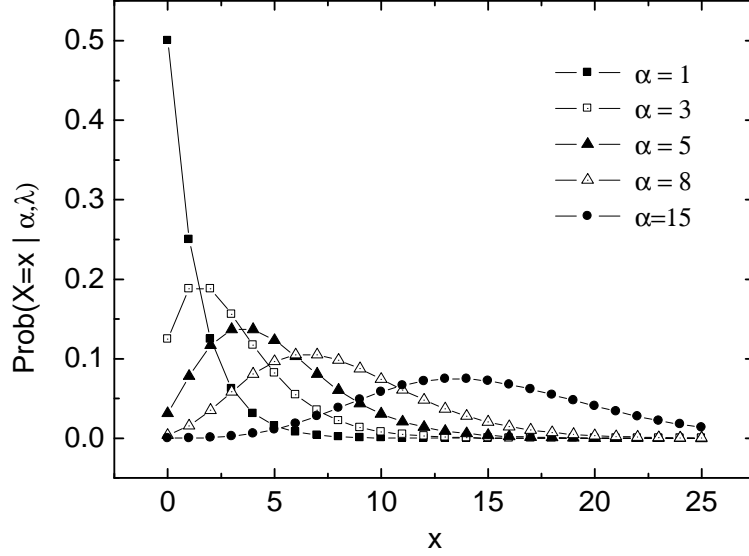


Figure 2.6: Effect of variation of the parameter α on the shape of the negative binomial distribution. As α gets closer to 1, it approaches the geometric distribution, while as α increases to infinity, it approaches the Poisson distribution.

distribution should hold for a reliability model as well. It is demonstrated that this non-uniform randomness of a defect distribution can be effectively incorporated into reliability-area modeling to get a more accurate area scaling factor.

Two distinct reliability models for the area scaling effect are derived from two yield models introduced in § 2.2.1 with different assumptions about the defect distribution. One is derived from the Poisson yield model assuming a uniform random distribution of defects, and the other is based on the negative binomial yield model to account for deviation from a uniform random distribution of defects caused by clustering, as stated above. A uniform random distribution is described by a single Poisson distribution, while non-uniformness needs mixing or compounding multiple distinct Poisson distributions. In deriving the models, the time-to-failure is assumed to have a Weibull distribution with shape parameter β , and scale parameter η . β is assumed to be independent of the circuit area as usual. Figure 2.8 demonstrates the overall mathematical process flow for derivation of the reliability models.

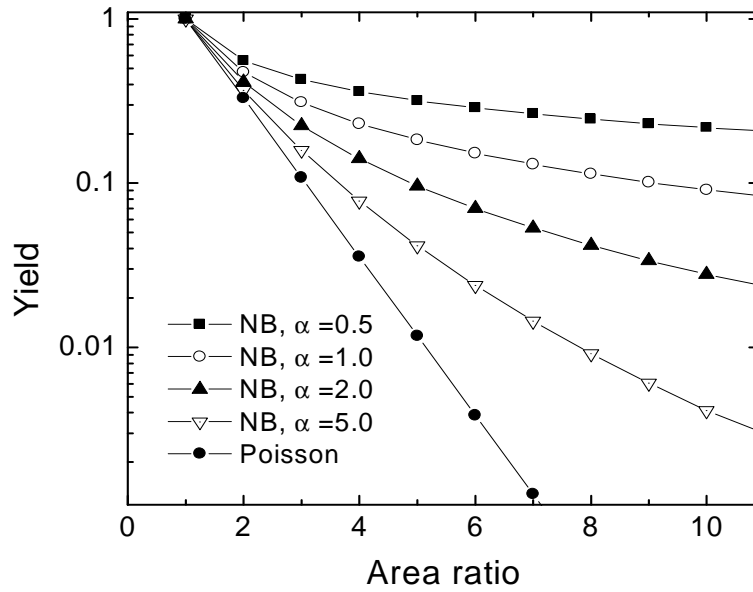


Figure 2.7: Comparison of the yield models based on different assumptions about defect distribution. NB denotes negative binomial model.

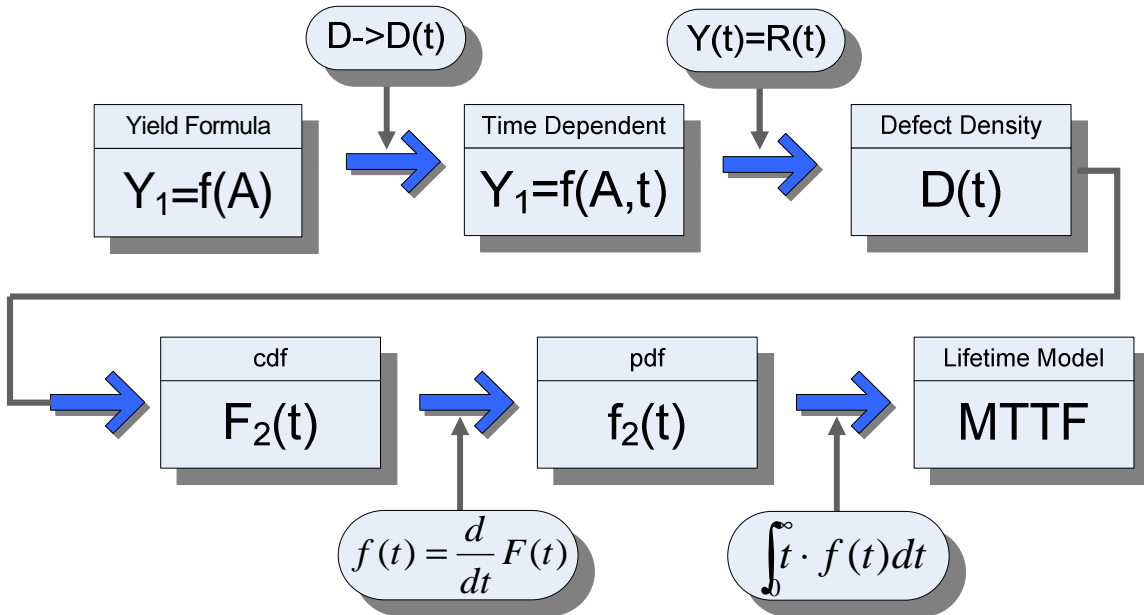


Figure 2.8: Mathematical flow for derivation of the reliability models.

2.2.2 Poisson model

In the Poisson yield model, yield is expressed in terms of critical circuit area A and defect density D as follows.

$$Y = e^{-AD} \quad (2.11)$$

This relation can be transformed to a time dependent form by setting $D = D(t)$ with the condition $D(t = 0) = 0$. Now D is the density of the defects causing reliability failure rather than the density of the defects causing immediate yield loss at $t = 0$. Accordingly, for a chip with area A_1 , the survival function can be equated with the yield formula in Eq. (2.11) as shown below:

$$\exp \left[- \left(\frac{t}{\eta_1} \right)^\beta \right] = \exp(-A_1 D) \quad (2.12)$$

Solving for $D(t)$ gives

$$D(t) = \left(\frac{t}{\eta_1} \right)^\beta \frac{1}{A_1} \quad (2.13)$$

Using Eq. (2.13), for a chip with a different area A_2 , the yield, or the probability of chips that have not failed is given by

$$Y_2 = e^{-A_2 D(t)} \quad (2.14)$$

Therefore, the cumulative distribution function of the probability of failure, $F_2(t) = 1 - Y_2(t)$, can be written as

$$F_2(t) = 1 - \exp \left[- \left(\frac{t}{\eta_1} \right)^\beta \frac{A_2}{A_1} \right] \quad (2.15)$$

Then, the probability density function $f(t)$ for the same chip is obtained by differentiating the cumulative distribution function $F_2(t)$,

$$\begin{aligned} f_2(t) &= \frac{d}{dt} F(t) \\ &= \frac{\beta}{\eta_1} \left(\frac{t}{\eta_1} \right)^{\beta-1} \frac{A_2}{A_1} \exp \left[- \left(\frac{t}{\eta_1} \right)^\beta \frac{A_2}{A_1} \right] \end{aligned} \quad (2.16)$$

The mean lifetime ($MTTF$) of the chip with area A_2 can now be calculated as follows

$$\begin{aligned}
MTTF_2 &= \int_0^\infty t f(t) dt \\
&= \int_0^\infty t \frac{\beta}{\eta_1} \left(\frac{t}{\eta_1}\right)^{\beta-1} \frac{A_2}{A_1} \exp\left[-\left(\frac{t}{\eta_1}\right)^\beta \frac{A_2}{A_1}\right] dt \quad (2.17)
\end{aligned}$$

Integrating Eq. (2.17) by substitution using $u = \left(\frac{t}{\eta_1}\right)^\beta \frac{A_2}{A_1}$ gives

$$\begin{aligned}
MTTF_2 &= \int_0^\infty \eta_1 \left(\frac{A_1}{A_2}\right)^{1/\beta} u^{1/\beta} \exp(-u) dt \\
&= \eta_1 \left(\frac{A_1}{A_2}\right)^{1/\beta} \Gamma\left(1 + \frac{1}{\beta}\right) \\
&= \left(\frac{A_1}{A_2}\right)^{1/\beta} MTTF_1 \quad (2.18)
\end{aligned}$$

Interestingly, the area scaling factor shown in Eq. (2.18) derived from the Poisson yield model ends up being of the same form as the one introduced earlier based on simplistic binomial statistics [46]. This is because the Poisson distribution is a generalization of the binomial distribution under the assumption that the population is infinitely large.

2.2.3 Negative Binomial Model

To incorporate the non-uniformity of the defect distribution caused by clustering, the modeling starts with the negative binomial yield model for a chip with area A_1 , defect density D , and the clustering parameter α [42]. The yield can be obtained by setting $x = 0$ in Eq. (2.10) and substituting for λ using the $\lambda = \frac{D}{\alpha}$ relationship. Yield is expressed as follows.

$$Y_1 = \left(1 + \frac{A_1 D}{\alpha}\right)^{-\alpha} \quad (2.19)$$

The survival function for this chip can be equated with Eq. (2.19) as shown below:

$$\exp\left[-\left(\frac{t}{\eta_1}\right)^\beta\right] = \left(1 + \frac{A_1 D(t)}{\alpha}\right) \quad (2.20)$$

Solving for $D(t)$ gives

$$D(t) = \frac{\alpha}{A_1} \left\{ \exp \left[\left(\frac{t}{\eta_1} \right)^\beta \frac{1}{\alpha} \right] - 1 \right\} \quad (2.21)$$

For a chip with a different area A_2 , the cumulative distribution function $F_2(t)$ can be written as

$$F_2(t) = 1 - \left(1 + \frac{A_2 D(t)}{\alpha} \right)^{-\alpha} \quad (2.22)$$

Then, the probability density function $f(t)$ for the same chip is

$$\begin{aligned} f_2(t) &= \frac{d}{dt} F(t) \\ &= \left(1 + \frac{A_2 D(t)}{\alpha} \right)^{-\alpha-1} \left(A_2 \frac{dD(t)}{dt} - \frac{A_2 d\alpha}{\alpha dt} \right) \end{aligned} \quad (2.23)$$

Assuming α is constant over time and using Equation 2.21, the mean lifetime of the chip with area A_2 can now be written as follows. This constant α assumption will be further discussed later.

$$\begin{aligned} MTTF_2 &= \int_0^\infty t f(t) dt \\ &= \int_0^\infty t \left(1 + \frac{A_2 D(t)}{\alpha} \right)^{-\alpha-1} A_2 \frac{dD(t)}{dt} dt \\ &= \int_0^\infty t \left\{ 1 + \frac{A_2}{A_1} \left[\exp \left[\left(\frac{t}{\eta_1} \right)^\beta \frac{1}{\alpha} \right] - 1 \right] \right\}^{-\alpha-1} \\ &\quad \frac{A_2}{A_1} \frac{1}{\eta_1^\beta} \beta t^{\beta-1} \exp \left[\left(\frac{t}{\eta_1} \right)^\beta \frac{1}{\alpha} \right] dt \end{aligned} \quad (2.24)$$

To get a relationship between the mean lifetimes of the chips with different areas, A_1 and A_2 , integration is performed on Eq. (2.24) by substitution using the following expression

$$u = \frac{A_2}{A_1} \left\{ \exp \left[\left(\frac{t}{\eta_1} \right)^\beta \frac{1}{\alpha} \right] - 1 \right\} \quad (2.25)$$

which results in

$$MTTF_2 = \alpha^{1+\frac{1}{\beta}} \cdot \eta_1 \int_0^\infty \frac{\left[\ln \left(\frac{A_1}{A_2} u + 1 \right) \right]^{\frac{1}{\beta}}}{(u+1)^{\alpha+1}} du \quad (2.26)$$

Using the following formula for $MTTF$,

$$MTTF = \eta \Gamma \left(1 + \frac{1}{\beta} \right) \quad (2.27)$$

the area scaling factor is expressed as the following:

$$\frac{MTTF_2}{MTTF_1} = \frac{\alpha^{1+\frac{1}{\beta}}}{\Gamma(1 + \frac{1}{\beta})} \int_0^\infty \frac{\left[\ln \left(\frac{A_1}{A_2} u + 1 \right) \right]^{\frac{1}{\beta}}}{(u + 1)^{\alpha+1}} du \quad (2.28)$$

Equation (2.28) is not in a closed form but can be evaluated using numerical methods. The area scaling factor in Eq. (2.28) is evaluated using the adaptive Simpson method, and the result is summarized in the next section in comparison with the result from Eq. (2.18).

2.3 Numerical Evaluation of the Models

Figure (2.9) demonstrates the numerical results obtained from the two models for the reliability-area relation derived above. Recapitulating, the Poisson model is based on the assumption of uniform random distribution of defects shown in Eq. (2.18), which is the same as the early model introduced in [46], and the negative binomial model assumes defect clustering to account for the effect of deviation from a uniform random distribution. As can be seen in the figure, departure from the Poisson model increases as the clustering parameter α decreases. A smaller clustering parameter means a higher degree of defect clustering. This trend makes a good analogy to the one shown in the yield-area relation displayed in Fig. 2.7.

In general, the reliability projection by the negative binomial model with some degree of clustering gives a more optimistic result than the one by the Poisson. In Fig. 2.10, the result is displayed as a function of the clustering parameter clearly showing the effect of the parameter on reliability projection. In Fig. 2.11, it is shown that the effect of decreasing β is exaggerated in the Poisson model as opposed to the negative binomial model.

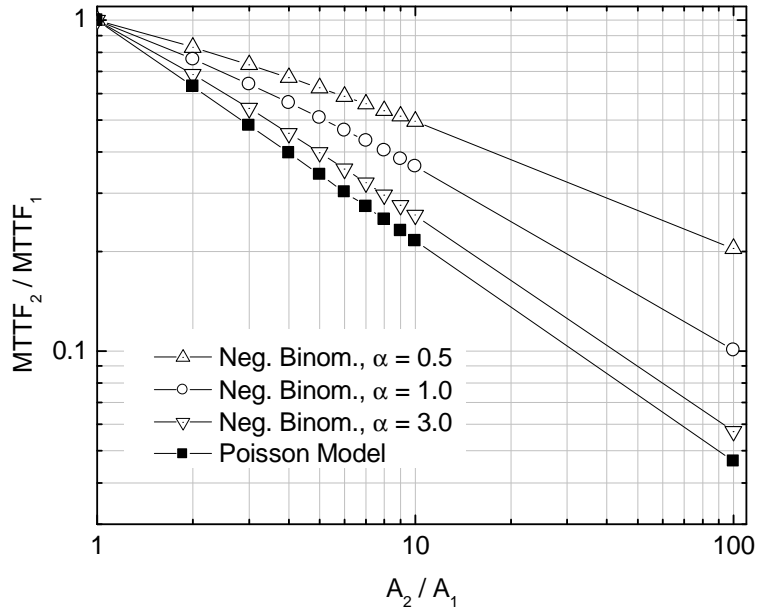


Figure 2.9: Numerical evaluation result of the reliability models; the negative binomial model and the Poisson model. The negative binomial model is shown with variations in α .

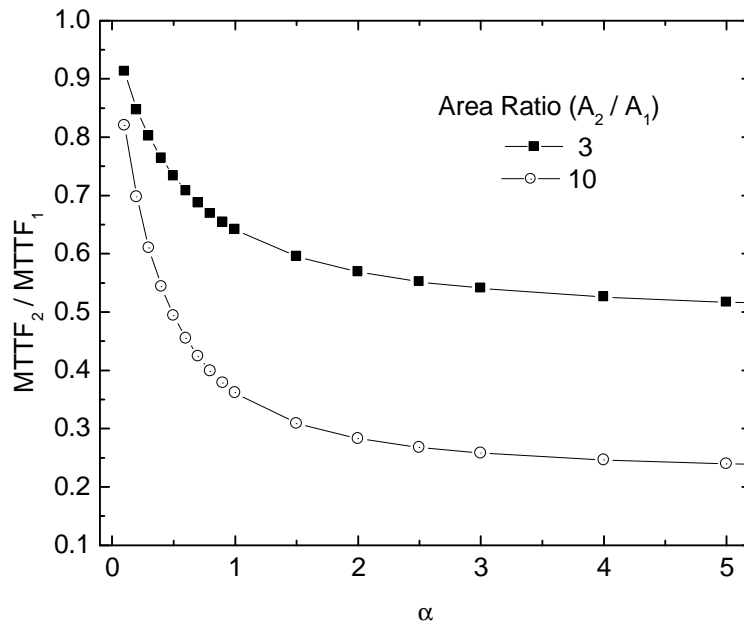


Figure 2.10: Mean time to failure ratio change as a function of the clustering parameter α . Smaller α means a more localized defect distribution, i.e. a higher degree of defect clustering, leading to a better reliability.

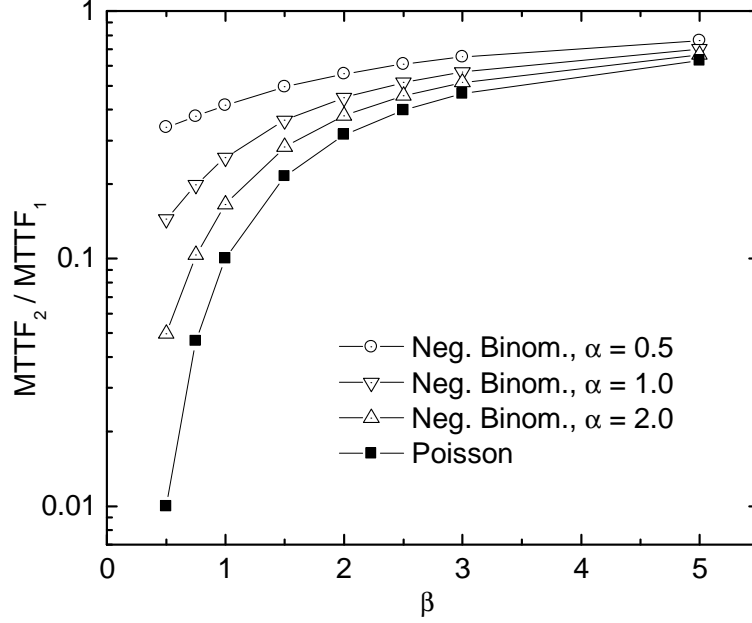


Figure 2.11: Effect of variation of the Weibull shape parameter β variation on reliability. β is shown to have a greater impact on reliability with a larger α for which the extreme case is the Poisson model.

2.4 Experimental Verification of Models

2.4.1 Experimental Approach

2.4.1.1 General Test Procedure for Back-end Dielectric Reliability Evaluation

Usually, the comb or comb-serpentine structure is used to evaluate the reliability of back-end dielectrics. Test structures are subjected to bias-temperature stress (BTS) tests for accelerated testing. The purpose of the accelerated life testing (ALT) is to reduce the amount of test time which could be tens of years if the test is performed under a normal operating condition, which is not practical considering the limited time for qualification of a new process or product.

It is usually known that the harsher the test condition is, the shorter the test time is. However, when deciding the test conditions for ALT, care must be taken not to use excessively harsh condition that can induce an abnormal failure mode. For example, at temperatures above 250°C, copper lines can have a large amount of thermally induced compressive stress that can exaggerate failures by extrusion [10].

When the extrusion failure predominates, the dielectric reliability data can become noisy or even overwhelmed by the abnormal extrusion failures. Therefore the test conditions for electrical or thermal accelerations should be chosen to be reasonably short considering the time allowed for evaluation and to be physically acceptable in terms of failure physics.

2.4.1.2 Experimental Configuration

The test structure used for the inter-metal dielectric (IMD) reliability study was an interdigitated comb structures, as is shown in Fig. 2.12. The structure was fabricated using a standard Cu/low- k damascene process. The typical length of a finger is approximately 100 μm , with a metal-to-metal spacing of 0.18 μm . As shown in Fig. 2.12, the test patterns have several variations in areas so that they can be used for the verification of the reliability-area relationship. The test patterns with larger areas were implemented by connecting the unit ($1\times$) pattern in parallel. By doing this, any size of test pattern can be implemented easily.

All measurements were performed at the wafer-level with hot chuck control: TDDB measurements were conducted at 150°C. The breakdown condition was typically defined as a leakage current level at 1 ~ 100 μA . Due to the relatively high voltages applied (usually > 50V), a hard breakdown with the current reaching the compliance limit was generally observed. Weibull statistics were employed in analyzing the TDDB lifetime distributions. Figure 2.13 is the schematic description of the test setup, and Fig. 2.14 shows an actual equipment configuration.

2.4.2 Experimental Result

The test patterns were biased at constant voltage until they fail. Figure 2.15 shows the typical current vs. time (I-t) plot for several test structures with different areas. It is clear that the larger circuits exhibit shorter lifetimes than the smaller ones.

The result is demonstrated in Fig. 2.16. The actual data shows a significant

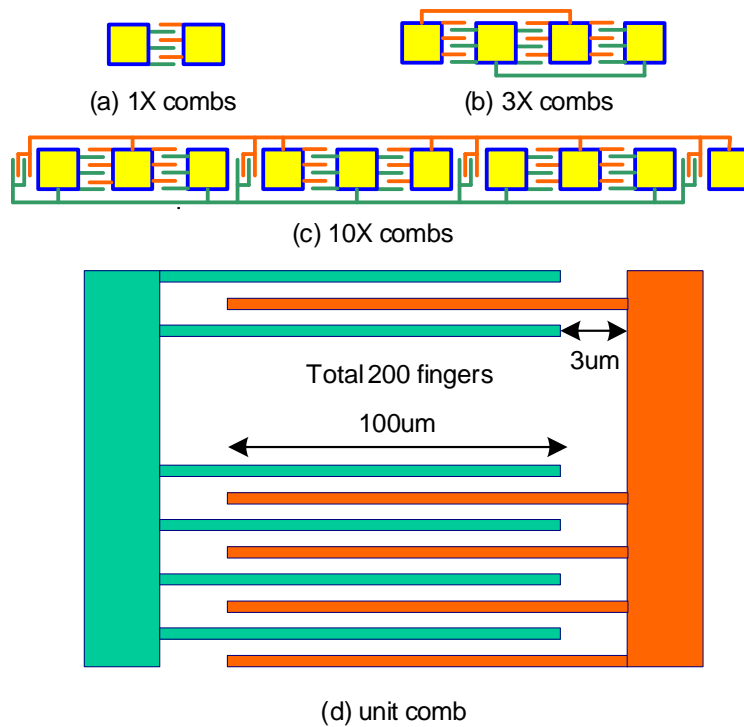


Figure 2.12: Configuration and specification of the reliability test structures used in this research; (a) $1 \times$ unit area, (b) $3 \times$ area, and (c) $10 \times$ area combs. (d) is an enlarged view for a unit area comb structure. The line width is $0.16 \mu\text{m}$ and space between lines is $0.18 \mu\text{m}$.

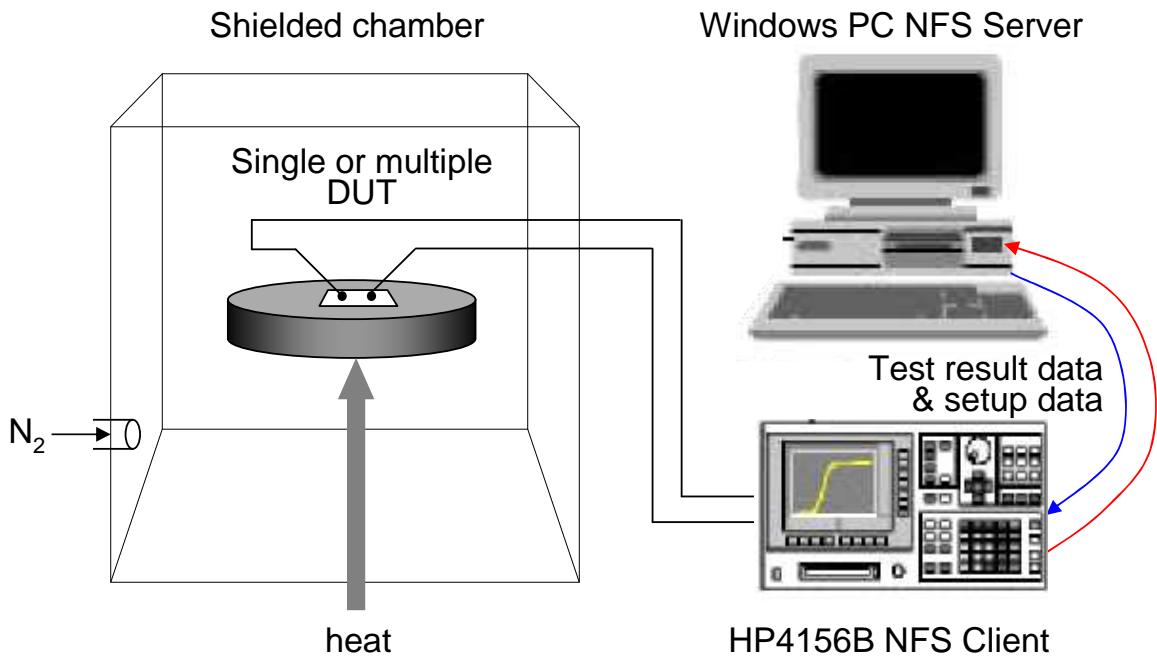
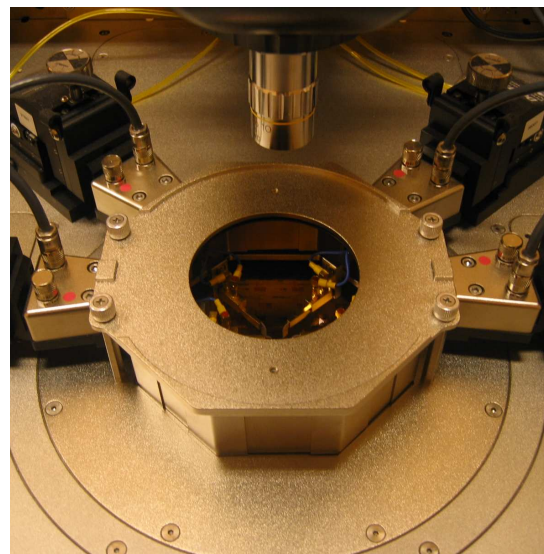


Figure 2.13: Schematic description of the test setup. The Agilent 4156 was used in conjunction with moisture- and noise-protected probe station to keep any external noise factors from affecting the DUT's lifetime.



(a)



(b)

Figure 2.14: Photographs of equipment used for BTS testing. It includes shielded chamber, thermal chuck, low noise probes, microscope, vibration isolation table (shown), temperature controller, and semiconductor parametric analyzer (not shown).

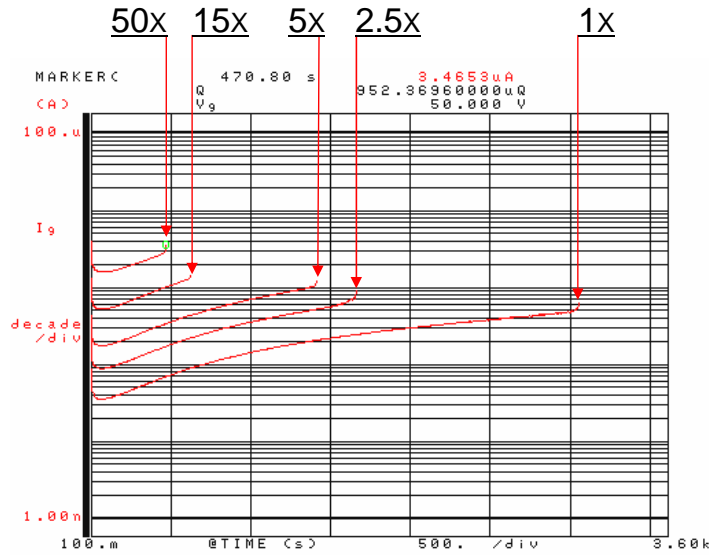


Figure 2.15: Screen shot of Agilent 4156 semiconductor parametric analyzer showing a typical current vs. time (I-t) plot for several test structures with different areas.

departure from the Poisson model but falls well within the narrow range projected by the negative binomial model with clustering parameter $\alpha = 1.0 \sim 2.2$, the shaded region in the figure. From Fig. 2.16, it is expected that the departure of the actual trend from the Poisson model will be even greater with a larger critical circuit area, and this can be accounted for with the negative binomial model. It is suspected, however, in Figure 2.16, that there is a curvature in the relationship between reliability and critical area, which cannot be explained even with the negative binomial model. If this is true, an even more optimistic reliability projection is possible.

The result from the negative binomial model was shown to provide a good explanation to the trend observed in experimental data. Although the new model was applied to back-end test structures in this research, it also should be possible to account for the reliability-area relation of other parts of a circuit, such as for the gate oxide.

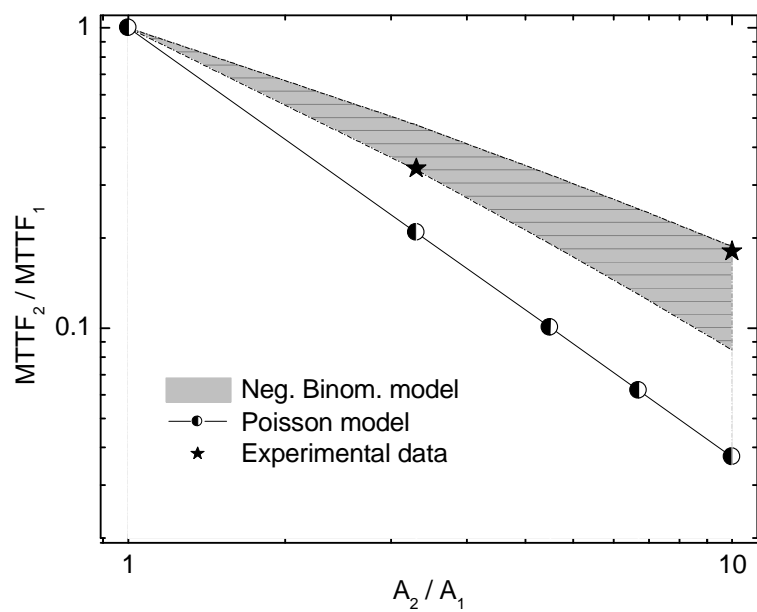


Figure 2.16: Experimental data juxtaposed with model data. Experimental data points fall in a range, shaded region, composed of two trend lines from negative binomial models with $\alpha = 1.0$ (upper) and $\alpha = 2.2$ (lower).

CHAPTER 3

BACK-END LAYOUT CHARACTERIZATION FOR RELIABILITY EVALUATION

3.1 Need for Layout Considerations

3.1.1 General Configuration to Examine Front-end Oxide Reliability

One of the simplest configurations to examine the integrity of a dielectric layer is a parallel plate capacitor configuration which is usually employed in front-end gate oxide reliability evaluations. In this configuration, a positive voltage is applied to one plate and the other plate is connected to the ground. As time increases, the dielectric integrity of the thermal oxide is degraded and a failure occurs through an abrupt increase in leakage current between the two plates of the MOS capacitor.

However this parallel plate capacitor test structure fails to examine some crucial aspect unique to the back-end dielectric structures. The uniqueness of the back-end dielectric test structures are summarized in the following section.

3.1.2 Uniqueness in Back-end Reliability Evaluation

The electric field between adjacent conductors is dependent on the shape/geometry of the conductors involved [5, 47]. In this regards, the electric field between interconnects in back-end of line (BEOL) also should be layout-dependent. Therefore the geometry-dependent characteristics of back-end dielectric reliability test have to be considered in the evaluation process.

Reliability for integrated line structures is more complicated than for a parallel plate capacitor case due to the presence of more interfaces [10]. Unlike the front-end gate oxide MOS structure, the back-end structure include many interfaces between

interconnect metal and inter-metal dielectric, metal and capping layer, inter-metal dielectric and capping layer, and etch stop layer (ESL) and inter-metal dielectric. The multitude of interfaces makes failure most likely to happen in mixed modes and makes the analysis more challenging.

Due to the greater complexity of this structure, failure times can be even more varied than in the parallel plate capacitor case. An additional complication of this structure is that the failure mode may not be as well defined as in the case of a parallel plate capacitor [10].

The purpose of this part of the research is to characterize the electric field between interconnects of various geometries extracted from full chip layouts of certain standard circuits using the finite element method (FEM) in order to identify potential vulnerabilities to reliability problems in designs.

This part is organized as follows. The next section summarizes the methodology. Simulation results are presented in § 3.3, including the impact of layout and vertical architecture on the electric field. This section also includes improved test structure designs to aid in characterization and modeling of breakdown.

3.2 Layout Analysis

Representative layout patterns were extracted from International Symposium on Circuits and Systems (ISCAS) benchmark circuits 3540, 6288, and 7552. These patterns are shown in Fig. 3.1. Model A, in Fig 3.1, which consists of two parallel interconnects, is the control pattern. In selecting these patterns, the frequency of appearance in full chip circuit layouts was taken into account, considering the shape/geometry as the primary factor. These pattern models are processed using a photolithography process simulator to generate more realistic aerial images that can be found on actual chips.

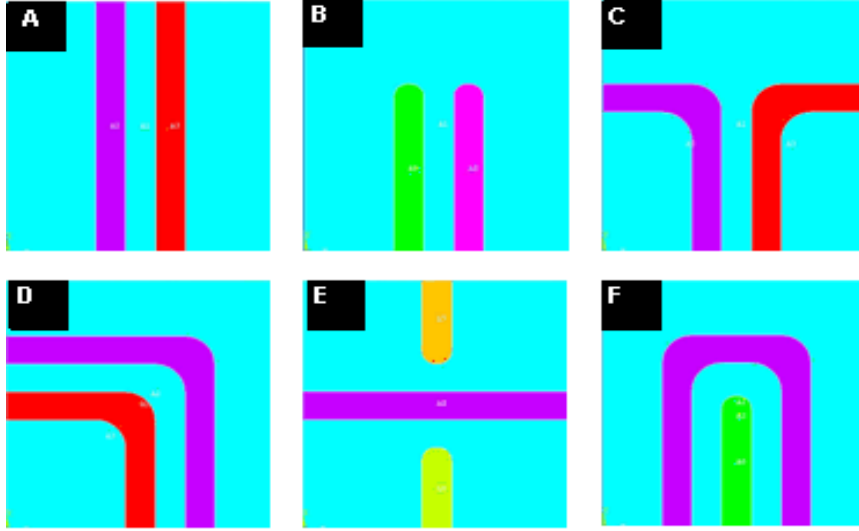


Figure 3.1: Model layout geometries used for electric field simulation in this research. This figure shows the lithographically simulated patterns reflecting the optical proximity effect.

Solid models for finite element analysis with different metal width/space combinations are created for each model: from $0.2\mu\text{m}$ to $0.5\mu\text{m}$ with $0.1\mu\text{m}$ increments, to see the change in electric field according to device scaling. Finally, the electric field distribution is analyzed using two and three dimensional field solvers based on finite element analysis to see the impact of layout geometries on electric field. Maximum field locations are identified as the most probable leakage paths between adjacent interconnects. Constant voltage stress tests are performed on actual comb test patterns to observe the locations of physical breakdown. Figure 3.2 illustrates the simulation flow for electric field characterization taken in this research project.

3.3 Simulation Results

3.3.1 Layout effect on the field distribution

Electric field contours and probable leakage paths are shown in Fig. 3.3 for all six patterns. It can be seen that the highest field points are located at the bends or the tips of interconnects where the field flux lines converge.

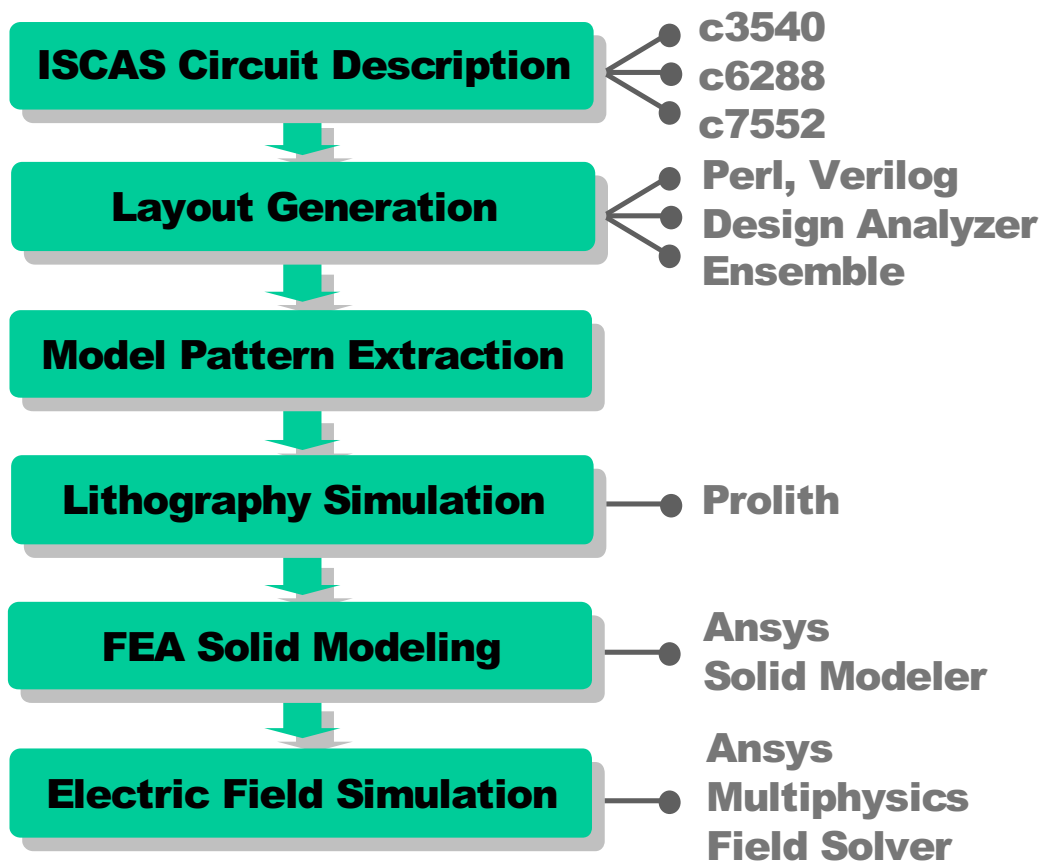


Figure 3.2: Simulation flow for electric field characterization of various geometries in circuit layouts. Simulation starts with generating layouts from ISCAS benchmark circuits c3540, c6288, and c7552.

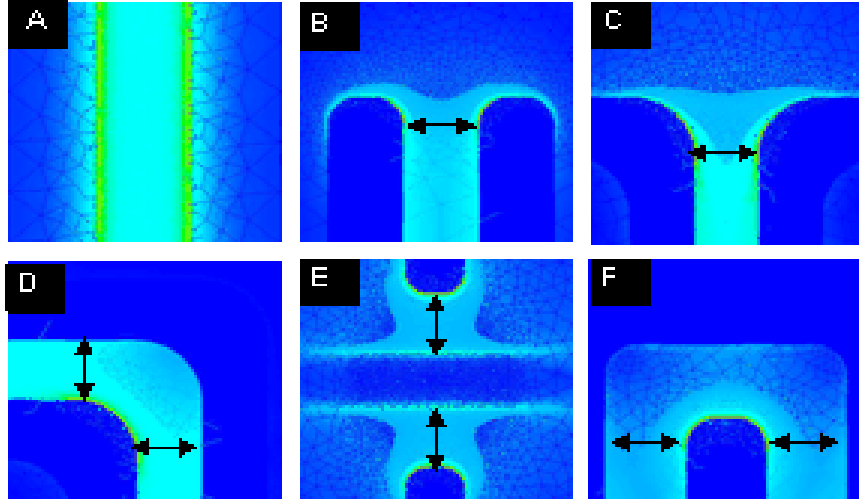


Figure 3.3: Electric field contour plots (top view) showing enhanced electric field intensities at bends and tips. Most probable leakage paths are indicated with arrows between adjacent peak electric field points.

Figure 3.4 shows peak electric field intensities near the critical points for all six models with various feature sizes. From this result, it is clear that the electric fields for test patterns (Model B to F) are distinguishably higher than for parallel interconnects (Model A). For example, looking at the data for metal width/space of $0.2\mu\text{m}$, we can see that the highest electric field intensity, which is for Model F, is almost three times stronger than the one for parallel interconnects.

Figure 3.5 shows the sensitivities of electric field to minor layout changes. It is clear that a small change in layout geometry can result in a significant change in electric field in a back-end structure.

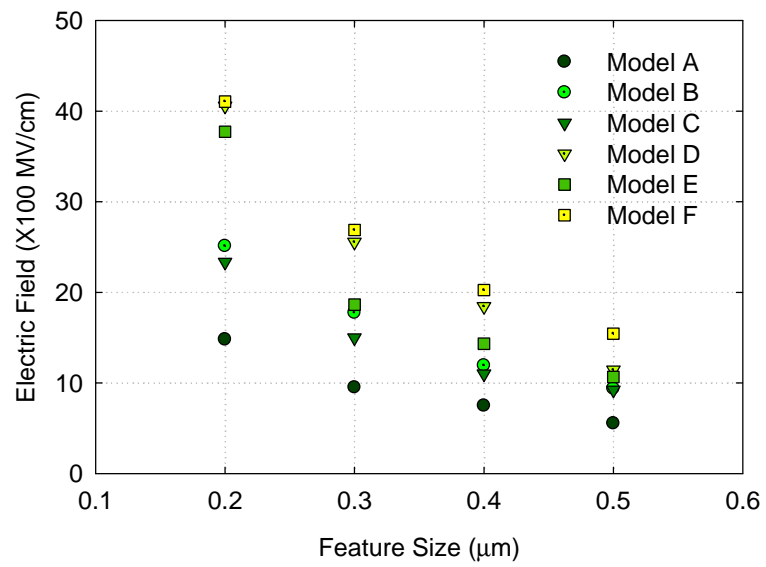


Figure 3.4: Comparison of peak electric field as a function of interconnect feature size for pattern models.

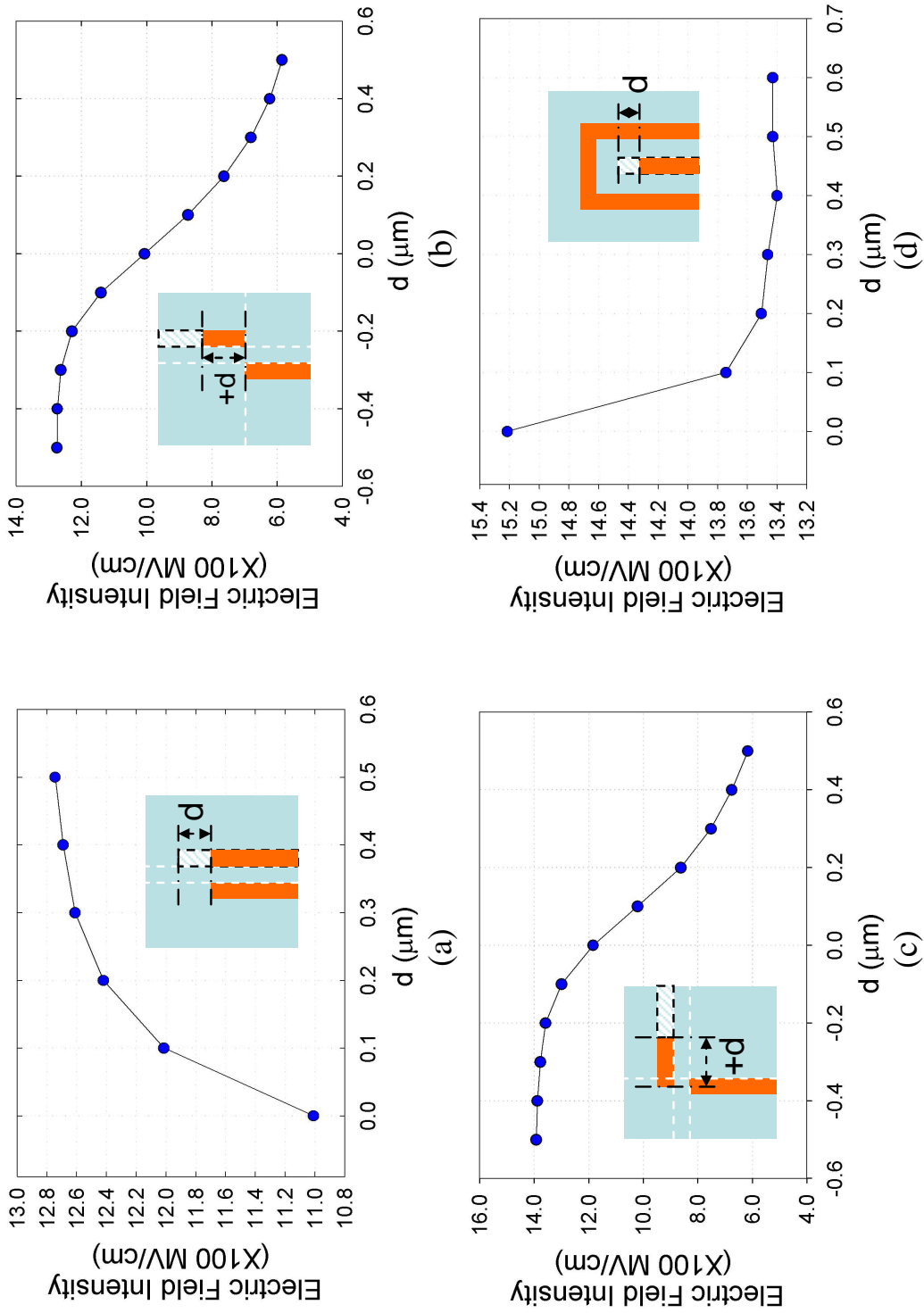


Figure 3.5: Plots showing sensitivities of electric field change from minor layout changes.

Figure 3.6 shows the electric field intensity distributions on cut planes at different depths for Model A and B. To do this, 3-D solid models were sliced along the x-y plane. The areas of cut planes were divided into small grids, and then electric field intensities in each grid were counted. Section A corresponds to the cut plane aligned with the interconnect top surface belongs to and section G corresponds to the cut plane aligned with the interconnect bottom surface. The vertical height between these two cut planes was evenly divided and assigned to sections B to F. From this, it is clear that the strongest electric field is along section A and G which coincide with the top and bottom surfaces.

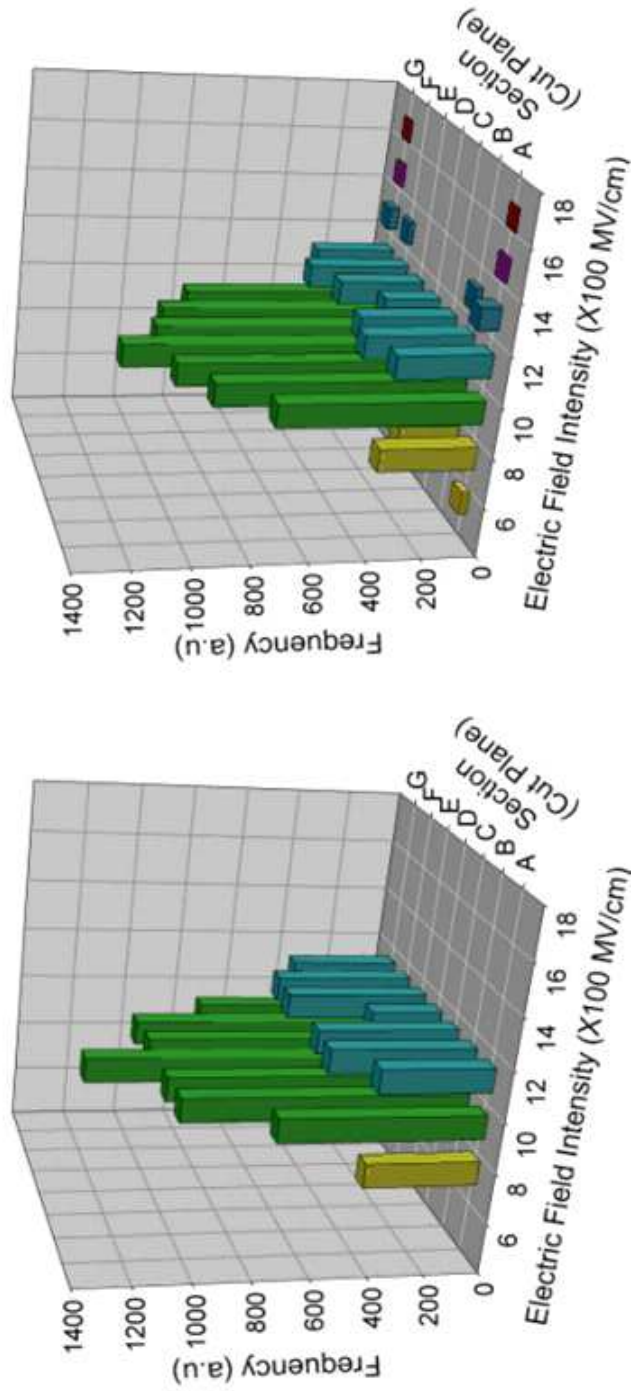


Figure 3.6: Histograms showing the field strength distribution on cut planes for Model A (a) and Model B (b). See Fig. 2.16 for cut plane positions.

High electric fields can lead to stronger and faster copper ion (Cu^{2+} or Cu^+) drift into the inter-metal dielectric film along the leakage paths between interconnects [5, 7]. Considering copper ion drift as the most important factor for back-end dielectric breakdown, we can safely conclude that test patterns (Model B to F) are much more vulnerable to dielectric breakdown than parallel interconnect (Model A). Figure 3.7 demonstrates the breakdown sites in actual test structures.

3.3.2 Effect of vertical structure and material property (dielectric constant) on electric field

Figure 3.8 shows the electric field intensity along a straight vertical path designated by the arrow on the inset contour plot. From this figure, it is apparent that the electric field is much stronger at the top and bottom corners of the interconnects as previously shown in Fig. 3.6. By observing the electric field distribution in the vertical cross section shown in Fig. 3.9, it is clear that the electric field is concentrated at the corners. These highest electric field locations coincide with the interface between the low- k dielectric and the etch stop layer which is formed by chemical mechanical polishing (CMP).

It should be noted that it is not the high dielectric constant of the etch stop layer (ESL) which is usually SiC or SiN_x that makes the electric field strongest at the corners. What varies when the dielectric constants of materials change is the D-field (electric flux density or displacement) as shown in Fig. 3.10. The fact that the electric field is strongest at the corners, which is a part of the CMP surface, has significant meaning from the reliability point of view. This is because the interface formed by the CMP process is of low quality with many interface states and dangling bonds [15, 13]. Therefore high electric fields in this region make copper ion drift along the interface easier and make this the most probable leakage path between interconnects.

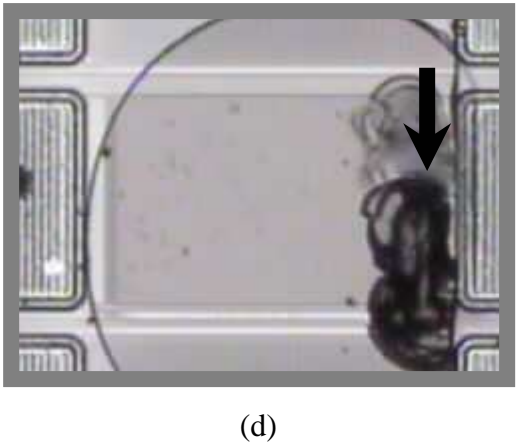
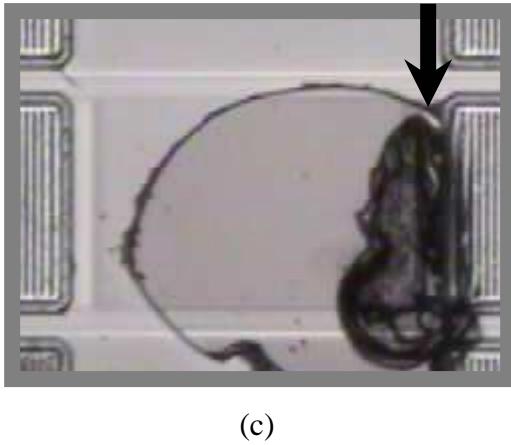
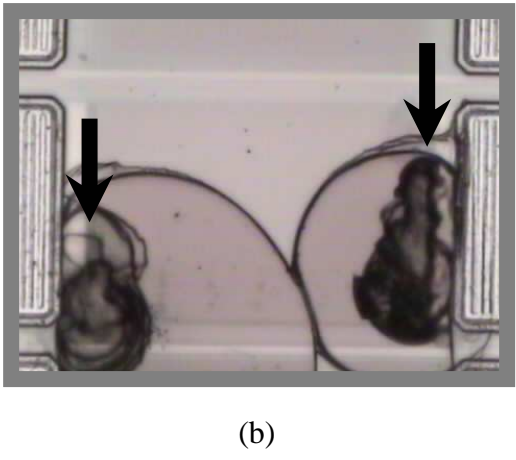
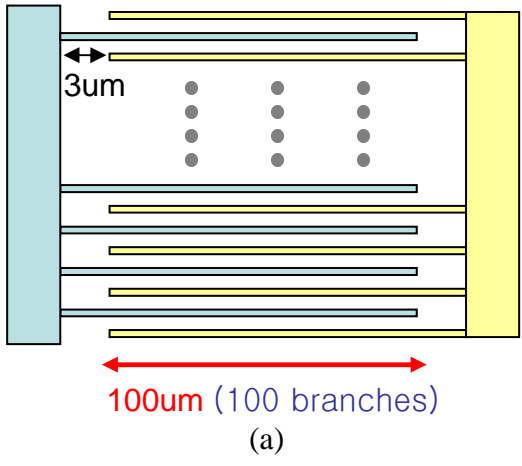


Figure 3.7: Comb test structure used for BTS lifetime testing (a), and microphotographs of failed samples (b),(c), and (d). The failure sites that the arrows are pointing to are where the line terminations are.

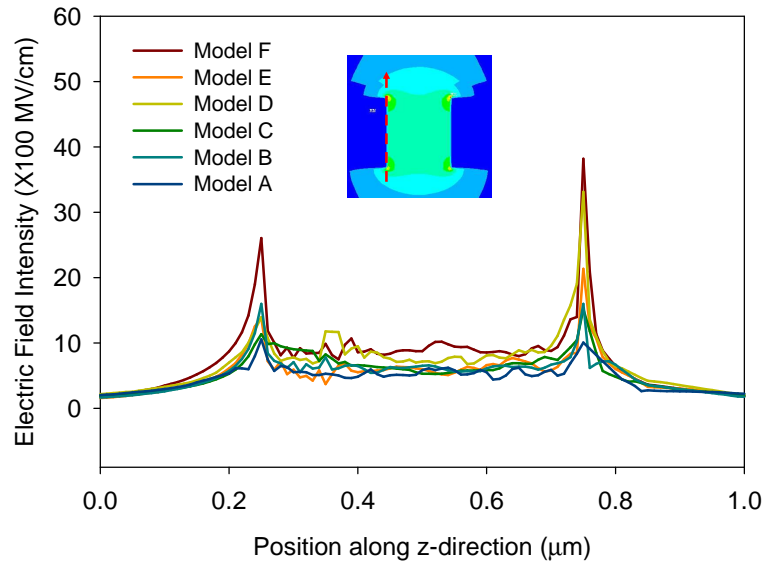


Figure 3.8: Electric field along a vertical path in inter-metal dielectric (IMD) (path designated with the arrow in the inset contour plot). The peaks occur at the bottom ($\sim 0.2\mu\text{m}$) and the top ($\sim 0.8\mu\text{m}$) of the IMD.

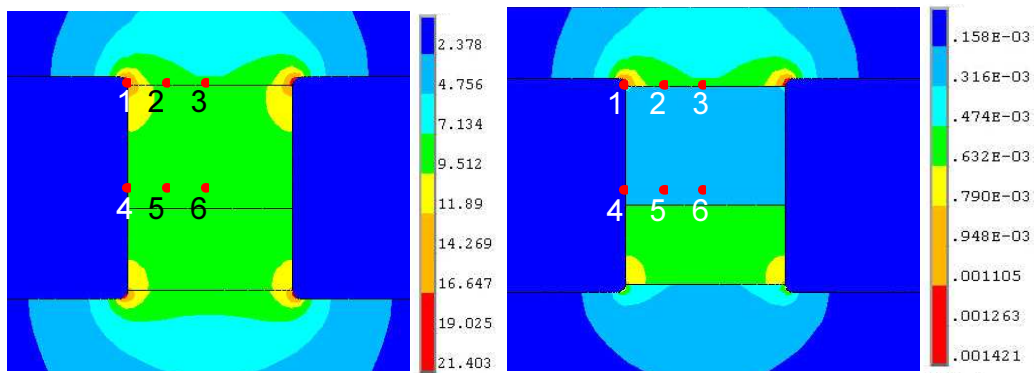


Figure 3.9: Cross section contour plots for electric field (left), and electric flux density (right). (Red dots are reference points for Fig. 3.10 below)

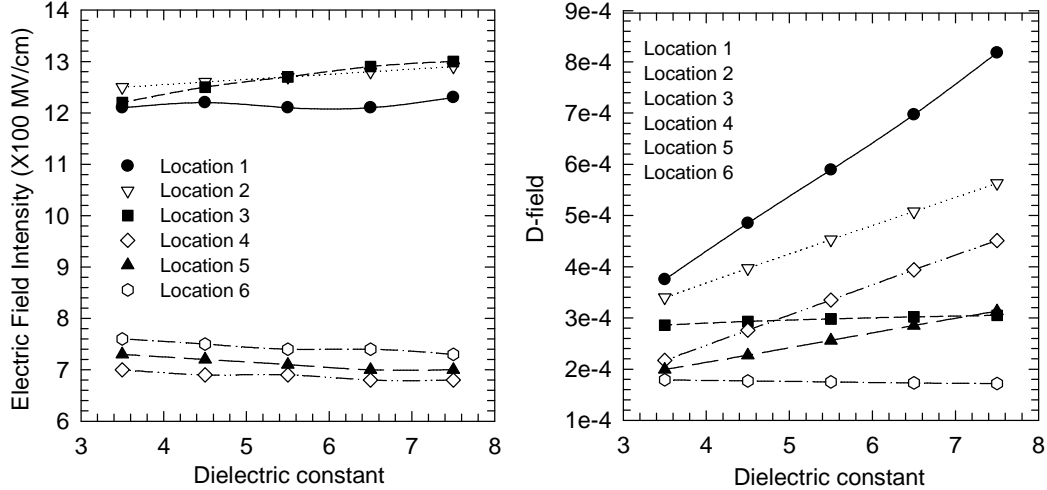


Figure 3.10: Electric field (left), and electric flux density (right) as a function of dielectric constant. The electric field does not show a major change while electric flux density does as a function of the dielectric constant. (Refer to Fig. 3.9 for the location references.)

3.3.3 Improved Test Structure Design

Typically, the test structures used for the evaluation of back-end dielectric breakdown are the simple comb or the comb/serpentine structures, shown in Fig. 3.7(a). This structure primarily consists of parallel lines (Model A) and features in Model F.

Because the electric field in the back-end is non-uniform due to the complexity of the actual layouts, this conventional test structure is not capable of representing the actual chips. Therefore a wider variety of structures are required to develop models of the relationship between electric field and breakdown. We suggest extending the set of structures for characterization of back-end dielectric breakdown to the larger set shown in Fig. 3.11.

Figure 3.11 (a) contains the features from Models D and F, with the minimal distance between the tip and the adjacent interconnect. To maximize the sensitivity of the test result to geometrical factor, it is important to minimize the parallel-line portion in the test structure. Figure 3.11 (b)-(d) are variations of Models B and C, and emphasizes structures with parallel tips/lines or parallel tips/tips. Figure 3.11

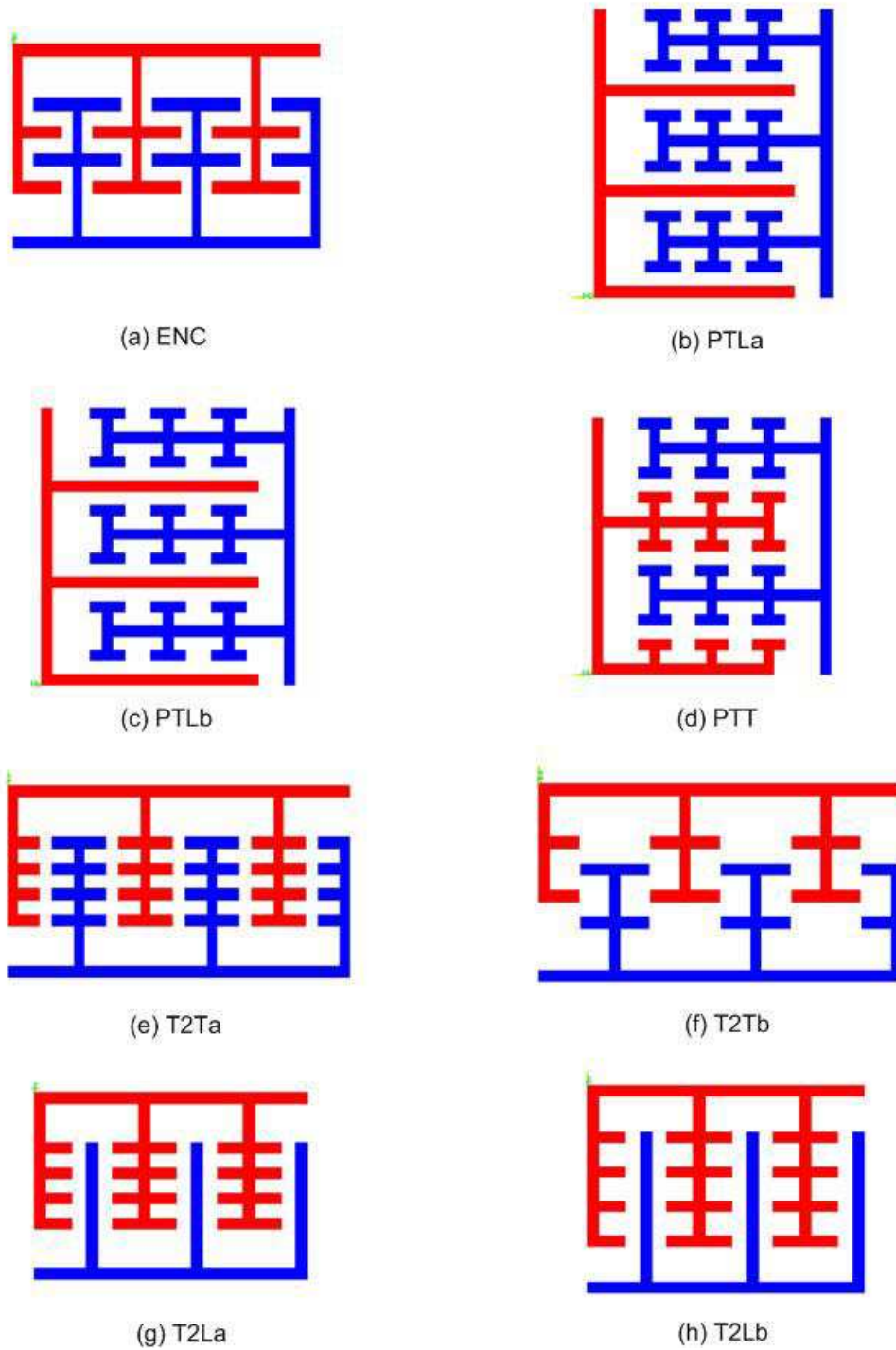


Figure 3.11: New test structures suggested in this research to develop models of the relationship between electric field and breakdown. (a) ENC (Enclosed tips), (b) PTLa (Parallel tip and line, closely packed), (c) PTLb (Parallel tip and line, loosely packed), (d) PTT (Parallel tip and tip), (e) T2Ta (Facing tip to tip, aligned), (f) T2Tb (Facing tip to tip, with offset) (g) T2La (Facing tip to line, closely packed), and (h) T2Lb (Facing tip to line, loosely packed).

(e)-(h) are variations of Model E and emphasizes tips abutting tips (e and f) or tips abutting line (g and h). These structures enable characterizing the relationship between the electric field distribution and breakdown.

In this section, it was shown that there are significant changes in electric field among different layout patterns, and the field is much stronger at critical points like bends or tips. High electric fields along the critical leakage paths between adjacent interconnects can be a major driving force for copper ion drift. Hence, most probable leakage paths are identified based on the electric field. Considering copper ion drift as the most important factor for failure of the inter-metal dielectric, we can safely conclude that the test patterns (Models B to F) are much more vulnerable to failure than parallel interconnect (Model A). The high electric field combined with some process problems like low quality interfaces formed by CMP or copper contamination from back sputtering of copper during via etch can degrade the reliability drastically. This result emphasizes the importance of taking feature geometries into account when characterizing BEOL structure reliability.

3.4 Full Chip Analysis

A full chip is composed of a combination of area scaled versions of all of the test structures. To find the full chip failure rate, we start by calculating the activated defect densities, $D_{test,i}$ for each test structure, i:

$$D_{test,i} = \frac{\alpha_i}{A_{test,i}} \left[\exp \left\{ \frac{1}{\alpha_i} \left(\frac{t}{\eta_i} \right)^{\beta_i} \right\} - 1 \right] \quad (3.1)$$

where $A_{test,i}$ is the area of the i^{th} test structure, α_i is the clustering parameter extracted from data for the i^{th} test structure, and β_i and η_i are Weibull shape and scale parameters respectively extracted from data from the i^{th} test structure.

However, we have to notice that the test structures are composed of tips and parallel area between the adjacent interconnects. Therefore we need to separate

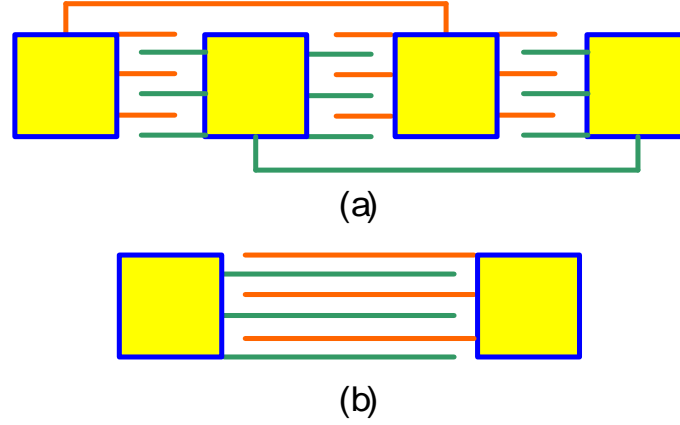


Figure 3.12: Two possible area multiplication schemes in designing test structure, (a) repeated segments structure, and (b) continuously extended structure. Note the difference in the number of line-end terminations between the two schemes while the parallel region areas are the same.

$D_{test,i}$ for the parallel area from that for the tips. For this purpose, two kinds of test structures, continuously extended and repeated segment structures, can be used. These test structures are shown in Fig. 3.12.

Notice that those test structures shown in Figure 3.12 have the same parallel areas but different number of tips. The repeated-segment test structure shown in Fig. 3.12 (a) has three times more tips than the continuously extended test structure shown in Fig. 3.12 (b).

With these two test structures, we can use Eq. (3.1) to find $D_{test,i} \cdot A_{test,i}$, which is the total number of defects, for the two test structures. Let's suppose we get $D_{cont} \cdot A_{cont}$ from the continuously extended structure and $D_{seg} \cdot A_{seg}$ from the repeated-segment structure. Then the number of defects due to the surplus tips in repeated-segment test structure is

$$D_{seg} \cdot A_{seg} - D_{cont} \cdot A_{cont} \quad (3.2)$$

Here the number of tips is known and we can compute the defect density originated only from tips. The number of defects for $1 \times$ tips is

$$\frac{D_{seg} \cdot A_{seg} - D_{cont} \cdot A_{cont}}{2} \quad (3.3)$$

Therefore, the number of defects for the parallel area in continuously extended test structure is

$$D_{cont} \cdot A_{cont} - \frac{D_{seg} \cdot A_{seg} - D_{cont} \cdot A_{cont}}{2}. \quad (3.4)$$

With this and the known area between the parallel lines, we can compute the defect density for the parallel area. This sequence explains how the defect densities for the tips and the parallel areas can be separated and the same method can be applied to all the test structures shown in Fig. 3.11.

Let's suppose that the chip contains area $A_{test,i}$ with features that match the i^{th} test structure. The yield is then the product of the yield corresponding to each of the areas, $A_{test,i}$:

$$S(t) = \prod_i S_i(t) = \prod_i \left(1 + \frac{A_{chip}}{\alpha_i} D_{test,i}(t) \right)^{-\alpha_i} \quad (3.5)$$

Consequently, the cumulative probability density function of the failure rate for the full chip is given by

$$F_{chip}(t) = 1 - \prod_i \left[1 + \frac{A_{chip}}{A_{test,i}} \left\{ \exp \left(\frac{1}{\alpha_i} \left(\frac{t}{\eta_i} \right)^{\beta_i} \right) - 1 \right\} \right]^{-\alpha_i} \quad (3.6)$$

We find the probability density function of the failure rate by differentiating the cumulative probability density function, as follows.

$$f_{chip}(t) = \frac{d}{dt} F_{chip}(t) \quad (3.7)$$

and we find the mean time to failure by integrating, as follows.

$$MTTF_{chip} = \int_0^{\infty} t f_{chip}(t) dt \quad (3.8)$$

Figure 3.13 demonstrates schematically the process flow for full chip reliability evaluation in the design stage. In this methodology, first, critical circuit area is calculated and the critical patterns are extracted from the layout. Second, critical area is used to compute the reliability while extracted patterns are compared with

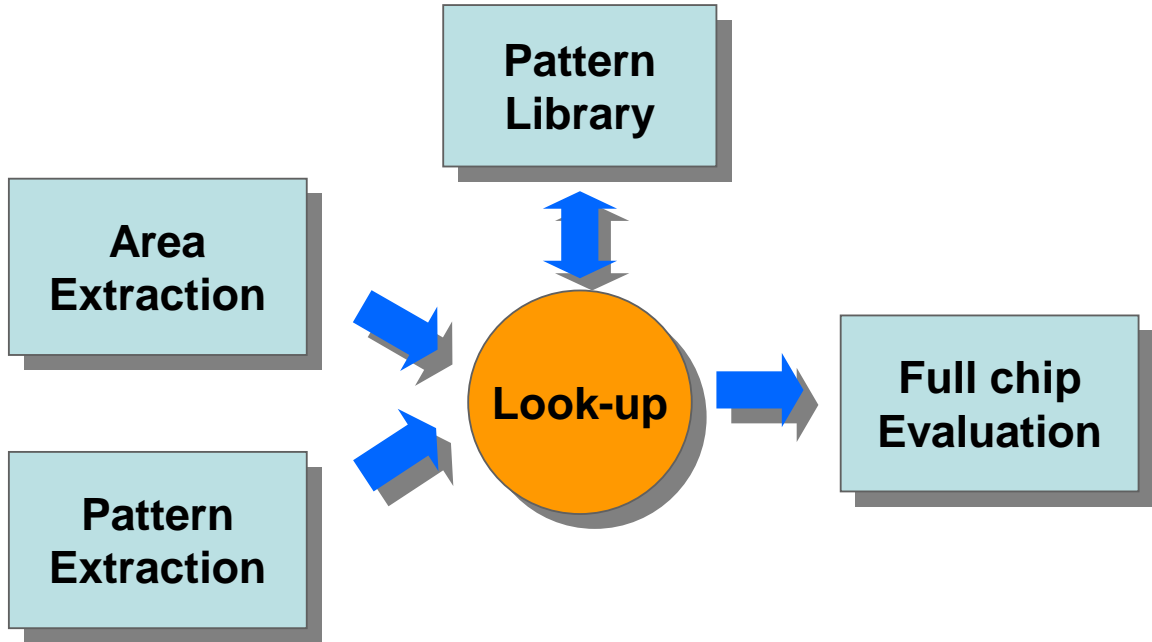


Figure 3.13: Diagram showing the full chip reliability evaluation process flow.

pattern library for their weight on reliability. By considering the impacts from both the circuit area and the layout geometries, we will be able to predict the reliability of a back-end structure at the design stage.

However there are other physical design factors than the ones mentioned above that affect circuit reliability. They include pattern density and vias, and they will be discussed in the following chapter.

CHAPTER 4

ANOTHER PHYSICAL DESIGN FACTOR : PATTERN DENSITY EFFECT

4.1 Impact of Seemingly Unrelated Factor, Linewidth, on Dielectric Reliability

As devices are scaled to smaller dimensions, existing minute variations in the manufacturing processes are expected to affect key circuit performance parameters. For example, small variation in the channel length of metal oxide semiconductor field effect transistors (MOSFETs) did not cause any serious problems before the drawn channel length became comparable to the wavelength used in lithography. Such variation is now commonly recognized as one of the most fundamental roadblocks to device scaling. It has also been demonstrated that the local interconnect density and process variations in photolithography and chemical mechanical polishing (CMP) result in the fluctuation of circuit performance metrics.

The discussion of the effect of process variation is expanded to the area of reliability, especially for back-end dielectrics, from the design-for-reliability (DFR) viewpoint. The spacing between metal lines is commonly known as the only design parameter that affects the reliability of the dielectric film between the lines. Through a series of experiments and simulations, it is shown that a seemingly unrelated factor - metal line width - also affects the dielectric reliability. A similar result was also reported earlier by another researcher [48].

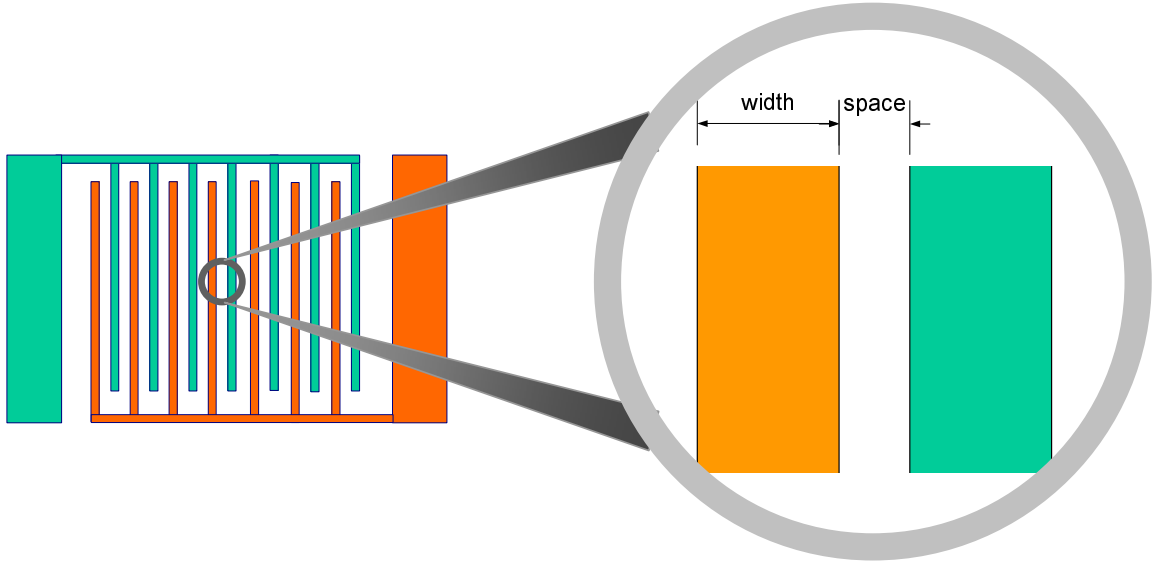


Figure 4.1: Test structure used for investigation of metal linewidth effect on reliability.

4.2 *Experiment*

4.2.1 Test Structures

Comb test structures with various splits in metal line width, with two fixed line spacings of $0.12\mu\text{m}$ and $0.17\mu\text{m}$, were used in this work. The test vehicle was fabricated using a Cu/low- k process. Figure 4.1 depicts the test structure schematically and Table 4.1 shows the specification of the test structures used for this purpose.

4.2.2 TDDB Test Results

The test structures were subjected to bias temperature stress (BTS) tests to characterize the time-dependent dielectric breakdown (TDDB) distribution at the test temperature of 150°C .

Figure 4.2 displays a typical current vs. time plot from the TDDB test. It is clear that the metal line width has a significant impact on inter-metal dielectric lifetime.

Figure 4.3 is the time to failure distributions for the test structures with line spaces of (a) $0.12\mu\text{m}$ and (b) $0.17\mu\text{m}$ respectively. In each case, there are three variations in metal line widths, as indicated in the figure. It is clear that for the wider the metal

Table 4.1: Test structure specifications

(units in μm)			
	Width	Space	Length
Group 1	0.12	0.12	10000
	0.14	0.12	10000
	0.18	0.12	10000
	0.12	0.14 ^a	20000 ^c
Group 2	0.12	0.18 ^b	20000 ^c
	0.18	0.17	10000
	0.80	0.17	10000

^a 0.12 m/0.14 m test pattern is used to evaluate the lithographic variation effect on reliability.

^b This slightly larger space than other patterns in the Group2 can lead to a better reliability test result.

^c Different lengths for patterns d and e will be accounted for and compensated by applying an area scaling factor in the data analysis [49].

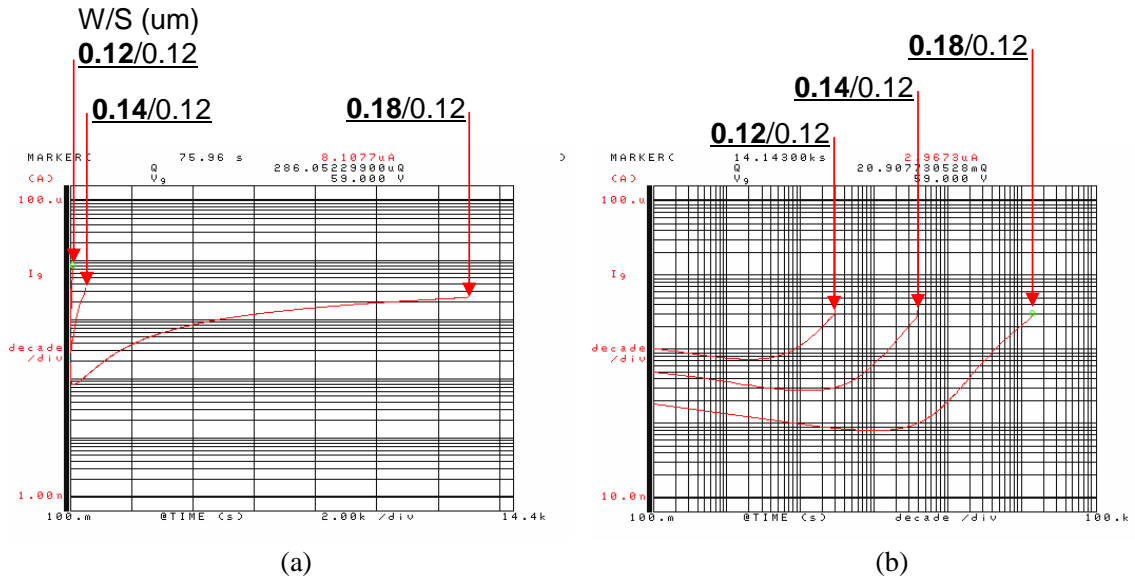


Figure 4.2: Typical current-time characteristics for the space=0.12 μm series on the semi-log scale (a), and the log-log scale (b).

lines, the mean time to failure is longer. Figure 4.4 demonstrates the same trend more clearly. As can be seen in this figure, with the wider space between lines, the metal linewidth effect becomes weaker. Also, it should be noted that the metal linewidth effect on failure distribution becomes saturated at some point, as shown for the case of the $0.17\mu\text{m}$ metal line space.

4.3 Study on Physical Causes

In this section, several feasible causes for the test results shown in § 4.2.2 are suggested. The physical causes discussed in this section include electric field enhancement, optical proximity effect, and micro-loading effect.

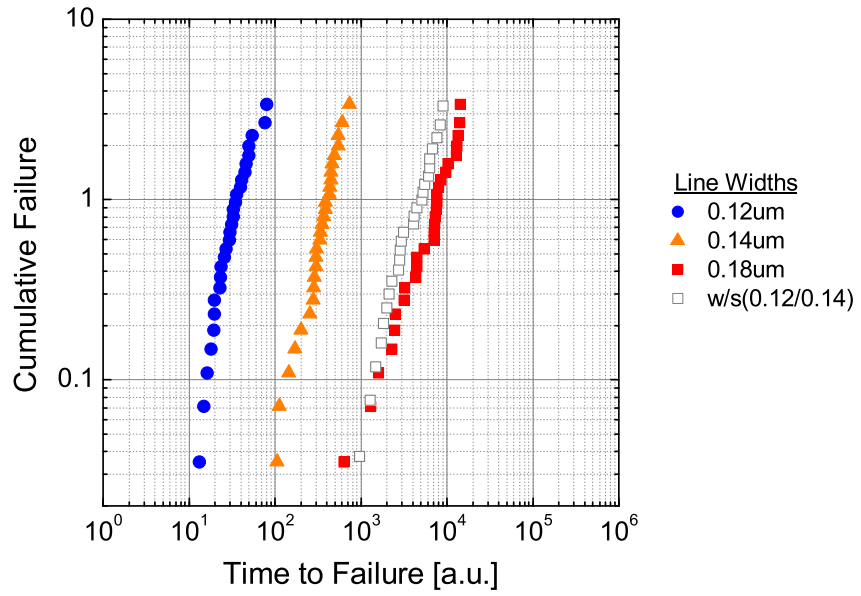
4.3.1 Enhanced Electric Fields

First, the electric field distribution is investigated using finite element analysis, and the result is displayed in Fig. 4.5(a). It should be noted that as the metal line width becomes smaller, the electric fields from neighboring lines start to overlap. In Fig. 4.5(b), the overall trend is demonstrated more clearly. In accordance with the result from the experiments, Fig. 4.5(b) shows that the line-width effect on electric field starts to decrease as the space between lines increases. However it is conjectured that the electric field effect alone cannot successfully explain the observed reliability differences because the enhancement is limited in its magnitude.

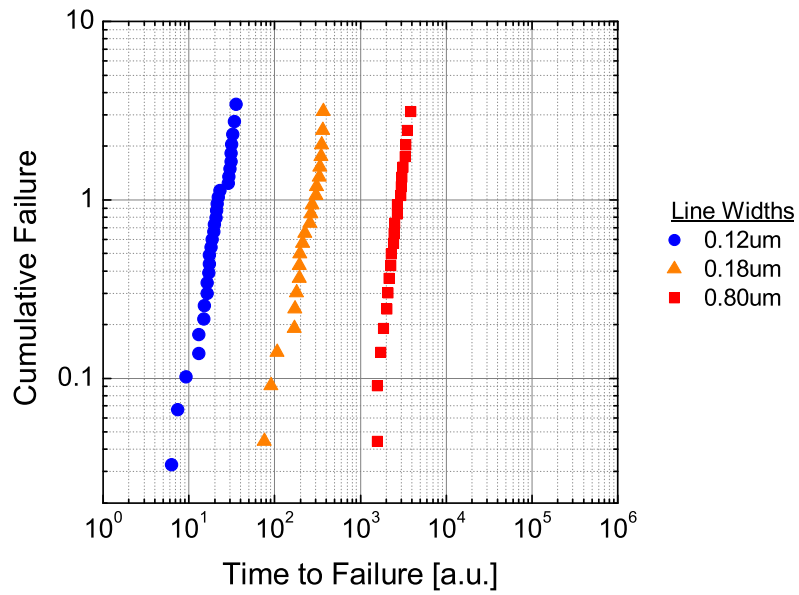
4.3.2 Physical Analysis Result

For the purpose of investigating the physical differences between test structures in terms of spacing between the metal lines, A scanning electron microscopy (SEM) analysis was performed. Figure 4.6 demonstrates the physical analysis point and the cross-section of the test structure.

Figure 4.7 ~ 4.10 show the results from SEM analyses. Figure 4.7 and 4.8 are for the test structures with $0.17\mu\text{m}$ drawn space between metal lines and Fig. 4.9 and



(a)



(b)

Figure 4.3: Time to failure distributions for test structures with line spaces of (a) 0.12 μm and (b) 0.17 μm.

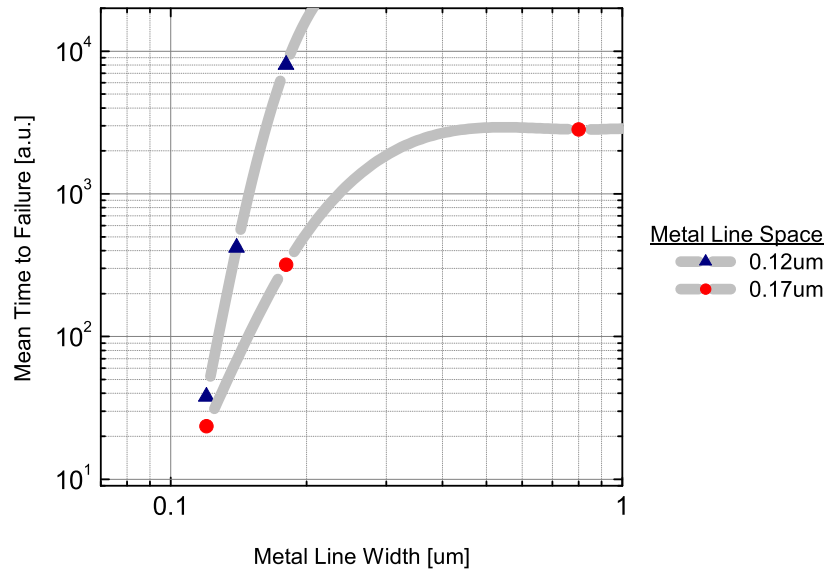


Figure 4.4: Mean time to failure (MTTF) trend as a function of metal line width at two fixed inter-metal spacings of $0.12\mu\text{m}$ and $0.17\mu\text{m}$.

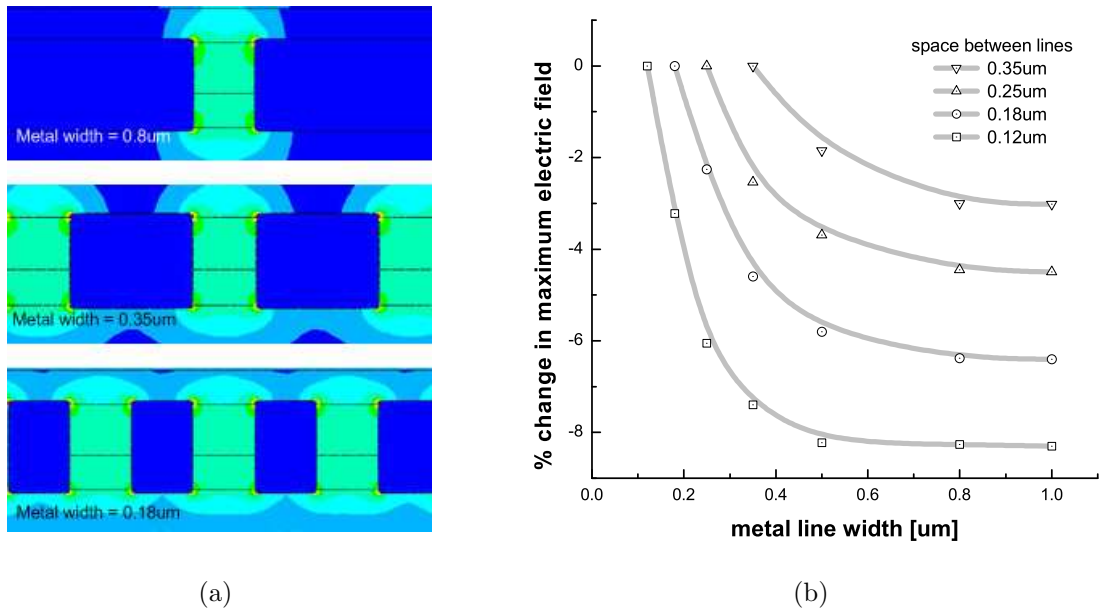


Figure 4.5: (a) Electric field contour plots for wide (width = $0.80\mu\text{m}$, at the top), intermediate (width = $0.35\mu\text{m}$, in the middle) and narrow (width = $0.18\mu\text{m}$, at the bottom) metal lines with the same inter-metal spacing. (b) Change in the peak electric field intensity as a function of metal line width.

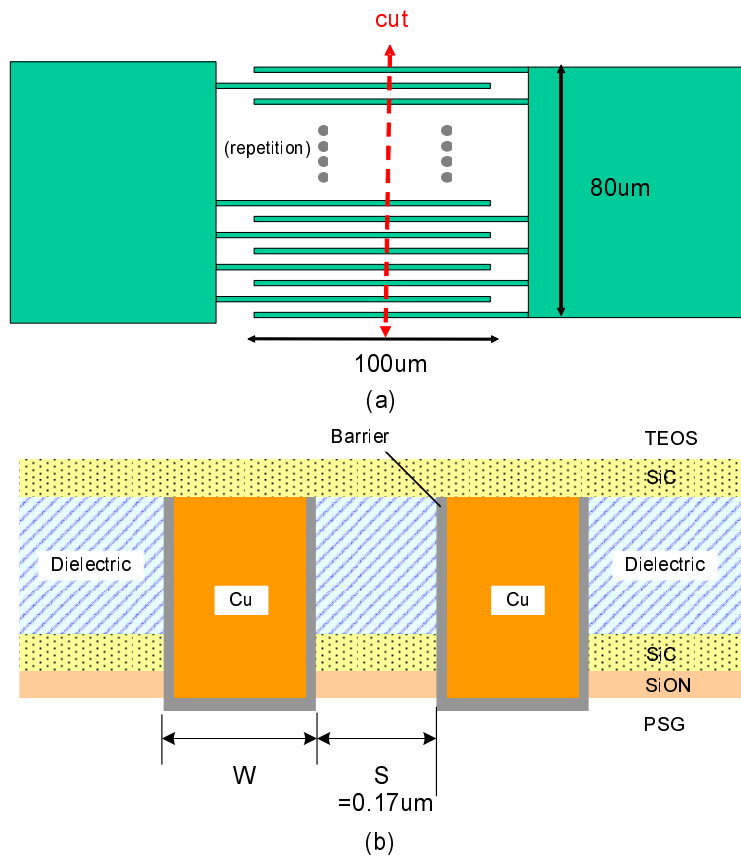


Figure 4.6: (a) Cut direction of the SEM analysis, and (b) description of the cross section.

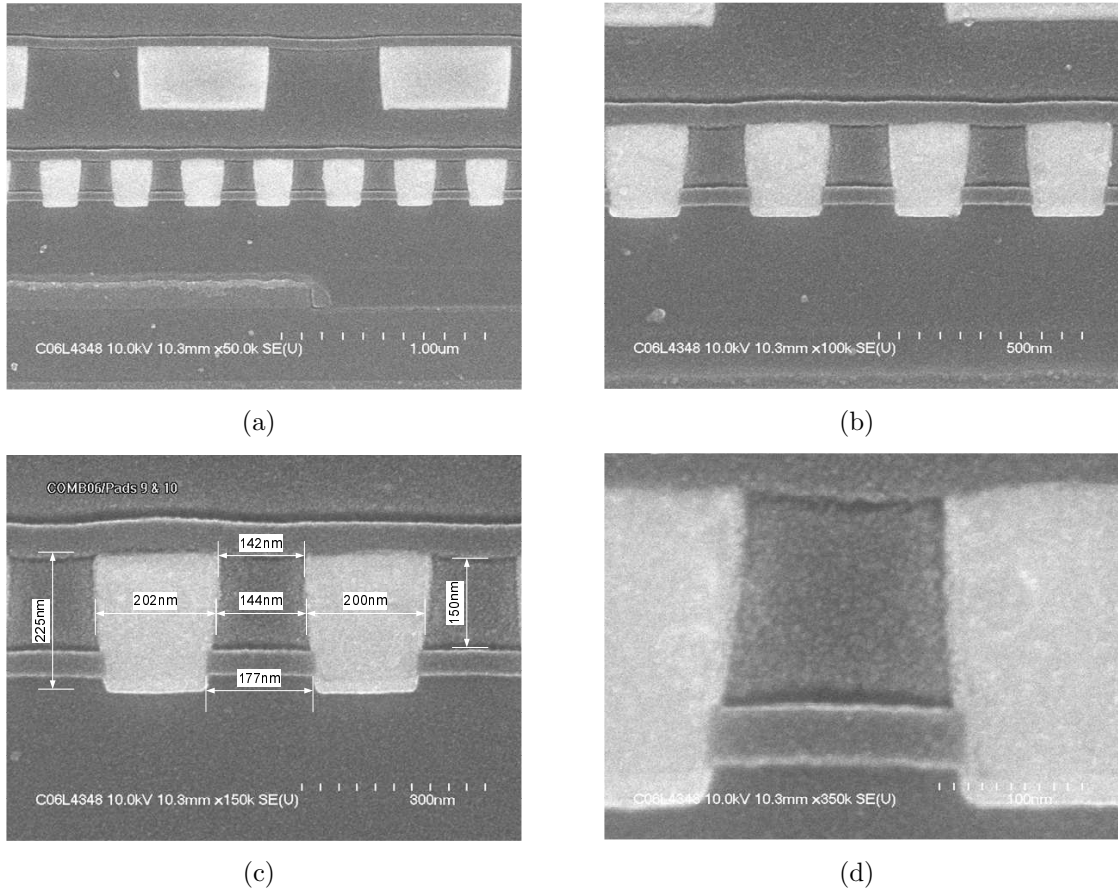
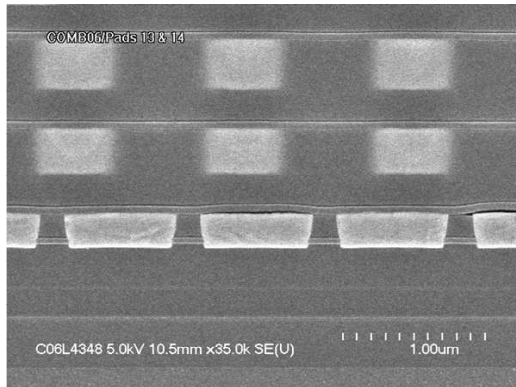


Figure 4.7: Cross-section SEM photographs of the comb test structure with space=0.17µm and width=0.18µm.

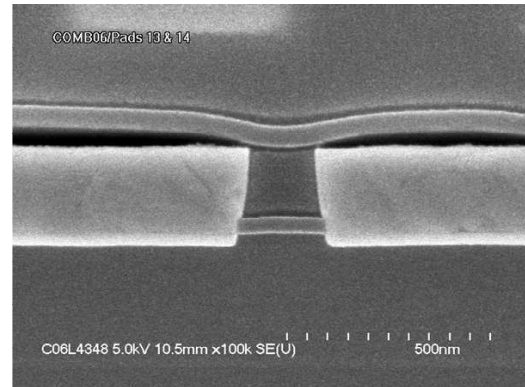
4.10 are for the test structures with 0.12µm drawn space.

Table 4.2 and 4.3 summarize the variation of spaces between lines as a function of line width at different vertical locations. Table 4.2 is for the case of test structures with drawn space of 0.17µm and Table 4.3 is for the case of test structures with drawn space of 0.12µm.

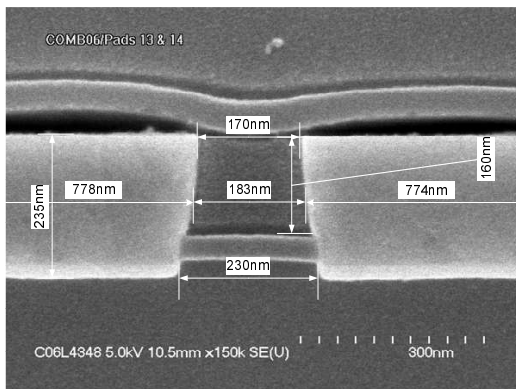
From the analysis result shown in Tables 4.2 and 4.3, it is clear that the spacing between metal lines does vary as a function of adjacent metal line widths. This result corroborates the trend predicted from the study on photolithographic and etch micro-loading effect as was explained in § 4.3.



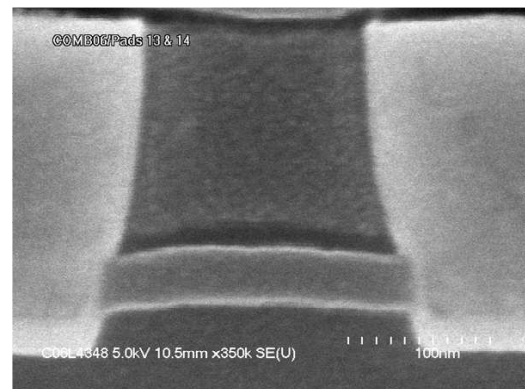
(a)



(b)

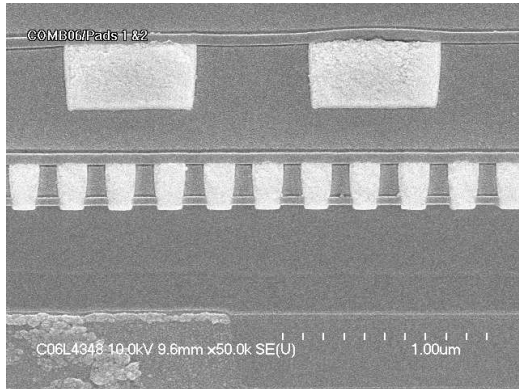


(c)

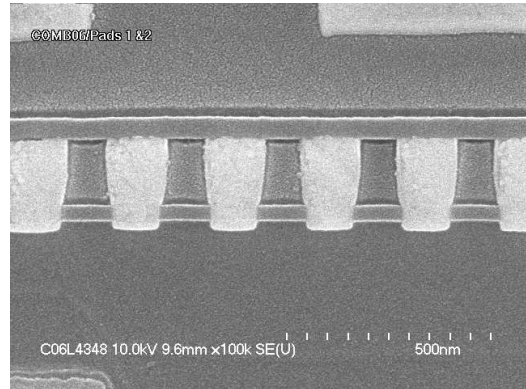


(d)

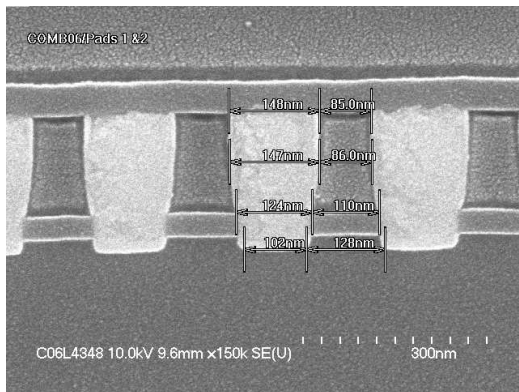
Figure 4.8: Cross-section SEM photographs of the comb test structure with space=0.17um and width=0.80um.



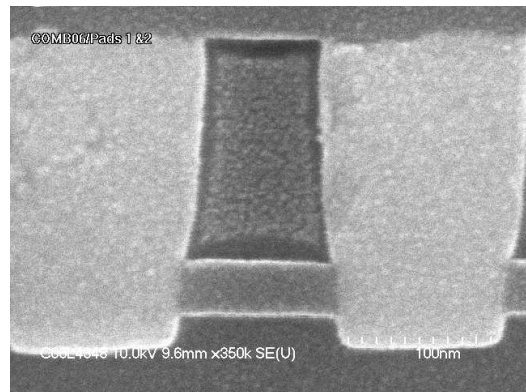
(a)



(b)

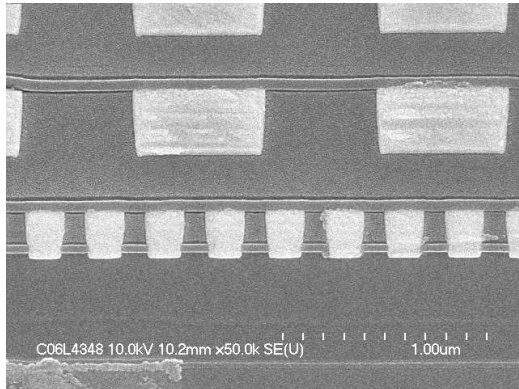


(c)

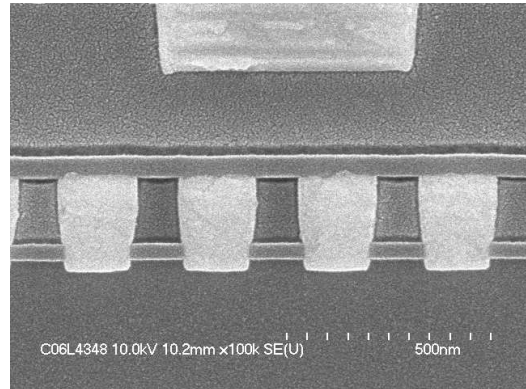


(d)

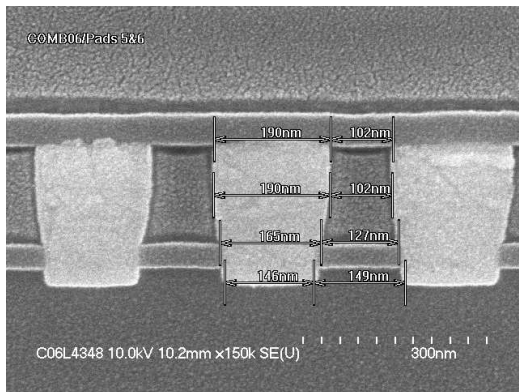
Figure 4.9: Cross-section SEM photographs of the comb test structure with space=0.12μm and width=0.12μm.



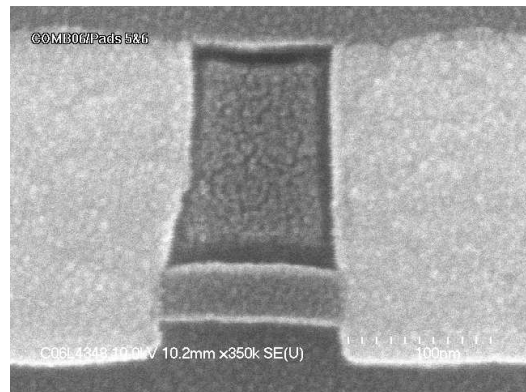
(a)



(b)



(c)



(d)

Figure 4.10: Cross-section SEM photographs of the comb test structure with space=0.12um and width=0.18um.

Table 4.2: Variation of spaces between lines as a function of line width at different locations for test structures with drawn space of 0.17 μ m.

Measurement	Space between lines (nm)		Difference
Location	Group I (W=0.80 μ m)	Group II (W=0.18 μ m)	(%)
Entrance	170	142	16.5
Middle	183	144	21.3
Bottom	230	177	23.0

Table 4.3: Variation of spaces between lines as a function of line width at different locations for test structures with drawn space of 0.12 μ m.

Measurement	Space between lines (nm)		Difference
Location	Group I (W=0.18 μ m)	Group II (W=0.12 μ m)	(%)
Entrance	102	85	16.7
Middle	102	86	15.7
Bottom	149	128	14.1

4.3.3 Origin of Dimensional Variation

Because of the significance of the dimensional variation in the spacing between the metal lines as a function of metal line width, it is reasonable to conjecture that the dimensional change can be the biggest contribution that makes the TDDB difference shown in § 4.2.2. The next step will be to find out what is causing this dimensional variation. We are presenting two feasible factors below: optical proximity effect in the photolithography process and micro-loading effect in etch process.

4.3.3.1 Optical Proximity Effect

A series of lithography simulations were performed to see how much the optical proximity phenomenon affects the spacing between adjacent interconnects. Figure 4.11

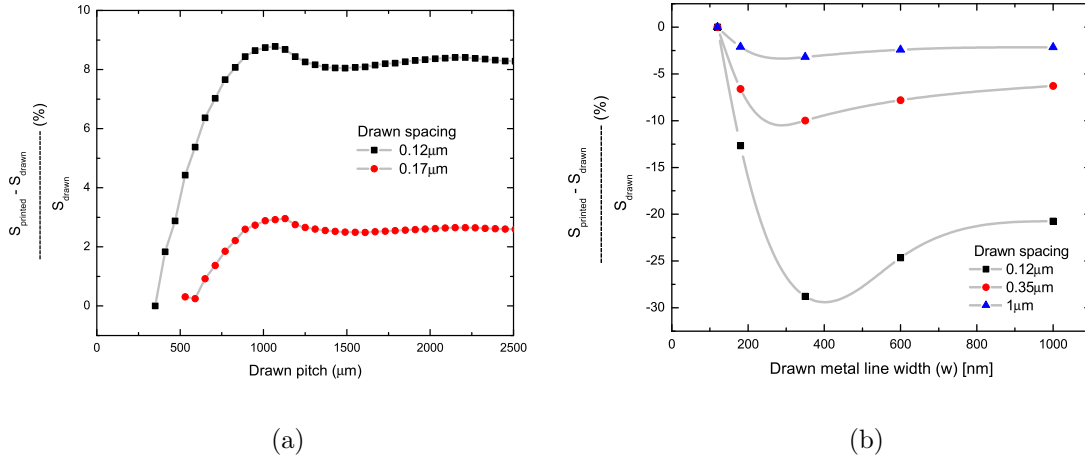


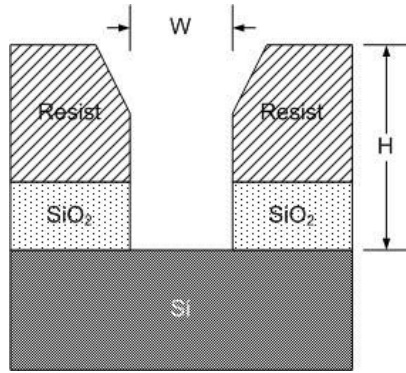
Figure 4.11: (a) Printed spacing between lines as a function of drawn size of the metal line pitch for three different drawn spacings between lines. $\text{NA} = 0.75$, ArF source, and conventional illumination with $\sigma=0.8$. (b) Printed spacing between lines as a function of drawn size of metal line width for three different drawn spacings between lines. $\text{NA} = 0.75$, ArF source, and annular illumination $0.85/0.55$.

displays the simulation results using two distinct lithography process parameter combinations. It shows that the metal line width has a measurable impact on the printed space between the lines.

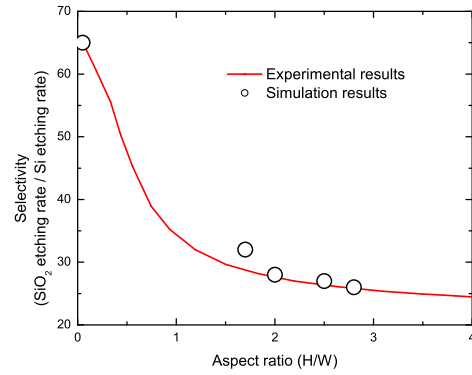
However it also should be noted that the photolithographic parameter setting is proprietary to specific manufactures and varies over a wide range. Therefore they can have any combination that lead to very different results as can be seen from the difference between Figs. 4.11(a) and 4.11(b). This means that the actual optical proximity effect can either be less distinguishable or even be reversed to give exactly the opposite trend in some cases with different parametric combinations. Therefore, optical proximity effect in lithography process cannot provide a decisive explanation for the MTTF trend shown in § 4.2.2.

4.3.3.2 Micro-Loading Effect in Etch Processes

Micro-loading can happen in etch process and it can provide an explanation for the difference observed in the TDDDB result between the test structures with the same



(a)



(b)

Figure 4.12: Micro-loading effect displayed in terms of etch selectivity between Si and SiO₂. (a) Vertical structure of the etch sample, and (b) etch selectivity as a function of the aspect ratio. Reproduced from [50].

drawn spaces but with different metal line widths. In dry etching processes, the key output parameters such as etch rate and etch selectivity are known to strongly depend upon pattern density and size of the etch sample.

Misaka *et al* reported the change of etch selectivity as a function of pattern aspect ratio as shown in Fig. 4.12 [50]. Micro-loading effect was demonstrated in terms of etch selectivity between Si and SiO₂. The same trend can be applied to other materials such as Si₃N₄, SiC and low-*k* dielectrics. In Figure 4.12, we can see that the etch selectivity decreases as the trench (or hole) size decreases. This means that the etch process becomes more isotropic as the etch feature size decreases.

Figure 4.13 demonstrates the mechanism schematically. Etched profiles are shown for three different sizes indicating the significant difference in the amount of deposited polymer film on the sidewalls. It is shown that the amount of polymer deposition is proportional to the size of the pattern. The polymer film deposited on the sidewalls prevents the etching of the sidewall therefore it explains the better etch selectivity.

Pattern density difference of the etch samples can worsen this anisotropy problem. As can be seen in Fig. 4.13, the etch rate depends on the etchable area (or pattern

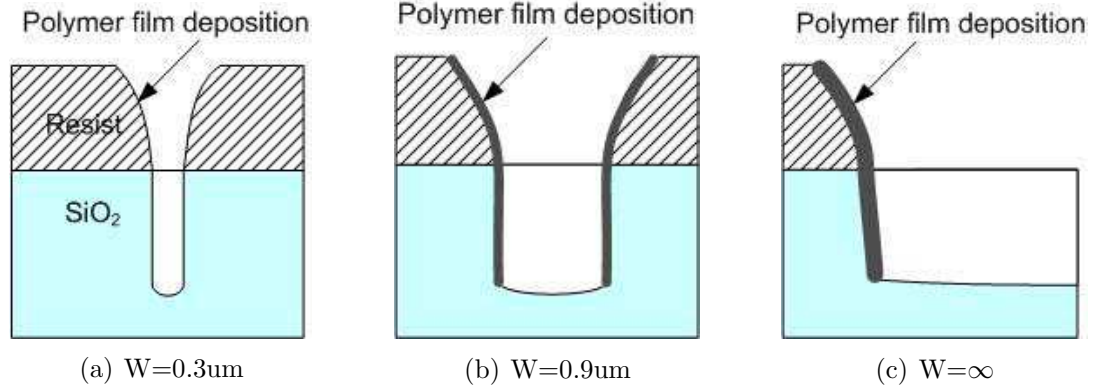


Figure 4.13: Schematic description for the origin of the etch micro-loading effect. Etched profiles are shown for three different sizes indicating the significant difference in the amount of deposited polymer film on the sidewalls. It is shown that the amount of polymer deposition is proportional to the size of the pattern resulting in the better etch selectivity. Reproduced from [50].

density) of the sample. It is shown that the etch rate becomes faster when the etchable becomes smaller, which in turn means the narrower metal lines.

The fit line in Fig. 4.13 is the Mogab model and it is expressed as follows.

$$ER = \frac{\beta\tau G}{1 + \beta\tau \frac{A_w d}{V}} \quad (4.1)$$

where β is the proportionality factor to etching species, τ is the mean lifetime of active etchant species, G is the etchant generation rate, A_w is the etchable area, d is a constant factor depending on density and molecular weight of the material to be etched, chemical reaction etc. and V is the reactor volume. Mogab model clearly shows the relationship between the etchable area and the etch rate.

The etchable area-etch rate relationship combined with the micro-loading effect introduced previously can be successfully applied to explain the TDDB lifetime difference shown in Fig. 4.3. In a test pattern with a narrow metal line width, the etch process becomes more anisotropic than in a wider metal line case. On top of that, the etch rate becomes faster in a narrower metal line cases making the anisotropy problem more significant. As a result, the space between narrower metal lines becomes narrower than the space between wider metal lines leading to a shorter TDDB

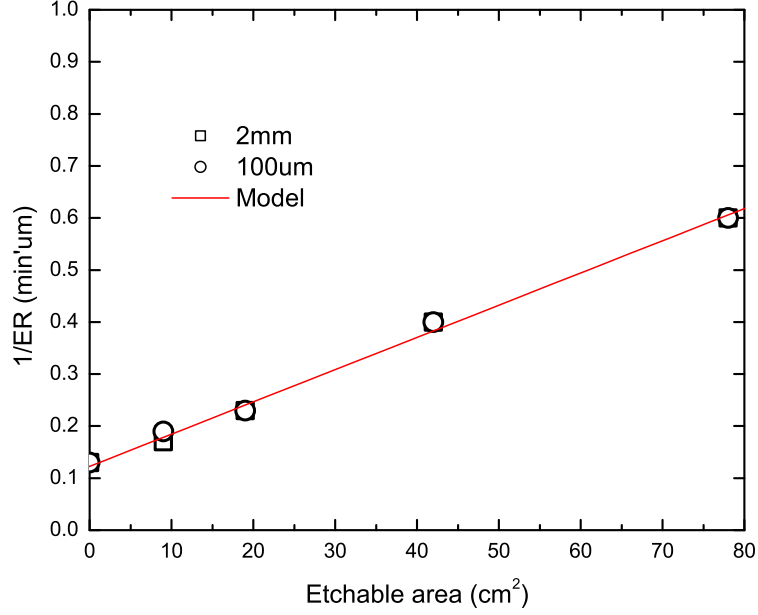


Figure 4.14: Etch rate displayed as a function of loading for 2mm square and 100 μ m line. The data is fitted to the model of Mogab [51]. Reproduced from [52].

lifetime. This is shown in Fig.e 4.15.

4.4 Mathematical Modeling

In this section, a mathematical model for the etch micro-loading effect is suggested. It is commonly known that etch does not have perfect anisotropy, and etch time is set to make sure that the worst location finishes etching to the bottom of the hole. This means that there is always some degree of lateral etching which is a function of etch time, etch rate and etch isotropy. Therefore, the actual dimension of the space after etch process can be expressed as follows.

$$S_{actual} = S_{drawn} + L_o + 2 \sigma_e t_e R_e \quad (4.2)$$

$$S_{actual} - S_{drawn} = \Delta S = L_o + 2 \sigma_e t_e R_e \quad (4.3)$$

where S_{actual} is the space after etch process, S_{drawn} is the drawn space size in the layout, L_o is the offset due to lithography process, σ_e is the degree of etch isotropy, t_e is the etch time, and R_e is the etch rate. Etch rate (R_e) can also be expressed as

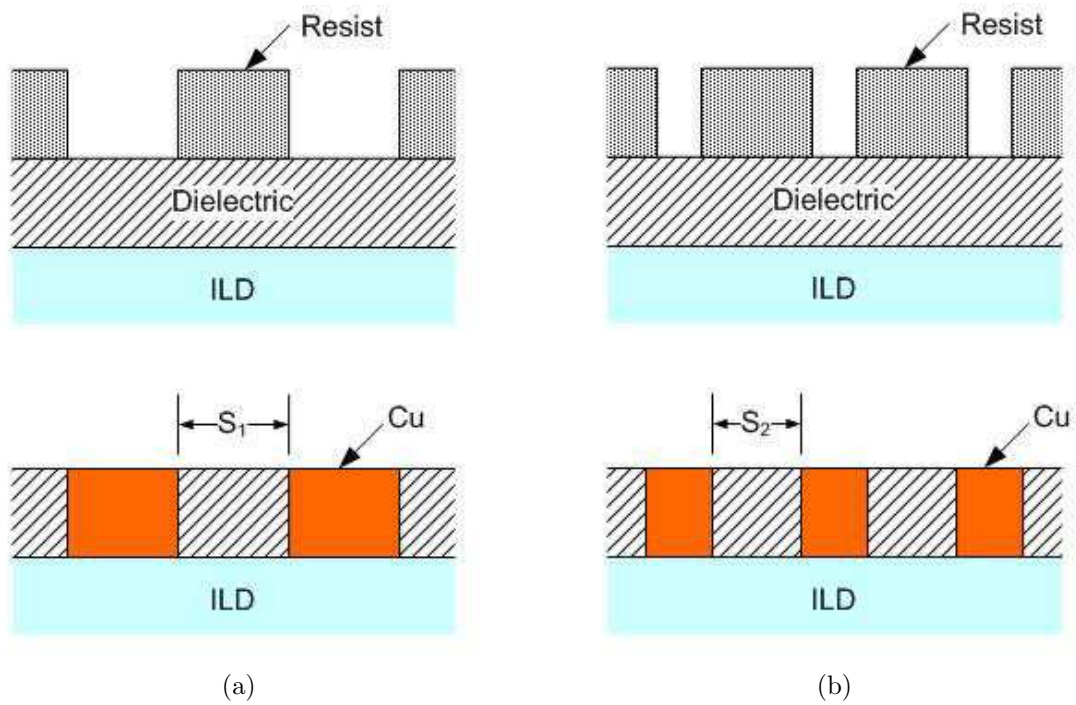


Figure 4.15: Predicted pattern dimension difference based on the micro-loading theory ($S_1 > S_2$). In the wider metal line case (a), the drawn space size is maintained (S_1), while in the narrower case (b), the space between the metal lines (S_2) shrinks as a result of the low-selectivity etch caused by the micro-loading.

follows.

$$R_e = \frac{C}{1 + BA_e} \quad (4.4)$$

where B and C are constants.

Letting $\alpha = 2 C \sigma_e t_e$, Eq. (4.3) can be rewritten as follows.

$$\Delta S = L_o + \frac{\alpha}{1 + BA_e} \quad (4.5)$$

The parameter α includes all the factors that determine the amount of lateral encroachment so that it can be appropriately called the lateral etch parameter.

Table 4.4 displays the etchable areas (A_e) along with the measured space between the lines and the ΔS calculated using the data shown in § 4.3.2 for all the test structures.

Table 4.4: Space between the lines as a function of line width and etchable area

S_{drawn}	Line Width	A_e	S_{actual} (measured)	ΔS
	0.12	3840	0.086	-0.034
0.12	0.14	4135	-	-
	0.18	4608	0.102	-0.018
	0.12	3178	-	-
0.17	0.18	3950	0.144	-0.026
	0.80	6334	0.183	0.013

(All units are in μm or μm^2 .)

Figure 4.16 demonstrates $S_{actual(model)}$, the space between the lines calculated using the model equation (4.5), and $S_{actual(measured)}$, the measured space between the lines as shown in § 4.3.2, as a function of metal line width.

Figure 4.16 clearly shows that the width of the adjacent metal lines affect the space between them and also that this effect gets more significant as the feature size becomes smaller.

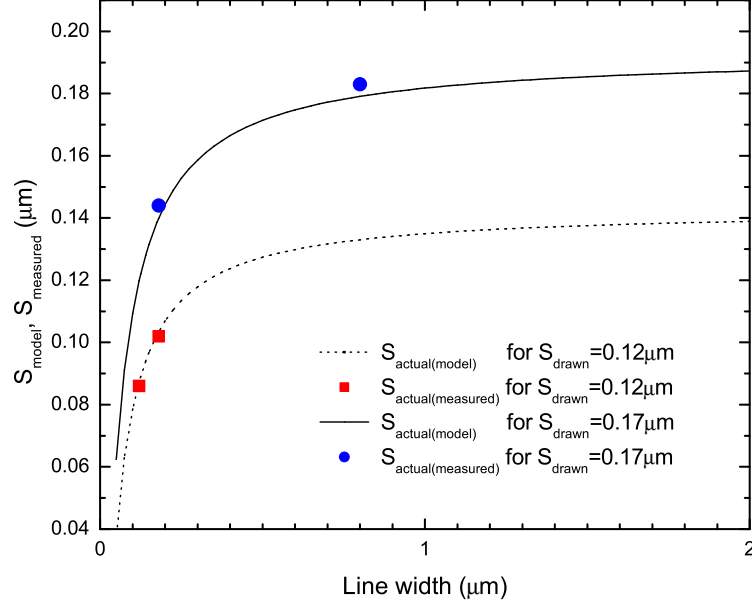


Figure 4.16: Change of the space between the lines as a function of the metal line width.

The space information can then be converted into MTTF data. In E -model, MTTF can be expressed in terms of electric field (E) as follows:

$$MTTF = F' \exp(-G'' E) \quad (4.6)$$

and also

$$\log(MTTF) = F + G' E. \quad (4.7)$$

where F' , F , G'' , and G' are all constants.

Using the relationship $E = \frac{V}{S}$, Eq. (4.7) can be rewritten as follows.

$$\log(MTTF) = F + \frac{G}{S_{actual}} \quad (4.8)$$

where F and G are constants and S is the actual space between the adjacent interconnects. We can use Eqs. (4.3) and (4.5) to convert Eq. (4.8) to a more direct relationship between $\log(MTTF)$ and metal line width, W .

By plugging Eq. (4.3) to Eq. (4.8), we get

$$\begin{aligned}
\log(MTTF) &= F + \frac{G}{S_{actual}} \\
&= F + \frac{G}{S_{drawn} + \Delta S} \\
&= F + \frac{G}{S_{drawn} + L_o + \frac{\alpha}{1 + BA_e}}
\end{aligned} \tag{4.9}$$

Etchable area, A_e , can be expressed as follows:

$$\begin{aligned}
A_e &= L_h W N \\
&= L_h W \frac{L_v}{W + S_{drawn}}
\end{aligned} \tag{4.10}$$

where L_h , L_v , W , and N are horizontal and vertical dimensions of the entire test structure, and the metal line width, and the number of the slots to be etched away respectively.

Plugging Eq. (4.10) into Eq. (4.9), we get

$$\begin{aligned}
\log(MTTF) &= F + \frac{G}{S_{drawn} + L_o + \frac{\alpha}{1 + BL_h W \frac{L_v}{W + S_{drawn}}}} \\
&= F + \frac{G(W + S_{drawn} + BL_h L_v W)}{(S_{drawn} + L_o)(W + S_{drawn} + BL_h L_v W) + \alpha(W + S_{drawn})} \\
&= F + \frac{G[W(1 + BL_h L_v) + S_{drawn}]}{W[(S_{drawn} + L_o)(1 + BL_h L_v) + \alpha] + S_{drawn}(S_{drawn} + L_o + \alpha)}
\end{aligned} \tag{4.11}$$

Using Eq. (4.11), we can now clearly see the impact of metal line width on the reliability of a test structure (MTTF). Figures 4.17 and 4.18 demonstrate the relationship between MTTF and the metal line width graphically. From these figures, we can see that the measurement data agrees well with the calculation using the model.

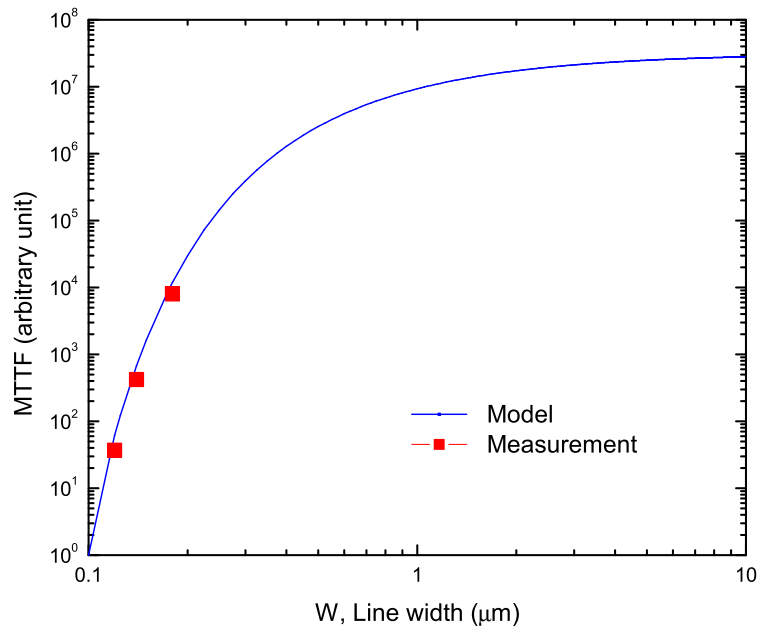


Figure 4.17: MTTF change of the test structures as a function of the metal line width, W , for $S_{drawn} = 0.12\mu\text{m}$ case.

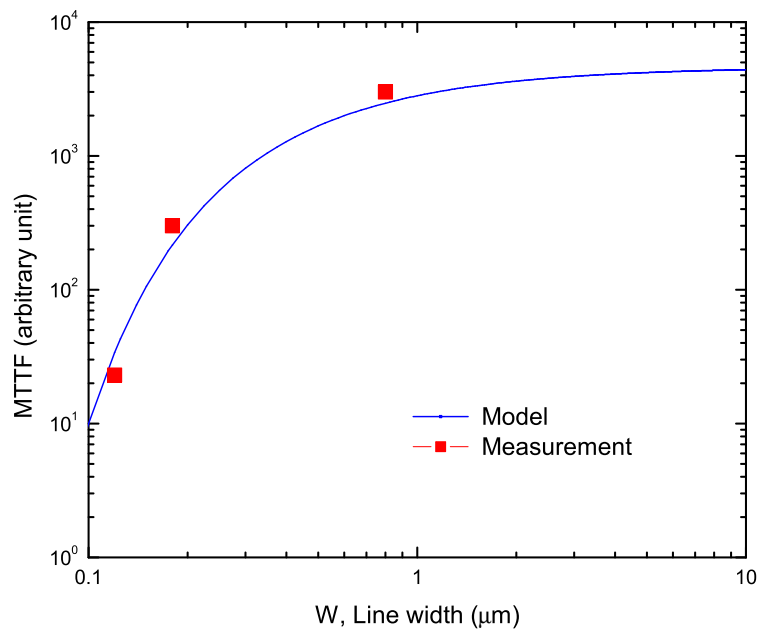


Figure 4.18: MTTF change of the test structures as a function of the metal line width, W , for $S_{drawn} = 0.17\mu\text{m}$ case.

4.5 Discussion

The relationship between the width of adjacent metal lines and the space between them was discussed above. Beginning from the observation that the dielectric layer between wider metal lines has significantly better reliability compared to the one between narrower metal lines, we suggested several feasible physical mechanisms that can explain the root cause for the observation. The mechanisms discussed in this research include enhanced electric field effect, optical proximity effect and etch micro-loading effect.

Among these, the etch micro-loading effect provided most probable explanation for the observation considering the degree and direction of the impact on the dielectric reliability. A mathematical model was suggested to enable a quantitative application of the newly developed theory.

CHAPTER 5

BACK-END RELIABILITY CONCERNS FROM POROUS DIELECTRICS

5.1 Background

5.1.1 Thrust for Ultralow- k Dielectrics

Interconnect delay has become an increasingly large portion of the entire signal propagation delay as the devices are scaled down. The parasitics in the back-end start to dominate and overwhelm the benefit of improved front-end transistor performance from the smaller feature size at the technology nodes of $0.18\mu\text{m}$ and beyond. Interconnect delay has two components: Interconnect resistance (R) and dielectric capacitance (C). Low dielectric constant (k) materials have been introduced as a solution for reducing RC delay for advanced technology nodes.

Many schemes have been developed to lower the dielectric constant of the intermetal dielectric (IMD) and these can be categorized into two groups. One is to decrease the polarization by using materials with less polar bonds and the other is to decrease the density of the material by introducing porosity. The example for the first kind includes certain low- k materials, where some of the Si-O bonds in silica have been replaced with less polar bonds such as Si-F or Si-C. A more fundamental reduction can be achieved by using virtually all non-polar bonds, such as C-C or C-H, for example, in materials like organic polymers [3]. Table 5.1 shows some low- k materials along with their typical dielectric constants.

One of the ways to obtain a low dielectric constant is fluorination of either inorganic or organic dielectric materials [54]. However, the low dielectric constant

Table 5.1: Low- k materials*

Material	k	Description
CVD-SiO ₂	4.2	
Thermal SiO ₂	3.9	
FSG	3.2 ~ 3.6	Fluorinated Silicated Glass
Polyimides	3.0 ~ 3.5	
HSQ	2.8 ~ 3.0	Hydrogen Silsesquioxane
MSQ	~ 2.7	Methyl Silsesquioxane
SiOC	2.7 ~ 2.9	OSG (Organo Silicated Glass)
BCB	~ 2.6	Benzocyclobutene
Parylene	2.2 ~ 2.6	
a-C:F	2.1 ~ 2.5	Fluorinated Amorphous Carbon
Porous Materials	< 2.0	k value depends on porosity and $k < 2.0$ typical with porosity > 50%

* Modified from [53].

available for fluorinated dense materials is around $k = 1.9$ and none of the current approaches using dense materials is expected to achieve a k value lower than that. Despite their initial hydrophobic nature, porous low- k materials are easily hydrophilized due to plasma damage in different processing steps, which makes these materials extremely susceptible to moisture absorption. The combination of plasma damage and moisture absorption leads to an increase of both the k -value and the leakage current in low- k materials.

5.1.2 Porous Low- k Materials

Because there is a limit in lowering the dielectric constant by manipulating the polarizability of the bonds, it seems inevitable to reduce the material density to achieve even lower dielectric constants as required by the International Technology Roadmap for Semiconductors [4]. The point in the idea of reducing material density is to remove any source of polarization.

A certain material can be polarized in one or more of the three ways: electronic,

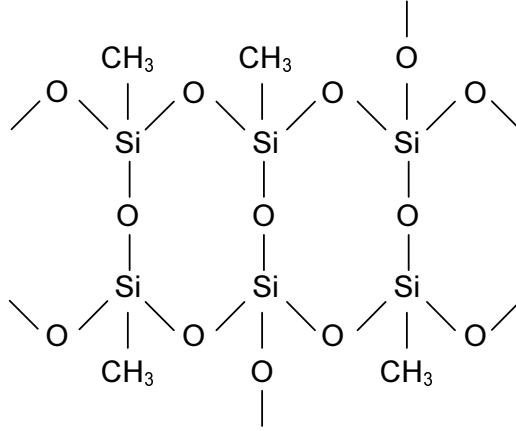


Figure 5.1: Molecular structure of MSQ (methyl silsesquioxane).

distortion, or orientation polarization. Electronic polarization is due to the displacement of electrons in the atomic structure, and displacement of ions is responsible for distortion polarization, while orientation polarization is caused by rearrangement of molecules in the direction of the applied electric field. Therefore, by reducing material density or removing part of the material, the overall polarization will be decreased accordingly, resulting in a lower dielectric constant. The ultimate goal in this case will be to replace the entire dielectric with air whose k value is the lowest possible, that is 1.

This scheme is not entirely new because, even in the early stage of low- k material development, it was used to achieve a lower dielectric constant. The idea of lowering the density of a material in the early days was implemented by replacing atoms with larger molecules, as shown in Fig. 5.1. In MSQ, it is shown that the oxygen atoms are replaced by a methyl group to create less-densely packed material, and this leads to a material with a lower dielectric constant.

The density of a material can be more effectively decreased by increasing the free volume through introducing porosity constitutively or subtractively. Constitutive porosity refers to the self-organization of a material. The porosity is relatively low (usually less than 15%), and pore sizes are about 10\AA in diameter [3]. Subtractive

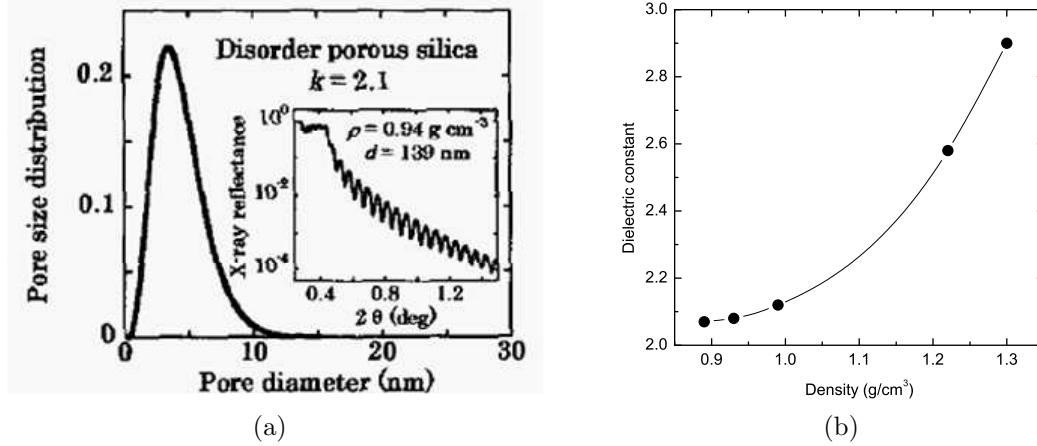


Figure 5.2: (a) A typical distribution of pore size in a porous silica film. (b) A plot showing the dielectric constant as a function of material density.

porosity is formed through selective removal of part of the material. This can be achieved via an intentionally added ingredient called a porogen or by selective removal of particular kind of bond by etching. Porogen is a thermally degradable substance which is removed by an anneal to leave pores behind. Subtractive porosity can be as high as 90%, and pore sizes vary from 2 nm to tens of nanometers [3]. Figure 5.2 shows the distribution of the pore size in typical porous low- k dielectrics.

The definition of a pore is any localized region in the silica matrix (may be a few or several angstroms in size) that contains low polarizability material, and, in fact, may be a microvoid. Such materials will be referred to as being “porous” even though a material may/may not actually be in the pore [14].

The dielectric constant of a porous material can be computed using the Clausius-Mossotti equation shown below.

$$\frac{k_{eff} - 1}{k_{eff} + 2} = \frac{4\pi}{3} \sum_i N_i \alpha_i = f_1 \frac{k_1 - 1}{k_1 + 2} + f_2 \frac{k_2 - 1}{k_2 + 2} \quad (5.1)$$

where N_i the number of molecules per unit volume of type “i” in the dielectric and α_i is the molecular polarizability. Here, f_1 and $f_2 = 1 - f_1$ are the volume fractions of the two components with dielectric constants k_1 and k_2 , respectively.

Table 5.2: Thermal conductivities of several low- k thin-film samples*

Material	K_{th} (W/m°C)
non-porous TEOS	1.260
Xerogel 48% porous	0.250
63%	0.157
70%	0.108
77%	0.065

* Modified from [53].

5.1.3 Reliability Issues of Porous Low- k 's

Even though low- k dielectrics can be a promising solution for advancing device performance, their effect on reliability can be detrimental if not addressed properly. Materials used as low- k IMD are inherently leaky and have several well-known problems like low mechanical strength, poor thermal conductivity, and moisture absorption, which all can affect device reliability negatively [55, 56]. If the porosity is introduced into this already-poor material, the electrical and structural properties are expected to become even worse.

Porosity in the film can result in degradation of mechanical strength and promote chemical absorption if the pores have an open connection to the surface. Absorbed chemicals can also degrade electrical properties and cause mechanical properties to worsen. Contamination found in patterned low- k films can originate from the etch, ash and cleaning processes used to structure the low- k dielectric stack. Photoresist poisoning in the via first integration scheme caused by trapped ammonia formed during an N_2/H_2 ash is an example of one such issue [57]. The poor thermal conductivity of porous low- k materials is also well known and can be clearly seen in Table 5.2.

TDDDB reliability of damascene structures has to be assessed as a system of a dielectric, diffusion barrier, and copper interconnects [58]. This becomes mandatory

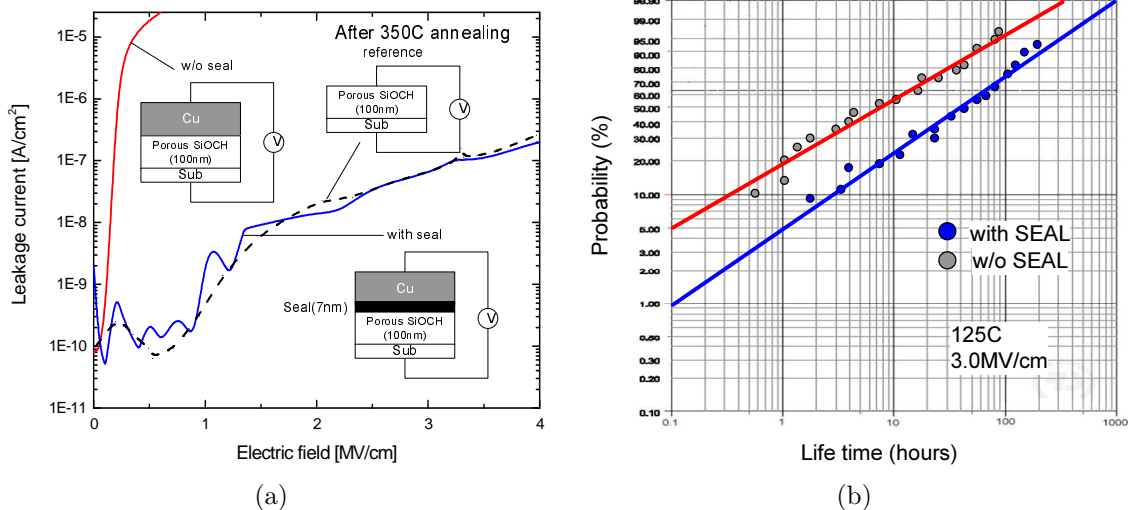


Figure 5.3: (a) Current-voltage plot from various test structures showing the impact of the absence of a pore sealing layer. (b) Weibull plots showing the lifetime distributions of test structures with and without a pore sealing layer.

when porous low- k materials are considered, since barrier integrity is a key contributor to TDDB behavior. According to the International Technology Roadmap for Semiconductors, the use of ultra low- k materials with a copper barrier thickness of 5nm is required for the 45nm node. Barrier deposition onto porous substrates is extremely challenging. Especially the surface porosity of a porous film is one of the critical problems, which causes gas-absorption, metal-diffusion and discontinuity of the barrier metal [59]. When open pores are exposed during metal barrier deposition, the barrier dielectric interface is not well defined.

Abrupt changes of the time to dielectric breakdown and the flat-band voltage shift were observed when the porosity of the low- k material was between 20 and 30% [60]. Such a characteristic agrees with the positronium annihilation lifetime spectroscopy (PALS) data, which indicates that the interconnectibility of the pores abruptly increases when the porosity is between 20 and 30%. Figure 5.3 clearly shows the impact of pore sealing on reliability.

High porosity dielectrics may need the use of conformal metallic barrier deposition methods like CVD or ALD. One of the key issues for integration of such materials

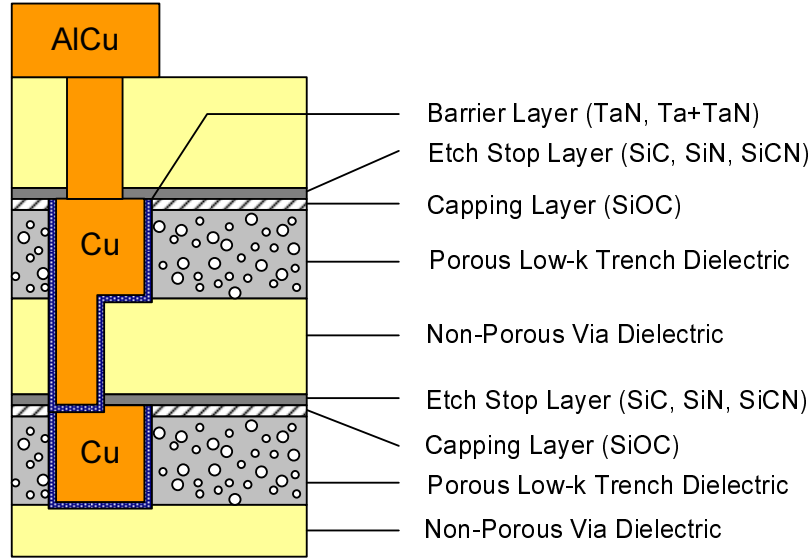


Figure 5.4: A typical vertical structure using a porous low- k dielectric formed by a dual damascene process.

comes from the tendency for a precursor to diffuse through the porous structure degrading the effective k value. Various pore sealing techniques were already investigated and reported, and they can be categorized into two groups. One group of pore sealing techniques is to use plasma treatment. N_2 , N_2 - H_2 , He and N_2O plasmas were reported to be effective in pore sealing. The other group of techniques is to use a thin dielectric liner such as SiO_2 , Si_3N_4 , or SiC before the metallic diffusion barrier deposition. This thin dielectric barrier covers the surface pores and prevents the diffusion of metallic barrier precursors into the porous dielectric [61].

Low damage damascene fabrication of low- k ILDs is also a key for reliable Cu/low- k integration. Among fabrication processes of low- k ILDs, resist ashing has been most critical. A dual hard-mask process has been developed to prevent porous low- k ILDs from exposure to plasma damage, as is shown in Fig. 5.4 [62].

Ogawa et al have reported a Monte Carlo simulation result of porous dielectric breakdown [14]. The result is quoted in Figs. 5.5 and 5.6. In Fig. 5.5, the defect generation processes were compared between non-porous and porous dielectrics. It is shown that the porosity clearly helps the breakdown process. It is more precisely

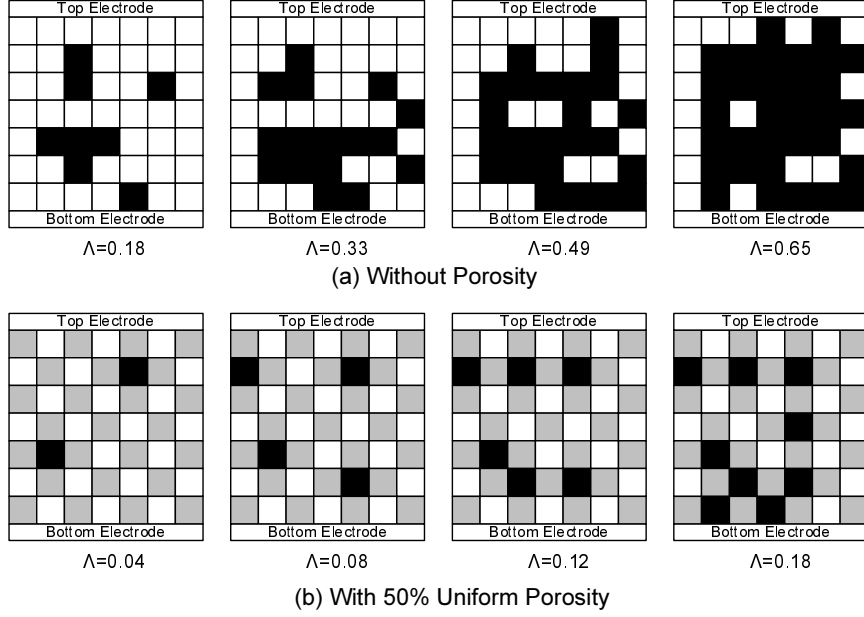


Figure 5.5: Graphical descriptions of Monte Carlo simulation results for defect generation (a) without porosity, and (b) with 50% uniform porosity. Gray-colored cells represent the pores or free volumes while the black ones are the defects that are generated as a function of time (Λ). It is shown that a conducting path composed of the pores and the generated defects is formed much more quickly in porous dielectrics than in non-porous ones. Reproduced from [14].

pointed out in Fig. 5.6 by comparing the TDDB lifetimes for both materials.

Another useful result is shown in Fig. 5.7. The mean lifetime ($t_{63.2}$) is shown to be inversely proportional to the porosity. The flat band shift is also displayed as a function of porosity, which means that the porous dielectrics have a higher level of defects.

In the following, it is demonstrated that the porosity included in low- k dielectrics to achieve ultra-low value of k can cause an unexpected side effect in electric field distribution and intensity making the situation even worse in view of reliability.

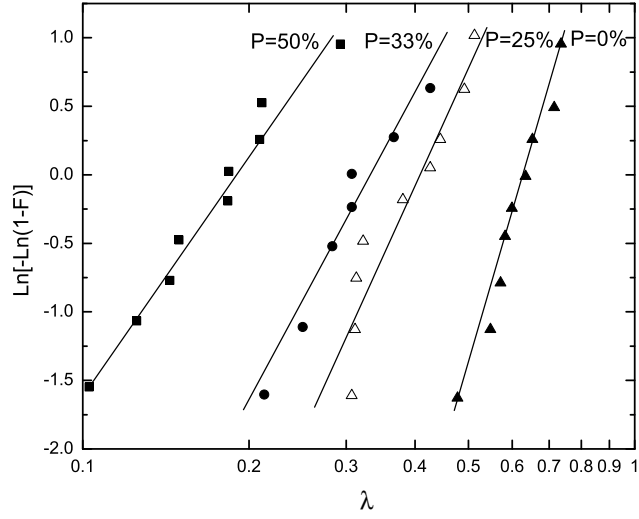


Figure 5.6: Simulated Weibull plot showing the lifetime distributions for dielectrics varying in porosity. Reproduced from [14].

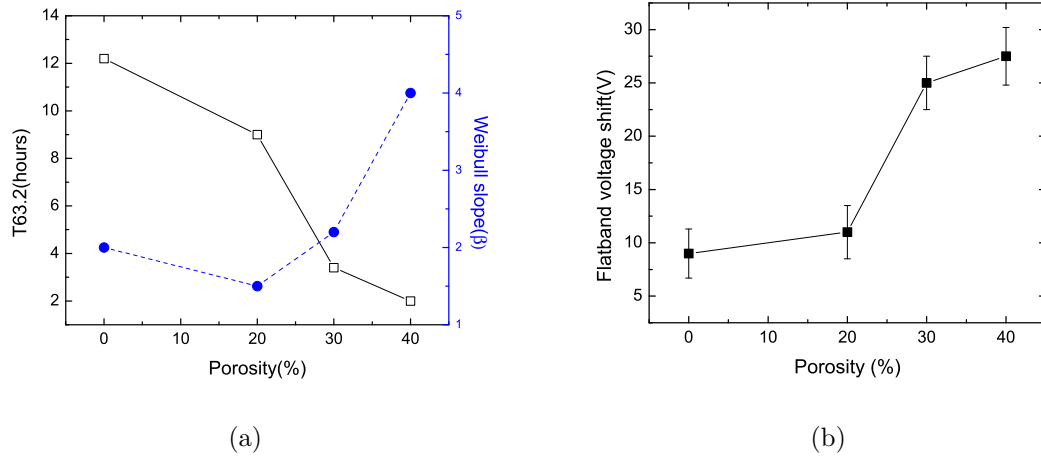


Figure 5.7: Plots showing (a) the mean lifetime and (b) flatband voltage shift as a function of porosity.

5.2 *Electric Field Distribution*

5.2.1 Design of Simulation

To see the effect of porosity on the electric field distribution and intensity in a dielectric film, finite element analysis simulations are performed. The simulation parameters include pore shape, size, permittivity, and interconnectivity. Pores are assumed to have elliptical shape and are modeled with aspect ratios varying from 0.25 to 4. Pore sizes are assumed to be in the range from 1nm to 5nm based on reports from many researchers using various techniques such as positron annihilation lifetime spectroscopy (PALS) [63], gas adsorption, X-ray/Neutron porosimetry [64], or small angle neutron scattering (SANS) [65].

The cases when the pores are filled with substances other than air are accounted for by varying the permittivity of the pores from 1.0 to 7.0. The effect of interconnectivity is also considered. The degree of interconnectivity varies according to the level of porosity. Above a certain level of porosity, interconnected pores are unavoidable [66]. Interconnected pores are most likely to provide a efficient conduction path for drifting charged species

5.2.2 Electric Field Distribution

Contour plots in Fig. 5.8 show what the electric field distributions look like when the pores are introduced into the dielectric matrix. The simulation results in the figure are displayed for the cases with various values of pore permittivity ranging from 1.0 to 7.0, while the dielectric matrix permittivity is fixed at a typical value of $k_{matrix} = 2.5$. Figure 5.8(a) is for the case when the pore is a free volume filled with air ($k = 1$), and the cases when some substances other than air are trapped in the pore are also shown in Figs. 5.8(b)-(f). It is clear that the electric field distribution and intensity is a function of the pore permittivity. When k_{pore} is smaller than k_{matrix} , as the case in Figure 5.8(a), the electric field at the side is enhanced, while the electric field at

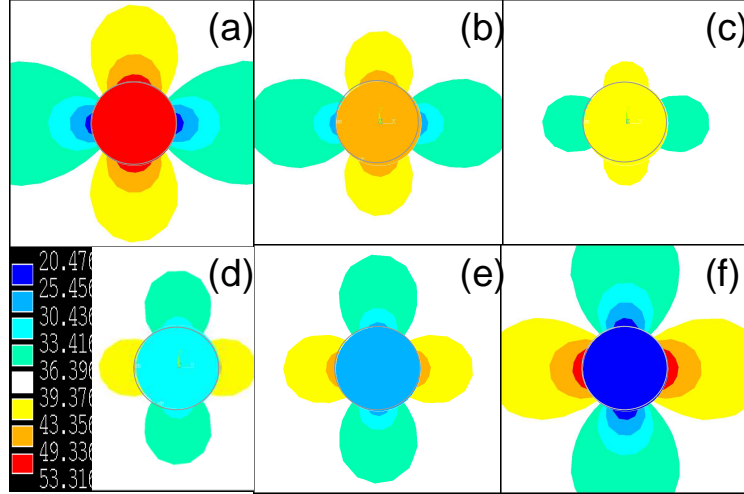


Figure 5.8: Effect of variation of pore permittivity on the electric field distribution and intensity near a pore. Permittivity values for the pores are (a) 1.0, (b) 1.5, (c) 2.0, (d) 3.0, (e) 4.0, (f) 7.0, while the matrix permittivity is fixed at 2.5.

the back and front of the pore is enhanced when k_{pore} is greater than k_{matrix} , as in the case shown in Fig. 5.8(f). The degree of change in the electric field distribution becomes more distinguishable as the permittivity difference between the pore and the matrix becomes greater.

Electric field is in the direction from left to right. In Fig. 5.9, the electric field distributions along several paths around the pore are extracted and displayed for the case shown in Figure 5.8(a) with $k_{pore} = 1$ and $k_{matrix} = 2.5$. It can be seen that the electric field is much stronger inside and near the pore than in the matrix away from the pore. This means that the charged species passing through or by the pore can be accelerated by the enhanced electric field around the pore giving rise to an increased leakage current. Figure 5.10 shows the electric field intensities along path 2 for the pores with various permittivity values. It confirms the fact that the electric field intensity is enhanced when k_{pore} is smaller than k_{matrix} , but is mitigated when k_{pore} is greater than k_{matrix} . In other words, the worst-case situation happens when the pore is a free volume filled with air, which is the case with porous ultra-low- k dielectrics.

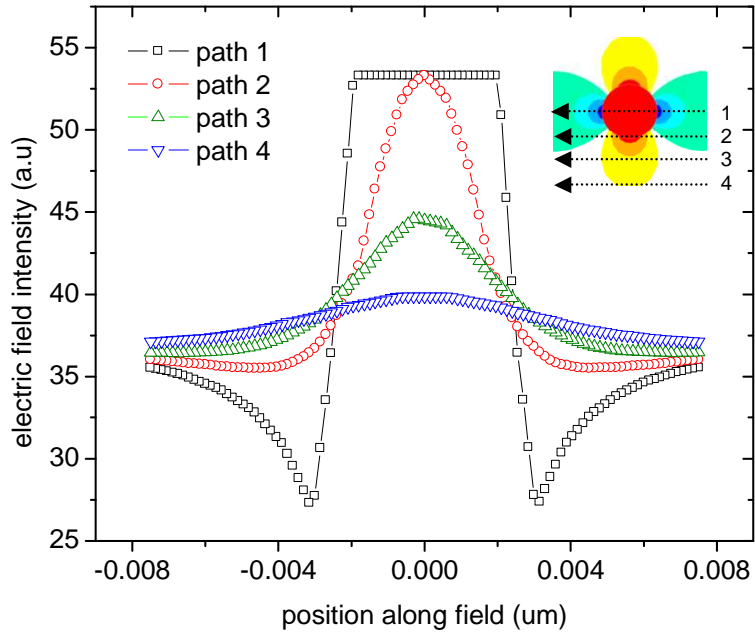


Figure 5.9: Path plot of the electric field intensity along several paths, 1 to 4 for the case with $k_{pore} = 1$ and $k_{matrix} = 2.5$. The direction of the electric field is the same as the arrows shown.

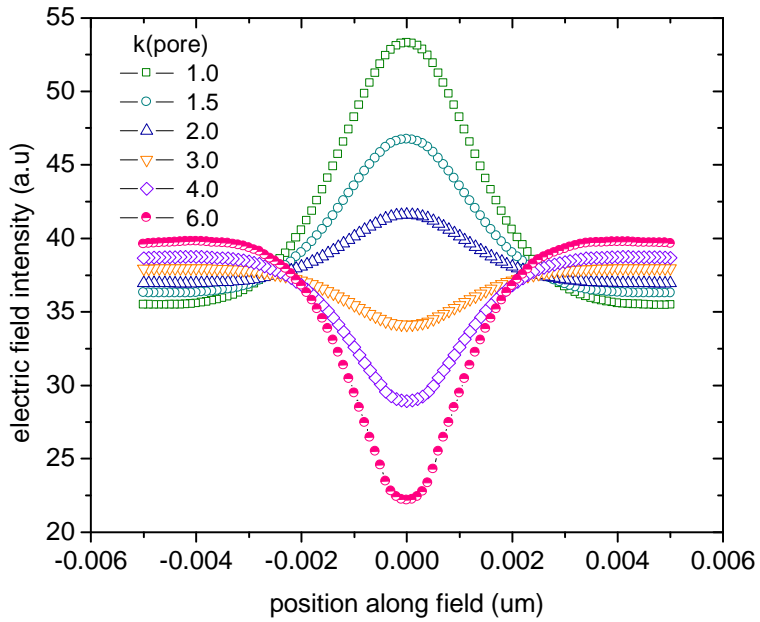


Figure 5.10: Electric field intensities along path 2 (see Fig. 5.9) for the pores with various permittivity values. $k_{matrix} = 2.5$.

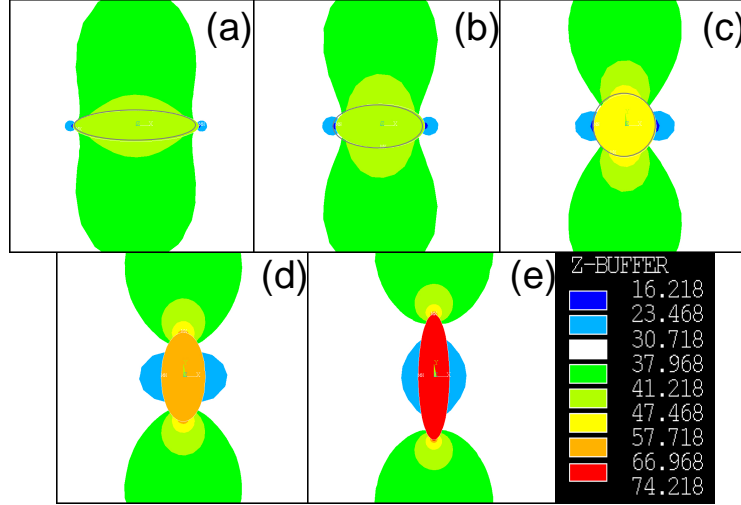


Figure 5.11: Effect of pore shape on the electric field distribution and intensity near the pore. The aspect ratios are (a) 0.25, (b) 0.5, (c) 1.0, (d) 2.0, (e) 4.0. $k_{pore} = 1$ and $k_{matrix} = 2.5$. The electric field is in the direction from left to right.

The electric field distribution as a function of pore shape is illustrated in Fig. 5.11 for the case with $k_{pore} = 1$ and $k_{matrix} = 2.5$. From this result, it is clear that the pore shape has an impact on the electric field distribution and intensity. As the long axis of the elliptical pore is aligned in the direction perpendicular to the electric field, the maximum electric field intensity around the pores becomes stronger. The maximum electric field intensities around the pores are plotted as a function of pore aspect ratio in Fig. 5.12. Also, it can be noticed that the pore size variation has little or no effect on the maximum electric field.

One possible scenario for a porous ultra-low- k dielectric with a certain level of porosity and interconnectivity is described in Fig. 5.13. It is clear that the network of interconnected pores can form a path with highly enhanced electric field that can provide a very effective conduction route for drifting charged species leading to enhanced dielectric breakdown.

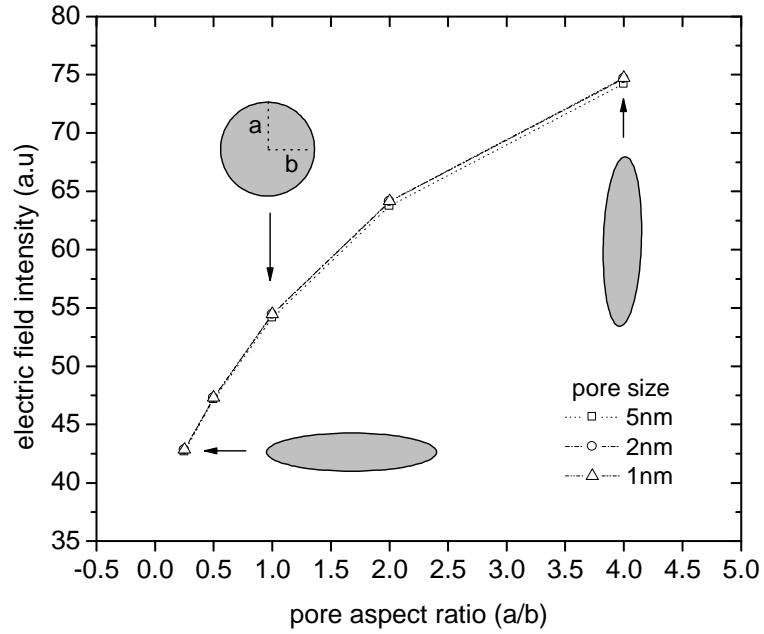


Figure 5.12: Comparison of maximum electric fields as a function of pore shape (aspect ratio = a/b). The electric field is in the direction parallel to the x-axis.

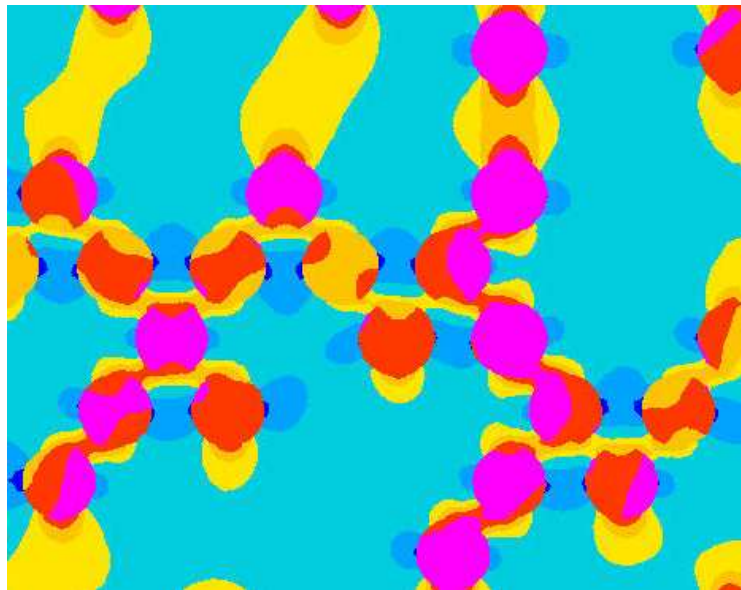


Figure 5.13: High electric field path formed by the network of interconnected pores in the IMD. $k_{pore} = 1$ and $k_{matrix} = 2.5$. The electric field is in the direction from left to right.

5.3 Monte Carlo Study of Charge Transport in Porous Dielectrics

5.3.1 Design of Simulation

It is demonstrated that the charge transport in the porous dielectric is indeed accelerated by the presence of pores and the enhanced electric field by the pores. Charge transport in the porous dielectric is simulated using the Monte Carlo technique. The free volumes or pores are assumed to be evenly distributed throughout a dielectric film. A packet of charged particles is injected into the dielectric film. The trajectory is determined by a stochastic algorithm with several model parameters. The next move of a particle is determined based on the information about the current position.

As shown in Fig. 5.14, the electric field acts against the thermodynamic energy barrier against transition to the next available state. Hopping is basically a tunneling process between two trap sites in close proximity separated by the energy barrier. A lower energy barrier means that a particle can hop from one trap site to another more easily, which, in turn, means a higher hopping frequency and shorter residence time at a trap. Electric field intensity is also assumed to affect the anisotropy of the particle trajectory. The anisotropy is modeled with the Henyey-Greenstein scattering function. The results are displayed in a time-resolved manner showing the positional distribution of a particle packet at several time points.

5.3.2 Simulation Result

The results from the time-resolved Monte Carlo simulation for charge transport are shown in Figs. 5.15 and 5.16. Figure 5.15 shows the positional distribution of particles at several time points for varying porosity levels. After injected into the dielectric, each particle is modeled to take the next move based on the information about current position. The stochastic parameters employed in determining the particles' move are the time spent at a trap site before hopping to the next one and the anisotropy of

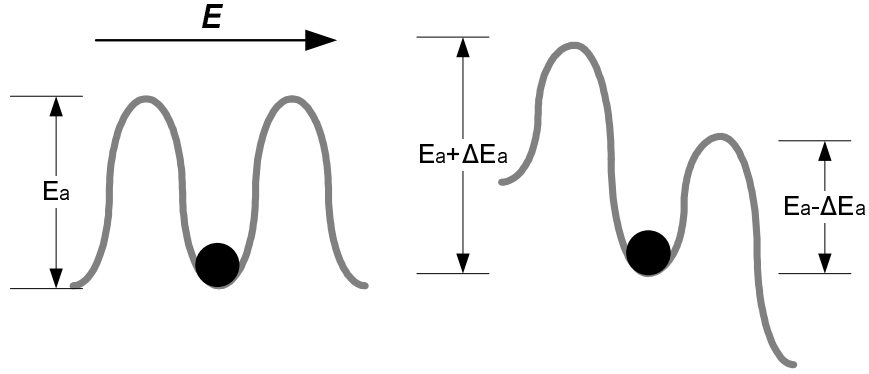


Figure 5.14: Energy barrier diagram before and after the electric field is applied. With the electric field applied, the chance to move in the direction against the field decreases exponentially, while the probability of moving along the field increases exponentially.

the transitional course.

It is shown that the particles travel across the dielectric faster in the presence of pores compared to in conventional non-porous dielectrics. It is also shown that the higher the porosity level is, the faster the particles move across the dielectric.

The electric current usually denotes the electric charges flowing through a medium in a unit period of time as expressed in the following formula.

$$I = \frac{Q}{t} \quad (5.2)$$

where I is the current, Q is the amount of charges and t is time. If we use the average transit time for each level of porosity as t in Equation 5.2, we can appreciate the impact of porosity on the leakage current level. The higher the porosity, the shorter the average transit time, which leads to the higher level of leakage current.

This result suggests that the porosity facilitates the conduction process, and thus enhances the breakdown mechanism leading to poor dielectric reliability.

Figure 5.16 recounts the effect of porosity by comparing the average travel time for a packet of particles across a dielectric film for several levels of porosity. The same result as shown in Fig. 5.15 is corroborated. In this figure, the effect of t_{trap} , the time spent at a trap, is also shown.

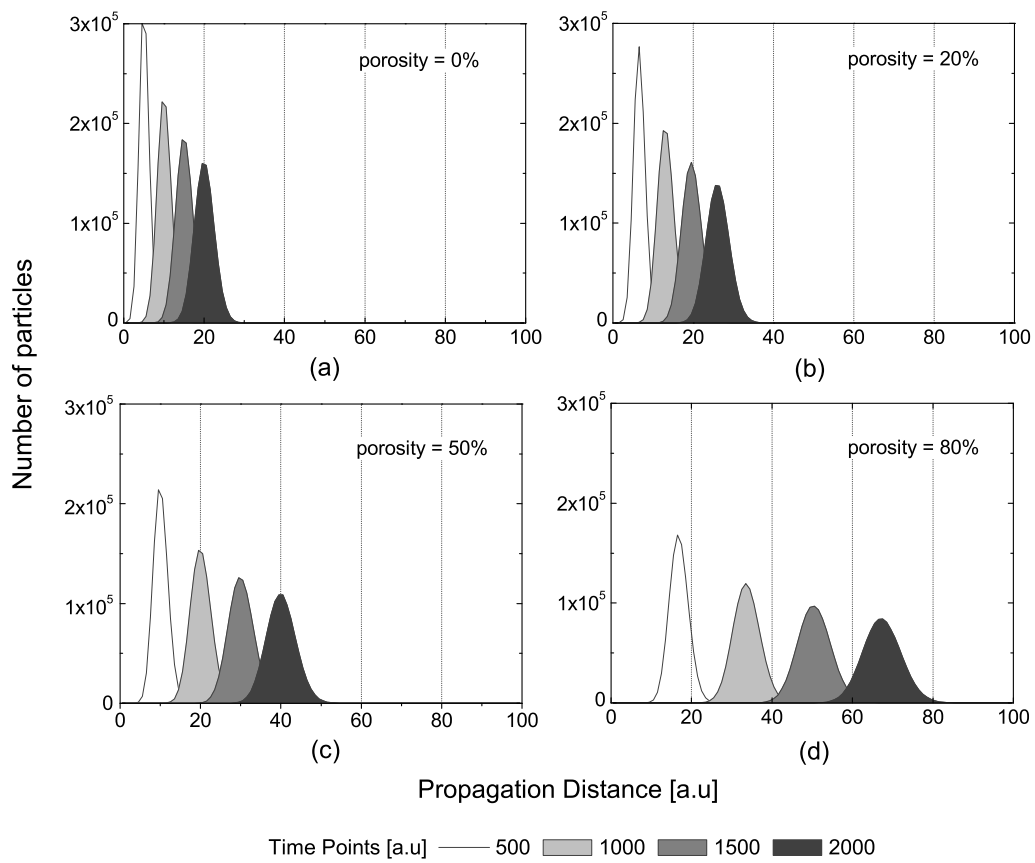


Figure 5.15: Time-resolved Monte Carlo simulation result showing the positional distribution of particles injected into the dielectric moving along the direction of the electric field at several time points.

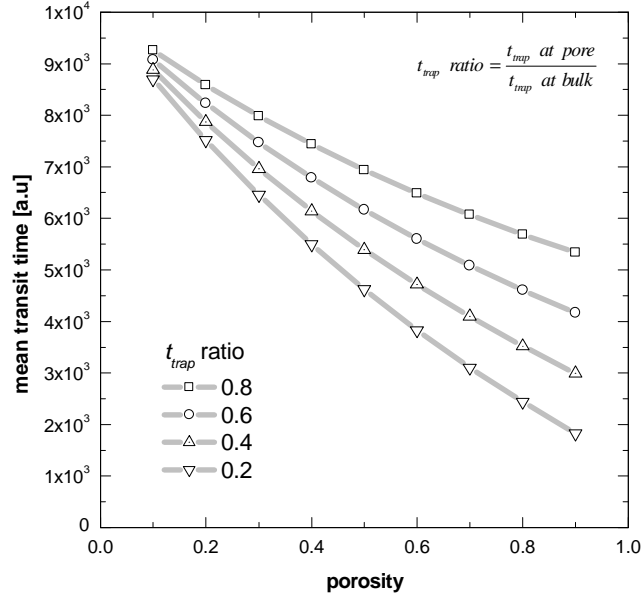


Figure 5.16: Time-resolved Monte Carlo simulation result showing the average transit time for the particles to cross the dielectric. The result is displayed as a function of variation in t_{trap} ratio, which is the ratio of t_{trap} at the pore site to t_{trap} at the bulk site.

5.4 Summary

The effect of porosity inclusion in the dielectrics to achieve a lower dielectric constant for advanced technology nodes has been considered in view of electric field. The porosity in the dielectrics has been shown to modify the electric field distribution and intensity. The degree and direction of change depend on several parameters such as pore shape, and permittivity. The analyses have also shown that the presence of interconnected or proximity pores can act against reliability by enhancing the drift of charged species like ions and electrons through providing paths with higher electric field than in the matrix. This leads to the conclusion that the porous dielectrics can show poorer insulating properties than the non-porous counterparts, let alone the effects from other known problems like barrier integrity and pore poisoning.

CHAPTER 6

CONCLUSIONS

6.1 Summary of Results

6.1.1 Reliability-Area Modeling

The reliability-area relation was formulated based on two assumptions about the defect distribution: a Poisson distribution and a negative binomial distribution. The negative binomial assumption gives a more realistic description for the defect distribution in actual circuits. Experimental result corroborated the validity of this model.

6.1.2 Layout Characterization

Physical design factors were analyzed for the purpose of reliability characterization during design. The factors include layout geometry and interconnect pattern density. As for the layout geometry, the analysis is based on a series of simulations of the electric field, accounting for lithography. It was confirmed that layout geometry changes cause electric field variation, and in some cases the increase in the peak electric field is strong enough to lead to localized dielectric breakdown at a singular point.

As for the interconnect pattern density, simulation and experimental methods were employed. Several feasible reasons were suggested through simulations and corroborated by physical analysis. It is conjectured that the etch micro-loading effect is the biggest factor that is causing the lifetime difference of the dielectrics between the metal lines with different widths.

6.1.3 Monte Carlo Modeling of Dielectric Breakdown

To understand the impact of porosity in the inter-metal dielectric on the reliability of dielectrics, simulation studies were performed. First, electric field simulation revealed that the electric field distribution around the pores is distinguishably disturbed by the presence of pores. Next, this electric field simulation result was fed into a Monte Carlo simulator to yield information about the charge transport in dielectrics.

The result from the Monte Carlo simulation for charge transport led to the conclusion that charge carrier transport is enhanced by the porosity in dielectrics. The meaning of the result is that porous dielectrics that are used to improve the circuit performance can affect circuit reliability negatively by enhancing the breakdown mechanisms.

6.2 *Future Work*

6.2.1 Experimental Model Verification

In the derivation, it was assumed that the clustering parameter is constant. Although this is a reasonable assumption to avoid mathematical difficulties, it is also known that the degree of clustering varies from wafer to wafer. To build a more inclusive model, the effect of the variable clustering parameter has to be further investigated.

Another issue regarding the experimental verification of the back-end dielectric breakdown model derived in Chapter 2 is how much the layout geometry factor will affect the result. There are two different schemes for multiplying test structure area when designing large area test structures. One is the continuous extension method, and the other is the repeated segments method. The difference is in that the continuously extended comb structures are multiplying only the area between parallel comb fingers while the repeated segments comb structures are multiplying the number of the terminations at the line-ends as well. This can make a fundamental difference in the test results if the electric field is enhanced by some sensitive layout geometries

such as line terminations in this case, as demonstrated in Chapter 3.

6.2.2 Layout Characterization

As shown in Chapter 3, some specific layout geometries can be the origin of the highly enhanced electric fields and can give rise to the possibility of premature breakdown in some specific parts of a device. However, as also was pointed out earlier, the actual geometries on the fabricated chips are a strong function of lithographic factors, such as the optical proximity effect, lens aberrations, and details of the lithography tool set. Also, the use of optical proximity correction (OPC) algorithms can affect the actual patterns implemented on chip.

With actual lithographic factors affecting the printed patterns, the electric field enhancement effect demonstrated in Chapter 3 can either be very significant or hardly noticeable. To see this, it is desirable to use lithographic simulations and use the resulting geometries in the electric field calculations. A wide variety of parameter combinations should be tested for this purpose.

The physical origin of reliability variation as a function of metal pattern density should be determined rigorously. Lithographic simulations should incorporate all feasible optical parameters and aberrations to see all possible scenarios that can result in reliability variation. Also, the effect of vias on inter-metal dielectric reliability should be further studied to find out the root cause of reliability variation. A sound understanding about the cause of the reliability variation from these physical layout factors will help us to design more wisely for circuit reliability.

6.2.3 Impact of Vias on Back-end Dielectric Reliability

Usually the vias are recognized as the weakest link for interconnect reliability. Vias act as a flux divergence point in electromigration because the flux of electron-wind-blown atoms are blocked by the presence of the diffusion barrier at the via bottom.

Vias can also be considered in view of the inter-metal dielectric reliability. Kim

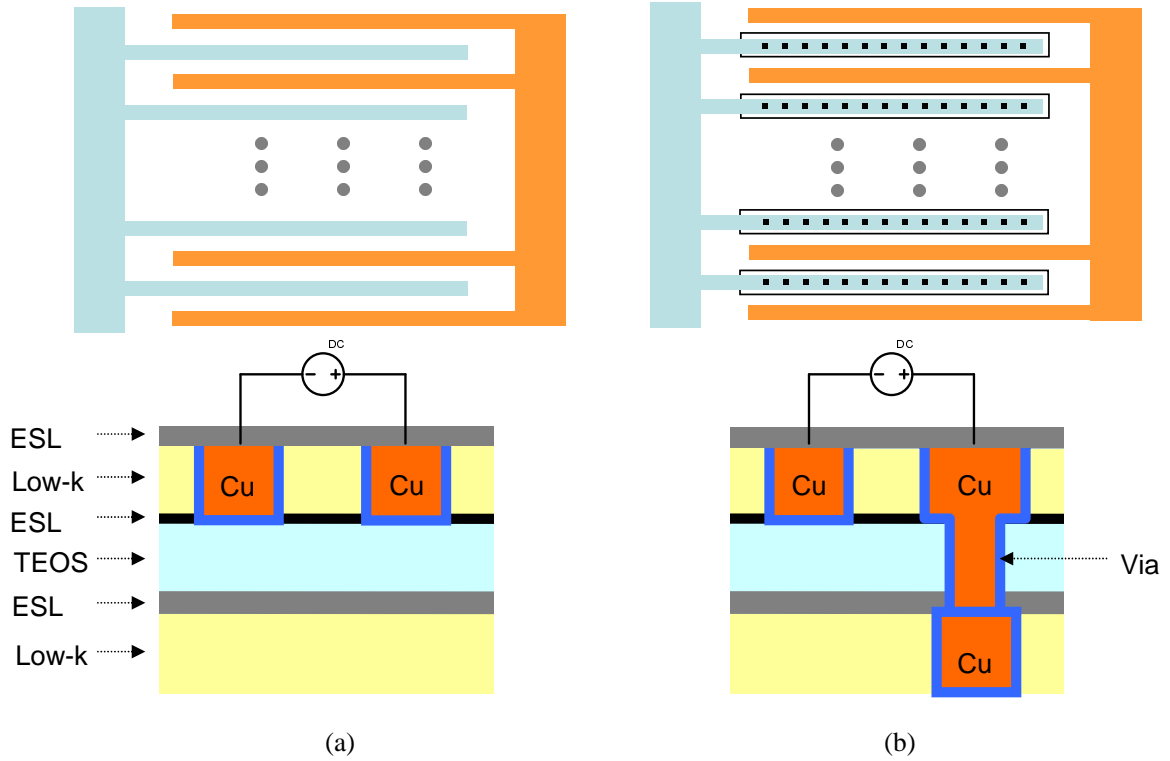


Figure 6.1: Diagrams showing the test structures (a) without and (b) with vias. Two upper figures are top views and the lower ones are the vertical architectures.

et al have reported an interesting result regarding leakage and breakdown characteristics of low- k dielectrics in a dual damascene Cu process with a via-incorporated interconnect structure scaled to the $0.13 \mu\text{m}$ design rule [47, 67]. It was shown that the vias may play a key role in dielectric reliability.

It has been reported that the back-end structures including vias do exhibit a noticeably degraded reliability characteristics using experimental method [67]. This was confirmed by the author using comb test structures including vias as shown in Fig. 6.1. The test structures were subjected to the bias temperature stress test at 150°C and 3.8 MV/cm test conditions.

Figure 6.2 shows the lifetime distributions of the two test structures shown in Fig. 6.1. As can be clearly seen in the figure, the mean lifetime of the test structures with vias shows a big difference compared with the mean lifetime of the test structure without vias.

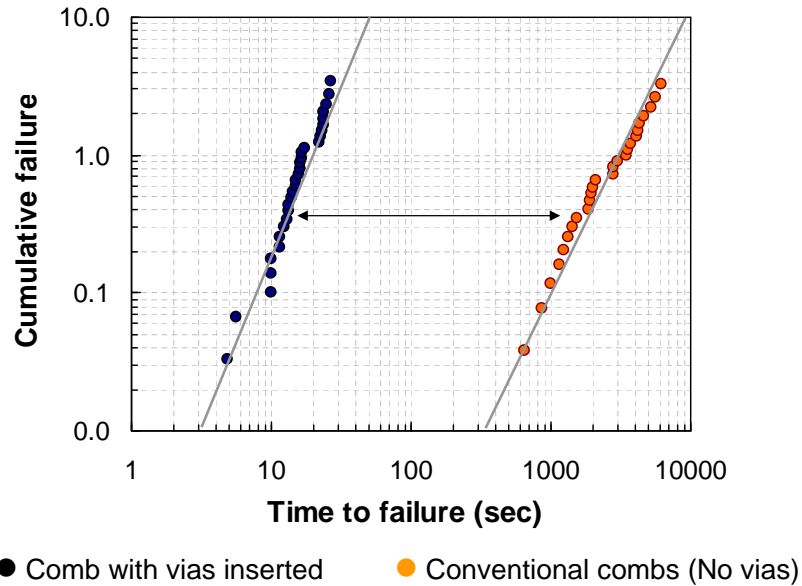


Figure 6.2: Weibull plots showing the lifetime distributions of combs with vias and conventional combs (no vias).

Therefore the impact of vias on inter-metal dielectric reliability has to be further researched in the design-for-reliability point of view.

6.2.4 Integrated Reliability Prediction Tool Development

When all the major physical design factors are identified and evaluated for their impact on reliability, it is possible to make an integrated tool for prediction of reliability at the design stage. Figure 6.3 demonstrates the concept.

Once all the factors are considered, the only work remaining will be putting them together in an integrated software format and making it more efficient in terms of time and effort.

6.3 Concluding Remarks

The purpose of this research is to enable the prediction of circuit reliability at the design stage without depending on test methods using fabricated chips. The major components for the methodology were identified and evaluated in terms of their impact on circuit reliability through simulations and/or experiments. The significance

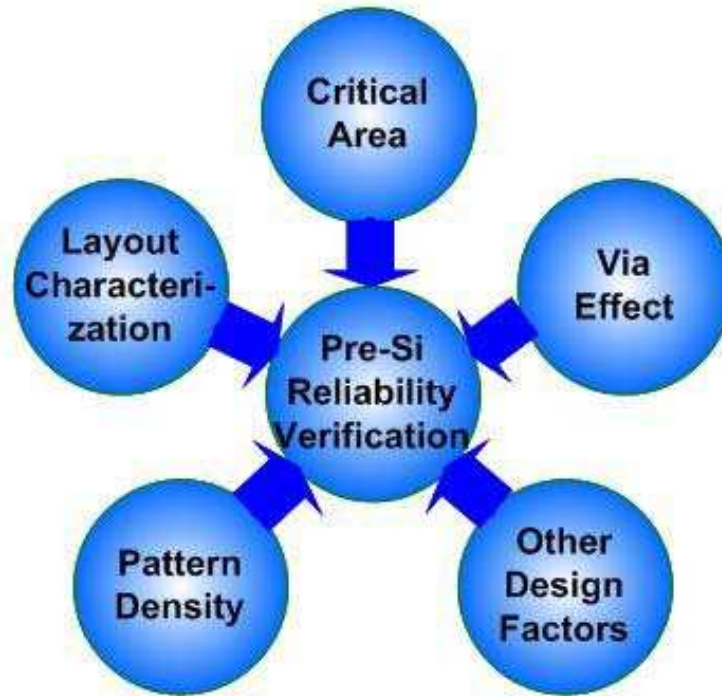


Figure 6.3: Conceptual diagram demonstrating design for reliability.

of this research is to make the reliability evaluation process more efficient in terms of time and resources.

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