

**UNDERSTANDING THE DYNAMIC OPERATION LIMITS AND RELIABILITY
OF HIGHLY-SCALED SILICON GERMANIUM HETEROJUNCTION BIPOLAR
TRANSISTORS**

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TRANSISTORS**

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To my friends and family,
Thank you for your never-ending support.

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SUMMARY

The objective of this work is to expand upon understood reliability effects in silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) and bridge the gap between a device-level understanding of reliability and system-level performance of circuits using HBTs. The aim is to better understand the safe limits of transistor biasing and investigate dynamic, transient swings past the traditional DC-defined safe operating area (SOA) of the transistor.

Chapter 1 describes the need for understanding the reliability physics of SiGe HBTs. This chapter will describe how the device SOA is measured and defined and will briefly discuss the physical mechanisms at the limit of transistor operation, including avalanche multiplication, thermal runaway, and base current reversal. This chapter will also briefly discuss the design of an additional, medium breakdown (MB) transistor profile which allows for a designer to include aggressively scaled high speed HBTs with a higher breakdown transistor in the same technology platform.

Chapter 2 discusses the common damage mechanisms at play in SiGe HBTs, namely mixed-mode (MM) and high-current (HC). These two damage mechanisms occur at the outer limits of the device SOA, and understanding of these mechanisms is critical to understand how to maximize the potential of SiGe HBTs by operating at the edge of the device limits. Understanding damage mechanisms will also enable designers to consider the intended lifetime of the circuit to ensure the system meets specifications across the entire target lifetime.

Chapter 3 uses pulsed-voltage measurements to investigate the dynamic breakdown of SiGe HBTs under high field. As a high voltage is applied to the collector of the device, self-heating within the transistor activates a positive feedback mechanism between device temperature, collector current, and power consumed, resulting in an uncontrollable thermal runaway. Measurements are performed by using pulsed voltage in conjunction with an

emitter ballast resistor to reduce the effect of self-heating on the transistor. Results show that as self-heating is reduced, the maximum voltage limit of the device increases, and breakdown switches from being thermally dominated to impact-ionization dominated. This is significant because high-speed RF and mmWave signals switch at faster speeds than the device self-heating, and thus at high frequency, the dominant breakdown mechanism may be different from the conventional DC-defined SOA. The data and analysis presented in Chapter 3 has been published and presented at the 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium [1].

Chapter 4 compares the performance and reliability tradeoffs of cascode amplifier cells designed using different transistor profiles. Test structures were created using the medium breakdown (MB) and high performance (HP) variants of an advanced SiGe HBT technology (GlobalFoundries 9HP). Small-signal (f_T/f_{max}) and large-signal (gain compression) measurements are performed to quantify the performance difference between cascodes with HP and MB devices in the common base (CB) stage, and DC+RF stress measurements are used to identify the reliability difference. The results show that large cascode cells operating well below the transistor peak f_T show roughly equivalent performance between HP and MB, and that the cascode reliability is largely dependent upon the selected bias point and load-line swing in conjunction with the top device selection. Thus, it may be possible for circuit designers to optimize the reliability of a circuit without sacrificing performance by carefully selecting the device profile and the dynamic output swing of the cascode cell. The data and analysis presented in Chapter 4 has been published and presented at the 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium [2].

CHAPTER 1

INTRODUCTION

In recent years, the demand for low-cost, high-performance integrated RF and mmWave circuit technologies has rapidly increased as several crucial industries have found need for high-speed circuits and systems. These technologies are desired for civilian applications, namely 5G cellular networks, satellite internet, and smart devices; military applications such as radar and electronic warfare; and scientific applications like remote sensing and space and extraterrestrial exploration. This growth has been achieved by constant generation-to-generation scaling of transistors in order to increase core performance parameters, such as high operation speeds, low noise, and high dynamic range.

An unfortunate consequence of the scaling trend of transistors is a restriction of the transistor safe operating area (SOA) that comes as a tradeoff with increased performance. Traditionally, this SOA boundary is conservatively defined by foundries as a range of biases that will give minimum performance degradation over the lifetime of the device. This may be acceptable for certain applications, but for circuit designers who wish to maximize the performance of their circuits and systems, this conservative SOA may discourage an aggressive bias that may improve performance over the intended application lifetime. Additionally, the SOA measurements are generally performed as a series of DC measurements, which can underestimate the actual dynamic range of the device during brief voltage and current swings beyond the DC SOA.

Ultimately, in order to design circuits that maximize performance while selectively violating the SOA guidelines, it is necessary to understand and model the dynamics of transistor breakdown, and to qualify the tradeoffs between circuit-level performance and reliability.

1.1 SiGe BiCMOS Technology

The introduction of germanium epitaxy into the development of bipolar silicon transistors allows the introduction of bandgap engineering to improve performance along with the classical advantages of silicon manufacturing, namely attractive thermal properties, high yield, and low cost. SiGe HBTs are attractive due to their high cutoff frequency, low noise, high transconductance per unit area, and on-chip integration with CMOS logic and RF passives. Generations are defined by improvements in small-signal transistor performance rather than lateral dimensions as in pure CMOS technologies [3].

Generational scaling has allowed SiGe BiCMOS technologies to achieve operation frequencies that are competitive with III-V technologies, while maintaining cost, manufacturing, and integration advantages inherent to silicon platforms. Recent platforms have achieved peak unity current gain cutoff frequency f_T as high as 350 GHz and peak unity power gain cutoff frequency of greater than 500 GHz [4], [5]. SiGe BiCMOS technologies are also attractive for cryogenic applications as the peak transit frequencies improve at reduced temperature, with near- THz speeds measured at cryogenic temperature [6].

1.2 The SiGe HBT

From a process perspective, silicon-germanium HBTs have a similar structure to pure silicon BJTs, but with the addition of an epitaxially grown SiGe layer in the base. An example cross section of a first-generation npn HBT is shown in Figure 1.1 and the corresponding doping profile in Figure 1.2.

The principal effect of introducing germanium to the transistor is an offset in the energy band diagram proportional with the germanium content. Figure 1.3 demonstrates the effect of a graded germanium base, which introduces a built-in drift field within the base. The intrinsic band offset due to the introduction of the germanium occurs in the valence band, not the conduction band as illustrated, but due to the p-type doping, the offset between the

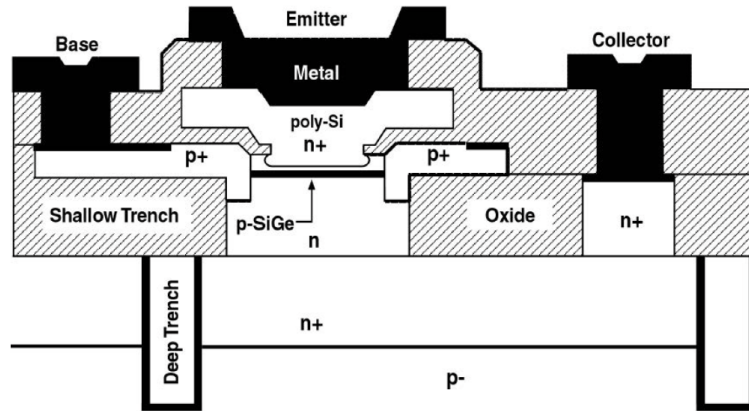


Figure 1.1: Cross-section example of a first-generation *npn* SiGe HBT (after [3]).

Fermi level and the valence band remains constant. Because the Fermi level must remain constant in equilibrium, the band offset appears in the conduction band instead [3].

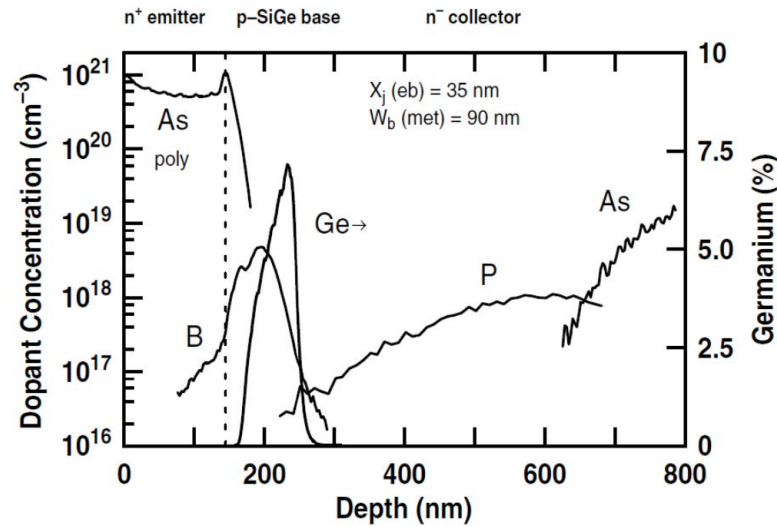


Figure 1.2: Sample SIMS profile of a first-generation *npn* SiGe HBT (after [3]).

The conduction band offset provides several improvements to the DC operation of the transistor. The germanium content at the emitter-base junction reduces the barrier for electrons to travel from the emitter to the base, resulting in an increase in electron current for a given bias, and accordingly an increase in the transistor current gain β . The graded bandgap reaches a minimum value in the collector-base junction which weighs the minority carrier profile in the base such that the backside depletion of the neutral base is limited [3].

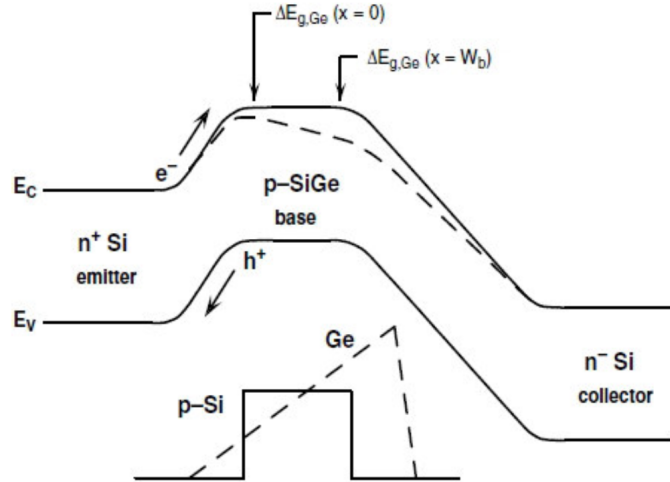


Figure 1.3: Effect of graded germanium on the energy band profile of an npn bipolar transistor (after [3]).

The germanium grading also provides benefits to the AC performance of the transistor. The graded conduction band acts as a built-in drift field within the base, reducing the base transit time τ_b which in turn helps improve the unity current and power gain cutoff frequencies f_T and f_{max} . Additionally, the enhanced majority carrier mobility in the base that results from the introduction of germanium helps reduce the transistor r_{bi} [3].

1.3 Breakdown Due to Impact Ionization

With increased operating speeds comes a reduction in the maximum operation voltage of transistors. The established tradeoff between maximum cutoff frequency f_T/f_{max} and breakdown BV_{CEO} is known as the Johnson Limit [7].

In principle, the transistor f_T increases with J_C bias until the onset of the Kirk effect [8]. State-of-the-art SiGe HBTs look to delay the onset of the Kirk Effect to the highest bias possible by using a heavy implant to achieve a highly doped collector. A consequence of the heavy collector doping is an increased electric field across the collector-base (CB) junction, increasing the impact ionization rate. The rate of impact ionization can be characterized by the avalanche multiplication factor ($M - 1$). The multiplication factor is defined in [3] as

$$M - 1 = \frac{I_{n,out}}{I_{n,in}} - 1 = \frac{I_C}{I_E - I_B|_{V_{CB}=0}} - 1 \quad (1.1)$$

where $I_{n,in}$ is the electron current flowing into the collector-base space charge region and $I_{n,out}$ is the current that flows out. Any difference between the two can only be caused by extra electrons generated due to impact-ionization. It is important to note that the multiplication factor will also be a function of the input bias (V_{BE} , I_B , or I_E). In principle, a higher $M - 1$ will result in a lower breakdown voltage, which partly explains the reduction in breakdown voltage as devices are scaled to improve f_T/f_{max} .

Advanced SiGe BiCMOS processes tend to achieve high performance under bias conditions where the CB field is large, and accordingly impact ionization presents a key reliability challenge for advanced transistors. Classically, the device operation limits under impact ionization are defined using the open base collector-emitter breakdown voltage (BV_{CEO}) and the open emitter collector-base breakdown voltage (BV_{CBO}). Importantly, the impedance provided at the base terminal will determine which breakdown limits the device [9]. BV_{CEO} is lower than BV_{CBO} and represents a worst-case breakdown when the base resistance is very large ($R_B \rightarrow \infty$). Conversely, BV_{CBO} will represent a best case when the base resistance is low ($R_B = 0 \Omega$). To account for the dependence of breakdown on base resistance, the literature sometimes uses BV_{CER} as a figure of merit for breakdown with resistance dependence [9].

BV_{CEO} is often defined as the location of base current reversal. As the name suggests, the base current can reverse from positive to negative as impact-ionization increases. At the point of reversal, the base is effectively open (no current flowing), and thus BV_{CEO} is defined. Figure 1.4 illustrates (a) the measurement setup used for base current reversal and (b) the physics behind current reversal. As collector-base voltage increases, impact ionization causes excess holes to flow back into the base. Eventually, these holes outnumber the holes flowing out across the EB junction, and base current switches direction as the difference must flow out of the base terminal. Mathematically, this occurs at the bias where

the product of β and $M - 1$ becomes greater than unity. Note that because β and $M - 1$ have bias dependence, so too will BV_{CEO} .

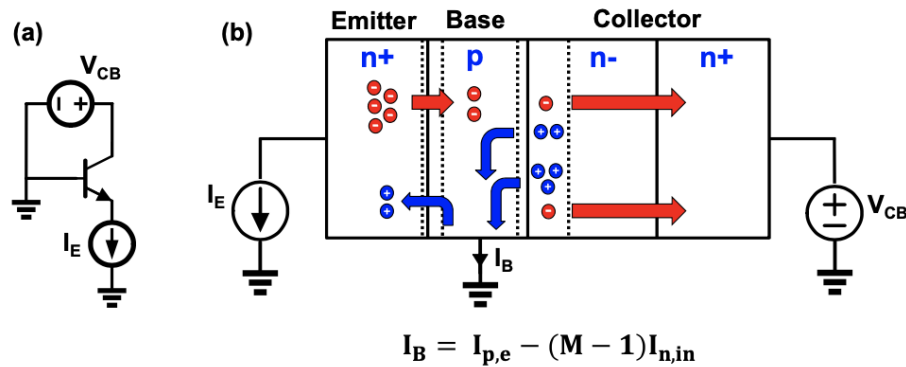


Figure 1.4: (a) Example measurement setup for base current reversal, where emitter current is forced and collector-base voltage is swept, and (b) visual representation of base current reversal.

BV_{CBO} is instead the result of breakdown across the collector-base pn junction. As the junction field increases, impact ionization also increases until the current across the junction becomes excessive. Unlike BV_{CEO} , BV_{CBO} is more loosely defined and will typically be defined by the foundry based on a specific increase from the zero-bias collector current as collector-base voltage is swept.

While BV_{CEO} is the classically-defined SOA boundary, literature has shown safe operation beyond BV_{CEO} [10] and even beyond BV_{CBO} [11]. In general, operating beyond these limits will come at a risk for stress damage, as described in the next chapter. Additionally, operation at these high voltages requires careful optimization of the base impedance of the transistor and output waveform-design to minimize the time overlap between voltage and current swings. Being able to design amplifier circuits to operate in these regions beyond the traditional SOA-defined breakdown voltages is desirable to improve circuit performance and requires a strong understanding and model of the transistor breakdown effects.

1.4 The Medium Breakdown HBT

Because transistor speed and breakdown voltage must necessarily be traded off as described by the Johnson Limit, device designers may elect to additionally include a lower speed, higher breakdown device to complement the aggressively scaled device that is the centerpiece of the technology. From a process integration standpoint, it is costly and impractical to keep substantially different recipes for the growth of the MB and HP *npn* devices. For this reason, the two process are integrated together using the same process with the exception of a single mask step. This keeps all structural aspects of the devices the same with the exception of the collector profile [12]. The process variation centers around suppressing or altogether removing the effect of the selectively-implanted collector (SIC), and is shown qualitatively in Figure 1.5.

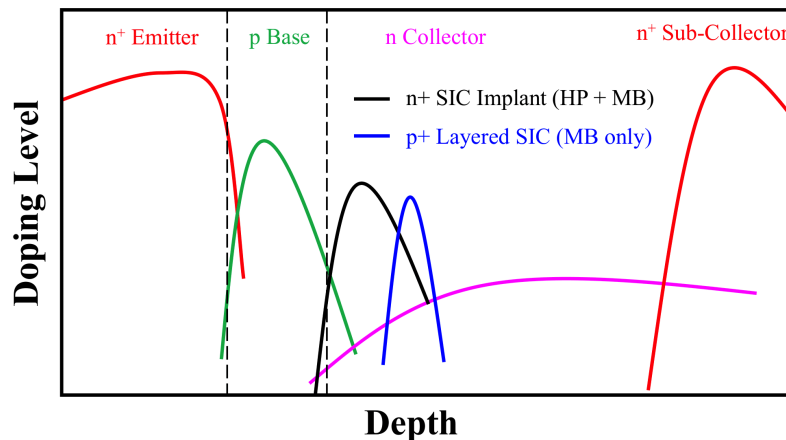


Figure 1.5: Qualitative schematic of the doping profile of a high-performance and medium-breakdown SiGe HBT demonstrating the introduction of a layered SIC.

In aggressively scaled SiGe *npn* devices, the SIC is used to reduce parasitics and delay the onset of base push out (the Kirk effect). The tradeoff resulting from the SIC implant is increased impact-ionization in the collector-base junction and accordingly reduced breakdown voltages. For the MB device, designers may choose to omit the SIC or use additional implants in order to reduce the impact of the SIC. One such method would be a “layered SIC”, using an additional p-type implant to reduce the electric field near the base (similar

to a *pn* “superjunction” [13]). This layered SIC distributes the field throughout the base, reducing impact-ionization at a given voltage and thus allowing for higher breakdown voltages, at the cost of an earlier onset of Kirk effect and greatly reduced f_T .

Including the MB device in the package with the aggressively-scaled HP device is beneficial for circuit designers, but necessarily adds complexity to any reliability studies, as the varied collector profile will result in different breakdown behavior within the two types of transistor.

CHAPTER 2

SiGe HBT RELIABILITY PHYSICS

2.1 Introduction

As generation-to-generation scaling has led to the creation of higher performing devices, it has become necessary to bias and operate SiGe HBTs as aggressively as possible in order to leverage the enhanced performance. As a result, the reliability of transistors at the edge of the SOA has become a key concern for understanding device operation limits and device lifetime. In order to reach higher peak f_T and delay the onset of the Kirk effect, the high collector doping results in a large field across the collector-base junction. Additionally, high current biases near the onset of Kirk effect are needed to maximize the frequency response of the transistor. This combination of high internal field and high current bias leads to hot carrier damage effects within the transistor that contribute to damage over the course of the device lifetime.

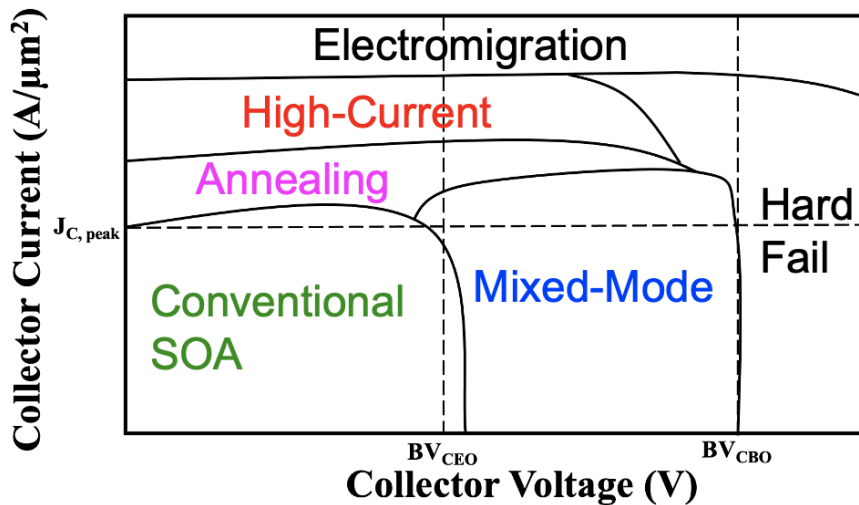


Figure 2.1: Sample output plane of a SiGe HBT, identifying SOA (green), annealing region (magenta), damage regions (red and blue), and hard failure regions (black).

An example of the damage mechanisms on the output plane of the transistor is shown in Figure 2.1. While extreme biases will result in a complete junction failure and catastrophic failure, known as “hard failure”, of interest in this work is the gradual degradation in device parameters as damage is accumulated up to the end of device lifetime. This gradual aging of the device is generally attributed to hot, or high-energy, charge carriers, which create traps at the EB spacer and STI oxide interfaces. These traps can be visualized as an increase in base leakage current in the low-injection region of the Gummel plots. In general, EB spacer traps will be prominent in the forward-mode Gummel, and STI traps will be prominent in the inverse-mode Gummel.

Section 2.2 will discuss in more detail the physical mechanism behind hot carrier damage. Two common damage mechanisms will then be described: Section 2.3 will discuss mixed-mode damage [14], and Section 2.4 will include a discussion on high-current damage [15].

2.2 Trap Generation Due to Hot Carriers

The generation of traps in SiGe HBTs due to hot carriers can be split up into two mechanisms. The first is the generation of hot carriers and their propagation to the oxide interfaces. The second is the generation and annealing of traps as the hot carriers expose dangling bonds at the oxide interface.

During the growth of the transistor, the interface between the silicon crystal and the silicon oxide has dangling bonds, because the two crystals have different structure and thus do not form together perfectly. Because these dangling bonds can trap carriers, leading to unwanted Shockley-Read-Hall (SRH) mechanisms which increase leakage current, process engineers flood the crystal with hydrogen during an annealing step. The hydrogen atoms passivate the dangling bonds, removing potential traps from the crystal. Literature has shown [16] that $2.3 eV$ are required to de-passivate a silicon bond at the oxide interface. Thus, in order for a trap to be generated, charge carriers must receive $2.3 eV$ of excess

energy, and then travel to the oxide interface while avoiding energy-robbing collisions. The mechanisms by which these hot carriers are generated will be discussed in the following sections.

Once the hydrogen atom has been knocked free of the dangling bond in the oxide interface, it can diffuse away from the newly created trap. After traps are generated, it is possible for an annealing mechanism to occur, with positive temperature dependence, wherein loose hydrogen atoms return to the oxide interface and re-passivate dangling bonds. This reverse process can help a device recover some, but not all, of the damage accumulated due to stress. From a measurement perspective, it is important to quickly measure damage after performing electrical stress to minimize the amount of time during which the transistor can self-anneal damage away.

2.3 Mixed-Mode Damage

Mixed-Mode (MM) describes the damage region when the device is subjected to a large collector-base field and a moderate to high collector current [14]. In general, mixed-mode damage starts to become prevalent when a device is subject to a field greater than BV_{CEO} . Impact-ionization is the primary force behind the generation of hot carriers, and accordingly this damage mechanism is most prevalent in aggressively-scaled technologies where a high collector doping is used to improve peak f_T by delaying the Kirk effect and heterojunction barrier effects, at the cost of an increased built-in collector-base junction field and increased impact-ionization.

Figure 2.2 illustrates the generation (P_1) of hot carriers and their propagation (P_2) to the STI and EB spacer interfaces. Carriers travel from the emitter through the base and undergo impact-ionization in the high field region of the CB junction. After undergoing impact-ionization, the newly-energized hot carriers then travel with some probability to either the STI region or the EB spacer, where they can de-passivate bonds and create traps.

An example Gummel stress evolution for a device under mixed-mode stress conditions

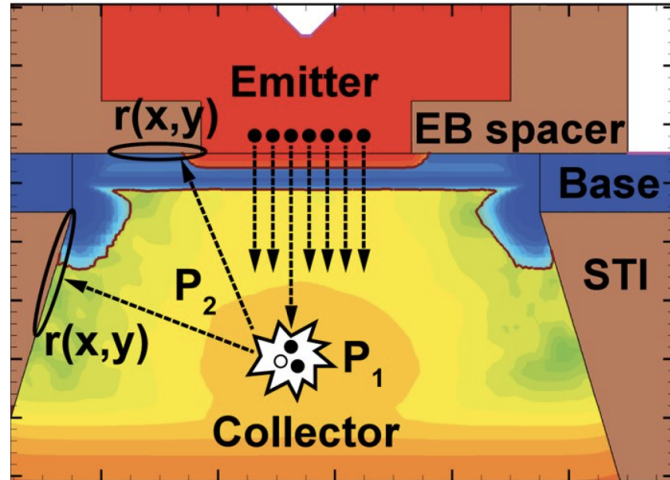


Figure 2.2: Cross-section of a SiGe HBT illustrating the mechanism behind mixed-mode damage (after [17]).

is presented in Figure 2.3. The increased traps at oxide interfaces result in an increased non-ideal base current in low-injection. This results in a degradation in transistor β over device lifetime. The forward Gummel will show trap generation at the EB spacer and the inverse Gummel shows trap generation at the STI interface. Changes in base current from measured data can be implemented back into both TCAD [17] and compact modeling [18] environments.

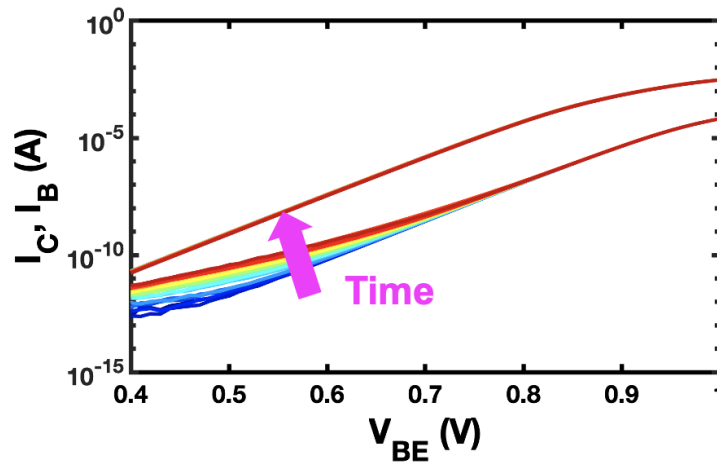


Figure 2.3: Example Gummel evolution of a SiGe HBT after experiencing mixed-mode stress.

2.4 High-Current Damage

High-Current (HC) damage refers to the damage region where the device is subjected to a large bias current and a relatively small collector-base field. Unlike MM damage, the hot-carriers are produced not by high fields, but rather by Auger recombination effects occurring within the emitter of the transistor [15]. Because the energy required for de-passivation (2.3 eV , from [16]) is roughly twice the bandgap of silicon, hot-carriers are only generated with sufficient energy to cause damage when multiple Auger events occur in quick succession.

Figure 2.4 gives an example from TCAD of the probability of double-Augur events to create hot carriers with sufficient energy to break traps. In general, this rate increases both with temperature and current density, as these both contribute to a larger density of Auger events occurring within the emitter. A cross-section visualizing the movement of these hot carriers to oxide interfaces is shown in Figure 2.5.

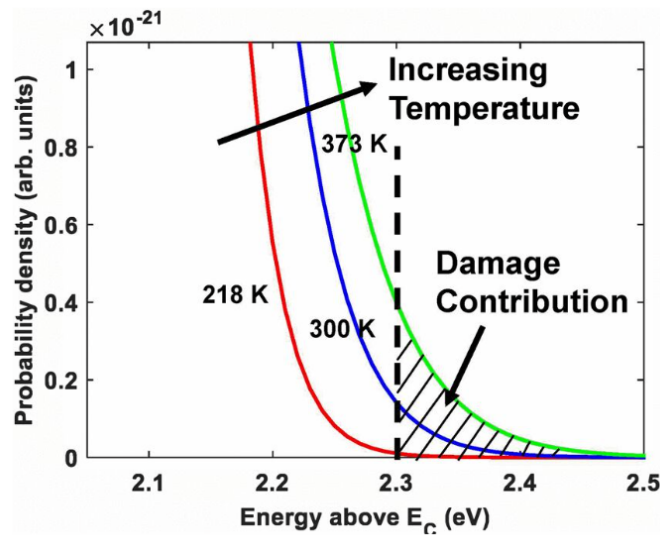


Figure 2.4: TCAD representation of relative frequency of double-Augur events with sufficient energy to create traps (after [19]).

Figure 2.6 plots the Gummel evolution of a SiGe HBT after high current stress. As with the MM stress condition, low-injection base leakage increases, resulting in a degradation

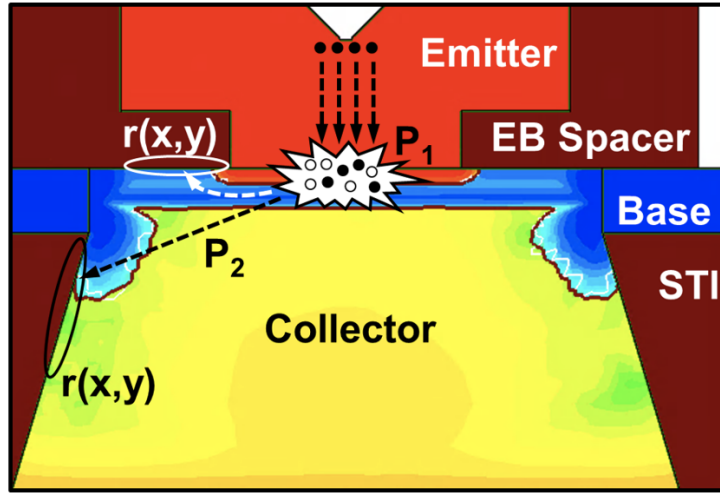


Figure 2.5: Cross-section of a SiGe HBT illustrating the mechanism behind high-current damage (after [20]).

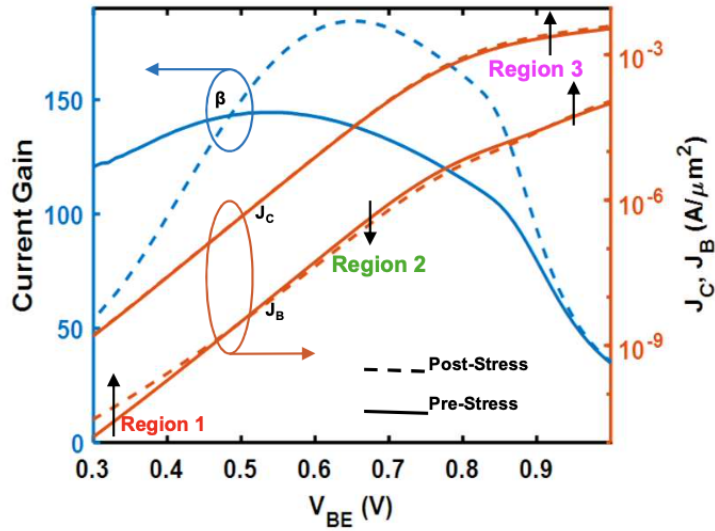


Figure 2.6: Gummel evolution of a SiGe HBT subject to high current stress, demonstrating three distinct damage regions (after [21]).

in β . However, in medium-injection, the base-current decreases and β is enhanced. This has been known as the current gain enhancement (CGE) effect and is attributed to damage at the poly-silicon grain boundary interfaces under the same HC damage mechanism [21]. Damage at the polySi grain boundaries alter the resistivity of the crystal, thus changing the carrier mobility (causing the shift in region 2) and the resistance (causing the slight shift in region 3). The leakage current can be modeled in the same way as that caused by MM damage, but the damage to the polySi grain boundary is exclusive to HC damage and can be more challenging to model. Additionally, the magnitude of the damage will be dependent on the quality of the polySi crystal grown during the process flow.

CHAPTER 3

DYNAMIC BEHAVIOR OF BREAKDOWN MECHANISMS IN SIGE HBTs

3.1 Introduction

SiGe HBTs are an attractive option for implementing power amplifiers [22], wireline drivers [23], and high-speed op-amps [24], due to their good linearity, ease of integration with BiCMOS technology, and low manufacturing cost. As SiGe HBTs are scaled for higher-frequency operation, breakdown effects such as thermal runaway and impact-ionization, which limit their maximum voltage and current ratings, become more prevalent. Increased doping in the selectively implanted collector (SIC) region boosts cutoff frequency (f_T), but at the cost of increased impact-ionization and reduced breakdown voltage [25]. Additionally, state-of-the-art high-performance SiGe HBTs use oxide trench isolation to reduce parasitics at the cost of increased thermal resistance and self-heating inevitably worsens with technology scaling [26].

While breakdown limits and the defined device safe operating area (SOA) are traditionally characterized via DC measurements [27], it is well-known [28] that the dynamic SOA, the RF-SOA, of devices may be expanded well beyond DC limits, as RF signals spend little time at the high voltages and currents that induce the thermal runaway evident in DC measurements. Therefore, for amplifiers and drivers where high output voltages and currents are produced by high-frequency RF signals, it is more useful to measure the SOA under pulsed-mode conditions, which help alleviate self-heating. In pulsed-mode measurements, the device is turned on and measured before significant self-heating occurs, resulting in current-voltage data that more closely represents the actual device operating conditions with the operative circuit.

In the present paper, pulsed-mode measurements are used to suppress the impact of

self-heating on the transistor, and thereby explore the dynamics of device breakdown for high-speed SiGe HBTs. At high input voltage, self-heating is the dominant breakdown mechanism (i.e., thermal runaway) and tends to suppress impact-ionization related effects within the device [29]. By using pulsed-mode measurements, and adding a small ballasting resistor to reduce the effects of self-heating on conventional forced-voltage output curves, it is possible to partially decouple the two breakdown mechanisms and show a time-dependence of the dominant process. This paper concludes with a discussion of the implications of a dynamic breakdown mechanism and how that might be used to reliably expand circuit operating conditions, as well as a provide better understanding of the performance-reliability tradeoffs as we approach the SOA limit.

3.2 Breakdown Mechanisms in SiGe HBTs

Two common sets of output curves used to assess the SOA limits of a SiGe HBT are the common-emitter (CE), forced base-emitter voltage (V_{BE}), and the common-base (CB) forced emitter current (I_E) curves. For both sets of curves, an input signal (V_{BE} or I_E) turns the device on, and then the collector voltage (V_C) is swept. The collector current (I_C) and base current (I_B) are then measured at each V_C bias point.

Impact-ionization induced breakdown, referred to as avalanche breakdown, occurs when high voltages are applied to the collector-base junction. Avalanche breakdown is most evident in forced- I_E measurements, since $I_C \approx I_E$ regardless of the amount of self-heating. As the collector-base junction voltage V_{CB} is swept, impact-ionization in the collector-base junction generates extra electron-hole pairs. These excess generated electrons flow out of the collector, while the extra holes flow back into the base. The additional electrons increase I_C rapidly, eventually causing damage or failure to the device.

Thermal runaway, on the other hand, occurs in forced- V_{BE} curves, because I_C exhibits a strong temperature dependence when driven by V_{BE} . If V_{BE} is large enough to present a high I_C , self-heating of the device will occur as the power delivered to the device increases.

As the device heats up, I_C increases, creating a positive feedback loop between device temperature and power consumed, causing I_C to increase uncontrollably (often termed thermal runaway).

Because both thermal runaway and avalanche breakdown cause an increase in I_C , the dominant breakdown mechanism can be most clearly determined by examining the behavior of I_B . In the case of thermal runaway, the base current will grow along with collector current as the output voltage is swept. In the case of avalanche breakdown, however, the holes generated within the collector-base junction flow back into the base, replacing the holes flowing out across the emitter-base junction. Eventually, the direction of I_B is physically reversed as excess holes begin to flow out of the base contact. This process is called base current reversal (BCR). The two breakdown mechanisms are compared in Figure 3.1. Observe from I_C in Figure 3.1(a) that the forced- V_{BE} measurement experiences thermal runaway well before I_C begins to shift in the forced- I_E measurement. On the I_B plot in Figure 3.1(b), the forced- I_E curve changes sign due to impact ionization (indicated by the notch in the log-scale plot) while the forced- V_{BE} curve remains positive throughout.

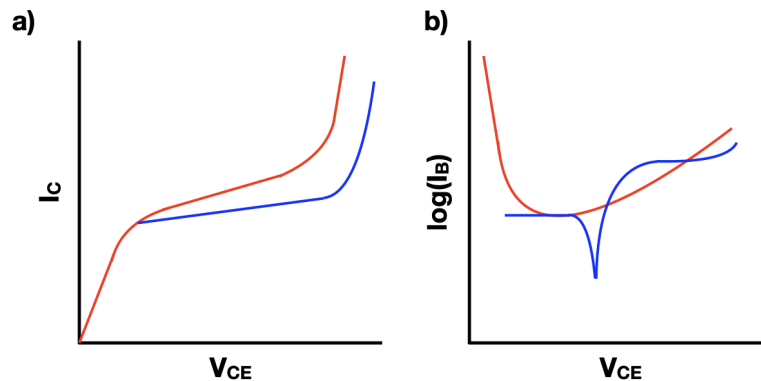


Figure 3.1: (a) I_C and (b) I_B plotted vs V_{CE} for forced- V_{BE} and forced- I_E measurements. The values for V_{BE} and I_E were selected to produce the same I_C at $V_{CB} = 0$ V.

In cases where avalanche breakdown dominates, and the current flowing out of the base becomes sufficiently large, device “pinch-in” occurs [30]. During pinch-in, the base current creates an internal voltage gradient across the distributed intrinsic base resistance, with a

peak voltage located at the center of the device. The electron current flowing through the HBT is then constricted primarily to the center of the device. This concentration of current leads to bias instabilities within the device, resulting in an abrupt decrease in I_C , as seen in Figure 3.2. The simulation inset shows the current distribution in a cross-section of the device at the onset of pinch-in.

Modeling pinch-in is a challenge, as it requires either the use of multiple transistors [30] or a bias-dependent base resistance [31]. Both of these solutions increase the computation time and complexity of compact models, and are difficult to implement. Because pinch-in results in bias instabilities, small-signal performance near pinch-in cannot be easily captured. The result is that device operation in and around the pinch-in region remains unmodeled, and circuit designers cannot predict how circuits that swing dynamically into the pinch-in region will perform. This situation is clearly problematic. It is thus necessary to characterize the dynamic behavior of SiGe HBTs in this region of operation to enable complete large- and small-signal pinch-in models to be developed.

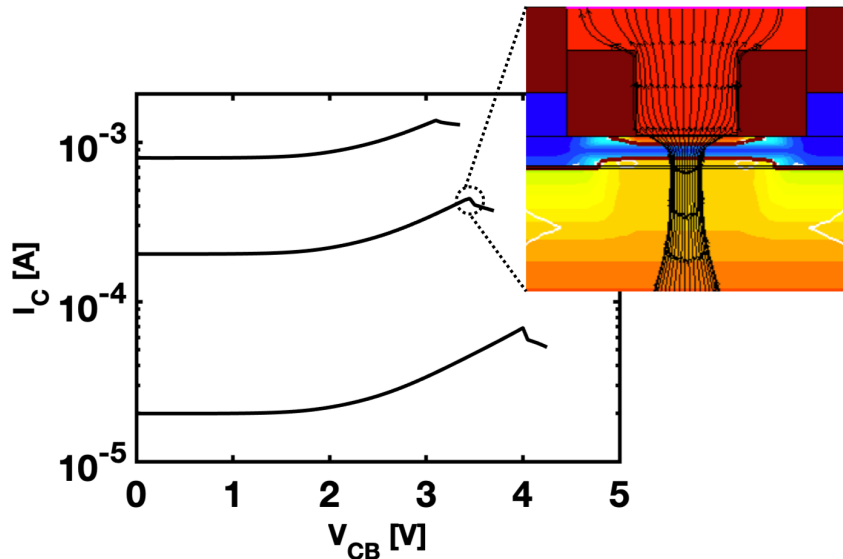


Figure 3.2: Collector current as a function of collector-base voltage for three forced-emitter currents demonstrating a pinch-in effect. (inset) SiGe HBT cross-section simulated in TCAD showing the central current distribution at the onset of pinch-in.

3.3 Measurement Setup

The devices measured were the high-performance *npn* SiGe HBTs from GLOBALFOUNDRIES 90-nm 9HP SiGe BiCMOS platform. The devices feature an open-base breakdown voltage BV_{CEO} of 1.7 V and open-emitter breakdown voltage BV_{CBO} of 5.2 V, along with unity current and unity power gain frequencies f_T/f_{max} of 300/350 GHz, respectively.

DC measurements were performed using an Agilent 4155 Semiconductor Parameter Analyzer. Pulsed-mode measurements were performed using a Keithley 4200A-SCS Parameter Analyzer, with pulse-measure unit (PMU) extension. The PMU is capable of simultaneously sourcing voltage and measuring current at pulse widths down to 100 ns. The measured structures were AC test structures with 50 Ω traces and ground-signal-ground access to the emitter, base, and collector terminals.

Pinch-in is typically measured using forced- I_E output curves on common-base (CB) structures, but the Keithley is not equipped to provide pulsed current. Instead, measurements here are performed pulsing both terminals to measure forced- V_{BE} output curves on a device in common-emitter (CE) configuration. Due to the high thermal resistance of the SiGe HBTs, pulsed-mode measurements alone are not enough to replicate pinch-in with forced-voltage. Thus, an alternative method was devised in Figure 3.3. One technique already used in amplifier design is the introduction of a ballasting resistor on the emitter of the SiGe HBT [32]. With the addition of the ballast resistor, an increase in I_C results in a decrease in the V_{BE} delivered to the device, breaking the feedback loop that results in thermal runaway. In addition to the improved thermal management, ballast resistors have been shown [33] to improve RF amplifier performance. This approach will be used to replicate dynamic swings into a high voltage region where impact-ionization is significant, but that are also fast enough to limit thermal effects, as might occur, for instance, in a high-power amplifier circuits.

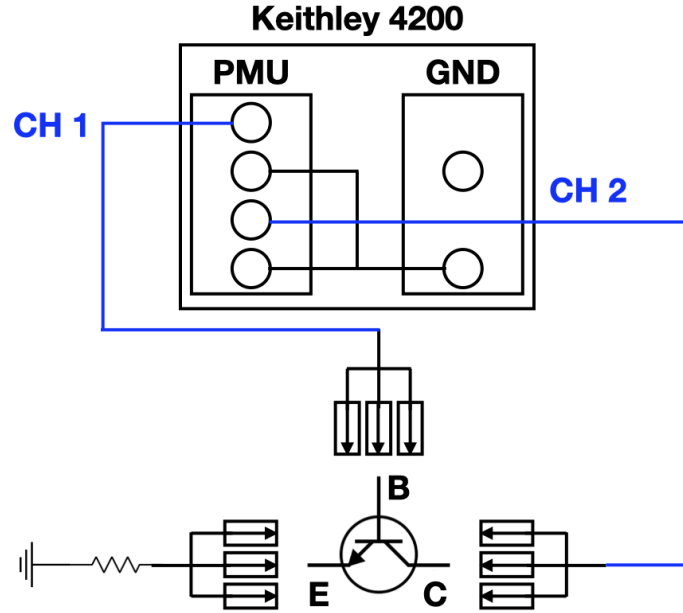


Figure 3.3: Diagram of Keithley 4200 measurement setup with emitter ballast resistor included.

3.4 Measurement Results

DC measurements were taken first in order to verify that the ballast resistor reduces self-heating effects in the forced-voltage output curves sufficiently to recreate pinch-in. These measurements were also used to tune the value of the ballast resistor before beginning pulsed-mode measurements. If the ballast resistor is too small, it will be unable to reduce the base-emitter voltage enough to offset the impact of device self-heating, and thermal runaway will still occur. Conversely, if the chosen resistor is too large, it will substantially change the operating point of the device and prevent extrapolation back to the performance of the intrinsic device. The ballast resistor was selected by sweeping the collector voltage through a small range ($V_{CE} = 0 - 2 \text{ V}$), while biasing at a high input base-emitter voltage ($V_{BE} = 1 \text{ V}$). When the change in the collector current remained within 5% across the limited voltage sweep, the ballast resistor was deemed large enough to counter the effects of self-heating. In this paper, a 30Ω resistor was chosen for emitter ballasting, which is optimal for this technology platform.

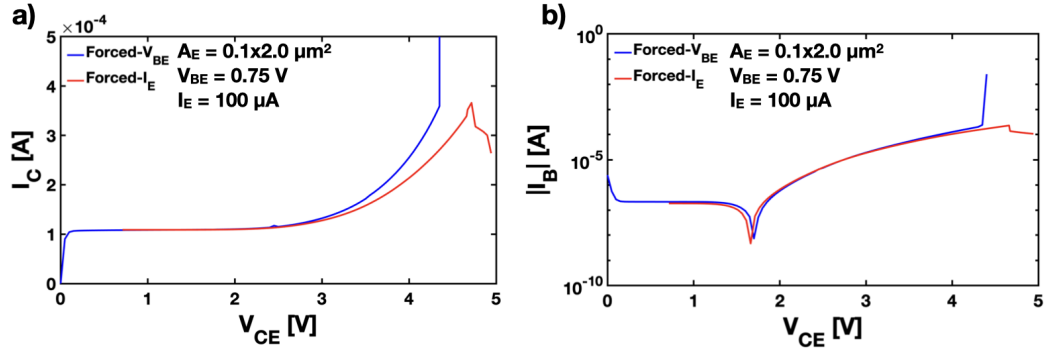


Figure 3.4: a) I_C and (b) I_B plotted vs V_{CE} for forced- V_{BE} with ballast resistor and forced- I_E measurements.

DC measurements using this setup are shown in Figure 3.4. With the addition of the ballasting resistor, thermal runaway is effectively suppressed and the forced- V_{BE} and forced- I_E curves track closely, as desired. The key difference between these two measurements is the high-field region where pinch-in occurs. From the forced- I_E curve, the collector current decreases slightly at pinch-in. This is because the emitter current concentrated in the center of the device raises the emitter voltage as it flows across the intrinsic emitter resistance. In the forced- V_{BE} curve, both the emitter voltage and base voltage are set by voltage sources, and are not able to shift as drastically, resulting instead in a sharp increase in both currents that will lead quickly to catastrophic failure.

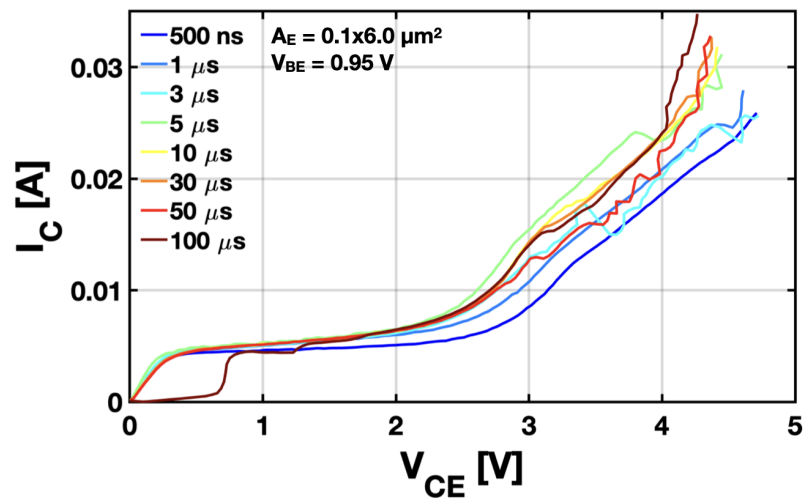


Figure 3.5: Collector current vs pulsed collector voltage sweep at set V_{BE} for different pulse widths.

After the ballast resistor was selected, pulsed-mode voltage measurements were made. In Figure 3.5, the collector current decreases with pulse width, as expected, since the device has less time to self-heat. From the base current plot in Figure 3.6, each curve has a reversal point at the same point of about 2.4 V, just slightly past the BV_{CEO} of the device. However, a second base current reversal, with a dependence on pulse width, occurs at higher voltages as the base current switches back in the positive direction. A second base current reversal has been discussed before [34] in high voltage SiGe HBTs, where impact ionization effects are weaker overall due to reduced collector doping, but in that work was not explored as a function of the time duration of transient signals.

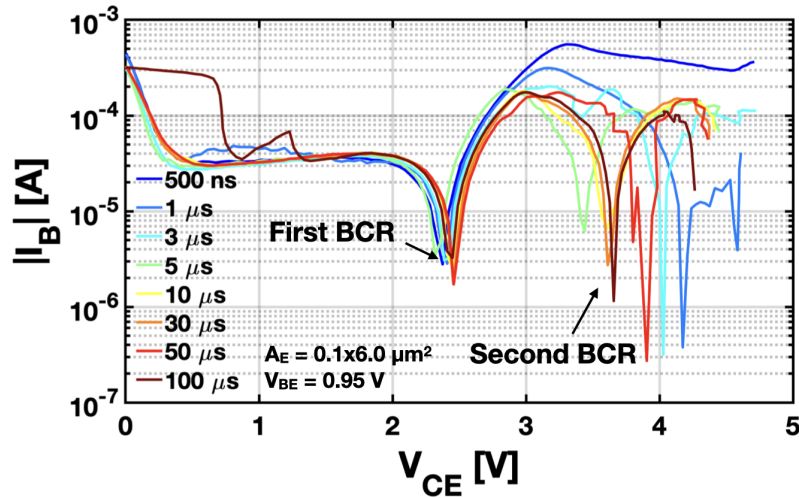


Figure 3.6: Base current vs. pulsed collector voltage sweep at set V_{BE} for different pulse widths.

To probe deeper into the underlying cause of this second reversal, oscilloscope captures have been taken, and are plotted in Figure 3.7. From the scope captures, the base current waveform becomes negative almost immediately, as a result of impact-ionization. The waveform then gradually increases as the device begins to self-heat. If the pulse width is sufficiently long, the base current will reverse again as self-heating begins to dominate. From the waveforms, it is also evident that impact-ionization and self-heating occur at different time scales. The impact-ionization response occurs immediately as the device turns on, while self-heating occurs gradually over the 1.6 μ s pulse. This is expected given

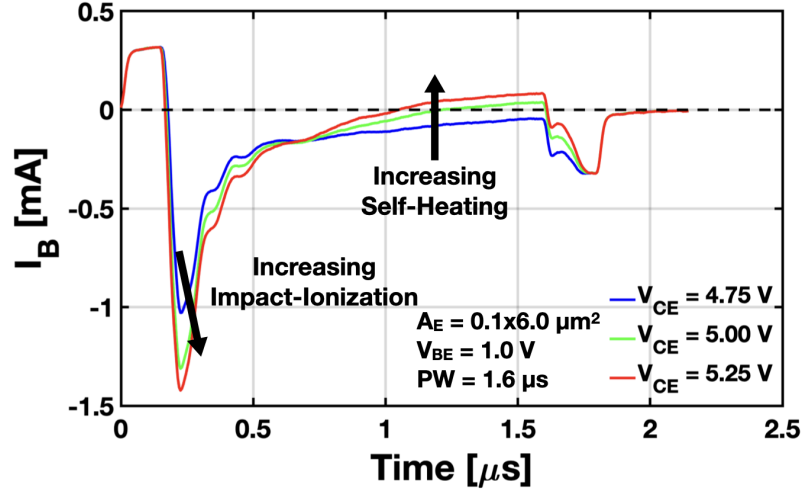


Figure 3.7: Oscilloscope captures of base current waveform at set V_{BE} for three different V_{CE} , around the point of second BCR.

the magnitude of the thermal time constant in these devices. Figure 3.8 shows the V_{CE} at which base current reversal occurs, versus the pulse width used in the measurement. The first reversal point remains constant as a function of pulse width, suggesting that self-heating doesn't influence the physics of the first base current reversal. By comparison, the second base current reversal occurs at lower V_{CE} as pulse width increases. At lower pulse widths, more power must be consumed within the SiGe HBT in order to heat it enough to reverse for a second time. The shortest pulse never reverses, indicating that for short enough pulse widths, this second reversal can be avoided altogether.

3.5 Summary

In this paper, pulsed-mode voltage measurements were implemented using a modified device characterization test bench, in order to investigate the two dominant breakdown effects under high fields. With the pulsed-mode measurement setup, it is possible to reduce the effects of device self-heating enough to allow an investigation of impact-ionization at high power, where thermal effects typically dominate. Measurements also indicated two base current reversals are operative in these conditions: a pulse width-independent base current reversal caused by impact-ionization, and a second base current reversal, which is

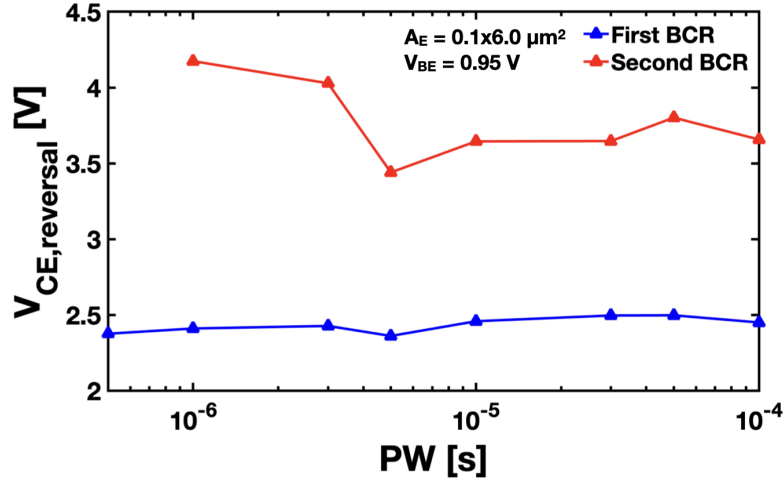


Figure 3.8: V_{CE} corresponding to the location of each base current reversal point in Figure 3.6.

pulse width-dependent because of self-heating. Additionally, the pulsed-mode voltage bias was safely applied beyond conventional DC-defined SOA, allowing for extra output power compared to the DC limit.

The paper also showed that short pulse width measurements can maintain a steady bias as the device approaches pinch-in. The logical next step is to implement pulsed-RF measurements, in which a RF signal is modulated with a pulsed biasing voltage. This is underway. Pulsed-RF measurements can be used to explore the small-signal response of transistors near pinch-in, including how the linearity, small-signal gain, and noise performance of devices changes when biased near pinch-in. A complete understanding of large- and small-signal performance of SiGe HBTs near pinch-in will give circuit designers access to a new range of potential operating points to maximize device performance while maintaining reliable performance.

CHAPTER 4

PERFORMANCE VS. RELIABILITY TRADEOFFS OF MEDIUM BREAKDOWN AND HIGH PERFORMANCE CASCODE AMPLIFIER CELLS

4.1 Introduction

In recent years, SiGe HBTs have become attractive options for high-speed communications due to the addition of germanium bandgap engineering to the existing manufacturing advantages of silicon; namely high-yield, low cost, and high integration levels. Generation-to-generation evolution of SiGe platforms has seen advancements in lateral scaling, vertical profile optimization, and careful bandgap engineering, enabling unity-current gain cutoff frequency f_T in excess of 300 GHz, and unity power gain cutoff frequency f_{max} in excess of 500 GHz [4]. This increase in f_T/f_{max} comes with an inevitable tradeoff in the device safe voltage operating limits [7]. The reduced voltage limits pose a challenge for applications requiring high RF power handling. One solution is to utilize distinct variants of the SiGe HBTs available, each optimized for different breakdown voltages and peak transit frequencies, in order to provide extra flexibility for any given application. In fact, many commercial SiGe platforms offer both high performance and high breakdown variants of SiGe HBTs to facilitate having a single platform which provides for multiple targeted designs [12].

One key application space for RF front-end modules is the power amplifier (PA) block. SiGe HBTs possess favorable thermal properties and reliability compared to III-V alternatives such as GaAs [35], but are limited by lower comparative breakdown voltage, in part due to the smaller bandgap. In order to obtain high output power density, designers must either increase the available current swing by using multiple larger devices in parallel, or increase the available output voltage swing by using cascode [36] or stacked [37] amplifier

topologies.

Previous investigations exist on the RF reliability of cascode structures [38] and on reliability differences between MB and HP transistors [39]. However, the performance-reliability tradeoffs for MB and HP cascode amplifier cells remains unexplored. The present paper measures single devices and cascode cells to investigate the performance and reliability of MB and HP cascode cells in order to define best practices for designers regarding the selection of MB and HP devices for high output power cascode amplifiers.

4.2 Measurement Setup

This study used devices from the GLOBALFOUNDRIES 90 nm 9HP SiGe BiCMOS platform, which offers high performance (HP) and medium breakdown (MB) variants of *npn* SiGe HBTs. The device performance operating limits and breakdown voltages (from [40]) are summarized in Table 4.1.

Table 4.1: HP vs MB Device Comparison

Device	f_T	f_{max}	$J_{C,peakfT}$	BV_{CEO}	BV_{CBO}
HP	300 GHz	360 GHz	20 mA/ μm^2	1.7 V	5.2 V
MB	135 GHz	350 GHz	5 mA/ μm^2	2.4 V	7.9 V

The MB device is fabricated with a nearly identical structure and profile, with a simple alteration to the collector profile using ion implantation [12] to increase breakdown voltage at the cost of both peak f_T and the current-handling capability of the transistor.

Of interest to a circuit designer will be how MB devices can be leveraged to improve amplifier reliability under large output voltage swing, and what the resulting tradeoff will be between achieving this increased reliability at the expense of reduced performance from lower f_T and $J_{C,peakfT}$. To test this, measurements have been performed on custom-designed cascode test structures, as shown in Figure 4.1. For each test structure, the common-emitter (CE) device and the common-base (CB) device are of identical emitter

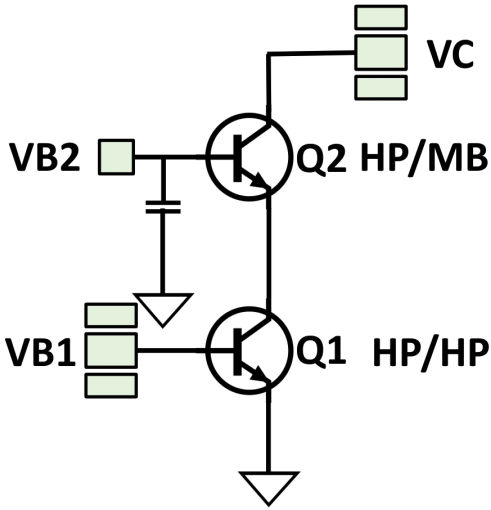


Figure 4.1: Schematic representing HP and MB cascode structures used in the study. AC contacts are placed at the Q1 base (input) and Q2 collector (output), while the Q2 base is kept grounded and DC biased.

area to facilitate comparisons. The emitter width for all devices is $0.1\mu m$, and structures are available with emitter lengths of 2, 4, and $8\mu m$. HP devices are always used for the CE stage, but variants of the CB stage are available using either HP or MB devices. The cascodes will be distinguished based on the top device and the emitter length of the transistors. Single device DC structures are also measured for each size of HP and MB device to decouple device vs. circuit effects.

4.3 HP vs MB Operating Limits and Performance Comparison

Before characterizing reliability, it is important to first demonstrate the circuit-level merits of using MB devices. The CB device in the cascode will be subject to large collector-base voltage V_{CB} , both from the biasing and from the large output RF swing. As V_{CB} increases, impact ionization will first cause base current reversal [41]. Then, excess holes flow out of the base, leading to device pinch-in instabilities [30].

Figure 4.2 plots measured pinch-in limits from single-device DC structures. Each device was biased across a range, from low-valued forced emitter current ($\sim 1\% J_{C,peak}$) up to

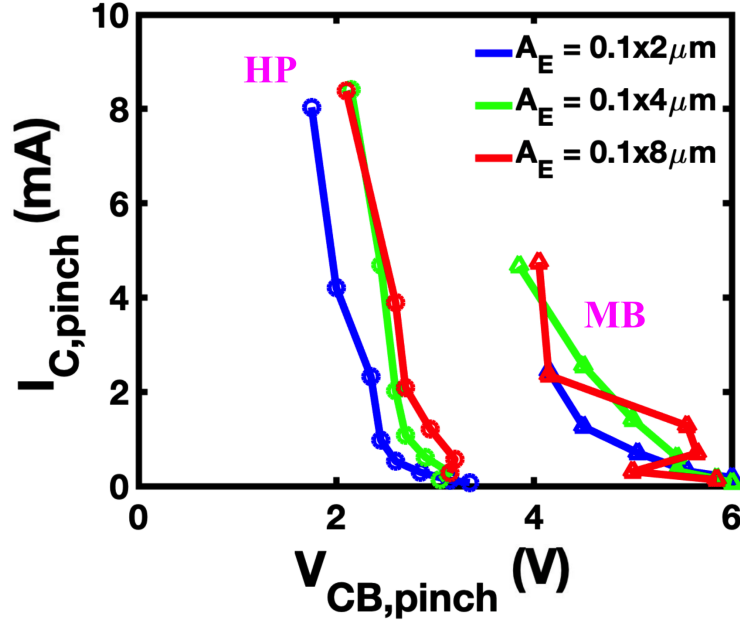


Figure 4.2: Point of pinch-in for HP and MB devices of $2\mu\text{m}$, $4\mu\text{m}$, and $8\mu\text{m}$ emitter length, for current biases up to $J_{C,peak}$

twice $J_{C,peak}$, with the base grounded and the collector voltage swept. The point of pinch-in is visible as a sudden change in the slope of the collector and base currents, but is more robustly defined as the point of a significant instantaneous reduction in measured base-emitter voltage. The MB devices roughly double the limit $V_{CB,pinch}$, at the cost of roughly half of the maximum $I_{C,pinch}$. With regards to cascode biasing limits, $V_{B2} + V_{CB,pinch}$ represents the bias limit of V_C for a given current bias, driven by V_{B1} . At equivalent I_C , the larger devices are generally able to handle a slightly larger V_{CB} before pinching in.

Table 4.2: Peak f_T for Cascode Across Geometry

Device	$L_E = 2\mu\text{m}$	$L_E = 4\mu\text{m}$	$L_E = 8\mu\text{m}$
HP	235 GHz	244 GHz	238 GHz
MB	213 GHz	215 GHz	205 GHz

While the extra available output voltage is an obvious advantage of using MB devices, circuit designers will be concerned with potential tradeoffs from the reduced f_T . Table 4.2 shows the peak measured f_T for each cascode test structure. For these measurements, V_{B1}

and V_{B2} are swept, as done in a cascode gummel measurement, with the collector voltage set so that the top device V_{CB} is held at the value that gives an individual device peak f_T (0.3 V for HP, 1.0 V for MB). From the table, there is a drop of about 10% in f_T from HP to MB, substantially smaller than the single device difference.

Figure 4.3 compares the cascode f_T behavior across V_{CB} . The structures are first biased at their peak f_T from the previous measurement, and then V_{CB} is swept. The base current of the CB stage device is plotted in order to give insight into when the device experiences base current reversal, and when it experiences pinch-in instabilities.

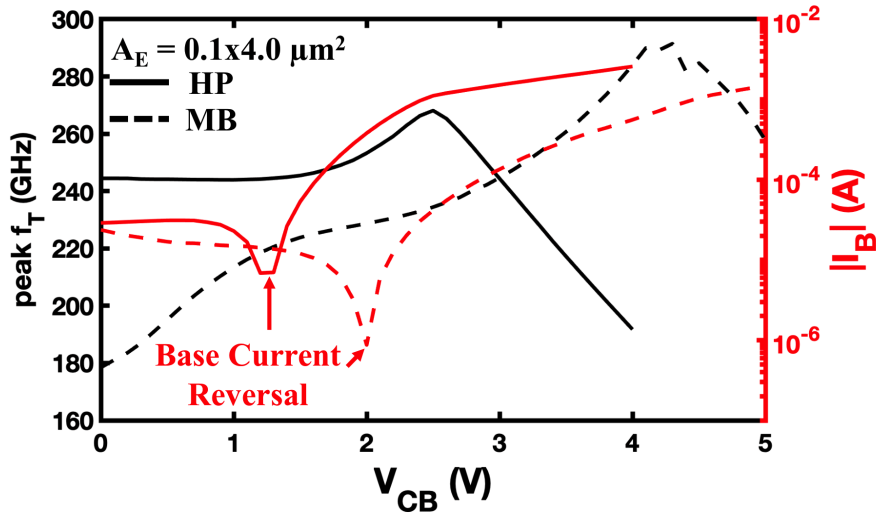


Figure 4.3: Measured f_T across swept $V_{CB,top}$ for $0.1 \times 4.0 \mu m^2$ HP and MB cascode structures.

From the measurements, there is no change in f_T after base current reversal, and in fact the peak f_T increases with more impact-ionization. The f_T reaches a maximum at a critical V_{CB} , which notably is about 2 V higher for the MB cascode than for the HP cascode. In addition, it is significant that although the f_T of the MB cascode is smaller at low bias, at high V_{CB} , the peak f_T exceeds that of the HP cascode. For applications with a large power budget or access to high voltage bias, MB cascode cells can provide higher peak f_T than the HP cells, an interesting and potentially important result.

For high-power RF applications, designers will also be concerned with device linearity,

specifically the maximum output power achievable before gain compression. For comparison, the cascodes are measured at a single frequency as the input power was swept. The chosen frequency of 5 GHz represents a common application frequency (Wi-Fi) and is intentionally far away from the peak f_T of the cascodes in order to compare performance when operating far from the maximum frequency limits. The input power was swept from -35 dBm to -5 dBm in order to capture amplifier behavior before and after compression.

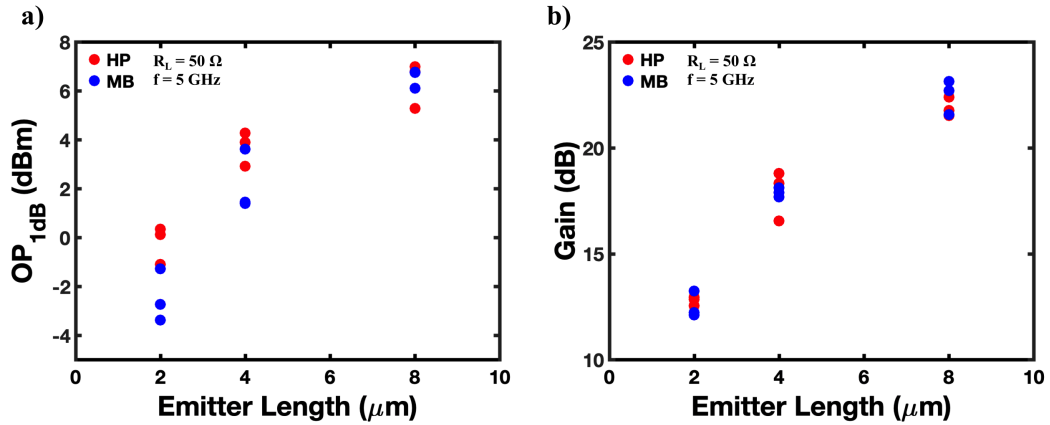


Figure 4.4: (a) Output-referenced 1 dB compression point and (b) pre-compression gain, for HP and MB cascode cells with equal emitter length.

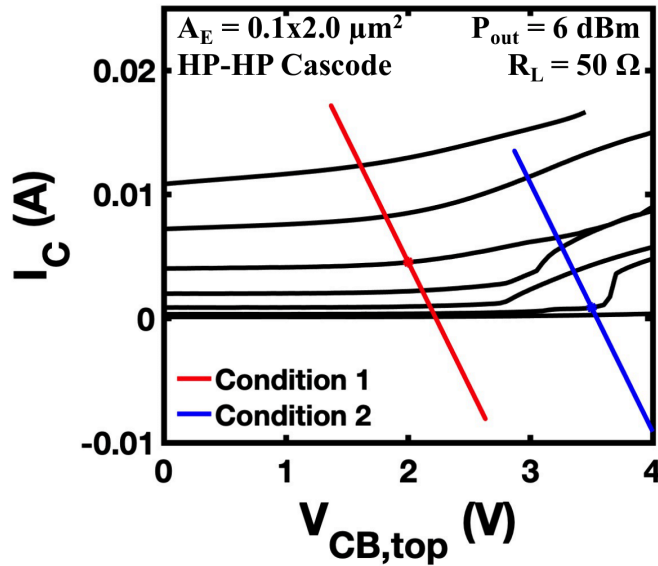


Figure 4.5: Sample load-lines laid over the output curves for a cascode structure. Condition 1: $V_{BE} = 0.91 \text{ V}$, $V_{CB} = 2.0 \text{ V}$; Condition 2: $V_{BE} = 0.85 \text{ V}$, $V_{CB} = 3.5 \text{ V}$.

The sweep results are summarized in Figure 4.4. The scatter plots display three samples of each cascode cell in order to reduce the impact of device-to-device variation on the results. The set bias condition is $V_{B1} = 0.91\text{ V}$, $V_{B2} = 2.02\text{ V}$, $V_C = 4.02\text{ V}$ for all samples. This condition forces a bias current near the $J_{C,peak}$, and an aggressive output voltage intended to increase output voltage swing headroom. In practice, a higher V_C could be chosen for the MB cascode to further leverage the increased voltage headroom, but the MB performance at this bias isn't substantially worse, especially for the largest device. From Figure 4.4(a), the smallest MB cells see a reduction of a few dB in the output-referenced 1-dB compression point (OP_{1dB}), but the $8\text{ }\mu\text{m}$ variation has equal OP_{1dB} . Since most PA applications will try to maximize output power, the largest device will be preferred, and the performance difference between MB and HP is insignificant. The gain referenced in Figure 4.4(b) is the maximum gain as the input power was swept. For HP and MB devices at the set frequency, there is no substantial difference in gain.

The takeaway for cascode amplifier cell design is that MB devices expand the usable output voltage range at the cost of a reduction in current-handling capability. Using an MB CB device in the cascode does not result in a large reduction in the maximum operation frequency, or in the gain, or the $1dB$ gain compression of the cell at frequencies well below the peak f_T . For high power applications, larger devices should be selected due to their high gain and OP_{1dB} .

4.4 RF Reliability of MB vs. HP Cascode Structures

In order to make educated decisions about the use of HP vs. MB devices, the reliability of cascode amplifier cells clearly must be explored in addition to the performance discussed above. To quantify the reliability tradeoff of HP and MB cascode cells under large output swings, RF stress measurements were performed, combining aggressive bias and large output swing to accelerate damage. RF stress was performed for 3,600 seconds, stopping periodically to measure the stress damage in the CB transistor. Because both mixed-mode

(MM) and high current (HC) stress result in increased base leakage, change in base current for the CB device is used to monitor the relative rates of damage. By monitoring the change in base current, it is possible to monitor the relative rate of damage in each cascode cell.

Figure 4.5 gives two example load-lines overlaid on a set of output curves for a cascode structure. Both load-lines represent an output power of 6 dBm fed into a load impedance of 50Ω . Condition 1, at $V_{BE} = 0.91V$ and $V_{CB} = 2V$, represents a bias near the peak f_T of the structures. The second condition, at a reduced $V_{BE} = 0.85V$ and increased $V_{CB} = 3.5V$, is chosen arbitrarily with increased V_{CB} and decreased I_{bias} as an alternate condition a designer might use to take advantage of the different operating limits of the MB device. The DC bias is represented on the two plots by a solid dot at the center of the load line.

Because the load-line swings across high voltages and currents, the CB device will be subject to both mixed-mode and high-current stress. Mixed-mode (MM) damage occurs at large collector-base voltage and moderate-to-low current bias (below $J_{C,peak}$), and is driven by the creation of hot carriers across the collector-base junction [14]. High current (HC) damage occurs under high current density ($\gg J_{C,peak}$) and low field, and is driven by high Auger recombination [15]. DC stress of single devices suggests that MB devices are more resilient to MM damage, while HP devices are more resilient to HC damage [39].

The results for the largest structure, with CB and CE device $L_E = 8.0\mu m$, are depicted in Figure 4.6, where the relative shift in base current at constant $V_{BE} = 0.7V$ is shown. Under both conditions, the MB cascode exhibits negligible damage compared to the substantial damage experienced by the HP version.

Figure 4.7 shows the same outcome for a smaller device structure. Under the first stress condition, the damage is higher for the MB device, but for the second condition, the HP device is more heavily damaged. The reliability difference results because the load-line for each stress condition swings into a different operative damage region. Condition 1 swings the output current well past the HC damage threshold for MB devices but not

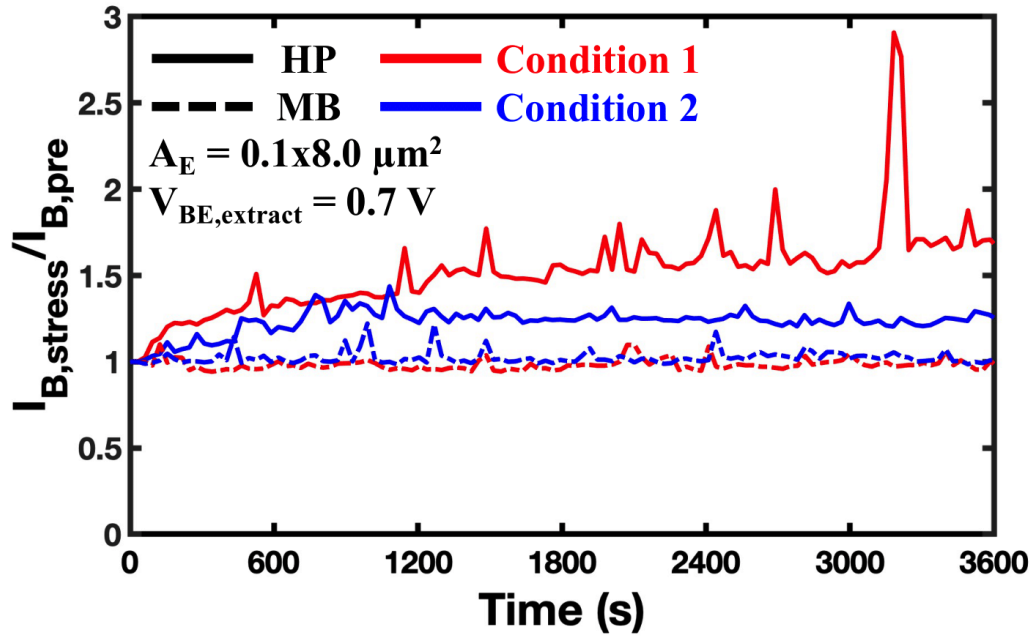


Figure 4.6: Change in base current leakage for $8\mu\text{m}$ HP and MB cascode structures extracted at $V_{BE} = 0.7V$.

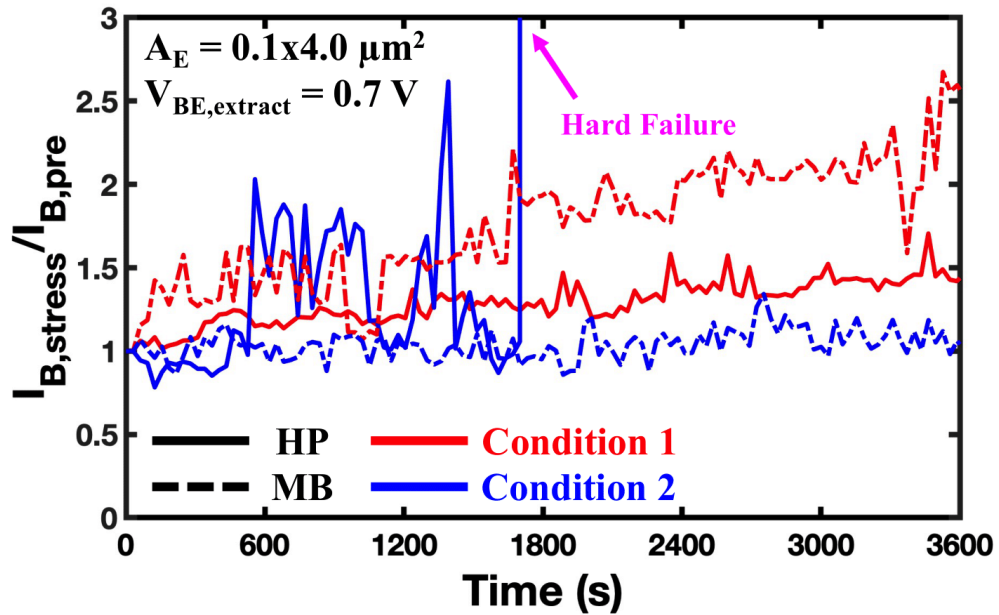


Figure 4.7: Change in base current leakage for $4\mu\text{m}$ HP and MB cascode structures extracted at $V_{BE} = 0.7V$.

for HP devices, thus subjecting the MB device to more damage. Conversely, condition 2 doesn't swing to as high an output current, and the MB device is not subjected to extra HC damage. Condition 2 is at a higher voltage bias, however, meaning that it swings to a high enough V_{CB} for the HP cascode to experience MM damage but not the MB cascode, resulting in overall worse reliability for the HP cell.

It is important to note that both size cascodes are driven to the same output power and output load, meaning they have the same output current swing. The smaller device experiences a larger J_C swing due to its reduced area. Because HC damage is dependent on current density, the smaller device will thus be more susceptible to HC damage. This is the key reason why condition 1, with a higher bias current, has a geometry dependence for the "most reliable" cascode, whereas condition 2, which has a bias current low enough to avoid swinging into the HC damage regime, shows consistently better reliability with a MB top device.

Overall, the results demonstrate that the MB cascode reliability can be improved by adjusting the biasing scheme, in order to operate at a higher voltage but a lower current. At frequencies well below f_T , this can be accomplished with minimal cost to performance, and results in improved lifetime of the cascode. For applications requiring operation closer to peak f_T , it will become necessary to use HP devices for the CB stage of the cascode. For these applications, circuit designers should aim instead to bias at low voltage and high current in order to maximize circuit lifetime.

4.5 Summary

This paper has investigated the reliability and performance trade-offs of cascode structures using high-performance (HP) and medium breakdown (MB) common-base (CB) devices. First, the performance and reliability differences of HP and MB transistors were discussed. DC Measurements were performed on single devices and then on cascode structures to establish a DC safe operating limit. Small- and large-signal RF measurements indicated a

small decrease in peak f_T for cascodes with MB CB devices, but that the gain and OP_{1dB} at frequencies well below f_T were comparable between HP and MB structures. RF stress measurements indicate that the MB cascodes are more stress resilient than HP cascodes, especially at large transistor sizes. For smaller devices, careful selection of the bias point will determine whether HP or MB devices are more reliable. At frequencies approaching f_T , designers have no choice but to use HP devices, and will instead have to maximize device current swing and minimize voltage swing to improve device lifetime.

CHAPTER 5

CONCLUSION

5.1 Contributions

The results presented in Chapter 3 on dynamic breakdown mechanisms in a fourth-generation SiGe BiCMOS technology are significant for circuits in which aggressive biasing schemes are applied to maximize device performance. Conventional device characterization involves using purely DC measurements in order to establish a “traditional” safe operating area (SOA). It was shown that as rapid measurements were taken to vary the amount of self-heating within the transistor, the dominant mechanism causing uncontrollable I_C increase and breakdown was changed. For practical applications, where the device may be dynamically biased to minimize idle power consumption or where the output waveform may dynamically swing beyond the traditional SOA, it is important to identify the dominant breakdown effect so that the circuit may be designed for maximum lifetime. The results in this chapter were published and presented at the 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium.

The results in Chapter 4 focus on the performance and reliability tradeoff of cascode cells comprised of SiGe heterojunction bipolar transistors when multiple device profiles are available within a technology platform, with different performance metrics and operation limits. In this study, a cursory advantage into the small- and large-signal performance of these cascode cells was combined with stress measurements to quantify the change in performance and reliability of the high performance (HP) and medium breakdown (MB) device variants. The results and analysis were published and presented at the 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium. An extension of the work is currently in preparation and will be submitted for publication

in IEEE Transactions on Electron Devices.

5.2 Future Work

5.2.1 RF Breakdown and Reliability Comparison of SiGe HBTs Optimized for Performance and Breakdown

In order to elevate device-level understanding of device performance and reliability to circuit-relevant guidelines, it is necessary to expand measurement of devices to imitate how devices will be used, and how devices are likely to fail, in practical applications. RF breakdown is a measurement technique that sets a hard limit for bias voltage plus output swing of a high output power amplifier. These limits will be of interest to circuit designers because they establish absolute limits for the operation of devices in amplifier circuits.

Load-pull measurement techniques can also be used to alter the dynamic output swing of the amplifier. Coupled with the results from Chapters 3 and 4, this analysis can be used to co-optimize device SOA, lifetime, and performance in “reliability-aware” circuit designs. These designs can then help push both the performance and lifetime of existing technologies.

5.2.2 Profile Optimization of Performance and Reliability Tradeoffs of SiGe HBTs

As mentioned in Chapter 1, and measured in Chapter 4, SiGe BiCMOS technology platforms often compensate for the reliability tradeoff of a highly-scaled device by including an alternate profile with more conservative performance but improved reliability. For the technology in question, this is achieved by altering the selectively implanted collector profile in order to delay breakdown, but other techniques are likely available to create device variations in a single technology platform with minimal mask deviation. Measurement of experimental hardware, coupled with TCAD simulation of different profiles can allow device designers to determine profile alterations to optimize performance and reliability of SiGe HBTs based on the intended application.

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