GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION
SPONSORED PROJECT INITIATION

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Date: 1/16/79

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Project No: A-2294

Project Director: Mr. Glenn E. Riley

Sponsor: US Army Missile R&D Command; Attn: DRDMI-ICBB; Redstone Arsenal, AL 35809

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SPONSORED PROJECT TERMINATION

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Project No: A-2294

Project Director: Mr. G. E. Riley

Sponsor: U.S. Army Missile R&D Command; ATTN: DRDMI-ICBB; Redstone Arsenal, AL 35809

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FINAL REPORT

ELECTRONIC TARGET SIGNAL GENERATOR (ETSG) HARDWARE DESIGN AND FABRICATION

By

M.J. Sinclair

Contract Number DAAK40-78-D-0008
Delivery Order Numbers 0007 and 0009

Georgia Tech Project Numbers A-2294 and A-2316

Prepared for

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)* Following the design phase of this program, a first-pass PC Card implementation was attempted. A major effort in isolated card diagnostics was realized as the circuits feeding and receiving information from the device under test were not always available. As a result, an intelligent logic analyzer and word generator was designed and constructed and software written to emulate the input and output signals of the PC card being tested. This report contains a brief description of the systems submodules which exist in final card-rack-mounted PC boards.		

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FOREWORD

This report was prepared by the Engineering Experiment Station at Georgia Tech under Contract DAAK40-78-D-0008, Delivery Order Nos. 0007 and 0009. The work described was performed in the Electro-Optics Division of the Electromagnetics Laboratory under the supervision of G.E. Riley, Program Director. The objectives and results of the work cover the hardware design and fabrication phase of the Electronic Target Signal Generator (ETSG) development. The assistance and technical advice of D. Dublin, contract technical monitor at MICOM is gratefully acknowledged. The contributions by G.E. Riley, J.E. Tumblin, A. Davis and G.R. Loefer of the Engineering Experiment Station were most helpful during this phase of the program.

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I. INTRODUCTION AND SUMMARY

The conceptual design of a flexible, programmable, hybrid computer controlled Electronic Target Signal Generator (ETSG) for electro-optical seeker simulation work at MIRADCOM has been completed. The ETSG generates a simulated signal equivalent to the detector output of a variety of electro-optical seekers such as REDEYE, STINGER, STINGER/POST as well as known or postulated electro-optical threat seekers.

The basic concept for the ETSG is a hybrid general purpose and special purpose computer which can create and control up to 20 sources of specified shape, size, spatial orientation, spatial position, intensity, and intensity gradient. The simulation of a particular target/background/countermeasure scenario can be made by selecting various combinations of sources to represent the various parts of the total target signature. Each source is then controlled independently.

An operator's console and display are used to initialize the simulation, and display dynamic position of the seeker field-of-view (FOV) and each target/source position relative to the FOV center. The simulation must be initialized for seeker, target, flare and pulse jammer paramenters. After initialization the ETSG accepts dynamic target/source parameters from the CDC 6600 via the Direct Cell Interface. These parameters are then mapped onto a memory representing the seeker image plane. This image plane is then convolved with the seeker scan pattern which may be a reticle or scan pattern such as a rosette. For scan systems other than reticle, scan signals must be supplied to the ETSG via the seeker electronics or other electronics external to the ETSG. Using either prestored reticle patterns or scan signals, the scan is convolved with the seeker image plane. The resulting digital signal is converted to analog signal, ripple filtered and output as the seeker detector signal. This signal is supplied directly to the seeker electronics where it is used to generate gyro torquing signals and guidance commands

for AD-4 analog computer. The AD-4 supplies flight data to the CDC 6600 which has a 6-DOF airframe simulation. New target/source positions relative to an inertia frame of reference are calculated in terms of missile position, target position and gyro gimbal angels. These outputs are supplied to the direct cell for temporary storage. When the ETSG has completed a new data sample, a priority interrupt to the CDC 6600 is generated. This allows the 6600 to clear itself for the next calculation. Simultaneous with this interrupt signal, a handshake operation between the ETSG and Direct Cell Interface allows new target data to be transferred to the ETSG.

This contract provided for the specific fabrication of the printed circuit boards and associated components of the ETSG. Console, operation, and diagnostic software was also produced for the ETSG.

II. DESCRIPTION OF MAJOR SUBMODULES

Following the design stage of this task, a first-pass PC card implementation was attempted. A major effort in isolated card diagnostics was realized as the circuits feeding and receiving information from the device under test were not always available. As a result, an intelligent logic analyzer and word generator was designed and constructed and software written to emulate the input and output signals of the PC card being tested.

The following is a brief description of the system's submodules which exist in final card rack mounted PC boards. Refer to the ETSG BLOCK DIAGRAM of Figure 1 for system location.

INITIALIZATION PROCESSOR AND CONSOLE

A commercially available MOTOROLA EXORCISOR was purchased for this requirement. It consists of a 1 MHz 6800 microprocessor, 48K bytes of RAM, dual 8" floppy disks, and a serial interface. All of the ETSG

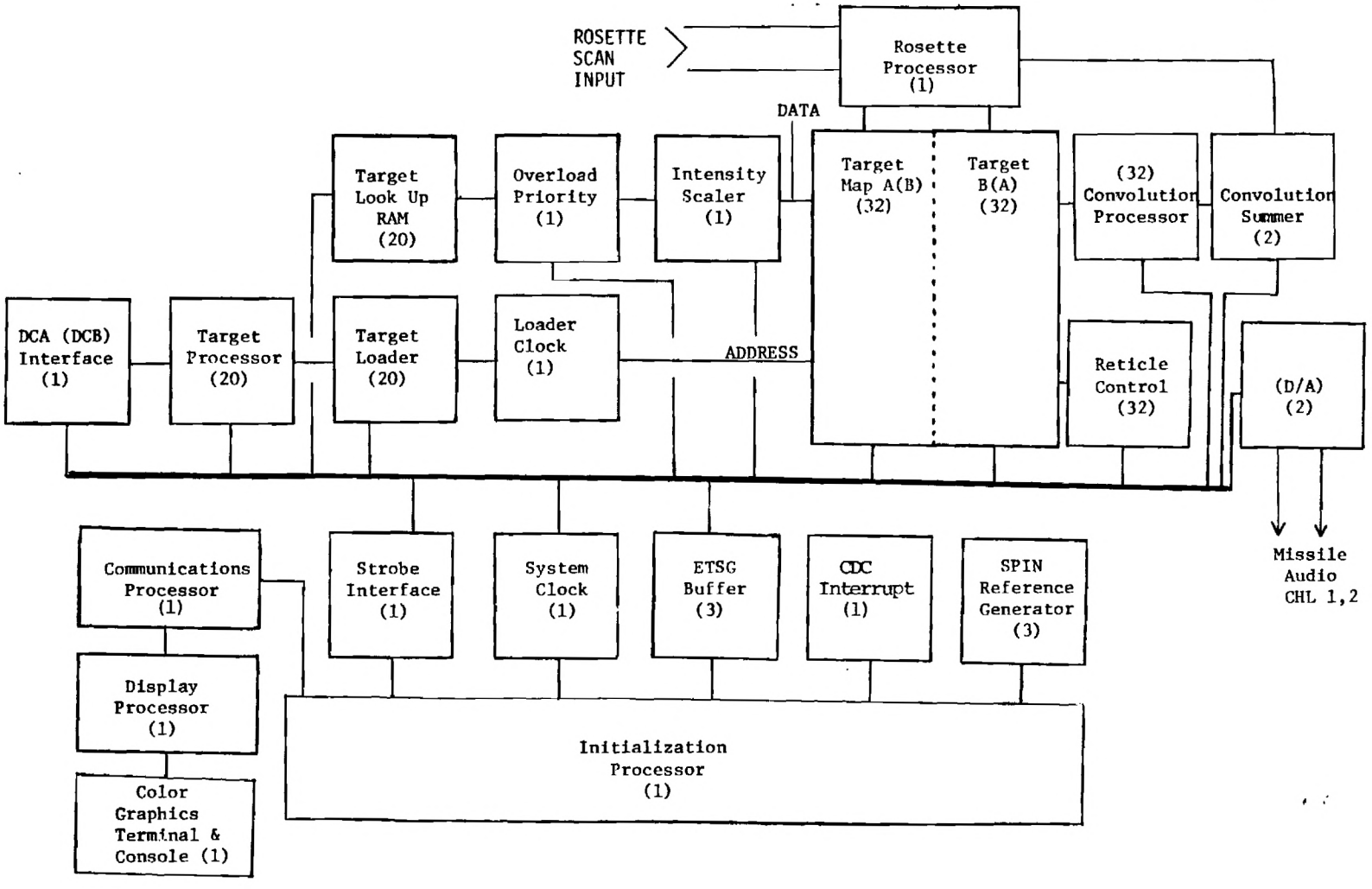

FIGURE 1
ETSG BLOCK DIAGRAM

software was written on this machine using a FORTRAN compiler. A commercially purchased ISC 8002 color graphics terminal was used as the console monitor and ETSG graphics display.

- DISPLAY PROCESSOR

A 6800 microprocessor based controller samples the incoming DCA(DCB) target LOS data and roll angle and presents the color graphics terminal with a derolled TFOV image with colors defining the targets.

COMMUNICATIONS INTERFACE

This submodule is controlled by a 6800 microprocessor which augments the color graphics terminal. It will initialize the terminal as either a graphics display or alphanumeric console but not allow intermixing (which was found to be intolerable when using the graphics terminal alone). This device will also intelligently couple to a modem or printer on command from the keyboard.

STROBE INTERFACE

A two port 4K byte RAM is used as a programmable 32K bit generator. The bit pattern is loaded into the RAM by the initializing processor (IP). A separate 32 KHz clock then sequences through each bit in succession providing the strobbed jammer's temporal signature. This bit serial signal is processed by the TARGET MAP as the strobe bit flag.

MASTER CLOCK

A phase locked digital frequency synthesizer is locked to the frequency specified in a parameter sent by the DCA (DCB). Various other timing signals are derived from this frequency to synchronously

drive the submodules of the ETSG. Thus, the ETSG's throughput rate is directly affected by this specified parameter. In this case of a reticle seeker, this frequency is equal to the spin rate.

ETSG BUFFER

A digital buffer and address decoder was implemented to interface various ETSG subsystems with the IP. The address logic performs window mapping of the ETSG's 836K+ bytes of RAM to the IP's 4K byte window.

CDC INTERRUPT

A thumbwheel settable pulse generator is provided to produce pulses with periods ranging from .1 to 99.9 milliseconds in .1 millisecond increments. These pulses are sent to the CDC 6600 for interrupt timing.

SPIN REFERENCE

Three analog spin reference signals are provided to interface with the breadboard and AD-4 computer. One of the spin reference sine waves is phase locked to the ETSG's system clock while the others have software selectable phase offsets from the first reference. These phase offsets can be specified in 1.8^{o} increments.

DCA (DCB) INTERFACE

Proper digital transmitters and receivers are provided along with compatible handshaking signals to interface with either the DIRECT CELL A or B. This circuit provides the ETSG with dynamic target and seeker parameters.

TARGET CPU

The function of this module is to translate the downloaded DCA (DCB) information into useable signals so the TARGET LOADER can load the TARGET MAP with LOS target coordinates. During initialization, the CPU's are loaded with temporal irradiance history curves if the target is a flare or strobe flag if that target is to be part of the strobbed jammer. These processors are also based on the 6800 microprocessor and utilize a high speed 16 x 16 bit bipolar multiplier to reduce computing time to around 700 microseconds per target transfer.

LOADER CLOCK

The function of this module is to provide the TARGET LOADERS with a target map address sequence whereby they may calculate the presence or absence of data for the particular pixel being loaded.

TARGET LOADER

With the proper information from its TARGET CPU, the TARGET LOADER's function is to provide a digital signal indicating the presence or absence of data from that particular target in the TARGET MAP pixle being addressed. A VARIABLE PATH ADDRESSING algorithm is implemented for this function in bipolar hardware.

TARGET LOOKUP RAM

Each of the 20 TARGET LOOKUP RAM modules contain up to three separate 4K byte bipolar RAM memories. These are loaded during initialization with cross sectional irradiant "views" of the target for difaspects angles. During a run, irradiance values are mapped in the TARGET MAP provided:

1. That target is in the FOV
2. That target has the highest priority in case of contention with another target,
3. The data is non-zero, and
4. If that target is designated as a strobbed target, the strobe function must be "on".

OVERLAP PRIORITY

As described previously, in case of contention of two or more target loaders desiring to map data into the same target map pixel, this circuit arbitrates as a function of initialized target priorities - the highest priority will map its data.

INTENSITY SCALER

This submodule is a floating point binary multiplier and normalizes the mapped irradiance as a function of range, whether or not the target is resolved, initial absolute target irradiance, and flare time history should the target be designated as such. The INTENSITY SCALER provides the data to be mapped into the TARGET MAP.

TARGET MAP

Two 4K x 12 bit bipolar RAM modules constitute each TARGET MAP. As the INTENSITY SCALER and TARGET LOADER are refreshing one of the maps with a new target scene, the other is split into 16 parallel sections (for speed) and the total intensity summed through a RETICLE MASK. The maps are then swapped and refresh and summation repeats. Eight of twelve bits represent pixel intensity as a floating point binary number. One bit indicates the pixel's polarity with respect to the background and another target flag. Two bits are presently uncommitted.

CONVOLUTION PROCESSOR

During summation, the TARGET MAP address logic causes successive pixel intensities to be accumulated as a binary floating point number. Each of the 16 TARGET MAP sections has its own convolution processor which presents partial sums to the CONVOLUTION SUMMER.

RETICLE CONTROL (Con Scan)

As the summation process proceeds, a one bit map of the reticle is addressed along with the TARGET MAP and allows data to pass on if the corresponding reticle pixel is 'transparent'. After each TFOV summation, the reticle is 'rotated' by 1.8 degrees and the process repeats until the reticle has been through 360 degrees or 200 repetitions. Each 16th section of the TARGET MAP has a complete 4K x 1 bit RETICLE RAM map that has been loaded with one bit a 'picture' of the reticle transmission. During operation, a corresponding portion of the RETICLE MAP is address-overlayed with the target map section and a pixel by pixel ending procudes the data to be accumulated by the CONVOLUTION SUMMER. The address-overlay logic includes a reticle rotation RAM which is loaded with the path address that the particular TARGET MAP section traverses with respect to the RETICLE MAP during rotation.

ROSETTE PROCESSOR

To implement a rosette scan system, rectilinear scan signals are presented to the ROSETTE PROCESSOR which, in turn, addresses the corresponding pixel of the TARGET MAP as well as the surrounding 8 pixels (for a system with an IFOV of 3 x 3 pixels). The target map data is accumulated for each IFOV sample via the CONVOLUTION SUMMER.

CONVOLUTION SUMMER

Depending on the seeker type chosen, either the ROSETTE PROCESSOR or CONVOLUTION PROCESSOR inputs to the convolution summer where a number is computed to be the final IFOV or TFOV image intensity. This subsystem also contains a floating point accumulator.

D/A

The DIGITAL TO ANALOG converter is composed of a floating point to straight binary converter and three 14 bit linear DACs. Extended dynamic is achieved by converting AGC signals (from the breadboard) to digital to extend the range of the 14 bit DACs.

From the target map to the D/A, two separate and independent channels are provided to emulate two spectral bands. A separate D/A is also provided for a grey level background intensity for each spectral channel.

III. CONCLUSIONS

Final PC board checkout is in progress with the majority of the system software written. One target chain (from target CPU to convolution summer) has been debugged and is being used to check out the other boards. Some work remains on the D/A boards and direct cell interfaces to work in final form. IP peripheral boards - master clock, ETSG buffer, CDC interrupt strobe interfacing, spin reference, display CPU, and communications processor - have been thoroughly checked out and are in final PC form.

The hardware work that remains is interfacing the direct cell module and verifying the D/A circuit. Individual hand assembled diagnostic software has been written but only board level using our INTERFACE PROCESSOR logic analyzer. When a completed system is operating, the system level diagnostic software will be checked out and rewritten if necessary.

An attempt will be made to forward a working direct cell interface for MICOM verification with the DCA and DCB.

Cabinet fabrication is nearly complete with AC and DC power wiring remaining. Most of the interconnecting ribbon cables have been fabricated and are waiting PC card installation.