

Stacked Low-Inertia Converter or Solid-State Transformer: Modeling and Model Predictive Priority-Shifting Control for Voltage Balance

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Abstract—This paper presents control challenges of stacked low-inertia converter (SLIC) or cascaded reduced dc-link solid-state transformer (SST) and proposes a novel model predictive priority-shifting (MPPS) control with implicit modulator and a discrete-time large-signal model for voltage balancing and dc-link regulation. Low-inertia converters, featuring small electrolytic capacitor-less dc links, dramatically reduce cost, size, and weight compared to conventional solutions. However, without a large dc-link buffer, the input and output are tightly coupled, leading to significant control challenges. The control becomes even more challenging with these converters stacked input-series output-parallel (ISOP) for medium-voltage (MV) grid, which causes coupling between the modules besides the coupling within each module. This paper analyzes the multi-objective, multi-degree of freedom control problem, using the modular soft-switching solid-state transformer (M-S4T) as an example of the SLIC. First, distribution of control efforts under controller saturation is critical because multiple control objectives can be conflicting, especially when the module voltages are unbalanced and are being restored. The MPPS can shift the priorities to address this issue. Second, due to the low inertia and high dc-link ripple, classic space vector pulse-width modulation (SVPWM), average model with small-ripple assumption, and control design based on small-signal model cannot accurately modulate, model, and control the nonlinear reduced dc link. Therefore, a discrete-time large-signal model of the M-S4T is established to derive the predictive control in the MPPS. The MPPS and the PI control are compared in MV simulations to show the issue of applying the PI to the SLIC and the effectiveness of the MPPS for voltage balancing and dc-link regulation in a deadbeat manner. Finally, the proposed control is tested on a 5 kV ISOP SiC SST prototype to verify priority shifting to address controller saturation issue and fast and robust voltage balancing.

Index Terms—DC transformer (DCT), digital multivariable control, input-series output-parallel (ISOP), isolated bidirectional

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dc-dc converter (IBDC), medium-voltage DC (MVDC), model predictive control (MPC), modular multilevel solid-state transformer (SST), power and voltage balancing, power electronic transformer (PET), stacked low-inertia converter (SLIC).

I. INTRODUCTION

MEDIUM-VOLTAGE (MV) high-power converters are widely used in rolling mills, pipeline pumps, electric propulsion, power quality, medium-voltage DC (MVDC) distribution, wind energy integration, and solar farm grid interface applications [1]-[6]. Improving the power density, efficiency, and reliability with reduced costs has attracted tremendous interest in the power electronics community for the last several decades. The passive components, especially the dc-link capacitor or the dc-link inductor, account normally for more than 20% of the converter size and weight [7]. Furthermore, the electrolytic capacitor is usually the weakest link in the power converters, limiting the reliability and the operating temperature. In order to improve the power density, reliability, and operating temperature, decreasing the dc-link energy storage and employing film capacitor can be a viable method [8]-[10]. The converter with a relatively small dc link can be referred to as a low-inertia converter or a reduced dc-link converter. Despite the benefits, control of such a converter is a huge challenge because of the increased coupling between the input and output stages.

The control can be even more challenging in the SLIC owing to the additional coupling between the modules. In MV converters, either the devices or the converter modules are connected in series to achieve high voltages [1]-[2], [11]-[13]. For the series-connected devices, snubbers, auxiliary circuits or active gate drivers are required for voltage balancing, which adds additional complexity [11]-[13]. A modular approach is easy to scale for higher voltage and power, and achieves redundancy for improved reliability [2]-[4]. The major challenge in modular converters, e.g., the solid-state transformers (SST) or power electronic transformers (PET) in [14]-[18] is to dynamically balance the voltage across series-connected modules with fast and robust control. This problem is typically solved using a large dc link as an energy buffer and different bandwidths for different control loops to decouple the interaction between the input stage and output stage and between voltage balancing control and load voltage regulation. The large dc link can absorb the transient power mismatch during the control reaction time. In [14]-[18], the cascaded H-

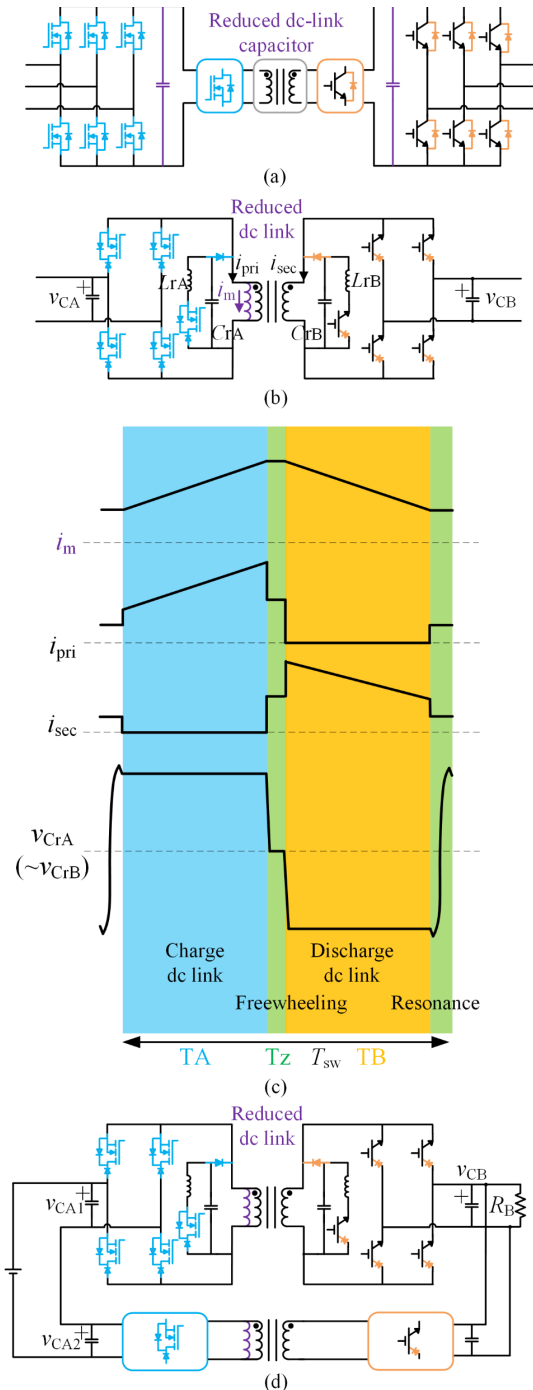


Fig. 1. (a) A low-inertia or a reduced dc-link converter. Take a conventional three-stage solid-state transformer as an example. (b) A representative of the low-inertia converter: soft-switching solid-state transformer (S4T). (c) The conceptual operation diagram of the S4T. (d) A representative of the SLIC: a modular-S4T (M-S4T) converter.

bridge (CHB) stage and the isolated bidirectional dc-dc converter (IBDC) stage are controlled accordingly with separate PI controllers to achieve different objectives. In [15], the CHBs control average dc-link voltage and voltage balancing, while the IBDCs regulate the LV-side voltage. In [18], the IBDCs have their PI control loops for the voltage

balancing, while the CHBs control the overall power drawn from the grid to regulate the total dc-link voltages.

However, in the stacked low-inertia converters (SLIC) with reduced dc links, the voltage balancing and dc-link control problem must be addressed holistically with prioritized control objectives and high-bandwidth control due to the inherent couplings in the SLIC. With a reduced dc link, disturbances can propagate easily and result in large fluctuations of the state variables and controller saturation. In addition to the series-side voltage balancing, other control objectives that should be coordinated include regulating the dc link and the output voltages/currents. For this multi-objective and multi-degree of freedom control problem, the major challenge is how to trade off the control efforts to realize the multiple objectives with high bandwidth and address the possible controller saturation under large disturbances when not all the control objectives can be met. The PI control which works well for power and balance control in conventional high-inertia MV converters in [14]–[18] cannot enable fast and stable operation of the SLIC. A control method called model predictive priority-shifting (MPPS) control is thereby proposed for the SLIC.

Appropriate modelling of the SLIC is another key issue. Without an accurate model, high-performance predictive control is impossible. First, traditional continuous-time averaged modelling [19] and small-signal model-based control design work well in high-inertia converters tuned for lower bandwidth, e.g., [18] yet they cannot capture the SLIC's dc-link dynamics accurately because the low ripple assumption does not hold. Second, digital controlled converters including MV SSTs and PETs can be modelled in the discrete-time domain more precisely. Therefore, a discrete-time large-signal model of the SLIC is proposed, which forms the basis for fast predictive control in the MPPS for a deadbeat response on the dc link.

A dc-dc modular soft-switching solid-state transformer (M-S4T) with a reduced dc link is selected as an example of the SLIC to explore the control problem and verify the proposed MPPS control. However, the discussion is equally applicable to any low-inertia converters or solid-state transformers. The soft-switching solid-state transformer (S4T) with reduced conduction loss [20] in Fig. 1 (b) is a single-stage solid-state transformer with one reverse-blocking bridge on each side of a high-frequency transformer and auxiliary resonant circuits to achieve full load range zero-voltage switching (ZVS) [20]–[23]. The operation mode is similar to a flyback converter, but with restricted duty ratio because of the lost time for the ZVS in Fig. 1 (c). The transformer magnetizing inductance L_m acts as an inductive dc link and is sized for 40%–60% peak-peak ripple to reduce transformer cost, size, and leakage inductance. Hence, the S4T is considered as a low-inertia converter. For MV applications, the S4T modules can be stacked to be M-S4T as shown in Fig. 1 (d).

The rest of the paper is organized as follows. Section II explains the multi-objective, multi-degree of freedom SLIC control problem. Section III presents the challenges and

simulation results of applying a conventional PI controller to achieve a fast and stable operation of the SLIC. Section IV is dedicated to the challenges of employing conventional hysteresis control, model predictive control, and deadbeat control for the SLIC. Section V presents the basic principles of the MPPS and the large-signal model of the SLIC, whereas simulation results are described in Section VI. Experimental results on a MV M-S4T prototype verify the proposed MPPS control in Section VII. Section VIII concludes the paper.

II. KEY REQUIREMENTS OF SLIC CONTROL – LARGE-SIGNAL MODELING, PRIORITY SHIFTING, AND HIGH BANDWIDTH

A. Low-Inertia Converters

In a conventional converter with standard control, the dc link is sized for very small peak-to-peak ripple, typically $< 1\%$ for a voltage-source converter (VSC) in steady state so that the voltage overshoot on the dc link is limited under abrupt load change and stability is ensured [24]–[26]. In a low-inertia converter, the dc-link storage is intentionally sized smaller to reduce size and cost. The inertia factor (IF) in (1) can be used to compare low-inertia and high-inertia converters. $\sum E_{\text{filter}}$ and $\sum E_{\text{dc_Link}}$ are energy stored in the filters and the dc links of the converter. P_{rated} is rated power. f_{sw} is switching frequency.

$$IF = \frac{\sum E_{\text{filter}} + \sum E_{\text{dc_Link}}}{P_{\text{rated}}/f_{\text{sw}}} \quad (1)$$

For a reduced dc-link or low-inertia VSC, e.g., the LV converter prototype in [24], the IF is 7.49 for 5% peak-peak ripple. If the dc-link capacitance is sized 10X larger as a conventional VSC, the IF will be 68.24. In another example, the conventional LV VSC prototype in [25] has an IF of 78.67. The S4T, as a low-inertia converter, has a 7.34 IF for the prototype in [22]. Low-inertia converter modules can be stacked to be the SLIC for higher voltage applications.

B. Multi-Objective Multi-Degree-Of-Freedom Problem

The multiple control objectives of the SLIC are described as follows:

- First and foremost, to ensure the converter can robustly and safely process power up to its nominal or desired power rating, the dc-link state variable should be maintained within certain ranges. For a current-source converter, if an overshoot occurs on the dc-link current, the dc-link inductor can saturate and the device and the converter reliability can suffer with increased thermal stress. Consider a case where a transient results in controller saturation and the controller commands full power to restore voltage balance promptly. If the dc-link current now drops below its reference, the converter can only be commanded up to a fraction of its nominal power, which worsens the controller saturation condition.
- Second, the stacked-side voltages of converter modules should be regulated to ensure safe operation of the system. If the voltages exceed the safe operating area of the devices, the devices will break down immediately.

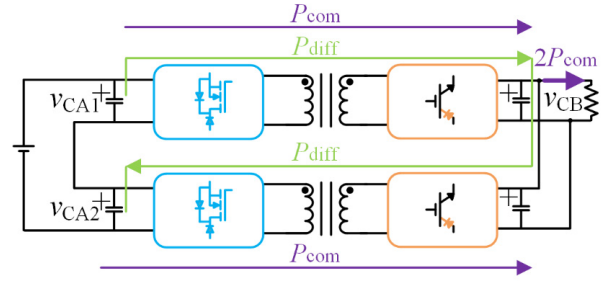


Fig. 2. The conceptual power flow diagram of the two-module M-S4T under stacked-side large-signal disturbance. P_{diff} balances the stacked-side capacitor voltages. P_{com} supplies the load power.

- Third, the load voltage and current should track their references.

Considering a two-module case shown in Fig. 1 (d), the objectives translate to the mismatch between the stacked-side voltage of module 1 (v_{CA1}) and the stacked-side voltage of module 2 (v_{CA2}), the magnetizing current of module 1 (i_{m1}), the magnetizing current of module 2 (i_{m2}), and the output voltage of the two modules (v_{CB}). As the converter is a current-source converter, the magnetizing current is its dc-link current. The degrees of freedom are the input and output bridge duty cycles. In a single S4T with a constant switching frequency, we have two degrees of freedom, i.e., A bridge or MV bridge (blue in Fig. 1) duty cycle (D_A), and B bridge or LV bridge (orange in Fig. 1) duty cycle (D_B). For the two-module cases, four degrees of freedom exists, i.e., D_{A1} , D_{A2} , D_{B1} , and D_{B2} .

C. Small-Signal vs Large-Signal Disturbance and Modelling

In a high-inertia converter, the dc-link storage absorbs all the transients and the controller typically experiences huge transients only during faults or startup/shutdown. Normally, special control actions are prepared in advance for these conditions. Hence, for a high-inertia converter, a small-signal model based control is sufficient. In a low-inertia converter, even during steady state, a large ripple exists across the dc-link. Considering the controller saturation case under a large-signal disturbance for the SLIC, a controller design based on a large-signal model is crucial and necessary for a fast response and robustness.

D. The Need for Priority Shifting

In case of large-signal disturbances on the stacked-side capacitor voltages, which can potentially occur under lightning surges, insertion, bypass, and fault tolerance of individual modules, etc., the controller needs to restore the capacitor voltage balance as quickly as possible. Irrespective of the control method, a differential-mode power will flow between the two modules to balance the voltage in Fig. 2. The common-mode power will supply the load power. However, each module has a total power saturation limit, e.g., (2) for the upper module in Fig. 2.

$$|P_{\text{com}} + P_{\text{diff}}| < P_{\text{overload_limit}} \quad (2)$$

Suppose a case where the converter is balanced and delivering 0.8 pu load, i.e., $P_{\text{diff}} = 0$, $P_{\text{com}} = 0.8$. If a large

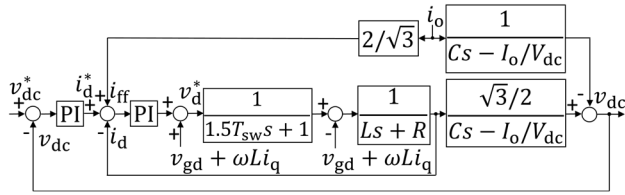


Fig. 3. The standard synchronous-reference-frame dual-loop PI control of the grid-side converter in a BTB VSC with load current feedforward [25], [27]-[28]. A $1.5T_{sw}$ computation, modulation and sampling delay is considered [28]. L and R are the filter's inductance and resistance. C is the dc-link capacitance. T_{sw} is the switching period. $v_{gd,q}$ and $i_{d,q}$ are grid voltages and currents in the synchronous dq reference frame, respectively.

disturbance occurs across the series-connected capacitors, with a fast control method, the differential-mode power required for balancing will be high, and one or more modules will saturate at 1.0 pu. If the 0.8 pu P_{com} takes priority, the balancing effort will be restricted to 0.2 pu according to (2), i.e., $P_{diff} = 0.2$, $P_{com} = 0.8$. Restoring the voltage balance will take more time, while any overvoltage exceeding the limits will immediately cause device breakdown. A more severe case to illustrate the significance of control efforts distribution would be full load condition, i.e., $P_{diff} = 0$, $P_{com} = 1$. If the 1 pu P_{com} , i.e., load power delivery takes priority, we will have balancing efforts restricted to 0 pu and the voltage balance can take very long time. Therefore, if the unbalance is large, the control efforts distribution should be $P_{diff} = 1$, $P_{com} = 0$. It should be noted that for traditional controls which cannot prioritize control objectives, the magnitude of effort devoted to the most serious concern (e.g., module overvoltage) is limited.

In other words, under an unbalanced condition, four degrees of freedom, i.e., D_{A1} , D_{A2} , D_{B1} , D_{B2} are not fully independent under the controller saturation constraint, e.g., $D_{A1} + D_{B1} < 1$. Therefore, not all the four variables, i.e., $v_{CA1} - v_{CA2}$, i_{m1} , i_{m2} , v_{CB} can be regulated with full control efforts. Unfortunately, load voltage (v_{CB}) regulation has to be temporarily given up to achieve capacitor voltage balancing as quickly as possible.

Under large-signal disturbances, controller saturation is expected because of physical constraints, e.g., the converter power rating. Consequently, the control objectives should be prioritized and only the most important variables for safe operation, the dc-link current and the stacked capacitor voltage, should be fully controlled. Though the large transient unbalance rarely occurs, considering the worst case is essential to ensure safety and robustness.

E. The Need for High Bandwidth Control

The low-inertia nature of the SLIC requires high-bandwidth control because the reduced dc link cannot store much energy and can suffer from large overshoot or stability issue under rapid load-current change with conventional control. To further explain this low-inertia challenge, a 6 kHz 25kW 380V back-to-back (BTB) VSC with 700 V dc-link voltage is taken as an example. The block diagram of the classic dual-loop PI control with load current feedforward in [25], [27] is shown in Fig. 3 [28], where i_o is the current drawn from the dc link into the load-side converter. The symmetrical optimum PI tuning

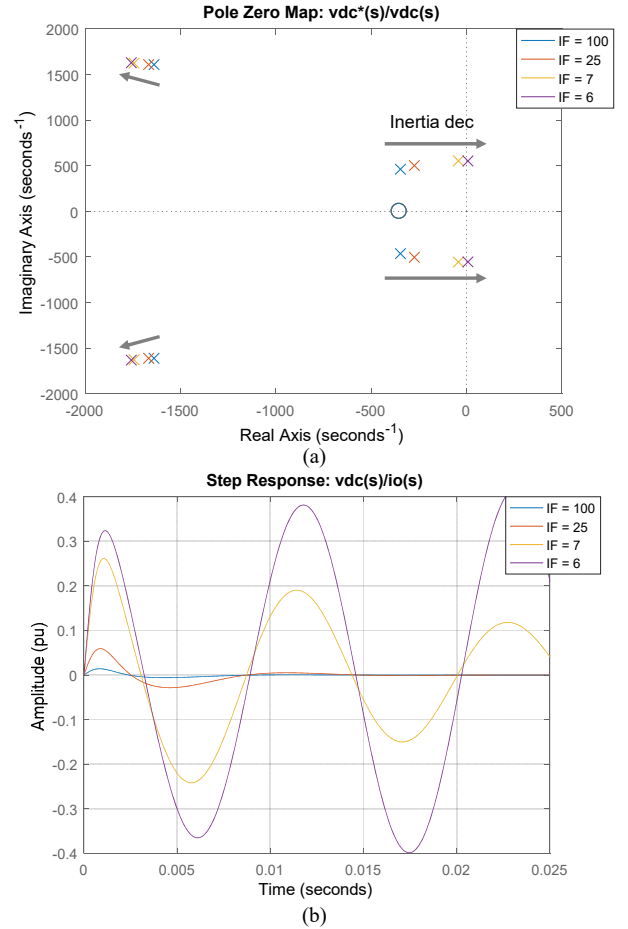


Fig. 4. Influence of reduced inertia on the dual-loop-PI-controlled VSC. (a) A pole-zero map of $v_{dc}^*(s)/v_{dc}(s)$. (b) Step response of $v_{dc}(s)/i_o(s)$ normalized with rated voltage and current. IF = 100, 25, 7, and 6 roughly correspond to peak-to-peak dc-link ripple 0.4%, 1.5%, 5%, and 6%.

methods in [28] are applied for 45 degree phase margin, $f_{sw}/50$ outer-voltage-loop crossover frequency and $f_{sw}/20$ inner-current-loop crossover frequency.

In Fig. 4 (a), a pole-zero map of $v_{dc}^*(s)/v_{dc}(s)$ is illustrated. With conventional PI tuning and control, the stability boundary of the IF for this system is around 6. In fact, the right-half-plane pole at I_o/CV_{dc} in Fig. 3 can move to high frequency and lead to instability with reduced C or IF [28]. Step response of $v_{dc}(s)/i_o(s)$ is shown in Fig. 4 (b). Note that IF = 7 or 5% dc-link peak-to-peak ripple can induce 25% overshoot and the system becomes unstable when $IF \leq 6$.

Without the big dc link to buffer input output power mismatch, it is critical to realize that cycle by cycle or other fast control to balance the input and output power is required to reject the disturbance that can be propagated into the dc link. In a SLIC, high bandwidth on both the stacked-side balancing and the dc-link regulation is necessary.

To summarize, the stacked low-inertia converter control is a multi-objective and multi-degree of freedom problem. It is difficult to control the dc-link current, stacked-side voltage and load voltage simultaneously, especially under large-signal

disturbances or controller saturation, which is not emphasized in traditional high-inertia converter control and small-signal analysis. Also, a large-signal model including the dc-link dynamics and high-bandwidth control are needed. Priority shifting and large-signal-model-based fast control are the key.

III. THE CHALLENGES OF APPLYING PI CONTROLLER TO SLICS

The PI controllers with feedforward are based on small-signal averaged models. Therefore, the conventional averaged model is discussed [19]. The S4T works like a flyback converter but with a zero vector. From this section on, the dc-link inductor and the magnetizing inductance refer to the same component in this current-source topology. The dc link is energized from input for duration T_A or duty cycle D_A in (3), while the stored energy in the dc link is delivered to output for duration T_B or duty cycle D_B in (4). The zero vector has a duration T_Z or duty cycle D_Z in (5). In (3)-(5), i is the dc-link current, v is the load voltage, v_s is the source voltage, C is the filter capacitor on the load side, and L is the dc-link inductor.

$$\frac{d}{dt} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -1/RC \end{bmatrix} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} v_s(t) \quad (3)$$

$$\frac{d}{dt} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix} = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_s(t) \quad (4)$$

$$\frac{d}{dt} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -1/RC \end{bmatrix} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_s(t) \quad (5)$$

The state-space averaging can be used to derive the transfer functions in (6) between control inputs $d_a(s)$ and $d_b(s)$, and state variables $i(s)$ and $v(s)$. Accordingly, the small-signal model of single module is shown in Fig. 5 (a).

$$\begin{bmatrix} i(s) \\ v(s) \end{bmatrix} = \begin{bmatrix} \frac{V_s(Cs + \frac{1}{R})}{LCs^2 + \frac{L}{R}s + D_b^2} & \frac{-V_s C s - \frac{V}{R} - D_b I}{LCs^2 + \frac{L}{R}s + D_b^2} \\ \frac{D_b V_s}{LCs^2 + \frac{L}{R}s + D_b^2} & \frac{I L s - D_b V}{LCs^2 + \frac{L}{R}s + D_b^2} \end{bmatrix} \begin{bmatrix} d_a(s) \\ d_b(s) \end{bmatrix} + \begin{bmatrix} \frac{D_a(Cs + \frac{1}{R})}{LCs^2 + \frac{L}{R}s + D_b^2} \\ \frac{D_a D_b}{LCs^2 + \frac{L}{R}s + D_b^2} \end{bmatrix} v_s(s) \quad (6)$$

For the small-signal model of two modules in Fig. 5 (b), the transfer function between control inputs, i.e., $d_{1a}(s)$, $d_{2a}(s)$, $d_{1b}(s)$, and $d_{2b}(s)$, and control objectives, i.e., dc-link current $i_k(s)$, load voltage $v(s)$ and stacked capacitor voltage balance $v_1(s) - v_2(s)$ can be derived in (7)-(9), where $k = 1, 2$. Assume $L_1 = L_2 = L$, $C_{1A} = C_{2A} = C_A$ and the same operating point for two modules.

$$\frac{i_k(s)}{d_{ka}(s)} = \frac{V_k(C_B s + \frac{1}{R})}{L_k C_B s^2 + \frac{L_k}{R} s + D_{kb}^2} \quad (7)$$

$$\frac{v(s)}{d_{kb}(s)} = \frac{I_k L_k s - D_{kb} V}{L_k C_B s^2 + \frac{L_k}{R} s + D_{kb}^2} \quad (8)$$

$$\frac{v_1(s) - v_2(s)}{d_{1b}(s) - d_{2b}(s)} = \frac{D_a V C_A s + D_a \frac{V}{R} + D_a D_b I}{L C_A s^2 + \frac{L}{R} s + D_b^2} \quad (9)$$

Three major groups of control methods for input-series output parallel (ISOP) dc-dc converters include common-duty-cycle control [29]-[30], master-slave control [31]-[32], and voltage sharing control [33]-[34]. The common-duty-cycle control cannot achieve excellent voltage balancing under parameter mismatches, especially as passives have 5-20%

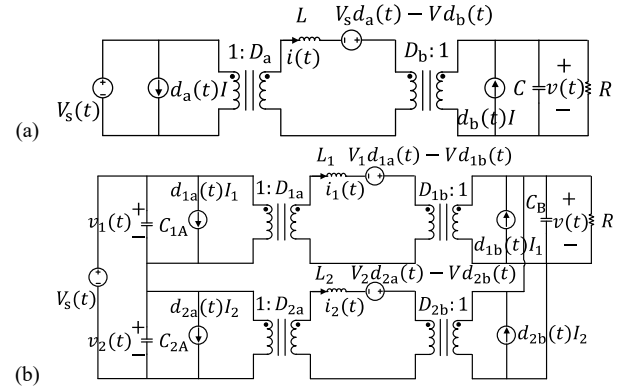


Fig. 5. Averaged models of (a) single module and (b) two-module M-S4T.

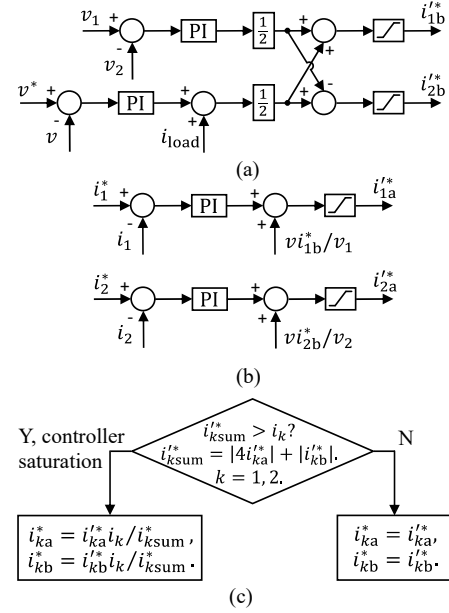


Fig. 6. PI controller applied to the M-S4T in Fig. 5 (b). (a) Stacked-side voltage balancing and load voltage regulation. i_{1b}^* stands for the reference current of modules 1's B-bridge injected into the load. (b) DC-link current control with feedforward. i_{1a}^* stands for the reference current of modules 1's A-bridge drawn from the source. (c) A saturation block to limit the total reference currents (referred to the LV-side with a 4:1 transformer turns ratio) within the converter's physical rating.

tolerance. The master-slave control employs one module for load voltage regulation and the others for stacked-side balancing, resulting in uneven thermal stress. All ISOP modules under the control in [33]-[34] play an equal role with evenly distributed control tasks and achieve more balanced thermal stress. Hence, control adapted from [33]-[34] is applied as shown in Fig. 6. The stacked-side balancing loop and the parallel-side load regulation loop in Fig. 6 (a) indicate that the difference between the two modules' currents drawn from the source maintains stacked voltage balancing, while the sum of the currents regulates the load. Fig. 6 (b) represents the dc-link regulation loop with load-power feedforward. The current references cannot be translated accurately into duty cycles with SVPWM due to the large dc-link ripple in the SLIC, and the charge modulation is used [35]-[36]. Note that at any time, the

dc-link current can flow through either A-bridge or B-bridge but not both simultaneously, similar to a flyback converter. Hence, i_{1a}^* , i_{1b}^* , i_{2a}^* , and i_{2b}^* are limited within the nominal dc-link current rating and a saturation block in Fig. 6 (c) is implemented to limit the total reference currents up to the dc-link current. When the sum of i_{1a}^* and i_{1b}^* is larger than the dc-link current, the controller saturates and i_{1a}^* and i_{1b}^* are scaled downwards proportionally. In other words, under controller saturation, i_{1a}^* needs to compete with i_{1b}^* within a converter module for limited resource, i.e., the dc-link current.

In (6)-(9) and Fig. 5, both $i(s)$ and $v(s)$ are coupled to $d_a(s)$ and $d_b(s)$, which is a challenge for the SLIC control. Also, the coupling terms vary with operating points. In other words, without a big energy buffer, the input-bridge duty cycle or a disturbance can influence the output easily as explained in Section II. For a high-inertia converter, i.e., large L in (6), $v(s)/d_a(s)$ can be negligible compared to $v(s)/d_b(s)$. Nevertheless, even with large L , $i(s)/d_a(s)$ is of similar magnitude as $i(s)/d_b(s)$. Conventionally, the coupling is mitigated by tuning the load regulation loop in Fig. 6 (a) to be much faster than the dc-link regulation loop in Fig. 6 (b), relying on the large dc link to absorb the power mismatch between the input and output to enable the control loop decoupling [28]. This approach cannot be used for a SLIC due to the reduced dc link.

A 5 kV dc to 600 V dc M-S4T at 20 kHz switching frequency is simulated in Fig. 7 with parameters in Table I. At 25 ms, the stacked-side voltages are forced to be unequal, i.e., 3.5 kV and 1.5 kV. Due to the coupling inside the SLIC, interactions between the stacked-side balancing and the dc-link current regulation can be clearly observed. The stacked-side balancing controller in Fig. 6 (a) commands module 1 with overvoltage in Fig. 7 to output more current to the load than module 2. The sudden increase in module 1's output current reference results in more energy delivered to the output than drawn from the input during the dc-link control loop reaction time, leading to the module 1's dc-link current drop. When the dc-link current of the current-source converter is below the nominal value, module 1 cannot output nominal power and eventually the controller saturates. Then, the dc-link current is stuck at an abnormal equilibrium point because under the controller saturation, the PI loses the regulation capability [37]-[38] to restore the dc link. Even with anti-windup methods [39], e.g., stopping integration under saturation which is applied in the simulation, the PI can still lose the controllability under saturation [38]. The PI saturation issue is regarded important in controller design for electric drives, microgrids, dc-dc converters, etc., [37]-[41]. In this case, the PI controller does not know that under saturation, the dc link should be prioritized and restored so that the converter can process desired amount of power for voltage balancing and load regulation. In fact, the physical meaning of the right-half-plane (RHP) zero in (8) indicates that if the output is commanded to rise, the output will have to decrease first, before the dc-link current increases to an appropriate level, and then increase.

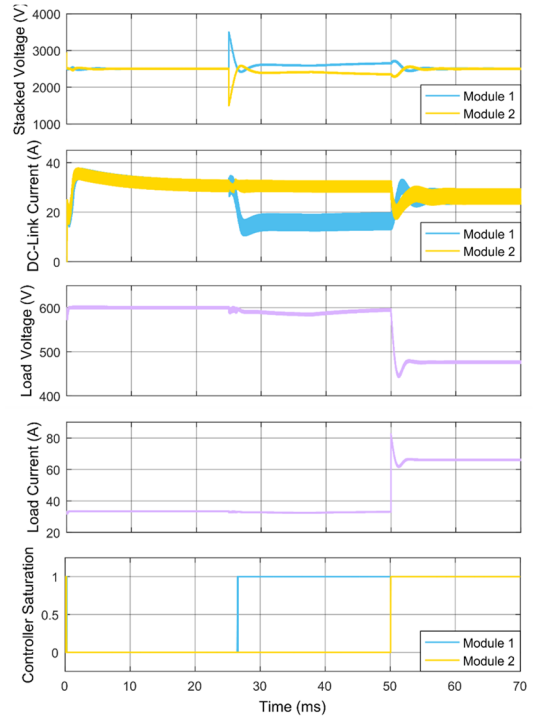


Fig. 7. Simulation waveforms of the PI controlled M-S4T. The dc-link current, i.e., magnetizing current is referred to the MV side of the 4:1 transformer. Controller saturation in Fig. 6 (c) (“1” in the controller saturation trace above) occurs.

Table I. Simulation parameters of the M-S4T under PI control.

Parameters	Module 1	Module 2
Magnetizing inductance (L_m)	7.35 mH	7 mH
Filter capacitor (C_A)	5.25 μ F	4.75 μ F
Filter capacitor (C_B)	64 μ F	64 μ F
DC-link current loop (k_p, k_i)	0.1, 10	0.1, 10
Stacked-side voltage loop (k_p, k_i)		0.01, 10
Load voltage loop (k_p, k_i)		1, 100

At 50 ms, a 40% to 100% load step change is applied. The sudden load-current change propagates through load-current feedforward term and eventually saturates the controller of module 2. Similar to module 1, the dc-link current of module 2 cannot be brought back to normal, and the converter is trapped in an abnormal operating point under controller saturation [37]-[38]. Since the dc-link current is at \sim 80% of the nominal, the output voltage is stuck at \sim 80% of the 600 V reference.

To summarize, the conventional PI controller cannot control the SLIC robustly under large-signal disturbance and controller saturation. Prioritizing control objectives is critical to distribute control efforts appropriately under these conditions. For a traditional converter with a large dc link, issues related to saturation and control efforts distribution are not severe because the dc link can easily serve as an energy buffer with small fluctuation at a larger time scale. Moreover, high-bandwidth control is important for the SLIC, which requires an accurate model to capture the low-inertia dc-link dynamics. Then, the impact of the cross-coupling terms can be mitigated and the dc link can be controlled better under transients.

The next question would be whether improving the traditional PI can solve the SLIC control problem. There exists such a possibility with the converter model incorporated. The model is needed for precise feedforward [27], [42] and delay compensation [43]-[44] to increase the bandwidth and prevent dc-link overshoot. Linear extrapolation cannot compensate the delay accurately due to the fast SLIC dynamics [43]. Moreover, the converter model is needed to adaptively distribute control efforts and assign saturation thresholds to address the saturation issue. When the converter model is anyway needed, predictive control can achieve even better performance compared to small-signal-based PI due to large-signal-based design for all operating points, cycle-by-cycle peak current limiting/control, avoiding cascaded loop structure [45], and fast deadbeat response on the low-inertia dc link [46].

IV. THE CHALLENGES OF APPLYING OTHER EXISTING CONTROLS TO SLICS

Existing control schemes are examined for the SLIC control problem. Hysteresis control is known for its simplicity, robustness, and high bandwidth [47]-[48]. Variable switching frequency can be a shortcoming. Normally, the hysteresis control is employed for VSC's current control with a PI control loop for dc-link regulation. Its high bandwidth is based on the assumption of a large dc-link buffer to absorb any input and output power mismatch so that the inverter can source whatever the requested output current is. However, for the SLIC, transients on the low-inertia dc link should be considered and intelligence is required to trade off control efforts among all the control objectives under large-signal disturbances and controller saturations.

Deadbeat control has a high bandwidth by effectively utilizing the converter model [49]-[53]. It is designed for current control in PWM rectifiers and active filters [49]-[50] and filter-inductor current and output voltage control in uninterruptible power supply (UPS) [51]-[53]. For the deadbeat control [49]-[53], stable dc links are assumed with batteries in UPS or large dc-link capacitors controlled by another slow loop in PWM rectifiers. Nevertheless, owing to the low inertia and the tight couplings in the SLIC, the dc link needs to be regulated with fast control and holistically considered in conjunction with the output control and the stacked-side balancing, which has not been addressed in the literature. Moreover, the prioritized control effort distribution under controller saturation and large-signal disturbance are not considered in the deadbeat control.

Model predictive control (MPC) uses optimization to realize multiple control objectives simultaneously with a high bandwidth [54]-[55], which is needed for the SLIC. However, performance of the MPC under a large-signal disturbance is not guaranteed and weight selection for various objectives for proper trade-off is challenging [54]-[55].

To summarize, the existing controls cannot completely fulfill the requirements for the SLIC control. The major limitation is the capability of multivariable control under controller saturation and large-signal disturbance.

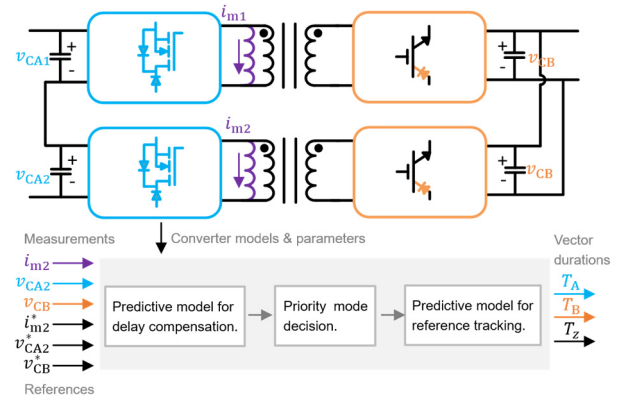


Fig. 8. A block diagram of the proposed MPPS control. Only the control of module 2 is shown. The vector dwelling times are fed to a state machine in the FPGA for real-time execution.

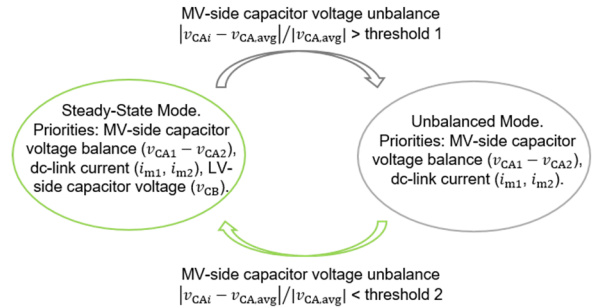


Fig. 9. The priority shifting feature of the proposed MPPS method. $i = 1, 2$. In each converter module's controller, if the MV-side filter capacitor voltage deviates from the average MV-side filter capacitor voltage, i.e., the grid voltage divided by the number of modules, more than threshold 1, the controller will enter the unbalanced mode.

V. PROPOSED MODEL PREDICTIVE PRIORITY-SHIFTING (MPPS) CONTROL FOR STACKED LOW-INERTIA CONVERTERS (SLICS)

To address the SLIC control problem, a novel control method, model predictive priority-shifting control (MPPS) is proposed. The proposed MPPS in Fig. 8 is explained with respect to the M-S4T converter in Fig. 1 (d) for MV to LV power flow. The analysis can also be extended to the other power flow direction. The MPPS has two important features: priority shifting and model prediction.

A. Priority Shifting Feature

As illustrated in Fig. 9, the proposed MPPS method consists of two priority modes: the steady-state mode and the unbalanced mode. The controller normally operates in the steady-state mode, but transitions to the unbalanced mode when the stacked-side voltage unbalance is out of band. The controller transitions back to the steady-state mode, once the stacked-side voltage balancing is restored to a preset threshold. In this paper, unless specified, the controller of each module receives its own MV output voltage and the average voltage of all the modules and decides its own mode according to Fig. 9.

In the unbalanced mode, the control priorities include stacked-side voltage balancing and dc-link regulation, while the LV load voltage is not regulated. In the steady-state mode, all the control objectives are realized, and all the state variables are controlled to settle at their corresponding references. As has

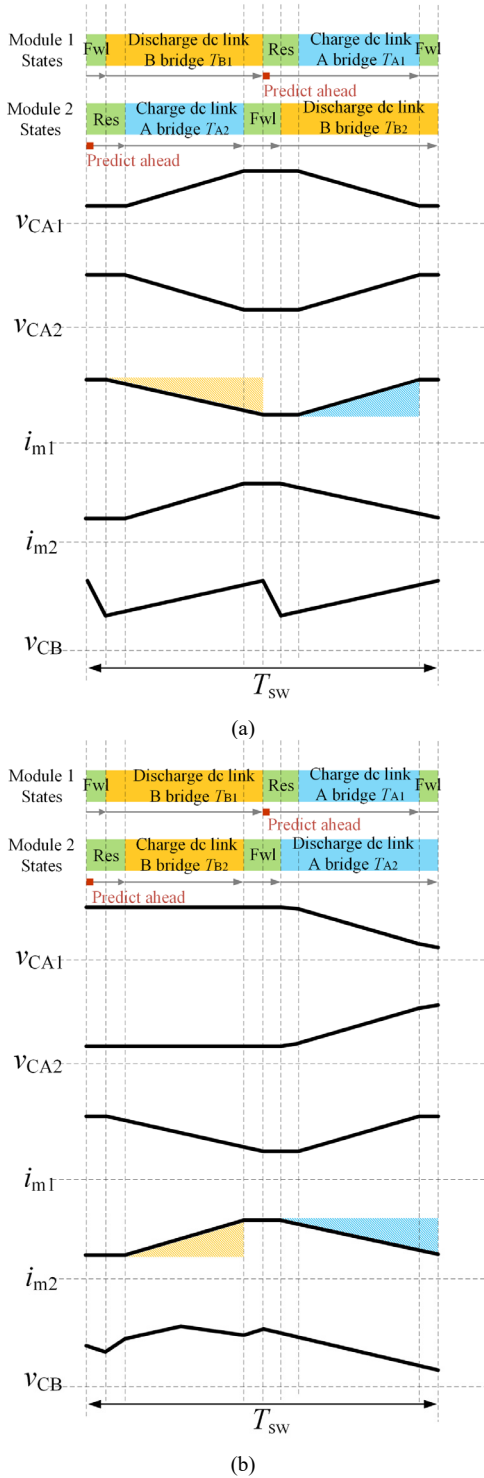


Fig. 10. The interleaved operation of two modules when the steady-state power flow direction is MV to LV with the model prediction feature in (a) steady-state mode, (b) unbalanced mode. In the steady-state mode, module 1 and module 2 have power flow direction from MV to LV. In the unbalanced mode, to restore the stacked-side balance, module 1 with overvoltage has power flow direction from MV to LV to decrease its stacked-side voltage, while module 2 has power flow direction LV to MV to increase its stacked-side voltage. The A-bridge corresponds to the blue MV bridge in Fig. 8 and the B-bridge corresponds to the orange LV bridge. Due to the reduced dc link, the shadowed areas are the charge deviations from the traditional thinking of neglecting the dc-link ripple.

been discussed in Section II, the reason for priority shifting is briefly mentioned here. MV stacked-capacitor voltage balancing is critical for safe and reliable operation and should be restored as fast as possible. However, as shown in Fig. 2 and (2), load-voltage regulation occupies power conversion resources, which limits the resource that can be distributed to the stacked-side balancing and results in controller saturation. In fact, four control inputs D_{A1} , D_{A2} , D_{B1} , D_{B2} are not independent under controller saturation constraints, e.g., $D_{A1} + D_{B1} < 1$ and cannot fully control four variables $v_{CA1} - v_{CA2}$, i_{m1} , i_{m2} , v_{CB} . Therefore, the load voltage (v_{CB}) control should be sacrificed in the unbalanced mode for safety.

B. Model Prediction Feature

To respond promptly under large-signal disturbances, the controller should predict ahead and calculate the duty ratio for the next switching cycle as shown in Fig. 10 for the interleaved M-S4T. Ideally for each module, at the start of the switching cycle, the duty cycles for A bridge ($D_A = T_A / T_{sw}$), B bridge ($D_B = T_B / T_{sw}$) and freewheeling state ($D_z = T_z / T_{sw}$) are calculated. The predictive control law is derived to achieve deadbeat response on the reduced dc link, based on a discrete-time large-signal model which can accurately capture the low-inertia dc-link dynamics.

C. Discrete-Time Large-Signal Model in Steady-State Mode

In the steady-state mode in Fig. 10 (a), the stacked voltage is balanced and within the threshold in Fig. 9. The priority is given to the dc-link current and the load voltage regulation, while the stacked voltage balance is indirectly maintained. For instance, the module with the stacked-side voltage higher than the average or the reference is controlled to supply more load power and draw more source current to reduce its stacked-side voltage. In this section, the module is considered with a 1:1 transformer or equivalently per-unit voltage and current for simplicity. The discrete-time large-signal model will be derived where the load is a resistor. However, the derivation procedure is also applicable when the load is a current source.

The equivalent circuits for the stacked-side capacitor voltage during the A-bridge active period T_{A1} and A-bridge inactive period $T_{sw} - T_{A1}$ are shown in Fig. 11. The system equations during $T_{sw} - T_{A1}$ and T_{A1} are given in (10) and (11), respectively.

$$v_{CA1}(t + T_{sw} - T_{A1}) = v_{CA1}(t) \quad (10)$$

$$\frac{d}{dt} \begin{bmatrix} v_{CA1}(t) \\ i_{m1}(t) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C_{A1} + C_{A2}} \\ \frac{1}{L_{m1}} & 0 \end{bmatrix} \begin{bmatrix} v_{CA1}(t) \\ i_{m1}(t) \end{bmatrix} \quad (11)$$

The voltage and current after T_{A1} can be derived in (12). If T_{A1} is small compared to the natural frequency in (13), all trigonometric functions in (12) can be approximated as linear terms. Generally, the approximation holds for conventional converters owing to large dc links. However, it is not the case for the SLIC. The sized filter and the dc link (e.g., Table III for experiments) should be plugged into the equations to see the contribution of high-order terms in the Taylor series to the

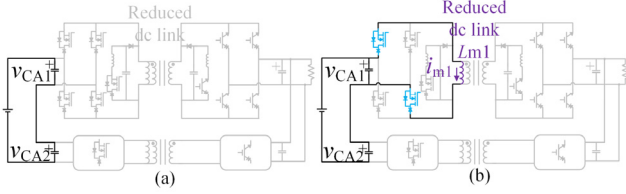


Fig. 11. The equivalent circuit concerning the stacked-side capacitor voltage for the MV to LV power flow direction: (a) during $T_{sw} - T_{A1}$, (b) during T_{A1} . Only the components that are active and affecting the stacked-side capacitor voltage are highlighted.

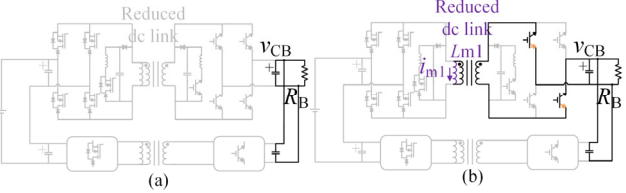


Fig. 12. The equivalent circuit concerning the LV-side load voltage for the MV to LV power flow direction: (a) during $T_{sw} - T_{B1}$, (b) during T_{B1} .

variation of the state variables compared to other terms. For example, the contribution of the third-order term in (14) to $v_{CA1}(t + T_{A1}) - v_{CA1}(t)$ is very small compared to other terms in (12) and can be neglected. The final result is given in (12). The physical meaning of the second-order term in (12) is additional charge absorbed from the stacked-side filter capacitors because of the dc-link current ripple during T_{A1} , which is illustrated as the blue shadowed area in Fig. 10 (a).

$$\begin{bmatrix} v_{CA1}(t + T_{A1}) \\ i_{m1}(t + T_{A1}) \end{bmatrix} = \begin{bmatrix} \cos(\omega_0 T_{A1}) & -\frac{\sin(\omega_0 T_{A1})}{\omega_0(C_{A1} + C_{A2})} \\ \frac{\sin(\omega_0 T_{A1})}{\omega_0 L_{m1}} & \cos(\omega_0 T_{A1}) \end{bmatrix} \begin{bmatrix} v_{CA1}(t) \\ i_{m1}(t) \end{bmatrix} \quad (12)$$

$$\approx \begin{bmatrix} 1 - \frac{T_{A1}^2}{2L_{m1}(C_{A1} + C_{A2})} & -\frac{T_{A1}}{C_{A1} + C_{A2}} \\ \frac{T_{A1}}{L_{m1}} & 1 \end{bmatrix} \begin{bmatrix} v_{CA1}(t) \\ i_{m1}(t) \end{bmatrix} \quad (13)$$

$$\omega_0 = \frac{1}{\sqrt{L_{m1}(C_{A1} + C_{A2})}} \quad (13)$$

$$\frac{T_{A1}^2}{2L_{m1}(C_{A1} + C_{A2})} v_{CA1}(t) \gg \frac{T_{A1}^3}{6L_{m1}(C_{A1} + C_{A2})^2} i_{m1}(t) \quad (14)$$

The equivalent circuits for the LV load voltage during the B-bridge active period T_{B1} and B-bridge inactive period $T_{sw} - T_{B1}$ are shown in Fig. 12. During $T_{sw} - T_{B1}$, (15) can be derived.

$$v_{CB}(t + T_{sw} - T_{B1}) = v_{CB}(t) e^{-\frac{T_{sw} - T_{B1}}{R_B C_B}} \approx v_{CB}(t) \left(1 - \frac{T_{sw} - T_{B1}}{R_B C_B} \right) \quad (15)$$

During T_{B1} , the state equation is given by (16).

$$\frac{d}{dt} \begin{bmatrix} v_{CB}(t) \\ i_{m1}(t) \end{bmatrix} = \mathbf{A} \begin{bmatrix} v_{CB}(t) \\ i_{m1}(t) \end{bmatrix} \quad (16)$$

$$\mathbf{A} \triangleq \begin{bmatrix} -\frac{1}{R_B C_B} & \frac{1}{C_B} \\ -\frac{1}{L_{m1}} & 0 \end{bmatrix} \quad (17)$$

The states after T_{B1} can be derived in (18)-(20). Importantly, the contribution of high-order terms in (19), i.e., the second-order term $T_{B1}^2/2L_{m1}C_B$ in (20) cannot be ignored. This term

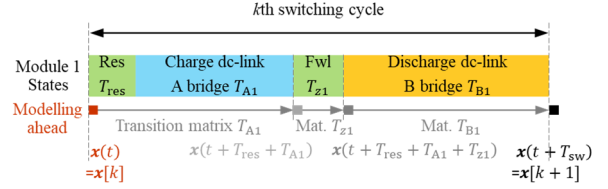


Fig. 13. Derivation of the discrete-time large-signal model of the M-S4T.

can be of the same order of magnitude as the linear term $T_{B1}/R_B C_B$. The contribution of high-order terms is one crucial difference in modelling between the SLIC and the conventional converter where the large dc link allows for neglecting such terms. The root cause of the second-order term is the large switching ripple on the dc-link inductor in Fig. 10. Therefore, we cannot apply the conventional thinking of SVPWM and use the dc-link current at the start of T_{B1} multiplied by dwelling time to compute the charge delivered. The physical meaning of this term is that less charge is delivered to the load compared to the negligible ripple case, i.e., the orange shadowed area in Fig. 10 (a) due to the dc-link current fluctuation during T_{B1} .

$$\begin{bmatrix} v_{CB}(t + T_{B1}) \\ i_{m1}(t + T_{B1}) \end{bmatrix} = e^{\mathbf{A}T_{B1}} \begin{bmatrix} v_{CB}(t) \\ i_{m1}(t) \end{bmatrix} \quad (18)$$

$$e^{\mathbf{A}T_{B1}} = \mathbf{I} + \mathbf{A}T_{B1} + \frac{(\mathbf{A}T_{B1})^2}{2!} + \frac{(\mathbf{A}T_{B1})^3}{3!} + \dots \quad (19)$$

$$\begin{bmatrix} v_{CB}(t + T_{B1}) \\ i_{m1}(t + T_{B1}) \end{bmatrix} \approx \begin{bmatrix} 1 - \frac{T_{B1}}{R_B C_B} - \frac{T_{B1}^2}{2L_{m1}C_B} & \frac{T_{B1}}{C_B} \\ -\frac{T_{B1}}{L_{m1}} & 1 \end{bmatrix} \begin{bmatrix} v_{CB}(t) \\ i_{m1}(t) \end{bmatrix} \quad (20)$$

In the steady-state mode, the converter traverses from the resonant state through the charge dc-link state of A-bridge and the freewheeling state to the discharge dc-link state of B-bridge sequentially in a switching cycle in Fig. 13. Accordingly, the state trajectories of module 1 are derived by combing the state variable variation during each state, e.g., (20) for load and dc-link variations during T_{B1} and are finally given in (21)-(23).

$$i_{m1}(t + T_{sw}) = \frac{T_{A1}}{L_{m1}} v_{CA1}(t) - \frac{T_{B1}}{L_{m1}} v_{CB}(t + T_{sw} - T_{B1}) + i_{m1}(t) \quad (21)$$

$$v_{CA1}(t + T_{sw}) = \left(1 - \frac{T_{A1}^2}{2L_{m1}(C_{A1} + C_{A2})} \right) v_{CA1}(t) - \frac{T_{A1} i_{m1}(t)}{C_{A1} + C_{A2}} \quad (22)$$

$$v_{CB}(t + T_{sw}) = \left(1 - \frac{T_{sw}}{R_B C_B} - \frac{T_{B1}^2}{2L_{m1}C_B} \right) v_{CB}(t) + \frac{T_{B1} i_{m1}(t + T_{sw} - T_{B1})}{C_B} \quad (23)$$

In the freewheeling state, only device conduction drops are applied across the dc-link inductor and the corresponding dc-link current variation is neglected in (21). For (22)-(23), only the contribution of the module 1 on v_{CA1} and v_{CB} is considered. The same model can be applied to module 2 in the steady-state mode to include its contribution to v_{CB} and v_{CA1} . Then, (24)-(25) can be derived. The interleaved module 2 has its switching cycle and sample instant displaced by $T_{sw}/2$ relative to the module 1.

$$v_{CA1}(t + T_{sw}) \approx \left(1 - \frac{T_{A1}^2}{2L_{m1}(C_{A1} + C_{A2})} \right) v_{CA1}(t) + \frac{T_{A2}^2}{2L_{m2}(C_{A1} + C_{A2})} v_{CA2}(t) - \frac{T_{A1}}{C_{A1} + C_{A2}} i_{m1}(t) + \frac{T_{A2}}{C_{A1} + C_{A2}} i_{m2}\left(t + \frac{T_{sw}}{2}\right) \quad (24)$$

$$v_{CB}(t + T_{sw}) \approx \left(1 - \frac{T_{sw}}{R_B C_B} - \frac{T_{B1}^2}{2L_{m1}C_B} - \frac{T_{B2}^2}{2L_{m2}C_B}\right)v_{CB}(t) + \frac{T_{B1}}{C_B}i_{m1}(t + T_{sw} - T_{B1}) + \frac{T_{B2}}{C_B}i_{m2}\left(t + \frac{T_{sw}}{2} - T_{B2}\right) \quad (25)$$

The discrete-time large-signal model of two modules is organized in compact matrix format in the appendix.

To summarize, a discrete-time large-signal model of the M-S4T is established. Note that critical second-order terms affecting dynamics of the SLIC are captured. These terms are negligible in conventional high-inertia converters and not modelled in the traditional average model with small ripple assumption.

D. Predictive Control in Steady-State Mode

The priorities in the steady-state mode are the dc-link current and the load voltage while maintaining the stacked-side balance. With the plant model and references $i_{m1}^*(t + T_{A1})$, $v_{CB}^*(t + T_{sw})$, we can use T_{A1} to control the dc-link current i_{m1} and T_{B1} to regulate the load-side voltage v_{CB} . Here, $i_{m1}^*(t + T_{A1})$ is the peak current reference of i_{m1} for convenience, as the dc-link current reaches its peak after the charge dc-link state in Fig. 10 (a). The peak current reference can be directly commanded or converted from the average current reference $i_{m1_avg}^*(t)$ and the estimated dc-link ripple as shown in (26).

$$i_{m1}^*(t + T_{A1}) = i_{m1_avg}^*(t) + \frac{v_{CB}(t) i_{load}(t)/N}{2L_{m1} i_{m1_avg}^*(t)} m T_{sw} \quad (26)$$

where $i_{load}(t)$ is the load current, N is the number of modules, i.e., two in this paper, m is a form factor > 1 , e.g., 1.2 to add margin for robustness in case of a ripple estimation error because the converter cannot process full power if the dc-link current reference is lower than expected.

With the model in (12), the vector timing T_{A1} to let the dc-link current track the reference in (26) can be calculated in (27). If T_{A1} in (27) is calculated to be larger than a switching cycle minus lost time due to the ZVS transition and the resonant states, i.e., $T_{sw} - T_{ZVS} - T_{res}$, a saturation upper limit should be enforced. The calculation of the lost time is given in (28)-(29), where L_r resonant inductor in Fig. 1 (b), C_r resonant capacitor, I_{m1_avg} average dc-link current, and V_{pk} peak input/output voltage should be referred to the same side of the transformer. The prediction of the dc-link current after T_{A1} is given by (30).

$$T_{A1} = \frac{i_{m1}^*(t + T_{A1}) - i_{m1}(t)}{v_{CA1}(t)/L_{m1}} \quad (27)$$

$$T_{res} = \sqrt{L_r C_r} (2\pi - \text{asin}\left(\frac{\sqrt{I_{m1_avg}^2 V_{pk}^2 C_r / L_r}}{I_{m1_avg}^2 / 4 + V_{pk}^2 C_r / L_r}\right)) \quad (28)$$

$$T_{ZVS} = \frac{2V_{pk}}{I_{m1_avg}/2C_r} \quad (29)$$

$$i_{m1}(t + T_{A1}) = \frac{T_{A1}}{L_{m1}} v_{CA1}(t) + i_{m1}(t) \quad (30)$$

With the model in (25) and the predicted dc-link current in (30), the vector timing T_{B1} for load voltage regulation is derived in (31)-(32). In (31), the physical meaning of the first term is the required charge to track the load voltage reference, while the second term is for load-current feedforward. The load

resistor R_B value is not necessary and a current sensor to measure the load current is enough in (31). Note that because of the reduced dc link, second-order terms exist in (25). To avoid solving a quadratic equation real time in a DSP, which can be computationally intensive, T_{B1}^2 in (32) can be substituted by last switching cycle's $T_{B1_last}^2$. In (31), the first term in $\left(\frac{1}{N} + k_p(v_{CA1}(t) - v_{CA1}^*(t))\right)$ means that N modules are in parallel on the LV side to share the load current. The second term is a feedback term to balance the stacked-side voltages where higher v_{CA1} leads to supplying higher i_{load} to decrease v_{CA1} . k_p is used to translate the per-unit voltage unbalance into vector timing difference, which is essentially a current-reference feedback correction term. For example, to translate ~10% per-unit voltage unbalance with nominal voltage 2500 V to ~50% current sharing difference, k_p is calculated to be 0.002.

$$T_{B1}' = \left(\frac{(v_{CB}^*(t + T_{sw}) - v_{CB}(t))C_B}{i_{m1}(t + T_{A1})} + \frac{i_{load}(t)T_{sw}}{i_{m1}(t + T_{A1})}\right)\left(\frac{1}{N} + k_p(v_{CA1}(t) - v_{CA1}^*(t))\right) \quad (31)$$

$$T_{B1} = T_{B1}' + \frac{v_{CB}(t)T_{B1_last}^2}{2L_{m1}i_{m1}(t + T_{A1})} \quad (32)$$

The prediction of the dc-link current after T_{B1} , i.e., at the end of a switching cycle, is given in (33).

$$i_{m1}(t + T_{sw}) = -\frac{T_{B1}}{L_{m1}}v_{CB}(t) + i_{m1}(t + T_{A1}) \quad (33)$$

It is critical to ensure that the dc-link current is around its reference to have desirable power processing capability, avoid dc-link inductor saturation and limit the thermal stress. Hence, if $i_{m1}(t + T_{sw})$ is outside the limits, e.g., [0.6, 1.5] pu of its reference, the saturation limit should be enforced and the updated T_{B1} is given by (34).

$$T_{B1} = \frac{i_{m1}(t + T_{A1}) - i_{m1_lower_limit}(t)}{v_{CB}(t)/L_{m1}} \quad (34)$$

Moreover, if T_{B1} is calculated to be larger than the remaining switching cycle, i.e., $T_{sw} - T_{ZVS} - T_{res} - T_{A1}$, a saturation upper limit should be enforced. Finally, for constant T_{sw} , the zero-vector timing is calculated in (35).

$$T_{z1} = T_{sw} - T_{ZVS} - T_{res} - T_{A1} - T_{B1} \quad (35)$$

To summarize, the control in the steady-state mode is illustrated in the flow chart in Fig. 16. Based on the discrete-time large-signal model of the SLIC, load-voltage control and robust dc-link current control can be achieved by the MPPS to ensure no large over/undercurrent while maintaining the stacked voltage balance.

E. Discrete-Time Large-Signal Model in Unbalanced Mode

In the unbalanced mode in Fig. 10 (b), module 1 with overvoltage has a MV-LV power flow direction while module 2 with undervoltage has a LV-MV power flow direction for voltage balancing. The current is drawn from module 1's MV filter capacitor to decrease its voltage. Moreover, the module 2 injects current into its MV filter capacitor to increase its

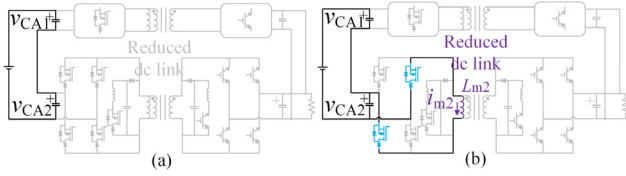


Fig. 14. Equivalent circuits concerning the stacked-side capacitor voltage of module 2 under LV to MV power flow direction in the unbalanced mode: (a) during $T_{sw}-T_{A2}$, (b) during T_{A2} .

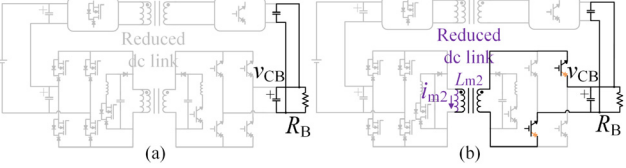


Fig. 15. Equivalent circuits concerning the LV load voltage of module 2 under LV to MV power flow direction in the unbalanced mode: (a) during $T_{sw}-T_{B2}$, (b) during T_{B2} . C_B here is the total LV-side capacitors of the two modules.

voltage. As the MV-LV power flow direction modelling has been covered in the steady-state mode, only the modelling for the LV-MV power flow direction is presented in detail for module 2 in this case.

For the LV-MV power flow of module 2, the equivalent circuits concerning the stacked capacitor voltage during T_{A2} and $T_{sw} - T_{A2}$ are shown in Fig. 14. During $T_{sw} - T_{A2}$, no current flows into the capacitor C_{A2} and (36) holds.

$$v_{CA2}(t + T_{sw} - T_{A2}) = v_{CA2}(t) \quad (36)$$

During T_{A2} , the state equation is given by (37).

$$\frac{d}{dt} \begin{bmatrix} v_{CA2}(t) \\ i_{m2}(t) \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C_{A1}+C_{A2}} \\ -\frac{1}{L_{m2}} & 0 \end{bmatrix} \begin{bmatrix} v_{CA2}(t) \\ i_{m2}(t) \end{bmatrix} \quad (37)$$

The voltage and current after T_{A2} can be obtained in (38) by evaluating the high-order terms in the Taylor series. The physical meaning of the second-order term in (38) is less charge in the blue shadowed area in Fig. 10 (b) injected into the stacked-side filter capacitors due to the dc-link current fluctuation during T_{A2} .

$$\begin{bmatrix} v_{CA2}(t + T_{A2}) \\ i_{m2}(t + T_{A2}) \end{bmatrix} \approx \begin{bmatrix} 1 - \frac{T_{A2}^2}{2L_{m2}(C_{A1}+C_{A2})} & \frac{T_{A2}}{C_{A1}+C_{A2}} \\ -\frac{T_{A2}}{L_{m2}} & 1 \end{bmatrix} \begin{bmatrix} v_{CA2}(t) \\ i_{m2}(t) \end{bmatrix} \quad (38)$$

The equivalent circuit concerning the LV load voltage during T_{B2} and $T_{sw} - T_{B2}$ are shown in Fig. 15. During $T_{sw} - T_{B2}$, (39) can be derived.

$$v_{CB}(t + T_{sw} - T_{B2}) \approx v_{CB}(t) \left(1 - \frac{T_{sw}-T_{B2}}{R_B C_B}\right) \quad (39)$$

During T_{B2} , the state differential equation is given by (40).

$$\frac{d}{dt} \begin{bmatrix} v_{CB}(t) \\ i_{m2}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_B C_B} & -\frac{1}{C_B} \\ \frac{1}{L_{m2}} & 0 \end{bmatrix} \begin{bmatrix} v_{CB}(t) \\ i_{m2}(t) \end{bmatrix} \quad (40)$$

The states after T_{B2} are derived in (41). The second-order term in (41) represents the additional charge sourced by the load capacitor during T_{B2} in the orange shadowed area in Fig. 10 (b).

$$\begin{bmatrix} v_{CB}(t + T_{B2}) \\ i_{m1}(t + T_{B2}) \end{bmatrix} \approx \begin{bmatrix} 1 - \frac{T_{B2}}{R_B C_B} - \frac{T_{B2}^2}{2L_{m2}C_B} & -\frac{T_{B2}}{C_B} \\ \frac{T_{B2}}{L_{m2}} & 1 \end{bmatrix} \begin{bmatrix} v_{CB}(t) \\ i_{m2}(t) \end{bmatrix} \quad (41)$$

Now, the state trajectories can be predicted with a similar procedure in Fig. 13. In the unbalanced mode of module 2 in Fig. 10 (b), the converter goes from the resonance state through the charge dc-link state of B-bridge and the freewheeling state to the discharge dc-link state of A-bridge in a switching cycle. Accordingly, the variation of the state variables across a full cycle are shown in (42)-(44), where t corresponds to the start of a module 2's switching cycle, i.e., the resonant state.

$$i_{m2}(t + T_{sw}) = \frac{T_{B2}}{L_{m2}} v_{CB}(t) - \frac{T_{A2}}{L_{m2}} v_{CA2}(t + T_{sw} - T_{A1}) + i_{m2}(t) \quad (42)$$

$$v_{CA2}(t + T_{sw}) = \left(1 - \frac{T_{A2}^2}{2L_{m2}(C_{A1}+C_{A2})}\right) v_{CA2}(t) + \frac{T_{A2}}{C_{A1}+C_{A2}} i_{m2}(t + T_{sw} - T_{A2}) \quad (43)$$

$$v_{CB}(t + T_{sw}) = \left(1 - \frac{T_{B2}}{R_B C_B} - \frac{T_{B2}^2}{2L_{m2}C_B}\right) v_{CB}(t) - \frac{T_{B2}}{C_B} i_{m2}(t) \quad (44)$$

For (42)-(44), only the contribution of module 2 is considered. With the contribution from interleaved operation of module 1 under the unbalanced mode, (45)-(46) are derived.

$$v_{CA2}(t + T_{sw}) \approx \frac{T_{A1}}{C_{A1}+C_{A2}} i_{m1}\left(t + \frac{T_{sw}}{2}\right) + \frac{T_{A2}}{C_{A1}+C_{A2}} i_{m2}(t + T_{sw} - T_{A2}) + \left(1 - \frac{T_{A2}^2}{2L_{m2}(C_{A1}+C_{A2})}\right) v_{CA2}(t) + \frac{T_{A1}^2}{2L_{m1}(C_{A1}+C_{A2})} v_{CA1}(t) \quad (45)$$

$$v_{CB}(t + T_{sw}) \approx \left(1 - \frac{T_{B1}}{R_B C_B} - \frac{T_{B1}^2}{2L_{m1}C_B} - \frac{T_{B2}}{R_B C_B} - \frac{T_{B2}^2}{2L_{m2}C_B}\right) v_{CB}(t) + \frac{T_{B1}}{C_B} i_{m1}\left(t + \frac{T_{sw}}{2} - T_{B1}\right) - \frac{T_{B2}}{C_B} i_{m2}(t) \quad (46)$$

F. Predictive Control in Unbalanced Mode

For module 2, the priorities in the unbalanced mode are the dc-link current and the stacked voltage balancing. With the predictive model in (42), (45)-(46), and references $i_{m2}^*(t + T_{B2})$, $v_{CA2}^*(t + T_{sw})$, we can use T_{B2} to regulate the dc-link current i_{m2} and T_{A2} to control the stacked-side voltage v_{CA2} . Here, $i_{m2}^*(t + T_{B2})$ is the peak current reference of i_{m2} and can be converted from the average reference $i_{m2,avg}^*(t)$, which is similar to (26).

With the system model in (41), the vector timing T_{B2} to control the dc-link current to track its reference can be calculated in (47). If T_{B2} in (47) is calculated to be larger than $T_{sw} - T_{ZVS} - T_{res}$, a saturation upper limit should be enforced.

$$T_{B2} = \frac{i_{m2}^*(t+T_{B2}) - i_{m2}(t)}{v_{CB}(t)/L_{m2}} \quad (47)$$

The dc-link current prediction after T_{B2} is given by (48).

$$i_{m2}(t + T_{B2}) = \frac{T_{B2}}{L_{m2}} v_{CB}(t) + i_{m2}(t) \quad (48)$$

With the system model in (45) and two modules to restore the balance, the vector timing T_{A2} to regulate the stacked-side voltage for its reference is obtained in (49). Here, the second-

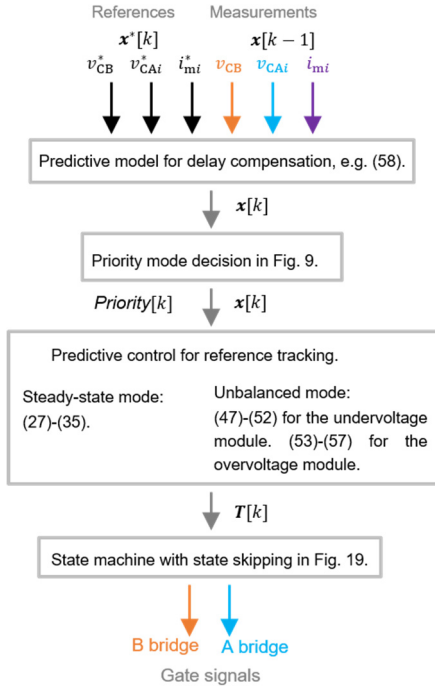


Fig. 16. The control flow chart for the MPPS control method.

order term is optional and is a trade-off between simplicity and accuracy. In the steady-state mode, steady-state error is important and the second-order term should be included, while the unbalanced mode is not related to the steady-state error. The function of the unbalanced mode is to steer the state variables to restore the voltage balance and then the converter will transition to the steady-state mode.

$$T_{A2} = \frac{(v_{CA2}^*(t+T_{sw}) - v_{CA2}(t))(C_{A1} + C_{A2})}{2i_{m2}(t+T_{B2})} \quad (49)$$

The dc-link current prediction after T_{A2} is given by (50).

$$i_{m2}(t + T_{sw}) = -\frac{T_{A2}}{L_{m2}} v_{CA}(t) + i_{m2}(t + T_{B2}) \quad (50)$$

To ensure no big undershoot, the dc-link current is compared to the lower limit and a saturation limit in (51) can be enforced.

$$T_{A2} = \frac{i_{m2}(t+T_{B2}) - i_{m2_lower_limit}(t)}{v_{CB}(t)/L_{m2}} \quad (51)$$

For a constant switching frequency, (52) is used for the zero-vector dwelling time. In fact, after T_{A2} or T_{B2} computation, the sum of the existing vectors' dwelling time should be examined and the maximum limit is allowed up to $T_{sw} - T_{ZVS} - T_{res}$.

$$T_{z2} = T_{sw} - T_{ZVS} - T_{res} - T_{A2} - T_{B2} \quad (52)$$

For module 1, i.e., the overvoltage module in Fig. 10 (b) in the unbalanced mode, the vector sequence is the same as that of module 1 in the steady-state mode due to the same MV-LV power flow direction. The control equations are similarly derived. To track the stacked-side capacitor voltage reference v_{CA1}^* , the A bridge switching time T_{A1} can be obtained in (53).

$$T_{A1} = \frac{(v_{CA1}(t) - v_{CA1}^*(t+T_{sw}))(C_{A1} + C_{A2})}{2i_{m1}(t)} \quad (53)$$

Table II. Simulation parameters of the M-S4T under the MPPS control.

Parameters	Module 1	Module 2	Controllers
Magnetizing Inductance (L_m)	7.7 mH	6.3 mH	7 mH
Filter Capacitor (C_A)	5.25 μ F	4.75 μ F	5 μ F
Filter Capacitor (C_B)	115.2 μ F in total for the LV-paralleled modules		128 μ F

The dc-link current after T_{A1} can be predicted by (54).

$$i_{m1}(t + T_{A1}) = \frac{T_{A1}}{L_{m1}} v_{CA1}(t) + i_{m1}(t) \quad (54)$$

If the dc-link current is outside certain limits, e.g., [0.6, 1.5] pu, a saturation limit should be applied to T_{A1} in (55).

$$T_{A1} = \frac{i_{m1_upper_limit}(t) - i_{m1}(t)}{v_{CA1}(t)/L_{m1}} \quad (55)$$

For the dc-link current reference tracking, the switching time for the B bridge is given by (56). Here, $i_{m1}^*(t + T_{sw})$ is the reference for the valley of the dc-link current and can be commanded directly or converted from the average value, which is similar to (26).

$$T_{B1} = \frac{i_{m1}(t+T_{A1}) - i_{m1}^*(t+T_{sw})}{v_{CB}(t)/L_{m1}} \quad (56)$$

The freewheeling time is then calculated using (57). After the calculation of (53), (55) and (56), the sum of the existing vector timings are examined to ensure that T_{z1} will be non-negative.

$$T_{z1} = T_{sw} - T_{ZVS} - T_{res} - T_{A1} - T_{B1} \quad (57)$$

To summarize, the control in the unbalanced mode based on the discrete-time large-signal model is shown in the flow chart in Fig. 16. The stacked-side balancing can be restored as fast as possible and the robust dc-link current regulation is ensured.

VI. SIMULATION AND IMPLEMENTATION OF THE MPPS FOR SLICS

A. Simulation Results with Parameter Mismatch

The proposed MPPS is simulated in the M-S4T, with parameter mismatch intentionally increased to 10% in Table II, to verify robustness of the MPPS. Threshold 1 in Fig. 9 for priority shifting is 5%, while threshold 2 is 3%. The dc-link current upper and lower limits are 1.3 pu and 0.7 pu with respect to its reference value. k_p in (32) is 0.002.

The simulation results are shown in Fig. 17 with the same disturbances in the PI simulation, i.e., stacked-side unbalance at 25 ms and a 40% to 100% load step change at 50 ms. Fig. 17 illustrates that at 25 ms, the stacked-side voltage balance falls outside of the 5% threshold. In the priority trace, the two converter modules decide to enter the unbalanced mode as expected. The priority is given to the stacked-side balancing and the dc-link current regulation to restore the stacked-side voltage balancing quickly. Consequently, load voltage is temporarily sacrificed and drops, while the stacked-side balance is quickly being restored. After several switching cycles, the stacked-side is balanced again, i.e., within the 3% threshold and the converter modules go back into the steady-

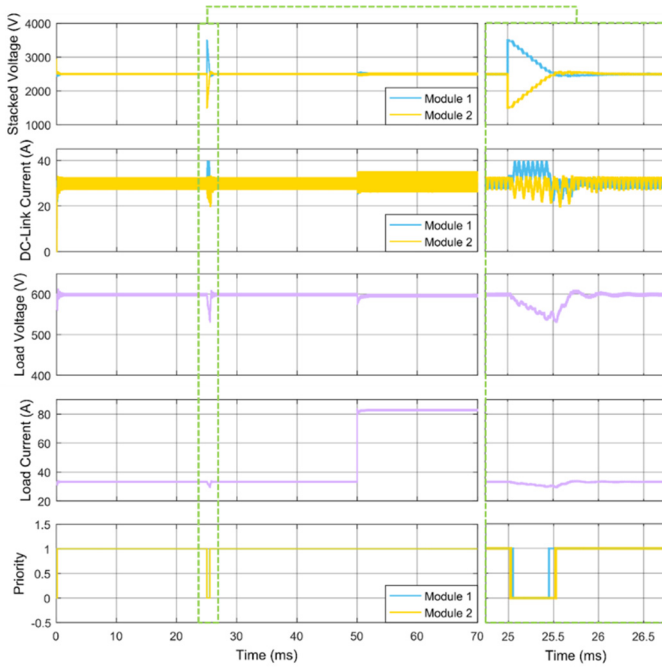


Fig. 17. Simulation results of the two-module M-S4T with the MPPS control for comparison against the PI control. The zoomed results have the same legends. For the priority mode plot, “0” stands for the unbalanced mode and “1” stands for the steady-state mode.

state mode as shown in the priority trace. Then, the load voltage is regulated to its reference value. The dc-link peak current limit $i_{m_upper_limit}$ in the control equations, e.g., (55), is set to be 1.3 pu. In other words, higher dc-link current is allowed under transients for temporary higher power processing capability, which is why module 1’s dc-link current goes as high as 40 A. It indicates the dc-link current is under the MPPS control and follows the preset limit. At 50 ms, when the load change is applied, all the state variables are regulated about their references. Especially, the stacked-side balancing is not perturbed, which shows almost no coupling among the load regulation, the dc-link regulation, and the stacked-side balancing in the steady-state mode. Moreover, the response speed is fast with only $\sim 4\%$ undershoot on the load voltage.

To further verify the scalability of the MPPS control to higher number of modules, a four-module M-S4T is simulated, where two of the four modules have the same mismatched parameters as module 1 in Table II and the other two of the four modules have parameters the same as module 2 in Table II. The filter capacitor C_B is sized to be 281.6 μF in the plant and 256 μF in the controller. Threshold 1 and threshold 2 in Fig. 9 for priority shifting are 8% and 5%, respectively. In this simulation, with priority mode information communicated to each other, all the modules will enter the unbalanced mode if any module has stacked-side voltage deviation higher than threshold 1. The other parameters remain the same as the two-module M-S4T. MPPS control equations and converter models for the four-module case are derived similar to the two-module case. At 25 ms, stacked-side voltage unbalance is intentionally induced. The modules transition to the unbalanced mode and the stacked-side voltages converge to balanced values in several switching cycles. Then, the load voltage is regulated back to the

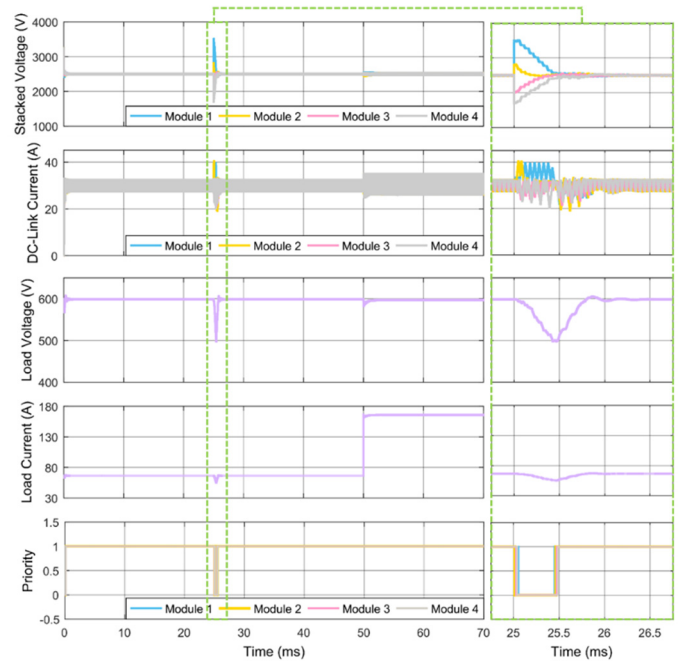


Fig. 18. Simulation results of a four-module M-S4T with the MPPS control. The scalability of the MPPS control is verified.

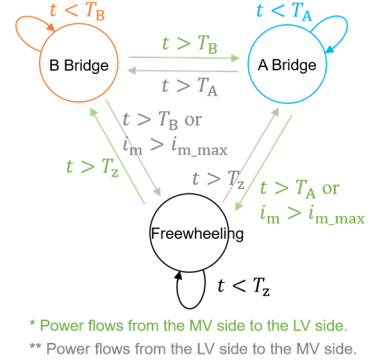


Fig. 19. State machine in the FPGA with real-time state skipping to avoid the dc-link overcurrent for robustness under large disturbances.

reference. At 50 ms, a 40% to 100% load step change occurs. The stacked-side voltage remains balanced even under this disturbance and the load voltage only has $\sim 3\%$ undershoot.

To summarize, the capability of the MPPS control to achieve fast and robust regulation under large disturbances and the scalability to high number of modules have been verified.

B. The State Transition Diagram and State Skipping to Ensure No Overcurrent under Large Disturbances

A state machine is implemented in a FPGA controller for vector transitions as illustrated in Fig. 19. For the SLIC, the dc-link current can be energized from a normal to an abnormal value within a switching cycle. Therefore, when faults or large disturbances occur, taking action immediately is better than waiting until the next switching cycle. Hence, once dc-link overcurrent is detected higher than the preset threshold, the converter leaves the dc-link charging state, i.e., state skipping. Moreover, as the freewheeling state is after the dc-link charging state, the freewheeling time in this switching cycle can be

increased accordingly to maintain a constant switching frequency.

C. Computation and Sampling Delay Compensation

In practical implementation of any digital control method, the sampling and computation delays should be considered. Ideally, the controller takes samples $x[k]$ at the instant k and computes $T[k]$ instantaneously for the converter to execute at the instant k . However, this doesn't occur due to non-zero sampling and computation time. Suppose it takes one switching cycle for the DSP to compute. The measurements $x[k-1]$ are taken at the instant $k-1$. Then, the computation for vector timings $T[k]$ starts at the instant $k-1$ and ends at the instant k . The converter executes $T[k]$ at the instant k and expects the variables to reach their references at $k+1$. Thus, the state variables $x[k]$ are needed at the instant $k-1$ for the controller to compute $T[k]$. Fortunately, $x[k]$ can be predicted using the system model with the measurements $x[k-1]$ and the vector timings $T[k-1]$ to be applied to compensate for the delay. Take the dc-link current as an example. Suppose the converter is commanded in the steady-state mode and the plant model in (21) can be used. In (58), the dc-link current can be estimated to compensate for the sampling and computation delay, assuming that the voltage variation in (15) is small enough and neglected. For other state variables, similar strategy can be applied.

$$i_{m1}[k] \approx \frac{T_{A1}[k-1]v_{CA1}[k-1] - T_{B1}[k-1]v_{CB}[k-1]}{L_{m1}} + i_{m1}[k-1] \quad (58)$$

VII. EXPERIMENTAL VERIFICATION OF THE MPPS FOR SLICS

The experimental setup of a two-module series-stacked 600 V to 5 kV DC transformer (DCT) is shown in Fig. 20. Each MVDC DCT module is based on the improved S4T with reduced conduction loss topology [20]. The tested power flow direction is LV to MV due to the lack of high-voltage high-power dc source. The MPPS control is based on the same principle as the MV-LV power flow direction. The MV side is connected to a load resistor bank and the LV side is coupled to a LV rectifier. The magnetizing inductance of the 4:1 transformer is used as the dc link of the S4T. The parameters of the designed 25 kVA 16 kHz module is shown in Table III. The transformers are manufactured with the same core and the filter capacitors are from the same manufacturer, but the authors did not intentionally tune the parameters of the two modules to be the same to further verify the robustness of the MPPS under practical conditions. The film capacitor and the magnetizing inductance of the transformer typically have $\pm 10\%$ - 20% tolerance. A controller with FPGA Cyclone IV EP4CE75F23C7 and DSP TMS320C6713B is used to implement the MPPS code. The sampling and computation delay of the DSP is compensated with the predictive model in (58). The thresholds 1 and 2 in Fig. 9 for priority shifting are both 10%. However, hysteresis-based transition can be added similar to the simulation depending on the specific operating conditions.

Table III. The parameters of the designed converter prototype of the improved S4T with reduced conduction loss.

Parameters	Value
Magnetizing inductance (L_m)	4.3 mH
Resonance inductor (L_{rA})	80 μ H
Resonant capacitor (C_{rA})	6.25 nF
Resonance inductor (L_{rB})	5 μ H
Resonant capacitor (C_{rB})	100 nF
Filter capacitor (C_{A1}, C_{A2})	4.9 μ F
Filter capacitor (C_B)	60.0 μ F

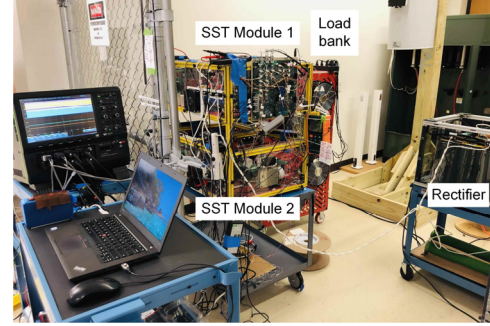


Fig. 20. The 5 kV dc M-S4T test setup.

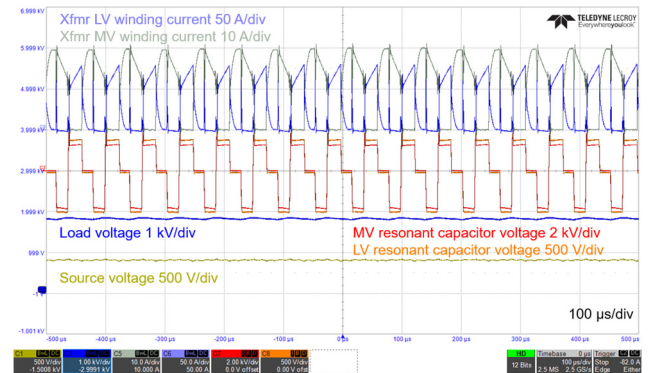


Fig. 21. Steady-state waveforms of one SST module.

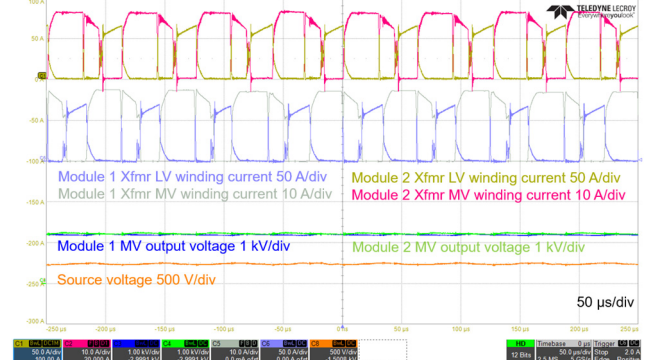


Fig. 22. Steady-state waveforms of two stacked SST modules. The two modules are interleaved by half of a switching cycle.

The steady-state operation of a single module is illustrated in Fig. 21, where the transformer LV and MV winding currents are i_{sec} and i_{pri} in Fig. 1 (b). The magnetizing current i_m is the sum of the MV and the LV winding currents and can be observed from the envelopes of the winding currents. The MV and LV resonant capacitors are C_{rA} and C_{rB} . The load voltage refers to the MV output voltage, i.e., v_{CA} . The source voltage refers to v_{CB} . In this section, these terms are used to describe

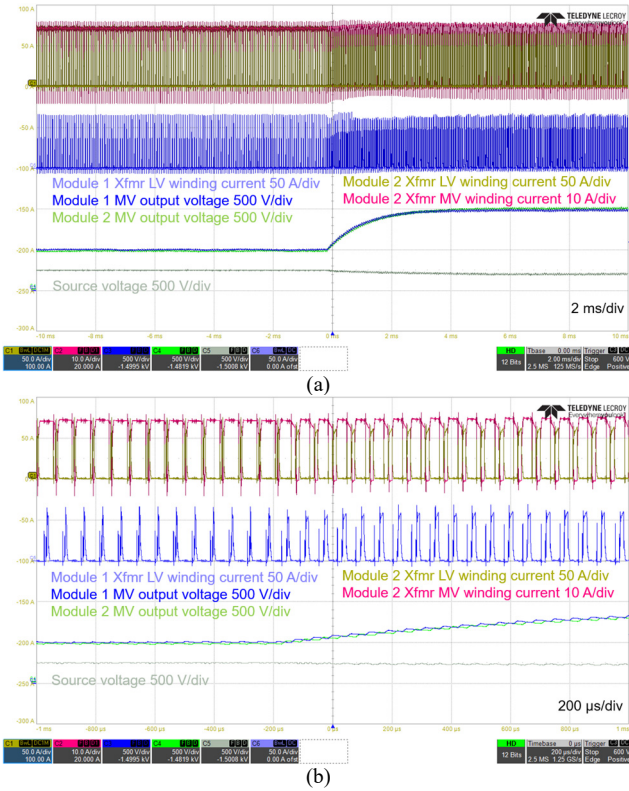


Fig. 23. (a) Load-voltage-reference step-change test of two stacked SST modules. (b) Zoomed version.

the results. In Fig. 21, in steady state, the magnetizing current and the load voltage are regulated about their references. Considering the 3.3 kV devices on the MV side and the 1.2 kV devices on the LV side, the resonant capacitor voltages are within safe operating limits.

The steady-state operation of two stacked modules is shown in Fig. 22, where the interleaved operation can be observed. The controller is in the steady-state priority mode as the stacked-side capacitor voltages, i.e., MV output voltages of the two modules are balanced. During steady state, the magnetizing current and the load voltage are regulated about their references. The output voltages of the two modules are balanced and steady with low distortions. In Fig. 22, the high-frequency noise in the transformer MV winding current of module 2 is due to the noise picked up by that current probe.

The step response of the two stacked modules is shown in Fig. 23. The envelopes of the transformer’s winding current of the two modules are steady with very small transients. Hence, the dc-link currents, i.e., the magnetizing currents of both the modules are regulated about the references even during the stacked-side step change. Moreover, during the step change, it should be noted that the two modules’ output voltages, i.e., the stacked-side filter capacitor voltages are balanced and the two modules are in the steady-state priority mode. In fact, one challenge aforementioned for the SLIC control is the coupling between the input and the output and between the stacked modules due to the reduced dc link. The above observations in the waveforms indicate the balancing function in the MPPS method is to some extent decoupled with the dc-link regulation

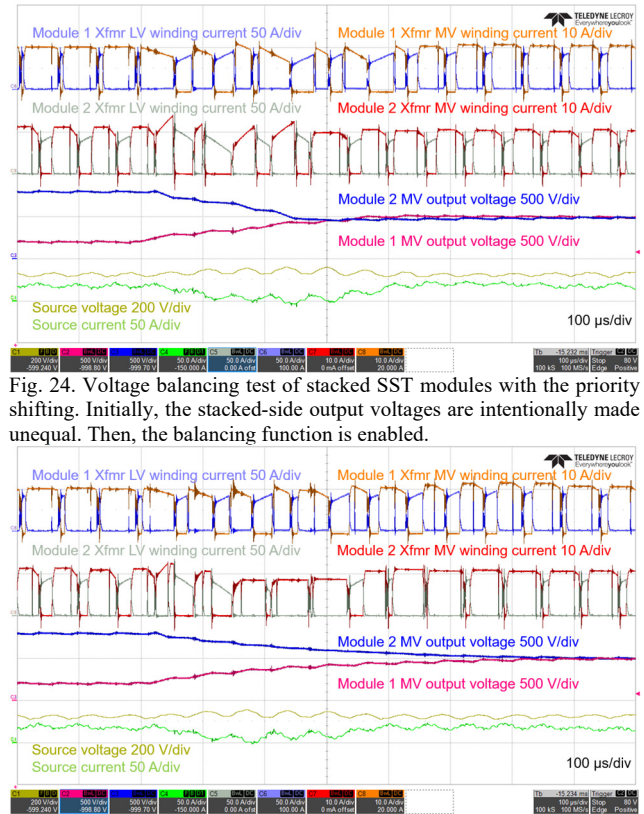


Fig. 24. Voltage balancing test of stacked SST modules with the priority shifting. Initially, the stacked-side output voltages are intentionally made unequal. Then, the balancing function is enabled.

Fig. 25. Voltage balancing test of stacked SST modules without the priority shifting. The settling time is longer than that with the priority shifting because with priority shifting more control efforts are devoted to the stacked-side balancing to restore the balance as fast as possible.

and the output-voltage regulation functions, which is desirable. Moreover, the 2 ms step response speed is fast, compared to the conventional high-inertia SSTs with PI controllers.

In Figs. 24-25, the voltage balancing function of the proposed MPPS control is verified. The model prediction feature is enabled in both Fig. 24 and Fig. 25. Meanwhile, the priority shifting feature is enabled in Fig. 24 but not in Fig. 25. In other words, the converter is always in the steady-state mode in Fig. 25, while in Fig. 24 the converter can transition to the unbalanced mode according to Fig. 9. Remember in the steady-state mode, as described in Fig. 2, the common-mode power supplies the load, while the differential-mode power balances the stacked-side voltages. However, the saturation limit in (2), i.e., finite power rating of the converter, defines the sum of the maximum control efforts devoted to the load-voltage regulation and the stacked-side balancing. Thus, these two objectives share the full power rating of the converter. With priority shifting, the load-voltage regulation is given up and more control efforts are devoted to the stacked side. Therefore, the stacked-side balancing can be restored much faster.

In Fig. 24, when the unbalance is larger than 10%, the converter modules are in the unbalanced mode. During this time, the module 2 has higher voltage than the module 1 and the module 2’s transformer LV winding current has negative slope, which indicates that the magnetizing inductance is discharged by the LV source when the stacked-side balance is

being restored. That is the dc-link inductance of the module 2 absorbs energy from its MV filter capacitor and releases energy to the LV source. With the temporary MV-LV power flow direction, the module 2 can decrease its stacked-side voltage and contributes to the restoration of the balancing. Moreover, during the unbalanced mode in Fig. 24, the zero-vector dwelling time is nearly zero, i.e., the duration when the magnetizing current is freewheeling and the transformer winding current is nearly constant. The small zero-vector time indicates that the converter has saturated and is processing the maximum power possible to restore the balancing in the shortest time possible. The settling time is approximately 250 μs . In Fig. 25, though the module 2 also changes its power flow direction and contributes to the stacked-side balancing to some extent when the voltages are unbalanced, less control efforts are devoted to the balancing task as discussed. The settling time is approximately 500 μs . With the model prediction feature, the settling time of 500 μs is already fast, while the priority shifting feature in Fig. 24 can further improve the settling time by 50%.

To summarize, the two-module test verifies the effectiveness of the proposed MPPS method on fast and robust stacked-side voltage balancing and dc-link regulation for the SLIC. The settling time of the system is achieved to be hundreds of microseconds to several milliseconds, smaller than the hundreds of milliseconds in the conventional SSTs with similar range of the switching frequency in [14]-[18] by more than an order of magnitude, thanks to the low-inertia nature of the converter and the fast and robust MPPS control method based on the large-signal model.

VIII. CONCLUSION

This paper presents the multi-objective, multi-degree of freedom control problem of the stacked low-inertia converters (SLIC) or cascaded reduced dc-link solid-state transformers (SST). Due to the small dc-link storage, which increases the coupling between input and output and between modules, priority shifting and high-bandwidth control are the key to ensure dc-link regulation and voltage balance under disturbances and controller saturation conditions. Moreover, owing to the large dc-link ripple, the traditional SVPWM, the average model, and the small-signal-model-based control design cannot accurately modulate, capture, and control the dynamics of the reduced dc link. The conventional PI controller's inability to achieve stable operation of the SLIC is simulated and discussed. A discrete-time large-signal model and a fast and robust model predictive priority-shifting (MPPS) control method for the SLIC are proposed. The performance of the proposed control is verified through simulations and experiments on a 5 kV low-inertia SST prototype. According to existing literature, the settling time is achieved more than an order of magnitude smaller than the conventional high-inertia SST or PET.

APPENDIX

The large-signal model of the two-module M-S4T in the steady-state mode is shown in (A1), where the second-order

term exists to capture the reduced dc-link dynamics. (A2) is the voltage unbalance term in (A1).

$$\begin{aligned} & \begin{bmatrix} i_{m1}[k+1] \\ i_{m2}[k+1] \\ v_{CA12}[k+1] \\ v_{CB}[k+1] \end{bmatrix} \approx \\ & \begin{bmatrix} i_{m1}[k] + \frac{T_{A1}[k]}{L_{m1}} v_{CA1}[k] - \frac{T_{B1}[k]}{L_{m1}} v_{CB}[k] \\ i_{m2}[k] + \frac{T_{A2}[k]}{L_{m2}} v_{CA2}[k] - \frac{T_{B2}[k]}{L_{m2}} v_{CB}[k] \\ v_{CA12}[k] + \sum_{i=1}^2 (-1)^i \left(\frac{2i m_i[k]}{C_{A1} + C_{A2}} T_{Ai}[k] + \frac{T_{Ai}^2[k]}{L_{mi}(C_{A1} + C_{A2})} v_{CAi}[k] \right) \\ v_{CB}[k] - \frac{v_{CB}[k]}{R_{BCB}} T_{sw} + \sum_{i=1}^2 \left(i_{mi}[k] + \frac{v_{CAi}[k] T_{Ai}[k]}{L_{mi}} \right) \frac{T_{Bi}[k]}{C_B} - \frac{T_{Bi}^2[k] v_{CB}[k]}{2L_{mi} C_B} \end{bmatrix} \quad (\text{A1}) \\ & v_{CA12}[k] = v_{CA1}[k] - v_{CA2}[k] \quad (\text{A2}) \end{aligned}$$

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