

Development of Broadband Noise Models and Radio Frequency Integrated Circuits using Silicon Germanium HBTs

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Development of Broadband Noise Models and Radio Frequency Integrated Circuits using Silicon Germanium HBTs

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To my parents

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SUMMARY

A novel “transit time” based analytical broadband noise model is developed and implemented for high frequency bipolar transistors. This model is applied to a complementary ($npn + pnp$) silicon germanium (SiGe) heterojunction bipolar transistors (HBT). A complete set of analytical equations are derived using this transit time noise model, to express the four fundamental noise parameters in terms of device parameters.

A comprehensive analysis on the ac , dc and broadband noise performance of a 200 GHz SiGe HBT technology, under cryogenic temperatures, is presented. The transit time based noise model is used to analyze the RF noise behavior of the SiGe HBT down to 85 K. Significant performance gain is demonstrated in cryogenic temperatures indicating the suitability of SiGe HBT for extreme environment electronics.

A sub-circuit based substrate parasitic modeling methodology, in silicon based processes, is presented. A test case low noise amplifier, operating in the 5 GHz band, is designed in a SiGe HBT process and is used to demonstrate the validity of the design methodology. A dual-band, dual-mode transceiver front end for IEEE802.11a/b/g WLAN applications, is designed in a $0.8 \mu m$ SiGe HBT process. The transceiver uses a new architecture which uses an on-chip frequency doubler and a single off-chip frequency synthesizer for both the 2.4 and 5 GHz bands. The performance of the transceiver meets the specification of the IEEE802.11a/b/g standards.

The work described in the dissertation significantly advances the state-of-the-art in bipolar broadband noise modeling and RF, microwave circuit design using silicon based processes. The contributions and implications of this work for future research are discussed.

CHAPTER I

INTRODUCTION

1.1 The Information Age

We live in the information age. The spectacular growth of solid-state semiconductor technology has made it possible for people to stay connected and exchange information in a multitude of ways. Information reaches us through various different means, such as telephones, cellular networks, radios, televisions, and computers. Modern day life thrives on information, be it the satellite links that bring images from different parts of the world into our living rooms or sensitive information critical for a country's defense.

Information could be transmitted over a wired channel (e.g., copper wire, optical fiber, etc.) or over a wireless channel (e.g. ambient air, vacuum, and water). The wired communication era started with the use of copper wire as the medium that connected the entities that exchange information. This concept was employed in telephone and telegraph systems. With the advent of the laser in 1960, optical communication became a reality which allows much faster information exchange. Optical communication opens up enormous bandwidths of data exchange. A wavelength of 694 nm, for example, corresponds to a frequency of 5×10^{12} Hz. Such enormous speeds can not be achieved by purely electronic approaches.

Wireless communication technology came into existence at the turn of the 20th century, when Guglielmo Marconi demonstrated that information could be transmitted as electromagnetic waves. This was a revolutionary step in communication technology with far reaching consequences and great prospects. Over the next 100 years, wireless communication matured from two-way military-specific applications to

one-way radios and television broadcasting for the common man. However, ordinary two-way communication was still achievable only through wired channels. The invention of the transistor by John Bardeen, Walter Brattain, and William Shockley in 1947, and the development of Shannon's information theory, paved the way for affordable mobile communication in the form of car phones and eventually mobile cellular phones. In addition to cellular phones and pagers, wireless technology has opened up a variety of consumer markets with great potential of growth, namely, wireless local area network (WLAN), global positioning system (GPS), radio frequency identification system (RFID), etc. The ever-increasing number of applications has created the need for higher frequency carrier waves with proportionally increasing modulation bandwidths. The restrictions in band allocation for different applications make it necessary to transmit more and more information in a limited spectrum. This leads to an increased complexity of signal modulations that have evolved from scalar modulation schemes, such as amplitude modulation (AM) and frequency modulation (FM), to vector modulation schemes, such as phase shift keying (PSK), frequency shift keying (FSK), quadrature amplitude modulation (QAM), etc. Multiplexing schemes, such as time division multiple access (TDMA), frequency division multiple access (FDMA), and code division multiple access (CDMA) add another layer of hardware complexity. The use of highly complex signal modulation and multiplexing schemes accompanied by the use of denser constellations for maximum spectral efficiency place a stringent requirement on the performance of devices and circuits for next generation wireless communication systems.

Regardless of what the information is and how it is transmitted, we want to process it accurately, as fast as possible, at a low cost, and with minimal space and power consumption. Silicon Germanium (SiGe) Bipolar-CMOS (BiCMOS) technology is increasingly becoming the technology of choice for next generation communication systems, rising to the challenge of meeting stringent specifications required for

these applications, providing high levels of integration and lower overall cost.

1.2 SiGe HBT Technology and it's Applications

The concept of heterostructure was pioneered by Herbert Kroemer in 1957 which formed the basic theory behind the development of SiGe heterojunction bipolar transistor [1],[2] for which he was awarded the Nobel Prize in physics in 2000. Heterostructures may be defined as heterogeneous semiconductor structures built from two or more different semiconductors with different bandgaps, such as Gallium Arsenide (GaAs), Aluminum Gallium Arsenide (AlGaAs), Indium Phosphide (InP), Indium Gallium Arsenic Phosphide (InGaAsP), and SiGe. The material structures are selected so that the crystal structures can fit one another, implying that there is a minimal lattice mismatch between the semiconductor materials.

It is possible to engineer the electrical and optical properties of a heterostructure material. Through the choice of layer compositions, thicknesses and doping, one can optimize the motion of electrons, control the interaction between electrons and photons (light), and build optical waveguides for controlling the propagation of light.

In HBTs, the current gain, β , increases drastically with increasing difference in the bandgap energies of the two semiconductors. The reason for this is the strong dependence of the intrinsic carrier concentration on the bandgap difference [3]:

$$n_i \propto e^{\sqrt{\frac{-\Delta E_g}{kT}}} \quad (1)$$

where n_i is the intrinsic carrier concentration, ΔE_g is the bandgap energy difference, k is the Boltzmann's constant and T is the absolute temperature. Assuming a short base and neglecting base recombination, the current gain can be related to the physical parameters of the device by,

$$\beta = \frac{D_B W_E N_E e^{\frac{\Delta E_g}{kT}}}{W_B N_B D_E} \quad (2)$$

where ΔE_g is the difference in the bandgap between the emitter and the base, D_B

is the diffusion constant for electrons (in the case of an *npn* device) in the base, D_E is the diffusion constant for holes in the emitter, W_B is the width of the base, W_E is the width of the emitter, N_B is the doping concentration in the base, and N_E is the doping concentration in the emitter.

The exponential term in equation (2) can be quite large, thus leading to a large value of β . Furthermore, this gain enhancement can be achieved while simultaneously increasing the base doping which means that the base width can be lowered without risking device “punch-through,” and hence reducing the base resistance. The higher current density in an HBT also allows the use of smaller device size than a BJT, for equivalent currents, thus reducing the device parasitics. As a result, an HBT has a higher unity current gain cutoff-frequency (f_T) and maximum frequency of oscillation (f_{max}) compared to a BJT.

The physical realization of the SiGe HBT took a good 30 years owing to material growth limitation, largely because of a 4% mismatch in the lattice constants of silicon and germanium. Though the first functional SiGe HBT was demonstrated in 1987 [4], [5], the SiGe HBT technology turned a corner in 1990 with the demonstration of a non-self-aligned SiGe HBT grown by ultra-high vacuum/chemical vapor deposition (UHV/CVD) technique, with a peak cut-off frequency (f_T) of 75 GHz [6], [7]. Within a span of three years, the peak- f_T of SiGe HBTs crossed the 100 GHz mark [8], and the first commercial production was started in 1994 [9]. Commercial SiGe HBT technologies with transistor peak- f_T in the 50-100 GHz range exist in many companies worldwide now (e.g. [10]) and peak- f_T greater than 350 GHz has been reported in the literature [11]. Figure 1 shows the trend of peak- f_T of silicon based bipolar transistors since the early 1980s [12], [13]. The tremendous increase in the speed of operation of SiGe HBT’s opens up the possibility of designing radio frequency (RF), microwave and millimeter-wave ($f > 30$ GHz) circuits in silicon based technologies.

Early development in SiGe HBT technology was almost exclusively based on

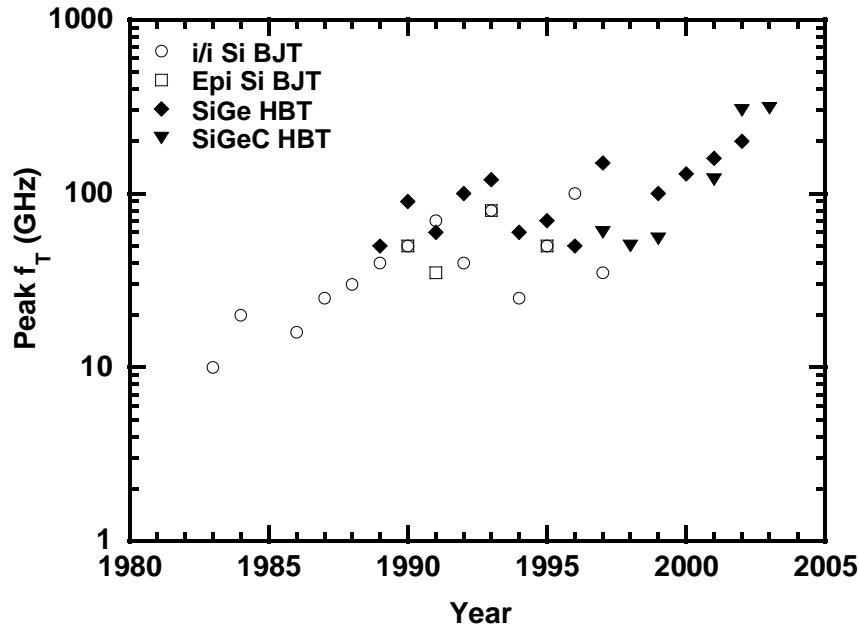


Figure 1: Trend of peak cutoff-frequency (f_T) of Si and SiGe bipolar transistors over the years.

npn-only processes, with very poor performance of *pn**p* transistors. The design and optimization of *pn**p* SiGe HBTs is an extremely complicated process [13], and their successful monolithic integration with *npn* SiGe HBTs proved to be extremely challenging to achieve in practice. High performance complementary-SiGe (C-SiGe) BiCMOS technologies containing both *npn* and *pn**p* HBTs have been reported very recently [14], [15], allowing for the development of high precision analog circuits which require complementary bipolar transistors. These C-SiGe processes can be effectively employed in designing a multitude of analog, mixed-signal, and RF integrated circuits (IC), such as driver amplifiers, data converters, cable modems, etc. The high performance *pn**p* transistors can be used to design “push-pull” driver stages and active loads, and are very useful in designing low-voltage, and low-power circuits. They can help enhance circuit performance by reducing the total supply current, and improving the power-delay performance.

Bandgap engineering also has a very favorable influence on the low-temperature

and cryogenic operation of SiGe HBTs, an area where silicon-BJTs proved to be inadequate [16]. Cryogenic electronics represent an important niche market with applications such as high-sensitivity cooled sensors and detectors, satellite systems, deep-space and planetary missions, very high precision instrumentation and detector electronics, superconductor-semiconductor hybrid electronic systems, and very low-noise receivers for radio astronomy applications.

The rapid development of SiGe device technology has paved the way for a huge application space for silicon based devices and, consequently, has introduced many challenges in the characterization, modeling and circuit development using SiGe HBTs. Analysis of the broadband noise performance of the transistors is critical for the design of wireless and wired communication ICs, where low noise and high gain at high frequencies are essential. A complete noise characterization of SiGe HBTs and robust models that fit the data, are necessary for designing radio frequency integrated circuits (RFICs), monolithic microwave integrated circuits (MMICs), and opto-electronic integrated circuits (OEICs). Much research has been devoted to the high frequency broadband noise of bipolar transistors [17]-[27], cryogenic operation of SiGe HBTs [28]-[32], and RFIC development in SiGe, in the 2-10 GHz band [33]-[40]. However, with the advent of very high- f_T SiGe HBTs (in hundreds of GHz), the broadband noise models need to be explored more thoroughly, and the impact of increase in the gain (β) and cutoff-frequency (f_T) need to be fully analyzed. The overall ac and noise performance of SiGe HBTs under cryogenic temperatures is not very well understood and a comprehensive investigation needs to be done to quantify the performance of SiGe in cryogenic regimes. RF front-end circuits need to be developed to investigate the performance leverage SiGe HBTs provide. Signal coupling through the lossy substrate becomes quite a significant problem in the design of RF circuits using silicon based technologies. The substrate parasitics need to be carefully accounted for, and modeled to optimize the circuit performance and achieve

desired specifications.

1.3 Conclusion

Silicon germanium heterojunction bipolar transistor technology has recently emerged as a prominent enabler for high-frequency analog, RF and mixed-signal applications. The tremendous advancement of SiGe technology over the last few years has led to a remarkable improvement in the SiGe HBT performance and has allowed it to challenge traditional III-V device technologies like GaAs and InP. The excellent device performance of SiGe HBTs, coupled with the high level of single chip integrability with standard silicon complementary metal oxide semiconductor (CMOS) technology has made it a technology of choice for various wireless and wired communication systems in the 800 MHz - 10 GHz range, encompassing applications like CDMA, global system for mobile communications (GSM), IEEE 802.11a/b/g WLAN, etc. SiGe HBT technologies are also demonstrating competitive performance for certain niche applications like radio astronomy, extreme-environment electronics, etc., traditionally a forte of compound semiconductor technologies, such as, InP.

This work contributes to the ongoing research efforts to develop accurate bipolar broadband noise models for circuit design by developing a “transit-time” based noise model using the “noisy two port” analysis [19]. This work is envisioned to provide a framework for the development of accurate noise models for very high performance bipolar transistors. The proposed modeling technique is demonstrated for a C-SiGe (*nnp* + *pnp*) HBT technology. In a bipolar transistor (both BJT and HBT) the sources of noise are the base and collector “shot noise” currents and the thermal noise of the base-resistance. The correlation of the base and collector shot noise sources is neglected in the traditional and state-of-the-art modeling approaches, such as, Vertical Bipolar Inter-Company (VBIC) model [41], Most Exquisite Transistor Model (MEXTRAM) [42], and the High Current Compact Transistor Model

(HICUM) [43]. While that approximation is valid for frequencies significantly lower than the peak- f_T and for low gain devices, it does not accurately model the noise for highly scaled, high performance HBTs which have much higher operating frequencies and current gains. In such cases, it becomes essential to account for this correlation term. In this work a transit time based noise model is developed for a complementary SiGe HBT technology that takes into account this correlation. A complete set of analytical equations are derived to express the four fundamental noise parameters in terms of the device parameters of an HBT. A comprehensive ac and broadband noise characterization of a 200 GHz peak- f_T SiGe HBT technology, is performed at different temperatures, from room temperature (300 K) down to 85 K, to analyze and quantify the cryogenic performance of SiGe HBTs.

From the circuit design point of view, the emergence of high performance SiGe HBT technologies has motivated the design of RF circuits in silicon as a possible alternative to using GaAs HBT. However, the significantly higher substrate parasitics in silicon [44]-[46], lower gain of the devices, and higher noise, make RF circuit design in SiGe HBT a considerable challenge. In this work some of these challenges are addressed, and techniques for the development of RF circuits using silicon based processes are explored. A sub-circuit based substrate parasitic model is developed that uses the physical distance between different circuit components on the same substrate, and the electrical properties of the substrate, to accurately model the effect of these parasitic resistances, capacitances and inductances. A low noise amplifier (LNA) is designed to operate in the 5 GHz band where the substrate modeling methodology is employed to account for the parasitics. Excellent agreement between simulation and measurement results of the LNA is demonstrated. A dual-band, dual-mode RF front-end transceiver is developed for IEEE 802.11a/b/g wireless local area network (WLAN) applications using a SiGe HBT process. Careful modeling of the substrate parasitics is done to optimize the circuit performance. A novel architecture, using

an on chip frequency doubler for the receiver, is developed which requires only one external frequency synthesizer for both 2.4 GHz (802.11b/g) and 5 GHz (802.11a) frequency bands. This is envisioned to pave the way for the development of mixed signal, RF, microwave and millimeter wave circuits for emerging applications, such as, 60 GHz WLAN, using SiGe HBTs and advance the state-of-the-art in the design of silicon-based RF circuits.

1.4 Organization

The rest of the thesis is organized as follows:

Chapter 2 discusses the fundamentals of bipolar noise modeling using a “two-port” noise theory. The “transit time” based noise model is described in detail and the comprehensive modeling results are presented for a C-SiGe HBT technology.

Chapter 3 describes the fundamentals of cryogenic ac and broadband noise measurements. The measurement setup is described in detail and the challenges in performing cryogenic measurements are discussed. A comprehensive analysis on the ac and RF noise performance of a 200 GHz SiGe HBT technology is presented.

Chapter 4 examines the substrate parasitic effects in silicon and presents a methodology for the development of RF front-end circuits on silicon. A sub-circuit based model is developed to account for the substrate parasitics and a 5 GHz test-case LNA is developed in a SiGe HBT technology to demonstrate the validity of the modeling technique.

Chapter 5 presents an IEEE 802.11a/b/g dual-band dual-mode RF front-end transceiver with a novel architecture that uses an on-chip frequency doubler and a single off-chip frequency synthesizer to switch between two bands (2.4 GHz and 5 GHz).

Chapter 6 summarizes the contributions of this dissertation and discusses the possible future work that this work could motivate.

CHAPTER II

BROADBAND NOISE MODELING OF HETEROJUNCTION BIPOLAR TRANSISTORS

2.1 *Two-port Noise Theory*

The full noise characterization of any transistor (or any two-port network) requires the determination of the four noise parameters:

1. minimum noise figure, NF_{min} , (or alternately, the minimum noise factor F_{min}),
2. noise resistance, R_n ,
3. optimum source conductance, $G_{s,opt}$,
4. optimum source susceptance, $B_{s,opt}$.

From the theory of linear noisy networks [47], any noisy two-port can be replaced by its noise-less counterpart and two input-referred noise sources. Figure 2 shows the noise equivalent circuit of a SiGe HBT with an input-referred voltage noise generator v_n and an input-referred current noise generator i_n . These two noise sources are, in general, correlated. Regardless of the physical sources of noise in the device, the four noise parameters (F_{min} , R_n , $G_{s,opt}$, and $B_{s,opt}$) can be expressed as functions of the noise spectral densities S_{i_n} , S_{v_n} and their cross-correlation $S_{i_nv_n^*}$ [47]:

$$F_{min} = 1 + 2(C_r + \sqrt{R_n G_n - C_i^2}) \quad (3)$$

$$G_{s,opt} = \sqrt{\frac{G_n}{R_n} - \left(\frac{C_i}{R_n}\right)^2} \quad (4)$$

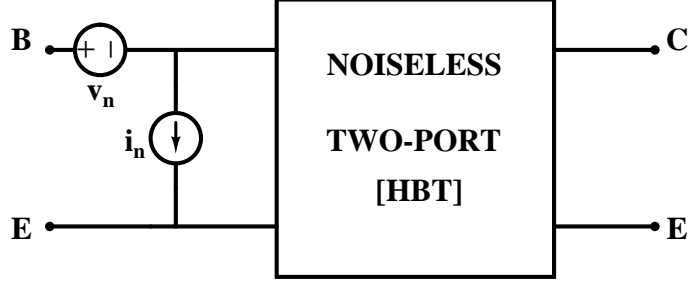


Figure 2: Schematic illustration of the noisy two-port representation of the SiGe HBT.

$$B_{s,opt} = \frac{C_i}{R_n} \quad (5)$$

where,

$$R_n = \frac{S_{v_n}}{4kT} \quad (6)$$

$$G_n = \frac{S_{i_n}}{4kT} \quad (7)$$

$$C_r = -\frac{Re\{S_{i_n v_n^*}\}}{4kT} \quad (8)$$

$$C_i = -\frac{Im\{S_{i_n v_n^*}\}}{4kT}. \quad (9)$$

The noise factor for some other source admittance $Y_s = G_s + jB_s$ is given by,

$$F = F_{min} + \frac{R_n}{G_s} |Y_s - Y_{s,opt}|^2. \quad (10)$$

In many cases, the reflection coefficient Γ_s is preferred as opposed to the source admittance Y_s . The relation between any admittance and the corresponding reflection coefficient is given by

$$\Gamma_s = \frac{1 - Y_s Z_0}{1 + Y_s Z_0} \quad (11)$$

where Z_0 is the characteristic impedance, and is 50Ω in our case. Using equation (11), we can thus find the $\Gamma_{s,opt}$ from the $Y_{s,opt}$, and vice versa.

system known from the calibration data.

2.3 Broadband Noise in Bipolar Transistors

In bipolar transistors, the dominant sources of noise at RF and microwave frequencies are the base and collector current shot noises and the base-resistance-induced thermal noise. The base and collector shot noises are given by

$$\overline{i_b^2} = 2qI_B\Delta f \quad (13)$$

$$\overline{i_c^2} = 2qI_C\Delta f \quad (14)$$

where I_B and I_C are the *dc* base and collector currents, respectively. In many standard noise modeling approaches used for computer aided design (CAD) (e.g., SPICE Gummel-Poon, VBIC, MEXTRAM, and HICUM models, or the thermodynamic model [24]), these base and collector noise terms are assumed to be uncorrelated. While this approach is acceptable for low operating frequencies [25], this assumption needs to be accounted for at higher frequencies and high current densities. Recent approaches using a “transit time” based noise modeling approach for *npn* SiGe HBTs have been presented previously [26], [27], using a common-base version of a correlated transit time model. The cross-correlation of the base and collector shot noises in that model is given by [17], [18],

$$\overline{i_b^* i_c} = 2qI_C(e^{-j\omega\tau_n} - 1)\Delta f \quad (15)$$

where τ_n represents the time delay between the base and the collector, and is extracted by fitting the NF_{min} versus frequency curve. From equations (13)-(15), and noting that the thermal noise due to the base resistance is $4kTr_b$, we can derive the noise spectral densities to obtain [59],

$$S_{v_n} = 4kTr_b + \frac{2qI_C}{|Y_{21}|^2}, \quad (16)$$

$$S_{i_n} = 2q \frac{I_C}{\beta} + \frac{2qI_C}{|H_{21}|^2} - 4qI_C \operatorname{Re} \left[(e^{-j\omega\tau_n} - 1) \frac{Y_{11}}{Y_{21}} \right] \quad (17)$$

where $H_{21} = Y_{21}/Y_{11}$, by definition, and the cross-correlation terms are given by,

$$S_{v_n i_n^*} = 2qI_C \frac{Y_{11}^*}{|Y_{21}|^2} - \frac{2qI_C(e^{-j\omega\tau_n} - 1)}{Y_{21}} \quad (18)$$

and,

$$S_{v_n^* i_n} = [S_{v_n i_n^*}]^* \quad (19)$$

The base resistance r_b can be extracted from the measured Y-parameters using the circle impedance method [13]. Another important figure-of-merit from circuit design perspective is the associated gain (G_A), which is a measure of the maximum output power achievable when the input is noise matched, and is given by,

$$G_A = \left| \frac{Y_{21}}{Y_{11} + Y_{s,opt}} \right|^2 \frac{\operatorname{Re}(Y_{s,opt})}{\operatorname{Re}(Y_{out})} \quad (20)$$

where,

$$Y_{out} = Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11} + Y_{s,opt}} \quad (21)$$

To obtain analytic expressions for the four noise parameters, clearly useful for gaining more insight into device noise optimization, we need express the Y-parameters in terms of the fundamental device parameters, namely, β , g_m and f_T . The I - V relation can be written as,

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} g_{be} + j\omega(C_{be} + C_{bc}) & -j\omega C_{bc} \\ g_m - j\omega C_{bc} & j\omega C_{bc} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix} \quad (22)$$

We can then write the Y-parameters as,

$$Y_{11} = \frac{g_m}{\beta} + j\omega C_i \quad (23)$$

$$Y_{12} = -j\omega C_{bc} \quad (24)$$

$$Y_{21} \simeq g_m \quad (25)$$

$$Y_{22} = j\omega C_{bc} \quad (26)$$

where, $g_m = qI_C/kT$, $C_i = C_{be} + C_{bc}$, and $f_T = g_m/2\pi C_i$. Using equations (23)-(26) and substituting in equations(16)-(18), we obtain,

$$S_{v_n} = 4kTr_b + \frac{2kT}{g_m} \quad (27)$$

$$S_{i_n} \simeq 2qI_C \left[\frac{1}{\beta} + \frac{\omega^2 C_i}{g_m} \left(\frac{C_i}{g_m} - 2\tau_n \right) \right] \quad (28)$$

$$S_{v_n i_n^*} = 2kT \left[\frac{1}{\beta} + \frac{j\omega C_i}{g_m} \right] - \frac{2qI_C(e^{-j\omega\tau_n} - 1)}{g_m} \quad (29)$$

From equations (27)-(29) and using equations (3)-(9), we can rewrite the noise parameters as,

$$R_n = \frac{S_{v_n}}{4kT} = r_b + \frac{1}{2g_m} \quad (30)$$

$$G_{s,opt} = \sqrt{\frac{g_m}{2R_n\beta} + \frac{(\omega C_i)^2}{2g_m R_n} - \frac{\omega^2 C_i \tau_n}{R_n} \left(1 - \frac{1}{2g_m R_n} \right)} \quad (31)$$

$$B_{s,opt} = -\frac{\omega C_i}{2R_n g_m} - \frac{\omega \tau_n}{2R_n} \quad (32)$$

and F_{min} can be written as,

$$F_{min} = 1 + 2R_n \left[G_{s,opt} + \frac{Re(S_{i_n v_n^*})}{S_{v_n}} \right] \quad (33)$$

which gives,

$$F_{min} \simeq 1 + \frac{1}{\beta} + \sqrt{\frac{2g_m R_n}{\beta} + \left(\frac{2R_n(\omega C_i)^2}{g_m} - \omega^2 C_i \tau_n R_n \right) \left(1 - \frac{1}{2g_m R_n} \right)} \quad (34)$$

Equations (31)-(34) are the first reported complete set of analytical equations representing the fundamental noise parameters in terms of fundamental device parameters

including the noise transit time model, that allows us to better understand the need of the transit time based noise model at high frequencies while neglecting it at lower frequencies. As can be seen from this equation, at lower frequencies, the term containing the transit time factor ($\omega^2 C_i \tau_n R_n$) is very small and negligible compared to the other terms. Hence at lower frequencies, we do not see any effects of the correlation term τ_n . However, as the frequency increases, the term becomes larger in value and starts affecting (actually lowering) the F_{min} . This is the reason why the SPICE noise model works well at low frequencies while overestimating the NF_{min} at higher frequencies and the transit time noise model is required to correctly model the noise.

2.4 Device Technology and Experiment

This simple transit time based noise model is applied here to *npn* and *pnp* SiGe HBT transistors of a Complementary SiGe BiCMOS process and is used to explore the inherent differences in the noise parameter values and modeling for the *npn* and *pnp* SiGe transistors. These modeling results are also compared with the standard SPICE noise modeling approach [25] to demonstrate its usefulness. The process involves a dual depositions of SiGe epitaxy (boron doped for the *npn* and arsenic doped for the *pnp*), shallow and deep trench isolations, and polysilicon emitter contacts with thin, interfacial oxide layers [14]. The schematic of the cross-section is shown in Figure 4. The *npn* and the *pnp* SiGe HBTs along with Si-CMOS transistors, were integrated on SOI material for improved isolation. Due to the need of achieving comparable current gains between the *npn* and *pnp* transistors, a controlled emitter interfacial oxide layer (between the single crystal Si emitter and the heavily doped polysilicon contact) was used to independently adjust the current gain of the *npn* and *pnp* transistors. For the standard C-SiGe process, the *npn* and *pnp* transistors have a peak f_T of about 20 GHz, a BV_{CEO} of 7.0 V/6.0 V, and an Early voltage of 150 V/100 V, respectively. The *dc* characteristics were measured on-wafer using an HP 4155C Semiconductor

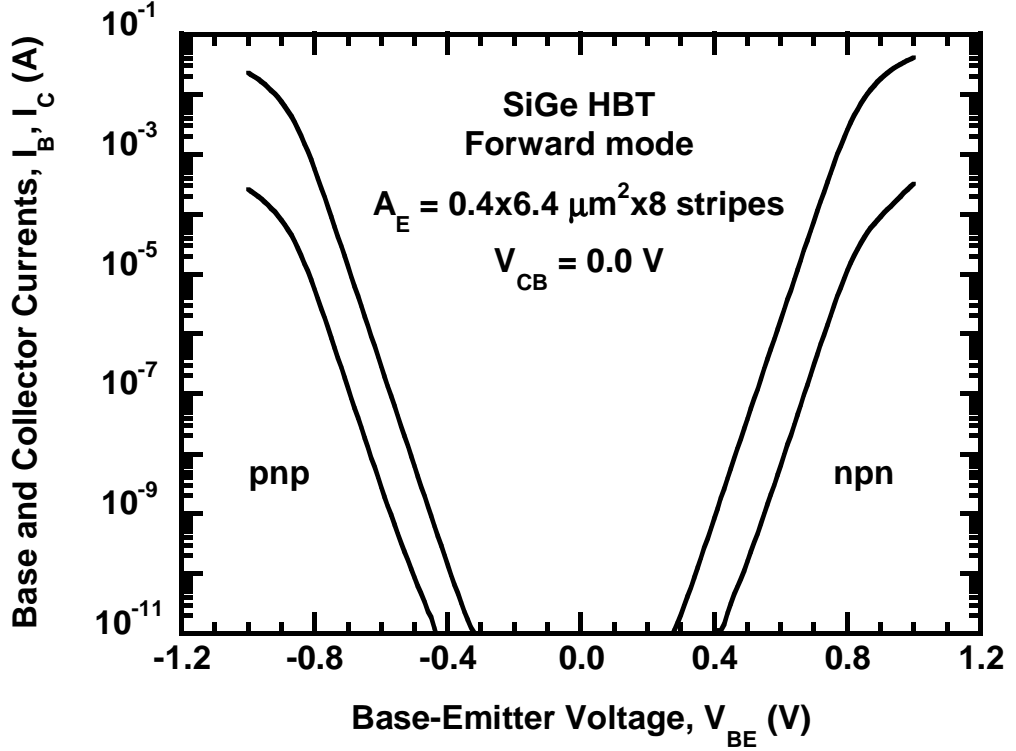


Figure 5: Gummel characteristics for the complementary SiGe HBTs ($A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$ and $V_{CB} = 0.0\text{V}$).

peak- f_T for the *npn* and *pnp* transistors are well-matched and about 22 GHz, while the peak- f_{max} is about 45 GHz for *npn* and about 40 GHz for the *pnp* transistor, for $|V_{CE}| = 3.0\text{V}$.

2.5 Modeling Results

The measured and modeled NF_{min} and R_n for the transistors are shown in Figures 9 and 10, and are compared with the SPICE-based noise model. The minimum NF_{min} of the *npn* SiGe HBT is about 1.0 dB, with a slightly higher value of 1.4 dB for the *pnp* SiGe HBT, both at a frequency of 2 GHz. This difference is mainly because the *npn* device having a higher β than the *pnp* device (Figure 6). Both the SPICE and transit time noise models match very well with the measured *npn* data at low frequencies. At higher frequencies, however, the SPICE model overestimates the noise

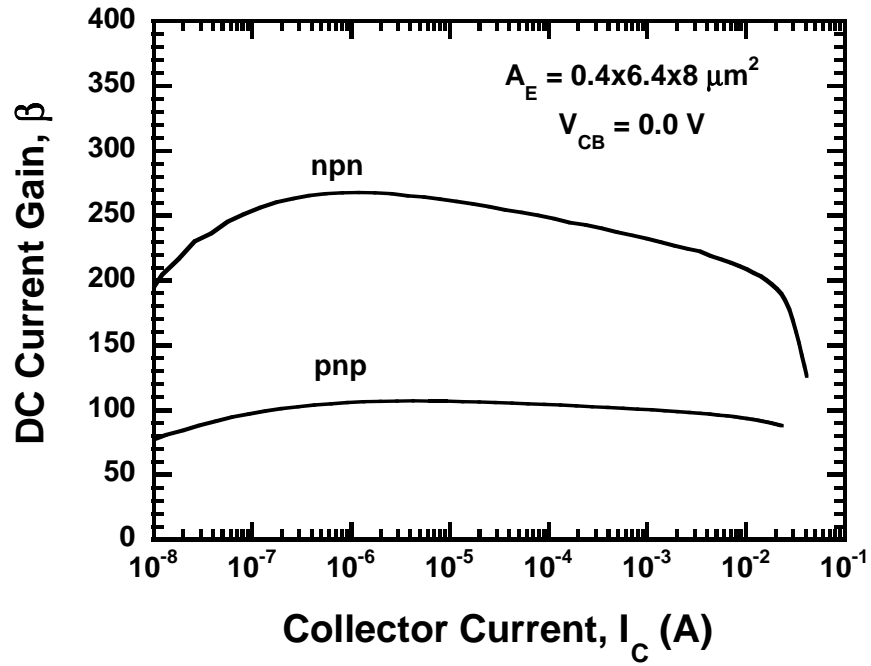


Figure 6: *dc* Current Gain as a function of collector current for the *npn* and *pnp* SiGe HBTs ($A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

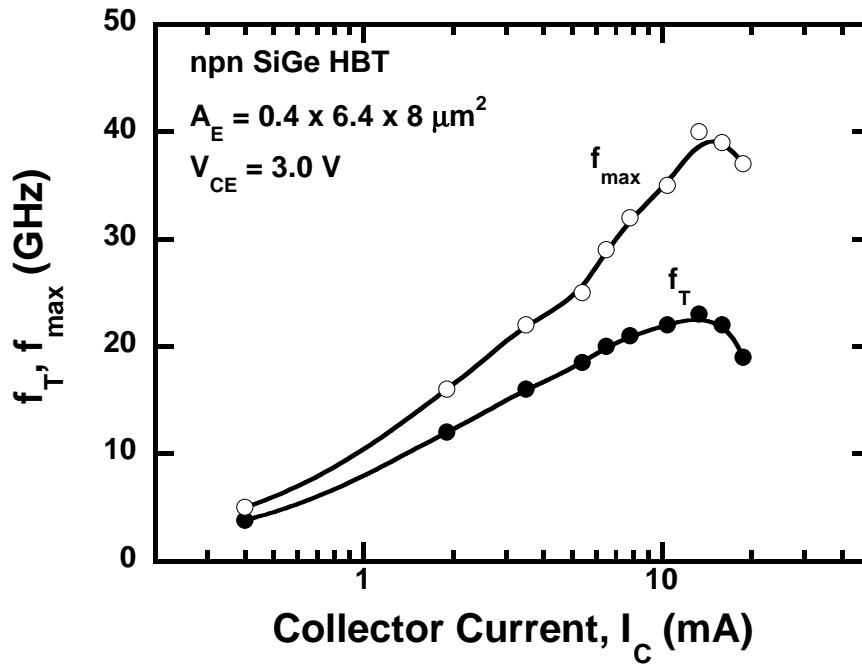


Figure 7: Cutoff Frequency f_T and the f_{max} as a function of frequency for the *npn* SiGe HBTs ($A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

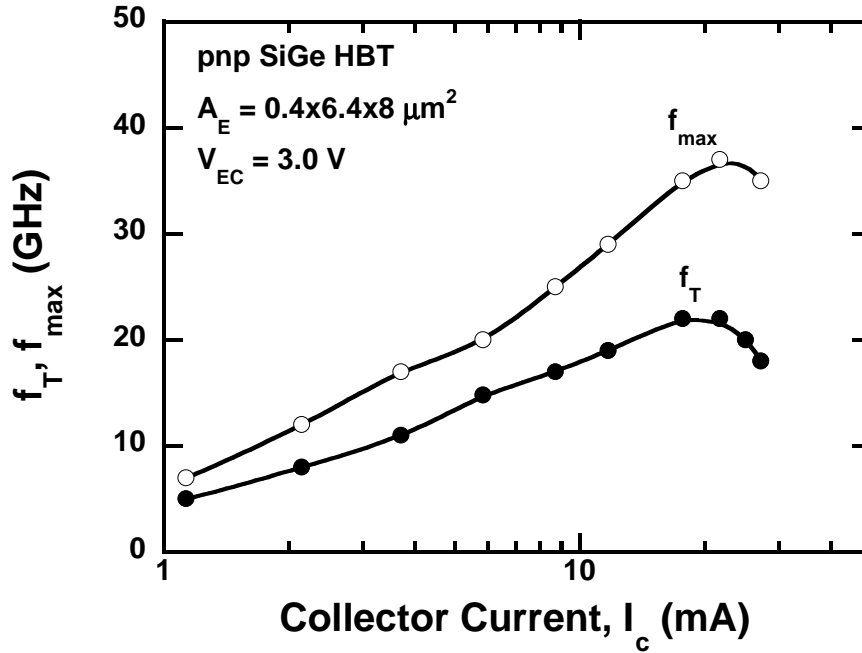


Figure 8: Cutoff Frequency f_T and the f_{max} as a function of frequency for the *pn*p SiGe HBTs ($A_E = 0.4 \times 6.4 \times 8 \mu m^2$).

figure, whereas the transit time model gives very good agreement. This difference in data-to-model match at high frequencies is the result of the increasing importance of the cross-correlation between i_b and i_c at increasing frequency, which is neglected in the SPICE noise model. In the case of the *pn*p SiGe HBT, however, the SPICE model leads to a reasonably good match with the measured data and does not differ significantly from results obtained for the transit time model. This is because of the lower β of the *pn*p's as compared to the *npn*'s as expected from equation (34). The earlier terms in equation (34) which are directly proportional to $1/\beta$ dominate in the case of the *pn*p transistors and hence gives reasonable match with the SPICE noise model. In this case, the noise transit time (τ_n) was estimated to be around 1.5 psec for the *npn* SiGe HBT and about 0.5 psec for the *pn*p SiGe HBT, using a best fit for the minimum noise figure versus frequency curve. The noise resistance of both the *npn* and *pn*p devices are modeled in the same manner for both the SPICE and transit time models, and both give good agreement with the measured data. We see that the

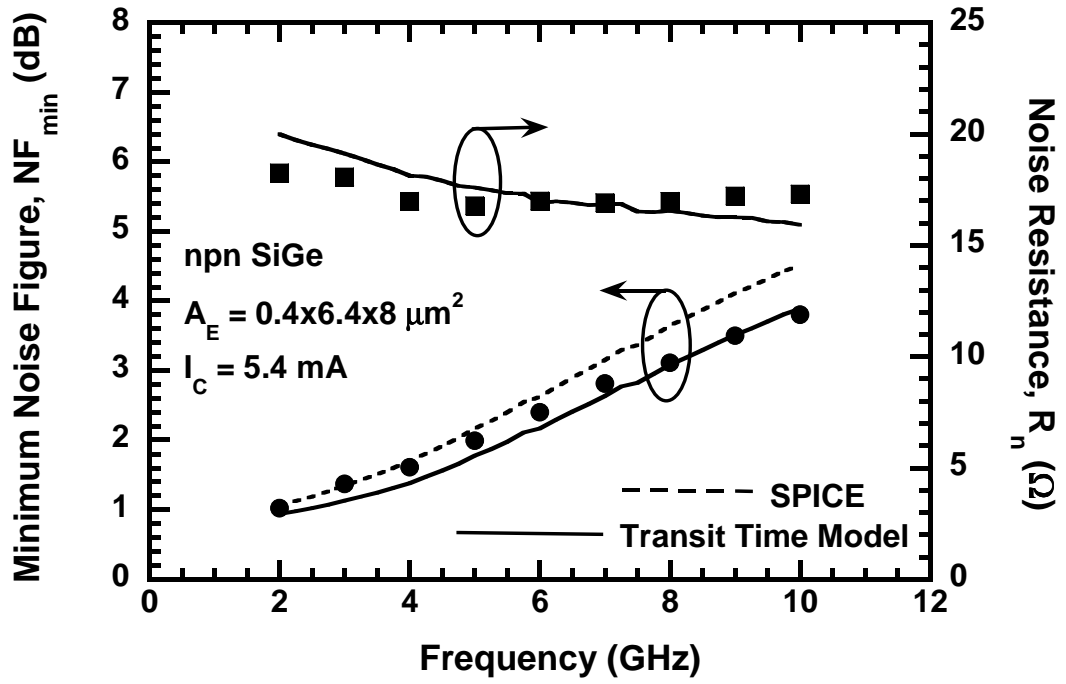


Figure 9: Measured and modeled NF_{min} and R_n as a function of frequency for an *nnp* SiGe HBT ($I_C = 5.4\text{mA}$ and $A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

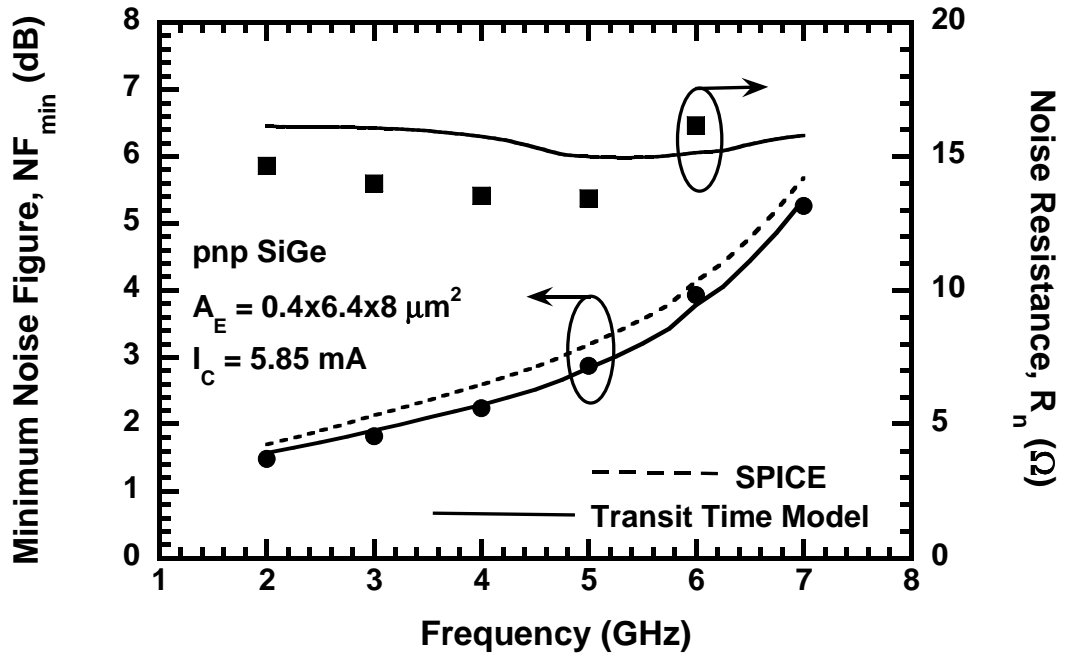


Figure 10: Measured and modeled NF_{min} and R_n as a function of frequency, for a *pnp* SiGe HBT ($I_C = 5.84\text{mA}$ and $A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

R_n in either case is quite low for this C-SiGe technology, indicating low sensitivity to source impedance matching for low-noise circuit design, obviously a benefit in analog IC design. Due to the combined effect of lower R_n and lower β , at a given collector current density and frequency, the NF_{min} of the pnp transistors are higher and less sensitive to the correlation term τ_n . This not only leads to the higher noise figure NF_{min} of the pnp transistors, but also reduces the importance of the correlation term ($\overline{i_b^* i_c}$) between the base and collector shot noise. We should expect to see the correlation term coming into play for the pnp HBTs for a higher frequency (through the term $\omega^2 C_i \tau_n R_n$ of equation (34)) than it does for the nnp and presumably not in the measured frequency range.

The magnitude and angle of $\Gamma_{s,opt}$ as a function of frequency for the nnp and pnp transistors are shown in Figures 11, 12. The angle of Γ for the both the transistors show a steady increase with frequency. For the pnp transistor, however, we observe a numerical jump. The sudden change observed in Figure 12 is only a “numerical” shift and not a physical shift. This is because the angle of Γ is defined in the range $(-180^\circ, 180^\circ]$ and since for the pnp it increases from 45° to about 170° and starts going beyond the 180° range, it goes through a numerical phase shift by 360° so that it stays in the defined range. Modeling of pnp transistors beyond the 8 GHz frequency becomes very difficult as the associated gain of the transistor goes below zero and we start getting very close to the f_T of the devices. The associated gain as a function of frequency are shown in Figures 13 and 14 for the nnp and the pnp SiGe HBT, respectively. The nnp SiGe HBT has a slightly higher gain compared to the pnp SiGe HBT. The variation of NF_{min} with collector current for both the nnp and pnp SiGe HBTs are shown in Figures 15 and 16. Minimum NF_{min} is reached at about 5.5 mA for the nnp and at about 6.5 mA for the pnp . Figures 17 and 18 show the collector current dependence of R_n at 5 GHz. Excellent agreement is observed between the modeled and the measured R_n for both the nnp and pnp SiGe HBTs.

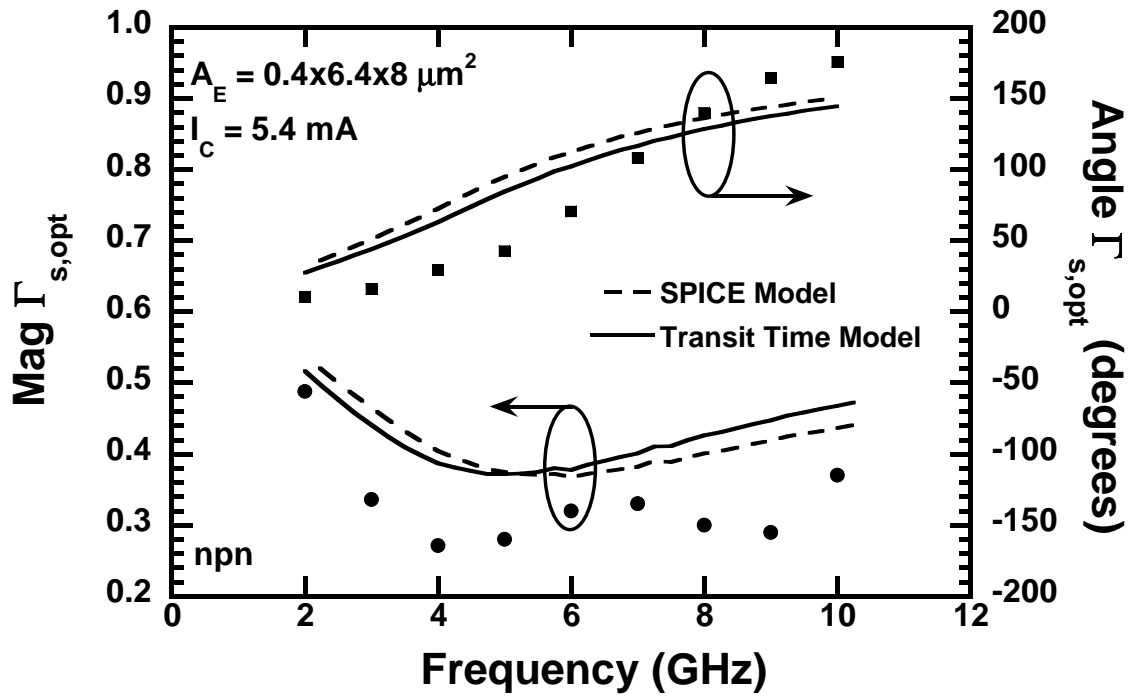


Figure 11: Comparison of modeled and measured $\Gamma_{s,opt}$ of an *npn* SiGe HBT as a function of frequency ($I_C = 5.4 \text{ mA}$ and $A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

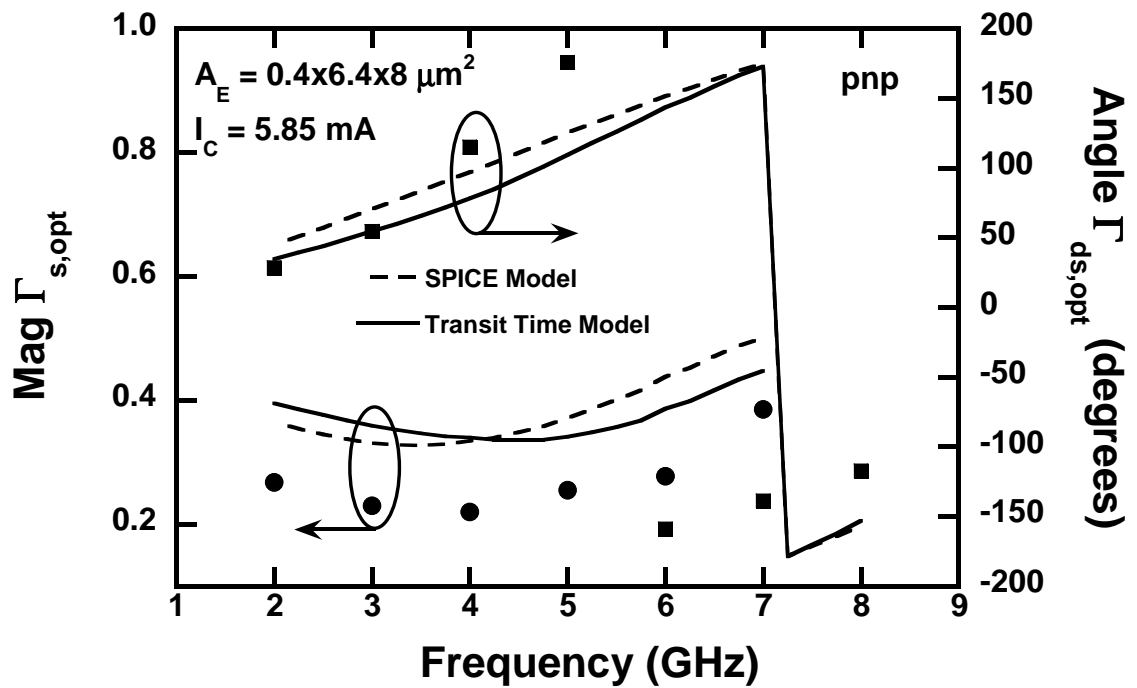


Figure 12: Comparison of modeled and measured $\Gamma_{s,opt}$ of a *pnp* SiGe HBT as a function of frequency ($I_C = 5.84 \text{ mA}$ and $A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

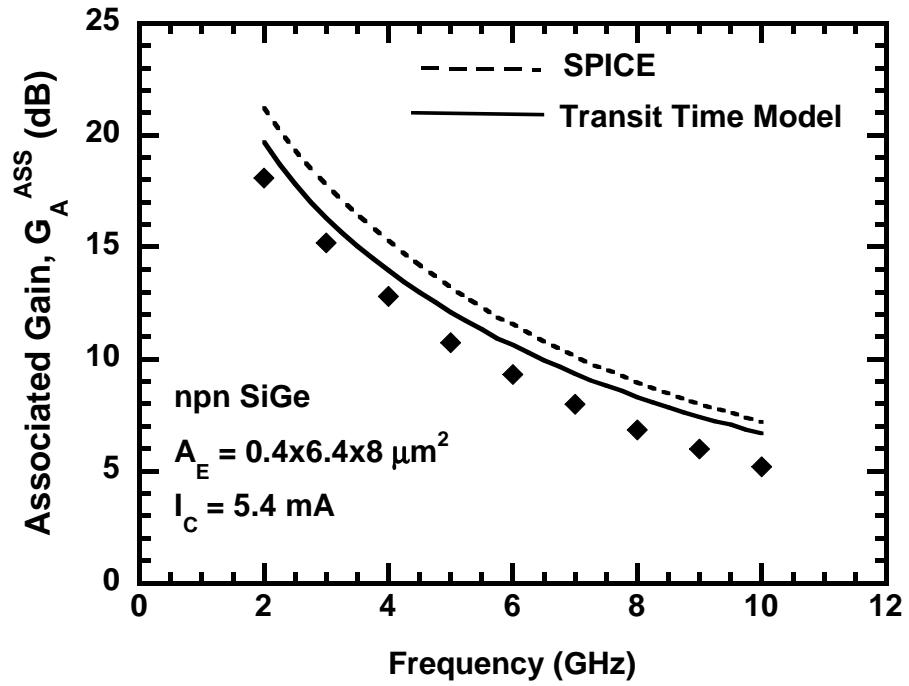


Figure 13: Associated gain G_A as a function of frequency for an npn SiGe HBT ($I_C = 5.4 \text{ mA}$ and $A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

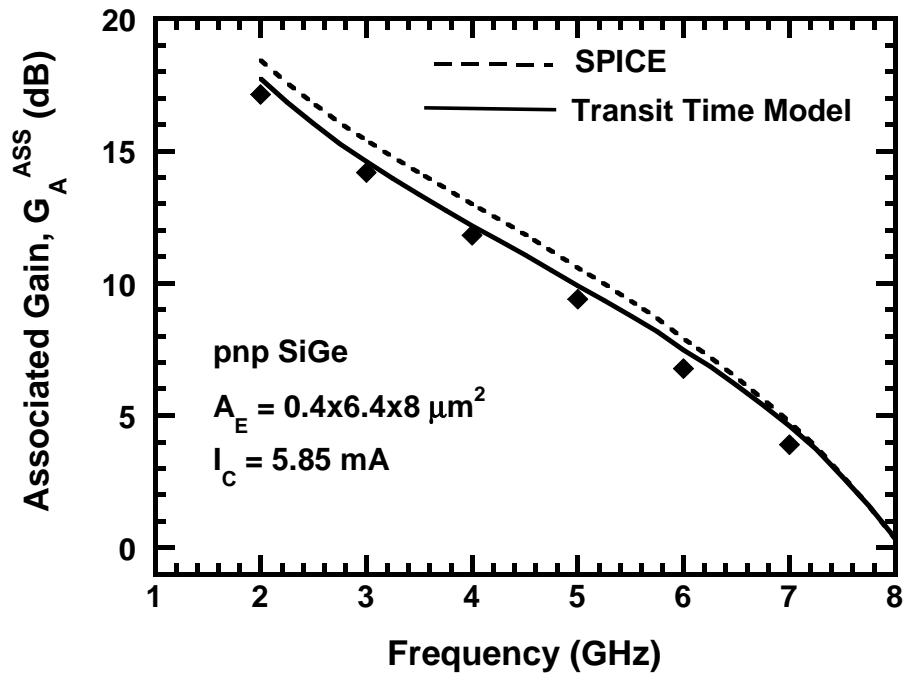


Figure 14: Associated gain G_A as a function of frequency for a pnp SiGe HBT ($I_C = 5.4 \text{ mA}$ and $A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

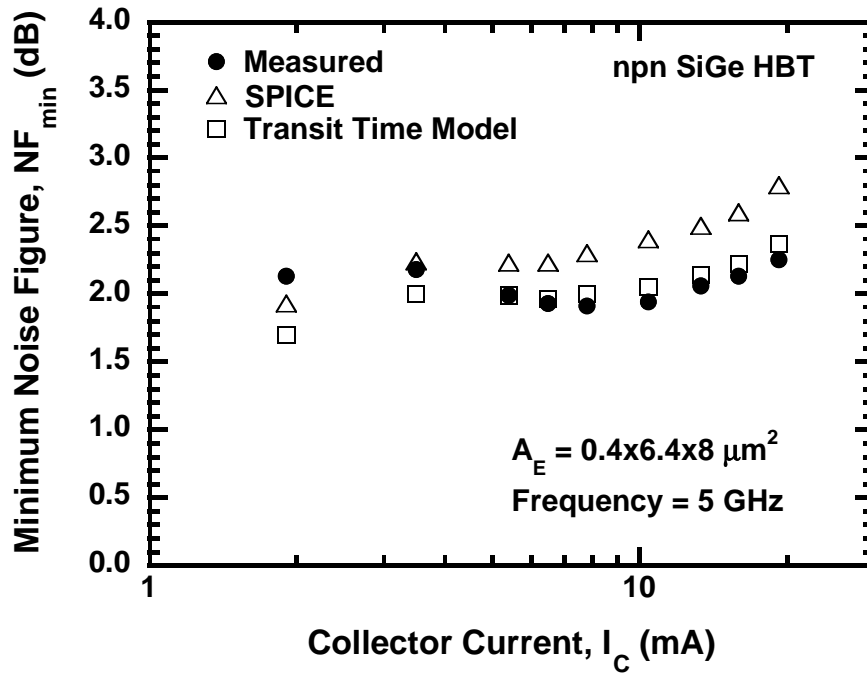


Figure 15: Comparison of modeled and measured NF_{min} versus collector current at 5 GHz for an *nnp* SiGe HBT ($A_E = 0.4 \times 6.4 \times 8 \mu m^2$).

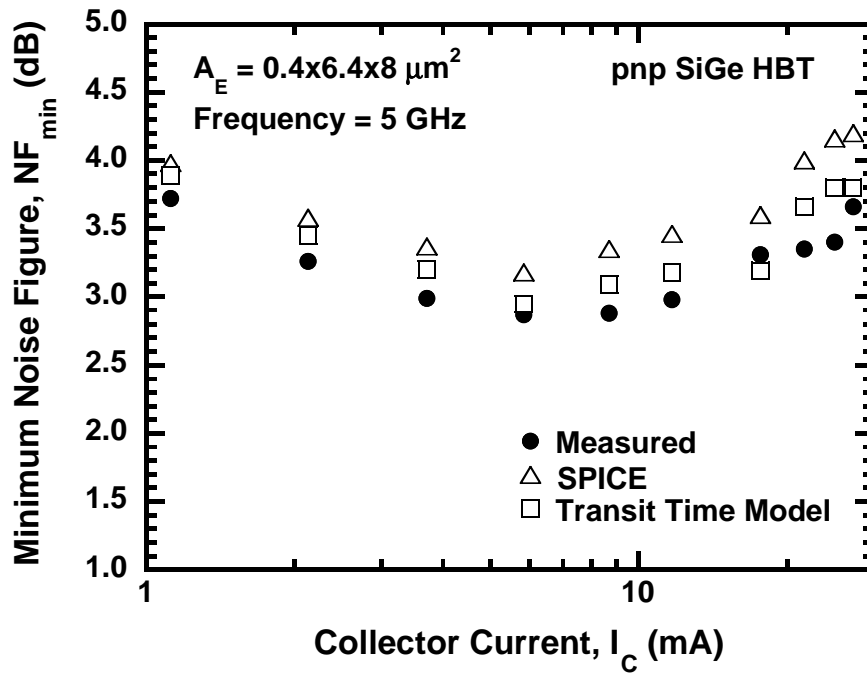


Figure 16: Comparison of modeled and measured NF_{min} versus collector current at 5 GHz for a *pnp* SiGe HBT ($A_E = 0.4 \times 6.4 \times 8 \mu m^2$).

Since in both the SPICE model and transit time model, R_n is modeled in the same manner, only the results for the latter model compared with the measured data is shown. Both the SPICE model and the base-transit time model models the Γ as a function of bias with moderate accuracy. The values of Γ , especially close to the peak f_T , becomes very sensitive to the measurement accuracy and can create errors in the modeling. Nevertheless, both the models capture the data for Γ with reasonable accuracy, with the transit time model predicting the behavior better than the SPICE model.

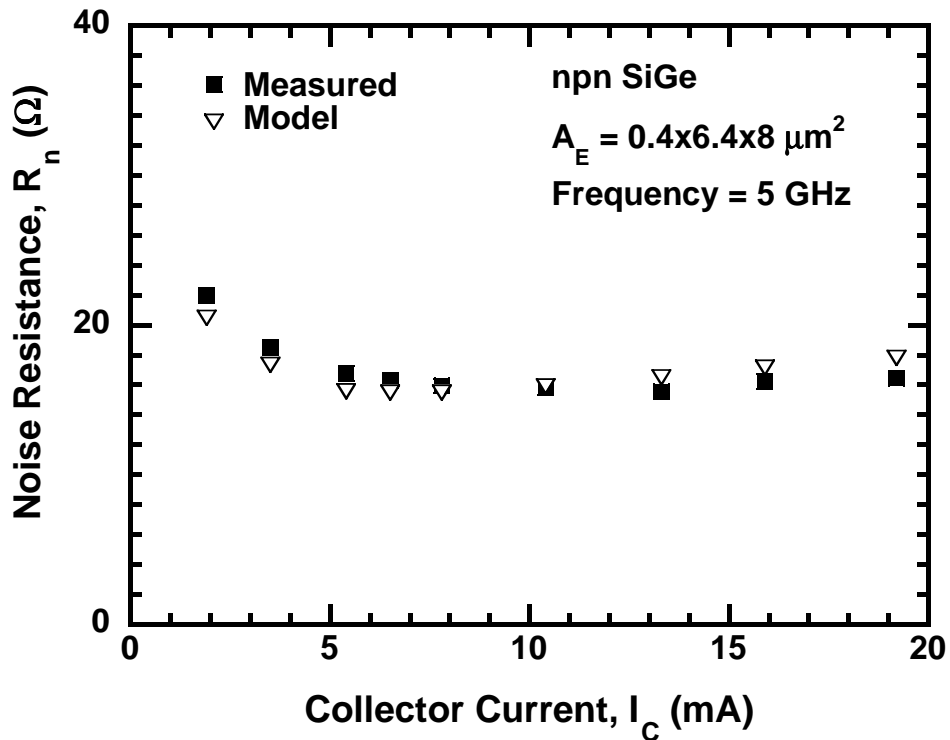


Figure 17: Comparison of modeled and measured R_n versus collector current at 5 GHz for an *nnpn* SiGe HBT ($A_E = 0.4 \times 6.4 \times 8 \mu m^2$).

Thus, a simple “transit-time” based broadband noise model, for bipolar transistors, is developed and applied to a complementary SiGe HBT technology. The four fundamental noise parameters (NF_{min} , R_n , and $\Gamma_{s,opt}$ - magnitude and angle) have been extracted using a two-port noise model of the C-SiGe HBT technology, which

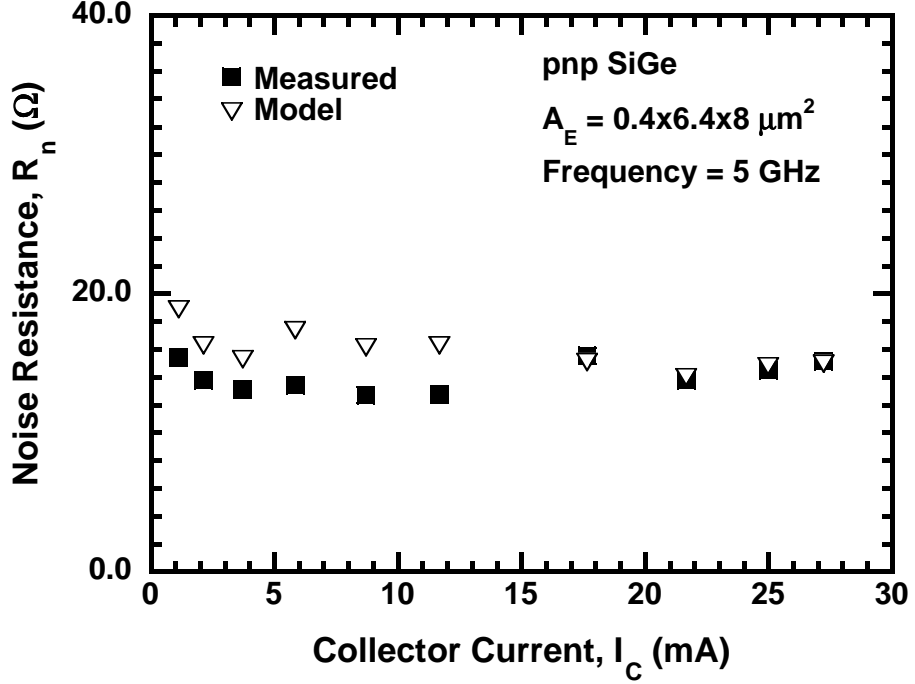


Figure 18: Comparison of modeled and measured R_n versus collector current at 5 GHz for a *pnp* SiGe HBT ($A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

links the fundamental noise current sources in an HBT to the circuit level noise. Analytical expressions for the four fundamental noise parameters are derived after including the transit time model and is used to explain the need of the transit time model at high frequencies. It is used to explore the differences in the high frequency noise behavior between the *npn* and *pnp* transistors. The noise of the HBT is modeled from its measured *dc* and scattering parameter data and is verified by direct noise measurements across bias and frequency. The validity of conventional SPICE noise model and a base-transit time based simple noise model for the *npn* and *pnp* SiGe HBTs is investigated. The SPICE model is more accurate for the *pnp* SiGe HBT than for the *npn* SiGe HBT, where it overestimates the NF_{min} at high frequencies. The base-transit time correlation term extracted for the *pnp* ($\simeq 0.5\text{ps}$) is smaller than the *npn* ($\simeq 1.5\text{ps}$) indicating lesser cross-correlation of the base and collector shot noises in case of the *pnp* transistor. Owing to the combined effect of lower β and

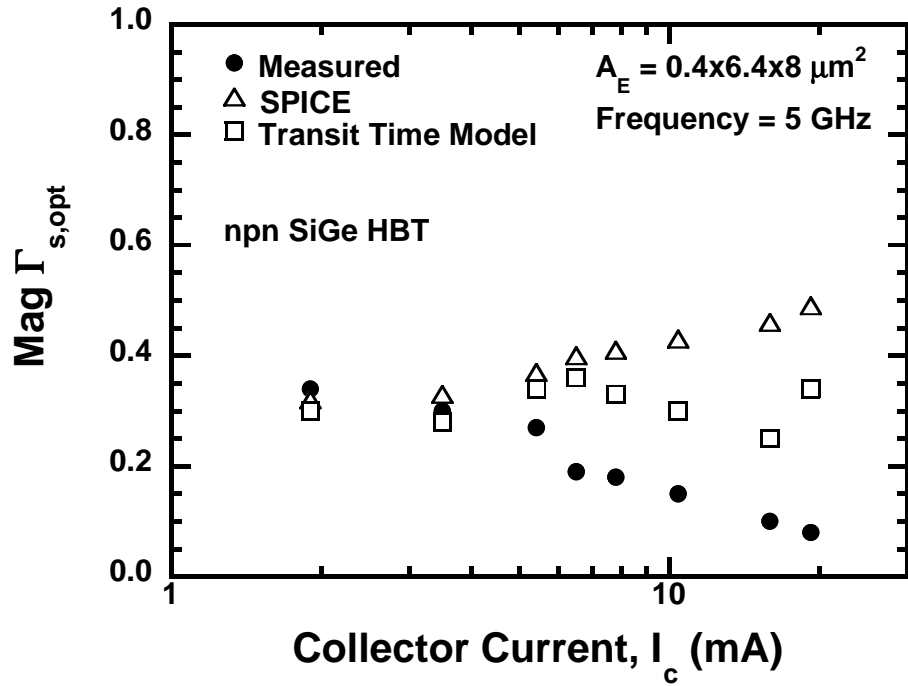


Figure 19: Comparison of modeled and measured magnitude of $\Gamma_{s,opt}$ of an *npn* SiGe HBT as a function of collector current I_C ($f = 5\text{GHz}$ and $A_E = 0.4 \times 6.4 \times 8\mu\text{m}^2$).

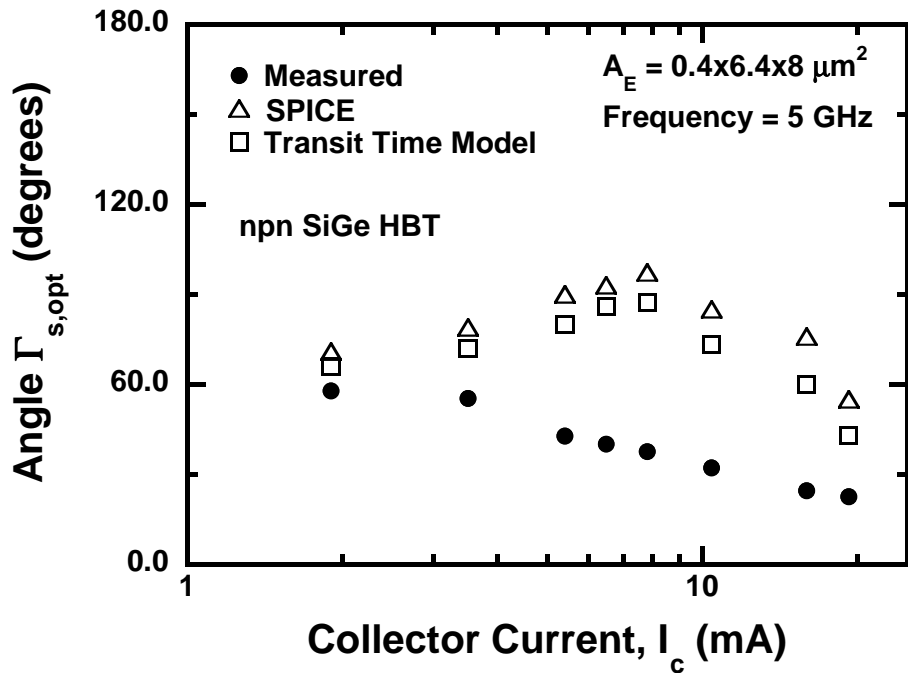


Figure 20: Comparison of modeled and measured angle of $\Gamma_{s,opt}$ of an *npn* SiGe HBT as a function of collector current I_C ($f = 5\text{GHz}$ and $A_E = 0.4 \times 6.4 \times 8\mu\text{m}^2$).

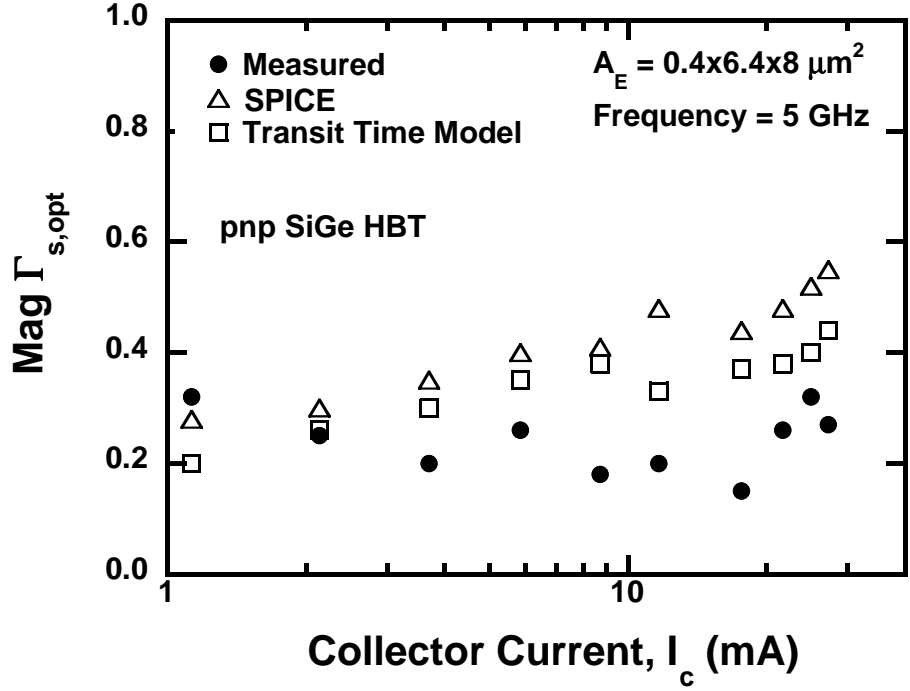


Figure 21: Comparison of modeled and measured magnitude of $\Gamma_{s,opt}$ of a *pnp* SiGe HBT as a function of collector current I_c ($f = 5\text{GHz}$ and $A_E = 0.4 \times 6.4 \times 8 \mu\text{m}^2$).

lower R_n of the *pnp* transistors, the NF_{min} becomes a weaker function of the cross correlation term of the base-transit time at the given frequencies. The transit time based simple noise model presented for the C-SiGe HBTs gives excellent agreement with the measured data for both the *nnp* and the *pnp* SiGe HBTs, and should thus prove useful for compact model implementations.

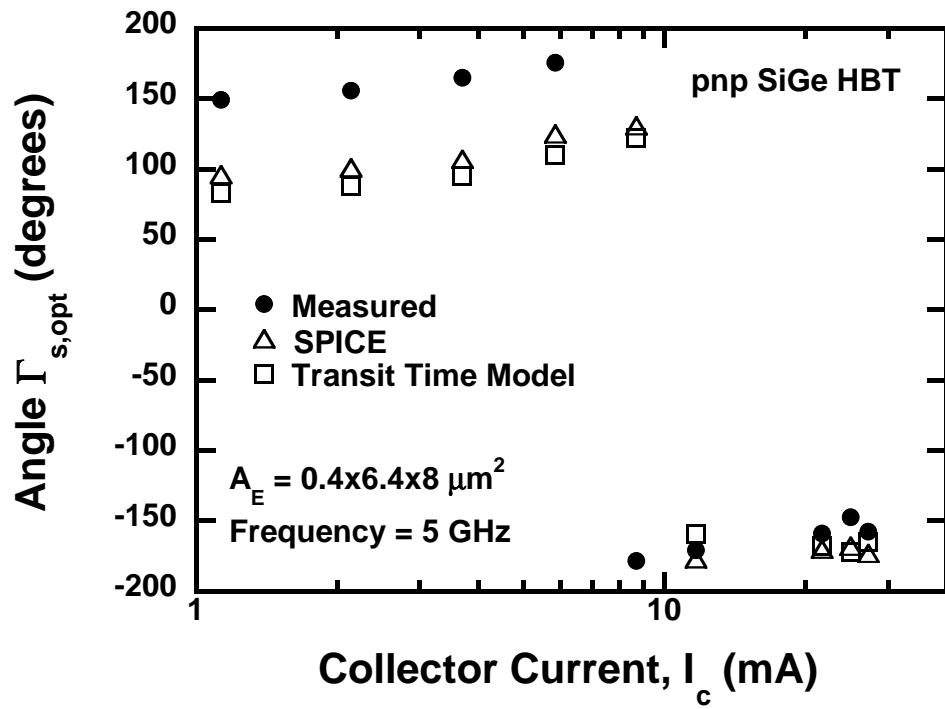


Figure 22: Comparison of modeled and measured angle of $\Gamma_{s,opt}$ of a *pnp* SiGe HBT as a function of collector current I_C ($f = 5GHz$ and $A_E = 0.4 \times 6.4 \times 8\mu\text{m}^2$).

CHAPTER III

CRYOGENIC PERFORMANCE OF SILICON GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

Cryogenic electronics represent a small but important niche market, with applications such as high-sensitivity cooled sensors and detectors, satellite systems, deep-space and planetary space missions, very high precision instrumentation and detector electronics, superconductor-semiconductor hybrid electronic systems, and very-low-noise receivers for astronomy. It is well-established that due to band-gap engineering, SiGe HBTs are naturally suited for use in the cryogenic environment (e.g., at 77K, or even down to 4.2K) [16], an operational regime traditionally forbidden to conventional silicon (Si) bipolar junction transistors (BJTs). A comprehensive investigation of the small-signal RF and broadband noise performance of a 200 GHz peak f_T SiGe HBT is presented in this chapter.

3.1 On Wafer Cryogenic Measurement Setup

Measurements were performed using a custom-designed cryogenic probing system which enables on-wafer microwave measurements across the temperature range of 18K to 350K [61]. The cryogenic probing system contains ports for RF and DC cables, temperature sensors, vacuum pumps, dry nitrogen back-fill lines, manipulators for coplanar waveguide probe and fiber optics holder, and a closed cycle refrigerator cold head. The probe body rests on a copper block attached to a fiberglass post that reduces the thermal load and is coupled to the wafer stage with flexible copper braids

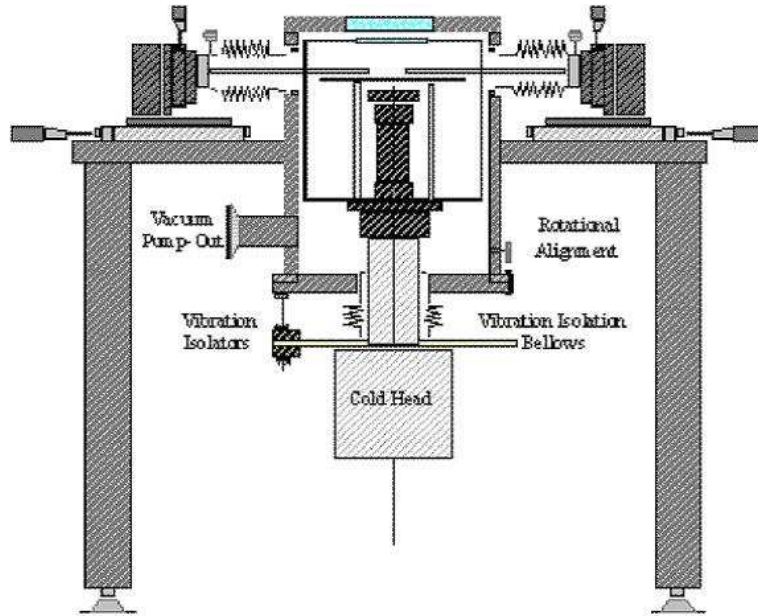


Figure 23: Schematic of the side view of cryogenic probe station.

to ensure thermal stability. Figures 23 and 24 show the schematic of the side and top view of the cryogenic system.

The cold wafer stage is also supported on fiberglass posts above the cold head and copper braiding from the cold head anchors the wafer stage to its temperature. The copper braids thermally stabilize the probes and the wafer stage to the cold head, assuring the appropriate sample temperatures. The device under test (DUT) is mounted on the cold wafer stage and the test chamber is evacuated to prevent frost build up and large thermal grading when cooling the chamber. A view port on the top permits accurate positioning of the RF probes on the sample. The most important feature of this cryogenic probe system is its closed-cycle helium refrigerator system. Previous cryogenic probe systems used open-cycle cooling to reduce start-up costs and avoid mechanical vibrations. However, for long-term stability, a closed-cycle liquid helium source provides the ideal solution. Decoupling and damping of the vibrations from the cold head to the probe station are accomplished with bellows and a vibration mount.

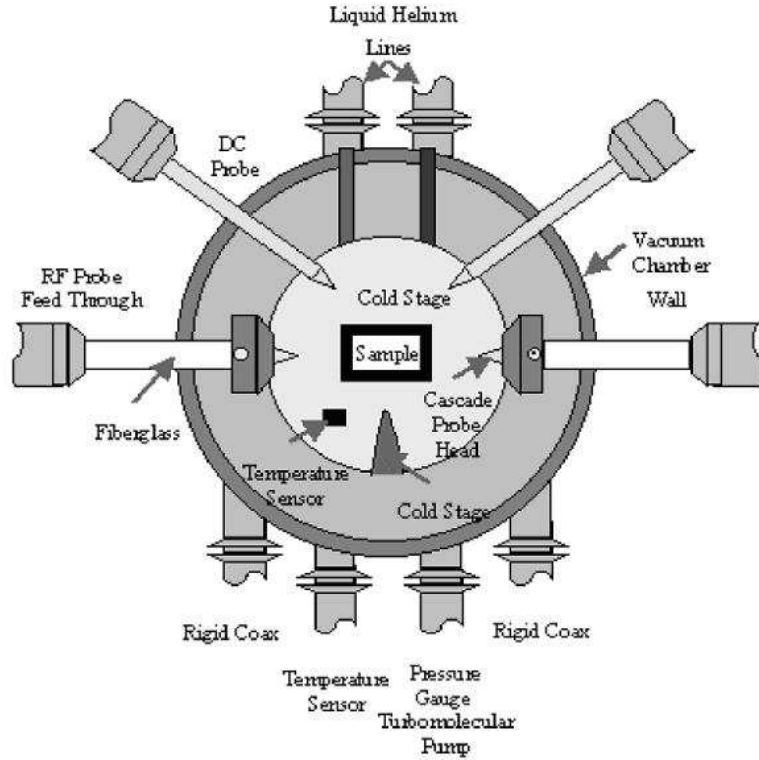


Figure 24: Schematic of the top view of the cryogenic probe station chuck.

S-parameters were measured to 26 GHz using an HP 8510C VNA. Noise parameters were measured from 2 GHz to 26 GHz using an automated ATN noise measurement system as described in the last chapter. The thermometry of the cryogenic setup was carefully verified using transistor *dc* measurements dipped in a bath of liquid-nitrogen (i.e., 77.3K). Conventional “open” structure, Y-subtraction parasitic de-embedding was used for both the S-parameter and noise parameter measurements, and system calibration was performed at each temperature to ensure accuracy across the entire temperature range.

3.2 SiGe HBTs in Cryogenic Temperatures

It has long been known that conventional Si BJTs are not suitable for operation at cryogenic temperatures because of the combined detrimental effects of: 1) the

exponential decrease in current gain with cooling due to heavy-doping induced band-gap narrowing in the emitter; 2) the increase in base resistance with cooling due to carrier freeze-out in the base; and 3) the decrease in frequency response due to the degradation of the minority carrier diffusivity in the base region with cooling [13]. Thus, for Si BJTs optimized for high-speed operation at 300K, current gain (β) degrades quasi-exponentially with cooling, the f_T and f_{max} degrade with cooling, and not surprisingly, the circuit delay (e.g., ECL) increases (degrades) with cooling, precluding their use at cryogenic temperatures.

Bandgap engineering has a very positive influence, however, on the low temperature operation of SiGe HBTs. The thermal energy (kT), *in every instance*, is arranged in the SiGe HBT equations such that it favorably affects the low-temperature performance metric in question. For a SiGe HBT optimized for 300K operation, when compared to similarly constructed Si BJT, $\beta(T)$ should increase exponentially with decreasing temperature, since

$$\left. \frac{\beta_{SiGe}}{\beta_{Si}} \right|_{V_{BE}} \simeq \left\{ \frac{\tilde{\gamma}\tilde{\eta}\Delta E_{g,Ge}(grade)/kT e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\} \quad (35)$$

where

$$\tilde{\eta} = \frac{(D_{nb})_{SiGe}}{(D_{nb})_{Si}} \quad (36)$$

is the ratio of the minority electron diffusivity between SiGe and Si, and

$$\tilde{\gamma} = \frac{(N_C N_V)_{SiGe}}{(N_C N_V)_{Si}} \quad (37)$$

is the “effective density-of-states ratio” between SiGe and Si. The Ge-induced reduction in the base bandgap occurring at the emitter-base edge of the quasi-neutral base is $\Delta E_{g,Ge}(x=0)$ and

$$\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0) \quad (38)$$

where W_b is the neutral base width. This indicates that one should expect a quasi-exponential increase in the SiGe-to-Si current gain ratio with decreasing temperature.

In addition, $V_A(T)$ should also increase exponentially with decreasing temperature when compared to Si BJT, since

$$\left. \frac{V_{A,SiGe}}{V_{A,Si}} \right|_{V_{BE}} \simeq e^{\Delta E_{g,Ge}(grade)/kT} \left[\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right] \quad (39)$$

Frequency response of SiGe HBTs should also improve with decreasing temperature, as can be seen from,

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} [1 - e^{-\Delta E_{g,Ge}(grade)/kT}] \right\} \quad (40)$$

and,

$$\frac{\tau_{e,SiGe}}{\tau_{e,Si}} \simeq \frac{J_{C,Si}}{J_{C,SiGe}} = \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\tilde{\gamma}\tilde{\eta} \frac{\Delta E_{g,Ge}(grade)}{kT} e^{\Delta E_{g,Ge}(0)/kT}} \quad (41)$$

both of which are favorably influenced by cooling. We assume here that the influence of the graded SiGe profile is also sufficient to overcome the inherent electron diffusivity degradation on τ_b with cooling.

Hence, it is expected that SiGe HBTs, even without optimization for cryogenic operation, to naturally have improved performance with cooling, provided carrier freeze-out is prevented by using an abrupt and heavily-doped (above the Mott transition) epitaxial base.

3.3 Device Technology

The SiGe HBTs used in the investigation are from a commercial 120 nm, third-generation SiGe HBT process technology which employs a new, reduced thermal cycle, “raised extrinsic base” structure, and utilizes deep and shallow trench isolation, an *in-situ* doped polysilicon emitter, a silicided extrinsic base, and a carbon-doped, graded UHV/CVD epitaxial SiGe base (Figure 25 [60]) with a minimum emitter width of 0.12 μm , a measured peak f_T of 200 GHz and peak f_{max} of 285 GHz at room temperature (300K). It was not optimized for cryogenic operation in any way.

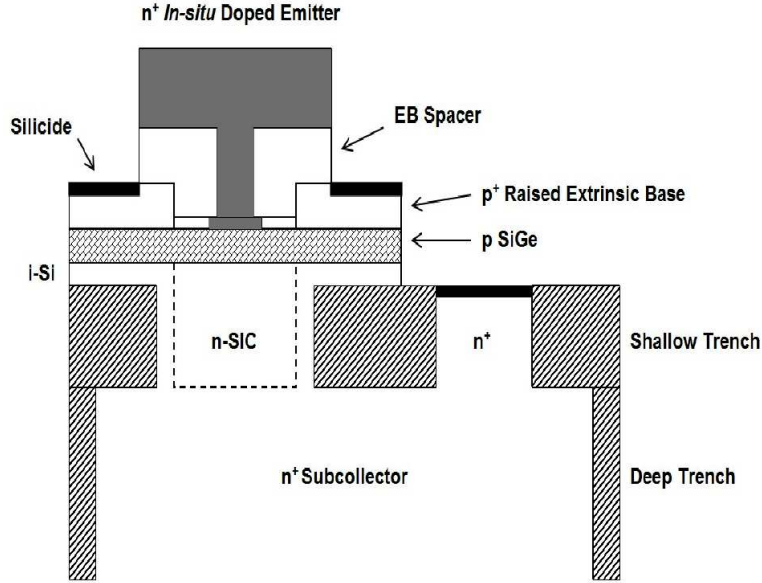


Figure 25: Schematic device cross-section of raised extrinsic base SiGe HBT.

3.4 Measurement Results and Discussion

3.4.1 DC Performance

Current-voltage measurements across the 300K to 85K temperature range were made on SiGe HBTs with an emitter area of $0.12 \times 10.0 \mu\text{m}^2$ [56]. The forward-gummel characteristics at 300K and 85K are shown in Figure 26, for $V_{CB} = 0$ V. In spite of the high peak base and emitter doping levels associated with these aggressively-scaled SiGe HBTs ($> 10^{19} \text{cm}^{-3}$), the base current remains reasonably ideal at 85K. This is the result of the lightly doped epitaxial spacer layer inserted between the base and emitter regions, and helps limit field-assisted tunneling and recombination at low temperatures. The base-emitter turn-on voltage increases with cooling, as expected, due to the exponential decrease of the intrinsic carrier concentration with cooling. The base and emitter regions in this device are both doped well above the Mott-transition, and ensure that carrier freeze-out does not negatively impact the base or emitter resistance below 100K. As can be seen in Figure 26 at 85K, this device is capable of very high current density operation ($> 25 \text{mA}/\mu\text{m}^2$), and thus the high

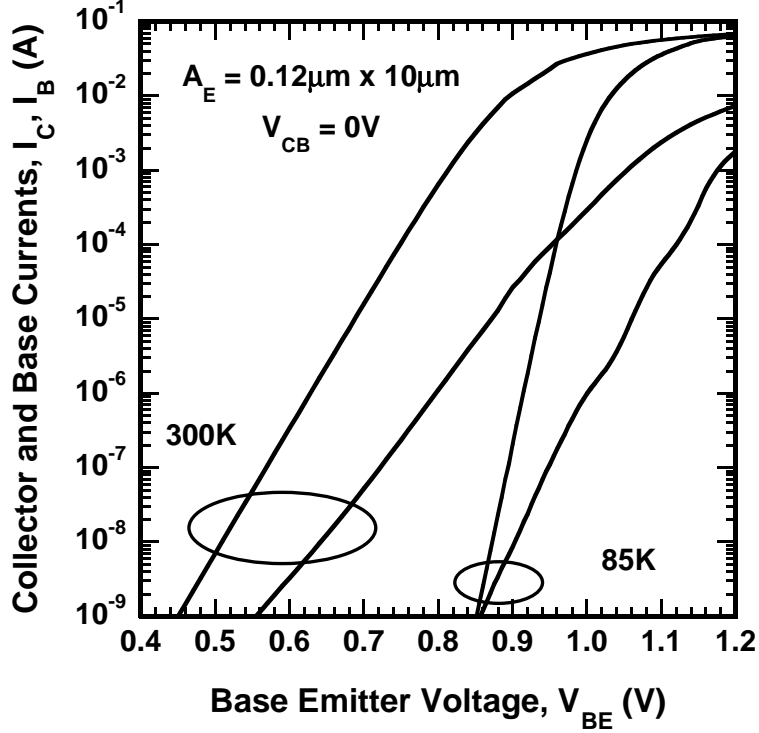


Figure 26: Forward Gummel Characteristics at 300K and 85K for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

collector doping level effectively limits the impact of heterojunction barrier effects at low temperatures, which can be a key design issue for the cryogenic operation of SiGe HBTs [16]. It can be noted that the slope of the collector current (g_m) increases with the base-emitter voltage as we decrease the temperature from 300K to 85K. For low injection, we can write

$$g_m = \frac{\partial I_C}{\partial V_{BE}} \simeq \frac{q I_C}{kT} \propto \frac{q}{kT} e^{qV_{BE}/kT} \quad (42)$$

Figure 27 shows the collector current as a function of the base-emitter voltage for various temperatures illustrating the change in the transconductance with temperature. Figure 28 shows the base-current as a function of the base-emitter voltage for various temperatures.

It is interesting to note that the the non-ideal base current increases dramatically at 85K compared to the collector current. This is because, at a given V_{BE} ,

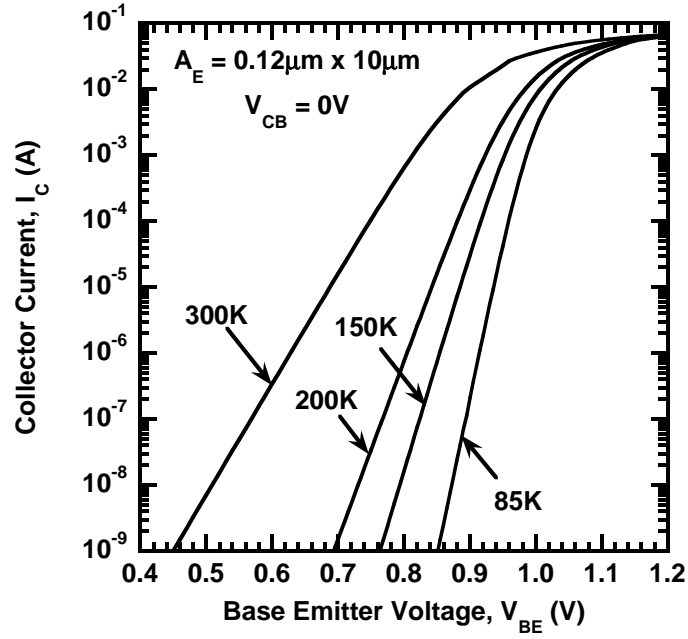


Figure 27: Collector Current as a function of base emitter voltage at various temperatures for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

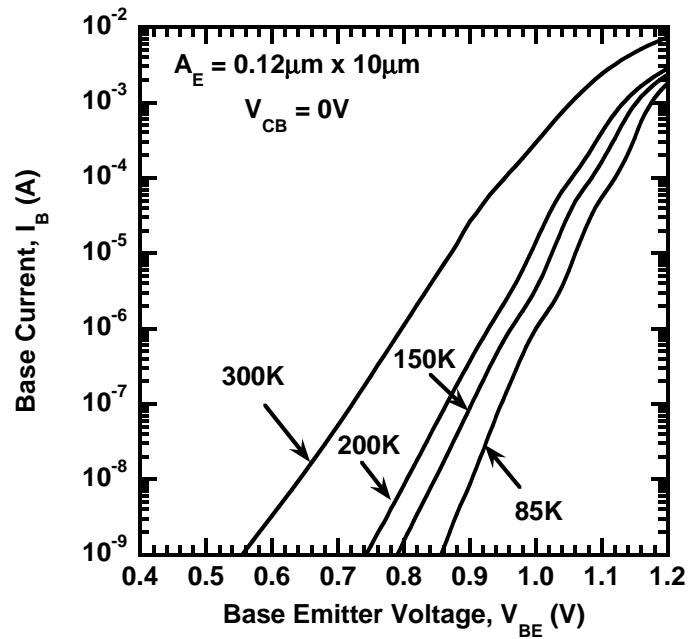


Figure 28: Base Current as a function of base emitter voltage at various temperatures for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

both the base and collector currents decrease strongly going from 300K to 85K. The leakage current in the base, induced by the tunneling and field-assisted recombination processes associated with the high electric field in the emitter-base junction, though, remains largely constant. This parasitic base leakage current increases the non-ideal base current as we go down from 300K to 85K.

Shown in Figure 29 are typical output characteristics of the SiGe HBTs at 300K and 85K. The output characteristics remain reasonably ideal at 85K with the breakdown voltage (BV_{CEO}) reducing from about 1.8V at 300K to about 1.6V at 85K.

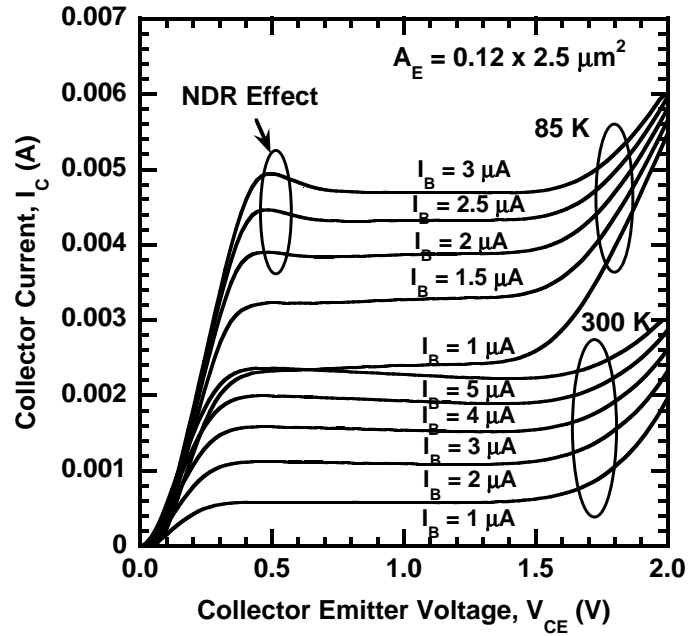


Figure 29: Common-emitter output characteristics at 300K and 85K for a $0.12 \times 0.25 \mu\text{m}^2$ SiGe HBT.

A “negative-differential-resistance” (NDR) effect is observed in the forced- I_B output characteristics which causes the overshoot like characteristics in the collector current at 85 K. A “hysteresis” in the voltage sweep direction of the $I - V$ characteristics appears in the NDR region at cryogenic temperatures. We observe (Figure 29), at 85K, that in the quasi-saturation region I_C decreases as V_{CE} increases thus

exhibiting NDR. The effect of the NDR is also observed in the forward-gummel (Figure 26) as we observe “dips” in the I_B curve (decreasing and then increasing I_B) as can be seen in Figure 28. These dips start showing up in a much pronounced way as we reach temperatures 150K and lower.

The current gain increases monotonically with cooling, from 600 at 300K, to 3800 at 85K as shown in Figure 30.

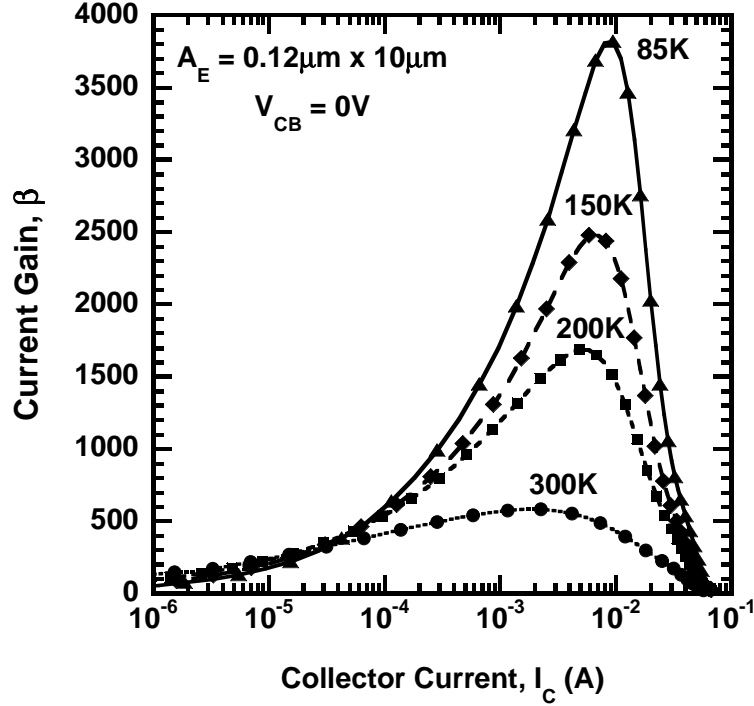


Figure 30: Current gain as a function of bias current and temperature for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

Two mechanisms are responsible for this improvement with cooling: 1) the (sizeable) Ge-induced band offset in this device (exponentially) increases the current gain with cooling (35), and 2) the heavily doped base region partially offsets the doping-induced bandgap narrowing associated with the emitter region. The strong decrease in the current gain above its peak value at 85K is associated with the “Ge-grading” effect [63], but the current gain remains above 2000 at 85K at the current density at which peak f_T is reached, effectively minimizing any emitter charge storage at low

temperatures. Figure 31 shows normalized peak β as a function of reciprocal temperature ($1000/T$) illustrating the increase in peak β with the decrease in temperature (about $7\times$ from 300K to 85K).

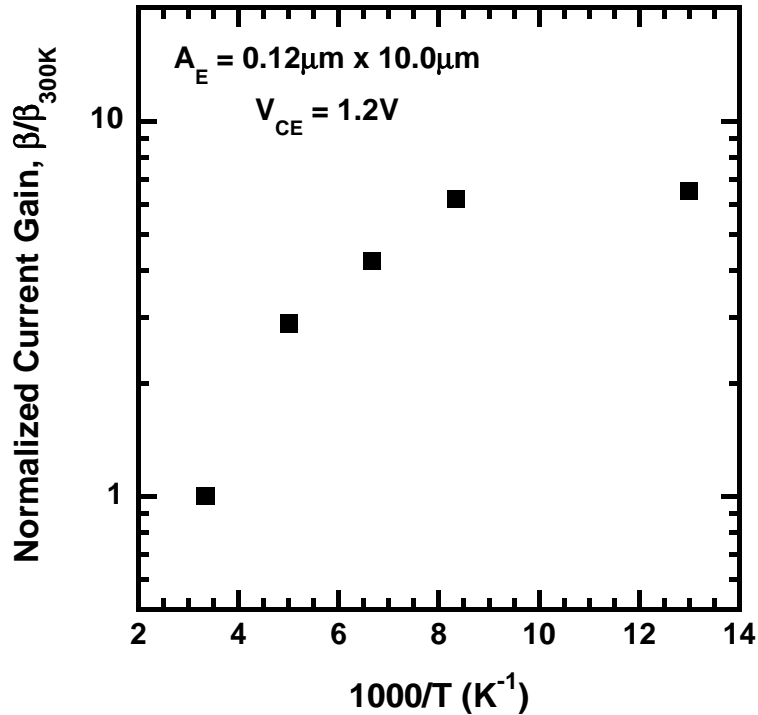


Figure 31: Normalized Peak Current gain as a function of reciprocal temperature $1000/T$ for a $0.12 \times 10.0 \mu m^2$ SiGe HBT.

Avalanche multiplication effects are also studied at 300K and 85K to ascertain the low temperature operation of this aggressively scaled SiGe HBTs. The $M - 1$ is calculated from $I-V$ measurements using,

$$M - 1 = \frac{\Delta I_B}{I_C - \Delta I_B} \quad (43)$$

Figure 32 shows the measured multiplication factor ($M - 1$) versus collector-base voltage (V_{CB}) at 85K and 300K. Since the collector current decreases strongly with V_{BE} as we go from 300K to 85K, to obtain similar I_C at 300K and 85K, the V_{BE} was increased from 0.65V at 300K to 0.93V at 85K. Only a weak increase with cooling is observed, as expected from previously reported work [64]. This modest temperature

dependence of $M - 1$ with cooling alleviates the power supply limit posed by the base current reversal voltage and indicates the suitability for these aggressively scaled SiGe HBTs for low-temperature digital applications requiring higher V_{CB} .

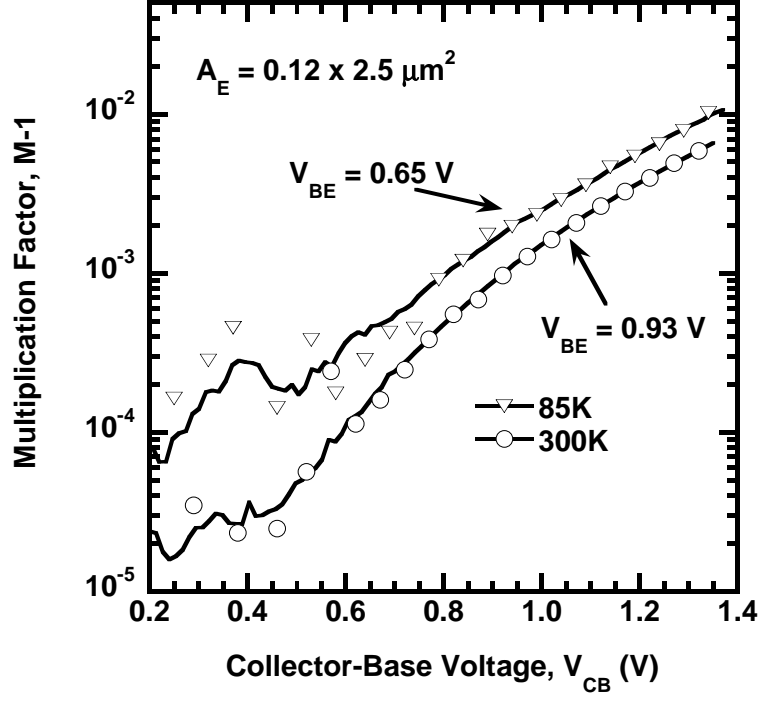


Figure 32: Multiplication Factor versus collector-base bias at 300K and 85K for a $0.12 \times 0.25 \mu\text{m}^2$ SiGe HBT.

3.4.2 Small-Signal Performance

On-wafer S-parameter measurements were performed at various temperatures. Figure 33 shows the measured small-signal gain on frequency at peak f_T for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT at 300K and 85K ($V_{CE} = 1.2\text{V}$). A near -20 dB/decade slope is obtained across a wide frequency range for all temperatures. Figure 34 shows the extracted cutoff frequency versus bias current data at 300K, 200K, 150K, 120K and 85K for the $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT. An increase in peak f_T from 200 GHz at 300K to 260 GHz at 85K is observed.

This increase in the peak f_T with cooling is proportionately smaller than has been

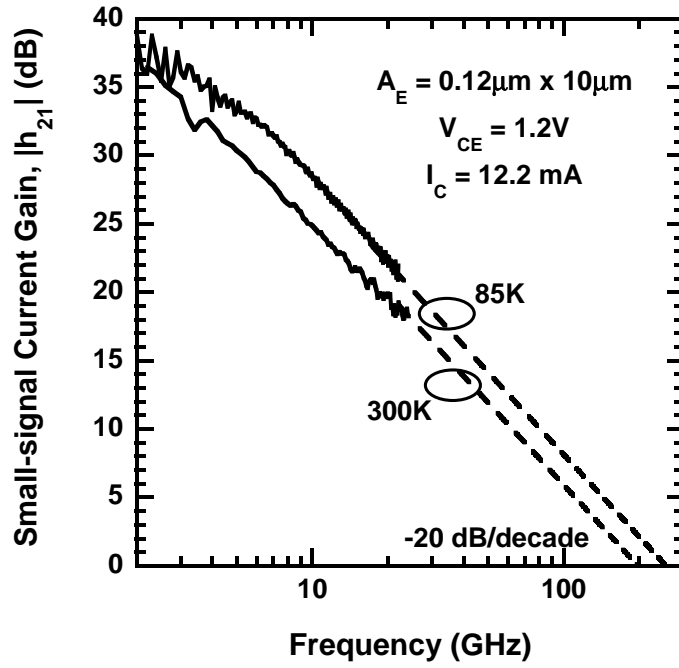


Figure 33: Small-signal gain as a function of frequency at 300K and 85K for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT. Lines are drawn at 20 dB/decade.

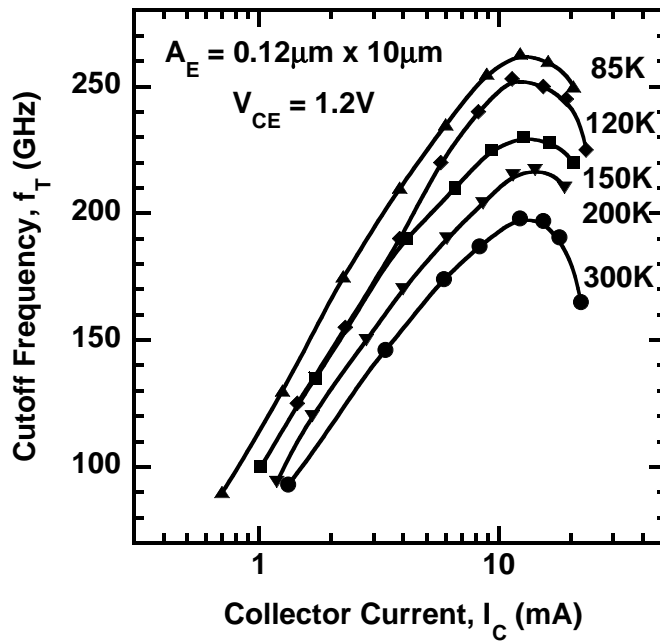


Figure 34: Extracted cutoff frequency as a function of bias current for various temperatures for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

reported in first-generation SiGe HBTs operated at 85K [65]. This is because in the present case, the base and emitter transit times in this 200 GHz device, which are favorably affected by both the Ge-grading and cooling, are already small compared to the collector delay time, and thus their relative influence on the total transit time with cooling is smaller. We observe very little difference between the cutoff frequencies for 120K and 150K at low currents which may be because of measurement and experimental errors. Figure 35 shows the plot of $1/(2\pi f_T)$ against $1/I_C$ at 300K, 150K and 85K. The extrapolated transit time decreases from 0.7ps at 300K to 0.6ps at 150K and 0.5ps at 85K, and the total depletion capacitance of the device decreases with cooling, as expected, since the junction built-in voltages increase with cooling.

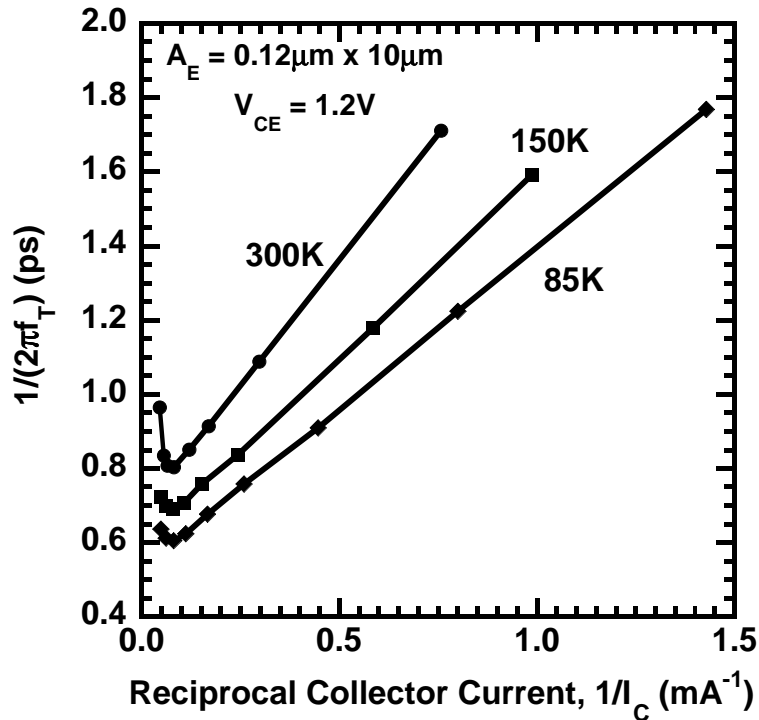


Figure 35: Extrapolated transit time as a function of reciprocal current $1/I_C$ at various temperatures for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

f_{max} is extracted from the measured S-parameters by extrapolating the unilateral gain at a -20 dB/decade slope. The peak f_{max} as a function of temperature is shown in figure 36. We observe that the peak f_{max} increases from about 280 GHz at 300K

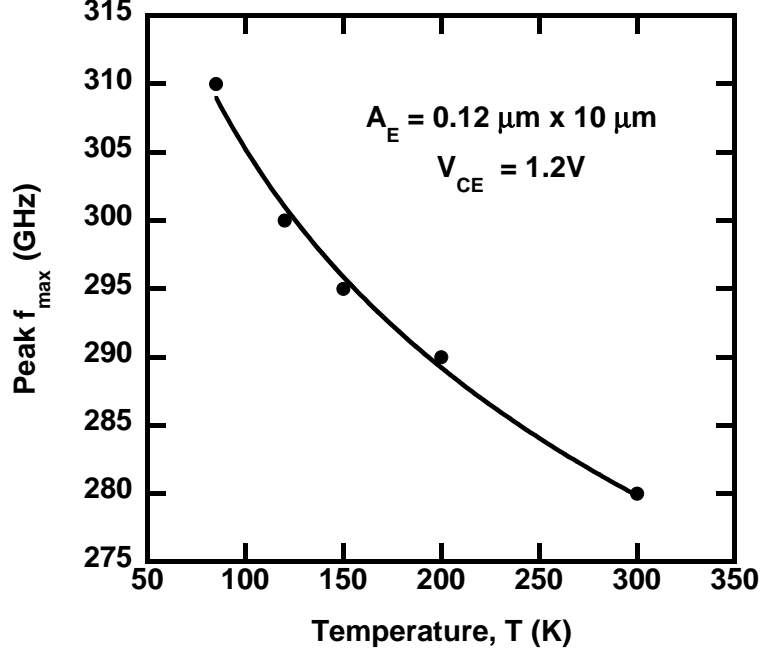


Figure 36: Peak f_{max} as a function of temperature for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

to 310 GHz at 85K.

3.4.3 Broadband Noise Performance

The main sources of broadband noise in these SiGe HBTs are the base and collector shot noise components, and the base resistance-induced thermal noise. High f_T and β , along with low base resistance, can be used to produce SiGe HBTs with excellent broad-band noise performance at 300 K [66, 67]. The minimum noise figure NF_{min} as a function of the collector current I_C (through g_m) can be written as (using the “transit time” model),

$$F_{min} \simeq 1 + \frac{1}{\beta} + \sqrt{\frac{2g_m R_n}{\beta} + \left(\frac{2R_n(\omega C_i)^2}{g_m} - \omega^2 C_i \tau_n R_n \right) \left(1 - \frac{1}{2g_m R_n} \right)} \quad (44)$$

The noise resistance R_n can be written as,

$$R_n = \frac{S_{v_n}}{4kT_0} = \frac{1}{4kT_0} \left(4kTr_{bb} + \frac{2qI_C}{|Y_{21}|^2} \right) \simeq \frac{T}{T_0} \left(r_{bb} + \frac{1}{2g_m} \right) \quad (45)$$

where, T_0 is 290 K and T is the ambient temperature. This indicates that as we go down in temperature, R_n also decreases and eventually becomes smaller than r_{bb} .

The variation of R_n and r_{bb} with temperature are shown in figure 37. This decrease in the extracted r_{bb} also indicates that the f_{max} should increase with cooling which is indeed the case here as was shown in figure 36.

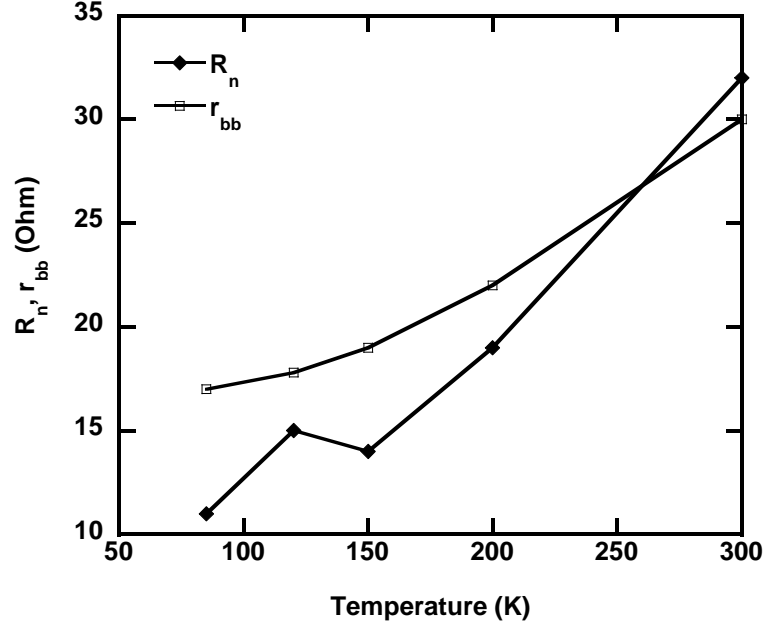


Figure 37: R_n and r_{bb} as functions of temperature for a $0.12 \times 10.0 \mu m^2$ SiGe HBT for $I_C = 12 mA$ and $f = 14 GHz$.

Since in this case, the current gain β increases drastically with cooling (figure 38) and there is a significant decrease in R_n , one would expect improved noise performance at low temperatures, provided the base resistance (r_{bb}) does not increase due to carrier freezeout at low temperatures. The measured noise data were well-behaved at all temperatures with near-ideal parabolic impedance surfaces. Error bars are estimated on the extracted noise data of approximately ± 0.1 dB.

Figure 39 shows the measured and modeled NF_{min} as a function of frequency at $I_C = 12 mA$ (peak f_T) for a $0.12 \times 10.0 \mu m^2$ SiGe HBT, at 300 K and 85 K. Because of the tremendous increase in peak- β from 600 to 3800 and decrease in R_n from 34Ω to 12Ω as we go from 300 K to 85 K, at the same I_C (g_m), the NF_{min} decreases significantly and becomes a little weaker function of the frequency at 85 K than 300

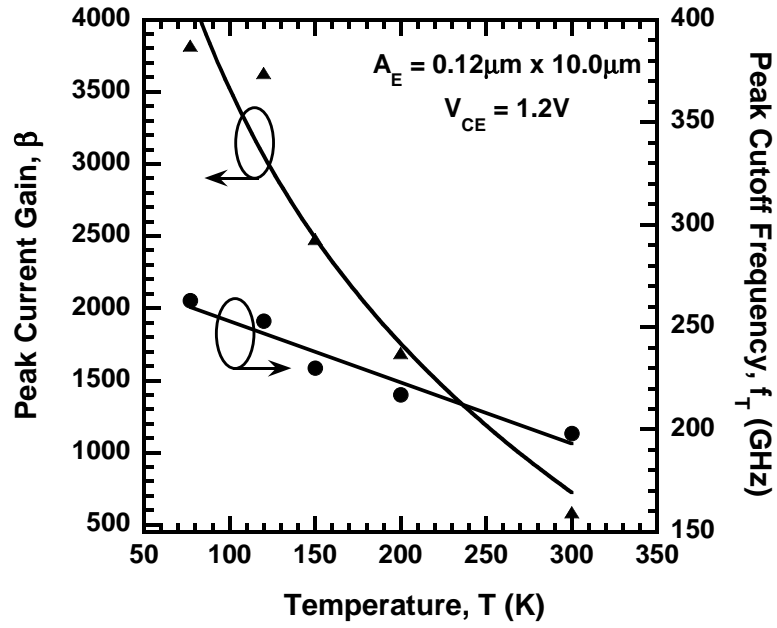


Figure 38: Cutoff frequency and current gain as a function of temperature for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

K (equations 44, 45). Hence the NF_{min} increases at a slower rate with frequency at

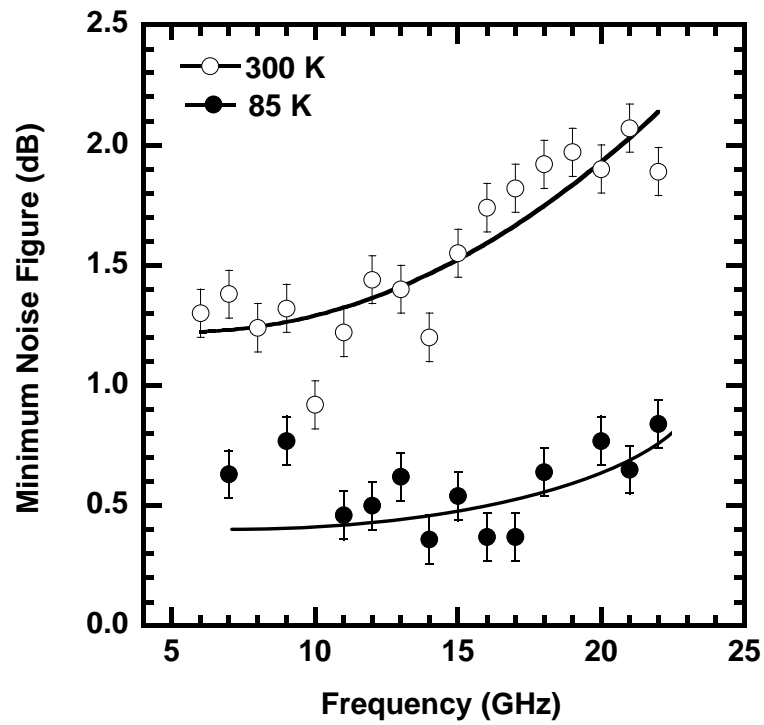


Figure 39: Measured and modeled minimum noise figure (NF_{min}) as a function of frequency at 300 K and 85 K. $I_C = 12 \text{ mA}$, $A_E = 0.12 \times 10.0 \mu\text{m}^2$.

85 K than at 300 K as shown in figure 39. At 85 K, this device achieves a minimum NF_{min} of about 0.3 dB at 14 GHz, and a minimum NF_{min} of about 0.75 dB at 20 GHz.

Figure 40 shows the measured and modeled noise resistance as a function of frequency at 300 K and 85 K. From equation 45, one would expect R_n to be constant

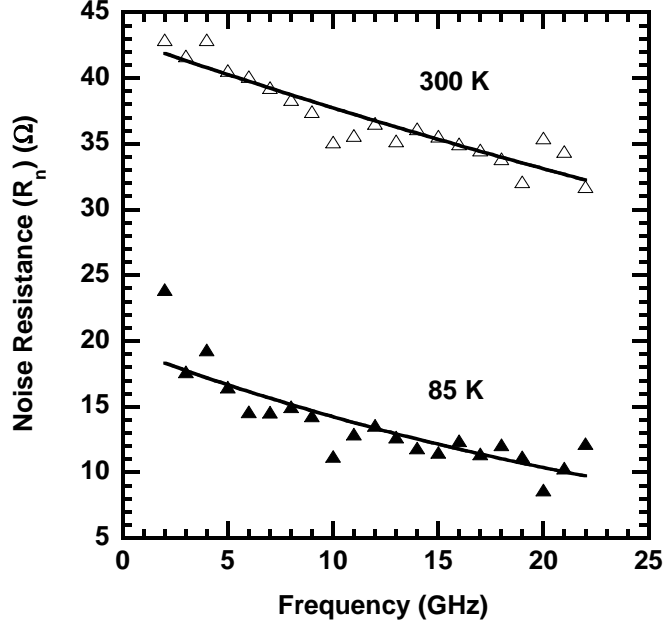


Figure 40: Measured and modeled noise resistance (R_n) as a function of frequency at 300 K and 85 K. $I_C = 12 \text{ mA}$, $A_E = 0.12 \times 10.0 \text{ } \mu\text{m}^2$.

with frequency. However, a closer look yields $|Y_{21}|^2 = g_m^2 + (\omega C_{bc})^2$, which increases with frequency (ω), thus reducing R_n as we go high in frequency. Figure 41 shows the measured and modeled associated gain as a function of frequency at 300 K and 85 K. The associated gain increases as we go from 300 K to 85 K, owing to the increase of $|Y_{21}|$ and significant decrease in $|Y_{11}|$ which can be seen from equations 46. As explained in chapter 2, the associated gain can be written as,

$$G_A = \left| \frac{Y_{21}}{Y_{11} + Y_{s,opt}} \right|^2 \frac{Re(Y_{s,opt})}{Re(Y_{out})} \quad (46)$$

where, $Y_{11} = g_m/\beta + j\omega C_i$, etc. (equation 22).

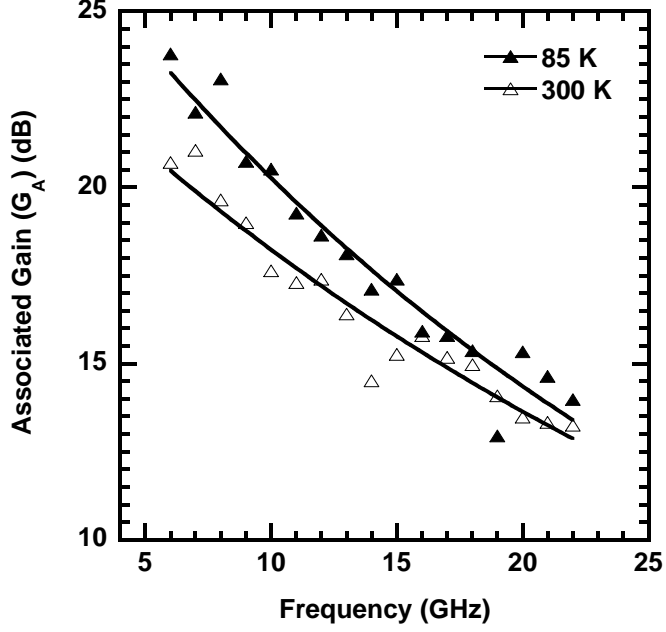


Figure 41: Measured and modeled associated gain as a function of frequency at 300 K and 85 K. $I_C = 12 \text{ mA}$, $A_E = 0.12 \times 10.0 \text{ } \mu\text{m}^2$.

Figures 42 and 43 show the measured and modeled minimum noise figure (NF_{min}) as a function of bias current at 14 GHz at 300 K and 85 K, respectively. Interestingly, the rapid increase in NF_{min} at high bias currents at 300 K, which is primarily determined by the base shot noise component, disappears at cryogenic temperatures, again due to the combined increase in β , and g_m , and decrease of R_n with cooling (44), allowing lower NF_{min} to be achieved at peak f_T at 85 K.

Figure 44 shows the behavior of minimum NF_{min} as a function of temperature. At a fixed collector current I_C (g_m) and frequency, NF_{min} depends on R_n , β and r_{bb} and hence NF_{min} decreases as the temperature goes down from 300 K to 85 K (44). This combined effect leads to a substantial decrease in the NF_{min} with decreasing temperature, before it gets dominated by the saturation of the base resistance, and the minimum noise figure tends to saturate.

To summarize, the current-voltage (dc), small-signal ac , and broadband noise characteristics of a 200 GHz SiGe HBT technology have been measured down to 85

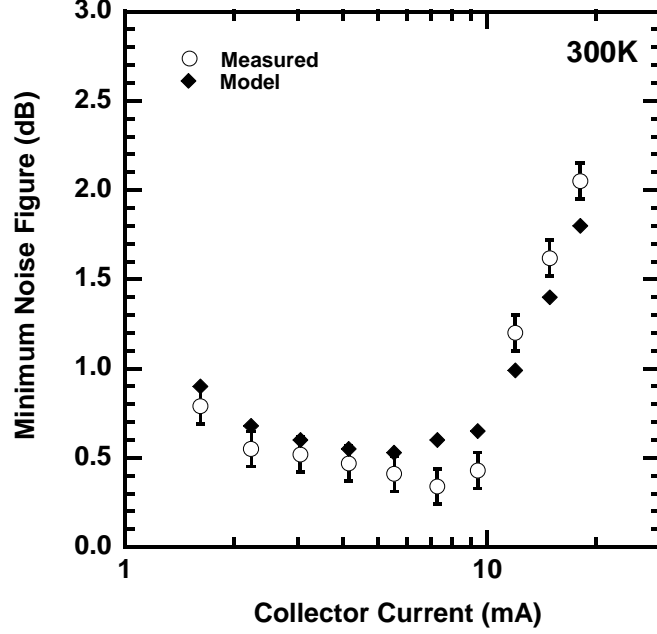


Figure 42: Minimum Noise Figure as a function of bias current at 300K for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

K. At cryogenic temperatures, these SiGe HBTs maintain excellent dc ideality, with a peak current gain of 3800, a peak cut-off frequency of 260 GHz, a peak of 310 GHz, and a minimum noise figure of approximately 0.30 dB at a frequency of 14 GHz and in all cases represent significant improvements over their corresponding 300 K values. The “transit-time” based noise model is used to model the noise figure, associated gain and noise resistance (R_n) as functions of frequency and bias. The model gives an excellent agreement to the measurements and demonstrates the validity of the modeling approach at cryogenic temperatures. The significant improvement in the noise performance at cryogenic temperatures indicate the excellent opportunity for designing circuits for extreme environment electronics using SiGe HBTs. Low R_n also means that the noise in the circuit is less sensitive to the source impedances thus paving the way for broadband low noise circuit design at cryogenic temperatures. Overall SiGe HBTs promise to be a compelling alternative to InP and GaAs for certain niche cryogenic applications.

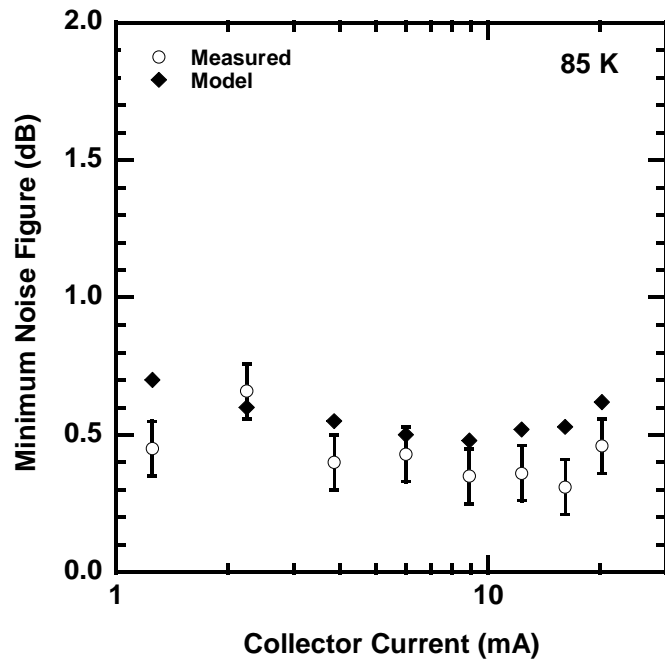


Figure 43: Minimum Noise Figure as a function of bias current at 85K for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

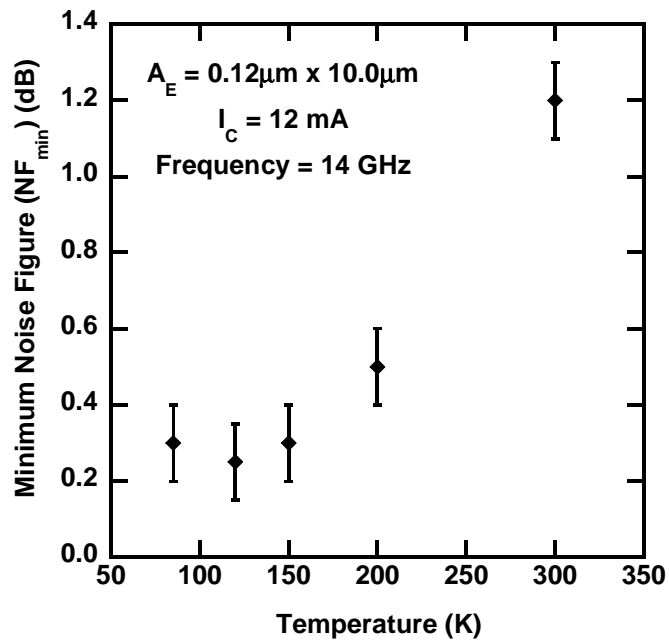


Figure 44: Minimum Noise Figure as a function of temperature for a $0.12 \times 10.0 \mu\text{m}^2$ SiGe HBT.

CHAPTER IV

SUBSTRATE PARASITIC MODELING IN SILICON GERMANIUM TECHNOLOGY

In this chapter the effects of substrate parasitics in silicon germanium and silicon-based processes, in general, are analyzed. A methodology for designing RF circuits in silicon is presented. Excellent agreement between simulations and measurements for a test-case LNA, designed for IEEE 802.11a application, is demonstrated. The LNA operates in the 5-6 GHz band and employs gain switching. It is designed in a 0.8 μm SiGe bipolar technology with a peak f_T of 50 GHz.

4.1 Substrate Effects in Silicon

Coupling of signal through the substrate is a significant problem in designing radio frequency, microwave and millimeter wave integrated circuits on silicon based processes. This is due to the non-ideal isolation provided by the common substrate shared between different circuits components on the chip. The interaction through the substrate is also present between different devices of the same circuit that needs to be taken into account during the design [50], [68].

Figure 45 shows an example of the typical substrate parasitic effect that exists in silicon. Generally, the parasitics affect the performance of an amplifier by lowering the gain and increasing the noise figure. This is due to undesirable feedback and shift in the input and output match. Also, appreciable positive feedback can lead to oscillations in the circuit. Figure 46 shows a typical example of how the parasitics were modeled in simulations. A feedback path consisting of a capacitor in series with a resistor is placed between the collector and the base of a transistor to account for

the substrate coupling.

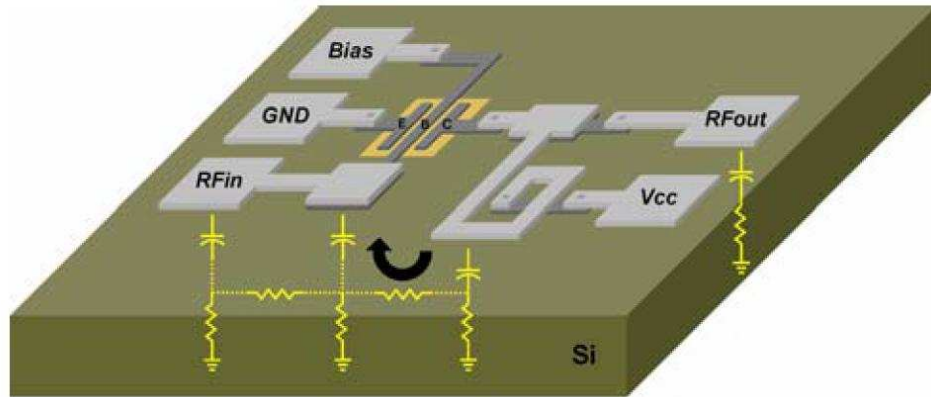


Figure 45: The effects of substrate parasitics in silicon. A positive feedback from an inductor to a capacitor is shown as an example.

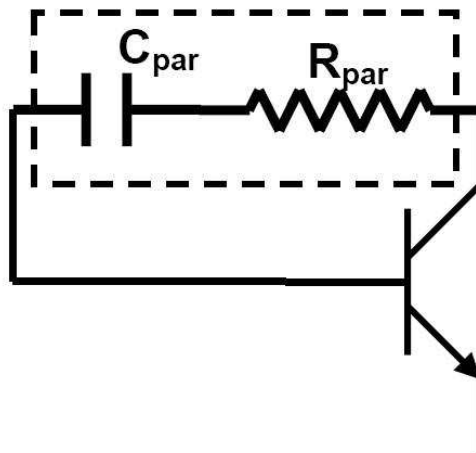


Figure 46: Illustration of how the substrate modeling was introduced in simulations.

The value of the resistor and the capacitor (R_{par} and C_{par}) depends on the physical distance between the points in the layout, resistivity of the substrate and the thickness of the dielectric layer between the metal line and the substrate. In our case, the resistivity of the material was $20 \Omega - cm$. The substrate resistances were of the order of few hundreds (300-400) of ohms for a distance of about $200 \mu m$. Also, the feedback capacitors were of the order of 0.01-0.05 pF. The capacitance was calculated

using the standard formula:

$$C = \epsilon_0 \epsilon_r \frac{L}{A} \quad (47)$$

The metal lines used in the layout for connection has also been modeled as a distributed transmission line, as shown in Figure 47. R_{Line} is estimated using the given

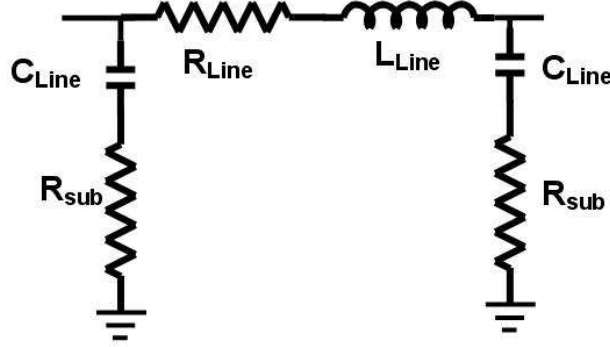


Figure 47: Transmission line model used for the metal connectors in the layout.

resistivity of the metal, while C_{Line} takes into account the dielectric constant of the material and the thickness of the dielectric layer between the metal line and the substrate. R_{sub} is estimated to be a constant resistance for a metal layer (which in our case was approximately 500Ω). The inductor (L_{Line}) is estimated from the substrate parameters as in case of a microstrip line [69]. In many cases where the distance between the two ends are appreciably large, like in case of inductors, the estimation of the parasitics was done for the two ends separately and an average was taken. The equivalent model for this case is shown in figure 48 where the feedback is distributed between the two ends.

4.2 5-6 GHz SiGe LNA Design

The simplified schematic of the LNA is shown in Figure 49.

The LNA is a 3-stage common emitter design. A common emitter topology provides a narrow band tuned to the desired band using the load inductance and a

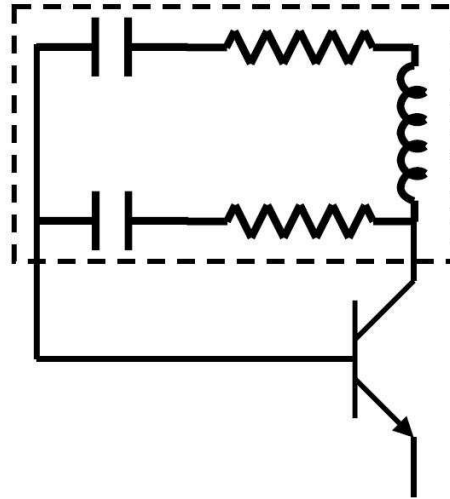


Figure 48: Typical model for the distributed feedback in case of a large component like inductor

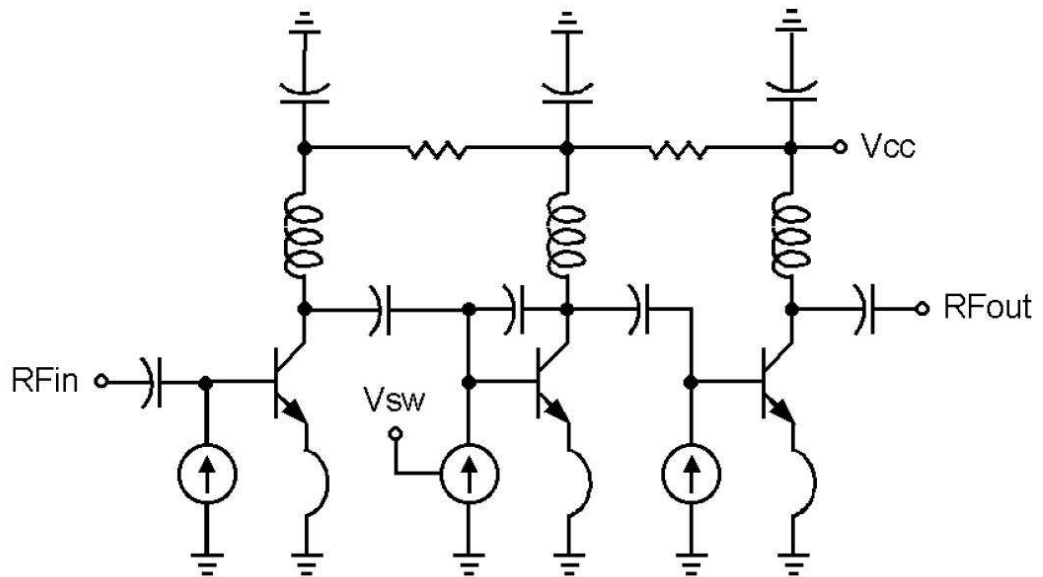


Figure 49: Simplified circuit schematic of the Switched-Gain LNA.

capacitive output match, while maintaining a low noise figure. The input and output of the LNA are matched to a 50Ω impedance. The second-stage of the LNA is used for gain switching, while the first and third stages are used as buffers to keep the input and output impedances matched in both the high and low-gain modes. The two-modes of operation, high-gain and low-gain are to account for the large signal magnitude in case of close proximity of the receiver to the the transmitter. In such

case, the gain is reduced by switching off the second stage thus limiting the signal power so that it does not saturate the circuit blocks which follow the LNA in the complete receiver.

Figure 50 shows the schematic of the LNA with the effect of parasitics taken into account while designing. The modeled parasitics are plugged into the simulations and the circuit is further optimized. The metal line models are not shown in this figure but included during simulations.

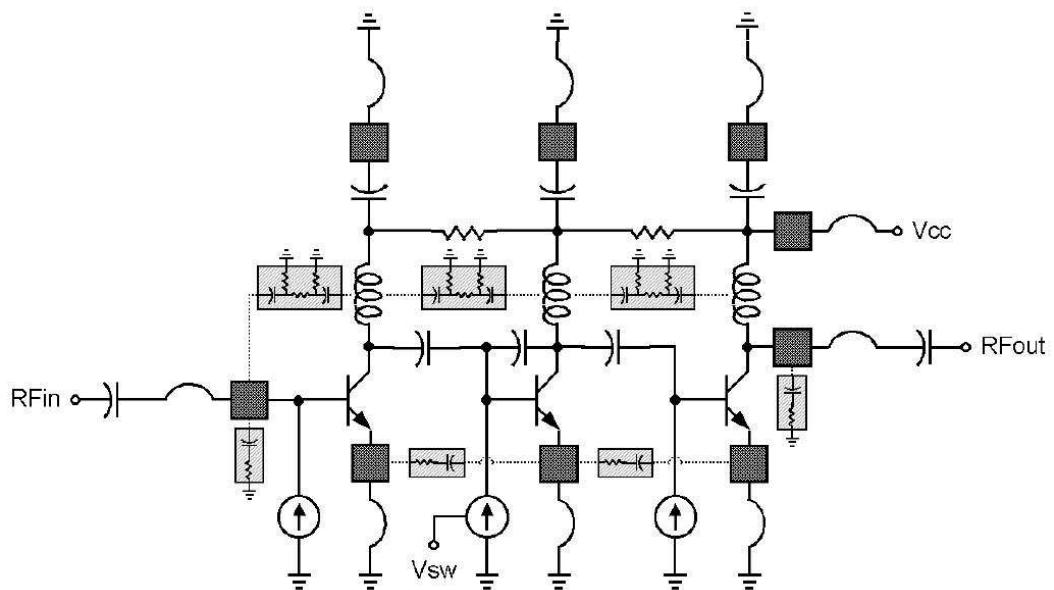


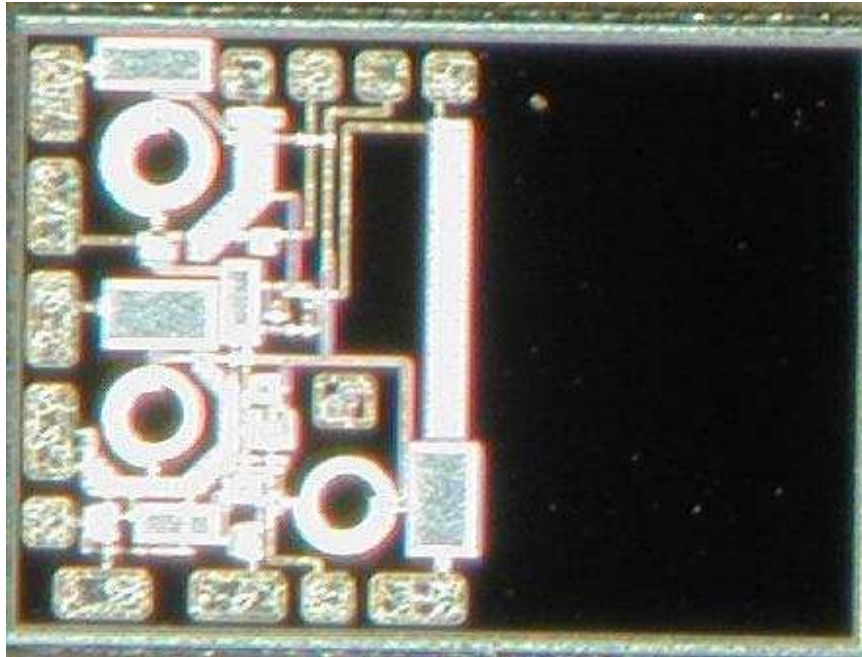
Figure 50: Circuit schematic of the Switched-Gain LNA with the substrate parasitics.

4.3 Measurement Results and Discussion

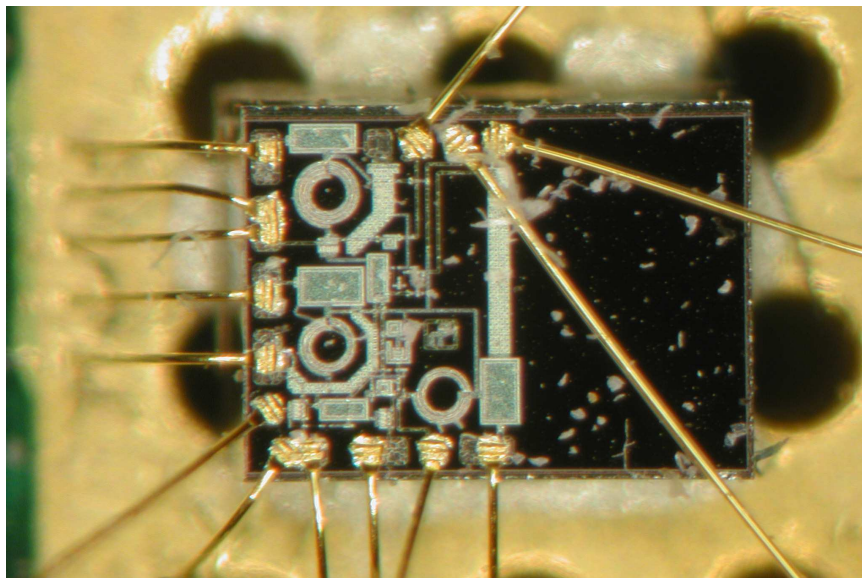
The die-micrograph and the bonding diagram of the LNA are shown in figure 51. The die-size is $620 \mu m \times 790 \mu m$.

Figure 52 shows the correspondence between simulations and measurement results for the gain (S_{21}) of the LNA in high and low gain modes of operation.

Figure 53 shows the measured gain and noise figure of the LNA in both the high and low-gain modes. As shown, this topology yields not only a low noise figure of



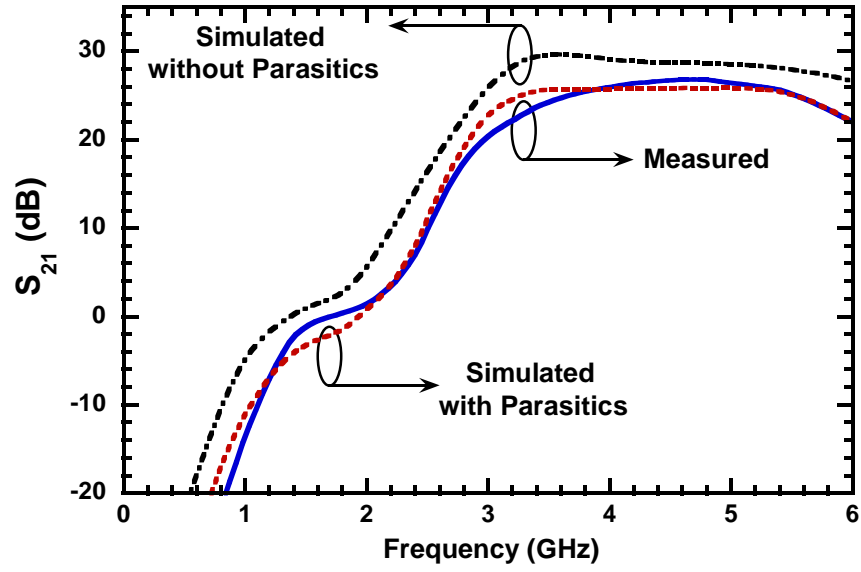
(a)



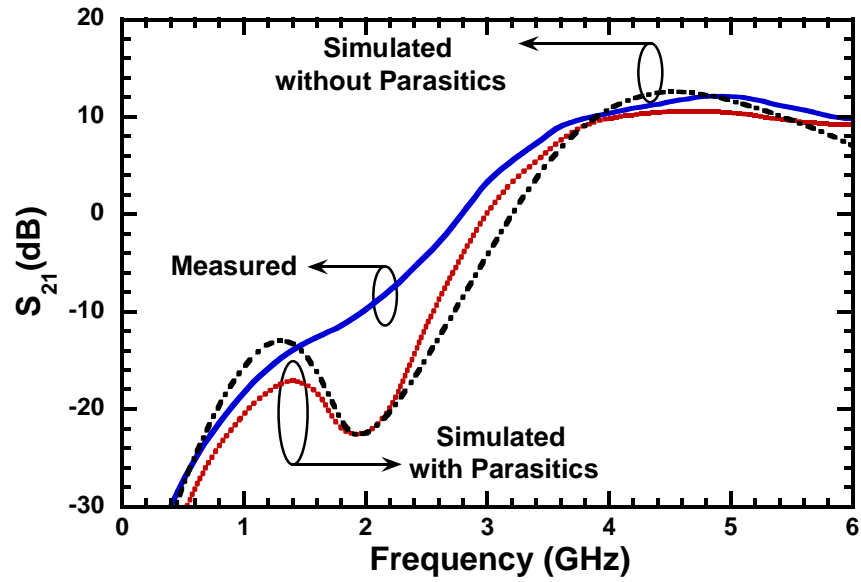
(b)

Figure 51: (a) Die-microphotograph and the (b) bonding diagram of the LNA.

2.5 dB in the high-gain mode, but also maintains a noise figure below 4dB in low-gain mode over the entire 5-6 GHz band. Table 1 shows the complete measured performance of the LNA. The supply voltage used for the LNA is 3 V. The IIP_3 measurement was performed with two tones at 5.5 GHz and 5.499 GHz.



(a)



(b)

Figure 52: Simulated and measured S_{21} of the 5-GHz LNA for (a) High-Gain Mode, and (b) Low-Gain Mode.

Hence, a methodology for design of RF circuits in silicon based processes is demonstrated. This methodology allows for accurate simulation of key performance criteria and accounts for impact of substrate parasitics. Measurement show excellent correlation with the simulation results verifying the techniques presented. The parasitic

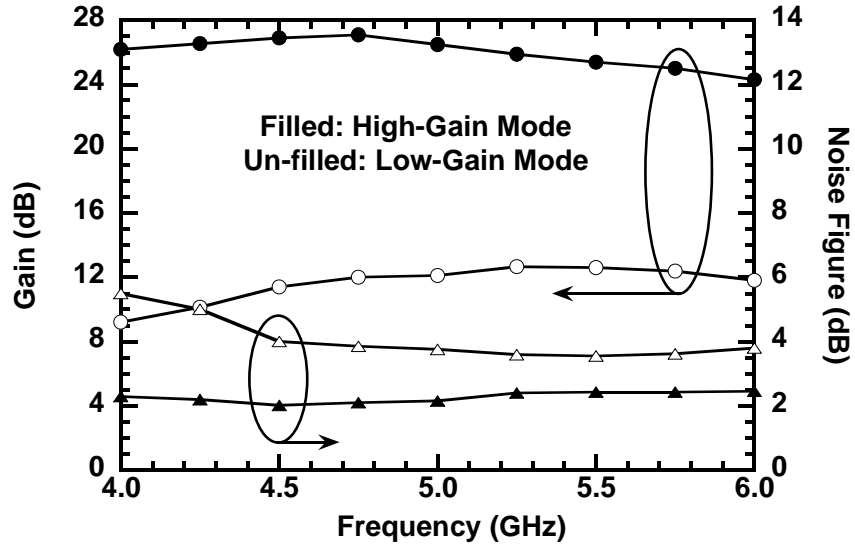


Figure 53: Measurement results of 5-GHz LNA in High-Gain and Low-Gain Modes of operation.

Table 1: Measured data for the LNA at 5.5 GHz. Supply voltage is 3 V.

	High-Gain Mode	Low-Gain Mode
Gain	25 dB	12 dB
Noise Figure	2.5 dB	3.7 dB
IIP_3	-13 dBm	-2.3 dB
S_{11}	-12 dB	-8 dB
DC Current	18 mA	16 mW

effects of the silicon substrate are taken into account during the design and a good agreement has been established between simulated and measured data for a test-case LNA designed for the 5 GHz band. A measured gain of more than 24dB and a noise figure better than 2.5 dB are achieved in the 5–6 GHz band.

CHAPTER V

DEVELOPMENT OF A TRANSCEIVER FRONT END FOR IEEE 802.11A/B/G WIRELESS LAN APPLICATIONS

In this chapter, a complete RF Front-End Receiver is presented that is designed using a $0.8 \mu m$ Silicon Germanium HBT process. The circuit is implemented for IEEE 802.11a/b/g wireless local area network (WLAN) applications. The RF IC uses an on-chip frequency doubler for the 2.4 GHz band and by-passes that with an LO buffer for the 5 GHz band. This simple and compact architecture allows the use of only one external frequency synthesizer for both the bands and helps in providing immunity to interference. The transceiver also consists of two switched-gain low noise amplifiers (LNAs), receive and transmit mixers, two transmit drivers, a local oscillator (LO) doubler/buffer and power management control and selects between transmit/receive, high/low-gain (for receive) and 2.4/5 GHz modes of operation.

5.1 IEEE 802.11a/b/g WLAN Standard

IEEE 802.11 refers to the set of WLAN standards developed by the IEEE standards committee. The IEEE 802.11 family currently has six wireless modulation techniques using the same protocol. Among them the standards defined by 802.11a, 802.11b and 802.11g are the most popular amendments to the original standard. The 802.11b and 802.11g standards operate at the 2.4 GHz band while the IEEE 802.11a occupies the 5 GHz band. This choice in frequency makes the 802.11b/g equipments susceptible to interference from other equipments working in the same 2.4 GHz band, such as,

cordless telephones, bluetooth devices, microwave ovens, etc. The 802.11a standard, however, is unaffected by these interferers.

The original IEEE 802.11 standard was released in 1997 and specified two raw data rates of 1 megabits per second (Mbps) and 2 Mbps, transmitted using infrared (IR) signals by Frequency Hopping Spread spectrum (FHSS) and Direct Sequence Spread Spectrum (DSSS) in the Industrial Scientific Medical (ISM) frequency band of 2.4 GHz. In order to improve the reliability of the data transmissions, a significant amount of raw channel capacity was devoted to Carrier Sense Multiple Access with Collision Avoidance method (CSMA/CA). The 802.11b amendment to the 802.11 standard was ratified in 1999. The 802.11b standard allows a maximum data rate of 11 Mbps employing the same CSMA/CA method and uses a Complementary Code Keying (CCK) modulation technique. Though the maximum data rate is 11 Mbps, it scales down to 5.5 Mbps, 2 Mbps and 1 Mbps if there is a degradation in the signal quality because of various external factors. This is called the Adaptive Rate Selection. The less complex modulation schemes and more redundant data encoding at lower data rates renders the signal more robust against interference and attenuation.

The 802.11a amendment to the original 802.11 standard was also ratified in 1999. This uses the same core protocol but operates in the 5 GHz band employing an Orthogonal Frequency Division Multiplexing (OFDM) modulation scheme using 52-subcarriers. The maximum data rate achievable is 54 Mbps, and scales down to 48, 36, 24, 18, 12, 9 and 6 Mbps speeds as required to maintain adequate signal quality. The 802.11a standard has 12 non-overlapping channels, 8 dedicated for indoor applications and 4 to point-to-point applications. The main advantage of the 802.11a standard is the higher data rates and less interference from the 2.4 GHz ISM band which houses a plethora of applications. The high frequency band also leads to the main disadvantage of this standard which is the lack of signal penetration and significant signal attenuation over short distances. This “line of sight” requirement

necessitates the use of more access points and signal repeaters and hence more power consumption. The total bandwidth is 20 MHz with an occupied bandwidth of 16.6 MHz. The symbol duration is $4 \mu s$ and there is a guard interval of $0.8 \mu s$. The 52 OFDM subcarriers are split into 4 pilot and 48 data subcarriers with a separation of 312.5 kHz ($20 \text{ MHz}/64$). Each of these subcarriers is modulated using either BPSK, QPSK, 16-QAM or 64-QAM. Figure 54 shows the schematic of the spectrum of 802.11a signal. The use of OFDM helps in increasing the spectral efficiency and reduces the effects of multipath fading.

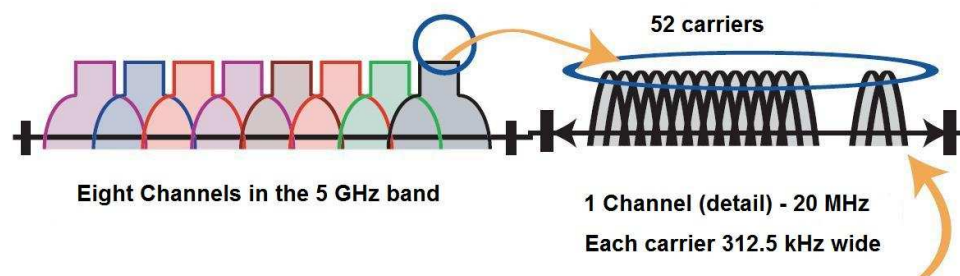


Figure 54: Schematic of the OFDM signal spectrum of IEEE 802.11a WLAN standard.

A third amendment to the original 802.11 standard led to the 802.11g standard in 2003. This works in the same ISM band (2.4 GHz) as the 802.11b standard but offers data rates of upto 54 Mbps similar to the 802.11a standard and at the same time it is back compatible to the 802.11b standard. 802.11g also employs OFDM for the data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps and reverts to CCK for 5.5 and 11 Mbps and DBPSK/DQPSK + DSSS for 1 and 2 Mbps. Although the maximum range for 802.11g (at 54 Mbps) is shorter than that of 802.11b, it is slightly more than that at comparable data speeds. This makes it a good combination of both 802.11a and 802.11b. Table 2 shows the salient features of IEEE 802.11a/b/g standards.

Table 2: IEEE 802.11a/b/g Operating Specifications

Protocol	Frequency Band	Data Rate (Typ.)	Data Rate (Max.)	Range (Indoor)
802.11a	5 GHz	25 Mbps	54 Mbps	30 m
802.11b	2.4 GHz	6.5 Mbps	11 Mbps	30 m (11 Mbps) 90 m (1 Mbps)
802.11g	2.4 GHz	25 Mbps	54 Mbps	30 m

5.2 Architecture and Design Considerations

Figure 55 shows the block diagram of the dual-band super-heterodyne transceiver with a typical dual-band GaAs front-end module, encapsulating the RF switches, a dual-band power amplifier (PA), and the low-pass harmonic filters. All the other RF blocks are integrated on a single dual-band SiGe RF IC. In integration of this dual-band RF IC, problem of high package pin count and poor RF isolation were addressed through modification to the receiver system design.

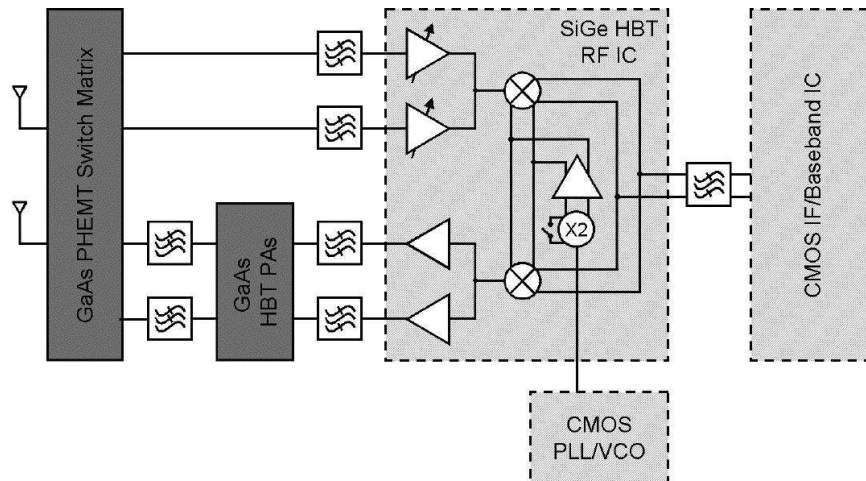


Figure 55: Block Diagram of the SiGe Transceiver with a typical GaAs front-end module.

As shown in figure 55, all off-chip RF filters are placed in front of the LNAs (for the receive path) and the driver amplifiers (for the transmit path) instead of the typical location in between the mixer and LNA's/drivers. This unique architecture reduces filter count by allowing multiplexing of the transmit and receive chains. The proposed architecture here shares the LO, IF chip and the RF first down conversion. The first up down converter and LO are broadband IC components so that they can cover both the 2.4 and 5 GHz bands.

All the pins associated with routing the RF signals for off-chip filtering are eliminated which, while reducing size and complexity, unfortunately increases the overall receiver noise figure and image interference in the receive path. Therefore, successful implementations of this architecture depends on judicial choice of high IF frequency and full utilization of low-noise SiGe devices in the design of the LNAs. The on-chip digital logic controls can be configured independently to turn-off the transmit and receive chains, as well as the LO buffer when not in use. Hence the IC consumes very little current and requires only a single positive supply.

This proposed dual-band system architecture allows operation in either / or 802.11 a, b and g modes, has many advantages, and solves some significant performance challenges. This broadband architecture uses less number of RF chips and is much smaller size and lower in cost than the narrowband architectures.

The architecture has a 2.4 GHz to 5 GHz RF front-end which converts the RF to an IF of 300–600 MHz. The first IF is chosen to be 374 MHz which allows for the low-cost surface acoustic wave (SAW) filtering with high rejection of spurious and LO signals. A single off-chip VCO/PLL frequency synthesizer is used in combination with an on-chip doubler/buffer. The doubler path is selected when operating in the 802.11a mode while it is shunted as a buffer when in the 802.11b/g mode. This choice of IF allows for LO signals to be generated with the same off-chip PLL for both the 2.4 GHz and 5 GHz bands. The PLL generates 1800–2200 MHz LO needed for the 2.4

GHz conversion, and 2275–2825 MHz is generated for the 5 GHz band and doubled to get the proper LO.

Another unique feature of this architecture is the common first RF mixer for transmit and receive path. This eliminates the need for extra RF mixer in the lineup by sharing the mixer. The common RF mixer allows for sharing of the band pass filter in transmit and receive paths allowing lower area and cost of the radio. The components of the broadband IC must be designed carefully to meet all the specifications needed for each of the bands. In particular the LNA must be designed to meet the tough noise figure specs for the 5 GHz band without sacrificing the performance at 2.4 GHz. This is done by using a broadband five element matching network at the LNA input. Similarly the LO amplifier and the mixer also need to have a broadband circuit topology covering 2.4- 5.8 GHz bandwidth. Another benefit of this architecture is that this transceiver is also usable for the 3.5 GHz which is a popular band for the broadband wireless access (BWA) applications which is evolving as the IEEE 802.16 WiMax standard.

A great deal of attention was given to substrate parasitic effects in silicon, as explained in the last chapter, which becomes quite substantial at the 5 GHz band. The substrate is modeled as in [55], and [50], so as to optimize the performance of individual blocks and also to have accurate matching between different sub-circuits.

The front end was implemented in a 2-metal layer, 0.8- μm SiGe bipolar process with an f_T of 50 GHz.

5.3 Front End Circuit Blocks

5.3.1 Low Noise Amplifiers

The 5 GHz low-noise amplifier (LNA) is a three stage common-emitter design, as described in the last chapter (figure 49), with the second stage used for gain switching. The first and third stage provide buffering for the middle stage so that the input and

output impedances of the LNA do not change between high- and low-gain modes of operation. For a broadband matching over the 2.4-5 GHz bands, both amplifiers use a combination of input wire-bond inductance, off-chip capacitors and emitter-degeneration using down-bond inductance to optimize input noise figure (NF) and provide a $50\ \Omega$ match. For the 2.4 GHz LNA, sufficient gain is achieved with only two stages. Owing to the high gain of the SiGe devices at 2.4 GHz, lack of a third-stage impedance buffering and mismatch is tolerable for this band.

5.3.2 Mixers

The receive mixer uses a modified Gilbert Cell (GC) design that incorporates single-ended to differential conversion on the RF path as shown in figure 56.

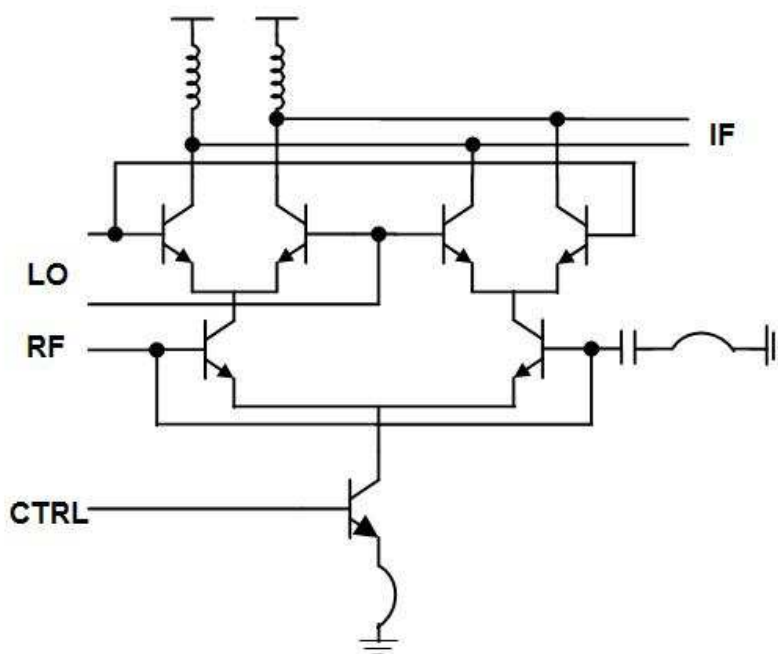


Figure 56: Simple Circuit Schematic of the Receive Mixer

The performance of the mixer is optimized for the 5 GHz band while still providing adequate performance at 2.4 GHz. Again, a broadband match is achieved using a five

element matching network. To provide sufficient image rejection, the outputs of both LNAs combine on-chip through a single LC duplexer and connect to the receive mixer. For flexibility, the output mixer utilizes off-chip reactive matching for a $200\ \Omega$ IF interface with a tunable frequency range from 150 to 800 MHz. The transmit mixer uses a similar GC topology that mates with the receive mixer at the IF port and feeds the drivers through a differential to single-ended converter.

5.3.3 Frequency Doubler

A standard GC mixer is used as a frequency doubler. The LO drive to both the mixers is fed from either the GC doubler or a parallel-connected emitter follower buffer. Figure 57 shows the simple circuit schematic of the frequency doubler. The doubler path is selected when operating in the 802.11a mode and the buffer when in the 802.11b/g mode. The LO doubler and buffer share a common single-ended input that is matched internally to $50\ \Omega$ and can accept an LO input power range of -7 dBm to 0 dBm.

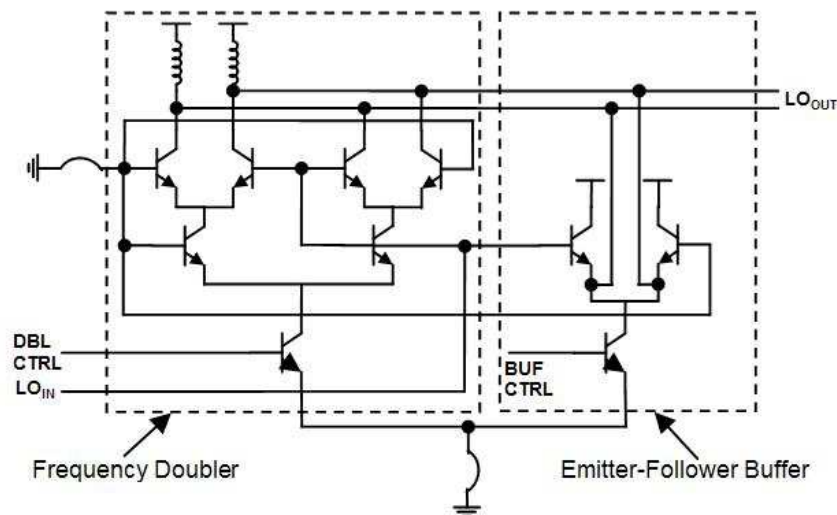


Figure 57: Simple Circuit Schematic of the Frequency Doubler/Buffer

5.3.4 Transmit Drivers

The output of the transmit mixer is connected to the two transmit drivers through on-chip LC tanks. The on-chip LC duplexer helps to provide isolation between drivers while providing LO and image rejection. The drivers utilize single-ended common emitter topology that helps to reduce dc power consumption and overcome substrate loss at 5 GHz band. Both drivers make use of on-chip matching with an exception of a single off-chip capacitor for the 5 GHz driver.

5.4 Measurement Results and Discussion

Figure 58 shows the die microphotograph of the dual-band SiGe RF IC. The die size was $1.6 \text{ mm} \times 2.5 \text{ mm}$. This IC is successfully implemented in a 32-pin $5 \times 5 \text{ mm}^2$ low-profile lead-less package.

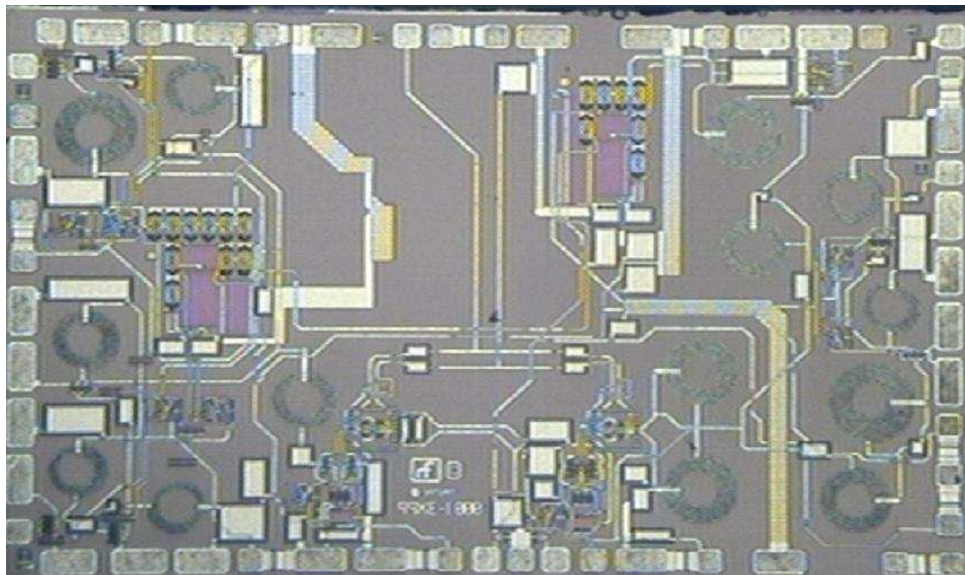


Figure 58: Die Microphotograph of the SiGe RF IC. Die size: $1.6 \text{ mm} \times 2.5 \text{ mm}$.

Figure 59 shows the Conversion Gain (CG) of the receiver chains as a function of frequency, for the 5 GHz and 2.4 GHz bands, respectively. The peak gain for the 5 GHz band is about 28 dB at 5.25 GHz in the high-gain (HG) mode and about 16 dB in the low-gain (LG) mode. For the 2.4 GHz band, the peak gain is about 23 dB in the at 2.5 GHz in the HG mode and about 3 dB in the LG mode.

Figure 60 shows the noise figures and gain of the receiver for the IEEE802.11a band operation. A minimum noise figure of 4.8 dB is obtained in the high gain mode with a gain of about 18 dB. In the low gain mode, the gain drops by about 15 dB. Figure 61 shows the noise figures and gain of the receiver for the IEEE802.11b/g band operation. A minimum noise figure of 3 dB is obtained in the high gain mode with a gain of about 20 dB. In the low gain mode, the gain drops by about 18 dB.

The conversion-gain as a function of local-oscillator (LO) power is shown in figure 62. The gains are seen to be nearly constant for an LO power variation from -10 dBm to 0 dBm for both high and low gain modes of operation in both the bands. The results are for the frequencies of 5.25 GHz and 2.45 GHz for an IF power of -40 dBm. Figure 63 shows the conversion gain as a function of LO power. As can be seen, for both the bands the CG increases till an LO-power of -5dBm and then saturates. This allows us to choose an LO-power of -5dBm and save on LO-power requirement and get the required CG.

Figure 64 shows the conversion gain for the transmit-chain as a function of frequency in the 5 GHz and 2.4 GHz bands, respectively. Gains of the transmit mixer and the driver amplifier are shown along with the overall gain of the transmit chain. As can be seen, the mixer-gain remains nearly constant with frequency. In both the 5 GHz and 2.4 GHz bands, the overall gain peaks to about 15 dB.

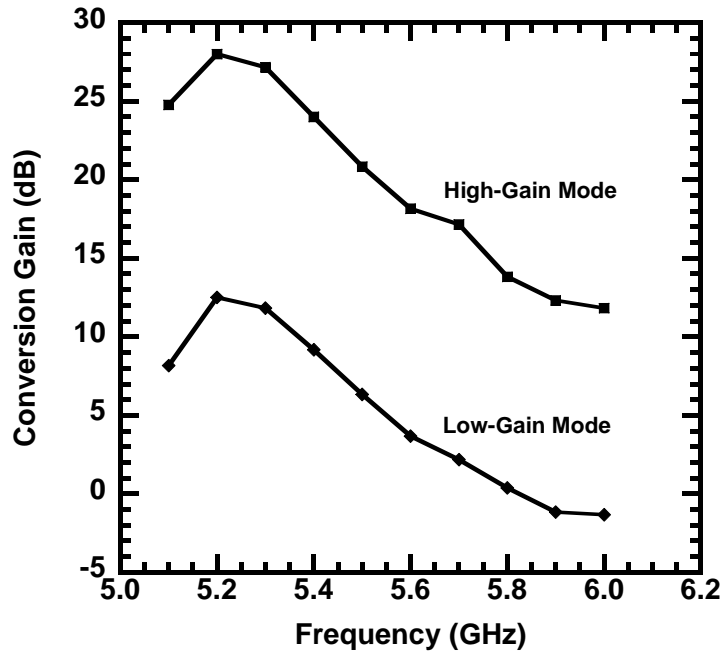
Figures 65 - 67 show the transmit spectrum for the 5 GHz and 2.4 GHz bands, respectively, compared to the IEEE802.11a/b/g standards specification masks. As can be seen, the transmit spectra meet the required specifications.

Table 3 shows the a performance summary of the receive chain of the RF IC at an IF of 374 MHz and LO power of -7 dBm, for both 802.11a and 802.11b/g RF frequency bands. Table 4 summarizes the performance of the transmit-chain for an LO power of -6 dBm.

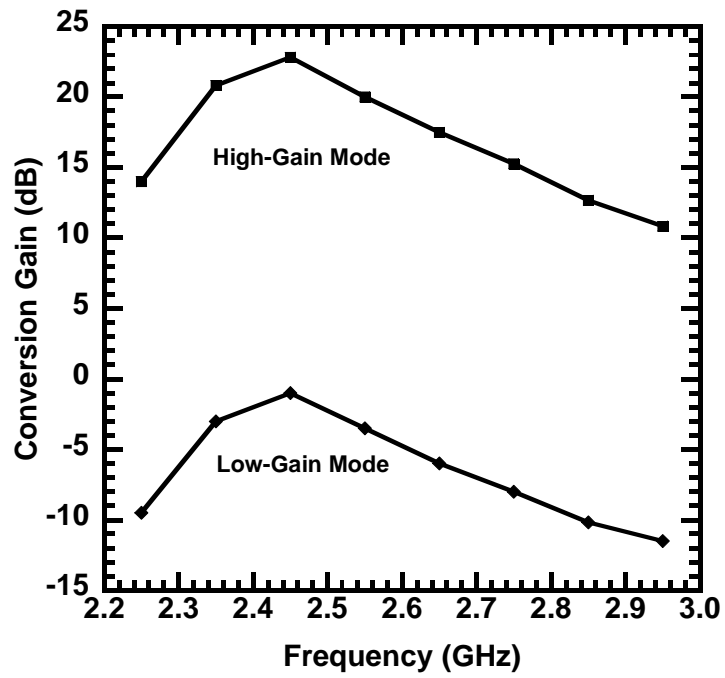
Table 3: Summary of the RF IC Performance - Receive Chain

Parameters	802.11a (High Gain)	802.11a (Low Gain)	802.11b/g (High Gain)	802.11b/g (Low Gain)
Conversion Gain	29 dB	12 dB	24 dB	-1 dB
Input P1dB	-36 dBm	-17 dBm	-31 dBm	-5 dBm
IIP3	-23 dBm	-8 dBm	-20 dBm	4 dBm
Noise Figure	7.0 dB	18 dB	6.2 dB	23.0 dB
Image Rejection	10 dB	11 dB	15 dB	14 dB
LO/IF Isolation	37.8 dB	40 dB	68.5 dB	43.3 dB
RF Return Loss	10 dB	9 dB	11.5 dB	14.3 dB
IF Return Loss	>12dB	>12 dB	>12 dB	>12 dB
LO Power	-7 dBm	-7 dBm	-7 dBm	-7 dBm
Current	34 mA	30 mA	30 mA	26 mA
Power Consumption	102 mW	90 mW	90 mW	78 mW

To summarize, a novel architecture for IEEE 802.11a/b/g WLAN dualband transceiver in SiGe bipolar process is developed. A new topology with an on-chip doubler/LO-buffer is presented which uses only one off-chip frequency synthesizer for both the 2.4 GHz and 5 GHz bands. The 3.0 V transceiver has been implemented in a 2 metal layer, 0.8 μm , 50 GHz SiGe bipolar technology. The overall measured performance of the transceiver meets the requirements of IEEE802.11a/b/g WLAN standards.

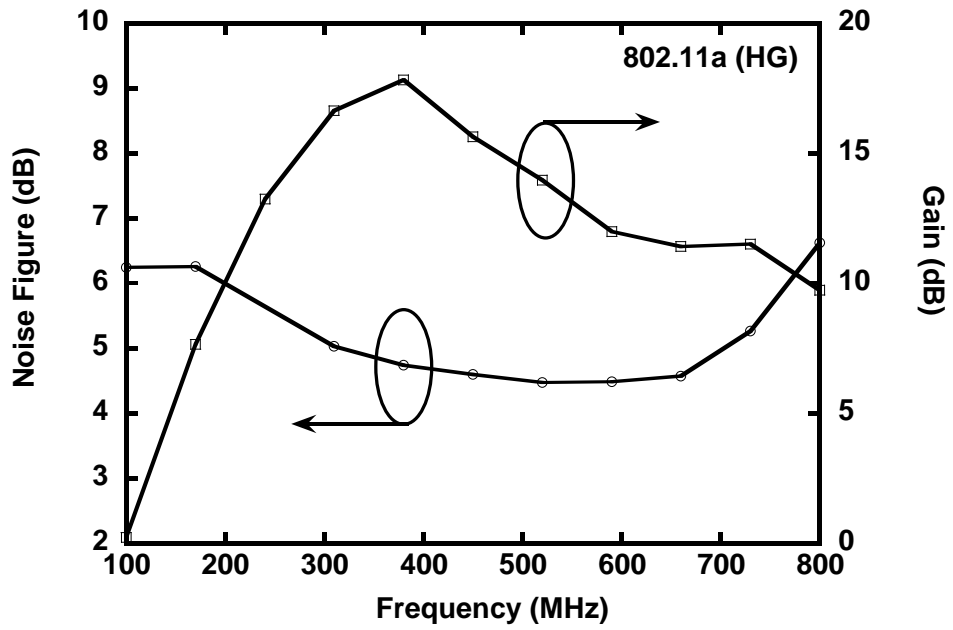


(a)

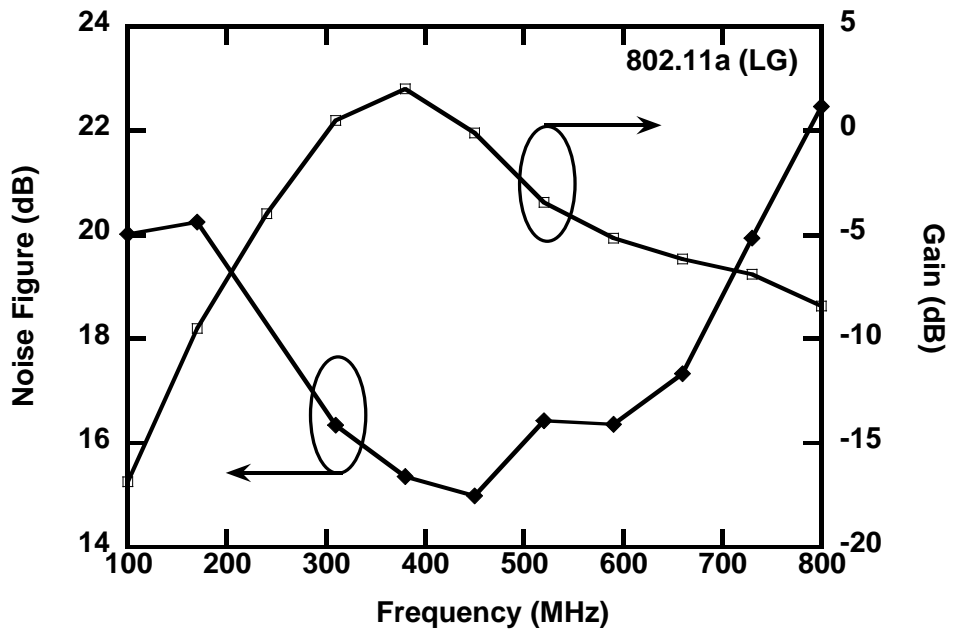


(b)

Figure 59: Conversion Gain of the Receiver Chain as a function of Frequency for the (a) 5 GHz and (b) 2.4 GHz bands. RF Power = -40 dBm, LO Power = -5 dBm and LO Frequency (into the doubler) for (a) 2.438 GHz, (b) 2.076 GHz.

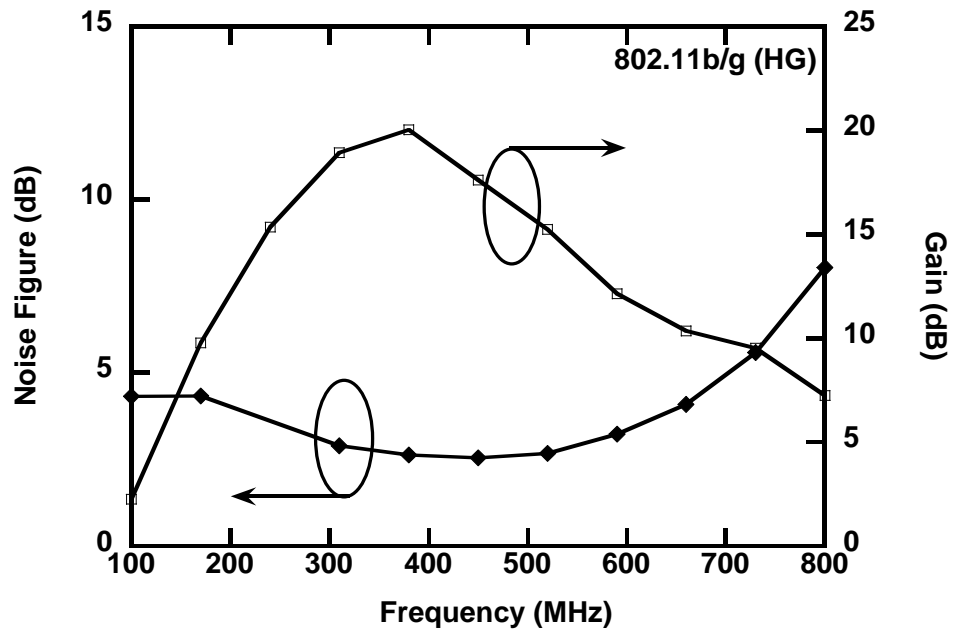


(a)

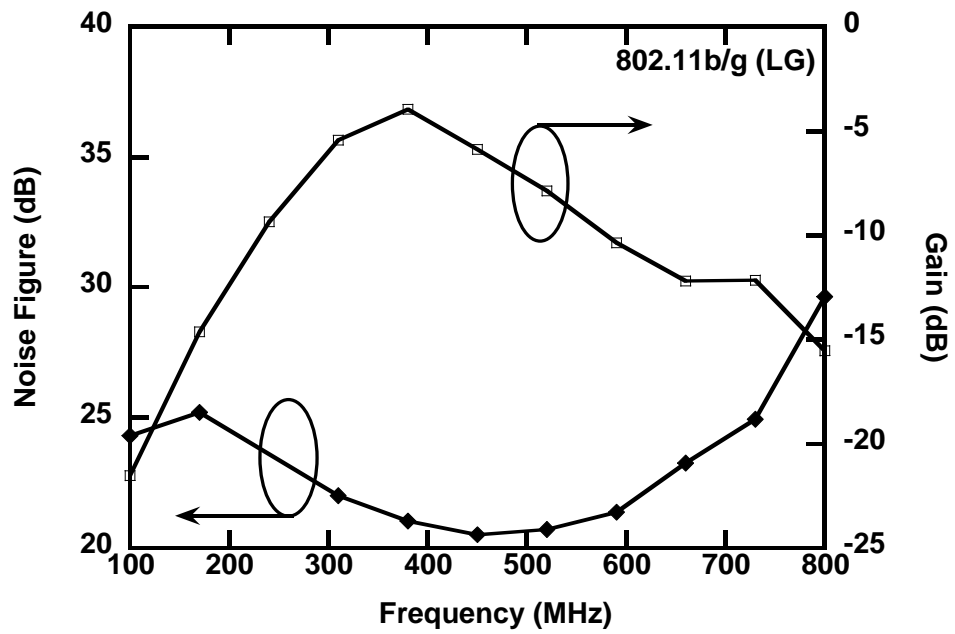


(b)

Figure 60: Noise Figure and Gain of the receiver chain for IEEE802.11a band of operation for (a) High Gain mode and (b) Low Gain mode.



(a)



(b)

Figure 61: Noise Figure and Gain of the receiver chain for IEEE802.11b/g band of operation for (a) High Gain mode and (b) Low Gain mode.

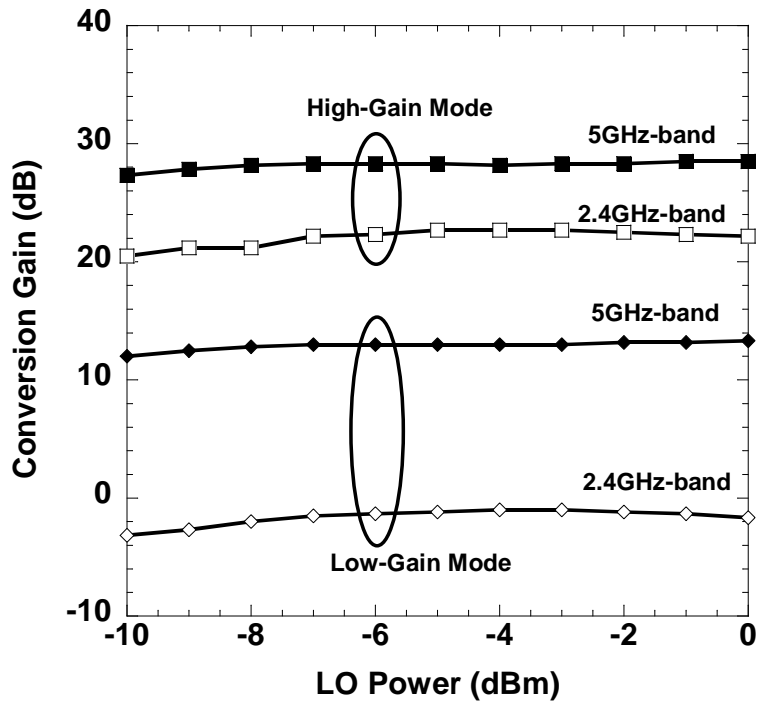


Figure 62: Conversion Gain of the Receiver Chain as a function of LO power for the 2.4 GHz and 5 GHz bands for both High and Low Gain modes of operation (IF Power = -40dBm, IF Frequency = 374 MHz).

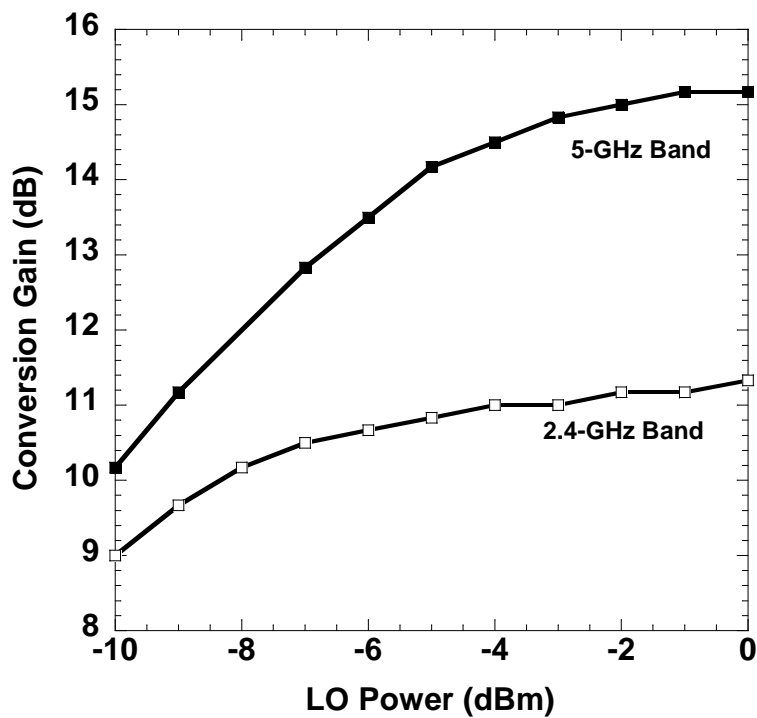
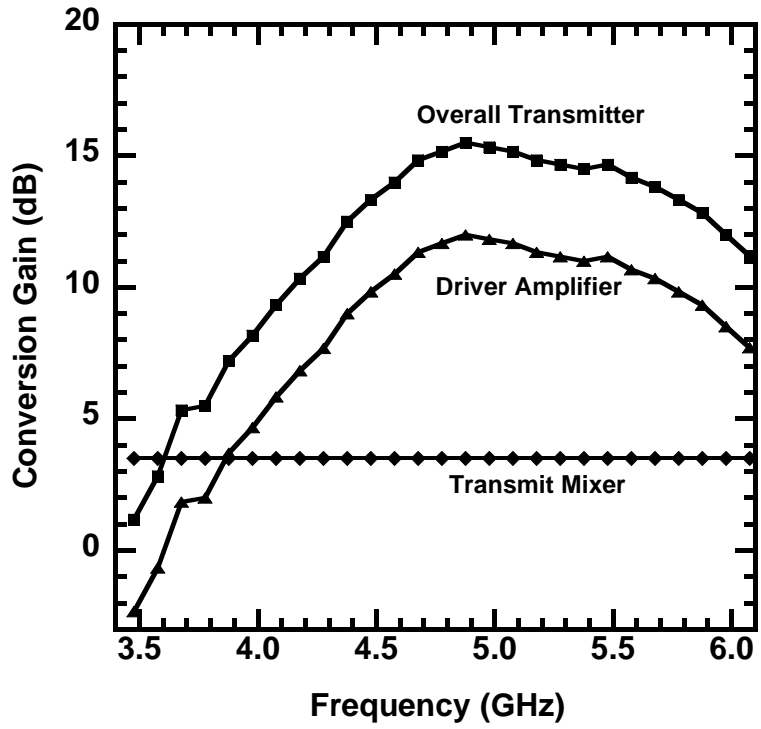
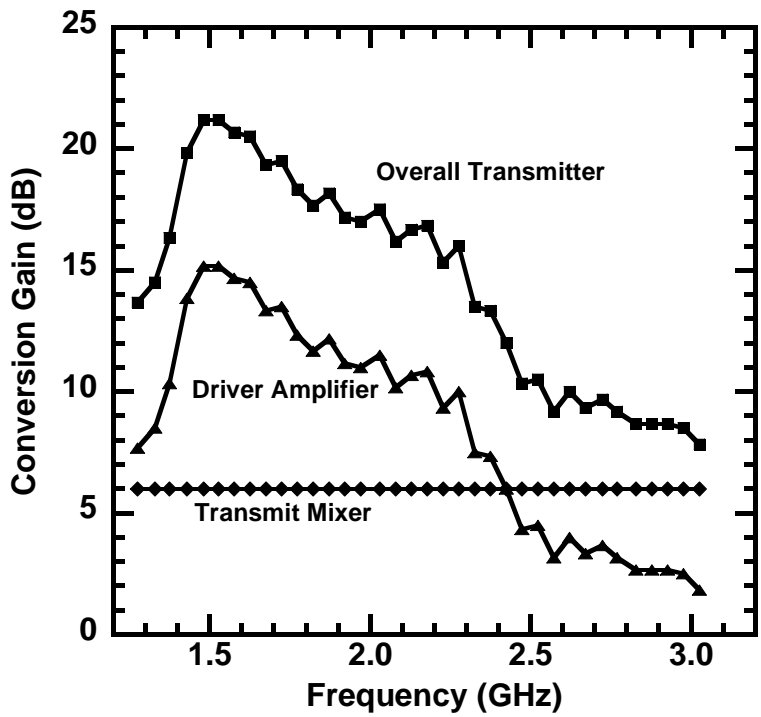


Figure 63: Conversion Gain of the Transmitter Chain as a function of LO power for the 2.4 GHz and 5 GHz bands (IF Power = -40dBm, IF Frequency = 374 MHz).



(a)



(b)

Figure 64: Conversion Gain of the Transmit Chain as a function of Frequency for the (a) 5 GHz band, (b) 2.4 GHz Band. IF Power = -40dBm, LO Power = -5 dBm and IF Frequency = 374 MHz.

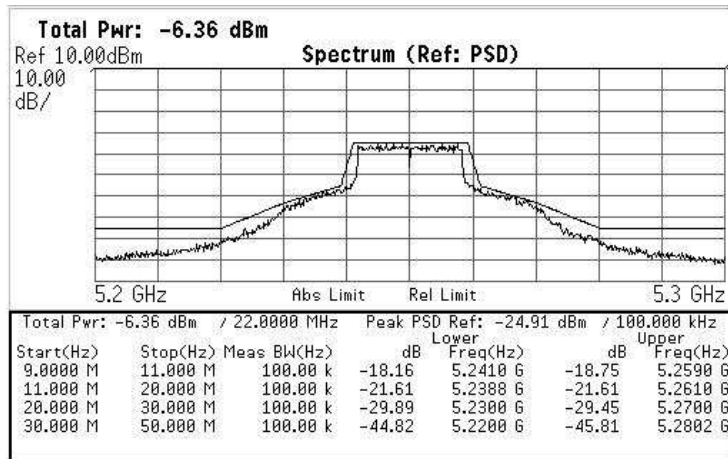


Figure 65: Transmit Spectrum Mask in the 5 GHz band (802.11a mode).

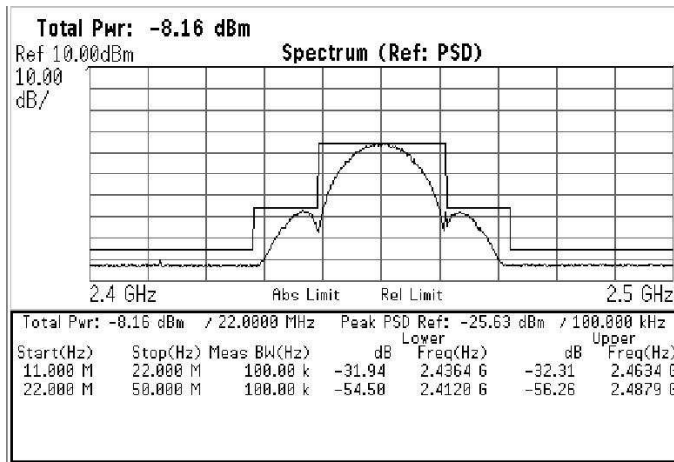


Figure 66: Transmit Spectrum Mask in the 2.4 GHz band (802.11b mode).

Table 4: Summary of the RF IC Performance - Transmit Chain

Parameters	802.11a	802.11b/g
Conversion Gain	15 dB	12 dB
Output P1dB	5 dBm	6 dBm
LO/RF Isolation	15 dB	25 dB
RF Return Loss	10 dB	10 dB
IF Return Loss	>12dB	>12 dB
LO Power	-6 dBm	-6 dBm
Current	46 mA	46 mA
Power Consumption	138 mW	138 mW

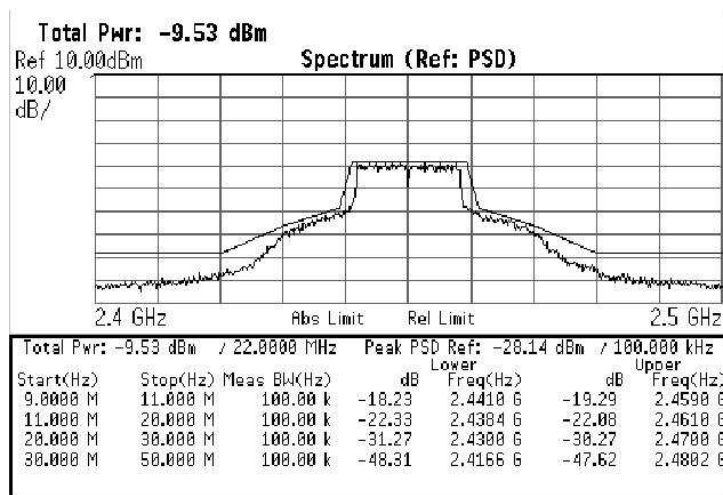


Figure 67: Transmit Spectrum Mask in the 2.4 GHz band (802.11g mode).

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

6.1 Contributions and Impact of the Dissertation

The contributions of this work can be summarized as:

1. A simple “two-port” noise theory based “transit-time” noise model has been developed for a complementary ($nnp + npn$) SiGe HBT process. A complete set of analytical equations are derived to express the four fundamental noise parameters in terms of the device parameters. The noise model is used to compare and contrast the broadband noise behavior of nnp and npn bipolar transistors.
2. A comprehensive investigation of the dc, ac and broadband noise performance of a 200 GHz peak- f_T SiGe HBT under cryogenic regimes has been performed and the performance enhancement of SiGe HBTs for extreme environment electronics has been explored. The “transit-time” based noise model is used to analyze the RF noise performance in cryogenic temperatures.
3. A sub-circuit based substrate modeling and design methodology for RF circuits, using SiGe, has been developed. The substrate parasitics provide undesirable signal feedback in the circuit causing in lowering of the gain, increase in noise and, in some cases, oscillations. These parasitics are estimated from the physical distance between the various components from the circuit layout and the electrical parameters of the substrate. The parasitics are modeled as distributed feedback circuits and the metal traces are modeled as transmission lines and

are included in circuit simulation for optimum performance. Excellent agreement between simulation and measurement is demonstrated for a test-case LNA designed for the 5 GHz band.

4. A dual-band, dual-mode transceiver is developed for IEEE 802.11a/b/g WLAN applications in a SiGe HBT process. A new architecture, using an on-chip “frequency doubler”, is developed to achieve the dual-band operation using a single off-chip frequency synthesizer for both 2.4 GHz (IEEE 802.11b/g) and 5 GHz (IEEE 802.11a) bands of operation. Gain switching was employed in the receive path to mitigate the problem of receiver power saturation in case of close proximity to the transmitter. Special attention was given to substrate parasitics which were modeled as sub-circuits in the simulations to achieve optimum performance.

Thus, the work described above, advances the state-of-the-art in the understanding and analysis of the RF performance of SiGe HBTs, by improving the RF noise modeling at room temperature which is used to explain the noise performance at cryogenic temperatures. The state-of-the-art in RF circuits in silicon is also enhanced with the development of 2.4 GHz and 5 GHz (C, X and Ku band) RF front-end circuits using a SiGe HBT technology. The work presented in the thesis has led to several publications in peer reviewed journals and conferences as listed in Appendix A.

6.2 Scope for Future Research

The work described above could be extended to various interesting and challenging directions in the future. Moving to the nano-technology regime, with minimum feature sizes less than 100 nm, has broadened the application space of silicon technologies (both SiGe and Si-CMOS) to span a gamut of emerging applications, such as the

broadband WLAN (59–64 GHz), and RF sensor systems for automotive radars. The broadband noise model developed for C, X and Ku bands (2 GHz - 20 GHz) could be extended to encompass V and W bands (50–110 GHz) which will facilitate the development of millimeter wave circuit design using state-of-the-art silicon technologies. The substrate parasitics in silicon will have a greater role to play at mm-wave frequencies, and hence need to be modeled very accurately to obtain the optimum circuit performance. Further improvement in circuit and system level design, along with robust device models at V and W bands, should be investigated.

APPENDIX A

PUBLICATIONS

1. B. Banerjee, S. Venkataraman, E. Zhao, C.-H. Lee, J. D. Cressler, J. Laskar, B. E.-Kareh, S. Balster, and H. Yasuda, "Modeling of Broadband Noise in Complementary (nnp + pnp) SiGe HBTs," being submitted to *IEEE Trans. Elect. Devices*.
2. B. Banerjee, S. Venkataraman, E. Zhao, C.-H. Lee, J. D. Cressler, J. Laskar, B. E.-Kareh, S. Balster, and H. Yasuda, "Modeling of Broadband Noise in Complementary (nnp + pnp) SiGe HBTs," in *Dig. IEEE Radio Frequency Integrated Circuits Symp.*, Long Beach, CA, USA, Jun. 2005.
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5. B. Banerjee, S. Venkataraman, Y. Lu, S. Nuttinck, D. Heo, Y.-J. E. Chen, J. D. Cressler, J. Laskar, G. Freeman and D. Ahlgren, "Cryogenic Performance of a 200 GHz SiGe HBT Technology," *Proc. IEEE Bipolar/BiCMOS Circuits and*

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 10. C.-H. Lee, B. Banerjee and J. Laskar, "A Novel DP4T Switch for Dual-band WLAN Applications," in *Proc. IEEE RFIC Symposium*, pp. 571-574, 2004.
 11. C.-H. Lee, B. Banerjee and J. Laskar, "Novel T/R Switch Architectures for MIMO Applications," in *Dig. IEEE International Microwave Symposium MTT-S*, 2004.
 12. A. Raghavan, S. Venkataraman, B. Banerjee, Y. Suh, D. Heo and J. Laskar, "Direct Extraction of an Empirical Temperature-Dependent InGaP-GaAs HBT Large-Signal Model," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1443-1450, Sep. 2003.

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