

Power Distribution in Gigascale Integration (GSI)

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By

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To My Parents

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Summary

The main objective of this thesis is to develop models for the power distribution network of high performance gigascale chips. The two main concerns in distributing power in a chip are voltage drop and electromigration-induced reliability failures. The voltage drop on the power distribution network is due to IR-drop and simultaneous switching noise. IR-drop is the voltage drop due to current passing through the resistances of the power distribution network. Simultaneous switching noise is due to varying current passing through the inductances of the power distribution network. Compact physical models are derived for the IR-drop and electromigration for different types of packages. These chip-package co-design models enable designers in the early stages of the design to estimate the on-chip interconnect resources, and also to choose type and size of the package required for power distribution.

Modeling of the simultaneous switching noise requires the simulation of a large circuit with thousands of inductances. The main obstacle challenging the simulation of a simultaneous switching noise circuit model is the computing resources required to solve the dense inductance matrix. In this work, a new *relative* inductance matrix is introduced to solve massively coupled RLC interconnects. It is proven that the analysis using this method is accurate for a wide frequency range and all configurations. Using the new inductance matrix makes the circuit simulations significantly faster without losing accuracy.

Chapter 1

Introduction and Background

1.1 Introduction

As technology advances, Gigascale Integration (GSI) chips become more power hungry, requiring higher currents in the power distribution network [1]. High current will cause larger supply noise and less reliability in the power distribution network. The tolerable supply noise by a circuit, however, decreases for future technologies because of lower supply voltages [1]. The higher supply noise and lower noise margins make the design of the power distribution network a big challenge.

An over-designed power distribution network would consume too much area and an under-designed network (if even a portion) can lead to many problems in wire routing. To have a good design for the power distribution, accurate models are needed for the power distribution network.

The two noise sources that make the supply noise are IR-drop and simultaneous switching noise. IR-drop voltage is the voltage drop in the power distribution network resulting from the current passing through the parasitic resistances of the power distribution network. Simultaneous switching noise is the result of the current change that passes through the parasitic inductance of the power distribution network. The amount of IR-drop and simultaneous switching noise that can be tolerated determines the amount of wiring resources and the number of package pins that need to be dedicated to power

distribution. Hence, designers need accurate models for IR-drop and the simultaneous switching noise to be able to design the power distribution network. These models also enable designers to predict the number of power/ground I/Os that a package should have for a target IR-drop and simultaneous switching noise.

Previously, different models have been introduced for the IR-drop voltage of an on-chip power distribution grid. In [2] a simple model is proposed for the IR-drop voltage of a flip-chip package and it is used to find the limitations imposed by the I/O pads. Another model is introduced in [3] for IR-drop voltage for a flip-chip package when the pad is connected to the grid through a single via. To be able to design the power distribution network of future chips, more accurate models are needed for the IR-drop.

Simultaneous switching noise is due to the parasitic inductances of the package and the on-chip power distribution grid. There are many tools to extract parasitic inductance of the package with good accuracy [4], [5]. However extracting the on-chip parasitic inductance of the on-chip power distribution grid is not easy. It requires knowledge of the current return paths for each segment of the power distribution. The return paths however, are not known before the circuit is simulated. This problem was solved by introducing the partial inductance method [6], [7]. The advantage of this method is that the inductance can be extracted without knowing the return paths beforehand. However, the problem is that there is mutual inductance between any two segments in the circuit. As a result the inductance matrix will be a large dense matrix, which makes the simulations of large circuits almost impossible. For example a circuit with 1000 parallel segments will have $1000^2=1000000$ mutual inductances. To simulate large circuits like the on-chip power distribution network, a technique is needed to sparsify the inductance

matrix. Unfortunately, the sparsification is not simple [8]. Different sparsification techniques have been introduced [9], [10], [11] and [12]. All of the sparsification techniques assume that the segments return paths are near and neglect mutual inductance between far segments. These techniques are suitable for modeling signal propagation at high frequencies along an interconnect, where mutual inductance between far segments are negligible. In a power distribution network the return paths are not near and therefore the mutual inductances between far segments are not negligible. Therefore these techniques are not suitable for modeling the power distribution network. A new sparsification technique is introduced to sparsify the inductance matrix without neglecting the mutual inductance of far-apart segments. This method is very general and can be used to model any system.

The other concern in designing the power distribution network is reliability which is mainly due to electromigration. Electromigration happens when the current density passing through a conductor passes a certain limit, the collision between the electrons and the metal atoms causes the atoms to migrate [13]. It not only causes open and short circuits in the power grid, but also increases the grid segment resistances, which leads to increased IR-drop and simultaneous switching noise. Electromigration might occur because of high current densities at the grid segments and the grid vias. Therefore finding the current density at the segments and vias would be key to modeling electromigration.

The other part of the chip which affects the power distribution noise is the chip substrate. It makes a parallel path for the current passing through the power distribution network. Therefore, it affects both the simultaneous switching noise and the IR-drop voltage [14], [15]. Previous models for the substrate spreading resistance are either

empirical [16], [17], [18] or are too complicated with many approximations [19], [20]. New models are introduced to extract spreading resistance of multiple contacts to the substrate.

The supply noise affects the circuits, reducing the circuit's noise margin and delay. Noise margin is defined as the maximum input noise that can be tolerated by the circuit. The supply noise however, reduces the noise margin of the circuit. The effect of the supply noise on noise margin has not been modeled. Therefore, to find the supply noise affect on the noise margin of different logic families, new models are introduced. These models can be used to model input noise and supply noise of different logic families at the same time.

Supply noise will also reduce the worst case delay of the logic gates, reducing the maximum clock frequency of a GSI chip. The delay of any logic gate depends on the discharge time of a load capacitor through series-connected MOSFETs. Therefore, to model the effect of the supply noise on delay, a model is needed for series-connected MOSFETs. This model enables the designers to find how the supply noise will affect the delay of different logic families.

Domino logic families [1] which are extensively used in high-speed GSI chips, are very sensitive to noise. They are faster than static logic families [1] and consume less space on the silicon. However, scaling requires lower threshold voltage, which results in a lower noise margin for domino logic families. Therefore, domino logic circuits have a smaller noise margin compared to static logic circuits and are more susceptible to noise for future generations. Different techniques have been introduced [21], [22] and [23] to increase their noise margin. In all of the introduced techniques, increasing the noise

margin will reduce the gate speed. Circuits introduced in [24] and [25] increase the noise margin without affecting speed, but both of them have very complex timing requirements, which makes them almost impractical to implement. A new domino logic circuit is introduced to increase the noise margin of a domino logic circuit without affecting the delay.

A big fraction of simultaneous switching noise is due to the parasitic inductances of the package bumps. Inductance is defined for a loop. Parasitic inductance for bumps is defined by the loop surrounded by the power and ground bumps. The parasitic inductance can be reduced by reducing the distance between power and ground bumps. However, the minimum distance between them is limited by technology requirements. A new coaxial structure is introduced for the chip input/outputs used for power distribution. The coaxial structure enables us to have power and ground input/outputs next to each other and as a result reduce the parasitic inductance by at least two decades.

The outline of this thesis is as follows. In Chapter 2, compact delay models are derived for the on-chip power distribution grid for wire-bond and flip-chip packages. A new relative inductance is introduced in Chapter 3 to sparsify the inductance matrix of the power distribution grid and as a result accelerate the simultaneous switching noise modeling of the power distribution grid. Models derived in Chapter 2 are used in Chapter 4 to derive current density in the on-chip power distribution grid. The current density models can then be used to derive compact models for electromigration in the segments and vias of the power distribution grid. In Chapter 5, compact models are introduced for the spreading resistance of the chip substrate. These models can be used to increase accuracy of the on-chip power distribution models. A technique is introduced in Chapter

6 to transfer supply noise to the input of a circuit and as a result model both noise sources at the same time. To be able to model supply noise effect on delay, compact delay models are introduced in Chapter 7 for series connected MOSFETs (series connected MOSFETs are used in many different logic families). A new dynamic logic family is introduced in Chapter 8 which is less sensitive to all sources of noise than other dynamic logic circuits. In Chapter 9 ultra low inductance I/O's are introduced to reduce the simultaneous switching noise due to parasitic inductance of the I/O's and finally, conclusions and future work are portrayed in Chapter 9.

1.2 IR-drop Models for the On-Chip Power Distribution Grid

The supply voltage decrease and power density increase of future GSI chips demand accurate models for the IR-drop. A partial differential equation is rigorously derived for power grid IR-drop voltage and then solved for two types of packages, the wire-bond package and the flip-chip package. In the early stages of design, these models enable accurate estimates of all required power/ground grid interconnect dimensions and chip pad counts that are needed for power distribution. The models also quantify the tradeoff between on-chip interconnect dimensions and the number of I/O pads required for power distribution and therefore enable rigorous chip/package co-design.

1.3 Relative Inductance extraction method

A new relative inductance extraction method is defined to accelerate simulation of massively coupled RLC circuits. The new relative inductance generates a sparse

inductance matrix. Therefore, it enables modeling of large circuits with reasonable speed and accuracy. It maintains accuracy for a wide frequency range and all configurations. Simulations done for a 16 bit bus with each bus line divided into 32 segments show that this relative inductance method is 20 times faster and requires 9.5 times less memory to simulate than using the established dense partial inductance matrix.

1.4 Electromigration

Using the models developed for the IR-drop, the current density in the segments and vias are modeled for two types of packages: wire-bond and flip-chip. These models enable designers in the early stages of the design to determine the places where current density in the power distribution network would be high. It helps to find the critical points and find a solution in the early stages, reducing the cost of redesign.

1.5 Substrate Model

To model the impact of the substrate on the power supply noise of digital circuits [26], [27], a model is introduced for the substrate impedance. This model can also be used to find the noise caused by digital circuits on the analogue circuits in a mixed-signal chip. Compact physical 2D and 3D models have been derived for the spreading resistance between multiple contacts as a function of the substrate doping, size of the contacts, and the distance between them. The models are derived for two different kinds of substrates. These models can be used to estimate substrate noise.

1.6 Supply Noise Effect on Noise Margin

New models are developed for effect of the supply noise on the noise margin of static and dynamic logic families. These models enable us to include IR-drop and the simultaneous switching noise in the noise margin models of the circuits.

1.7 Compact delay model for series connected MOSFETs

A compact delay model for series connected MOSFETs has been derived. This model enables accurate prediction of worst-case delay of different logic families such as dynamic logic. It also provides insight into delay change as the device parameters change. Key results show that the relative delay of series connected MOSFETs is almost invariant for different generations of technology.

1.8 New Logic Family to Increase Noise Margin without Affecting the Delay

The speed and area advantage of domino logic circuits compared to static logic circuits makes them a favorite choice for the critical path of high performance processors. However they suffer from low noise margin. Noise is not scaling at the same rate as the supply voltage therefore new domino logic circuits are required to increase the noise margin. A new domino circuit is introduced. Simulations for a 3-input 180nm AND gate shows that the noise margin can be increased by 62% with only 3% reduction in the speed.

1.9 Coaxial Polymer Pillars

An ultra-low inductance I/O interconnect, called a coaxial polymer pillar (CoPP) is introduced that is compatible with sea of polymer pillars (SoPP) recently presented [28], [29]. Polymer pillars are highly process-integrated and mechanically flexible (compliant) electrical-optical I/O interconnections that mitigate thermo-mechanical expansion mismatches. The 100× smaller parasitic inductance of the CoPP (in the range of 0.1pH) compared to the inductance of a solder bump or a regular polymer pillar makes it an excellent I/O interconnect technology for power distribution. The density of CoPP's may exceeds $10^5/\text{cm}^2$.

Chapter 2

Compact Physical IR-Drop Models for Chip/Package Co-design of the Power/Ground Interconnection Networks

2.1 Introduction

One of the main concerns in power distribution is the voltage drop on the power distribution network, which causes power supply noise and gate delay variation leading to lower performance. The voltage drop is due to IR-drop and simultaneous switching noise. IR-drop is the voltage drop due to current passing through the resistances of the power distribution network. Simultaneous switching noise is due to varying current passing through the inductances of the power distribution network.

As technology advances, the power dissipation in Gigascale Integration (GSI) chips increases, causing higher current densities in the power distribution network [1]. The higher current density leads to higher IR-drops. The tolerable IR-drop, however, decreases for future technologies because of lower supply voltages. The IR-drop problem, therefore, is becoming more serious as technology advances.

A microprocessor power distribution network typically employs a significant number of routing tracks that incorporate a large number of interconnections. Initial design and layout of the power distribution network must be done early in the design process and then gradually refined [30]. An over-designed network consumes too much area and an under-designed network (if even a portion) can lead to many problems in wire routing. Thus, if problems associated with the design and implementation of a power distribution

network go undetected early in the design cycle, they can become very costly to fix later. To reduce design costs, compact and accurate models are needed for IR-drop of the power distribution network, helping designers in the early stages of design estimate the on-chip and off-chip resources needed for power distribution.

There are different methods to distribute power on a high performance microprocessor chip. The most common one is to use a grid made of orthogonal interconnects routed on separate metal levels connected through vias [30]. Another method is to dedicate a whole metal level to power and another level to ground. It results in small on-chip power distribution parasitics and as a result small voltage drop. This technique is relatively expensive and has been reported only in the Alpha 21264 microprocessor [31].

Wire-bond and flip-chip packages are the most common type of packages used [1]. Wire-bond packages are cheaper than flip-chip packages; however, the wire-bond package suffers from higher voltage drops in the power distribution network due to higher parasitics. In a wire-bond package, power and ground are distributed from the surrounding of the package resulting in a high parasitic to the center of the chip. In a flip-chip the voltage drop is reduced by spreading the package pads along the surface of the chip and, therefore reducing the power distribution network parasitics.

The parasitic resistance of the power distribution network consists of two parts: the parasitic resistance of the power distribution network on the package and the parasitic resistance of the on-chip power distribution network. The package resistances are however negligible compared to the resistances of the on-chip power distribution network, and therefore the IR-drop is mainly due to voltage drop of the on-chip power distribution network.

Previously, different IR-drop models have been introduced. In [2] a very simple IR-drop model with limited accuracy is introduced for a flip-chip package to predict the number of pads required for future generations of technology.

In this section compact physical IR-drop models are introduced for two generic types of packages, the wire-bond and the flip-chip package. These models are very general and can be used for many kinds of chips and packages.

In Section 2.2 a partial differential equation is derived for the voltage drop of a grid. The partial differential equation is solved to derive an IR-drop model for a wire-bond package in Section 2.3. In Section 2.4, IR-drop is modeled for a flip-chip package regardless of the shape of the pads. The pads are modeled in Section 2.5, and then used to find the maximum IR-drop of a flip-chip package. The general IR-drop of flip-chip packages is modeled for different cases in Section 2.6. In Section 2.7, IR-drop for future cost performance processors is predicted based on the ITRS [1]. The tradeoffs between on-chip power distribution and the package parameters are studied in Section 2.8. Section 2.9 shows the trade off between the size and number of pads used for power distribution, and finally in Section 2.10, the optimum placement is found for the pads to get minimum IR-drop.

2.2 Partial Differential Equation for the IR-Drop of a Power Distribution Grid

The most common way to distribute power in a GSI chip is to distribute it through an on-chip grid made of orthogonal segments (Figure 2-1). The horizontal and vertical segments of a grid are routed at different metal levels and are connected through vias at the crossing points. The metal levels making the grid might have different thicknesses resulting in an *anisotropic* grid with different resistances in x and y directions. There are thousands of parallel vias in a grid, and therefore the voltage drops on the vias are negligible.

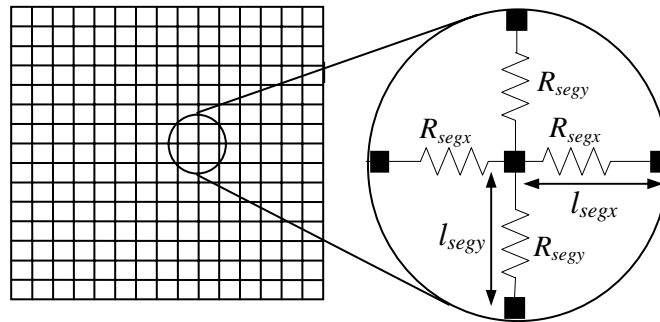


Figure 2-1: Power Distribution grid on the chip. The horizontal and vertical segments of a grid are routed at different metal levels and are connected through vias at the crossing points.

The number of segments of the grid is usually large; therefore, the power distribution grid can be modeled as a continuous planar surface which distributes power across the chip. Each node of the power distribution grid is connected to the four neighboring nodes as shown in Figure 2-2. A current source is placed at each node equal to the amount of current distributed to the chip by that node. The IR-drop of a node on the grid is the

voltage difference between that node and the voltage at the chip pad. The IR-drop of a point on the grid can be calculated from the IR-drop of the four neighboring points as

$$\begin{aligned} \frac{V_{IR}(x, y) - V_{IR}(x + \Delta x, y)}{R_{sx} \frac{\Delta x}{\Delta y}} + \frac{V_{IR}(x, y) - V_{IR}(x, y + \Delta y)}{R_{sy} \frac{\Delta y}{\Delta x}} + \frac{V_{IR}(x, y) - V_{IR}(x - \Delta x, y)}{R_{sx} \frac{\Delta x}{\Delta y}} \\ + \frac{V_{IR}(x, y) - V_{IR}(x, y - \Delta y)}{R_{sy} \frac{\Delta y}{\Delta x}} = -J_0 \cdot \Delta x \cdot \Delta y \quad , \end{aligned} \quad (2.1)$$

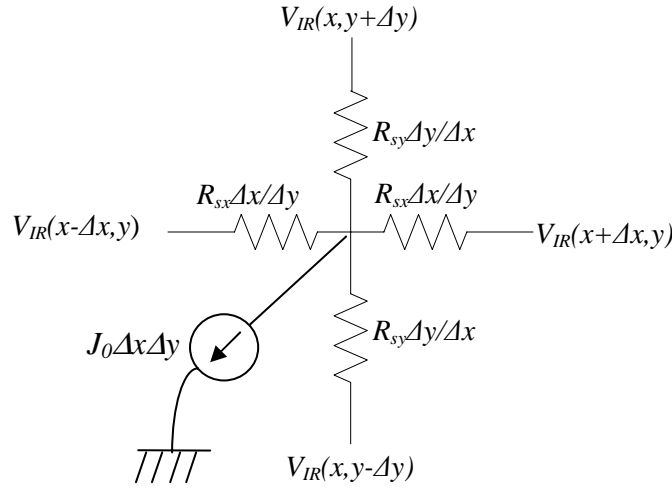


Figure 2-2: Differential model for a node in the grid.

where $V_{IR}(x, y)$ is the IR-drop of a point at (x, y) on the power/ground grid, J_0 is current per unit area distributed to the circuits by the grid, and R_{sx} and R_{sy} are the sheet resistances (Ohm units) in x and y directions respectively. The sheet resistances can be calculated from the segment resistances as:

$$R_{sx} = R_{segx} \times \frac{l_{segx}}{l_{segx}} = \frac{\rho}{T_x} \frac{l_{segx}}{W_x} \times \frac{l_{segx}}{l_{segx}} = \frac{\rho}{T_x} \frac{l_{segx}}{W_x}, \quad (2.2)$$

and

$$R_{sy} = R_{segy} \times \frac{l_{segx}}{l_{segy}} = \frac{\rho}{T_y} \frac{l_{segy}}{W_y} \times \frac{l_{segx}}{l_{segy}} = \frac{\rho}{T_y} \frac{l_{segx}}{W_y}, \quad (2.3)$$

where l_{segx} and l_{segy} are the length of the segments in x and y directions respectively, R_{segx} and R_{segy} are the segment resistances in x and y directions (Ω) (Figure 2-1), W_x and W_y are the widths of the segments in x and y directions, T_x and T_y are the thicknesses of the segments in x and y directions, and ρ is the resistivity of the grid metal. Replacing each of the neighboring voltages in (2.1) with their Taylor series and *assuming that the grid is a continuous planar surface*, Equation (2.1) can be simplified as

$$\frac{1}{R_{sx}} \frac{\partial^2 V_{IR}(x, y)}{\partial x^2} + \frac{1}{R_{sy}} \frac{\partial^2 V_{IR}(x, y)}{\partial y^2} = J_0. \quad (2.4)$$

The IR-drop for different packages can be calculated by applying the appropriate boundary conditions to equation (2.4). For an *isotropic* grid, where the resistances in x and y directions are equal ($R_{sx}=R_{sy}=R_s$), Equation (2.4) can be simplified as

$$\nabla^2 V_{IR}(x, y) = R_s J_0, \quad (2.5)$$

called the Poisson equation.

In a GSI chip power is distributed through parallel grids on multiple levels of metal [30]. The total sheet resistances in x and y directions for a chip with multiple grids are equal to

$$R_{sxTot}^{-1} = R_{sx1}^{-1} + R_{sx2}^{-1} + \dots + R_{sxn}^{-1}, \quad (2.6)$$

and

$$R_{syTot}^{-1} = R_{sy1}^{-1} + R_{sy2}^{-1} + \dots + R_{syn}^{-1}, \quad (2.7)$$

where $R_{sx1}, R_{sx2}, \dots, R_{sxn}$ are the sheet resistances in the x direction of grids 1,2,...,n, and $R_{sy1}, R_{sy2}, \dots, R_{syn}$ are the sheet resistances in the y direction of grids 1,2,...,n. Equation

(2.4) can be used for the IR-drop calculation by replacing the sheet resistances in x and y directions (R_{sx} and R_{sy}) with the total sheet resistances in x and y directions. (R_{sxTot} and R_{syTot}).

In the following sections the boundary conditions defined by two types of packages, the wire-bond and the flip-chip package, are derived and then used to solve Equation (2.4) to model IR-drop.

2.3 IR-Drop of an Anisotropic Grid with a Wire-Bond Technology Package

Wire-bond packages are an inexpensive packaging solution. In this kind of package, the package to chip connections surround the die (Figure 2-3) [32]. Multiple power/ground pins are used to distribute power/ground to the chip. These power/ground pins are connected with wire-bonds to a power/ground ring surrounding the die ((Figure 2-3) [32]. This power/ground ring is connected to the on-chip power/ground grid, which distributes power across the chip. The ring is made wide to reduce the voltage drop along it. Hence, IR-drop is negligible within the power/ground ring, resulting in the constant voltage boundary condition shown in Figure 2-4.

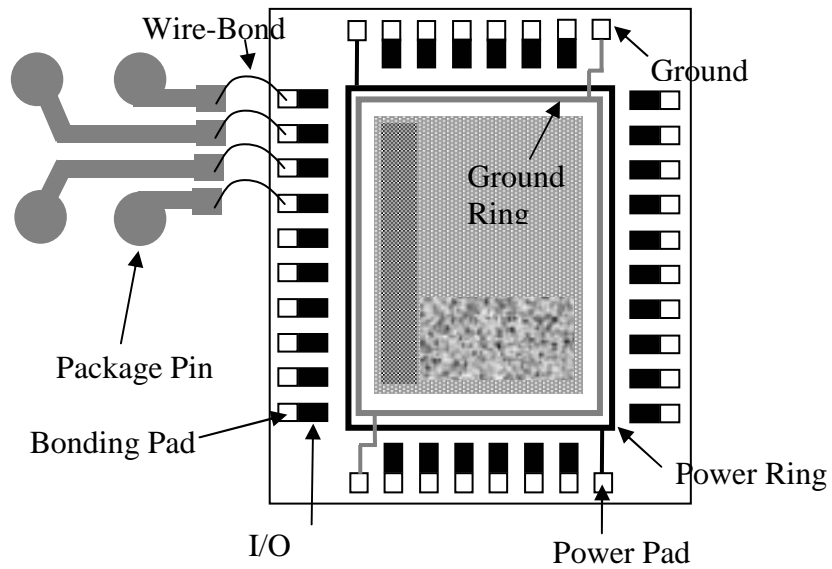


Figure 2-3: Wire-bond package. The power/ground pins are connected with wire-bonds to a power/ground ring surrounding the die. The power/ground ring is connected to the on-chip power/ground grid, which distributes power across the chip.

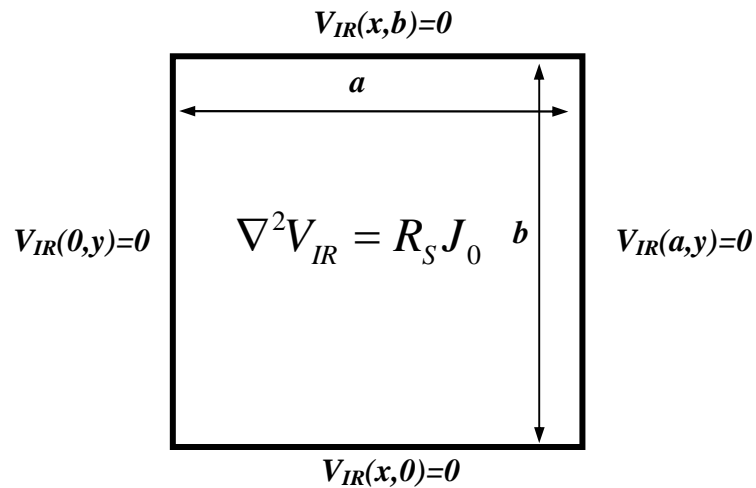


Figure 2-4: Boundary condition for wire-bond package with a power ring. IR-drop is negligible within the power/ground ring, resulting in the constant voltage boundary condition.

In this section the IR-drop is modeled for an anisotropic grid. Therefore, Equation (2.4) should be solved with the boundary condition shown in Figure 2-4. The general solution of Equation (2.4) with the boundary condition shown in Figure 2-4 is

$$V(x, y) = \sum_{n=1}^{\infty} \sum_{m=1}^{\infty} E_{mn} \sin\left(\frac{m\pi}{a}x\right) \sin\left(\frac{n\pi}{b}y\right), \quad (2.8)$$

where a and b are the lengths of the sides of the ring, and E_{mn} is a coefficient which depends on the current distribution across the chip. This voltage drop should satisfy the Poisson equation

$$\sum_{n=1}^{\infty} \sum_{m=1}^{\infty} -E_{mn} \left[\frac{1}{R_{sx}} \left(\frac{m\pi}{a}\right)^2 + \frac{1}{R_{sy}} \left(\frac{n\pi}{b}\right)^2 \right] \sin\left(\frac{m\pi}{a}x\right) \sin\left(\frac{n\pi}{b}y\right) = J_0 \quad (2.9)$$

E_{mn} can be solved from the double Fourier series.

$$E_{mn} = \frac{-4}{ab\lambda_{mn}} \int_0^b \int_0^a J_0 \sin\left(\frac{m\pi}{a}x\right) \sin\left(\frac{n\pi}{b}y\right) dx dy \quad (2.10)$$

where λ_{mn} is

$$\lambda_{mn} = \left[\frac{1}{R_{sx}} \left(\frac{m\pi}{a}\right)^2 + \frac{1}{R_{sy}} \left(\frac{n\pi}{b}\right)^2 \right] \quad (2.11)$$

Solving E_{mn} and placing it in (2.8) results in

$$V_{IR}(x, y) = \frac{16J_0}{\pi^4} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\sin\left((2k+1)\frac{\pi}{a}x\right) \sin\left((2l+1)\frac{\pi}{b}y\right)}{(2k+1)(2l+1) \left(\frac{(2k+1)^2}{R_{sx}a^2} + \frac{(2l+1)^2}{R_{sy}b^2} \right)}. \quad (2.12)$$

Equation (2.12) is the IR-drop between a point on an anisotropic power/ground grid and the power/ground ring for a wire-bond package (Figure 2-5). Substituting R_{segx} and R_{segy} from (2.2) and (2.3) into (2.12) we have

$$V_{IR}(x, y) = \frac{16J_0}{\pi^4} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\sin\left((2k+1)\frac{\pi}{a}x\right) \sin\left((2l+1)\frac{\pi}{b}y\right)}{(2k+1)(2l+1) \left(\frac{l_{segx}^2 (2k+1)^2}{R_{segx} l_{segx} a^2} + \frac{l_{segy}^2 (2l+1)^2}{R_{segy} l_{segx} b^2} \right)} \quad (2.13)$$

or

$$V_{IR}(x, y) = \frac{16J_0\rho}{\pi^4} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\sin\left((2k+1)\frac{\pi}{a}x\right) \sin\left((2l+1)\frac{\pi}{b}y\right)}{(2k+1)(2l+1) \left(\frac{T_x W_x (2k+1)^2}{a^2 l_{segy}} + \frac{T_y W_y (2l+1)^2}{b^2 l_{segx}} \right)}. \quad (2.14)$$

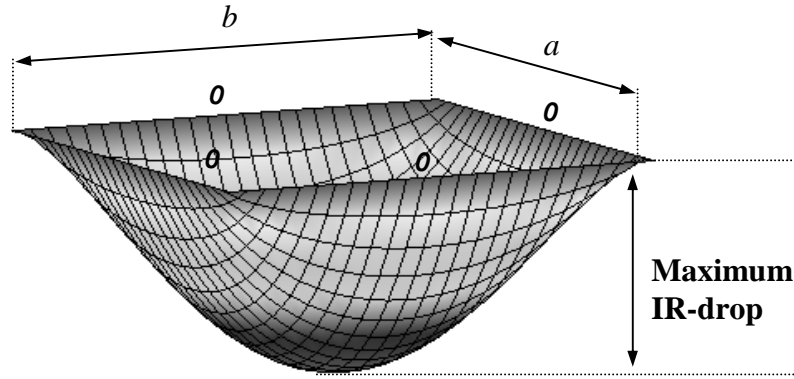


Figure 2-5: IR-drop of the wire-bond package. The maximum voltage drop is at the center of the chip.

This equation gives physical insight into tradeoffs among power grid dimensions T_x , T_y , W_x , W_y , l_{segx} , and l_{segy} , and chip dimensions a and b . Figure 2-5 shows the IR-drop of a wire-bond chip using equation (2.14). For a uniform current distribution, the maximum voltage drop is at the center of the chip as shown in Figure 2-5, and therefore can be calculated from

$$V_{IR\max} = V_{IR} \left(x = \frac{a}{2}, y = \frac{b}{2} \right). \quad (2.15)$$

For square die ($a=b$) with an isotropic grid ($R_{sx}=R_{sy}=R_s$), the maximum IR-drop can be simplified and is equal to

$$V_{IR\max} = 0.0736 \cdot R_s \cdot J_0 \cdot a^2 = 0.0736 \cdot \rho \frac{l_{seg} J_0 a^2}{WT}, \quad (2.16)$$

or

$$V_{IR\max} = 0.0736 \cdot \rho \frac{l_{seg} I_{Total}}{WT}, \quad (2.17)$$

where I_{Total} is the total chip current. SPICE simulations for different grids show that the results (2.16) have less than 1% error.

2.4 IR-Drop of an Isotropic Grid in a Flip-Chip Package

In a flip-chip package, the package I/O's are connected to the chip I/O's through metal bumps distributed across the chip surface (Figure 2-6). These bumps are connected to I/O pads that can be in different shapes, located at the top metal levels. The flip-chip package is more expensive than a wire-bond package. However, the flip-chip package has smaller I/O parasitics. The distributed pads also result in lower power distribution parasitics on-chip and consequently lower voltage drop.

Power distribution for a high performance microprocessor requires many pads. Almost two-thirds of the total pads are used for power distribution [1]. These power and ground pads are spread throughout the surface of the chip to reduce voltage drop.

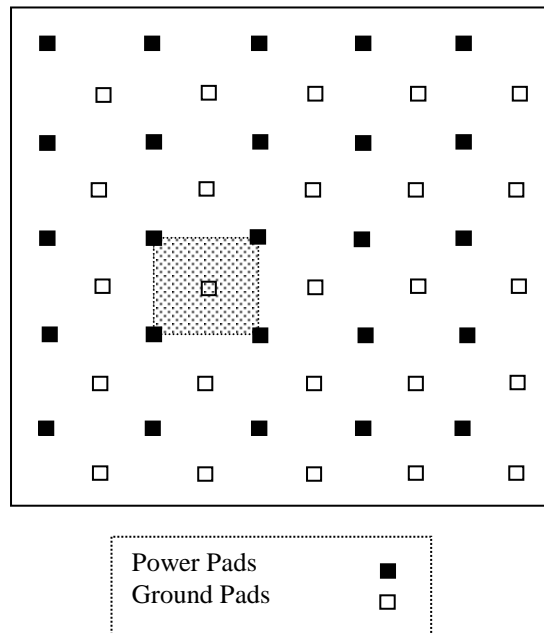


Figure 2-6: Power and ground pads for a flip-chip package are distributed across the chip surface to reduce IR-drop and simultaneous switching noise.

The chip is composed of macrocells such as an ALU, clock circuits, cache, etc. The power grid IR-drop is calculated for each macrocell. The current density within each macrocell is assumed to be uniform; therefore the IR-drop distribution is the same for the area surrounded by four neighboring pads called a *cell* (shown shaded in Figure 2-6). Hence, the partial differential equation needs to be solved only for one cell. A single cell is shown in detail in Figure 2-7. Because of the uniform current density in a macrocell no current passes through the cell borders, resulting in the boundary condition shown in Figure 2-8(a). Figure 2-8(b) shows the simplified boundary condition assuming a pad size of zero dimensions. This boundary condition is solved in this section and then the effect of pad size and shape are added to the models in Section 2.5.

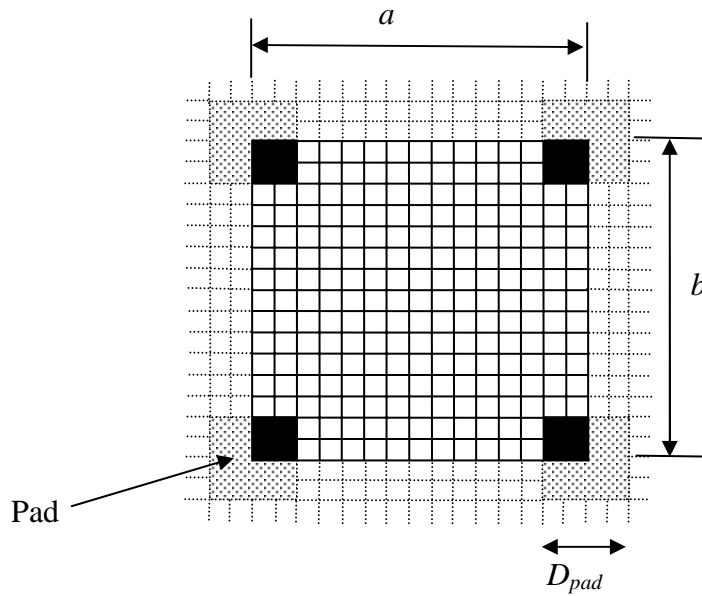


Figure 2-7: Grid between four neighboring pads. This area is called a cell.

The Poisson equation with the boundary condition shown in Figure 2-8(b) can be divided into two partial differential equations with boundary conditions shown in Figure 2-9. To find the IR-drop, each partial differential equation with its boundary condition (Figure 2-9) should be solved. The IR-drop is calculated from

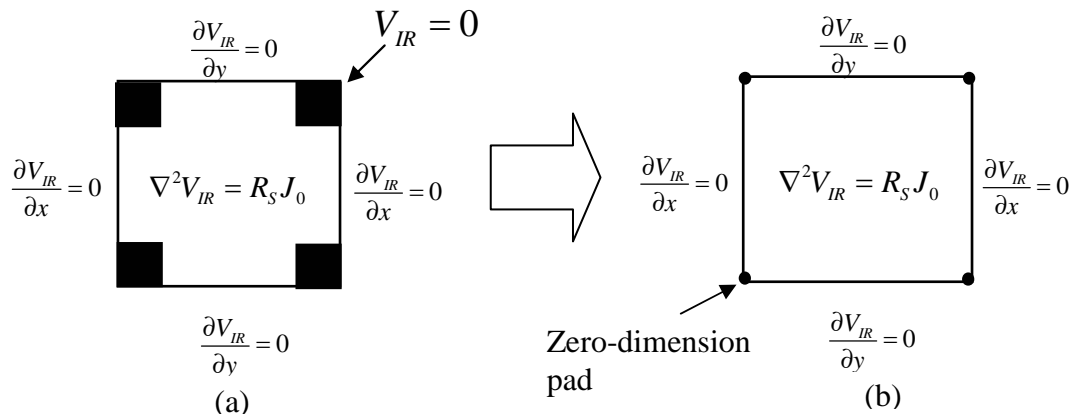


Figure 2-8: Boundary condition for each region surrounded by four pads. a) Boundary condition for a cell. b) Boundary condition for a cell assuming a pad radius of zero.

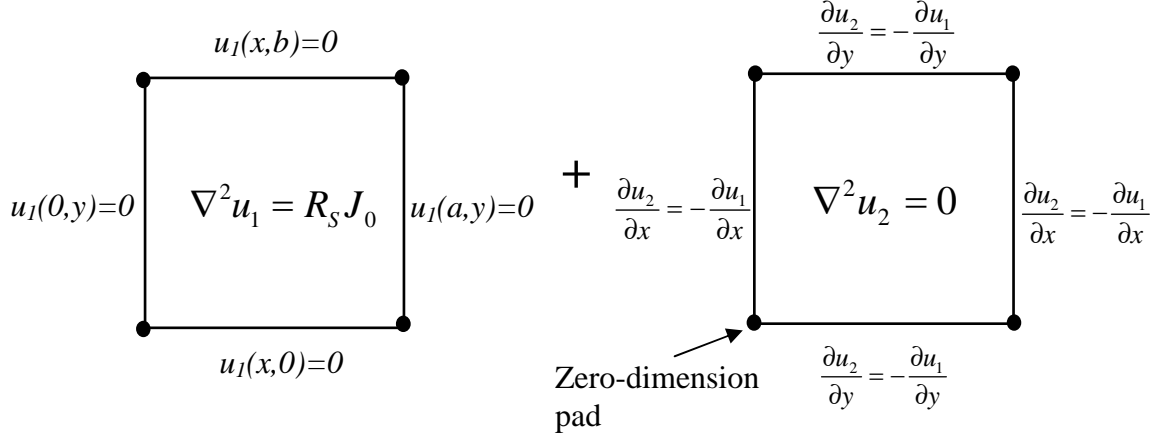


Figure 2-9: Partial differential equations with boundary conditions for IR-drop of a flip-chip package can be divided into two partial differential equations with boundary conditions.

$$V_{IR}(x, y) = u_1(x, y) + u_2(x, y), \quad (2.18)$$

$u_1(x, y)$ is the solution to the Poisson equation (2.5) with zero boundary conditions and $u_2(x, y)$ is the solution of the Laplace equation with the boundary conditions shown in Figure 2-9.

$u_1(x, y)$ was solved in (2.12). Assuming $R_{sx}=R_{sy}=R_s$ and $a=b$, we have:

$$u_1(x, y) = -\frac{16 \cdot R_s \cdot J_0 \cdot a^2}{\pi^4} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\sin\left(\frac{(2k+1) \cdot \pi \cdot x}{a}\right) \sin\left(\frac{(2l+1) \cdot \pi \cdot y}{a}\right)}{(2k+1)(2l+1)((2k+1)^2 + (2l+1)^2)} \quad (2.19)$$

The boundary condition for $u_2(x, y)$ is calculated by differentiating u_1 at the boundary

$$\left. \frac{\partial u_1(x, y)}{\partial x} \right|_{x=0} = -\frac{16 \cdot R_s \cdot J_0 \cdot a}{\pi^3} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\sin\left(\frac{(2l+1) \cdot \pi \cdot y}{a}\right)}{(2l+1)((2k+1)^2 + (2l+1)^2)}, \quad (2.20)$$

or

$$\left. \frac{\partial u_1(x, y)}{\partial x} \right|_{x=0} = R_s \cdot J_0 \cdot a \cdot \sum_{l=0}^{\infty} \left[\lambda_l \sin \left(\frac{(2l+1)}{a} \cdot \pi \cdot y \right) \right], \quad (2.21)$$

where λ_l is

$$\lambda_l = -\frac{16}{\pi^3} \sum_{k=0}^{\infty} \frac{1}{(2l+1) \left((2k+1)^2 + (2l+1)^2 \right)}. \quad (2.22)$$

To find $u_2(x, y)$, the coefficients (A_n, B_n, C_n, D_n) in the general solution

$$u_2(x, y) = R_s J_0 \sum_{n=1}^{\infty} A_n \cos \left(\frac{n\pi}{a} x \right) \cosh \left(\frac{n\pi}{a} (a-y) \right) + R_s J_0 \sum_{n=1}^{\infty} B_n \cos \left(\frac{n\pi}{a} x \right) \cosh \left(\frac{n\pi}{a} y \right) + R_s J_0 \sum_{n=1}^{\infty} C_n \cos \left(\frac{n\pi}{a} y \right) \cosh \left(\frac{n\pi}{a} (a-x) \right) + R_s J_0 \sum_{n=1}^{\infty} D_n \cos \left(\frac{n\pi}{a} y \right) \cosh \left(\frac{n\pi}{a} x \right) \quad (2.23)$$

of the Laplace differential equation ($u_2(x, y)$ in Figure 2-9) should be calculated.

The four boundary conditions at the sides are the same therefore $u_2(x, y)$ can be simplified

as

$$u_2(x, y) = R_s J_0 \sum_{n=1}^{\infty} A_n \left[\begin{aligned} &\cos \left(\frac{n\pi}{a} x \right) \cosh \left(\frac{n\pi}{a} (a-y) \right) + \cos \left(\frac{n\pi}{a} x \right) \cosh \left(\frac{n\pi}{a} y \right) + \\ &+ \cos \left(\frac{n\pi}{a} y \right) \cosh \left(\frac{n\pi}{a} (a-x) \right) + \cos \left(\frac{n\pi}{a} y \right) \cosh \left(\frac{n\pi}{a} x \right) \end{aligned} \right] \quad (2.24)$$

Finding the slope at the boundary we have

$$\left. \frac{\partial u_2(x, y)}{\partial x} \right|_{x=0} = -R_s J_0 \sum_{n=1}^{\infty} A_n n\pi \sinh(n\pi) \cos(n\pi y). \quad (2.25)$$

The boundary condition is (Figure 2-9)

$$\left. \frac{\partial u_1(x, y)}{\partial x} \right|_{x=0} = -\left. \frac{\partial u_2(x, y)}{\partial x} \right|_{x=0}. \quad (2.26)$$

We have

$$R_s J_0 \sum_{l=0}^{\infty} \left(\lambda_l \sin(2l+1)\pi \cdot y \right) = -R_s J_0 \sum_{n=1}^{\infty} A_n n\pi \sinh(n\pi) \cos(n\pi y). \quad (2.27)$$

A_n can be calculated from the definition of the Fourier cosine series. However, the problem is that the left side of equation (2.27) has a DC value but the right side of the equation (2.27) is a Fourier cosine series with a zero DC value ($n \neq 0$). To solve this problem a function is defined as Figure 2-10. This function has a DC value between zero and one, but can be expanded as a Fourier cosine series. Therefore A_n can be divided into two parts

$$A_n = E_n + F_n \quad 0 < n < \infty, \quad (2.28)$$

where E_n 's are the Fourier cosine series coefficients assuming there is a no DC value ($1 \leq n < \infty$), and F_n 's are the Fourier cosine series coefficients for the DC value (Fourier cosine series of Figure 2-10).

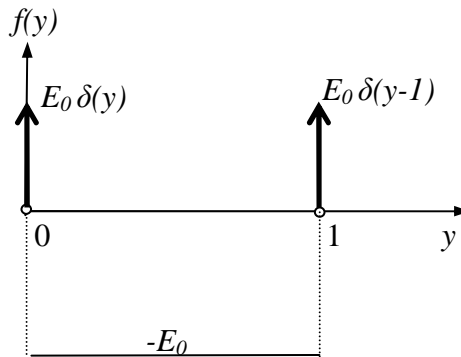


Figure 2-10: This function has a dc value of E_0 from 0 to 1 and can be expanded as a Fourier cosine series. $\delta(y)$ is a impulse function.

We start with E_n . From the definition of the Cosine Fourier Series we have

$$E_n = \frac{2}{n\pi \sinh(n\pi)} \int_0^1 f(y) \cos(n\pi y) dy, \quad (2.29)$$

and

$$E_0 = \frac{1}{n\pi \sinh(n\pi)} \int_0^1 f(y) dy, \quad (2.30)$$

or

$$E_n = \frac{2}{n\pi \sinh(n\pi)} \int_0^1 \left[\sum_{l=0}^{\infty} (\lambda_l \sin(2l+1)\pi \cdot y) \cos(n\pi y) \right] dy. \quad (2.31)$$

We know that

$$\int_0^{\pi} \sin(ax) \cos(bx) dx = \begin{cases} \frac{2a}{a^2 - b^2} & a - b \text{ odd} \\ 0 & a - b \text{ even} \end{cases}, \quad (2.32)$$

or

$$\int_0^1 \sin(a\pi x) \cos(b\pi x) dx = \begin{cases} \frac{2a}{\pi(a^2 - b^2)} & a - b \text{ odd} \\ 0 & a - b \text{ even} \end{cases}. \quad (2.33)$$

Therefore, from (2.31) and (2.33), we have

$$E_n = \frac{2}{n\pi \sinh(n\pi)} \sum_{l=0}^{\infty} \left(\lambda_l \left(\int_0^1 \sin((2l+1)\pi \cdot y) \cos(n\pi y) \cdot dy \right) \right). \quad (2.34)$$

which results in

$$E_n = \begin{cases} \frac{2}{n\pi^2 \sinh(n\pi)} \sum_{l=0}^{\infty} \left(\frac{\lambda_l 2(2l+1)}{(2l+1)^2 - n^2} \right) & \text{for } n \text{ even} \\ 0 & \text{for } n \text{ odd} \end{cases}, \quad (2.35)$$

and

$$E_0 = \frac{-2}{\pi} \sum_{l=0}^{\infty} \left(\frac{\lambda_l}{(2l+1)} \right). \quad (2.36)$$

F_n 's are the coefficients of a Fourier cosine series for the function shown in Figure 2-10

$$E_0 - E_0\delta(y) - E_0\delta(y-1) = -\sum_{n=1}^{\infty} F_n n\pi \sinh(n\pi) \cos(n\pi y). \quad (2.37)$$

F_n can be calculated from the definition of the Fourier cosine series as

$$F_n = \frac{2}{n\pi \sinh(n\pi)} \int_0^1 \left[(E_0\delta(y) + E_0\delta(y-1) - E_0) \cos(n\pi y) \right] dy, \quad (2.38)$$

and

$$F_n = \frac{2E_0}{n\pi \sinh(n\pi)}. \quad (2.39)$$

Placing (2.35) and (2.39) in (2.28)

$$A_n = \frac{4}{n\pi^2 \sinh(n\pi)} \sum_{l=0}^{\infty} \left(\frac{\lambda_l (2l+1)}{(2l+1)^2 - n^2} \right) - \frac{2E_0}{n\pi \sinh(n\pi)}, \quad (2.40)$$

or

$$A_n = \frac{4}{n\pi^2 \sinh(n\pi)} \sum_{l=0}^{\infty} \left(\lambda_l \left(\frac{(2l+1)}{(2l+1)^2 - n^2} + \frac{1}{2l+1} \right) \right). \quad (2.41)$$

From (2.18), (2.19), (2.22), (2.24), (2.41) the total result is equal to:

$$u_1(x, y) = -\frac{16 \cdot R_s \cdot J_0 \cdot a^2}{\pi^4} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\sin\left(\frac{(2k+1) \cdot \pi \cdot x}{a}\right) \sin\left(\frac{(2l+1) \cdot \pi \cdot y}{a}\right)}{(2k+1)(2l+1)\left((2k+1)^2 + (2l+1)^2\right)}, \quad (2.42)$$

$$u_2(x, y) = R_s J_0 \sum_{n=1}^{\infty} \left[A_n \left(\cos\left(\frac{n\pi}{a} x\right) \cosh\left(\frac{n\pi}{a}(a-y)\right) + \cos\left(\frac{n\pi}{a} x\right) \cosh\left(\frac{n\pi}{a} y\right) + \right. \right. \\ \left. \left. + \cos\left(\frac{n\pi}{a} y\right) \cosh\left(\frac{n\pi}{a}(a-x)\right) + \cos\left(\frac{n\pi}{a} y\right) \cosh\left(\frac{n\pi}{a} x\right) \right) \right], \quad (2.43)$$

$$A_n = \frac{4}{n\pi^2 \sinh(n\pi)} \sum_{l=0}^{\infty} \left(\lambda_l \left(\frac{(2l+1)}{(2l+1)^2 - n^2} + \frac{1}{2l+1} \right) \right), \quad (2.44)$$

$$\lambda_l = -\frac{16}{\pi^3} \sum_{k=0}^{\infty} \frac{1}{(2l+1)\left((2k+1)^2 + (2l+1)^2\right)}, \quad (2.45)$$

$$V(x, y) = u_1(x, y) + u_2(x, y). \quad (2.46)$$

Equations (2.42)-(2.46) are the general IR-drop solution independent of the number of segments. In this model, it is assumed that zero dimension pads are connected to the continuous planar surface (grid) at the corners of the cell. This will result in infinite voltage drops at the corners. In the following section the effect of pad shape and size on the IR-drop models (2.42)-(2.46) are considered to calculate the maximum IR-drop.

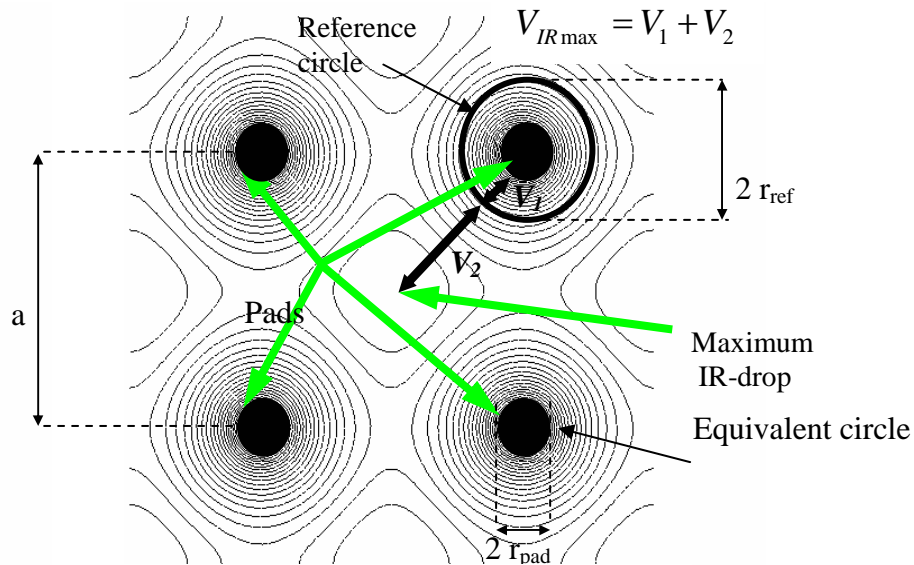


Figure 2-11: The IR-drop contour for a cell with zero dimension pads at the corners.

2.5 IR-Drop of an Isotropic Grid in a Flip-Chip Package

The pads can be in different shapes. In this section IR-drop is calculated for two shapes of pads, round pads and square pads.

The IR-drop contour for a cell with zero dimension pads at the corners is shown in Figure 2-11. The voltage contours near the zero dimension pads are circular. The voltage drop increases toward the center of the chip, where the maximum voltage drop happens (Figure 2-12). If circle pads with the same size as one of the circle contours are placed at the corners of this cell, it will result in the same voltage contour in the cell. For each pad shape and size an equivalent pad radius can be calculated which results in the same IR-drop. The maximum IR-drop is the voltage drop between the center of the cell and the equivalent circular voltage contour (Figure 2-11). This equivalent circular pad has the

same resistance to the continuous grid as the pad does. The equivalent pad radius for different pad shapes is calculated in Appendix I and is of the form

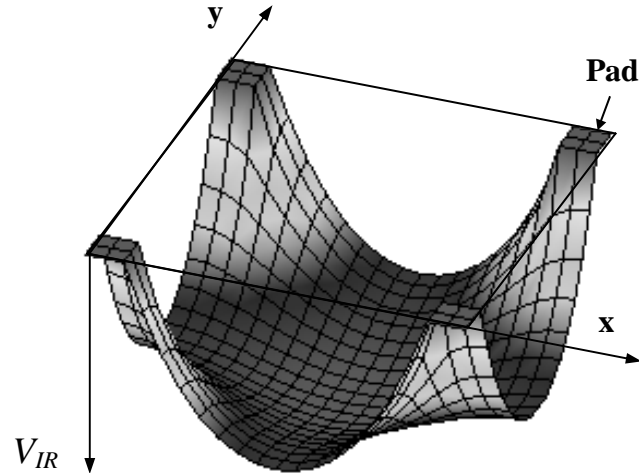


Figure 2-12: IR-drop on the grid of in a flip-chip package. The voltage drop increases toward the center of the chip, where the maximum voltage drop happens.

$$r_{pad} = \alpha D_{pad}, \quad (2.47)$$

where α is a function of the pad shape and D_{pad} is the pad dimension (Table 2-1).

Table 2-1. Pad shape parameter.

Kind of pad	α
Circular pad	0.5
Square pad	0.5903
The pad is connected to a single pad in the grid	0.2

The voltage contours are circular around the pad and they change shape as the distance to the pad is increased (Figure 2-11). The voltage contours at the center of the cell are not a function of the pad shape and radius. If a reference circle is selected between the equivalent circle and the center of the cell (e.g. $r_{ref} = \frac{a}{20}$) (Figure 2-11), then the maximum IR-drop is divided into two parts: the voltage drop (V_1) from the equivalent circle (r_{pad}) to the reference circle (r_{ref}) and the voltage drop (V_2) from the reference circle (r_{ref}) to the center of the cell (Figure 2-11)

$$V_{IR \max} = V_1 + V_2. \quad (2.48)$$

The voltage contours are circular between the equivalent circle (r_{pad}) and the reference circle (r_{ref}). Therefore the voltage drop from the equivalent circle to the reference circle can be calculated from

$$V_1 = \frac{R_{seg}}{2\pi} \int_{r_{pad}}^{r_{ref}} \frac{I_1}{r} \cdot dr, \quad (2.49)$$

where r is the distance to the center of the pad, and I_1 is the current distributed by the grid in a circle of radius r . I_1 is equal to

$$I_1 = I_{pad} \left(1 - \frac{\pi r^2}{A_{cell}} \right), \quad (2.50)$$

where I_{pad} is the current distributed by the pad, and A_{cell} is the cell area. Replacing I_1 in (2.49) with (2.50), we have

$$V_1 = \frac{R_{seg} I_{pad}}{2\pi} \int_{r_{pad}}^{r_{ref}} \left(1 - \frac{\pi r^2}{A_{cell}} \right) \frac{1}{r} dr = \frac{R_{seg} I_{pad}}{2\pi} \ln \left(\frac{r_{ref}}{r_{pad}} \right) - \frac{R_{seg} I_{pad}}{4A_{cell}} (r_{ref}^2 - r_{pad}^2). \quad (2.51)$$

where r_{ref} and r_{pad} are the reference and the pad radii respectively. The radius of the reference circle is assumed to be

$$r_{ref} = \frac{a}{20}, \quad (2.52)$$

where a is the distance between two neighboring pads. Replacing the parameters in (2.51) by their equivalents (2.47) and (2.52) results in

$$V_1 = \frac{R_s I_{pad}}{2\pi} \ln \left(\frac{a}{20 \alpha D_{pad}} \right) - \frac{R_s I_{pad}}{400} \left(\frac{1}{4} - \frac{100 \alpha^2 D_{pad}^2}{a^2} \right). \quad (2.53)$$

The voltage drop from the reference circle to the center of the chip is not a function of the pad shape and size and can be calculated from equations (2.42)-(2.46). Simplifying results in

$$V_2 = 0.326 \cdot R_s \cdot I_{pad}. \quad (2.54)$$

Replacing V_1 and V_2 in (2.48) with (2.53) and (2.54), and simplifying the results we have

$$V_{IRmax} = \frac{R_s I_{pad}}{2\pi} \ln \left(\frac{0.387 a}{\alpha \cdot D_{pad}} \right). \quad (2.55)$$

This equation gives the maximum IR-drop on the power/ground grid from the pad voltage for a flip-chip package as a function of on-chip and package parameters. SPICE simulations show that the results using (2.55) and have less than 5% error.

2.6 IR-Drop of an Anisotropic Grid in a Flip-Chip Package with Rectangular Cells

This case is the most general case for the IR-drop of a flip-chip package, which includes an anisotropic grid with rectangular cells. The voltage drop on an anisotropic grid (different resistances in x and y directions) is calculated by applying the boundary

conditions determined by the package to Equation (2.4). This equation can be simplified to a Poisson equation by simple change of variables:

$$x_1 = \sqrt{R_{sx}} x, \quad (2.56)$$

and

$$y_1 = \sqrt{R_{sy}} y. \quad (2.57)$$

Applying (2.56) and (2.57) to Equation (2.4) we have

$$\frac{\partial^2 V_{IR}(x_1, y_1)}{\partial x_1^2} + \frac{\partial^2 V_{IR}(x_1, y_1)}{\partial y_1^2} = J_0 \sqrt{R_{sx} R_{sy}} \quad (2.58)$$

or

$$\nabla^2 V_{IR}(x_1, y_1) = J_0 \sqrt{R_{sx} R_{sy}}, \quad (2.59)$$

which is the same Poisson equation (2.5). The change of variables shown in (2.56) and (2.57) is applied to the boundary condition shown in Figure 2-8. The new boundary condition is shown in Figure 2-13. The radius of the equivalent circle for the pad having the same resistance to the grid is [33]

$$r_{pad} = 0.5 \alpha \left(\sqrt{R_{sx}} + \sqrt{R_{sy}} \right) \times D_{pad}, \quad (2.60)$$

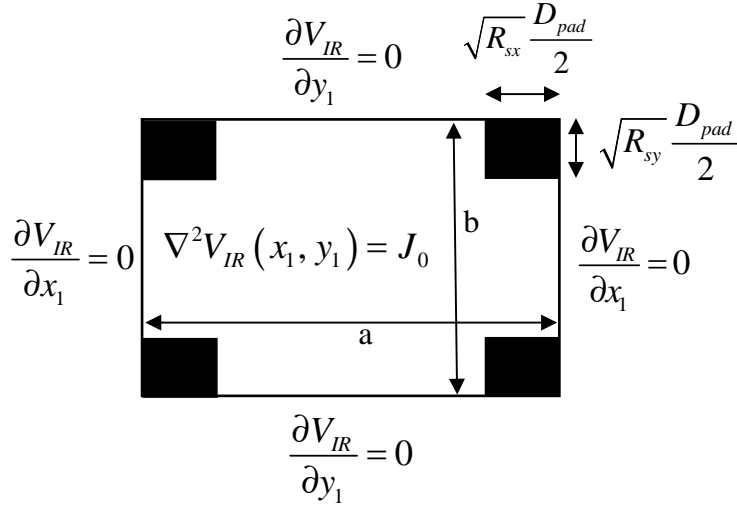


Figure 2-13: Boundary condition for a grid in a rectangular cells with change of variables.

where α depends on the shape of the pad (TABLE 1). The equivalent radius of the reference is [33]

$$r_{ref} = 0.025 \left(a\sqrt{R_{sx}} + b\sqrt{R_{sy}} \right). \quad (2.61)$$

Using the same definitions for V_1 and V_2 used in Section 2.5, and simplifying the results we have

$$V_{IR \max} = \frac{\sqrt{R_{sx} R_{sy}} I_{pad}}{2\pi} \ln \left(\frac{0.387 \left(a\sqrt{R_{sx}} + b\sqrt{R_{sy}} \right)}{\alpha \cdot D_{pad} \left(\sqrt{R_{sx}} + \sqrt{R_{sy}} \right)} \right). \quad (2.62)$$

Substituting R_{segx} and R_{segy} from (2.2) and (2.3) into (2.62) we have

$$V_{IR \max} = \frac{\rho I_{Total}}{2\pi n_{pg}} \sqrt{\frac{l_{segx} l_{segy}}{T_x T_y W_x W_y}} \ln \left(\frac{0.387 \left(b\sqrt{T_x W_x l_{segx}} + a\sqrt{T_y W_y l_{segy}} \right)}{\alpha \cdot D_{pad} \left(\sqrt{T_x W_x l_{segx}} + \sqrt{T_y W_y l_{segy}} \right)} \right), \quad (2.63)$$

where, I_{Total} is the total macrocell current and n_{pg} is the number of power/ground pads in a macrocell. This equation is the fundamental equation for chip-package co-design of the

power distribution network. It quantifies the tradeoff between the power grid parameters (l_{segx} , l_{segy} , T_x , T_y , W_x , W_y) and pad parameters such as: pad shape and size (α , D_{pad}), number of pads (n_{pg}), and distance between pads (a,b).

2.7 IR-Drop for Future Cost-Performance Processors

The models derived for the maximum IR-drop (2.63), can be used to predict IR-drop for different generations of technology. In this section the maximum IR-drop is derived for a cost-performance processor with a flip-chip package for different generations of technology based on ITRS [1]. The maximum IR-drop that can be tolerated by a cost performance processor is decreasing due to smaller supply voltages of future generations. Figure 2-14 shows the maximum IR-drop that a circuit can tolerate for different generations. It also shows IR-drop for different generations of technology calculated using (2.63) for a cost performance processor. The IR-drop is calculated for a cost-performance processor with two global levels and two semi-global levels used for the power distribution grid. There are three signal wires between each power/ground (Figure 2-14). As shown the IR-drop increases due to higher current densities in the power distribution network. The curve also shows that the IR-drop gets larger than the maximum tolerable in 2009, and as a result the IR-drop should be reduced by either increasing the number or size of pads or increasing the grid metal used for power distribution.

In the following section the tradeoff between package parameters and the on-chip metal used for power distribution are studied.

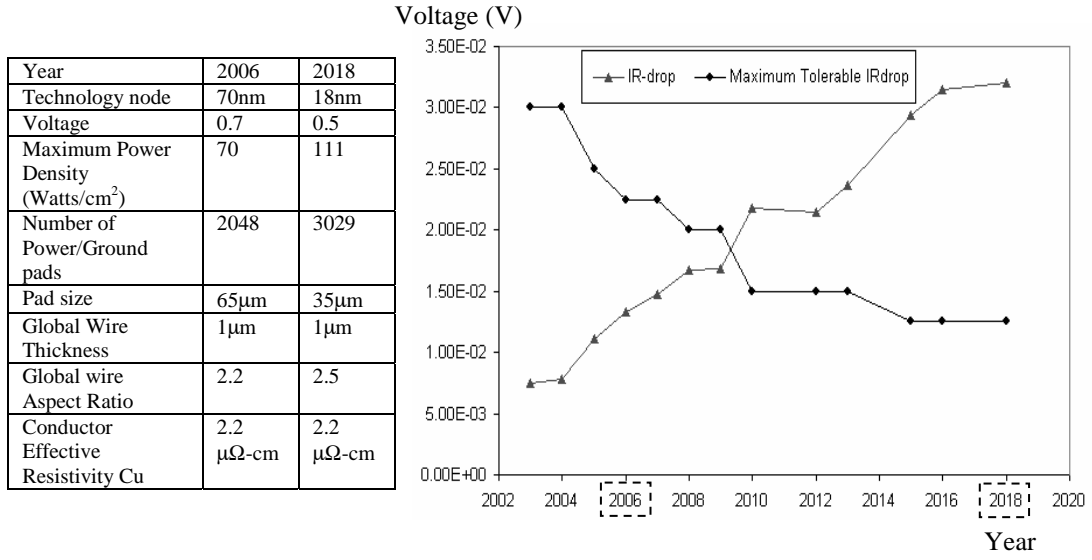


Figure 2-14: (a) IR-drop for different generations of technology for a cost performance processor based on ITRS 2003 [1]. The tables show the parameters used to estimate IR-drop for the years 2006 and 2018 based on ITRS 2003 [1].

2.8 Tradeoff between the Number of Pads and Area Percentage of Top Metal Layers Used for Power Distribution

The IR-drop of a flip-chip package (2.62) can be rewritten as a function of the total macrocell current distributed by the pads

$$V_{IR \max} = \frac{\sqrt{R_{segx} R_{segy}} I_{total}}{2\pi n_{pg}} \ln \left(\frac{0.387 (a \cdot l_{segy} \sqrt{R_{segx}} + b \cdot l_{segx} \sqrt{R_{segy}})}{\alpha \cdot D_{pad} (l_{segy} \sqrt{R_{segx}} + l_{segx} \sqrt{R_{segy}})} \right), \quad (2.64)$$

where n_{pg} is the number of power or ground pads in the macrocell. The model shows tradeoff between the on-chip power distribution network (described by R_{segx} , R_{segy} , l_{segx} , l_{segy}) and package parameters (described by D_{pad} , n_{pg} and α). Figure 2-15 shows this tradeoff for a microprocessor in 2018. As shown in the figure increasing the pad size (D_{pad}) or the number of pads (n_{pg}) reduces the percentage area of the top metal layer used for power distribution.

Another trade off is between size and number of pads which is studied in the following section.

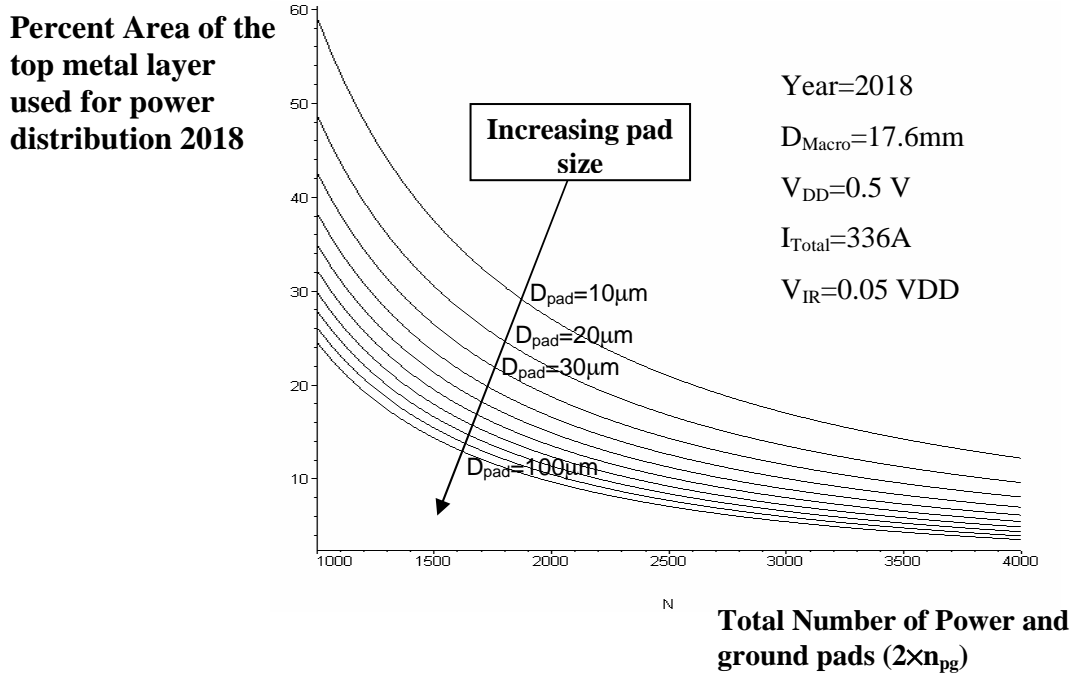


Figure 2-15: Tradeoff between the Number of Pads and Area Percentage of Top Metal Layers Used for Power Distribution for different pad sizes.

2.9 Size and Number of Pads Tradeoff

There is a tradeoff between pad size and the number of pads. The question we want to address in this section is: “Assuming a certain area for the total pads, is it better to have a large number of small pads or small number of large pads to minimize the IR-drop?”

The modeling is done for an isotropic grid with square pads; however, it can be extended to other cases too. Area of a single square pad is

$$A_{pad} = D_{pad}^2 \cdot \quad (2.65)$$

Therefore the total pad area which is assumed to be constant is

$$A_{Tpad} = n_{pg} D_{pad}^2, \quad (2.66)$$

where n_{pg} is the number of power and ground pads in the macrocell. Assuming a constant total pad area, Equation (2.55) can be rewritten as

$$V_{IR\max} = \frac{R_s \cdot I_{Total} \cdot D_{pad}^2}{2\pi \cdot A_{Tpad}} \ln \left(\frac{0.387 \cdot D_{Macro}}{\alpha \sqrt{A_{Tpad}}} \right), \quad (2.67)$$

or

$$V_{IR\max} = \frac{\rho l_{seg} I_{Total} D_{pad}^2}{2\pi W T A_{Tpad}} \ln \left(\frac{0.387 \cdot D_{Macro}}{\alpha \sqrt{A_{Tpad}}} \right). \quad (2.68)$$

All of the parameters in this equation are constant except for D_{pad} . This equation suggests reducing D_{pad} in order to reduce $V_{IR\max}$. In other words the IR-drop is minimized by using a large number of small pads instead of a small number of large pads.

2.10 Optimum Placement of the Power and Ground Pads for an Anisotropic Grid for Minimum IR-Drop

Placement of the power and ground pads is important in reducing the IR-drop. In this section the optimum placement of the power and ground pads will be derived assuming a certain number of power and ground pads. The total number of pads dedicated to power and ground for a macrocell is assumed to be constant resulting in a constant cell area.

$$a \cdot b = A_{Cell}, \quad (2.69)$$

where a and b are the size of the cell in x and y directions and A_{Cell} is the cell area which is constant. We want to find a and b so that the IR-drop is minimized for an anisotropic

grid. In this case, the only variables are a and b , therefore, the maximum IR-drop can be written as

$$V_{IR\max} = K_1 \ln \left(K_2 \left(a\sqrt{R_{sx}} + b\sqrt{R_{sy}} \right) \right). \quad (2.70)$$

where K_1 and K_2 are two constants. The minimum IR-drop happens when we have

$$a = b \sqrt{\frac{R_{sy}}{R_{sx}}}. \quad (2.71)$$

This result suggests making a rectangular cell to minimize the IR-drop in an anisotropic grid. For an isotropic grid ($R_{sx}=R_{sy}$) the cells should be square to minimize the IR-drop.

2.11 Conclusion

Compact physical IR-drop models are derived for the power distribution network of high performance microprocessors. These models help designers in the early stages of the design to estimate accurately the on-chip and package resources which need to be dedicated to power distribution, reducing the cost of over-design. On-chip power is distributed through a grid made of vertical and horizontal interconnects at different metal levels. The IR-drop model of the on-chip power distribution grid is derived for the wire-bond and the flip-chip packages. The models are used to predict IR-drop for future generations of microprocessors. They show the trade off between the on-chip interconnects parameters (segment length, width and thickness) and the package parameters (shape, number and size of pads). The models suggest using a large number of small pads for power distribution instead of a small number of large pads to reduce the IR-drop. The optimum placement of these pads is also derived to minimize the IR-drop.

In this chapter compact models were introduced for IR-drop. Simulating IR-drop on chip can easily be done by a circuit simulator such as SPICE. However circuit model for simultaneous switching noise results in massively coupled RLC circuit. In the next chapter a new inductance is defined called relative inductance. This new inductance will accelerate simulations of massively coupled RLC circuits and as a result enables us to simulate simultaneous switching noise.

Chapter 3

Relative Inductance

3.1 Introduction

As the on-chip wavelength becomes comparable with the length of global interconnects, inductance effects become important for many clock, signal and power interconnects. To model an interconnect, it is first divided into small segments along the length of the interconnect. The length of each segment should be selected so that it is shorter than the length of the wavelength of the highest frequency of interest. For each segment, inductance resistance and capacitance is extracted. Since inductance is defined for a loop, the current loop should be known in order to calculate inductance. On the other hand, to find the current loop, the inductance should be known. To solve this dilemma, partial inductance was [34], [35] defined for each segment of a conductor assuming that its return path is at infinity (Figure 3-1) and was proved to generate correct results. Using this method, the inductance can be extracted for each segment without prior knowledge of the current loops.

The extracted partial inductances can be used with extracted capacitance and resistance of the interconnect to form a distributed RLC which is called Partial Equivalent Element Circuit method (PEEC)[36]. To use this model for higher frequencies the skin effect and the proximity effect in the interconnect should also be modeled. The skin effect and the proximity effect in an interconnect can be modeled by dividing the

interconnect segment into a bundle of filaments [37], where each filament carries a constant current (Figure 3-2). For each filament the partial inductance and parasitic resistance are extracted and at the end of filaments of each segment are connected to the parasitic capacitances.

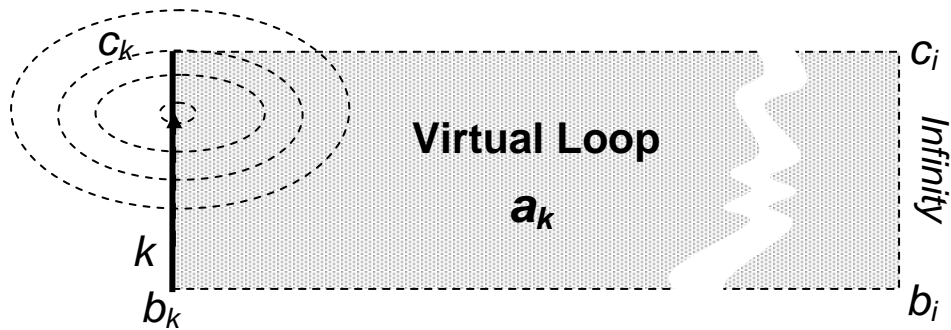


Figure 3-1: Artificial virtual loop defined in the partial inductance method. Self partial inductance is determined by the magnetic flux passing through the virtual loop ($b_k c_k c_i b_i$) of a filament when unit current is passing through the filament (k).

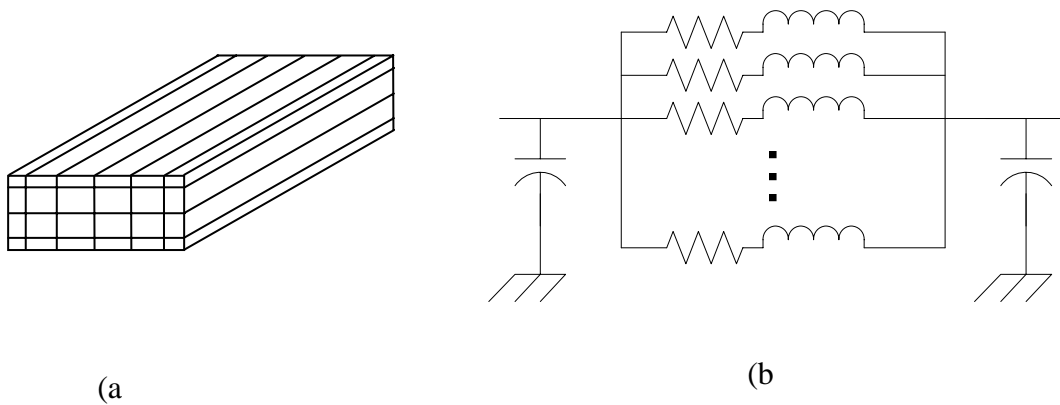


Figure 3-2: Model of an interconnect segment. a) The wire segment is divided into parallel filaments. b) For each filament the parasitic resistance and inductance is extracted. The equivalent capacitances are added at the end of the segment model.

One of the main advantages of using the PEEC method is that the extracted equivalent circuit can be simulated in a circuit simulator with nonlinear devices such as transistors in time domain. The partial inductance method, however, generates a very dense inductance matrix (large number of mutual inductances) because there is a considerable coupling between even very far filaments [7], [8]. Number of couplings in this method is of the order of $O(N^2)$ with N being the number of filaments. Manipulating such large and dense matrices is infeasible for a gigascale chip due to impractical time and memory requirements for the circuit simulator.

There have been two approaches to accelerate the circuit simulations. In the first approach the inductance and capacitance is extracted and then acceleration is done by generating reduced order models via moment matching techniques [38], [39], [40] and [41]. In the second approach the inductance matrix is sparsified and therefore can be directly used in a circuit simulator to accelerate simulations. To sparsify the inductance matrix various methods [42], [43], [44], [45] and [46] have been proposed, each of which assumes that there are only inductance couplings between filaments within a certain radius (window) of the filament. If the return path of a segment is near the segment the flux made by the segment is canceled by the flux made by its return path at a far distance from the segment (Figure 3-3). Therefore, the mutual inductances between far segments are negligible for a circuit where the return paths are near. For a signal wire, the return paths at high frequencies are near the signal wire, and therefore mutual inductances between far segments are negligible. Hence, the windowing methods ([42]-[46]) which neglect mutual inductance between far segments can be used to model signal wires.

However, if the design is such that there is far inductance coupling (return path is not near), then a new sparsification technique is needed.

Figure 3-4 shows the power and ground pads used for power distribution. The grids connected to the power and ground pads are not shown in Figure 3-4. Power is distributed from the power pads through the grid to the circuit and returns through the ground grid to the ground pad. The arrows in Figure 3-4 show the current directions, from the power pads to the ground pads. Figure 3-5 shows a power and a ground pad in more detail. In this figure part of the power and ground grids distributing power to the gates are shown. As shown the current directions in the power and ground grids are in the same direction. Therefore, the mutual inductance between far segments is not negligible due to near return paths (Figure 3-3) and there is considerable mutual inductance between even far segments. Hence, the windowing methods ([42]-[46]) which neglect mutual inductance between far segments can not be used to model the on-chip power distribution network.

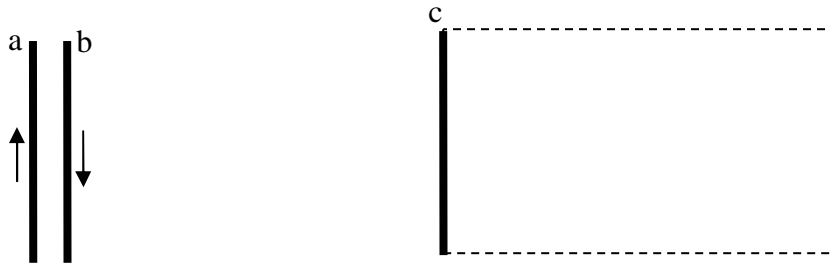


Figure 3-3. The return path of segment *a* is segment *b* which is near. Segment *c* is far from segments *a* and *b*. The flux passing through the virtual loop of segment *c* due to segment *a* is canceled by the flux made by segment *b*. Therefore, the mutual inductance between far segments can be neglected when the return paths are near the segments.

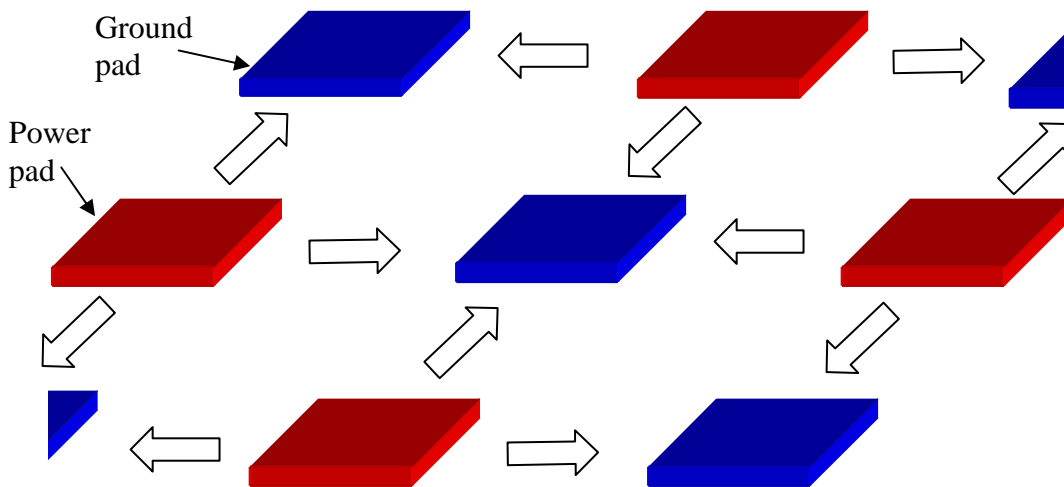


Figure 3-4. The power and ground pads for a flip-chip package are shown. The grids connected to the power and ground pads are not shown. Power is distributed from the power pads through the grid to the circuit and returns through the ground grid to the ground pad.

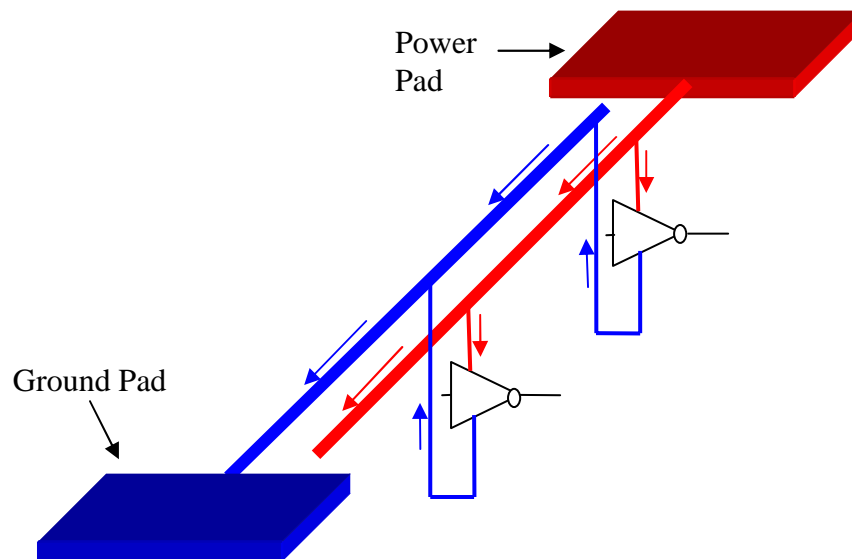


Figure 3-5. This figure shows two neighboring pads, part of the grid and two gates connected to the power and ground pads. As shown the direction of current in the segments of the power and ground grids are in the same direction and the return path is not through the neighboring segment.

The distribution of return current of a signal wire is always such that the overall impedance is minimized. Hence, at low frequencies, where the impedance is largely

determined by resistance of the lines, return current spreads among many power and ground lines. Therefore, the previous methods [42]-[46], which assume that return current is within a window, underestimate the low frequency inductance and are not accurate for low frequencies.

The hierarchical method of parasitic extraction has been used extensively to accelerate (in FastCap and FastHenry) the extraction of parasitic capacitances or inductances (multipole acceleration methods) [47], [48], [49]. FastCap is a tool to extract capacitance and FastHenry is a tool to extract inductance and resistance. Although being very powerful methods, they can not be used to accelerate the simulations of RLC circuits. The first step to implement a hierarchical inductance which can be used in circuit simulators to simulate RLC circuits was taken in [50]. In this method the mutual inductances between far filaments are modeled through calculating average group mutual inductances, assuming equal currents (Zeroth order wavelet current) in conductors in each group. This simple assumption will introduce error in the simulations of far mutual inductance couplings.

A new hierarchical inductance extraction method (*relative inductance*) is introduced, in which relative inductance of a filament is calculated relative to some arbitrary virtual return path. It has been demonstrated that this new inductance matrix is equivalent to the conventional partial inductance matrix and is accurate for a large frequency range and all configurations. It, however, is considerably sparser (total number of couplings for the entire interconnect system is $O(N)$), and solving interconnect problems using this matrix is hence much faster and requires less memory.

In Section 3.2, the partial inductance method and sparsification techniques are briefly discussed. The new relative inductance is introduced in Section 3.3, wherein it is proven to be equivalent to the partial inductance method. In Section 3.4, it is shown that the relative inductance can be calculated for 3D structures. In Section 3.5, it is illustrated that most of the elements of the new matrix are so small that they can be truncated for a certain accuracy. In Section 3.6, the new approach is applied to a 16-bit bus and the results are compared with the partial inductance method. The new approach is also applied to a power distribution network.

3.2 Partial Inductance Models

Partial inductance [35] is defined for each conductor filament and does not depend on its return path. For each filament (k), an artificial virtual loop is defined between the filament and infinity (Figure 3-1). The partial self inductance is determined by the magnetic flux passing through the virtual loop of a filament when unit current is passing through the filament (k)

$$L_{P(k,k)} = \frac{1}{I_k} \int_{a_k} B_{k,k} \cdot da_k . \quad (3.1)$$

The partial mutual inductance between two filaments is defined as the magnetic flux linkage between one filament (m) and the virtual loop of the other filament (k) when unit current is passing through m (Figure 3-6). Partial mutual inductance between two filaments k and m can be calculated from [35]

$$L_{P(k,m)} = \frac{1}{I_m} \int_{a_k} B_{k,m} \cdot da_k , \quad (3.2)$$

where I_m is the current in filament m , $B_{k,m}$ is flux density created in the virtual loop of filament k (Figure 3-6) due to current passing through filament m , and a_k is the area bounded by the virtual loop. Magnetic vector potential is defined as

$$B_{k,m} = \nabla \times A_{k,m}, \quad (3.3)$$

Therefore, using Stokes' theorem [51], (3.2) can be written as

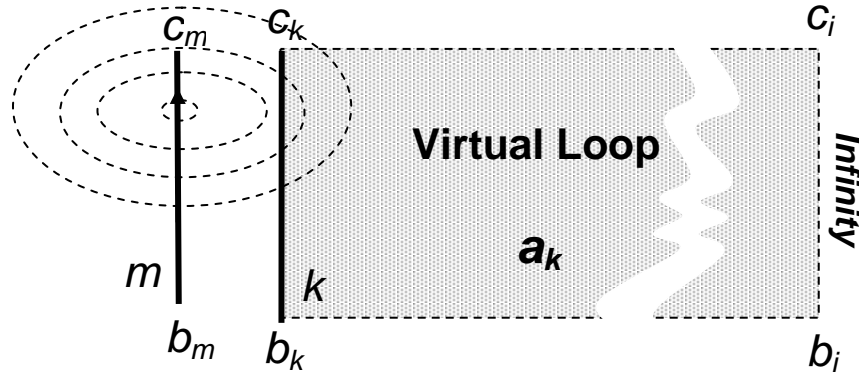


Figure 3-6: Partial mutual inductance. The partial mutual inductance between two filaments m and k is defined as the magnetic flux linkage between one filament (m) and the virtual loop ($b_k c_k c_i b_i$) of the other filament (k) when unit current is passing through m .

$$L_{p(k,m)} = \frac{1}{I_m} \int_{a_k} (\nabla \times A_{k,m}) \cdot da_k = \frac{1}{I_m} \oint_C A_{k,m} \cdot dl_k, \quad (3.4)$$

where C is the loop $b_k c_k c_i b_i$ surrounding the area a_k (Figure 3-6). The magnetic vector potential is in the direction of current, therefore, the integral along the perpendicular sides ($c_k c_i$ and $b_k b_i$) is zero. The magnetic vector potential is zero at infinity; therefore, the integral along the side which is at infinity ($b_i c_i$) is also zero. As a result partial mutual inductance is equal to

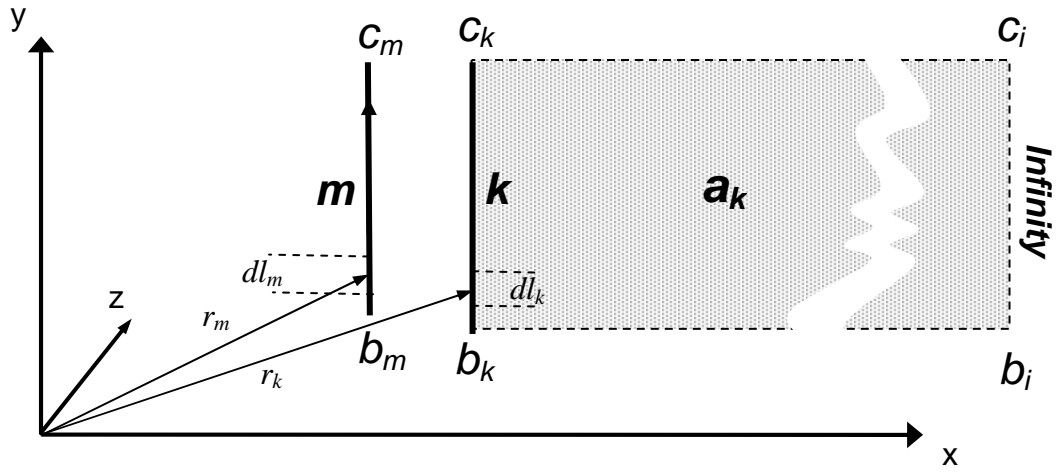


Figure 3-7: Partial mutual inductance in Cartesian coordinates.

$$L_{P(k,m)} = \frac{1}{I_m} \int_{b_k}^{c_k} A_{k,m} \cdot dl_k \quad (3.5)$$

The magnetic vector potential can be calculated from [51]

$$A_{k,m} = I_m \frac{\mu}{4\pi} \int_{b_m}^{c_m} \frac{dl_m}{r_{k,m}}, \quad (3.6)$$

where μ is the permeability of the medium, dl_m is an element of length of conductor m along its axis, and

$$r_{k,m} = |r_k - r_m|, \quad (3.7)$$

where r_k and r_m are the position vectors of filaments k and m (

Figure 3-7), respectively. Replacing A_{km} in (3.5) by (3.6), we have

$$L_{P(k,m)} = \frac{\mu}{4\pi} \int_{b_k}^{c_k} \int_{b_m}^{c_m} \frac{dl_m \cdot dl_k}{r_{k,m}}. \quad (3.8)$$

The loop self inductance can be calculated from the partial inductances of the filaments making the loop, using the following equation [35]

$$L_{loop} = \sum_k \sum_m S_{d(k,m)} L_{P(k,m)}, \quad (3.9)$$

where $S_{d(k,m)}$ is +1 if the currents in the filaments k and m are in the same direction, -1 if their currents are in opposite directions and zero if the filaments are orthogonal. The advantage of using the partial inductance method is that inductance can be extracted without prior knowledge of return paths. Figure 3-8 shows a loop. The virtual loops associated to filaments 1 and 3 are considered. The flux associated with partial self inductance of filament 1 extends from the filament to infinity. As shown the currents in those filaments are in opposite directions ($S_{d(1,3)} = -1$) and the virtual loop of the partial mutual inductance, $L_{p(1,3)}$, extends from filament 3 to infinity. Therefore, the flux area outside of the loop cancels out in the loop inductance calculation (3.9). This example shows how the partial inductance can be used without knowledge of the actual return paths [7].

The virtual loop of the partial inductance method however, is infinitely large; therefore, the mutual inductance between any two filaments is considerably large. As a result the inductance matrix for a large circuit is large and dense (total number of couplings for the entire interconnects system is $O(N^2)$) and thereby, simulating large circuits is almost impractical. For instance, a circuit with 1,000 parallel filaments will have $1,000^2 = 1,000,000$ elements. Dealing with such a large matrix in a circuit simulator is prohibitively time and memory consuming.

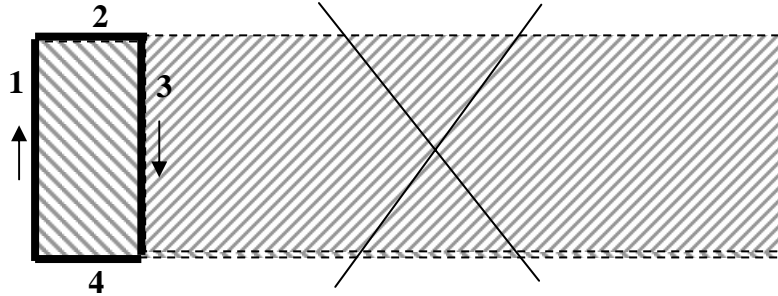


Figure 3-8. The return path of segment 1 is segment 3. As shown those parts of the virtual loop which are outside of the loop will cancel out, and therefore the partial inductance loop can be used without knowledge of the actual return paths.

To simulate large circuits like on-chip power distribution networks, a technique is needed to sparsify the inductance matrix. It can be proven that the inductance matrix should be positive definite [52], otherwise it will produce energy in the system (Matrix \mathbf{L} is positive definite, if $\mathbf{x}^T \mathbf{L} \mathbf{x} > 0$ for all nonzero vectors $\mathbf{x} \in \mathbb{R}^n$, where \mathbf{x}^T is the transpose of \mathbf{x} and \mathbb{R}^n is the space of all vectors of size n). Hence, any technique which is used to sparsify the matrix must result in a positive definite matrix. Truncating mutual inductances between far filaments can result in a non-positive definite matrix [35] and therefore, the sparsification is not simple. Several different sparsification methods have been introduced [42]-[46] based on windowing, where they sparsify the inductance matrix assuming that there is only mutual inductance coupling between filaments within the window and neglect couplings with filaments out of the window. It is therefore, applicable to designs wherein return paths are near signal lines and far inductance coupling are negligible. At high frequencies the return current of a signal interconnect is through neighboring interconnects and as a result the windowing techniques can be used to model a signal interconnect at high frequencies. The low-frequency return current of a signal interconnect however, is distributed through many different return paths.

Windowing underestimates the low frequency inductance by assuming that the return paths are through interconnects within the window. Another place where windowing would cause error would be the on-chip power/ground distribution grid where the return paths of the power/ground wires are not necessarily through the neighboring power/ground wires. Therefore, there is significant coupling between far filaments and sparsifying the inductance matrix using windowing [42]-[46] causes errors in the simulation of the on-chip power distribution grid.

In the following section, a new definition for inductance is introduced which results in a sparse inductance matrix without ignoring the coupling between far filaments.

3.3 Relative Inductance

In this section the relative inductance is introduced to sparsify the inductance matrix and as a result reduce the processing power and memory needed to simulate a massively coupled RLC circuit. Partial mutual inductance between two filaments is calculated from (3.8). To define relative inductance a reference with an arbitrary direction is selected parallel to the filament (Figure 3-9 and Figure 3-10). The virtual loop of the partial inductance ($b_k c_k c_i b_i$) can be divided into two loops (Figure 3-9 and Figure 3-10), the virtual loop of the partial inductance of the reference ($b_r c_r c_i b_i$) and the *relative* loop defined as the loop ($b_k c_k c_r b_r$), which is between the filament and the reference. From (3.8) the partial mutual inductance of filament m and the reference is equal to

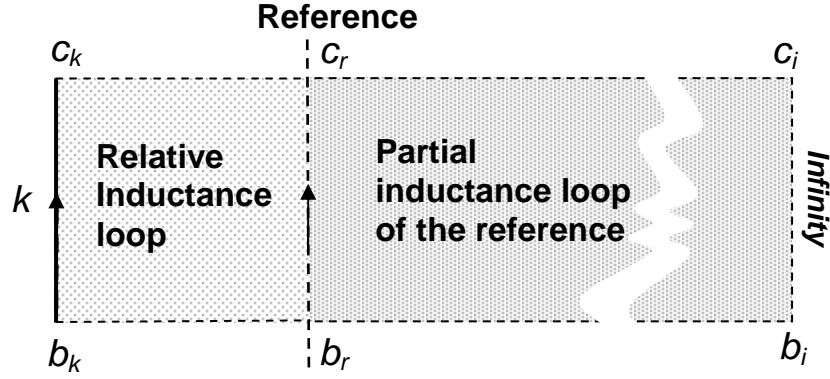


Figure 3-9: Relative self inductance. The virtual loop of self partial inductance of filament k ($b_k c_k c_i b_i$) is divided into two loops the relative inductance loop ($b_k c_k c_r b_r$) and the partial inductance loop of the reference ($b_r c_r c_i b_i$).

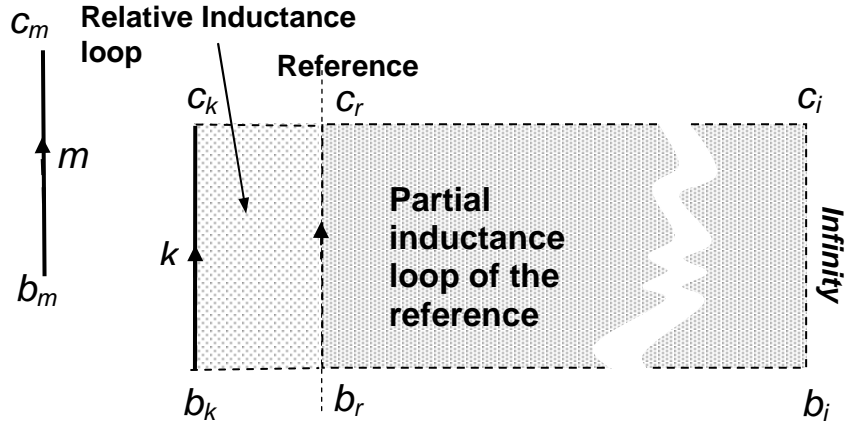


Figure 3-10: Relative mutual inductance. The virtual loop of mutual partial inductance of filament m ($b_k c_k c_i b_i$) is divided into two loops the relative inductance loop ($b_k c_k c_r b_r$) and the partial inductance loop of the reference ($b_r c_r c_i b_i$).

$$L_{P(r,m)} = \frac{\mu}{4\pi} \int_{b_r}^{c_r} \int_{b_m}^{c_m} \frac{dl_m \cdot dl_r}{r_{r,m}}, \quad (3.10)$$

and the relative inductance is equal to

$$L_{r(k,m)} = \frac{\mu}{4\pi} \int_{b_k}^{c_k} \int_{b_m}^{c_m} \frac{dl_m \cdot dl_k}{r_{k,m}} - \frac{\mu}{4\pi} \int_{b_r}^{c_r} \int_{b_m}^{c_m} \frac{dl_m \cdot dl_l}{r_{l,m}}. \quad (3.11)$$

The partial mutual inductance (3.8) can be written as

$$L_{P(k,m)} = L_{r(k,m)} + L_{P(r,m)} = \frac{\mu}{4\pi} \int_{b_k}^{c_k} \int_{b_m}^{c_m} \frac{dl_m \cdot dl_k}{r_{k,m}} - \frac{\mu}{4\pi} \int_{b_r}^{c_r} \int_{b_m}^{c_m} \frac{dl_m \cdot dl_l}{r_{l,m}} + \frac{\mu}{4\pi} \int_{b_r}^{c_r} \int_{b_m}^{c_m} \frac{dl_m \cdot dl_r}{r_{r,m}}. \quad (3.12)$$

Depending on the placement of the source (m), victim (k) and reference (r), four different situations might happen as shown in Figure 3-11. Hence, the partial mutual inductance of two filaments can be written as a function of *relative mutual inductance* and the partial mutual inductance of the filament (m) and the reference as

$$L_{P(k,m)} = S_{l(k,m)} L_{r(k,m)} + L_{P(r,m)}, \quad (3.13)$$

where $S_{l(k,m)}$ is defined by the location of the filaments with respect to the reference as

$$S_{l(k,m)} = \begin{cases} +1 & \text{if } k \text{ is nearer to } m \\ -1 & \text{if the reference is nearer to } m \end{cases}. \quad (3.14)$$

A new sign is defined called the *relative sign*

$$S_{r(k,m)} = S_{d_k} S_{d_m} S_{l(k,m)}, \quad (3.15)$$

where S_{d_x} is called the *direction sign* of filament x

$$S_{d_x} = \begin{cases} +1 & \text{if current in } x \text{ has the same direction} \\ & \text{as the reference direction} \\ -1 & \text{if current in } x \text{ is in the opposite direction} \end{cases} \quad (3.16)$$

The sign defined in partial inductance method (3.9) can be written as a function of the *direction sign* for the two filaments

$$S_{d(k,m)} = S_{d_k} S_{d_m}. \quad (3.17)$$

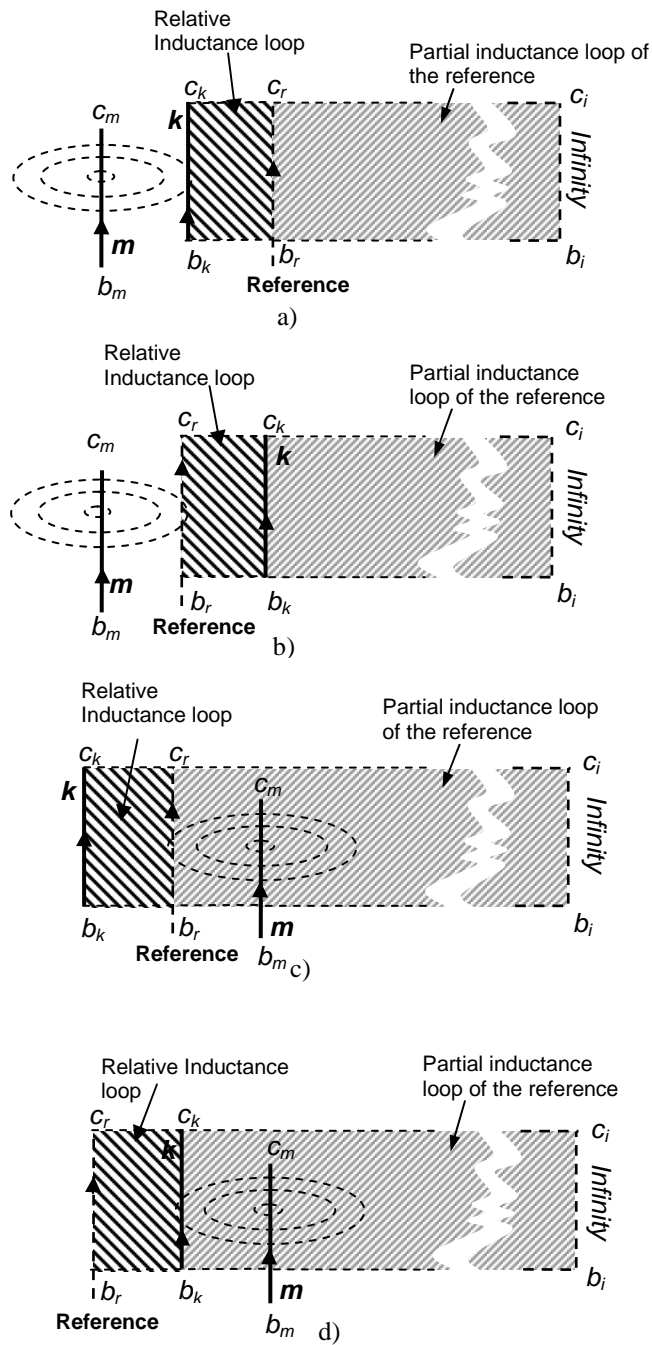


Figure 3-11: Partial and relative mutual inductance for a filament. Four different situations might happen depending on the location of the source filament m and victim filament k with respect to the reference r .

3.4 Relative Mutual Inductance for 3D structures

In this section it is proved that the relative inductance method can be used for any 3D structure. Figure 3-12 shows two planes orthogonal to the filament k . Any line on these orthogonal planes will be orthogonal to the filament and therefore, the mutual inductance between the filament and any line on these orthogonal planes is zero (3.5). Paths on the orthogonal planes which are selected for the virtual loop do not change the partial mutual inductance and thereby any path can be selected for the sides of the virtual loop.

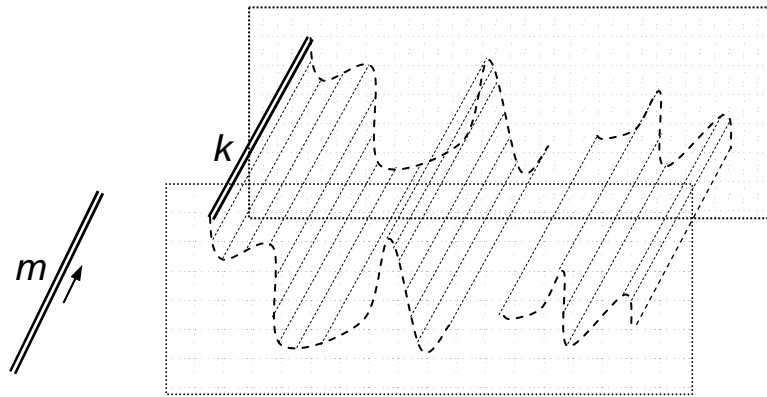


Figure 3-12: Any orthogonal path which is on the orthogonal planes to the filaments has no coupling with the filament. Therefore any path can be selected on the orthogonal planes for the sides of the virtual loop.

Figure 3-13 shows the case where the two filaments and the reference are not on the same plane. Two loops are selected: The first loop is the partial virtual loop $b_k c_k e_i d_i$, defined by [35]. The second loop is from the second filament (k) to the reference (relative loop $b_k c_k c_r b_r$) and from the reference to infinity $b_r c_r c_i b_i$ (partial mutual inductance of the filament m and the reference). Since the paths selected for the side lines are on the orthogonal planes, the partial inductances of the virtual loops are equal. As a result, we have

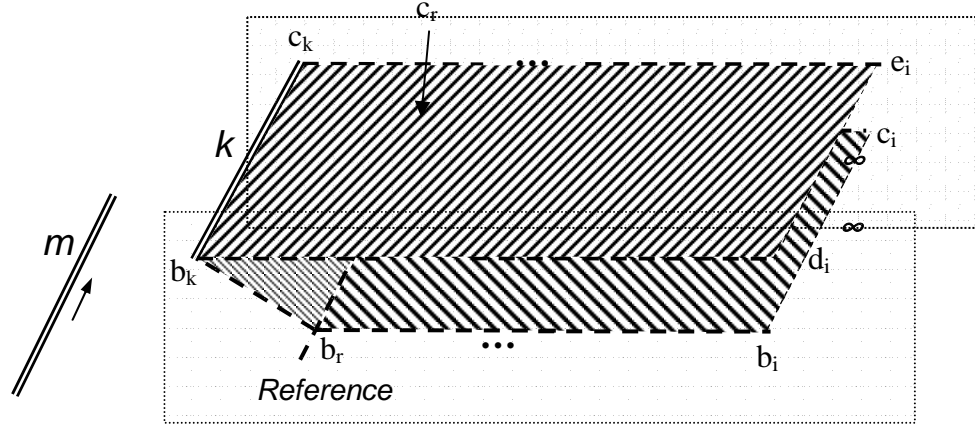


Figure 3-13: Two equal virtual loops are shown. The first one is the virtual loop $b_k c_k e_i d_i$ (virtual loop for partial inductance [7]) and the second loop is from the filament k to the reference (relative loop $b_k c_k c_r b_r$) and from the reference to infinity (mutual partial inductance of the reference $b_r c_r c_i b_i$).

$$L_{p(k,m)} = S_{l(k,m)} L_{r(k,m)} + L_{p(r,m)}. \quad (3.18)$$

Therefore, even if the relative loop and the partial inductance loop of the reference are not on the same plane, the same equation (3.13), exists between the relative and the partial inductance loop as long as the sides are on the orthogonal planes. As a result, the relative inductance can be used for any 3D structure.

3.5 Sparsifying the Relative Inductance Matrix

In this section it is proved that the relative inductance defined in the previous sections will result in a sparse matrix. Magnetic flux is related to current as

$$\boldsymbol{\varphi} = \mathbf{L} \times \mathbf{I}, \quad (3.19)$$

where $\boldsymbol{\varphi}$ is the magnetic flux matrix, \mathbf{I} is the current matrix and \mathbf{L} is the partial inductance matrix. Equation (3.19) can be rewritten as

$$\begin{bmatrix} \varphi_1 \\ \varphi_2 \\ \varphi_3 \\ \vdots \\ \varphi_n \end{bmatrix} = \begin{bmatrix} L_{p(1,1)} & S_{d(1,2)} L_{p(1,2)} & S_{d(1,3)} L_{p(1,3)} & \cdots & S_{d(1,n)} L_{p(1,n)} \\ S_{d(2,1)} L_{p(2,1)} & L_{p(2,2)} & S_{d(2,3)} L_{p(2,3)} & \cdots & S_{d(2,n)} L_{p(2,n)} \\ S_{d(3,1)} L_{p(3,1)} & S_{d(3,2)} L_{p(3,2)} & L_{p(3,3)} & & S_{d(3,n)} L_{p(3,n)} \\ \vdots & \vdots & & \ddots & \\ S_{d(n,1)} L_{p(n,1)} & S_{d(n,2)} L_{p(n,2)} & S_{d(n,3)} L_{p(n,3)} & \cdots & S_{d(n,n)} L_{p(n,n)} \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ \vdots \\ I_n \end{bmatrix}, \quad (3.20)$$

where each element of the inductance matrix is the partial inductance (3.2), defined in [35]. The inductance matrix is symmetric, hence is equal to its transpose:

$$\mathbf{L} = \mathbf{L}^T = \begin{bmatrix} L_{p(1,1)} & S_{d(2,1)} L_{p(2,1)} & S_{d(3,1)} L_{p(3,1)} & \cdots & S_{d(n,1)} L_{p(n,1)} \\ S_{d(1,2)} L_{p(1,2)} & L_{p(2,2)} & S_{d(3,2)} L_{p(3,2)} & \cdots & S_{d(n,2)} L_{p(n,2)} \\ S_{d(1,3)} L_{p(1,3)} & S_{d(2,3)} L_{p(2,3)} & L_{p(3,3)} & & \\ \vdots & \vdots & & \ddots & \\ S_{d(1,n)} L_{p(1,n)} & S_{d(2,n)} L_{p(2,n)} & S_{d(3,n)} L_{p(3,n)} & & S_{d(n,n)} L_{p(n,n)} \end{bmatrix} \quad (3.21)$$

Replacing the partial inductances by the relative inductances described by (3.13), (3.21) can be rewritten as

$$\mathbf{L} = \begin{bmatrix} S_{d(1,1)} (L_{(1,1)} + L_{r(1,1)}) & S_{d(2,1)} (S_{(2,1)} L_{(2,1)} + L_{r(1,1)}) & \cdots & S_{d(n,1)} (S_{(n,1)} L_{(n,1)} + L_{r(1,1)}) \\ S_{d(1,2)} (S_{(1,2)} L_{(1,2)} + L_{r(1,2)}) & S_{d(2,2)} (L_{(2,2)} + L_{r(1,2)}) & \cdots & S_{d(n,2)} (S_{(n,2)} L_{(n,2)} + L_{r(1,2)}) \\ \vdots & \vdots & \ddots & \vdots \\ S_{d(1,n)} (S_{(1,n)} L_{(1,n)} + L_{r(1,n)}) & S_{d(2,n)} (S_{(2,n)} L_{(2,n)} + L_{r(1,n)}) & & S_{d(n,n)} (L_{(n,n)} + L_{r(1,n)}) \end{bmatrix} \quad (3.22)$$

Equation (3.20) can be rewritten with an extra row and column

$$\begin{bmatrix} \varphi_1 \\ \varphi_2 \\ \varphi_3 \\ \vdots \\ \varphi_n \\ 0 \end{bmatrix} = \begin{bmatrix} L_{r(1,1)} & S_{r(2,1)} L_{r(2,1)} & S_{r(3,1)} L_{r(3,1)} & \cdots & S_{r(n,1)} L_{r(n,1)} & S_{d_1} L_{p(r,1,1)} \\ S_{r(1,2)} L_{r(1,2)} & L_{r(2,2)} & S_{r(3,2)} L_{r(3,2)} & \cdots & S_{r(n,2)} L_{r(n,2)} & S_{d_2} L_{p(r,1,2)} \\ S_{r(1,3)} L_{r(1,3)} & S_{r(2,3)} L_{r(2,3)} & L_{r(3,3)} & & S_{r(n,3)} L_{r(n,3)} & S_{d_3} L_{p(r,1,3)} \\ \vdots & \vdots & & \ddots & & \\ S_{r(1,n)} L_{r(1,n)} & S_{r(2,n)} L_{r(2,n)} & S_{r(3,n)} L_{r(3,n)} & & L_{r(n,n)} & S_{d_n} L_{p(r,1,n)} \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} |i_1| \\ |i_2| \\ |i_3| \\ \vdots \\ |i_n| \\ \sum_{i=1}^{n(r)} S_{d_i} |i_i| \end{bmatrix}, \quad (3.23)$$

wherein all magnetic flux and current elements are the same as those in (3.20) and $n(rI)$ is the number of filaments associated with reference rI . This equation (3.23) describes the magnetic flux as a function of the relative inductances to the reference and the partial inductances of the references. This matrix is still dense. To make a sparse matrix, multiple references should be defined (Figure 3-14). The filaments are divided into different groups with the same length and a reference is defined for each group of filaments (Figure 3-14). The relative inductance for each filament is calculated to reference in that group. The relative inductance loop for a filament is shown shaded in Figure 3-14.

To make the inductance matrix for a circuit with multiple references an extra row and column should be added to the inductance matrix \mathbf{L} , for each added reference. An extra current element which is the summation of the currents in the filaments related to that reference should also be added to the current vector. Equation (3.19) for a circuit with multiple references can be rewritten as shown in Figure 3-15 (using the same technique to derive(3.23)).

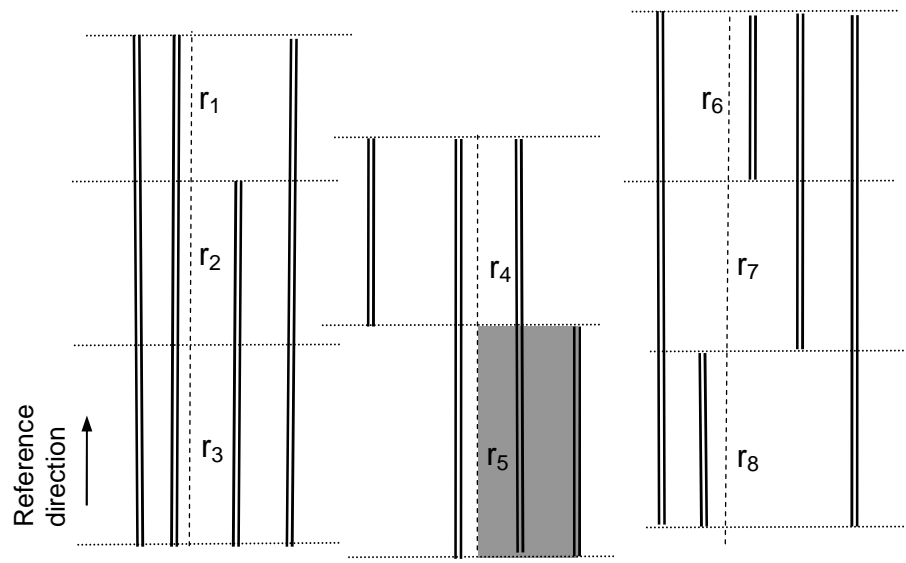


Figure 3-14: Multiple references should be used. The filaments are divided into groups with equal lengths and a reference is defined for each group. In this example, the interconnects are divided into 8 groups and 8 references are defined for each group of filaments. The relative mutual inductance should be calculated to the reference in the same group. The relative inductance loop for one of the filaments is shown shaded.

Figure 3-16 shows the mutual inductance between two filaments versus distance for partial and relative inductance methods. In the partial inductance method the virtual inductance is an infinitely large loop. Therefore, even if the distance between the two filaments is large the flux passing through this virtual loop is not negligible and as a result the mutual partial inductance of far segments can not be neglected. The relative inductance loop however, is small and therefore the flux which passes through it gets very small as the distance between the two filaments is increased. The mutual relative inductance of far filaments can therefore be truncated for a certain accuracy, which makes the inductance matrix of Figure 3-15 sparse.

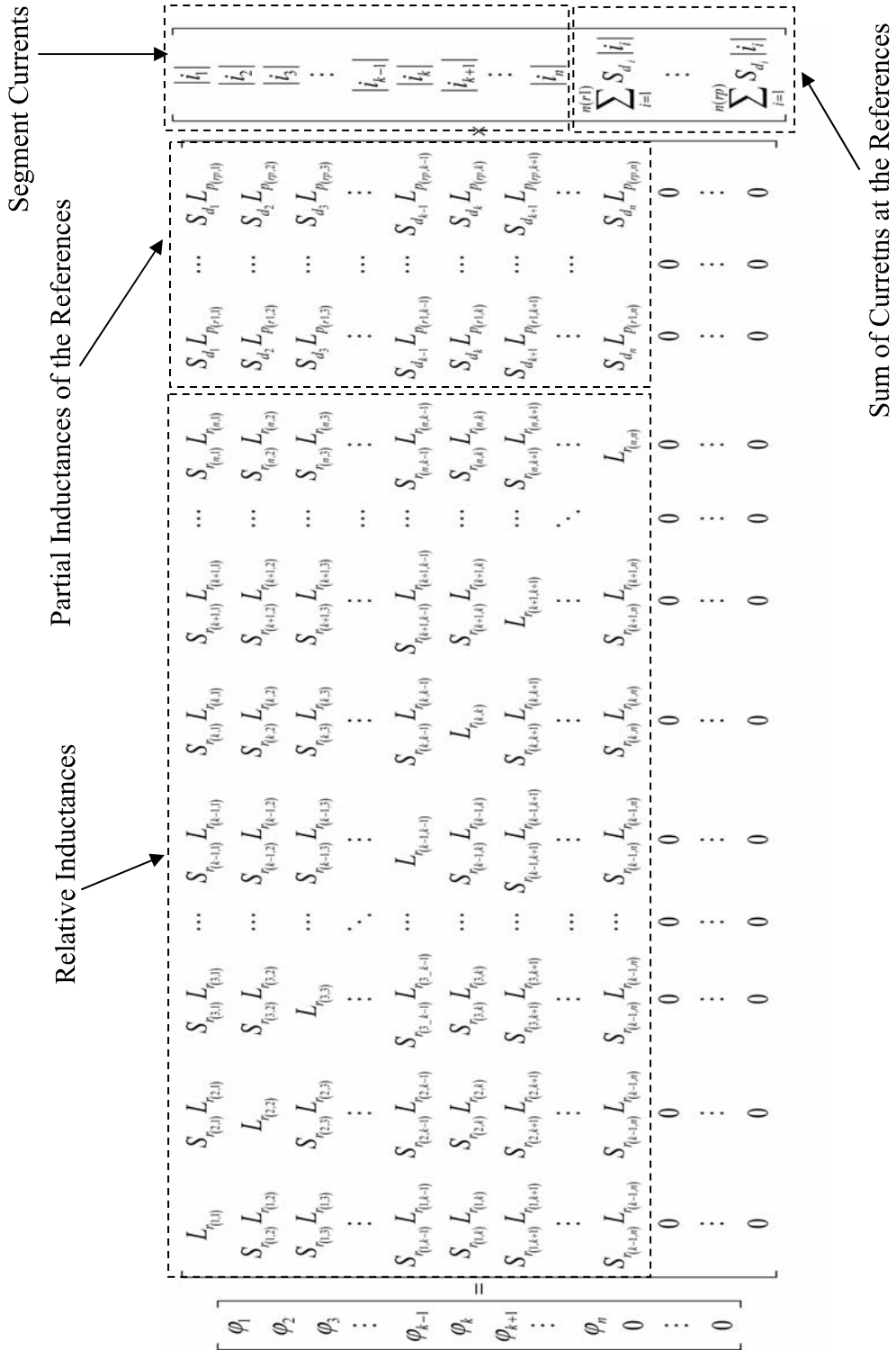


Figure 3-15: Flux matrix as a function of inductance matrix and current for a system with multiple references.

In [53] it is shown that the two-dimensional inductance modeling can be used for certain applications and frequencies to reduce the complexity of the system and accelerate circuit simulations. Figure 3-17 shows two filaments that their lengths are large compared to the distance of the filaments to their references. The flux due to current passing through filament k which passes through the virtual relative loop of filament l is negligible and as a result would be truncated in the truncation process. Therefore the relative inductance method would automatically convert the 3D problem to a 2D problem and reduce the complexity.

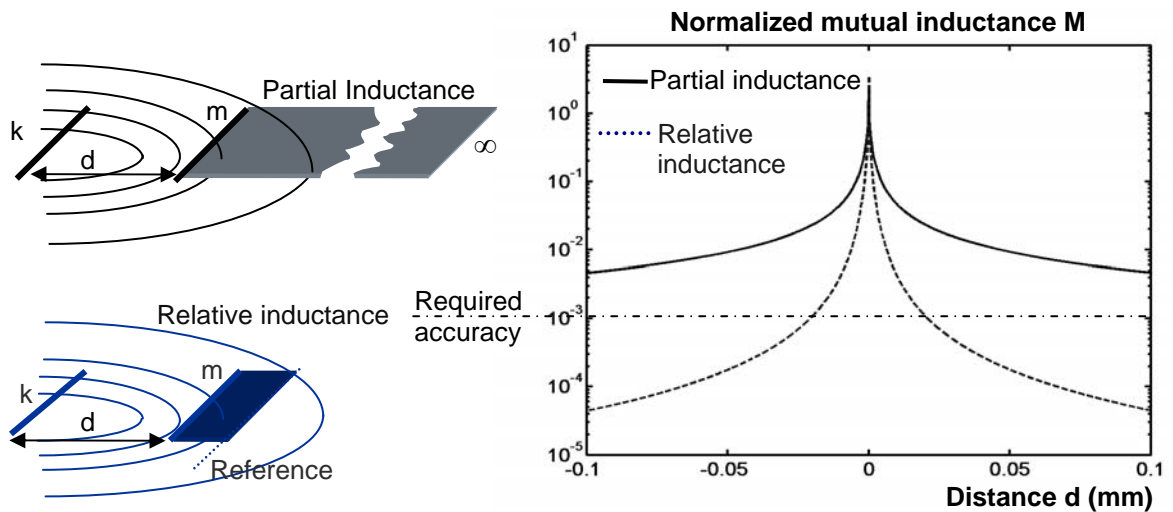


Figure 3-16: Mutual inductance versus distance d for partial inductance and the relative mutual inductance. The relative inductance drops faster than the partial inductance, and therefore truncating the coupling between far filaments for a certain accuracy (e.g. $M < 10^{-3}$) results in a sparse relative inductance matrix.

To model an interconnect circuit, the interconnect is first divided into filaments as shown in Figure 3-2. Then the filaments are divided into different groups with the same length and a reference is defined for each group (Figure 3-14). All of the filaments in each group should be near each other, so that the relative inductance loops are small (small relative inductance loops will result in a sparse matrix). The number of groups (references) should be selected appropriately. A small number of groups (references) will

result in large relative inductance loops and as result a small number of zeros in the sparse matrix. On the other hand a large number of groups (references) will slow the simulations time due to overhead added by the partial inductances of the references.

Part of the matrix which has the partial mutual inductances between the references and the filaments is dense. To accelerate simulations for large circuits with many references, the dense partial inductances of the references can also be sparsified by using a hierarchy of references. The hierarchy is made by defining new references and applying the relative inductance method to the partial inductances of the references.

In the relative inductance method the coupling between far filaments is not neglected (Figure 3-18). As shown in Figure 3-18 the magnetic flux due to far filaments in the partial inductance method is replaced by a magnetic flux made by a current at the reference equal to the total currents of the filaments belonging to that reference.

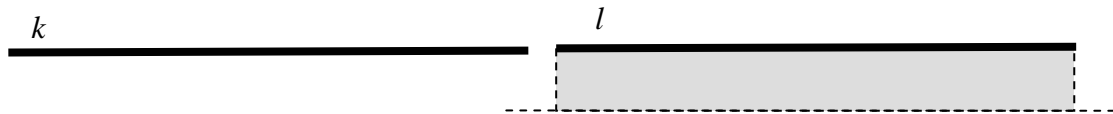


Figure 3-17: The flux due to current passing through filament k which passes through the virtual relative loop of filament l is negligible and as a result would be truncated in the truncation process. Therefore the relative inductance method would automatically convert the 3D problem to a 2D problem and reduce the complexity, when the length of the filament is large compared to the distance of the filament to its reference.

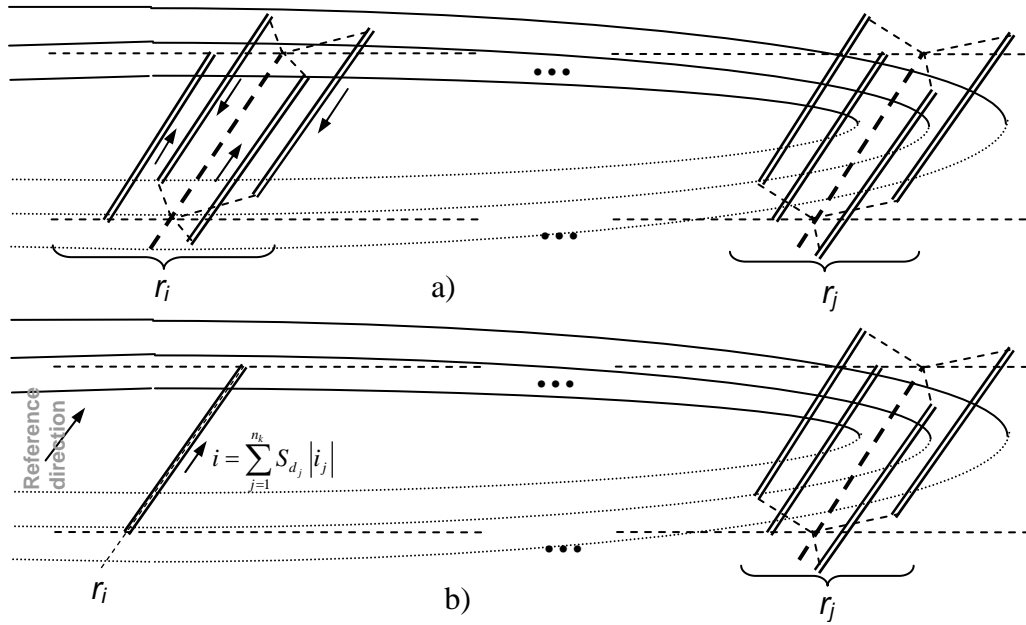


Figure 3-18: Assume two references are far apart. The flux at reference r_j due to filaments at reference r_i can be modeled as a single filament at reference r_i with a current equal to the total currents of filaments belonging to reference (r_i).

The average number of mutual relative inductances per filament (M) for certain accuracy does not change by increasing the number of filaments. Therefore, the total number of mutual relative inductance couplings for the entire interconnect network is $M*N$ (of the order of $O(N)$) [50]. Although the number of mutual inductances between the references and the filaments is of the order of $O(N^2)$, it is usually negligible for small circuits (Small number of references). In large circuits the relative inductance extraction method can be used in a hierarchical manner, defining new references for the current references and finding relative inductance of the references. By using this method the number of mutual inductances of the references will reduce to the order of $O(N)$. Therefore by using the relative inductance extraction method in a hierarchical manner the number of mutual inductances of any circuit can be reduced to $O(N)$.

3.6 Implementation

To implement a circuit model using the relative inductance method in SPICE we have to look at some interesting features that the relative inductance has:

- 1) Although the new inductance matrix has more elements than the original matrix, it is significantly sparser.
- 2) It is asymmetrical because L_{ij} is not equal to L_{ji} .
- 3) If a filament and its reference are at the same location, the relative self inductance of the filament will be zero. It however, has nonzero mutual inductances to other filaments.

To simulate the circuits, the extracted matrices should be incorporated in a circuit which can be simulated by HSPICE [54]. Mutual and self inductances entered in HSPICE simulators need to have the following properties:

$$M_{ij} = M_{ji} , \quad (3.24)$$

and

$$M_{ij} = K \sqrt{L_i \cdot L_j} \quad 0 < |K| \leq 1, \quad (3.25)$$

where M_{ij} is the mutual inductance on filament i due to current passing through filament j , and L is the self inductance. These conditions are not satisfied for the new relative inductance matrix. The inductance matrix is asymmetrical (L_{ij} is not equal to L_{ji}) and as explained before in the features of this matrix, K is not limited between zero and one. Therefore, in HSPICE simulations, the relative inductances are implemented using voltage-controlled voltage sources (Figure 3-19), the references are implemented as voltage-controlled current sources (Figure 3-20.a) and the voltage drop due to references is modeled as voltage-controlled voltage (Figure 3-20.b). Using these circuits will add

extra nodes to the circuit implementation of the relative inductance and as a result slow the simulations.

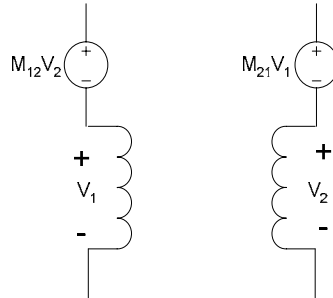


Figure 3-19: Equivalent circuit for simulating two inductances with an asymmetrical inductance ($M_{12} \neq M_{21}$) matrix in a circuit simulator such as SPICE which does not support asymmetrical inductance matrices.

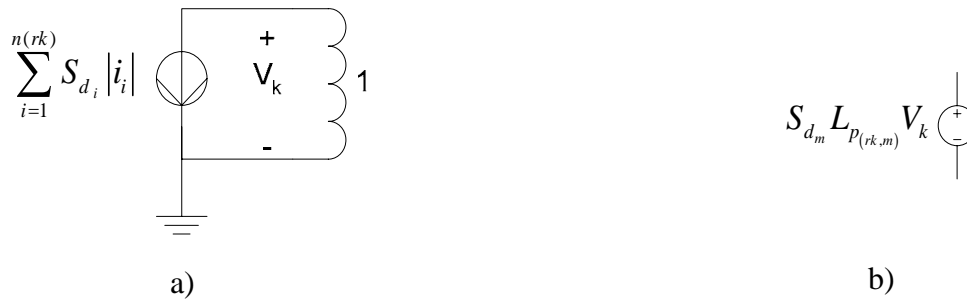


Figure 3-20: Equivalent circuit for simulating the references. a) Equivalent circuit for the current passing through reference k . b) Equivalent circuit for the voltage drop due to reference k on inductance m .

In the following section two examples are shown. In the first example a sixteen-bit bus is considered. The inductance values are extracted for three different methods and the results are compared. The second example is a power distribution grid on the chip. This example is chosen to prove that this method can be used in applications where mutual inductances between far segments are important.

3.6.1 Simulating a 16-bit bus

To compare the relative inductance method with other sparsification techniques, a 16-bit bus has been simulated with ground lines placed for every 4 signal wires (Figure 3-21). The simulations have been done for the partial inductance model, the relative inductance model and the block diagonal sparsification method [46] (Appendix B). For the case where the line is divided into 4 segments the references selected for the relative inductance method are as shown in Figure 3-22. The partial self and mutual inductance are calculated from 55 . The number of references used for this example is equal to the number of segments per line. The relative inductance for each segment is calculated from the partial inductance of the segment and the partial inductance of the reference (3.12).

Results of the simulations are shown in Figure 3-23. As shown, there is very good agreement between the partial inductance method and the relative inductance method. However the results are different for the block diagonal sparsification method. Figure 3-24 shows simulation time results of the three methods for different numbers of segments per line. Results show that for a small number of segments the overhead caused by the references will actually increase the simulation time. However, as the number of segments increases, the relative inductance method is much faster because of the sparser inductance matrix. The simulation time for the block diagonal sparsification method lies between the other methods. Figure 3-25 shows the memory required by the simulator using the three methods for different numbers of segments per line. As shown the relative inductance method uses less memory due to the sparser inductance matrix. The results also show that the relative inductance method achieves accuracy with less simulation time and memory.

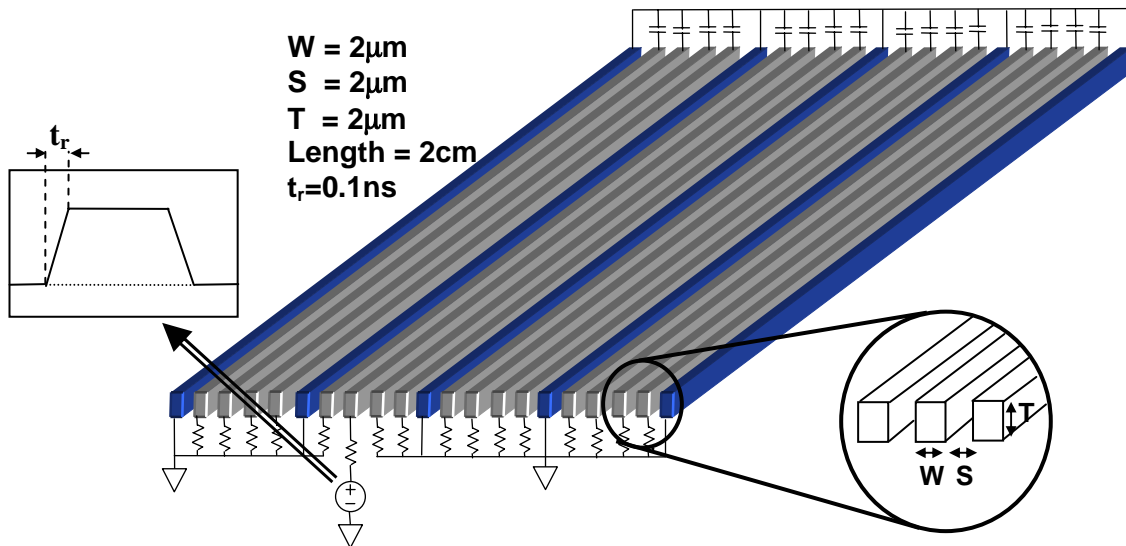


Figure 3-21: 16-bit bus structure with five power/ground lines. To simulate, each interconnect is divided into different number of segments. Then inductance of each segment is extracted using the partial inductance method, the relative inductance method and the block diagonal sparsification method [46].

The results (Figure 3-24, Figure 3-25) show that although extra nodes are added to the relative inductance implementation of the circuit, the required simulation time and memory are less than the partial inductance method for large circuits. As shown in Figure 3-19 and Figure 3-20 extra elements are added in order to overcome the restrictions of current SPICE circuit simulators. The simulation time and memory using the relative inductance method can be reduced even further by eliminating the restrictions of current SPICE simulators in future.

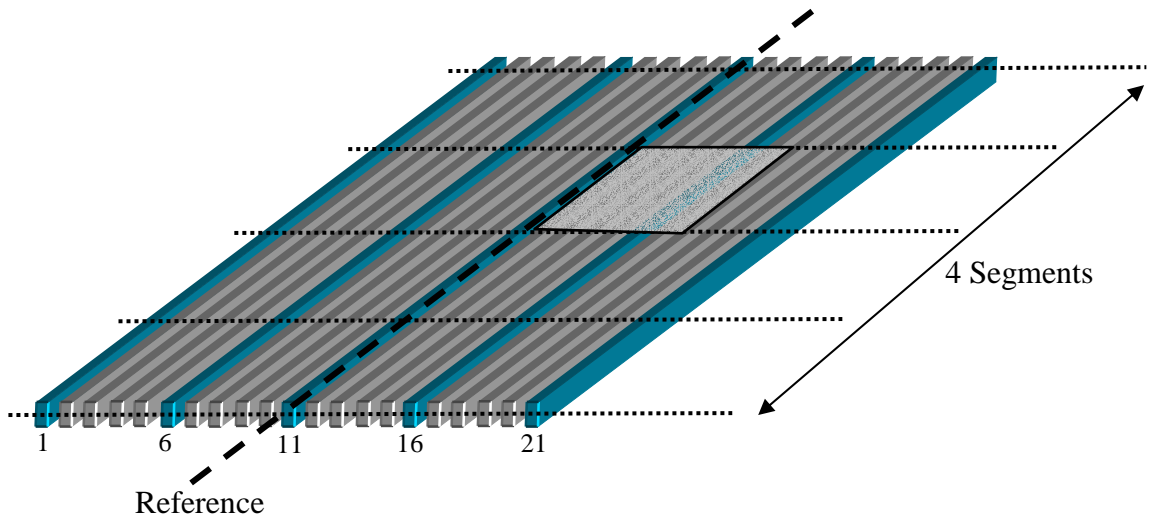


Figure 3-22: 16-bit bus structure used to extract relative inductance matrix. In this example each line is divided into four segments. One reference is selected parallel to the wire lines and is divided to 4 segments in this example, making a total number of 4 references. The relative inductance loop of the third segment of wire 18 is shown shaded in the figure.

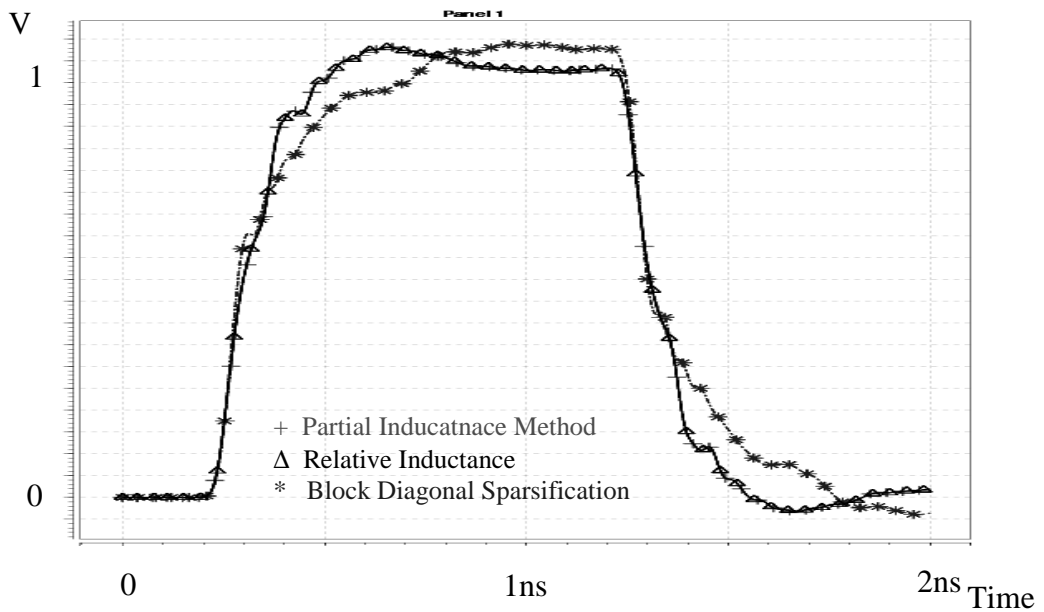


Figure 3-23: SPICE simulation of active line for a 16-bit bus (Figure 3-21) using the partial inductance method, the relative inductance method and the block diagonal sparsification method [46]. Each signal line is divided into 16 segments in the simulations.

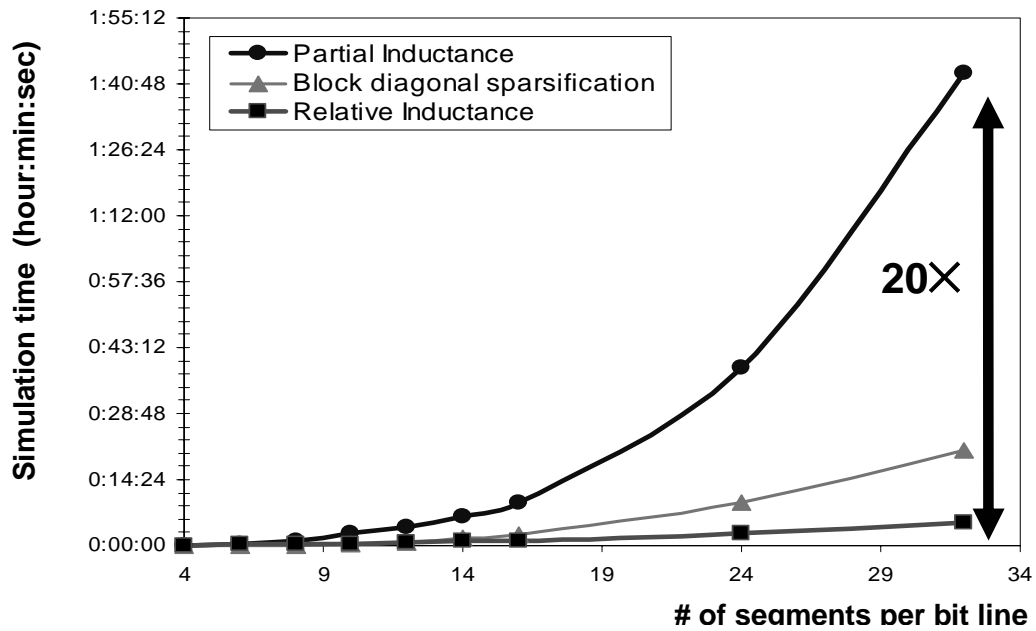


Figure 3-24: Simulation time of a 16-bit bus for different numbers of segments per bit-line, using the partial inductance method, the relative inductance method and the block diagonal sparsification method [46]. Simulations have been done on a SUN Blade 2000 with 1024 Mbyte memory.

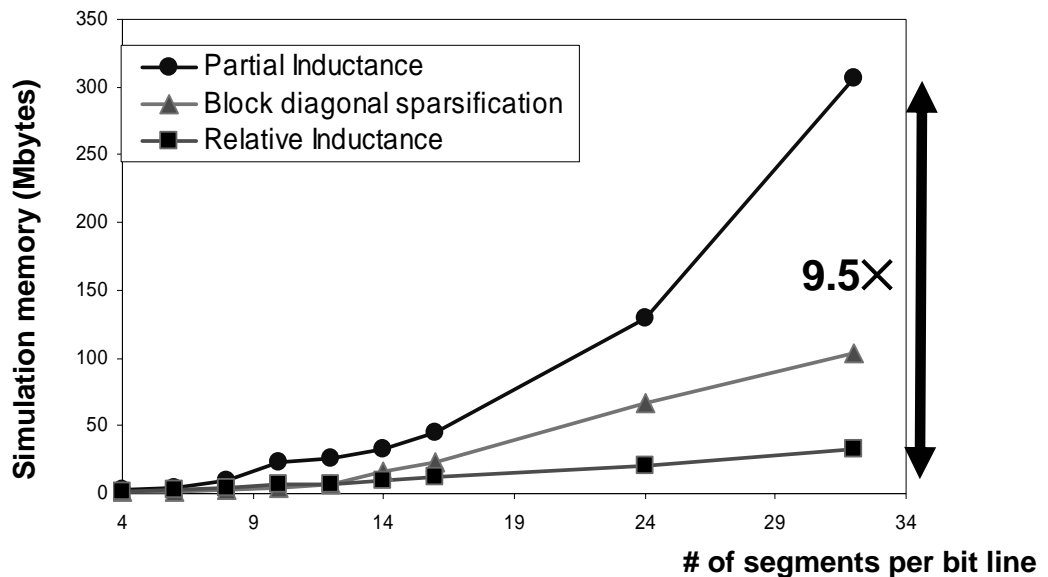


Figure 3-25: Memory required for simulation of a 16-bit bus for different numbers of segments per bit-line, using the partial inductance method, the relative inductance method and the block diagonal sparsification method [46]. Simulations have been done on a SUN Blade 2000 with 1024 Mbyte memory.

3.6.2 Simulation of a power grid cell

In the second example a 20×20 power distribution grid is simulated (Figure 3-26) (Appendix C). The grid is connected to four pads at the corners. A block at the center of the grid is turned on. The length of each segment of the grid is $28 \mu\text{m}$. Each segment is $1 \mu\text{m}$ thick and $1 \mu\text{m}$ tall. A capacitance of 1.5 pF is placed at each crossing for the on-chip decoupling capacitance. The pad size is $54 \mu\text{m}$ by $54 \mu\text{m}$. A circuit block at the center is turned on. The size of the block is $140 \mu\text{m}$ by $140 \mu\text{m}$. The block current is a step function of 144 mA (Figure 3-27). To calculate relative inductance 5 references are selected along the segments in each direction (x and y), each reference is divided into 20 segments. The total references in each direction are $5 \times 20 = 100$. The simulations have been done for two methods, the relative inductance method and the partial inductance method.

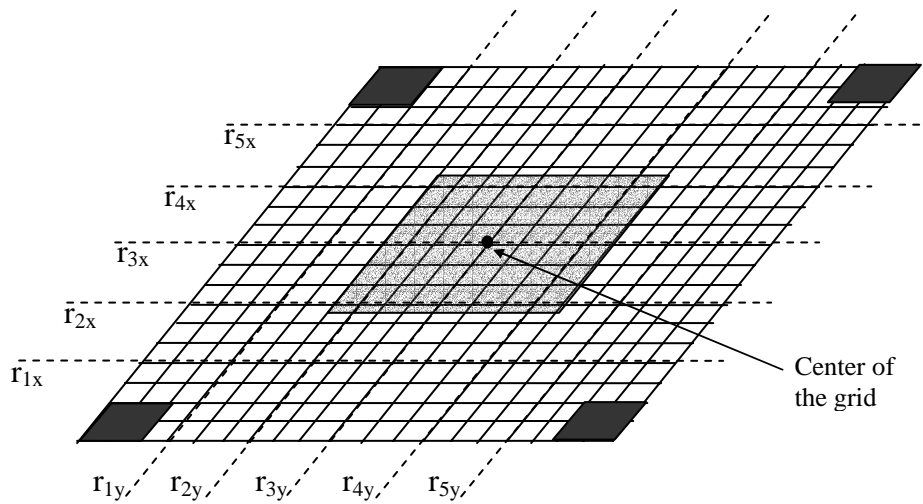


Figure 3-26: A 20×20 grid with four pads at the corners. A circuit block is turned on at the center of the grid.

Results of the simulation of the grid (Figure 3-26) are shown in Figure 3-28. As shown there is very good agreement between the simulations using relative inductance and the partial inductance. Simulation shows that the relative inductance is almost three times faster than the partial inductance method. The advantage of using the relative inductance would be more obvious by simulating even larger grids.

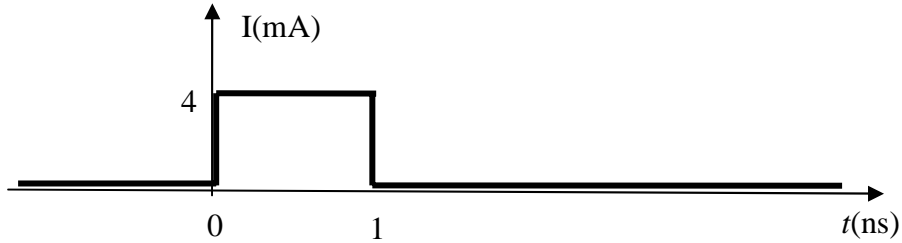


Figure 3-27: Current source placed at each crossing in the circuit block.

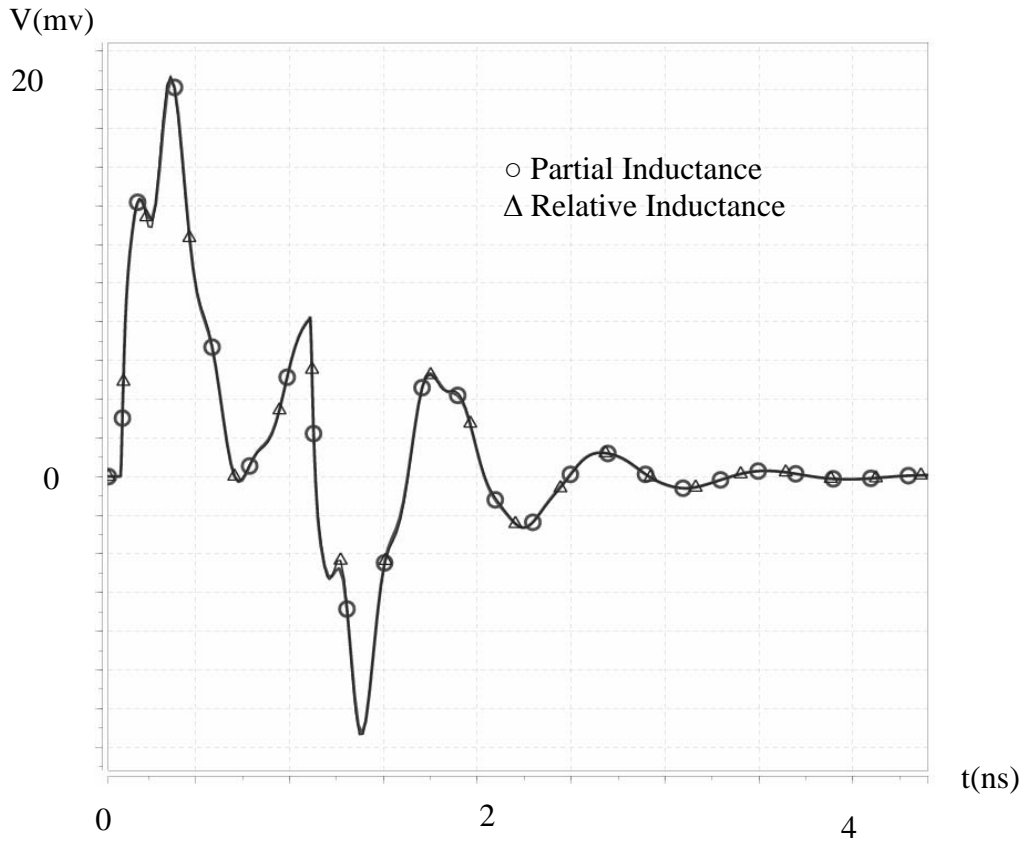


Figure 3-28: Voltage simulation at the center of the grid. For two different method, partial inductance method, relative inductance method.

3.7 Conclusion

A new relative inductance matrix is defined for solving massively coupled RLC interconnects. All self and mutual inductance elements are calculated using several virtual return paths that are relatively close to interconnects, and the new inductance matrix is hence very sparse. It has been demonstrated that the relative inductance matrix is equivalent to the conventional partial inductance matrix that calculates all inductance elements assuming return paths are at infinity. The analysis is hence accurate for wide range of frequencies and configurations. Using the new relative inductance matrix makes the circuit simulations significantly faster and reduces the required memory for simulating. Simulations for a 16-bit bus show that the new technique is 20 times faster and requires 9.5 times less memory to simulate than the conventional dense partial inductance technique.

In Chapter 2 a compact model was derived for IR-drop and in Chapter 3 the relative inductance was introduced to accelerate simulation of simultaneous switching noise. In both chapters our concern was supply noise. However the other concern in the design of the power distribution network is reliability. In the next chapter electromigration which affects reliability of the power distribution will be modeled.

Chapter 4

Electromigration

4.1 Introduction

As integrated circuits become progressively more complex, the components must become increasingly more reliable if the reliability of the whole is to be acceptable. However, due to continuing miniaturization of gigascale integrated (GSI) circuits, interconnects are subject to increasingly high current densities. However, when direct current density in a wire exceeds a certain limit, the metal atoms are moved in the direction of the electron flow because of the collisions between the atoms and the electrons. This phenomenon is called electromigration [13], [56]. Under these conditions, electromigration can lead to the electrical failure of interconnects in relatively short times, reducing the circuit lifetime to an unacceptable level. It can not only cause open and short circuits in the power distribution network, but it also increases the resistances of the power distribution network, which leads to increased IR-drop and simultaneous switching noise [13]. It is therefore important to model the direct current in the power distribution network which causes electromigration failure in interconnects.

Traditionally, it has been observed that electromigration failure followed $1/J^2$, where J is current density. This has become known as Black's Law (4.1) [57], [58]. Black's pioneering work included the first careful systematic investigations of electromigration failure kinetics. His experiments uncovered the curious behavior that electromigration

failures followed kinetics that depended not on the inverse of the current density, but on the inverse square [57], [58]

$$t_{50} = AJ^{-2} \exp\left[\frac{\nabla H}{kT}\right], \quad (4.1)$$

where t_{50} is the median time to failure in an ensemble of samples, A is a constant that needs to be empirically determined, J is current density, ∇H is the activation energy for failure, k is Boltzmann's constant and T is temperature. This equation has proven to be adequate even to the present day. Only small corrections, often too small to be detected experimentally have been needed to keep Black's Law consistent with the latest theoretical developments [13].

Electromigration not only causes open and short circuits in the power grid, but it also increases the segment resistances in the grid, which leads to increased IR-drop and simultaneous switching noise. Electromigration can occur at the grid segments and the grid vias of the power distribution network. In Section 4.2 the electromigration current is calculated for a grid segment. Then, in Section 4.3 the electromigration is computed for vias of the power distribution network.

4.2 Electromigration of Grid Segments

The direct current passing through grid segments causes electromigration. The grid segment direct current can be calculated from the IR-drop voltage by finding the IR-drop voltage slope for each segment in the grid. The segments current in the x and y direction can be calculated from

$$I_x = \frac{l_{segx}}{R_{segx}} \frac{\partial V_{IR}}{\partial x}, \quad (4.2)$$

and

$$I_y = \frac{l_{segy}}{R_{segy}} \frac{\partial V_{IR}}{\partial y}. \quad (4.3)$$

The segment current in the x direction for a wire-bond package can be calculated from (2.13) and (4.2)

$$I_x(x, y) = \frac{16 \cdot l_{segx} \cdot J_0}{R_{segx} a \cdot \pi^3} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\cos\left((2k+1)\frac{\pi}{a} \cdot x\right) \sin\left((2l+1)\frac{\pi}{b} \cdot y\right)}{(2l+1) \left(\frac{l_{segx} (2k+1)^2}{R_{segx} l_{segy} a^2} + \frac{l_{segy} (2l+1)^2}{R_{segy} l_{segx} b^2} \right)}. \quad (4.4)$$

The segment current in the y direction can be calculated in the same way. Figure 4-1 shows the segment current in the x direction for a wire-bond package. As shown, the segments having the maximum currents are near the power ring. If the current density in those segments exceed the maximum allowable current calculated from (4.1), then the segment wire widths needs to be increased near the power ring to reduce the current density in those segments.

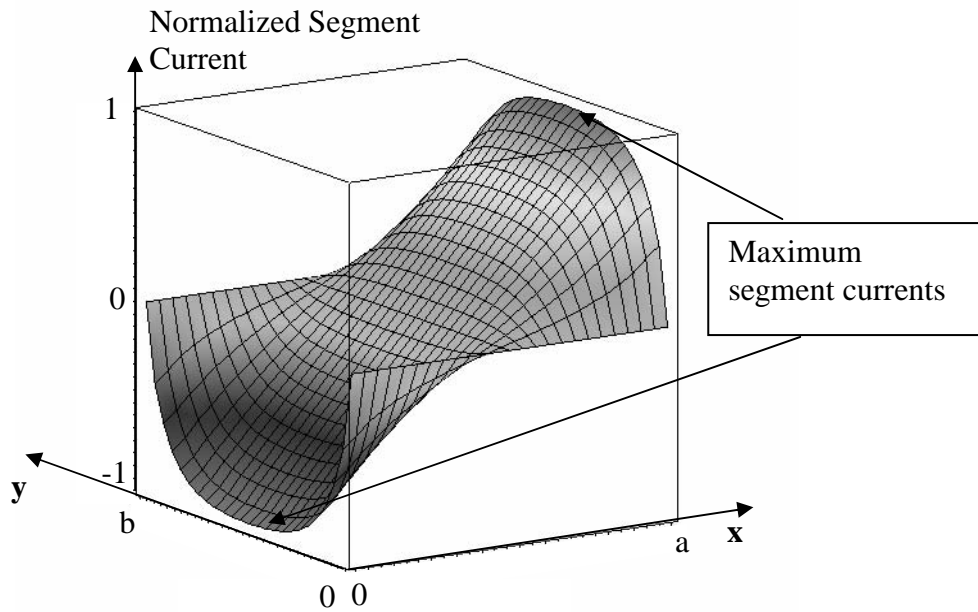


Figure 4-1: Normalized segment current (normalized to its maximum) in x direction for a wire bond package across the chip. The segments having the maximum currents are near the power ring.

In a flip-chip package, the segment current can be calculated by applying (4.2) and (4.3) to equations (2.42) to (2.46). Figure 4-2 shows the segment current in the x direction for a flip-chip package. As shown in Figure 4-2, the maximum segment current occurs near the pads. If the current density in those segments exceeds the maximum allowable current density then the segment widths needs to be increased near the pads.

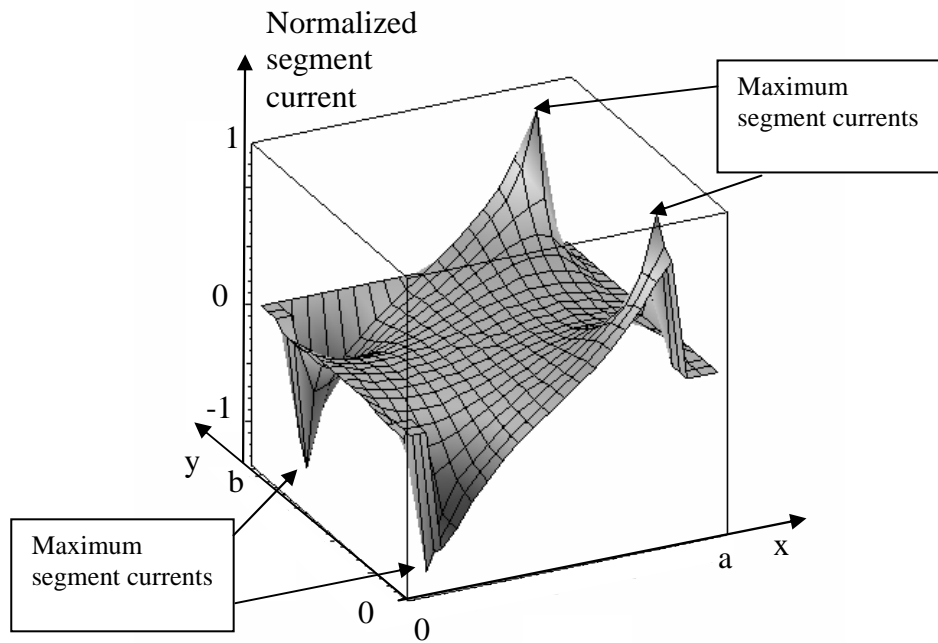


Figure 4-2: Normalized segment current (normalized to its maximum) in x direction for an area array package. The maximum segment current occurs near the pads.

4.3 Electromigration in the Vias

Electromigration also happens in the vias of the power distribution grid, where a pair is defined as two orthogonal metal levels. A power distribution network is made of multiple pairs in parallel. To model the current density in the vias of a power distribution network, two kinds of vias are defined:

- 1) Vias that connect different power/ground pairs together (Figure 4-3a).
- 2) Vias that connect the grids within a power/ground pair (Figure 4-3b).

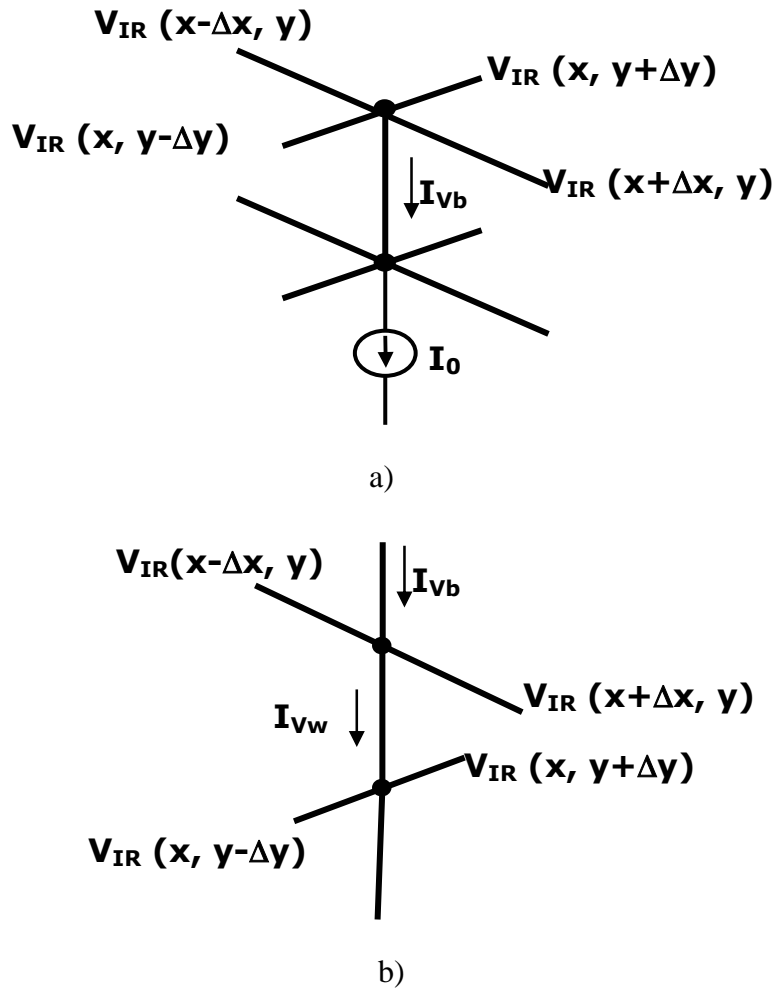


Figure 4-3: Via current for the on-chip power distribution grid. a) Current of the via which is between two different pairs. b) Current of the within-pair via.

4.4 Electromigration of the Vias Between Different Power/Ground pairs

The current of the via that is between isotropic pairs k and $k+1$ can be calculated from the voltage of its four neighboring nodes (Figure 4-3a)

$$\begin{aligned} & \frac{V_{IR}(x, y) - V_{IR}(x + \Delta x, y)}{R_{sTk} \frac{\Delta x}{\Delta y}} + \frac{V_{IR}(x, y) - V_{IR}(x, y + \Delta y)}{R_{sTk} \frac{\Delta y}{\Delta x}} \\ & + \frac{V_{IR}(x, y) - V_{IR}(x - \Delta x, y)}{R_{sTk} \frac{\Delta x}{\Delta y}} + \frac{V_{IR}(x, y) - V_{IR}(x, y - \Delta y)}{R_{sTk} \frac{\Delta y}{\Delta x}} = -J_{vb} \cdot \Delta x \cdot \Delta y \end{aligned} \quad , (4.5)$$

where J_{vb} is the current density of the current passing between the pairs k and $k+1$, R_{sTk} is the equivalent sheet resistance of the pairs that are above layer $k+1$ and can be calculated from

$$\frac{1}{R_{sTk}} = \frac{1}{R_{s(k+1)}} + \frac{1}{R_{s(k+2)}} + \dots + \frac{1}{R_{s(n)}}, \quad (4.6)$$

where $R_{s(n)}$ is the sheet resistance of pair n and for an isotropic pair is equal to

$$R_{s(n)} = R_{segn} \quad \text{for} \quad l_{segx} = l_{segy} = l_{seg}. \quad (4.7)$$

Simplifying (4.5) we have

$$\nabla^2 V_{IR} = R_{sTk} J_{vb}, \quad (4.8)$$

This is the same Poisson equation for the IR-drop voltage of the grid. From (4.8) and (2.5) we have

$$I_{vb} = l_{seg}^2 J_{vb} = \frac{R_{sTot} l_{seg}^2 J_0}{R_{sTk}}, \quad (4.9)$$

where I_{vb} is the via current which is between pairs k and $k+1$, l_{seg} is the segment length and R_{sTot} is the equivalent sheet resistance of all pairs,

$$\frac{1}{R_{sTot}} = \frac{1}{R_{s(1)}} + \frac{1}{R_{s(2)}} + \dots + \frac{1}{R_{s(n)}} \quad (4.10)$$

4.5 Electromigration of the Within-pair Vias of a Power/Ground Grid

The current of the vias within an isotropic power/ground pair N can be calculated from the neighboring voltages (Figure 4-3b)

$$\frac{V_{IR}(x, y) - V_{IR}(x + \Delta x, y)}{R_{s(n)} \frac{\Delta x}{\Delta y}} + \frac{V_{IR}(x, y) - V_{IR}(x - \Delta x, y)}{R_{s(n)} \frac{\Delta x}{\Delta y}} = -(J_{Vw} - J_{Vb}) \cdot \Delta x \cdot \Delta y, \quad (4.11)$$

where J_{Vw} is the current density of the current within a pair, and $R_{s(n)}$ is the sheet resistance of the pair N in which the via is located. Writing the Taylor series for the two neighboring voltages we have

$$V_{IR}(x + \Delta x, y) = V_{IR}(x, y) + \Delta x \frac{\partial V_{IR}(x, y)}{\partial x} + \frac{\Delta x^2}{2} \frac{\partial^2 V_{IR}(x, y)}{\partial x^2} + \dots, \quad (4.12)$$

$$V_{IR}(x - \Delta x, y) = V_{IR}(x, y) - \Delta x \frac{\partial V_{IR}(x, y)}{\partial x} + \frac{\Delta x^2}{2} \frac{\partial^2 V_{IR}(x, y)}{\partial x^2} + \dots \quad (4.13)$$

Replacing the neighbor node voltages in (4.11) with the Taylor series and simplifying the result we have

$$\frac{\partial^2 V_{IR}(x, y)}{\partial x^2} = R_{s(n)} (J_{Vw} - J_{Vb}). \quad (4.14)$$

or

$$I_{Vw} = I_{Vb} + \frac{l_{seg}^2}{R_{s(n)}} \frac{\partial^2 V_{IR}(x, y)}{\partial x^2} \quad (4.15)$$

This equation gives the current of the within-pair vias.

4.6 Within-pair Via Currents for a Wire-Bond Package

The within-pair via currents in a wire-bond package can be calculated from (2.13), (4.9) and (4.15):

$$I_{Vw} = I_{Vb} + \frac{l_{seg}^2}{R_{s(n)}} \frac{\partial^2 V_{IR}(x, y)}{\partial x^2} = \frac{R_{sTot} l_{seg}^2 J_0}{R_{sTk}} - \frac{16R_{sTot} l_{seg}^2 J_0}{a^2 \pi^2 R_{s(n)}} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \left[\frac{(2k+1) \sin\left((2k+1)\frac{\pi}{a} \cdot x\right) \sin\left((2l+1)\frac{\pi}{b} \cdot y\right)}{(2l+1) \left(\frac{(2k+1)^2}{a^2} + \frac{(2l+1)^2}{b^2}\right)} \right], \quad (4.16)$$

and is shown in Figure 4-4.

The first row of vias that connects the pair to the power-ring have a higher current compared to the other vias. The within-pair via currents, including the first row currents, are shown in Figure 4-5.

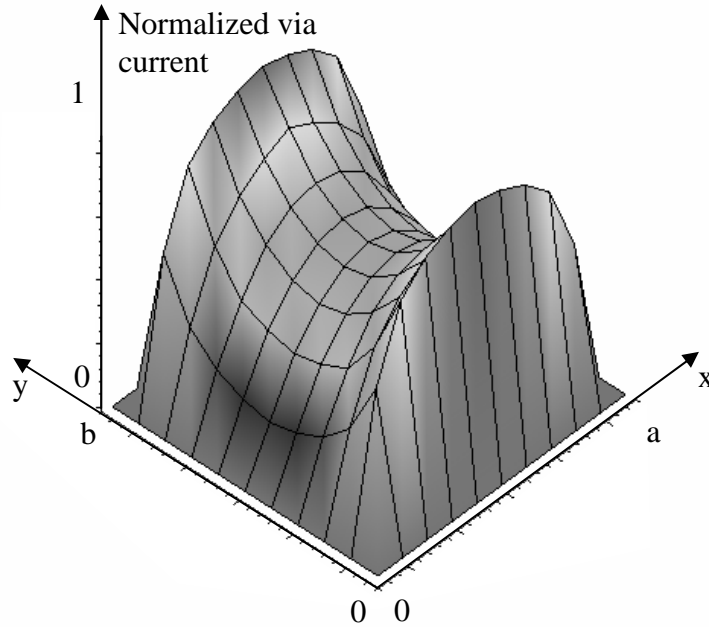


Figure 4-4: Normalized within-pair via current (normalized to its maximum) for a wire-bond package.

The first-row via current is equal to the current at the first segment, which can be calculated from the slope of the IR-drop voltage (4.4).

$$I_x(x=0, y) = \frac{16 \cdot l_{segx} \cdot J_0}{R_{segx} \cdot a \cdot \pi^3} \sum_{l=0}^{\infty} \sum_{k=0}^{\infty} \frac{\sin\left((2l+1)\frac{\pi}{b} \cdot y\right)}{(2l+1) \left(\frac{l_{segx} (2k+1)^2}{R_{segx} l_{segy} a^2} + \frac{l_{segy} (2l+1)^2}{R_{segx} l_{segx} b^2} \right)} \quad (4.17).$$

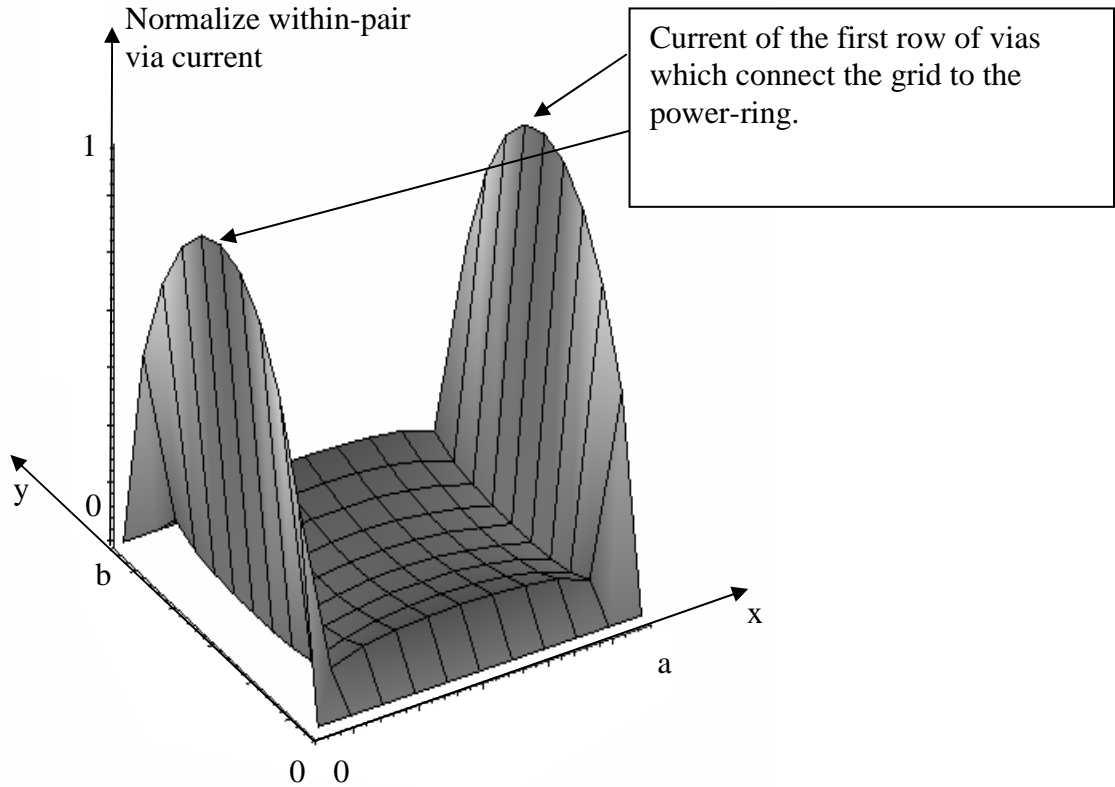


Figure 4-5: Normalized within-pair via current (normalized to its maximum) including the first row of vias that connects the grid to the power-ring have a higher current compared to the other vias.

This current is much higher than the within-pair current of the other vias. If the via current exceeds the maximum current, then extra via should be placed to reduce the current density in those vias and as a result increase their lifetime.

4.7 Within-pair Via Currents for a Flip-chip Package

The within-pair via current for a flip-chip package is calculated from (4.15) and is shown in Figure 4-6 and Figure 4-7. As shown in Figure 4-6, the within-pair via current is larger near the pads. A positive current in Figure 4-6 means that current is passing from the top level to the lower level and a negative current means that current is passing from the lower level to the top level.

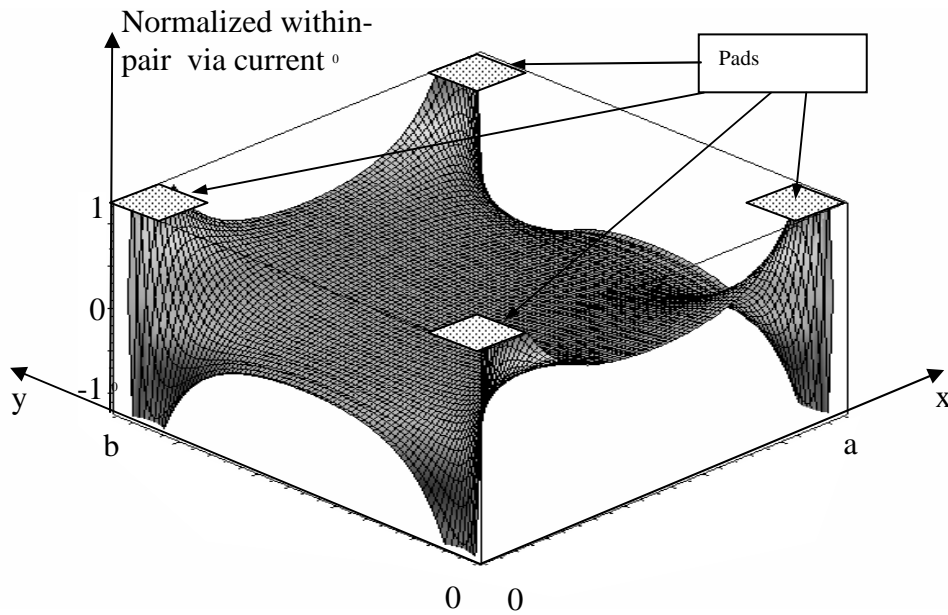


Figure 4-6: Normalized current of within-pair via (normalized to its maximum) for a cell in an Area Array Package. The within-pair via current is larger near the pads.

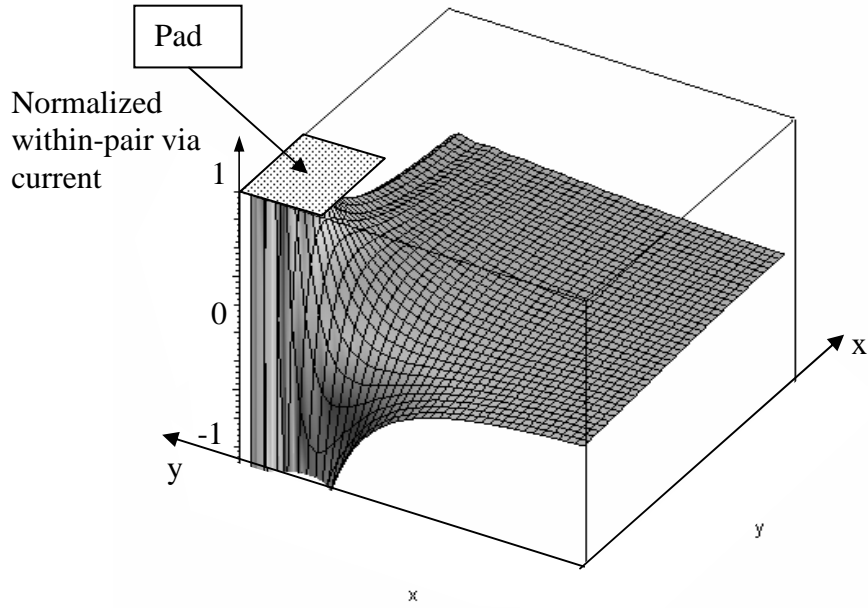


Figure 4-7: Normalized within-pair via (normalized to its maximum) of an area array package near the pads.

The voltage at (x,y) which is near the pad is calculated from (2.51). r_{ref} in (2.51) should be replaced with

$$r_{ref} = \sqrt{x^2 + y^2} . \quad (4.18)$$

In (2.51), for the voltage at (x,y) which is near the pad we have

$$\frac{(r_{ref}^2 - r_{pad}^2)}{A_{cell}} \ll \ln\left(\frac{r_{ref}}{r_{pad}}\right), \quad (4.19)$$

and therefore (2.51) can be simplified as

$$V_{IR} = \frac{R_{sTot} I_{pad}}{2\pi} \ln\left(\frac{\sqrt{x^2 + y^2}}{r}\right), \quad (4.20)$$

where I_{pad} is the current passing through each pad, r is the equivalent radius of the pad.

Calculating the within-pair current (4.15) for the vias near the pads we have

$$I_{Vw}(x, y) = I_{Vb} + \frac{l_{seg}^2}{R_{s(n)}} \frac{\partial^2 V_{IR}(x, y)}{\partial x^2} = I_{Vb} + \frac{R_{sTot} l_{seg}^2 I_{pad} (y^2 - x^2)}{2\pi R_{s(n)} (y^2 + x^2)^2}. \quad (4.21)$$

The maximum via current occurs at the edges of the cell (Figure 4-7) and can be calculated from

$$I_{Vmax}(x_1, y = 0) = I_{Vb} + \frac{R_{sTot} l_{seg}^2 I_{pad}}{2\pi R_{s(n)1} x_1^2}, \quad (4.22)$$

where x_1 is the distance of the nearest via to the center of the pad. Equation (4.22) has been compared to SPICE simulations and has error less than 5%.

Table 4-1: Comparison between simulation and model for I_{Vmax}

	SPICE Simulation	Model
5×5 grid, $R_{seg}=1\Omega$, $l_{seg}=28\mu\text{m}$, $I_{pad}=0.1\text{A}$, $D_{pad}=112\mu\text{m}$	1.46mA	1.71mA
10×10 grid, $R_{seg}=1\Omega$, $l_{seg}=14\mu\text{m}$, $I_{pad}=0.1\text{A}$, $D_{pad}=112\mu\text{m}$	0.57mA	0.61mA
20×20 grid, $R_{seg}=1\Omega$, $l_{seg}=7\mu\text{m}$, $I_{pad}=0.1\text{A}$, $D_{pad}=112\mu\text{m}$	0.19mA	0.18mA

The vias having the maximum and minimum current are shown in Figure 4-8. The vias shown in red have the maximum current ($x=0$ in (4.21)) and the vias shown in yellow have the minimum via current ($x=y$ in (4.21)). If the current in the vias exceeds the maximum tolerable, then extra vias should be placed in parallel to them to reduce the current density in those vias.

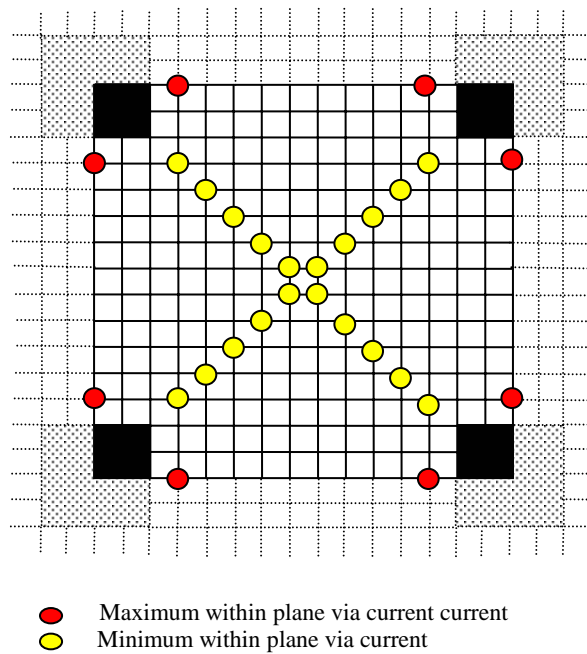


Figure 4-8: Maximum and minimum within-pair via current. The vias shown in red have the maximum current and the vias shown in yellow have the minimum via current.

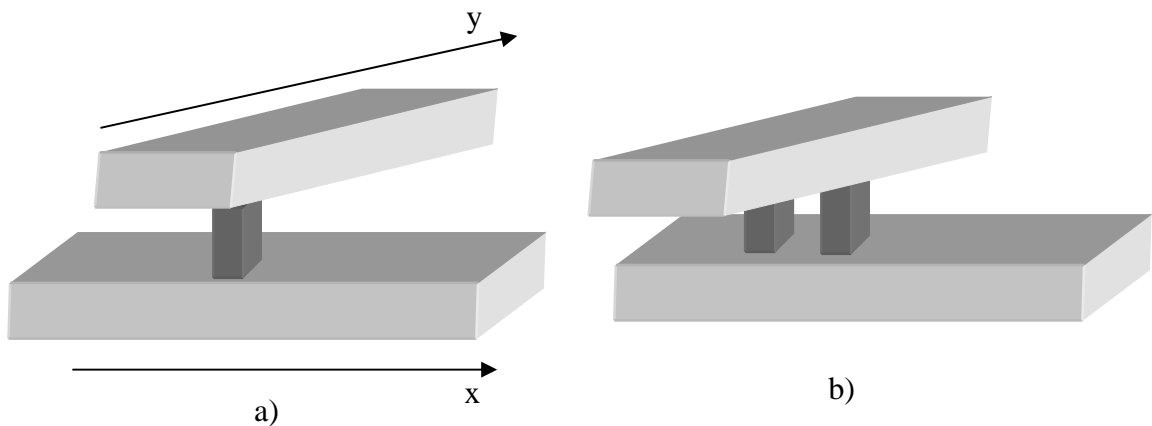


Figure 4-9: Adding extra vias to reduce current density through them: a) shows two segments in x and y direction, b) Extra vias are added to reduce current density in the vias.

4.8 Conclusion

Compact physical models are derived for the direct current is the power distribution network of a high performance microprocessor. These models help designers in the early stages of the design to find locations in the power distribution grid which are susceptible to electromigration. These models will reduce the cost of redesign by predicting the places in the power distribution which have high current densities. Comparisons with SPICE simulations show that they have less than 5% error.

Chapter 5

Substrate Spreading Resistance

5.1 Introduction

The chip substrate is a conductor that makes a parallel path for the current passing through the power distribution network. Figure 5-1 shows the ground grid and the substrate. The substrate is connected to ground through contacts as shown in Figure 5-1. Therefore, it makes a parallel path for the current, and it affects both the simultaneous switching noise and the IR-drop voltage [14], [15].

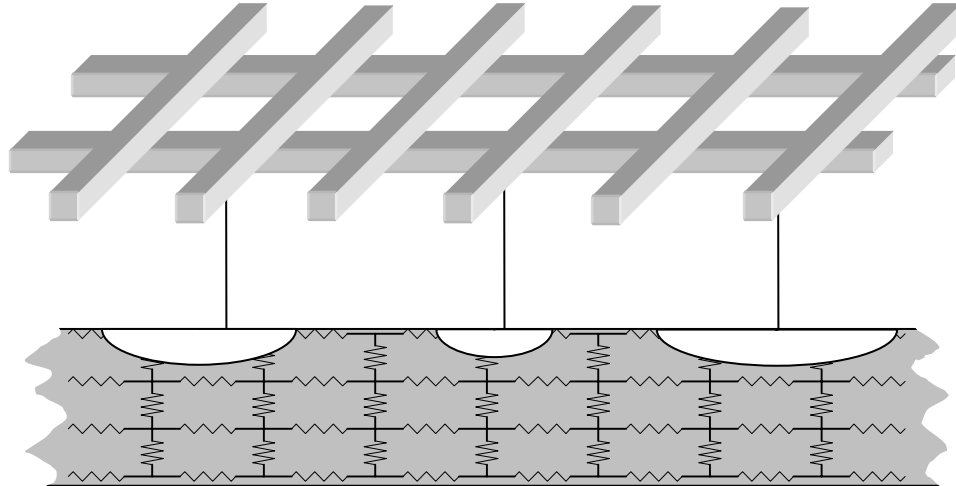


Figure 5-1: The substrate is a distributed resistance making a parallel path for the current passing through the power distribution network.

To model the impact of the substrate on the power supply noise of digital circuits a model is needed for the substrate impedance [14], [15]. This model can also be used to

find the noise caused by digital circuits on the analogue circuits in a mixed signal chip. One method to model the substrate is to divide the substrate into a 3D resistance grid (Figure 5-2.a). This method however, will result in a large number of resistances for a substrate with many contacts. The number of resistances can be reduced by modeling the resistance between any two contacts (Figure 5-2.b). This method will significantly reduce the number of resistances required for modeling the substrate. Models previously derived for the resistance between contacts are either empirical [16], [17], [18] or too complicated with many approximations [19], [20]. New compact physical models are introduced, which enable modeling of the spreading resistance between multiple contacts as a function of the substrate doping, size of the contacts and the distance between them for two kinds of substrates, the p- substrate and the p+ substrate. The p- substrate has uniform doping, and the p+ substrate has a low doping epitaxial layer on a high doping substrate (Figure 5-3).

The calculation of the spreading resistance between two contacts using the capacitance between them is described in Section 5.2. The models for 2D spreading resistances of the p- and p+ substrate are described in Sections 5.3 and 5.4 respectively. The models for the 3D spreading resistances are described in Sections 5.5 and 5.6. In Section 5.7 spreading resistance is calculated for multiple contacts using the models derived in the previous sections.

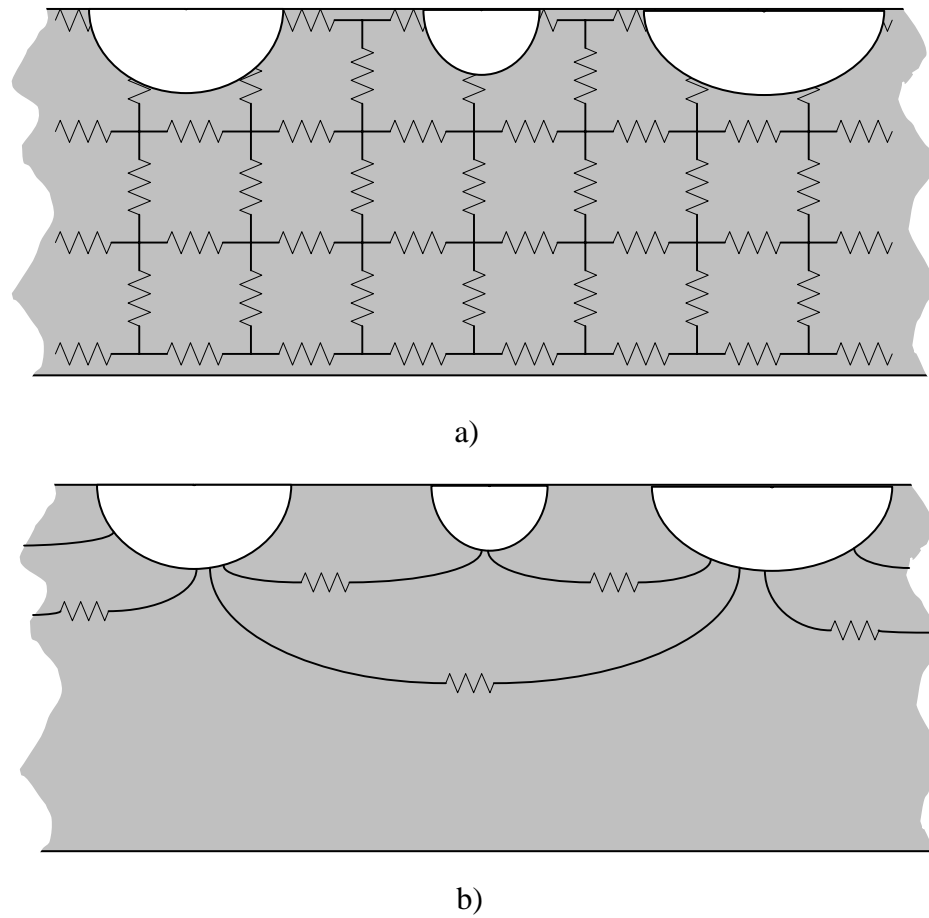


Figure 5-2: Methods to model the substrate resistance: a) the substrate is divided into a distributed 3D resistance, b) the substrate is modeled with resistances between any two contacts.

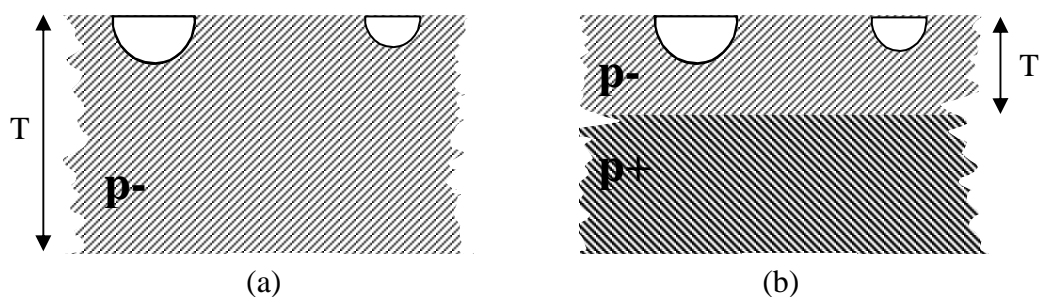


Figure 5-3: Contacts to two different substrates (a) The p^- substrate has uniform doping (b) the p^+ substrate is a low doping epitaxial layer on a high doping substrate.

5.2 Spreading Resistance Calculation

A medium is called homogenous if the dielectric constant and the conductivity of the medium have the same space dependence (independent of space coordinates). The resistance and capacitance between two conductors in a homogenous medium are related as [59]

$$RC = \frac{\varepsilon}{\sigma}, \quad (5.1)$$

where R and C are the resistance and capacitance between the conductors, and ε and σ are the dielectric constant and the conductivity of the medium respectively. Therefore, by calculating the capacitance between two conductors the resistance between them can be calculated. By replacing resistance with capacitance, the current paths in the substrate are replaced by electric field paths (Figure 5-4).

The capacitance between two conductors can be calculated by calculating the voltage potential between them because of their charges

$$C = \frac{q}{V}, \quad (5.2)$$

where V is the voltage difference between the conductors because of the charge q on one of the conductors and $-q$ on the other. Substituting for C in (5.1) by (5.2), the resistance can be calculated as

$$R = \frac{\varepsilon \cdot V}{\sigma \cdot q}. \quad (5.3)$$

Figure 5-3.a and Figure 5-3.b show contacts connected to the p- and the p+ substrates. If their mirror is added to them, the fields are not changed (Figure 5-5); however, their

capacitances are increased by two times. As a result the contact resistances shown in Figure 5-3 are twice the resistance calculated for Figure 5-5,

$$R_{Contact} = \frac{2 \cdot \epsilon \cdot V}{\sigma \cdot q} \quad (5.4)$$

Hence, the contact resistance can be calculated by calculating the voltage difference between the conductors shown in Figure 5-5, because of a charge $+q$ on one of them and a $-q$ on the other.

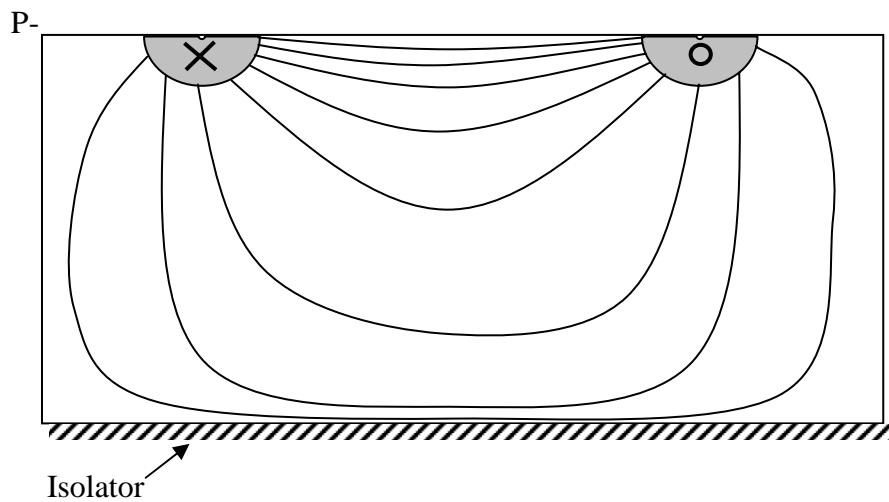


Figure 5-4. The current paths in p- substrate between two contacts. By replacing the contact with charges the paths for current is replaced by electric field paths. The electric field at the insulator surface is parallel to the insulator. The insulator in this case insulates electric field.

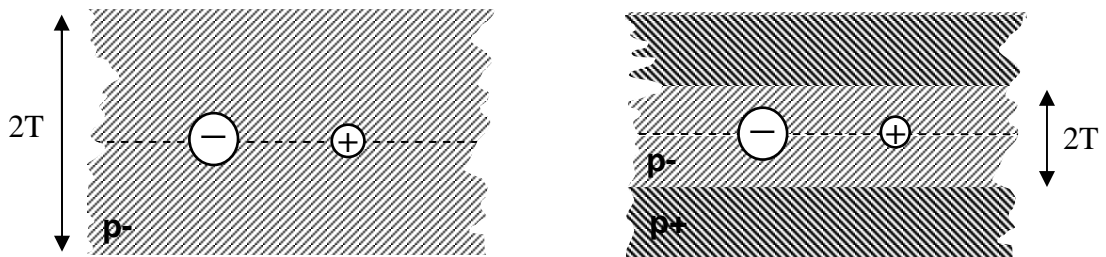


Figure 5-5: Contacts to different substrates. The resistance calculated for this case is half the resistance calculated for Fig.1. (a) p- substrate (b) p+ substrate

5.3 2D Spreading Resistance for p- Substrate

The p- substrate is shown in Figure 5-3.a and its equivalent is shown in Figure 5-5.a. Air at both sides of Figure 5-5.a acts as an insulator. By using the image method used in electromagnetics, the insulator can be omitted by placing a charge with the same charge and same distance at the other side of the insulator. If there are insulators at both sides then they should be replaced by an infinite number of charges as shown in Figure 5-7.

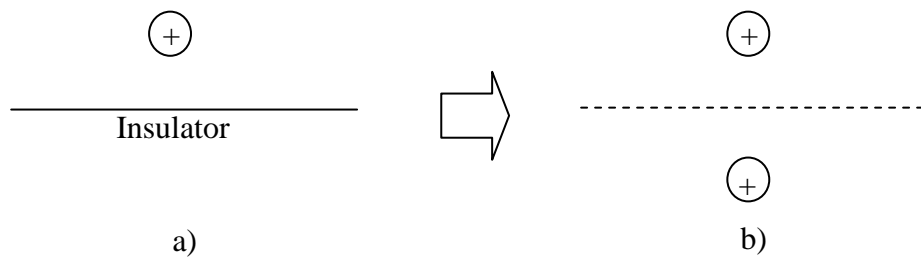


Figure 5-6. Image method. The insulator in part a) can be replaced by another charge at the other side making the same potential contours.

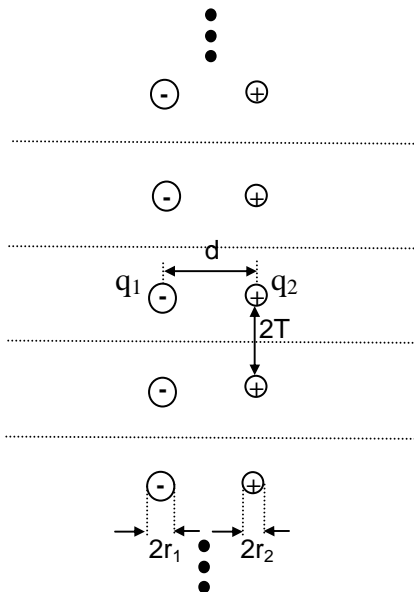


Figure 5-7: Infinite series of charges replacing the two insulators on both sides of Figure 5-5.a.

The next step is to calculate the voltage difference between q_1 and q_2 because of the charges.

The voltage difference between two cylinders with radiuses r_1 and r_2 can be calculated using the image method [68]

$$V = \frac{\rho_\ell}{\pi\epsilon} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{d^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) \right]. \quad (5.5)$$

If the cylinders are far apart, the voltage difference due to one cylinder can be calculated from coulombs law [68]

$$V = \frac{\rho_\ell}{2\pi\epsilon_0} \int_D^{r_1} \frac{dr}{r} = \frac{\rho_\ell}{2\pi\epsilon_0} \ln \left(\frac{r_1}{d} \right), \quad (5.6)$$

where d is the center-to-center distance between cylinders and r_1 is the radius of the cylinder.

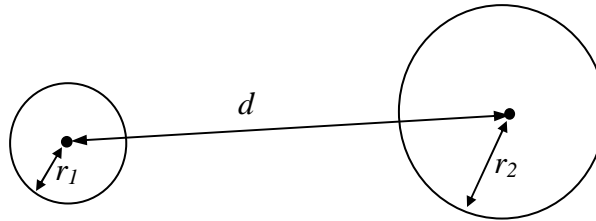


Figure 5-8. Two cylinders with radius r_1 and r_2 . The distance between the centers is d .

The voltage difference because of charges q_1 and q_2 (V_1) can be calculated from (5.5).

The radius of the cylinders (r_1 and r_2) are much smaller than the substrate thickness (T) and therefore the voltage difference due to other charges (V_2) can be calculated from(5.6).

Adding the voltages due to all charges

$$V = V_1 + V_2, \quad (5.7)$$

or

$$V = \frac{\rho_\ell}{2\pi\epsilon_0} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{d^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) + 2 \left(\begin{aligned} &\ln(2T) - \ln(\sqrt{d^2 + 4T^2}) + \ln(4T) - \ln(\sqrt{d^2 + 16T^2}) \\ &+ \ln(6T) - \ln(\sqrt{d^2 + 36T^2}) + \dots \end{aligned} \right) \right], \quad (5.8)$$

can be rewritten as

$$V = \frac{\rho_\ell}{2\pi\epsilon_0} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{d^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) + \left(\begin{aligned} &\ln(4T^2) - \ln(d^2 + 4T^2) + \ln(16T^2) - \ln(d^2 + 16T^2) \\ &+ \ln(36T^2) - \ln(d^2 + 36T^2) + \dots \end{aligned} \right) \right], \quad (5.9)$$

and simplified as

$$V = \frac{\rho_\ell}{2\pi\epsilon_0} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{d^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) - \left(\ln \left(1 + \frac{d^2}{4T^2} \right) + \ln \left(1 + \frac{d^2}{16T^2} \right) + \ln \left(1 + \frac{d^2}{36T^2} \right) + \dots \right) \right] \quad (5.10)$$

or

$$V = \frac{\rho_\ell}{2\pi\epsilon_0} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{d^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) - \left(\ln \left[\left(1 + \frac{d^2}{4T^2} \right) \left(1 + \frac{d^2}{16T^2} \right) \left(1 + \frac{d^2}{36T^2} \right) \dots \right] \right) \right] \quad (5.11)$$

Rewriting (5.10) we have

$$V = \frac{\rho_\ell}{\pi\epsilon} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{d^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) + \ln \left[\prod_{k=1}^{\infty} \left(1 + \frac{d^2}{4k^2 T^2} \right) \right] \right] \quad (5.12)$$

where d is the distance between the contacts, T is the thickness of the substrate, ρ_ℓ is the charge per unit length of the cylinder [coulombs/cm], and r_1 and r_2 are the radii of the contacts,

$$\rho_\ell = \frac{q}{\ell}, \quad (5.13)$$

where ℓ is the length of the cylinder. The contact resistance can be calculated using (5.4) and (5.12)

$$R_{Contact} = \frac{2}{\pi\sigma\ell} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{d^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) + \ln \left[\prod_{k=1}^{\infty} \left(1 + \frac{d^2}{4k^2 T^2} \right) \right] \right]. \quad (5.14)$$

The series in the above equation can be simplified as [60]

$$\left(\frac{\pi \cdot d}{2T} \right) \cdot \prod_{k=1}^{\infty} \left(1 + \frac{d^2}{4k^2 T^2} \right) = \sinh \left(\frac{\pi \cdot d}{2T} \right). \quad (5.15)$$

As a result the resistance between two cylindrical contacts of length ℓ can be calculated

$$R_{Contacts} = \frac{2}{\pi\sigma\ell} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{d^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) + \ln \left[\frac{\sinh \left(\frac{\pi \cdot d}{2T} \right)}{\left(\frac{\pi \cdot d}{2T} \right)} \right] \right]. \quad (5.16)$$

Figure 5-9 shows a comparison between the model and simulation done by Raphael [61].

As shown the model has less than 1% error with the simulations done by Raphael.

The model shows that for short distances, the resistance increases very rapidly. The rate of increase of the resistance is reduced for longer distances. Therefore, in this case the noise is not only a function of the area of the noise source but also a function of the distance from the noise source.

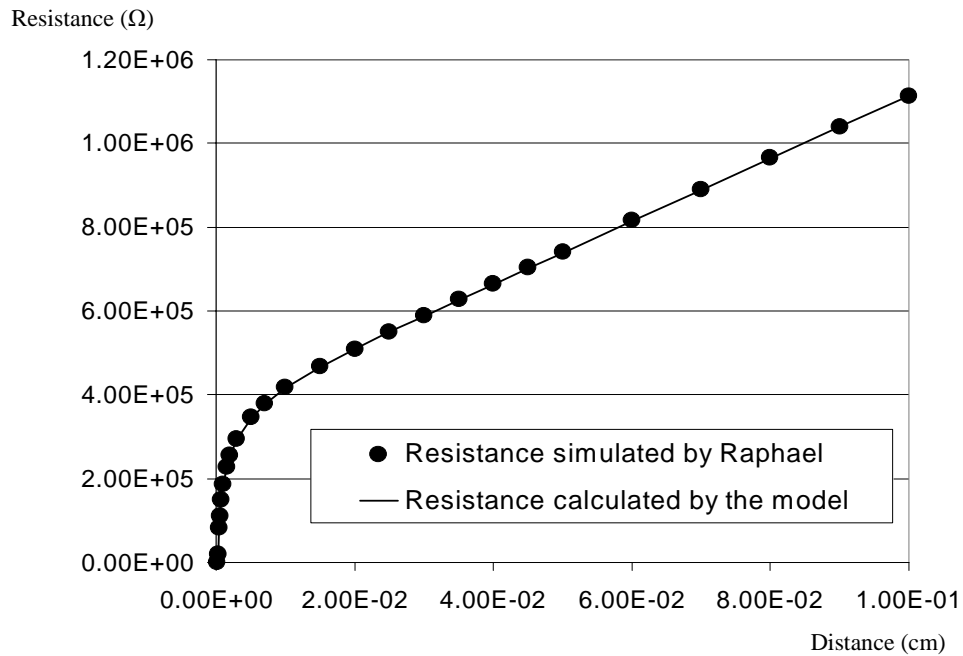


Figure 5-9: Substrate resistance between two cylinders 1 μm long as a function of the distance between them in a p- substrate. ($r_1=1\mu\text{m}$, $r_2=2\mu\text{m}$, $T=200\mu\text{m}$, $\sigma =0.067(\Omega\text{-cm})^{-1}$)

5.4 2D Spreading Resistance for p+ Substrate

The p+ substrate is made by a low doping epitaxial layer on a high doping substrate (Figure 5-3). The substrate in this case has a very low resistance compared to the resistance of the epitaxial layer; therefore it can be modeled as a good conductor. Using the image technique, the conductors can be replaced by an infinite number of charges as shown in Figure 5-11.

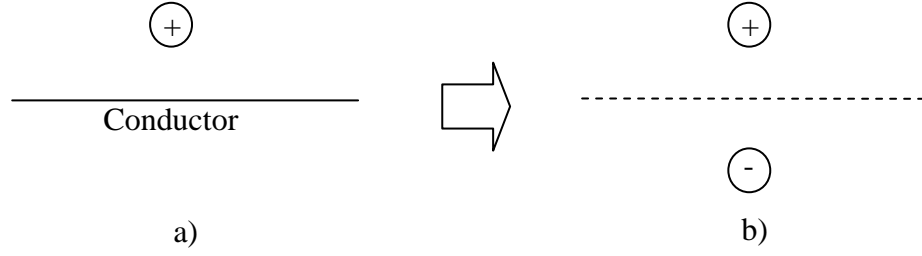


Figure 5-10. Image method. The insulator in part a) can be replaced by another charge at the other side making the same potential contours.

The voltage difference because of charges q_1 and q_2 (V_1) can be calculated from (5.5).

The radii of the cylinders (r_1 and r_2) are much smaller than the substrate thickness (T) and therefore the voltage difference due to other charges (V_2) can be calculated from (5.6).

Adding the voltages due to all charges

$$V = \frac{\rho_\ell}{2\pi\epsilon_0} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{D^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) + 2 \left(\begin{array}{l} -\ln(2T) + \ln(\sqrt{d^2 + 4T^2}) + \ln(4T) - \ln(\sqrt{d^2 + 16T^2}) \\ -\ln(6T) + \ln(\sqrt{d^2 + 36T^2}) + \dots \end{array} \right) \right], \quad (5.17)$$

or

$$V = \frac{\rho_\ell}{2\pi\epsilon_0} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{D^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) + \left(\begin{array}{l} -\ln(4T^2) + \ln(d^2 + 4T^2) + \ln(16T^2) - \ln(d^2 + 16T^2) \\ -\ln(36T^2) + \ln(d^2 + 36T^2) + \dots \end{array} \right) \right], \quad (5.18)$$

can be simplified to

$$V = \frac{\rho_\ell}{2\pi\epsilon_0} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{D^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) + \left(\ln \left(1 + \frac{d^2}{4T^2} \right) - \ln \left(1 + \frac{d^2}{16T^2} \right) + \ln \left(1 + \frac{d^2}{36T^2} \right) - \dots \right) \right], \quad (5.19)$$

or

$$V = \frac{\rho_\ell}{2\pi\epsilon_0} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{D^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) - \ln \left[\frac{\left(1 + \frac{d^2}{4T^2} \right) \left(1 + \frac{d^2}{36T^2} \right) \dots}{\left(1 + \frac{d^2}{16T^2} \right) \left(1 + \frac{d^2}{64T^2} \right) \dots} \right] \right], \quad (5.20)$$

Rewriting (5.20) we have

$$V = \frac{\rho_\ell}{\pi\epsilon} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{D^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) - \ln \left[\prod_{k=1}^{\infty} \frac{1 + \frac{d^2}{4(2k-1)^2 T^2}}{1 + \frac{d^2}{16k^2 T^2}} \right] \right]. \quad (5.21)$$

Substituting (5.21) in (5.4) the contacts spreading resistance can be calculated

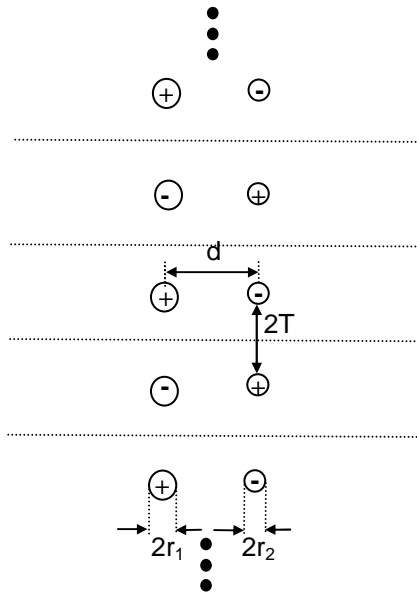


Figure 5-11: Infinite series of charges replacing the two conductors on both sides of Figure 5-5.b.

$$R_{Contact} = \frac{2}{\pi\sigma\ell} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{D^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) - \ln \left[\prod_{k=1}^{\infty} \frac{1 + \frac{d^2}{4(2k-1)^2 T^2}}{1 + \frac{d^2}{16k^2 T^2}} \right] \right]. \quad (5.22)$$

The series can be simplified as [60]

$$\prod_{k=1}^{\infty} \left(\frac{1 + \frac{d^2}{4(2k-1)^2 T^2}}{1 + \frac{d^2}{16k^2 T^2}} \right) = \frac{\pi \cdot d}{4T} \coth \left(\frac{\pi \cdot d}{4T} \right). \quad (5.23)$$

Replacing it in (5.22) the spreading resistance of two cylindrical contacts with length ℓ can be calculated

$$R_{Contacts} = \frac{2}{\pi \sigma \ell} \left[\frac{1}{2} \cosh^{-1} \left(\frac{1}{2} \left(\frac{D^2}{r_1 r_2} - \frac{r_1}{r_2} - \frac{r_2}{r_1} \right) \right) - \ln \left[\frac{\pi \cdot d}{4T} \coth \left(\frac{\pi \cdot d}{4T} \right) \right] \right]. \quad (5.24)$$

Figure 5-12 shows the resistances calculated from simulation using Raphael and from the model. As seen in Figure 5-12 error using the model is less than 1%.

Results show that the resistance increases as the distance between the contacts is increased until it saturates. For long distances, the resistance is constant and is not a function of the distances between the contacts, because in this case most of the current passes straight down to the low resistance substrate and then passes through the low resistance substrate. Therefore because of the low resistivity of the p+ substrate the resistance increases a little, as the distance between the contacts increase. Noise for the p+ substrate is proportional to the size (r) of the noise source and not the distance between the noise source and the victim. One technique to reduce noise is to add ground contacts to the substrate. The model shows that the noise reduction because of the ground connections to the substrate is proportional to the area of the connections and not to the distance between the connection and the noise source unless the distance between them is too small.

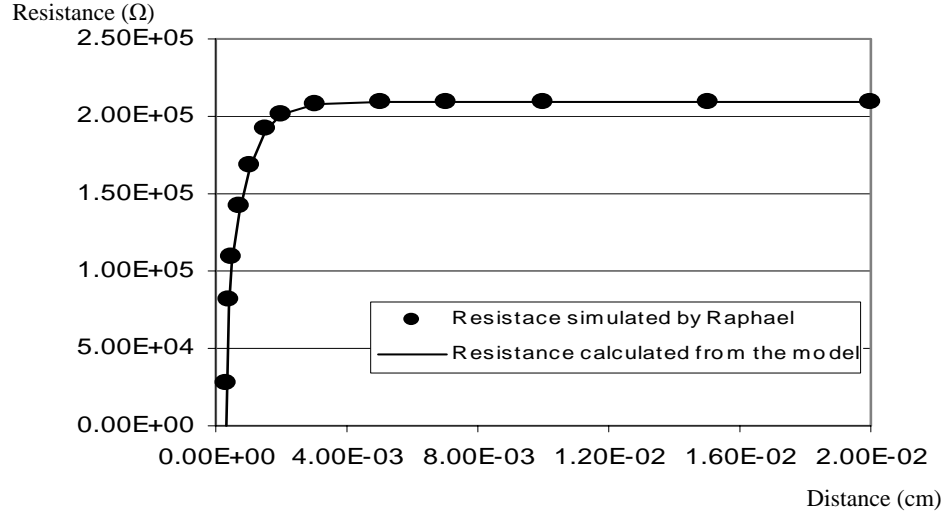


Figure 5-12: Substrate resistance between two cylinders 1 μm long as a function of the distance between them in a p+ substrate. ($r_1=1\mu\text{m}$, $r_2=2\mu\text{m}$, $T=10\mu\text{m}$, $\sigma=0.067(\Omega\text{-cm})^{-1}$)

5.5 3D Spreading Resistance for p- Substrate

The 3D spreading resistance modeled in this part is the resistance between two half spheres on a p- substrate. Using the same mirror technique which was used for the 2D case the insulators can be removed by replacing them with an infinite number of charges.

The resistance between the two spheres with different radiuses (R_{sph}) in an infinite space can be calculated from the following group of equations [61]

$$C_{self1} = 4\pi\epsilon r_1 r_2 \left[\frac{1}{r_2} - \frac{1}{d} + \frac{r_1}{d^2 - r_2^2} - \dots \right], \quad (5.25)$$

$$C_{self2} = 4\pi\epsilon r_1 r_2 \left[\frac{1}{r_1} - \frac{1}{d} + \frac{r_2}{d^2 - r_1^2} - \dots \right], \quad (5.26)$$

$$C_{mutual} = 4\pi\epsilon r_1 r_2 \left[\frac{1}{d} + \frac{r_1 r_2}{d^3 - d(r_1^2 + r_2^2)} - \dots \right], \quad (5.27)$$

$$R_{sph} = \frac{\varepsilon}{\sigma} \left(\frac{C_{self1} C_{self2}}{C_{self1} + C_{self2}} + C_{mutual} \right)^{-1}. \quad (5.28)$$

The voltage difference because of charges q_1 and q_2 can be calculated from (5.25) to (5.28) and the voltage due to a charge between two nodes which are at a distance d_1 and d_2 can be calculated from

$$V = \frac{\rho_\ell}{4\pi\varepsilon_0} \int_d^{r_i} \frac{dr}{r^2} = \frac{\rho_\ell}{4\pi\varepsilon_0} \left(\frac{1}{d_1} - \frac{1}{d_2} \right) \quad (5.29)$$

Adding the voltages due to all charges

$$V = \frac{q}{4\pi\varepsilon_0} \left[\frac{2}{2T} + \frac{2}{4T} + \frac{2}{6T} + \dots - \frac{2}{\sqrt{d^2 + 4T^2}} - \frac{2}{\sqrt{d^2 + 16T^2}} - \frac{2}{\sqrt{d^2 + 36T^2}} - \dots \right] \quad (5.30)$$

or

$$V = \frac{q}{4\pi\varepsilon_0} \left[\frac{1}{T} \sum_{k=1}^{\infty} \frac{1}{k} - 2 \sum_{k=1}^{\infty} \frac{1}{\sqrt{d^2 + 4k^2 T^2}} \right] \quad (5.31)$$

The voltage caused by the infinite number of charges can be calculated from

$$V = \frac{q}{2\pi\varepsilon} \left[\frac{1}{T} \sum_{k=1}^{\infty} \frac{1}{k} - 2 \sum_{k=1}^{\infty} \frac{1}{\sqrt{d^2 + 4k^2 T^2}} \right]. \quad (5.32)$$

Therefore that part of resistance which is because of the infinite charges is

$$R_{series} = \frac{1}{\pi\sigma} \left[\frac{1}{T} \sum_{k=1}^{\infty} \frac{1}{k} - 2 \sum_{k=1}^{\infty} \frac{1}{\sqrt{d^2 + 4k^2 T^2}} \right]. \quad (5.33)$$

The total resistance can be calculated by adding (5.28) and (5.33)

$$R_{Contact} = R_{Sph} + \frac{1}{\pi\sigma} \left[\frac{1}{T} \sum_{k=1}^{\infty} \frac{1}{k} - 2 \sum_{k=1}^{\infty} \frac{1}{\sqrt{d^2 + 4k^2 T^2}} \right]. \quad (5.34)$$

Figure 5-13 shows the comparison between this model and simulation done by Raphael as shown in Figure 5-13. The error between the model and the simulations is less than 5%. Despite the 2D model of the p- substrate where the resistance increased as the

$$V = \frac{q}{4\pi\epsilon_0} \left[-\frac{2}{2T} + \frac{2}{4T} - \frac{2}{6T} + \dots + \frac{2}{\sqrt{d^2 + 4T^2}} - \frac{2}{\sqrt{d^2 + 16T^2}} + \frac{2}{\sqrt{d^2 + 36T^2}} - \dots \right] \quad (5.35)$$

or

$$V = \frac{q}{4\pi\epsilon_0} \left[\frac{1}{T} \sum_{k=1}^{\infty} \left(\frac{1}{2k} - \frac{1}{2k-1} \right) + 2 \sum_{k=1}^{\infty} \left(\frac{1}{\sqrt{d^2 + 4(2k-1)^2 T^2}} - \frac{1}{\sqrt{d^2 + 16k^2 T^2}} \right) \right] \quad (5.36)$$

The resistance between the spheres is the same as (5.28). The voltage between the two contacts because of the infinite series is

$$V = \frac{q}{2\pi\epsilon} \left[\frac{1}{T} \sum_{k=1}^{\infty} \left(\frac{1}{2k} - \frac{1}{2k-1} \right) - 2 \sum_{k=1}^{\infty} \left(\frac{1}{\sqrt{d^2 + 4(2k-1)^2 T^2}} - \frac{1}{\sqrt{d^2 + 16k^2 T^2}} \right) \right]. \quad (5.37)$$

Therefore the part of the resistance which is because of the infinite series is

$$R_{series} = \frac{1}{\pi\sigma} \left[\frac{1}{T} \sum_{k=1}^{\infty} \left(\frac{1}{2k} - \frac{1}{2k-1} \right) - 2 \sum_{k=1}^{\infty} \left(\frac{1}{\sqrt{d^2 + 4(2k-1)^2 T^2}} - \frac{1}{\sqrt{d^2 + 16k^2 T^2}} \right) \right]. \quad (5.38)$$

Therefore the total resistance can be calculated from

$$R_{Contact} = R_{Sph} + \frac{1}{\pi\sigma} \left[\frac{1}{T} \sum_{k=1}^{\infty} \left(\frac{1}{2k} - \frac{1}{2k-1} \right) - 2 \sum_{k=1}^{\infty} \left(\frac{1}{\sqrt{d^2 + 4(2k-1)^2 T^2}} - \frac{1}{\sqrt{d^2 + 16k^2 T^2}} \right) \right]. \quad (5.39)$$

Figure 5-14 shows the resistance between two contacts on a p+ substrate versus the distance between them. As shown in Figure 5-14 the results have less than 5% error. It also shows that the resistance saturates as the distance between the contacts increases. In other words, when there is a long distance from the noise source, the resistance between the source noise and the victim saturates. Therefore, noise does not change as the distance

from the source noise is more than a certain value (more than 20 μm for the contact shown in Figure 5-14).

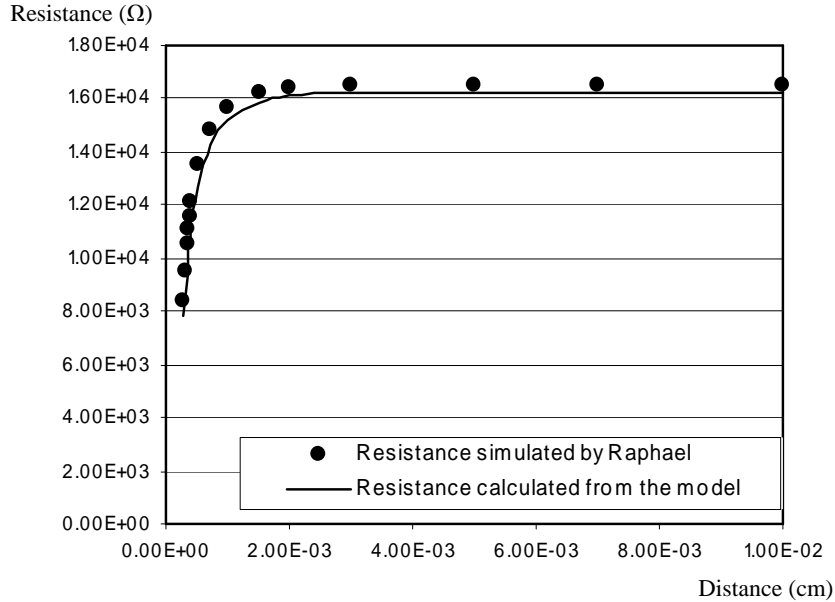


Figure 5-14: Substrate resistance as a function of the distance between the contacts for two spheres in a p+ substrate. ($r_1=1\mu\text{m}$, $r_2=2\mu\text{m}$, $T=10\mu\text{m}$, $\sigma=0.067(\Omega\text{-cm})^{-1}$)

5.7 Spreading resistance calculation for multiple contacts

Figure 5-15 shows part of a substrate with n contacts. One of the contacts is connected to ground and the voltages of the other contacts are measured relative to ground. Since the relation between voltage and current is linear we may write the following set of $n-1$ equations relating the voltages and the current of the n contacts.

$$\begin{pmatrix} v_1 \\ v_2 \\ \vdots \\ v_{n-1} \end{pmatrix} = \begin{pmatrix} r_{11} & r_{12} & \cdots & r_{1(n-1)} \\ r_{21} & r_{22} & & \vdots \\ \vdots & & & \\ r_{(n-1)1} & \cdots & & r_{(n-1)(n-1)} \end{pmatrix} \times \begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_{n-1} \end{pmatrix}, \quad (5.40)$$

or

$$\mathbf{v} = \mathbf{r} \times \mathbf{i} \quad (5.41)$$

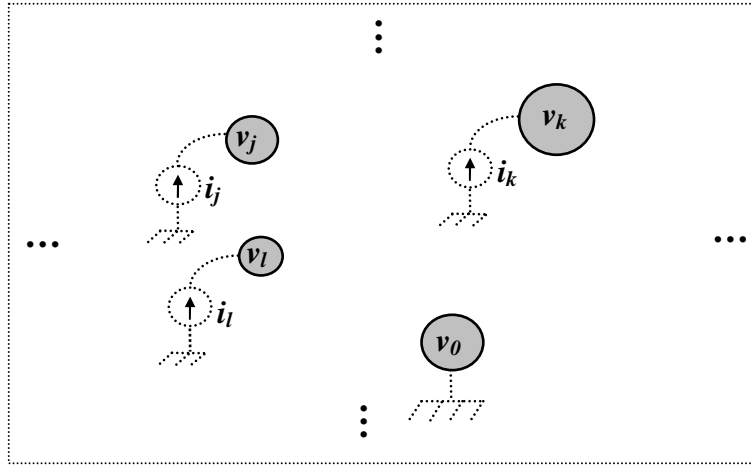


Figure 5-15: Multiple contacts on the substrate. One of the contacts is connected to ground and the voltages of the other contacts are measured relative to ground.

where v_j is the voltage of contact j , i_j is the current going into contact j and r_{jk} can be calculated from

$$r_{jk} = \begin{cases} R_{j0} & \text{if } j = k \\ \frac{1}{2}(R_{j0} + R_{k0} - R_{jk}) & \text{if } j \neq k \end{cases} \quad (5.42)$$

where R_{jk} is the resistance calculated by the model between nodes j and k . Using these equations, the voltage of each contact can be calculated in a substrate with multiple contacts.

5.8 Conclusion

The substrate makes a parallel path for the power distribution network, affecting both IR-drop and simultaneous switching noise (SSN). New compact physical models for 2D

and 3D spreading resistances are introduced to calculate the substrate resistance between multiple contacts for two different substrates (p- and p+). Results show that there is less than 5% error between the model and the simulation done with Raphael.

Chapter 6

Supply Noise Effect on Noise Margin

6.1 Introduction

To have a single model for all sources of noise, a model is needed which enables us to model the input noise and the supply noise of a digital circuit at the same time. Noise margin is the maximum noise voltage that a circuit can tolerate at its input without resulting in a false output. Different models have been introduced for the noise margin of different logic gates [66]. These models can be expressed as

$$V_{NM} = f(V_{DD}, V_{th}, W, L, \dots), \quad (6.1)$$

where V_{DD} is the supply voltage, V_{th} is the threshold voltage of the transistors, W is the Width and L is the length of the transistors. These models are derived for a constant supply voltage and the supply noise is not considered in the models [66]. In this chapter of the thesis new techniques are introduced to include supply noise in the noise margin models. The supply noise in these models is divided into two parts: Part of the supply noise can be modeled as input noise and the other part of it can be modeled as change in the supply voltage V_{DD} , which reduces the noise margin of the circuit. The models are derived for two generic types of logic gates which are very common. These models can be used to model supply noise for other types of gates too. Figure 6-1 shows the most common types of logic gates: static and domino logic [1].

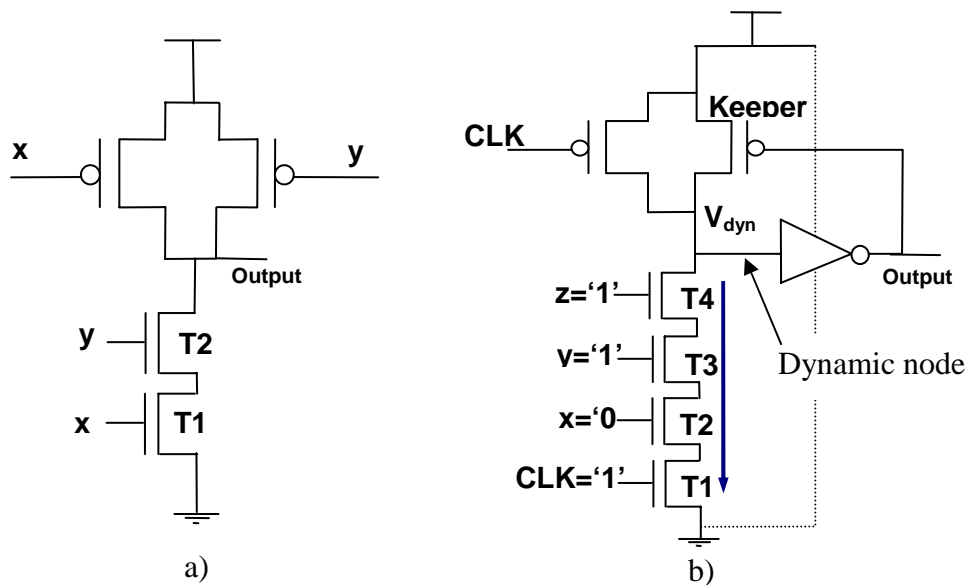


Figure 6-1: Typical static and domino logic circuits, a) A two-input static NAND gate. b) A Three-input domino NAND gate.

There are two sources of supply noise: simultaneous switching noise (SSN) and IR-drop. Simultaneous switching noise will be modeled in Section 6.2. In Section 6.3, the simultaneous switching noise models will be applied to domino logic circuits. IR-drop will be modeled and then applied to domino logic circuits in Sections 6.4 and 6.5 respectively. Then the models derived in Sections 6.3 and 6.5 for the simultaneous switching noise and IR-drop will be applied at the same time to domino logic circuits in Section 6.6.

6.2 Model for Transferring Simultaneous Switching Noise to the Input

The simultaneous switching noise might cause the supply voltage to increase or decrease. Models will be derived to transfer simultaneous switching noise from the

supply to the input of a gate, enabling us to model both source noises (signal noise and supply noise) at the same time. Two cases have been considered for two gates connected to each other. In the first case the gates are far from each other and therefore, the power and ground of the two gates change independently due to simultaneous switching noise. The worst case simultaneous switching noise is shown in Figure 6-2.a. As shown the power supply and ground voltage can independently change due to simultaneous switching noise (ΔV_{SSN}) and are not correlated. The simultaneous switching noise for this case can be transferred to its input as shown in Figure 6-2.b.

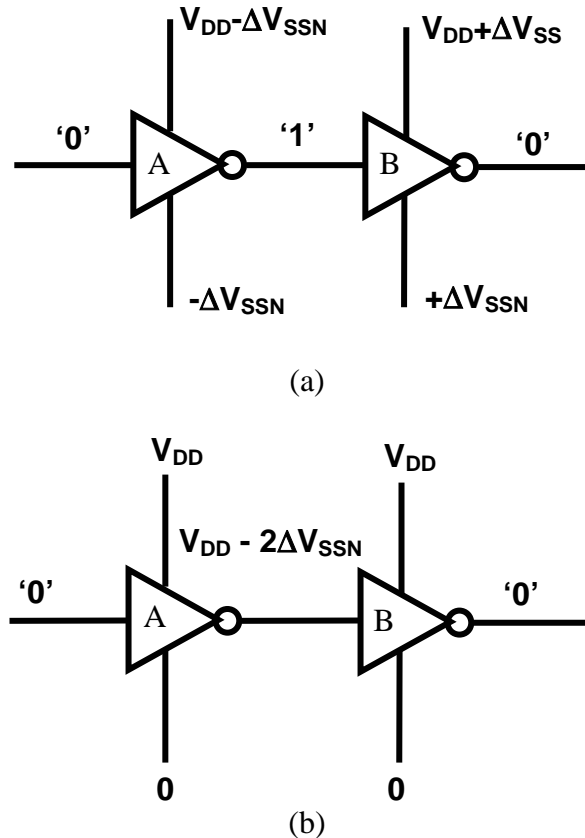


Figure 6-2: Simultaneous switching noise transfer model for two gates which are far apart on the chip (These models can be used for any type of gate such as NAND, NOR...). In this case the supply voltages can change because of simultaneous switching noise independently: (a) Worst case simultaneous switching noise for two circuits with uncorrelated powers and grounds; (b) equivalent circuit model for the circuit shown in part (a).

The noise margin for the gate B can be calculated by applying the supply voltage and noise in the input of the gate to (6.1)

$$V_{NM} = f(V_{DD}, V_{th}, W, L, \dots) - 2\Delta V_{SSN} \quad (6.2)$$

The second case is shown in Figure 6-3. In this case the circuits are near and therefore the supply and simultaneous switching noise voltages of the two circuits are the same. The worst case is shown in Figure 6-3.a. The simultaneous switching noise can be transferred to the input as shown in Figure 6-3.b. The noise margin for the gate B can be calculated by applying the supply voltage and noise in the input of the gate to (6.1)

$$V_{NM} = f(V_{DD} - 2\Delta V_{SSN}, V_{th}, W, L, \dots) \quad (6.3)$$

The worst case supply noise happens when the gates are far apart. Therefore, when there is no information about the locations of the two gates with respect to each other, the worst case noise is calculated assuming that they are far apart.

6.2.1. Example for calculating the noise margin of two inverters assuming simultaneous switching noise

Two inverters are shown in Figure 6-3.b. The inverters near each other. The threshold voltage of gate B is calculated assuming simultaneous switching noise. The saturation current for a long channel NFET transistor and the PFET transistor used in the inverter is calculated from [66]

$$I_{Satn} = \frac{\beta_n}{2} (V_{GS} - V_{thn})^2, \quad (6.4)$$

and

$$I_{Satp} = \frac{\beta_p}{2} (V_{GS} - V_{thp})^2, \quad (6.5)$$

where V_{thn} and V_{thp} are the threshold voltages of the NFET and the PFET transistors, V_{GS} is the voltage difference between the gate and the source and β_n and β_p are device parameters defined by the transistor technology and size [66].

The noise margin of an inverter gate without any supply noise can be calculated from [66]

$$V_{NM} = \frac{V_{DD} - |V_{thp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{thn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}. \quad (6.6)$$

The inverters are near each other; therefore the new noise margin can be calculated by applying (6.3) to (6.6) and is equal to

$$V_{NM} = \frac{V_{DD} - 2\Delta V_{SSN} - |V_{thp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{thn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}. \quad (6.7)$$

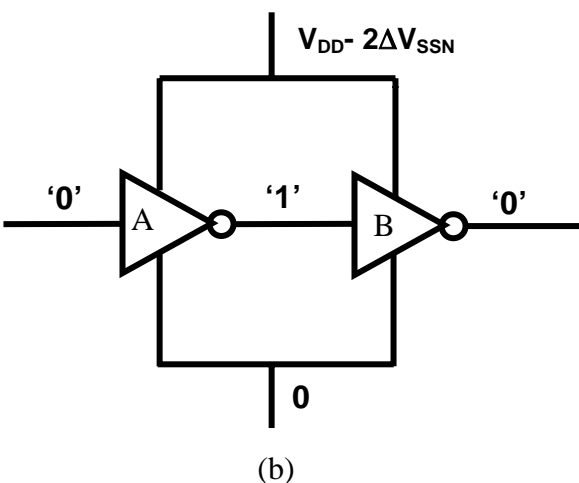
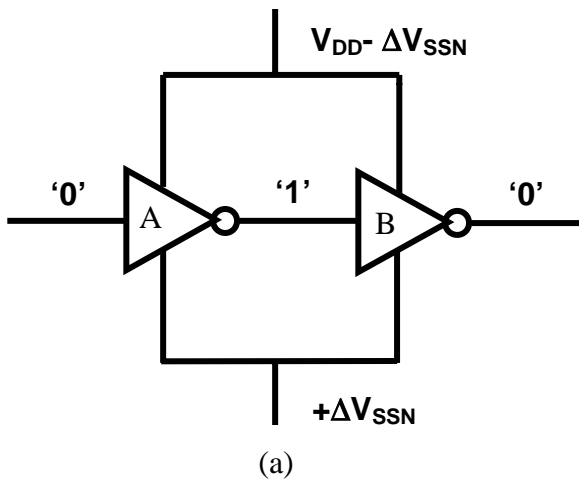


Figure 6-3: Simultaneous switching noise transfer model for two gates which near on the chip (These models can be used for any gate, In this figure inverters are shown). In this case the supply voltages of both gates change the same, because of simultaneous switching noise. (a) Worst case simultaneous switching noise for two circuits with correlated power supply and ground voltages. (b) equivalent circuit model for the circuit shown in part (a).

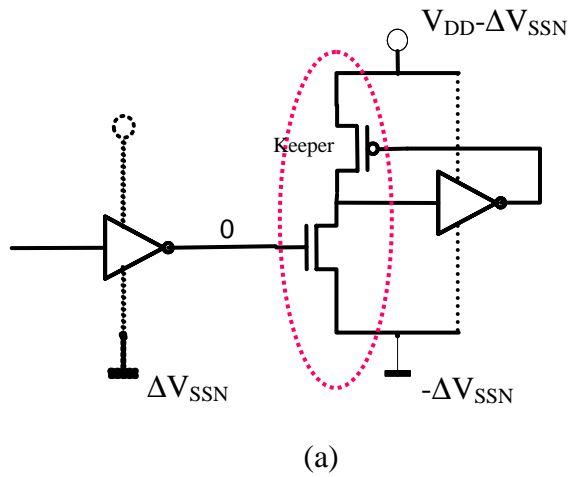
6.3 Simultaneous Switching Noise Model for Domino Logic Circuits

A three input domino logic and gate is shown in Figure 6-1.b. It operates in two phases defined by the clock signal (CLK). The first phase is when CLK='0'. In this phase the dynamic node is charged to V_{DD} . The second phase is called evaluation phase (CLK='1'). In this phase depending on the input the dynamic either remains as '1' or is

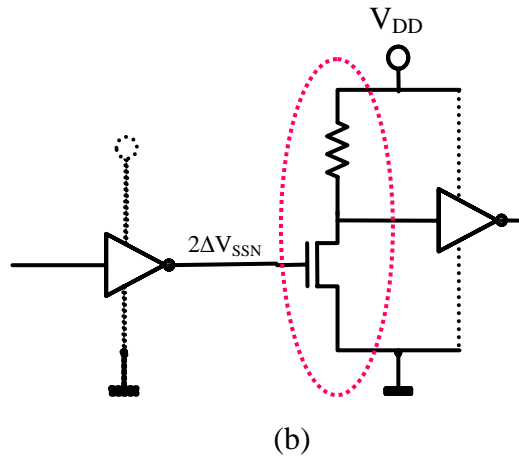
discharged to '0' [66] . The advantage of this kind of logic circuit relative to static logic circuit is speed, however it suffers from a lower noise margin compared to static logic circuits. A noise might discharge the dynamic node and result in an incorrect output.

Noise in the input or the power supply of a domino gate causes the domino node to be discharged and may result in an incorrect output. Applying the techniques introduced in Section 6.2 to a domino logic gate, enables us to model the supply noise and signal noise for these kinds of circuits.

The supply noise should be modeled for two parts of a domino logic circuit: the dynamic node and the input. The dynamic node and the output inverter in a domino logic are located near each other and therefore their supply noise voltages are the same. The domino logic input, however, comes from another gate. Therefore, the worst case input noise for a domino logic circuit is modeled assuming the domino gate and the gate driving it are far apart and their supply voltages can change independently. Figure 6-4 shows the worst case for the input signal. In this case the keeper is in the linear region and therefore can be replaced with an equivalent resistor (Figure 6-4.b). Transferring the noise to the inputs, the worst case noise for the input is shown in Figure 6-4.b



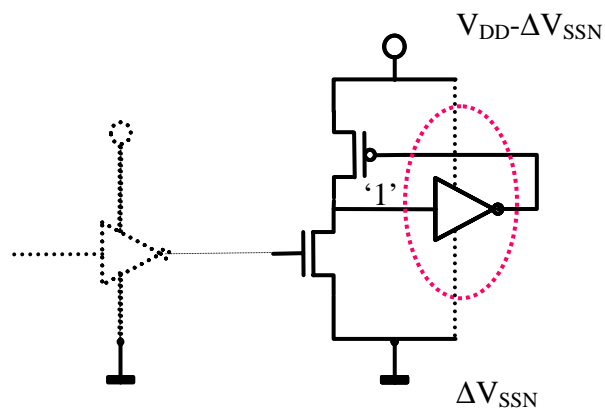
(a)



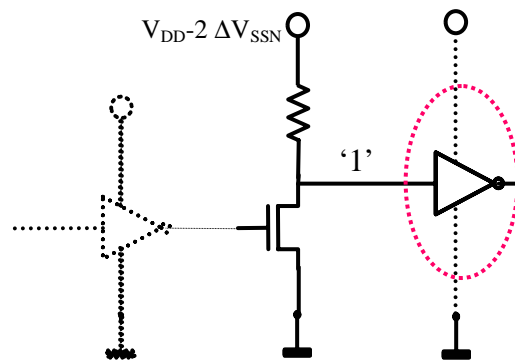
(b)

Figure 6-4: Simultaneous switching noise model for the input of a domino logic circuit: a) Worst case simultaneous switching noise for the input of a domino logic circuit; b) Equivalent model for transferring simultaneous switching noise to the input of circuit shown in part (a).

The dynamic node is usually near the output inverter, and therefore the worst case supply noise for a domino logic gate is shown in Figure 6-5. Using the techniques introduced in Section 6.2 (Figure 6-2 and Figure 6-3), the supply noises can be transferred to the dynamic node. The worst case is shown in Figure 6-5.b.



(a)



(b)

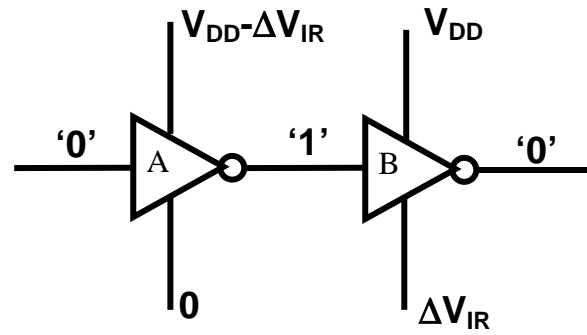
Figure 6-5: Simultaneous switching noise model for the dynamic node of a domino logic circuit: a) Worst case simultaneous switching noise for the dynamic node of a domino logic circuit; b) Equivalent model for transferring simultaneous switching noise to the input of circuit shown in part (a).

6.4 Model for Transferring IR-Drop Noise to the Input

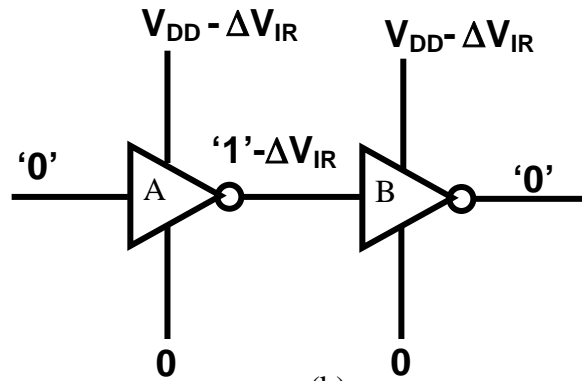
The difference between IR-drop and the simultaneous switching noise is that the simultaneous switching noise can either increase or decrease the supply voltages; however, IR-drop causes the supply voltage to reduce and the ground voltage to increase.

Two cases are considered. In the first case the gates are far apart and therefore, the power and ground of the two circuits can change independently (Figure 6-6). As shown the IR-drop voltages of the gates can change independently and are not correlated. The second case is where the circuits are near each other and therefore the supply voltages are the same (Figure 6-7).

The worst case noise for the uncorrelated supply voltages is shown in Figure 6-6.a. It can be modeled as shown in Figure 6-6.b. So for separate supplies the worst case supply noise can be modeled as a drop of ΔV_{IR} on the supply and a ΔV_{IR} noise on the signal line.



(a)



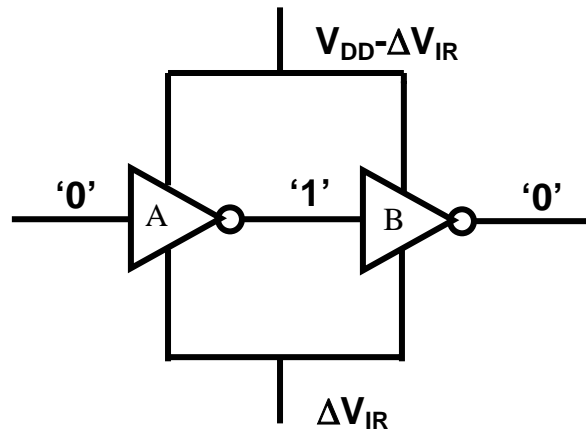
(b)

Figure 6-6: IR-drop transfer model for two gates which are far apart on the chip (These models can be used for any gate, In this figure inverters are shown). In this case the supply voltages can change because of IR-drop independently: (a) Worst case IR-drop for two circuits with uncorrelated powers and grounds; (b) equivalent circuit model for the circuit shown in part (a).

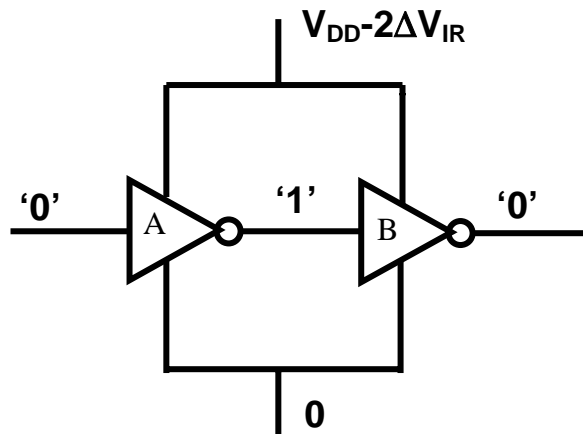
The noise margin for the gate *B* can be calculated by applying the supply voltage and noise in the input of the gate to (6.1)

$$V_{NM} = f(V_{DD} - \Delta V_{IR}, V_{th}, W, L, \dots) - \Delta V_{IR} \quad (6.8)$$

The worst case noise for the correlated supply voltages is shown in Figure 6-7.a. The IR-drop noise can be transferred to the input as shown in Figure 6-7.b. As shown the power supply and ground voltage can change due to IR-drop independently and are not correlated. The IR-drop noise can be transferred to the input as shown in Figure 6-7.b.



(a)



(b)

Figure 6-7: IR-drop transfer model for two gates which are near on the chip (These models can be used for any gate, In this figure inverters are shown). In this case the supply voltages of both gates change the same, because of IR-drop: (a) Worst case IR-drop for two circuits with correlated powers and grounds; (b) equivalent circuit model for the circuit shown in part (a).

The noise margin for the gate *B* can be calculated by applying the supply voltage and noise in the input of the gate to (6.1)

$$V_{NM} = f(V_{DD} - 2\Delta V_{IR}, V_{th}, W, L, \dots) \quad (6.9)$$

6.5 IR-drop Noise Model for Domino Logic Circuits

Applying the techniques introduced in Section 6.4 to a domino logic gate, enables us to model the IR-drop noise for these kinds of circuits. The dynamic node and the output inverter in a domino logic are located near each other and therefore their supply voltages are the same. The domino logic input comes from another gate. Therefore, the worst case input is modeled assuming their supply voltages can change independently. Figure 6-8 shows the worst case IR-drop for the input signal. In this case the keeper is in the linear region and therefore can be replaced with a resistor (Figure 6-8.b). Transferring the IR-drop noise to the input, the worst case noise for the input is shown in (Figure 6-8.b).

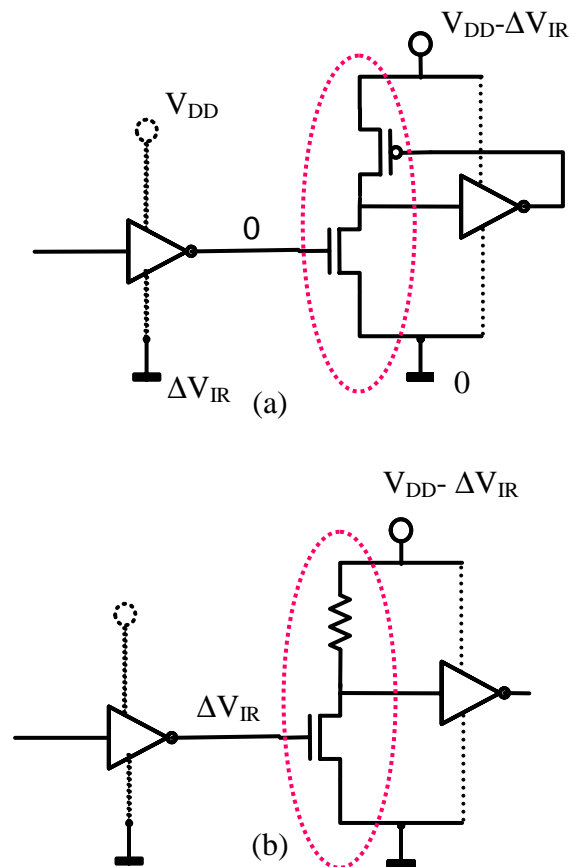


Figure 6-8: IR-drop model for the input of a domino logic circuit: a) Worst case IR-drop for the input of a domino logic circuit; b) Equivalent model for transferring IR-drop to the input of circuit shown in part (a).

The dynamic node is usually near the output inverter, and therefore the worst case IR-drop noise for a domino logic gate is as shown in Figure 6-9. Using the techniques introduced in Section 6.4, the IR-drop noise can be transferred to the dynamic node. The worst case is shown in Figure 6-9.b.

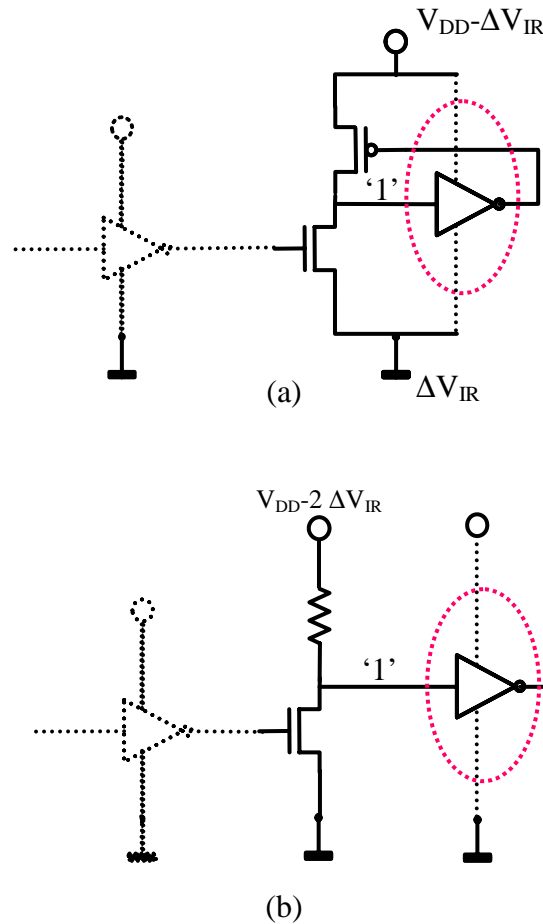


Figure 6-9: IR-drop model for the dynamic node of a domino logic circuit: a) Worst case IR-drop for the dynamic node of a domino logic circuit; b) Equivalent model for transferring IR-drop to the input of circuit shown in part (a).

6.6 Supply Noise Model for Domino Logic Circuits

The supply noise is because of IR-drop and simultaneous switching. In worst case the IR-drop and the simultaneous switching are independent and as a result the worst case supply noise can be modeled as Figure 6-10.

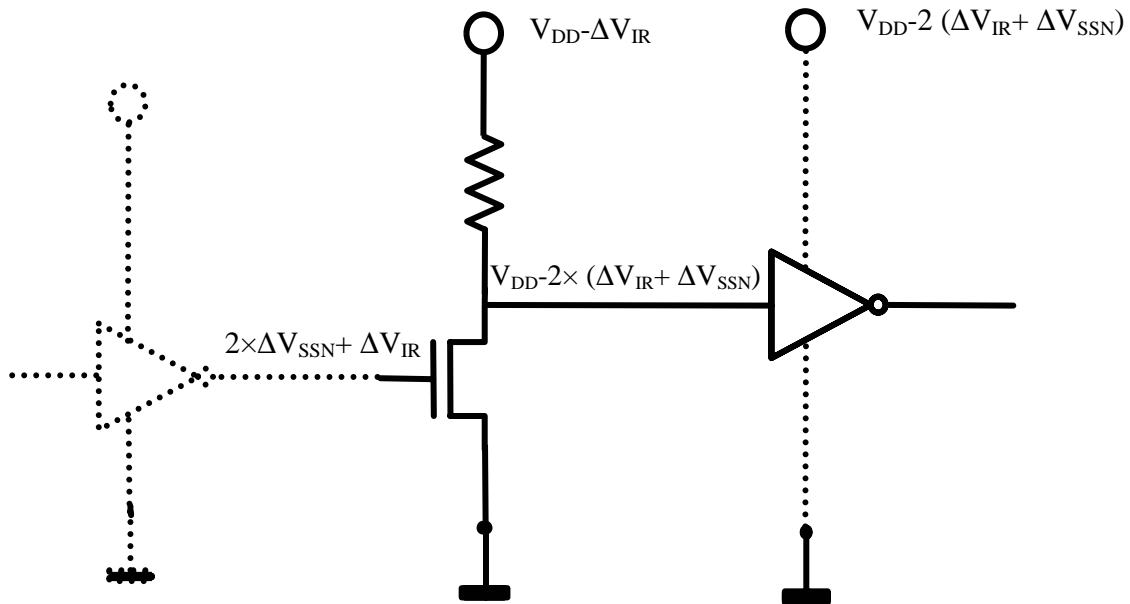


Figure 6-10: Worst case supply noise model for a domino logic circuit.

6.7 Conclusion:

Models are derived to transfer supply noise of digital circuits to their input. The models are derived for two generic types of logic gates which are very common. These models can be used to model the input noise and the supply noise of a digital circuit at the same time. The models are derived for two generic types of logic gates which are very common.

Chapter 7

A Compact Delay Model for Series Connected MOSFETs

7.1 Introduction

Series connected MOSFETs (Figure 7-1) are used in different logic families including dynamic logic families and static CMOS gates. A compact model for series connected MOSFETs when the drain/source capacitance of the MOSFET is small compared to the load capacitance has been derived by Sakurai [62]. Sakurai's model can be used for static logic families, in which the load capacitance is much larger than drain/source capacitances. However, in logic families such as dynamic logic circuits, where the drain/source capacitance is not negligible compared to the load capacitance, there is no compact analytical model for the delay of series connected MOSFETs. Therefore, a model for series connected MOSFETs where the drain/source capacitance is not negligible compared to the load capacitance is described.

The alpha power law model has been used for the transistor model [63]. Although this model is very simple it represents accurately the velocity saturation effect of the transistor. Therefore, it is a useful model for sub-micrometer devices. The disadvantage of this model is that it is empirical and is not able to predict MOSFET behavior for future generations. The physical alpha power law model [64] for MOSFETs provides a physical

interpretation of the device parameters; therefore it enables projections for future generations:

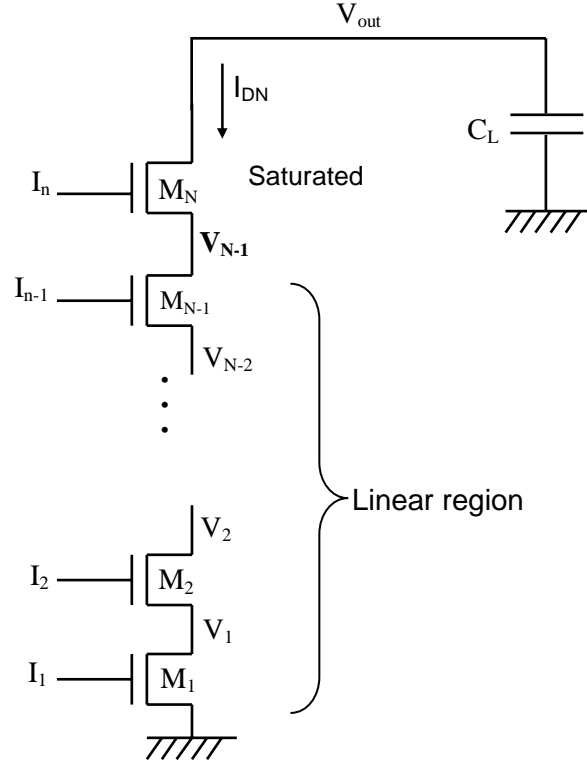


Figure 7-1: Series connected MOSFET transistors discharging a capacitive load. The transistor connected to the load is in saturation and the other transistors are all in linear region.

$$\begin{cases}
 I_D = I_{DSAT} \left(2 - \frac{V_{DS}}{V_{DSAT}} \right) \left(\frac{1 + \lambda \cdot V_{DS}}{1 + \lambda \cdot V_{DD}} \right) \frac{V_{DS}}{V_{DSAT}} & (V_{DS} < V_{DSAT}) \text{ Linear region} \\
 I_D = I_{DSAT} \left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{T0}} \right)^\alpha \left(\frac{1 + \lambda \cdot V_{DS}}{1 + \lambda \cdot V_{DD}} \right) & (V_{DS} \geq V_{DSAT}) \text{ Saturation region}
 \end{cases} \quad (7.1)$$

In this model I_{DSAT} is the drain current when $V_{GS}=V_{DS}=V_{DD}$, V_{DSAT} is the drain saturation voltage when $V_{GS}=V_{DD}$, V_{T0} is the threshold voltage with no body bias, V_{TH} is the

threshold voltage with body bias, V_{T0} is the threshold voltage with no body bias, α is an empirical parameter and λ is the channel length modulation parameter. A linear approximation of the body effect is used for the device threshold voltage (V_{TH})

$$V_{TH} = V_{T0} - \gamma_1 V_{BS} . \quad (7.2)$$

In this equation V_{BS} is the bulk-source voltage and γ_1 is the body-bias factor.

7.2 Negligible Drain/Source Capacitance

Sakurai [62] describes a model for series connected transistors when the drain/source capacitance is small compared to the load capacitance, C_L . In this case, the ratio of the delay of Series Connected MOSFETS (SCMS) to the delay of a single transistor, as a function of the number of transistors n is

$$\begin{aligned} F_D &= \frac{\text{delay}(SCMS)}{\text{delay}(inverter)} = \frac{I_{DSAT}}{I_{DN}} = 1 + \frac{1-1/\sqrt{2}}{1-1/\alpha\sqrt{2}} \frac{V_{DSAT}}{V_{DD} - V_{TH}} (1 + \gamma_1)(N - 1) \\ &\approx 1 + \frac{1}{2} \alpha \frac{V_{DSAT}}{V_{DD} - V_{TH}} (1 + \gamma_1)(N - 1), \end{aligned} \quad (7.3)$$

where F_D is the ratio of the delay of N transistors in series to the delay of a single transistor discharging the same load capacitance, I_{DN} is the equivalent current of the SCMS and N is the number of transistors in series. This model can be used only if the load capacitance, C_L is large compared to the drain/source capacitances of the MOSFETs. In regular static CMOS gates, the load capacitance (C_L) is large compared to the drain/source capacitances so the results are in good agreement with the delay of regular static CMOS gates. However, in dynamic circuits where the load capacitance (C_L) is

comparable to drain/source capacitance the model described by (7.3) doesn't have good agreement with SPICE simulations.

7.3 Elmore Delay Model When Drain/Source Capacitances are not Negligible

In this case, we cannot neglect the drain and source capacitances. In the Elmore delay model transistors are modeled as resistors and capacitors and the delay T can be calculated using the Elmore delay rules [64].

$$T = 0.69 \times \left(R_1 C_1 + (R_1 + R_2) \times C_2 + (R_1 + R_2 + R_3) \times C_3 + \dots + (R_1 + R_2 + \dots + R_{N-1}) \times C_{N-1} + (R_1 + R_2 + \dots + R_N) \times C_L \right), \quad (7.4)$$

where C_L is equal to the total capacitance at V_{out} , R_1, R_2, \dots, R_N are the equivalent resistances of the MOSFETs M_1, M_2, \dots, M_N and C_1, C_2, \dots, C_{N-1} are their drain/source capacitances. If the transistors are of the same size we have

$$\begin{aligned} R_1 = R_2 = \dots = R_N = R \\ C_1 = C_2 = \dots = C_N = C \end{aligned} \quad (7.5)$$

As a result, the delay expression can be simplified to

$$T = 0.69 \times \left(\frac{N^2 - N}{2} RC + N \cdot R \cdot C_L \right). \quad (7.6)$$

Figure 7-2 shows the F_D of a dynamic logic AND gate versus number of inputs. As shown in the figure these models do not have good agreement with SPICE simulations [54]. The RC model overestimates the delay and Sakurai's model underestimates it. Therefore in the next section a new model is introduced for the delay of series connected MOSFETs.

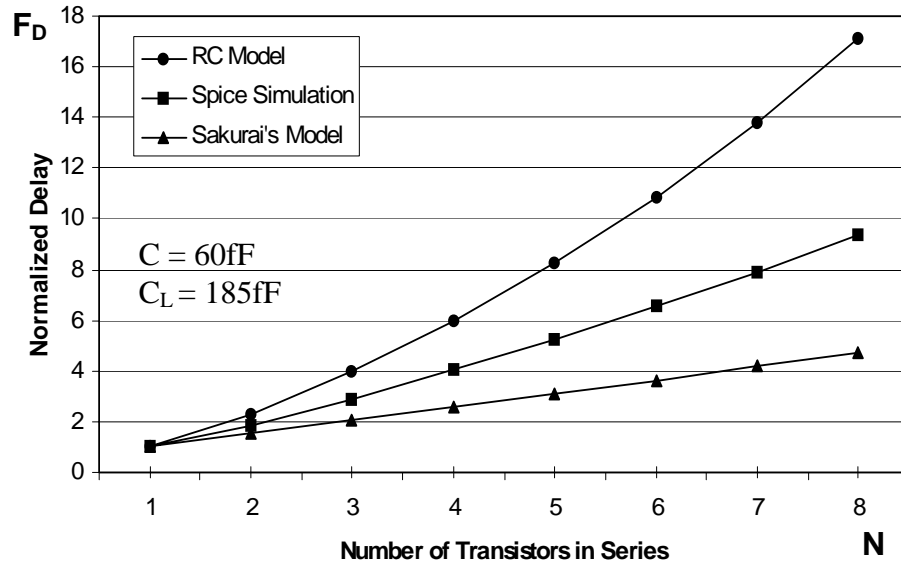


Figure 7-2: Normalized delay versus number of transistors for SPICE simulations and different models.

7.4 Modeling

Depending on which transistor switches, the delay of series connected MOSFETs changes. To find the worst-case delay for series connected MOSFETs different input combinations should be examined (Figure 7-1). Different input situations are:

- i) Transistors M_1 to M_{N-1} are all on and transistor M_N is off. In this case, all of the drain/source capacitances are already discharged. Therefore when M_N is turned on, the switching is fast.

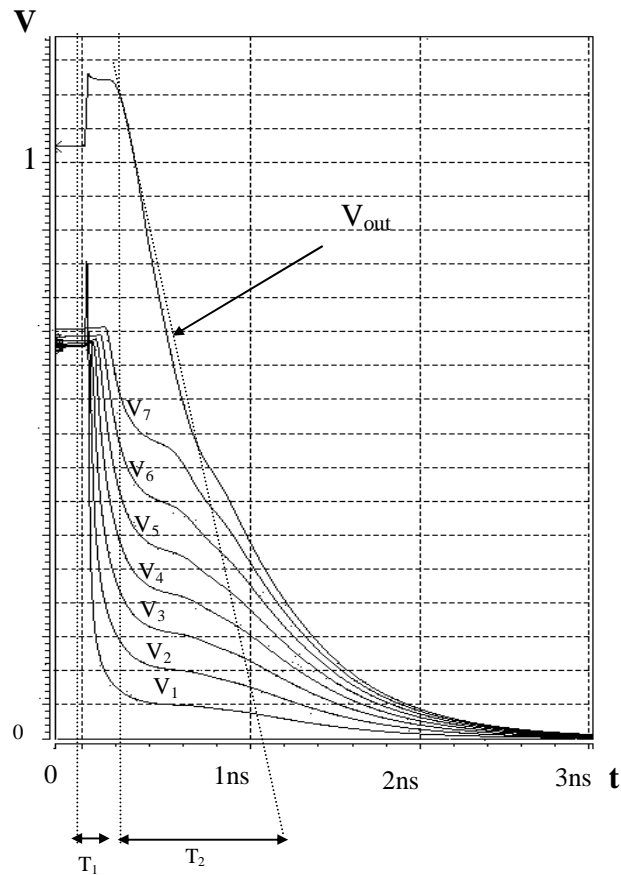


Figure 7-3: The voltage of the nodes of eight transistors in series for the worst-case delay. During time T_1 , the output is constant and transistor M_1 just discharges the drain/source capacitances. During T_2 , the voltages of the drain/source capacitances are constant and transistor M_7 discharges the output voltage (V_{out}).

- ii) Transistors M_1 to M_{k-1} and M_{k+1} to M_N are all on and transistor M_k is off. In this case, the drain/source capacitances of transistors M_1 through M_{k-1} are all already discharged and the drain/source capacitances of transistors M_{k+1} to M_N are all charged to V_{max} , which is the highest voltage to which they can be charged through an NFET transistor. When the transistor M_k is turned on the charged drain/source capacitances of transistors M_{k+1} to M_N are discharged through transistors M_1 to M_{k-1} . Therefore the delay in this case is more than the previous case.

- iii) The worst-case delay is when transistors M_2 to M_N are all on and M_1 is off. In this case the drain/source capacitances are all charged to V_{max} before switching and when switched they are all discharged through transistors M_1 to M_N . This case has the maximum delay and therefore has been modeled.

Figure 7-3 shows the voltage of the nodes of eight transistors in series for the worst-case delay. In this case, the initial voltages of the drain/source nodes are V_{DD} . When the lowest transistor, M_1 is turned on, it starts discharging the drain/source capacitances until T_1 without affecting the V_{out} (Figure 7-3). After T_1 the series transistors start discharging the load capacitance (Figure 7-3). Therefore the output can be modeled as shown in Figure 7-4. It is made of two parts T_1 and T_2 . T_2 has been modeled by Sakurai (7.3) but the first part which is because of the discharge time of the drain/source capacitances has not been modeled. Therefore a model is needed for time T_1 . During T_1 transistors M_1 to M_{N-1} are all non-saturated. Therefore, they can be represented as resistors. Using the alpha power law model the equivalent resistances of these transistors can be modeled as

$$R = \frac{(2 - \sqrt{2}) \cdot (1 + \lambda \cdot V_{DD}) V_{DSAT}}{\left(1 + \lambda \cdot V_{DSAT} \left(1 - \frac{\sqrt{2}}{2}\right)\right) I_{DSAT}}. \quad (7.7)$$

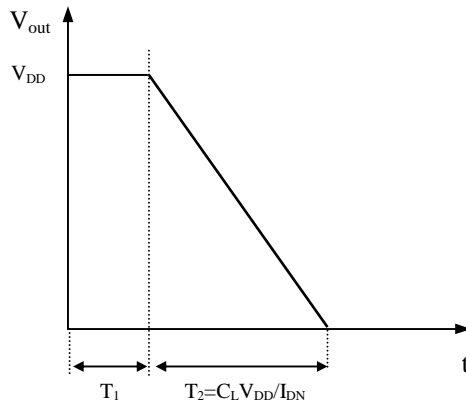


Figure 7-4: Output voltage of series connected transistors.

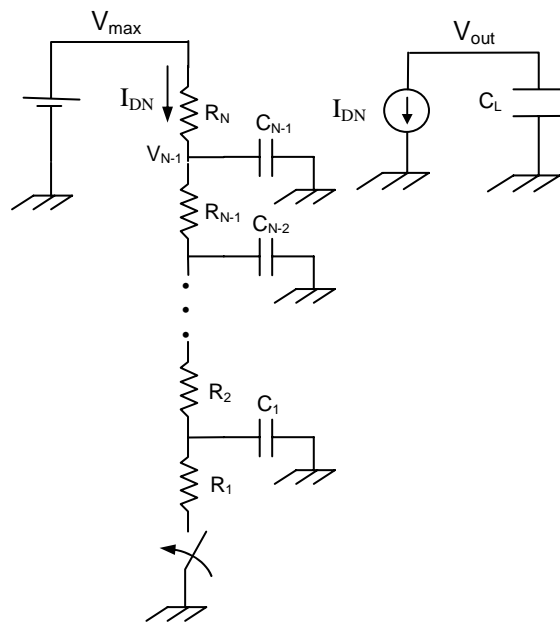


Figure 7-5: Circuit model for series connected transistors. During time T_1 , the output is constant and transistor M_1 just discharges the drain/source capacitances (C_1, C_2, \dots, C_{n-1}). During T_2 , the voltages of the drain/source capacitances are constant and transistor M_1 discharges the output voltage (V_{out}) through current source I_{DN} .

Transistor M_N is saturated for $t < T_1$ and its current is a function of its source voltage (V_{N-1}). It can be modeled as a resistor R_N connected to a power supply equal to V_{max}

$$V_{\max} = \frac{V_{DD} - V_{T0}}{1 + \gamma_1}, \quad (7.8)$$

and

$$R_N = \frac{V_{\max} \cdot (1 + \lambda V_{DD})}{2^{\left(\frac{1}{\alpha} - 1\right)} \cdot I_{DSAT} \cdot \left(1 + \lambda \left(V_{DD} - V_{\max} \left(1 - 2^{-1/\alpha}\right)\right)\right)} . \quad (7.9)$$

As a result, the series transistors during time T_I can be modeled as shown in Figure 7-5.

The current passing through resistor R_N discharges the load capacitance. V_x , which is

$$V_x = V_{\max} - V_{N-1}, \quad (7.10)$$

is shown in Figure 7-6. V_x/R_N is the current discharging the load capacitance. Therefore, the charge removed from the output capacitance at time t is equal to the area under V_x/R_N curve at that time. This waveform can be approximated by a step function with the same area and delay T_1 (Figure 7-6).

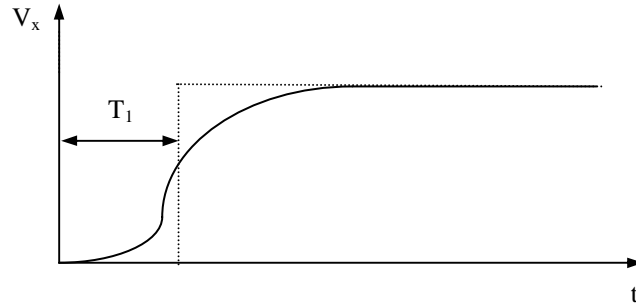


Figure 7-6: Voltage of V_x as a function of time. V_x/R_N is the current discharging the load capacitance.

If V'_x is the impulse response of the circuit then T_I can be approximated by [64]

$$T_1 = \int_0^{\infty} t \times V'_x dt . \quad (7.11)$$

The system is modeled as a linear system therefore the transfer function of the system can be written as

$$H(s) = \frac{1 + a_1s + a_2s^2 + \dots + a_ns^n}{1 + b_1s + b_2s^2 + \dots + b_ms^m}, \quad (7.12)$$

where a_i and b_i are real and $m > n$. By dividing the numerator by the denominator of the transfer function we have

$$H(s) = 1 - (b_1 - a_1)s + (b_1^2 - a_1b_1 + a_2 - b_2)s^2 + \dots \quad (7.13)$$

From the definition of Laplace transform we have

$$\begin{aligned} H(s) &= \int_0^{\infty} V_x' e^{-st} dt = 1 - s \int_0^{\infty} t \times V_x' dt + \frac{s^2}{2!} \int_0^{\infty} t^2 \times V_x' dt - \dots \\ &= 1 - s \times T_1 + s^2 \times T_2 \dots \end{aligned} \quad (7.14)$$

Therefore from equations (7.13) and (7.14), T_1 can be calculated as

$$T_1 = b_1 - a_1. \quad (7.15)$$

For series connected MOSFETs and the worst-case initial condition a_1 is zero and b_1 is equal to [64]

$$b_1 = \left(\frac{R_1 \times (R_2 + \dots + R_N)}{(R_1 + R_2 + \dots + R_N)} C_1 + \frac{(R_1 + R_2) \times (R_3 + \dots + R_N)}{(R_1 + R_2 + \dots + R_N)} C_2 + \dots \right. \\ \left. \frac{(R_1 + R_2 + \dots + R_{N-1}) \times R_N}{(R_1 + R_2 + \dots + R_N)} C_{N-1} \right). \quad (7.16)$$

Therefore, T_1 is given by

$$T_1 = b_1 - a_1 = \left(\frac{R_1 \times (R_2 + \dots + R_N)}{(R_1 + R_2 + \dots + R_N)} C_1 + \frac{(R_1 + R_2) \times (R_3 + \dots + R_N)}{(R_1 + R_2 + \dots + R_N)} C_2 + \dots \right. \\ \left. \frac{(R_1 + R_2 + \dots + R_{N-1}) \times R_N}{(R_1 + R_2 + \dots + R_N)} C_{N-1} \right). \quad (7.17)$$

When the transistors are of equal size, they can be modeled as equal resistors and capacitors indicated by

$$\begin{aligned} R_1 = R_2 = \dots = R_N = R \\ C_1 = C_2 = \dots = C_N = C \end{aligned} \quad (7.18)$$

Simplifying (17) results in

$$T_1 = \frac{RC \cdot N \cdot (N-1)}{R_N + (N-1)R} \left[\frac{R_N}{2} + R \cdot \left(\frac{N}{6} - \frac{1}{3} \right) \right], \quad (7.19)$$

where R and R_N can be calculated by (7) and (9) respectively.

During time T_2 , the current discharging C_L can be calculated from (3), therefore

$$T_2 = \frac{C_L \cdot V_{DD}}{I_{DN}} = \frac{C_L \cdot V_{DD} \cdot F_D}{I_{DSAT}}. \quad (7.20)$$

As a result the output voltage is

$$V_{out} = V_{DD} - \frac{I_{DSAT}}{C_L \cdot F_D} (t - T_1) \times u(t - T_1) \quad t < T_1 + T_2, \quad (7.21)$$

where $u(t - T_1)$ is the step function delayed by T_1 .

7.5 Validation of the Results

Figure 7-7 shows the normalized delay of dynamic AND gates implemented with $0.5\mu\text{m}$ transistors versus number of inputs. The results show good agreement between the new model and the SPICE simulations.

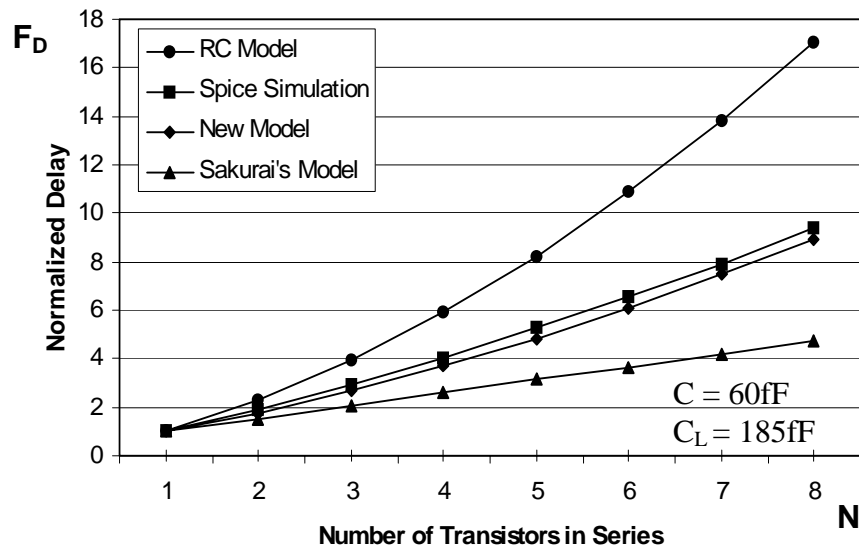


Figure 7-7: Normalized delay of dynamic AND gates versus number of inputs for different models.

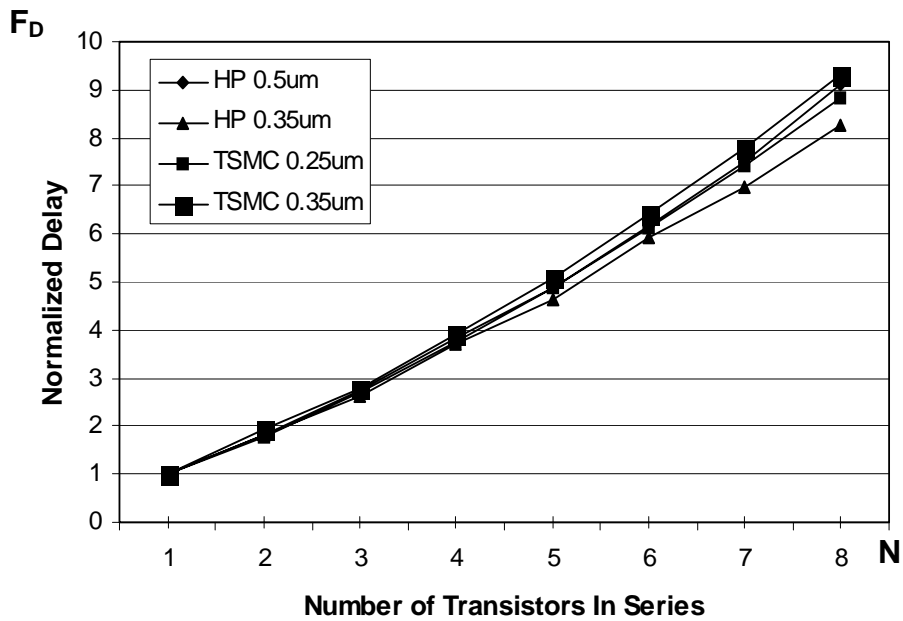


Figure 7-8: Normalized delay versus number of transistors for different generations of technology.

7.6 Results

Figure 7-8 shows normalized delay as a function of the number of transistors in series for different sub-micrometer generations. The model shows that the delay for series connected MOSFETs does not change for these sub-micrometer generations, because α is almost constant. In other words these sub-micrometer devices are equally velocity saturated due to scaling both device dimensions and supply voltage.

7.7 Conclusion

A new model has been derived for the delay of series connected MOSFETs that can be used to calculate the delay of series connected MOSFETs used in any logic family. It also enables us to predict delay of different logic families for future generations and see how different parameters of the device affect the delay. Key results show that the relative delay of series connected MOSFETs is almost invariant for different generations of technology.

Chapter 8

Three Phase Domino Logic Circuits

8.1 Introduction

The scaling trend of MOSFETs requires the supply voltage and the threshold voltage to be reduced. Scaling is required to reduce power and increase the speed. However, as devices are scaled noise is becoming a more important issue. Noise is increasing because of higher switching speeds, capacitive/inductive noise coupling and fluctuation of device parameters.

Domino logic families are extensively used in high speed processors. They are faster than static logic families and consume less space on the silicon. However, scaling requires lower threshold voltage which results in lower noise margin for domino logic families. Therefore domino logic circuits which have smaller noise margin compared to static logic circuits are more susceptible to noise for future generations. Different techniques have been introduced [21], [22], [23], to increase their noise margin. In all of the introduced techniques increasing the noise margin will reduce the gate speed. Circuits introduced in [23], [24] increase the noise margin without affecting speed but both of them have very hard timing requirements which makes them almost impractical to implement. A novel technique is introduced to increase the noise margin of delayed domino logic circuits with a small impact on the speed. Using this circuit the charge

sharing noise is limited and the crosstalk noise which is also one of the most important sources of noise in digital circuits can be controlled.

8.2 Noise Margin

Noise Margin (NM) of a circuit is defined as the maximum noise voltage that can be tolerated by the circuit. Two kinds of noise can be defined [65] to find the noise margin:

- Static noise: is a DC noise voltage. It is defined only by its voltage level.
- Dynamic noise: is a noise which has a limited duration. It is defined by amplitude, shape and duration.

The static noise is used to model worst case noise of circuits which are susceptible to the input at any time and the dynamic noise is used to model worst case noise for a circuit which is susceptible to input noise for a limited amount of time. Therefore, two kinds of noise margin are defined:

- Static noise margin: The amount of static noise voltage, which can be tolerated. Static noise margin is only a function of the noise voltage level.
- Dynamic noise margin: The amount of dynamic noise voltage, which can be tolerated. It is a function of amplitude, shape and duration.

In logic circuits the inputs affect the circuit at any time and the noise may have any duration. In worst-case it is assumed that a DC noise is on the input of the circuit, and therefore, the static noise margin is used to calculate the worst-case noise margin [66].

Limiting the duration in which the logic is sensitive to the inputs, or in other words limiting the evaluation time, will result in a higher noise margin, because the noise has

limited time to affect the output. To be able to limit the evaluation time two questions should be answered:

- 1- When are all of the inputs to a logic gate ready?
- 2- How much is the delay of the logic gate?

If these two questions are answered in a logic family the evaluation time can be limited. If the evaluation time is limited in a logic family then the duration in which the circuit is affected by the inputs is limited and as a result the noise duration is limited. The noise has limited time to affect the circuit and therefore the dynamic noise margin should be used to calculate the noise margin of this logic gate. The dynamic noise for this gate is shown in Figure 8-1, which is a pulse with duration equal to the evaluation phase.

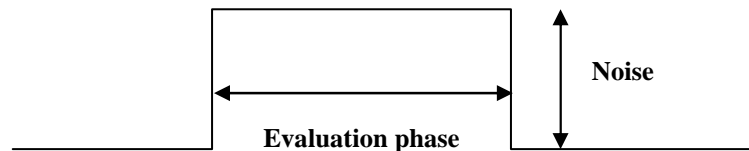


Figure 8-1: Noise shape for a logic gate with limited evaluation time.

The proposed logic family should have three phases (Figure 8-2). The first phase is the precharge phase. In this phase the input should not affect the output and the circuit gets ready for the evaluate phase to start. The evaluation phase begins when all of the inputs to that stage are ready. In this phase the output changes depending on the input and the logic performed in the circuit. This phase is the only phase during which the circuit is affected by the inputs. Therefore noise may affect the output of the circuit only in this phase. After the evaluation phase the save phase begins. In this phase the evaluated value is saved for the next stages of the circuit. The circuit should be designed so that it is not

affected by the inputs in the save phase. In the next section a new circuit is introduced to implement the three required phases.

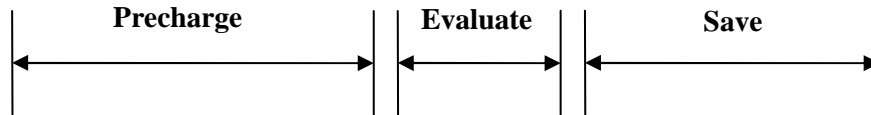


Figure 8-2: Three phases required for a gate with limited evaluation time.

8.3 Implementing the Three Phase Domino (TP-Domino) Logic

There is a family of domino logic circuits named Clock-Delayed Domino (CD-Domino) logic [67] in which, a clock signal is propagated in parallel to the logic network. Therefore the clock of each stage is the delayed form of the clock of the previous stage. In this logic family the evaluation starts by the rising edge of the clock for that stage. The clock delay of each gate is designed so that it arrives when all of the inputs to that gate are ready. By a small change in CD-Domino we are able to implement the three phases proposed in the previous section.

Figure 8-3 shows the Three Phase Domino circuit. In this circuit CLKD is the delayed form of the CLK signal (Figure 8-4), the save PFET transistor is larger than the normal keeper transistors used in conventional domino gates and the NOT (Figure 6-1.b) is changed by a NAND gate.

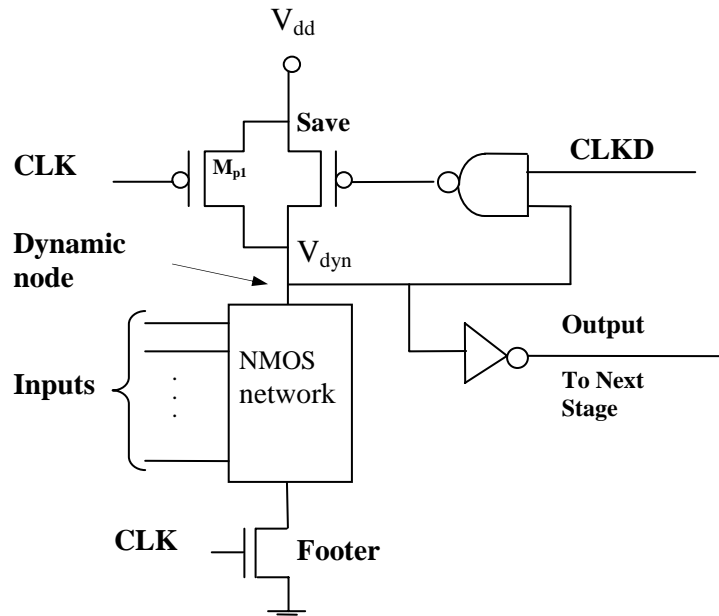


Figure 8-3: Three Phase Domino circuit.

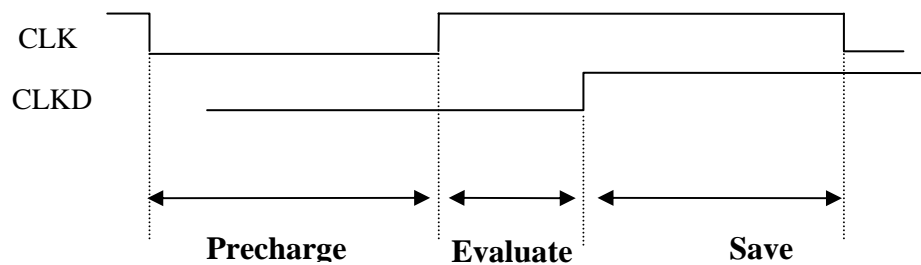


Figure 8-4: Clock signals required for the Three Phase Domino logic circuit.

In precharge phase the footer transistor is off and M_{p1} is on therefore the dynamic node V_{dyn} is charged to V_{dd} which is the same as the precharge phase in CD-Domino. The footer transistor is off therefore the inputs have no affect on the dynamic node in this phase. In the evaluation phase the CLK signal changes to one turning off M_{p1} and turning on the footer transistor. Therefore the evaluation is done depending on the inputs and the logic of the NMOS network. The pull-down transistors can discharge the dynamic node very fast because both of the PFETs are off in this phase. The next phase is the save

phase which starts when CLKD changes to V_{dd} . When CLKD changes to V_{dd} , the NAND acts as a NOT gate. Therefore if the dynamic node is discharged, the output of the NAND stays one and as a result the save transistor remains off. On the other hand if the dynamic node is not discharged the NAND output changes to zero which turns on the save transistor. Thus the dynamic node is connected to V_{dd} through the PFET save transistor. If the dynamic node is discharged the inputs can not affect the dynamic node voltage because it is not able to charge it again and if it is not discharged the save transistor is strong enough to keep the dynamic node voltage to be larger than the threshold voltage of the NAND gate. Therefore in either case the output of the gate does not change when the inputs change in the save phase.

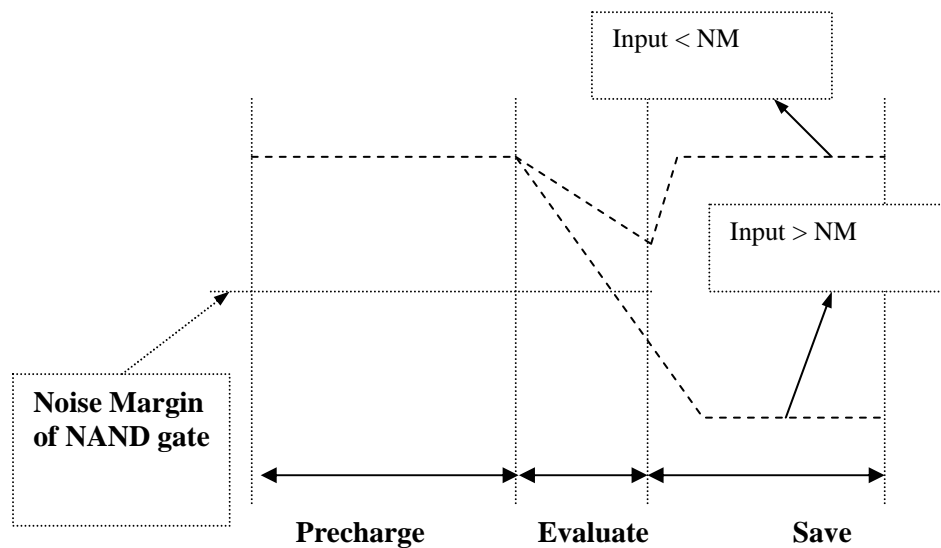


Figure 8-5: Outputs for two different inputs:, 1) Input < NM, in this case the output return to one 2) Input > NM, in this case the input results in a wrong output state.

The width of the noise pulse is determined by the evaluation time. The noise pulse causes the dynamic node to drop as shown in Figure 8-5. This figure shows two cases.

The first case is when the input is less than the low NM. In this case the output drops but the voltage drop is less than the high noise margin of the NAND gate. Therefore in the save phase, the save transistor restores the dynamic node to V_{dd} . In the second case the input is larger than the low NM. Therefore the voltage drop of the dynamic node is more than the high NM of the NAND gate and as a result it is not restored.

The save transistor is off in the evaluate phase. Therefore in the evaluate phase it acts as a parasitic capacitance. On the other hand there is no keeper transistor which is used in normal clock delayed dynamic logic circuits. Therefore the delay compared to the delay of CD-domino may be either higher because of the added parasitic capacitors of the save transistor or lower because of omitting the keeper transistor. SPICE simulations for a 3-input AND gate show that the delay is increased by only 3% compared to CD-Domino logic circuits.

8.4 Results

Figure 8-6 and Figure 8-7 shows the SPICE simulations of a 3-input AND gate for different inputs. In Figure 8-6 an input equal to V_{dd} is applied therefore in the evaluation phase the dynamic node drops to zero and the output of the circuit changes from zero to V_{dd} . The output of the NAND gate remains at V_{dd} , as a result the save transistor stays off. Figure 8-7 shows the signals of the same gate when zero is applied to the input. In this case the dynamic node remains at V_{dd} and the output remains at zero. The output of the NAND gate changes from V_{dd} to zero which turns on the save transistor and as a result the dynamic node is connected to V_{dd} by the save transistor.

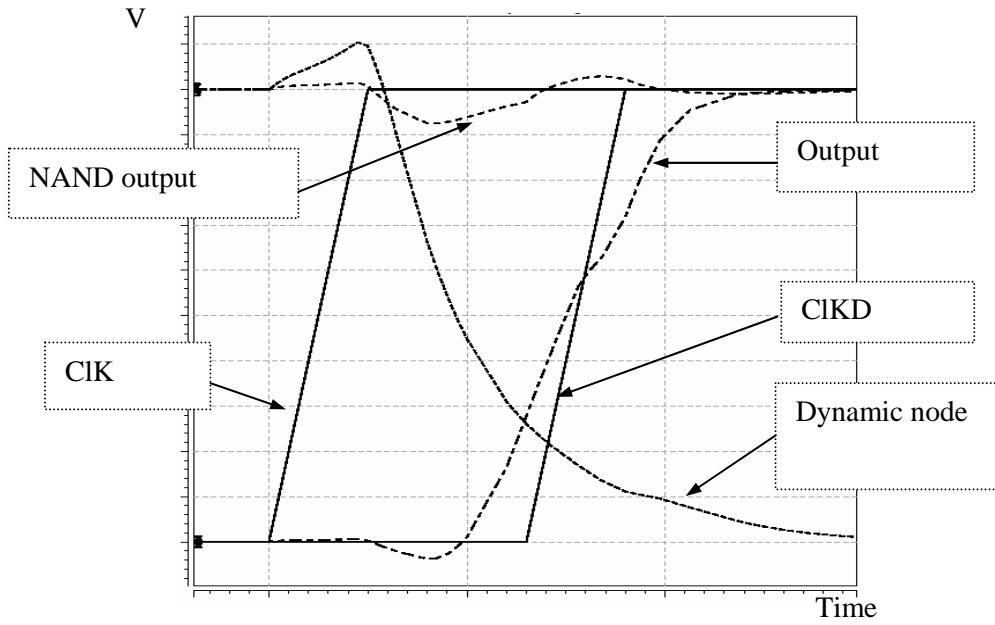


Figure 8-6: Outputs voltage of the three phase domino logic circuit when the input is one.

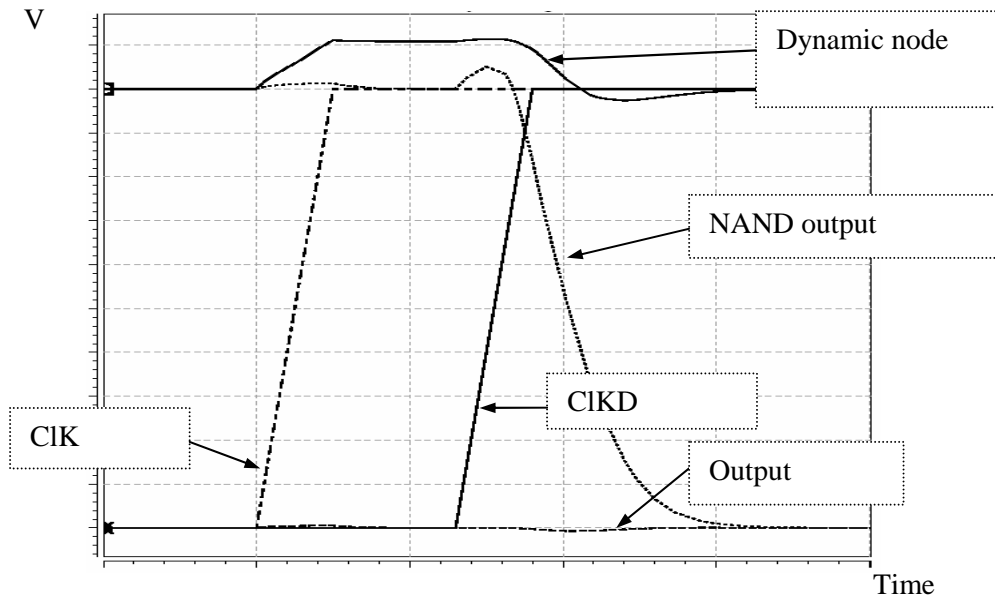


Figure 8-7: Outputs voltage of the three phase domino logic circuit when the input is zero.

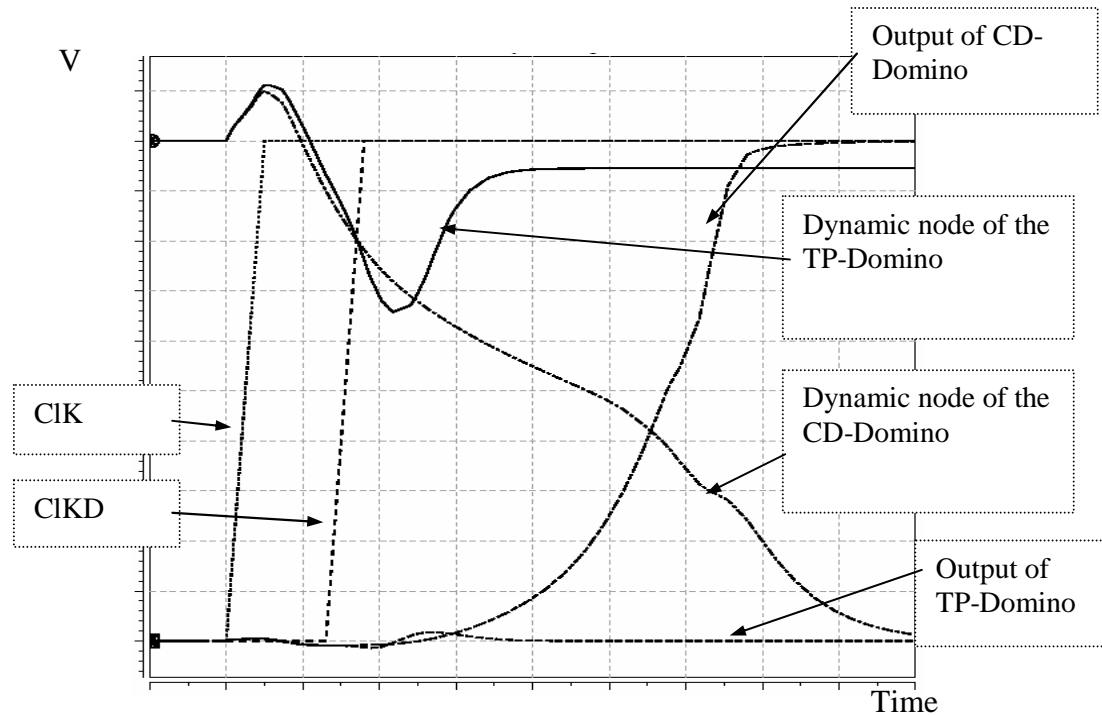


Figure 8-8: Outputs of the Three-Phase Domino and clock delayed domino for an input noise.

Figure 8-8 shows the output of a CD-Domino 3-input AND gate and the output of the TP-Domino 3-input AND gate when noise is applied in the input. As shown the dynamic node of the CD-Domino logic drops to zero but the output of the TP-Domino circuit is charged to V_{dd} when the save phase is turned on. In this case the output of the CD-Domino logic switches but the output of the TP-Domino logic remains at zero.

The noise margin of the circuit is determined by the evaluation time and the noise margin of the NAND gate. Reducing the evaluation time increases the low noise margin and reduces the high noise margin and vice versa. Figure 8-9 shows SPICE simulations of how the normalized low and high noise margin are changed for a 3-input 180nm AND gate as a function of the normalized evaluation phase duration. Normalized evaluation phase is defined as the ratio of the evaluation phase duration to the delay of the gate. As

shown reducing the evaluation phase duration increases the low noise margin and reduces the high noise margin. When the high noise margin is equal to the low noise margin the circuit has the highest immunity to noise. As shown in Figure 8-9 the noise margin of the circuit in the best case is increased by 62%. If the evaluation duration is very long the noise margin reaches the noise margin of normal CD-Domino logic circuits.

The save transistor should be large enough so that the circuit is not sensitive to noise in the save phase. On the other hand it should be as small as possible to reduce the amount of parasitic capacitance that it adds to the dynamic node.

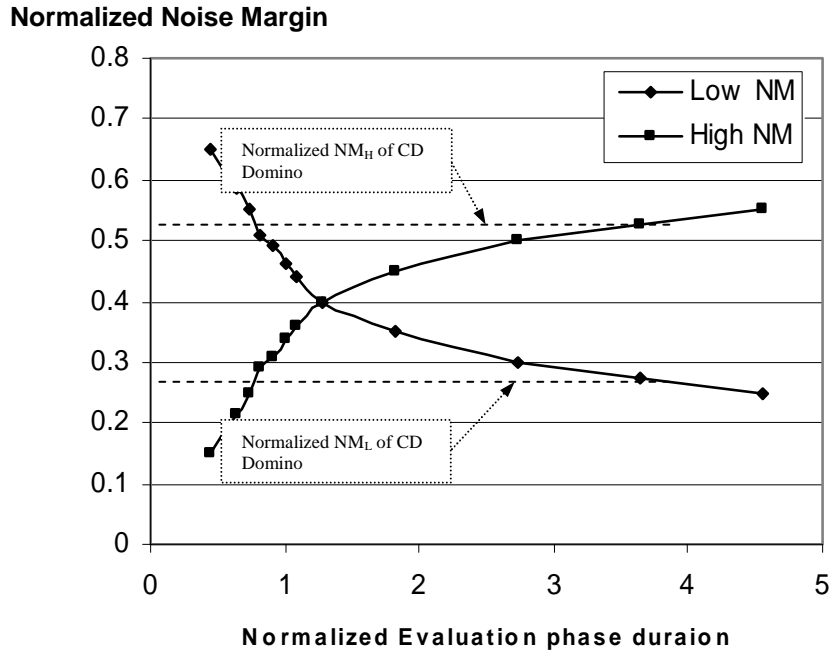


Figure 8-9: Normalized Noise Margin as a function of the normalized evaluation phase duration for a three phase domino logic gate.

8.5 Leakage Current

Domino logic circuits are sensitive to leakage current. The leakage current of the NFET transistors discharges the charge on the dynamic node in the evaluation phase. A small keeper is used to prevent the dynamic node voltage from dropping. As transistors are scaled the leakage current is increased, therefore a small keeper might not be enough to keep the charge on the dynamic node.

In the TP-Domino the time in which the dynamic node may be discharged by the leakage current of the NFET transistors is limited. In the precharge phase the dynamic node is connected to V_{dd} through M_{p1} which is a large PFET transistor. Therefore the leakage current has no effect on the dynamic node charge in this phase. In the save phase if the dynamic node voltage is one it is connected to V_{dd} through the save transistor which also is a large transistor. Therefore the leakage current has no affect in the precharge and the save phase. It can only affect the dynamic node in the evaluation phase. The duration of the evaluate phase is comparable to the delay of the gate. On the other hand, the leakage current of a transistor is very small compared to the on-current. Therefore the voltage drop caused by the leakage current during the evaluation phase is negligible. As a result no keeper transistor is needed in this kind of domino logic circuits.

8.6 Charge Sharing Noise

Charge sharing noise happens because of sharing charge between the dynamic node and the parasitic capacitors within the gate. It reduces the charge on the dynamic node and as a result it reduces the dynamic node voltage.

In Three Phase Domino logic circuits the inputs of each stage change when the circuit is in the precharge phase. At the precharge phase the dynamic node is connected to V_{dd} through M_{p1} which is a large PFET transistor. Therefore the charge sharing noise is much smaller in TP-domino compared to other domino logic families

8.7 Crosstalk Noise

Crosstalk noise occurs on a wire when the neighboring wire switches. The switching wire is called the aggressor and the other one is called the victim wire. The wires used to connect dynamic logic gates are local wires, and therefore there is only capacitive coupling between neighboring wires and the inductive coupling is negligible [69]. Therefore this kind of noise occurs when the aggressor wire switches and therefore, it is not a random noise.

In these kinds of circuits the output switches in the evaluation phase and it is only sensitive to the input in this phase. Therefore for each wire the phase at which it is switching and the phase when the following gate is sensitive to the input is known. This can be shown with an example (Figure 8-10). In Figure 8-10.a it is assumed that there are four phases. Each gate does the evaluation in one of those phases. The phase when the gate does the evaluation is shown on the gate (Figure 8-10.b). Each wire is labeled as (x,y) , where x is the phase when the wire is switching and y is the phase when the following gate is sensitive to the input. Figure 8-10.c shows an example of two wires which are beside each other and crosstalk between them does not affect the circuit. The top wire switches in phase 2 and the bottom wire is sensitive to the input in phase 3 ($2 \neq 3$), therefore crosstalk noise due to the top wire switching will not affect the bottom

wire. The bottom wire switches in phase 1 and the top wire is sensitive to the input in phase 4 ($1 \neq 4$), therefore crosstalk noise due to the bottom wire switching will not affect the top wire. Figure 8-10.d shows an example of two wires which are beside each other and crosstalk between them is important. The top wire switches in phase 3 and the bottom wire is sensitive to the input in the same phase 3. Therefore, a voltage change on the top wire will affect the bottom wire. Figure 8-10.e shows the same circuit shown in Figure 8-10.d, however the crosstalk is reduced by increasing the distance between the aggressor and victim wire. It can even be eliminated by placing a ground wire between them. Even if the layout is done automatically, it can be easily implemented in the CAD tool. By using this technique the crosstalk noise which is the largest noise source can be easily eliminated or reduced for these phase domino logic circuits.

8.8 Conclusion

Domino logic circuits are extensively used in the critical path of high performance processors. Speed and area advantage of this family of logic circuits compared to static logic circuits makes them a favorite choice; however, they suffer from their low noise margin. A novel domino circuit is introduced to easily increase the noise margin of these kinds of circuits without affecting their speed. Simulations for a 3-input 180nm AND gate show that the noise margin can be increased by 62% with only 3% reduction in the speed. The Three-Phase circuit does not suffer from leakage current. It is not sensitive to charge sharing noise which is an important source of noise in dynamic logic circuits. The crosstalk noise which is the biggest source of noise can also be eliminated by applying some simple rules when laying out the wires.

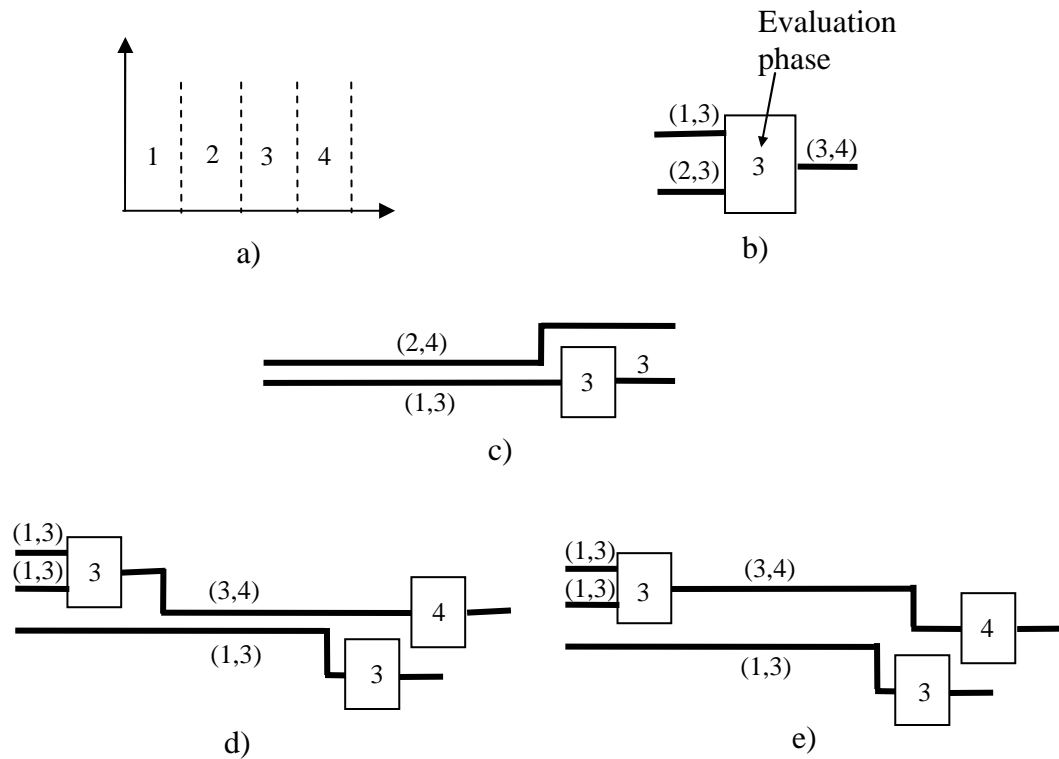


Figure 8-10: Crosstalk noise in three phase logic circuits. a) In this example there are four phases. b) A gate is shown which evaluates in phase 3. Each wire is labeled with (x,y) , where x is the phase where the wire is switching and y is the phase where the following gate is sensitive to the input. c) An example of two wires beside each other, where there is no cross talk problem. d) An example of two wires beside each other, where there is cross talk. e) Crosstalk is reduced by increasing the distance between the wires in part (d).

Chapter 9

Coaxial Polymer Pillars: Ultra-Low Inductance Compliant Wafer-Level Electrical Input/Output Interconnects for Power Distribution

9.1 Introduction

The main concern in distributing power to the chip is the voltage drop. The voltage drop is composed of two parts: the IR-drop and the simultaneous switching noise (SSN). Figure 9-1 shows the voltage drop model of the die to board [69]. The IR-drop is due to the voltage drop on the resistances of the power distribution network. The resistances of the I/O's (R_{IO}) are negligible and therefore the resistance of power distribution is mainly due to the on-chip resistance of the power distribution (R_{PG}). The SSN is caused by the current change that passes through the parasitic inductance of the power distribution network. The parasitic inductances of the I/O's (L_{IO}) are large compared to the parasitic inductances of the on-chip power distribution network (L_{PG}) [69]. Therefore, the parasitic inductance of the power distribution network is mainly due to the I/O parasitic inductances. SSN can be reduced by either reducing the I/O's inductances or by increasing the on-chip decoupling capacitances (C_{DeI}).

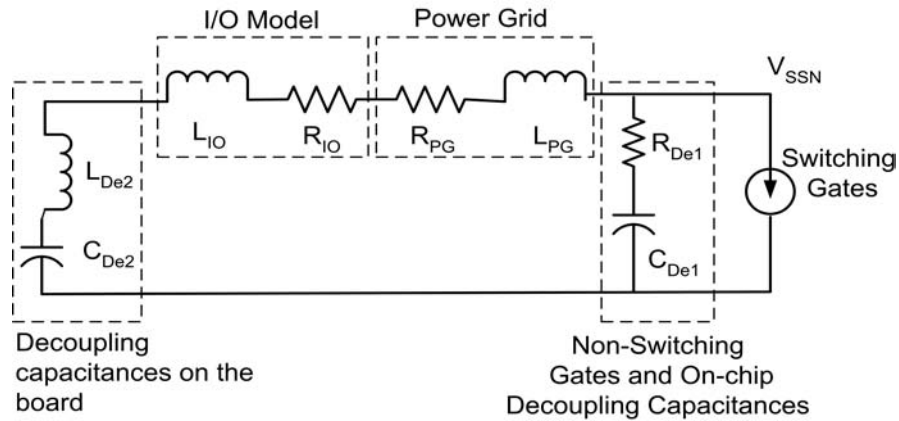


Figure 9-1: A simplified power distribution model for chip to substrate.

Sea of polymer pillars (SoPP) has recently been invented [28], [29]. It provides mechanically flexible optical/electrical I/O's that mitigate thermo-mechanical expansion mismatches. A new structure for the electrical polymer pillars is introduced that exhibits very small parasitic inductance and is suitable to distribute power to the die. The reduced parasitic inductance reduces the required number of pillars needed for power distribution in a chip where the number of I/O's are limited by simultaneous switching noise. Using these new pillars also reduces the size of the required on-chip decoupling capacitor.

In Section 9.2, it is shown how parasitic inductance is measured and how to reduce it. Then a new structure is introduced for the pillars to reduce their parasitic inductance significantly. Finally, the process used to fabricate the new pillar is described in Section 9.3.

9.2 Parasitic Inductance

Parasitic inductance of a segment depends on the area between the segment and its return path (Figure 9-2) [68]. Reducing the distance to the return path reduces the area

and as a result reduces its inductance. Therefore, in order to reduce the inductance, the distance between a segment and its return path should be reduced as much as possible. In a flip-chip package [69], reliability problems limit the minimum distance between power and ground I/O's. Therefore, a new structure is needed to reduce the distance between power and ground I/O's.

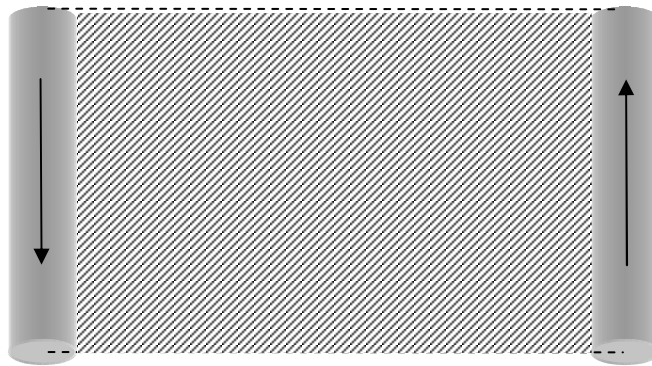


Figure 9-2: Parasitic inductance is proportional to the area surrounded by the segment and its return path.

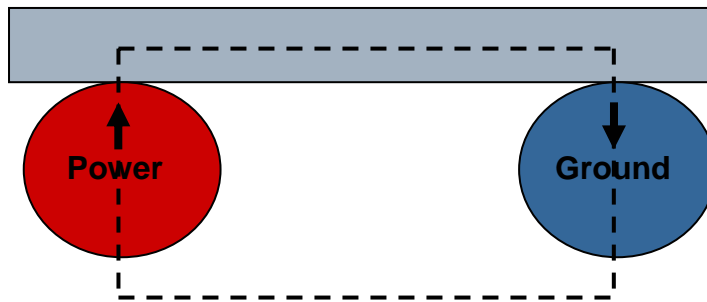


Figure 9-3: In a flip-chip package the parasitic inductance is proportional to the area surrounded by the power and ground bumps.

One of the best structures to reduce the distance between the segment and its return path is the coaxial structure (Figure 9-4). To use a coaxial structure for power distribution, the power is connected to the center wire and the ground is connected to the

conducting shell surrounding it (Figure 9-4). Therefore, the return path of the power is through ground surrounding it which results in a small parasitic inductance.

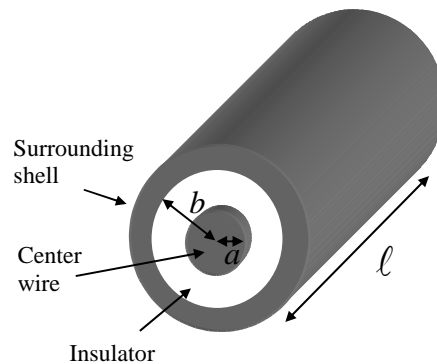


Figure 9-4: Low frequency currents in a coaxial structure. Current at low frequencies is distributed through the metal.

The current is distributed through the cross section of the center and the surrounding wires at low frequencies (Figure 9-4). At high frequency due to proximity effect the current passes through the outer surface of the center wire and the inner surface of the surrounding wire (Figure 9-5) resulting in a smaller inductance loop and smaller inductance (Figure 9-6) [68]. To reduce the inductance at low frequencies the thickness of the center and surrounding metal should be reduced (Figure 9-6). This will result in a smaller inductance loop at low frequencies and as a result smaller low frequency inductance.

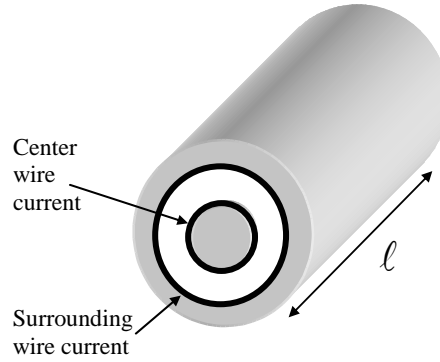


Figure 9-5: High frequency current in a coaxial structure. Current at high frequencies flows through the outer region of the center wire and inner region of the surrounding conducting shell.

The parasitic inductance of a coaxial structure with thin metals used for the center and the surrounding cylinder can be calculated from [68]

$$L = \frac{\mu\ell}{2\pi} \ln\left(\frac{b}{a}\right) \quad (9.1)$$

where μ is the permeability of the insulator, ℓ is the length of the coaxial structure, a is the inner metal radius and, b is the outer metal radius (Figure 9-4). Reducing the insulation thickness between the two metal layers reduces the parasitic inductance.

Inductance

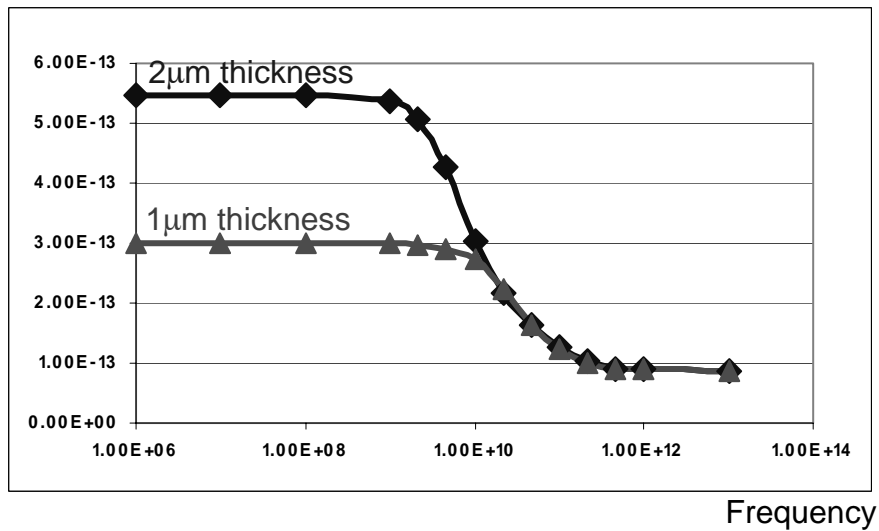


Figure 9-6: Simulation results for the inductance of a coaxial polymer pillar for two different metal thicknesses. The coaxial polymer pillars are : 50μm wide ,100μm tall and dielectric thickness is 0.1μm.

The other advantage of using a coaxial structure for power distribution is the capacitance between the two conductors. Reducing the thickness of the dielectric between two conductors not only reduces the parasitic inductance, but also increases the parasitic capacitance between those conductors. The parasitic capacitance acts as a decoupling capacitance reducing the SSN even further. The capacitance of a coaxial structure can be calculated from [68]

$$C = \frac{2\pi\epsilon_r\epsilon_0\ell}{\ln\left(\frac{b}{a}\right)} \quad (9.2)$$

where ϵ is the dielectric constant of the dielectric between the layers.

The coaxial structure can be easily implemented by the polymer pillars (Figure 9-7). The inductance of a coaxial polymer pillar (CoPP) 50μm wide and 100μm tall with a dielectric of 0.1μm is 0.08pH which is almost two decades smaller than the inductance of

a solder bump or a regular polymer pillar. The capacitance of the introduced CoPP is 5.4 pF. Assuming 3000 pins/cm², the total capacitance added due to these pins is

$$C_{Tot} = 3000 * 5.4 * 10^{-12} = 16.2 \text{ nF} / \text{cm}^2. \quad (9.3)$$

The capacitance per unit area due to the gates not switching for the year 2004 [1] is $C_{decoupling} = 64 \text{ nF/cm}^2$. Therefore, the on-chip decoupling capacitance is increased by almost 25% by adding these CoPP's.

Reducing the parasitic inductance of the I/O's and adding capacitance reduces the need to fabricate large decoupling capacitances on the chip. On-chip capacitances are expensive and consume chip area; therefore, using this coaxial structure reduces the chip cost.

There are many different ways to implement these coaxial pillars. In the following section, one fabrication method is described and demonstrated.

9.3 Fabrication Process

CoPP's have been fabricated using the process shown in Figure 9-7. Polymer pillars (Figure 9-8) are fabricated using the photodefinable polymer Avatrel 2000P as previously described [28], [29]. Following pillar fabrication (Figure 9-7.a.), a metal film (~0.2 μm) is deposited over the polymer pillars (Figure 9-7.b) (Figure 9-9). Next, a dielectric film is deposited and patterned such that a via is formed at the tip region of the pillar, as shown in Figure 9-7.c. A 0.1 μm thick SiO₂ film was used as the dielectric, although, low modulus polymers may be used as well. A wet etch was performed to fabricate the vias. Finally, the second metallic film is deposited and patterned such that it only covers the sidewalls of the pillars (Figure 9-7.d) (Figure 9-9). Both Cu and Au have been used to

encapsulate the pillars. The SiO₂ film not only provides the electrical isolation between the two metallic films, but it also serves as a solder mask. This is important during assembly. To interconnect these CoPP's to the board, solder would be fabricated in the center and perimeter of each polymer socket to make contact to the respective metal film on the pillars.

Providing the mechanical interconnection between the chip and the board becomes more challenging as low-k dielectrics are integrated in high performance chips. The coefficient of thermal expansion (CTE) mismatch between the Si chip and the board can cause damage in the low-k interlayer dielectric. Problems caused by CTE mismatch may be overcome with the use of mechanically compliant I/O interconnections. The intrinsic pillars are designed to be mechanically compliant. The thicknesses of the metal films and insulating layers are selected to minimize the degradation in the lateral compliance of the pillars. High aspect ratio pillars have demonstrated compliance larger than 10 μ m/mN [28].

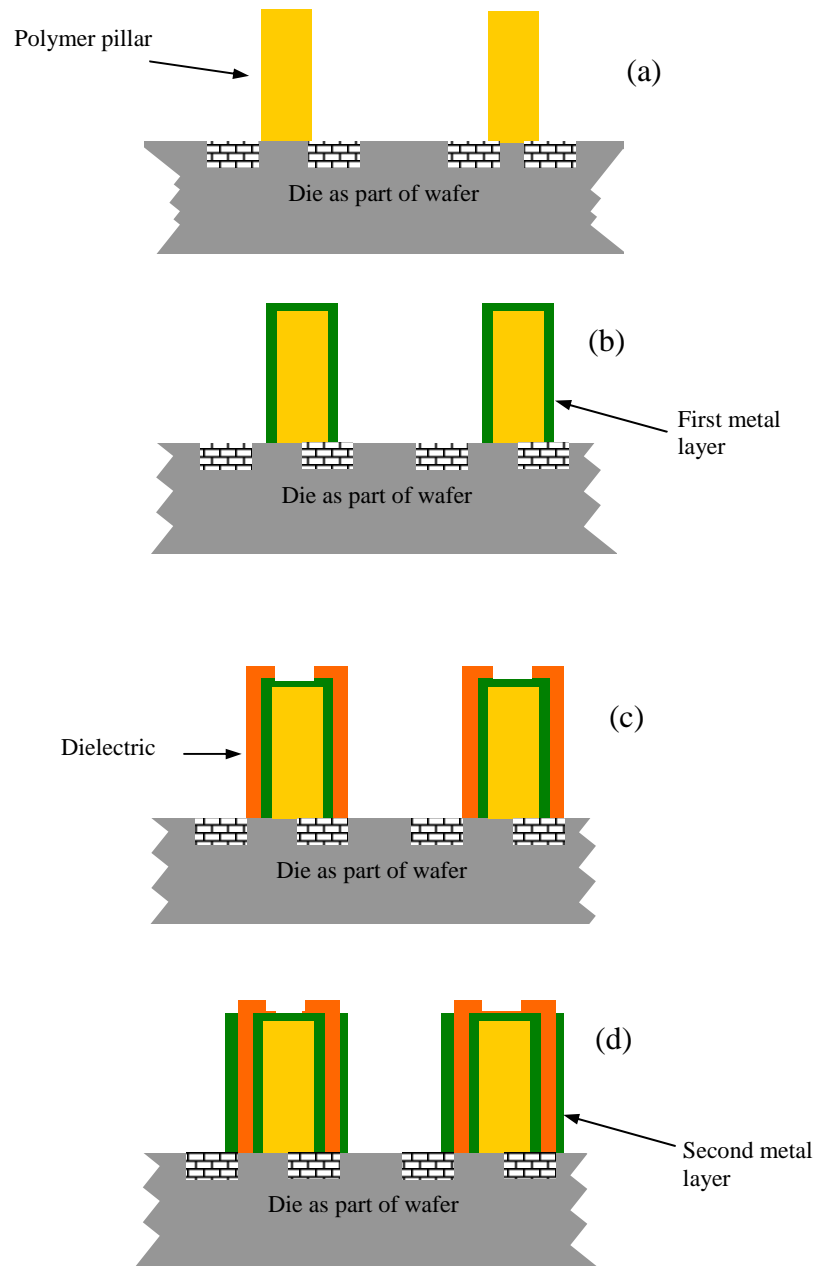


Figure 9-7: Schematic of one version of the fabrication process used to fabricate compliant coaxial polymer pillars. Pillars are fabricated using a photodefinable polymer (a), metal layer is deposited on the pillars (b), dielectric is deposited and a portion of it at the tip of the pillar is etched to enable access to the underlying electrical layer (c), second metal layer is deposited and patterned such that it only covers the sidewalls of the pillars. Alternatively, metallic pillars may substitute for the metallized pillars in (b).

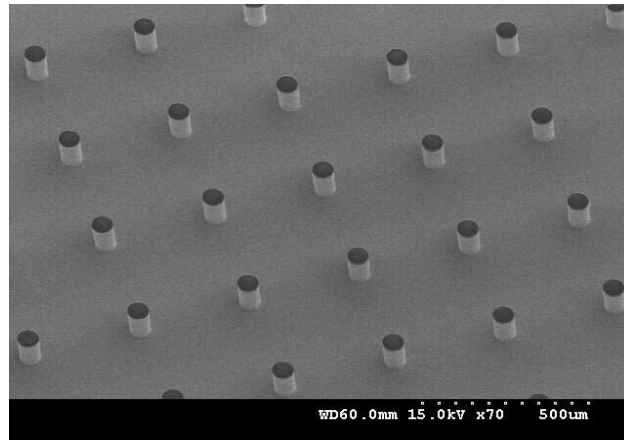


Figure 9-8: Scanning electron microscope (SEM) micrograph of an array of polymer pillars.

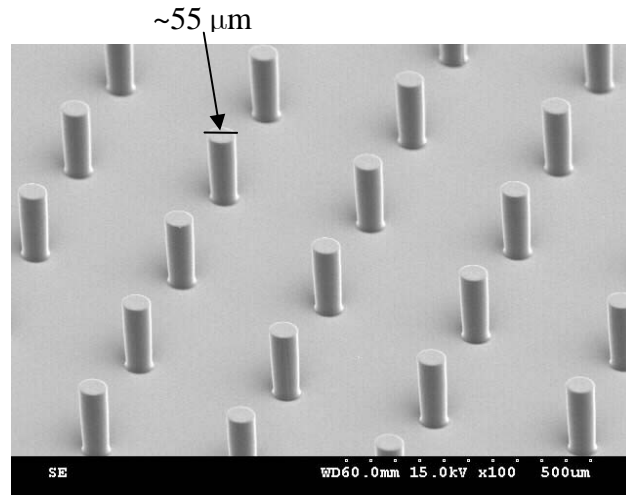


Figure 9-9: Scanning electron microscope (SEM) micrograph of polymer pillars with metal films covering their Sidewall.

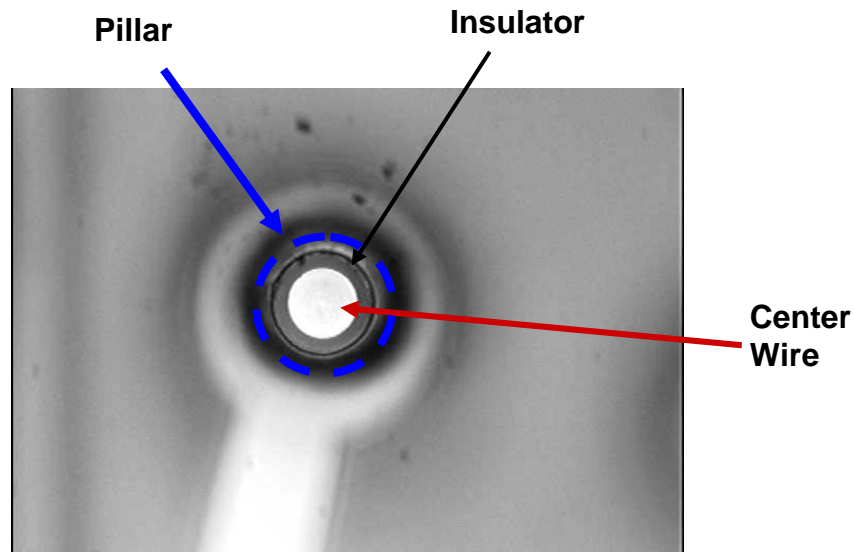


Figure 9-10: Scanning electron microscope (SEM) micrograph of a coaxial polymer pillar.

9.4 Conclusion

Simultaneous switching noise (SSN), which is due to varying current passing through the parasitic inductances of I/O interconnects, has become a limiting factor to increase the speed of future high performance VLSI chips. Coaxial polymer pillars (CoPP) are introduced to minimize the parasitic inductances of I/O interconnects and as a result minimize SSN. In a regular chip, thousands of these CoPP's are needed, resulting in a significant decoupling capacitance which reduces the SSN even further. A CoPP 50 μm wide and 100 μm tall, with a dielectric of 0.1 μm , has a parasitic inductance of only 0.08pH which is almost two decades smaller than the inductance of a solder bump or a regular polymer pillar. A key feature of this technology is its compatibility with optical polymer pillars.

Providing the mechanical interconnection between the chip and the board becomes more challenging as low-k dielectrics are integrated in high performance chips. The coefficient of thermal expansion (CTE) mismatch between the Si chip and the board can cause damage in the low-k interlayer dielectric. Problems caused by CTE mismatch may be overcome with the use of mechanically compliant I/O interconnections. The intrinsic pillars are designed to be mechanically compliant. The thickness of the metal films and insulating layer are selected to minimize the degradation in the lateral compliance of the pillars. High aspect ratio pillars have demonstrated compliance larger than $10\mu\text{m}/\text{mN}$.

Chapter 10

Conclusion and Future Work

In this chapter, the key conclusions of this dissertation are summarized (Section 10.1) and possible extensions of this dissertation are discussed. These extensions include: 1) Extending chip-package co-design methodologies for simultaneous switching noise; 2) Developing a CAD tool for relative inductance; 3) Developing a model for substrate spreading resistance to be included in the IR-drop and simultaneous switching noise models.

10.1 Conclusion of Dissertation

The main objectives of this thesis are: 1) to introduce new chip-package co-design models for IR-drop and electromigration in a GSI chip, 2) accelerate the simulation time of simulating the simultaneous switching noise, 3) introduce a new dynamic logic circuit which is more robust and less sensitive to noise, and 4) to introduce a new input/output technology for power distribution to reduce simultaneous switching noise.

The main contributions of this thesis are as follows:

1. Novel compact physical models for IR-drop of on-chip power/ground interconnection networks are derived for two generic types of packages. These models quantify the tradeoff between on-chip interconnect dimensions and the

number of I/O pads required and therefore enable rigorous chip/package co-design.

2. A new equivalent inductance matrix called the *relative* inductance matrix is defined to solve massively coupled RLC interconnects. Unlike previous inductance sparsification methods, the new method maintains accuracy for all frequencies even for the cases that there are no near return paths. Therefore it enables modeling of large circuits with reasonable speed and accuracy.
3. Compact models are introduced for the current density in the segments and vias making the power distribution network. These models enable designers of the power distribution network to find the places in the network which are more susceptible to noise and solve the problem sooner, reducing the cost of over-design.
4. Compact physical 2D and 3D models have been derived for the spreading resistance between multiple contacts within two different substrates. These models can be used to estimate substrate noise.
5. A new model is introduced to consider the supply noise effect on the noise margin of different logic families (dynamic logic and static logic). These models enable designers to model input noise and supply noise at the same time.
6. A compact delay model for series connected MOSFETs has been derived. This model enables accurate prediction of worst-case delay of different logic families such as dynamic logic. It also provides insight into delay change as the device parameters change. Key results show that the relative delay of series connected MOSFETs is almost invariant for different generations of technology.

7. A novel domino circuit is introduced to easily increase the noise margin of these kinds of circuits without affecting their speed. Simulations for a 3-input 180nm AND gate shows that the noise margin can be increased by 62% with only 3% reduction in the speed. The Three-Phase circuit does not suffer from leakage current. It is not sensitive to charge sharing noise which is an important source of noise in dynamic logic circuits. The crosstalk noise which is the biggest source of noise can also be eliminated by applying some simple rules when laying out the wires.
8. An ultra-low inductance I/O interconnect called coaxial polymer pillar (CoPP) is introduced that is compatible with sea of polymer pillars (SoPP) [28], [29]. Polymer pillars are highly process-integrated and mechanically flexible (compliant) electrical-optical I/O interconnections that mitigate thermo-mechanical expansion mismatches. The 100× smaller parasitic inductance of the CoPP (in the range of 0.1pH) compared to the inductance of a solder bump or a regular polymer pillar makes it an excellent I/O interconnect technology for power distribution. The density of CoPP's exceeds $10^5/\text{cm}^2$.

10.2 Extending Chip-Package Co-Design Methodologies for Simultaneous Switching Noise

In this thesis new compact models were introduced for IR-drop. However, the other source of supply noise is simultaneous switching noise. Compact simultaneous switching noise models would be needed for the designers to estimate the chip-package resources required to meet a target supply noise.

10.3 Developing a Tool for Relative Inductance

Relative inductance was introduced in this thesis. It produces a sparse matrix. It was used to model two examples. However, the use of it is not limited to those applications. It can be used in many applications such as:

- Modeling simultaneous switching noise for the on-chip and the package power distribution network.
- Modeling near and far cross-talk noise for interconnects.
- Modeling jitter and skew for clock tree.
- Modeling of package input/output interconnects.
- Modeling spiral inductance for RF circuits.
- Modeling any application which requires inductance extraction.

The tool that has been written has limited flexibility and can be used to just model different size busses and grids. However, a more flexible tool is needed which can be used to model any configuration.

10.4 Developing Models for Substrate Spreading Resistance to be Included in the IR-drop and Simultaneous Switching Noise Models

The models introduced in this thesis are for multiple contacts on two different substrates. To be able to use these models in the IR-drop and simultaneous switching noise models, new models are needed to extract spreading resistance between blocks of circuits. The new models can be added to the IR-drop models to take into account the

effect of the substrate on IR-drop. They can also be used in the circuit model for simultaneous switching noise.

Appendix A

Equivalent Radius for Different Pad Shapes

In [61] an equivalent cylinder has been calculated which has the same capacitance to the surrounding as a non-circular cylinder does. In a homogenous medium, where dielectric permittivity (ϵ) and conductivity (σ) have the same space dependence (independent of space coordinates), the resistance (R) and capacitance (C) for different shapes are related through [68]

$$RC = \frac{C}{G} = \frac{\epsilon}{\sigma}. \quad (10.1)$$

Using this equation if the capacitance between two conductors in an isotropic medium is known the resistance between them can be calculated. Therefore, if an equivalent circle can be found for the pad to have the same capacitance to infinity, then they will have equal resistance to infinity too.

In general the equivalent pad radius is of the form

$$r_{pad} = \alpha D_{pad}, \quad (10.2)$$

where α is a function of the pad shape (TABLE 1).

Appendix B

MATLAB Source Code for Simulating an n-bit Bus

A MATLAB program has been written to simulate different size buses. The inputs to this program are the physical properties of the bus such as: bus size, line width, line thickness, line length... The outputs are three SPICE files for the bus using: partial inductance method, relative inductance method and block diagonal sparsification method. In this appendix the complete source code of this program is given. Each function should be saved in a file with the same name and extension 'm'. For example if the function name is "inductance" it should be saved in a file named "inductance.m". The functions are as follows:

1. Function inductance is the main function. Running this function will make the SPICE files described.

```
function ind=inductance()
% Main function
% the filaments are in y direction
% x_fil is the filament x position
% y_fil is the filament y position
% l_fil is the filament length
% W_fil is the filament Width
% T_fil is the filament Thickness
% S_int is the spacing between interconnects
% input_num is the line number in the bus, where the input is connected to
% num_sig_pg is the number of signal wires between two neighboring power and ground
% sec_size is the size of a section in the Galia sparsification technique
% num_fil_int is the number of filaments per interconnect

num_fil_in=16;
num_int=12+4;
x_int=zeros(1,num_int);
y_int=zeros(1,num_int);
W_int_all=2e-4;
T_int_all=2e-4;
S_int_all=2e-4;
l_int_all=20000e-4;
input_num=8;
```

```

num_sig_pg=4+1;

sec_size=6;

l_int=l_int_all*ones(1,num_int);
W_int=W_int_all*ones(1,num_int);
T_int=T_int_all*ones(1,num_int);

x_int(1)=0;
for i=2:num_int
    x_int(i)=x_int(i-1)+W_int_all+S_int_all;
end

x_ref_int=[14e-4 ,32e-4 ];

[xx,num_int]=size(x_int);
[xx,num_ref_int_1]=size(x_ref_int);
num_ref_int=num_ref_int_1-1;
ref=1;
nfr=0;

T=T_int(1);
W=W_int(1);
S=x_int(2)-x_int(1)-W;
H=1e-4;

Line_to_line_cap=l_int(1)*1e-2/num_fil_int*3.9*8.85e-12*(1.93*(T/H)^1.1+1.14*(W/H)^0.31)*(S/H+0.51)^(-1.45)

C1=3.9*8.85e-12*(2.8*(T/H)^0.222+1.15*(W/H))

Non_ideal_return_cap=l_int(1)*1e-2/num_fil_int*(C1+3.9*8.85e-12*(0.83*(T/H)-0.07*(T/H)^0.222+0.03*(W/H))*(S/H)^(-
1.34))-2*Line_to_line_cap

Load_cap=10e-15;
r_seg=2.2e-6*l_int(1)/num_fil_int/W_int(1)/T_int(1);

% Dividing the interconnection into filaments in y direction

for i=1:num_int
    for j=1:num_fil_int
        x_fil(i,j)=x_int(i);
        y_fil(i,j)=y_int(i)+(j-1)*l_int(i)/num_fil_int;
    end
end

```

```

        L_fil(i,j)=L_int(i)/num_fil_int;
        W_fil(i,j)=W_int(i);
        T_fil(i,j)=T_int(i);
    end
end

% Dividing the interconnection references into filament references in y direction
for i=1:num_ref_int+1
    for j=1:num_fil_int
        x_ref(i,j)=x_ref_int(i);
        y_ref_fil(i,j)=y_int(i)+(j-1)*L_int(i)/num_fil_int;
    end
end

% Assigning the nearest reference to each interconnect
for j=1:num_fil_int
    ref=1;
    nfr=0;
    for i=1:num_int
        if abs(x_fil(i,j)-x_ref_int(ref)) > abs(x_fil(i,j)-x_ref_int(ref+1))
            if ref < num_ref_int
                num_fil_ref(ref,j)=nfr;        % Number of filaments per reference
                ref=ref+1;
                nfr=0;
            end
        end
        nfr=nfr+1;
        ref_fil(i,j)=ref;
    end
    num_fil_ref(ref,j)=nfr;
end

num_int_ref(ref)=nfr;

L_Mat=L_matrix(x_fil,y_fil,l_fil,W_fil,T_fil); % Make the partial inductance matrix

MK_L_spice_file (L_Mat,num_int,num_fil_int,r_seg,input_num,num_sig_pg); % Write the SPICE file for the partial
inductance matrix

Ins_cap_L(Line_to_line_cap,Non_ideal_return_cap,Load_cap,num_fil_int,num_int,num_sig_pg); % Add the capacitances
to the SPICE file

RL_Mat=RL_matrix(x_fil,y_fil,l_fil,W_fil,T_fil,x_ref,ref_fil,y_ref_fil); % Make the relative inductance matrix

```

```
MK_RL_spice_file (RL_Mat,num_int,num_fil_int,num_ref_int,num_fil_ref,r_seg,input_num,num_sig_pg); % Write the
SPICE file for the relative inductance matrix
```

```
Ins_cap_RL(Line_to_line_cap,Non_ideal_return_cap,Load_cap,num_fil_int,num_int,num_sig_pg); % Add the
capacitances to the SPICE file
```

```
SL_Mat=SL_matrix(x_fil,y_fil,l_fil,W_fil,T_fil,sec_size); % Make the diagonal sparsification matrix
```

```
MK_SL_spice_file (SL_Mat,num_int,num_fil_int,r_seg,input_num,num_sig_pg); % Write the SPICE file for the diagonal
sparsification matrix
```

```
Ins_cap_SL(Line_to_line_cap,Non_ideal_return_cap,Load_cap,num_fil_int,num_int,num_sig_pg); % Add the
capacitances to the SPICE file
```

2. This function makes the partial inductance matrix for the bus.

```
function ind=L_matrix(x_fil,y_fil,l_fil,W_fil,T_fil)
```

```
% Inductance extraction function
% the filaments are in y direction
% x_fil is the filament x position
% y_fil is the filament y position
% l_fil is the filament length
% W_fil is the filament Width
% T_fil is the filament Thickness
```

```
[num_int,num_fil_int]=size(x_fil);
```

```
for i1=0:(num_int-1)
```

```
    for i2=1:num_fil_int
```

```
        for j1=0:(num_int-1)
```

```
            for j2=1:num_fil_int
```

```
                n1=i1*num_fil_int+i2;
```

```
                n2=j1*num_fil_int+j2;
```

```
                if n1==n2
```

```
                    ind(n1,n2)=self_ind(W_fil(i1+1,i2),T_fil(i1+1,i2),l_fil(i1+1,i2));
```

```
                else
```

```
                    ind(n1,n2)=mut_ind(l_fil(i1+1,i2),l_fil(j1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_fil(j1+1,j2),y_fil(j1+1,j2),W_fil(i1+1,i2),T_fil(i1+1,i2));
```

```
                end
```

```
            end
```

```

    end
  end
end

```

3. This function makes the SPICE file for the partial inductance matrix.

```
function MK_L_spice_file (L_matrix,num_int,num_fil_int,r_seg,input_num,num_sig_pg)
```

```
% Make Spice file for inductance
```

```
[xx,num_fil]=size(L_matrix);
```

```
% Self inductances are saves in the spice file
```

```
file_name=strcat('hs_',int2str(num_int-floor(num_int/num_sig_pg)-
1),'_',int2str(floor(num_int/num_sig_pg)+1),'_',int2str(num_fil_int),'_L.sp');
```

```
fid = fopen(file_name,'W');
```

```
fprintf(fid,'\n* Self Inductances\n');
```

```
fprintf(fid,'\n\n .OPTIONS post INGOLD=2 LIST');
```

```
fprintf(fid,'\n\n *.OPTION CONVERGE=1 GMINDC= 1.0000E-12');
```

```
fprintf(fid,'\n\n .OPTION ACCT=2');
```

```
fprintf(fid,'\n\n .OPTIONS METHOD=GEAR');
```

```
fprintf(fid,'\n\n .TRAN .001NS .5nS');
```

```
fprintf(fid,'\n\n vcc1 vcc 0 3v');
```

```
for i=1:num_int
```

```
  if mod(i,num_sig_pg) == 1
```

```
    fprintf(fid,'\n\n rpg0_%d VOL_%d_1 0 0.01',i,i);
```

```
  elseif i ~= input_num
```

```
    fprintf(fid,'\n\n r0_%d VOL_%d_1 0 30',i,i);
```

```
  else
```

```
    fprintf(fid,'\n\n vin_1 VOL_%d_1 0 pulse (0,1,0.1n,0.01n,0.01n,1n,5n)',i);
```

```
  end
```

```
end
```

```
fprintf(fid,'\n\n');
```

```
RL_zero=1e-17;
```

```
L_self_ref=10e-15;
```

```
for i=1:num_int
```

```
  for j=1:num_fil_int
```

```

n=j+num_fil_int*(i-1);

fprintf(fid,' L_%d_%d VOL_%d_%d V1L_%d_%d  %e \n',i,j,i,j,L_matrix(n,n));

end
end

% Mutual inductances are saved as voltage controlled voltage sources of the inductance voltages
fprintf(fid,'\n\n* Mutual Inductances');

for i1=1:num_int
for i2=1:num_fil_int

ni=num_fil_int*(i1-1)+i2;

% Mutual inductances of the other inductances

for j1=1:num_int
for j2=1:num_fil_int

nj=num_fil_int*(j1-1)+j2;

if (ni < nj)

fprintf(fid,'\n k_mut_%d_%d L_%d_%d L_%d_%d %e
',ni,nj,i1,i2,j1,j2,L_matrix(ni,nj)/(L_matrix(ni,ni)*L_matrix(nj,nj))^0.5);
end

end

end

end

end

fprintf(fid,'\n\n* Resistances');
for i=1:num_int
for j=1:num_fil_int

n=j+num_fil_int*(i-1);

fprintf(fid,'\n r_%d_%d V1L_%d_%d VOL_%d_%d  %e \n',i,j,i,j+1,r_seg);

end

end
end

```

```
fclose(fid);
```

4. This function adds the parasitic capacitances to the SPICE file for the partial inductance matrix.

```
function [ output_args ] = Ins_cap_L(Line_to_line_cap,Non_ideal_return_cap,Load_cap,num_fil_int,num_int,num_sig_pg)
% Add capacitance to the L spice file
% Detailed explanation goes here
```

```
%fid = fopen('test_L.sp','a');
file_name=strcat('hs_',int2str(num_int-floor(num_int/num_sig_pg)-
1),'_',int2str(floor(num_int/num_sig_pg)+1),'_',int2str(num_fil_int),'_L.sp');
fid = fopen(file_name,'a');
fprintf(fid,'\n\n\n* Line to Line Capacitances and Non-deal return path Added\n\n');

for i=1:num_int-1
    for j=1:num_fil_int

        fprintf(fid,' C_L2L_%d_%d V0L_%d_%d V0L_%d_%d %e \n',i,j,i,j,i+1,j,Line_to_line_cap); %Line to Line

        fprintf(fid,' C_L2N_%d_%d V0L_%d_%d Vn0L_%d %e \n',i,j,i,j,j,Non_ideal_return_cap); %Non Ideal return path
        capacitance

    end
end

i=i+1;
for j=1:num_fil_int

    fprintf(fid,' C_L2N_%d_%d V0L_%d_%d Vn0L_%d %e \n',i,j,i,j,j,Non_ideal_return_cap); %Non Ideal return path
    capacitance
    fprintf(fid,' r_L2N_%d_%d Vn0L_%d 0 1e6 \n',i,j,j); %dummy resitance

end

fprintf(fid,'\n\n\n* Load Capacitance \n\n',i,j,i,j,i+1,j,Load_cap);

for i=1:num_int
    if mod(i,num_sig_pg) == 1
```

```

        fprintf(fid, '\n\n rpg1_%d VOL_%d_%d V_end 0.1\n', i, i, j+1);
    else
        fprintf(fid, ' CL_%d_%d VOL_%d_%d V_end %e \n', i, j+1, i, j+1, Load_cap);
    end
end
end

fprintf(fid, '\n\n .end\n');

fclose(fid);

```

5. This function makes the relative inductance matrix.

```

function ind=RL_matrix(x_fil,y_fil,l_fil,W_fil,T_fil,x_ref,ref_fil,y_ref_fil)
% Relative inductance extraction function
% the filaments are in y direction
% x_fil is the filament x position
% y_fil is the filament y position
% l_fil is the filament length
% W_fil is the filament Width
% T_fil is the filament Thickness
% x_ref_fil is the x location of the filament
% ref_fil is the reference nearest to the filament

[num_int,num_fil_int]=size(x_fil)
[num_ref_1,xx]=size(x_ref);
num_ref=num_ref_1-1

for i1=0:(num_int-1)
    for i2=1:num_fil_int
        for j1=0:(num_int-1)
            for j2=1:num_fil_int
                n1=i1*num_fil_int+i2; % row
                n2=j1*num_fil_int+j2; % column
                if n1==n2
                    % Relative Self inductance
                    if abs(x_ref(ref_fil(i1+1,i2),i2) - x_fil(i1+1,i2)) <= 1e-6
                        ind(n1,n2)=0;
                    else

```

```

        ind(n1,n2)=self_ind(W_fil(i1+1,i2),T_fil(i1+1,i2),L_fil(i1+1,i2))-
mut_ind(L_fil(i1+1,i2),l_fil(i1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_ref(ref_fil(i1+1,i2),i2),y_fil(i1+1,i2),W_fil(i1+1,i2),T_fil(i1+1,i2)
);
        end

    else
        % Relative Mutual Inductance
        if abs(x_fil(j1+1,j2)-x_fil(i1+1,i2)) > abs(x_fil(i1+1,i2)-x_ref(ref_fil(j1+1,j2),j2))
            sign = -1;
        else
            sign = +1;
        end

        if abs(x_ref(ref_fil(j1+1,j2),j2) - x_fil(j1+1,j2)) < 1e-6 %The second line is on the reference

            ind(n1,n2)=0;

            elseif (abs(x_ref(ref_fil(j1+1,j2)) - x_fil(i1+1,i2)) < 1e-6 ) & (abs(y_fil(i1+1,i2)-y_fil(j1+1,j2)) < 1e-6) % The
reference of the second filament is on the first filament

            ind(n1,n2)=sign*abs(self_ind(W_fil(i1+1,i2),T_fil(i1+1,i2),L_fil(i1+1,i2))-
mut_ind(L_fil(i1+1,i2),l_fil(j1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_fil(j1+1,j2),y_fil(j1+1,j2),W_fil(i1+1,i2),T_fil(i1+1,i2)));

        else %Relative mutual inductance of the rest of the filaments
            if (y_fil(i1+1,i2)~=y_fil(j1+1,j2))
                ind(n1,n2)=0;
            else

ind(n1,n2)=sign*abs(mut_ind(L_fil(i1+1,i2),l_fil(j1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_fil(j1+1,j2),y_fil(j1+1,j2),W_fil(i1+1,i2),T
_fil(i1+1,i2))-
mut_ind(L_fil(i1+1,i2),l_fil(j1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_ref(ref_fil(j1+1,j2),j2),y_fil(j1+1,j2),W_fil(i1+1,i2),T_fil(i1+1,i2)
));

            end
        end
    end
end
end
end
end
end
end

%% References

for i1=0:(num_int-1)
    for i2=1:num_fil_int

        for j1=0:num_ref-1

```

```

for j2=1:num_fil_int
    n1=i1*num_fil_int+i2;          % Row
    n2=num_fil_int*num_int+j1*num_fil_int+j2; % Column

    % if abs(x_ref(j1+1,j2)-x_fil(i1+1,i2)) > abs(x_fil(i1+1,i2)-x_fil(i1+1,i2))
    %     sign = -1;
    % else
    %     sign = +1;
    % end

    if abs(x_fil(i1+1,i2) - x_ref(j1+1,j2)) < 1e-6 & (abs(y_fil(i1+1,i2)-y_ref_fil(j1+1,j2)) < 1e-6)

        ind(n1,n2)=abs(self_ind(W_fil(i1+1,i2),T_fil(i1+1,i2),L_fil(i1+1,i2)));

    else

ind(n1,n2)=abs((mut_ind(l_fil(i1+1,i2),l_fil(i1+1,i2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_ref(j1+1,j2),y_ref_fil(j1+1,j2),W_fil(i1+1,i2),T
_fil(i1+1,i2))));

        end
    end
end

end
end

end

end

for i=num_int*num_fil_int+1:num_int*num_fil_int+num_ref*num_fil_int

    for j=1:(num_int*num_fil_int+num_ref*num_fil_int)

        ind(i,j)=0;

    end

end
end

```

6. This function makes the SPICE file for the relative inductance matrix.

```
function MK_RL_spice_file (RL_matrix,num_int,num_fil_int,num_ref,num_int_ref,r_seg,input_num,num_sig_pg)
% Make Saprse Spice file for relative inductance
% Self inductances are saved in the spice file
% The total inductance for each inductacne is between 0L0%d and 1L0%d'

file_name=strcat('hs_',int2str(num_int-floor(num_int/num_sig_pg)-
1),'_',int2str(floor(num_int/num_sig_pg)+1),'_',int2str(num_fil_int),'_RL.sp');
fid = fopen(file_name,'W');

fprintf(fid,'\n* Self Inductances\n');

fprintf(fid,'\n\n .OPTIONS post INGOLD=2 LIST');
fprintf(fid,'\n\n *.OPTION CONVERGE=1 GMINDC= 1.0000E-12');
fprintf(fid,'\n\n .OPTION ACCT=2');
fprintf(fid,'\n\n .OPTIONS METHOD=GEAR');
fprintf(fid,'\n\n .TRAN .001NS .5nS');
fprintf(fid,'\n\n vcc1 vcc 0 3v');

for i=1:num_int
    if mod(i,num_sig_pg) == 1
        fprintf(fid,'\n\n rpg0_%d VOL_%d_1 0 0.01',i,i);
    elseif i ~= input_num
        fprintf(fid,'\n\n r0_%d VOL_%d_1 0 30',i,i);
    else
        fprintf(fid,'\n\n vin_1 VOL_%d_1 0 pulse (0,1,0.1n,0.01n,0.01n,1n,5n)',i);
    end
end

fprintf(fid,'\n\n');

RL_zero=1e-15;
L_self_ref=10e-9;

num_int
num_fil_int

for i=1:num_int
    for j=1:num_fil_int
        n=j+num_fil_int*(i-1);
        if RL_matrix(n,n)==0
```

```

        fprintf(fid,'L_%d_%d V0L_%d_%d V1L_%d_%d %e \n',i,j,i,j,i,j,RL_zero); % If the self inductance is zero put a
small inductance there for mutual inductance
    else
        fprintf(fid,'L_%d_%d V0L_%d_%d V1L_%d_%d %e \n',i,j,i,j,i,j,RL_matrix(n,n));
    end
    %fprintf(fid,'VV_%d_%d V3L_%d_%d V1L_%d_%d %e \n\n',i,j,i,j,i,j,0);
end
end

% Mutual inductances are saved as voltage controlled voltage sources of the inductance voltages
fprintf(fid,'\n\n* Mutual Inductances');
for i1=1:num_int
    for i2=1:num_fil_int
        i=i2+num_fil_int*(i1-1);

        num=0;

        for k1=1:num_int
            for k2=1:num_fil_int
                k=k2+num_fil_int*(k1-1);
                if RL_matrix(k,k)==0
                    if abs(RL_matrix(i,k)/RL_zero) > 0.1
                        if i~=k
                            num=num+1;
                        end
                    end
                else
                    if abs(RL_matrix(i,k)/RL_matrix(k,k)) > 0.1
                        if i~=k
                            num=num+1;
                        end
                    end
                end
            end
        end
    end
end

fprintf(fid,'\n\n e_mut_%d_%d V1L_%d_%d V2L_%d_%d POLY(%d) \n + ',i1,i2,i1,i2,num+num_ref*num_fil_int);
% Mutual inductances of the other inductances
num_mut=0;
for j1=1:num_int
    for j2=1:num_fil_int
        j=j2+num_fil_int*(j1-1);
        if RL_matrix(j,j)==0
            if abs(RL_matrix(i,j)/RL_zero) > 0.1
                num_mut=num_mut+1;
            end
        end
    end
end

```

```

        if i~=j
            fprintf(fid,'VOL_%d_%d V1L_%d_%d ',j1,j2,j1,j2);
        end
    end
else
    if abs(RL_matrix(i,j)/RL_matrix(j,i)) > 0.1
        num_mut=num_mut+1;
        if i~=j
            fprintf(fid,'VOL_%d_%d V1L_%d_%d ',j1,j2,j1,j2);
        end
    end
end
end
if mod(num_mut,8)==0
    fprintf(fid,'\n + ');
    num_mut=num_mut+1;
end
end
end
end

```

% Mutual inductances of the references

```

for j1=1:num_ref
    for j2=1:num_fil_int
        fprintf(fid,'TOL_%d_%d 0 ',j1,j2);
        if mod(num_mut,8)==0
            fprintf(fid,'\n + ');
        end
        num_mut=num_mut+1;
    end
end
end

```

```

fprintf(fid,'\n + 0 ');

```

% Mutual inductances of the other inductances

```

num_mut=1;
for j=1:num_int*num_fil_int
    if i~=j
        if RL_matrix(j,j)==0
            if abs(RL_matrix(i,j)/RL_zero) > 0.1
                num_mut=num_mut+1;
                fprintf(fid,'%e ',RL_matrix(i,j)/RL_zero);
            end
        else
            if abs(RL_matrix(i,j)/RL_matrix(j,i)) > 0.1
                num_mut=num_mut+1;
            end
        end
    end
end

```

```

        fprintf(fid,'%e ',RL_matrix(i,j)/RL_matrix(j,j));
    end

    end

end

if mod(num_mut,8)==0
    fprintf(fid,'\n + ');
    num_mut=num_mut+1;
end

end

end

% Mutual inductances of the references
for j=num_int*num_fil_int+1:num_int*num_fil_int+num_ref*num_fil_int
    fprintf(fid,'%e ',RL_matrix(i,j)/L_self_ref);
    if mod(num_mut,8)==0
        fprintf(fid,'\n + ');
    end
    num_mut=num_mut+1;
end

end

end

end

fprintf(fid,'\n\n');

% Current sources for each reference are calculated. It is the sum of all the filaments of that reference

k=ones(1,num_fil_int+1);

for i1=1:num_ref

    for i2=1:num_fil_int
        n=(i1-1)*num_fil_int+i2;
        fprintf(fid,'\n\n G_tot_ref_%d_%d 0 TOL_%d_%d VCCS POLY(%d) \n + ',i1,i2,i1,i2,num_int_ref(i1,i2));

        for j1=1:num_int_ref(i1,i2)

            fprintf(fid,'\V2L_%d_%d V0L_%d_%d ',k(i2),i2,k(i2),i2+1);
            k(i2)=k(i2)+1;
            if mod(j1,10)==0
                fprintf(fid,'\n + ');
            end
        end
    end

    fprintf(fid,'\n + 0 ');
end

```

```

for j=1:num_int_ref(i1,i2)

    fprintf(fid,'%e ',1/r_seg);

    if mod(j,5)==0

        fprintf(fid,'\n + ');
    end
end
end
end

% Self Inductance for each reference

fprintf(fid,'\n\n\n* Self Inductances for references\n');
for i1=1:num_ref
    for i2=1:num_fil_int
        n=(i1-1)*num_fil_int+i2;
        fprintf(fid,'Lr_%d_%d TOL_%d_%d 0 %e \n',i1,i2,i1,i2,L_self_ref);
    end
end

fprintf(fid,'\n\n\n* Resistances');
for i=1:num_int
    for j=1:num_fil_int

        n=j+num_fil_int*(i-1);

        fprintf(fid,'\n r_%d_%d V2L_%d_%d V0L_%d_%d %e \n',i,j,i,j+1,r_seg);

    end
end

fclose(fid);

```

7. This function adds the parasitic capacitances to the SPICE file for the relative inductance matrix.

```
function [ output_args ] =
    Ins_cap_RL(Line_to_line_cap,Non_ideal_return_cap,Load_cap,num_fil_int,num_int,num_sig_pg)
% Add capacitance to the L spice file
% Detailed explanation goes here

%fid = fopen('test_RL.sp','a');
file_name=strcat('hs_',int2str(num_int-floor(num_int/num_sig_pg)-
1),'_',int2str(floor(num_int/num_sig_pg)+1),'_',int2str(num_fil_int),'_RL.sp');
fid = fopen(file_name,'a');

fprintf(fid,'\n\n\n* Line to Line Capacitances and Non-deal return path Added\n\n');

for i=1:num_int-1
    for j=1:num_fil_int

        fprintf(fid,' C_L2L_%d_%d V0L_%d_%d V0L_%d_%d  %e \n',i,j,i,j,i+1,j,Line_to_line_cap); %Line to Line

        fprintf(fid,' C_L2N_%d_%d V0L_%d_%d Vn0L_%d  %e \n',i,j,i,j,j,Non_ideal_return_cap); %Non Ideal return path
        capacitance

    end
end

%for j=1:num_fil_int

%    fprintf(fid,' C_L3N_%d 0 Vn0L_%d 1e-18 \n',i,j); %Non Ideal return path capacitance

%end

i=i+1;
for j=1:num_fil_int

        fprintf(fid,' C_L2N_%d_%d V0L_%d_%d Vn0L_%d  %e \n',i,j,i,j,j,Non_ideal_return_cap); %Non Ideal return path
        capacitance
        fprintf(fid,' r_L2N_%d_%d Vn0L_%d 0 1e6 \n',i,j,j); %dummy resitance
    end
end
```

```

fprintf(fid, '\n\n* Load Capacitance \n\n',i,j,i,j,i+1,j,Load_cap);

for i=1:num_int
    if mod(i,num_sig_pg) == 1
        fprintf(fid, '\n\n rpg1_ %d VOL_ %d_ %d V_end 0.1\n',i,i,j+1);
    else
        fprintf(fid, ' CL_ %d_ %d VOL_ %d_ %d V_end %e \n',i,j+1,i,j+1,Load_cap);
    end
end

fprintf(fid, '\n\n .end\n');

fclose(fid);

```

8. This function makes the block diagonal sparsification inductance matrix.

```

function ind=SL_matrix(x_fil,y_fil,l_fil,W_fil,T_fil,sec_size)
% Inductance extraction function
% the filaments are in y direction
% x_fil is the filament x position
% y_fil is the filament y position
% l_fil is the filament length
% W_fil is the filament Width
% T_fil is the filament Thickness

[num_int,num_fil_int]=size(x_fil);

ind=zeros(num_int*num_fil_int,num_int,num_fil_int);

for i1=1: num_int
    for i2=1:num_fil_int
        sh=floor(mod(num_int,sec_size)/2);
        k1=floor((i1-1+sh)/sec_size);
        for j1=max(1,k1*sec_size-sh+1) : min((k1+1)*sec_size - sh,num_int) %Sections are selected to be symmetrical from
the center nterconnect
            for j2=1:num_fil_int
                n1=(i1-1)*num_fil_int+i2;
                n2=(j1-1)*num_fil_int+j2;
                if n1==n2
                    ind(n1,n2)=self_ind(W_fil(i1,i2),T_fil(i1,i2),l_fil(i1,i2));
                else
                    ind(n1,n2)=mut_ind(l_fil(i1,i2),l_fil(j1,j2),x_fil(i1,i2),y_fil(i1,i2),x_fil(j1,j2),y_fil(j1,j2),W_fil(i1,i2),T_fil(i1,i2));
                end
            end
        end
    end
end

```

```

        end
    end
end
end
end

```

9. This function makes the SPICE file for the block diagonal sparsification inductance matrix.

```

function MK_SL_spice_file (SL_matrix,num_int,num_fil_int,r_seg,input_num,num_sig_pg)

% Make Sparse Spice file for inductance based on a technique introduced in Dac 2000 by Gala

[xx,num_fil]=size(SL_matrix);

% Self inductances are saved in the spice file
file_name=strcat('hs_',int2str(num_int-floor(num_int/num_sig_pg)-
1),'_',int2str(floor(num_int/num_sig_pg)+1),'_',int2str(num_fil_int),'_SL.sp');
fid = fopen(file_name,'W');
fprintf(fid,'\n* Self Inductances\n');

fprintf(fid,'\n\n .OPTIONS post INGOLD=2 LIST');
fprintf(fid,'\n\n *.OPTION CONVERGE=1 GMINDC= 1.0000E-12');
fprintf(fid,'\n\n .OPTION ACCT=2');
fprintf(fid,'\n\n .OPTIONS METHOD=GEAR');
fprintf(fid,'\n\n .TRAN .001NS .5nS');
fprintf(fid,'\n\n vcc1 vcc 0 3v');

for i=1:num_int
    if mod(i,num_sig_pg) == 1
        fprintf(fid,'\n\n rpg0_%d VOL_%d_1 0 0.01',i,i);
    elseif i ~= input_num
        fprintf(fid,'\n\n r0_%d VOL_%d_1 0 30',i,i);
    else
        fprintf(fid,'\n\n vin_1 VOL_%d_1 0 pulse (0,1,0.1n,0.01n,0.01n,1n,5n)',i);
    end
end
end

fprintf(fid,'\n\n');

RL_zero=1e-17;
L_self_ref=10e-15;

```

```

for i=1:num_int
    for j=1:num_fil_int

        n=j+num_fil_int*(i-1);

        fprintf(fid,' L_%d_%d V0L_%d_%d V1L_%d_%d  %e \n',i,j,i,j,SL_matrix(n,n));

    end
end

% Mutual inductances are saved as voltage controlled voltage sources of the inductance voltages
fprintf(fid,'\n\n* Mutual Inductances');

for i1=1:num_int
    for i2=1:num_fil_int

        ni=num_fil_int*(i1-1)+i2;

        % Mutual inductances of the other inductances

        for j1=1:num_int
            for j2=1:num_fil_int

                nj=num_fil_int*(j1-1)+j2;

                if (ni < nj)
                    if SL_matrix(ni,nj) ~= 0
                        fprintf(fid,'\n k_mut_%d_%d L_%d_%d L_%d_%d %e
',ni,nj,i1,i2,j1,j2,SL_matrix(ni,nj)/(SL_matrix(ni,ni)*SL_matrix(nj,nj))^0.5);
                    end
                end
            end
        end
    end
end

end
end

fprintf(fid,'\n\n* Resistances');

for i=1:num_int
    for j=1:num_fil_int

```

```

n=j+num_fil_int*(i-1);
fprintf(fid,'\n r_%d_%d V1L_%d_%d V0L_%d_%d %e \n',i,j,i,j+1,r_seg);

end
end

fclose(fid);

```

10. This function adds the parasitic capacitances to the SPICE file for the block diagonal sparsification inductance matrix.

```

function [ output_args ] =
Ins_cap_SL(Line_to_line_cap,Non_ideal_return_cap,Load_cap,num_fil_int,num_int,num_sig_pg)
% Add capacitance to the L spice file
% Detailed explanation goes here

%fid = fopen('test_SL.sp','a');
file_name=strcat('hs_',int2str(num_int-floor(num_int/num_sig_pg)-
1),'_',int2str(floor(num_int/num_sig_pg)+1),'_',int2str(num_fil_int),'_SL.sp');
fid = fopen(file_name,'a');

fprintf(fid,'\n\n\n\n* Line to Line Capacitances and Non-deal return path Added\n\n');

for i=1:num_int-1
for j=1:num_fil_int

fprintf(fid,' C_L2L_%d_%d V0L_%d_%d V0L_%d_%d %e \n',i,j,i,j+1,j,Line_to_line_cap); %Line to Line

fprintf(fid,' C_L2N_%d_%d V0L_%d_%d Vn0L_%d %e \n',i,j,i,j,Non_ideal_return_cap); %Non Ideal return path
capacitance

end
end

i=i+1;
for j=1:num_fil_int

```

```

        fprintf(fid,' C_L2N_%d_%d VOL_%d_%d Vn0L_%d %e \n',i,j,i,j,Non_ideal_return_cap); %Non Ideal return path
        capacitance
        fprintf(fid,' r_L2N_%d_%d Vn0L_%d 0 1e6 \n',i,j,j); %dummy resitance

    end

    fprintf(fid,'\n\n Load Capacitance \n\n',i,j,i,j,i+1,j,Load_cap);

    for i=1:num_int
        if mod(i,num_sig_pg) == 1
            fprintf(fid,'\n\n rpg1_%d VOL_%d_%d V_end 0.1\n',i,i,j+1);
        else
            fprintf(fid,' CL_%d_%d VOL_%d_%d V_end %e \n',i,j+1,i,j+1,Load_cap);
        end
    end

    fprintf(fid,'\n\n .end\n');

    fclose(fid);

```

11. This function calculates the self inductance.

```

function self=self_ind (W0,T0,L0)
% Self inductance calculation for a filament
% Fast henry
% All lengths are in cm

w=W0/L0;
t=T0/L0;
r=(w^2+t^2)^0.5;
aw=(w^2+1)^0.5;
at=(t^2+1)^0.5;
ar=(w^2+t^2+1)^0.5;

self=L0/100*2*(4*pi*1e-7)/pi* ( 1/4*(1/w*asinh(w/at)+1/t*asinh(t/aw)+asinh(1/r))+ 1/24*(t^2/w*asinh(w/t/at/(r+ar))
+w^2/t*asinh(t/w/aw/(r+ar))+ t^2/w^2*
asinh(w^2/t/r/(at+ar))+w^2/t^2*asinh(t^2/w/r/(aw+ar))+1/w*t^2*asinh(w*t^2/at/(aw+ar))+1/t*w^2*asinh(t*w^2/aw/(at+ar))) -
1/6*(1/w*t*atan(w*t/ar)+t*w*atan(w/t/ar)+w*t*atan(t/w/ar)) -1/60*( (ar+r+t+at)*t^2/ (ar+r)/(r+t)/(t+at)/(at+ar) +

```

$$\frac{(ar+r+w+aw)*w^2}{(ar+r)(r+w)(w+aw)(aw+ar)} + \frac{(ar+aw+1+at)}{(ar+aw)(aw+1)(1+at)(at+ar)} - \frac{1}{20} \left(\frac{1}{(r+ar)} + \frac{1}{(aw+ar)} + \frac{1}{(at+ar)} \right);$$

12. This function calculates the mutual inductance.

```
function mut=mut_ind (l,m,x1,y1,x2,y2,W1,T1)
% Mutual inductance calculation for a filament
% Grover
% All lengths are in cm

d=abs(x2-x1);
%if abs(d) > 1e-6

if abs(y2-y1)<=0.01*l
mut=0;

if y2>y1
delta=y2-y1-l;
else
delta=y1-y2-l;
end

alpha=l+m+delta;
beta=l+delta;
gama=m+delta;

mut=1e-6*0.001*(alpha*asinh(alpha/d)-beta*asinh(beta/d)-gama*asinh(gama/d)+delta*asinh(delta/d)-
(alpha^2+d^2)^0.5+(beta^2+d^2)^0.5+(gama^2+d^2)^0.5-(delta^2+d^2)^0.5);

else
if abs(y2-y1)-l<=0.01*l

mut=(self_ind(W1,T1,l+m)-2*self_ind(W1,T1,l))/2; %Wires are in series and they have the same thickness

else

mut=(self_ind(W1,T1,abs(y2-y1)+m)-self_ind(W1,T1,abs(y2-y1)-l+m)-self_ind(W1,T1,abs(y2-
y1))+self_ind(W1,T1,abs(y2-y1)-l))/2; %Wires are in series and they have the same thickness

end
end
```

Appendix C

MATLAB Source Code for Simulating Simultaneous Switching Noise in a Grid

A MATLAB program has been written to simulate simultaneous switching noise for different size grids. The inputs to this program are the physical properties of the grid such as: grid size, grid segment width, grid segment thickness, grid segment length... The outputs are two SPICE files for the bus using: partial inductance method and relative inductance method. In this appendix the complete source code of this program is given. Each function should be saved in a file with the same name and extension 'm'. For example if the function name is "SSN" it should be saved in a file named "SSN.m". The functions are as follows:

1. Function SSN is the main function. Running this function will make the SPICE files described.

```
function ind=SSN()
% Main function
% the filaments are in y direction
% x_fil is the filament x position
% y_fil is the filament y position
% l_fil is the filament length
% W_fil is the filament Width
% T_fil is the filament Thickness
% S_int is the spacing between interconnects
% input_num is the line number in the bus, where the input is connected to
% num_sig_pg is the number of signal wires between two neighboring power and ground
% sec_size is the size of a section in the Galia sparsification technique

num_int=40;
num_fil_int=num_int;

num_int=num_int+1;
```

```

x_int=zeros(1,num_int);
y_int=zeros(1,num_int);
W_int_all=1e-4;
T_int_all=1e-4;
S_int_all=1e-4;
l_int_all=28e-4*num_int;
Deco_cap=1.5e-12;
pin_every_n_seg=18;
curr_per_seg=40e-4;
num_ref_int=5;
reso=0.02;

x_ref_int=[114e-4, 344e-4 ,574e-4 ,803e-4, 1033e-4, 1262e-4];

RL_ref=self_ind(W_int_all,T_int_all,l_int_all/num_int);

l_int=l_int_all*ones(1,num_int);
W_int=W_int_all*ones(1,num_int);
T_int=T_int_all*ones(1,num_int);

x_int(1)=0;
for i=1:num_int
    x_int(i)=i*28e-4;
end

[xx,num_int]=size(x_int);
[xx,num_ref_int_1]=size(x_ref_int);
%num_ref_int=num_ref_int_1-1;
ref=1;
nfr=0;

T=T_int(1);
W=W_int(1);
S=x_int(2)-x_int(1)-W;
H=1e-4;

r_seg=2.2e-6*l_int(1)/num_fil_int/W_int(1)/T_int(1);

% Dividing the interconnection into filaments in y direction

for i=1:num_int
    for j=1:num_fil_int

```

```

    x_fil(i,j)=x_int(i);
    y_fil(i,j)=y_int(i)+(j-1)*l_int(i)/num_fil_int;
    l_fil(i,j)=l_int(i)/num_fil_int;
    W_fil(i,j)=W_int(i);
    T_fil(i,j)=T_int(i);
end
end

% Dividing the interconnection references into filament references in y direction
for i=1:num_ref_int+1
    for j=1:num_fil_int
        x_ref(i,j)=x_ref_int(i);
        y_ref_fil(i,j)=y_int(i)+(j-1)*l_int(i)/num_fil_int;
    end
end

for j=1:num_fil_int
    ref=1;
    nfr=0;
    for i=1:num_int
        if abs(x_fil(i,j)-x_ref_int(ref)) > abs(x_fil(i,j)-x_ref_int(ref+1))
            if ref < num_ref_int
                num_fil_ref(ref,j)=nfr;        % Number of filaments per reference
                ref=ref+1;
                nfr=0;
            end
        end
        nfr=nfr+1;
        ref_fil(i,j)=ref;
    end
    num_fil_ref(ref,j)=nfr;
end

num_int_ref(ref)=nfr;

L_Mat=L_matrix(x_fil,y_fil,l_fil,W_fil,T_fil);
MK_L_spice_file(L_Mat,num_int,num_fil_int,r_seg,pin_every_n_seg,curr_per_seg);
Ins_cap_L(Deco_cap,num_fil_int,num_int);

RL_Mat=RL_matrix(x_fil,y_fil,l_fil,W_fil,T_fil,x_ref,ref_fil,y_ref_fil);
MK_RL_spice_file(RL_Mat,num_int,num_fil_int,num_ref_int,num_fil_ref,r_seg,pin_every_n_seg,curr_per_seg,reso,RL_ref
);

Ins_cap_RL(Deco_cap,num_fil_int,num_int,num_ref_int);

```

2. This function makes the partial inductance matrix for the grid.

```
function ind=L_matrix(x_fil,y_fil,L_fil,W_fil,T_fil)
% Inductance extraction function
% the filaments are in y direction
% x_fil is the filament x position
% y_fil is the filament y positon
% L_fil is the filametrn length
% W_fil is the filament Width
% T_fil is the filament Tickness

[num_int,num_fil_int]=size(x_fil);

for i1=0:(num_int-1)
    for i2=1:num_fil_int
        for j1=0:(num_int-1)
            for j2=1:num_fil_int
                n1=i1*num_fil_int+i2;
                n2=j1*num_fil_int+j2;
                if n1==n2
                    ind(n1,n2)=self_ind(W_fil(i1+1,i2),T_fil(i1+1,i2),L_fil(i1+1,i2));
                else

ind(n1,n2)=mut_ind(l_fil(i1+1,i2),l_fil(j1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_fil(j1+1,j2),y_fil(j1+1,j2),W_fil(i1+1,i2),T_fil(i1+1,i2
));
                    end
                end
            end
        end
    end
end
end
```

3. This function makes the SPICE file for the partial inductance matrix.

```
function MK_L_spice_file (L_matrix,num_int,num_fil_int,r_seg,pin_every_n_seg,curr_per_seg)

% Make Spice file for inductance

[xx,num_fil]=size(L_matrix);

% Self inductances are saved in the spice file
```

```

file_name=strcat('hs_',int2str(num_int-1),'_',int2str(num_fil_int),'_L.sp');
fid = fopen(file_name,'W');
fprintf(fid,'\n* Self Inductances\n');

fprintf(fid,'\n\n .OPTIONS post INGOLD=2 LIST');
fprintf(fid,'\n\n *.OPTION CONVERGE=1 GMINDC= 1.0000E-12');
fprintf(fid,'\n\n .OPTION ACCT=2');
fprintf(fid,'\n\n .OPTIONS METHOD=GEAR');
fprintf(fid,'\n\n .TRAN .01NS 100nS');

for i=1:6
    for j=1:6
        fprintf(fid,'\n lin%d_%d 0 VOL%d_%d pulse (0,%d,0.1n,0.01n,0.01n,1n,50n)',i,j,floor(num_int/2)+1-
3+i,floor(num_int/2)+1-3+j,curr_per_seg);
    end
end

t=zeros(num_int+1,num_int+1);

for i=1:num_int
    for j=1:num_fil_int+1
        if mod(i,pin_every_n_seg)-mod(floor((num_int-pin_every_n_seg)/2)+1,pin_every_n_seg)==0 &
mod(j,pin_every_n_seg)-mod(floor((num_fil_int+1-pin_every_n_seg)/2)+1,pin_every_n_seg)==0

            t(i,j)=1;
            fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i-1,j-1,i-1,j-1);
            fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i-1,j,i,j);
            fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i-1,j+1,i-1,j+1);
            fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i,j-1,i,j-1);
            fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i,j,i,j);
            fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i,j+1,i,j+1);
            fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i+1,j-1,i+1,j-1);
            fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i+1,j,i+1,j);
            fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i+1,j+1,i+1,j+1);

        end
    end
end

spy(t);

fprintf(fid,'\n\n');

```

```

RL_zero=1e-17;
L_self_ref=10e-15;

%self inductance of segments in y direction
fprintf(fid,'\n\n* Self Inductances of segments in y direction\n');
for i=1:num_int
    for j=1:num_fil_int

        n=j+num_fil_int*(i-1);

        fprintf(fid,' Ly%d_%d VOL%d_%d V1y%d_%d  %e \n',i,j,i,j,i,j,L_matrix(n,n));

    end
end

%self inductance of segments in x direction
fprintf(fid,'\n\n* Self Inductances of segments in x direction\n');
for i=1:num_int
    for j=1:num_fil_int

        n=j+num_fil_int*(i-1);

        fprintf(fid,' Lx%d_%d VOL%d_%d V1x%d_%d  %e \n',j,i,j,i,j,i,L_matrix(n,n));

    end
end

% Mutual inductances of segments in y direction
fprintf(fid,'\n\n* Mutual Inductances of segments in y direction\n');

for i1=1:num_int
    for i2=1:num_fil_int

        ni=num_fil_int*(i1-1)+i2;

        % Mutual inductances of the other inductances

        for j1=1:num_int
            for j2=1:num_fil_int

                nj=num_fil_int*(j1-1)+j2;

```

```

        if (ni < nj)

            fprintf(fid, '\n ky%d_%d Ly%d_%d Ly%d_%d %e
', ni, nj, i1, i2, j1, j2, L_matrix(ni, nj)/(L_matrix(ni, ni)*L_matrix(nj, nj))^0.5);
            end

        end
    end

end

end

end

end

% Mutual inductances of segments in x direction
fprintf(fid, '\n\n* Mutual Inductances of segments in x direction\n');

for i1=1:num_int
    for i2=1:num_fil_int

        ni=num_fil_int*(i1-1)+i2;

        % Mutual inductances of the other inductances

        for j1=1:num_int
            for j2=1:num_fil_int

                nj=num_fil_int*(j1-1)+j2;

                if (ni < nj)

                    fprintf(fid, '\n kx%d_%d Lx%d_%d Lx%d_%d %e
', nj, ni, i2, i1, j2, j1, L_matrix(ni, nj)/(L_matrix(ni, ni)*L_matrix(nj, nj))^0.5);
                    end

                end
            end
        end

    end

end

end

end

% Resistance of segments in y direction

fprintf(fid, '\n\n* Resistances');
for i=1:num_int

```

```

for j=1:num_fil_int

    n=j+num_fil_int*(i-1);

    fprintf(fid,'\n ry%d_%d V1y%d_%d VOL%d_%d  %e \n',i,j,i,j,i,j+1,r_seg);

end

end

% Resistance of segments in x direction

fprintf(fid,'\n\n* Resistances');
for i=1:num_int
    for j=1:num_fil_int

        n=j+num_fil_int*(i-1);

        fprintf(fid,'\n rx%d_%d V1x%d_%d VOL%d_%d  %e \n',j,i,j,i,j+1,i,r_seg);

    end

end

fclose(fid);

```

4. This function adds the parasitic capacitances to the SPICE file for the partial inductance matrix.

```

function [ output_args ] = Ins_cap_L(Deco_cap,num_fil_int,num_int,num_sig_pg)
% Add capacitance to the L spice file
% Detailed explanation goes here

%fid = fopen('test_L.sp','a');

file_name=strcat('hs_',int2str(num_int-1),'_',int2str(num_fil_int),'_L.sp');
fid = fopen(file_name,'a');
fprintf(fid,'\n\n\n\n* Decoupling Capacitances Added\n\n');

```

```

for i=1:num_int
    for j=1:num_int

        fprintf(fid,' Cde%d_%d VOL%d_%d 0 %e \n',i,j,i,j,Deco_cap); %Line to Line

    end
end

fprintf(fid,'\n\n .end\n');

fclose(fid);

```

5. This function makes the relative inductance matrix.

```

function ind=RL_matrix(x_fil,y_fil,l_fil,W_fil,T_fil,x_ref,ref_fil,y_ref_fil)
% Relative inductance extraction function
% the filaments are in y direction
% x_fil is the filament x position
% y_fil is the filament y position
% l_fil is the filament length
% W_fil is the filament Width
% T_fil is the filament Thickness
% x_ref_fil is the x location of the filament
% ref_fil is the reference nearest to the filament

[num_int,num_fil_int]=size(x_fil)
[num_ref_1,xx]=size(x_ref);
num_ref=num_ref_1-1

for i1=0:(num_int-1)
    for i2=1:num_fil_int
        for j1=0:(num_int-1)
            for j2=1:num_fil_int
                n1=i1*num_fil_int+i2; % row
                n2=j1*num_fil_int+j2; % column
                if n1==n2
                    % Relative Self inductance
                    if abs(x_ref(ref_fil(i1+1,i2),i2) - x_fil(i1+1,i2)) <= 1e-6

```

```

        ind(n1,n2)=0;
    else
        ind(n1,n2)=self_ind(W_fil(i1+1,i2),T_fil(i1+1,i2),L_fil(i1+1,i2))-
mut_ind(l_fil(i1+1,i2),l_fil(i1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_ref(ref_fil(i1+1,i2),i2),y_fil(i1+1,i2),W_fil(i1+1,i2),T_fil(i1+1,i2)
));
    end

else
    % Relative Mutual Inductance
    if abs(x_fil(j1+1,j2)-x_fil(i1+1,i2)) > abs(x_fil(i1+1,i2)-x_ref(ref_fil(j1+1,j2),j2))
        sign = -1;
    else
        sign = +1;
    end

    if abs(x_ref(ref_fil(j1+1,j2),j2) - x_fil(j1+1,j2)) < 1e-6 %The second line is on the reference

        ind(n1,n2)=0;

        elseif (abs(x_ref(ref_fil(j1+1,j2)) - x_fil(i1+1,i2)) < 1e-6 ) & (abs(y_fil(i1+1,i2)-y_fil(j1+1,j2)) < 1e-6) % The
reference of the second filament is on the first filament

        ind(n1,n2)=sign*abs(self_ind(W_fil(i1+1,i2),T_fil(i1+1,i2),l_fil(i1+1,i2))-
mut_ind(l_fil(i1+1,i2),l_fil(j1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_fil(j1+1,j2),y_fil(j1+1,j2),W_fil(i1+1,i2),T_fil(i1+1,i2)));

    else %Relative mutual inductance of the rest of the filaments
        %if (y_fil(i1+1,i2)~=y_fil(j1+1,j2))
        % ind(n1,n2)=0;
        %else

ind(n1,n2)=sign*abs(mut_ind(l_fil(i1+1,i2),l_fil(j1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_fil(j1+1,j2),y_fil(j1+1,j2),W_fil(i1+1,i2),T
_fil(i1+1,i2))-
mut_ind(l_fil(i1+1,i2),l_fil(j1+1,j2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_ref(ref_fil(j1+1,j2),j2),y_fil(j1+1,j2),W_fil(i1+1,i2),T_fil(i1+1,i2)
)));

        %end
    end
end
end
end
end
end
end

%% References

for i1=0:(num_int-1)
    for i2=1:num_fil_int

```

```

for j1=0:num_ref-1
    for j2=1:num_fil_int
        n1=i1*num_fil_int+i2;          % Row
        n2=num_fil_int*num_int+j1*num_fil_int+j2; % Column

        if abs(x_fil(i1+1,i2) - x_ref(j1+1,j2)) < 1e-6 & (abs(y_fil(i1+1,i2)-y_ref_fil(j1+1,j2)) < 1e-6)

            ind(n1,n2)=abs(self_ind(W_fil(i1+1,i2),T_fil(i1+1,i2),L_fil(i1+1,i2)));

        else

            ind(n1,n2)=abs((mut_ind(L_fil(i1+1,i2),L_fil(i1+1,i2),x_fil(i1+1,i2),y_fil(i1+1,i2),x_ref(j1+1,j2),y_ref_fil(j1+1,j2),W_fil(i1+1,i2),T
            _fil(i1+1,i2))));

        end
    end
end

end

end

end

end

for i=num_int*num_fil_int+1:num_int*num_fil_int+num_ref*num_fil_int

    for j=1:(num_int*num_fil_int+num_ref*num_fil_int)

        ind(i,j)=0;

    end

end

end

```

6. This function makes the SPICE file for the relative inductance matrix.

```

function MK_RL_spice_file
(RL_matrix,num_int,num_fil_int,num_ref,num_int_ref,r_seg,pin_every_n_seg,curr_per_seg,reso,RL_ref)

```

```

% Make Saprse Spice file for relative inductance
% Self inductances are saved in the spice file
% The total inductance for each inductacne is between 0L0%d and 1L0%d'

file_name=strcat('hs_',int2str(num_int-1),'_',int2str(num_fil_int),'_',int2str(num_ref),'_RL.sp');
fid = fopen(file_name,'W');

fprintf(fid,'\n* Self Inductances\n');

fprintf(fid,'\n\n .OPTIONS post INGOLD=2 LIST');
fprintf(fid,'\n\n *.OPTION CONVERGE=1 GMINDC= 1.0000E-12');
fprintf(fid,'\n\n .OPTION ACCT=2');
fprintf(fid,'\n\n .OPTIONS METHOD=GEAR');
fprintf(fid,'\n\n .TRAN .01NS 100nS');
fprintf(fid,'\n\n vcc1 vcc 0 3v');

for i=1:6
    for j=1:6
        fprintf(fid,'\n\n lin%d_%d 0 VOL%d_%d pulse (0,%d,0.1n,0.01n,0.01n,1n,50n)',i,j,floor(num_int/2)+1-3+i,floor(num_int/2)+1-3+j,curr_per_seg);
    end
end

for i=1:num_int
    for j=1:num_fil_int+1
        if mod(i,pin_every_n_seg)-mod(floor((num_int-pin_every_n_seg)/2)+1,pin_every_n_seg)==0 &
            mod(j,pin_every_n_seg)-mod(floor((num_fil_int+1-pin_every_n_seg)/2)+1,pin_every_n_seg)==0

                fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i-1,j-1,i-1,j-1);
                fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i-1,j,i,j);
                fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i-1,j+1,i-1,j+1);
                fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i,j-1,i,j-1);
                fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i,j,i,j);
                fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i,j+1,i,j+1);
                fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i+1,j-1,i+1,j-1);
                fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i+1,j,i+1,j);
                fprintf(fid,'\n\n r0%d_%d VOL%d_%d 0 0.001',i+1,j+1,i+1,j+1);

            end
        end
    end

    fprintf(fid,'\n\n');

```

```

RL_zero=1e-15;
L_self_ref=10e-9;

num_int
num_fil_int

% Self Inductance in y direction
fprintf(fid,'\n* Self Inductance in y direction\n');
for i=1:num_int
    for j=1:num_fil_int
        n=j+num_fil_int*(i-1);
        if RL_matrix(n,n)==0
            fprintf(fid,'Ly%d_%d VOL%d_%d V1Ly%d_%d %e \n',i,j,i,j,i,j,RL_zero); % If the self inductance is zero put a small
inducatance there for mutual inductance
        else
            fprintf(fid,'Ly%d_%d VOL%d_%d V1Ly%d_%d %e \n',i,j,i,j,i,j,RL_matrix(n,n));
        end
    end
end

% Self Inductance in x direction
fprintf(fid,'\n* Self Inductance in x direction\n');

for i=1:num_int
    for j=1:num_fil_int
        n=j+num_fil_int*(i-1);
        if RL_matrix(n,n)==0
            fprintf(fid,'Lx%d_%d VOL%d_%d V1Lx%d_%d %e \n',j,i,j,i,j,i,RL_zero); % If the self inductance is zero put a small
inducatance there for mutual inductance
        else
            fprintf(fid,'Lx%d_%d VOL%d_%d V1Lx%d_%d %e \n',j,i,j,i,j,i,RL_matrix(n,n));
        end
    end
end

% Mutual inductances in y direction
% Mutual inductances are saved as voltage controlled voltage sources of the inductance voltages
fprintf(fid,'\n\n* Mutual Inductances in y direction\n');
for i1=1:num_int
    for i2=1:num_fil_int
        i=i2+num_fil_int*(i1-1);

```

```

num=0;

for k1=1:num_int
    for k2=1:num_fil_int
        k=k2+num_fil_int*(k1-1);
        if abs(RL_matrix(i,k)/RL_ref) > reso
            if i~=k
                num=num+1;
            end
        end
    end
end

fprintf(fid,'\n\n e_my%d_%d V1Ly%d_%d V2y%d_%d POLY(%d) \n + ',i1,i2,i1,i2,num+num_ref*num_fil_int);
% Mutual inductances of non-reference segments in y direction
num_mut=0;
for j1=1:num_int
    for j2=1:num_fil_int
        j=j2+num_fil_int*(j1-1);

        if abs(RL_matrix(i,j)/RL_ref) > reso
            num_mut=num_mut+1;
            if i~=j
                fprintf(fid,'VOL%d_%d V1Ly%d_%d ',j1,j2,j1,j2);
            end
        end
    end

    if mod(num_mut,8)==0
        fprintf(fid,'\n + ');
        num_mut=num_mut+1;
    end
end
end

% Mutual inductances of the references in y direction
for j1=1:num_ref
    for j2=1:num_fil_int
        fprintf(fid,'T0y%d_%d 0 ',j1,j2);
        if mod(num_mut,8)==0
            fprintf(fid,'\n + ');
        end
        num_mut=num_mut+1;
    end
end
end

```

```

fprintf(fid, '\n + 0 ');

% Value of Mutual inductances of non-reference segments in y direction
num_mut=1;
for j=1:num_int*num_fil_int
    if i~=j
        if abs(RL_matrix(i,j)/RL_ref) > reso
            if RL_matrix(j,j)==0
                num_mut=num_mut+1;
                fprintf(fid, '%e ', RL_matrix(i,j)/RL_zero);
            else
                num_mut=num_mut+1;
                fprintf(fid, '%e ', RL_matrix(i,j)/RL_matrix(j,j));
            end
        end
    end
end
if mod(num_mut,8)==0
    fprintf(fid, '\n + ');
    num_mut=num_mut+1;
end
end

% Value of Mutual inductances of the references in y direction
for j=num_int*num_fil_int+1:num_int*num_fil_int+num_ref*num_fil_int
    fprintf(fid, '%e ', RL_matrix(i,j)/L_self_ref);
    if mod(num_mut,8)==0
        fprintf(fid, '\n + ');
    end
    num_mut=num_mut+1;
end
end
end

fprintf(fid, '\n\n');

% Mutual inductances in x direction
% Mutual inductances are saved as voltage controlled voltage sources of the inductance voltages
fprintf(fid, '\n\n* Mutual Inductances in x direction\n');
for i1=1:num_int
    for i2=1:num_fil_int
        i=i2+num_fil_int*(i1-1);

```

```

num=0;

for k1=1:num_int
    for k2=1:num_fil_int
        k=k2+num_fil_int*(k1-1);
        if abs(RL_matrix(i,k)/RL_ref) > reso
            if i~=k
                num=num+1;
            end
        end
    end
end

fprintf(fid,'\n\n e_mx%d_%d V1Lx%d_%d V2x%d_%d POLY(%d) \n + ',i2,i1,i2,i1,i2,i1,num+num_ref*num_fil_int);
% Mutual inductances of non-reference segments in x direction
num_mut=0;
for j1=1:num_int
    for j2=1:num_fil_int
        j=j2+num_fil_int*(j1-1);
        if abs(RL_matrix(i,j)/RL_ref) > reso
            num_mut=num_mut+1;
            if i~=j
                fprintf(fid,'VOL%d_%d V1Lx%d_%d ',j2,j1,j2,j1);
            end
        end
    end

    if mod(num_mut,8)==0
        fprintf(fid,'\n + ');
        num_mut=num_mut+1;
    end
end
end

% Mutual inductances of the references in x direction
for j1=1:num_ref
    for j2=1:num_fil_int
        fprintf(fid,'TOx%d_%d 0 ',j2,j1);
        if mod(num_mut,8)==0
            fprintf(fid,'\n + ');
        end
        num_mut=num_mut+1;
    end
end
end

```

```

fprintf(fid, '\n + 0 ');

% Value of Mutual inductances of non-reference segments in x direction
num_mut=1;
for j=1:num_int*num_fil_int
    if i~=j
        if abs(RL_matrix(i,j)/RL_ref) > reso
            if RL_matrix(j,j)==0
                num_mut=num_mut+1;
                fprintf(fid, '%e ', RL_matrix(i,j)/RL_zero);
            else
                num_mut=num_mut+1;
                fprintf(fid, '%e ', RL_matrix(i,j)/RL_matrix(j,j));
            end
        end
    end
end

if mod(num_mut,8)==0
    fprintf(fid, '\n + ');
    num_mut=num_mut+1;
end
end

% Value of Mutual inductances of the references in x direction
for j=num_int*num_fil_int+1:num_int*num_fil_int+num_ref*num_fil_int
    fprintf(fid, '%e ', RL_matrix(i,j)/L_self_ref);
    if mod(num_mut,8)==0
        fprintf(fid, '\n + ');
    end
    num_mut=num_mut+1;
end
end
end

fprintf(fid, '\n\n');

```

% Current sources for each reference in y direction are calculated. It is the sum of all the filaments of that reference

```

k=ones(1,num_fil_int+1);

for i1=1:num_ref

    for i2=1:num_fil_int
        n=(i1-1)*num_fil_int+i2;

```

```

fprintf(fid,'\n\n Gytr%d_%d 0 T0y%d_%d VCCS POLY(%d) \n + ',i1,i2,i1,i2,num_int_ref(i1,1));

for j1=1:num_int_ref(i1,1)

    fprintf(fid,'\V2y%d_%d VOL%d_%d ',k(i2),i2,k(i2),i2+1);
    k(i2)=k(i2)+1;
    if mod(j1,10)==0
        fprintf(fid,'\n + ');
    end
end

fprintf(fid,'\n + 0 ');

for j=1:num_int_ref(i1,1)

    fprintf(fid,'%e ',1/r_seg);

    if mod(j,5)==0

        fprintf(fid,'\n + ');
    end
end
end
end

% Current sources for each reference in x direction are calculated. It is the sum of all the filaments of that reference

k=ones(1,num_fil_int+1);

for i1=1:num_ref

    for i2=1:num_fil_int
        n=(i1-1)*num_fil_int+i2;
        fprintf(fid,'\n\n Gxtr%d_%d 0 T0x%d_%d VCCS POLY(%d) \n + ',i2,i1,i2,i1,num_int_ref(i1,1));

        for j1=1:num_int_ref(i1,1)

            fprintf(fid,'\V2x%d_%d VOL%d_%d ',i2,k(i2),i2+1,k(i2)); %k(i2),i2,k(i2),i2+1);
            k(i2)=k(i2)+1;
            if mod(j1,10)==0
                fprintf(fid,'\n + ');
            end
        end
    end
end

```

```

end

fprintf(fid,'\n + 0 ');

for j=1:num_int_ref(i1,1)

    fprintf(fid,'%e ',1/r_seg);

    if mod(j,5)==0

        fprintf(fid,'\n + ');
    end
end
end
end

% Self Inductance for each references in y direction

fprintf(fid,'\n\n* Self Inductances for references in y direction\n');
for i1=1:num_ref
    for i2=1:num_fil_int
        n=(i1-1)*num_fil_int+i2;
        fprintf(fid,'Lry%d_%d T0y%d_%d 0 %e \n',i1,i2,i1,i2,L_self_ref);
    end
end

% Self Inductance for each references in x direction

fprintf(fid,'\n\n* Self Inductances for references in x direction\n');
for i1=1:num_ref
    for i2=1:num_fil_int
        n=(i1-1)*num_fil_int+i2;
        fprintf(fid,'Lrx%d_%d T0x%d_%d 0 %e \n',i2,i1,i2,i1,L_self_ref);
    end
end

% Resistances in y direction
fprintf(fid,'\n\n* Resistances in y direction');
for i=1:num_int
    for j=1:num_fil_int

        n=j+num_fil_int*(i-1);

```

```

        fprintf(fid, '\n ry%d_%d V2y%d_%d VOL%d_%d  %e \n', i, j, i, j+1, r_seg);

    end
end

% Resistances in x direction
fprintf(fid, '\n\n* Resistances in x direction');
for i=1:num_int
    for j=1:num_fil_int

        n=j+num_fil_int*(i-1);

        fprintf(fid, '\n rx%d_%d V2x%d_%d VOL%d_%d  %e \n', j, i, j, i+1, i, r_seg);

    end
end

fclose(fid);

```

7. This function adds the parasitic capacitances to the SPICE file for the relative inductance matrix.

```

function [ output_args ] = Ins_cap_RL(Deco_cap,num_fil_int,num_int,num_ref)
% Add capacitance to the L spice file
% Detailed explanation goes here

%fid = fopen('test_RL.sp','a');

file_name=strcat('hs_',int2str(num_int-1),'_',int2str(num_fil_int),'_',int2str(num_ref),'_RL.sp');
fid = fopen(file_name,'a');

fprintf(fid, '\n\n\n* Line to Line Capacitances and Non-deal return path Added\n\n');

for i=1:num_int
    for j=1:num_int

        fprintf(fid, ' Cde%d_%d VOL%d_%d 0 %e \n', i, j, i, j, Deco_cap); %Line to Line
    end
end

```

```
end  
end
```

```
fprintf(fid, '\n\n.end\n');
```

```
fclose(fid);
```

8. Functions “self_ind” and “mut_ind” used in Appendix B are not changed.

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