SILICON-GERMANIUM DEVICES AND CIRCUITS FOR HIGH TEMPERATURE APPLICATIONS

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by

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SILICON-GERMANIUM DEVICES AND CIRCUITS FOR HIGH TEMPERATURE APPLICATIONS

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SUMMARY

Using bandgap engineering, silicon-germanium (SiGe) BiCMOS technology effectively combines III-V transistor performance with the cost and integration advantages associated with CMOS manufacturing. The suitability of SiGe technology for cryogenic and radiation-intense environments is well known, yet SiGe has been generally overlooked for applications involving extreme high temperature operation. This work is an investigation into the potential capabilities of SiGe technology for operation at temperature up to 300°C, including the development of packaging and testing procedures to enable the necessary measurements. At the device level, SiGe heterojunction bipolar transistors (HBTs), field-effect transistors (FETs), and resistors are verified to maintain acceptable functionality across the temperature range, laying the foundation for high temperature circuit design. This work also includes the characterization of existing bandgap reference circuits, redesign for high temperature operation, validation, and further optimization recommendations. A closely related bandgap-based temperature sensor circuit is also characterized, representing another critical building-block for data acquisition and health monitoring systems. In addition, the performance of an operational amplifier circuit is presented, along with potential improvements. Finally, an existing output buffer circuit is tested under extreme high temperature conditions. To the author's knowledge this work represents the first demonstration of functional circuits from a SiGe technology platform in ambient temperatures up to 300°C; furthermore, the optimized bandgap reference presented in this work is believed to show the best performance recorded across a 500°C range in any bulk-silicon technology platform.

The research undertaken for this thesis has also contributed several publications to the scientific community: one conference paper presented at the 2009 International Conference and Exhibition on High Temperature Electronics Network (HiTEN), one conference paper in press for the 2010 International Conference on High Temperature Electronics (HiTEC), and one journal article under review by Solid-State Electronics.

CHAPTER I

INTRODUCTION

1.1 Motivation

Interest in high temperature electronics has increased steadily over the past decade as technology improvements have begun to open up new application opportunities. Of the emerging markets, the automotive industry represents one of the largest, especially with the recent move toward hybrid electric and fully electric vehicles. Under-the-hood electronics must withstand temperatures up to 200ºC, with even higher temperatures needed for brake systems, cylinder pressure sensors, or exhaust sensing [1]. Related to the push for electric vehicles, the need for more effective downhole well logging requires electronics able to function at temperatures up to 300ºC and beyond [2]. In addition, next generation commercial aircraft hope to reduce complexity and weight by moving electronics closer the systems they are controlling, and which often operate at elevated ambient temperatures [3]. Not to be overlooked, high temperature electronics are key requirements for potential NASA missions to Venus and Jupiter, where temperatures can exceed 400ºC [4]. NASA's proposed missions to the surface of Venus will likely use a dual-temperature zone or hybrid system of high temperature electronics (250ºC and 460ºC) with dramatically longer survival times [5]. In order to satisfy these emerging applications, we must carefully re-evaluate existing device, circuit, manufacturing, and packaging design options.

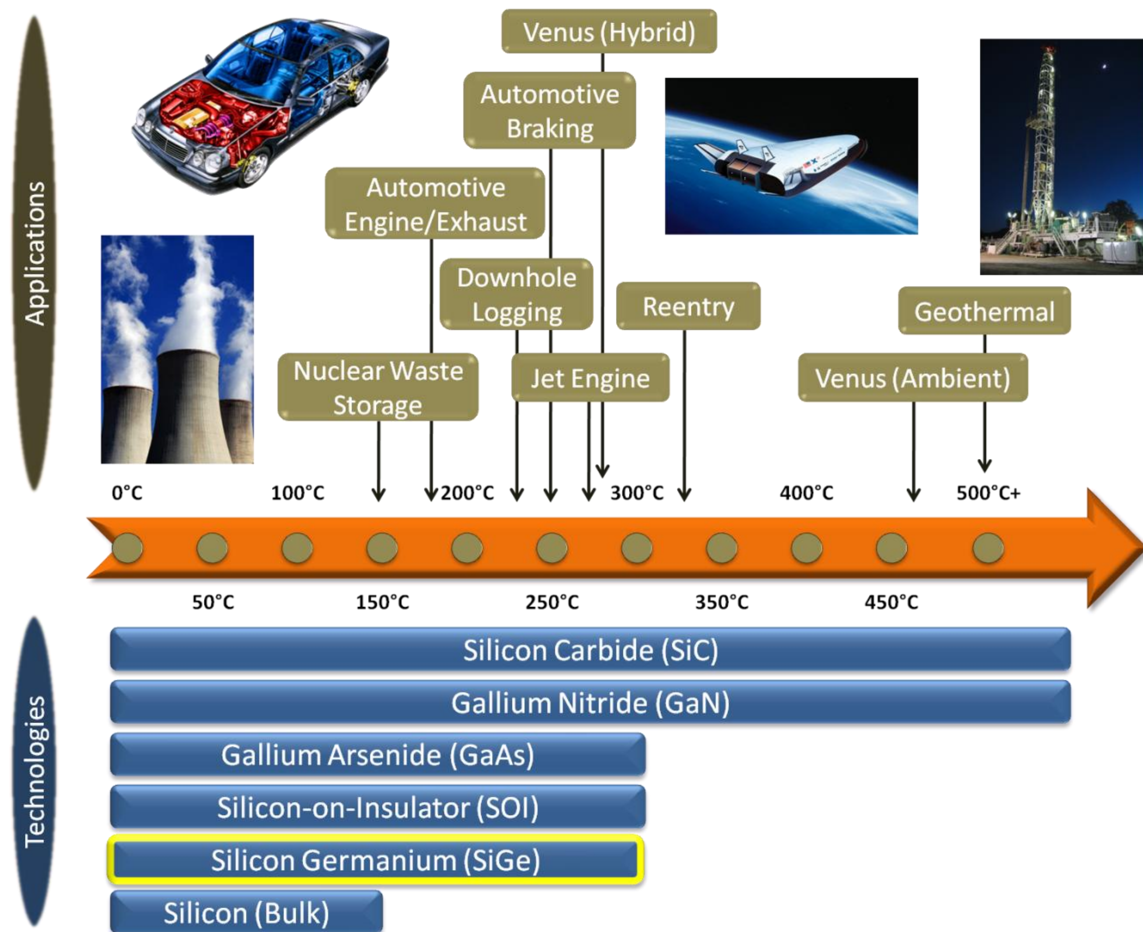

Figure 1: Overview of emerging applications for high temperature electronics compared to current temperature limits of various semiconductor technologies.

Due to the known limitations of conventional bulk silicon processes used for most commercial electronics needs, researchers have been forced to look for alternative semiconductor materials in order to satisfy the electronics needs of high temperature applications. Above 150ºC, leakage currents and reliability concerns in commercial bulk silicon platforms have prompted the move to silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) processes for applications up to 300ºC [6], [7]. The other traditional approach has been to use wide bandgap (WBG) semiconductors such as GaAs, SiC or GaN, which have been shown to be capable of operating at temperatures as high as

600ºC [8]-[10]. With its similarities to conventional Si CMOS, silicon-germanium (SiGe) BiCMOS technology has to date been largely dismissed in the quest for high temperature electronics. However, bulk-SiGe platforms could potentially offer a very cost-effective solution if creative device and circuit designs can overcome the inherent limitations. Figure 1 summarizes some of the major emerging applications requiring high temperature electronics and contrasts them with the capabilities of various semiconductor technology platforms.

The goal of this thesis is to establish SiGe as a viable semiconductor technology platform for high temperature applications up to 300°C, demonstrating through experimental results basic functionality, adequate performance levels to meet minimum specifications, and reliability of operation to survive in these extreme conditions for a reasonable amount of time before failure. Following a brief overview of SiGe BiCMOS technology, Chapter 2 discusses the packaging challenges encountered while attempting characterize SiGe devices and circuits up to 300°C along with the various solutions devised to create a robust, easy-to-use high temperature measurement system. Using that test system, the over-temperature performance of fundamental BiCMOS devices – SiGe HBTs, MOSFETs, and resistors – are characterized in Chapter 3. In Chapter 4, two closely-related, bandgap-based circuits (voltage reference and temperature sensor) are investigated for elevated temperature conditions, and a new high temperature compensation technique that stabilizes the voltage reference's output is presented. The high temperature performance of a charge-collection amplifier and output buffer are discussed in Chapter 5. Finally, Chapter 6 describes how the circuits under investigation

can be used to create data acquisition and monitoring systems and future work that remains to completely realize these goals.

1.2 SiGe BiCMOS Technology Overview

Through the use of bandgap engineering, SiGe heterojunction bipolar transistors (HBTs) are reaching performance levels on par with many III-V technologies such as GaAs or InP, and current state-of-the-art SiGe HBTs have demonstrated cutoff frequencies in excess of 350 GHz at room temperature [11]. However, the manufacturing process for SiGe HBTs – unlike their III-V counterparts – is compatible with commercial Si fabrication lines. The resulting BiCMOS technologies have allowed designers to match the superior device performance of SiGe HBTs with well-developed Si-based digital CMOS to create low-cost mixed-signal and RF solutions.

In addition to these benefits, SiGe is a prime candidate for operation in extreme environments including: cryogenic temperatures, extreme high temperatures, wide temperature ranges, and under radiation exposure [12], [13]. As would be expected, the performance of SiGe HBTs improves with decreasing temperature, and a large body of work has explored these capabilities [14]. SiGe HBTs are also inherently tolerant to total ionizing dose (TID) radiation, although they remain vulnerable to single event effects (SEE). Conventional wisdom would suggest that SiGe HBTs should experience a decline in performance as temperatures increase because of their natural improvements with cooling. For this reason, SiGe has largely been ignored as an option for high temperature operation. The versatility of SiGe makes it an especially attractive candidate for extraterrestrial conditions.

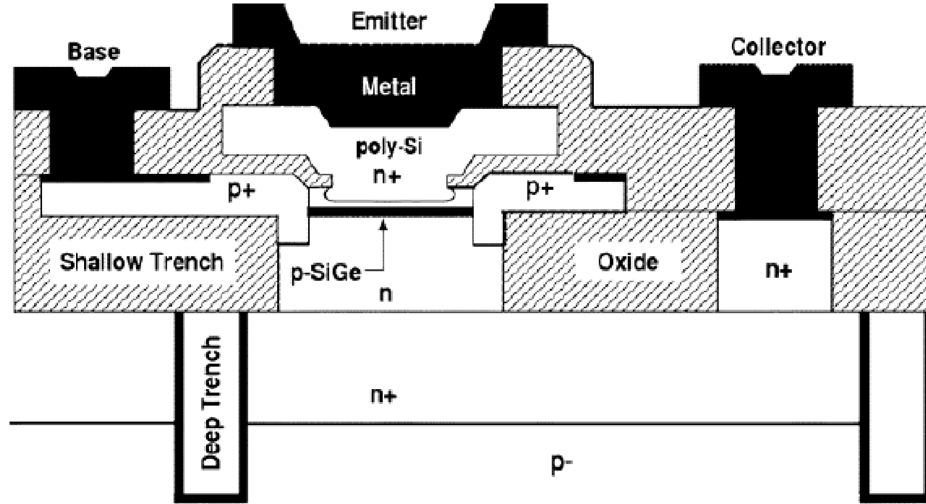

Figure 2: Cross-section of 1st generation SiGe HBT.

The SiGe platform used in this study is a 1st generation, commercial SiGe BiCMOS technology by IBM which combines 0.50 μm, 3.5 V BV_{CEO}, 50 GHz f_T SiGe HBTs with 0.35 μm, 3.3 V Si CMOS devices. Figure 2 shows the cross-section view of the SiGe HBT available in this platform. This SiGe technology platform includes both shallow and deep trench isolation, and a variety of resistors and capacitors. In addition, between four and seven metal layers are available along with a thick top aluminum metal. Neither the manufacturing process nor device design was optimized for high temperature operation. Currently, 3rd generation SiGe BiCMOS platforms with 200 GHz f_T / f_{max} SiGe HBTs are the industry standard for high frequency applications, and future research into the high temperature capabilities of these platforms will be of great interest to the electronics community.

Utilizing a graded Ge profile in the base similar to that shown in Figure 3, the specific performance benefits derived from the strained SiGe layer is worth a brief discussion. First, the smaller base bandgap leads to a greater current gain due to higher electron injection. Perhaps of more importance, the graded conduction band offset induces a drift

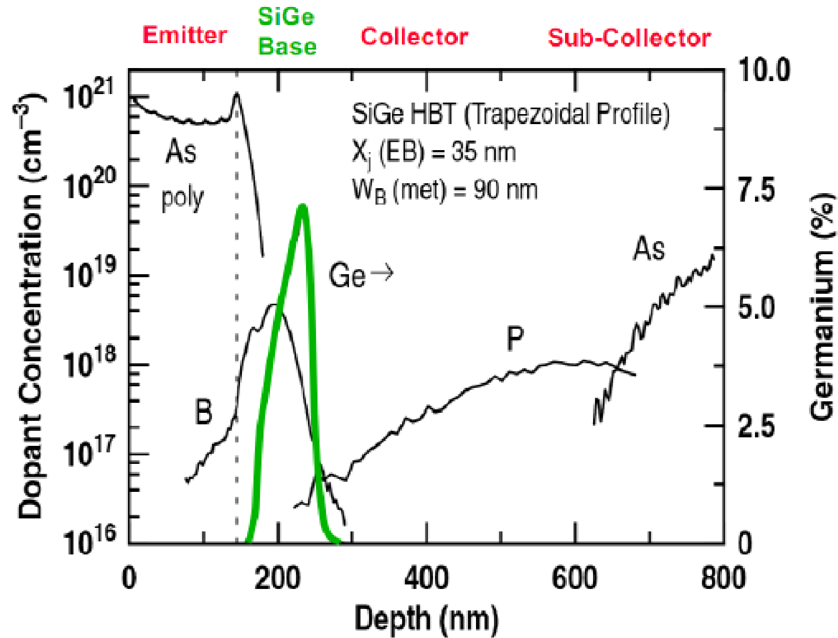

Figure 3: Doping profile representative of a 1st generation SiGe HBT with graded Ge base.

field in the base which serves to decrease minority carrier base transit time, thereby increasing f_T. In addition, the base Ge grading gives rise to an improved Early voltage. Finally, the engineered energy band for a typical SiGe HBT, shown in Figure 4, also results in a decoupling of the base profile and previously described performance metrics [15].

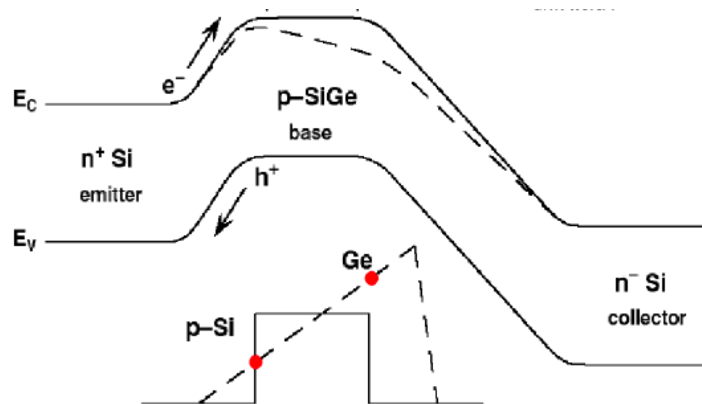

Figure 4: Energy band diagrams for a Si BJT and SiGe HBT, biased in forward active mode at low-injection [16].

CHAPTER II

HIGH TEMPERATURE TEST SYSTEM

2.1 Introduction

Assuming the design of high temperature capable devices, circuits, and associated manufacturing processes are available, producing commercially-viable electronics requires several other key steps including packaging, testing/verification, and qualification. FR-4, lead-tin solders, and other conventional packaging solutions used for commercial electronics begin to fail around 150ºC [17]. Special attention must be paid to the printed wiring board or substrate material, wire bonding method, interconnect metallization, ceramic package, adhesive, and wiring/cabling for reliable operation up to and beyond 200ºC [18]. Unfortunately, no standard method for reliable, high temperature packaging has been established, forcing researchers to design custom solutions based on the resources and capabilities at hand [19-20]. Without standardized packaging solutions, the design of test benches to validate and characterize designs also becomes a challenging task, and each company or research group must "re-invent the wheel" by developing their custom systems [21]. Commercial, let alone military-grade, qualification procedures require more fully developed packaging and testing capabilities and procedures.

The first decision to make when designing a high temperature system is whether to use a localized heating or a self-contained environmental chamber. Localized heaters selectively heat only the device-under-test (DUT), and several examples of such systems are probing stations with a high temperature chuck, vacuum chamber dewars with

electrical heater circuitry in thermal contact with the DUT, or calibrated, on-chip resistive heating circuitry in conjunction with thermal imaging equipment [22]. These solutions eliminate the need for special cables to contact the DUT, making them more suitable for AC measurements; however, thermal losses in the connection between the heating element and the device or circuit (not just the die or wafer) must be calibrated out in order to obtain an accurate measurement temperature. Because of the inherent difficulty in designing high temperature packaging that also has excellent, precisely-known thermal conductivity, the second approach – a self-contained test chamber – was chosen as the more easily implemented approach. In oven-based systems, the DUT is entirely contained within the chamber, which carefully controls the internal ambient temperature. This solution closely recreates "real-world" conditions, but it has the added complication of requiring a fixture and/or cables capable of withstanding the same extreme temperatures inside the chamber. For this reason, oven systems are not suitable for high frequency characterization.

Shown in Figure 5, the proposed high temperature test bench would include a high temperature chamber, a custom-designed fixture/packaging method, and a high temperature wire to transfer signals in and out of the oven. Once outside the oven, the wires would connect to a coax cable adapter, which could then be connected to a variety of standard measurement equipment. Finally, the oven and all measurement equipment would be remotely controlled by a laptop over a GPIB interface to allow for automated measurements.

A Delta Design 9023 environmental test chamber with 9016 temperature controller had been previously purchased for low temperature annealing and curing, and it proved to

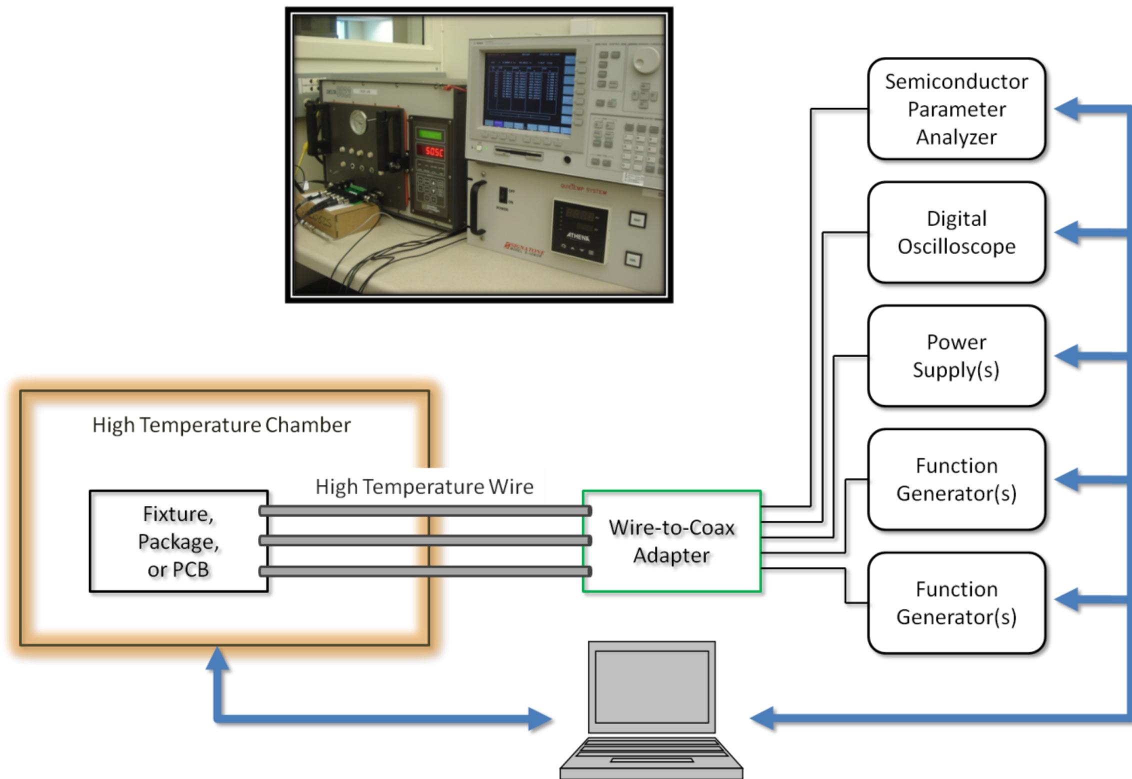

Figure 5: Diagram of proposed high temperature test station with inset image of completed system.

be a suitable choice with a 640 in^3 chamber, ten feed-through ports for wires or cables, and most importantly, a 315°C maximum temperature capability [23]. Reaching 300°C was a critical design parameter because that range contains the majority of today's high temperature applications while also representing the upper limit of current SOI technology. A nickel-clad copper wire with fiberglass insulation was chosen as the cabling method for its low resistivity (< 1 Ω/ft) and maximum temperature rating (480°C), and a PCB with screw-style terminal blocks was designed to simplify the wire-to-coax interface [24]. The various fixture and packaging solutions within the test chamber will be discussed in the following sections.

2.2 Printed Circuit Board (PCB) Approach

Printed circuit boards (PCBs) are a pervasive element of modern electronics, and based on past experience designing PCBs, this approach was the first one attempted. However, the most widely-used material for PCB designs, FR-4, is not suitable for high temperature applications due to its low glass transition temperature (T_g) of 140°C. Above this temperature, FR-4 laminate will begin to deform and lose structural integrity, although short-term exposure to higher temperature will not cause catastrophic failure assuming the board is not under mechanical stress. The coefficient of thermal expansion (CTE) is also an important factor when choosing a PCB substrate for wide temperature range applications because of concerns over the reliability of solder joints, plated vias, and traces. Several substrate materials with higher T_g's, such as a high temperature FR4 variant (180°C) and polyimide (260°C), are widely available, but none are specified to 300°C [18].

The Rogers 4003C laminate is often chosen for high frequency applications due to its low loss tangent, but it also has the highest T_g of any commercially available PCB substrate material (T_g > 280°C) [25]. Furthermore, Rogers 4003C's T_g is only specified as "greater than 280°C," with substantial failure not occurring until a much higher temperature. Using this laminate, the PCB was designed to accept a variety of die sizes and I/O signals, carried over traces finished with electroless nickel immersion gold (ENIG) plating to avoid oxidation of the underlying copper. The dies were mounted directly onto exposed ENIG bases using a thermally-conductive silver epoxy putty and then gold ball wire bonded to nearby bond pads on the PCB. To improve reliability at the

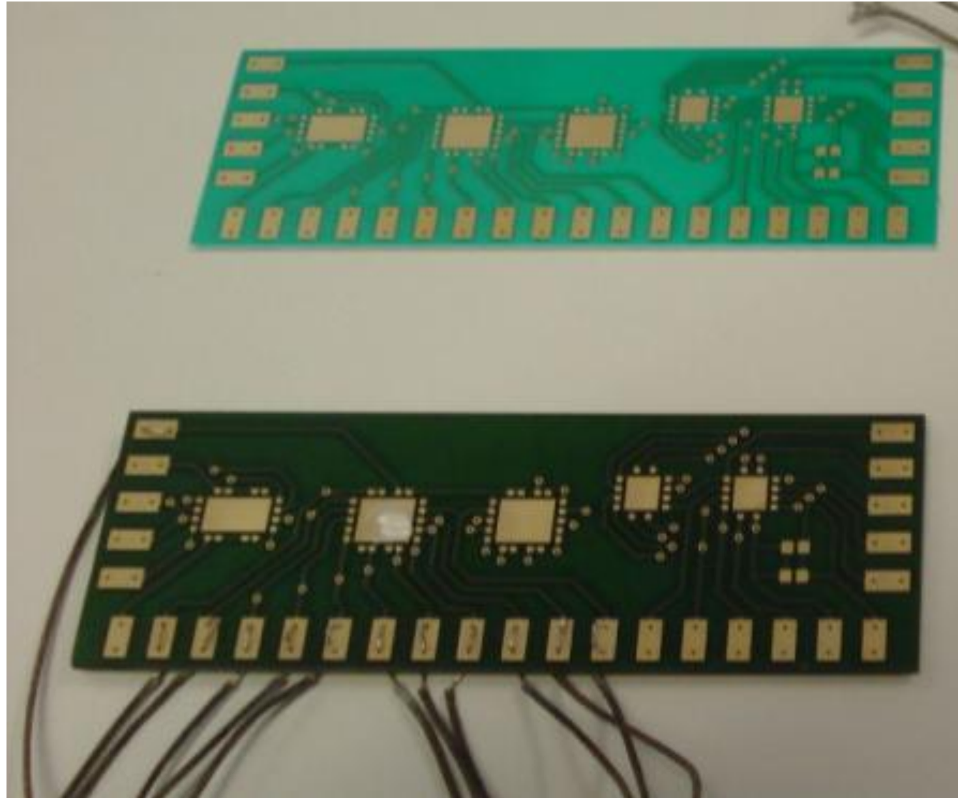

Figure 6: Unused high temperature PCB (top) and PCB after approximately 1 hour exposure to 300°C conditions (bottom).

bond wedge-pad interface, a thicker layer of electroless gold was selectively plated on the bond pads.

Because few solders are viable for 300ºC, a physical wire attach process was chosen for simplicity. For each signal, two exposed pads were placed on the top and bottom of the PCB, which were connected with two vias carefully-sized to just fit the 26 AWG high temperature wire. Each wire was inserted through one via, brought down through the other, and crimped to maintain the electrical connection. Figure 6 shows an example of the custom PCB with high temperature wire mechanically secured to multiple traces. As an alternative to the mechanical approach, two high temperature soldering techniques where attempted: traditional soldering using lead-tin-silver solder and resistance soldering with silver solder paste; however, neither approach formed acceptable electrical

or mechanical connections [26]. The high-lead solder did not reflow well at the ENIG trace/nickel-plated wire interface, while the smooth surfaces of the pads and wires were not conducive to the resistance soldering technique typically used to join twisted wires. Finally, brazing was ruled out due to the inherent danger of the process and the likely damage to the PCB itself.

Although the Rogers substrate proved suitable for short exposures to 300°C, extended periods in these ambient conditions exposed several limitations to this packaging method. Also shown in Figure 6, the solder mask layer on the PCB degraded at high temperatures, gradually darkening from green to black, and given enough time, the solder mask would completely break down and crack apart while taking on a white-gray color. The traces also separated from the substrate after extended exposure due to the CTE mismatch between the two materials. Lastly, the silver epoxy used for die attach became brittle and resulted in lifting of the die, which is shown in Figure 7. On the other hand, the gold wirebonds showed no sign of voiding, as they were able to hold the die to the board after the epoxy failure, and the physical wire-to-trace connection was deemed fully reliable.

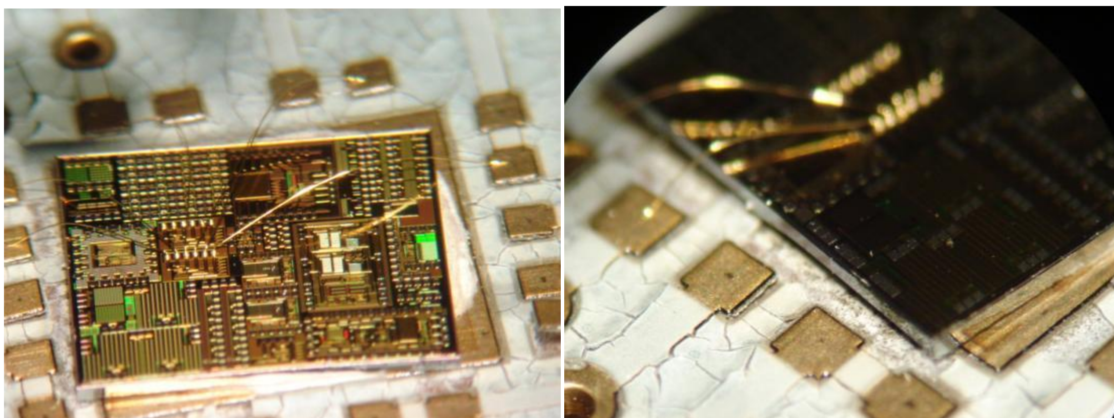

Figure 7: High temperature PCB packaging solution after 150 hour exposure to 300°C.

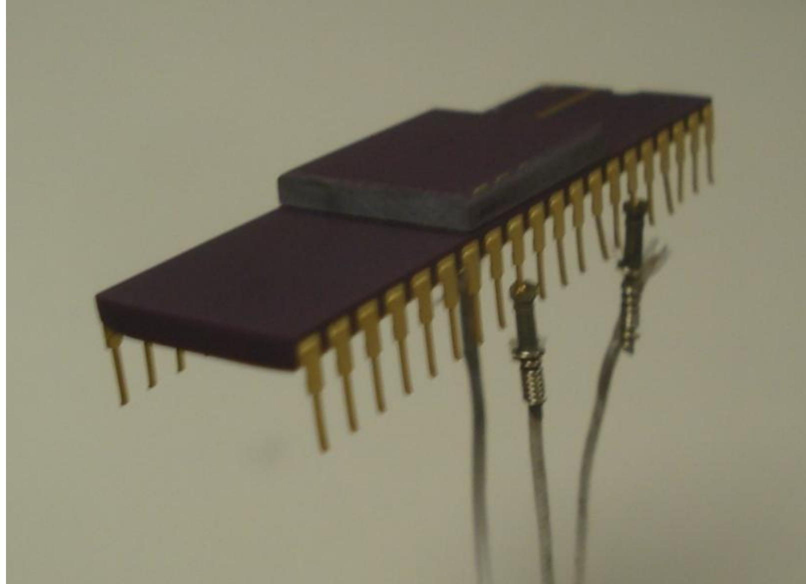

Figure 8: Ceramic DIP approach with high temperature wires attached to wire-wrap pins.

2.3 Dual-Inline Package Approach

Although the PCB packaging process was used for initial reliability testing, there was concern over the integrity of this approach for long term testing. For the second round of reliability testing of the SiGe voltage reference, a more robust packaging solution was developed in conjunction with Dr. R. Wayne Johnson (Auburn University) and Leora Peltz (Boeing Phantom Works). The die was secured to a 40-pin ceramic DIP with a gold-germanium ($Au_{88}Ge_{12}$) eutectic die attach, bonded with gold ball bonding, and sealed with an inverted 40-pin DIP lid using a gold-tin ($Au_{80}Sn_{20}$) alloy. Next, standard tin wire-wrap socket pins were carefully removed from their plastic housing, and the nickel-plated high temperature wire was wrapped onto each individual pin. Then the individual wire-wrapped sockets were slid onto alternating pins of the DIP as shown in Figure 8, allowing the package to hang freely in the test chamber. This approach worked remarkably well during long-term reliability tests; however, the wire-wrapped pins

needed to be reconstructed for each measurement. In the interest of reducing material waste and setup time for subsequent measurements, a permanent fixture was necessary.

2.4 Ceramic Fixture

Both the PCB and DIP packaging solutions allowed for 300°C measurements, but each had its own drawbacks. The PCB approach called for costly Rogers 4003 substrate and ENIG finishing for each board and was not suited for long-term measurements, while the individual wire-wrapped pins in the DIP approach were tedious and time-consuming to construct for each experiment. Furthermore, the $Au_{88}Ge_{12}/Au_{80}Sn_{20}$ eutectic die attach processes required outside assistance, adding additional cost to the DIP approach. Drawing upon the knowledge gained from these previous attempts at high temperature packaging, a permanent, reusable ceramic fixture was designed to allow quick and easy swapping of ceramic packages. Figure 9 shows the completed high temperature fixture with packaged SiGe circuit ready to be place inside the environmental chamber for testing.

Using an ultra-high temperature glass-mica ceramic called Macor, the fixture was designed to accept a 44-pin ceramic quad-flatpack, which was self-aligned by carefully-sized grooves for each lead on the package. Macor was chosen for its low CTE, high maximum continuous operating temperature (800°C), excellent electrical insulation, and relative ease of manufacturing [27]. Four bar clamps, one on each side, were then screwed down over the leads to secure the package in the fixture. Because of the previous success using mechanical force to maintain electrical continuity between the package/PCB and the high temperature wires, two small holes were drilled in each bar, and a high temperature wire was passed through one hole, along a groove acting as a

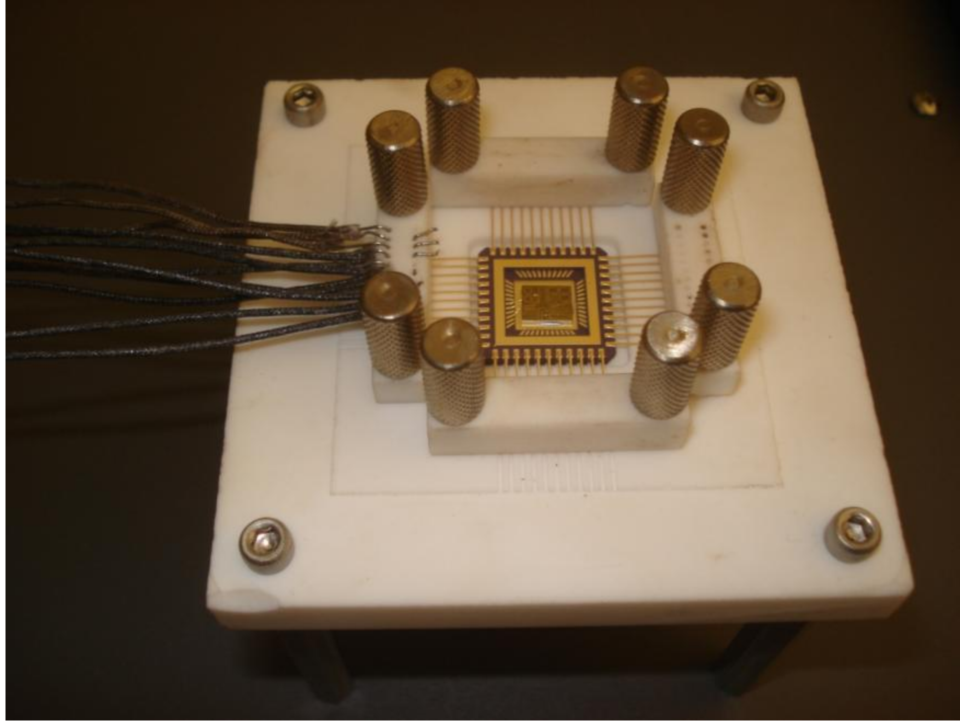

Figure 9: Reusable ceramic fixture with packaged SiGe circuit ready for high-temperature characterization.

guide, and back up through the second hole. Each bar clamp included eleven such wire slots to match the number of package leads, which allowed for a simple, reusable wire interface not present in past packaging approaches. Finally, stainless steel offsets were added to the fixture to align the platform height with the ports on the oven in order to keep the wire length to less than 6 inches, minimizing losses.

2.5 System Bandwidth Limitations

The high temperature test system was designed with DC and low-frequency measurement capabilities in mind, with AC characterization (above 1 GHz) to be performed on separate, custom-designed equipment. To determine the upper frequency limit of the high temperature system, the magnitude of the transfer function of the package or PCB with two bond pads wire bonded together was measured across temperature and is shown

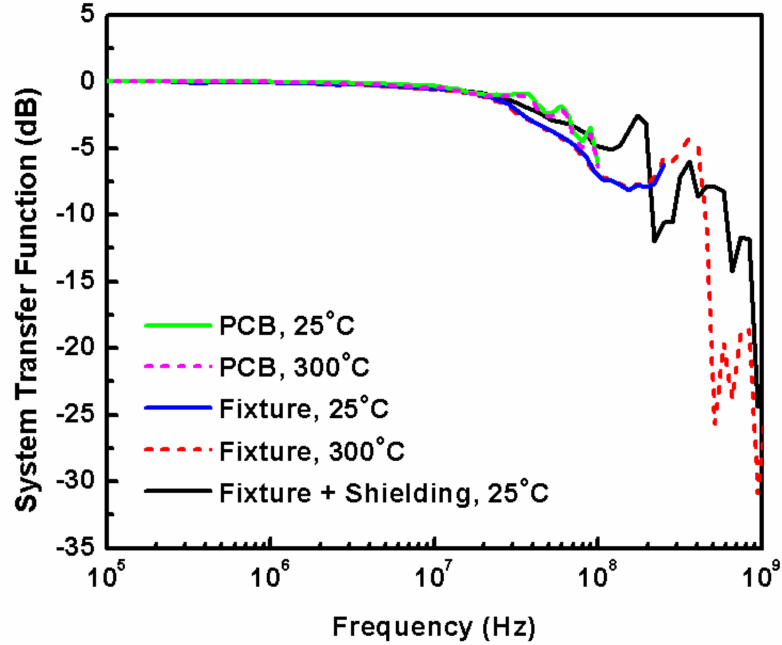

Figure 10. Bandwidth of high temperature test system across temperature for multiple packaging techniques.

in Figure 10. Overall system bandwidth was similar regardless of whether PCB or ceramic packages were used, limited to just over 10 MHz. The unshielded wires were suspected to be the primary limiting factor, and in an attempt to increase the maximum bandwidth, a second wire was hand-twisted around the signal wires to form a makeshift twisted-pair shielding. With the shielding wire grounded, the ceramic fixture showed a slight improvement, but the resulting transfer function was extremely sensitive to wire position and difficult to reproduce exactly. Perhaps the most important result was that ambient temperature had absolutely no effect on frequency response for either approach.

2.6 Summary

A high temperature test system was demonstrated for measuring devices and circuits in ambient temperatures up to 300°C. Three different packaging approaches were designed,

implemented, and analyzed for their suitability, and all were found capable of operating under the extreme conditions. Most importantly, this test system will provide future researchers and students with an easily accessible path for high temperature DC and low-frequency characterization for a wide variety of electronics. The lessons learned during the design of this system and packaging solutions will aid future work into creating an AC measurement system with high temperature capabilities.

CHAPTER III

DEVICE CHARACTERIZATION

3.1 Introduction

With a reliable means for characterizing electronics at high temperatures established, the first task was to determine the ability of basic devices from a SiGe BiCMOS platform to function up to 300°C. The available device models and Cadence simulation tools were not designed with such high temperatures in mind, which meant that the devices needed to be characterized experimentally. Assuming functional operation, the performance of the fundamental devices was of considerable interest, and any relevant limitations also needed to be exposed through experimental characterization. For example, significant substrate leakage currents were expected at high temperatures because the technology of interest was a bulk-Si based platforms.

As mentioned previously, the first generation SiGe technology under consideration in this work includes the SiGe HBT, n-type and p-type enhancement mode MOSFETs, a wide variety of resistors, and several other fundamental building blocks such as capacitors and diodes. All of these devices are used in different types of circuits, but the HBTs, MOSFETs, and resistors formed the basis for the low-level circuits which would be investigated later. In this chapter, the characterization of these three device classes is presented, verifying acceptable operation up to 300°C. The results presented here could also be used as the basis for more advanced software models optimized for high temperature simulation – a necessary future development for circuit design.

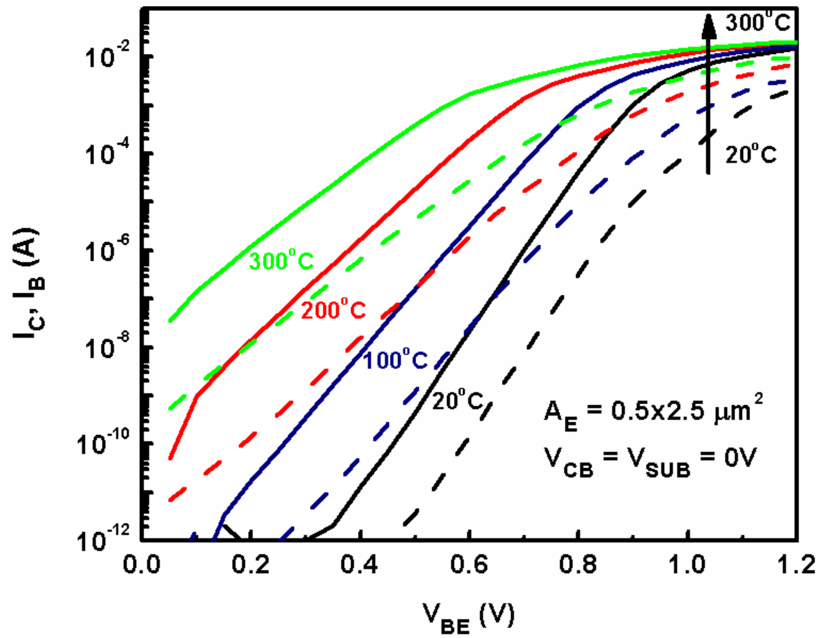

Figure 11: SiGe HBT Gummel characteristics as a function of temperature.

3.2 SiGe Heterojunction Bipolar Transistors (HBTs)

SiGe HBTs are the centerpiece for the BiCMOS technology of interest, and as such, demonstrating their functionality at high temperatures was the foremost question to address. Shown in Figure 11, the Gummel characteristics for a standard 0.5 μm by 2.5 μm SiGe HBT remained ideal from room temperature up to 300°C, and with functionality proven, the focus can shift to whether acceptable performance is being achieved [28]. The results indicate a usable bias range extending over two orders of magnitude. Figure 12 shows a typical family of output characteristics, which further reinforces the satisfactory performance up to 300°C. Although collector current decreased and the distinction between the saturation and forward active region was less defined, suggesting

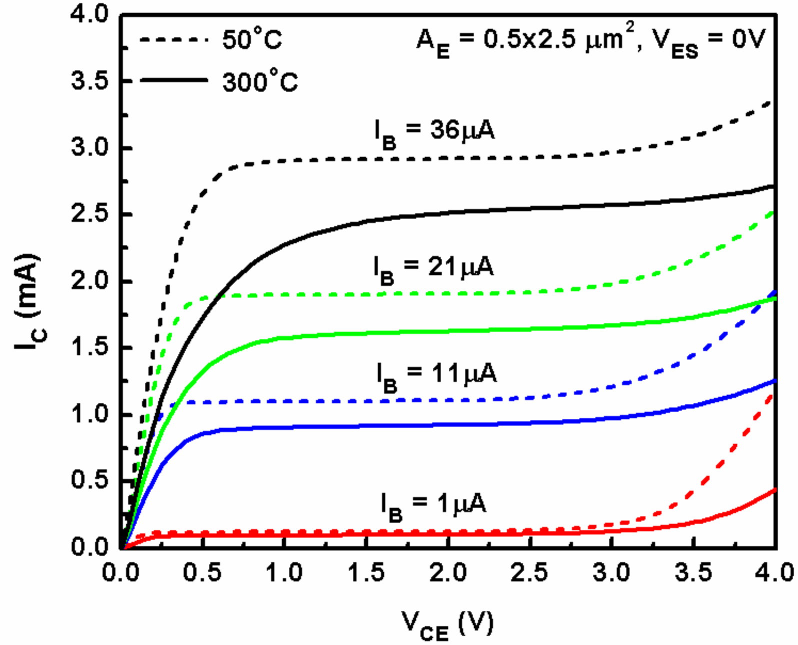

Figure 12: SiGe HBT output characteristic family across temperature.

decreased Early voltage, the forward active region extended to a higher V_{CE}, indicating a possible delay of avalanche breakdown.

Using the Gummel characteristics, the forward current gain – also known as beta (β) and defined as I_C/I_B – can be calculated. As shown in Figure 13, current gain decreased with increasing temperature as expected in a SiGe HBT which is the opposite behavior compared to a Si BJT. The inverse-temperature dependency of β in SiGe HBTs can in fact be a positive aspect because it serves to limit thermal runaway, which occurs when increasing temperature and current gain form a positive feedback loop that can result in non-ideal circuit operation at the very least and destruction of the device in a worst-case scenario. Higher values of β are desirable from a circuit designer's perspective, and the SiGe HBT's β remains near 100 even at 300°C – a very usable level. Existing work has

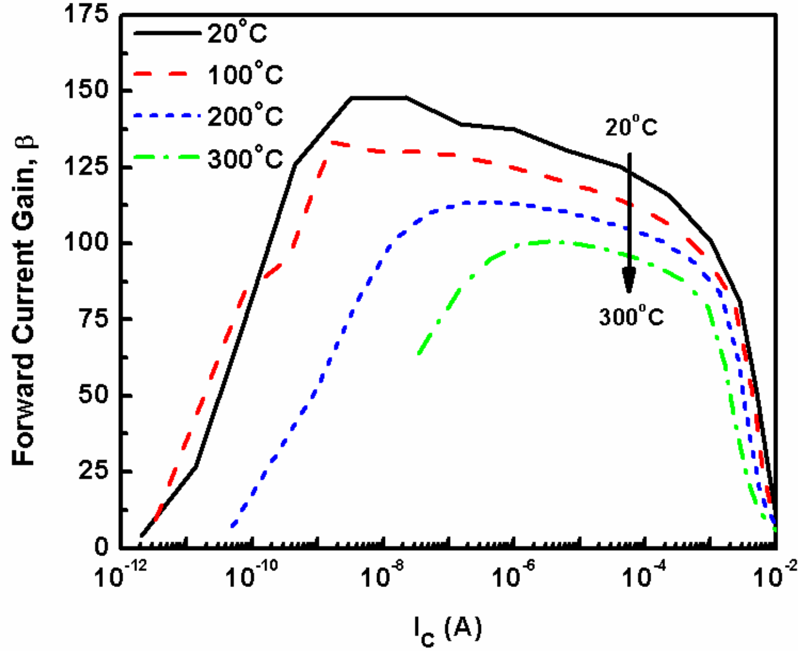

Figure 13: Forward current gain of SiGe HBT across temperature.

provided a more detailed look at the key specifications for SiGe HBTs such as gain, breakdown voltage, cutoff frequency, and low-frequency noise [29].

Although thermal runaway is a limiting factor at higher temperatures, the primary concern for bulk-Si based technologies is the dramatic rise in leakage currents above 200°C. At these temperatures, the intrinsic carrier concentration of the Si substrate approaches 10^{16}, which is on the order of the substrate doping level. The SiGe HBTs under consideration displayed substantially higher leakage currents equal to approximately 1 μA at 300°C. Should leakage currents become a limiting factor in circuit design, the traditional solution has been to utilize an SOI process with lateral transistors, and the availability of SiGe-on-insulator (SGOI) technology in recent years offers true HBTs with superior performance compared to lateral transistor structures at higher temperatures [30].

In addition to wide temperature range applications, radiation-intense environments comprise another area that is generating a substantial interest for SiGe electronics, and radiation-hardening-by-design (RHBD) techniques for improving tolerance to single event effects (SEEs) are being pursued at both the device and circuit level as cost-effective alternatives to process alterations. One promising device-level RHBD approach is the inclusion of an n-type implant surrounding the deep trench isolation of an HBT, which is known as an "external n-ring" [31]. The cross-section of a SiGe HBT with external n-ring is shown in Figure 14. With a positive bias applied to the n-ring, the charge deposited during heavy ion strikes is collected by the n-ring rather than the collector, and this action helps mitigate any changes in HBT biasing due to ion strikes. In high temperature environments, the n-ring's presence was expected to alter the electric field near the collector-substrate junction, thereby reducing collector-substrate leakage currents in bulk-SiGe HBTs.

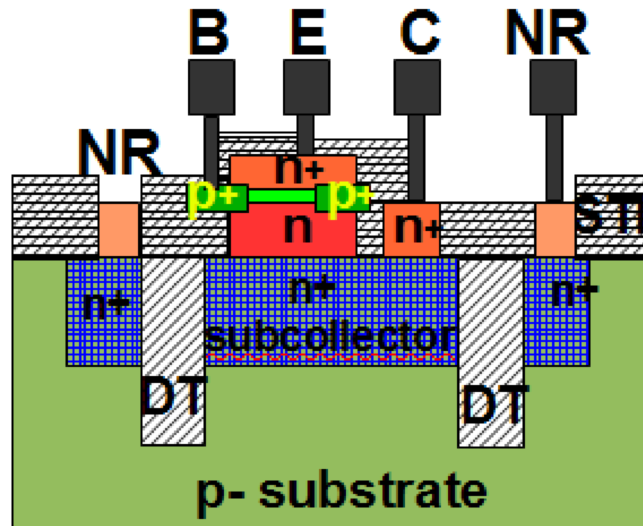

Figure 14: Cross-section of RHBD SiGe HBT with external n-ring [31].

Examining this prediction, the current through the collector-substrate junction is governed by the Shockley diode equation,

$$I = I_0\left(e^{qV_A/kT} - 1\right) \tag{1}$$

where I_0 is the reverse saturation current, q is the electron charge, k is Boltzmann's constant, and T is temperature [32]. Because the collector-substrate junction is always reverse-biased, the exponential term goes to zero, and the leakage current is given by

$$I_0 = qA\left(\frac{D_n}{L_n}n_p + \frac{D_p}{L_p}p_n\right) \tag{2}$$

where A is the area of the collector-substrate junction, D is the minority carrier diffusion coefficient, L is the minority carrier diffusion length, and n_p / p_n are the number of minority electrons and holes in the substrate and collector, respectively. Moving one step further, the number of minority carrier electrons in the substrate is given by

$$n_p = \frac{N_D - N_A}{2} + \left[\left(\frac{N_D - N_A}{2}\right)^2 + n_i^2\right]^{1/2} \tag{3}$$

where n_i is the intrinsic carrier concentration of silicon and N_A and N_D are the acceptor and donor doping concentrations in the substrate, respectively. As temperature increases, n_i increases, approaching N_A and causing the number of free electrons to increase dramatically. The external n-ring should counteract the increasing n_p by acting as a

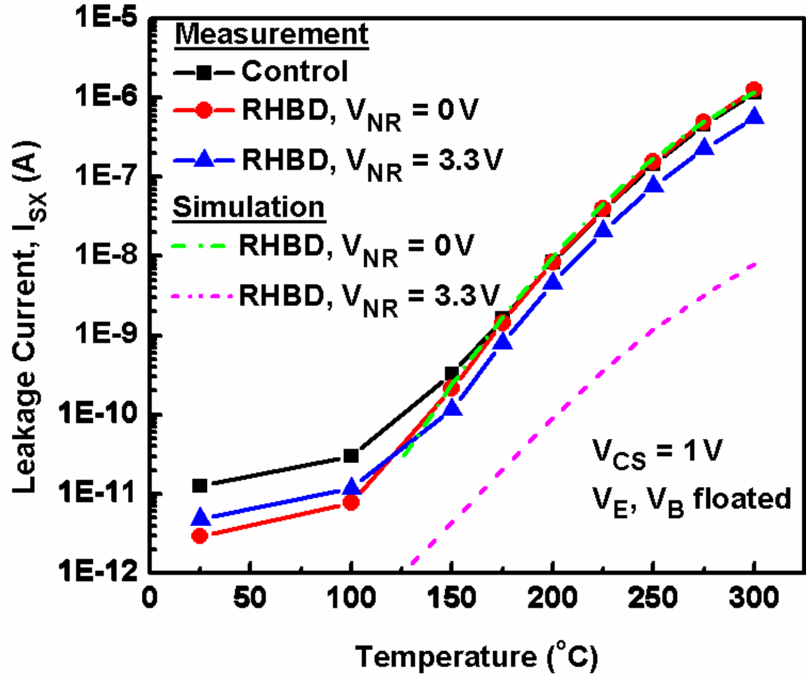

Figure 15: Substrate leakage currents for a SiGe HBT collector-substrate junction across temperature, both with and without RHBD "external n-ring" structure.

vacuum and pulling excess free electrons in the vicinity away from the collector, which in turn should suppress leakage currents at higher temperatures.

Shown in Figure 15, measurements confirmed that leakage currents were reduced by a factor of two in ambient conditions above 175°C. Also in Figure 15, the SiGe HBT with external n-ring was modeled in Sentaurus TCAD, and the same general behavior was observed – a drop in leakage current with a bias applied to the n-ring. However, simulations showed a decrease in leakage current by two orders of magnitude, considerably higher than observed in measurement. Despite the discrepancy, this RHBD technique could allow bulk-Si platforms to function in higher temperature environments than previously thought.

3.3 MOSFETs

In addition to the SiGe HBT, the other major building block in a BiCMOS platform is the MOSFET, and as the name suggests, both enhancement-mode nFETs and pFETs are available in the 1st generation platform under investigation. With the SiGe HBTs proven to be usable up to 300°C, the next step was to investigate the performance of the FETs because it would be nearly impossible to design relevant circuits without them. Fortunately, the output characteristics for both FETs (nFET and pFET) demonstrated acceptable performance up to 300C. As shown in Figure 16a, the drain current of the nFET decreases with increasing temperature at higher gate biases. The drain current, I_D, in the saturation region is given by

$$I_D = \frac{K'}{2}\frac{W}{L}(1 + \lambda V_{DS})(V_{GS} - V_{TH}) \tag{4}$$

where K' is a transconductance parameter, W is channel width, L is channel length, λ is the channel length modulation factor, and V_{TH} is the threshold voltage of the transistor. As temperature increases, so does K', which is proportional to electron mobility, driving the decrease in I_D even though V_{TH} is expected to decrease. The slope of the curves in the saturation region remains roughly the same over temperature, indicating λ is insensitive to temperature – a welcome benefit. Similar observations can be made from observing the nFET behavior in the triode region of operation.

Figure 16b shows the output characteristics for a typical pFET whose performance is similar to the nFET at 300°C. The channel width of the pFET was decreased by a factor of two in order to compensate for the lower mobility of holes and thereby provided a

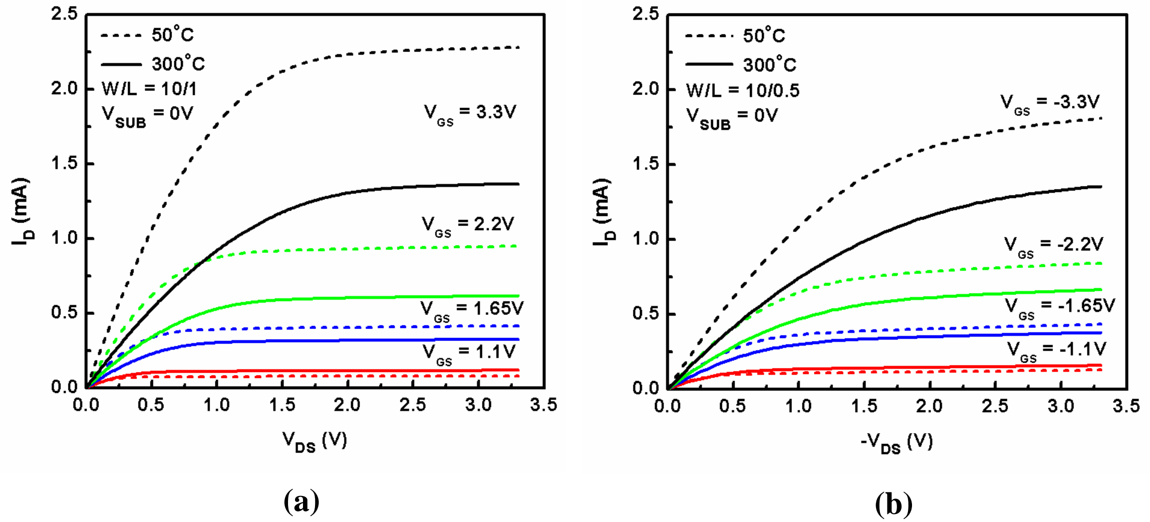

Figure 16: Comparison of output characteristics for an (a) nFET and (b) pFET at 50°C and 300ºC.

closer match in I_D between the two devices. Of particular note, the pFET's shorter channel length has a dramatic effect on λ, which could be a concern in some applications. Lastly, although both FETs exhibited a lower drain current at 300°C compared to room temperature for higher gate voltages, the opposite behavior was observed for V_{GS} below 1.5 V.

Just as important as the output characteristics, the subthreshold characteristics provide a more complete understanding of FET performance across temperature. Figure 17 shows these results for the nFET and pFET, and several relevant observations should be made. First, increasing temperature has a significant effect on the "off" state leakage current, which exceeds 0.1 μA at 300°C – a potentially serious issue if power consumption is a major concern. This effect is slightly more pronounced in the pFET, primarily due to the shorter channel width. A second takeaway is the presence of a zero-temperature coefficient (ZTC) bias point in both devices [33]. Depending on V_{DS}, the

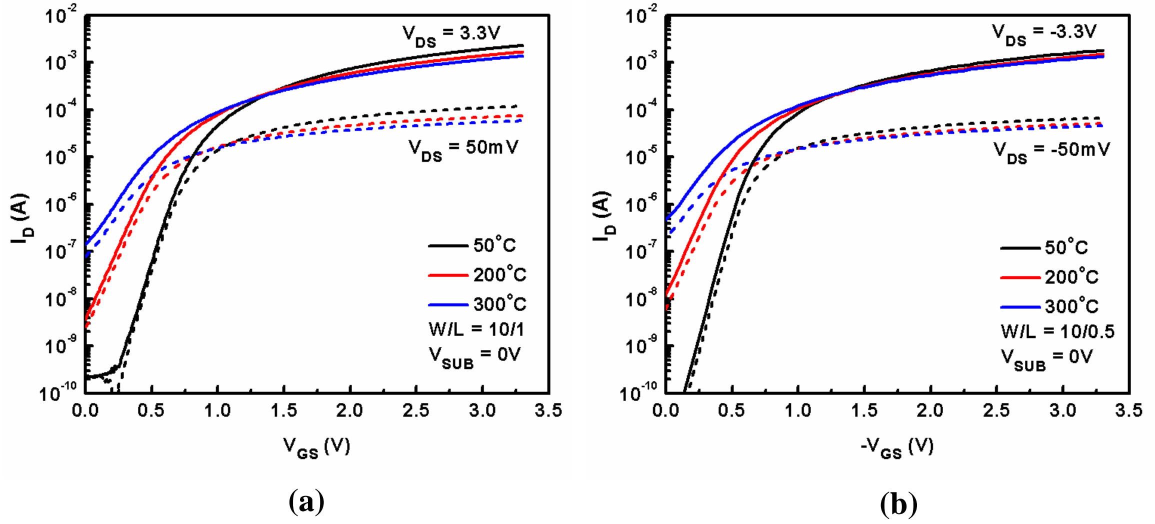

Figure 17: Subthreshold characteristics for an (a) nFET and (b) pFET over temperature.

ZTC point is between 1 V and 1.5 V for these FETs; additionally, the ZTC point explains why I_D increased with temperature for V_{GS} less than the ZTC point.

Another well-known characteristic of FETs is that V_{TH} is inversely proportional to temperature. As expected, the threshold voltage decreased according to the relationship

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{V_{SB} + \phi_F} - \sqrt{2\phi_F}\right) \tag{5}$$

where V_{TO} is the threshold voltage for zero substrate (body) bias, γ is the body effect parameter, V_{SB} is the source-body voltage, and ϕ_F is the surface potential at the gate oxide interface. V_{TO} encapsulates a number of underlying physical parameters; therefore, it is most easily determined experimentally from the subthreshold curves. Shown in Figure 18 are the threshold voltages, including V_{TO}, of the standard-size nFET for various substrate bias conditions across temperature. The net effect is an approximately linear relationship between V_{TH} and temperature, and although V_{TO} is the dominant factor, ϕ_F

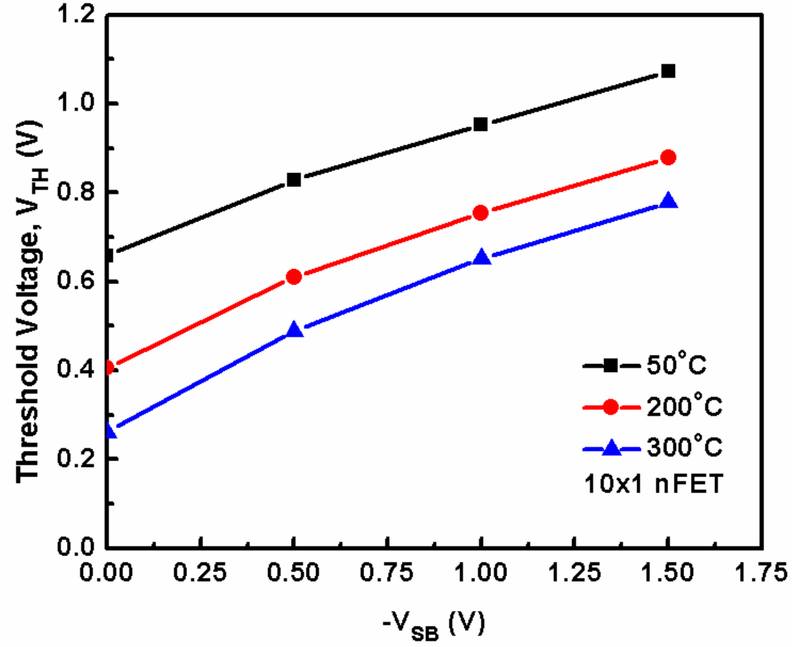

Figure 18: Threshold voltages for a 10x1 nFET with different substrate biases across temperature.

also increases linearly with temperature while γ remains relatively constant except in the case where n_i is greater than N_A in the substrate.

Transistor sizing is a cornerstone of circuit design because in both the saturation and triode modes of operation the drain current is related to the channel length and width. The ratio of width to length (W/L) is a constant design parameter that influences I_D in saturation and triode operating regions, governed by

$$I_D = K'\frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right) \tag{6}$$

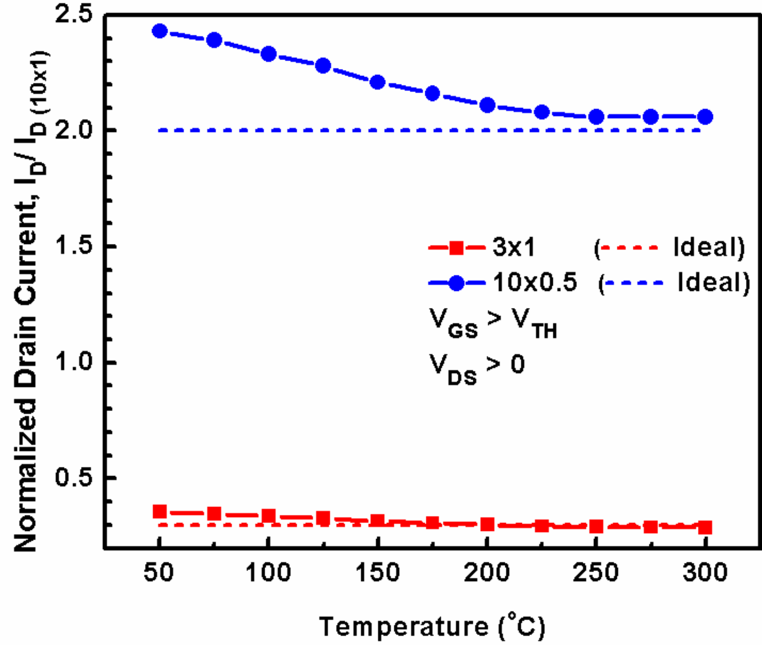

Figure 19: Ratio of the drain current of 3x1 and 10x0.5 nFETs versus drain current of a 10x1 nFET showing the linearity of transistor sizing across temperature.

W/L remains constant regardless of the operating temperature, but there was concern about whether short-channel or other effects could distort I_D at elevated temperatures. In order to verify that I_D remained ideal when W or L were reduced below the standard device size of 10x1, 3x1 and 10x0.5 nFETs were characterized up to 300°C. The average drain current for these two transistor sizes, normalized to the 10x1 drain current, is plotted against temperature in Figure 19. Using the output characteristics when the nFETs were in either triode or saturation operating mode ($V_{GS} > V_{TH}$ and $V_{DS} > 0$), the average value shows relatively good agreement with the ideal values, shown with dashed lines. Surprisingly, the best match was found at higher temperatures, which is unexpected considering the transistors measured were from the same wafer, albeit on different die. This result is partially explained in that I_D for both alternate-sized devices

deviated from the expected values considerably at lower values of V_{GS} for lower temperatures. As gate bias increased, so did agreement with expected values of I_D.

As was the case with the HBTs, substrate leakage currents are a concern for FETs as well. Fortunately, the magnitude of these currents was only on the order of 0.1 μA at 300°C, which should not pose a problem for most circuits using reasonably-sized transistors. Should even these values be too high, a similar structure to the external n-ring used for the RHBD SiGe HBTs could be added to the FETs to further suppress leakage current. Finally, the presence of a non-zero substrate bias had minimal effect on substrate leakage and in fact, actually suppressed leakage currents slightly. This result is particularly important for analog circuit designs that often require a non-zero V_{SB}, such as in current mirrors.

3.4 Resistors

Three classes of resistors were available in the SiGe BiCMOS platform under investigation: standard polysilicon, high sheet resistivity (ρ) polysilicon, and implant resistors. Furthermore, both types of polysilicon resistor could be constructed over either a subcollector ground plane (to reduce substrate coupling, [NS]) or deep trench oxide (lower parasitic capacitance, [DT]). As shown in Figure 20, all resistors maintained a linear relationship across the entire temperature range, and each class of resistor demonstrated a unique temperature dependency. The various implant resistors – n-type reach-through (RN), p-type silicon (RI), and subcollector – showed a strongly proportional dependence on temperature. Relatively temperature independent, the standard polysilicon resistors (PB) exhibited a weakly proportional behavior. Finally, the

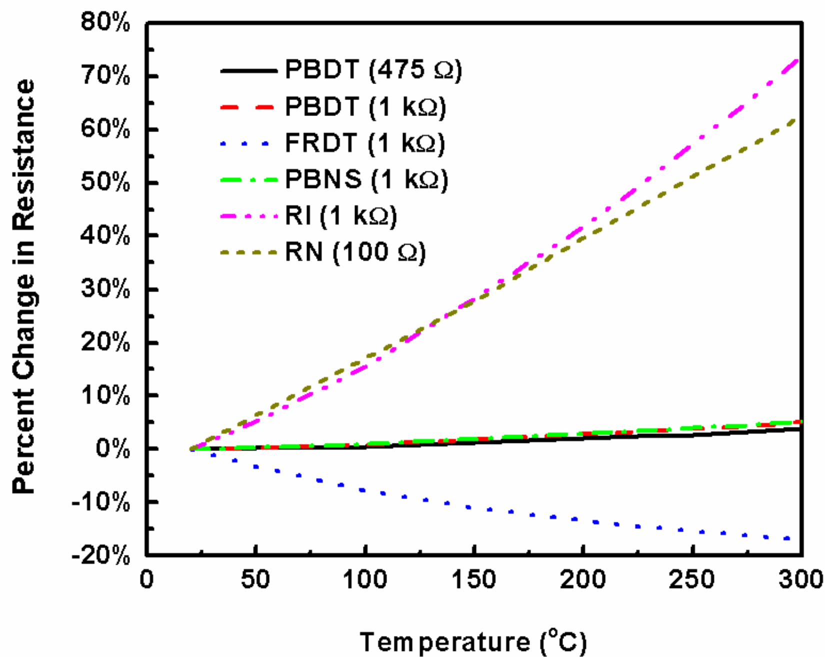

Figure 20: Temperature dependencies of the various resistors available in the SiGe platform under investigation.

third group consisting of high sheet ρ polysilicon resistors demonstrated the exact opposite behavior, an inverse relationship with temperature.

The PBDT (p+ poly over oxide) resistor is particularly important because it was utilized extensively in the bandgap reference and temperature sensor circuits described in the following sections. This resistor, with its relative temperature-independence, experienced only a 5% increase in resistance between room temperature and 300°C regardless of geometry.

CHAPTER IV

BANDGAP BASED CIRCUITS

4.1 Introduction

Precision voltage references are a key primitive building block for analog and mixed-signal circuit designs, and a temperature independent voltage source is a prerequisite for more complex systems. A number of high temperature voltage reference circuits have been demonstrated over the past several years. Using SOI or SiC processes, these circuits offer temperature limits ranging from 225ºC to 350ºC and beyond; however, both SOI and SiC are considerably more expensive compared to commercial bulk-Si [34]-[40]. Because the AC performance of a voltage reference is not of concern, the bandgap reference (BGR) circuit was an ideal step in the progression from simple devices to a complete circuit considering the previously discussed limitations of the high temperature measurement system. Additionally, the over-temperature behavior is perhaps the most important characteristic of a voltage reference, adding further incentive. Once the high temperature performance was understood, new compensation techniques could be devised to allow cost-effective SiGe BGRs to compete with those in SOI platforms.

The same principles used to design a BGR can be used to create a simple temperature sensor circuit based on the bandgap of SiGe HBTs. Compared to the stable output of a BGR, the temperature sensor circuit seeks to produce a linear output that is proportional to absolute temperature, and the same factors impacting the performance of the BGR should be present in the temperature sensor. In turn, similar high temperature compensation techniques could likely be applied to design SiGe temperature sensors that

will remain linear up to 300°C. Both of these circuits are critical components of data acquisition and health monitoring systems, a key area of interest for high temperature electronics.

4.2 Voltage Reference Circuit Topologies

The bandgap reference (BGR) circuit was introduced in the early 1970s as a temperature-stable voltage reference well-suited for voltage regulators, A/D and D/A converters, and other precision analog circuits such as measurement systems [41]. The most basic version of a BGR circuit combines the negative temperature coefficient of the base-emitter voltage (V_{BE}) of a bipolar transistor with a proportional-to-absolute temperature (PTAT) current source to produce an output voltage that is constant over temperature. In a silicon BJT, V_{BE} is given by

$$V_{BE} = V_G(T) + \frac{T}{T_r}[V_{BE}(T_r) - V_G(T_r)] - \eta\left(\frac{kT}{q}\right) ln\left(\frac{T}{T_r}\right) + \frac{kT}{q} ln\left(\frac{I_C(T)}{I_C(T_r)}\right) \tag{7}$$

where V_G is the bandgap voltage of silicon, T_r is the reference temperature, and η is the temperature dependency parameter of silicon [42]. For the SiGe HBTs used in this work, the effects of the Ge grading on the bandgap, and hence V_{BE}, are discussed in greater detail in [43]; however, the same approximately linear negative temperature dependency is present.

In order to generate the PTAT current, the differential voltage between the base-emitter voltages of two HBTs with different collector current densities can be used. This voltage, ΔV_{BE}, is given by

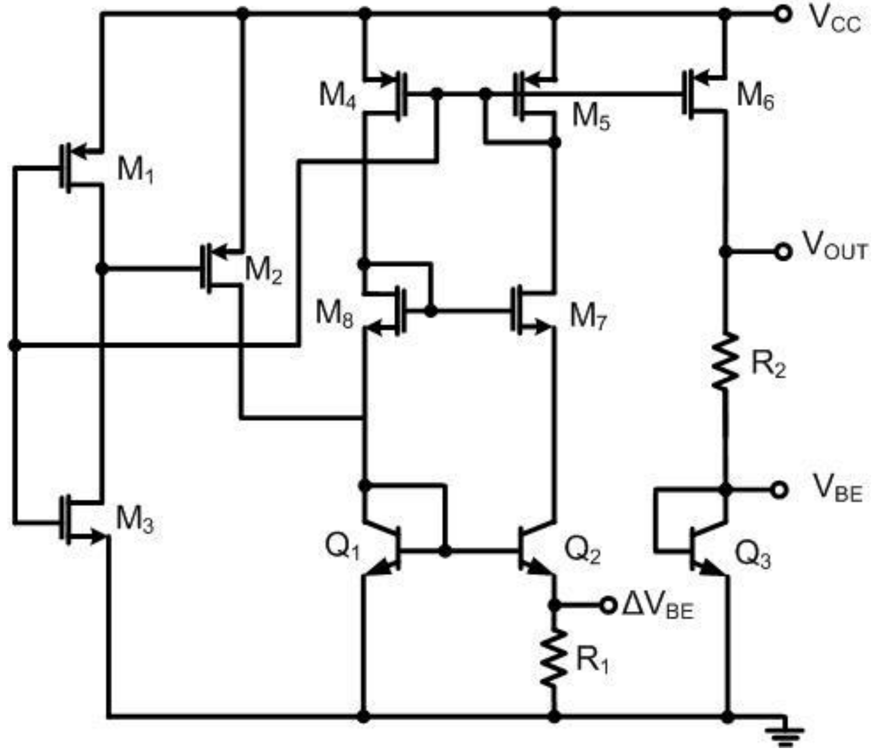

Figure 21: Schematic of the first-order (control) SiGe BGR circuit.

$$\Delta V_{BE} = \frac{kT}{q} ln\left(\frac{J_1}{J_2}\right) \tag{8}$$

where J_1 and J_2 are the current densities of the HBTs. Assuming the collector current is held identical in the both transistors, the ratio of current densities will be entirely determined by the ratio of the emitter areas. This differential voltage increases linearly with temperature, and when applied across a resistor of known value, the PTAT current can be controlled. Figure 21 shows a first-order BGR circuit implemented using these principles. Combining (6) and (7), the output voltage of the first-order BGR is given by

$$V_{OUT} = V_{BE} + \Delta V_{BE} \frac{R_2}{R_1} \tag{9}$$

Unfortunately, the first-order BGR fails to compensate for the non-linear terms in (6), which means the output will not be perfectly stable across temperature. A variety of techniques have been developed to cancel out the higher-order terms, but one particular approach has been shown to work very well in BiCMOS platforms. This technique, called exponential-curvature compensation, utilizes the exponential temperature dependency of the forward current gain of a bipolar transistor to reduce variation in output voltage across temperature [44]. With the addition of the exponential term, the output voltage is given by

$$V_{OUT} = V_{BE} + \Delta V_{BE} \frac{R_2}{R_1} + \frac{c R_2 T}{\beta(T)} \quad (10)$$

where $\beta(T)$ is the forward current gain (beta) at a given temperature and c is a circuit design parameter related to the pFET current mirror sizing ratio. The schematic for the BGR with exponential-compensation is shown in Figure 22.

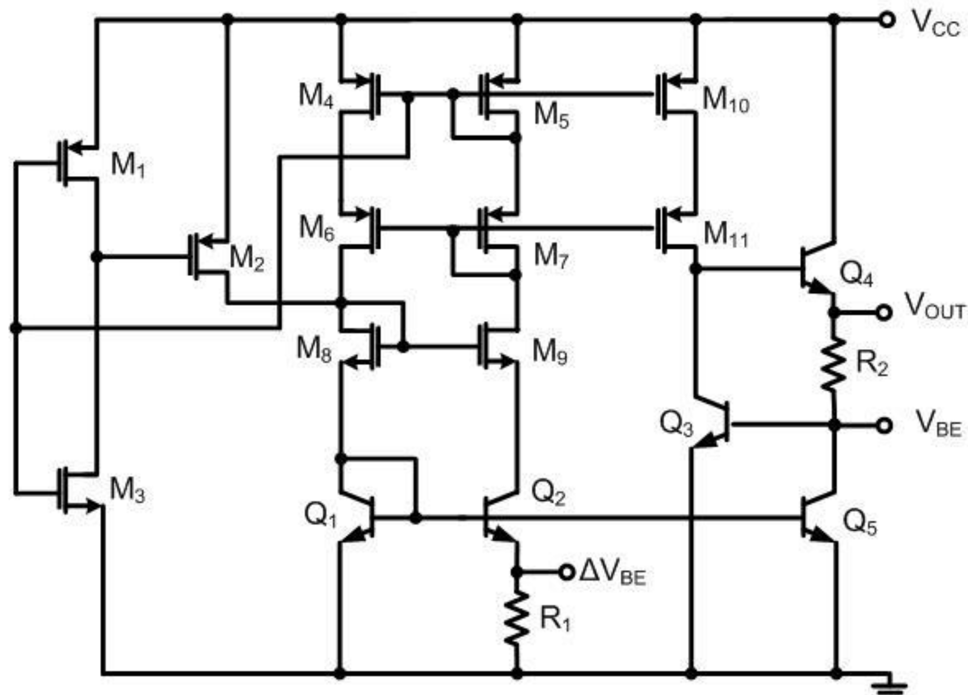

Figure 22: Schematic of BGR with exponential compensation.

4.3 Voltage Reference Characterization

In order to establish SiGe as a viable option for high temperature applications, the first-order BGR circuit – also referred to as the "control" BGR – was characterized from room temperature to 300ºC. Figure 23 shows the output voltage across temperature. Even though this circuit was in no way optimized for high temperature operation, the output voltage remained flat to 200ºC, with a ΔV_{OUT} of only 10 mV. Above 200ºC, the output voltage rose rapidly, but the BGR remained operational and stable to 300ºC.

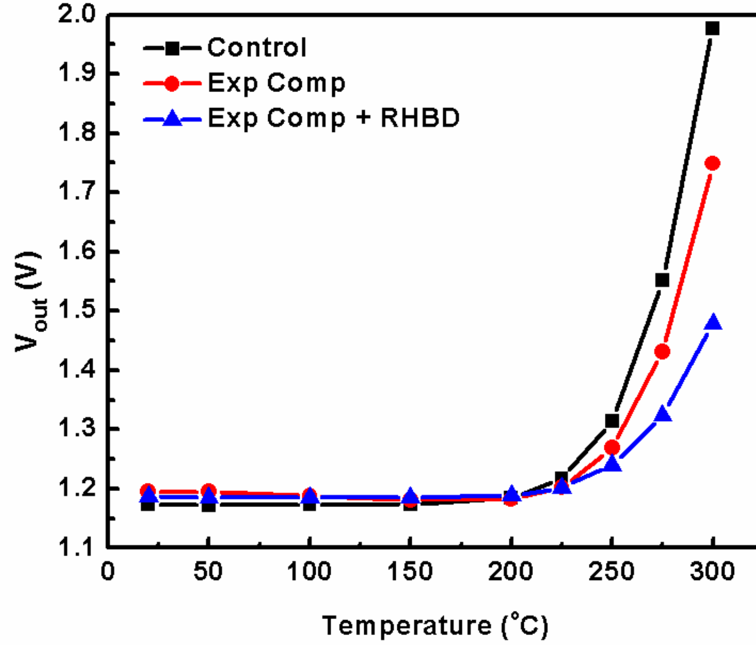

Figure 23: BGR output voltage versus temperature.

Even more promising were the results from two BGR circuits using the exponential-compensation architecture described earlier. With exponential-compensation, the SiGe BGR has been shown to achieve a 49.8 ppm/ºC temperature coefficient over a 200ºC range, from room temperature to -180ºC [45]. Furthermore, the same BGR architecture extends the useful operating temperature up to 225ºC ($\Delta V_{OUT} \approx$ 13 mV) and reduces V_{OUT} from 1.977 V to 1.749 V at 300ºC. A third BGR that combined exponential compensation with the transistor level RHBD external n-ring technique to suppress leakage current was also measured. This BGR demonstrated the best high temperature performance, with ΔV_{OUT} equal to only 2.2 mV at 200ºC and a further reduction in V_{OUT} at 300ºC to 1.479 V. With the simple addition of RHBD n-ring structures, the BGR improves its high temperature performance considerably at a very minor penalty to layout area.

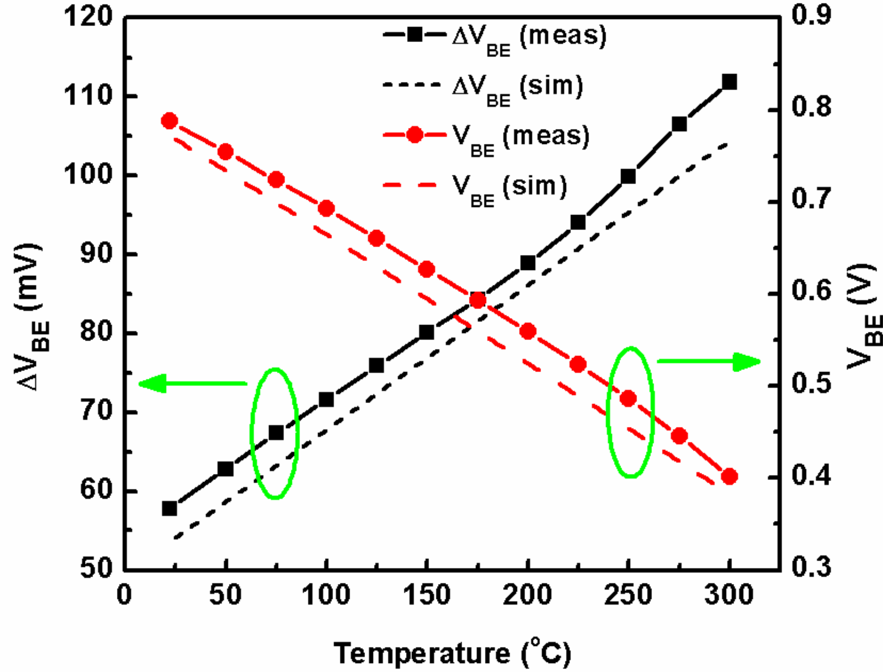

Figure 24: Comparison of simulated and measured BGR voltages over temperature.

The successful operation of a voltage reference in a bulk-SiGe platform to such high temperatures is very encouraging; however, the rapid rise in output voltage above 200ºC warrants further investigation. If the underlying mechanisms causing this behavior can be identified, then design techniques at the device and circuit level could be explored to extend the useful operating range of bulk-SiGe technology. As previously established, the PBDT resistors used for this circuit behave linearly across the entire temperature range, ruling them out as the cause of the output voltage rise. In Figure 24, the measured values for both V_{BE} and ΔV_{BE}, which represents the generated PTAT current, are linear across temperature, and they show good agreement with Cadence simulations. Unfortunately, those same simulations do not reproduce the behavior of V_{OUT} above 200°C, complicating matters considerably.

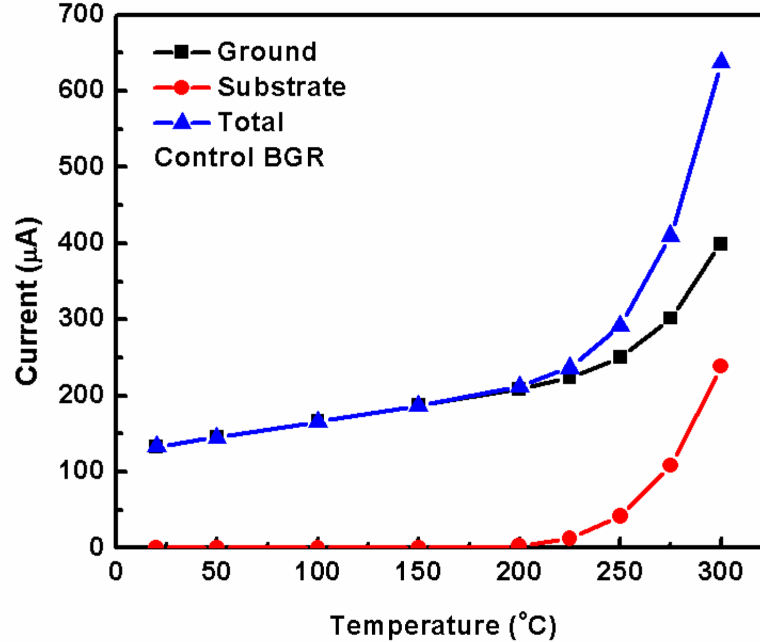

Figure 25: Currents flowing out of the control BGR circuit across temperature.

However, the circuit's current draw provides a clue about those underlying causes. Figure 25 shows the rapid rise in both substrate leakage and ground current occurring simultaneously with the V_{OUT} increase. These currents indicate the collector current in the output stage of the BGR (i.e., the current flowing through R_2) is no longer changing linearly with temperature, contributing to the increase in output voltage. Although the impact of substrate leakage was expected at high temperatures, the reason for the rise in current through the ground terminal was difficult to determine without simulation assistance. One hypothesis is a failure of the pFETs to accurately mirror the current from the PTAT generator to the output stage of the BGR, especially when combined with the uneven substrate leakages in Q_1 and Q_2 due to their 1:8 sizing ratio. A second, related possibility is that ΔV_{BE} does not accurately represent the PTAT current once substrate leakage in Q_2 becomes significant at temperatures above 200°C.

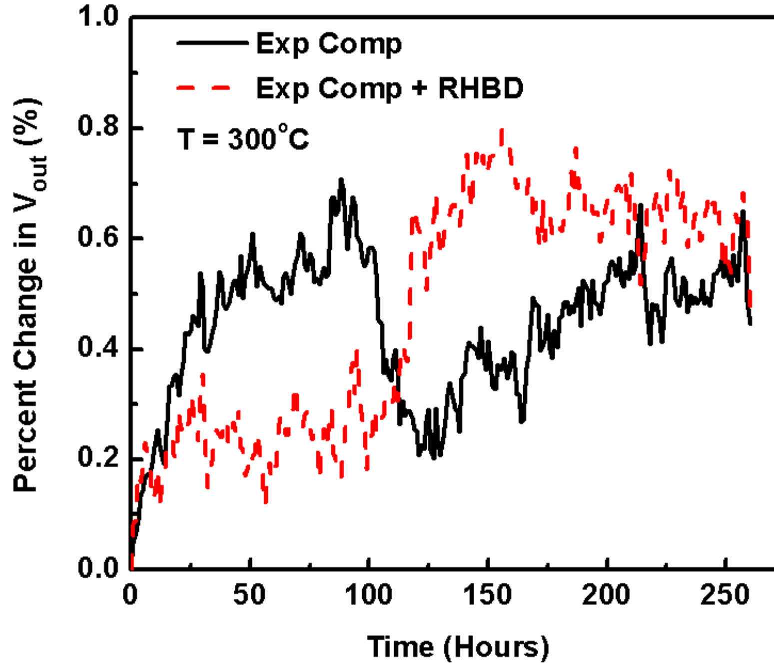

Figure 26: Reliability testing results for SiGe BGRs with exponential compensation.

High temperature applications require circuits that perform to acceptable specifications, but the effort is wasted if the circuits fail prematurely during use. With the BGRs' performance across temperature characterized, the reliability of the BGR with exponential compensation was investigated next. An initial run of approximately 150 hours at 300°C showed minimal to no degradation in V_{OUT}; however, there was concern over the suitability of the packaging technique – the PCB approach discussed previously – for long-term expose to such high temperatures. For the second reliability experiment, the ceramic DIP packaging technique was utilized to minimize the likelihood of packaging degradation or failure. After over 250 hours of continuous operation at 300ºC, the output of both BGRs had increased by only 0.6%, as shown in Figure 26. The circuits remained powered on for the duration of the test, with data samples collected every 30

seconds, which were then averaged into 1 hour data points for ease of viewing. Common failure mechanisms in high temperature environments, such as electromigration in interconnects or intermetallic voiding of the wirebonds, were not observed [17].

4.4 High Temperature Compensation Technique

With the functional operation of SiGe BGR circuits demonstrated in environments up to 300°C, the next step was to optimize these circuits to provide more acceptable performance at high temperatures. Based on the results of the previous measurements, the proposed approach to compensating for the rapid rise in V_{OUT} above 200°C is to shunt the non-linear current in the final stage of the circuit around R_2. Either a SiGe HBT or Si nFET can serve as the shunting device, with the base or gate terminal, respectively, connected to R_2 such that the transistor does not turn on until the temperature exceeds 200°C and changes in V_{OUT} occur. Three different shunting configurations were designed for characterization: full, split, and half-bypass.

As shown in Figure 27, the source of the shunting transistor was connected to V_{BE}, while the gate and drain provide control over the behavior of the circuit. In the full-bypass configuration, both the gate and drain were connected to V_{OUT}, shunting current around the entire resistor. By moving the gate connection to the mid-point of R_2 in the split-bypass configuration, the transistor would not become active until a higher temperature was reached, allowing for greater control over the compensation circuitry. The final configuration, half-bypass, had the nFET's drain tied to the gate at the resistor's midpoint, which further limited the compensation by only shunting current around a portion of R_2. A 0.5 μm x 2.5 μm SiGe HBT was also available to test the three configurations experimentally.

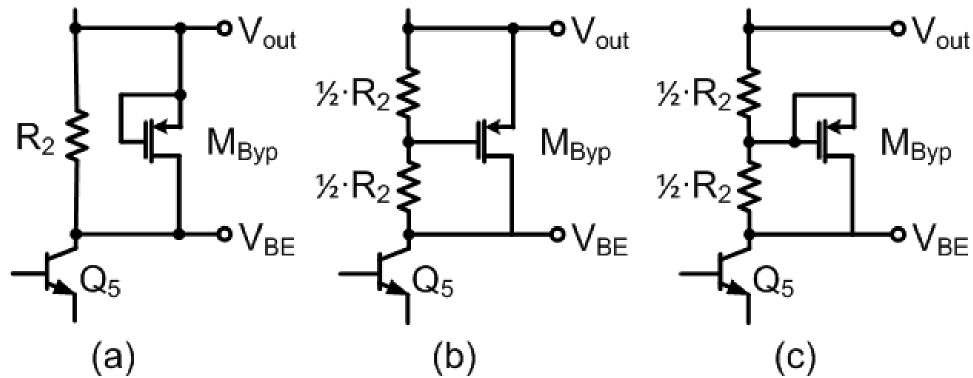

Figure 27: High temperature compensation network using a transistor connected in (a) full-bypass, (b) split-bypass, and (c) half-bypass configurations.

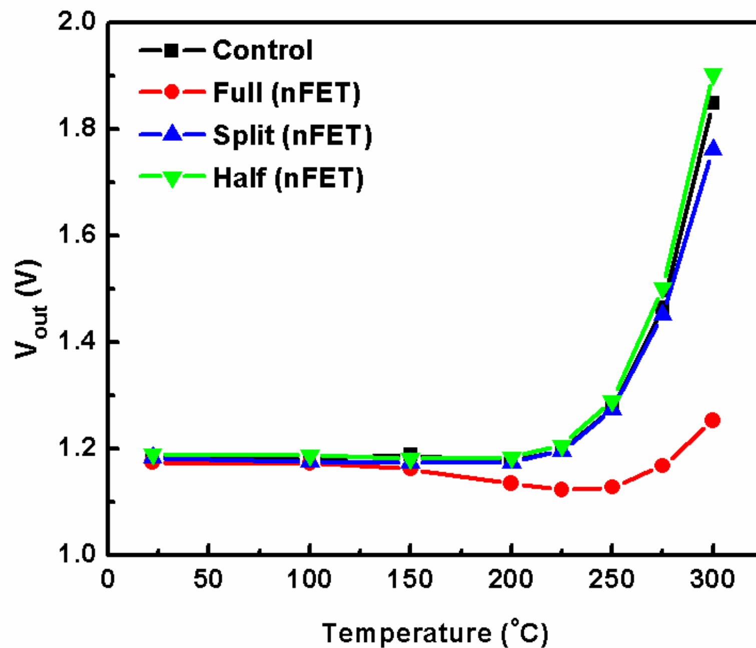

Figure 28: BGR output voltage across temperature with a single bypass nFET connected in various configurations.

4.5 Bypass Compensation Testing

The lack of accurate Cadence simulation capability left experimental verification of the bypass compensation technique as the only available route to determine its effectiveness.

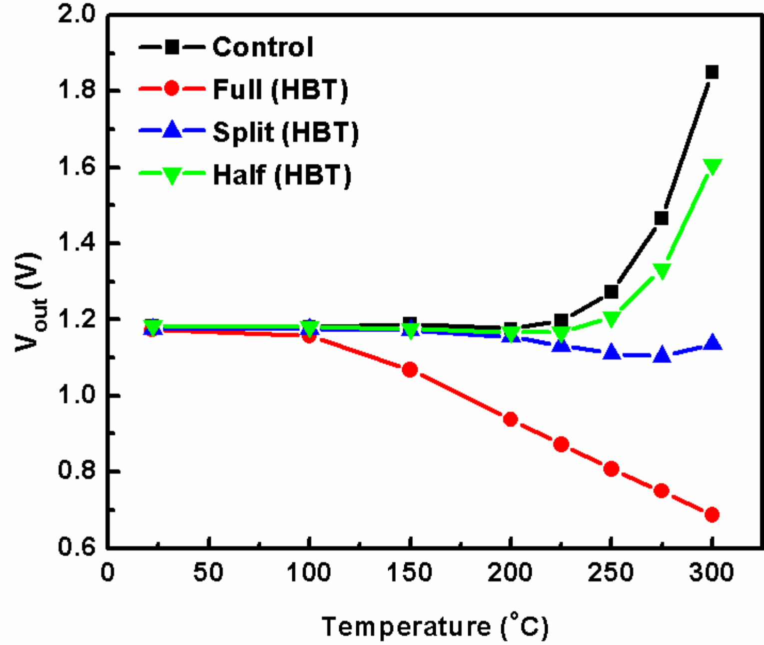

Figure 29: BGR output voltage across temperature with a single bypass HBT connected in various configurations.

Figure 28 shows the impact that each of the bypass configurations had on the output of the BGR with exponential compensation and no RHBD. Using the nFET as the bypass transistor, the split configuration showed a slight improvement above 250°C; however, the full configuration had a pronounced effect on V_{OUT}. In this configuration, the nFET turned on at a much lower temperature – below 150°C – leading to a gradual decrease in output voltage, followed by a stabilization and subsequent increase in V_{OUT} above 225°C. ΔV_{OUT} for the full-bypass configuration was 53 mV up to 275°C, a substantial improvement compared to the original BGR with exponential compensation. These results indicate the bypass transistor can be tuned for improved compensation by choosing the optimal location of the gate connection to R_2. However, altering the location of the drain connection did not improve performance, and in fact, the half-bypass

configuration actually demonstrated a larger increase in V_{OUT} compared to the control BGR. The bypass transistor did not turn on until approximately 250°C, and the leakage currents in the transistor at high temperatures must also flow through the upper, non-bypassed half of R_2, which were the major contributor to the decreased performance.

The bypass compensation technique also demonstrated effectiveness when a SiGe HBT was used in place of an nFET. Shown in Figure 29, the HBT had a stronger impact on output voltage compared to the nFET for all available configurations. The half-bypass configuration showed an improvement over the control, and the split-bypass configuration produced the smallest ΔV_{OUT} for either transistor, with a 73 mV variation to 300°C. Furthermore, the HBT in full-bypass shunted too much current, completely overpowering the PTAT current necessary for a stable output above 100°C. The locations of both the base and collector connections play a critical role in determining the effectiveness of the compensation technique, which could allow for better control during optimization.

4.6 Bypass Circuit Optimization

After demonstrating the functionality of the bypass compensation technique, the next step was to develop a numerical model for designing an optimized bypass network because the simulation tools in Cadence do not accurately model circuit behavior above 200°C. To simplify the optimization model, nFET(s) were chosen as the bypass transistor(s) due to their nature as voltage-controlled devices compared to the current-controlled SiGe HBTs. In addition, only the gate connection of the nFET needed optimization, whereas both base and collector connections of an HBT required it. The current shunted through the bypass transistor, I_{BYP}, was modeled by

$$I_{BYP}(T, \%_R) = \frac{V_{OUT}{}'(T) - V_{BE}(T)}{R_2(T)} - \frac{V_{OUT}{}''(T) - V_{BE}(T)}{R_2(T)} \tag{11}$$

where T is temperature (in K), $\%_R$ is the location of the gate connection to the resistor, V_{OUT}' is the output voltage of the control BGR, and V_{OUT}'' is the output voltage of the BGR for a given gate-resistor tap location. For $\%_R$, 1.0 and 0.5 signify full and split configurations, respectively, with a minimum value of zero ($V_G = V_{BE}$). V_{OUT}'' was measured experimentally by connecting the drain of the bypass transistor to V_{OUT} and sweeping the nFET gate voltage across the range of possible voltages as defined by V_{BE} and V_{OUT} for the control BGR at each temperature point.

Moving beyond the basic bypass circuit of a single nFET of a predetermined size, the numerical model also included the ability to use multiple nFETs with different gate connections, and the sizing of each nFET could also be scaled independently. The numerical model used to optimize the bypass compensation circuit design for the smallest variation in output voltage is given by

$$V_{OUT}(T) = V_{OUT}^{'}(T) - n_1 I_{BYP,1}(T, \%_{R1}) R_2(T) - n_2 I_{BYP,2}(T, \%_{R2}) R_2(T) - \ldots \tag{12}$$

where n is the scaling factor for the W/L ratio of each transistor, relative to 10/1. Figure 30 compares the match between the modeled and measured values for V_{OUT} in both full and split configurations. The output voltage predicted by the model is within 0.7% of the actual amount for both configurations at all temperatures, except for 300°C in the split configuration where there is still less than 3% difference.

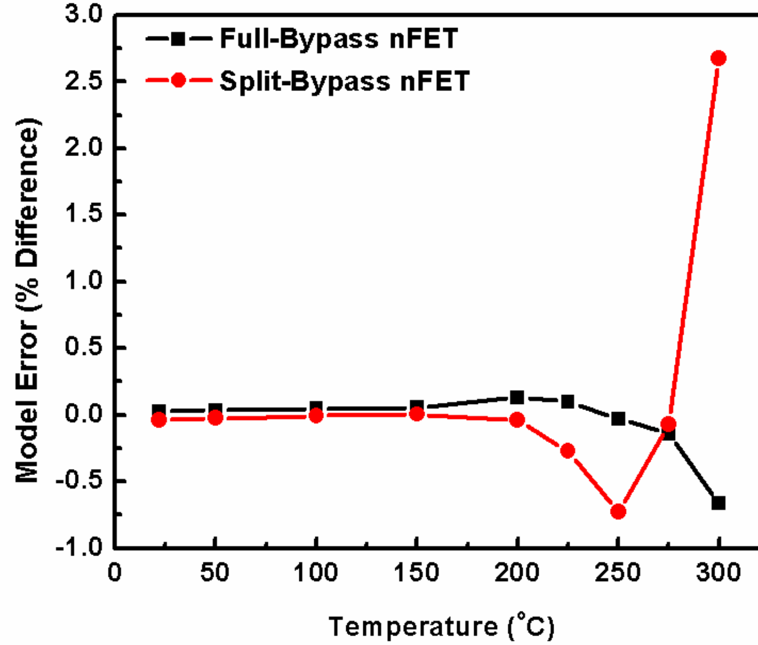

Figure 30: Measure of fit for numerical optimization model of compensation network with experimental data.

The model was then used to optimize the circuit over a 22°C to 275°C temperature range. When using a single bypass nFET, increasing the W/L ratio improved performance, albeit with diminishing returns. Figure 31 shows the optimal gate connection for various size nFETs, and a minimal predicted ΔV_{OUT} of 11.7 mV is obtained with W/L equal to 140/1, or equivalently, a single 10/1 nFET with fourteen fingers. Adding a second nFET to the compensation circuit provided a further improvement in ΔV_{OUT} to 7.3 mV, shown in Figure 32 with the predicted output for two single-transistor bypass networks. In both cases, the variation in output voltage generally

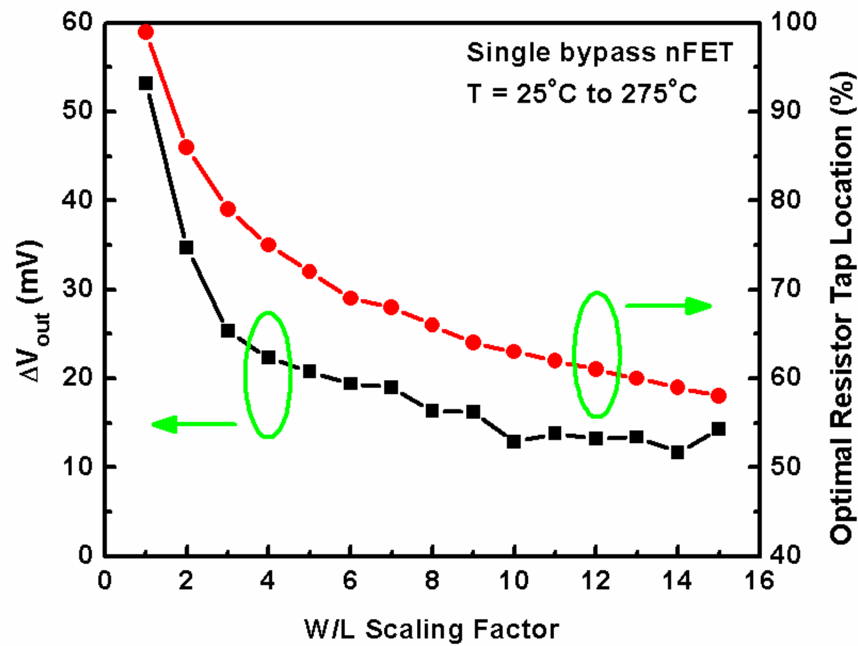

Figure 31: Optimal transistor sizing and gate connection for single nFET bypass compensation network.

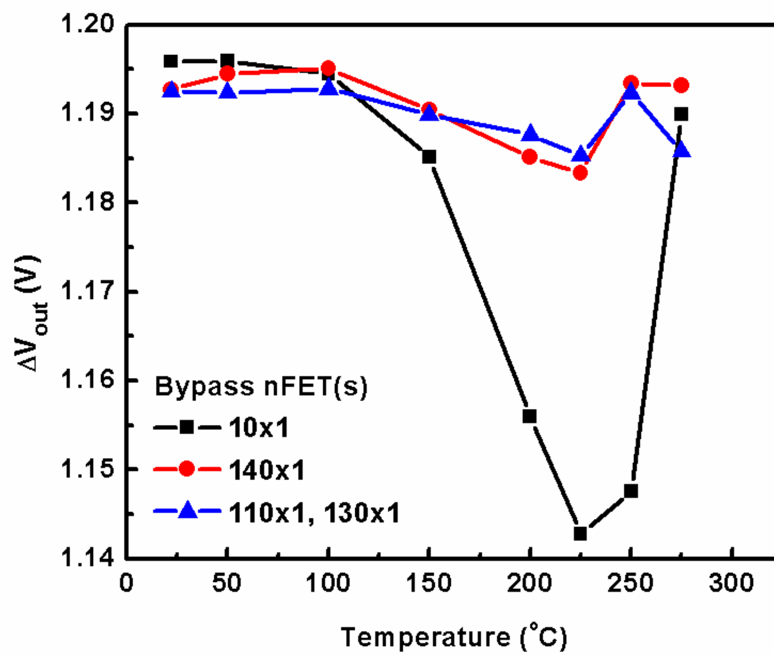

Figure 32: Predicted BGR output voltage for single and double bypass nFET compensation networks optimized for 275°C.

followed an inverse relationship to the size of the transistors used, shown in Figure 33 and Figure 34 for the two transistor bypass network.

Additionally, the location of the gate connection ($\%_R$) is worth discussing for the one- and two-transistor bypass networks. For both cases, the “dominant” nFET was connected above split-bypass configuration ($\%_R \approx 58\%$), causing it to turn on at a lower temperature and shunt the majority of the excess current around the resistor. When the second transistor was added, this “supplemental” nFET was connected below split-bypass ($\%_R \approx 44\%$), which means it only shunts current at the very upper end of the temperature range. Also, the size of the dominant transistor was reduced to accommodate the presence of the additional one, but the combined area penalty is substantially larger. Due to the diminishing returns in ΔV_{OUT}, adding more bypass transistors is not worth the extra die space.

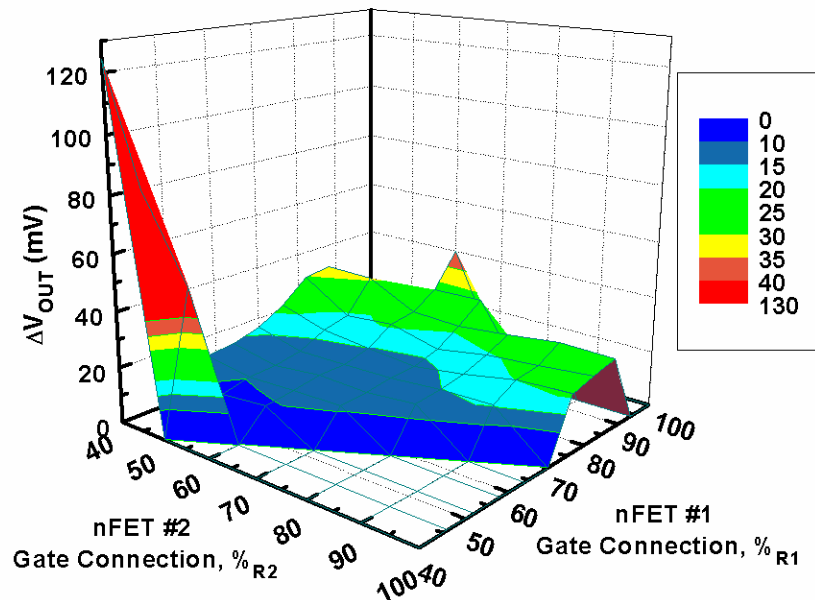

Figure 33: Optimization of ΔV_{OUT} from 25°C to 275°C for possible gate-resistor tap locations using two bypass nFETs.

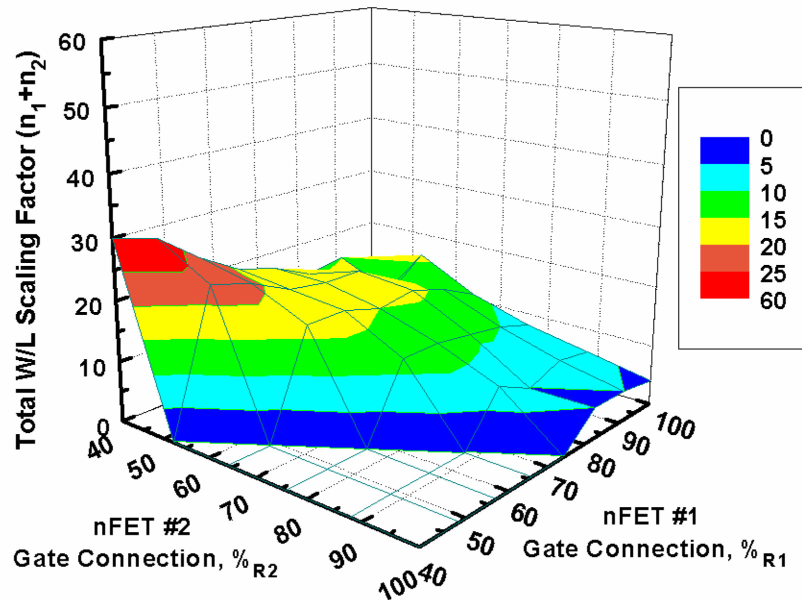

Figure 34: Optimal combined W/L sizing ratios using two bypass nFETs (n_1 + n_2) for minimum ΔV_{OUT} across a temperature range of 25°C to 275°C based on gate connection location.

Using the same procedure for an operating range extending from room temperature to 300°C, the optimal circuit values for ΔV_{OUT} of 34.7 mV and 30.7 mV were obtained using one and two bypass nFETs, respectively, shown in Figure 35. However, unlike the optimization for 275°C, the output voltage variation and transistor size showed minimal correlation for 300°C conditions. Rather, the optimal two-transistor design resulted in near-minimal transistor sizing. As with the 275°C optimization analysis, the first nFET was dominant, and in fact shunted an even larger percentage of the current. The dominant nFET was connected much closer to full-bypass configuration than split-bypass ($\%_R \approx 85\%$) for this temperature range, while the second nFET was connected almost identically to the previous range ($\%_R = 44\%$). The greater difference in $\%_R$ between the

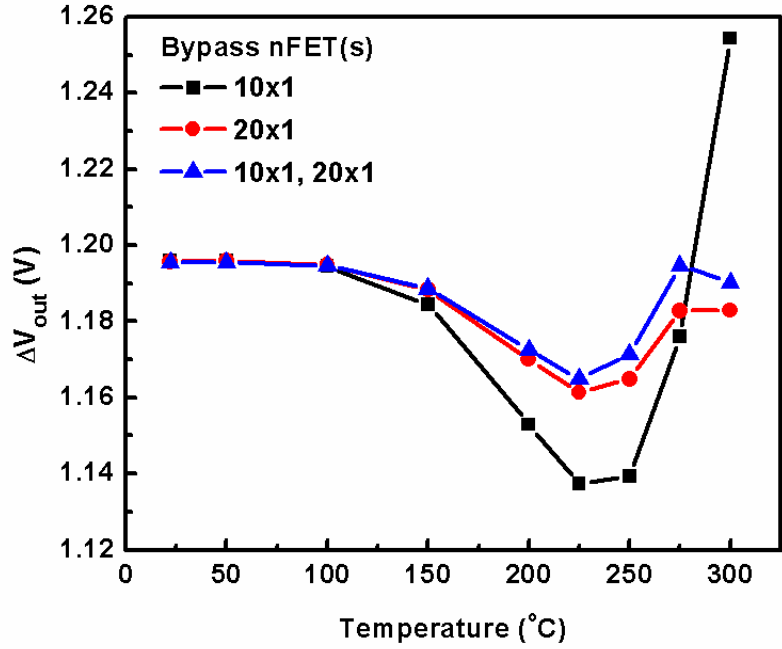

Figure 35: Predicted BGR output voltage for single and double bypass nFET compensation networks optimized for 300°C.

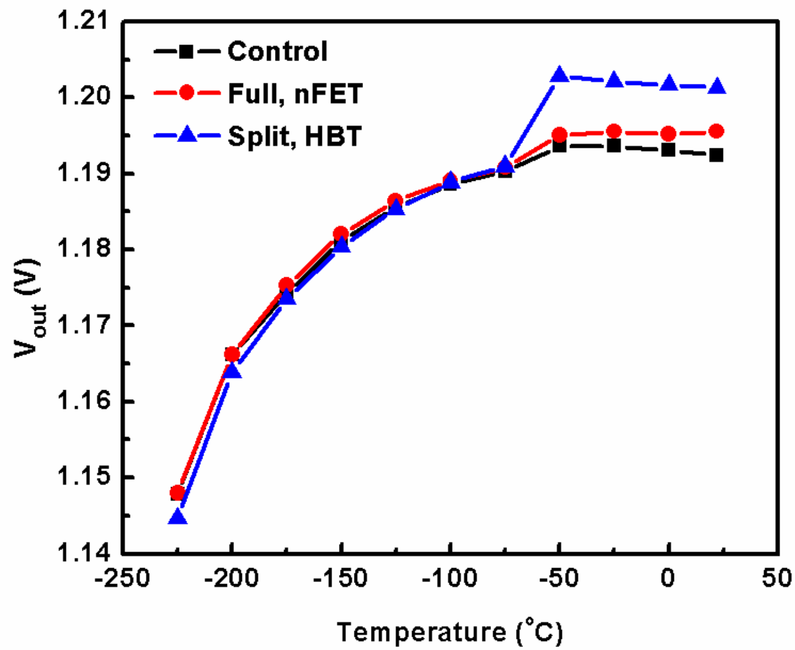

Figure 36: Cryogenic performance of SiGe BGR with high-temperature bypass compensation.

two transistors indicates extra nFETs will have even less impact on ΔV_{OUT} for higher temperatures.

Because the goal was to design a BGR for ultra-wide temperature range operation, ensuring the bypass compensation does not affect the superior cryogenic performance (derived from the exponential compensation architecture in [44]) is important. The two available hardware configurations with the best performance – nFET in full-bypass and SiGe HBT in split-bypass – were compared to the original BGR with exponential compensation, and the nFET in full-bypass configuration caused no deviation from the control at cryogenic temperatures. The HBT in split-bypass configuration performance was only slightly affected, with a deviation of approximately 3 mV at -225°C. Based on these results, the bypass compensation technique was verified to have minimal to no effect on cryogenic performance, allowing for operating ranges in excess of 500°C. The SiGe BGR with exponential compensation and nFET in full-bypass configuration achieved a ΔV_{OUT} equal to 59.2 mV from -225°C to 275°C. Furthermore, by combining the predicted output from the high-temperature optimization model with the low temperature measurements, ΔV_{OUT}'s of only 7.3 mV and 30.7 mV across temperatures ranges of 400°C and 500°C, respectively, are possible. Table 1 summarizes the performance of the various SiGe BGRs, which to the best of the author's knowledge are believed to be new records for bulk-Si technology platforms.

Table 1: Performance of SiGe BGRs across various temperature ranges.

BGR Type	V_{OUT}, 25°C (V)	Temp. Range (°C)	ΔV_{OUT} (mV)	TC (ppm/°C)
First-order	1.174	25 to 200	9.7	47.2
Exp Comp	1.196	-150 to 200	15.0	35.8
Exp Comp + RHBD	1.187	25 to 200	2.2	10.6
		25 to 225	14.0	59.0
Exp Comp + Split Bypass HBT	1.177	-225 to 300	98.6	159.6
Exp Comp + Full Bypass nFET	1.196	-225 to 275	59.2	98.0
Exp Comp + Bypass nFETs (model)	1.196	-125 to 275	7.3	15.3
		-200 to 300	30.8	51.5

4.7 Temperature Sensor Circuit

The same principles used to design the BGR circuit can also be adapted to create a temperature sensor. Using the same startup circuit and PTAT current generator, the temperature sensor substitutes a PBDT resistor in place of the SiGe HBT and its negative temperature dependence of V_{BE}, as shown in Figure 24. Three variant output stages were available for measurement. In the first output stage (V_{OUT1}), the intercept, which helps determine the room temperature voltage, can be altered by forcing an external current (I_{DC}) through an nFET current mirror, while having a minimal effect on the slope of the output voltage. By modifying the pFET sizing ratio in the current mirrors and the value of R_2, both the slope and offset of the output can be controlled at the design stage, as demonstrated by V_{OUT2}. Lastly, V_{OUT3} utilized an on-chip, 25 µA current source in place of an external I_{DC} to control the output voltage offset.

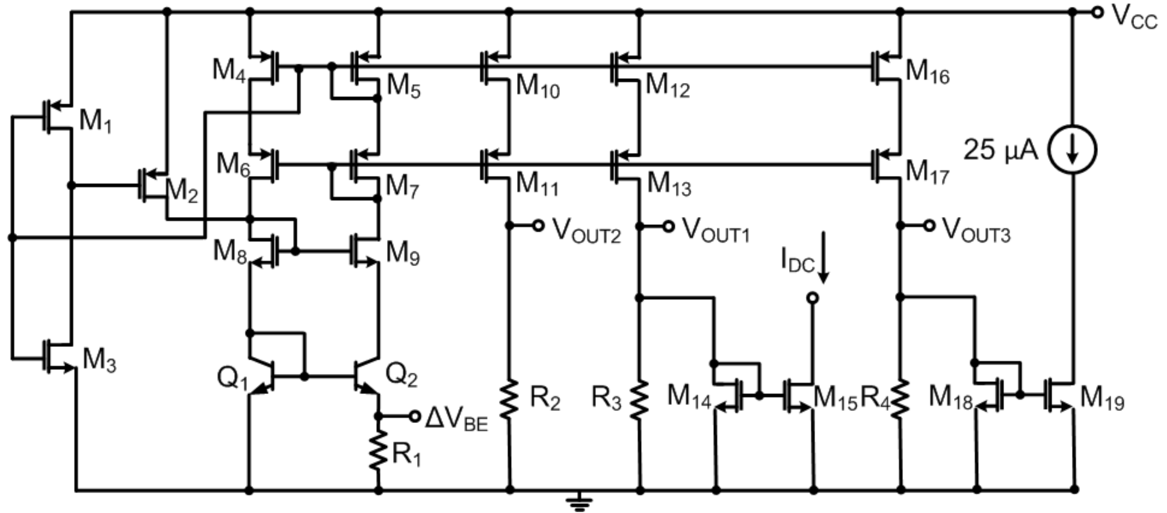

Figure 37: Schematic of SiGe temperature sensor circuit with multiple output terminals.

4.8 Temperature Sensor Testing

Similar to the BGR circuit, the temperature sensor behaved linearly up to 200°C, matching the simulated slopes closely while exhibiting a nominal offset of 20 to 40 mV compared to simulation. These results are summarized in Table 2. A minor non-linearity in the slope appeared between 200°C and 225°C, at which point the output voltages began to rise rapidly up to 300°C, shown in Figure 38. Of particular interest, the internal current source associated with V_{OUT3} proved slightly more effective than the externally-supplied I_{DC} at suppressing the voltage rise at high temperatures. This effect was likely due to a non-linear increase in the internal current source concurrent with the temperature increase, leading to a larger amount of current being shunted away from the resistor. Conversely, the external current was held constant at 30 µA and did not exhibit any additional temperature compensating properties.

Table 2: Measured and simulated SiGe temperature sensor performance up to 200°C.

	Measurement			Simulation	
	Intercept (mV)	Slope (mV/°C)	Correlation, R^2	Intercept (mV)	Slope (mV/°C)
V_{OUT1}, $I_{DC} = 0\mu A$	670.4	2.61	0.99902	700.3	2.58
V_{OUT2}	504.4	1.96	0.99902	525.2	1.94
V_{OUT3}	475.7	2.53	0.99889	502.4	2.51
V_{OUT1}, $I_{DC} = 30\mu A$	427.3	2.57	0.99901	466.4	2.50

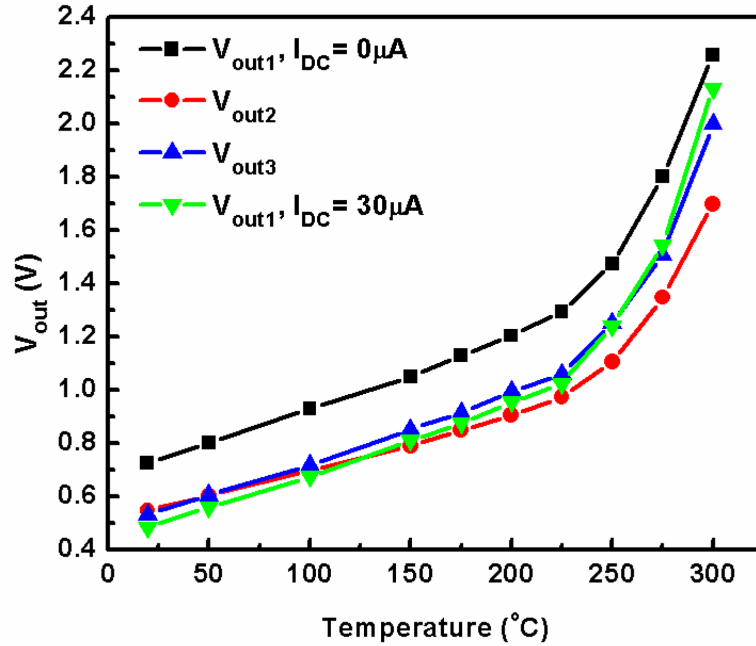

Figure 38: Temperature sensor output voltage across temperature for various terminals and bias conditions.

When considering the ability of a temperature sensor to accurately measure ambient temperature, a key concern is whether the circuit experiences self-heating. Self-heating occurs when the power dissipated in the circuit causes the local temperature of the die to increase. In a temperature sensor circuit, self-heating can cause a positive feedback action, whereby higher local temperatures force a higher current draw and which in turn causes the substrate temperature to increase again. This phenomenon can be exacerbated in silicon BJTs due to the positive correlation between current gain and temperature; however, a SiGe HBT's current gain varies inversely with temperature, as previously

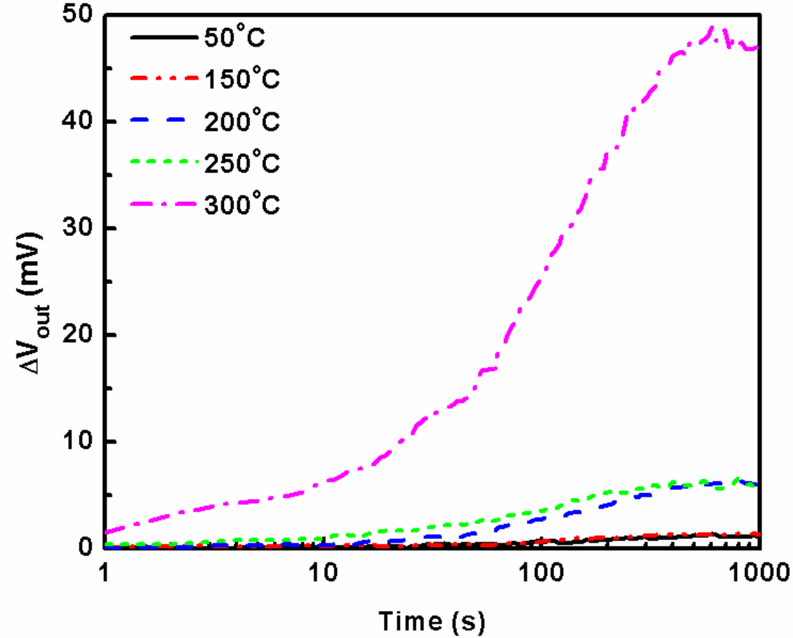

Figure 39: Self-heating of SiGe temperature sensor at various temperatures.

established. Accordingly, a temperature sensor that utilizes SiGe HBTs rather than Si BJTs should be less sensitive to self-heating errors.

To examine any self-heating effects in the temperature sensor, the circuit was allowed to stabilize at each temperature point in an "off" state for a period of at least 10 minutes, at which point the power supply was turned on. Samples at the output of two output stages were collected on each run, and a second temperature sweep was performed later to capture the remaining output configurations. Figure 39 shows the typical self-heating effects, represented by the change in V_{OUT3} over time, at temperature points ranging from 50°C to 300°C. Below 200°C, ΔV_{OUT} was approximately 1 mV, indicating virtually no self-heating occurred. At 200°C and 250°C, the sensor experienced a 5 mV shift in V_{OUT}; however, this change introduced an error of only 2°C at the output. Significant self-

heating was present at an ambient temperature of 300°C with ΔV_{OUT} an order of magnitude higher at nearly 50 mV. Similar results were observed in the other output stages.

In order to extend the operating temperature range of the sensor, the most obvious solution would be to add a non-linear current source to be forced through I_{DC} that mimics the excess current across the temperature range; however, the practical design of such a source is non-trivial. Another possibility would be to employ a transistor bypass network similar to that proposed in the previous section. Adding external n-rings to the HBTs would also likely provide enough leakage current suppression to extend the fully linear operating range from 200°C to at least 225°C in the event a slightly higher maximum temperature is needed, perhaps providing sufficient improvement to allow even 250°C operation. Lastly, the self-heating effects above 250°C must be addressed to reach the targeted 300°C ambient environments. Once the operating range is extended to match the BGR, the two circuits can be combined to produce a full analog-to-digital temperature sensor with additional features to refine performance, such as trimming [46].

4.9 Summary

Multiple bandgap-based circuits designed in a bulk SiGe BiCMOS platform were experimentally verified to remain functional in environments with ambient temperatures ranging from room temperature up to 300°C. Several pre-existing device and circuit level design improvements for cryogenic and under-radiation conditions were also shown to improve the performance of SiGe BGRs at high temperatures, and a new compensation technique utilizing a temperature-controlled current shunting method was presented.

This bypass compensation was shown to significantly reduce variations in output voltage at high temperatures. Using a combination of experimental results and numerical analysis, the bypass compensation network can be optimized for a desired temperature range, which predicts new records in voltage reference stability over 400°C and 500°C ranges for any bulk silicon-based process technology. A closely-related temperature sensor circuit was also found to operate ideally up to 200°C, and with minor modifications, could be combined with the proposed BGR to form the basis for an extreme wide range digital temperature sensor.

CHAPTER V

AMPLIFIER CIRCUITS

5.1 Introduction

With two bandgap based SiGe circuits demonstrated capable of handling extreme high temperature ambient conditions, the next step was to move from purely DC circuits to low frequency analog circuits. Fortunately, two such circuits were already available for characterization: an operational amplifier and an output buffer. Many types of operational amplifiers – “opamps” for short – have been developed, as they are used in an extremely wide variety of circuit applications ranging from simple mathematical functions (adders, differentiators, etc.) to high-power or low-noise gain stages to buffering. The opamp chosen for this investigation was designed to operate as the front end of a charge amplifier circuit, which requires the ability to handle large capacitive loads on the order of 10 nF.

Although opamps can be configured to behave as buffer circuits, specially designed buffers can provide superior performance while at the same time require a smaller layout area. In this chapter, an output buffer will also be characterized up to 300°C. This circuit, with its high input and low output impedances, is ideal for driving 50 Ω loads such as an oscilloscope with several feet of cabling. Both of these circuits had been previously designed as part of a multi-year program supported by NASA to develop a remote electronics unit (REU) for lunar and other extraterrestrial missions. As with the bandgap circuits, neither the opamp nor buffer were optimized for high temperature operating environments.

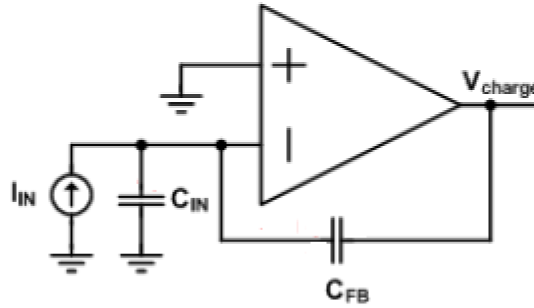

Figure 40: Simplified diagram of a typical charge amplifier circuit used to convert a sensor's input charge into an output voltage.

5.2 Operational Amplifier for Large Capacitive Loads

Piezoelectric sensors are a widely used class of sensors that measure pressure, acceleration, strain, or force by converting the desired input into an electrical current. Such sensors are highly desirable for high temperature applications, especially downhole [2]. In order to process the signal from the piezoelectric sensor, a data acquisition system must contain a charge amplifier to convert the incoming charge into a voltage, which is traditionally accomplished through the use of an operational amplifier with a capacitive feedback loop. Charge amplifiers are also useful with other charge-based devices such as photodiodes. Figure 40 depicts the basic structure of a charge amplifier.

To build a charge amplifier, an operational amplifier that is capable of handling the large capacitances in the system must be designed first. Shown in Figure 41, a suitable circuit using an operational transconductance amplifier (OTA) topology was available for characterization [47]. This circuit utilized a pFET differential pair to minimize input currents, which could compromise its sensitivity to small charge variations from the sensor, and because the circuit uses only SiGe HBTs and pFETs, it is inherently more radiation tolerant compared to a design with nFETs. Unfortunately, mismatch

Figure 41: Circuit topology for the operational amplifier for large capacitive loads [47].

(systematic or random) between the positive and negative stages of the amplifier could lead to offset problems that would be especially troubling at high temperatures.

Typical piezoelectric sensors operate at very low frequencies, which meant the associated charge amplifier did not require the superior RF performance derived from the SiGe HBTs but instead benefited from their low 1/*f* noise. Although the operational amplifier under investigation was only required to have a bandwidth of 5 kHz according to the specification, it was designed with higher frequency applications in mind for versatility and reusability. As with the BGR and temperature sensor, the sponsoring program had targeted this circuit for lunar operating conditions of -180°C to 125°C, with possible lows of -230°C in the shadowed craters and TID/SEE radiation as well.

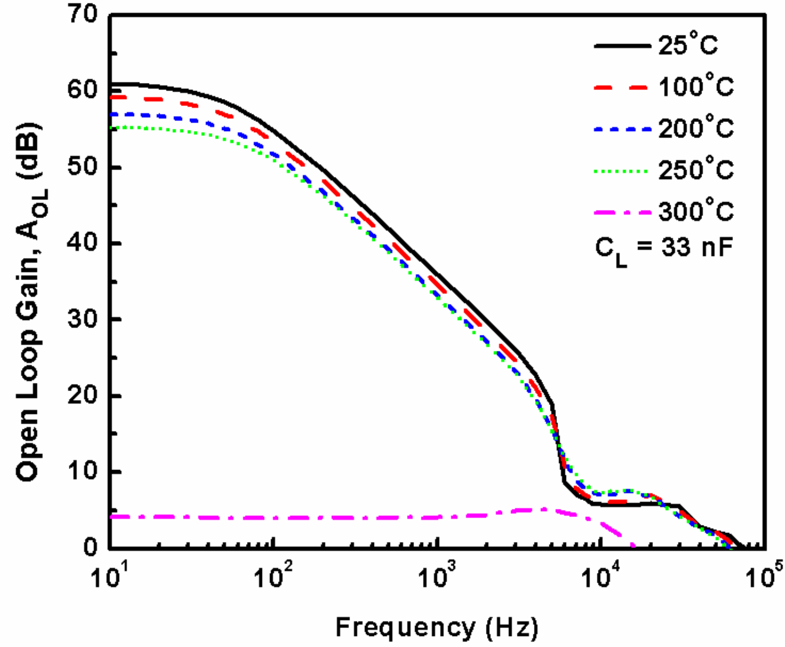

Figure 42: Frequency response of opamp with 33 nF load across temperature.

Figure 42 shows the measured frequency response of the opamp from room temperature to 300°C, with passives located outside the test chamber in room temperature conditions. From room temperature up to 250°C, the opamp was fully functional, experiencing minor drops in open loop (DC) gain, -3dB bandwidth (f_{3dB}), and unity gain bandwidth. DC gained remained above 55 dB across the temperature range, while -3dB and unity-gain bandwidth stayed above 55 Hz and 60 kHz, respectively. Above 250°C, the open loop gain began to fall off rapidly due to clipping and rising DC offset, and by 300°C, the amplifier was no longer usable in a practical system.

These results also show good agreement with Cadence simulations. In Figure 43, the experimental results match simulation except for a slightly lower DC gain, which is notoriously difficult to measure. The measured bandwidth was actually slightly higher

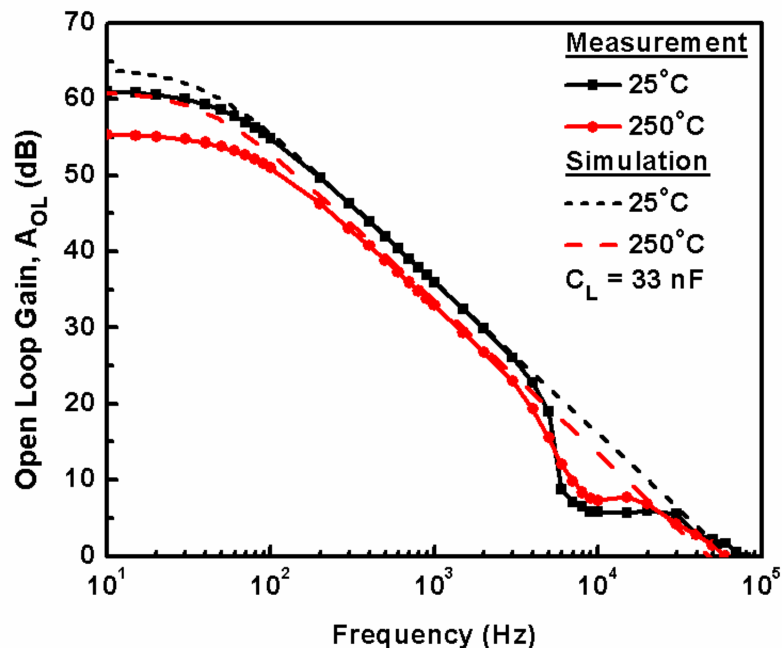

Figure 43: Comparison of simulated and measured frequency response of SiGe opamp at room temperature and 250°C.

compared to simulation. Lastly, the non-linearity observed near 10 kHz is believed to be caused by harmonics and reflections arising from a combination of the PCB packaging approach and parasitic effects between the amplifier and externally-located passives, especially in the feedback network.

In addition to the bandwidth of the amplifier, several other important parameters were characterized up to 300°C, although the results from room temperature to 250°C are presented here due to previously mentioned degradation above 250°C. The DC offset voltage for the opamp, measured at the output by grounding both input terminals through 100 Ω resistors, adding a 1 kΩ feedback resistor, and dividing out the gain factor (10), was significantly higher than anticipated, with values ranging from 5.93 mV at 25°C to

Table 3. Measured and simulated figures of merit for the SiGe operational amplifier.

Parameter	Measurement		Simulation		Unit
	25°C	250°C	25°C	250°C	
3dB Bandwidth, f_{3dB}	58	76	40	42	Hz
Open-loop Unity Gain Bandwidth	77	60	63	48	kHz
Open-loop (DC) Gain	61.0	55.3	64.1	61.1	dB
DC Offset (Gain = 10)	5.93	8.77	5.57	8.41	mV
Positive Slew Rate	42.3	46.5	47.5	45.4	kV/s
Negative Slew Rate	-51.1	-53.0	-51.5	-51.5	kV/s
Quiescent Current (V_{IN} = 1.65 V)	1432	1684	940	995	µA
Power Consumption (V_{IN} = 1.65 V)	4.73	5.56	3.10	3.28	mW
Maximum V_{OUT} ($V_{IN} = V_{DD}$)	2.63	2.83	2.62	2.86	V

8.77 mV at 250°C. However, using alternate simulation approaches not feasible for experimental characterization, DC offset was predicted to be on the order of 1 mV.

The slew rate of the amplifier, which is the maximum rate of change in the output voltage for all possible input signals, actually improved slightly with increasing temperature – a welcome sign. Furthermore, the quiescent current (Q-current) drifted only slightly higher with temperature, and accordingly, the power consumption of the amplifier remained near 5 mW. Shown in Table 3, all measurements agreed with simulation for the most part. Of final note, all measurements were taken with a 33 nF capacitive load at the output of the amplifier.

5.3 Low-Impedance Output Buffer

Many amplifiers designed for integrated systems lack the ability to drive low-impedance loads, necessitating the addition of an output buffer. In addition to a low output impedance, these buffer circuits offer a high input impedance and an inherent unity gain, and Figure 44a provides a high-level block diagram example of an output buffer with

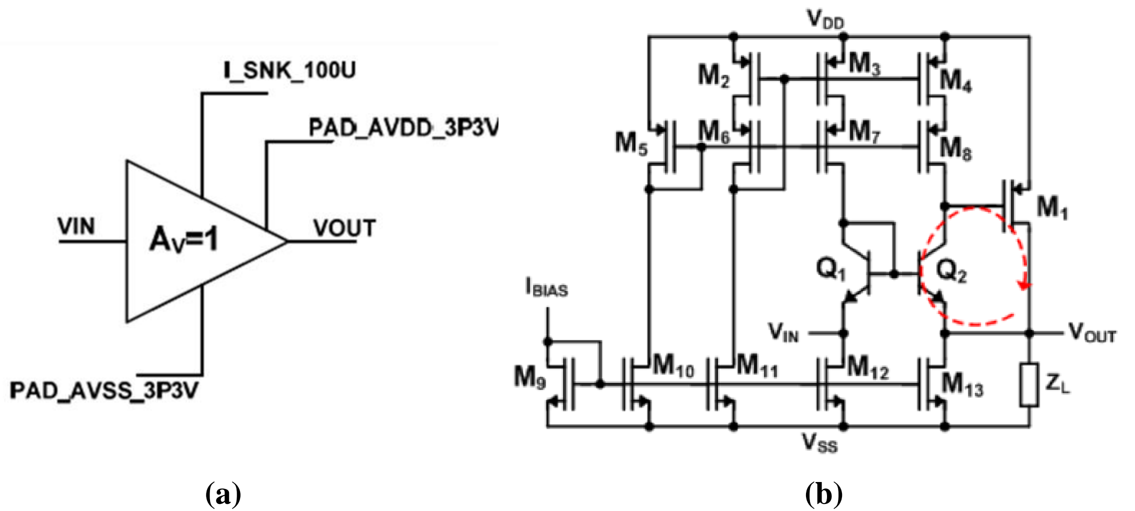

Figure 44: Output buffer circuit shown in (a) block diagram and (b) full circuit topology.

these characteristics. An emitter follower is the most basic topology for an output buffer; however, it exhibits undesirable DC gain behavior and signal distortion due to changes in transconductance during large signal swing. Shown in Figure 44b is a realized output buffer circuit using a "pony-amp" architecture with shunt-feedback at the output reduces the sensitivity inherent in emitter follower topologies [47]. This circuit was designed with a 50 Ω oscilloscope load in mind.

In addition to the standard supply voltage, the output buffer also required a 100 μA bias current, which could be provided from an external supply. Alternatively, an on-chip current source, based on the bandgap reference described earlier, was available. The voltage applied to a MOSFET switch determined whether the internal supply was used.

For this relatively simple circuit, the most important indicator of performance is the ability to generate a one-to-one match between the input and output signals across the widest possible input range. The DC transfer characteristic captures this fundamental performance metric, and the experimental results across temperature are shown in

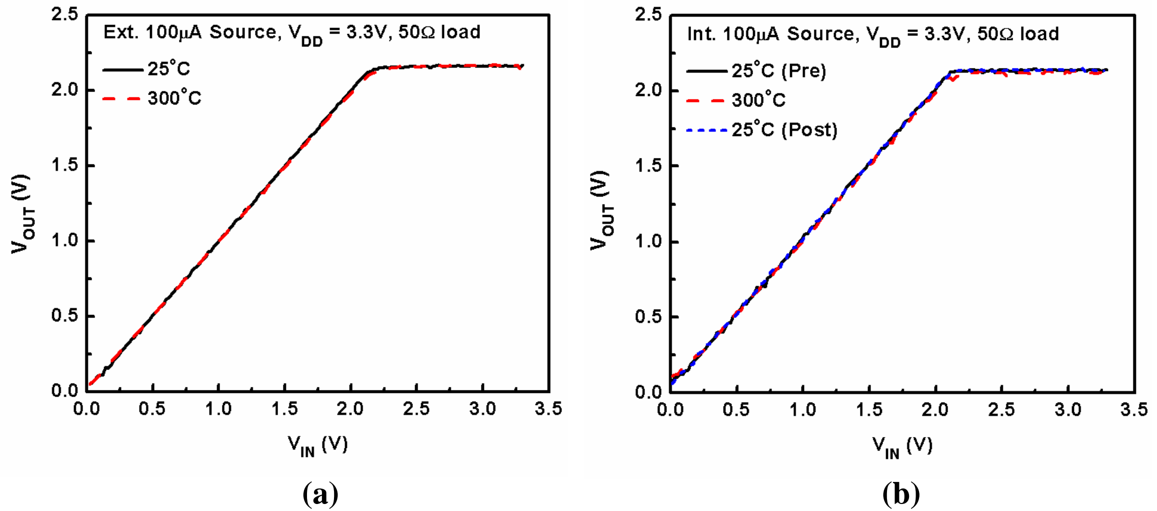

Figure 45: DC transfer characteristic for output buffer across temperature with 3.3V V_{DD}, 50 Ω load, 100 μA current source supplied (a) externally and (b) internally.

Figure 45a and Figure 45b for external and internal bias current, respectively. Impressively, neither configuration experienced a change in behavior between room temperature and 300°C; furthermore, there were no stress-related effects on the circuit after short-term exposure to 300°C, also shown in Figure 45b. These results also indicate the internal current source functioned properly. The continued lack of damage due to short-term exposure in SiGe circuits is very encouraging.

The minimum and maximum output voltages in Figure 45 were also largely temperature independent. For a grounded input, V_{OUT} remains well below 100 mV, and the maximum V_{OUT} remains just above 2.1 V across the entire temperature range. Input leakage currents do increase from 1.8 μA to 7.4 μA, but these levels are still acceptable for a high input impedance circuit. From a power consumption standpoint, the buffer requires 151 mW to drive a 50 Ω load with the input at mid-rail; however, less than a third of the power was consumed (45 mW) with no load attached (high-Z output). Both

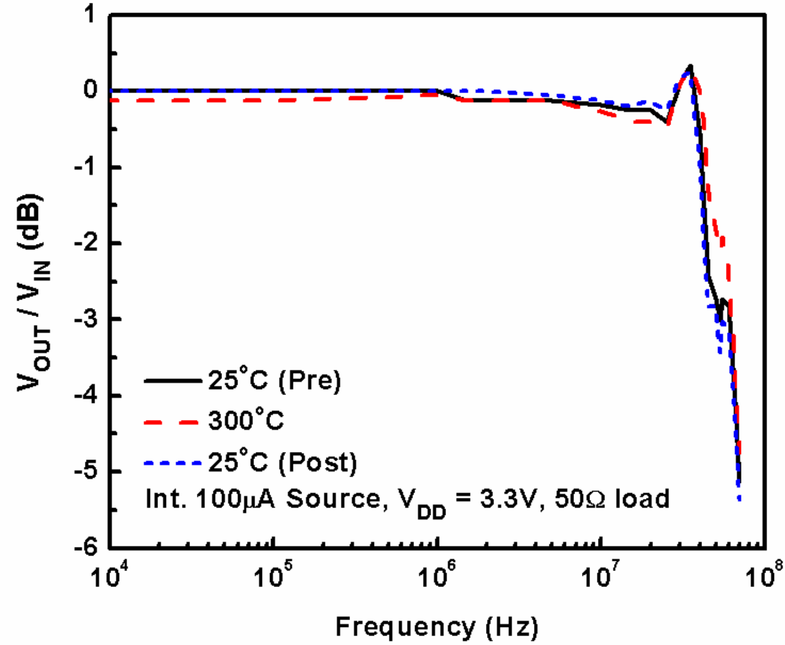

Figure 46: System-limited frequency response of SiGe output buffer across temperature using on-die 100 μA current source.

load conditions showed in little to no variation in power consumption with respect to temperature. Finally, the onboard current source, which drew only 12.1 mW at 25°C, required only 1 mW of additional power at 300°C.

With excellent DC characteristics over temperature established, the next step was to examine the AC performance. Simulations predicted a -3dB bandwidth on the order of several hundred MHz, but unfortunately, the high temperature station's measurement capabilities were limited to approximately 10 MHz, as described in Chapter 3. With this limitation in mind, the frequency response of the output buffer is shown in Figure 46, confirming that the circuit functioned as expected over the system-limited range. The circuit did demonstrate a minor 0.1 dB decrease in gain at 300°C which was not present in the DC characteristics.

Table 4: Measured and simulated figures of merit for SiGe output buffer with 3.3 V V_{DD}, internal 100 μA current source, and 50 Ω load unless otherwise specified.

Parameter	Measurement		Simulation		Unit
	25°C	300°C	25°C	300°C	
3dB Bandwidth, f_{3dB}	> 40	> 40	432	175	MHz
Q Current (V_{IN} = 1.65V)	45.8	48.0	46.7	46.3	mA
Q Current (V_{IN} = 1.65V, No load)	13.8	16.4	14.0	13.9	mA
Input Current (V_{IN} = 1.65V)	1.8	7.4	0.9	38.6	μA
Int. 100μA Source Power Consumption	12.1	13.1	1.5	1.6	mW
$V_{OUT,MIN}$	44	79	39	63	mV
$V_{OUT,MAX}$	2.14	2.12	2.17	2.13	V
$V_{OUT,MAX}$ (No load)	2.40	2.74	2.41	2.72	V

Finally, an attempt to measure the step response of the output buffer was made; however, the limitations on test system bandwidth again proved to be a problem. According to Cadence simulation, settle times were on the order of several nanoseconds – well beyond the experimental capabilities of the high temperature system. These results should not be a problem except for circuits that are pushing the upper limits of the buffer's frequency range. Both the DC and AC figures of merit are summarized in Table 4 for the output buffer with a 3.3 V power supply (V_{DD}).

In addition to the standard 3.3 V power supply specified for the SiGe BiCMOS technology under investigation, the output buffer circuit could be overdriven to accept a higher range of input signals by applying a 5 V supply. The maximum output voltage was extended beyond 3.3 V across the 300°C temperature range, and as expected, the power consumed increased proportionally for a mid-rail input. Simulation and measurement results for the primary figures of merit were in good agreement, summarized in Table 5. Further work to establish the reliability with a 5 V supply should be undertaken in order to fully qualify the output buffer under these conditions.

Table 5: Measured and simulated figures of merit for SiGe output buffer with 5 V V_{DD}, internal 100 μA current source, and 50 Ω load unless otherwise specified.

Parameter	Measurement		Simulation		Unit
	25°C	300°C	25°C	300°C	
Q Current (V_{IN} = 2.5V)	62.6	64.9	64.0	63.5	mA
Q Current (V_{IN} = 2.5V, No load)	13.9	16.6	14.4	14.1	mA
Input Current (V_{IN} = 2.5V)	-26.3	-16.6	-53.9	5.9	μA
$V_{OUT,MIN}$	83	144	48	75	mV
$V_{OUT,MAX}$	3.57	3.45	3.70	3.60	V
$V_{OUT,MAX}$ (No load)	4.09	4.43	4.11	4.40	V

5.4 Summary

Two classes of existing SiGe amplifier circuits have been shown to operate at very usable performance levels in high temperature environments. An OTA designed for use in a charge amplifier circuit performed well up to 250°C, while an output buffer for driving low-impedance loads experienced no virtually no degradation across the entire 300°C range. In order to extend the usable operating range of the opamp to match the buffer and BGR circuits, one possible approach would be to add RHBD external n-rings to the SiGe HBTs. Another potential solution to reduce offset would be to cascode the SiGe HBTs in the output stage with nFETs to shield the collectors from voltage mismatch [47]. In addition to the high temperature performance of these circuits, the simulation of their cryogenic capabilities suggests both of these circuits can be utilized at temperatures down to -180°C, if not lower. These results lend further support to the case for SiGe technology as suitable for ultra-wide temperature range applications.

CHAPTER VI

CONCLUSION

This work has described the development of a robust packaging approach and test system to enable characterization of devices and circuits in ambient temperatures from 25°C to 300°C. Using this test system, a first generation SiGe BiCMOS technology has been shown to perform acceptably up to 300°C, providing a cost-effective competitor for traditional high temperature electronics platforms such as SOI and SiC. For the first time ever, four types of circuits developed using SiGe HBTs (bandgap voltage reference, temperature sensor, operational amplifier, and output buffer) have also been characterized for use in high temperature environments, highlighted by the design of a novel BGR compensation technique to enable a 500°C operating range.

6.1 Future Work

The promising results presented here suggest a number of interesting opportunities for future research. Of immediate interest would be to optimize the temperature sensor and opamp circuits for high temperature environments to match the 300°C upper limit achieved by the BGR and output buffer. These components represent key building blocks of a new remote electronics unit (REU) for health monitoring and data acquisition being developed for NASA using SiGe technology. Shown in Figure 47, the additional circuit elements of the analog remote sensor interface (RSI) are also prime candidates for high temperature characterization and optimization, especially the improved operational amplifier described in [48]. Additional reliability testing would also be a useful pursuit. Finally, characterization of more recent generation SiGe BiCMOS technology nodes with

higher speed transistors is underway, as well as a study comparing bulk-SiGe and SiGe-on-insulator (SGOI) technology platforms.

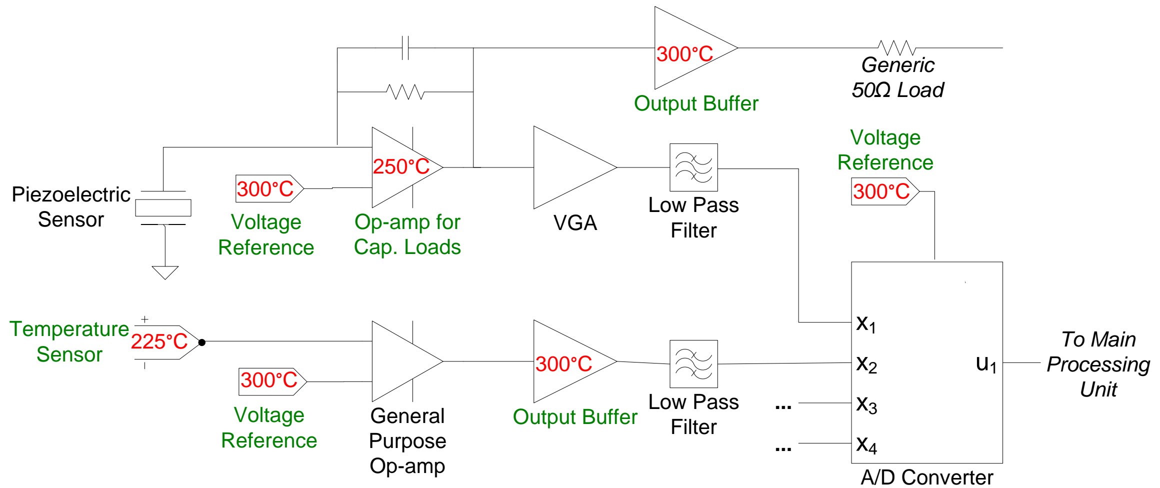

Figure 47: Overview of remote sensor interface (RSI) for extreme environments including components shown in this work to operate above 200°C.

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