ADAPTIVE OXIDE BASED LOW-POWER MEMRISTIVE DEVICES FOR NEUROMORPHIC COMPUTING

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ADAPTIVE OXIDE BASED LOW-POWER MEMRISTIVE DEVICES FOR NEUROMORPHIC COMPUTING

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LIST OF SYMBOLS AND ABBREVIATIONS

φ	Flux Linkage
ΔR	Resistance change
AC	Alternating Current
Ag	Silver
Al	Aluminum
ANN	Artificial Neural Network
Ar	Argon
Au	Gold
BE	Bottom Electrode
C	Capacitance
CF	Conducting Filament
CIM	Computation-in-memory
CMOS	Complementary-metal-oxide-semiconductor
CPU	Central Processing Unit
Cr	Chromium

DC	Direct Current
DNN	Deep Neural Network
DRAM	Dynamic random-access memory
EDSN	Even Driven form of Spiking Network
ECRAM	Electrochemical random-access memory
EIS	Electrochemical impedance spectroscopy
EMNIST	Extended Modified National Institute of Standards and Technology
EXAFS	Extended X-ray absorption fine structure
FinFET	Fin field-effect transistors
FTJ	Ferroelectric tunnel junction
GST	Germanium-antimony-tellurium
HAXPES	Hard X-ray Photoelectron Spectroscopy
HRS	High resistance state
I	Current
IEN	Institute for Electronics and Nanotechnology

IoT	Internet of Things
l	Length
Li	Lithium
LPEE	Liquid phase electro-epitaxy
LRS	Low resistance state
MBE	Molecular beam epitaxy
MFC	Mass flow controller
MIM	Metal-insulator-metal
MIT	Metal-insulator-transition
MOSFET	Metal-oxide-semiconductor field-effect transistor
MTJ	Magnetic tunnel junction
Nb	Niobium
Ni	Nickel
NDR	Negative Differential Resistance
NMR	Nuclear magnetic resonance
NR	Negative Resist

O	Oxygen
PCM	Phase change material
PPF	Pulsed Pair Facilitation
PR	Photoresist
Q	Charge
RAM	Random-access memory
RCA	Resistive crossbar array
RIE	Reactive ion etching
RNN	Recurrent neural network
rpm	Revolutions per minute
RRAM	Resistive random-access memory
SCCM	Standard Cubic Centimeter per Minute
SEM	Scanning electron microscopy
Si	Silicon
SIMS	Secondary ion mass spectroscopy
SNN	Spiking neural network

STDP	Spike-timing dependent plasticity
STT	Spin-transfer torque
T_c	Critical temperature
TE	Top Electrode
TFET	Tunnel field-effect transistor
Ti	Titanium
ToF-SIMS	Time-of-flight secondary ion mass spectroscopy
V	Voltage
XANES	X-ray absorption near edge structure
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

SUMMARY

It is estimated that humans created 2.5 quintillion bytes of data every day in 2020 which is predicted to go up to 463 exabytes per day by 2025 [1]. Meanwhile, data centers around the world are projected to use >20% of total energy produced globally by 2025 while spending 50% of this power in cooling infrastructure. Under the circumstances, brain-inspired neuromorphic computing has emerged as a crucial field in addressing this increased need for collection, analysis and decision making from high volumes of dynamic unstructured data at low power consumption. Memristive devices are a key enabling technology for developing large scale neuromorphic computing platforms. Lithium niobite (Li_xNbO_2) is an adaptive suboxide which has shown promise in developing volatile and non-volatile memristors for highly scalable and low-power neuromorphic circuitry. This thesis aims to develop a hardware platform using intercalation based Li_xNbO_2 memristors to implement scalable neuromorphic architectures with high energy-efficiency and co-localized processing and main memory, thus overcoming the memory wall.

CHAPTER 1 focuses on the motivation for neuromorphic computing including the need for non-von Neumann architectures for the next generation of computing hardware and the emergence of the human brain as a model for energy-efficient computation. CHAPTER 2 introduces memristors as a promising path for designing bottom-up neuromorphic platforms and surveys the field of memristive technologies. In addition, lithium niobite, the material of focus in this dissertation, is introduced and its advantage over contemporary memristor implementations is discussed. CHAPTER 3

delves into the detailed study of the lithium niobite material system: a metal-oxide semiconductor that employs lithium-ion motion as the key agent for enabling tunable resistivity (memristivity). CHAPTER 4 focuses on the development of nonvolatile lithium niobite memristors and probes the origin of memory in these devices. CHAPTER 5 details the systematic study of the frequency response of nonvolatile lithium niobite memristors to highlight the temporal flexibility inherent to this memristor technology. CHAPTER 6 investigates the underlying conduction mechanisms in nonvolatile lithium niobite memristors via the current-voltage response in these devices and highlights linear analog programming in these devices with flexibility in programming voltage. CHAPTER 7 summarizes and concludes this dissertation along with a perspective on the future directions for the implementation of neuromorphic platforms using developed lithium niobite memristive technology. The culmination of this work has demonstrated a memristive technology that implements all major functions of a neural network: analog training, linear resistive changes, temporal tuning, varied temporal response and adaptive activation, with each efficiently implemented in hardware.

CHAPTER 1. INTRODUCTION

1.1 Need for Beyond-CMOS Computing

The continued miniaturization of the complementary metal-oxide semiconductor (CMOS) technology has served as the backbone of sustained progress in computing, communication, and data processing since the early 1970s. This is demonstrated by the fact that the first integrated circuits in 1960 had ~10 transistors [2], while complex silicon chips of recent years surpass 10 billion transistors [3], radically transforming the daily operations of end-users and enterprises alike. Despite these incredible achievements in functionality, however, conventional computing has made limited progress in certain basic tasks that biological systems have mastered, such as speech and image recognition, dynamic learning and adaptive problem solving.

The geometrical scaling of transistors via sophisticated fabrication processes, as predicted by Moore's law [4] in 1965 and guided by Dennard scaling [5] rules, enabled an exponential rise in on-chip device integration density and clock frequency with a reduction in power consumption/dissipation per device. In the twenty-first century, geometric (dimension) scaling also incorporated equivalent scaling of transistors using strain, [6] high-κ/metal-gate stack [7] and non-planar fin field-effect transistors (FinFETs) [8] to continue the doubling of transistor count every two years.

More recently, however, it has become apparent that this device scaling trend and its associated performance improvements are not self-sustaining as the semiconductor manufacturing industry grapples with fundamental challenges of excessive subthreshold

leakage current and increased device power dissipation, along with soaring manufacturing costs at sub-10 nm technology nodes [9]. At smaller device dimensions and increased device density, subthreshold leakage current has begun to dominate power consumption at lower technology nodes [10]. Power delivery and dissipation limits have also emerged a key constraint in microprocessor design, limiting clock speeds and memory density. On an architectural level, conventional von-Neumann computing is bound by the processor-memory performance gap that has grown steadily over the last several decades resulting in memory latency becoming an overwhelming bottleneck in computer performance and limiting multi-core parallelism [11][12][13].

These challenges faced by conventional computing systems are exacerbated by (i) modern applications which are increasingly data-centric, generating and processing gigabytes of data [14]; and (ii) a juncture where the world is adapting to rely increasingly on semiconductor-powered technology to work, educate, communicate, entertain, diagnose, and do various other tasks remotely. This unique scenario necessitates the development of novel approaches in computing to keep pushing the boundaries of developing increasingly capable computers that excel at data-centric applications [15] while consuming decreasing amounts of energy.

1.1.1 Brain Inspired Computing in the Beyond-CMOS era

In the interim, the human brain has set a benchmark for speed and energy efficiency in the domain of interpreting and learning from large amounts of (often noisy) data and solving unfamiliar problems using this dynamic learning. This is demonstrated by the brain's ability to perform ~10^{16} synaptic operations per seconds while operating on

~20W of power [16]. This feat is achieved in the human brain via massive parallelism, low-power event driven temporal interactions between neurons with co-located computation and memory units within the same ionic substructure [17]. The previously discussed challenges in continued transistor scaling and the simultaneous emergence of the human brain as an efficient model for computation have inspired a plethora of research on emerging brain-inspired architectures where computation is executed in-situ within the data storage element by leveraging the ability of memory to implement matrix-vector multiplication.

Brain inspired neuromorphic architectures are aimed at addressing the needs of the beyond-CMOS era by having lower power consumption than conventional processors and being designed to support dynamic learning in the context of complex and unstructured data. In traditional von-Neumann computing systems, the processing unit (CPU) and main memory (DRAM) are physically separated wherein information, encoded in binary strings, is shuttled back and forth as sequential programs are executed, mediated by a central clock [18]. Alternatively, the brain's architecture does not have a central clock, and memory and computation in collocated over circuits of neurons and synapses [18]. These neural circuits integrate synaptic inputs in analog form for efficient temporal computation and produce binary-valued spikes for efficient communication [19][20]. Figure 1 (adapted from [21]) describes the delay time versus power dissipation for devices in contemporary technologies revealing that biological neurons and synapses exist in a region (top left corner) where no other technologies are available. The energy dissipation in a synapse is orders of magnitude smaller than its analogues although the speed is much slower.

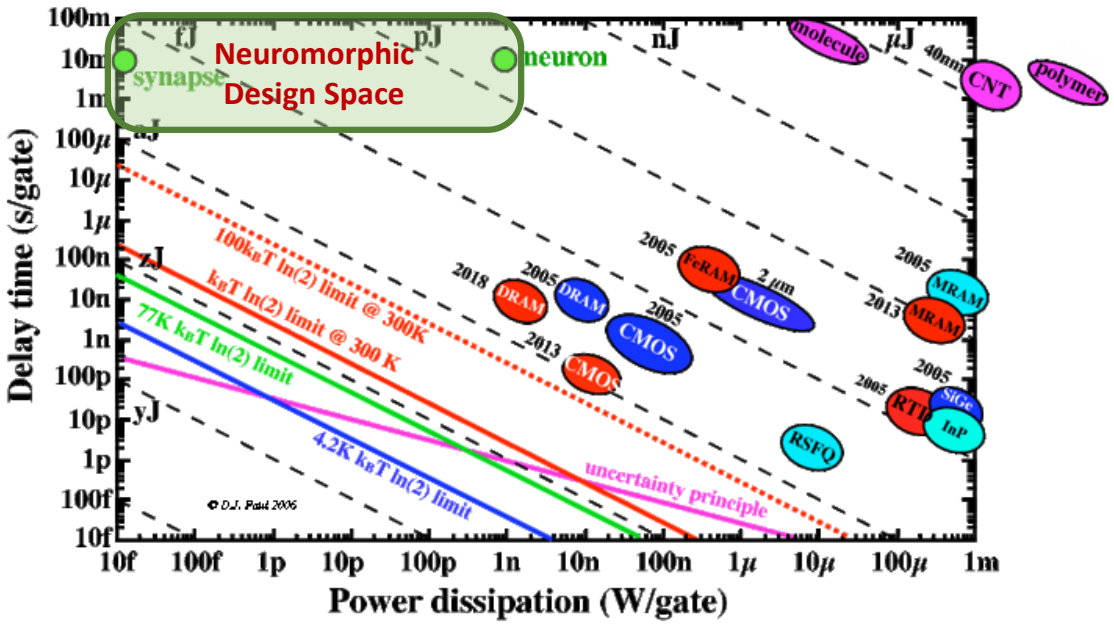


Figure 2-1: Delay time per transistor versus the power dissipation (Adapted from: http://userweb.eng.gla.ac.uk/douglas.paul/SiGe/limits.html)[21]

Characterized by an extensively parallel architecture connecting low-power computing elements (neurons) and adaptive memory elements (synapses), brain-inspired neuromorphic systems are predicted to outperform contemporary processors on tasks involving unstructured data classification or pattern recognition [22]. Neuromorphic computing will also provide an efficient solution for analyzing and processing the vast amounts of data generated by self-driving cars, automatons, and sensor networks within the Internet of Things (IoT).

1.2 Computation in the human brain

Understanding how the human brain performs computation and communication has been an intriguing and intricate problem in neuroscience. Neurons, the fundamental building blocks of the brain are composed of three main structural units:

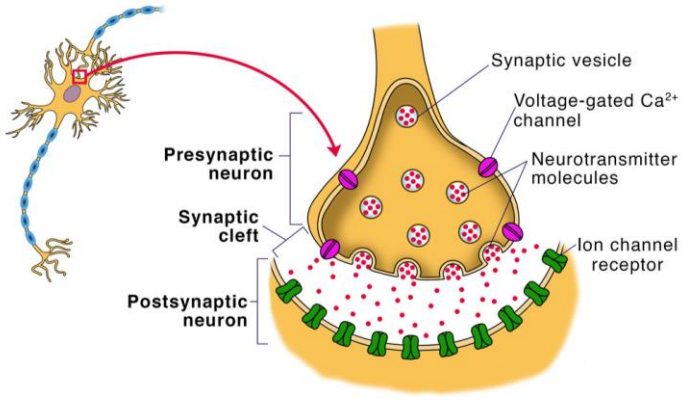


Figure 1-3: Structure of a neuron (left) and a typical chemical synapse (right): adapted from https://www.sciencefacts.net/synapse.html [28]

dendrites which receive the majority of inputs to the neuron, the soma (cell body) which is the site for protein synthesis and the axon which carries signals away from the soma and some information back to it. Neuronal computation [23] operates on timed events called action potentials or spikes via synapses which permits a neuron to pass an electrical/chemical signal to a neighboring neuron by converting spikes into small changes in the cell's membrane potential. The neuron then chemically integrates these changes in potential over time, and, under certain conditions (example: when multiple spikes arrive within a short time) the neuron generates (fires) a spike. Thus, spikes can be considered data (messages) in the computing sense, carrying information in the form of time of generation, magnitude, frequency and waveform shape. These action potentials/spikes and synaptic currents in the brain have considerably smaller magnitudes (10s of mV [24]) than that of electrical signals in von Neumann computers as brain signals are encoded by flow of charge carrying ions (Na^+, K^+, Ca^{2+}) through highly selective ion channels with non-linear conductance properties. The human brain contains about 10^{11} neurons [25] with 5000-10,000 synapses per neuron, showing sparse

connectivity at any instance; however, the total number of connections are of the order of 10^{15}. This distinguishes the brain's computation from conventional computers which have a dramatically lower fan-out connectivity.

Furthermore, computation in the brain is not fixed but can change as a function of activity: a process called 'learning'. Learning is enabled by the ability of synapses to strengthen or weaken over time depending on their activity, a process better known as synaptic plasticity. Fundamental principles for these synaptic changes have been discovered with the best-known method depending on the timing of spikes fired in pre-synaptic and post-synaptic neurons, thus termed spike timing dependent plasticity (STDP) [26]. STDP implements a form of Hebbian learning theory [27] where a synapse is strengthened (potentiation) if the pre-synaptic spike arrives within a certain time window preceding the spike of the post-synaptic neuron; or weakened (depressed) if the pre-synaptic spike arrives outside this time window. The brain's massively parallel, event-driven computation scheme and large-scale connectivity of neurons is likely the basis for its high efficiency in signal processing, inference and control while using less than 20W of power.

1.3 Existing Approaches to Neuromorphic Computing

Neuromorphic computing systems that intend to mimic computation in the brain must be able to implement key neuronal processes including the integrate and fire dynamics of neurons and the spike-triggered communication and plasticity of synapses. The Hodgkin-Huxley model [24] first introduced in 1952 formed the basis for mathematically modeling the initiation and propagation of action potentials in the

neurons. This model incorporates the voltage dependent dynamics of ions and leaky ion channels in the axon to describe the membrane potential and its evolution, thus implementing integrate and fire dynamics in neuromorphic systems.

Research in the field of neuromorphic computing hardware was pioneered by Carver Mead [29] and gained a huge impetus with the demonstration of memristors [30], originally theorized by Leon Chua in 1971 [31]. The primary challenges in designing neuromorphic hardware systems include (i) supporting arbitrary connectivity patterns between spiking neurons, (ii) designing hardware neural units with high fan-out yet sparse connectivity and (iii) mimicking structural plasticity with event/activity driven synaptic connections. Furthermore, these systems must be able to achieve high energy efficiency without compromising on performance or reliability, to leverage the benefits of biological systems. Early artificial implementations of spike-based synaptic plasticity used asynchronous spikes of identical amplitude and duration are referred to as Spiking Neural Networks (SNNs) [32]. In SNNs, just as in the brain, information is encoded into the timing and frequency of spikes. Unfortunately, SNNs require a lot of power as they must continually spike even in the absence of data. The Doolittle group has focused on a more generic Even Driven form of Spiking Network (EDSN) capable of long periods of "quiet" times and intermittent spiking as data arrives and thus capable of low power operation [109]. In addition to SNNs and EDSNs, which are based on the biologically realistic STDP learning rule but lack reliable learning architectures, deep neural networks (DNNs) [33] which are trained using supervised learning and error backpropagation have also achieved success in neuromorphic implementations. This section discusses some notable demonstrations of large-scale neuromorphic hardware platforms using both

CMOS and post CMOS technologies to implement digital or analog artificial neurons and neural networks.

1.3.1 Architectural and System level Design Approaches: (CMOS based)

Mixed analog-digital design and custom microprocessor-based neuromorphic approaches have been used to design event-driven communication frameworks that mimic the interconnectivity of the brain while taking advantage of the speed of digital electronics. This section highlights some of the system-level efforts towards Si CMOS based neuromorphic chips that started with the pioneering work of Carver Mead[25] and has developed for over three decades to be able to integrate over a million digital neurons. [34]

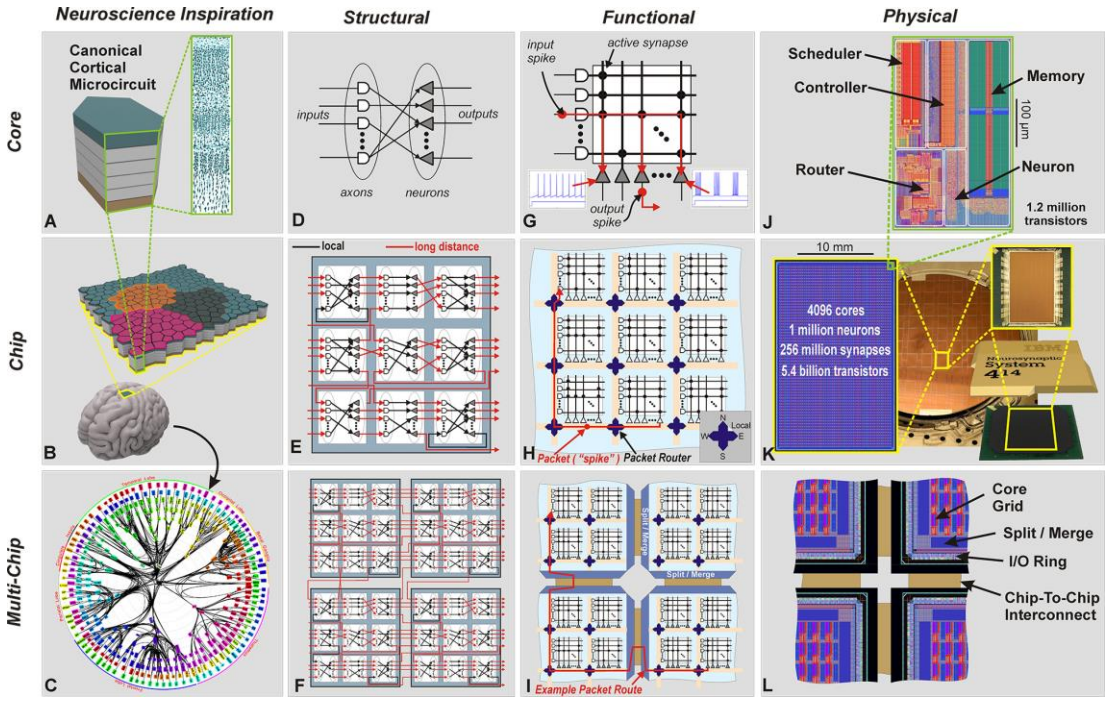


Figure 1-3: Schematic showing the architecture of the CMOS based IBM TrueNorth chip, adapted from DOI: 10.1126/science.1254642 [36]

SpiNNaker [35] was developed by the University of Manchester in 2013 comprising of $>10^6$ ARM9 cores and the ability to simulate a billion neurons in real time, implementing brain-inspired event-driven computation, information localization, high fan-in/fan-out connectivity, and communication with small information packets. In 2014 IBM demonstrated TrueNorth, [36] a million-neuron digital CMOS chip, fabricated using 28nm process technology, as shown in Figure 3. The digital neuron circuits in TrueNorth implement leaky integrate-and-fire dynamics by digital integer accumulation, spike-based communication and are designed to be time multiplexed to emulate the operation of up to 256 neurons, in an effort to be area and power efficient. Intel demonstrated their 14nm FinFET process neuromorphic chip, Loihi in 2018. [37] The multi-core Loihi chip supports the implementation of axonal and synaptic delays via digital delay lines, neuronal spiking threshold adaptation, and programmable synaptic learning rules based on spike timing and reward modulation. The neural cores in Loihi [37] can be programmed to implement neuromorphic learning rules such as pairwise STDP, triplet STDP, reinforcement learning protocols, and other rules that depend on spike rates as well as spike-timing. Spikes are transferred between cores using asynchronous network-on-chip (NoC), allowing on-chip and inter-chip connectivity. Intel recently announced Loihi 2 [34] which supports a maximum of 120 million synapses, built using 2.3 billion transistors in a 31 mm^2 die area, implemented via 7nm technology node.

Dynamic neuromorphic asynchronous processors (DYNAP) are a family of mixed-signal neuromorphic chips from INI Zurich [38]. DYNAP-SE is one such chip fabricated in 180 nm CMOS technology, integrating 1024 neurons and 64k synapses [38]. ODIN [39] is another 28 nm digital neuromorphic chip developed at Catholic University

Louvain in 2019, supporting simple forms of on-chip spike-driven synaptic plasticity (SDSP), demonstrating on-chip learning achieving 84.5% accuracy. Table I summarizes state-of-the-art digital neuromorphic chips and compares their performance metrics.

Despite significant advances discussed above, CMOS implementations of neuromorphic computing must tackle challenges in power consumption and scalability. The Loihi [37] Chips from Intel contain 128 cores per chip and implement ~131,000 neurons using 2×10^9 transistors (15,000 transistors per neuron) implemented using a 14 nm CMOS process. For practical applications, however, this approach is extremely limited in neural density and to scale this up to human intelligence would require a single CMOS chip with an area of ~40 square feet. The primary limitation for scaling of the digital approaches is the need for large circuitry to perform the same functions of small biologic elements. Thus, alongside the achievements of CMOS neuromorphic circuits discussed here, alternative *device-based approaches* [44] mimicking miniaturized neural building blocks is necessary for improved scalability of neuromorphic systems. Among the options for alternative device-based computing elements are the ionic analog devices discussed in later chapters.

Table 1-1: Recent developments in CMOS based Neuromorphic Chips

Neuromorphic Chip	Technology	Integration Density	Performance Metrics/Capabilities
SpiNNaker [35]	ARM968, 130-nm CMOS (next-gen: ARM M4F, 28-nm CMOS)	1,000 neurons/core, 1 million cores	Programmable numerical simulations with 72-bit messages for real-time simulation of spiking networks
Loihi [37]	Digital ASIC at 14-nm CMOS	130,000 neurons, 130 million synapses with variable weight	Supports on-chip learning with plasticity rules, eg: Hebbian, pairwise, and triplet

		resolution (1–9 bits)	STDP, 23.6 pJ per synaptic operation (at nominal operating conditions)
TrueNorth [36]	Digital ASIC at 28-nm CMOS	10^6 neurons, 256 million synapses; 1-bit synaptic state for connection, four programmable 9-bit weights per neuron	SNN emulation without on-chip learning; 26 pJ per synaptic operation
BrainScaleS [40]	Mixed-signal wafer-scale system, 180-nm CMOS (next-gen: 65-nm CMOS)	180,000 neurons, 40 million synapses per wafer	10^3–10^4-fold acceleration of spiking network emulations, with hardware-supported synaptic plasticity. Next gen: programmable plasticity
Braindrop [41]	Mixed-signal 28-nm CMOS	4,096 neurons, 64,000 programmable weights (with analog circuits for all-to-all connectivity)	0.38 pJ per synaptic update, implements the single core of a planned million-neuron chip
DYNAP-SE [38]	Mixed-signal 180-nm CMOS	1,024 neurons, 64,000 synapses (12-bit content-addressable memory)	Hybrid analog/digital circuits for emulating synapse and neuron dynamics, 17 pJ per synaptic operation
ODIN [39]	Digital ASIC at 28-nm CMOS	256 neurons, 64,000 synapses with 3-bit weight and 1 bit to encode learning	12.7 pJ per synaptic operation, implements on-chip spike-driven plasticity
ROLLS [42]	Mixed Signal 180 nm CMOS 1P6M process	256 neurons, 128,000 synapses	STP synapses, LTP synapses and I&F silicon neurons.
Neurogrid [43]	Mixed Signal 180 nm CMOS	256 x 256 neurons per core, 16 cores; 13-bit shared synapses	Cost effective shared dendrite architecture, 1 million single compartment neurons or 100,000 ten-compartment neurons

1.3.2 Memristor based approach to Neuromorphic Hardware Design

Though traditionally neuromorphic circuits were fabricated using MOSFETs, innovation in material science and development of novel electronic device structures has led to beyond CMOS implementations of neuromorphic systems that overcome the limitations introduced in the last section. Beyond CMOS implementations of neuromorphic hardware are driven by a new class of emerging nanoscale devices: memristors [30][31], which act as synaptic analogues and signal propagation elements, thus being well suited for developing computing substrates for Spiking Neural Networks (SNNs) [45]. In these memristive devices, information is stored in their resistance or conductance states and computing is performed by modifying these conductance values. Since neuromorphic systems integrate memory and computation in parallel, a large variety of memristors have evolved from memory devices and memory cells. The major types of memristive devices are phase-change memory (PCM) [45][46][47][48], metal–oxide-based resistive RAM (ReRAM) [49][50][51], conductive bridge RAM (CBRAM) [52][53][54][68], spin-transfer-torque magnetic RAM (STT-MRAM) [55][56][57], and intercalation/diffusion [58][59][60] driven memristors. The resistance state of these memristors is altered by the application of electrical pulses through various physical mechanisms, such as phase transition [45][46][47][48], ionic drift [59][60], and spintronic effects [55][56]. Chapter 2 discusses some notable efforts and progress in memristor based neuromorphic computing implementation and compares these efforts to non-memristor based neuromorphic computing platforms.

CHAPTER 2. MEMRISTOR BASED NEUROMORPHIC COMPUTING

The field of neuromorphic computing is built on the unique ability of the mammalian brain to execute high-level cognitive tasks including abstraction, generalization, prediction, decision making, recognition, and navigation in a dynamic environment at the extremely low power consumption of ~20 W [16]. Unlike the Boolean nature of CMOS-based computing, learning in the brain is implemented via the ability of synapses to reconfigure the strength by which they connect neurons, commonly known as "synaptic plasticity" [23][26], allowing for multiple states in a single synapse. The primary reasons learning at low power consumption is feasible in the brain is because (i) information exchange and processing are event driven; thus, energy is consumed only when and where it is needed; (ii) neurons and synapses are co-located within the same, highly interconnected neural network, where each neuron is connected to other 10^4 neurons, on the average [23]. Neuron/synapse co-location means that data processing, consisting of synaptic excitation and neuron firing, and memory, consisting of the synaptic weight and the neuron threshold, share the same location within the brain. Thus, neuromorphic implementations of synaptic analogs must be guided by plasticity effects and in-memory computation, which is missing from CMOS implementations discussed in Chapter 1.

Novel circuit elements have thus been proposed and investigated to reduce this disparity in energy efficiency between traditional computing and the brain's computing paradigm. One such promising candidate is the memristor (portmanteau of "memory and

"resistor"), a fundamental electronic element that directly relates electrical charge to flux. The memristor was first conceptualized by Leon O. Chua in 1971 [31] via the mathematical equation $d\phi = Mdq$, connecting the flux ϕ and the charge q. Although it was later understood that prior demonstrations existed but were not recognized, in 2008, Hewlett-Packard researchers presented the first memristor devices based on a titanium dioxide insulator layer sandwiched between two metal electrodes [30]. Compared to CMOS transistors, the memristor exhibits an I-V hysteresis [69], which makes it possible to change conductance states gradually, similar to the biological synaptic weight. Since the first report, there have been several innovative electronic technologies and attempts to implement the memristor with various material systems. Memristors are particularly suitable for serving as synapses in neuromorphic computing architectures because of their intrinsic dynamics, analog behavior, nonvolatility, high speed, viability of low power operation, high density, and remarkable scalability compared to CMOS implementation of neural networks [44]. The ability of the device dynamics of memristors to directly assist the computing function enables a less hierarchical and more interconnected computing architecture. Therefore, there is a constructive research effort to design such interconnected memristive systems with the potential to efficiently solve complex problems where the material system itself can contribute towards solving part of the problem. Chapter 2 discusses some notable memristor technologies and introduces the lithium niobite memristor that is investigated further in this dissertation.

2.1.1 Switching type Resistive Random Access Memory (ReRAM):

A ReRAM device consists of a metal-insulator-metal stack where a thin insulating oxide material serves as the switching layer [44], as described in Figure 2-1. The device is initiated by a preliminary electrical stimulus (forming) applied to the top electrode (TE) which causes a soft breakdown in the oxide (insulator), leading to the creation of a high conductivity path containing oxygen vacancies or metallic impurities, also known as a conductive filament (CF), within this oxide layer. This results in the change of the resistance of the device from the initial high resistance state (HRS) to a low resistance state (LRS). Upon forming, the application of negative and positive voltage pulses at TE leads the device to experience reset and set transitions, respectively. The application of a negative pulse causes the rupture of CF (reset), leading to the formation of a depleted gap via drift/diffusion migration of ion defects from bottom electrode (BE)

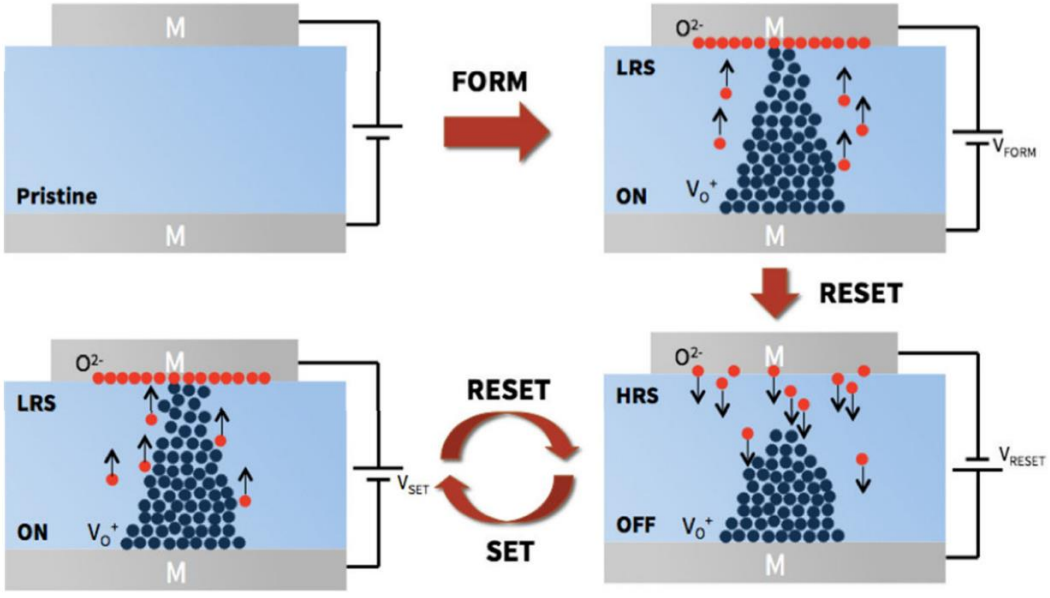


Figure 2-1: Schematic of ReRAM operation where blue region represents insulating metal oxide and grey regions denote conducting metal electrodes. Adapted from [70].

to TE, pushing the device to HRS. On the other hand, the application of a positive pulse allows the gap to be filled via field-driven migration of ion defects from TE to BE, thus leading the device back to LRS (set process). Typical switching oxides in RRAMs include HfO_x [45][61][63], TiO_x, [62] TaO_x, [51][64] WO_x, [65] SiO_x [66] etc. Intel has demonstrated TaO_x RRAM-based nonvolatile memory embedded into their 22FFL FinFET Technology node for mobile and RF applications [67]. Conductive-bridge random access memory (CBRAM) also operates on a similar principle where metallic CFs are created/disrupted between active Cu/Ag electrodes [53].

2.1.2 Phase Change Memory (PCM):

Phase change material (PCM) memristors rely on chalcogenide materials such as $Ge_2Sb_2Te_5$(GST) [54][71] as the switching layer. In these devices resistance switching arises from an atomic configuration (phase) change within the active layer from the crystalline to the amorphous phase and vice-versa via application of unipolar voltage pulses at the top electrode [44] as represented in Figure 2-2. As a voltage higher than that needed to induce the melting process within the active layer is applied across the cell, local melting takes place within the chalcogenide material leading the device to HRS because of the pinning of the Fermi level at the mid-gap. On the contrary, if the applied voltage is below the melting voltage a gradual crystallization process is triggered via local Joule heating leading the PCM device to enter the LRS. Compared to RRAM, PCM offers a higher resistance window ranging from 100 to 1000 [44], however, it is challenging to implement analog states in PCM devices. In addition to GST, other materials that have been investigated for PCM memristors include GeSb [72], Ge-Cu-Te [73][44], and N-doped GST [44][74]. Intel and Micron have developed 3D X-Point

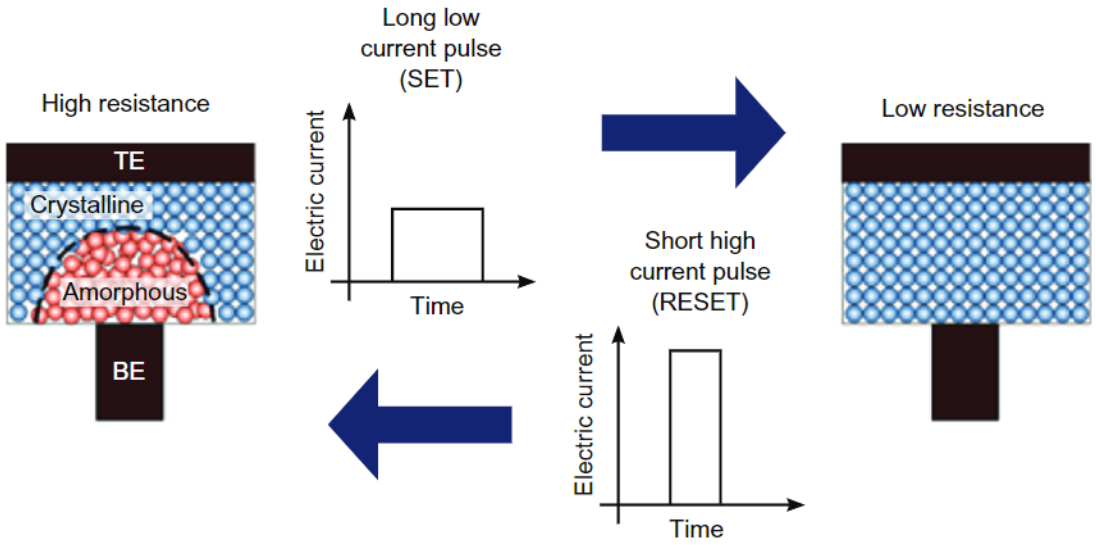


Figure 2-2: Operation principle of PCM consisting of a layer of phase-change material sandwiched between a top electrode (TE) and a narrower bottom electrode (BE). Adapted from [75]

memory which uses PCM devices as non-volatile memory cells with 20nm CMOS enabling 91.4% memory efficiency as an alternative to traditional flash memory. [76]

2.1.3 Spin based Memristors

Spin based memristors utilize the magnetic hysteresis of ferromagnetic materials under an applied magnetic field to switch between resistance states. These memristors demonstrate low energy consumption with high precision and fast switching. The spin-transfer torque (STT) effect driven STT-MRAM device operates using a magnetic tunnel junction with an ultrathin tunneling layer located between two ferromagnetic metal electrodes, named the pinned layer (PL) and free layer (FL) respectively [44]. Unlike the majority of memristor technologies which achieve multilevel operation, STT-MRAM allows only two states to be stored because of the tunnel magnetoresistance effect [77]. The two resistance states in STT-MRAM are

encoded in the relative orientation between PL magnetic polarization, which is fixed, and FL magnetic polarization, which is free to change via the spin-transfer torque mechanism [78][79]. A positive bias at the at top electrode causes the transition of the polarization orientation from anti-parallel to parallel and pushes the device to its LRS. A negative bias alternatively causes the transition from the parallel to anti-parallel state, pushing the device from LRS to HRS. STT-MRAM devices have shown very high cycling endurance [80][81] as well as fast switching speed [82], making them a suitable candidate to replace traditional SRAM in CMOS chips. Similarly, adding ferroelectric tunnel junctions that switch due to spontaneous electric polarization induced by an applied electric field are also under investigation for neuromorphic computing systems. Some ferroelectric materials used in STTRAM include doped HfO_2 [83] or perovskite compounds. [84]

2.1.4 Synaptic Transistors

Three terminal memristor configurations have also been demonstrated where a third terminal acts as an electrolytic gate for controlled electrochemical doping via ion intercalation [85] which in turn controls channel resistance, mostly notably in the electrochemical RAM (ECRAM) demonstrated by IBM [86] as shown in Figure 2-3 or the IGZO based synaptic transistor by Wang et al [87]. Ionic synaptic transistors have been demonstrated where the control terminal is used to control the ion concentration in a channel, typically Li^+ or H^+ which in turn controls the electrochemistry or band structure of the channel and hence conductivity [58][88]. Highly linear conductance change is achievable in this class of memristive devices, albeit at reduced resistance ranges, with decoupling of read and write paths. Ferroelectric field effect transistors consisting of a MOS structure with FE material as gate dielectric have been shown to exhibit voltage

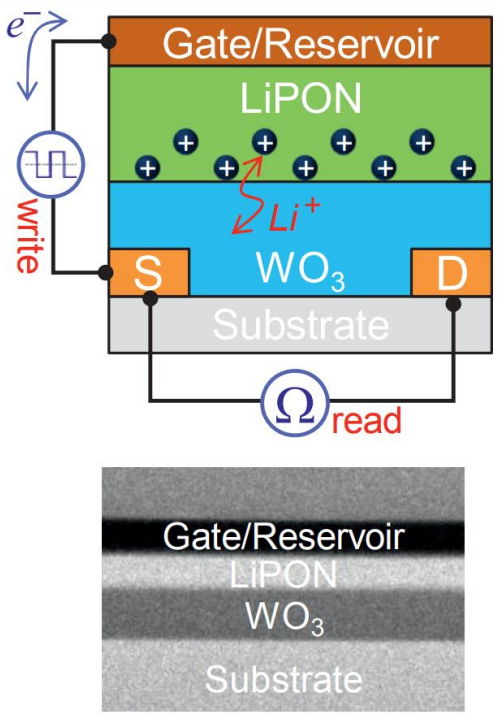


Figure 2-3: ECRAM device schematic (top) and cross-sectional TEM image (bottom). Adapted from [86].

controlled analog operation by Halter et al. using a HZO ($Hf_{0.57}Zr_{0.43}O_2$) layer [89] and by Kaneko et al. using a PZT ($Pb(Zr,Ti)O_3$) layer [90]. In these devices, the gate terminal receives external pulses that cause a non-volatile polarization switching in the FE dielectric. As a result, the threshold of the transistor changes, along with the conductivity of the channel, which can be measured by reading the current at the drain terminal.

In addition to the memristor technologies discussed above, optoelectronic memristors have also been demonstrated where reversible resistance switching is controlled by the polarization [91] or wavelength [92] of incident light via electro-optical interactions.

As compared to CMOS based neural circuits, memristor based neural implementation offers improved size scalability [93], fast switching (faster than 100 ps),

[49] and low energy per operation [49]. The tunable resistance states in memristors can be used both to store information and to perform computation, allowing computing and memory to be truly integrated in a highly parallel architecture. Compute-in-memory (CIM) accelerators have been demonstrated using ReRAM, [94] PCM [95] and FeFET [96] technologies on silicon. However, limitations in memristive neural network implementations arise from device non-idealities [97] in conductance response of memristors such as write non-linearity, asymmetry, and stochasticity, more commonly in ReRAM and PCM devices [98].

2.2 Lithium Niobite based Memristors

The rest of this dissertation focuses on the study of a specific class of analog memristors using lithium niobite ($LiNbO_2$) as the active material. Chapter 3 introduces the $LiNbO_2$ material system, and the following chapters focus on the development of non-volatile memristors using $LiNbO_2$ thin films. Lithium niobite ($LiNbO_2$) is a minimally studied suboxide of the common optical and acoustic material [99] lithium niobate ($LiNbO_3$), having a layered structure with planes of lithium ions separating sheets of metal oxide [100][102], similar to the crystal structure of common battery cathode materials such as $LiCoO_2$ [101]. $LiNbO_2$ possesses a pliable electronic structure [102] with tunable electrical and optical properties due to changes in the band structure as lithium is moved within the crystal or removed from the crystal (delithiation) [102]. This effect of loosely bound [103] lithium-ion motion in modifying the local occupancy of states also leads to memristive behavior [104][105] in bulk $LiNbO_2$ material. Early research on the fundamental properties of $LiNbO_2$ have shown that most material and electrical properties of lithium niobite are dependent on the lithium content including

crystalline lattice parameters [106], superconductivity transition temperature [107], optical bandgap and optical transition type (direct/indirect) [115] and resistivity [106]. More recently, volatile [104] and non-volatile [60] memristors have been demonstrated using $LiNbO_2$ and the origin of resistive switching has been shown to depend on the field-induced degenerate p-type doping of the delithiated $LiNbO_2$ crystal [108]. Zivasatienraj et al. have demonstrated $LiNbO_2$ based memristor operation at programming voltages down to 150 mV [60], thus establishing this technology as a strong candidate for ultra-low power neuromorphic hardware platforms with true analog resistance tuning. The device dynamics of $LiNbO_2$ memristors were later modeled by Zivasatienraj [109] to implement a self-training neural network architecture that allows the neural weights to self-update according to the temporal relationship between inputs and system-wide responses and avoid the need for the computationally expensive process of backpropagation and individual memristor manipulation. Such all-memristive networks were shown to seamlessly relearn different handwritten characters in succession from an EMNIST dataset, paving the way for lifelong self-learning, with generic signal agnosticism [109].

CHAPTER 3. LITHIUM NIOBITE

Lithium niobite ($LiNbO_2$) is a Li-intercalated layered suboxide of lithium niobate ($LiNbO_3$), first reported in 1974 by Meyer and Hoppe [110]. The crystal structure of $LiNbO_2$ shown in Figure 3-1 [111][112][114] consists of trigonal-prismatic niobium oxide layers separated by a layer of loosely bound Li atoms in a Li – O octahedral layer. This layered trigonal-prismatic configuration is stabilized mainly by overlapping Nb – Nb and Nb – O bonding orbitals that arise from the ligand-field splitting, whereas Li is completely ionized in Li – O bonds with negligibly overlapping orbitals [112][113]. At stoichiometric Li concentration, computational analysis predicts that the Nb and O states dominate in contributing to the density of states and intermix near the 2-eV band gap and form narrow energy bands just below the fermi level [112][115]. Geselbracht et. al.

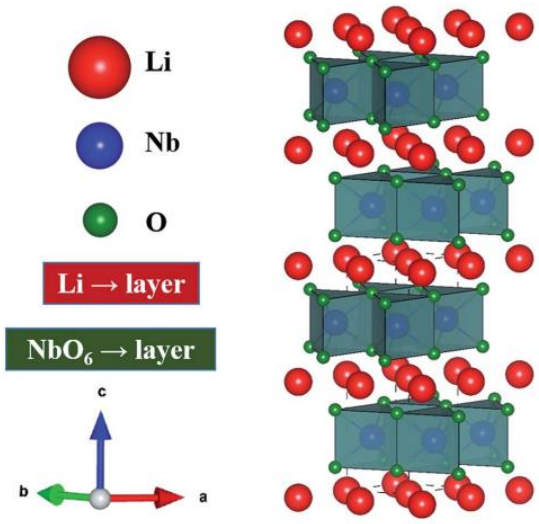


Figure 3-1: Schematic crystal structure of $LiNbO_2$ with layers of trigonal prismatic NbO_6 separated by sheets of mobile Li-ions. Adapted from [111].

[103][107] performed optical absorption spectroscopy observing an absorption onset at ~2eV, , and Shank [102] found photoluminescence with ~2 eV photon energy, solidifying the hypothesis of Kumada et. al. [106] that $LiNbO_2$ is a semiconductor. Given the extremely low binding energy (~ 300 meV) [103][105] of ionized Li^+ in the $LiNbO_2$ lattice, (i) Li ions can acts as mobile charge carriers at room temperature and (ii) Li ions are easy to delithiate leading to a non-stoichiometric Li_xNbO_2 system ($0.5 < x < 1$).

The broad investigation of Li deintercalation in layered Li-bearing compounds for battery applications led to the discovery of nonstoichiometric Li_xNbO_2 ($0.5 < x < 1$) via chemical delithiation in 1988 [116]. Since then, researchers have linked multiple material characteristics to the Li content of Li_xNbO_2 ($0.5 < x < 1$). Moshopoulou et al. [117] later reported the degree of delithiation of Li_xNbO_2 using aqueous chemical solutions as shown in Table 3-1.

Table 3-1: Degree of delithiation of $LiNbO_2$ from chemical treatment. Adapted from [117]

Aqueous Solution	Concentration of Solution	Duration (days)	*x* in $Li_{1-x}NbO_2$
H_2O		14	0.11
HCl	37%	14	0.31
HCl	3% (1 N)	14	0.21
HCl	3% (1 N)	43	0.28
HBr	40%	14	0.12
HNO_3	60%	14	0.16
H_2SO_4	95%	14	0.27
H_3PO_4	85%	14	0.06

Li concentration in the Li_xNbO_2 system dictates several material properties including thermal conductivity. An ideal stoichiometric $LiNbO_2$ single crystal is predicted to have a thermal conductivity as high as 31 $Wm^{-1}K^{-1}$ [119]. However, studies have shown that delithiation leads to a 40-70% reduction in the thermal conductivity as well as Seebeck coefficient of Li_xNbO_2 [118][119][111]. Delithiated $Li_{0.5}NbO_2$ has also been investigated for superconducting properties and was shown to be superconducting below T_c = 5.5K [115][120].

It thus becomes very important to understand the effect of delithiation on the band structure of Li_xNbO_2 to be able to design electronic devices using this material system. The first attempt at the electronic band structure calculation of Li_xNbO_2 by Novikov et. al. [115] indicated that the band structure must theoretically transition from a direct

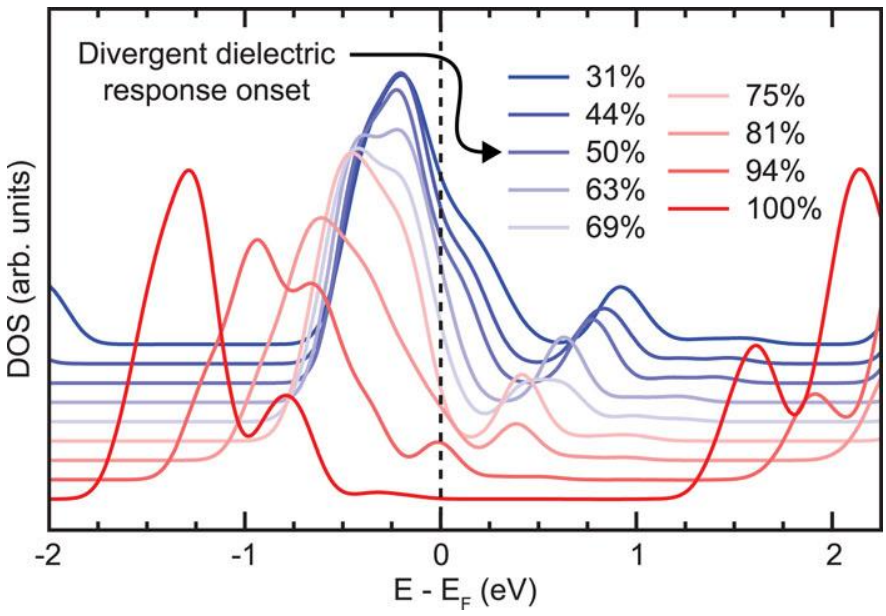


Figure 3-2: Evolution of the density of states as a function of *x* in Li_xNbO_2 showing continuously increasing hole population with decreasing Li, with onset of metallicity below *x* = 50%. Adapted from [108]

bandgap material (at x = 1) to an indirect bandgap material upon delithiation down to x = 0.5, with the Fermi level lying within the valence band with ionized Li^+ species donating electrons to fill the valence band. Howard et al. [108] later used first principal calculations to show that as lithium is removed from the Li_xNbO_2 system, there is an autodoping effect with the top of the valence band becoming heavily p-doped, with onset of metallicity around 50% delithiation, as shown in Figure 3-2. Rahman et al. [111] measured the temperature dependent electrical conductivities for Li_xNbO_2 confirming the increasing trend of electrical conductivity with increasing degree of delithiation (decreasing value of x). This ability to tune the film resistivity with Li concentration makes Li_xNbO_2 a promising candidate for implementing memristive devices. Greenlee et al. [122] used in situ O K-edge x-ray absorption spectroscopy (NEXAFS) to show that the memristive mechanism in analog $LiNbO_2$ memristors is attributed to the movement of lithium, which has a concentration gradient under external bias.

3.1 Memristive behavior in $LiNbO_2$

The unique lattice configuration of lithium niobite ($LiNbO_2$) allows lithium ions to intercalate through the Li_xNbO_2 thin film at room temperature, as observed by time-of-flight secondary ion mass spectroscopy (ToF-SIMS) [121], nuclear magnetic resonance (NMR) [103][107], and in situ near edge x-ray absorption fine structure spectroscopy (EXAFS) [108][122]. This property has also been observed in other lithium transition metal oxides such as lithium cobalt oxide ($LiCoO_2$), commonly used in batteries. As Li+ ions are removed from (or redistributed within) the Li_xNbO_2 system via external stimulus such as electrical or optical or even chemical delithiation, Li vacancies are generated that degenerately p-dope Li_xNbO_2, in turn changing the electrical conductivity (via doping) of

the system, demonstrating memristive behavior [108][122]. Since the source of conductivity tuning is Li concentration modulation, Li_xNbO_2 memristors are analog in nature, with a continuum of resistive states, which is tuned via intercalation-induced band structure re-arrangements [108]. These memristors being inherently non-binary (analog) can enable true bio-mimetic synaptic weight updating, and can be controlled via electrical, chemical, or optical stimulus, offering operational flexibility uncommon or nonexistent in other memristive platforms discussed thus far. Moreover, Li_xNbO_2 memristors can be energy efficient due to the low activation energy of Li ion motion in Li_xNbO_2 [103][105]. Prof. William Alan Doolittle's research team at the Georgia Institute of Technology first reported the memristive behavior in Li_xNbO_2 in 2012 [123][124]. These memristors were fabricated on Molecular Beam Epitaxy (MBE) deposited $LiNbO_2$ films and showed a continuously changing resistance response to a sinusoidal input [123]. Sputter deposited $LiNbO_2$ films were later used to design non-volatile memristors via Li-ion intercalation into a metal electrode [60][121]. Zivasatienraj [60] et al. also showed the ability to use device fabrication to design volatile (short-term plasticity), semi-volatile (medium-term plasticity) and non-volatile (long-term plasticity) memristors on Li_xNbO_2 thin-films, thus demonstrating the temporal flexibility necessary for bio-mimetic computation [125].

3.2 Deposition of Lithium Niobite (Li_xNbO_2) thin films

Various deposition approaches have been studied for the synthesis of device quality Li_xNbO_2 thin films. Liquid phase electro-epitaxy (LPEE) has been reported as a viable method to achieve high quality single-crystal Li_xNbO_2 ideal for material characterization studies [108][127]. However there has been limited success in depositing

Li_xNbO_2 thin films using LPEE, and device fabrication on small flakes from grown crystal is inconsistent due to the lack of a planar film, resulting in high device variation and surface roughness. High quality thin films of Li_xNbO_2 have also been grown and studied using molecular beam epitaxy (MBE) by a heavily modified Varian GEN II system [60][114][123][124]. A chloride-based growth chemistry is employed for this purpose, with $NbCl_5$ and Li as solid sources in an O_2 environment [114][123]. The major challenge of MBE-grown Li_xNbO_2 thin films is the deposition of single phase-$LiNbO_2$ due to the presence of unwanted lithium niobium oxide phases adjacent to the optimized growth regime, controlled by a multitude of intercoupled growth parameters [126]. The complexity of single phase Li_xNbO_2 thin film deposition compounded with the low growth rate (~85nm/hr.) makes MBE grown Li_xNbO_2 material suffer from low yield issues and unsuitable for device studies. Thus, all Li_xNbO_2 films and devices studied in this dissertation are obtained via room-temperature sputter deposition.

A modified-Denton Discovery 2 Sputter System was set up for the dual-sputtering of lithium niobium oxides with Li_2O and Nb targets in a reactive Oxygen (O_2) and Argon (Ar) environment [128]. The nonuniform sputter yield (preferential sputtering of Li) due to matrix effect [129] in pressed $LiNbO_2$ powder targets necessitates the use of co-sputtering of Li and Nb species with control over individual flux/deposition rates via power supplied to each sputter gun. The optimal deposition parameters for sputter deposition of single phase $LiNbO_2$ thin films continues to be a topic of research and may vary with device geometry. Shank et al. [128] demonstrated the sputter deposition of Li_xNbO_2 thin films achieved by utilizing a Li_2O target power of 200 W and Nb target power of 50 W, with chamber pressure of 1 mTorr during deposition in an Ar ambient of

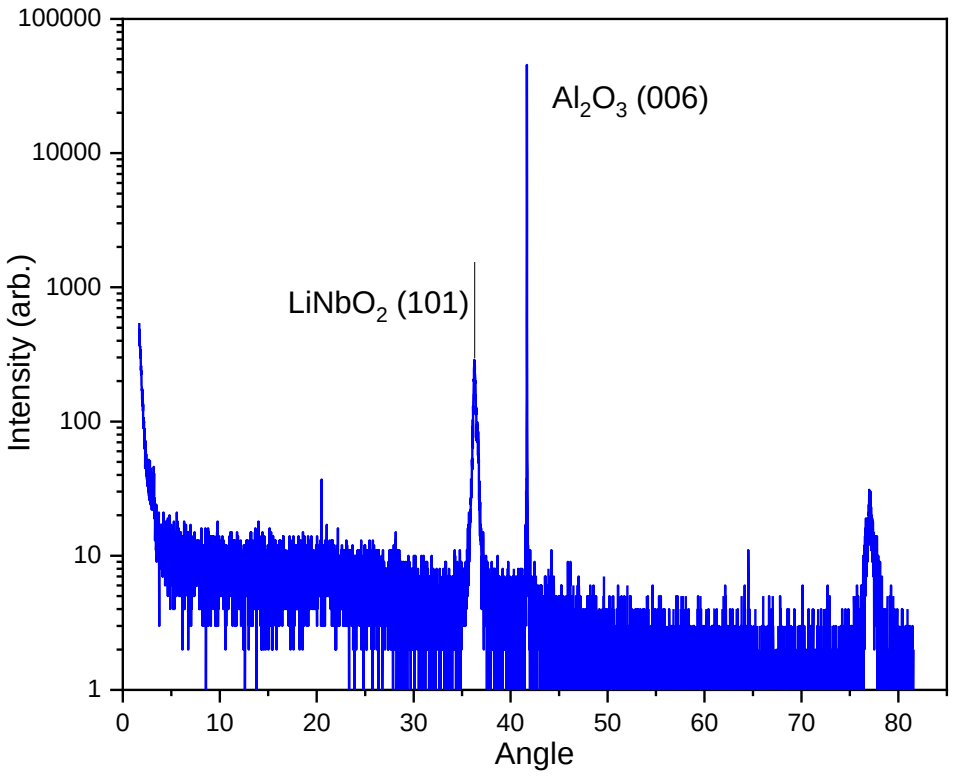


Figure 3-3: Symmetric x-ray diffractogram of the (101)-oriented Li_xNbO_2 thin-film sputter deposited in an Ar ambient with 200 W Li_2O and 50 W Nb source powers.

5 sccm. These deposition parameters resulted in a (101) oriented Li_xNbO_2 film as shown in X-Ray diffraction (XRD) scan in Figure 3-3 that was reactive to atmosphere, with the formation of an opaque film upon exposure post-deposition. This presumed surface Li_2O oxide was easily rinsed off with DI-water and did not hinder device fabrication. Further exposure to atmosphere did not lead to significant surface oxidation. A reactive deposition condition was also studied for Li_xNbO_2 thin films sputter deposited in a mixed O_2 and Ar ambient. Thin films deposited using reactive O_2 showed (101) oriented $LiNbO_2$ in XRD with smoother surfaces and marked improvement to metal-adhesion during device fabrication. X-Ray photoelectron spectroscopy (XPS) (Figure 3-4) of reactively sputtered Li_xNbO_2 thin films deposited at 100 W Li_2O power and 83 W Nb

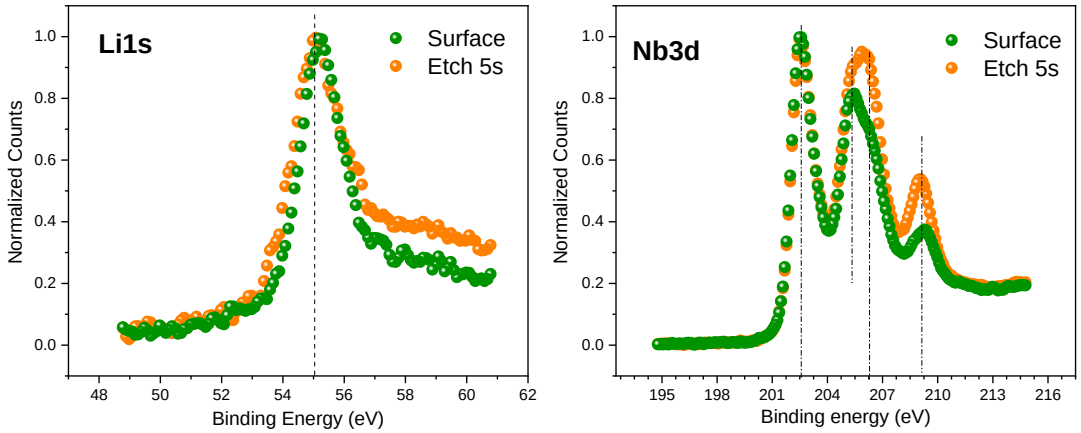


Figure 3-4: XPS Li1s (left) and Nb3d (right) spectra of reactive sputter deposited Li_xNbO_2 films at 100 W Li_2O power and 83 W Nb source power under 0.5 sccm O_2 flow.

source power in 0.5 sccm O_2 flow and 4.5 sccm Ar flow showed the presence of Li1s peak at ~55 eV and the presence of at least two sets of Nb doublets (oxidation states): a low energy doublet at ~202.8 eV and a high energy doublet at ~206.5 eV. These films showed less reactivity to air with no observed surface oxidation, in contrast to the films deposited without O_2 flow. Thin-films sputter deposited via both nonreactive (Ar only) and reactive (Ar + O_2) conditions have been successfully used to fabricate and test memristive devices.

3.3 Microfabrication of Li_xNbO_2 memristors

A standard photolithographic lift-off technique is used to define the mesa isolation for Li_xNbO_2 device structures on a sapphire substrate. The fabrication procedure, as shown in Figure 3-5, begins by spin-coating negative resist NR9 and patterning on a clean sapphire substrate via i-line photolithography on a maskless aligner. The first lithography step defines the mesa features for devices of varying dimensions and this patterned substrate is then loaded into the Denton Discovery 2 sputter-camber for

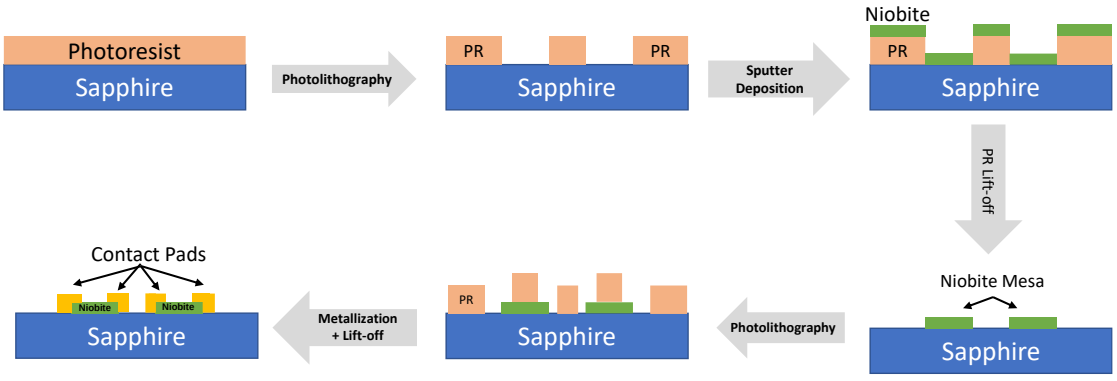


Figure 3-5: Schematic representation of fabrication procedure for the deposition of mesa isolated Li_xNbO_2. A lift-off photolithographic process using negative resist helps define device mesa and contact metallization area.

deposition of Li_xNbO_2 thin film. Post film deposition, two separate lift-off lithographic steps are used to define the contact metal electrode area, and an e-beam evaporator is used for metallization. A plasma descum is used at the end of each lithography develop step which was found to help metal adhesion but does likely oxidize the surface. Device deposition using the lift-off process for sputter deposited Li_xNbO_2 is found to be consistent and extremely convenient for a streamlined fabrication process. Figure 3-6 shows an optical microscope image of Li_xNbO_2 memristors that were isolated using the sputtered lift-off technique. Mesa features sizes down to 2 μm have been consistently fabricated and tested successfully.

3.4 Li_xNbO_2 based volatile and non-volatile memristors

Greenlee et al. first presented the development of lateral two-terminal Li_xNbO_2 memristors in ring-dot geometry with relatively large gaps (> 50 μm) between the electrodes [124][104][123]. These memristors used nickel (Ni) metal electrodes, which are known to have Li-blocking properties. In these devices, an external electric

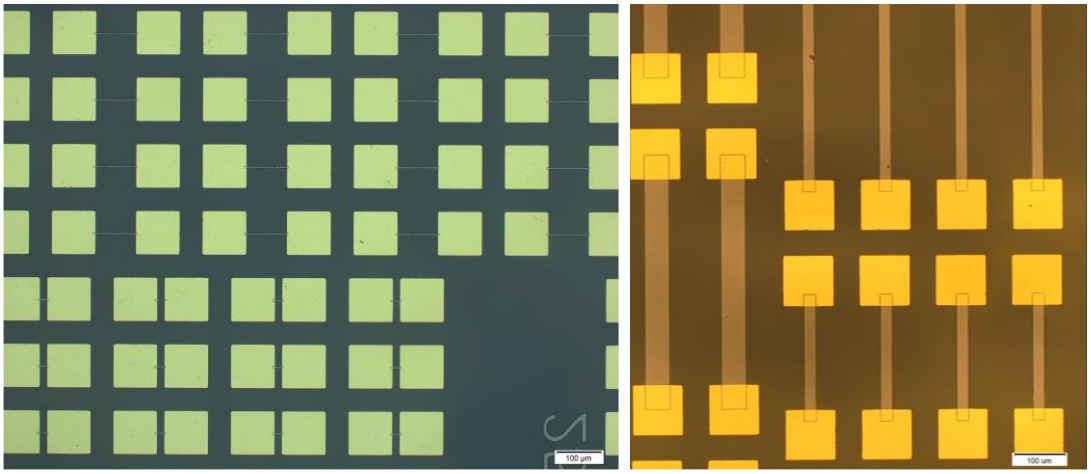


Figure 3-6: Optical microscope images of mesa isolated devices down to 5 µm x 25 µm fabricated via lift-off photolithography.

field redistributes the Li^+ ions inside the Li_xNbO_2 channel leading to the introduction and redistribution of p-dopant Li vacancies inside the channel leading to a hysteretic memristive response [127]. This volatility of conductivity changes was attributed to the Li-blocking nature of the contact metal such as Ni or titanium (Ti). These electrodes confine lithium within the metal oxide (Li_xNbO_2), allowing for Li diffusion and the restoration of a uniform Li distribution when the applied voltage stimulus is removed [130]. To introduce non-volatility in Li_xNbO_2 memristors, the contact metal must be able to intercalate Li ions without changing phase or forming an alloy at room temperature or temperatures attained during operation, to preserve the purely electric field driven device operation. Chapter 4 delves into the study of such Li-soluble contact electrode selection for designing non-volatile Li_xNbO_2 memristors.

CHAPTER 4. CONTACT ELECTRODE METAL DESIGN FOR LITHIUM NIOBITE MEMRISTORS

All devices presented here are fabricated on Li_xNbO_2 films deposited via sputtering on sapphire substrates using the Denton Discovery tool described in Chapter 3 and fabricated at the Marcus Inorganic Cleanroom facility at Georgia Tech.

4.1 $LiNbO_2$ based non-volatile memristor

The source of resistance modulation in $LiNbO_2$ memristors lies in a combination of ionic drift and diffusion of Li^+ ions inside the Li_xNbO_2 channel ($0.5 < x < 1$) in the presence of an external electric field [108]. However, $LiNbO_2$ memristors are inherently volatile as diffusion relaxes the non-uniform Li^+ ion distribution once the incident electric field is removed [130]. For practical applications of memristors in neuromorphic circuits, however, both volatile behavior and non-volatile behavior become necessary. Hence to be able to induce non-volatility in $LiNbO_2$ memristors, a Li absorbing contact electrode is used to intercalate Li+ out of the Li_xNbO_2 layer and store it inside the electrode to create a permanent change in the device resistance. Some candidate metals for designing the Li absorbing metal electrode in these memristors based on electrochemical potential, solubility limits, and alloy phases include aluminum (Al), magnesium (Mg), silver (Ag), tin (Sn), lead (Pb), gold (Au), platinum (Pt), cadmium (Cd) and zinc (Zn). It is thus important to understand the physics behind non-volatility in $LiNbO_2$ memristors and optimize this active electrode to achieve reliable non-volatile programming in $LiNbO_2$ memristors with significant resistance change.

4.1.1 Impact of contact electrode on non-volatility in $LiNbO_2$ memristors

To understand the impact of contact electrode on non-volatility in $LiNbO_2$ memristors, we fabricated devices on sputter deposited $LiNbO_2$ thin films with one lithium blocking Ti electrode and varied the second electrode metal to compare lithium absorbing Al, Ag and Cr metals, as shown in Figure 4-1. A control device with both Ti electrodes was also fabricated and tested. The device dimensions (500 µm x 50 µm) used in this study are rather large compared to traditional nm sized memristors and µm sized $LiNbO_2$ memristors that showed 2000+% programming [60] but the large size was needed to enable accurate SIMS chemical analysis used in later sections. A ~100nm gold

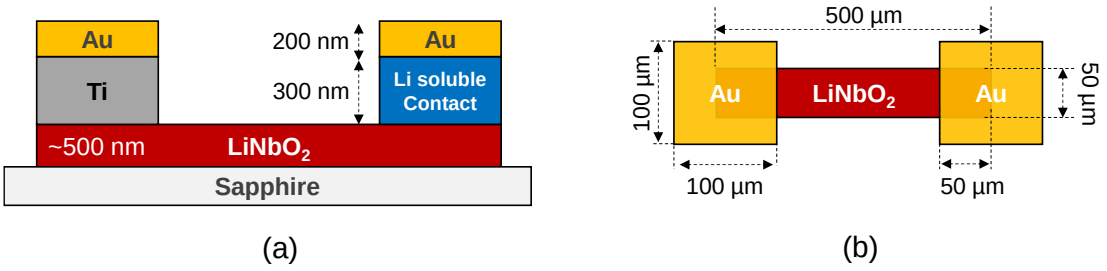


Figure 4-1: Illustration of (a) cross-section and (b) top-down view of $LiNbO_2$ based memristors with effective device area of (400 µm × 50 µm) with different contact metal electrodes. Adapted from [121].

(Au) layer is deposited on top of all electrodes to prevent oxidation of contact metal over time. These 500 µm x 50 µm devices were then programmed and deprogrammed using 20 voltage pulses to saturate ionic motion within the device and obtain stable resistance states. The devices are then compared on their resistance change (ΔR/R), retention time and required electric field for programming.

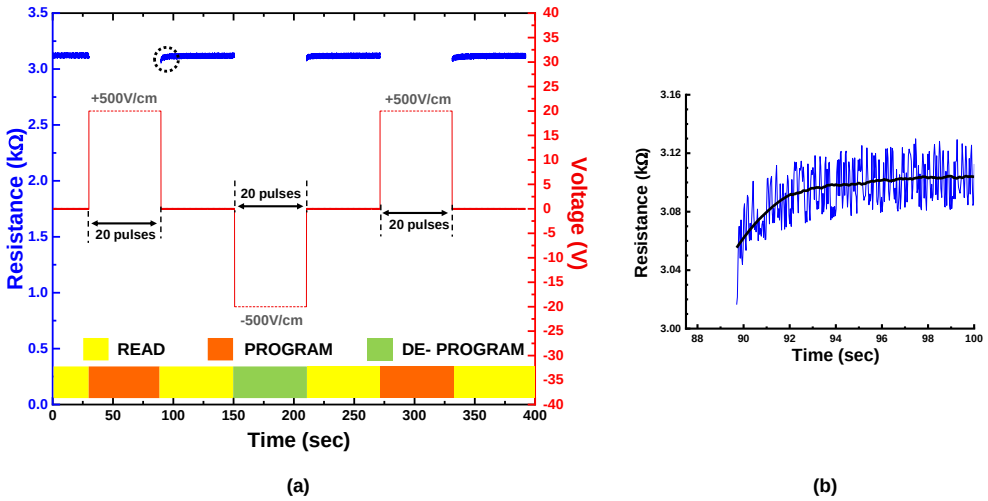


Figure 4-2: (a) Resistance plot for a volatile $LiNbO_2$ memristor with Ti contact metal showing no change in resistance for programming or de-programming cycles. (b) Magnified view of encircled region after programming cycle shows volatile behavior. Adapted from [121].

The control device is a volatile $LiNbO_2$ memristor with two Li-blocking Ti/Au contact electrodes and does not show any change in resistance with positive or negative voltage pulses as shown in Figure 4-2 (a). Figure 4-2 (b) zooms into the resistance state post programming pulses and demonstrates an initial lowered device resistance which quickly relaxes back to its pre-programming resistance state once the electric field is removed. Such volatile $LiNbO_2$ memristors can be used to implement short-term plasticity in neuromorphic circuits, with the ability to tune the timescale of relaxation by scaling the length of the oxide channel.

The non-volatile $LiNbO_2$ memristors with Al, Ag and Cr contact electrodes are first programmed (orange) with an electric field pushing Li+ into the Li absorbing electrode and then de-programmed (green) by having an electric field in the reverse direction pull Li+ from the contact metal back into the channel (Figure 4-3). The devices are then re-

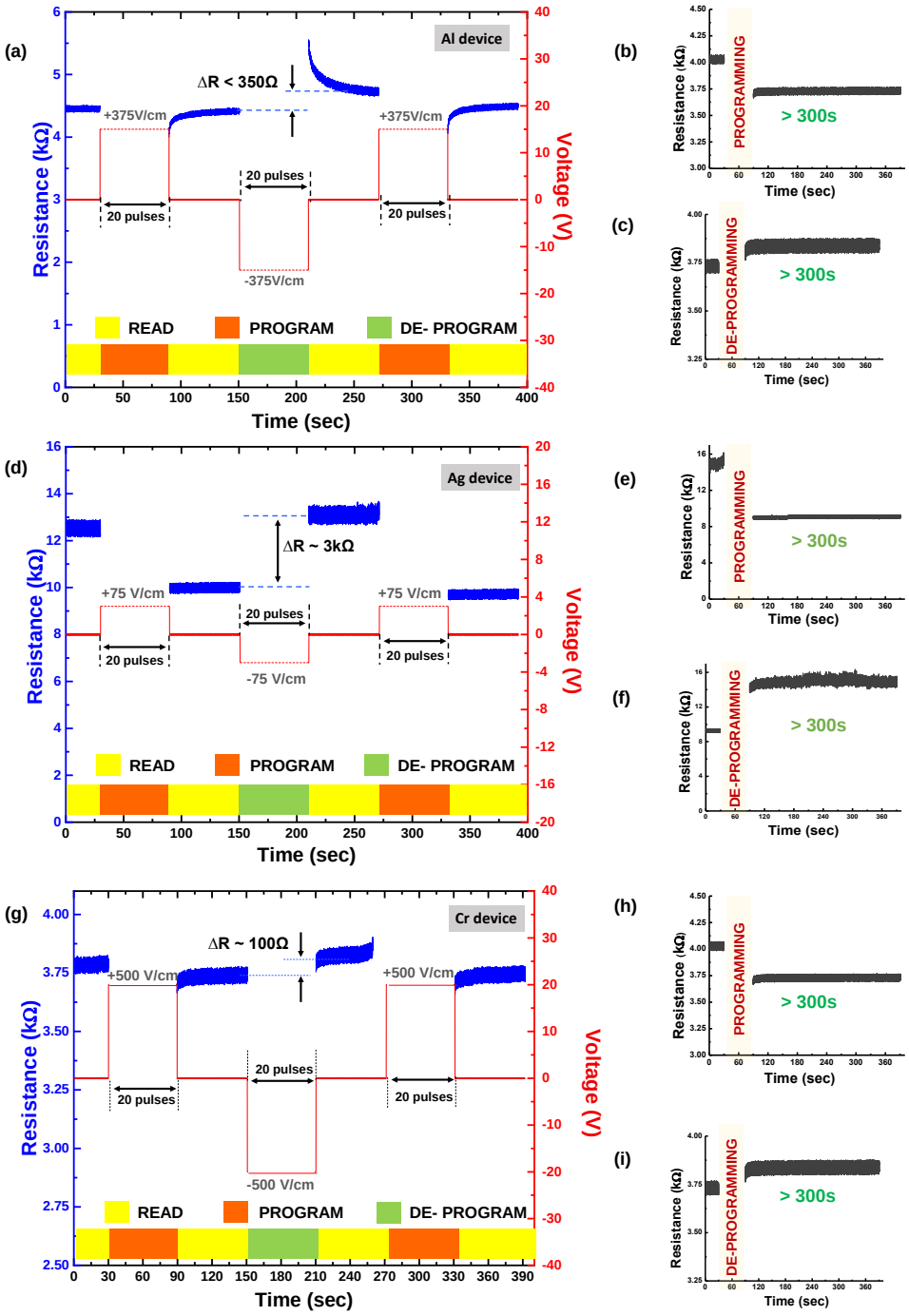


Figure 4-3: Resistance response to programming and de-programming of (a) Al electrode memristor with state retention after (b) programming and (c) de-programming; and similarly for (d-f) Ag electrode memristor and (g-i) Cr electrode memristor. Adapted from [121].

programmed into their low resistance state to validate repeatability. Both programmed (low) and de-programmed (high) resistance states are tested for retention in the order of 5

minutes. $LiNbO_2$ memristors with Al/Au non-volatile contact demonstrate an increase in resistance of ~350Ω in a 4.5kΩ device for a biasing electric field of 375 V cm^{-1} which increases to ~500 Ω for a biasing field of 500 V cm^{-1} across the device (Figure 4-3 (a)). In these devices upon application of a program/de-program pulse, the device resistance achieves an initial value but then relaxes to a stable programmed/de-programmed state. This relaxation is likely a combination of bulk Li diffusion similar to the volatile devices exaggerated by the very large size of these devices (100's of μm) as well as relaxation mechanisms at the Al/$LiNbO_2$ interface. This electrical relaxation response indicates both volatile and non-volatile components exist in $LiNbO_2$ memristors which can be tuned by the contact metal stack to implement desired flexibility in neural plasticity mechanisms in neuromorphic systems. $LiNbO_2$ memristors with Ag/Au as the Li soluble metal stack outperform other devices with a 30% (~3kΩ) change in resistance for a very small bias field of 75 V cm^{-1} which is then reset with the application of electric field in the opposite direction, as described in Figure 4-3 (d). Meanwhile memristors with Cr/Au electrode are least successful at programming with only achieving 100 Ω resistance change at E-fields in the order of 500 Vcm^{-1} (Figure 4-3 (g)). Cr electrodes also suffered from adhesion issues leading to low yield on Cr/Au electrode memristors. All non-volatile memristors show stable retention of high and low resistance states over the measured 5 minutes (Figure 4-3). In comparing the programming response of measured non-volatile devices, we can show successful non-volatile programming in $LiNbO_2$ memristors via Li-absorbing electrode metals and are able to identify Ag as a suitable electrode material for low-power programming. These results can be explained by examining the metallurgy of contact electrode metals when interacting with lithium. The Ag-Li phase diagram [131]

shows that Ag can support ~45% dissolved Li for a broad temperature range without any alloy formation. This would allow reversible intercalation and de-intercalation of Li from the Ag electrode without phase transitions enabling lower programming voltages for device operation with a large resistance window. In contrast, Al [132] and Cr [133] metals can dissolve less than 1% Li, and thus have significantly smaller resistance changes. It has also been shown that Li has a significantly higher diffusion coefficient in Ag ($\sim 10^{-6}$ cm^2s^{-1}) [134] as opposed to Al ($\sim 10^{-9}$ cm^2s^{-1}) [135] which could explain the abrupt change in device resistances for Ag contact metal devices, while Al devices showed some relaxation in the resistance state after programming/de-programming cycles.

Zivasatienraj et al. [60] reported on the low-power operation of developed Ag-electrode non-volatile $LiNbO_2$ memristors down to 150 mV for a 2 µm x 2 µm device, as well as the scaling of minimum required programming voltage with device length, indicating a purely electric field driven device operation. Thus, non-volatile $LiNbO_2$ memristors allow for operational flexibility via geometric scaling, and choice of electrode metal, an advantage few other memristor technologies provide.

4.1.2 Origin of non-volatility in $LiNbO_2$ memristors via SIMS

We have thus far assumed that non-volatility in above $LiNbO_2$ memristors originate from the intercalation of Li into the contact electrode. This is verified using time-of-flight resolved secondary ion mass spectrometry (ToF SIMS), a destructive elemental characterization technique which analyzes secondary ions ejected by controlled sputtering. A Cs ion beam is used for sputtering through the active metal electrode to

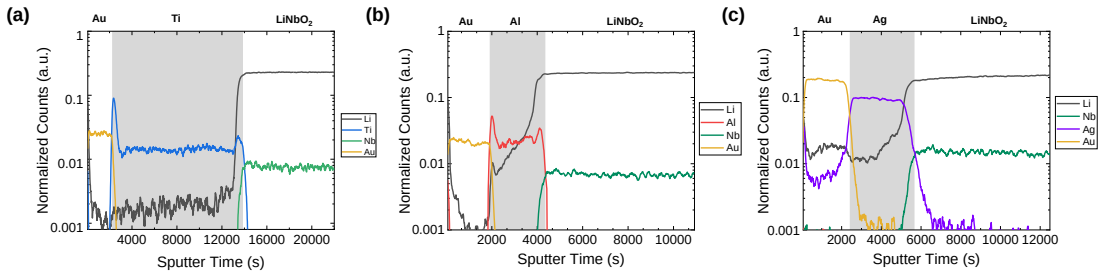


Figure 4-4: SIMS depth profile for (a) Ti/Au, (b) Al/Au pad and (c) Ag/Au pad after programming using Cs ion beam for sputtering. Adapted from [121].

probe the distribution of Li post device programming. SIMS is indeed a powerful tool for qualitatively studying the origin of non-volatile device operation, however, it does come with non-idealities in measurement that must be accounted for during data analysis. Lithium has a very high sputtering yield due to its low mass and low binding energy [136]. SIMS measurements suffer from a matrix-effect wherein elements have varied yield depending on the host material from which they are sputtered, giving rise to surface roughness in the sample causing broadened sampling depths and degraded depth resolution. Hence, the SIMS depth profile presented here must be treated qualitatively for our purposes and the relative intensity of two different elements are not representative of their relative composition. Similarly, the width of the interfaces observed are affected by prior sputter history and thus should be carefully interpreted. Figure 4-4 shows the SIMS depth profile for programmed memristors with (a) Ti, (b) Al and (c) Ag metal contacts respectively where the horizontal axis represents sputter time (and thus depth from Au top layer) and vertical axis shows the distribution of elemental species across the electrode-film interface. The Li signal is shown with a black solid line. Figure 4-4 (a) shows an abrupt interface between the Ti signal (blue) and Li (black), Nb (green) signals validating the lithium blocking nature of the Ti layer. The Li (black) signal in the Al (red)

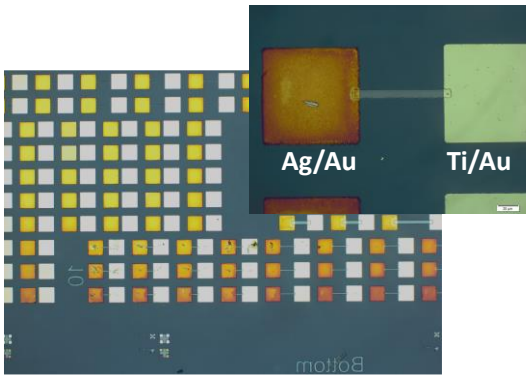


Figure 4-5: Discoloration of Ag/Au electrodes (LHS pads) over six months' time

device in Figure 4-4 (b) extends into the Al metal layer wherein the Nb (green) signal marks the interface between active electrode and $LiNbO_2$ film. In Figure 4-4 (c) the Li (black) signal can be seen to permeate through the entire Ag (purple) layer and into the Au (yellow) top layer which may contribute to the higher resistance change in the programmed device. The Ag signal also extends into the Au layer which indicates intermixing between the metal layers and leading to additional Li distributed into the Au/Ag top contact. Both non-volatile devices probed via SIMS show Li intercalation into the active electrode giving rise to permanent changes in the memristance; however, the qualitative nature of this data means that it cannot be directly correlated to the electrical characteristics of these devices.

4.1.3 Designing stable contact electrodes for non-volatile $LiNbO_2$ memristors

The intermixing of Ag layer and Au layer as seen from the SIMS data in the previous section results in the lack of long-term stability of contact electrodes with Ag/Au stack as shown in Figure 4-5 due to possible oxidation of Ag ions moving to the metal pad surface. A Ti blocking layer was introduced between the Ag and Au layers to

prevent intermixing and design devices with long term stability. Figure 4-6 (a) shows an example current – voltage (I-V) curve of 10 µm x 50 µm $LiNbO_2$ memristor with

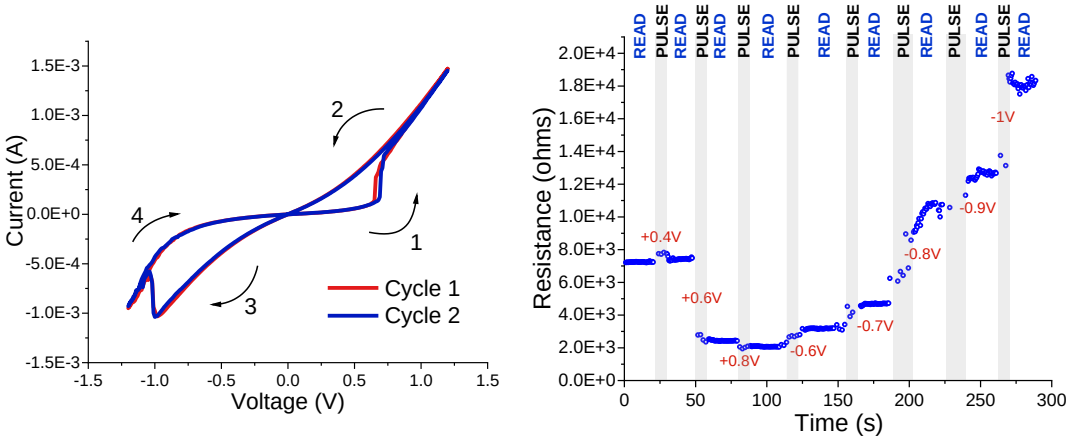


Figure 4-6: (a) Current-voltage response of a 10 µm x 50 µm non-volatile memristor with one Ag/Ti/Au electrode showing hysteresis; and (b) showing incremental programming and de-programming of resistance state between 400mV and 1V voltage pulses. Adapted from [144].

Ag/Ti/Au active electrode illustrating anti-clockwise hysteresis in the first quadrant and clockwise hysteresis response in the third quadrant with analog resistance tuning. In the first quadrant, as the voltage on the Ti electrode is swept positive, the Li+ ions move to the Ag electrode and the device conductivity (and current) increases from "1" to "2", resulting in the anti-clockwise hysteresis response. Similarly, in the third quadrant, as the voltage on the Ti electrode is swept negative, the Li+ ions move back into the channel from the Ag electrode and the device resistance increases from "3" to "4" resulting in a clockwise hysteresis response. Figure 4-6 (b) shows multilevel programming in a 10 µm x 50 µm $LiNbO_2$ memristor at 0.5 sec voltage pulses of varying magnitude between 400 mV and 1 V, demonstrating the ability of $LiNbO_2$ memristors to attain multi-state synaptic weights at a device level.

Chapter 3 introduced the field of $LiNbO_2$ and the efforts to develop memristors using this material system. Chapter 4 demonstrated the introduction non-volatility into the inherently volatile $LiNbO_2$ memristors via electrode chemistry. Chapter 5 focuses on the frequency response of developed non-volatile memristors as a consequence of the Li-intercalation driven memristance behavior substantiated in Chapter 4.

CHAPTER 5. FREQUENCY RESPONSE OF LITHIUM NIOBITE MEMRISTORS

In the last two Chapters we have introduced the design of flux-linkage driven $LiNbO_2$ memristors where the intercalation of Li atoms in and out of the Li_xNbO_2 channel and into a Li-absorbing electrode [121] can tune the device resistance without inducing phase change, enabling low-power device programming down to 100-150 mV [60]. This material system can be used to implement both volatility and non-volatility in memristive devices, where the degree of volatility can be tuned via choice of electrode metal [60][121], making it a flexible engineering platform for bio-realistic learning. These memristive devices are also unique in that the device resistance can be engineered from ~10 Ω to 1E7 Ω by the designer via CMOS-like geometric design rules [60].

Memristors have been conceptualized to exhibit characteristic device responses [137] including (i) a "pinched loop" hysteretic current response under an external voltage sweep, (ii) a dependence of the hysteresis lobe area on the frequency of applied voltage such that the area under hysteretic curve decreases with increasing frequency of excitation, and (iii) the ultimate collapse of hysteretic response to a single-valued function as the frequency of excitation increases to high values. This frequency dependent hysteresis response has also been analytically studied in ion-channel memristors in the human brain, making it critical for designing truly biomimetic systems [138]. Other memristor technologies that have experimentally demonstrated the theorized frequency dependent hysteresis response include ion-conducting Ge_2Se_3 self-directed-channel (SDC) memristors [139][140], GaO_x switching memristors [141], and some

memristor emulator circuits [142]. Meanwhile, TiO_2 based filamentary MIM devices were found to exhibit more complex frequency response to their hysteresis loops due to the convolution of memristive, memcapacitive and meminductive effects [143].

While the frequency-dependent hysteresis response in memristive systems has been observed and theorized, there has been limited evidence of controllability over this frequency behavior. This lack of control has hindered researchers from fully exploiting the potential advantages of the frequency dependence aspect of memristive behavior. However, if the temporal tunability of memristors can be established, it would enable novel approaches to frequency, phase delay, and dynamic computation. For instance, by aligning the input frequency with the response bandwidth of the memristor, circuits operating at specific frequencies could exert varying degrees of impact on neural weights. This opens up possibilities for enhanced manipulation and optimization of neural network functionality. Chapter 5 delves into the experimental observation of tunable frequency/temporal response in non-volatile Li_xNbO_2 memristors in conjunction with large resistance tunability via geometric scaling of devices [144].

5.1 Need for temporal flexibility in memristors

The ability to engineer the frequency dependent response of Li_xNbO_2 memristors via geometric scaling enables a wide array of applications including frequency tunable circuit components, frequency encoded neural network architectures and dynamic training speeds in crossbar-free large-scale networks for lifelong learning [145]. Frequency tunable memristors discussed in this chapter can be used in neural networks extending computation well beyond merely pulsed circuits. For example,

cutting edge recurrent neural networks have been shown to have improved performance when using multiple response time devices providing different time scales for recurrency [146]. Likewise, in implementing STDP based learning, the tunable frequency response can adjust the overlap window for plasticity and can utilize complex stimuli waveforms constructed of multiple Fourier frequency components including those occurring in biology. The tunable frequency characteristic enables designing networks with memristor nodes of varied geometries whose programming (weight changes) can be frequency encoded. Hence, one can selectively train nodes internal to an array as needed by only making one node sensitive to the input.

5.2 Experiment and Results

Non-volatile Li_xNbO_2 memristors of various dimensions with one Li-absorbing Ag/Ti/Au electrode and other Li-blocking Ti/Au electrode were fabricated post sputter deposition of ~140 nm Li_xNbO_2 thin films at 100 W Li_2O power and 83 W Nb target power under 0.5 sccm O_2 and 4.5 sccm Ar flow. Ag has been shown previously to intercalate Li and store it without alloying at room temperature and enable non-volatility in Li_xNbO_2 memristors, as discussed in Chapter 4 [121]. The thin Ti blocking layer between Ag and Au prevents intermixing or alloying of silver and gold which will lead to long term instability in these memristors. The Ag/Li_xNbO_2 interface in these memristors is a square of side equal to the device width (5 μm to 25 μm).

The fabricated memristors of varying dimensions were characterized using a Keithley 4200A-SCS parameter analyzer for large signal current-voltage (I-V) sweeps at variable rates and Agilent 4294A impedance analyzer for small signal impedance

spectroscopy at a frequency range of 40 Hz – 8 MHz. The experimental frequency limits for the 4200A-SCS were verified for each current range by calibrating with a sapphire mounted surface mount resistor ensuring minimal stray parasitics for this modest frequency range. Likewise, cable and probe response were nulled by calibrating the 4294A with a Cascade 101-190 wafer mounted impedance standard.

5.2.1 Large signal electrical characterization of non-volatile $LiNbO_2$ memristors

Figure 5-1 compares the large signal frequency response of the I-V characteristic for lateral memristors of 10 µm width and varying length from 200 µm to 50 µm. The inset of Figure 5-1 shows the probing scheme in lateral $LiNbO_2$ memristors with the positive terminal on the Li-blocking Ti/Au electrode, as the device is excited with a triangular voltage sweep of varying sweep rate (frequency). The voltage sweep range decreases for smaller device lengths for comparable hysteresis due to the electrical-field driven memristor response as reported by Zivasatienraj et al. [60]. In each of these memristors, increasing the sweep rate of the triangular excitation voltage leads to a decrease in the area under the hysteresis loop and ultimately collapses to a non-linear resistor, as theorized in memristors [137]. This stems from the inability of Li ions inside the oxide channel to follow the excitation at higher frequencies and thus there is no change in Li ion concentration in the channel and no resulting resistance change (hysteresis). However, in these Li_xNbO_2 memristors, we observe that the hysteresis closes at lower frequencies in the longer 200 µm device (2.5 KHz) than the 100 µm device (50 KHz) and at highest frequency in the shortest 50 µm memristor (> 312 KHz). For longer devices, the mobile Li ions need to travel farther to intercalate out of the channel, making it harder to follow faster sweep rates. This suggests that the flux-dependent ion-

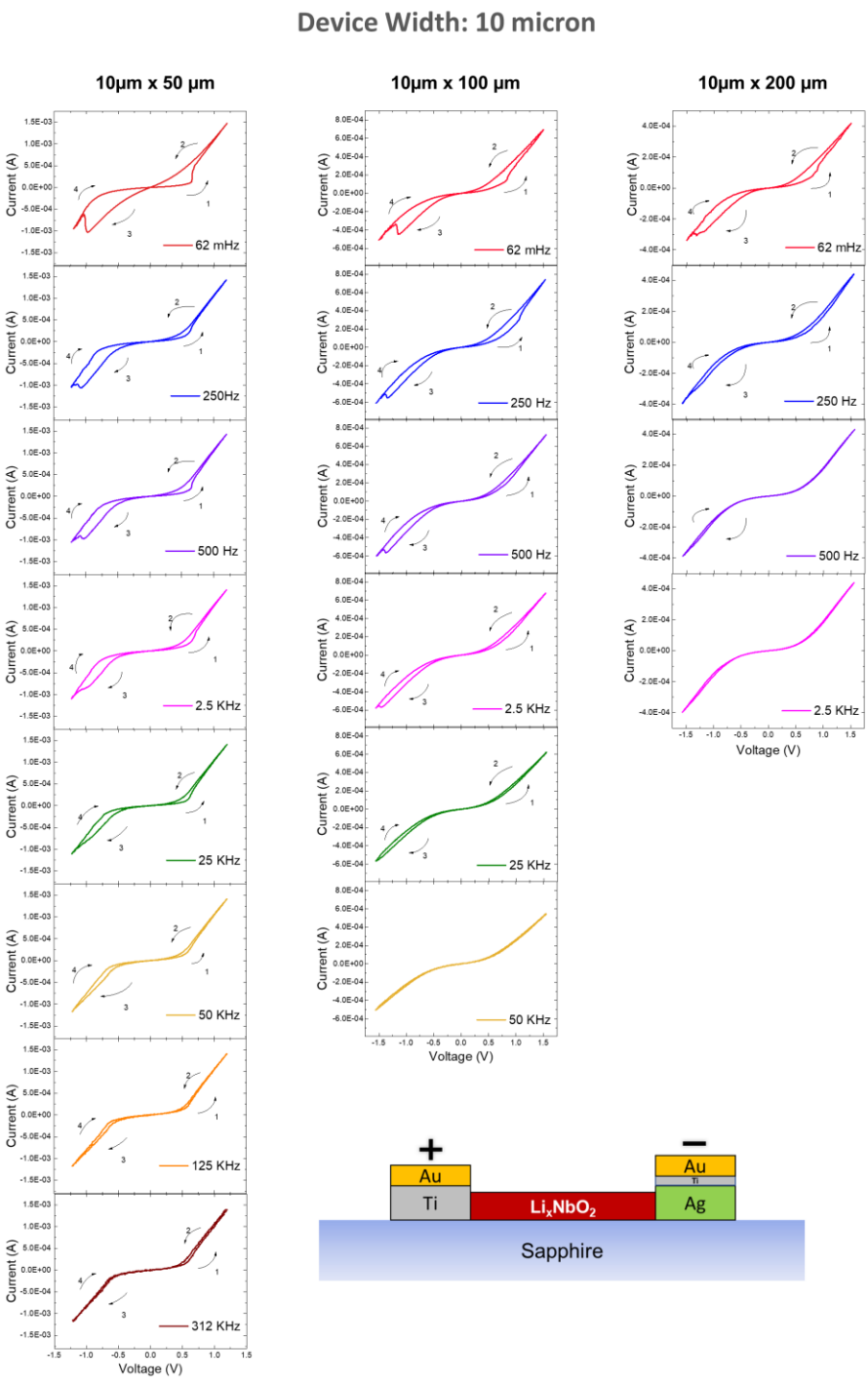


Figure 5-1: I-V sweeps of 10 μm wide Li_xNbO_2 memristors at increasing frequencies show hysteresis feature at low frequencies which disappears at some critical frequency which is in the order of 500 Hz for the 200 μm long device, 50 KHz for the 100 μm long device and > 300 KHz for the 50 μm long device. At frequencies above the critical frequency the I-V response collapses to a non-linear resistor. Adapted from [144].

intercalation based memristive mechanism in Li_xNbO_2 memristors allow the engineering

of the frequency response of the hysteretic I-V performance in these memristors.

We further investigate the device width dependence on the frequency response using three memristors of same aspect ratio (length/width) but shrinking the device width from 25 μm to 10 μm and the smallest 5 μm, as shown in Figure 5-2. The input voltage sweep range is smallest in the 5 μm x 25 μm device and increases with device length since the device hysteresis is dictated by electric field across the Li_xNbO_2 channel. The inset for Figure 5-2 shows the probing scheme in lateral $LiNbO_2$ memristors with the positive terminal on the Li-blocking Ti/Au electrode. For the same aspect ratio, the 5 μm device shows open hysteresis at 312 KHz whereas the hysteresis collapses in the 10 μm device around 312 KHz and 25 μm device around 2.5 KHz. Even at higher sweep rates, for the same aspect ratio a smaller device will see a larger percent volume change in channel Li ion concentration for the same excitation, resulting in larger hysteresis. The measurement system is limited in frequency/sweep rates and as a result the hysteresis collapse in the 5 μm x 25 μm devices is not observed within this frequency range.

As evident from Figure 5-1 and Figure 5-2, one can engineer the frequency range of hysteretic memristive behavior in these Li_xNbO_2 memristors using the device length and/or device width, enabling performance scaling on this platform akin to that on traditional CMOS.

5.2.2 Small signal electrochemical impedance spectroscopy (EIS) of non-volatile $LiNbO_2$ memristors

Electrochemical impedance spectroscopy (EIS) is a non-perturbative characterization technique that uses a small AC signal of variable frequency to probe the

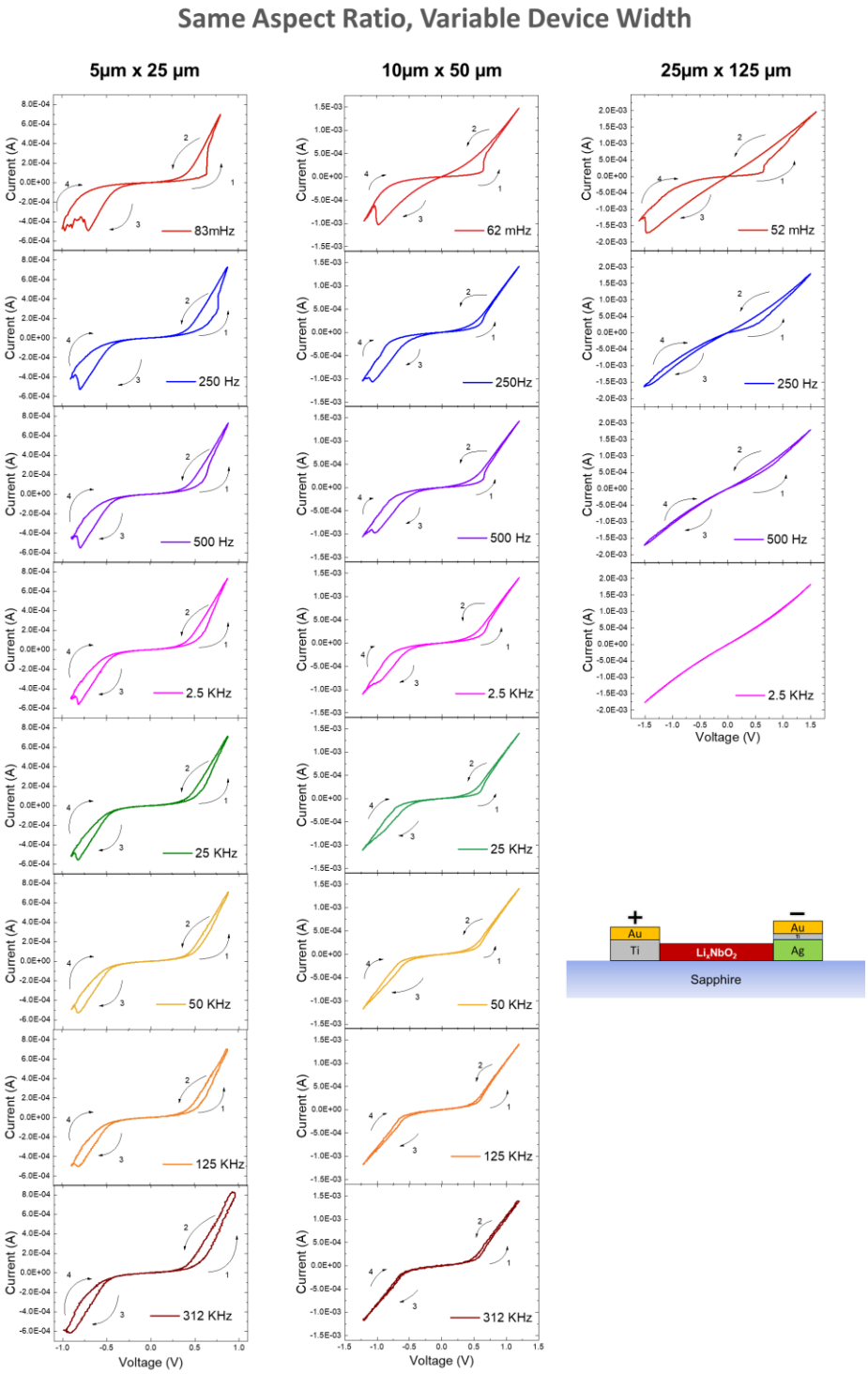


Figure 5-2: I-V sweeps at varying frequencies for Li_xNbO_2 memristors with same aspect ratio but decreasing device area shows hysteresis feature at low frequencies for all devices which disappears at some critical frequency which is in the order of 2.5 KHz for the 25 μm x 125 μm device, ~312 KHz for the 10 μm x 50 μm device and >> 312 KHz for the 5 μm x 25 μm device. Adapted from [144].

dynamics of bound or mobile charged particles in the bulk and interfacial regions of

mixed ionic-electronic conductors [147][148][149].

EIS is used in this dissertation to attempt to decouple the mixed ion-electron programming mechanism in Li_xNbO_2 memristors as both electronic and ionic species respond to low frequencies, however, above some critical frequency, ions can no longer follow the signal and the electronic response of the system can be measured. A 50 mV AC signal in the frequency range of 40 Hz to 8 MHz was employed to measure the complex impedance response of 10 µm wide $LiNbO_2$ memristors with variable device lengths (Figure 5-4 (a)) at incrementally programmed states. The small-signal nature of EIS ensures no programming/resistance change during measurement and is akin to the read signal used in neuromorphic circuits. This measurement technique thus lets us probe

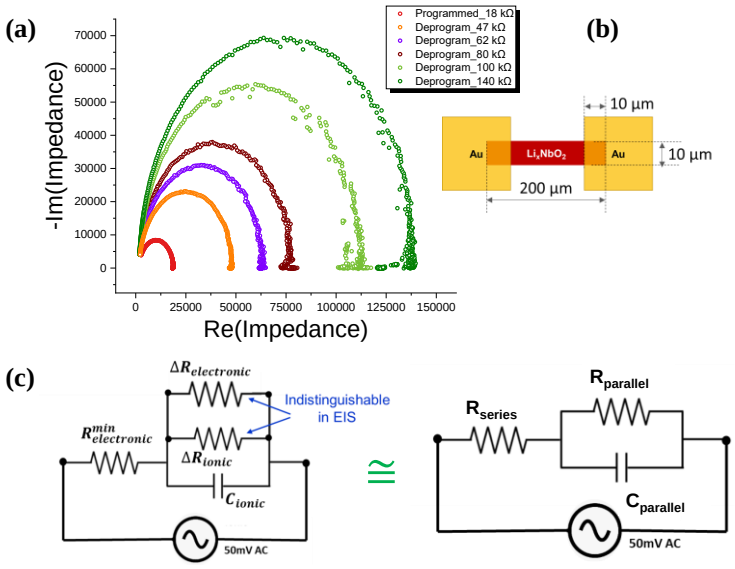
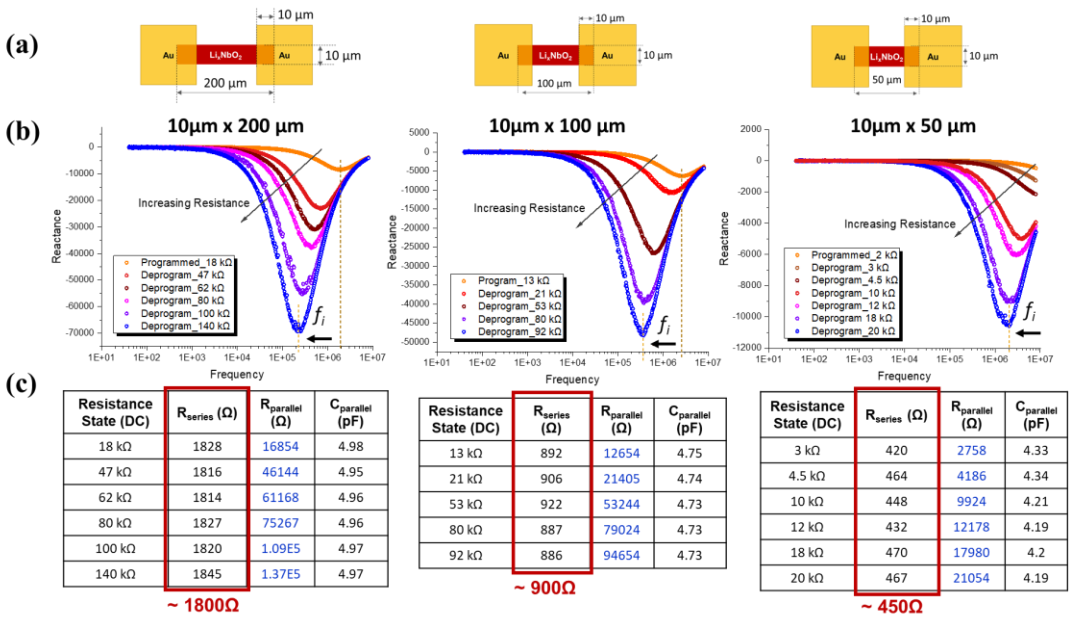


Figure 5-3: (a) Representative semicircular Nyquist plot measured between 40 Hz – 8 MHz for a (b) 10 µm x 200 µm non-volatile Li_xNbO_2 memristor; (c) equivalent Randles circuit with least components to fit measured Nyquist response shows series combination of electronic resistance component (R_{series}) and lumped RC element with parallel combination of capacitive element ($C_{parallel}$) and resistive element ($R_{parallel}$) which couples the change in ionic (ΔR_{ionic}) and electronic ($\Delta R_{electronic}$) resistances due to Li intercalation in/out of Li_xNbO_2 channel. Adapted from [144].



Resistance State (DC)	R_{series} (Ω)	$R_{parallel}$ (Ω)	$C_{parallel}$ (pF)
18 kΩ	1828	16854	4.98
47 kΩ	1816	46144	4.95
62 kΩ	1814	61168	4.96
80 kΩ	1827	75267	4.96
100 kΩ	1820	1.09E5	4.97
140 kΩ	1845	1.37E5	4.97

Resistance State (DC)	R_{series} (Ω)	$R_{parallel}$ (Ω)	$C_{parallel}$ (pF)
13 kΩ	892	12654	4.75
21 kΩ	906	21405	4.74
53 kΩ	922	53244	4.73
80 kΩ	887	79024	4.73
92 kΩ	886	94654	4.73

Resistance State (DC)	R_{series} (Ω)	$R_{parallel}$ (Ω)	$C_{parallel}$ (pF)
3 kΩ	420	2758	4.33
4.5 kΩ	464	4186	4.34
10 kΩ	448	9924	4.21
12 kΩ	432	12178	4.19
18 kΩ	470	17980	4.2
20 kΩ	467	21054	4.19

Figure 5-4: (a) Device schematic of 10 µm wide non-volatile $LiNbO_2$ memristors tested via EIS; (b) Bode plot of 10 µm wide $LiNbO_2$ memristors showing reactance minima (ion relaxation frequency, f_i) decreasing with increased resistance state; (c) Fit parameters for Nyquist plot of 10 µm wide $LiNbO_2$ memristors showing scaling of R_{series} with device length scaling and $R_{parallel}$ dictating incremental resistance tuning with programming in these memristors. Adapted from [144].

the non-volatile device dynamics at its intermediate resistance states. Figure 5-3 shows a typical measured EIS impedance response of a non-volatile Li_xNbO_2 memristor: negative reactance (capacitive) (y-axis) versus resistance (x-axis) with frequency increasing in a counterclockwise manner, for different programing states (shown as separate traces). The low and high frequency endpoints occur at zero reactance indicating the sum of ionic and electronic resistance and purely electronic resistance respectively. In between these endpoints, the ionic current has a phase shift to the excitation resulting in a reactance that peaks in magnitude when the ions are 90 degrees out of phase. The interpretation of this impedance response is discussed in later sections.

Figure 5-4 discusses the impact of device length on this impedance response of Li_xNbO_2 memristors at incrementally programmed resistance states. Figure 5-4 (b) shows the Bode plot for the reactance of 10 µm wide devices with channel length of 200 µm (left), 100 µm (center) and 50 µm (right), with constant interfacial area (10µm x 10µm). Across all Li_xNbO_2 memristors we observe that the frequency corresponding to the reactance minima, known as the ionic relaxation frequency (f_i) shifts to a lower value as the devices are programmed from a lower to a higher resistance state. This ionic relaxation frequency is related to the ionic conductivity (σ_i) via the equation [150][151]:

$$2\pi f_i = \frac{\sigma_i}{\epsilon} \qquad \text{Equation 5-1}$$

where ϵ is the low frequency dielectric constant. The dielectric constant of Li_xNbO_2 is calculated assuming $\epsilon_r \approx 1$ due to the high carrier conductivity and near-metallic nature of non-stoichiometric, degenerately doped lithium niobite. Using Equation 5-1, Figure 5-5

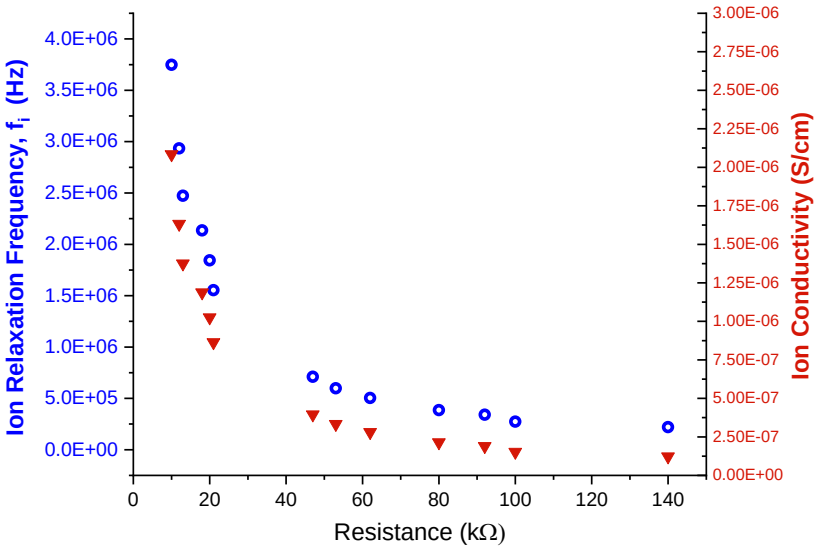


Figure 5-5: Plot showing ion relaxation frequency (blue) measured via EIS and derived ion conductivity (red) changing with resistance tuning in 10 µm wide Li_xNbO_2 memristors. Adapted from [144].

shows the ionic conductivity of 10 μm wide non-volatile memristors with varying channel lengths between 200 μm to 50 μm. By programming these devices, the relaxation frequency and thus, ionic conductivity, can be tuned over an order of magnitude by changing the percent Li ion concentration (x) in the Li_xNbO_2 channel. This is instrumented by the increased availability of ion hopping sites in a de-lithiated channel. Thus, more Li-vacancies in the channel result in a faster device. We note that even for these fairly large channel lengths, the frequency limits of our test equipment, 8 MHz, are reached limiting the number of observed relaxation frequency data available for the smaller devices. Thus, $LiNbO_2$ memristors can be substantially faster than represented here when scaled to nanometer devices. The small-signal EIS further corroborates and quantifies the ability to tune the frequency and temporal response in Li_xNbO_2 memristors by geometric scaling in conjunction with resistance tuning.

The Nyquist plot for these non-volatile $LiNbO_2$ memristors (Figure 5-3 (a)) are represented by a semicircle in the first quadrant with a non-zero resistance (x-axis) intercept at high frequencies, and a low frequency inductive hook, often associated with ionic motion [152]. The Nyquist plots of incrementally programmed memristors are modeled with the minimum required circuit components to decouple the resistive and capacitive components and their evolution with device programming. The equivalent Randles cell circuit [153] of the fit semicircle as shown in Figure 5-3 (c) consists of a series resistance component (R_{series}) which dictates the minimum resistance state of a memristor as extracted from the high-frequency x-intercept in Figure 5-3 (a), and a lumped parallel RC element. The convergence of all programmed states toward the same resistive R_{series} element suggests no ionic contribution to this element of the model which

is observed to scale with device length as shown in Figure 5-4. Hence, this series resistance is concluded to be contributed by resistance of metal pads, contact resistance and the minimum resistance state of the Li_xNbO_2 channel at maximum allowed delithiation (~30-50%) [108][116]. In series with this resistor is a lumped RC element which is a parallel combination of a resistor ($R_{parallel}$) and capacitance component ($C_{parallel}$). Further insight into the origin of these equivalent circuit components is gained via fitting and analyzing the Nyquist response of incrementally programmed scaled non-volatile memristors, as tabulated in Figure 5-4(c).

From Figure 5-4 (c) we observe that the R_{series} component in all measured devices is dictated by the device geometry, can be scaled by the device dimensions using design rules similar to CMOS length-to-width scaling rules, and does not change during programming. From the fitted parameters in Figure 5-4 (c) we also observe that the $R_{parallel}$ component is tuned during programming, indicating that this parallel resistor combines the effect of ionic conduction changes as well as hole conduction changes during programming. The ionic conduction (ΔR_{ionic}) and electronic conduction ($\Delta R_{electronic}$) components are inter-dependent on each other and cannot be decoupled in the EIS measurement. The capacitive component, $C_{parallel}$, is contributed by phase shifts in ionic conduction due to the finite mass of ions.

The small-signal impedance measurements thus corroborate the ability of Li_xNbO_2 memristors to be engineered for desired resistance and temporal/frequency response tuning via device scaling and fabrication.

5.3 Conclusion

In Chapter 5, both large and small signal characterization methods demonstrate the tunable frequency dependent memristive response in Li_xNbO_2 memristors is controlled via device geometry and scaling. In these memristors, device geometry can be used to engineer desired resistances, resistance changes (stronger changes in smaller devices), temporal and frequency responses, a characteristic thus far available only in traditional CMOS platform. Small signal response elucidates higher ion conductivity when deintercalated, due to increased availability of ion hopping sites in Li_xNbO_2 channel. The dynamic range of frequency response can be as high as one decade and the center tuning range increases beyond our measurement capability as device sizes decrease below ~50 μm channel length indicating respectably high-speed operation. Ion motion in these memristors is driven by extremely small voltages and is possible even via light [102]. Given their temporal flexibility, $LiNbO_2$ memristors will be able to emulate synaptic functionality at the device level allowing for input heterogeneity to build robust neuromorphic learning platforms. Lithium niobite ($LiNbO_2$) thus shows more design flexibility than contemporary memristor technologies enabling more biologically realistic circuits.

CHAPTER 6. CHARACTERIZATION OF NON-VOLATILE LITHIUM NIOBITE MEMRISTORS

The current-voltage (I-V) response of non-volatile $LiNbO_2$ memristors was first introduced in Chapter 4 and its tunability with the frequency of applied bias was described in Chapter 5. Chapter 6 focuses on understanding the hysteresis response of these memristors and uses this I-V response to probe underlying operation mechanisms in Li_xNbO_2 memristors. All electrical testing in Chapter 6 is performed on Li_xNbO_2 memristors deposited using the reactive sputter process outlined in Chapter 3 and tested with the positive terminal on the Li blocking Ti/Au electrode and the negative terminal on the Li-absorbing Ag/Ti/Au terminal.

6.1 Observation of "Burn-in" phenomenon in as-fabricated $LiNbO_2$ memristors

The methodology for testing Li_xNbO_2 memristors post-deposition, fabrication and metallization comprises of I-V cycling the devices at small voltage magnitudes (~100s of mV) and incrementally increasing voltage sweep magnitude until a repeatable hysteresis response is observed. What is observed is that the as-deposited memristor has a high resistance and I-V response as represented by Figure 6-1 (a). This initial I-V response seen in Figure 6-1 (a) resembles a diode turning on at ±600mV and having a weak clockwise hysteresis in the positive voltage sweep (first quadrant) and a weak anti-clockwise hysteresis in the negative voltage range (third quadrant). Then as the device is cycled to higher voltage ranges, at some voltage an irreversible "burn-in" phenomenon is observed where-in the I-V response changes to that represented in Figure 6-1 (b). Post

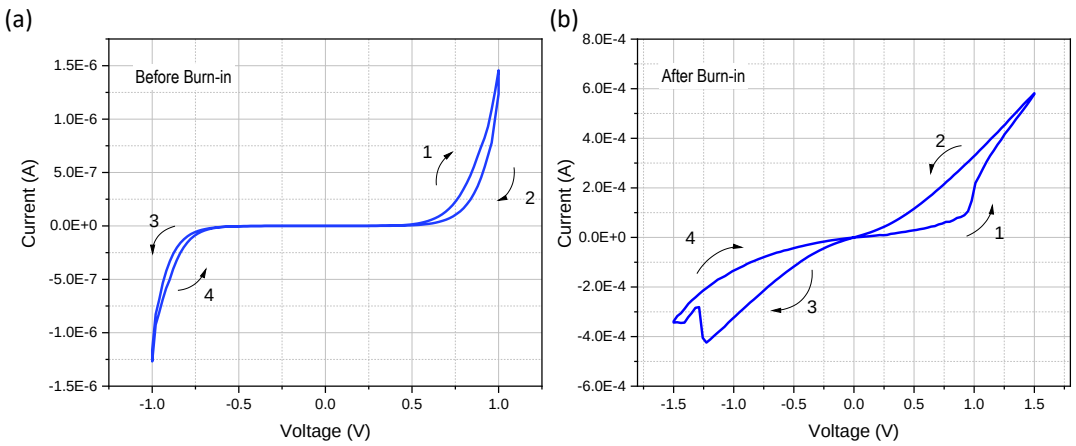


Figure 6-1: Current voltage (I-V) response of a 10 µm x 100 µm Li_xNbO_2 memristor (a) before "burn-in" and (b) after "burn-in" shows the hysteresis direction flips and device resistivity decreases after "burn-in".

"burn-in" the I-V response shows a strong anticlockwise hysteresis with positive voltage sweep (first quadrant) and a clockwise hysteresis in the negative voltage range (third quadrant). This post "burn-in" hysteresis behavior is consistent with positive voltage sweeping Li^+ into the Ag electrode resulting in a more conductive channel and negative voltage pushing Li^+ back into the channel and reducing the conductivity and thus current across the device. The conductivity of the film also increases post "burn-in" as observed in the increase in the y-axis (current) scale of Figure 6-1 (b) vs (a). The analog memristive behavior studied throughout this dissertation is that of post "burn-in" devices. The contrast in the resistivity and nature of hysteresis in pre vs post "burn-in" devices suggest an irreversible change in channel material or interfacial species during the device cycling past the "burn-in" voltage. This necessitates initial device cycling for reactive sputtered Li_xNbO_2 memristors before they are deployed in neuro-mimetic applications that was not required for the non-reactive devices previously studied. In-depth characterization studies such as XPS of the reactive Ag - Li_xNbO_2 interface in as-fabricated devices and post "burn in" devices must be performed to better understand the

physical origin of the "burn-in" mechanism in Li_xNbO_2 memristors. However, these studies are complicated by the tendency of the surface to oxidize and change composition as surface contaminants or metal electrodes are sputtered away, making such studies challenging.

6.2 Programming threshold in Li_xNbO_2 memristors

There exists a minimum programming voltage required to induce a non-volatile change in resistance of Li_xNbO_2 memristors. Figure 6-2 (a) demonstrates this threshold behavior in a 5 µm x 100 µm device where a 750 mV induces minimal if any change in the device current, simply retracing the high resistance branch '1' of the I-V response at ±1.5 V sweep, however, a 780 mV sweep incrementally changes the current in the devices to a higher value (lower resistance) by pushing Li^+ ions into the Ag electrode. In Figure 6-2 (b) a 5 µm x 25 µm device shows minimal resistance change at a ±300 mV sweep however shows an open hysteresis curve when cycled at ±500 mV. Zivasatienraj et

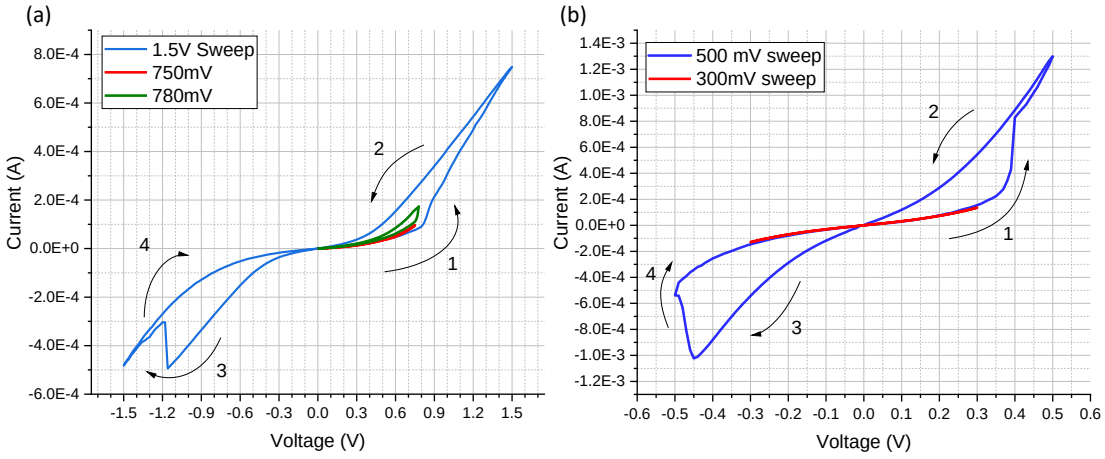


Figure 6-2: Current voltage (I-V) response of a (a) 5 µm x 100 µm Li_xNbO_2 memristor shows no resistance change at 750 mV sweep but hysteresis response above 780 mV; (b) that of a 5 µm x 25 µm Li_xNbO_2 memristor shows no resistance tuning at ±300 mV sweep but open hysteresis at a ±500 mV sweep.

al. [60] showed that this minimum programming voltage scales with device length, down to 150 mV for a 2 µm x 2 µm memristor. To probe the origin of the threshold mechanism in Li_xNbO_2 memristors, the temperature dependence of threshold voltage is studied in a 5 µm x 100 µm memristor, as shown in Figure 6-3. Figure 6-3 (a) shows the voltage threshold at room temperature to be ~780 mV where hysteresis appears but decreases to ~ 650 mV at 150º C in Figure 6-3 (b). The key takeaway from this observation is the surprisingly weak dependence of temperature on the magnitude of threshold voltage (ΔV_{th} = 130 mV for ΔT = 129 K) and on the magnitude of the current (roughly the same in Figure 6-3 (a) and (b)). This suggests that the origin of the thresholding mechanism is not Li^+ ion activation since Li^+ is known to be extremely mobile even at room temperature [103][105]. Likewise, it would appear the memristance and hysteresis are stable against large temperature changes.

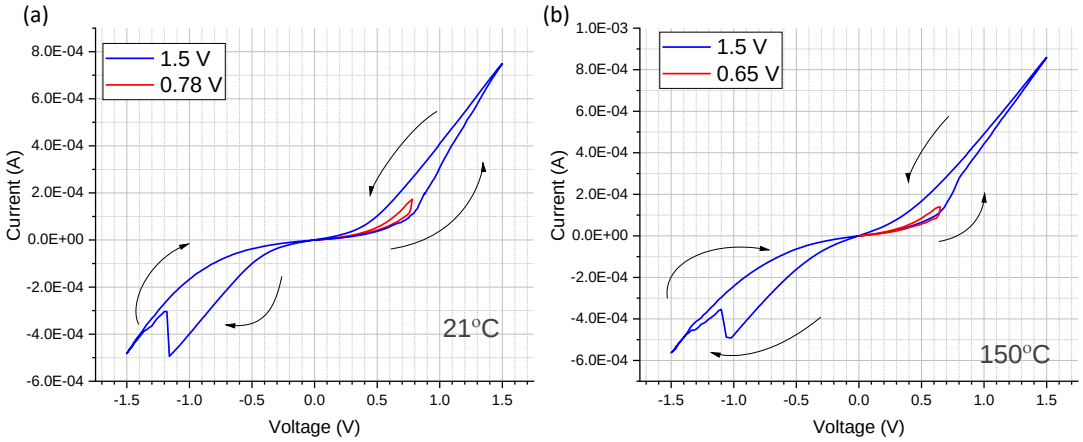


Figure 6-3: Current voltage (I-V) response of a 5 µm x 100 µm Li_xNbO_2 memristor at (a) 21ºC and (b) 150ºC shows the programming threshold decrease from 780 mV at room temperature to 650 mV at high temperature.

6.3 Analog resistance programming above threshold in Li_xNbO_2 memristors

Li_xNbO_2 memristors demonstrate voltage-dependent incremental hysteresis response between a lower limit of programming set by the threshold voltage and an upper

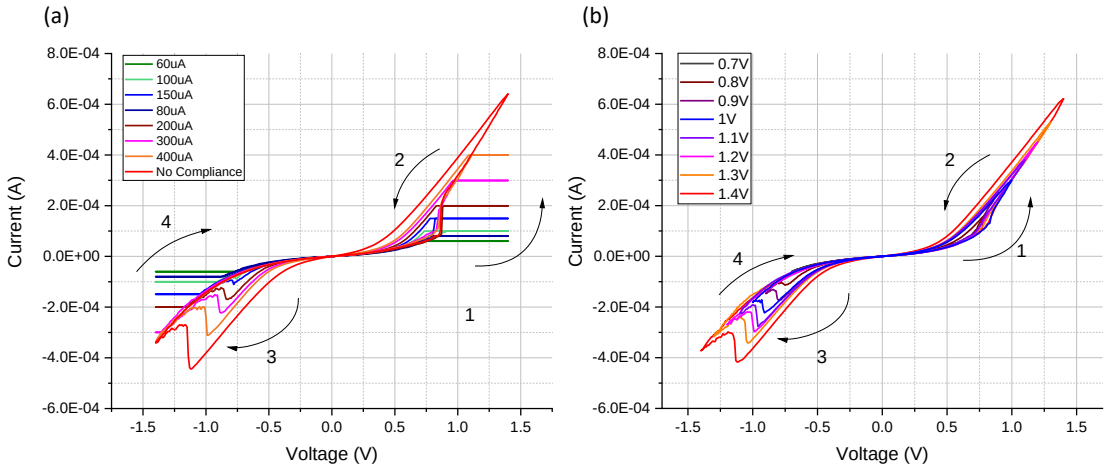


Figure 6-4: Current voltage (I-V) response of a 5 µm x 100 µm Li_xNbO_2 memristor shows tunable area under hysteresis curve with (a) varying current compliance and (b) varying magnitude of voltage sweep.

limit of programming voltage at which the channel is presumed delithiated to about ~50%. This analog resistance tunability is displayed in Figure 6-4 for a 5 µm x 100 µm memristor where the area under hysteresis curve can be incrementally tuned by varying the current limit of the voltage sweep (Figure 6-4 (a)) or varying the magnitude of voltage sweep (Figure 6-4 (b)). The hysteresis dependence on the magnitude of input signal has been established as a fingerprint of memristors [137]. In Figure 6-4, each I-V cycle starts at the high resistance branch "1" of the ±1.4 V curve which defines the highest resistance state of this device. Above the ~780 mV threshold increasing the magnitude of input voltage sweep traces an increasing resistance change from branch "1" to branch "2" as incremental amounts of Li^+ ions can move from the channel into the Ag electrode in the first quadrant of the I-V response. As the input voltage crosses zero and becomes negative, Li^+ ions are swept out of the Ag pad and into the channel, and the device resistance increases from the programmed resistance curve in branch "3" back to

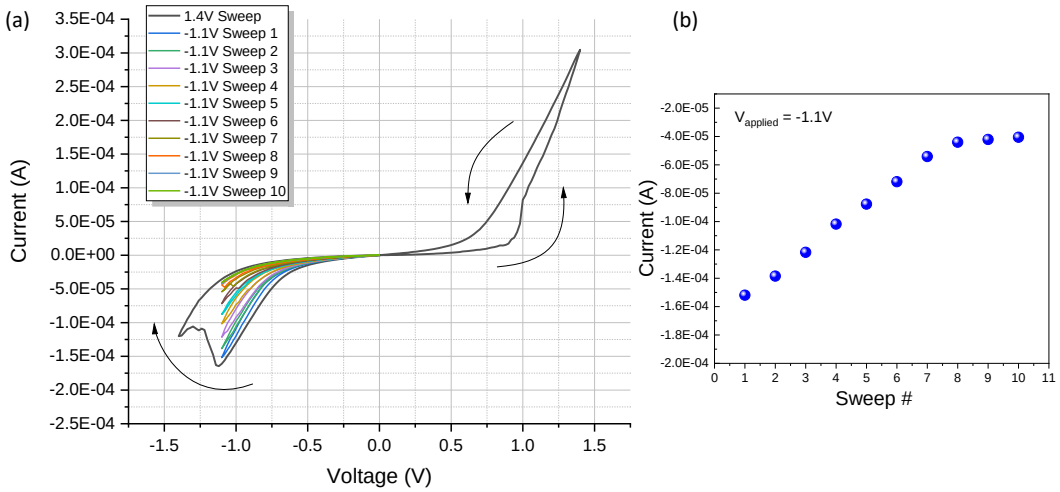


Figure 6-5: (a) Current voltage (I-V) response of a 5 µm x 100 µm Li_xNbO_2 memristor shows incremental analog de-programming using consecutive -1.1 V sweeps to retrace the de-programming achieved in a single -1.4 V sweep; (b) plot showing linear de-programming in device current with each -1.1 V sweep until saturation at presumed maximum lithiation of channel.

its maximum high resistance state in branch "4" which overlaps for each of the I-V sweeps. Thus, incremental field-dependent hysteresis is observed above the programming threshold and within the I-V response dictated by the ±1.4 V sweep. Pushing the 5 µm x 100 µm memristor to voltages above ±1.4 V can create larger resistance change but often leads to device failure due to the high current density in the device.

The analog memristive response in Li_xNbO_2 memristors is further demonstrated in Figure 6-5 (a) where the resistance deprogramming attained on the negative cycle of the ±1.4 V sweep (black curve) can be recreated by sequentially sweeping ~ ten –1.1 V cycles in a 5 µm x 100 µm memristor. Each –1.1 V sweep appears to deprogram the resistance by a constant amount, as Li^+ ions move from Ag electrode back into the channel. This suggests that for fine granularity in resistance tuning, a voltage slightly above the programming threshold should be used to achieve analog weight updates in Li_xNbO_2 memristors. Figure 6-5 (b) plots the incremental decrease in device current as

each of several -1.1 V sweeps push Li^+ ions into the channel and demonstrates high linearity in the analog de-programming, up until the device current begins to saturate as all available Li^+ is swept from the Ag electrode into the channel. Linear resistance changes have been shown vital for efficient and accurate neuromorphic circuit convergence [154].

The inherent analog device dynamics of Li_xNbO_2 memristors also provides flexibility in choice of programming voltage depending on the required granularity of synaptic weight-states in the end application. Figure 6-6 (a) shows the incremental programming of a 5 µm x 100 µm memristor via voltage sweeps of incremental magnitudes from +1 V to +1.4 V, pushing the device resistance from its highest resistance to lowest resistance state respectively, as described by the first quadrant of the ±1.4 V sweep in Figure 6-5 (a). Negligible resistance change is observed at the +1 V sweep, suggesting this is the approximate threshold voltage for the memristor. Figure 6-6

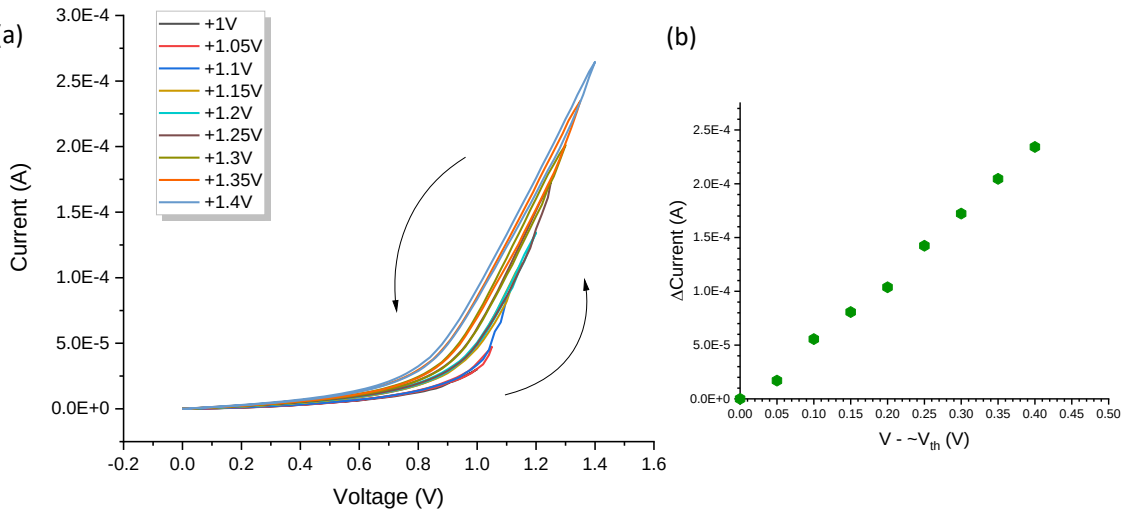


Figure 6-6: (a) Current voltage (I-V) response of a 5 µm x 100 µm Li_xNbO_2 memristor shows incremental analog programming using voltage sweeps of varied magnitude; (b) plot showing linearity in change in device current with magnitude of programming voltage above threshold ($V_{applied} - V_{th}$)

(b) plots the change in memristor current (via changing resistance) from its lowest current state at +1 V with the magnitude of voltage applied above this threshold voltage (+1 V), demonstrating linearity in programming step size with input voltage. A larger magnitude of voltage above threshold results in a larger electric field across the channel pushing an increased amount of Li^+ ions into the Ag electrode, with a linear trend. Section 6.3 thus demonstrates the analog nature of resistance tuning in Li_xNbO_2 memristors with flexibility in programming voltage and granularity of states, and inherent write linearity. Additionally, the design option of lowering the threshold voltage by making smaller devices (~100 mV to ~1.1V threshold windows have been shown [60][109]) allows for a selective threshold similar to the sigmoidal functions commonly used in neural circuits [155][156][157]. Thus, we have demonstrated a physical platform capable of linear programing with a selectable programing step that can be windowed in a sigmoidal manner – the core elements of neural computation.

6.4 Negative differential resistance during deprogramming cycle

The current-voltage response of lateral Li_xNbO_2 memristors of varied geometries discussed throughout this dissertation show a negative differential resistance (NDR) feature in the negative sweep cycle, as demonstrated in Figure 6-6 for a 10 µm x 50 µm memristor. The slow 17 mHz sweep in Figure 6-6, verifies that this feature in the fourth quadrant is not a switching mechanism as seen in filamentary memristors, but a continuous NDR response during the transition from lower device resistance in branch "3" to higher device resistance in branch "4" of the I-V response. Furthermore, as observed in Figure 5-1 and Figure 5-2 from Chapter 5, the NDR behavior is strongest at low frequencies and disappears with the closing up of the hysteresis at higher

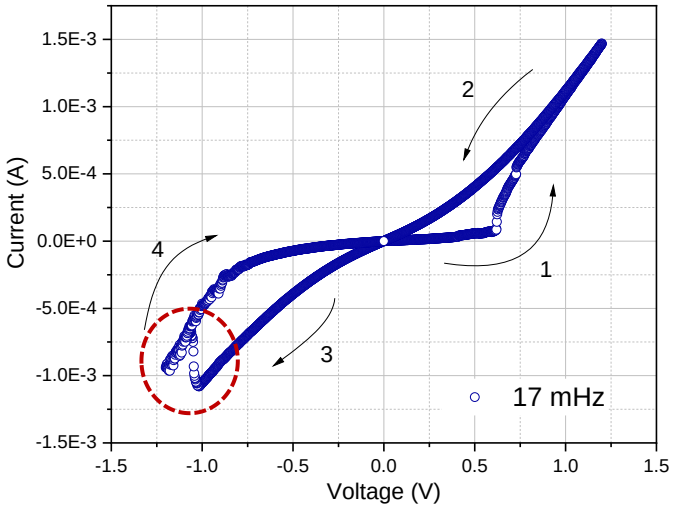


Figure 6-6: Current voltage (I-V) response of a 10 µm x 50 µm Li_xNbO_2 memristor using a slow DC voltage sweep showing NDR response (highlighted in red) as the input voltage is swept negative on the Ti/Au electrode.

frequencies. This frequency dependence suggests the origin of the NDR response lies in ion dynamics. Shank [158] had previously simulated a similar NDR response before the applied voltage reaches its minimum value in volatile $LiNbO_2$ memristors using an ion hopping conductivity model, and found it was a result of competitions in drift and diffusion assisted ion recovery returning the ion gradient to zero (from the linear ion profile under the external bias) and reversing its profile as the applied voltage polarity reverses. Said another way, there is a volume of stored charge in the ion profile that is not returned to zero as the voltage reaches zero and only returns to zero at a later time when the voltage is already negative. This ion current flow at zero voltage implies an ionic inductance that can result in massive apparent inductances such as those reported by Hodgkin and Huxley [159][160]. These ionic inductances have yet to be used for temporal benefit in neuromorphic devices. In non-volatile Li_xNbO_2 memristors discussed here, the NDR response occurs in the fourth quadrant as the external voltage sweeps Li+ ions in the channel towards the Li-blocking Ti/Au pad whereas Shank's volatile

memristor model showed hysteresis at both voltage extrema. Thus, Shank's model [158] built for volatile memristors with both Li-blocking electrodes can be used to explain the NDR behavior observed here but only for the portion of the cycle where Li is accumulating at the Li blocking contact.

6.5 Conclusion

Chapter 6 focuses on understanding the device response of Li_xNbO_2 memristors to external voltage which will help guide the design rules for using the developed memristors in biomimetic learning platforms. As-fabricated, reactive sputtered non-volatile Li_xNbO_2 memristors need a pre-conditioning cycle referred to as "burn-in" to initiate their memristive characteristics whereas prior non-reactive synthesized devices do not. The non-volatile memristors also exhibit a voltage threshold below which no resistance tuning/hysteresis is observed, and this minimum programming voltage is observed to scale with device length [60]. The finite but weak dependence of this threshold voltage on temperature suggests a non-ionic physical mechanism for its origin. Above threshold, the Li_xNbO_2 memristors show analog resistance tuning via Li^+ ion intercalation in and out of Li-absorbing Ag electrode. The granularity of resistance tuning and hence number of achievable resistance states (synaptic weights) is controlled by the magnitude of applied bias across the memristor which dictates the %Li driven out of the channel into Ag layer. The field-driven resistance tuning in these memristors enable linear programming at a fixed input voltage, as well as linear increase of degree of programming (ΔR) by varying the magnitude of input voltage implementing a displacement flux function $\int Vdt$. As Li^+ ions are then swept out of the Ag electrode into the channel and then towards the Ti/Au electrode, ion dynamics lead to a NDR response

that is sensitive to the frequency of voltage sweep. The mixed ion-electron dynamics inside the Ag- Li_xNbO_2 system thus enables flexibility in design and operation missing from the majority of other memristive technologies.

CHAPTER 7. CONCLUSIONS AND FUTURE OUTLOOK

7.1 Summary

Neuromorphic computing is an exciting field of research with the potential to mimic the brain's energy-efficiency, adaptability and parallelism and transform the next generation of computing. The realization of truly biomimetic systems has also become critical as the world is witnessing the rapid deployment of large-scale artificial intelligence (AI) models requiring vast amounts of data and power [161][162]. Developing neuromorphic platforms with memristors allow a new paradigm of bottom-up biomimetic computing where the dynamics of the material system can begin to directly contribute to computation. Although in its nascent stage, memristive technology is being widely investigated in various materials, each with their own device dynamics. This dissertation focused on lithium niobite (Li_xNbO_2) memristors, a unique Li-intercalation based material system that allows design flexibility in resistivity, resistance-tunability range, and operation frequency, along with fully analog, flux-linkage dependent response.

Li_xNbO_2 memristive devices were sputter deposited and fabricated using processing techniques that were extensively tested and optimized over the course of this work. Electrical and material characterization of non-volatile Li_xNbO_2 memristors performed in this work provided insight into the non-volatile programming mechanism and the ability to tune the degree of volatility using electrode chemistry. Systematic study of the frequency response of non-volatile Li_xNbO_2 memristors helped establish the temporal flexibility inherent to these devices, due to the dynamics of Li+ ion motion inside a non-stoichiometric Li_xNbO_2 channel ($0.5 < x < 1$). The hysteresis response of

these non-volatile memristors were also investigated to highlight the linear analog programmability inherent to Li_xNbO_2 memristors and identify physical mechanisms that control device operation. All major functions of a neural network, analog training, linear resistive changes, and adaptive activation are efficiently implemented in hardware during the course of this research.

7.2 Future Directions

The research presented in this dissertation only begins to scratch the potential of ion-intercalation driven $LiNbO_2$ memristors, but already highlights the versatility of this inherently analog memristive platform, and its advantages over other contemporary memristor technologies. As of this dissertation, research efforts on Li_xNbO_2 memristors has progressed from a materials-focused endeavor to device enhancement and understanding efforts. However, an unprecedented amount of research is still required for building neuromorphic compute-in-memory chips using this technology. This section highlights future research efforts required to push the Li_xNbO_2 memristors towards commercial application:

- **Enhancing resistance tunability window via lithiation of the Li_xNbO_2 material:** Notably, the largest tunability window in conductivity (and thus memristance) is observed when Li_xNbO_2 approaches near-stoichiometry ($x \sim 1$). Consequently, ongoing research efforts are focused on optimizing the material deposition conditions to deposit stoichiometric $LiNbO_2$ during sputtering. It is important to note, however, that common microfabrication processes including DI water rinse have been known to cause delithiation of Li_xNbO_2. Hence, it is crucial

to develop methods that target the latter stages of device fabrication, specifically just before the encapsulation process, with the aim of increasing the Li content in the material. Methods like ion implantation may be viable solutions to full lithiation of these devices.

- **Design of encapsulation layers for Li_xNbO_2 memristors:** Due to the highly reactive nature of Li, there are some concerns with the long-term stability in Li_xNbO_2 memristors due to the loss of Li to diffusion to the surface and subsequent oxidation with ambient air. Thus, it is necessary to encapsulate Li_xNbO_2 memristors with a protective dielectric material that is inert to air, blocks Li without interacting with it, and does not impact the memristor operation. Furthermore, it must be ensured that the processing steps for this encapsulating material deposition does not impair the memristor operation either.
- **Scale down device size for enhanced performance of Li_xNbO_2 memristors:** This dissertation has established the strong relationship between non-volatile Li_xNbO_2 memristor performance and device geometry. However, research thus far has investigated memristor dimensions in the micron range. In these devices, memristive performance has already been shown to improve as memristors are scaled down in size [60][144]. Furthermore, smaller device size means fewer material defects and more uniformity, resulting in higher device yield, with repeatable low-power operation. Thus, scaling of Li_xNbO_2 memristor should be performed down into the nanometer scale with the help of electron-beam lithography in research and advanced lithography if commercialized.

- **Endurance and retention studies for Li_xNbO_2 memristors:** Traditional retention testing techniques typically use temperature accelerated testing to estimate long-term device stability. Given the complex temperature dependent Li diffusion in Li_xNbO_2 devices, temperature accelerated testing is not a viable option as it is not representative of the expected retention at operational temperatures (close to room temperature). Therefore, actual long time period study remains as the only present option for retention testing in these devices. Thus, to test for a million seconds, one needs to wait a million seconds. Similarly, continuous device cycling for endurance testing leads to local temperature rise resulting in thermal effects hard to decouple from actual device endurance. There is thus a need for investigating alternative methods for optimal retention and endurance testing in Li_xNbO_2 memristors.
- **Probing device operation mechanisms in non-volatile Li_xNbO_2 memristors:** The major challenge in developing the Li_xNbO_2 memristor platform thus far has been the lack of characterization methods to decouple and clearly observe the various mechanisms involved with device operation, most importantly those occurring at the Ag-Li_xNbO_2 interface. This challenge arises in part from the high reactivity of Li with any mode of external stimulus and the sputtering matrix effect of Li and Nb having very different atomic mass making XPS and SIMS analysis challenging. Furthermore, niobium oxide is known to sputter preferentially becoming reduced under Ar ion bombardment [163], making it difficult to perform standard depth studies on Li_xNbO_2 memristors. There is thus a need for employing suitable probing techniques to (i) characterize the Ag-

Li_xNbO_2 interface during device cycling, and (ii) estimating the %Li change in Li_xNbO_2 channel for an applied electric field, to be able to engineer these memristors for commercial application.

- **Study the scalability and tunable performance of vertical Li_xNbO_2 memristors:** This dissertation delved into the design and tunable performance of lateral Li_xNbO_2 memristors, showcasing the versatility of the Li_xNbO_2 platform. However, for commercial integration of this platform, there is a strong need for vertical devices that will do away with the need for Li-blocking substrates and can be easily scaled down to ~nm order active oxide material. The vertical structure also reduces the surface area of niobite material exposed to the ambient, aiding long-term device reliability. Hence, there is a need for detailed understanding of vertical Li_xNbO_2 memristors and their performance dependence on geometry.
- **Physical implementation of STDP-enabled Paired Input Learning Layer (STDP-PILL) architectures using Li_xNbO_2 memristors:** Zivasatienraj et al. [109] have developed a self-training memristive network architecture driven by sets of paired inputs that use the advantages of Li_xNbO_2 memristor dynamics to eliminate the need for accessing or manipulating individual weights. These developed memristive architectures also execute temporal computations using signal agnosticism owing to the niobite memristor dynamics, adding another of flexibility to this memristive platform. Non-volatile Li_xNbO_2 memristors developed in this dissertation must be used to physically demonstrate the potential of such STDP-PILL based self-learning networks.

APPENDIX A. LITHIUM NIOBITE PROCESSING

A.1 Sputter Deposition in Denton Discovery 2

Non-reactive $LiNbO_2$ sputter recipe:

Lithium Oxide Source Power	200 W
Niobium Source Power	50 W (DC)
Chamber Pressure during deposition	1 mTorr
Argon flow during deposition	5 sccm
Oxygen flow during deposition	0 sccm

Reactive $LiNbO_2$ sputter recipe:

Lithium Oxide Source Power	100 W
Niobium Source Power	83 W (DC)
Chamber Pressure during deposition	1 mTorr
Argon flow during deposition	4.5 sccm
Oxygen flow during deposition	0.5 sccm

Niobium Oxide (Nb_2O_5) sputter recipe:

Lithium Oxide Source Power	0 W
Niobium Source Power	50 W (DC)
Chamber Pressure during deposition	10 mTorr
Argon flow during deposition	1 sccm
Oxygen flow during deposition	9 sccm

A.2 Photolithography

Patterning of all devices discussed in this dissertation was performed using a Heidelberg MLA150 maskless aligner in the Marcus Inorganic Cleanroom at Georgia Tech. A lift-off process is used for fabrication of lateral memristors on polished sapphire. The primary challenges with photolithography in these devices include (i) patterning on a non-flat surface due to presence of niobite mesa and metal pad structures leading to resist breaking at the mesa edges, and (ii) the difference in optical parameters of transparent sapphire substrate vs opaque niobite layer leading to nonuniform exposure for an incident dose. A thick ~2 μm resist layer is used in the 2nd and 3rd lithography steps to overcome the drawbacks of nonuniform surface height.

Lithography Layer 1: Defining mesa for $LiNbO_2$ sputter deposition

1. Solvent clean, DI water rinse, N_2 dry

2. Dehydration bake – 110°C for 5 minutes
3. Spin NR9-1500 PY at 500 rpm for 5 seconds, then 3500 rpm for 40 seconds
4. Soft bake – 110°C for 2 minutes
5. Exposure – 450 mJ/cm^2 at 375 nm
6. Post-exposure bake – 110°C for 2 minutes
7. Develop – RD6 for 17 seconds (depends heavily on feature size)
8. DI water rinse, N_2 dry
9. Descum: 30 seconds in O_2 plasma in a RIE chamber

Lithography Layer 2: Defining volatile contact pads for Ti/Au evaporation

1. Solvent clean, DI water rinse, N_2 dry
2. Spin NR9-1500 PY at 500 rpm for 5 seconds, then 2000 rpm for 40 seconds
3. Soft bake – 110°C for 2 minutes
4. Exposure – 950 mJ/cm^2 at 375 nm
5. Post-exposure bake – 110°C for 5 minutes
6. Develop – RD6 for 15 seconds
7. DI water rinse, N_2 dry
8. Descum: 30 seconds in O_2 plasma in a RIE chamber

Lithography Layer 3: Defining non-volatile contact pads for Ag/Ti/Au evaporation

1. Solvent clean, DI water rinse, N_2 dry
2. Spin NR9-1500 PY at 500 rpm for 5 seconds, then 2000 rpm for 40 seconds
3. Soft bake – 110°C for 2 minutes
4. Exposure – 1100 mJ/cm^2 at 375 nm

5. Post-exposure bake – 110°C for 5 minutes
6. Develop – RD6 for 15 seconds
7. DI water rinse, N_2 dry
8. Descum: 30 seconds in O_2 plasma in a RIE chamber

A.3 Metallization

Metal contacts were deposited either using the CHA Industries e-beam system or the Denton Explorer e-beam evaporator in the Marcus Inorganic cleanroom. Exposure to atmosphere post develop and descum is kept to minimum and chamber is always pumped down to at least ~$3x10^{-6}$ Torr to prevent contamination during metal deposition. Samples are adhered to the substrate holder using Kapton® polyimide tape and carefully dusted using N_2 just before loading into the evaporator chamber.

Typical volatile contact metal deposition:

Metals: 300 nm of Ti, followed by 200 nm of Au

Deposition: 3 Å/s rate with background pressure of ~$3x10^{-6}$ Torr

Typical non-volatile contact metal deposition:

Metals: 300 nm of Ag, then 100 nm of Ti, followed by 200 nm of Au

Deposition: 3 Å/s rate for Ag and Au, 2 Å/s for Ti

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