BACK-END-OF-LINE MECHANICAL STRESS EFFECTS IN SIGE HBTS AT CRYOGENIC TEMPERATURES

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LIST OF ACRONYMS

BEOL back-end-of-line

HBT heterojunction bipolar transistor

LNA low-noise amplifier

TCAD technology computer-aided design program

SUMMARY

SiGe heterojunction bipolar transistors (HBTs) are well suited to operating in cryogenic environments, which are found in areas from deep space exploration to radio astronomy and quantum computing. One problem in deploying SiGe HBTs to cryogenic environments is increased device-to-device variability, a major factor of which is variations in mechanical stress caused by metal routing (referred to as the back-end-of-line, or BEOL) above and in the immediate vicinity of the active devices. The impact of BEOL stress on SiGe HBTs at crygenic temperatures has been presented in [1]. This work does a deeper examination of the theoretical and measured impact of BEOL stress on SiGe HBTs at cryogenic temperatures.

CHAPTER 1
INTRODUCTION

1.1 Motivation

Transistor operation at cryogenic temperatures is relevant to several application areas. One of the oldest is in highly sensitive receivers for radio astronomy. Because the received signal is so small, radio telescopes require extremely sensitive receivers with some of the strictest noise requirements of any receiver applications. One commonly used solution employs SIS (superconductor-insulator-superconductor) mixers for downconversion, which achieve near-quantum-limit performance at high frequencies [2]. However, in regards to bandwidth, dynamic range, and noise performance at low frequencies (< 50 GHz), cryogenically cooled transistor-based low-noise amplifiers (LNAs) retain the advantage [3]. Currently, most transistor-based receivers use InP HEMTs in order to acheive the best possible noise performance [3]. However, next generation radio astronomy receivers will introduce new requirements which may open the door to other technologies. Since noise performance is already near theoretical limits, further improvements in sensitivity are expected to require larger collection areas with large numbers of smaller antennas [4]. These systems will require receivers that are lower cost, more compact, more reproducible, and tightly integrated to digital processing [4]. These new requirements line up well with the strengths of SiGe HBTs, which are an attractive choice if the performance compromise of moving from InP HEMTs to SiGe HBTs can be minimized.

Another area where cryogenic operation of transistors is important is for space. For deep space missions, typical electronics need to be actively heated to ensure correct operation in cold environments. This is commonly done with radioisotope heating units which constantly heat the spacecraft [5]. There are a few downsides to this approach. One is that

these heating units are expensive and complicate the design. Another is that these heaters are always on and cannot be turned off when heating is not needed. A better solution is to design electronics which can operate at low temperatures. Circuits designed to operate at extremely low temperatures without active heating would reduce size and weight and therefore launch cost [6]. An additional benefit to this approach is that these circuits can take advantage of the higher performance of devices and lower loss passives that come with low temperatures.

Another application of cryogenically cooled circuits is in quantum computing. This area is largely responsible for the recent increased level of attention on cryogenic circuits. In quantum computers, the current method for controlling and reading out qubits uses interconnects running from the cold head of the refrigerator out to room temperature lab equipment. In the larger scaled systems that will be necessary for quantum computers to perform useful operations, the number of interconnects would be prohibitively large. This is an issue both from a physical size point of view and considering the thermal load on the system. To solve this problem, is desirable to locate the electronic control circuitry inside the refrigerator at low temperatures [7]. Because there is little cooling power available at 20-100 mK where the qubits sit, a controller with readout circuitry would reside on a warmer stage with a temperature of 1-4 K [8]. A smaller number of transmit and receive units can be multiplexed to many qubits using a switch matrix on the 20-100 mK stage as in [9]. To avoid perturbing the qubit, the noise requirements of the readout circuitry are strict, but the inherent advantages of operating the readout circuitry on a low temperature stage will help to meet those requirements.

In all these applications, operation of transistor circuits at cryogenic temperatures has the possibility of bringing compelling benefits from both a system level (reduced size, reduced complexity, etc.) and on a circuit level (improved noise performance). However, since these devices will be operating far outside their intended operating conditions, the device characteristics and the operative physics are less well-understood than at room tem-

perature. This presents large challenges in modeling these devices and designing circuits with them. Improving these aspects must start with better understanding of the physics at play.

1.2 SiGe HBTs at Cryogenic Temperatures

SiGe HBTs are positioned in an advantageous position with regard to the applications above. For a given process node, SiGe HBTs have better high-frequency performance than CMOS while retaining the low cost associated with traditional CMOS manufacturing techniques. The highest speed SiGe HBTs retain a speed advantage over the most advanced CMOS [10] at a better price-to-performance point than III-V technologies. Furthermore, when compared to III-V technologies, the integration of high speed SiGe HBTs with CMOS in BiCMOS processes allows integration of dense digital circuitry with high-performance RF frontends. This integration with CMOS is a killer feature for SiGe BiCMOS processes, and it offers benefits for all three cryogenic circuit applications described above. In next-generation radio astronomy receivers, there is a need to bring more functions into the digital domain in order to reduce complexity and increase performance in large antenna arrays. In SiGe technology, the RF frontend can be directly integrated with a high-performance ADC, all on the same chip to reduce interconnect length and take advantage of the decreased noise at cryogenic temperatures. The low cost of SiGe technology makes it an attractive choice for large arrays with large numbers of pixels. For space applications, the space and power savings from tight RF-to-digital integration make SiGe BiCMOS processes a good choice. An additional benefit is that SiGe HBTs happen to be tolerant of extremely high doses of radiation. In fact, when it comes to many different kinds of extreme environments, SiGe HBTs tend to work well with no modifications from the typical high-volume production process flow [11]. For quantum computing, fully-functioning controllers will need digital logic alongside the high frequency circuits. This will allow keeping as much functionality as possible inside the dilution refrigerator,

reducing the required interconnects.

Given all of these benefits for using SiGe BiCMOS circuits in these applications, it is fortuitous that the performance of SiGe HBTs is greatly increased with cooling. This performance increase applies to nearly every important aspect of device operation [12]. Transconductance is strongly increased, theoretically scaling with the reciprocal of temperature. While there is an inherent decrease in electron diffusivity, the effect of Ge grading in the base in SiGe HBTs means that emitter and base transit times decrease with lower temperature, leading to higher transit frequency f_T. This improvement is can be quite large, as shown in Figure 1.1. Both current gain β and Early voltage V_A increase exponentially with cooling, a result of their dependence on Ge-induced band offsets in the base (β) and collector-base junction (V_A). For RF, analog, and high-speed digital purposes, these device-level performance increases mean that circuits designed for cryogenic temperatures have the possibility of not just working, but improving the relevant figures-of-merit compared to room temperature.

The main challenge posed by operating SiGe HBTs at cryogenic temperatures is not dealing with changes in performance – improvements there come essentially for free. Rather, the difficulty is that these devices can behave in unusual, unexpected ways, particularly at deep cryogenic temperatures below 40 or 50 K. Although the fundamental operation of the transistor is not changed, the theoretical equations for collector current and base current fall short of describing the observed characteristics at these temperatures. This behavior is indicative of physics mechanisms that are not relevant to room temperature operation. Because these effects are not well-understood, physics-based compact models fail to capture them. As a result, circuit design is very challenging. Better understanding of the physics of device operation at these temperatures is necessary for robust cryogenic design.

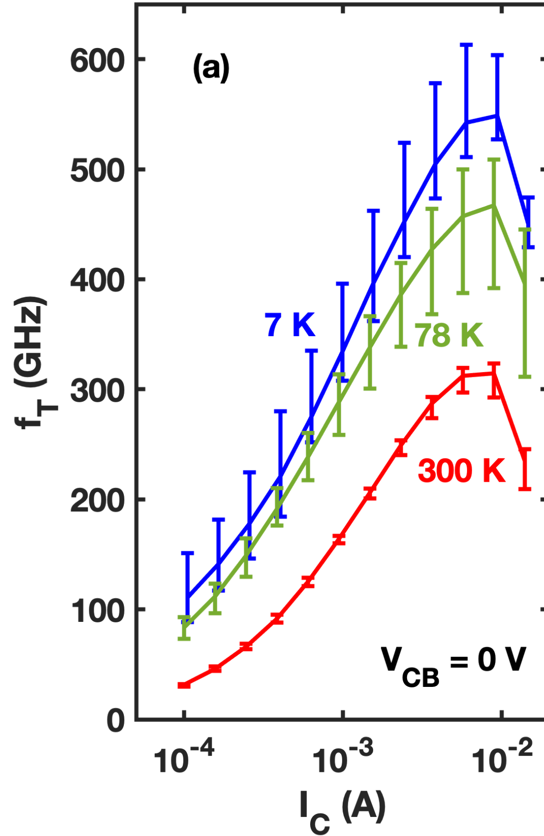

Figure 1.1: Transit frequency f_T as a function of I_C [13]. Peak f_T increases from around 315 GHz at 300 K to around 550 GHz at 7 K.

1.3 Mechanical Stress

A series of studies have shown that device-to-device variability increases greatly for SiGe HBTs when cooled to cryogenic temperatures [13, 14]. This observation is concerning for circuit designers, who need designs to be repeatable at scale. In [14], one of the main causes of increased cryogenic variability was identified to be mechanical stress. The practical difficulties of poor device-to-device matching at cryogenic temperatures is illustrated well in [15], which analyzes current mirror mismatches. In that work, current mismatch in both SiGe HBTs and CMOS current mirrors was observed to increase drastically at low temperatures. Common centroid layouts offered only marginally better results. Since analog circuits and bias circuits for RF designs both rely heavily on current mirrors, these

results are not good news for designers. In order to understand this effect and hopefully mitigate these effects, it is necessary to understand the physical mechanisms behind mechanical stress and its effect on device operation. Furthermore, it is important to track how these factors change as temperature is decreased from room temperature to cryogenic temperature.

It is well known that mechanical stress impacts the electrical properties of Si [16, 17]. This occurs because the crystal lattice under strain is deformed, resulting in a modified band structure. This effect has long been recognized to be important in MOS devices, and engineering strain in MOSFETs to be beneficial to device operation is a well-established practice [18, 19, 20]. SiGe HBTs have a large amount of strain built-in due to the lattice mismatch between Si and Ge. The impact of this strain on carrier mobilities and band structure has received a good amount of attention, and therefore modeling the effects of this built-in stress in device simulators and compact models is standard practice. What is often neglected is the impact of external structures on the stress seen by the device. Structures nearby a device in the circuit layout will have an effect on the mechanical stress experienced by the device, as well as how the die is packaged [21]. This work focuses on the former case, the impact on mechanical stress caused by metal routing layers placed above and nearby an active device. Since the routing and passive layers above the substrate are commonly referred to as the back-end-of-line (BEOL), mechanical stress caused in this manner is referred to as BEOL stress.

Several works have observed the effect of BEOL stress on SiGe HBT characteristics. In [22], devices subject to BEOL stress were observed to have an increase in collector current (I_C) or 25% at a given base-emitter voltage (V_{BE}). Similarly, the base current was observed to increase by 5%. The net effect was a 16.5% increase in β. High frequency performance was increased in the stressed device compared to an unstressed device. Transit frequency f_T increased by 3%, while maximum unilateral gain frequency f_{max} was increased by 12%. Simulations performed in [23] showed similar increases in DC operating currents,

although AC performance was not simulated. In [24], devices under mechanical stress were simulated in a TCAD simulator, using a full band structure Boltzmann transport equation (BTE) approach. That simulation showed that varying an applied uniaxial stress in the device could produce shifts in f_T similar to those seen in measurement.

The previous works were all conducted at room temperature. Although BEOL stress has been postulated as the cause of the device variability issues [14], direct measurement of mechanically stressed devices has not yet been performed at cryogenic temperatures. Furthermore, it is unclear whether the increased variability is caused by a temperature dependence in how stress impact a device or if the amount of stress experienced by the device changes as temperature is reduced. This work addresses that question. First, the theoretical background of device operation and the mechanisms behind BEOL stress effects are explained. Next, measurements of devices are presented. Following that is a demonstration of how mechanical stress can be simulated and used to predict potential issues related to BEOL stress. Finally, implications for circuit design are discussed.

CHAPTER 2
THEORETICAL BACKGROUND

2.1 SiGe HBTs at Low Temperatures

Before getting into the specifics of mechanical stress, it is important to understand the operation of SiGe HBTs at low temperatures. Due to the nature of Boltzmann statistics, the base and collector currents couple exponentially to the inverse of temperature. As given in [12], the temperature dependence of the loq-injection collector current density J_C in a Si BJT is given by

$$J_C \sim \eta_0(T) T^3 e^{-E_{gb}/kT} e^{E_{R_{bi}}/kT} e^{qV_{BE}/kT} \; . \tag{2.1}$$

In that equation, $\eta_0(T)$ accounts for the temperature characteristic of the diffusivity of electrons in the base, E_{gb} is the bandgap in the base (including both heavy-doping-induced and Ge-induced bandgap narrowing), and $E_{R_{bi}}$ represents the activation energy for freeze-out in the base. In modern devices, the base is doped highly enough ($>1 \times 10^{19}$ cm^{-3}) that carrier freeze-out does not occur, so the $e^{E_{R_{bi}}/kT}$ term can be dropped. There are two major takeaway features from this equation: the slope of J_C, when plotted in log scale against V_{BE} (the so-called Gummel characteristic), increases, and the entire characteristic shifts towards higher V_{BE} values. This shift can be seen in Figure 2.1. Note, however, that in that figure this trend seems to stop below 36 K. Going further down in temperature does not cause the low current slope to increase further, and the shift right stops so that the curves essentially superimpose over each other. This is a feature of SiGe HBTs that is not captured by the previous ideal collector current expression. This behavior is widely attributed to tunneling currents [25, 26]. At very low temperatures, the classical currents described by drift-diffusion transport are overwhelmed by the tunneling current, which occurs as electrons tunnel directly from the emitter to the collector through the base. The

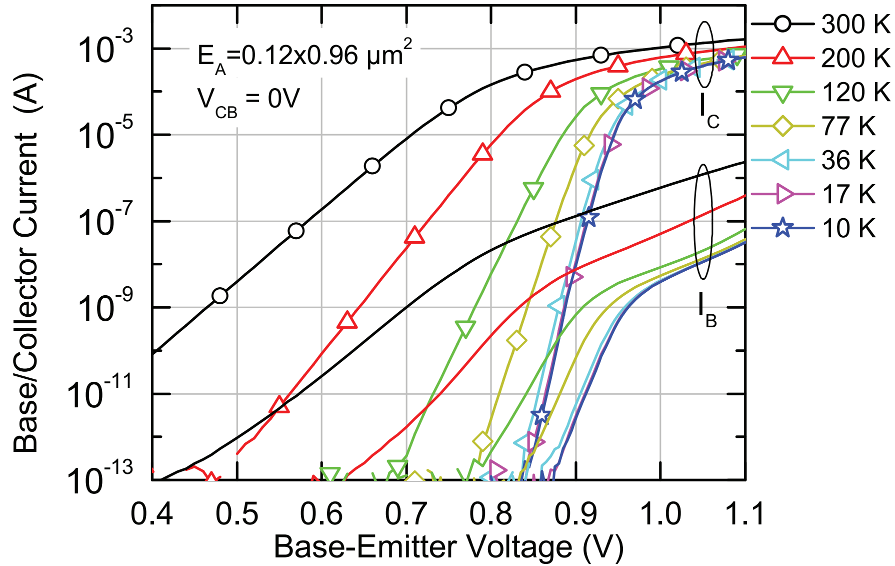

Figure 2.1: Collector current I_C and base current I_B across V_{BE} as temperature is decreased, from [25]. The saturating effect of tunneling is visible below 36 K.

saturating behavior is most clearly observed by looking at the transconductance g_m at a given I_C across temperature. Classical theory gives the expression for transconductance

$$g_m(T) = \frac{qI_C}{kT} \; . \tag{2.2}$$

At a fixed I_C, then, g_m should be proportional to $1/T$. However, when plotted across temperature, the saturation behavior results in a deviation from this behavior. A plot of g_m against $1/T$ is shown in Figure 2.2 (from [26]). There is a very clear breakpoint around 40 K where the transconductance stops increasing. Since both I_C and I_B saturate, the current gain also saturates.

It will be useful to have an equation for the tunneling current in order to have an intuition of what it depends on. [27] provides physics-based equations for this purpose. That work divides the math into two regions of operation: one where the potential barrier height formed by the base is less than the Fermi level, and another region where the potential barrier is greater than the Fermi level. In order to compare directly to the low-injection

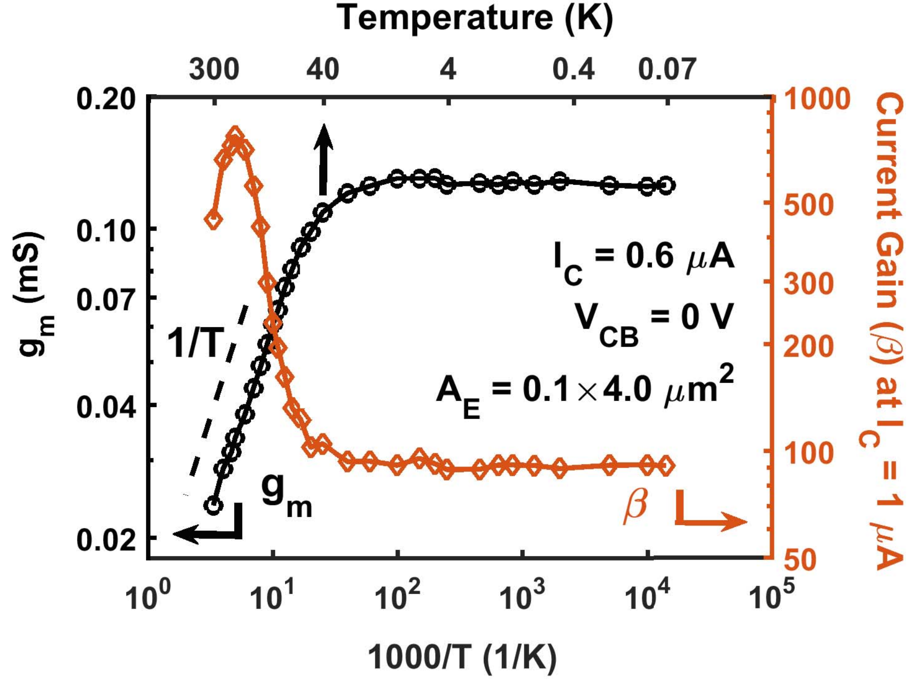

Figure 2.2: Transconductance g_m and current gain β plotted against $1/T$, from [26]. The saturating effect of tunneling is visible in the g_m curve below 40 K.

drift-diffusion formula and eliminate high-injection effects from consideration, this work will focus on the latter case. For this region, direct tunneling dominates, and the expression for J_C is given by

$$J_C = \frac{c_T}{B}\Delta W_E \left[\frac{e^{B\Delta W_E} - 1}{B\Delta W_E} - 1\right] e^{-BW_b} \; . \tag{2.3}$$

In Equation 2.3, the barrier height W_b is determined by the difference between the built-in potential of the base-emitter junction V_{DEi} and the base-emitter voltage. It is defined as $W_b = q(V_{DEi} - V_{BE})$. The difference between the Fermi level and conduction band in the emitter is ΔW_E. c_T is a constant. B is proportional to $1/\sqrt{W_b}$ and dependent on bias. Note that the exponential term e^{-BW_b} is equal to $e^{-Bq(V_{DEi}-V_{BE})}$. Since there is an exponential dependence on V_{BE} just as in the classical drift-diffusion case, the linear shape of the Gummel characteristic at low injection should be preserved just as in the classical drift-diffusion equation. However, there is no temperature term in the exponent, so the slope remains the same, as it should given the measured characteristics. This is true in

practice for I_C, but it is important to note that measured I_B curves show highly non-ideal behavior, and this characteristic is yet to be explained by the literature.

2.2 Mechanical Stress

The understanding that strain impacts the electrical properties of semiconductors has long been known, going back to the foundational work of Bardeen and Shockley [28, 29]. The intuitive reason for this is simple: mechanical stress causes physical deformation (strain) of the lattice structure. Since the electrical properties of semiconductors arise directly from the physical lattice structure, this deformation must have an impact on the electrical properties of the semiconductor. Modeling the precise effects of arbitrary strain on the band structure and mobility is where the physics gets complicated. The most straightforward aspect of strain is its impact on band edges. When strain is present in a semiconductor, the band edges are shifted and warped. This is commonly described by so-called deformation potential theory [17], which states that the band edge shift is proportional to a deformation potential tensor. In order to capture these band edge shifts fully, a device simulator which takes into account the full band structure is needed. However, because of the computational intensity of this approach, many device simulators simply lump the bad edge shifts into an equivalent bandgap narrowing ΔE_g. This simplified view of stress as causing bandgap narrowing will be useful in understanding how stress affects SiGe HBTs.

The other important aspect of how stress impacts devices is related to how mobility changes under strain. Because strain warps the energy bands in addition to shifting them up and down, the effective masses change, resulting in a change of carrier mobilities. More sophisticated methods than deformation potentials are typically used here, a common one being the empirical pseudopotential method (EPM) [30]. Then, solving the Boltzmann equation (typically a Monte-Carlo based approach [31]) and applying the Kubo-Greenwood formula [32] gives the mobility. Depending on the direction of applied stress and whether it is compressive or tensile, mobilities can increase or decrease. Figure 2.3 shows the effect

of strain on electron mobility in intrinsic silicon.

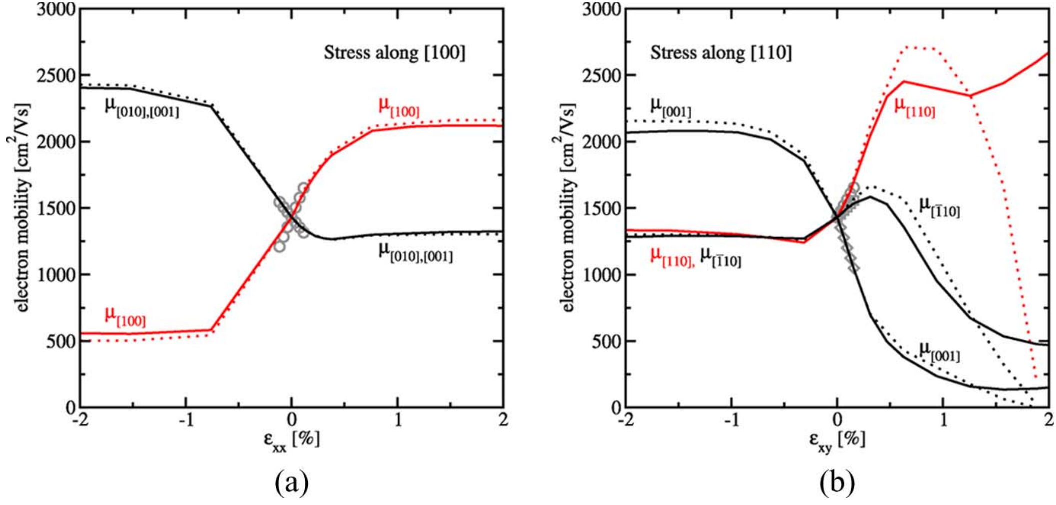

Figure 2.3: Computed electron mobility in intrinsic Si as a function of strain, shown for stress along [100] (a) and [110] (b) [33].

2.3 Back-End-of-Line Stress

Mechanical stress can be caused by a variety of factors, including external applied stress, stress from packaging, engineered stress layers designed to improve device performance, stress from through-silicon vias (TSVs), and stress caused by the back-end-of-line (BEOL). This work focuses on stress caused by the back-end-of-line. The back-end-of-line encompasses the oxide and metal layers above the silicon substrate, which serve the purpose of forming interconnects, capacitors, and inductors. The stackup from a process fabricated by IHP is shown in Figure 2.4. BEOL processing produces mechanical stress because of the mismatch between thermal coefficients of expansion between all the materials used. Copper and aluminum have higher coefficients of thermal expansion than silicon, which itself has a higher thermal expansion coefficient than oxide. Nominal thermal expansion coefficients for these materials at 300 K are listed in Table 2.1. Since the processing for the BEOL layers is done at elevated temperature, there is built-in stress once the die is cooled down to room temperature. The particular amount of stress that results depends on the

particular fabrication details of the process in question.

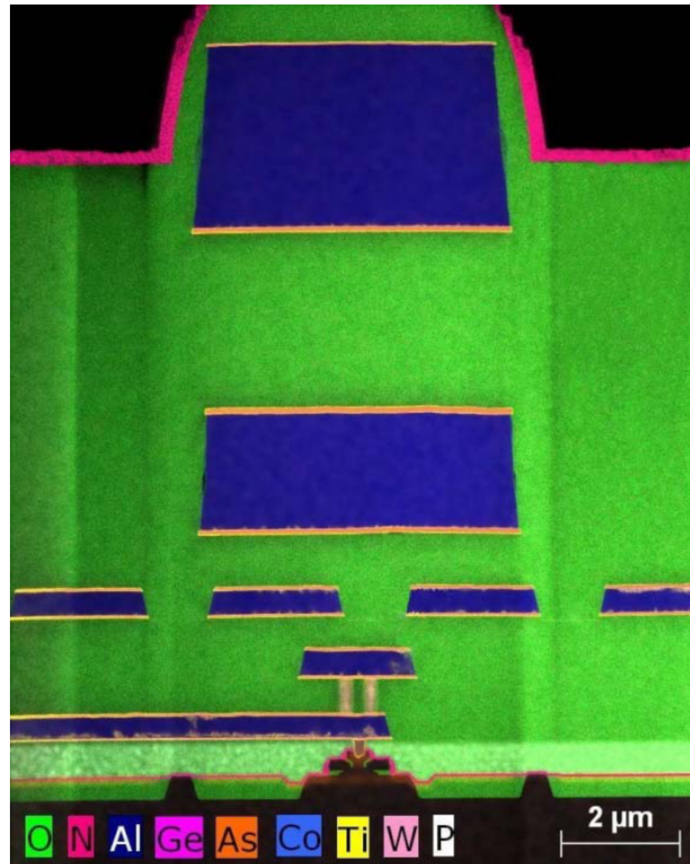

Figure 2.4: Cross section of the 5-layer metal stackup in an IHP process [23]. The HBT is the centered black mound at the bottom.

Table 2.1: Thermal expansion coefficients for common materials at 300 K.

Material	α ($\times 10^{-6}$ K^{-1})	Reference
Cu	16.71	[34]
Al	23.02	[34]
Si	2.63	[35]
SiO_2	0.24	[36]

2.4 Effect of BEOL Stress in SiGe HBTs

There have been two major studies that have looked at the impact of mechanical stress on SiGe HBTs. In [23], stress values were simulated with a process simulator. In that process,

stress in the vertical direction, normal to the plane of the die (hereafter referred to as out-of-plane stress) was the dominant contribution from BEOL stress. In the worst case from that study, an additional 380 MPa of stress resulted from a stack of metal added over the device. Measurements showed a collector current increase over a control device biased at the same V_{BE}. The study in [22] used a similar methodology to look at the effect in a process from STMicroelectronics. That work measured the change in AC characteristics, showing an increase of 21% in f_T and 12% in f_{max}. The improved high frequency performance was attributed to an increase in electron and hole mobility in the base.

In order to interpret measurement results, it is important to understand the theoretical impact of stress in a SiGe HBT. In order to simplify the analysis, a number of simplifications are required. One of these is to focus on the DC characteristics of the device. As will be shown below, the change in DC characteristics depend mainly on the induced bandgap narrowing, while AC characteristics depend on a much more complicated combination of bandgap narrowing and mobility enhancement. Additionally, small changes to the DC characteristics are easy to measure and very repeatable. AC measurements of f_{max} and to a lesser extent f_T are much more difficult to make accurately and therefore resolving the small differences that arise from stress is difficult (although not impossible). Another simplification is focusing on the low-current region of operation. There are two reasons for this. One is that the ideal closed-form solution to J_C in SiGe HBTs is limited to low injection. High-injection effects, although well-modeled in various compact models, do not yield a nice closed-form solution. The second reason is to eliminate self-heating from consideration. Adding BEOL metals near a SiGe HBT results in a noticeable reduction of thermal resistance [37]. At high currents, this would be a confounding variable.

The ideal closed-form solution for the collector current density in a linearly graded

SiGe HBT is given in [12]:

$$J_{C,SiGe} = \frac{qD_{nb}}{N_{ab}^{-}W_b}\left(e^{qV_{be}} - 1\right) n_{ib}^2 e^{\Delta E_{gb}^{app}/kT} \cdot \left\{ \frac{\widetilde{\gamma}\widetilde{\eta}\ \Delta E_{g,Ge}(grade)/kT\ e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\} . \tag{2.4}$$

In this expression, D_{nb} is the electron diffusivity in the base, N_{ab}^{-} is the doping in the base, and W_b is the base width. The intrinsic carrier concentration in the base is n_{ib}^2, and heavy-doping induced bandgap narrowing in the base is ΔE_{gb}^{app}. The terms $\widetilde{\gamma}$ and $\widetilde{\eta}$ describe the effective density-of-states ratio ($(N_C N_V)_{SiGe}/(N_C N_V)_{Si}$) and electron diffusivity ratio ($(\widetilde{D_{nb}})_{SiGe})/(D_{nb})_{Si}$), respectively, both averaged over position in the base. The term $\Delta E_{g,Ge}(grade)$ represents the amount by which the germanium content increases from the emitter-base (EB) junction to the base-collector (BC) junction (a linear grading is assumed). The term $\Delta E_{g,Ge}(0)$ is the germanium fraction at the EB junction. The terms in Equation 2.4 which depend on stress are just D_{nb} and n_{ib}^2. The electron diffusivity comes into play because it is proportional to electron mobility. The n_{ib}^2 term results in a collector current that is proportional to $e^{-E_g/kT}$. Under stress-induced bandgap narrowing, a term $e^{\Delta E_g/kT}$ can be pulled out. Taking this into account, a proportionality can be written

$$I_C \propto \mu_{nb} e^{\Delta E_g/kT} . \tag{2.5}$$

Equation 2.5 describes the effect of stress on SiGe HBTs at low injection. In practice, the μ_{nb} term can be dropped because the contribution of the mobility change is small compared to that of bandgap narrowing. Sentaurus Band Structure, which uses EPM and the Kubo-Greenwood formula to calculate mobility [38], predicts a 3.0% increase in electron mobility at 300 K with 100 MPa tensile out-of-plane stress (a reasonable value for BEOL test structures [23]). In comparison, bandgap narrowing for the same tensile stress contributes to a 28.8% increase in I_C (a narrowing of 6.54 meV). At 77 K and 100 MPa stress,

those values become 9.0% and 168.0%, respectively. Note that the simplified expression

$$I_C \propto e^{\Delta E_g/kT} \tag{2.6}$$

takes the same form as the V_{BE} dependence $I_C \propto e^{qV_{BE}/kT}$. This hints that there are two ways to view this change due to stress: as a thermally activated multiplication factor for I_C, as in Equation 2.6, and as a factor lumped in with V_{BE} (giving the proportionality $I_C \propto e^{q(V_{BE}+\Delta E_g/q)/kT}$). The second option, with the stress effect lumped in as a factor with V_{BE}, will be referred to as an equivalent V_{BE} shift (ΔV_{BE}). This quantity is useful because it is independent of temperature. The expression for equivalent V_{BE} shift is

$$\Delta V_{BE} \approx \Delta E_g/q \; . \tag{2.7}$$

It is also interesting to consider the impact of stress on base current. This work will not attempt a rigorous derivation since the non-ideal base current at cryogenic temperatures is still unexplained. However, an intuitive understanding can point towards the expected impact. Consider the band structure of a device under mechanical stress, as illustrated in Figure 2.5. In p-type silicon, stress-induced bandgap narrowing occurs primarily in the conduction band, while for n-type, it occurs primarily in the valence band [39]. Therefore, stress-induced bandgap narrowing in the base causes a reduction in the energy level of the valence band of the base. This increases the injection of electrons from the emitter to the collector, which increases collector current as expected from Equation 2.5. Similarly, bandgap narrowing in the emitter causes an increase in the conduction band level in the emitter. This increases the back-injection of holes from the base into the emitter. This current is the primary component of the base current. Therefore, it is expected that the base current should increase in a similar fashion to the base current. Since the effect is dependent on energy offsets in the band edge, the increase in base current should be thermally activated just like the collector current.

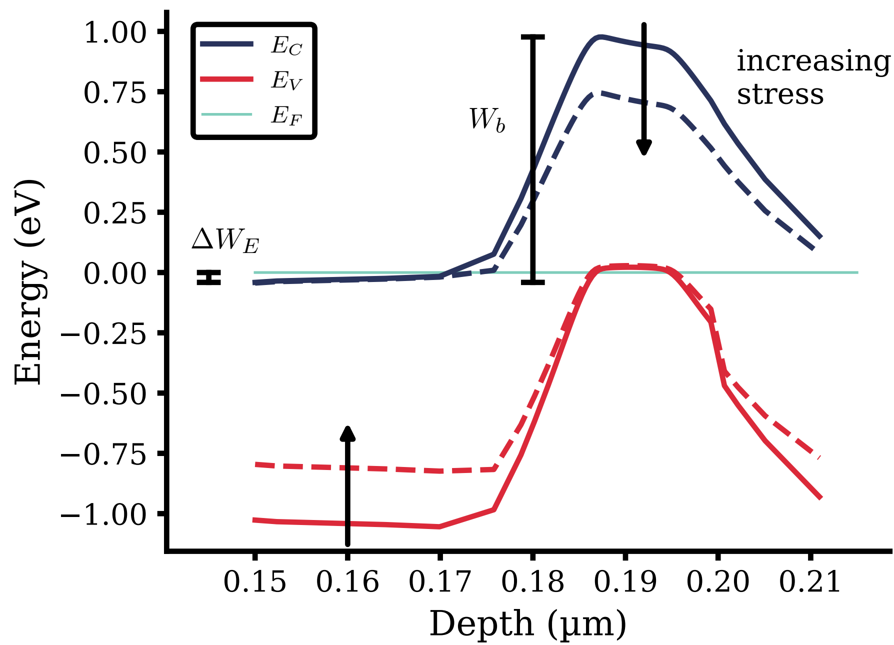

Figure 2.5: Simulated band structure at 75 K showing conduction band level E_C, valence band level E_V, and Fermi level E_F, with all device terminals grounded. W_b and ΔW_E are the base barrier height and difference between Fermi level in the emitter and conduction band in the emitter, respectively. The dashed lines represent a device under 5 GPa tensile stress.

Equation 2.4 is valid for room temperature and a wide range of temperatures around room temperature where the transport physics follow the classical drift-diffusion model. However, at deep cryogenic temperatures below $\sim$40 K, transport is dominated by tunneling. The question then arises whether this transition to tunneling-dominated transport changes the dependence on stress. The relevant quantity in Equation 2.3 which depend on mechanical stress is W_b. This is illustrated in Figure 2.5. Because bandgap narrowing in the emitter occurs in the valence band, ΔW_E is not changed as a result of stress. Accounting for stress, the new equation for W_b is given as

$$W_b = q(V_{DEi} - V_{BE}) - \Delta E_g \ . \tag{2.8}$$

Rearranging, this can be written as

$$W_b = q(V_{DEi} - (V_{BE} - \Delta E_g/q)) \ . \tag{2.9}$$

Clearly, this lead to an equivalent V_{BE} shift of $\Delta V_{BE} \approx \Delta E_g/q$, which is identical to Equation 2.7. This is an important and surprising point. Despite the transition to a completely different transport physics, the effect of stress a cryogenic temperatures takes on the exact same form as at room temperature (at least for collector current). As temperature decreases from room temperature to deep cryogenic temperature, there is no expected breakpoint or different trend; a direct measurement of ΔV_{BE} should remain valid over the entire temperature range. In hindsight, there is an intuitive explanation of this point. Mechanical stress causes a decrease in the conduction band level in the base, which is the exact same result as increasing V_{BE}. This is true for the conduction band; the valence band effect is different, but the valence band impacts the base current, not the collector current. So regardless of the particular details of the physics at play, stress-induced narrowing should appear additive to V_{BE}. This results in the equivalent V_{BE} shift.

Given the more complicated physics operating at cryogenic temperatures, it is necessary

to validate this finding with measurements.

CHAPTER 3

MEASUREMENT OF BEOL STRESS

3.1 Methodology

In order to measure the impact of BEOL stress on a device, two structures are necessary: a control device, and a device with additional BEOL stress. By comparing the DC characteristics of these two devices, it is possible to measure the I_C increase and equivalent V_{BE} shift. The additional BEOL stress can be introduced by adding metal shapes above and in the vicinity of the active devices. The devices used in the present work were from a fourth-generation, 90-nm SiGe BiCMOS process with f_T/f_{max} of 300/350 GHz at 300 K. The device size was 0.1×5 µm. The control device consited of the HBT with electrical connections made on the first metal layer. These connections were routed away from the device before connecting to the upper thick metal layers. This was done to ensure that no thick upper metal layers were present within 10 µm of the active device. Typically, all non-excluded area of a die is filled in with floating pieces of metal fill on each layer in order to ensure planarity of each layer and mechanical integrity of the mask layers. In order to avoid the effect of this fill, metal fill was excluded on all layers to at least 10 µm away from the device. An illustration of the layout of the control device is shown in Figure 3.1.

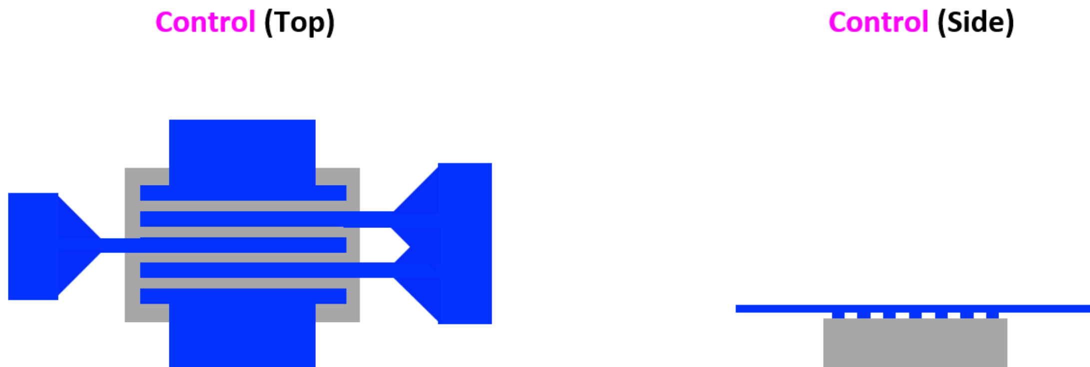

Figure 3.1: Top-down view and cross-section of test structure for the control device.

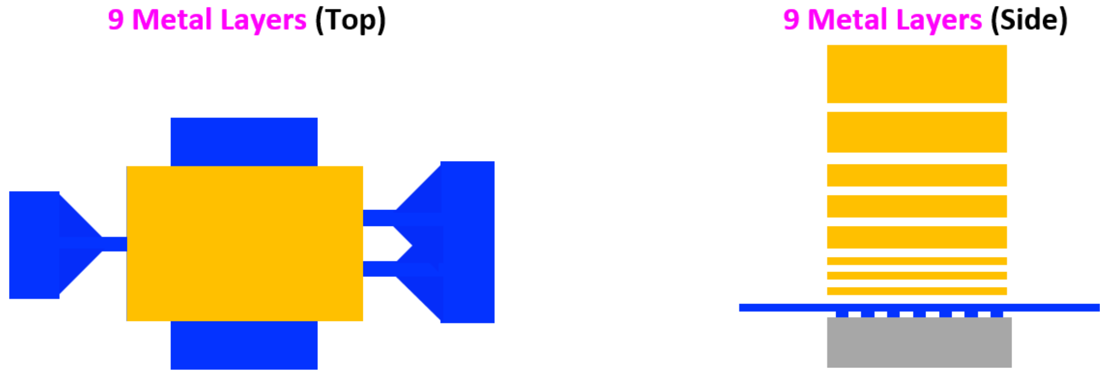

Figure 3.2: Top-down view and cross-section of test structure for the stressed device with 9 total metal layers.

The test structures with additional BEOL stress is identical to the control device with the addition of floating metal layers directly above the device. These floating metal rectangles were not electrically connected to the device, so any effect from them is limited to mechanical stress and a reduction in thermal resistance. As mentioned before, limiting the analysis to the low current region allows eliminating the effect on thermal resistance from consideration. The metal rectangles were sized to cover exactly the active device. Three versions of the stressed control structures were laid out: one with two additional metal layers, for a total of three layers, one with 5 additional metal layers, for a total of 6 layers, and one with 8 additional metal layers, for a total of 9 layers. The 3-metal-layer version uses the three lowest metal layers, the 5-metal-layer version the 5 lowest layers, and the 9-metal-layer version the 9 lowest metal layers. The 9-metal-layer test structure is shown in Figure 3.2. Since the versions with increased numbers of metal layers have more metal layers and move vertically upwards where the metal layers are thicker, it is reasonable to expect that the amount of stress should be largest in the 9-metal-layer device.

Identical structures from two different lots were measured to ensure repeatability of the results. Measurements were conducted in a closed-cycle cryostat probe station from Advanced Research Systems. Measurements were conducted from room temperature down to 13 K. Temperature was regulated by a Lakeshore 336 temperature controller. DC connections were provided through a terminated coaxial cable with RF probes to avoid oscillation.

Gummel characteristics (V_{BE} vs. I_C at a fixed collector-base voltage V_{CB}) were measured using an Agilent 4155 Semiconductor Parameter Analyzer.

3.2 Results

Figure 3.3 shows a measured Gummel from a control device (solid) and one of the 9-metal-layer stressed test structures (dashed). The left curve is taken at 295 K, and the right is taken at 13 K. This Gummel matches well with the theory discussed previously. For both the 295 K and 13 K measurements, the collector current is increased at a fixed V_{BE}. Since the slope of the 13 K curve is greater, the I_C increase at a given V_{BE} is clearly greater at low temperature, as expected. It is also visually clear what is meant by an equivalent V_{BE} shift: the Gummel makes a shift to the left by ΔV_{BE}. Comparing the 13 K curve to the 295 K curve, it appears that ΔV_{BE} is greater at cryogenic temperatures. That is an interesting observation, since at a given amount of stress (and therefore bandgap narrowing), the theoretical ΔV_{BE} is independent of temperature. In order to investigate further, ΔV_{BE} was plotted as a function of I_C at multiple temperatures. This is shown in Figure 3.4. In that figure, I_{C0} represents the collector current of the control device.

The trend of ΔV_{BE} across temperature shows that there is an increase of stress occurring as temperature decreases. Since ΔV_{BE} at a given stress is independent of temperature, the observed increase must be caused by an increase of stress. Since ΔV_{BE} approximately doubles from 295 K to 13 K, the implied reduction in bandgap ΔE_g must also be approximately doubling. This increase of stress is caused by the mismatched thermal coefficients of expansion. Just as cooling the deposited metal and oxide down from processing temperature to room temperature causes built-in stress, further cooling the die to cryogenic temperatures increases that stress. This factor is going to contribute to BEOL stress effects being larger at low temperatures.

The second way of viewing the effect of stress, as an increase of I_C at a fixed V_{BE}, gives a better view of how significant these stress effects are at each temperature. Figure 3.5

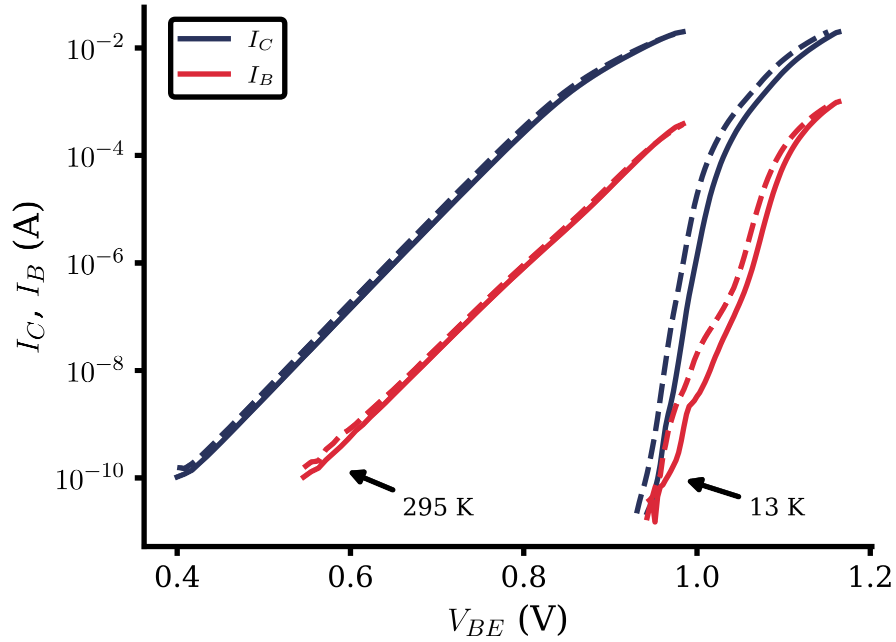

Figure 3.3: Gummel characteristics with $V_{CB} = 0$ of a control (solid) and stressed (dashed) device at 295 K and 13 K.

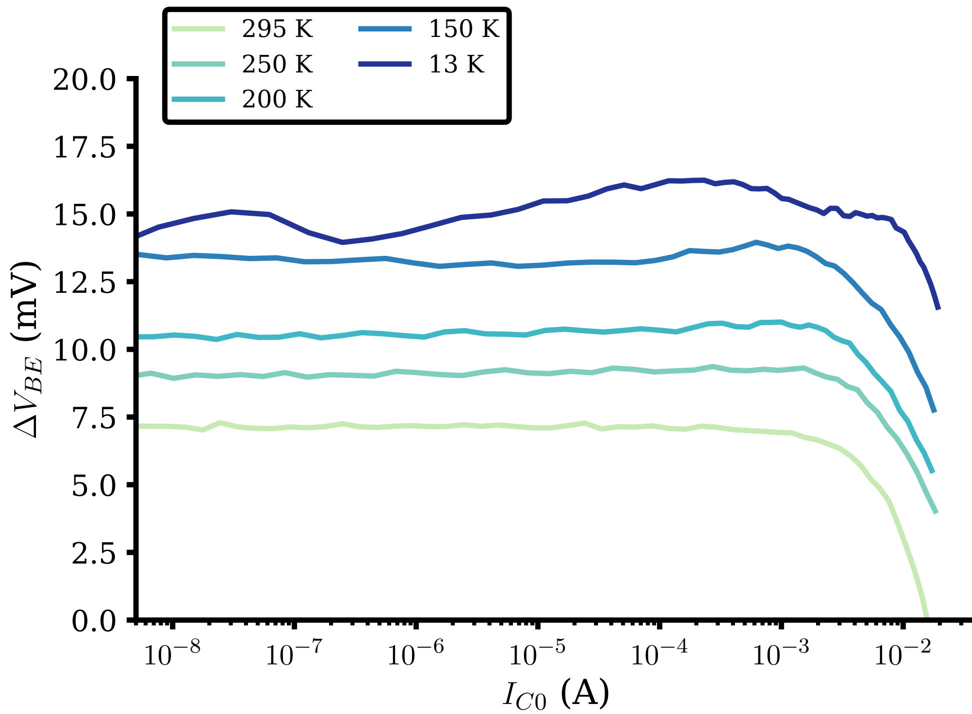

Figure 3.4: ΔV_{BE} increase in the stressed device compared to the control device across bias.

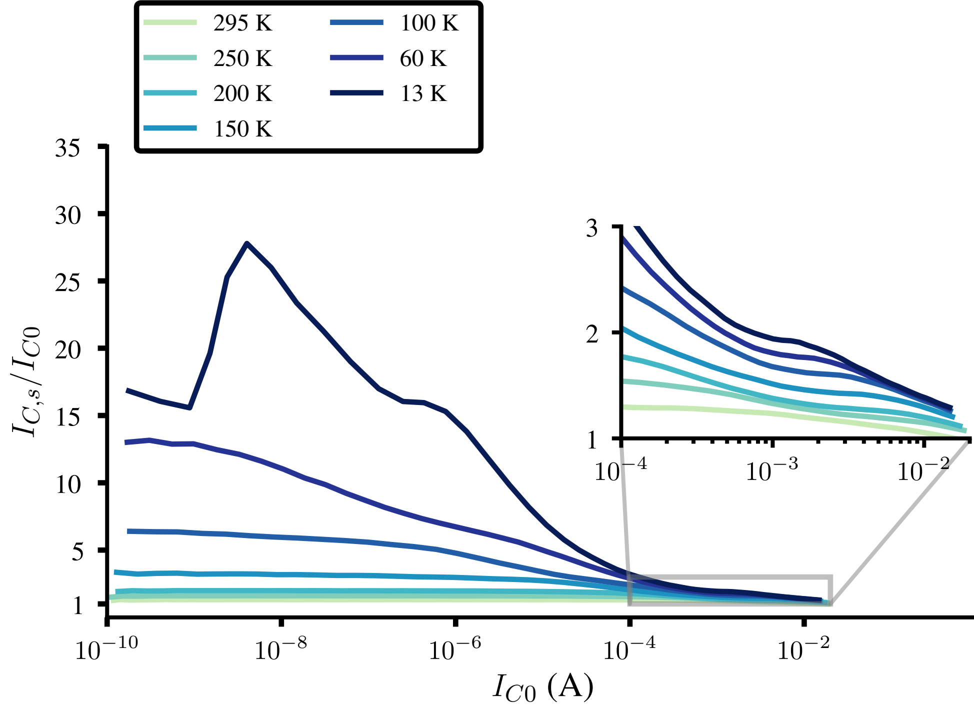

Figure 3.5: I_C increase in the stressed device compared to the control device across bias.

shows that the increase in stressed collector current $I_{C,s}$ over the control current I_{C0} is strongly enhanced as temperature decreases. Note that the increase in I_C is greater than 20× at 13 K. At higher currents, the I_C increase rolls off, but it remains greater than 2× for useful circuit biases at 13 K. Clearly this effect is very significant regardless of the region of operation. Furthermore, the effect on I_C is numerically much larger than the ΔV_{BE} shift and more strongly enhanced with cooling. This is a result of the exponential dependence on $1/kT$. Even given constant stress and a constant ΔE_g, the $1/kT$ dependence would amplify the impact to I_C with cooling. This is combined with the increase in the amount of stress, resulting in the extremely high sensitivity of I_C on BEOL stress.

The trend in ΔV_{BE} across temperature for the three different stressed structures (3-, 6-, and 9-metal-layer versions) is shown in Figure 3.6. The trend is roughly linear, with ΔV_{BE} approximately doubling from 300 K to 13 K for the most stressed 6- and 9-metal layers. Note that the 3-metal-layer version has comparatively little measured V_{BE} shift. This can

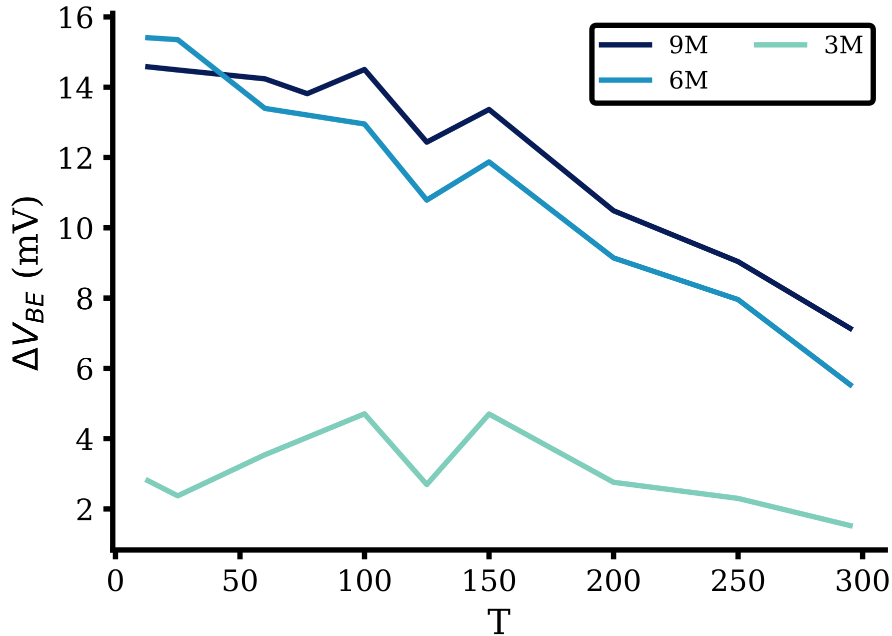

Figure 3.6: ΔV_{BE} increase in the stressed device compared to the control device across temperature.

be attributed to the fact that the three lowest metal layers are very thin and therefore have comparatively little contribution to stress. As the metal layers move upward, they get thicker. This is the reason for the large effect of moving from the 3-layer version to the 6-layer version. Despite the thicker metals, though, moving from the 6-layer version to the 9-layer version seems to add little additional stress. This can be attributed to the fact that the upper layers are further away from the device, so they have less impact. The sweet spot where the layers are thick enough to matter but still close enough to the device to have a large effect appears to occur in the middle three metal layers for this process. These layers have an outsized effect on adding BEOL stress.

Since BEOL stress is evidently a large concern at low temperatures, a natural question is what can be done to mitigate its effect. Some layouts should be result in less additional stress than others, and it would be useful to know which ones could pose problems. The most convenient way to address this question is to rely on mechanical stress simulations. Before attempting to draw conclusions, though, it is necessary to know whether mechanical

stress simulations combined with the theoretical expressions developed in section 2.4 can predict the changes observed at cryogenic temperatures.

CHAPTER 4
SIMULATING BEOL STRESS AT CRYOGENIC TEMPERATURES

4.1 Simulation Approach

There are three steps needed to predict the amount of V_{BE} shift as a result of stress. The first is to simulate the mechanical stress in the device. The second is to take the stress values from that simulator and compute a resultant amount of bandgap narrow ΔE_g. Finally this value of ΔE_g can be converted to an equivalent ΔV_{BE} through Equation 2.7 or an increase in I_C through Equation 2.6.

The setup for the mechanical simulator is fairly straightforward. Sentaurus Interconnect was used as the simulator. There are three pieces of information needed: the thermal expansion coefficients as a function of temperature, the mechanical properties across temperature (Poisson's ratio and Young's modulus, or equivalently bulk modulus and shear modulus), and the stress-free temperatures. Although default values for the material parameters are included in Sentaurus Interconnect for common materials, their temperature dependence is not included. However, it does allow inclusion of a table model to manually enter values at each temperature. Values for the thermal expansion coefficients and mechanical properties are readily available in the literature down to cryogenic temperatures [34, 40, 41]. The stress-free temperature is more difficult to determine since knowledge of the deposition temperatures is not available and generally a trade secret for the foundry. Reasonable guesses can be made based on published papers on processing techniques. The stress-free temperatures used in this work are based on [42]. In order to reduce simulation time, individual vias between metal layers were collapsed into larger vias with the same area. A cross-section of the simulation model is shown in Figure 4.1. The trenches into the silicon substrate (in gray) represent the deep trench isolation (DTI). The gray region inside

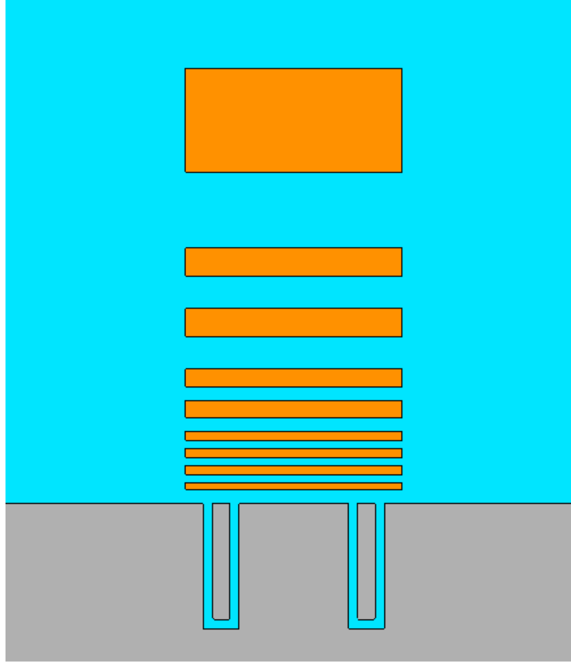

Figure 4.1: Cross-section of 9-metal-layer BEOL stress test structure.

the DTI models the polysilicon backfill inside the DTI.

Once the stress values averaged over the base region of the were obtained in Sentaurus Interconnect, it is necessary to convert the stress to a bandgap narrowing value ΔE_g. There are a variety of different methods to do this, but the simplest is to use the built-in models from a device simulator. This work uses the default stress modeling from Sentaurus Device.

4.2 Simulation Results

Simulation shows that the BEOL stress test structures put the device under tension in the out-of-plane direction and compression in the two orthogonal in-plane directions. This is illustrated in Figure 4.2. This is a result of the copper contracting more than the silicon and oxide as the structure is cooled, pulling upward on the device below and compressing it in the plane of the substrate. A detailed plot of the out-of-plane tensile stress is shown in Figure 4.3. This effect permeates fairly deep into the substrate and is largest near the border of the DTI. In contrast, the in-plane compressive stress is largest near the surface

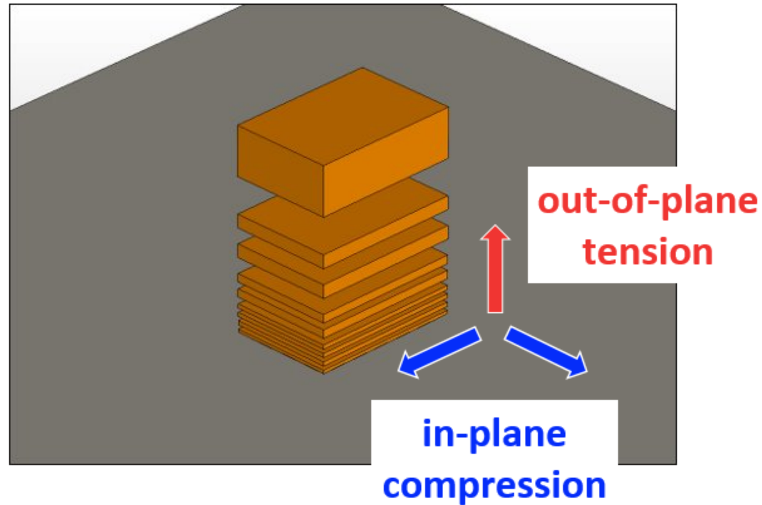

Figure 4.2: Illustration of the direction of stress in the device.

and falls quickly deeper in to the substrate. This is illustrated in Figure 4.4.

In order to validate the accuracy of the simulations, the simulated low-injection ΔV_{BE} was compared to the measured value across temperature. Two devices from different wafer runs were measured to ensure repeatability. Figure 4.5 shows that both measured devices show similar overall V_{BE} shifts and trends across temperature. The simulation matches very well at 300 K. At cryogenic temperatures, simulations show less increase in ΔV_{BE} than measured. However, this discrepancy is reasonable, given the incomplete knowledge of process parameters. An interesting characteristic of this plot is the nearly linear slope down to 13 K. This behavior is somewhat surprising given that the thermal expansion coefficient of copper decreases significantly below 100 K. However, simulations suggest that this decrease is compensated by a similar decrease in the thermal expansion coefficients of silicon and the oxide, both of which cross 0 and become slightly negative before approaching 0 near 0 K.

A convenient aspect of looking at stress in simulation is that it is possible to look at the individual elements of stress in each direction. It turns out that the temperature dependence of each component is a bit different. The trend across temperature is shown in Figure 4.6.

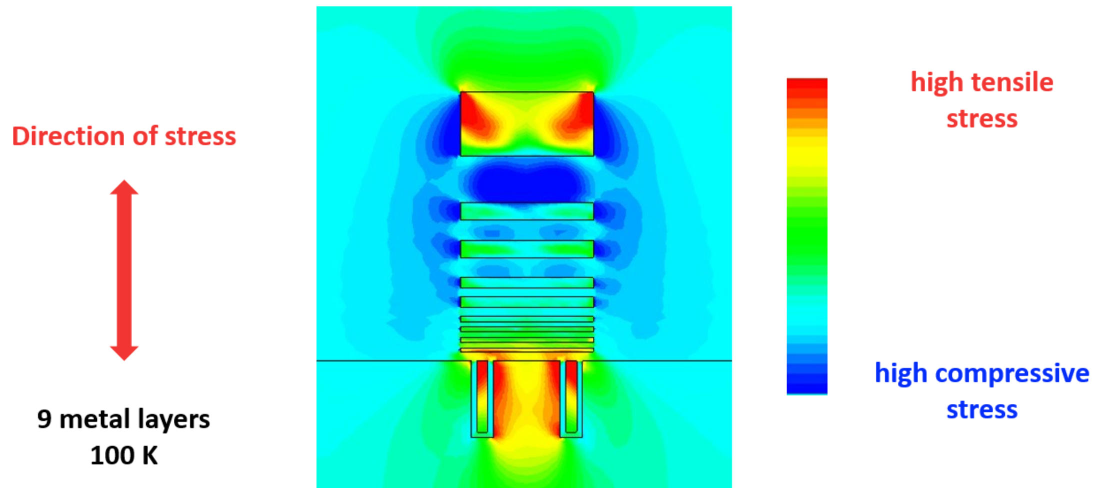

Figure 4.3: Simulation of out-of-plane stress at 100 K for 9-metal-layer test structure.

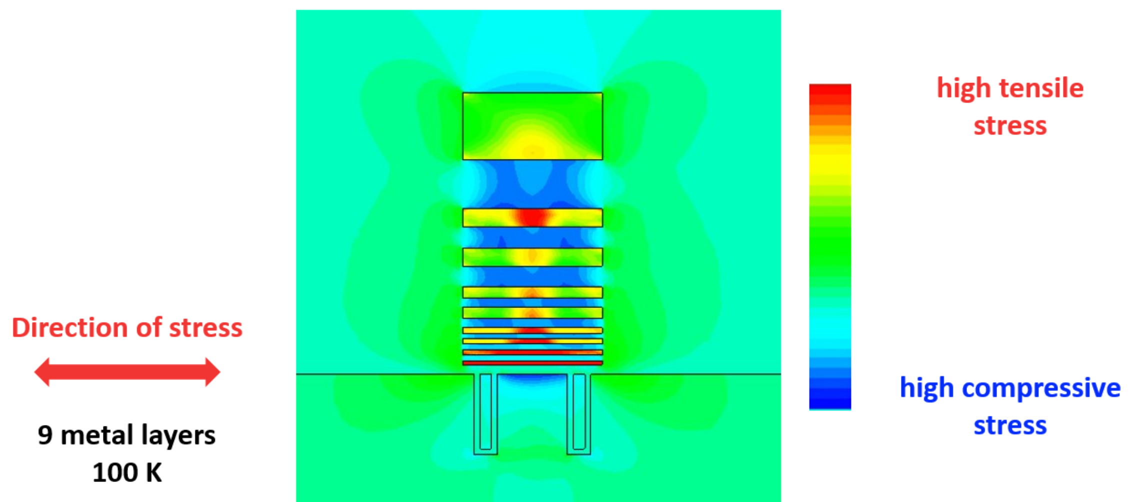

Figure 4.4: Simulation of in-plane stress at 100 K for 9-metal-layer test structure.

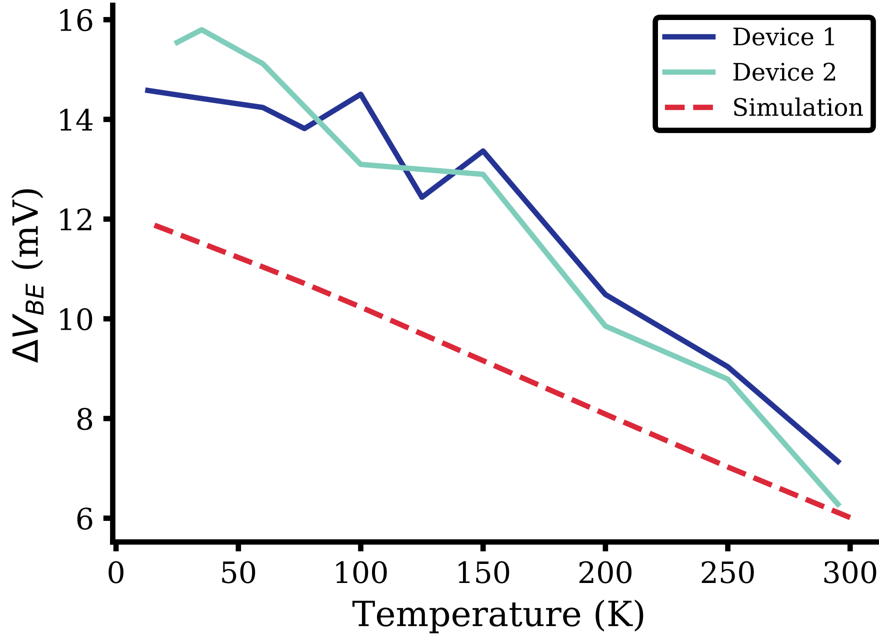

Figure 4.5: Measured ΔV_{BE} for devices from two different wafers (solid) compared to simulations (dashed). The measured ΔV_{BE} was averaged over a range corresponding to an I_{C0} from 5 nA to 500 nA.

This figure shows that at room temperature, the dominant component of stress is the out-of-plane tensile component. This component grows with cooling, but not as fast as the in-plane components. Because of the bigger increase in the in-plane components with cooling, at 13 K these components are larger than the out-of-plane component. Therefore the increase in stress effects overall can be largely attributed to the increase in the in-plane components.

Simulations were also carried out omitting the deep trench isolations in order to evaluate what role these structures have on stress in the device. In this case, the out-of-plane component remained essentially unchanged, but the in-plane components of stress were reduced to close to 0. At deep cryogenic temperatures, they remain small. Since the increase in BEOL stress effects can be attributed largely to the in-plane components, this means devices fabricated without a DTI should experience a smaller increase in ΔV_{BE} at low temperatures. Additionally, they should have a lower ΔV_{BE} to begin with at room temperatures. Since some processes forego the DTI in favor of diffused isolations while

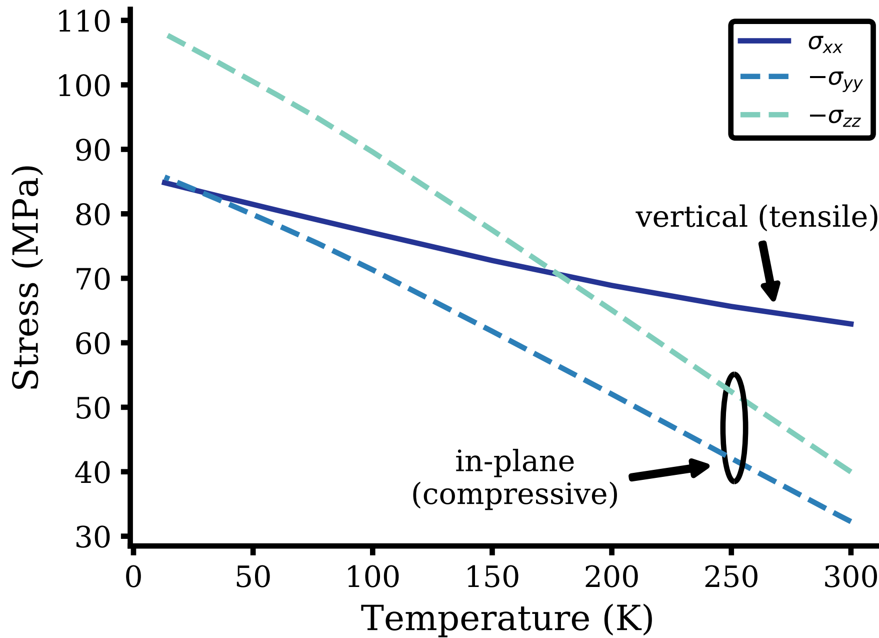

Figure 4.6: Simulated stress values for the out-of-plane direction (σ_{xx}), in-plane direction along the width of the device (σ_{yy}), and the in-plane lengthwise direction (σ_{zz}).

others stick with the DTI, knowing this information about a process gives an idea of what to expect in terms of the increased importance of BEOL stress at low temperatures. Processes with a DTI should be more sensitive.

4.3 Comparison of Interconnect Layouts

To illustrate the utility of having a calibrated simulation for stress at cryogenic temperatures, simulations were conducted for two common approaches to making electrical contact to the devices from the thick upper metal layers. One is to connect directly from the device upwards to the top metal layer. This approach is beneficial because it limits the length of the route on the lower layers, which are typically thinner and therefore have more loss. However, there will be more capacitance between the routes because they are placed close to each other. This approach will be referred to as the ”stacked” approach. The other approach is to gradually move outward as the route travels upwards. This minimizes the capacitance between the routes at the cost of loss in the lower metal layers. This approach

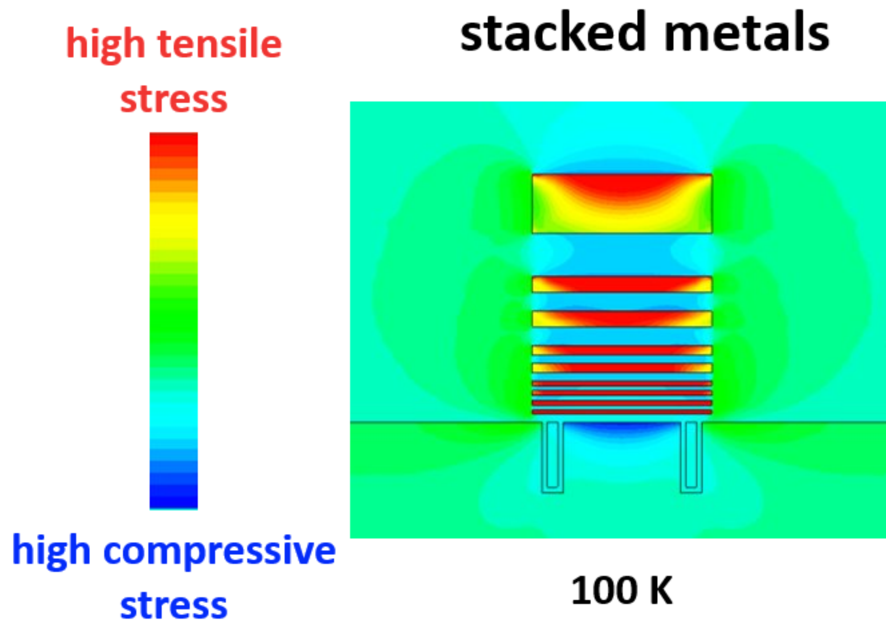

Figure 4.7: Simulation of in-plane stress at 100 K for stacked interconnect layout. The scale is the same as in Figure 4.8.

will be referred to as the ”staircased” approach. Simulations of the stress were performed for both the stacked (Figure 4.7) and staircased (Figure 4.8) versions. Since there is more metal above the device, the stacked version results in more stress in the device. Observe the deeper blue region under the stack in Figure 4.7, indicating more compressive stress. This simulation shows that even for realistic interconnect layouts, there can be significant differences in BEOL stress.

4.4 Effect of Metal Fill on BEOL Stress

In most commercial processes, metal fill is added to the design to ensure planarity and mechanical integrity of the masks. This fill is auto-generated and is added everywhere in the circuit that is not explicitly excluded. As mentioned in section 3.1, the test structures used in this work excluded the area around the device to avoid the impact of metal fill. However, it is useful to understand what the effect of that metal fill would be if it were

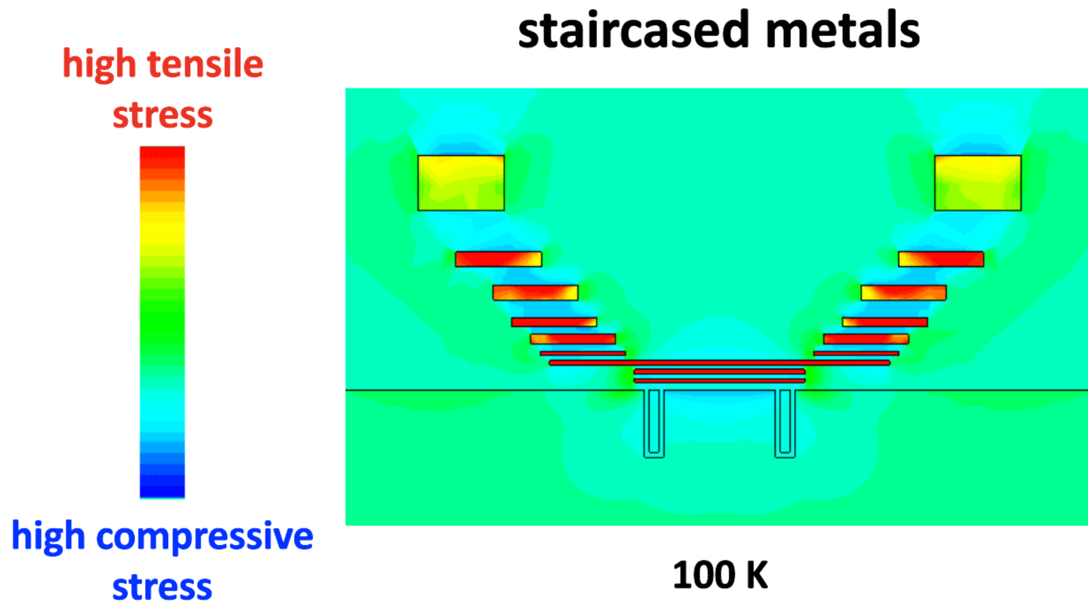

Figure 4.8: Simulation of in-plane stress at 100 K for staircased interconnect layout. The scale is the same as in Figure 4.7.

not excluded. To answer this question, simulation was employed using the same approach described in this chapter. To include the effect of the fill, floating metal squares were placed around the device with the same density as observed in the foundry's metal fill. The simulated structure is pictured in Figure 4.9.

The results of this simulation are shown in Figure 4.10. There are a few important features to note. One is that the in-plane compressive stress shows almost no change between the filled and excluded structures. The other is that the out-of-plane tensile stress is reduced in the filled structure. This comparison holds throughout the whole temperature range. The net result of this change is that the simulated ΔV_{BE} is reduced with the addition of metal fill. However, the difference is not huge, amounting only to 1 or 2 mV, a 10-15% reduction. This means that allowing fill around the device will somewhat decrease the severity of additional BEOL stress, but by itself it is not going to be a solution to eliminating issues caused by BEOL stress. It will still be necessary to evaluate the potential impacts circuits and consider other mitigation strategies.

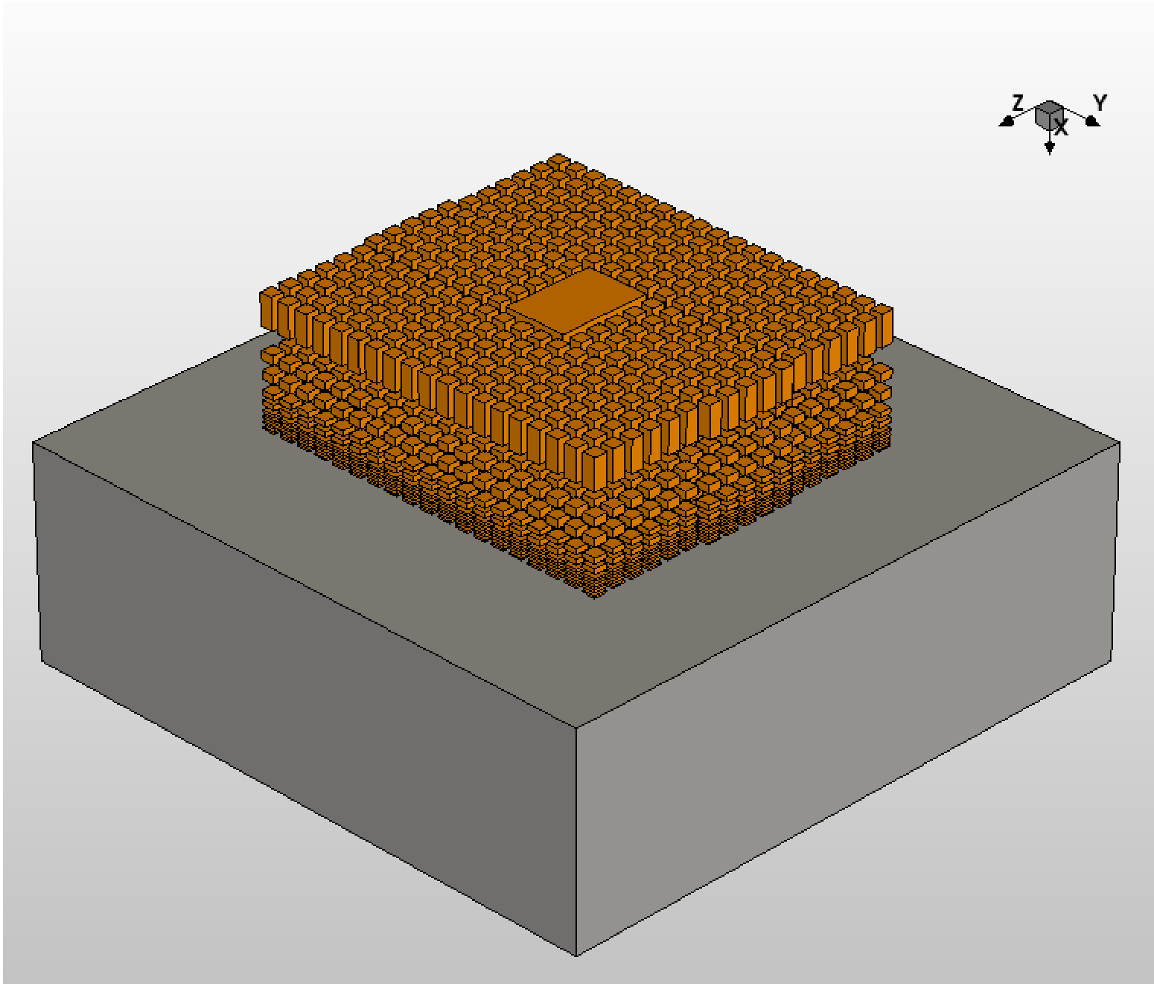

Figure 4.9: Simulated structure for comparison of filled and excluded 9-metal-layer test structure.

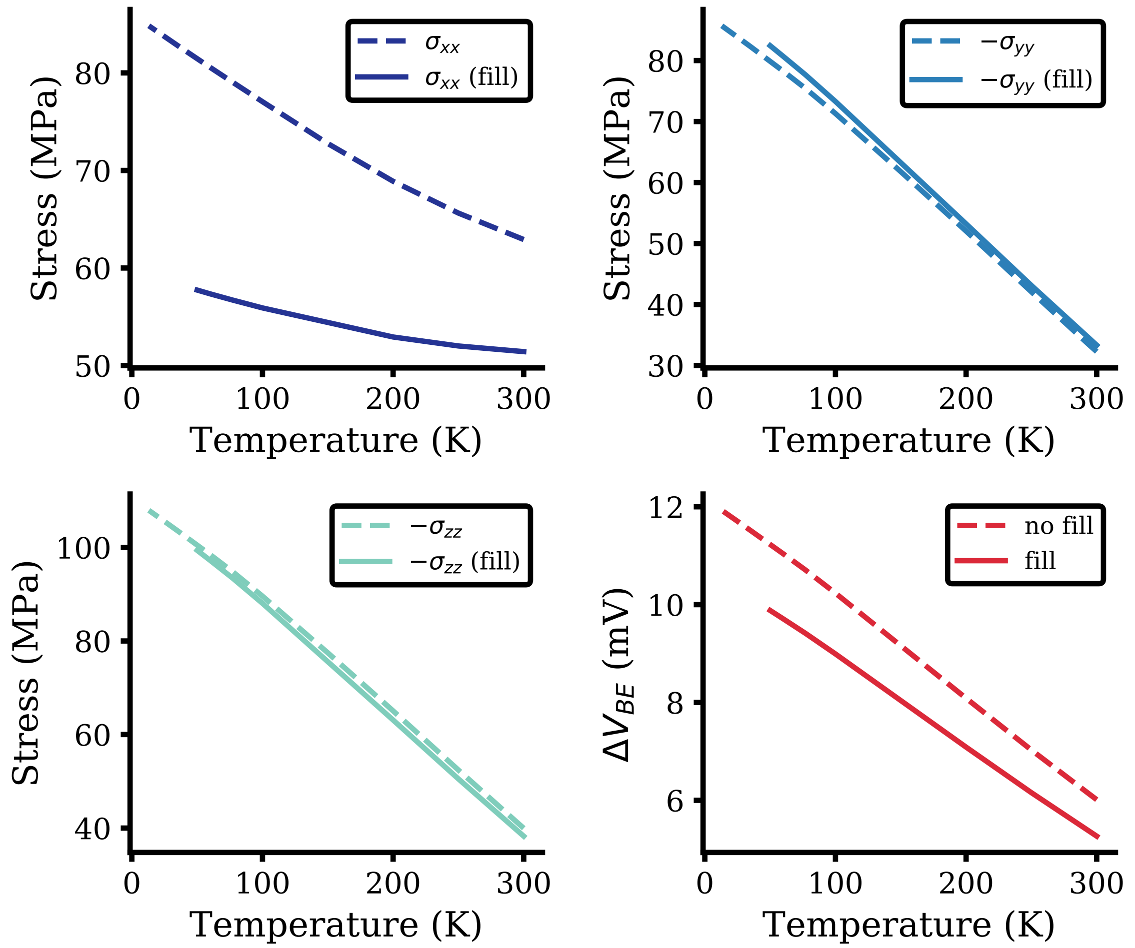

Figure 4.10: Simulated stress values and V_{BE} shift for the nominal 9-metal-layer structure with fill excluded (dashed) compared to the same structure with metal fill added (solid). Note the decrease in out-of-plane stress (σ_{xx}) in the filled case.

CHAPTER 5
IMPLICATIONS OF BEOL STRESS ON CIRCUIT DESIGN AT CRYOGENIC TEMPERATURE

There are a several considerations that have to be taken into account when determining how BEOL will affect a circuit. First, the good news: additional BEOL stress generally improves transistor performance. Other works have shown that devices with additional BEOL stress have higher f_T and f_{max} in the range of 10 to 20% [22]. This introduces an interesting possibility. By intentionally adding BEOL stress with metal layers over the device, devices and circuits should see increased performance. Furthermore, that performance increase should become even larger as circuits are cooled down to cryogenic temperature. However, there is a downside. This work has shown that DC characteristics undergo a significant shift as a result of BEOL stress. This can be a pitfall if not given proper considerations. Many analog circuits and biasing circuits for RF blocks require closely matched devices. Current mirrors in particular are very important. As shown previously, if one device of a current mirror were similar to the control device and the other were laid out similar to the 9-metal-layer test structure, the current mirror would experience a 20$\times$ mismatch at cryogenic temperatures. For op-amp-applications, the measured ΔV_{BE} will add directly to the offset voltage. These consequences are severe for analog circuits.

For RF circuits, there are other concerns as well. Circuit design uses compact models which are calibrated to particular test structures. Implicitly, this means that designers are using devices with a particular layout and amount of BEOL stress. If in the actual design the HBT is laid out differently, it will experience a different amount of BEOL stress, and this mismatch will become even larger as the device is cooled to low temperature. Since the device in the circuit will experience a different amount of stress, there is now unmodeled behavior in the fabricated circuit. If the actual device is experiencing more stress, it will

have more gain and could potentially be unstable. If it experiences less stress, it will have less gain and could fail to meet specifications. Either way, the unmodeled behavior is a problem.

Since these dangers are significant and become larger at cryogenic temperatures, it is important to understand what the mitigation strategies could be. The most effective approach is going to be ensuring that the relevant devices are laid out identically in their immediate vicinity. This goes for both devices that should be matched, as well as for the devices used to calibrate the compact models and the actual devices in the circuit. As was shown in Figure 4.5, devices with the same BEOL layout have similar stress even between devices from two different tapeout runs. This approach may not be feasible for certain high frequency applications where a compact layout and close routing is required. In that case, asymmetries in routing should be confined to the topmost metal layers, since those have less impact than the middle layers. In any case, if circuits are intended for operation at low temperatures, designers should consider independently biasing important HBTs and including some way of trimming the bias point. This would allow fine-tuning the operating point in a manner robust to BEOL-stress-induced DC operating point mismatch.

CHAPTER 6
FUTURE WORK

This work considered the impact of BEOL stress on DC characteristics of SiGe HBTs. One logical next step is to measure the AC characteristics of the same structures. This would allow extraction of the increase in f_T and f_{max} as a function of temperature. This would be a fairly challenging measurement since it would be necessary to resolve small differences in these AC figures-of-merit. The primary difficulty would be ensuring that the measured differences are repeatable and not a result of the natural scatter of measurements over multiple probe-downs. If done carefully, though, this data would be interesting to look at. Another interesting angle would be to look at the impact of BEOL stress on noise parameters. This could include both the high frequency noise parameters and the $1/f$ noise. Given the improved electron mobility, the high frequency noise should be expected to decrease with BEOL stress, but since there are many factors contributing it is difficult to predict how much. Another area which could be interesting to look at is how BEOL affects common analog circuits and approaches to mitigating these effects. For example, could a bandgap reference be devised which is insensitive to BEOL stress? Are there some designs which are more immune to BEOL stress than others? There are a number of circuits that would be interesting to test.

CHAPTER 7
CONCLUSIONS

This work has explored the impact of BEOL stress on SiGe HBTs at cryogenic temperatures. First the theory of the impact on I_C was discussed. It was shown that regardless of the temperature of operation, the effect of stress is primarily to introduce a shift in the Gummel equivalent to a shift in V_{BE} or an increase in I_C at a fixed V_{BE}. Second, the DC characteristics were measured experimentally down to 13 K. The layout of test structures designed to introduce additional BEOL stress was discussed. The results of these measurements were then compared to a control device. These measurements showed an increased sensitivity to BEOL stress as temperature is reduced. There are two contributing factors to this increased sensitivity. One is that the stress increases at low temperature because of the mismatched thermal expansion coefficients. The other is that for a given amount of stress, the resulting increase in I_C increases at low temperatures due to the the increased slope of the Gummel characteristic. An approach to simulation was explained which matches the measured trend in ΔV_{BE}. This calibrated simulation model was used to identify the in-plane compressive stress as a major driver of the increase in stress. Finally, mitigation strategies for addressing the potential pitfalls of BEOL stress in circuit design were discussed. The most important of these is to ensure identical layout between all devices required to be matched.

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