

GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION
SPONSORED PROJECT INITIATION

Date: September 21, 1976

Project Title: Adaptive Polarization ECM

Project No: A-1871

Project Director: ~~Mr. N. C. Hightower~~

H. W. Andrews

*Gr Cd
AF*

Sponsor: Aeronautical Systems Div. (AFSC); Attn: PPMEB: Wright-Patterson AFB, OH 45433

Agreement Period: From June 24, 1976 Until Feb 28/80 Feb. 28, 1978 (Perf. Period)

Type Agreement: Contract No. F33615-76-C-1250

TS

Amount: \$472,682 (Part. funded at \$110,000 thru 9/30/76)

Reports Required: Monthly R&D Status Reports; Program Schedule; TRACE Report; Final Technical Report; Presentation Materials; System Test Plan; Safety Statement; System Specifications; Engineering Drawings; Abstracts of:
Sponsor Contact Person (s): New Tech. (ANT); Opn. & Maint. Handbook

Technical Matters

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U. S. Air Force Avionics Laboratory
Air Force Systems Command
Wright-Patterson AFB, Ohio 45433

Contractual Matters

(thru OCA)

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325 Hinman Research Building
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Date 8/11/83

Project Title: Adaptive Polarization ECM

Project No: A-1871

Project Director: Harry W. Andrews

Sponsor: USAF/ASD(AFSC), Wright-Patterson AFB, OH

Effective Termination Date: 2/28/80

Clearance of Accounting Charges: 2/28/80

Grant/Contract Closeout Actions Remaining:

- ☒ Final Invoice and Closing Documents
- ☐ Final Fiscal Report
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A1871

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Number 11



REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER EES/GIT Project A-1871	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Operation and Maintenance Handbook for a Dual Circularly Polarized Antenna for Adaptive Polarization ECM		5. TYPE OF REPORT & PERIOD COVERED Final Report, March 1977 to December 1977
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) J. Gordon Neuberth David W. Rider		8. CONTRACT OR GRANT NUMBER(s) P.O. 08047-Q-20-600- A18-77-61400
9. PERFORMING ORGANIZATION NAME AND ADDRESS Nurad, Inc. 2165 Druid Park Drive Baltimore, Maryland 21211		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Georgia Institute of Technology Engineering Experiment Station Atlanta, Georgia 30332		12. REPORT DATE November, 1978
		13. NUMBER OF PAGES 94
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Georgia Institute of Technology Engineering Experiment Station Atlanta, Georgia 30332		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A
16. DISTRIBUTION STATEMENT (of this Report) Georgia Institute of Technology U.S. Air Force Aeronics Laboratory		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report) Georgia Institute of Technology U.S. Force Aeronics Laboratory		
18. SUPPLEMENTARY NOTES N/A		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Data Measurement Procedure Performance Data on Dual Circularly Polarized Antenna		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report covers the data measurement procedure and the resultant data obtained on the Nurad, Inc., dual circularly polarized antenna Model No. 8SDP2P, developed under contract with the Georgia Institute of Technology for use in adaptive polarization ECM systems. The data package includes appropriate radiation patterns, phase vs frequency, phase vs antenna positions, VSWR vs frequency, isolation vs frequency, axial ratio vs frequency, and gain measurement		

NURAD, Inc.

ANTENNAS

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TELEPHONE (301) 462-1700 TWX/TELEX (710) 234-1071

Operation and Maintenance Handbook

System Specifications and Drawings
(Volume 1 of 5)

EES/GIT Project A-1871

Dual Circularly Polarized Antenna

Adaptive Polarization ECM

Prepared for

U.S. Air Force Avionics Laboratory
Wright-Patterson Air Force Base
Ohio 45433

Prepared by

J. G. Neuberth and D. W. Rider

November 1978

Data Measurement Procedure

This data package, containing data measured on the 95 DP2P antenna under Nurad S.O. 1011, contains the following items:

- 1) Principal Plane Axial Ratio Radiation Patterns covering -90° to $+90^\circ$ measured at integral frequencies.
- 2) Axial Ratio Radiation Patterns recorded from 8.7 to 9.6 GHz at 100 MHz intervals.
- 3) Axial Ratio Radiation Patterns recorded at 9.0 GHz for 15° intervals of axial rotation.
- 4) Phase vs. frequency data recorded on antenna boresight for varying transmit antenna positions.
- 5) Phase vs. Antenna position data for principal plane and non-principal plane orientations with variable transmit antenna position.
- 6) VSWR vs. Frequency data.
- 7) Isolation vs. Frequency data.
- 8) Axial Ratio vs. Frequency data. Also contained within are test setup diagrams and explanations of the data and how to interpret it.

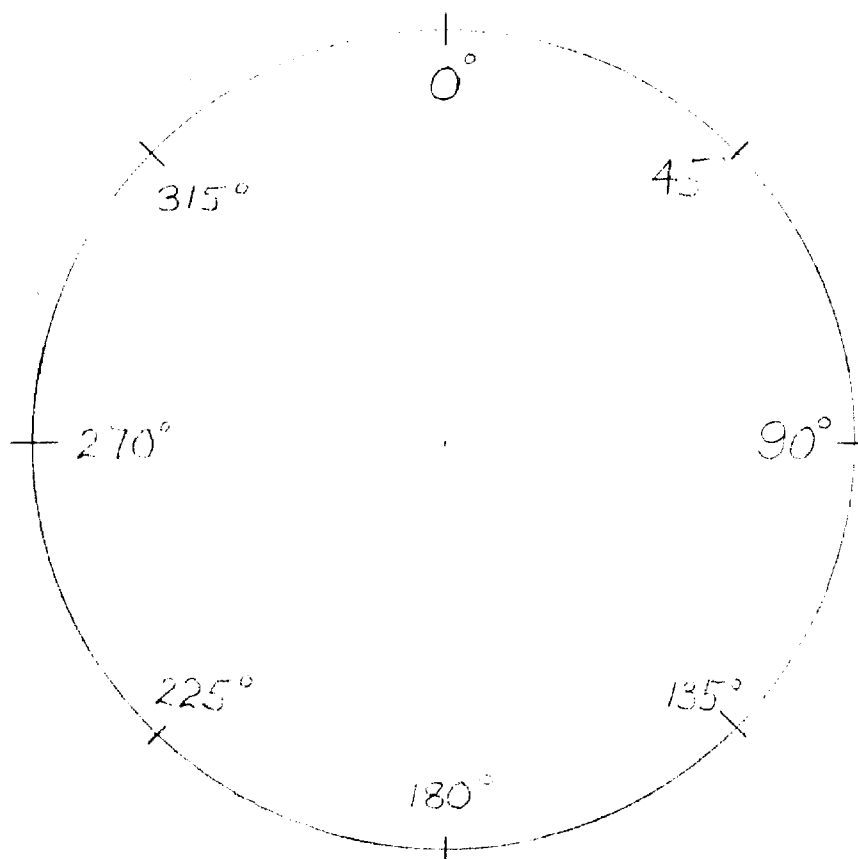
9) Gain Measurement Tabulations.

In data items 1 through 5 the antenna is tested in many physical positions. To make the data easier to understand, certain conventions have been adopted to describe the position of both the transmit and receive antennas. The position of the transmit antenna is given by the direction of the E vector observed from behind the transmit antenna. Coordinates are given in degrees, referenced to a 360° system, where 0° is vertically up and increasing angle moves in a clockwise direction. Refer to Figure 1.

The position of the test antenna is described by the position of the side port. The test antenna position is viewed from a location behind the transmit antenna. The same coordinate system is used as for the transmit antenna (Figure 1), with angle increasing in a clockwise direction from 0° on top. For instance, when the side port points up, the antenna position is described as 0°. When the side port is horizontally to the left of the antenna, the antenna position is described as 270°. In both cases the antenna is viewed from behind the transmit antenna.

Radiation Pattern Measurement

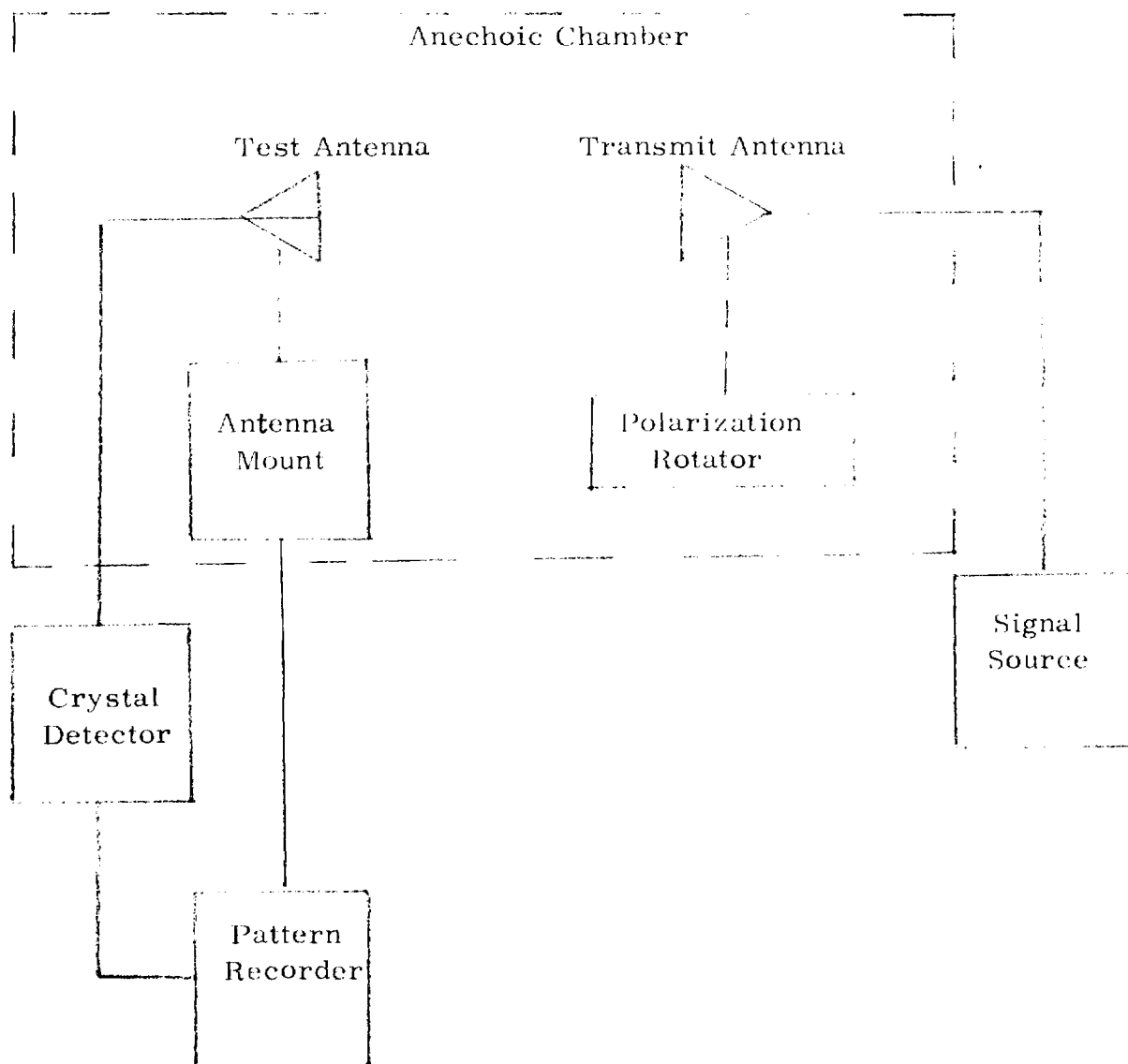
Figure 2 indicates the equipment setup used to record radiation patterns on the 95 DP2P antenna. During the testing the transmit antenna rapidly spins while the test antenna slowly turns in a horizontal plane. The posi-



Antenna Position Coordinate System

Figure 1

TITLE	NURAD, INC. 2165 DRUID PARK DR. BALTIMORE, MD. 21211	SIZE A	IDENT. NO. 25223	DWG. NO.	
				SH.	OF



Radiation Pattern Measurement
Test Setup

Figure 2

TITLE	NURAD, INC. 2165 DRUID PARK DR. BALTIMORE, MD. 21211	SIZE	IDENT. NO.	DWG. NO.	
		A	25223	SH.	OF

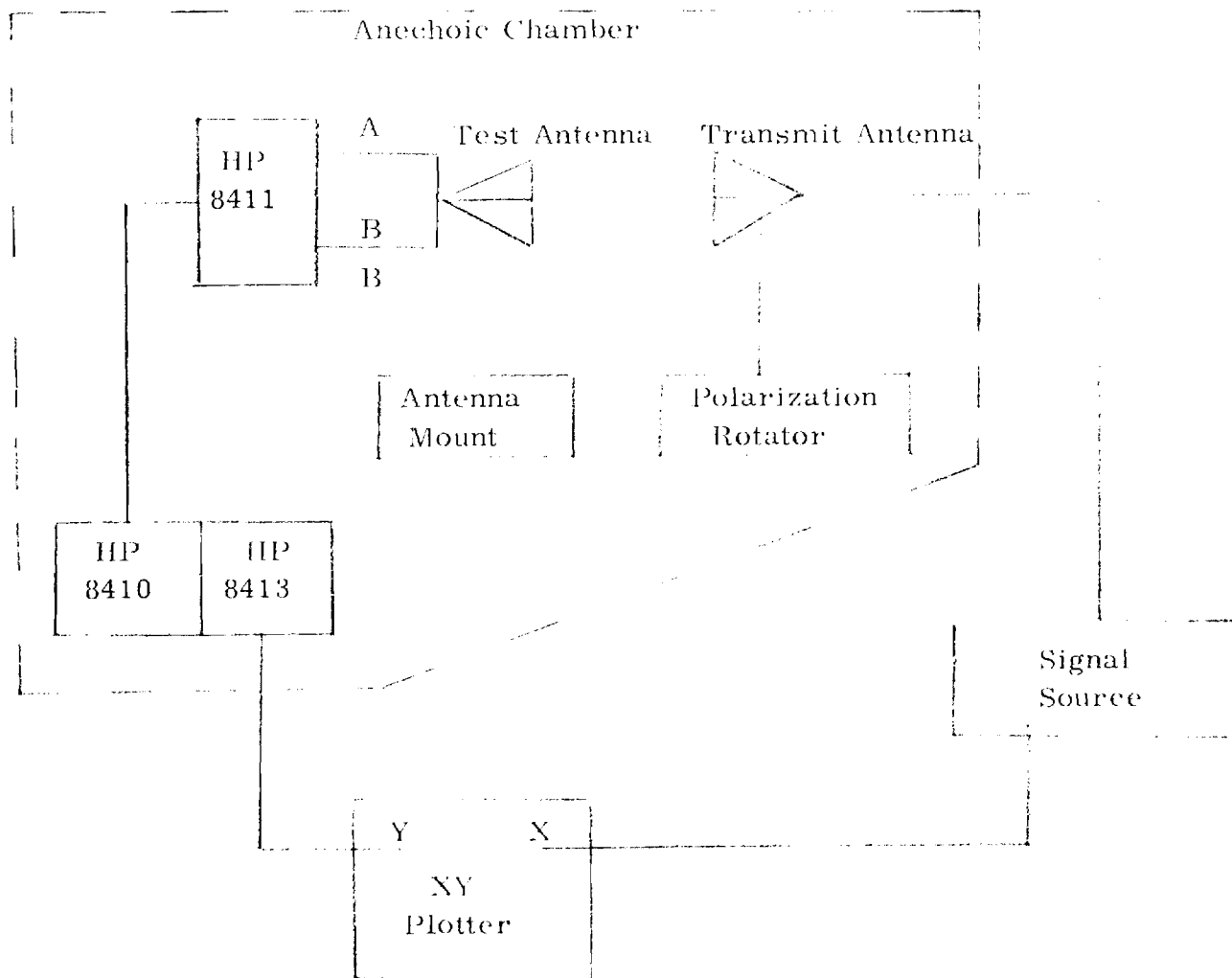
Radiation Pattern Measurement (cont'd.)

tion of the test antenna is indicated on the data. For instance, antenna position 0° describes the antenna mounted with the side port vertically up and with data taken as the antenna moves in a horizontal plane.

The first three data items consist of radiation patterns. In data item 1, principal plane axial ratio patterns are recorded at 1 GHz intervals. In data item 2 the 3 dB beamwidth axial ratio patterns are shown for the antenna mounted with the side port up for frequencies varying from 8.7 to 9.6 GHz. In data item 3 the axial ratio patterns are shown for the antenna at 9 GHz. The test antenna's position is changed from pattern to pattern and the position is noted on the data. In data items 1 through 3 the data is measured with output for both the side and rear ports. In all cases the unused port is loaded.

Phase vs. Frequency Measurement

Data item 4 consists of phase vs. frequency data. Figure 3 shows the setup which was used in this test. The signal generator provides a varying frequency signal which is transmitted to the test antenna. This antenna splits the signal into two orthogonally polarized components, which are then fed into the harmonic frequency converter section (HP 8411A) of the network analyzer. Here the signal is modified and travels to the mainframe section of the analyzer (HP 8410/8413) where it is modified again to pro-



Phase vs. Frequency Setup

Figure 3

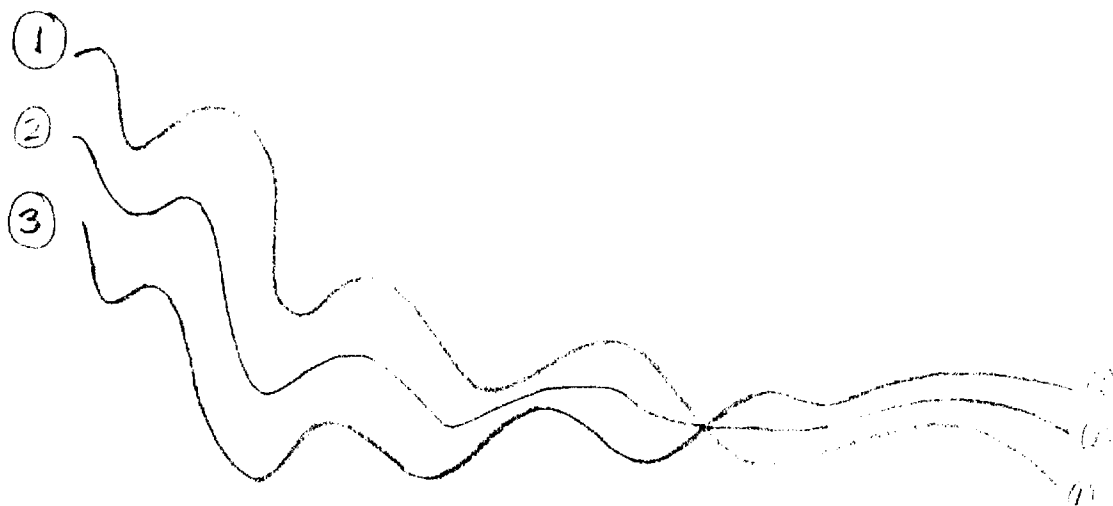
TITLE	NURAD, INC. 2165 DRUID PARK DR. BALTIMORE, MD. 21211	SIZE	IDENT. NO.	DWG. NO.	
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Phase vs. Frequency Measurement (cont'd.)

duce a phase proportional DC signal. An X-Y plotter utilizes this signal, along with another DC signal proportional to the frequency, to form a presentation of differential phase vs. frequency.

It is very important for purposes of interpretation of the data to understand how this differential phase measurement is made. Note that in this setup one output port is compared to the other output port. In Figure 4, a sample phase vs. frequency data plot, one can see the phase vs. frequency response of the antenna depicted on curve 1. This curve, when compared to the zero reference line (curve 2), will provide phase error data. Notice, however, curve 2 is not a straight line. This is because the cabling, connectors, and equipment used in measuring phase have differing transmission parameters through each line from an antenna port through the analyzer. These differing parameters, in the form of VSWR and different electrical path length, add both a slope and ripple to the reference line and data line.

One way of determining this frequency variable offset would be to calibrate the test equipment against a standard reference. An easier way is to switch the RF cables that attach to the output ports of the antenna and record the data again. In this way, the transmission line provides the path length and VSWR bias as before, but the differential phase information is



Sample Phase vs. Frequency Plot

Figure 4

TITLE	NURAD, INC. 2165 DRUID PARK DR. BALTIMORE, MD. 21211	SIZE A	IDENT. NO. 25223	DWG. NO.	
				SH.	OF

Phase vs. Frequency Measurement (cont'd.)

recorded in the opposite direction on the data. This is recorded as line 3 on Figure 4.

In symbolic form this procedure can be expressed as:

$$\text{Curve 1} = \text{Phase} + \text{System Error}$$

$$\text{Curve 3} = - \text{Phase} + \text{System Error}$$

Subtracting Curve 3 from Curve 1:

$$\text{Curve 1} - \text{Curve 3} = 2 (\text{Phase})$$

The Phase vs. Frequency data is recorded in the manner described above.

The data envelope, described by curves 1 & 3, is, in reality, double the phase error present between the two antenna ports. To find the phase error at a certain point, perform the following steps:

- 1) Determine the envelope width at the desired frequency.
- 2) Divide by 2.
- 3) Interpret that value according to the calibration line on the data.

One other piece of information is included in the phase vs. frequency data.

This is the phase offset between the two antenna ports. Although the antenna ports in this antenna phase track according to the specification, they are offset by a certain amount. This offset value is shown on all phase

Phase vs. Frequency Measurement (cont'd.)

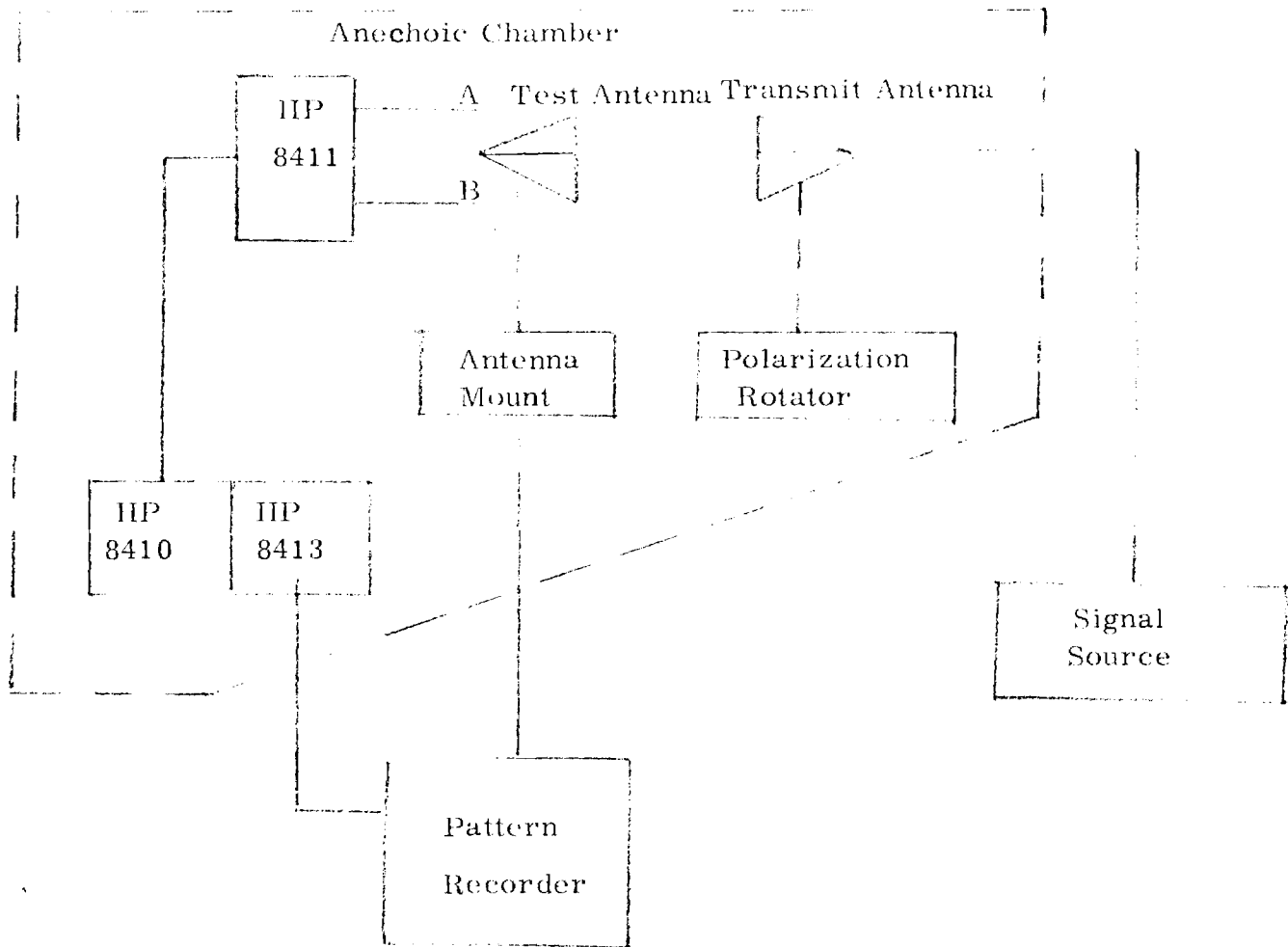
data supplied in this report. The amount of phase offset is a function of transmit antenna position. This dependency can be deduced from the information in data item 4. It is shown also in data item 4A in a more concise manner.

In data item 4A, four separate phase measurements are recorded on a single piece of paper. Each trace corresponds to a particular transmit antenna position and a particular phase offset setting. Note that by introducing an additional offset equal to twice the angular change of transmit antenna position results in nearly identical phase vs. frequency plots.

Phase vs. Position

Figure 5 describes the equipment setup used to perform Phase vs. Position measurements, data item 5. This setup is similar to that used for Phase vs. Frequency measurements, except that the network analyzer phase difference proportional signal is fed to the pattern recorder where it is combined with position information.

The measurement procedure used for Phase vs. Position measurements is also similar to the Phase vs. Frequency measurements. The antenna response is measured and then, when the test cables are switched at the antenna ports, the antenna is measured again. This procedure serves to



Phase vs. Position Setup

Figure 5

TITLE	NURAD, INC. 2165 DRUID PARK DR. BALTIMORE, MD. 21211	SIZE	IDENT. NO.	DWG. NO.	
		A	25223		
					SH. OF

Phase vs. Position Measurement (cont'd.)

subtract the measurement error from the system. To interpret the data use the following method:

- 1) Determine the envelope width defined by the two data traces.
- 2) Divide by 2.
- 3) Apply the calibration standard to determine phase error.

In this data, as in the previous Phase vs. Frequency data, phase offset is recorded next to each data trace. The data is recorded from 15° on antenna left to 15° on antenna right.

VSWR Measurement

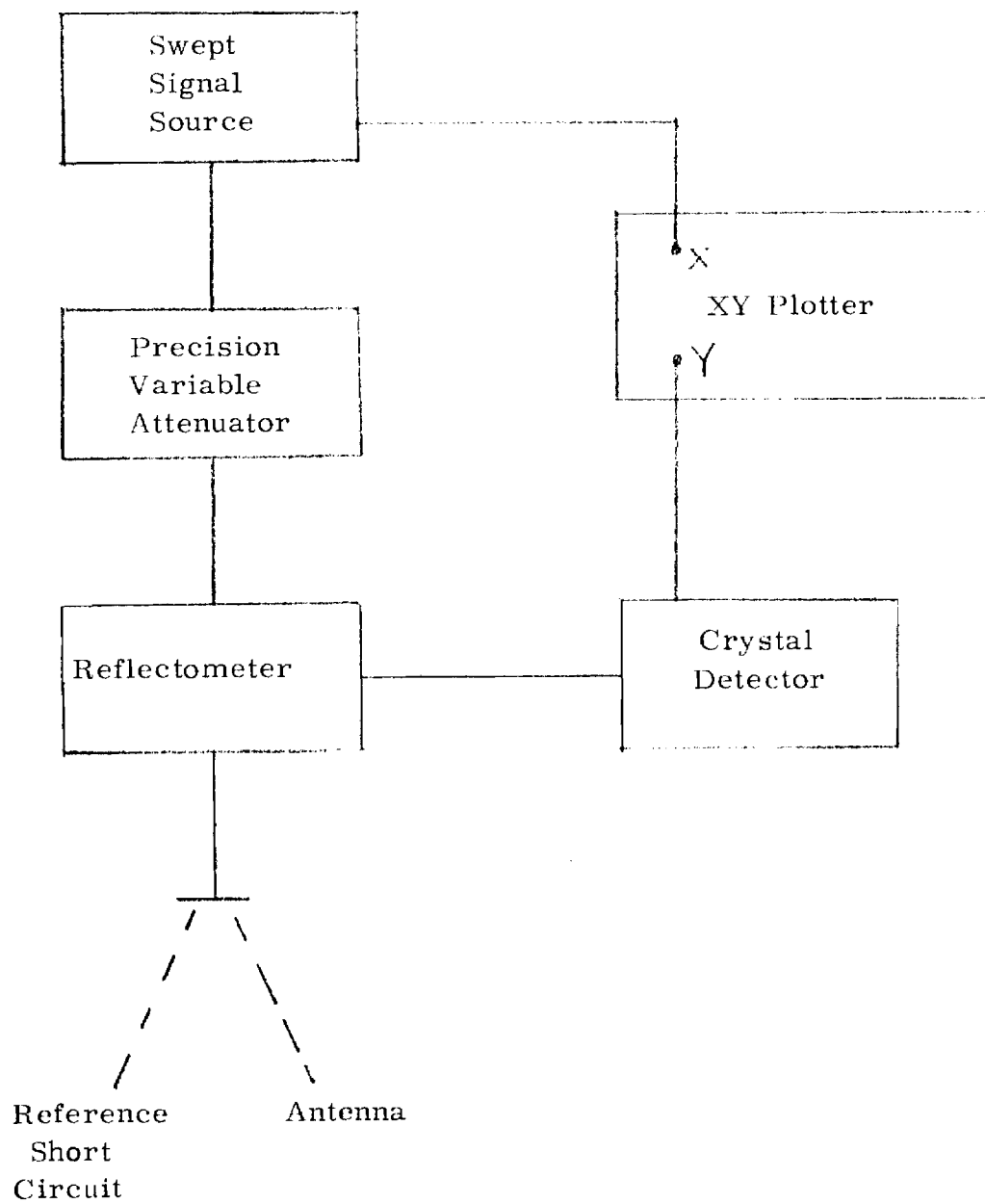
In data item 6, VSWR is measured as a function of frequency using equipment shown in Figure 6. Reference lines are recorded corresponding to VSWR values of 1.3:1 and 1.5:1.

Isolation Measurement

Data item 7 corresponds to output port isolation measured as a function of frequency. Reference lines are supplied corresponding to isolation values of 10, 20, and 30 dB. Figure 7 provides test setup information.

Swept Axial Ratio Measurement

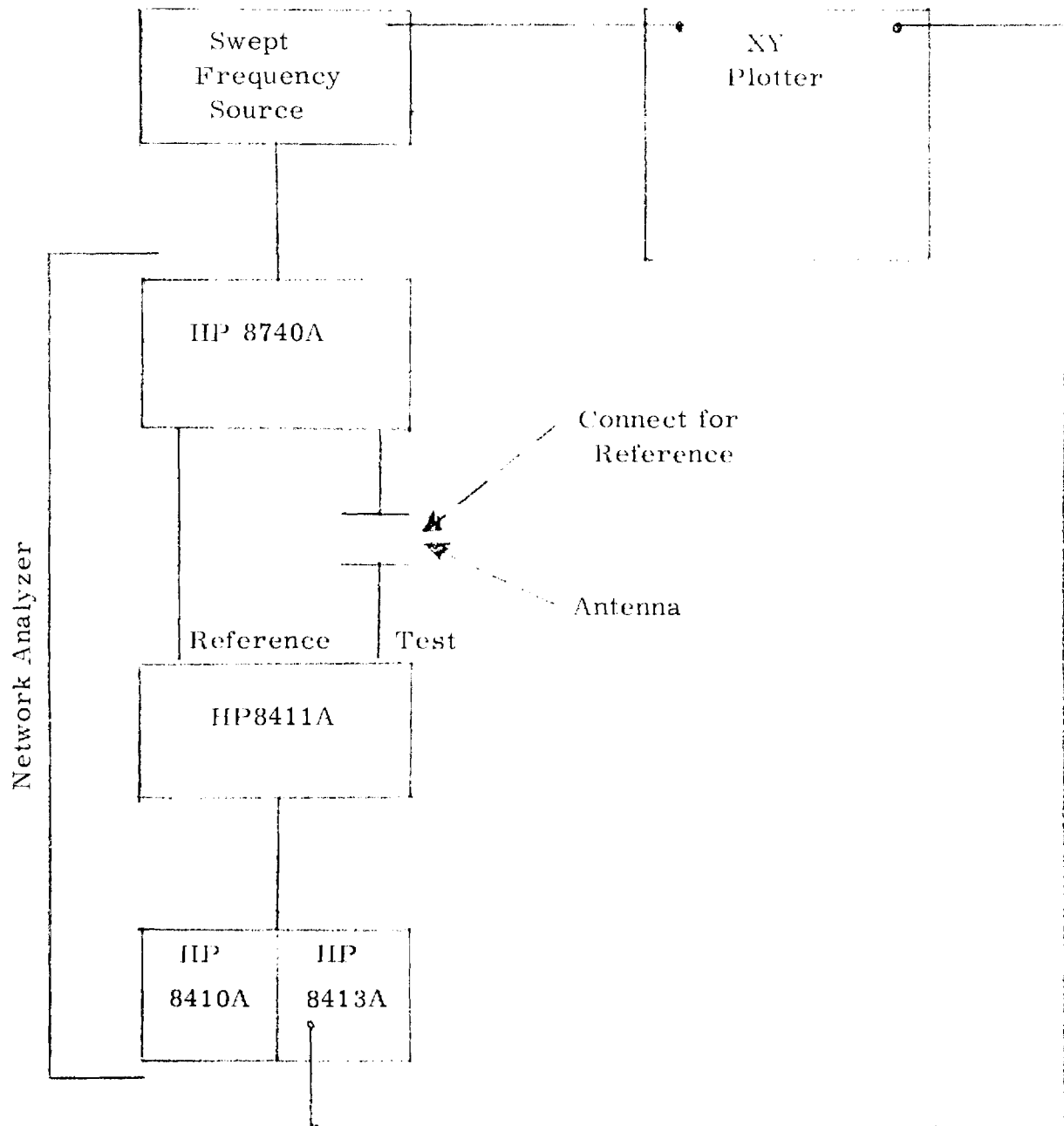
Data item 8 documents the Axial Ratio vs. Frequency measurement. The



VSWR Setup

Figure 3

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Isolation Setup

Figure 7

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		A	25223		
				SH.	OF

Swept Axial Ratio Measurement (cont'd.)

equipment used in this measurement is shown in Figure 8. Note that the power level fluctuates as a function of frequency. This is not a property of the antenna, but is, instead, a property of the signal source.

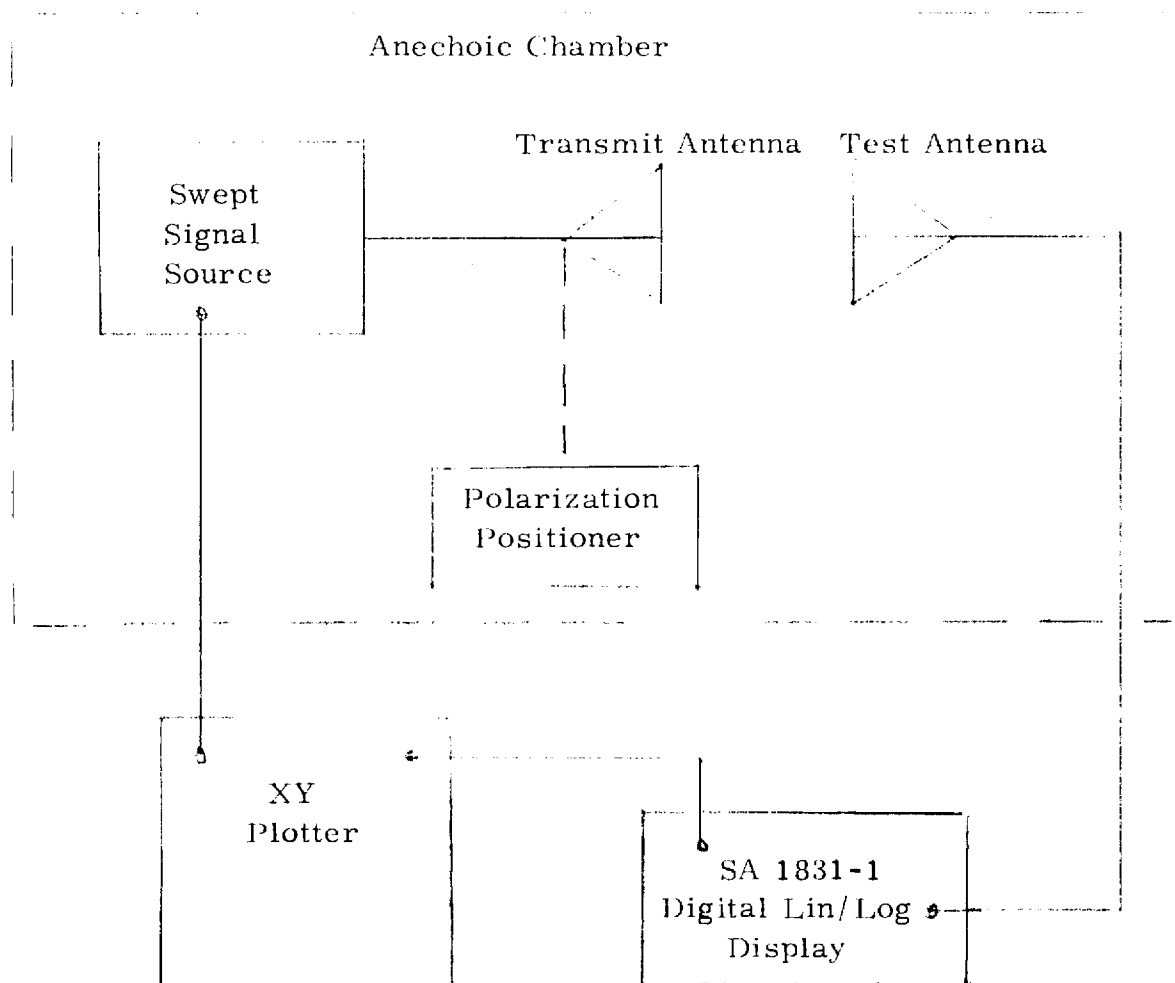
Gain Measurement

Data item 9 consists of gain measurements made on the antenna measured with respect to each output port. Gain is tabulated for integral frequencies in Figure 9. Included in this data is gain referenced to a linear isotropic antenna measured at the bottom of the polarization ellipse, boresight axial ratio, and circular gain. Circular gain is computed by the Sroka¹ method.

Appendix

Data measured for this report is contained in Appendix I at the rear of this report.

1. P. J. Sroka: "Nomograph Saves Time in Computing Antenna Gain," Microwaves, pages 54 and 55, March 1974



Axial Ratio vs. Frequency Setup

Figure 8

TITLE	NURAD, INC. 2165 DRUID PARK DR. BALTIMORE, MD. 21211	SIZE A	IDENT. NO. 25223	DWG. NO.	
			SH.		OF

Side Port

<u>(GHz)</u> <u>Frequency</u>	<u>Minimum</u> <u>Gain</u> <u>(dBi)</u>	<u>Axial</u> <u>Ratio</u> <u>(dB)</u>	<u>Circular</u> <u>Gain</u> <u>(dBci)</u>
8	11.3	1.8	15.3
9	12.7	0.2	15.8
10	14.5	0.6	17.8
11	14.8	0.6	18.1

Rear Port

8	11.4	1.7	15.3
9	12.7	0.2	15.8
10	14.4	0.5	17.7
11	14.6	0.6	17.9

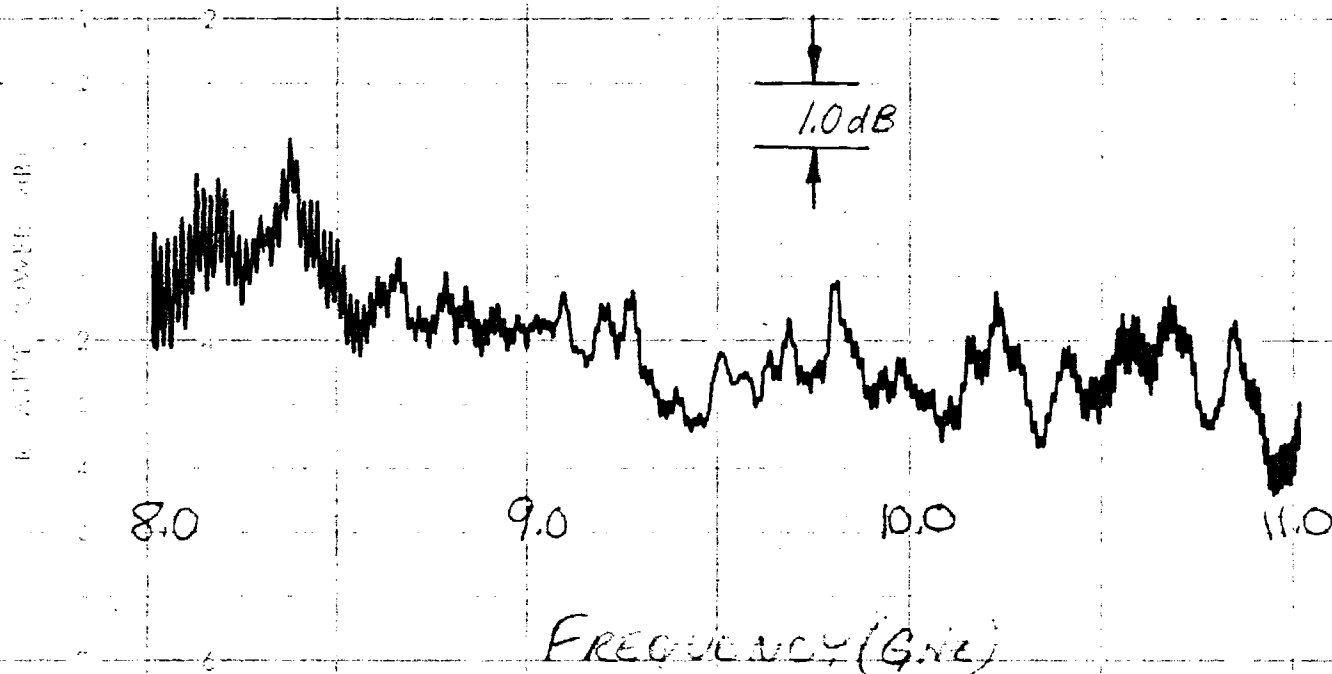
Gain Tabulation

Figure 9

17

TITLE	NURAD, INC. 2165 DRUID PARK DR. BALTIMORE, MD. 21211	SIZE	IDENT. NO.	DWG. NO.	
		A	25223		
				SH.	OF

DATA ITEM 8
AXIAL RATIO VS FREQUENCY
50 10 11 95 DP 2P
SIDE PORT



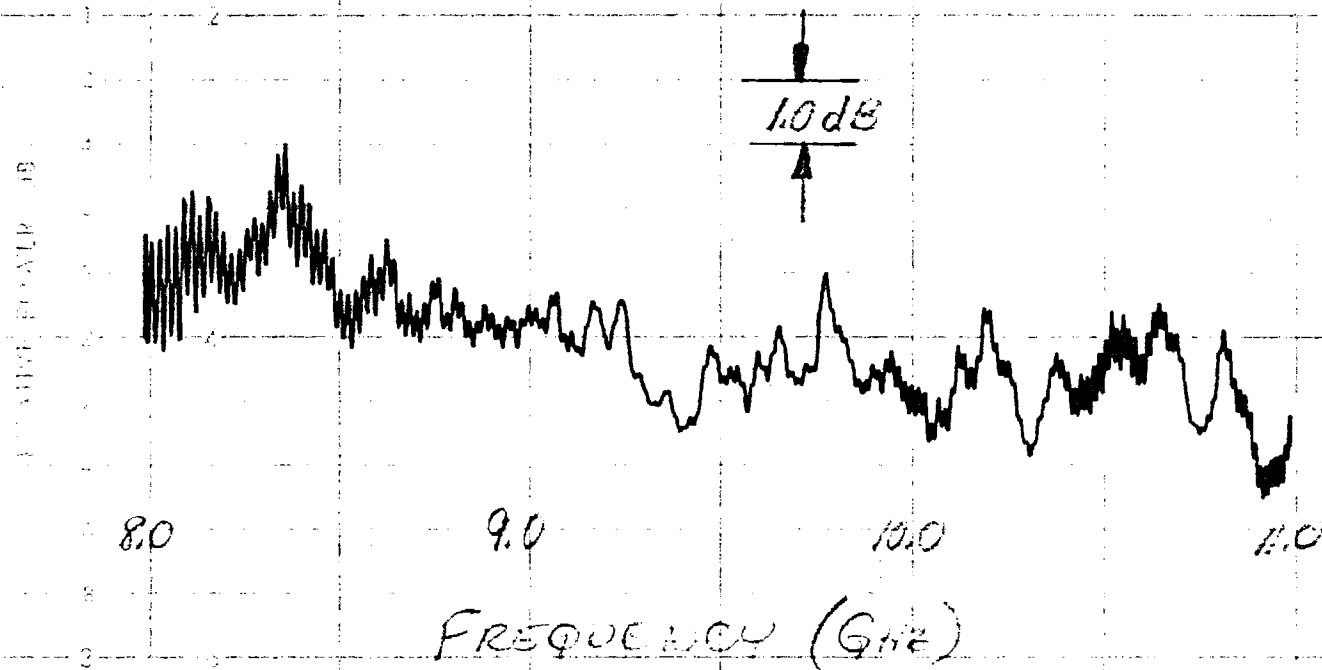
A-71

PATTERN NO.
PROJECT

DATE
ENGRS.

REMARKS

DATA ITEM 8
 AXIAL RATIO vs FREQUENCY
 SO 1011 95 DP 2F
 REAR PORT



A-72

PATTERN NO.

PROJECT

DATE

ENGRS.

REMARKS

SCALE

DATE

SCALE

DATE

ISOLATION VS FREQUENCY

12/14/77 F.B

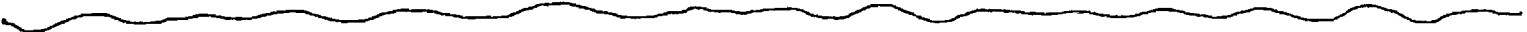
SO 1011 DP 952P

DATA ITEM 7

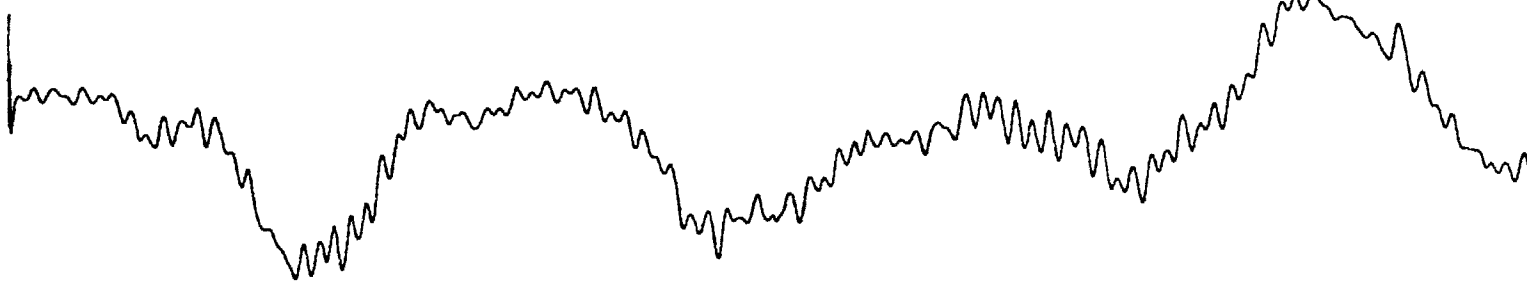
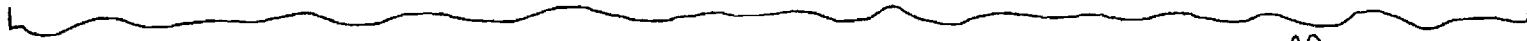
861/2

11662


10dB



20dB

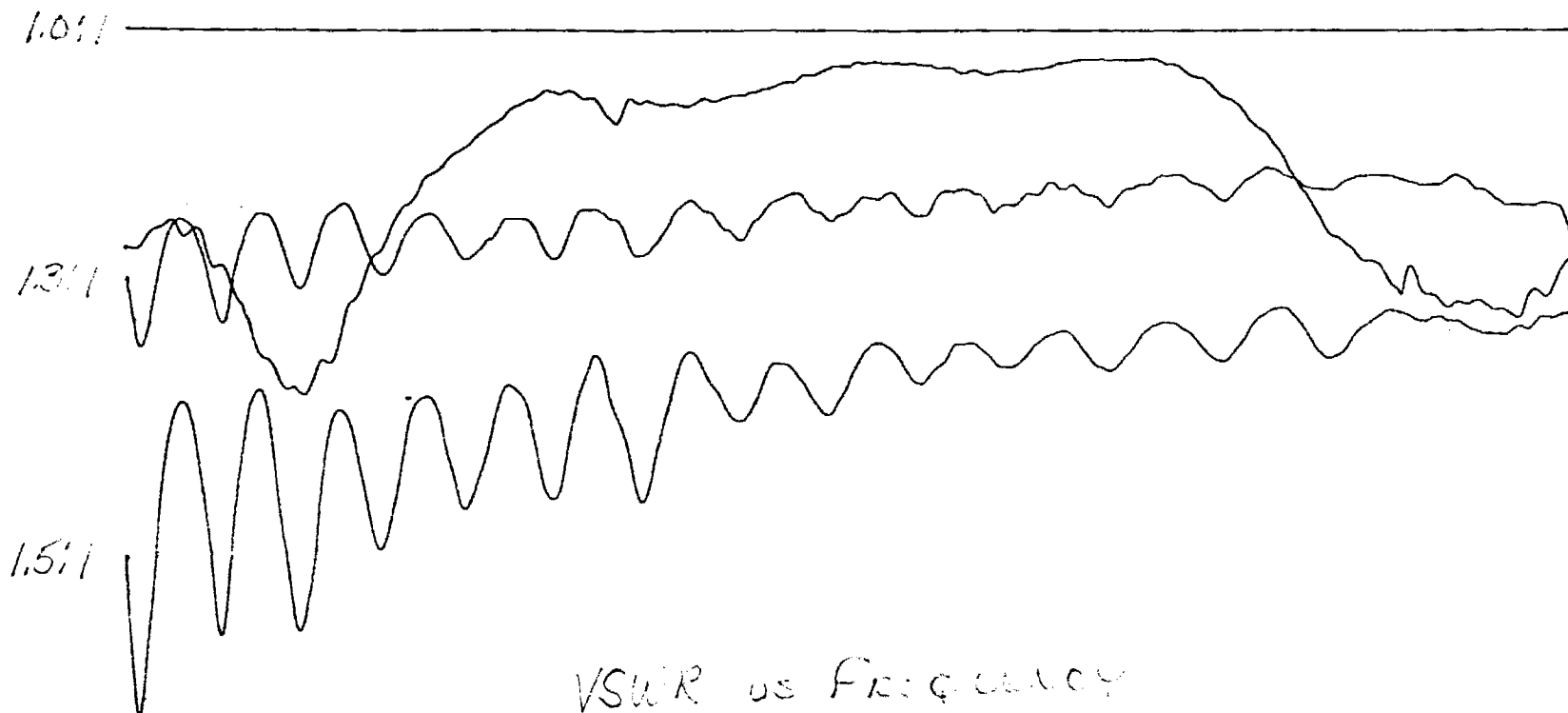


30dB



A-70

VSWR



1.0

1.3

8 GHz

VSWR vs FREQUENCY

SO 1011 95 D F 2 F

REAR PORT 12/14/77

DATA ITEM 6

11 GHz

VSWR

1.0:1

1.3:1

1.5:1

8 GHz

VSWR vs FREQUENCY

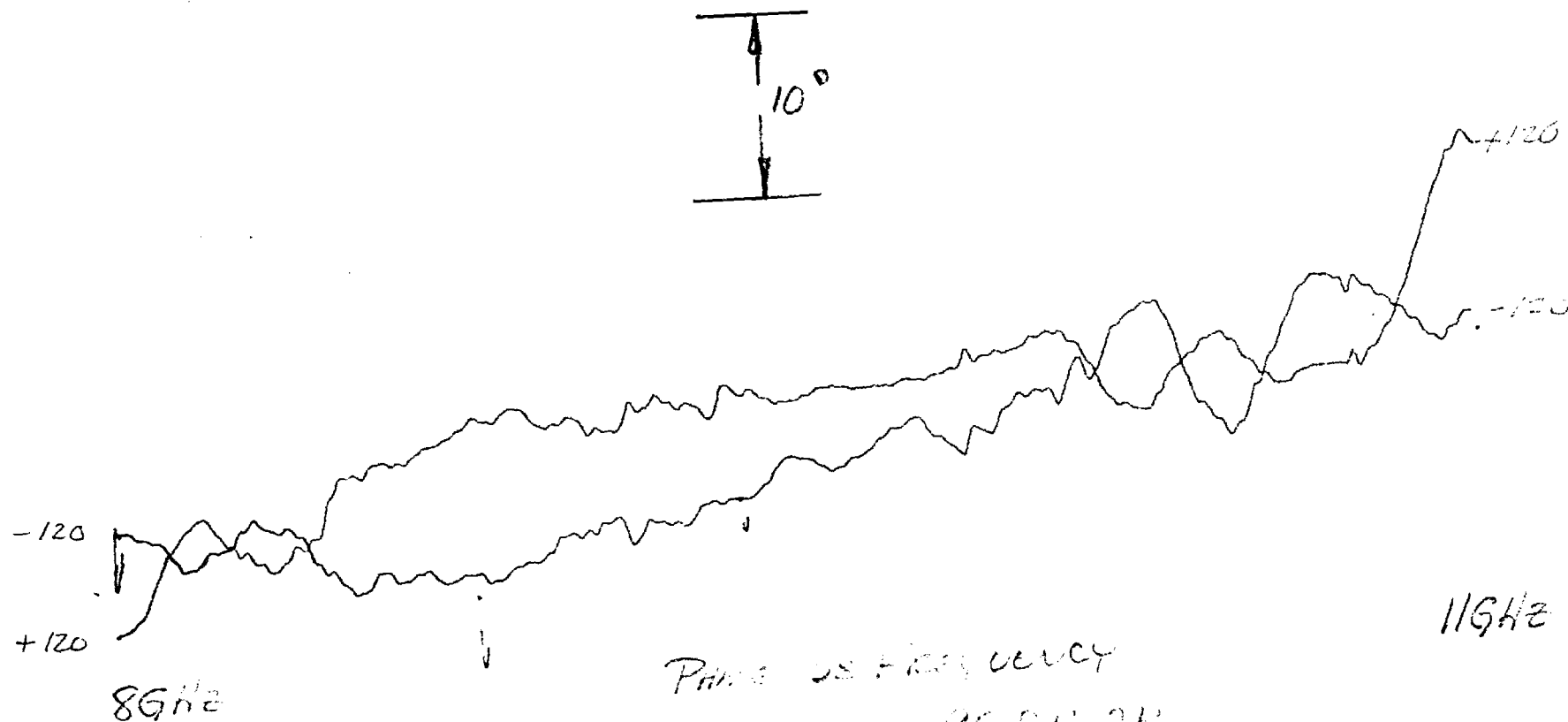
SO 1011 95 DP 2P

SIDE PORT 12/14/77

DATA ITEM 6

11 GHz

A-69



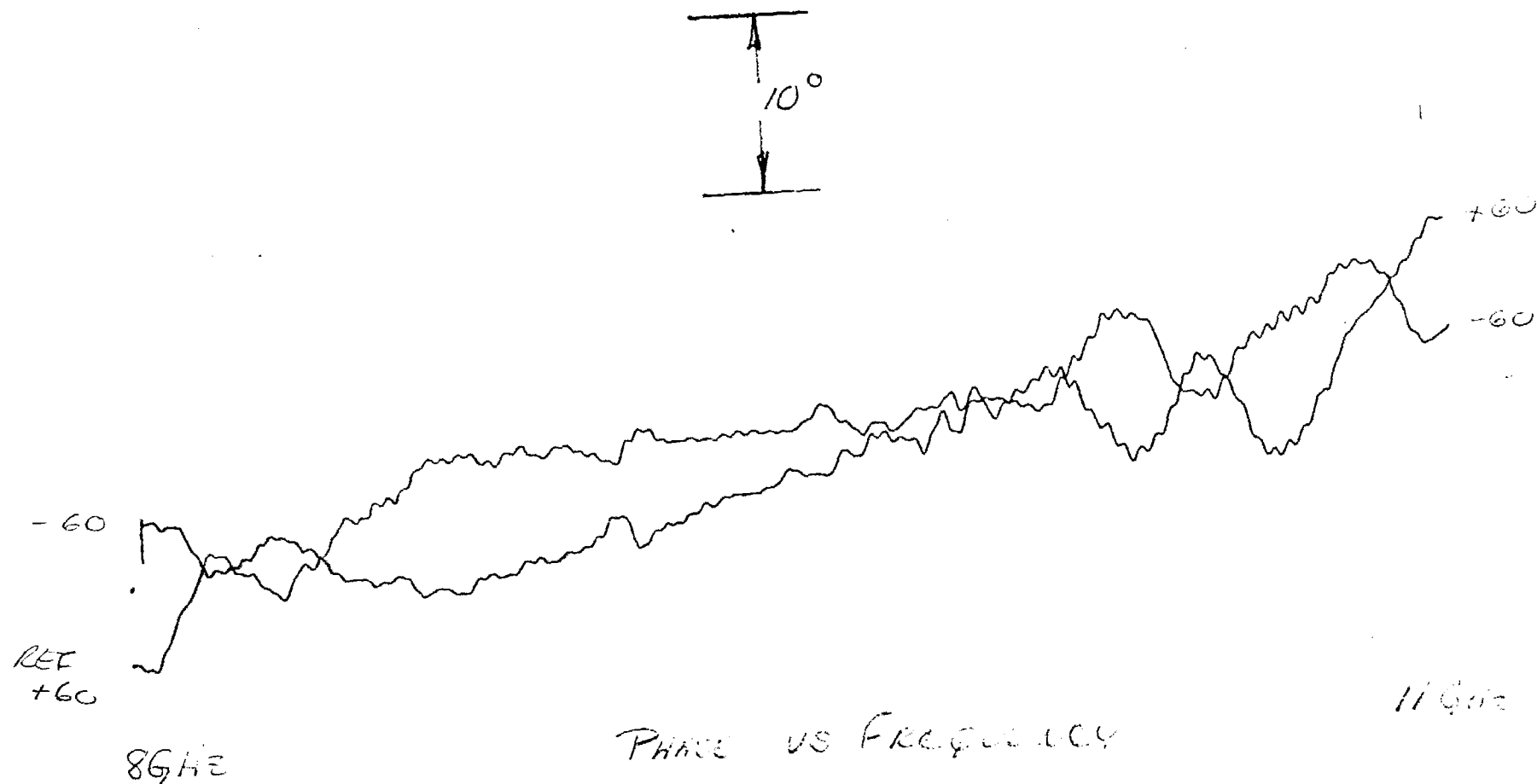
Phase vs Frequency
 20 100 95 dB 2P

12/7/71

TRANSMIT ANTENNA POSITION 180°

RECEIVE ANTENNA POSITION 0°

DATA ITEM 4



PHASE VS FREQUENCY

SO 1011 95 DP 2P

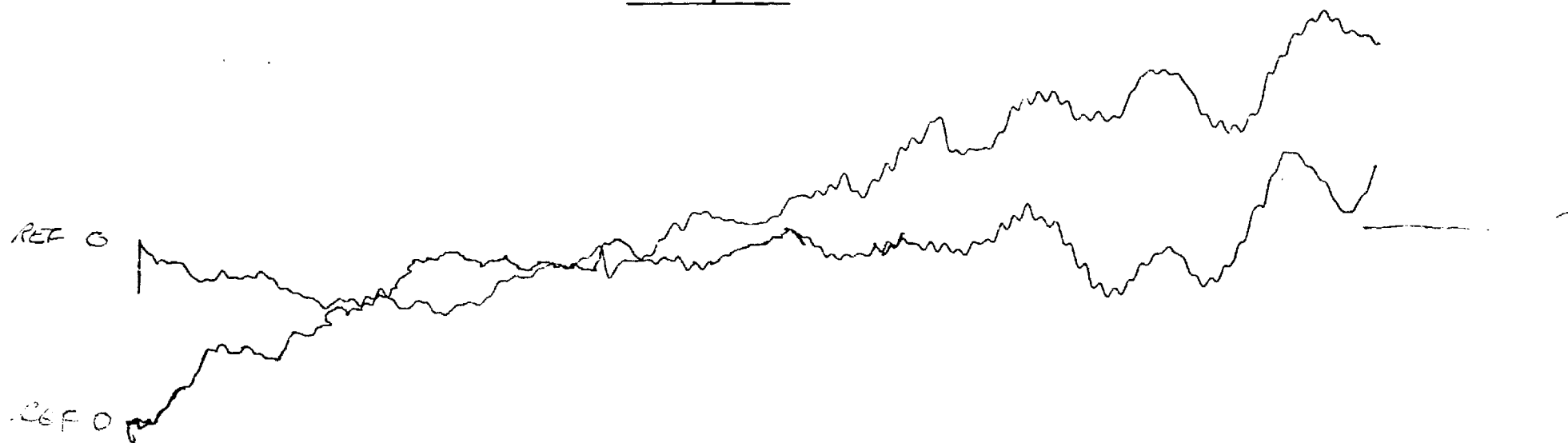
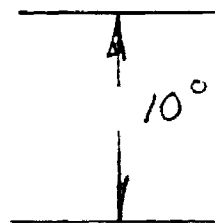
10/7/77

TRANSMIT ANTENNA POSITION 150°

RECEIVE ANTENNA POSITION 0°

DATA ITEM 4

A-52



8 GHz

PHASE VS FREQUENCY

11 GHz

50 101 95 DP 2P

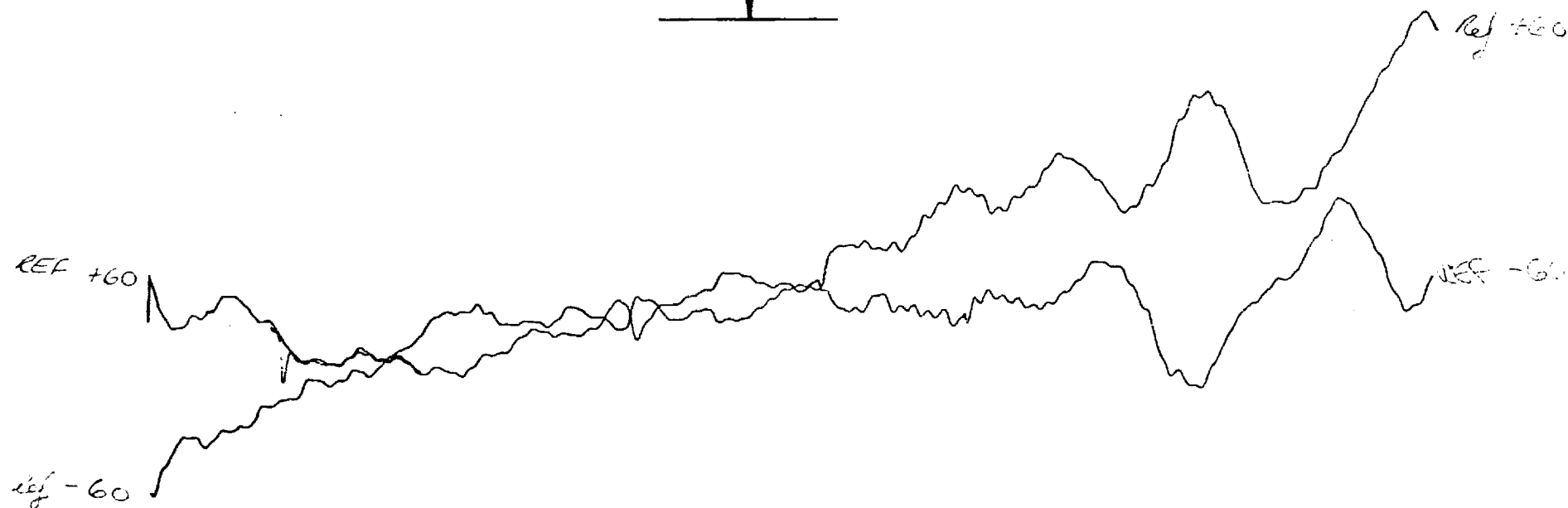
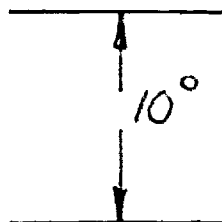
12/7/71

TRANSMIT ANTENNA POSITION 120°

RECEIVE ANTENNA POSITION 0°

DATA ITEM 4

2-53



8GHz

PHASE VS FREQUENCY

SO 10 11 95 DP 2P

12/7/77

11GHz

TRANSMIT ANTENNA POSITION 90°

RECEIVE ANTENNA POSITION 0°

DATA ITEM 4

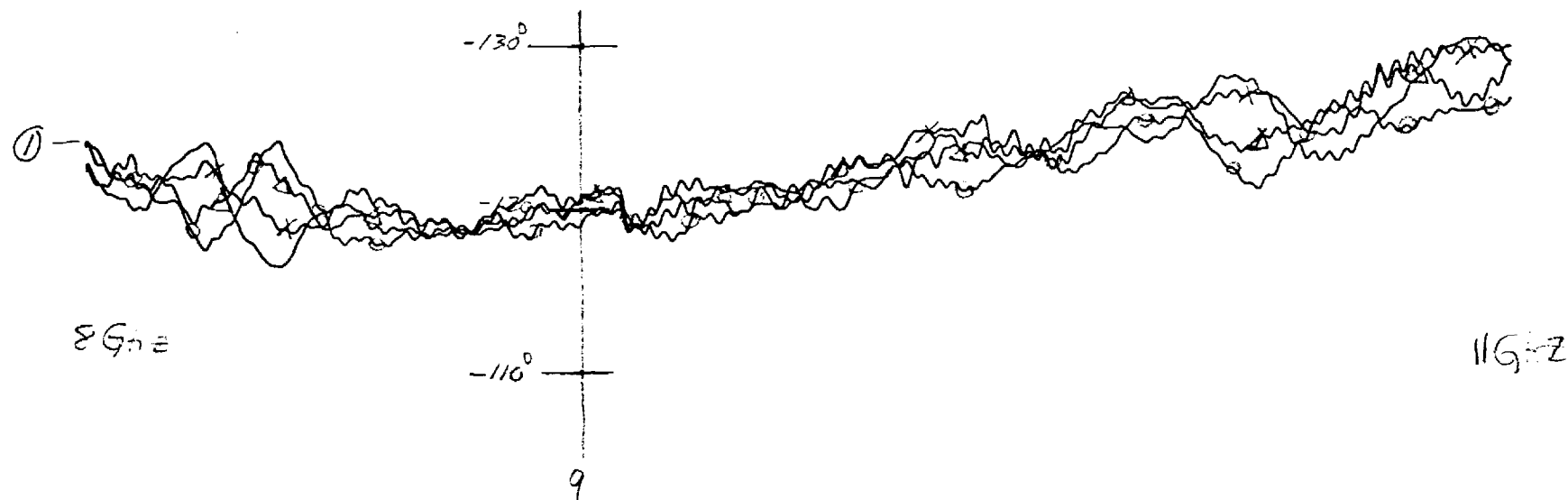
A-54

○ ○ ○	-120	OFFSET	TX 180
△ △ △	-60	OFFSET	TX 50
X X X	0	OFFSET	TX 120
— — —	+60	OFFSET	TX 90

PHASE VS FREQUENCY

50 100 150 200 250

12/13/77 23



DATA ITEM 4A

- ① -120° REFERENCE OFFSET, SIDE PORT TEST INPUT, REAR PORT REF. REAR COAX CONNECTOR POINTS DOWN, SIDE COAX CONNECTOR POINTS TO LEFT AS SEEN FROM TRANSMIT ANTENNA. TEST ANTENNA SIDE PORT FACES VERTICALLY UP, VERTICAL TRANSMIT -180°

A-55

PROJECT A-1871

OPERATION AND MAINTENANCE HANDBOOK
SYSTEM SPECIFICATIONS AND DRAWINGS (Volume 2 of 5)

TRANSMITTER SUBSYSTEM
ADAPTIVE POLARIZATION ECM

H. W. Andrews

5 October 1979

CONTRACT NO. F33615-76-C-1250

U.S. Air Force Avionics Laboratory
Wright-Patterson Air Force Base
Ohio 45433

Prepared by the

Engineering Experiment Station
Georgia Institute of Technology
Atlanta, Georgia 30332

PROJECT A-1871

OPERATION AND MAINTENANCE HANDBOOK
SYSTEM SPECIFICATIONS AND DRAWINGS (Volume 2 of 5)

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER 71-0008, 9, 10(2)	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. E (and Subtitle) Operation and Maintenance Handbook, System Specifications and Drawings (Vol. 2 of 5) Transmitter Subsystem Adaptive Polarization ECM)		5. TYPE OF REPORT & PERIOD COVERED
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) W. Andrews		8. CONTRACT OR GRANT NUMBER(s) F33615-76-C-1250
9. PERFORMING ORGANIZATION NAME AND ADDRESS Engineering Experiment Station Georgia Institute of Technology Atlanta, Georgia 30332		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS U.S. Air Force Avionics Laboratory Wright-Patterson Air Force Base, Ohio 45433		12. REPORT DATE 5 October 1979
		13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report)		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Adaptive Polarization ECM Polarization Modulations Polarization ECM Repeater Transmitter Transponder IG Double Cross ECM		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This handbook presents the directions for operating and maintaining the transmitter subsystem associated with the Adaptive Polarization ECM system as modified to include Double Cross ECM. In addition it includes the subsystem specifications and subsystem drawings. It is volume 2 of 5 volumes which completely describe the system.		

DISCLAIMER

The citing of trade names and names of manufacturers in this report is not to be construed as endorsement or approval of the commercial products referenced by either the Georgia Institute of Technology or the United States Government.

FOREWORD

The transmitter subsystem described in this handbook was designed and fabricated by the Antennas and Countermeasures Division, Systems and Techniques Laboratory of the Engineering Experiment Station, Georgia Institute of Technology, Atlanta, Georgia 30332. The program was sponsored by the Air Force Avionics Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio 45433. The requirement for the transmitter subsystem was established as part of the Adaptive Polarization ECM on Contract No. F33615-76-C-1250. This contract is designated Georgia Tech Project A-1871, and Mr. H. W. Andrews served as Project Director. Mr. D. W. Misek served as the Air Force Project Engineer, and his invaluable assistance and guidance throughout the program are greatly appreciated.

The combined efforts of many individuals have made the realization of this transmitter subsystem possible. In particular, the authors wish to express their gratitude to Mr. R. J. Hodges and Mr. N. C. Hightower, formerly of Georgia Tech, for the many hours they devoted to the overall project.

This transmitter subsystem handbook was submitted as the second of 5 volumes containing the operation and maintenance instructions, system specifications, and system drawings for the Adaptive Polarization ECM system as modified to include Double Cross ECM. The structure of the handbook is as follows:

Volume 1 : Dual Circularly Polarized Antenna

Volume 2 : Transmitter Subsystem

Volumes 3-5: Signal Processing Subsystem.

This handbook was submitted on 5 Oct 1979 to meet deliverable requirements expressed on Contract No. F33615-76-C-1250, Project 2000. These are:

System Specifications

System Drawings

Operation and Maintenance Handbook.

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1.0 INTRODUCTION AND SUMMARY

The Engineering Experiment Station (EES), Georgia Institute of Technology, Atlanta, Georgia, along with its major subcontractor, the Advanced Electromagnetics Unit of the Aerospace Electronics Systems Department of the General Electric Company, Utica, N.Y. have designed, developed, fabricated, and tested an Adaptive Polarization ECM (APECM) system for the Air Force Avionics Laboratory (AFAL) under Contract No. F33615-76-C-1250. In addition the APECM hardware was modified to implement a cross-eye technique known as "Double Cross" ECM (DCECM) which has also been incorporated into the system as directed by contract modification No. P-00008.

In order to fully document the APECM/DCECM hardware package, contract requirements were established for a set of reports which were to include the system specifications, system drawings, and an operation and maintenance manual. In an effort to present this information in a clear, concise, and easily interpretable manner, the APECM/DCECM hardware has been broken into three main blocks (subsystems) for documentation purposes. The system specifications, system drawings and the operation and maintenance instructions for each subsystem therefore appear in the same volume, wherever possible thus simplifying the maintenance and operational requirements of the total system. As such the three subsystems are:

- 1) Dual Circularly Polarized Antenna (Volume 1)
- 2) Transmitter Subsystem (Volume 2)
- 3) Signal Processing Subsystem (Volumes 3 through 5)

Figure 1 shows a block diagram of the APECM/DCECM system and its breakdown into these three subsystems.

This volume covers the system specifications, system drawings, and the operation and maintenance instructions for the Transmitter Subsystem. The main units which make up this subsystem are:

- 1) Driver
- 2) Auxiliary Receiver
- 3) CW TWT Amplifier
- 4) Pulse TWT Amplifier
- 5) Antennas

It should be noted that in the antennas section, only a cursory description

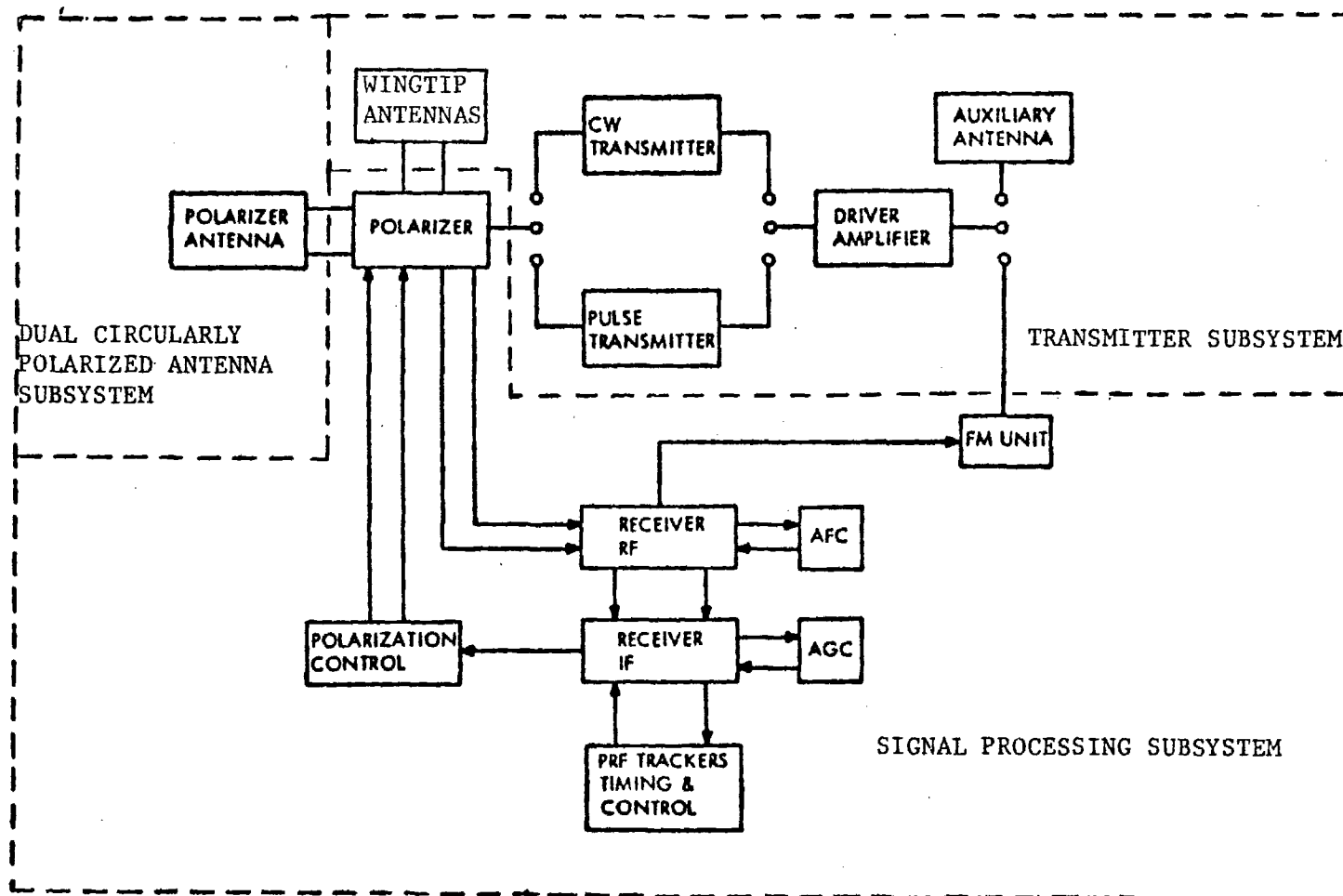


Figure 1. System Block Diagram

of the Main Dual Circularly Polarized Antenna (DCP) is included. Volume 1 should be referred to for a detailed technical description of the DCP.

This document contains information on the Transmitter Subsystem and has been arranged as follows. Section 2.0 provides an overall technical description of the subsystem and how the major units interphase with one another. Section 3.0 covers the technical details of the major components which make up each unit in the subsystem. Section 4.0 provides operational and maintenance procedures for the subsystem. Pertinent drawings, figures, and tables have been included into each section as appropriate rather than grouping them together in one section.

2.0 APECM/DCECM TRANSMITTER SUBSYSTEM TECHNICAL DESCRIPTION

The APECM/DCECM transmitter subsystem is subdivided into 5 main units. These are:

- 1) Driver
- 2) Auxiliary receiver
- 3) CW TWT amplifier
- 4) Pulse TWT amplifier
- 5) Antennas.

Although the auxiliary receiver is incorporated in the driver cabinet it was considered as a separate entity because the driver can be operated independently from the auxiliary receiver. The inverse is also true with a few minor changes.

The transmitter subsystem is designed to amplify RF signals from 8 to 11 GHz up to 500w CW or 2 Kw peak. These RF signals are available either from the auxiliary antenna (repeater mode) or from the RF receiver in the signal processing subsystem (transponder mode). Once these RF signals are amplified they are applied to the polarizer before finally radiating the RF energy through the antenna(s). Figure 2 shows a simplified block diagram of the transmitter subsystem.

The flexibility of the transmitter subsystem is typified in its many modes of operation. Besides having either pulse or CW capability, the subsystem is capable of operating in either repeater, transponder, or instantaneous inverse gain (IIG) modes, and can supply RF power, via the polarizer, to either the APECM antenna or the DCECM antennas. An amplitude modulator (AM) capability is also included, while FM capability is provided by the signal processing subsystem.

Sections 2.1 through 2.5 describe the 5 units which make up the subsystem while Section 2.6 describes the total subsystem performance. Detailed specifications of the components making up each unit of the subsystem are presented in Section 3.

2.1 Driver Description

The driver is the control center of the transmitter subsystem. Figure 3 shows the front panel controls, inputs, outputs, test points, and LED indicators. Figure 4 shows the rear panel of the driver. By

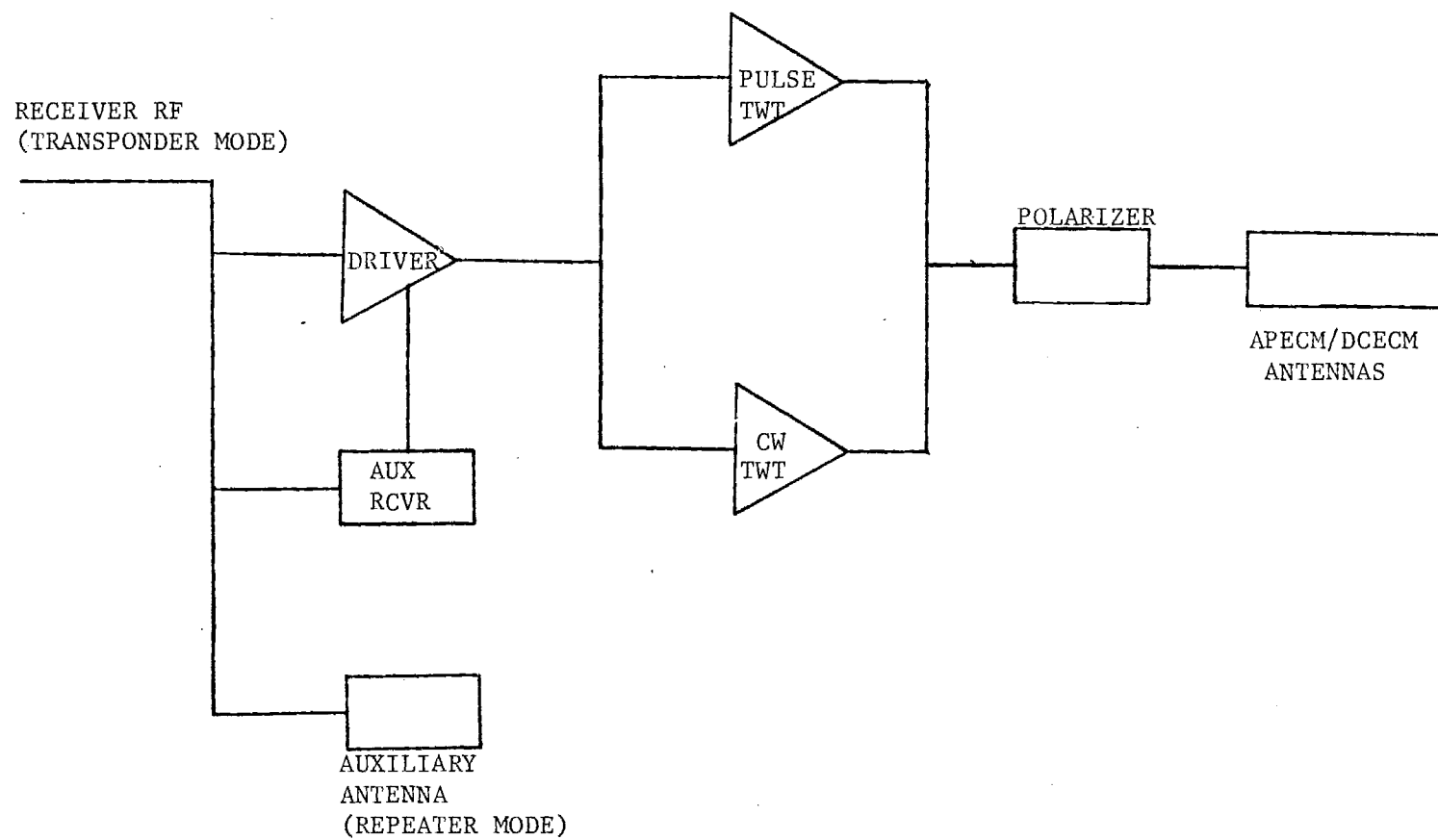


Figure 2. Simplified Transmitter Subsystem Block Diagram

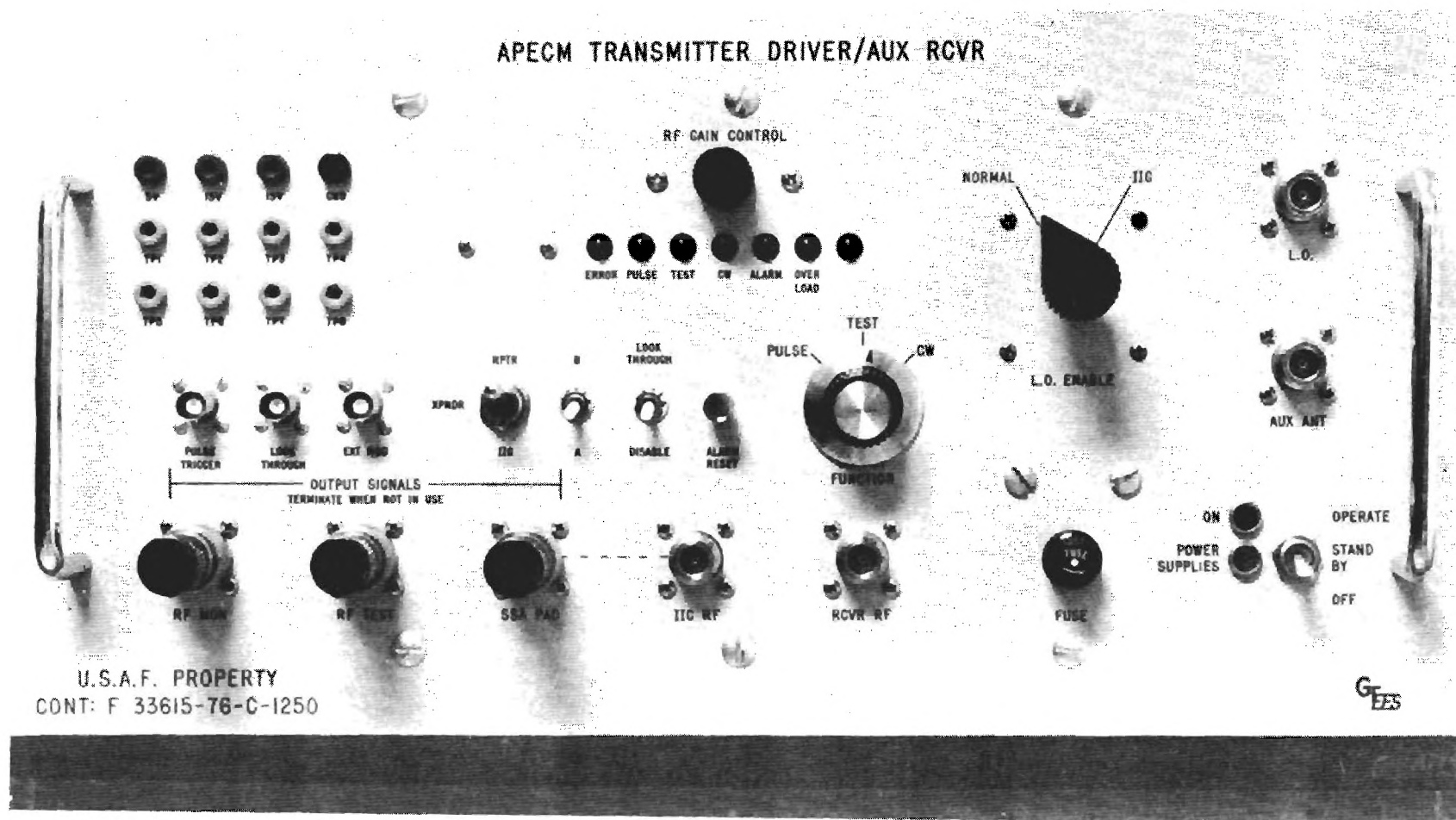


Figure 3. Driver (Front View)

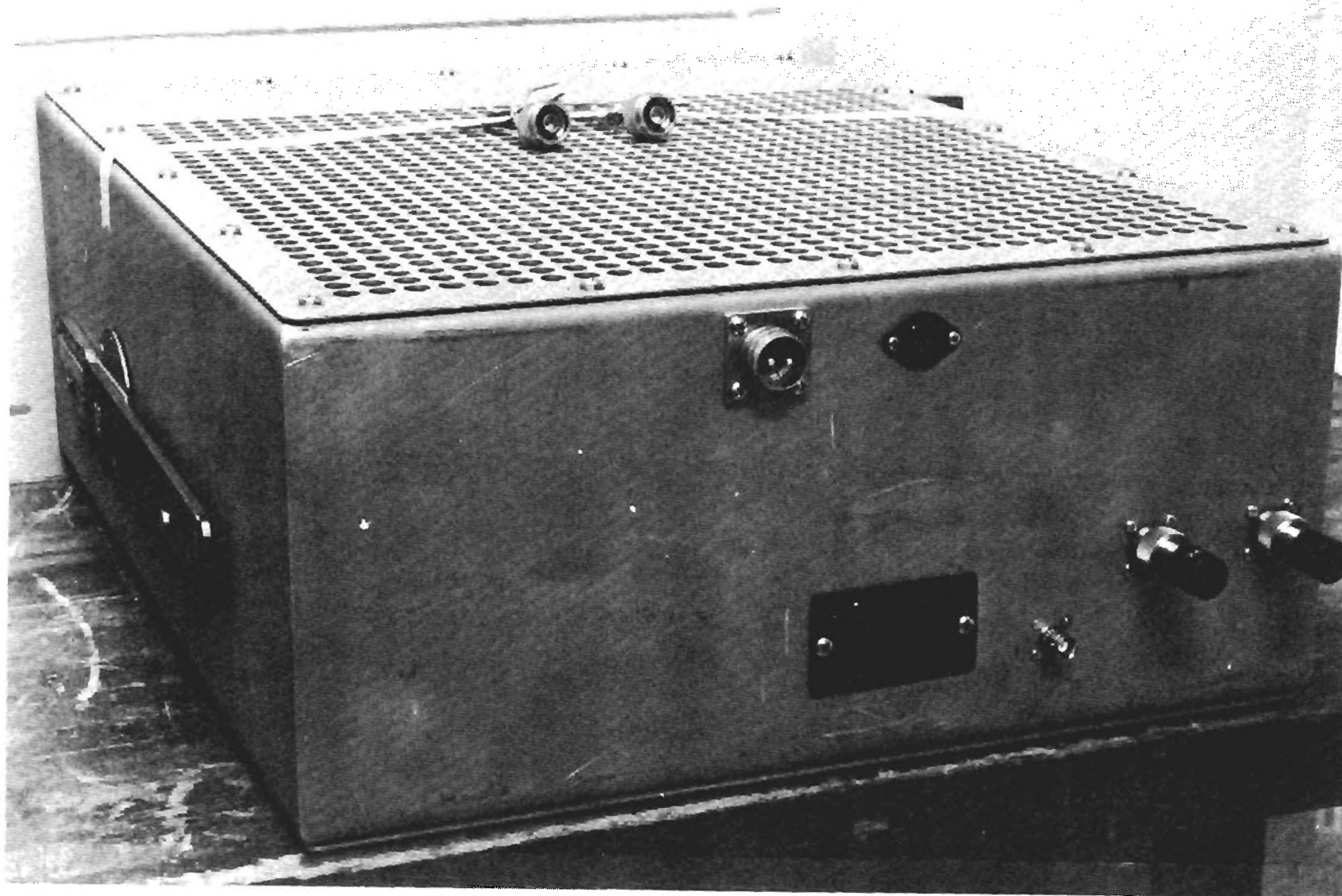


Figure 4. Driver (Rear View)

proper selection of these controls, the transmitter subsystem can be operated efficiently and expeditiously. Safety circuits located within the driver prevent operation of the transmitter subsystem in modes which could cause damage to the subsystem's principal components. These conditions are indicated by the LED's labeled ERROR, ALARM, and OVERLOAD on the driver front panel. A brief description of these controls follows.

2.1.1 Driver Inputs

There are 3 RF inputs and 3 control inputs on the driver. The RF inputs are the local oscillator (LO) input, the auxiliary antenna (AUX ANT) input, and the receiver RF (RCVR RF) input, with the LO and RCVR RF inputs coming from the signal processing subsystem. In cases when IIG is utilized, the RF input to the driver is changed to the IIG RF connector instead of the RCVR RF input connector. These RF inputs utilize N type connectors and must have the following properties to provide full output for the transmitter subsystem.

TABLE I
DRIVER RF INPUT SPECIFICATIONS FOR FULL OUTPUT
OF THE TRANSMITTER SUBSYSTEM

RF input	Frequency	Level
LO	8-11 GHz	-20 dBm
AUX ANT	8-11 GHz	-37 dBm
RCVR RF	8-11 GHz	-37 dBm
IIG RF	8-11 GHz	-17 dBm

If the above RF inputs are not available at the stated power levels, internal settings which have been set to prevent overload conditions can be readjusted to provide full output (see Section 2.1.7).

The 3 control inputs are the pulse trigger (PULSE TRIGGER) input used internally by the driver and to trigger the pulse TWT amplifier, the look-through (LOOK THROUGH) input used internally by the driver and to cut off the CW TWT amplifier, and the external modulation (EXT MOD) input

which provides external AM control. The latter signal is provided from any external signal source such as a function generator or similar test equipment. All three control signal inputs utilize BNC connectors and must have the following characteristics.

TABLE II
DRIVER CONTROL SIGNAL INPUT SPECIFICATIONS

Control Signal	Levels	Timing
PULSE TRIGGER	TTL	10 μ sec max pw, 0.2 μ sec min pw, 2% duty max
LOOK THROUGH	TTL	1.8 μ sec min pw, 5 KHz max
EXT MOD	± 10 V (adjustable)	DC - 100 KHz

2.1.2 Driver Outputs

There are 4 RF outputs and 2 control outputs on the drive. There are 2 RF outputs on the front panel (three when in the IIG mode, see Section 4.2.3.1) and 2 RF outputs and 2 control outputs in the rear panel. The 2 RF outputs in the rear panel provide the RF drive to the CW TWT amplifier and the pulse TWT amplifier as selected by the OUTPUT FUNCTION switch on the driver front panel provided other inputs are correctly employed. The output labeled RF TEST on the driver front panel provides RF power only when the OUTPUT FUNCTION switch is in the TEST position. RF energy is therefore provided to only one of these three outputs depending on the selected OUTPUT FUNCTION switch selection. If one of the safety rules has been violated RF energy will be internally terminated and thus will not be present at either of the three outputs above. The fourth RF output is on the driver front panel, RF MON, and is used to monitor the RF passing through the driver. This signal is available at all times. All RF outputs utilize type N connectors and have the following properties. (Note: All power levels are CW when in transponder mode.)

TABLE III
DRIVER RF OUTPUT SPECIFICATIONS

RF Output	Frequency	Level
CW output	8-11 GHz	adjusted max: +7 dBm, unadjusted max: +38 dBm
Pulse output	8-11 GHz	adjusted max: +23 dBm, unadjusted max: +38 dBm
RF TEST	8-11 GHz	same as above
RF MON	8-11 GHz	adjusted max: -13 dBm, unadjusted max: +18 dBm

The 2 control outputs are located on the rear panel of the driver. The first is a BNC connector which provides triggering information to the pulse TWT amplifier. Its specifications are the same as in Table II PULSE TRIGGER input. The second control signal output on the driver rear panel is a multipin connector which provides information and DC power to the CW TWT amplifier. In addition the power monitoring signals used in some of the driver safety circuits utilize this multipin connector. Table IV shows the details of this multipin connector.

2.1.3 Driver Control Switches

There are 7 control switches on the driver front panel which are used to determine the operational mode of the transmitter subsystem. From left to right on the front panel these are:

- 1) Three position toggle switch (RPTR, XPNDR, IIG). This switch is used to determine the mode; repeater, transponder, or instantaneous inverse gain according to the position selected.
- 2) Two position toggle switch (A, B). This switch is not connected and is merely a spare should it be needed in future uses.
- 3) Two position toggle switch (LOOKTHROUGH, DISABLE). This switch is normally in the LOOKTHROUGH position. However, to facilitate CW power measurements the DISABLE position can be used. By setting this switch in this position the input signal at the LOOKTHROUGH BNC input is

TABLE IV
DRIVER MULTIPIN CONNECTOR SIGNAL SPECIFICATIONS

Pin	Signal	Characteristic
1	LOOKTHROUGH (BKG)	Same as LOOKTHROUGH TABLE II
2	N.C.	--
3	N.C.	--
4	VSWR SENSE (E)	-10 V DC MAX (1 ma max)
5	-15 V DC	DC Power (see Section 3.1)
6	-15 V DC	DC Power (see Section 3.1)
7	N.C.	--
8	+5 V DC	DC Power (see Section 3.1)
9	+5 V DC	DC Power (see Section 3.1)
10	N.C.	--
11	+15 V DC	DC Power (see Section 3.1)
12	+15 V DC	DC Power (see Section 3.1)
13	GND	GROUND
14	GND	GROUND
15	GND	GROUND

disconnected from the subsystem allowing easy power measurements to be made without concern for the lookthrough window.

4) Momentary contact push button switch (ALARM RESET). This switch resets the VSWR alarm circuitry to allow normal operation after an alarm condition has been detected. The circuitry is designed to give priority to the alarm condition so that if the ALARM RESET switch is pushed and the alarm condition persists, the switch command is overridden.

5) Three position wafer switch (OUTPUT FUNCTION). This switch can be set to either PULSE, TEST, or CW to select the desired operational characteristic of the driver. If conditions have been properly set on other driver front panel controls and inputs, RF power will be available at the output connector which is set on this switch. If the other driver front panel controls and inputs have not been properly set, then the ERROR LED will be illuminated.

6) Two position RF switch (L.O. ENABLE). This RF switch is set on the NORMAL position for all operating conditions except instantaneous inverse gain in which case is set to the IIG position. By setting the switch to the IIG position the solid state amplifier in the driver is used to amplify the L.O. input signal.

7) Three position toggle switch (power switch). In the OFF position all power is disconnected from the driver. In the STANDBY position all DC power supplies in the driver are turned on and the driver TWT amplifier is placed on standby (heater elements, etc.). In the OPERATE position the TWT amplifier is turned on as well, and the driver is fully operational.

2.1.4 Driver Indicators

There are 7 LED indicators and 2 lamp indicators on the driver front panel. There is a running time meter on the driver rear panel which is a measure of the operational running time of the driver TWT amplifier. The running time meter is activated only when in the OPERATE power switch position. The two lamp indicators on the front panel verify AC power is being delivered to the power supplies (STANDBY) and to both the power supplies and the TWT amplifier (OPERATE).

The 7 LED indicators verify the output function which has been selected (PULSE, TEST, CW) as well as indicating fault conditions present (ERROR, ALARM, OVERLOAD). Lighting of the ERROR LED signifies an erroneous

setting on the driver front panel such as the OUTPUT FUNCTION switch set on CW and a pulse train input into the PULSE TRIGGER input. Lighting of the ALARM LED signifies a high VSWR is present at the output of either the CW or pulse TWT amplifiers. Lighting of the OVERLOAD LED signifies problems with the driver TWT amplifier. The seventh LED (unmarked) is a spare which has been left unwired for future use if required.

2.1.5 Driver Test Points

Several test points have been made available on the driver front panel. These are included to help monitor the driver operation, aid in trouble-shooting, and facilitate set-up and check-out procedures. Table V provides information about the signals available at each test point.

TABLE V
DRIVER TEST POINTS

Test Point	Signal	Characteristic
+5 V DC	DC pwr	See Section 3.1
+15 V DC	DC pwr	See Section 3.1
-15 V DC	DC pwr	See Section 3.1
GND	Ground	Ground
TP1	Mod input	6 V max
TP2	VSWR level set	-5.5 V DC (CW); -1.45 V DC (pulse)
TP3	VSWR level test	-10 V DC max
TP4	Missing pulse set	TTL levels
TP5	IIG phase set	10 V max VIDEO
TP6	N.C.	N.C.
TP7	N.C.	N.C.
TP8	N.C.	N.C.

The top row can be used to monitor the main DC power supplies, +5 V DC, +15 V DC, -15 V DC and ground (GND). These can also be used as power supply sources if necessary; however, the individual power supply specifi-

cations should be checked to ensure no damage will be caused by such usage.

TP1 is used to monitor the input into the pin diode modulator in the driver RF chain. TP2 is used to set and monitor the VSWR limits for both pulse and CW operation. TP3 is used to verify the settings of TP2 by applying the specified voltages for pulse and CW. TP4 is used to monitor the output of the missing pulse detector used in the circuit which protects the pulse TWT amplifier from being constantly turned on. TP5 is used in setting the phase of the auxiliary receiver output. TP6, 7, and 8 are not connected.

2.1.6 Driver RF Gain Control

The driver RF gain control provides continuous attenuation of the RF signal from 0 dB to 30 dB. In normal operation this attenuator would be set totally counter clockwise so as to provide 0 dB attenuation of the RF signal; however, it has been provided to allow flexibility which could be required in field operations.

2.1.7 Driver RF Chain

The driver RF chain is shown in Figure 5. It passes and amplifies signals in the 8-11 GHz range to power levels sufficient to drive the CW and pulse TWT amplifiers to maximum power output over most usable input power levels. The principal driver RF components are listed in Table VI and their specifications can be found in Section 3.1.

In either the repeater or transponder mode the RF signal is introduced into the driver via the AUX ANT or the RCVR RF input, respectively. Passing through the SPDT and the A side of the DPDT it is fed to the solid state amplifier (SSA). The SSA acts to amplify small level RF signals and to limit higher level signals to a level which, when adjusted by the 30 dB pad, will not cause the driver TWT to go beyond saturation. The RF signal from the SSA output is fed through the B side of the DPDT to the 30 dB pad for the above mentioned adjustment. The signal is further passed through the 30 dB ATTN (RF GAIN CONTROL on the driver front panel), the PIN MOD and to the driver TWT. Due to the limiting action of the SSA this TWT will not go beyond the maximum output level at saturation once the 30 dB PAD preceding it has been properly adjusted. The output of the driver TWT is passed through a second 30 dB PAD which is used to adjust the RF power

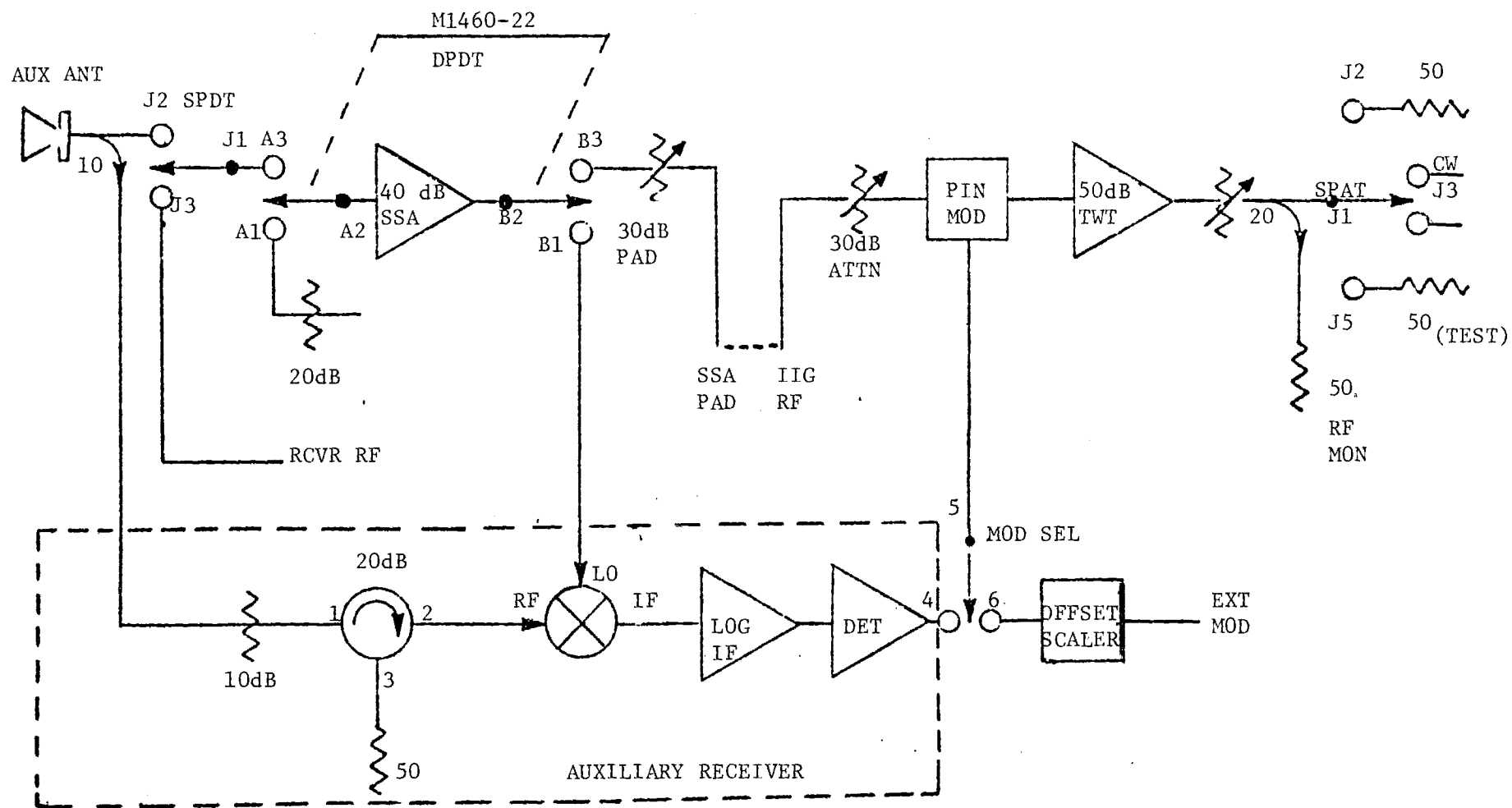


Figure 5. Driver RF Chain

level this time to prevent over-saturation of succeeding amplifiers. The 20 dB coupler provides the RF MON signal to the driver front panel and finally the SP4T directs the RF channel to the proper output connector; PULSE, TEST, or CW. The fourth terminal of the SP4T is used to terminate the RF energy into a 50 Ω load when a fault condition or VSWR ALARM condition exists. Figure 6 shows a simplified block diagram of the RF chain from either the AUX ANT or the RCVR RF input connector to the output connectors.

TABLE VI
DRIVER RF CHAIN PRINCIPAL COMPONENTS

Component	Manufacturer/Model
10 dB coupler	ARRA 6164-10
SPDT	General Microwave F8928
DPDT	Transco M1460-22
Solid State Amp (SSA)	W-J 5311-7
30 dB PAD (QTY2)	ARRA 6804-30 (Form 2191)
30 dB ATTN	ARRA 6804-30 (Form 3279)
PIN MOD	General Microwave D1958
TWT	Teledyne M9172N
20 dB coupler	ARRA 6164-20
SP4T	General Microwave F9140

Table VII shows the RF power levels present at key points in this simplified block diagram. Proper settings of the two 30 dB pads has been assumed for CW or pulse operation and all transmission losses have been taken into account. Figure 7 displays this input/output relation in graphic form.

These power levels are ± 0.5 dB across the 8-11 GHz band. The maximum RF power level from the driver is +34 dBm once all the intentional losses have been removed. The small signal gain for the driver is 43 dB for CW operation, and 59 dB for pulsed operation. The maximum attainable small signal gain if all intentional RF losses are removed is 85 dB; how-

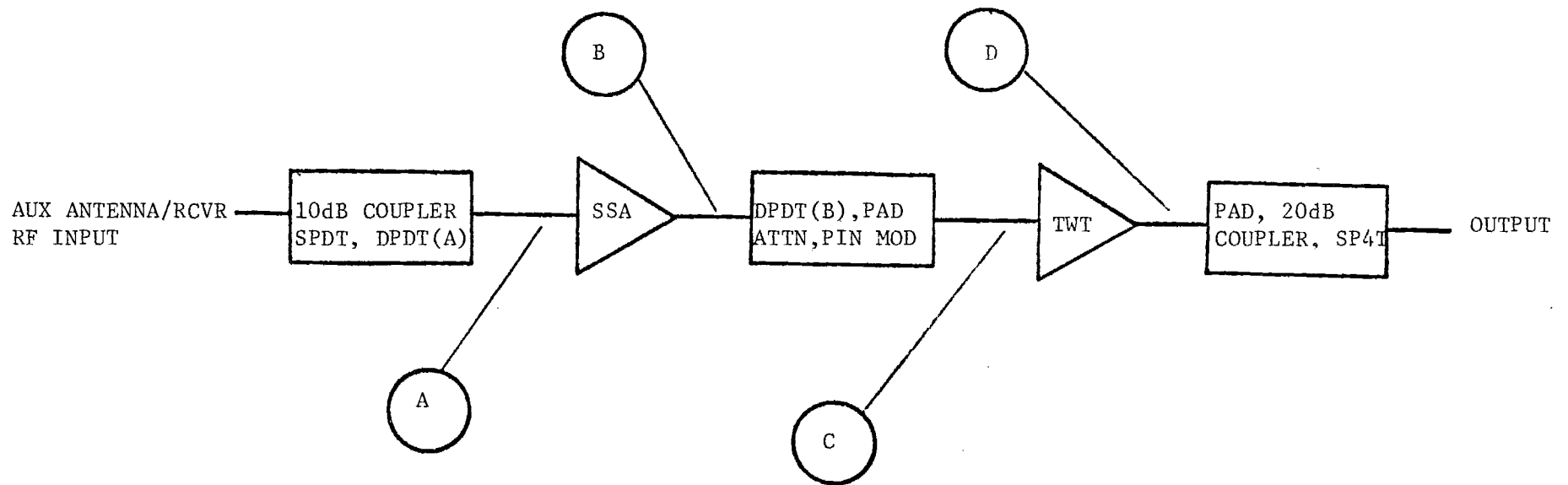


Figure 6. Simplified Block Diagram of Driver RF Chain

TABLE VII
ADJUSTED RF POWER LEVELS AT KEY POINTS
ON DRIVER RF CHAIN

INPUT (dBm)	A (dBm)	B (dBm)	C (dBm)	D (dBm)	DRIVER OUTPUT (dBm)	
					CW	Pulse
-100	-104	-58.5	-79.5	-26	-57	-41
- 90	- 94	-48.5	-69.5	-16	-47	-31
- 80	- 84	-38.5	-59.5	- 6	-37	-21
- 70	- 74	-28.5	-49.5	4	-27	-11
- 60	- 64	-18.5	-39.5	14	-17	- 1
- 50	- 54	- 8.5	-29.5	24	- 7	9
- 40	- 44	1.5	-19.5	32	1	17
- 37	- 41	4.5	-16.5	34	3	19
- 33	- 37	8.5	-12.5	36	5	21
- 30	- 34	11	-10	37	6	22
- 27	- 31	12.5	- 8.5	37.5	6.5	22.5
- 23	- 27	14.	- 7	38	7	23
-20 through +10	- 24 min	15.	- 6	38	7	23

DRIVER
OUTPUT POWER (dBm)

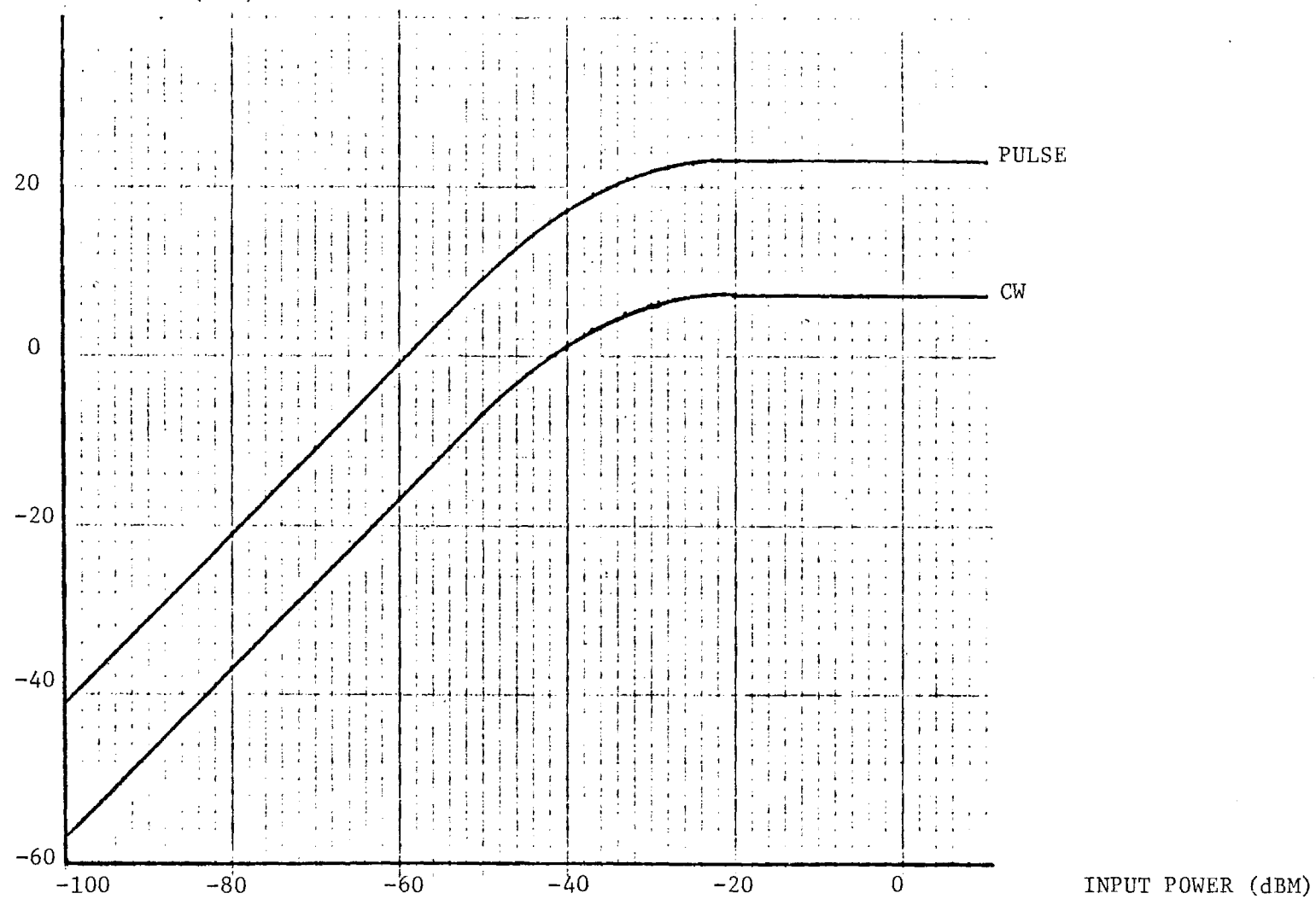


Figure 7. Driver Input/Output Relation Adjusted For Pulse Or
CW Operation

ever, caution should be exercised if the preset pads must be changed to increase gain. Failure to monitor the output of the driver could cause damage to the TWT amplifier within the driver or external TWT amplifiers.

Table VII can also be utilized to figure the effective AM introduced via the PIN MOD. As can be seen from Figure 6, if the RF signal level at point B is known, then the signal level at the output of the driver can readily be obtained from the table. For example, if a +11 dBm signal exists at point B, then the maximum signal level at point C is -10 dBm, while the minimum is 60 dB lower (10 dB/V, 6 V max for the PIN MOD) or -70 dBm. For CW operation the output of the driver then is +6 dBm max and -46.5 dBm min.; a total AM depth of 52.5 dB out of the driver. A complete table is shown for the transmitter subsystem as a whole in Section 2.6.

For the IIG mode the RF input to the driver is the IIG RF type N connector on the driver front panel. As such this input is equivalent to point B in Figure 6 and therefore Table VII can also be utilized as above with the input level being applied at point B.

Third harmonic intermodulation distortion (IMD) was measured for the driver. The worst case was discovered when two RF signals of different frequencies in the 8-11 GHz range whose third harmonic intermodulation coincided with the 8-11 GHz were introduced at the maximum allowable input power (+10 dBm). The result was an IMD which was at worst 10 dB below either of the two intentional RF signals. Decreasing either of the two intentional RF signals slowly decreased the IMD level until the SSA was no longer saturating both of the input signals. The IMD then fell at a much faster rate. Figure 8 shows the results of these tests when the input frequencies were 8 and 9 GHz thus generating a 10 GHz IMD signal.

2.1.8 Driver Electronic Circuits

The electronic circuitry within the driver is designed to accomplish basic electronic switching as commanded by the front panel controls or from fault detection signals. The driver electronic circuitry is contained within on printed circuit (PC) board which is the larger of the two PC boards housed in the driver chassis, and within an internally mounted metal box. The smaller PC board contains circuitry belonging to the auxiliary receiver.

OUTPUT POWER dBm

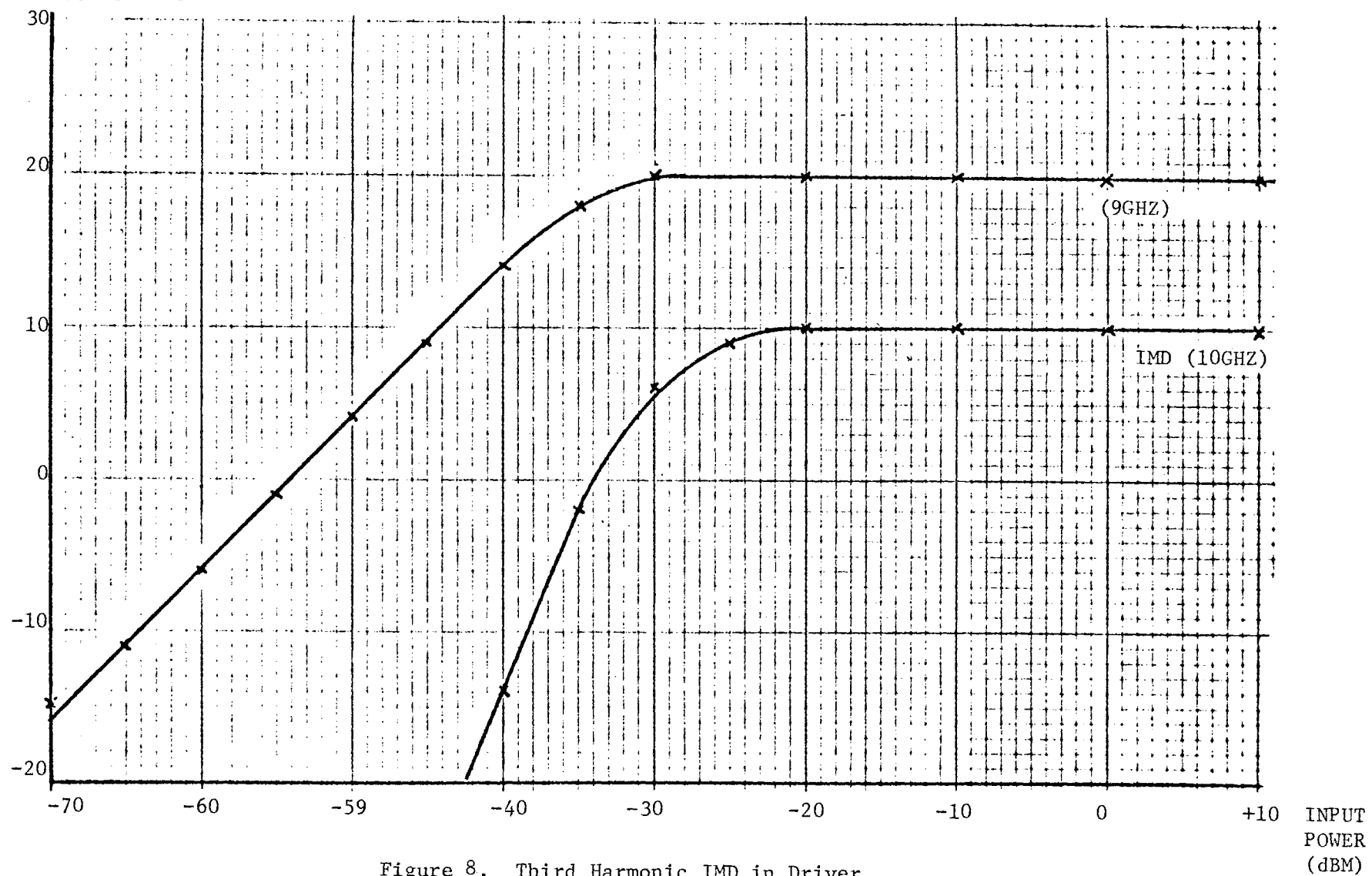


Figure 8. Third Harmonic IMD in Driver

The driver electronic circuitry can be separated into six main functional blocks. These are:

- 1) VSWR protection
- 2) Missing pulse detector
- 3) SP4T control
- 4) LED drivers
- 5) PIN MOD DC offset/scaler
- 6) Trigger shaping

The combined circuit schematics for these are found in Section 3.1. Individual circuit schematics are included in this section for clarity only.

The VSWR protection circuit (Figure 9) senses a voltage level which is proportional to the reflected power at either the pulse or CW TWT amplifier output. This level is then compared to a preset maximum level which is automatically set according to the position of the OUTPUT FUNCTION switch on the driver front panel. If the preset maximum level is exceeded the VSWR alarm flip-flop is DC preset causing the SP4T to redirect the RF energy into the driver internal 50 Ω coax load thus removing the cause of the fault. The LEDS labeled ALARM and ERROR are also lit at this time. The VSWR alarm flip-flop is reset by pushing the ALARM RESET push button switch on the driver front panel. Since this switch is a momentary contact switch the flip-flop can immediately preset again if the conditions which caused the initial alarm are still present.

The missing pulse detector (MPD) receives a pulse train from the signal processing subsystem and maintains a high TTL level at the output of the timer (TP4) as long as the pulse train is present. If the pulses cease this output goes to a TTL low which in turn causes the SP4T to redirect the RF energy into the driver internal 50 Ω coax load if the OUTPUT FUNCTION switch is set to the PULSE position. This prevents RF energy from reaching the pulse TWT amplifier and thus eliminates the possibility of causing damage to it due to the trigger input remaining in an ON condition for extended periods of time. The ERROR LED is lit if these conditions are satisfied. The MPD circuit is shown in Figure 10.

The SP4T control circuitry senses switch positions and fault conditions to direct the RF energy to the proper output connector or to the driver internal 50 Ω load. The truth table for the SP4T switch is shown as Table 8, where J2 is the internal load position, J3 is the CW position,

Figure 9. VSWR Protection Circuit

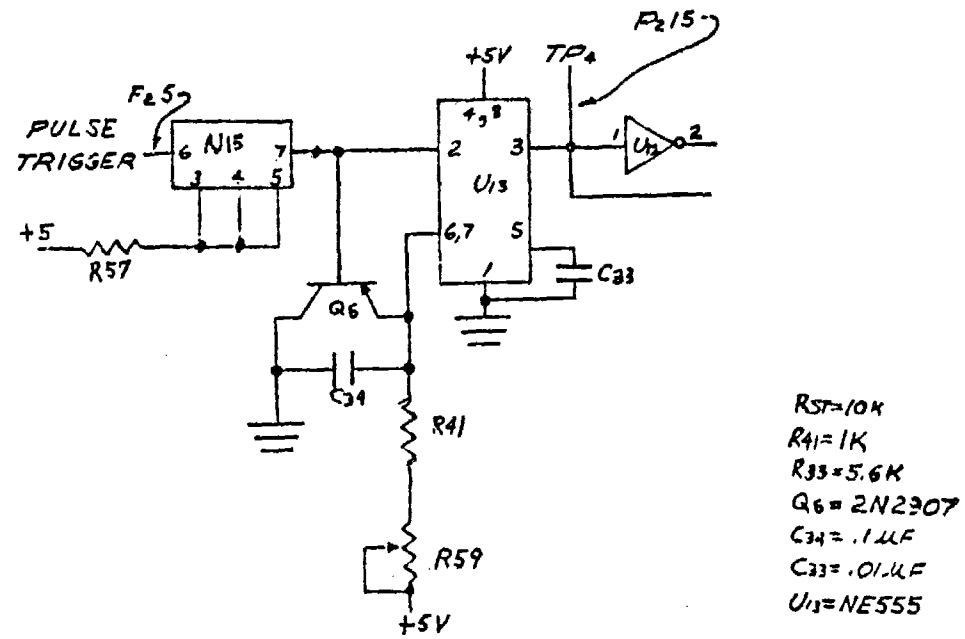


Figure 10. Missing Pulse Detector (MPD) Circuit

TABLE VIII
DRIVER SP4T TRUTH TABLE

Missing Pulse Detector	Look- through	OUTPUT FUNCTION			VSWR ALARM	SP4T				Condition
		CW	TEST	PULSE		J2	J3	J4	J5	
H	L	L	H	H	L	ON	OFF	OFF	OFF	ERROR
H	H	L	H	H	L	ON	OFF	OFF	OFF	ERROR
H	L	H	L	H	L	OFF	OFF	OFF	ON	TEST
H	H	H	L	H	L	OFF	OFF	OFF	ON	TEST
H	L	H	H	L	L	OFF	OFF	ON	OFF	PULSE
H	H	H	H	L	L	ON	OFF	OFF	OFF	ERROR
L	L	L	H	H	L	OFF	ON	OFF	OFF	CW (XMIT)
L	H	L	H	H	L	ON	OFF	OFF	OFF	CW (LOOKTHROUGH)
L	L	H	L	H	L	OFF	OFF	OFF	ON	TEST
L	H	H	L	H	L	OFF	OFF	OFF	ON	TEST
L	L	H	H	L	L	ON	OFF	OFF	OFF	ERROR
L	H	H	H	L	L	ON	OFF	OFF	OFF	ERROR
X	X	X	H	X	H	ON	OFF	OFF	OFF	ERROR VSWR ALARM
X	X	X	L	X	H	OFF	OFF	OFF	ON	VSWR ALARM LEVEL SET

J4 is the pulse position, and J5 is the test position. A TTL low (L) generates the ON condition. Figure 11 shows the schematic for the SP4T control circuit.

The LED drivers utilize open collector TTL drivers, along with current limiting resistors that allow sufficient current to flow through the LED's for illumination (13 ma). The inputs to the drivers are obtained from the three circuits described previously in this section as well as from the multipin connector on the driver TWT amplifier. The schematics for the LED drivers are shown in Figure 12.

The PIN MOD DC offset/scaler acts as the interphasing circuit between any externally generated AM signals and the pin diode modulator. By properly adjusting the two potentiometers in the circuit the gain of the circuit and the DC level of the signal can be varied. A maximum gain of 2.5 is attainable while the DC offset is variable from 0 to 6 volts. The polarity of modulating signal can be inverted through operation of a PC mounted switch. When the mode control switch on the driver front panel is placed in the IIG position, the external AM feature is disconnected and only signals from the auxiliary receiver can reach the PIN MOD. The 3 diodes at the output of the circuit prevent damage to the pin modulator which could be caused by overdriving its input. Figure 13 shows the schematic for the DC offset/scaler circuit. The trigger shaping circuit changes the TTL pulse trigger signal from the signal processing subsystem to a 15 V signal which can drive the pulse TWT amplifier. It is housed in a separate metal box inside the driver. The input and output of this box are SMA connectors. Figure 14 shows the circuit schematic for the trigger shaping circuit.

2.2 Auxiliary Receiver Description

The auxiliary receiver is incorporated into the driver drawer and is designed to give the transmitter subsystem an instantaneous inverse gain (IIG) capability against scanning type radars. A simplified block diagram of the auxiliary receiver is included in Figure 15, The RF frequency from the scanning radar is coupled from the auxiliary antenna and passed through a 10 dB pad and a 20 dB circulator which serve to prevent reradiation from the mixer RF input back out of the auxiliary antenna by 40 dB of isolation. The LO frequency is obtained from the signal processing sub-

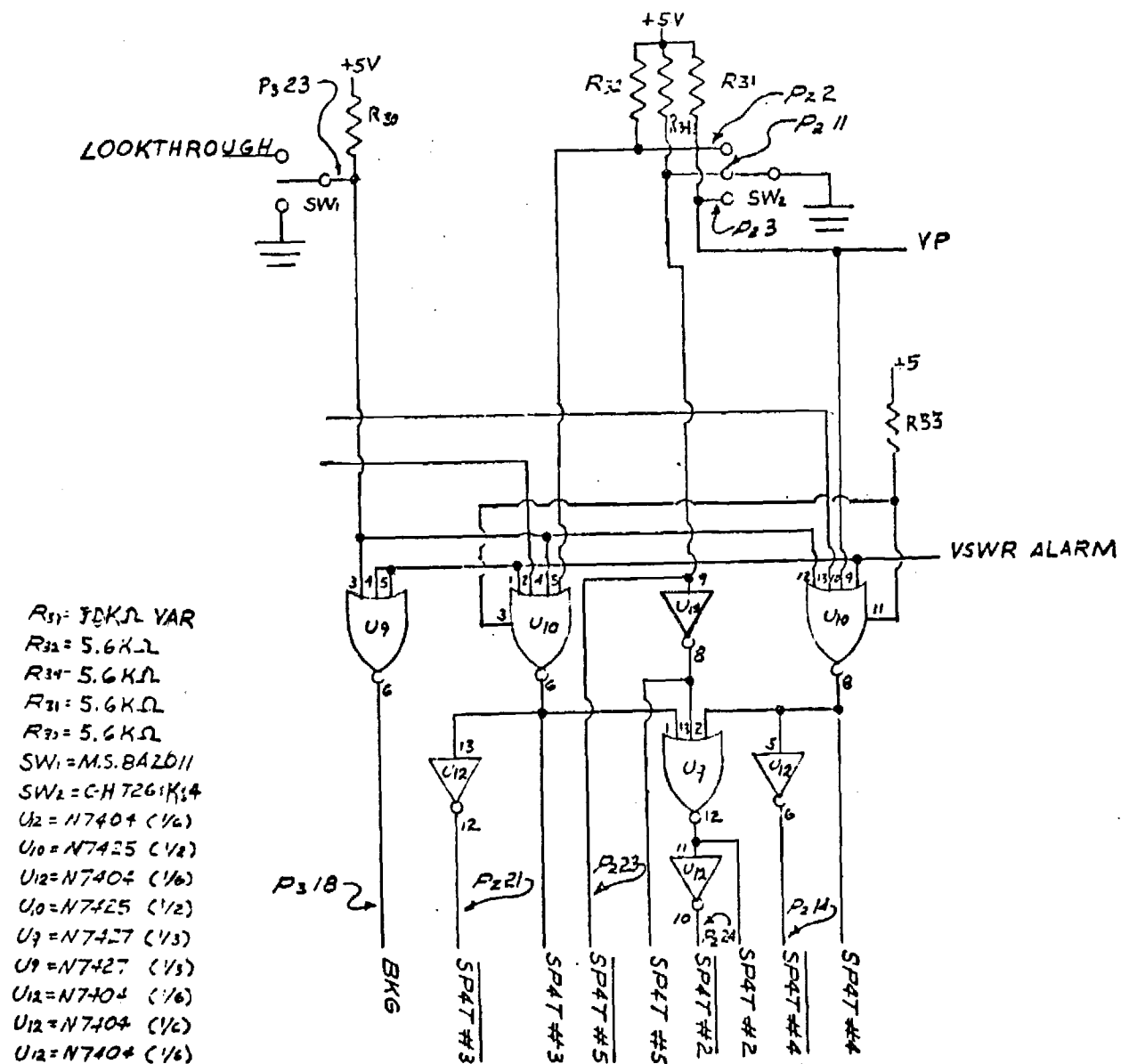
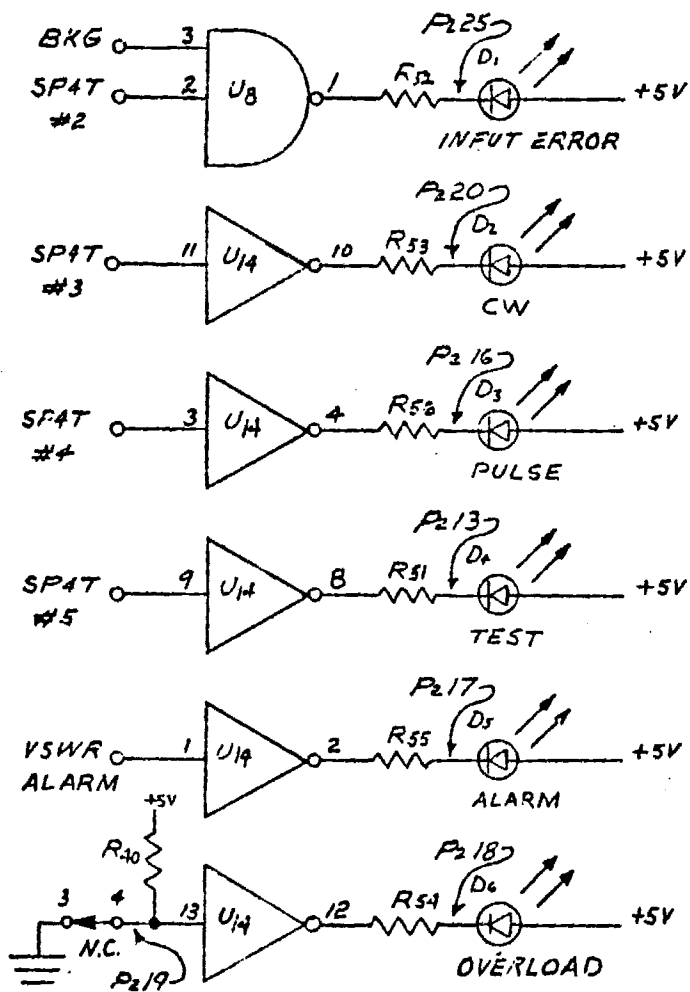


Figure 11: VSWR Alarm Circuit



$R_{51} = 270\Omega$
 $R_{53} = 270\Omega$
 $R_{52} = 270\Omega$
 $R_{51} = 270\Omega$
 $R_{53} = 270\Omega$
 $D_1 = \text{HP-5082-4655}$
 $D_2 = \text{HP-5082-4655}$
 $D_3 = \text{HP-5082-4655}$
 $D_4 = \text{HP-5082-4655}$
 $D_5 = \text{HP-5082-4655}$
 $U_8 = \text{N7401 (1/4)}$
 $U_{14} = \text{N7406 (1/6)}$
 $U_{14} = \text{N7406 (1/6)}$
 $U_{14} = \text{N7406 (1/6)}$
 $U_{14} = \text{N7406 (1/6)}$
 $U_{14} = \text{N7406 (1/6)}$
 $R_{54} = 270\Omega$
 $R_{40} = 5.6K\Omega$
 $D_6 = \text{HP-5082-4655}$
 $R_{28} = 5.6K\Omega$
 $R_{29} = 5.6K\Omega$

Figure 12. LED Drivers Circuit

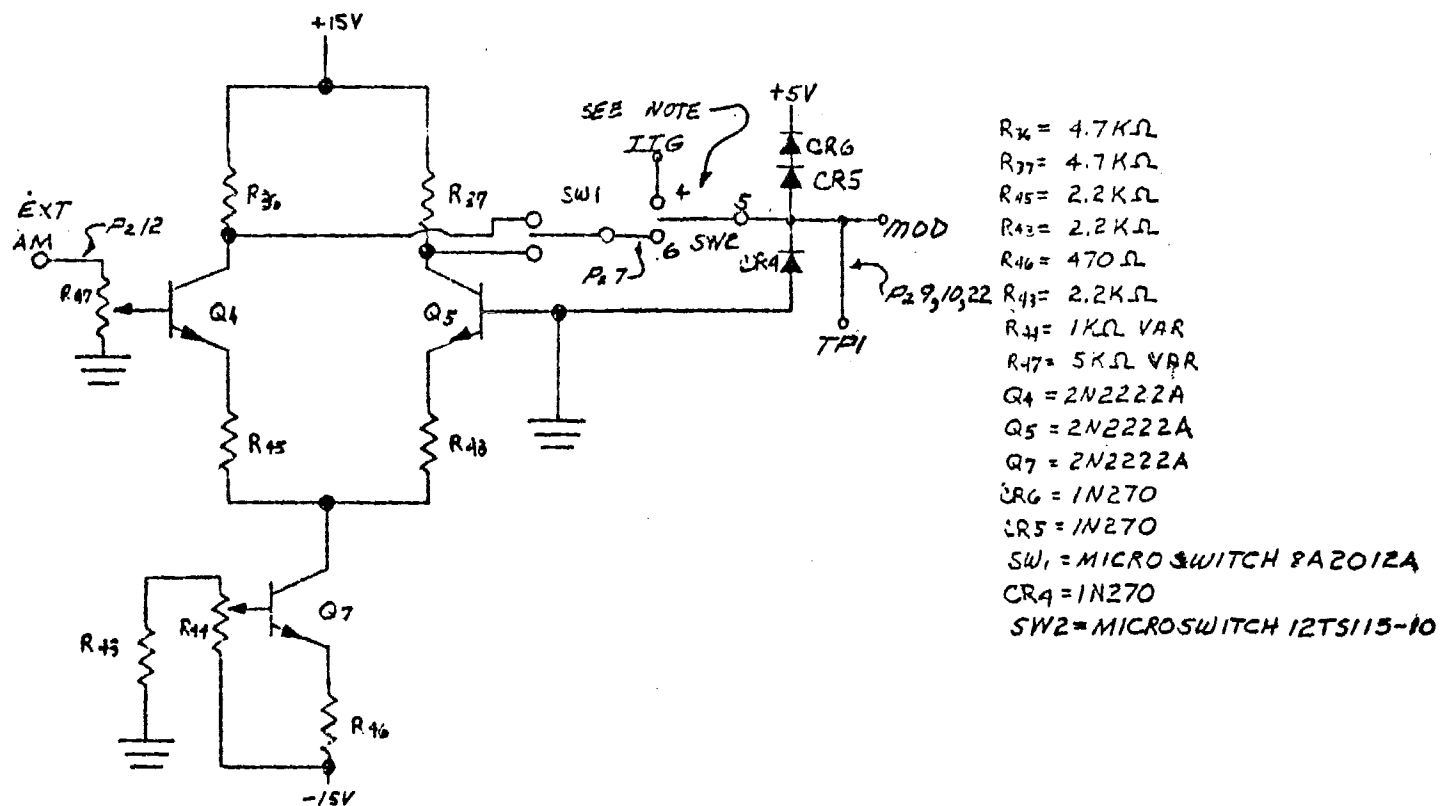


Figure 13. PIN MOD DC Offset/Scaler Circuit

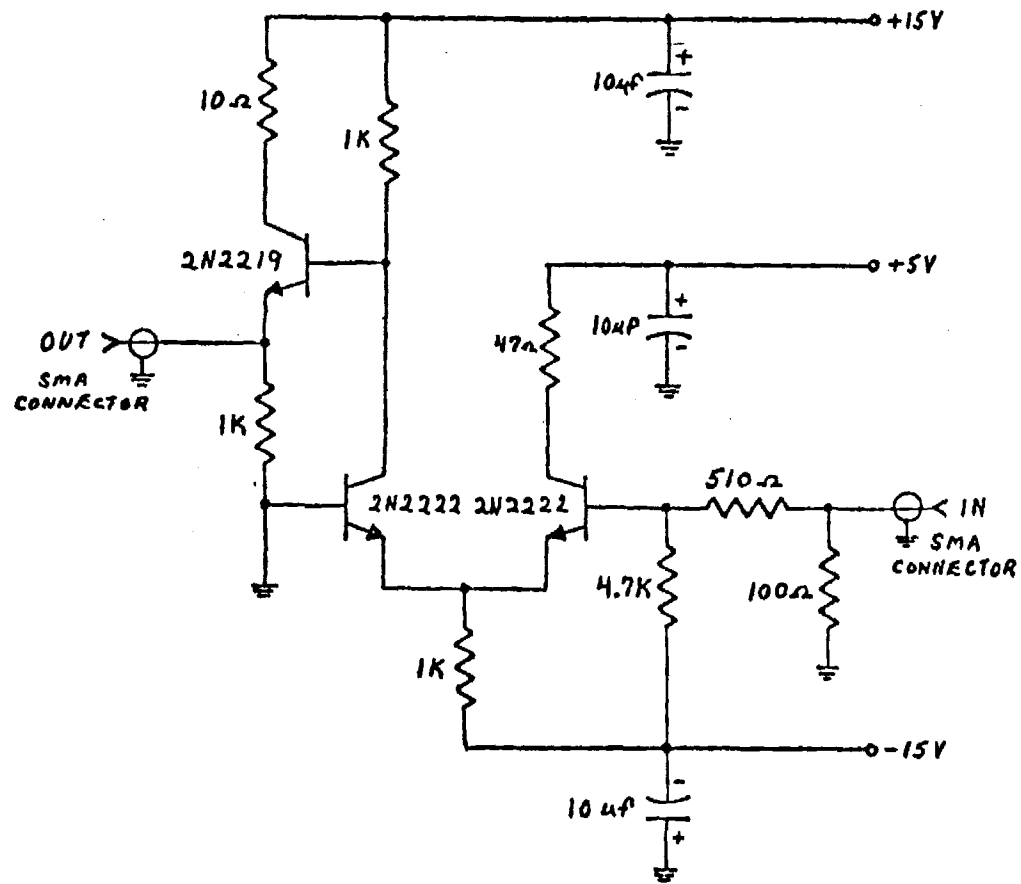


Figure 14. Trigger Shaping Circuit

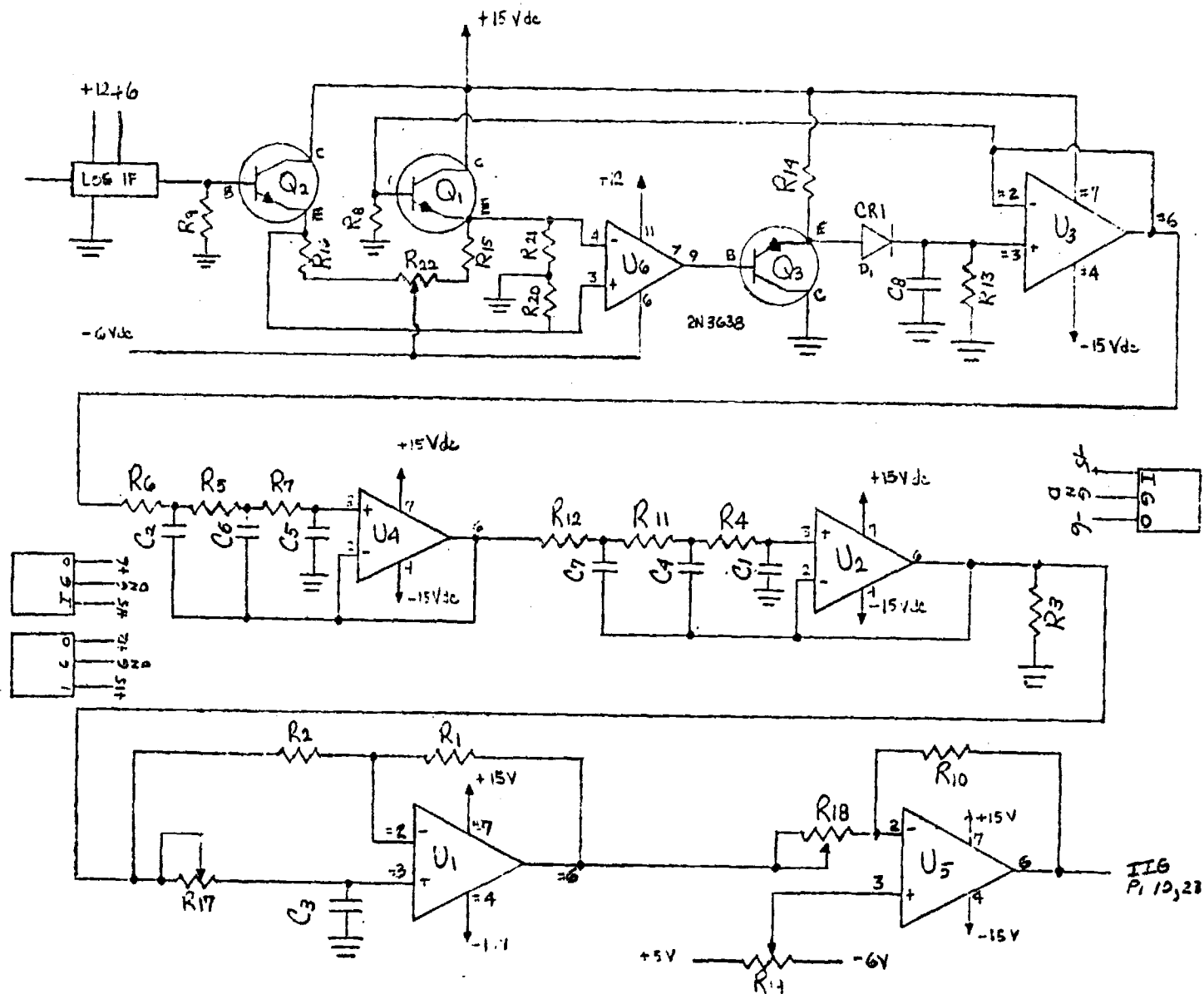


Figure 15. Auxiliary Receiver Detector

system and passed through a 20 dB pad and the 40 dB solid state amplifier before it is delivered to the mixer. The combination, using the Anaran 7F0128 balanced mixer, gives an S/N ratio of 40 dB when a -30 dBm signal is present at the auxiliary antenna. The resulting IF frequency is then processed through a log IF amplifier and detected.

A schematic diagram of the detector is shown in Figure 15. The portion of the circuit between Q2 and U3 performs the detection and sample and hold (S/H) function. U4, U2, and associated input resistors and capacitors filter the detected signal, while resistor R17 can be adjusted to provide the desired phase shift to the audio frequency which is necessary for successful IIG. Resistor R18 provides a gain control which adjusts the amplitude of the signal being delivered to the driver PIN MOD. The point at which this signal comes into the PIN MOD circuitry can be seen in Figure 13. Detailed descriptions of components can be found in Section 3.

2.3 CW TWT Amplifier Description

The CW TWT amplifier drawer, shown in Figures 16 and 17, houses not only the CW TWT and power supply, but also provides various monitoring points, houses power monitors used with safety circuits, accomplishes the switching function between PULSE and CW operation, and provides the output waveguide which is the input to the polarizer. A simplified block diagram of this drawer is shown in Figure 18.

2.3.1 CW TWT Amplifier RF Chain

The RF from the transmitter subsystem driver is the input to the CW TWT. The amplifier provides a minimum of 46 dB of gain in the 8-11 GHz frequency band at saturation power output of 500 watts. This RF signal is fed to one port of a two position, four port waveguide switch so that the energy is directed to the waveguide leading to the polarizer or terminated into a 500 W, 50 Ω load. The remaining port in the waveguide switch is used as the input for the energy being delivered from the PULSE TWT, so that its distribution is opposite from that of the CW TWT amplifier. When the CW TWT is being utilized its energy is guided toward the polarizer so that the PULSE TWT energy is guided into the dummy load and vice versa.

The RF output from the waveguide switch is then fed through a harmonic filter which reduces the second harmonic by at least 40 dB. A 40 dB cross-

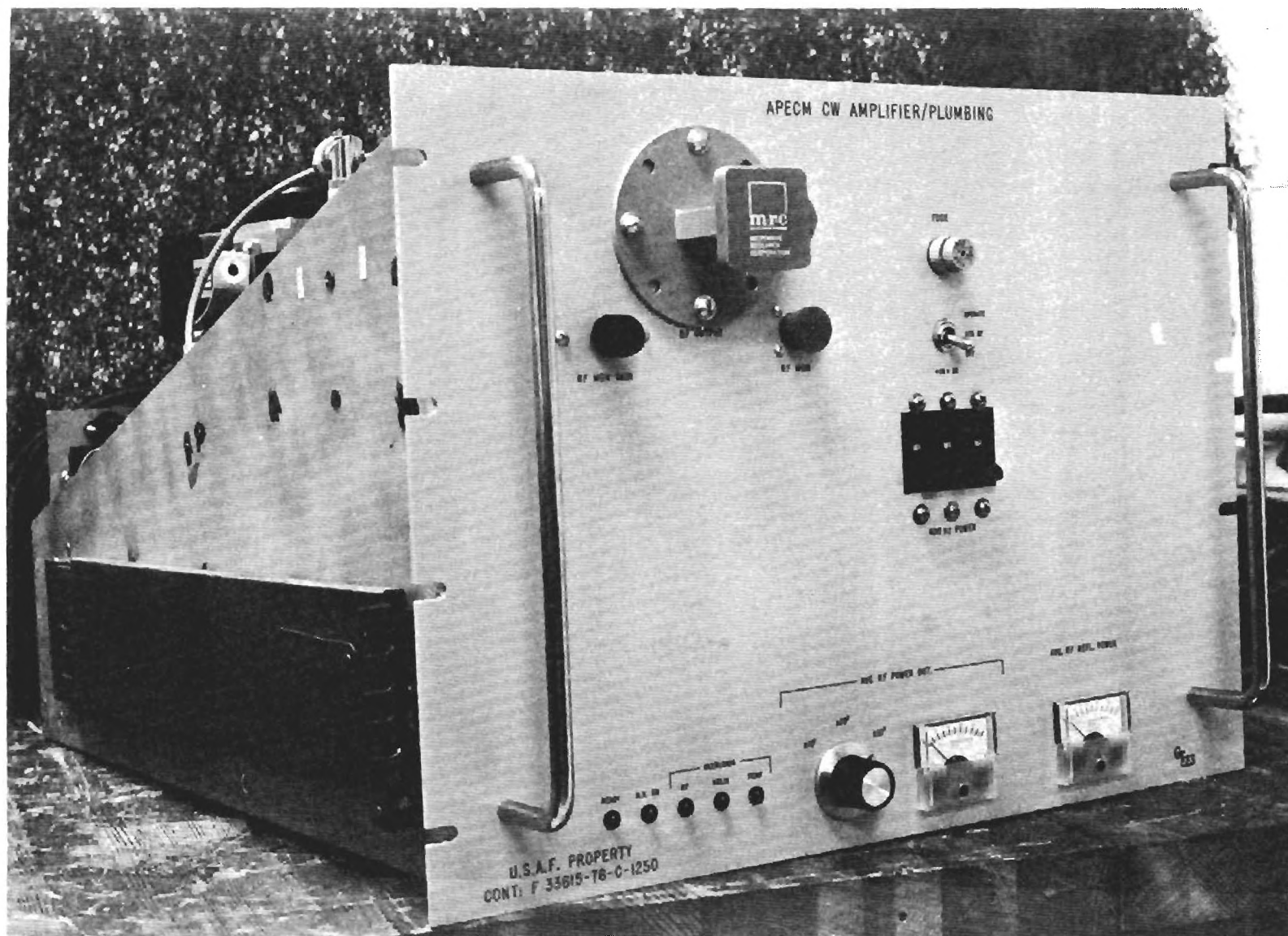


Figure 16. CW Amplifier/Plumbing Drawer (front view)

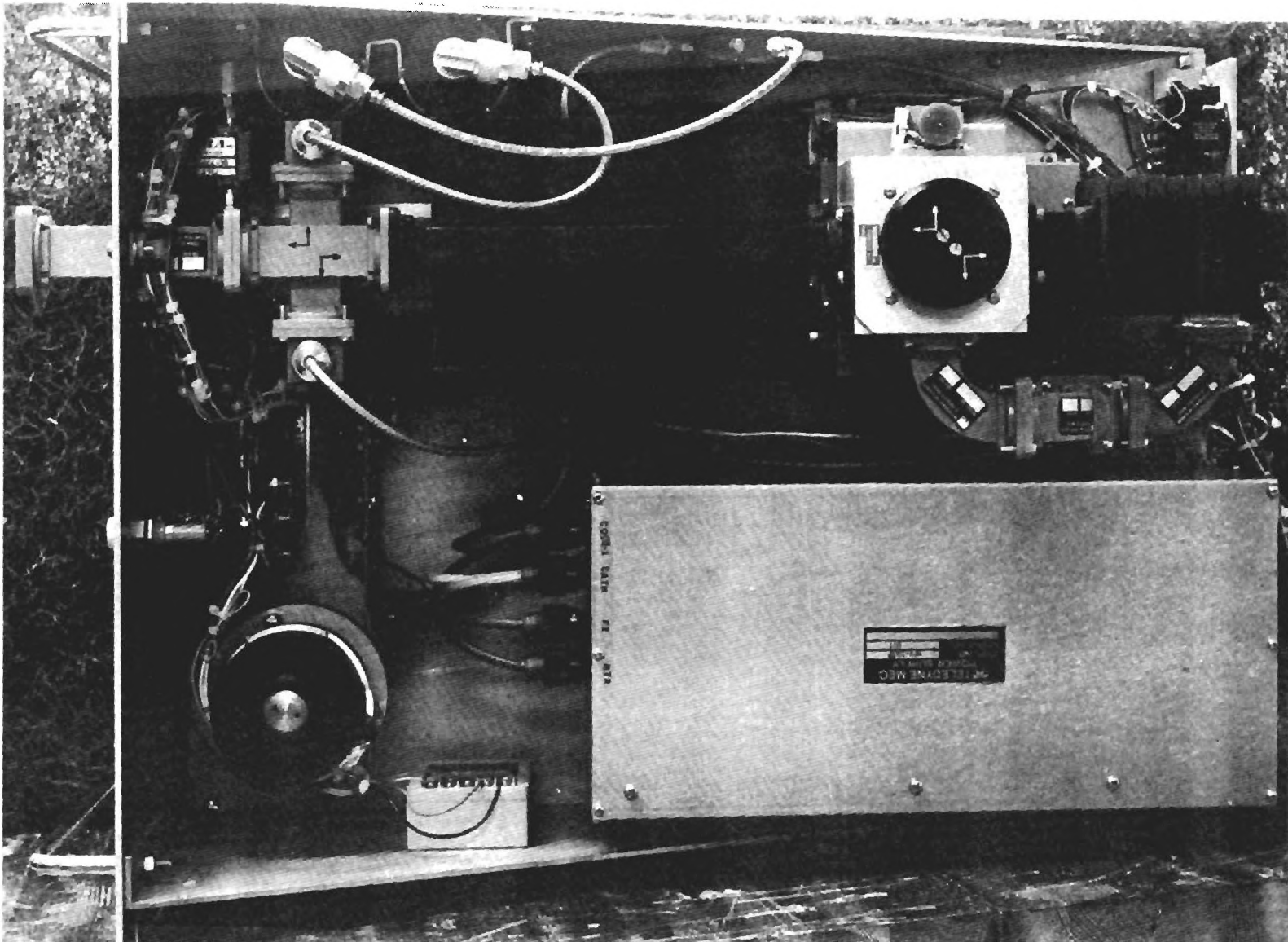


Figure 17. CW Amplifier/Plumbing Drawer (top view)

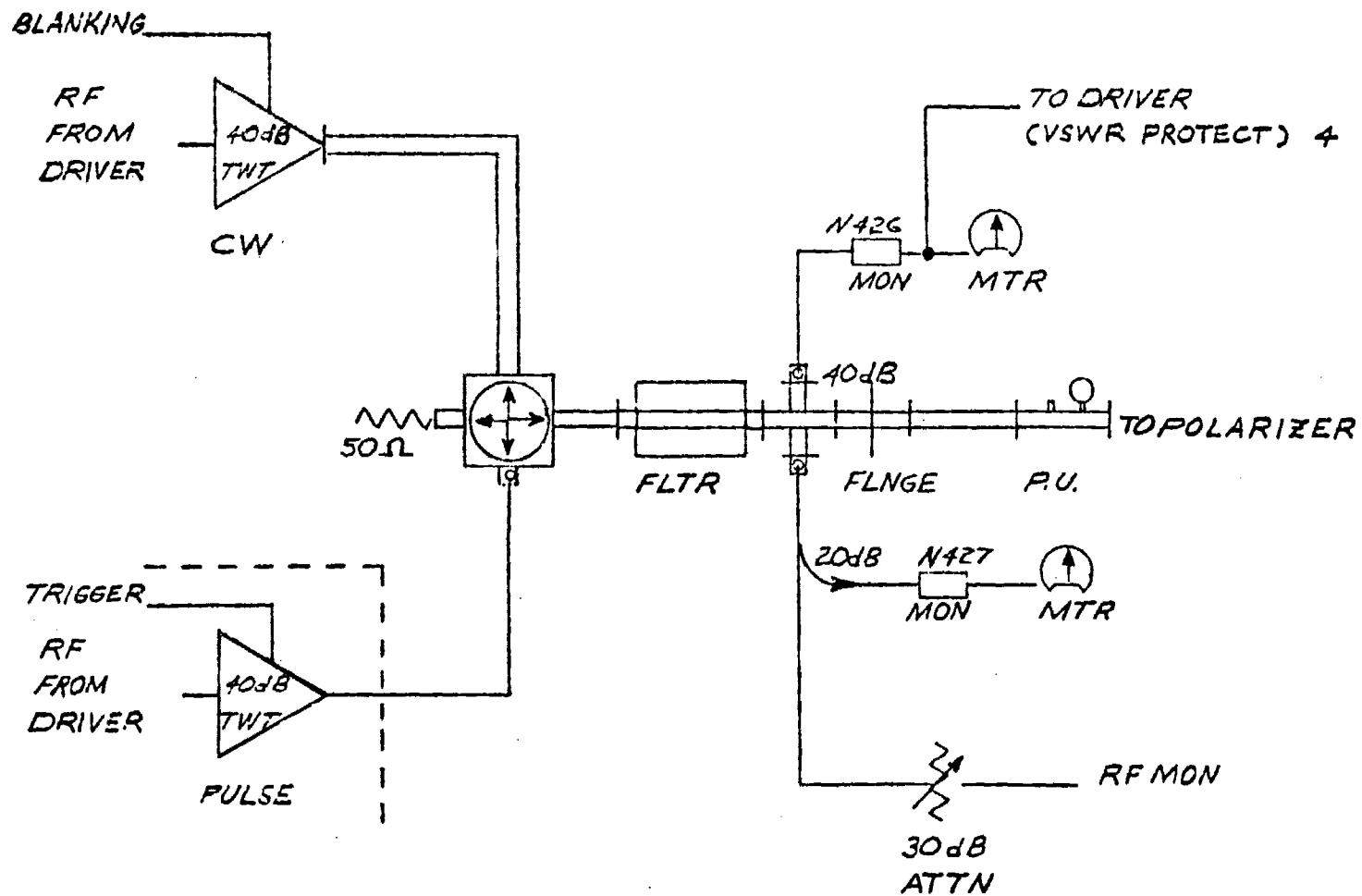


Figure 18. CW TWT Amplifier Drawer (schematic)

guide coupler serves to monitor the incident and reflected energy in the waveguide. These are displayed by two meters in the CW TWT drawer front panel as well as utilized in other safety and monitoring applications. The blanking input disconnects a portion of the TWT power supply to provide a lookthrough capability for the APECM system.

2.3.2 CW TWT Amplifier Safety Circuits

The CW TWT amplifier itself has several safety circuits which are internal to it. These safety circuits, which are externally monitored by LED's in the CW TWT drawer front panel, are:

- a) High Voltage ON indicate
- b) Ready indicate
- c) Helix Overload indicate
- d) Temperature Overload indicate
- e) RF Overload indicate.

Any one of these which detects a fault would automatically shut off the amplifier to prevent further damage.

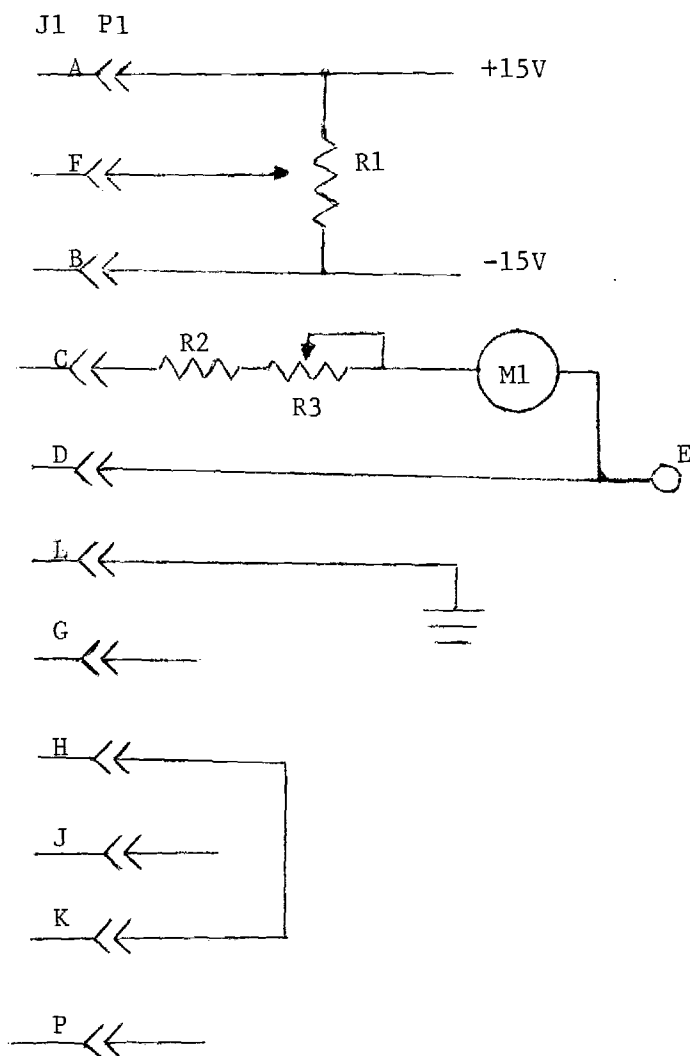
In addition to these, the reflected power back to the CW TWT drawer is constantly being monitored by the power monitor which is attached to the crossguide coupler. This power monitor sends a negative DC level to the VSWR ALARM detect circuitry of Figure 9 in the driver drawer. If the detected reflected power exceeds a preset level, the CW TWT amplifier is shut off via the blanking input which is also used for lookthrough. The power monitors wiring diagram is shown in Figure 19, and the DC voltages needed to bias them is obtained from the driver drawer via the multipin connector discussed in Section 2.1.2.

A detailed description of the components which make up the CW TWT amplifier drawer is given in Section 3.

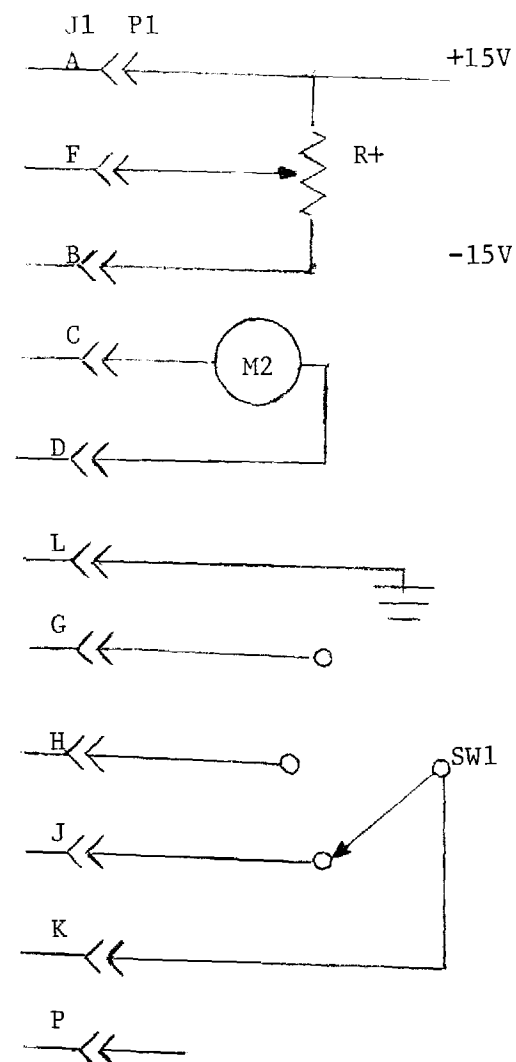
2.4 Pulse TWT Amplifier Description

The pulse TWT and associated power supply, shown in Figure 20, were manufactured by Litton Industries. The pulse TWT provides 2 KW of saturated output power from 8-11 GHz. The minimum gain required to drive the TWT to saturation is 47 dB.

The pulse TWT obtains both RF and trigger signals from the driver drawer, amplifies the pulsed RF, and delivers the energy to the waveguide



J1 = BT07A14-15P (N426)
 P1 = MS3116E14-15S
 R1 = 25K VAR
 R2 = 8.2K
 R3 = 2K VAR
 M1 = WESTON 7511-4841001



J1 = BT07A14-15P (N427)
 P1 = MS3116E14-15S
 R4 = 25K VAR
 M2 = WESTON 7511-4841001
 SW1 = C-H 7261k14 (MS25002-1)

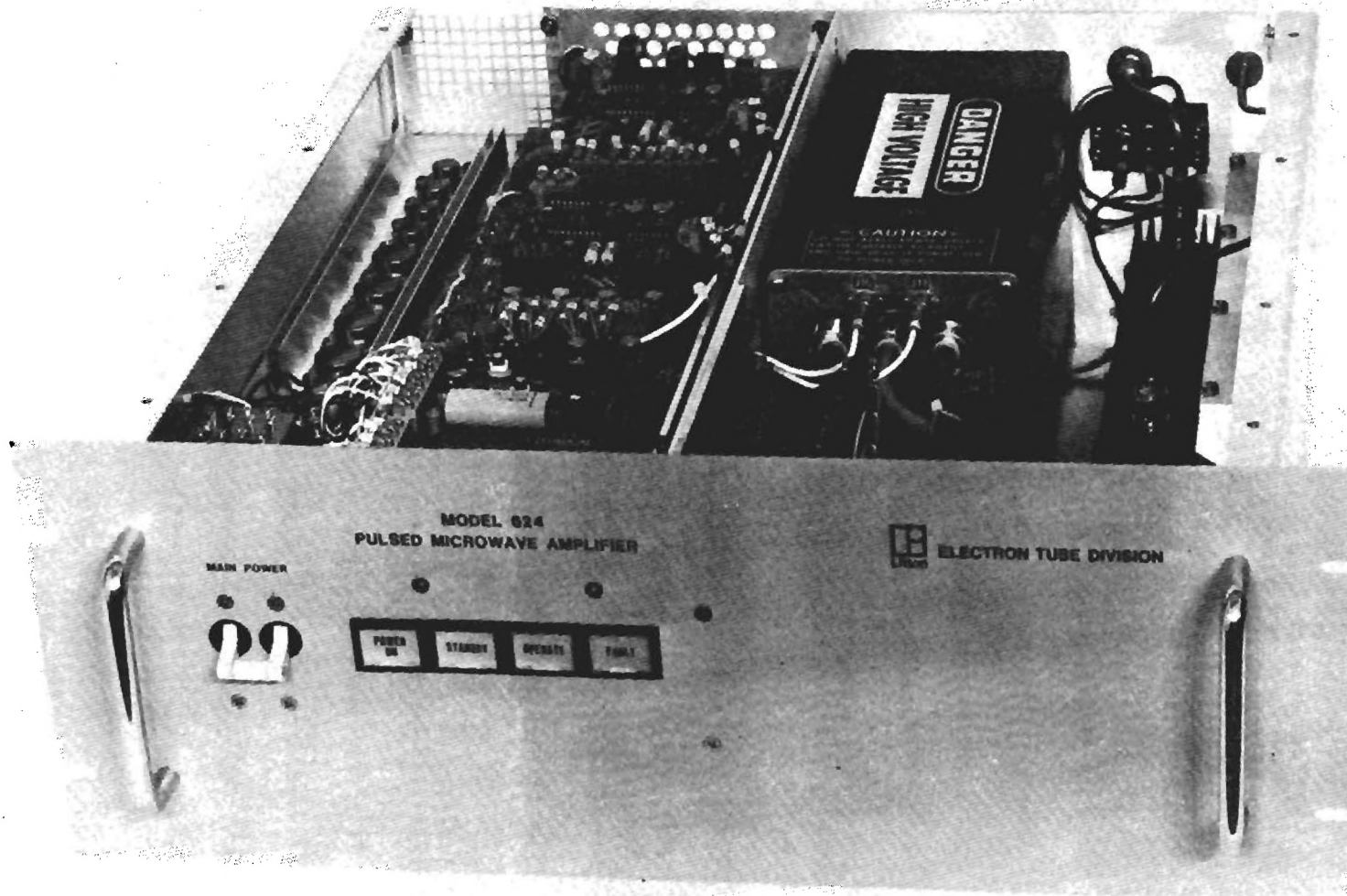


Figure 20. Pulse Amplifier Drawer

switch in the CW TWT drawer. Its output is protected by the same external safety circuits which protect the CW TWT, but to different levels which are preset when the OUTPUT FUNCTION switch in the driver front panel is set to the PULSE position.

The Pulse TWT is also internally protected for temperature overload, current overload, and grid pulse width limit control. The maximum duty cycle allowed is preset to 2% while the maximum pulse width allowed is preset to 11 μ sec.

A detailed description of the Pulse TWT specifications can be found in Section 3.

2.5 Antennas Description

Since the dual circularly polarized antenna used as the main antenna is covered in great detail in Volume 1 of the Operation and Maintenance Handbook, it will not be duplicated here. For detailed information regarding this antenna consult Volume 1. The antennas which will be described here are the auxiliary antenna and the wingtip antennas.

2.5.1 Auxiliary Antenna

This dual circularly polarized antenna consists of a square pyramidal horn fed by a polarizer consisting of a square waveguide section with a diagonal dielectric insert. The polarizer is in turn fed by a dual mode transducer. The antenna was tested with waveguide-to-coax adapters mounted at the orthogonal ports of the dual mode transducer. A shim had been previously added to one arm of the dual mode transducer for phase matching. The antenna was constructed from a dual linearly polarized antenna built by Georgia Tech for a previous internally funded project. It was converted to a dual circularly polarized antenna in order to provide a back-up antenna to the APECM system should the need arise for its use as the main polarization antenna and its parameter specifications were relaxed from those of the main antenna in order to test these effects upon the overall performance of the system. Some of the measured data relative to the nominally desired performance are discussed below.

2.5.1.1 VSWR

No performance goal was placed on this parameter. Return loss was measured over the 8.5 to 9.5 GHz range looking into each port of the

dual mode transducer. The V port refers to the port on the dual mode transducer with an extra shim which would yield the vertical polarization component had the dielectric slab not been introduced into the antenna. Maximum VSWR into the V port with teflon slab inserted is about 1.5; the corresponding number for the H port is about 1.4. With the slab removed from the polarizer, maximum VSWR at both ports increases to about 1.9.

2.5.1.2 Isolation

Port-to-port isolation of 30 dB was desired. Measured isolation with and without the polarizing slab were made and recorded. For the slab inserted cases, isolation at 8.5 GHz is about 16 dB. From about 8.8 GHz to 9.5 GHz isolation is about 25 dB minimum. Without the teflon slab, isolation across the 8.5 to 9.5 GHz range varies from about 35 dB to 50 dB.

2.5.1.3 Beamwidth

The nominal beamwidth is 30° azimuth by 30° elevation at 9.0 GHz.

2.5.1.4 Gain

The desired nominal gain was specified as 13 dB with respect to linear at 9 GHz on boresight. Measured gain data using a linearly polarized transmit signal and with one receive port terminated is 12 dB at 9 GHz.

2.5.1.5 Ellipticity

Desired ellipticity was 3.0 dB maximum across the 3 dB beamwidth at 9.0 GHz. Measured data showed a 1.5 dB ellipticity at 9 GHz.

2.5.2 Wingtip Antennas

Three wingtip antennas were purchased from American Electronic Laboratories (AEL), two of which were left circularly polarized and one of which was right circularly polarized. Any two of these can be flown at one time. The antennas use conventional waveguide twist and phase shifter approach to generate their circular properties. The aperture was covered with a radome which could withstand airspeeds up to 250 mph. A typical AEL H 6000 antenna similar to those used is shown in Figure 21.

The antenna covers the 8.2 - 12.4 GHz frequency range, has a maximum VSWR of 1.5 to 1, gain of 12 dB, 45° beamwidth, and a 3.0 dB maximum axial ratio. The basic measurements of the antenna are 4 1/16 x 2 1/4 inches.

The antenna can handle up to 250 watts average which precludes their being used with the 500 watt CW TWT amplifier.

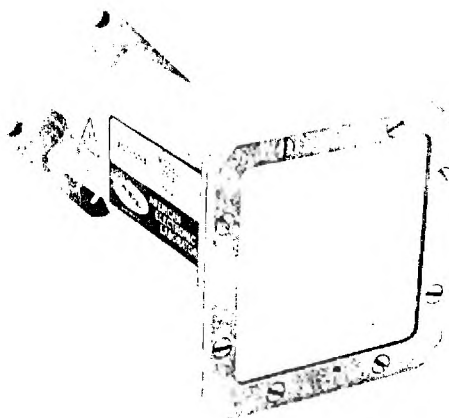


Figure 21. Typical AEL H 6000 Antenna

2.6 Transmitter Subsystem Performance

The transmitter subsystem provides a minimum gain of 100 dB in either the pulse or the CW mode as selected. The gain of the system can be further adjusted to provide further gain with a small sacrifice in power output when the final output stage is allowed to go beyond the top of the saturation curve. This feature is advantageous when the RF input signal is extremely small. The nominal output power of the transmitter subsystem is rated at 2 KW pulse and 500 watts CW. The pin diode modulator allows amplitude modulation signals to a depth of 45 dB below the peak power output of the final stage.

The nominal operating parameters for the transmitter subsystem are displayed in Tables IX and X, and in Figures 22 through 24. Figure 22 and Table IX show a simplified block diagram of the transmitter subsystem and give the various RF power levels present at key points. Figure 23 is a plot of the data on Table IX. Table X shows the power levels at the same key points when the variable attenuators have been adjusted to provide an additional 10 dB of gain through the subsystem. Notice that a net loss of 0.5 dB from the maximum output power results for the larger RF input levels under this condition. The effects of the pin modulator on the RF output power are shown in Figure 24.

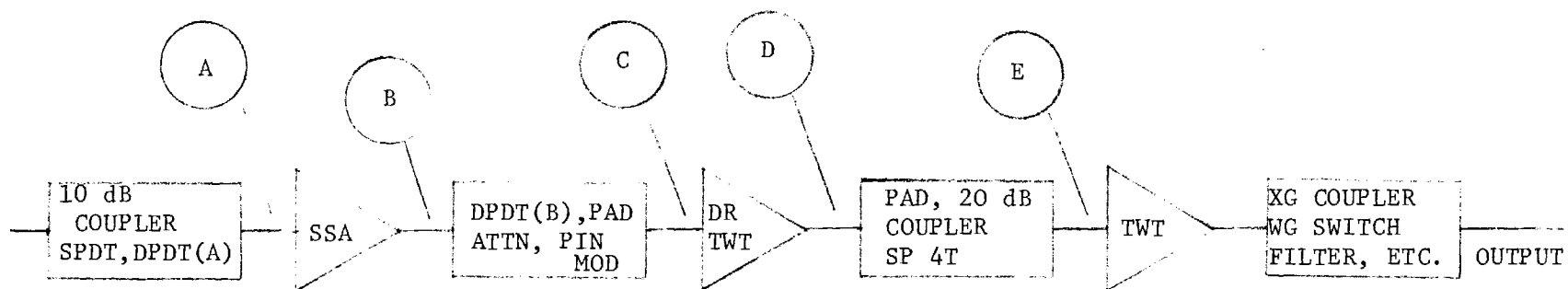


Figure 22. Simplified Block Diagram of Transmitter Subsystem RF Chain

TABLE IX

ADJUSTED RF POWER LEVELS AT KEY POINTS ON TRANSMITTER SUBSYSTEM RF CHAIN (NORMAL)

INPUT (dBm)	A (dBm)	B (dBm)	C (dBm)	D (dBm)	E (dBm)		OUTPUT (dBm)	
					CW	PULSE	CW	PULSE
-100	-104	-58.5	-79.5	-26	-57	-41	- 1	8
- 90	- 94	-48.5	-69.5	-16	-47	-31	9	18
- 80	- 84	-38.5	-59.5	- 6	-37	-21	19	28
- 70	- 74	-28.5	-49.5	4	-27	-11	29	38
- 60	64	-18.5	-39.5	14	-17	- 1	39	48
- 50	- 54	- 8.5	-29.5	24	- 7	9	49	57
- 40	- 44	1.5	-19.5	32	1	17	54.5	61
- 37	- 41	4.5	-16.5	34	3	19	55	61.5
- 33	- 37	8.5	-12.5	36	5	21	56	62
- 30	- 34	11.	-10	37	6	22	56	62
- 27	- 31	12.5	- 8.5	37.5	6.5	22.5	56	62
- 23	- 27	14	- 7	38	7	23	56	62
- 20 through +10	- 24 min	15	- 6	38	7	23	56	62

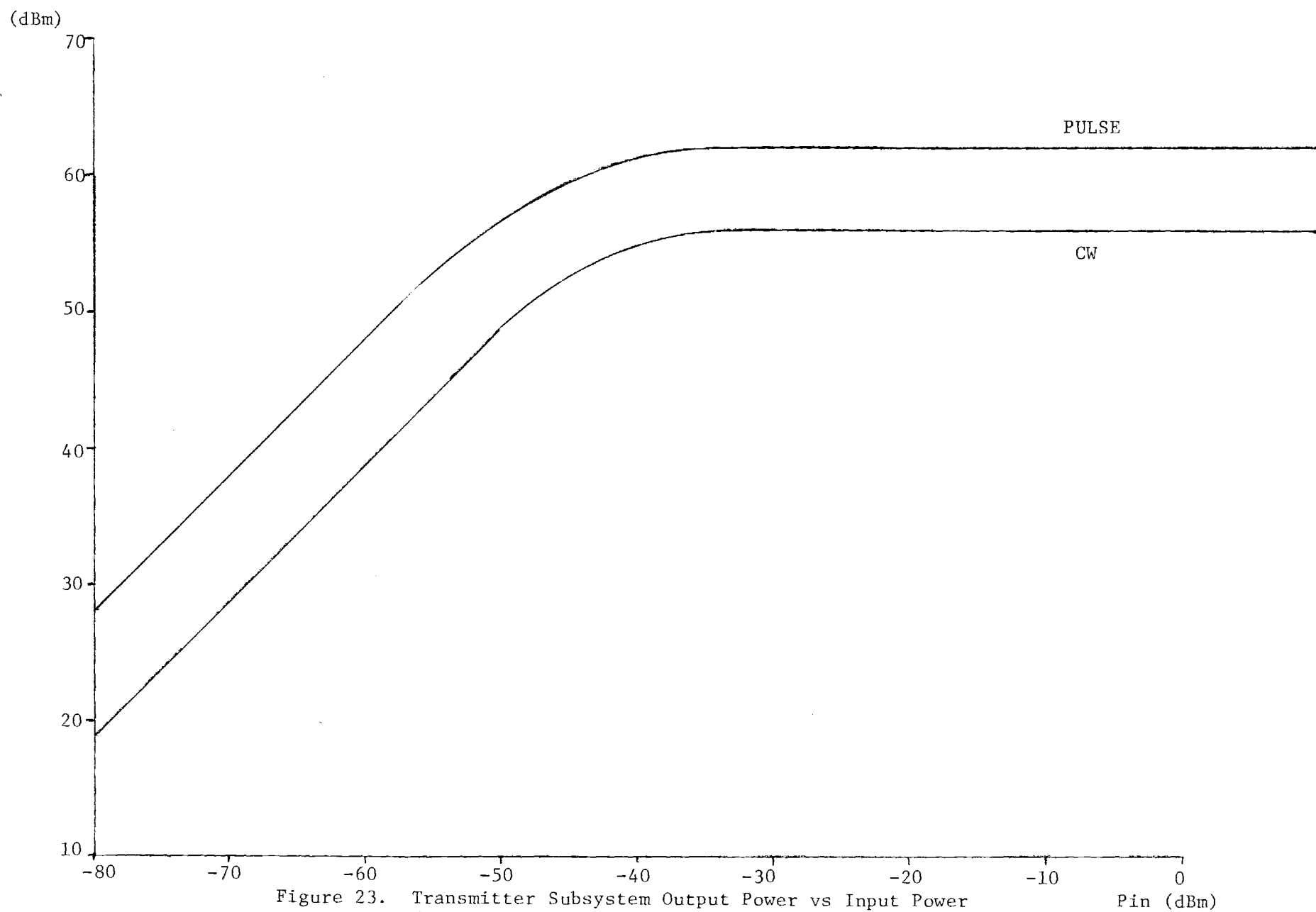


TABLE X

ADJUSTED RF POWER LEVELS AT KEY POINTS ON TRANSMITTER SUBSYSTEM RF CHAIN
(for additional 10 dB small signal gain)

INPUT (dBm)	A (dBm)	B (dBm)	C (dBm)	D (dBm)	E (dBm)		OUTPUT (dBm)	
					CW	PULSE	CW	PULSE
-100	-104	-58.5	-74.5	-21	-47	-31	9	18
- 90	- 94	-48.5	-64.5	-11	-37	-21	19	28
- 80	- 84	-38.5	-54.5	- 1	-27	-11	29	38
- 70	- 74	-28.5	-44.5	9	-17	- 1	39	48
- 60	- 64	-18.5	-34.5	19	- 7	9	49	56
- 50	- 54	- 8.5	-24.5	27	1	17	54.5	61
- 40	- 44	1.5	-14.5	35	9	25	56	62
- 37	- 41	4.5	-11.5	36.5	10.5	26.5	55.5	62
- 33	- 37	8.5	- 7.5	37.5	11.5	27.5	55	61.5
- 30	- 34	11	- 5	38	12	28	55	61.5
- 27	- 31	12.5	- 3.5	38	12	28	55	61.5
- 23	- 27	14	- 2	37.5	11.5	27.5	55	61.5
- 20 through +10	- 24 min	15	- 1	37	11	27	55.5	62

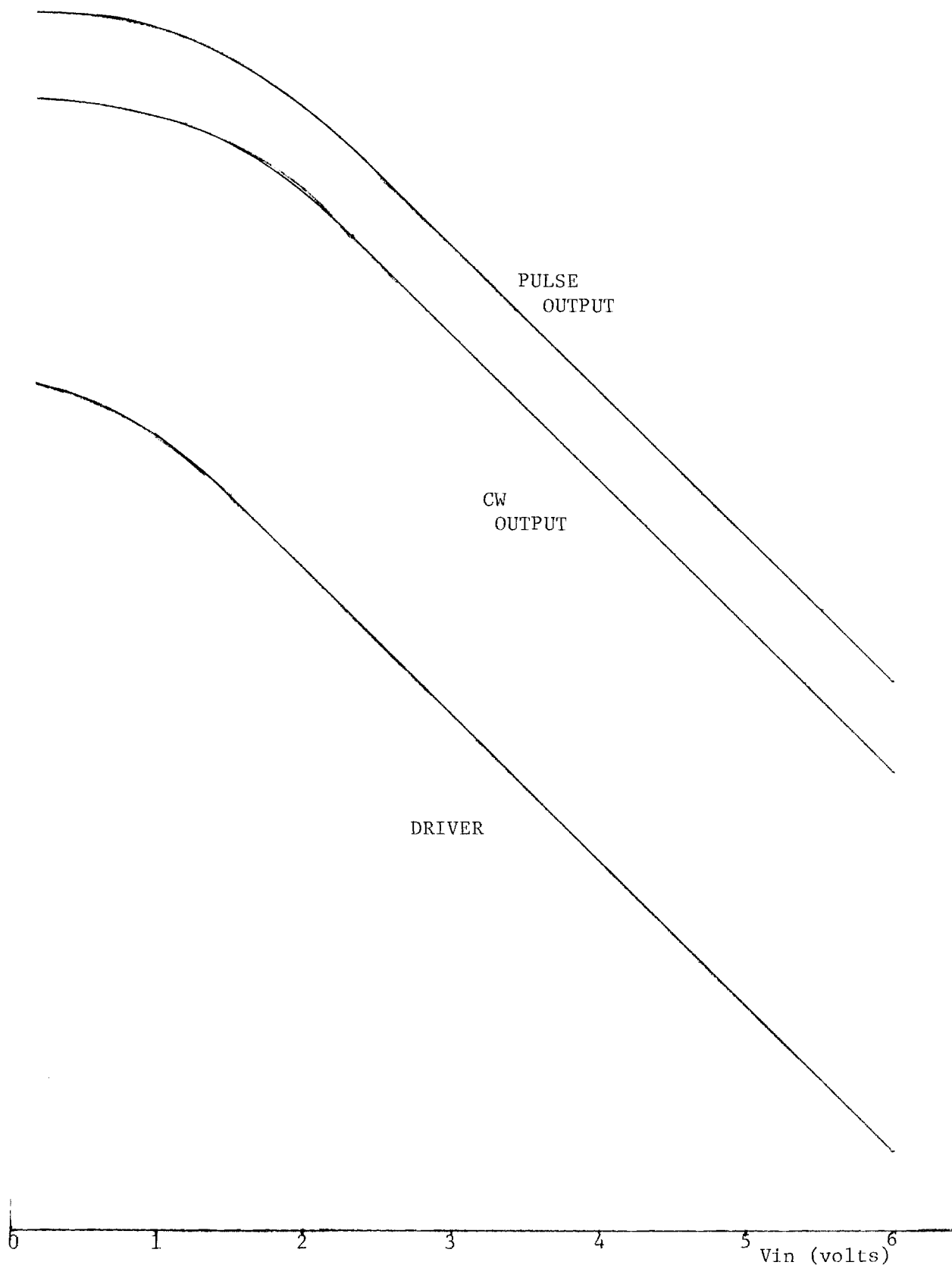


Figure 24. Effects of PIN Modulator on RF Output of the Transmitter Subsystem

3.0 APECM/DCECM TRANSMITTER SUBSYSTEM COMPONENT SPECIFICATIONS

This section contains the specifications for the major components used in the transmitter subsystem as well as an electronics parts list. Additional details about particular components can be obtained directly from the manufacturers. Sections 3.1 through 3.5 are in one-to-one correspondence to Sections 2.1 through 2.5 which detail the five units making up the subsystem.

3.1 Driver Components

The following are the specifications for the major components in the driver assembly. Included are the driver TWT, solid state amplifier (SSA), PIN modulator, RF switches, miscellaneous RF components, DC power supplies and printed circuit boards. A block diagram of the driver unit can be found in Section 2.1.7.

3.1.1 Driver TWT Specifications

The driver TWT and power supply are manufactured by Tele-dyne MEC, Palo Alto, CA. They are TWT type M5918 and power supply type M8172-M. The operating instructions are covered in TMEC document 37344. The specifications and final test data are detailed below.

TABLE XI
DRIVER TWT PERFORMANCE

Frequency	Small Signal Gain $P_{in} = -25$ dB	Output Power	Gain at Saturation	Noise Figure
Minimum	48	33	37	--
Maximum	53	--	--	18
GHz	dB	dBm	dB	dB
8.0	51.2	38.0	44.5	15.6
9.0	51.7	38.1	45.5	16.1
10.0	51.4	37.6	44.9	16.8
11.0	49.8	37.3	43.5	17.3

The power supply is designated to operate from a 115 Vac, 400 Hz source. It must NOT be operated from a 60 Hz source. Make certain that the 400 Hz source is de-energized before hookup. Connect the 400 Hz power to the M8172 primary power connector. This connector (P₁) has the following pin connections:

Pin 5	115 Vac TWT Filament	Pins 1 & 2	Fault Indicator Contacts (normally open)
Pin 7	115 Vac TWT Operation		
Pin 8	115 Vac Neutral (common)	Pins 3 & 4	Fault Indicator Contacts (normally closed)
Pin 12	TLM Common/Helix		
Pin 9	Meter, Helix Current Telemetry		
Pin 10	Meter, Coll. Current Telemetry	Pin 6	Not used
Pin 11	Meter, Helix Voltage Telemetry		

Neutral Pin 8 is the power return line for both STANDBY and ALERT, and need not be grounded. The power supply can be operated from single-phase or 3-phase power. STANDBY and ALERT can be operated from the same phase or different phases, and can be connected line-to-neutral or line-to-line on 3-phase, provided the input voltage (115 V) is correct.

TABLE XII
DRIVER TWT ENVIRONMENTAL CHARACTERISTICS

Temperature	-28° to +65°C (operating) -62° to +75°C (non-operating)
Vibration	per MIL-STD-167B Type 1
Shock	50 G's, 11 mS, 1/2 Sine, 6 Shocks each axis
Humidity	95% minimum @ 60°C (operating and non-operating)
Altitude	10,000 ft

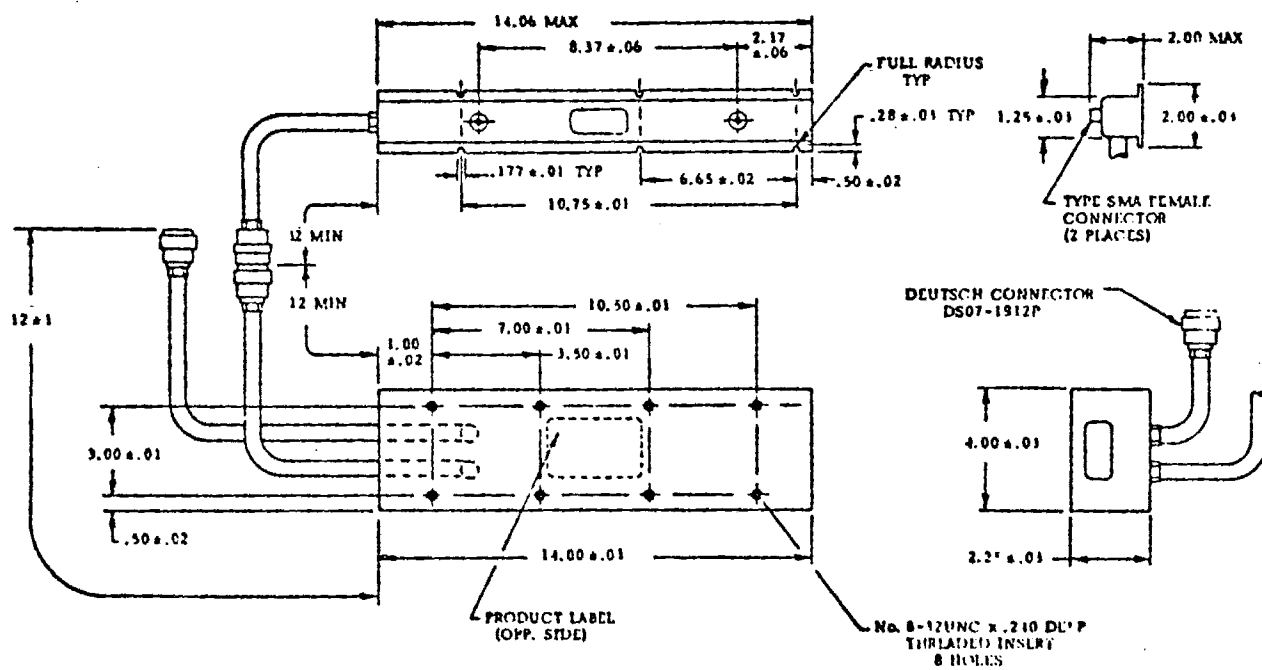


Figure 25. Mechanical Outline of Driver TWT and Power Supply

TABLE XIII
DRIVER TWT MECHANICAL CHARACTERISTICS

	TWT	Power Supply
Weight	60 oz	90 oz max
Length	14.06 in.	14.03 in. max
Height	2.00 in.	2.28 in. max
Width	2.03 in.	4.03 in. max
RF connectors		Type SMA Female
AC connector		DS07-1912P
Cooling		Conduction
Environment		MIL-E-16400 Class 2

3.1.2 Solid State Amplifier Specifications

The solid state amplifier (SSA) is manufactured by Watkins-Johnson, Palo Alto, CA. It is a model 5311-7 low noise, GAS-FET amplifier similar to the standard WJ model 5311-307 GAS-FET amplifier. The specifications and final test data are detailed below.

TABLE XIV
SOLID STATE AMPLIFIER PERFORMANCE

Parameter	Limits	Results							
		Frequency in GHz							
Frequency	8.0 - 11.0 GHz	8.0	8.5	9.0	9.5	10.0	10.5	11.0	
Noise Figure	10 dB max	4.9	5.2	5.0	5.8	6.0	6.0	6.0	
Small Signal Gain	40 dB min	45.4	45.4	45.6	45.8	45.6	45.6	45.7	
VSWR - input	2.0:1 max	Less than 2.0:1							
output	2.0:1 max	Less than 2.0:1							
Power Output	+7 dBm Note 1	+11		+11		+11			+11
Primary Power	+15 VDC			+15 VDC @ 165 mA					
Gain Variation	± 1.0 dB max			± 0.5					
Input Power	+10 dBm max								
Note 1: For 1 dB gain compression									

TABLE XV
SOLID STATE AMPLIFIER ENVIRONMENTAL
AND MECHANICAL CHARACTERISTICS

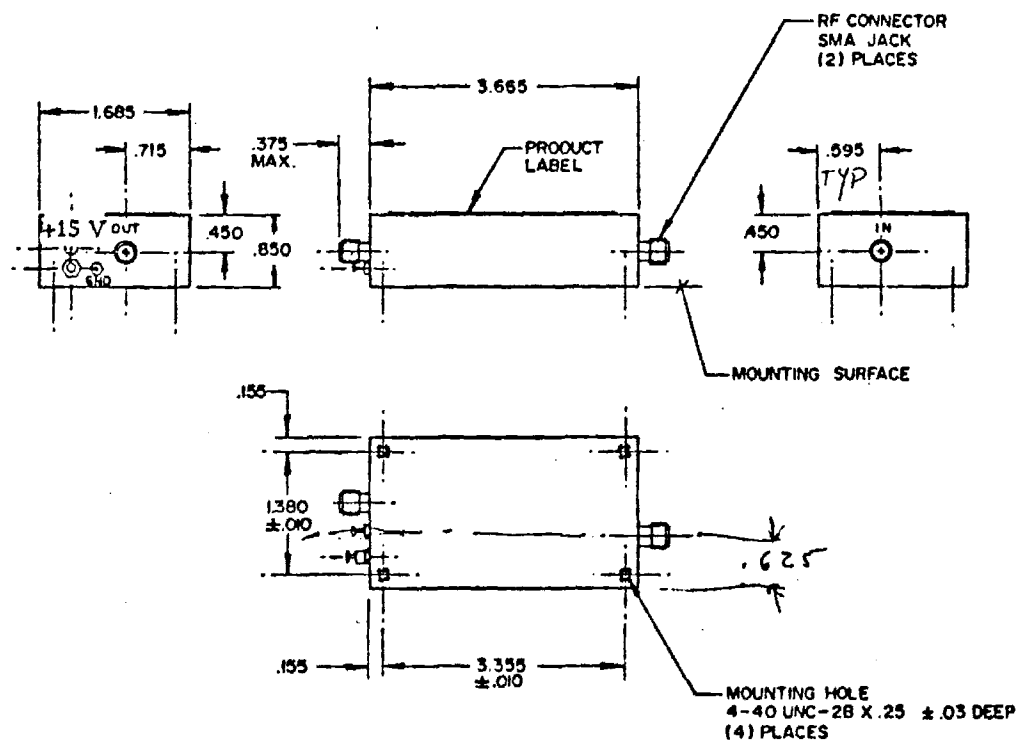
Temperature	-54°C to +61°C (operating)
Environment	MIL-E-5400 Class 2 MIL-E-16400 Class 2
Weight	12 ounces
Length	3.665 inches
Height	0.850 inch
Width	1.685 inches
RF Connectors	Type SMA Female
Cooling	Conduction

3.1.3 PIN Diode Modulator Specifications

The PIN diode modulator is manufactured by General Micro-wave, Farmingdale, N.Y. It is a model D1958 absorptive type with integral driver. The specifications are detailed below.

TABLE XVI
PIN Diode Modulator Performance

RF Frequency	8-18 GHz
Insertion Loss	2.5 dB max
Mid-band Attenuation Range	60 dB min
Switching Speed	\leq 10-15 nanoseconds
Power Handling Capability	100 mW average
Power Overload	1 W average, 70 W peak
Nominal Transfer Function	10 dB per volt
Control Signal Input Voltage Range	0 to +6 V
Control Signal Input Impedance	10 K ohms (nominal)
Power Supply Requirements	+12 V at 100 mA (max) - 12 V at 20 mA (max)
VSWR	1.8:1 max
Deviation from Nominal Attenuation:	
10 dB	\pm 0.9 dB max
20 dB	\pm 1.5 dB max
40 dB	\pm 3.0 dB max
60 dB	\pm 3.5 dB max



NOTES: (UNLESS OTHERWISE SPECIFIED)

- 1- UNIT WEIGHT: 12 OUNCES MAX.
(340.2 GRAMS)
- 2- FINISH: BLUE PER FED-STD-595, COLOR
NO 25109, MOUNTING SURFACE UNPAINTED
- 3- ALL DIMENSIONAL TOLERANCES ± .015

Figure 26. Mechanical Outline of Solid State Amplifier

TABLE XVII
PIN DIODE MODULATOR ENVIRONMENTAL AND MECHANICAL
CHARACTERISTICS

Temperature Range, Operating and Non-operating	-54°C to +110°C
Humidity, Shock, etc.	Per MIL-STD-202C
Weight	1 ounce
Length	1.25 inches
Height	0.50 inch
Width	1.25 inches
RF Connectors	SMA Female
Power Connectors	SMC Female

3.1.4 RF Switches Specifications

There are 2 PIN diode switches in the driver unit; an SPDT switch and an SP4T switch. Both of these diode switches are manufactured by General Microwave, Farmingdale, N.Y. The SPDT is a model F8928 while the SP4T is a model F9140. In addition, a mechanical DPDT manufactured by Transco Products, Venice, CA is also used. The DPDT model number is M1460-22. The specifications are detailed in Table XVIII.

TABLE XVIII
SPDT (F8928) CHARACTERISTICS

RF frequency	8-18 GHz
Insertion loss	2.3 dB max
Isolation	50 dB min
VSWR	2.2:1 max
Switching speed	10 nanoseconds max
Power handling capability (-65°C to +25°C) -- Average power	4 W
Peak power (1 μ sec max pulse width)	70 W
Control input impedance	TTL compatible, two-unit load (A unit load is 1.6 mA sink current and 40 μ A source current.)

TABLE XVIII (continued)

Control levels	-0.3 to +0.7 V (Logic "0") J1 - J2 +2.5 to +5.0 V (Logic "1") J1 - J3
Power supply requirements	+5 V \pm 2%, 125 mA -12 V to - 15 V, 2 mA
Temperature range	Operating: -65°C to +110°C Non-operating: -65°C to +125°C
Humidity, Shock, etc.	Per MIL-STD-202C
Weight	1 ounce
Length	1.10 inches
Height	0.32 inch
Width	0.85 inch
RF connectors	SMA female

TABLE XIX
SP4T (F9140) CHARACTERISTICS

Frequency range	2 to 18 GHz			
	<u>2-4 GHz</u>	<u>4-8 GHz</u>	<u>8-12.4 GHz</u>	<u>12.4-18 GHz</u>
Isolation, min (dB)	60	55	50	50
Insertion loss, max (dB)	1.5	1.5	2.0	2.5
VSWR, max (on position)	1.5	1.75	1.75	2.0
Switching speed, max	500 nanoseconds			
Control input impedance	TTL compatible, two unit load			
Control logic	Logic 0	port on		
	Logic 1	port off		
Power supply requirements	<u>+5 V \pm 2%</u> 150 mA	<u>-12 V to -15 V</u> 50 mA		
Power handling	2 W average, 75 W peak (1 μ sec max pulse width) over temp. range from -65°C to +25°C. Decreases linearly to 40% of rated value at 110°C.			
Temperature range	Operating: -65°C to +110°C Non-operating: -65°C to +125°C			
Humidity, shock, etc.	Per MIL-STD-202C			
Weight	NA			
Length	1.25 inches			

TABLE XIX (continued)

Height	0.63 inch
Width	1.25 inches
RF connectors	SMA female
Control connectors	SMC male

TABLE XX
DPDT (M1460-22) CHARACTERISTICS

Frequency range	1-11 GHz
Isolation	60 dB min
Insertion loss	0.4 dB max
VSWR	1.3:1 max
Power	300 watts C.W. (3000 MC & sea level)
Voltage	500 volts RF (sea level)
Temperature	-54°C to +85°C
Vibration	10 g's to 500 cps
Operating time	Type-E: .3 sec between positions
Life	Type-E: 60,000 op min Type-EM: 200,000 op. min
Weight	Type-E: 2.3 to 3.0 pounds Type-EM: 1.2 to 1.7 pounds
Mil specifications	MIL-E-5272, MIL-1-5422, BuAer 17R23
Weight	NA
Length	3.25 inches
Height	1.81 inches
Width	3.25 inches
RF connectors	N female

3.1.5 Coupler and Attenuator Specifications

TABLE XXI
COUPLER AND ATTENUATOR CHARACTERISTICS

Device	10 dB coupler	20 dB coupler	30 dB pad	30 dB attn
Frequency range	8-12.4 GHz	8-12.4 GHz	8-12.4 GHz	8-12.4 GHz
Manufacturer	ARRA	ARRA	ARRA	ARRA
Model	6164-10	6164-20	6804-30 Form 2191	6804-30 Form P2191
Range	± 1 dB	± 1 dB	0-30 dB	0-30 dB
Power (avg) (peak)	10 W 3 KW	5 W 3 KW	5 W 3 KW	5 W 3 KW
Insertion loss	0.2 dB	0.2 dB	0.5 dB	0.5 dB
VSWR	1.3:1	1.3:1	1.5:1	1.5:1
Directivity	15 dB	15 dB	NA	NA
Length	1.295 inches	1.295 inches	1.75 inches	2.00 inches
Width	1.188 inches	1.188 inches	1.00 inch	1.25 inches
Height	0.50 inch	0.50 inch	0.50 inch	0.50 inch
RF connectors	SMA female	SMA female	SMA female	SMA female

3.1.6 DC Power Supply Specifications

Two DC power supplies are incorporated into the driver unit; a single +5 V DC power supply model LXS-A-5-0V manufactured by Lambda Electronics, Melville, N.Y. and a dual ± 15 V DC power supply model LXD-C-152 also of the same manufacturer. The power supply specifications are listed below.

TABLE XXII
VOLTAGE AND CURRENT RANGES

Models	Voltage Range (Volts)	Maximum Current (amps) at Ambient Temperature			
		40°C	50°C	60°C	71°C
LXS-A-5-0V	5 ± 5%	4.0	3.4	2.7	2.0
LXD-C-152	± 15	2.5	2.3	1.9	1.5

DC Output - Voltage regulated for line and load. Current range must be chosen to suit the appropriate maximum ambient temperature. Current ratings apply for entire voltage range.

Regulated Voltage Output -

Regulation -- 0.1% line or load with input variations from 105-132 or 132-105 volts AC and load variations from no load to full load or full load to no load.

Ripple and Noise -- 1.5 millivolts rms; 5 millivolts peak to peak.

Temperature Coefficient -- Output change in voltage 0.03%/°C.

Overshoot - No overshoot under conditions of power turn-on, turn-off, or power failure.

AC Input - 105-132 VAC at 47-440 Hz. Ratings apply for 57-63 Hz; at 47-53 Hz input, delete 40°C current rating. For 63-440 Hz input, consult factory. The 5 volt unit requires 91 watts input power while the ± 15 volt unit requires 181 watts. With output loaded to full current rating and input voltage 132 volts AC, 60 Hz.

Tracking - Absolute voltage difference between negative and positive outputs within 2%; 0.2% change for all conditions of line, load and temperature for dual output unit.

Overvoltage Protection - Model LXS-A-5-0V includes a fixed built-in overvoltage protection circuit which prevents damage to the load caused by excessive power supply output voltage. Overvoltage protection range varies between 6.4 and 6.8 volts DC.

Overload Protection -

Thermal -- Thermostat, resets automatically when over temperature condition is eliminated.

Electrical -- External-Automatic electronic current limiting circuit, limits output current to a pre-set value less than 125% of 40°C current rating. Automatic current limiting protects the load and power supply when external overloads and direct shorts occur.

Internal-Fuses F1 and F2 provide protection against internal circuit failure.

Input and Output Connections -- Terminal block on rear of chassis.

Operating Ambient Temperature Range and Duty Cycle -- Continuous duty from 0°C to 71°C ambient.

Storage Temperature -- (non-operating) -55°C to 85°C

VDC Adj. Control -- Voltage adjust control permits adjustment of DC output.

Physical Data -

Size -- LXS-A; 3-3/16" x 3-3/4" x 6-1/2"

LXD-C; 3-3/16" x 4-15/16" x 9-3/8"

Weight -- LXS-A; 6 lbs net

LXD-C; 10 lbs. net

Finish -- Gray, FED. STD. 595 No. 26081.

3.1.7 Printed Circuit Boards Parts and Wiring Lists

Figures 27 and 28 show the schematic diagrams for the driver control printed circuit board. The auxiliary receiver printed circuit board circuit diagram is shown on Figure 29. Following these figures is the parts list as well as a wiring list for the two boards.

3.2 Auxiliary Receiver Components

The following are the specifications for the major components in the auxiliary receiver assembly. Included are the balanced mixer, and the 3-port circulator only. Information on the printed circuit board (detector) can be obtained from Section 3.1.7 while information on the logarithmic IF amplifier can be obtained from the Receiver-Transmitter manual for the AN/APX-76. The Federal Stock Numbers (FSN) for the LOG IF and filter which were used are 5895-00-118-2724 and 5915-00-119-1609 CW, respectively.

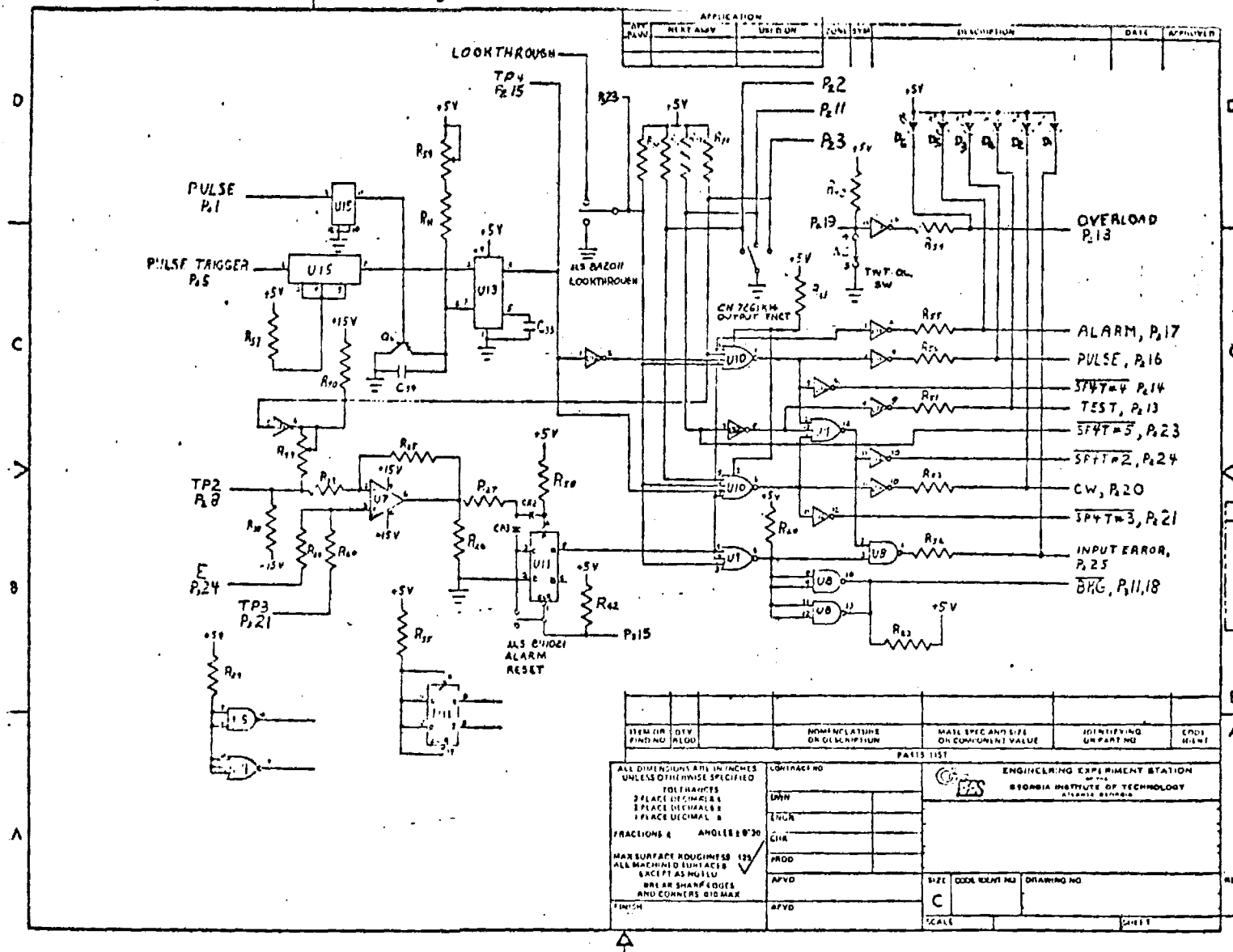


Figure 27. Driver Control Board Schematic (Sheet 1)

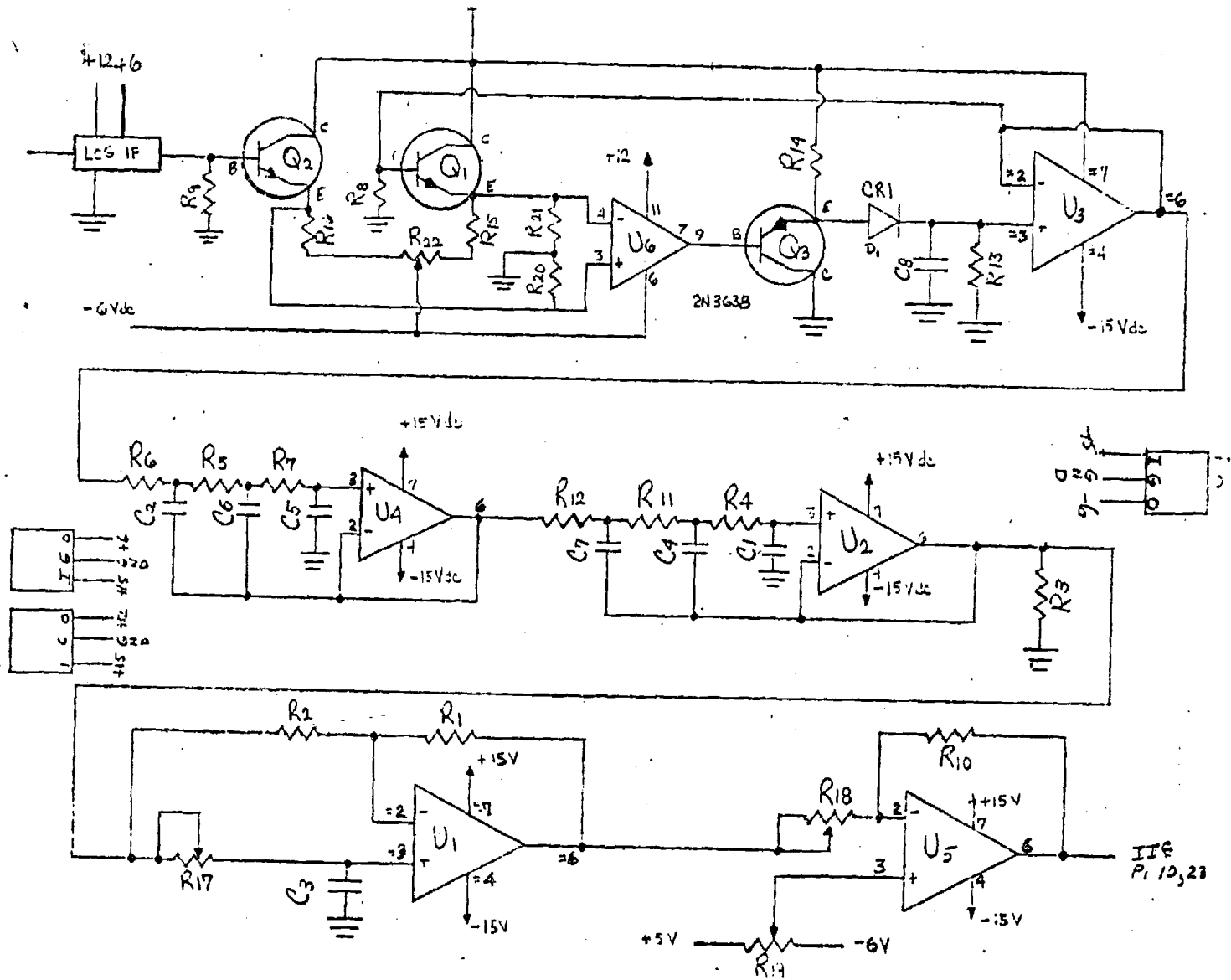


Figure 29. Auxiliary Receiver Schematic

PARTS AND WIRING LIST

Printed Circuit Boards in Driver Drawer

P1 CONNECTOR (AUXILIARY RECEIVER BOARD)

PINS

14	TP5 (GRAY)
12, 13, 25	+15 VDC (RED)
8, 20, 21	GND (BLACK)
3, 15, 16	-15 VDC (YELLOW)
10, 23	TO RPTR/XPNDR/IIG SWITCH PIN 4 (ORANGE)
5, 6, 18	+5 VDC (BLUE)

P2 CONNECTOR (DRIVER CONTROL BOARD)

1	TO TWT PULSE TRIGGER INPUT (TWISTED PAIR)
2	FUNCTION SWITCH (CW) (ORANGE)
3	FUNCTION SWITCH (PULSE) (BROWN)
5	PULSE TRIGGER IN (TWISTED PAIR)
7	TO PIN 6 OF RPTR/XPNDR/IIG SWITCH (BLUE)
8	TP2 (YELLOW)
9, 10, 22	TO MOD INPUT, TP1, & PIN 5 OF RPTR/XPNDR/IIG SWITCH (YELLOW, RED)
11, 23	FUNCTION SWITCH (TEST) & SP4TJ5 (WHITE, 174 FLEX)
12	EXT MOD BNC CONNECTOR (TWISTED PAIR)
13	TEST LED (BLACK)
14	SP4TJ4 (174 FLEX)
15	TP4 (GREEN)
16	PULSE LED (BLACK)
17	ALARM LED (ORANGE)
18	OVERLOAD LED (WHITE)
19	DRIVER TWT PIN 4 (GND PIN 3 OF TWT) (GREEN)
20	CW LED (BLACK)
21	SP4TJ3 (174 FLEX)
24	SP4TJ2 (174 FLEX)
25	TO INPUT ERROR LED (BLACK)

P3 CONNECTOR (DRIVER CONTROL BOARD)

1, 2, 14	+15 VDC (RED)
4, 5, 17	-15 VDC (YELLOW)
7, 19, 20	GND (BLACK)
9, 10, 22	+5 VDC (BLUE)
11	
12, 13, 25	GND (BLACK)
15	TO MOM ACTION SWITCH CENTER PIN (ORANGE)
18	TO CW TWT BLANKING, MULTIPIN CONN PIN 1 (TWISTED PAIR)
21	TP3 (BROWN)
23	LOOKTHROUGH SWITCH CENTER PIN (TWISTED PAIR)
24	TO POWER MONITOR MULTIPIN CONN PIN 4 (ORANGE)

$R_1 = 10K, 5\%$
 $R_2 = 10K, 5\%$
 $R_3 = 5.6K, 5\%$
 $R_4 = 150K, 5\%$
 $R_5 = 150K, 5\%$
 $R_6 = 150K, 5\%$
 $R_7 = 150K, 5\%$
 $R_8 = 1.5K, 5\%$
 $R_9 = 330\Omega, 5\%$
 $R_{10} = 10K, 5\%$
 $R_{11} = 150K, 5\%$
 $R_{12} = 150K, 5\%$
 $R_{13} = 22M, 5\%$
 $R_{14} = 4.7K, 5\%$
 $R_{15} = 20K, 5\%$
 $R_{16} = 20K, 5\%$
 $R_{17} = 1M, VAR$
 $R_{18} = 25K, VAR$
 $R_{19} = 20K, VAR$
 $R_{20} = 5K, 1\%$
 $R_{21} = 4.7K, 1\%$
 $R_{22} = 25K, VAR$
 $R_{23} = NOT\ USED$
 $R_{24} = 10K, 1\%$
 $R_{25} = 1M, 5\%$
 $R_{26} = 5.6K, 5\%$
 $R_{27} = 2.2K, 5\%$
 $R_{28} = 5.6K, 5\%$

$R_{29} = 5.6K, 5\%$
 $R_{30} = 5.6K, 5\%$
 $R_{31} = 5.6K, 5\%$
 $R_{32} = 5.6K, 5\%$
 $R_{33} = 5.6K, 5\%$
 $R_{34} = 5.6K, 5\%$
 $R_{35} = 10K, 5\%$
 $R_{36} = 4.7K, 5\%$
 $R_{37} = 4.7K, 5\%$
 $R_{38} = 1.6K, 1\%$
 $R_{39} = 10K, 1\%$
 $R_{40} = 5.6K, 5\%$
 $R_{41} = 1K, 5\%$
 $R_{42} = 5.6K, 5\%$
 $R_{43} = 2.2K, 5\%$
 $R_{44} = 1K, VAR$
 $R_{45} = 2.2K, 5\%$
 $R_{46} = 470\Omega, 5\%$
 $R_{47} = 5K, VAR$
 $R_{48} = 2.2K, 5\%$
 $R_{49} = 1K, VAR$
 $R_{50} = 1K, 1\%$
 $R_{51} = 270\Omega, 5\%$
 $R_{52} = 270\Omega, 5\%$
 $R_{53} = 270\Omega, 5\%$
 $R_{54} = 270\Omega, 5\%$
 $R_{55} = 270\Omega, 5\%$
 $R_{56} = 270\Omega, 5\%$

$R_{57} = 10K, 5\%$
 $R_{58} = 2.2K, 5\%$
 $R_{59} = 50K, VAR$
 $R_{60} = 10K, 1\%$
 $C_1 = .0015\ \mu f$
 $C_2 = .01\ \mu f$
 $C_3 = .01\ \mu f$
 $C_4 = .01\ \mu f$
 $C_5 = .005\ \mu f$
 $C_6 = .01\ \mu f$
 $C_7 = .01\ \mu f$
 $C_8 = 500\ pf$
 $C_9 = .1\ \mu f\ (FC)$
 $C_{10} = .1\ \mu f\ (FC)$
 $C_{11} = .1\ \mu f\ (FC)$
 $C_{12} = .1\ \mu f\ (FC)$
 $C_{13} = .1\ \mu f\ (FC)$
 $C_{14} = .1\ \mu f\ (FC)$
 $C_{15} = .1\ \mu f\ (FC)$
 $C_{16} = .1\ \mu f\ (FC)$
 $C_{17} = .1\ \mu f\ (FC)$
 $C_{18} = .1\ \mu f\ (FC)$
 $C_{19} = .1\ \mu f\ (FC)$
 $C_{20} = .1\ \mu f\ (FC)$
 $C_{21} = .1\ \mu f\ (FC)$
 $C_{22} = .1\ \mu f\ (FC)$
 $C_{23} = .1\ \mu f\ (FC)$
 $C_{24} = .1\ \mu f\ (FC)$

$C_{25} = .1 \mu f \text{ (FC)}$	$U_{11} = N7474$
$C_{26} = .1 \mu f \text{ (FC)}$	$U_{12} = N7404$
$C_{27} = .1 \mu f \text{ (FC)}$	$U_{13} = NE555$
$C_{28} = .1 \mu f \text{ (FC)}$	$U_{14} = N7406$
$C_{29} = .1 \mu f \text{ (FC)}$	$U_{15} = 54122$
$C_{30} = .1 \mu f \text{ (FC)}$	$CR_1 = 5082-2800$
$C_{31} = .1 \mu f \text{ (FC)}$	$CR_2 = IN270$
$C_{32} = .1 \mu f \text{ (FC)}$	$CR_3 = IN270$
$C_{33} = .01 \mu f$	$CR_4 = IN270$
$C_{34} = .1 \mu f$	$CR_5 = IN270$
$Q_1 = 2N3563$	$CR_6 = IN270$
$Q_2 = 2N3563$	$LED's = 5082-4655$
$Q_3 = 2N3638$	
$Q_4 = 2N2222A$	$TP_1 = \text{MODULATOR INPUT}$
$Q_5 = 2N2222A$	$TP_2 = \text{VSWR LEVEL SET}$
$Q_6 = 2N2907$	$TP_3 = \text{VSWR LEVEL TEST}$
$Q_7 = 2N2222A$	$TP_4 = \text{MISSING PULSE DETECTOR OUTPUT}$
$U_1 = CA3140$	$TP_5 = \text{LOG IF OUTPUT}$
$U_2 = CA3140$	$TP_6 = N.C.$
$U_3 = CA3140$	$TP_7 = N.C.$
$U_4 = CA3140$	$TP_8 = N.C.$
$U_5 = CA3140$	
$U_6 = \mu A710C$	
$U_7 = CA3140$	
$U_8 = N7401$	
$U_9 = N7427$	
$U_{10} = N7425$	

3.2.1 Balanced Mixer Specifications

The balanced mixer utilized in the auxiliary receiver unit is a model 7F0128 manufactured by Anaren, Syracuse, N.Y. The specifications are detailed below.

TABLE XXIII

BALANCED MIXER CHARACTERISTICS

Frequency Range	7.0 - 11.0 GHz
Isolation LO/RF	18 dB min
VSWR	1.8:1 max
Conversion Loss	8.5 dB max
Noise Figure	9.5 dB max
IF Bandwidth	DC - 400 MHz (60 MHz BW used)
LO Drive	7 mw typ
RF Connectors	SMA Female
Weight	3.5 ounces
Length	2.35 inches
Width	2.35 inches
Height	0.37 inch

3.2.2 Circulator Specifications

The 3-port circulator utilized in the auxiliary receiver is a model 3JC-7011 manufactured by Western Microwave, Sunnyvale, CA. The specifications are detailed in Table XXIV.

3.3 CW TWT Amplifier Components

The following are the specifications for the major components in the CW/TWT unit. They include the TWT and power supply as well as associated safety circuits, indicators, and other peripherals. A block diagram of the CW TWT assembly can be found in Section 2.3.1.

TABLE XXIV
CIRCULATOR CHARACTERISTICS

Frequency Range	7.0 - 11.0 GHz
Isolation	20 dB min
Insertion Loss	0.4 dB min
VSWR	1.2:1 max
Power: (avg)	50 w max
(peak)	500 w max
Temperature	-54°C to +85°C
RF Connectors	SMA Female
Length	1.13 inches
Width	1.13 inches
Height	0.75 inch

3.3.1 CW TWT Amplifier Specifications

The CW TWT amplifier and power supply are Teledyne Model No. MTI-5008 and MQI-1013, respectively. The specifications and final test data are contained below in Table XXV.

TABLE XXV
CW TWT SPECIFICATIONS

<u>Parameter</u>	<u>Specification</u>	<u>Final Test Data</u>		
Power Output				
Frequency	/	Sat PO 56 dBm (min)	Gain @ Sat 40 dB (min)	Gain @ 56 dBm
8.0 GHz		56.6 dBm	48.1 dB	52.6 dB
8.5		57.1	50.0	55.5
9.0		57.2	50.2	54.6
9.5		57.4	49.6	54.0
10.0		57.2	50.0	53.6
10.5		57.5	47.8	53.0
11.0		56.9	46.5	50.5
Noise Power	-25 (min)			-29 dBm/MHz unblanked
	-85 (min)			-98 dBm/MHz blanked

<u>Parameter</u>	<u>Specification</u>	<u>Final Test Data</u>		
Rise time to blank	150 (max)		8 μ sec	
Fall time to unblank	65 (max)		45 μ sec	
Delay time to blank	50 (max)		2 μ sec	
Delay time to unblank	120 (max)		120 μ sec	
Min pulse width blanked	500 (min)		1.8 μ sec RF off @ -99 dBm/MHz, 60 μ sec 10-90%	

<u>TWT Operating Parameters</u>	<u>Min</u>	<u>Nominal</u>	<u>Max</u>	<u>Units</u>
Helix Voltage		Ground		
Helix Current	0		25	mA
Helix Surge Current	0	100	200	mA
Cathode Voltage	9600	9800	10,100	VDC
Cathode Current			450	mA
Collector Voltage #1	5400	5940	6,540	VDC
Collector Voltage #2	3900	4290	4,720	VDC
Collector Current #1			200	mA
Collector Current #2			450	mA
Anode Voltage	180	200	220	Volts
Anode Current			2	mA
Focus Electrode Voltage				
Beam On	-3		-15	Volts
Beam Off	1000		1,250	Volts
Focus Electrode Current			100	μ A
Heater Voltage	6.2	6.3	6.4	Volts
Heater Current		1.8	2.5	Amps
Heater Warm-up Time	180	200		Sec
Prime Power (excluding filament power)				
AC Voltage	115/200 V, RMS \pm 10%, 3 phase, 380-420 Hz @ 2.8 KVA			
DC Voltage	+28 V DC @ 100 mA			
Input Signals	<u>Level</u>			
Blank Command	TTL Low			
HV ON Command	TTL High			
Output Signals				
HV ON Indicate	Drives LED (+5V)			
Ready Indicate	Drives LED (+5V)			
Helix Overload Indicate	Drives LED (+5V)			

Temp Overload Indicate (TWT or PS)	
High VSWR	Drives LED (+5V)
Outline Dimensions	14" x 7.5" x 5.75"
Weight	35 lbs max
Cooling -- The power supply shall be conduction cooled and shall meet all requirements of paragraphs 3 and 5 while being mounted to a baseplate at 75°C max.	
Connectors	
Prime Power	MS 3102R20-17P
Control/Monitor	MS 3112E14-19S
High Voltage	LGH-1/2 or equivalent
TWT Low Voltage	DEM-95
Environment -- In general supply must be designed to be installed in an airborne environment.	
Altitude	10,000 ft
Temperature (Operate)	0°C to 50°C
Temperature (Storage)	-25°C to 70°C

TABLE XXVI
CW TWT CONNECTIONS

J1-Control/Monitor

MS3112E14-19S

A	Blank Command
B	Blank Command Return
C	N.C.
D	H.V. On Indicator
E	Ready Indicator
F	RF O.L. Indicator
G	Helix O.L. Indicator
H	Temp O.L. Indicator
J	RF Arc (VSWR)
K	N.C.
L	VSWR
M	Ground
N	N.C.
P	N.C.
R	N.C.
S	N.C.
T	N.C.
U	N.C.
V	H.V. On (+28 VDC)

J7-Prime Power

MS3102A20-17P

A	115/200V-30
B	380-420 Hz
C	
D	N.C.
E	Ground
F	+28 VDC

J2-TWT Low Voltage

DEM-9S (ITT-Cannon)

1	+200 V Anode
2	N.C.
3	TWT Thermo
4	N.C.
5	N.C.
6	N.C.
7	N.C.
8	N.C.
9	Ground

J3	Collector 1	
J4	Cathode	
J5	Focus Electrode	TWT High Voltage
J6	Heater	Amp 834333-2
J8	Collector 2	

3.3.2 CW TWT Amplifier Amplifier Safety Circuits and Peripheral Equipment Specifications

When prime power is applied, the power supply enters the power on state. In this condition, power will be supplied to the filament of the TWT. The collector voltages shall not be energized in this state. After 180 ± 10 seconds of the power on state, the power supply will enter the READY state. A ready indicate drive for an LED is now generated. The TWT HV can now be applied.

Upon receipt of +28V "HV ON" command, the power supply cathode and collector voltages are energized. In addition, an HV ON indicator signal is generated. The power supply has a "soft turn-on capability," i.e., after receipt of the HV ON command and before the cathode and collector voltages have stabilized, the focus electrode voltage is in the biased off state. Once stabilization has occurred, and if the unit is not blanked, the focus electrode voltage goes to the on state.

If the power supply automatically shuts off for other than a thermal failure, the power supply remains off until fault reset is accomplished by removing and reapplying the HV ON command. The power supply contains fault protection circuitry to automatically turn off the TWT high voltage if there is

- excessive helix current,
- TWT over temperature,
- power supply over temperature and TWT thermal faults are self-resetting.

Two RF power monitors from General Microwave Corp., Farmingdale, N.Y., are utilized in the CW TWT Drawer. One is used to measure output power (N427a) while the other is used to measure reflected power (N426A). Although both have three full range scales, the N426A is permanently set on the middle scale since its output is used in the VSWR protection circuit. The outputs of both power monitors are monitored via voltage meters on the CW TWT Drawer front panel. The inputs to the monitor are provided from a cross guide coupler (Waveline 669-40). The RF from the CW TWT (or the Pulse TWT) is selected for transmission by a waveguide switch (Waveline 682) and further filtered by a dissipative Harmonic RF filter (MRC X72L type). Below in Tables XXVII and XXVIII are the specifications for the above components.

TABLE XXVII
RF POWER MONITOR SPECIFICATIONS

Model	N426A		N427A	
Frequency Range	0.01 to 12.4 GHz			
Full Scale Ranges	<u>dBm</u>	<u>mW</u>	<u>dBm</u>	<u>mW</u>
Range 1	+20	100	0	1
Range 2	+10	10	-10	0.1
Range 3	0	1	-20	0.01
Input Impedance	50 ohms			
Max VSWR	1.5			
Accuracy	±1% of full scale			
Operating Temperature Range	-55°C to +85°C			
Zero Drift	0.02% F.S./°C		0.035% F.S./°C	
Noise	0.02% F.S. (p-p)		0.035% F.S. (p-p)	
tft Element Temperature Sensitivity	0.1%°C			
Input Overload	300%			
Maximum DC Voltage	30 V		3 V	
Output				
Current Mode	1 mA full scale, each range			
Voltage Mode	-10 volts full scale (max), each range			
Pulse Energy				
Max Pulse Energy (w-μsec)	150		1.5	
Max Pulse Power ⁵ (w)	30		0.3	
Max Pulse Duration (μsec)	5		5	
Power Supply Requirements	±6 V to ±18 V, 10 mA, 0.1% regulation			
Size and Weight	3.06" L. x 2.00" D., 8 ounces (76,2 mm x 50,8 mm, 227 gm)			

TABLE XXVIII

CW TWT DRAWER PERIPHERAL EQUIPMENT SPECIFICATIONS

Device	40 dB WG coupler	20 dB coupler	RF filter	30 dB attn
Frequency Range	8.2-12.4 GHz	8012.4 GHz	8-11 GHz	8-12.4 GHz
Manufacturer	Waveline	ARRA	MRC	ARRA
Model	669-40	6164-20	X72L	6804-30 FORM P2191
Range	+1.5 dB	± 1 dB	20 dB	0-30 dB
Power (avg)	--	5 W	500 W	5 W
(peak)	--	3 KW	5 KW	3 KW
Insertion Loss	0.1 dB	0.2 dB	0.3 dB	0.5 dB
VSWR	1.1:1	1.3:1	1.15:1	1.5:1
Directivity	20 dB	15 dB	NA	NA
Length	3.0 inches	1.295 inches	9.00 in.	2.00 in.
Width	3.0 inches	1.188 inches	4.00 in.	1.25 in.
Height	1.25 inches	0.50 inch	4.00 in.	0.50 inch
RF Connectors	WR-90	SMA Fem	WR-90	SMA Fem

3.4 Pulse TWT Amplifier Specifications

The Pulse TWT and associated power supply are manufactured by the Electron Tube Division of Litton Industries, San Carlos, CA. The power supply employed is a model 624 unit while the TWT itself has varied including both L5655-52 and L5459-53 model TWT's. Both types cover the specified 8-11 GHz region; however, due to the unavailability of an additional L5655-52 in a timely manner during the performance of flight tests, the L5459-53 types were obtained and utilized. Three specifications are therefore given below; one for the 624 power supply itself and one for each TWT utilized. Georgia Tech would like to express its appreciation to Litton Industries for their versatility and quick reaction in helping us find a most suitable solution to problems which were encountered during the tests.

In addition the model 624 power supply is incorporated with standard safety circuitry including duty cycle limiter (2%), pulse length limit (10 μ sec), overtemperature protection, TWT average overcurrent protection, and a collector current monitoring BNC connector. The chassis dimensions are 16.9" x 18" x 6.7" while the front panel is 19" x 7". Additional information regarding the Litton model 624 TWT power supply can be found in the manufacturer's publication no. 157377.

The TWT type L5655-52 was the first pulse TWT utilized in the transmitter subsystem. Although it saw little utilization during flight tests, it is the recommended tube type due to its inherent high output power (greater than 63 dBm) across the 8-11 GHz band. The L5459-53 TWT was used during the majority of the flight tests although only as a substitute. The specifications for both are contained in Table XXX. The output vs frequency characteristics of the particular TWT amplifiers used are shown in Figures 30 and 31.

3.5 Auxiliary Antenna Specifications

The auxiliary antenna was manufactured at Georgia Tech for an internally funded project and was designed to cover a frequency range from 8.5 GHz to 9.5 GHz. Under the current contract it was modified to increase the beamwidth and to convert it from a dual linearly polarized horn to a dual circularly polarized one. In an emergency situation it could be used

TABLE XXIX
LITTON MODEL 624 POWER SUPPLY SPECIFICATIONS

Parameter	Min	Max	Typ.	Units
Line Voltage	103	132	115	Volts
Line Current				
Standby			1.2	Amps
Operate @ 1% Duty			4.5	Amps
Heater Voltage (E_f) (must be adjusted to 6.3 V for proper TWT operation)			6.3	Volts DC
Heater Current (I_f)		2.5	2.0	Amps
Cathode Voltage (E_k)*	9	11	10.5	KV DC
Cathode Voltage Ripple	1	5	2	Volts
Cathode Current (I_k)*	0	34	18	mA average
Cathode Current (i_k)*			1.8	Amps peak
Grid Bias (E_c) (referenced to cathode)*	-90		-128	Volts DC
Grid Current (I_c)*		.4	.25	Amps peak
Grid Modulator*				
Pulse width (t_p)	0.1	35		μsec
Pulse amplitude (e_c) (referenced to cathode)	+70	170		Volts peak
Filament time delay	2	4	3	Min
Temperature				
Operating	-10		60	°C
Non-operating	-55		85	°C

*These voltages are adjusted for each individual TWT. The values shown are typical for an X-band unit. The frequency band required determines the range and adjustment required.

TABLE XXX

LITTON MODEL 624 POWER SUPPLY TYPICAL CHARACTERISTICS

	Typ.	Units
Power Factor	.75	
Heater Voltage Ripple	20	mV peak to peak
Grid Bias Ripple	50	mV peak to peak
Grid Modulator		
Pulse rise time	75	nsec
Pulse fall time	160	nsec
Recovery time		
10 μ sec pulse	20	μ sec
1.0 μ sec pulse	2.5	μ sec
Overshoot	5	Volts
Droop	0.1	V/ μ sec
Jitter	5	nsec
Propagation delay	170	nsec
Turn-on delay (after operate command is given)	3	sec
Trigger amplitude	10 \pm 5	Volts
Trigger rise time (max)	100	nsec
Cathode Voltage (Droop ($i_k = 1.7$ amp peak))	6	V/ μ sec

TABLE XXXI
PULSE TWT AMPLIFIER SPECIFICATIONS

Parameter	L5655-52	L5459-53	Units
Heater Voltage E_f	- 6.3	- 6.3	Volts
Grid Bias E_c	- 90	-100	Volts
Grid Pulse e_c	+171	+130	Volts
Cathode Voltage E_w^*	- 10.30	- 11.00	kilovolts
Collector Voltage E_b	GND	GND	Volts
Heater Current I_f	1.75	1.55	Amps
Cathode Current i_k	1.88	1.65	Amps
Grid Current i_c	.280	N.A.	Amps
Body Current i_w	.50	.239	Amps
Collector Current i_b (w/o RF)	1.10	1.41	Amps
Frequency Range	8-11	8-11	GHz
Gain (min)	40	50	dB
Power Output	63	62	dBm
Duty Cycle (max)	2	2	%
Pulse Length (max)	10	10	μsec

* Cathode voltage with respect to ground, all other voltages with respect to cathode.

SATURATION POWER OUTPUT VS. FREQUENCY

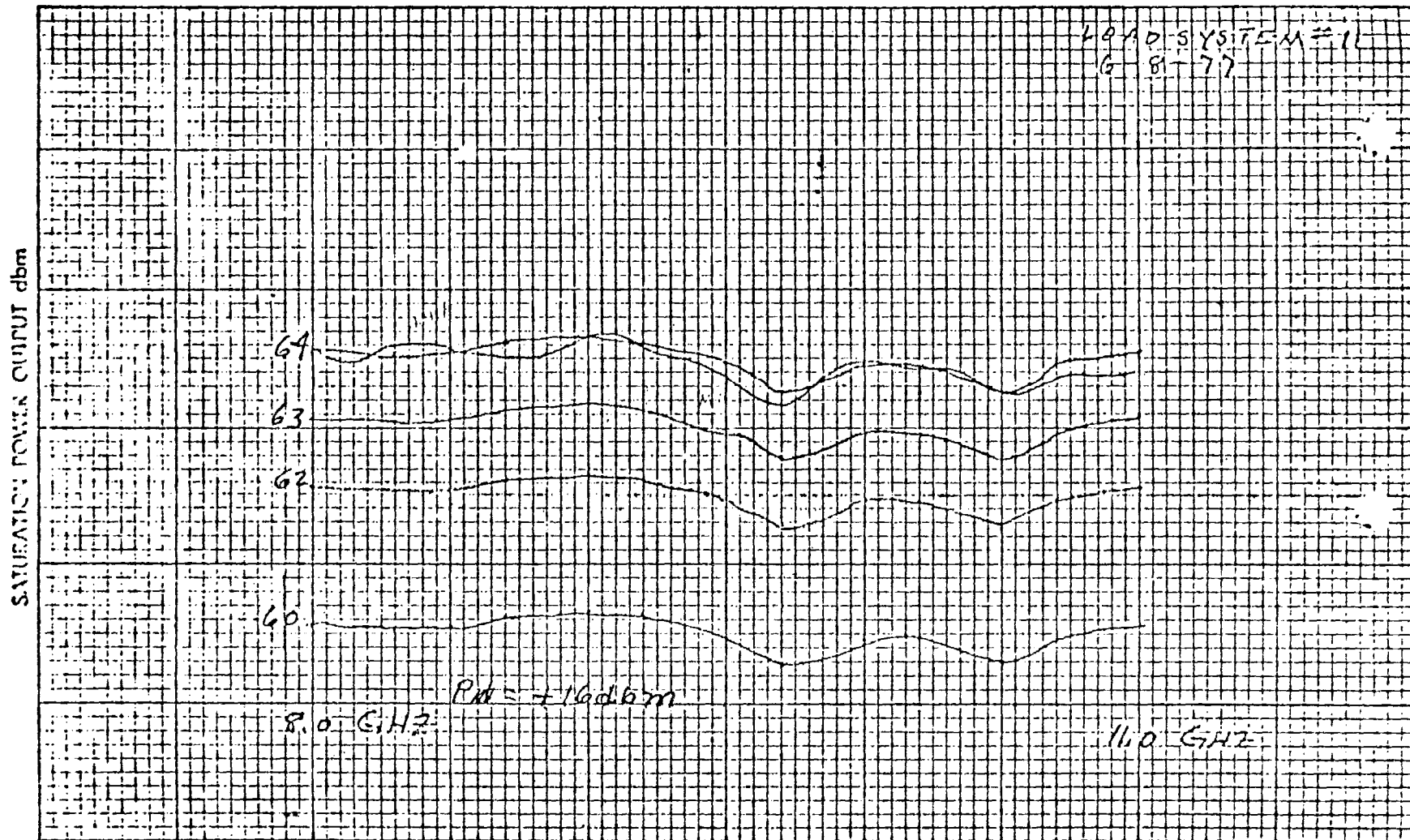
TUBE TYPE 6-10-77SERIAL NO. 2012DATE 6-10-77

Figure 30. L5655-52 TWT Output vs Frequency

SATURATION POWER OUTPUT VS. FREQUENCY

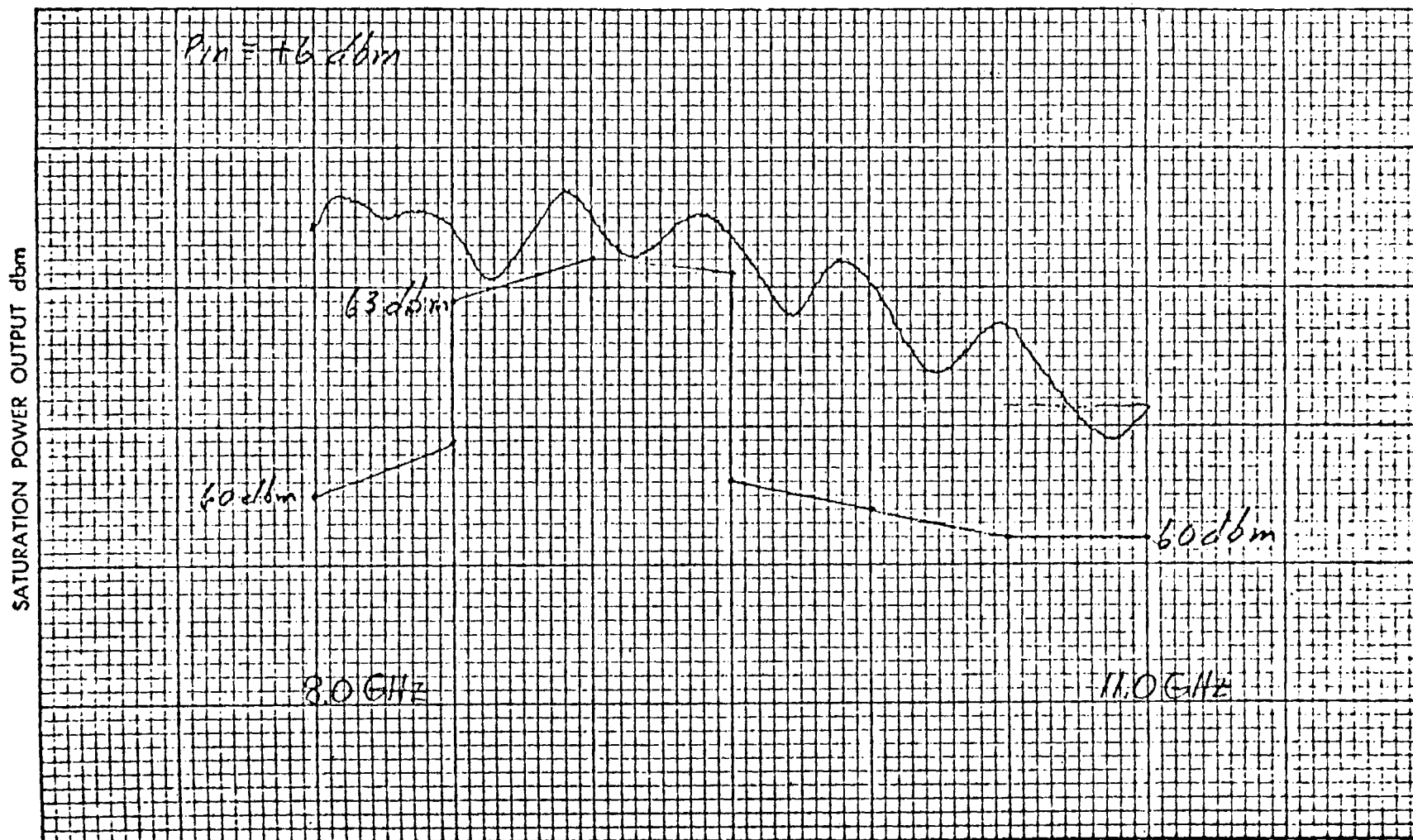
TUBE TYPE L-5459-53SERIAL NO. 2054DATE 5-22-79

Figure 31. L5459-53-TWT Output vs Frequency

to substitute for the main polarization antenna described in Volume 1 of this manual. Table XXXII and Figures 32 - 42 show the measured parameters of the auxiliary antenna under laboratory test conditions.

TABLE XXXII
MEASURED RELATIVE PHASES FOR LINEAR POLARIZATION
TRANSMISSIONS (AUXILIARY ANTENNA)

Frequency	Transmitted Polarization	Relative Phase, Port V to Port H
8.5 GHz	V	-100°
8.5 GHz	H	+ 77°
9.0 GHz	V	- 47°
9.0 GHz	H	+134°
9.5 GHz	V	- 50°
9.5 GHz	H	+130°

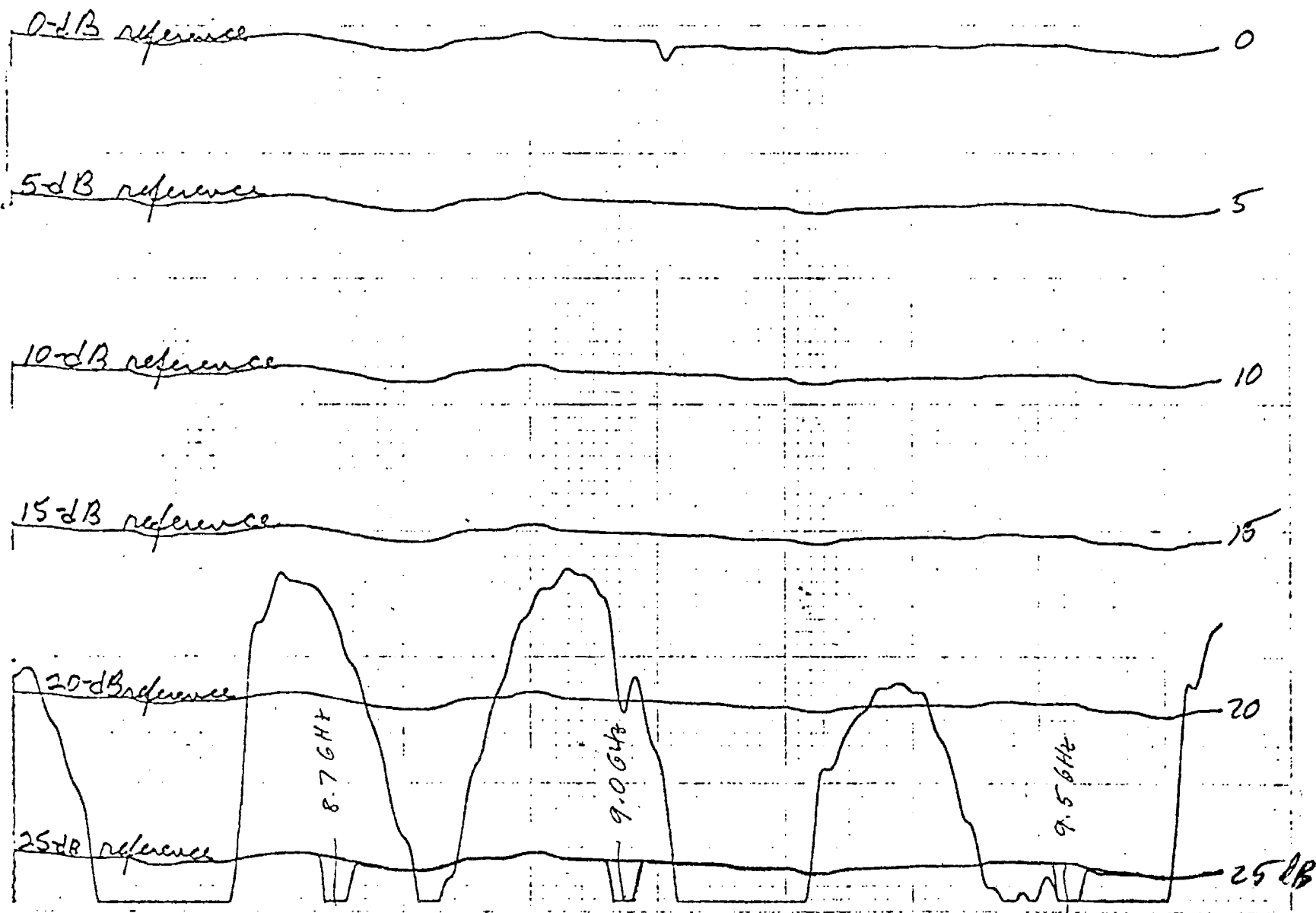


Figure 32. Return Loss vs Frequency into Auxiliary Antenna H-Port

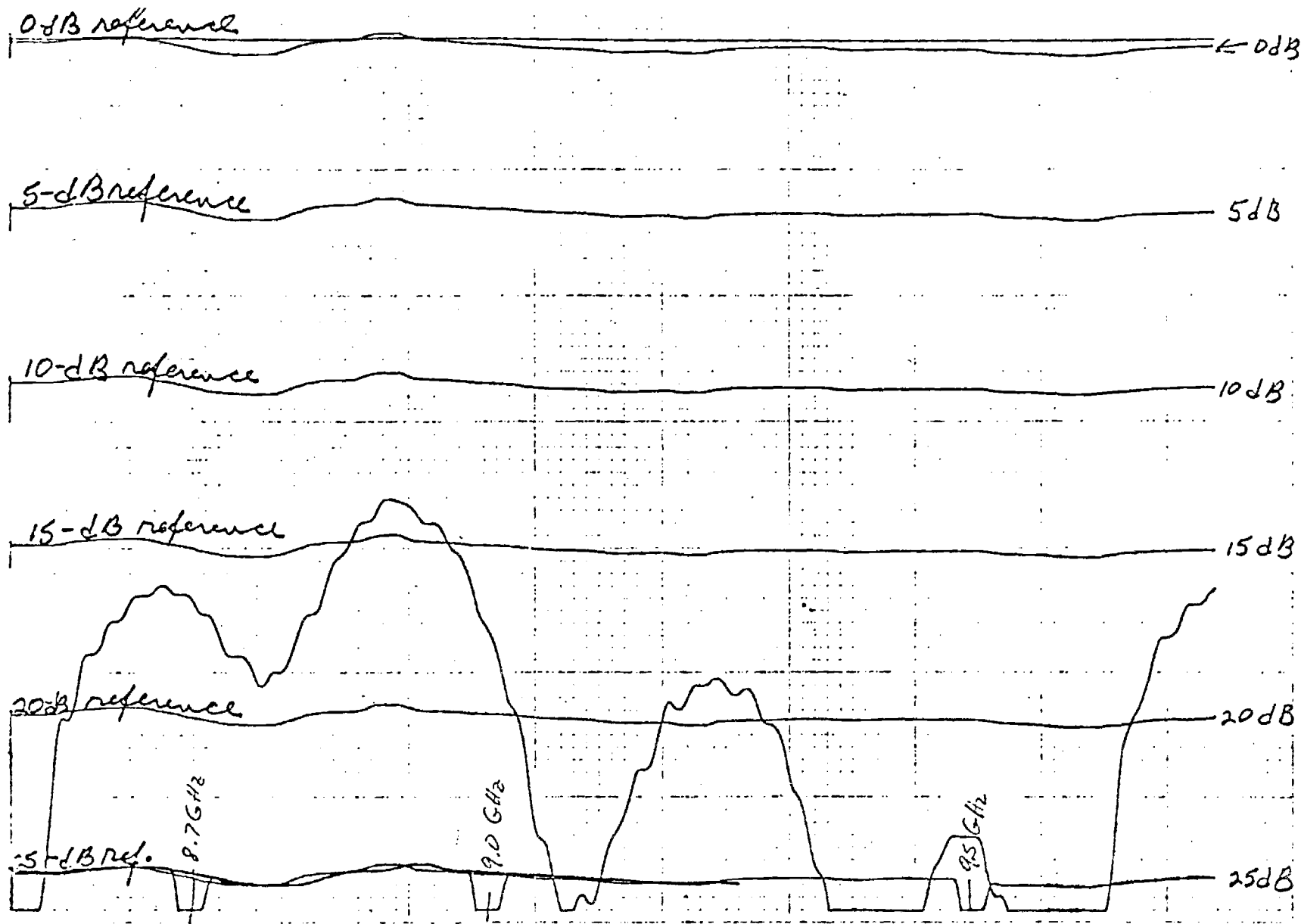


Figure 33. Return Loss vs Frequency into Auxiliary Antenna V-Port

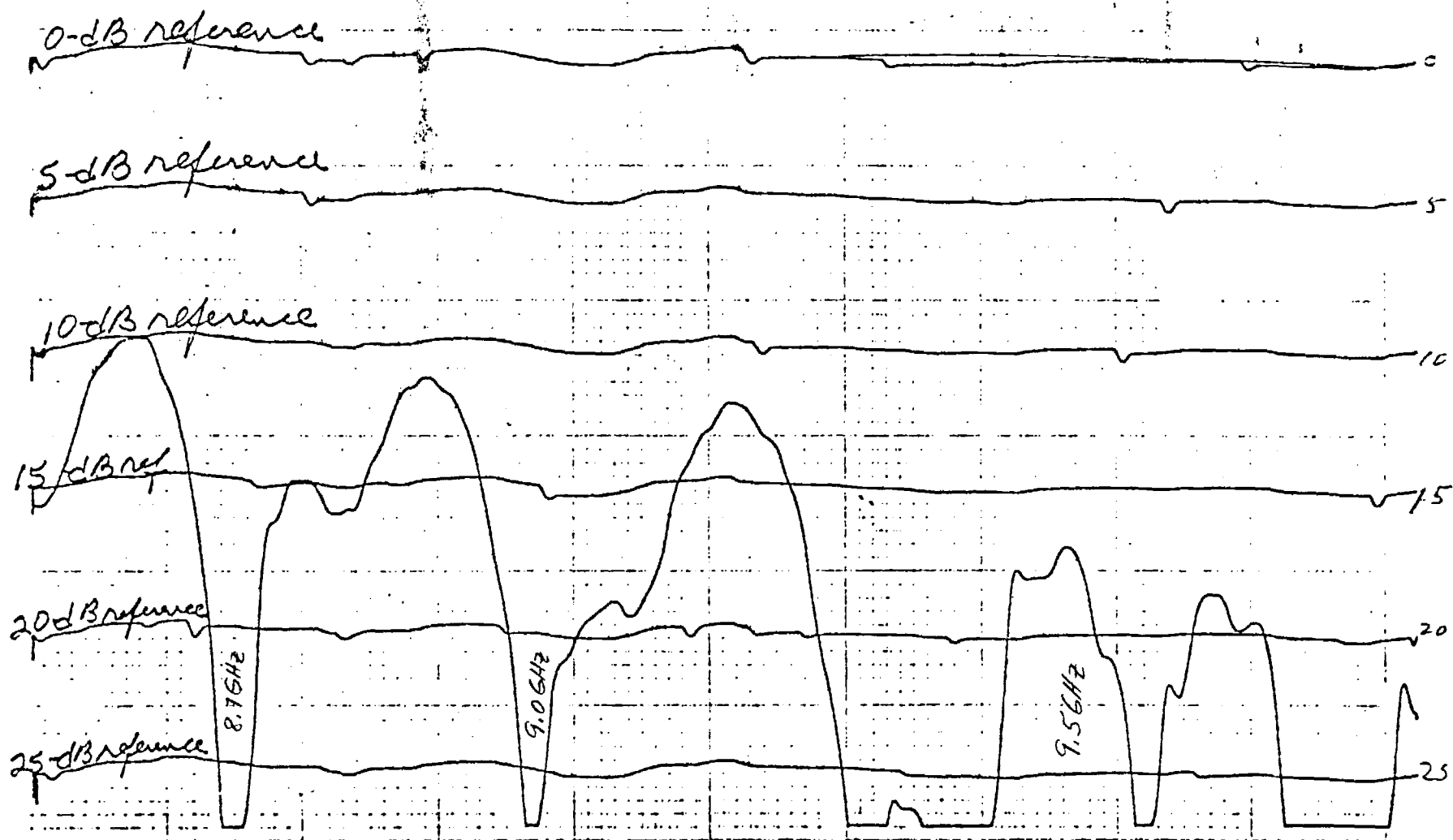


Figure 34. Return Loss vs Frequency into Auxiliary Antenna V-Port; Teflon Slab Removed from Polarizer Section

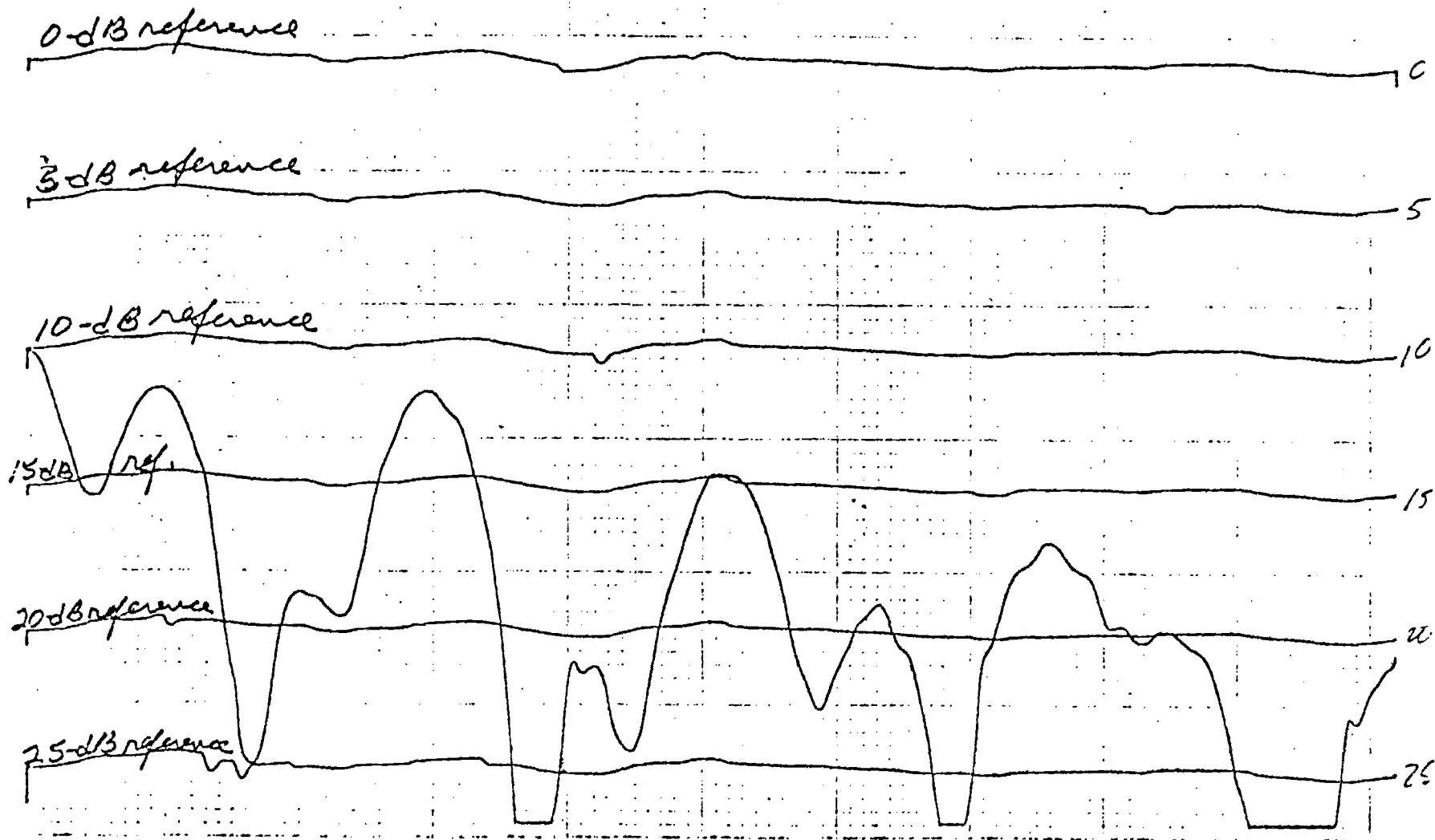


Figure 35. Return Loss vs Frequency into Auxiliary Antenna H-Port; Teflon Slab Removed from Polarizer Section

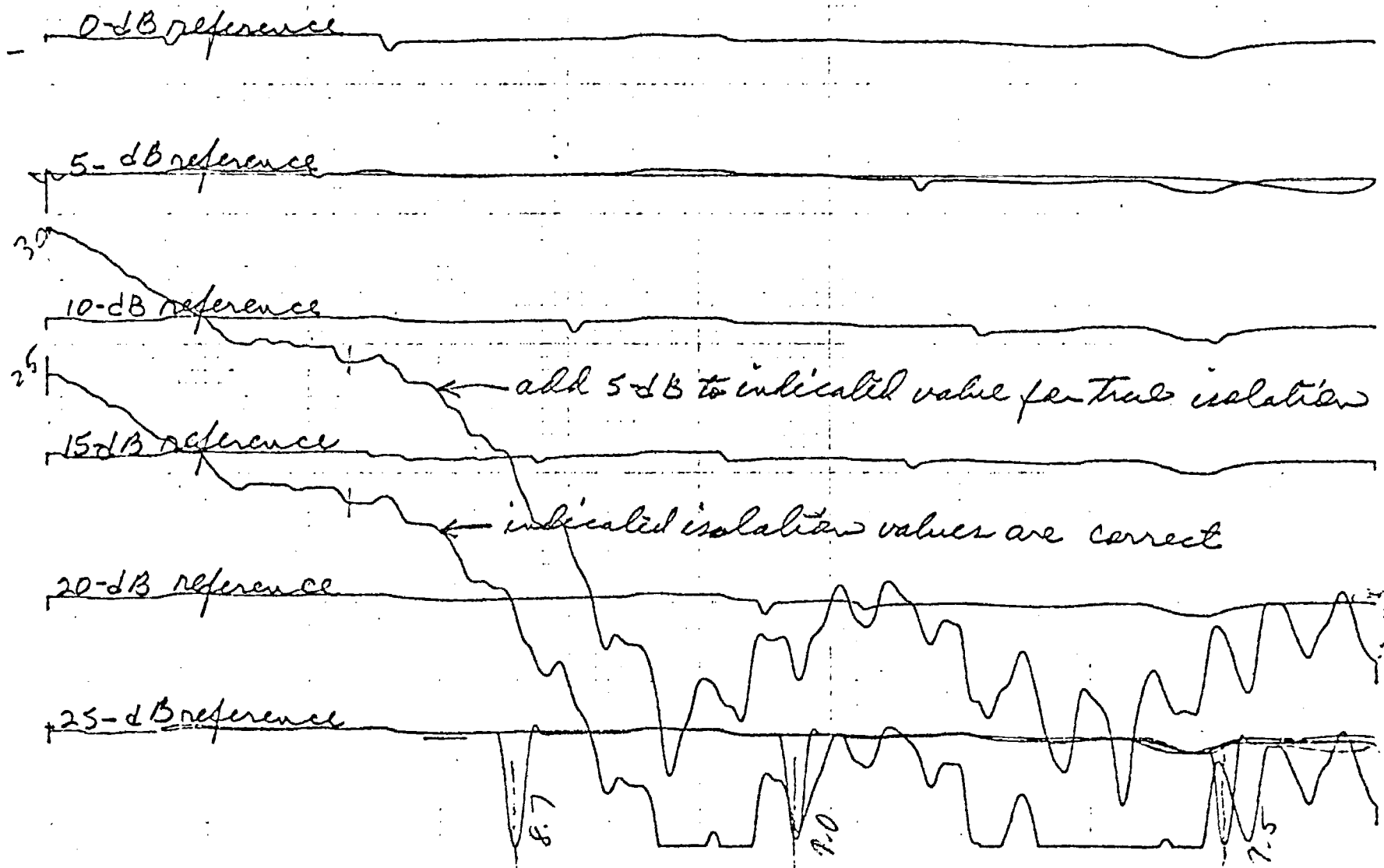


Figure 36. Auxiliary Antenna Port-to-Port Isolation vs Frequency;
H-Port Excited

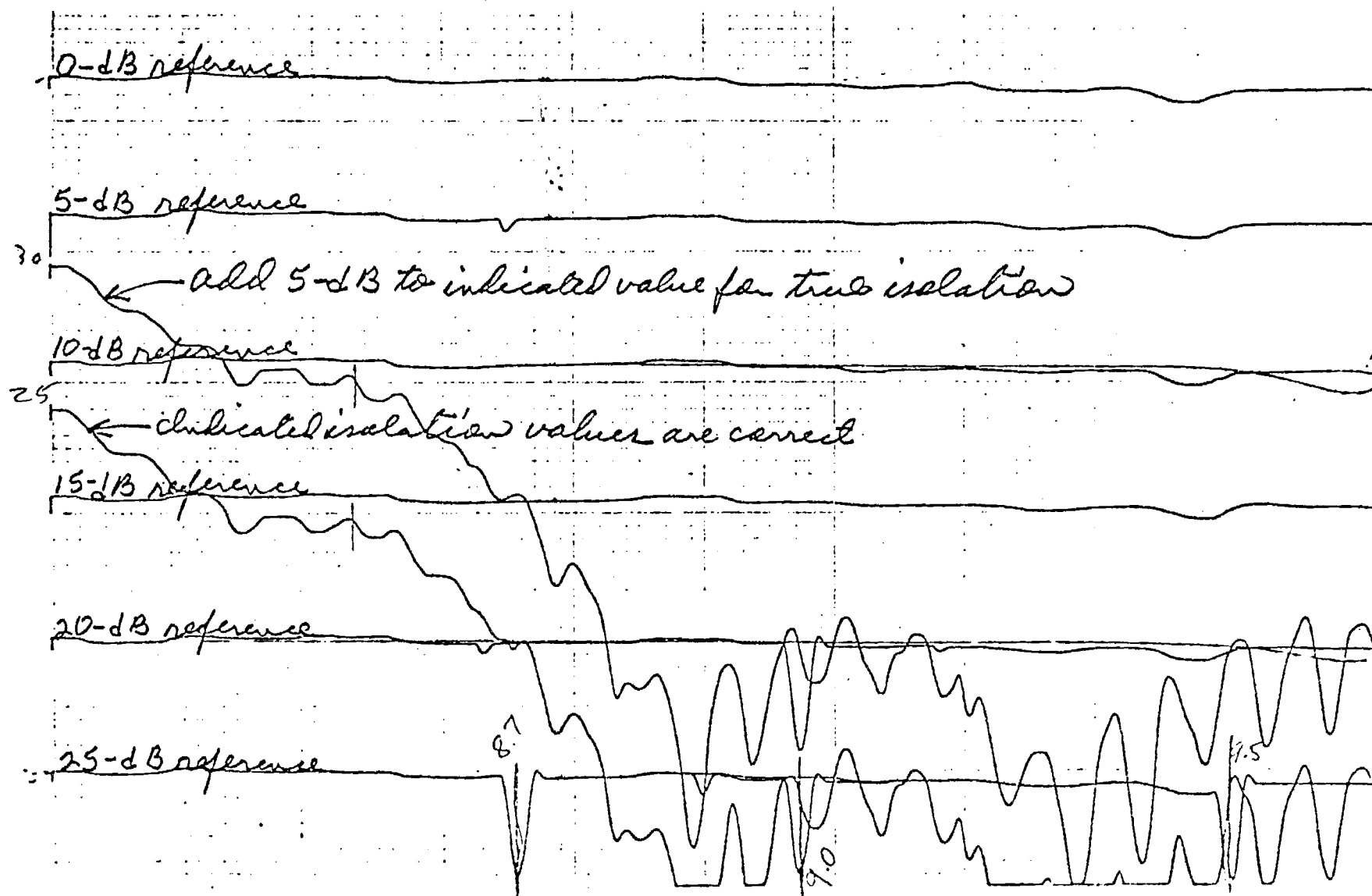


Figure 37. Auxiliary Antenna Port-to-Port Isolation vs Frequency;
V-Port Excited

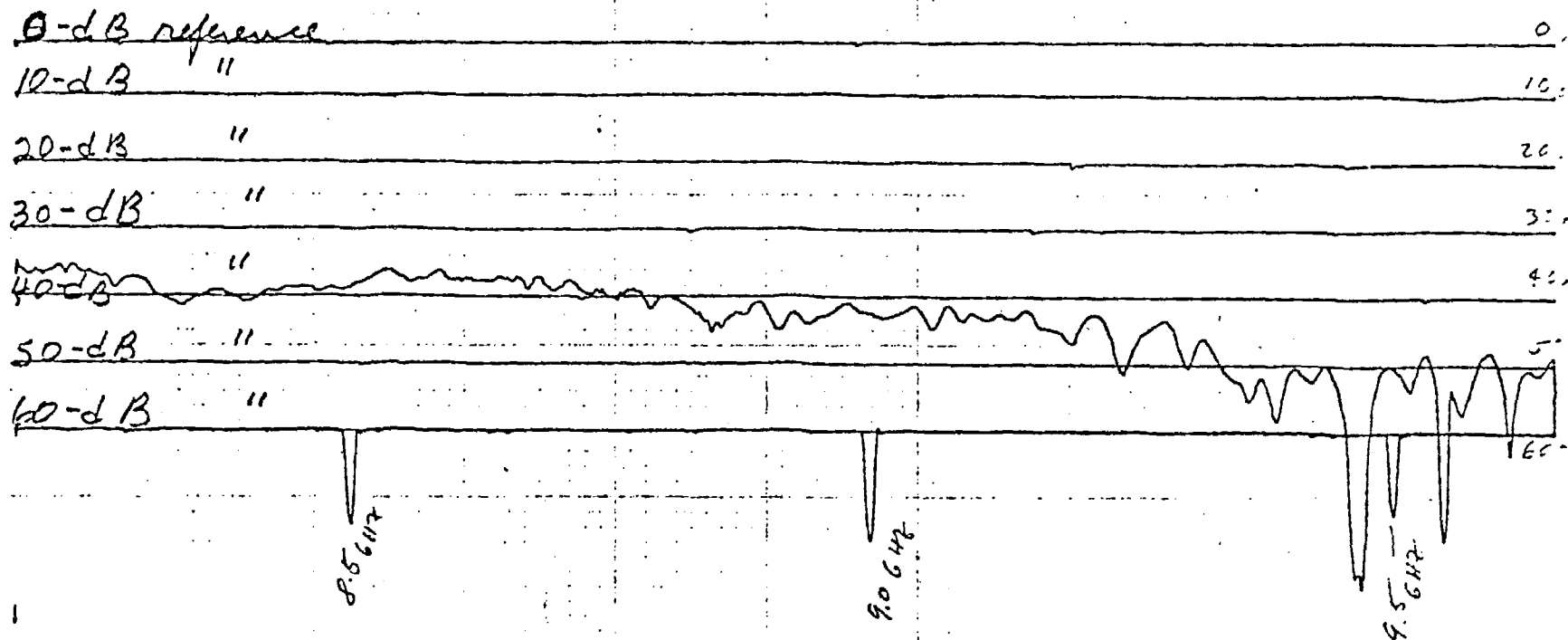


Figure 38. Auxiliary Antenna Port-to-Port Isolation vs Frequency with Teflon Slab Removed from Polarizer Section; H-Port Excited

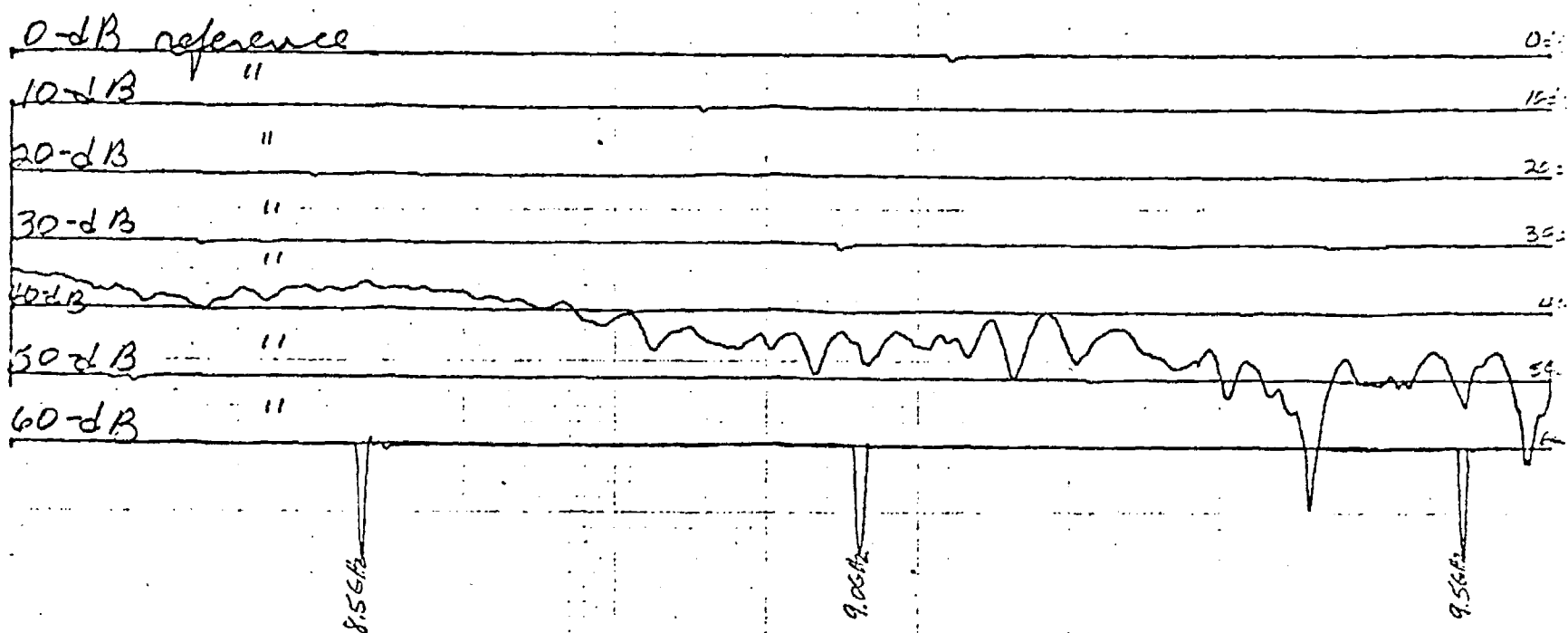


Figure 39. Auxiliary Antenna Port-to-Port Isolation vs Frequency with Teflon Slab Removed from Polarizer Section; V-Port Excited

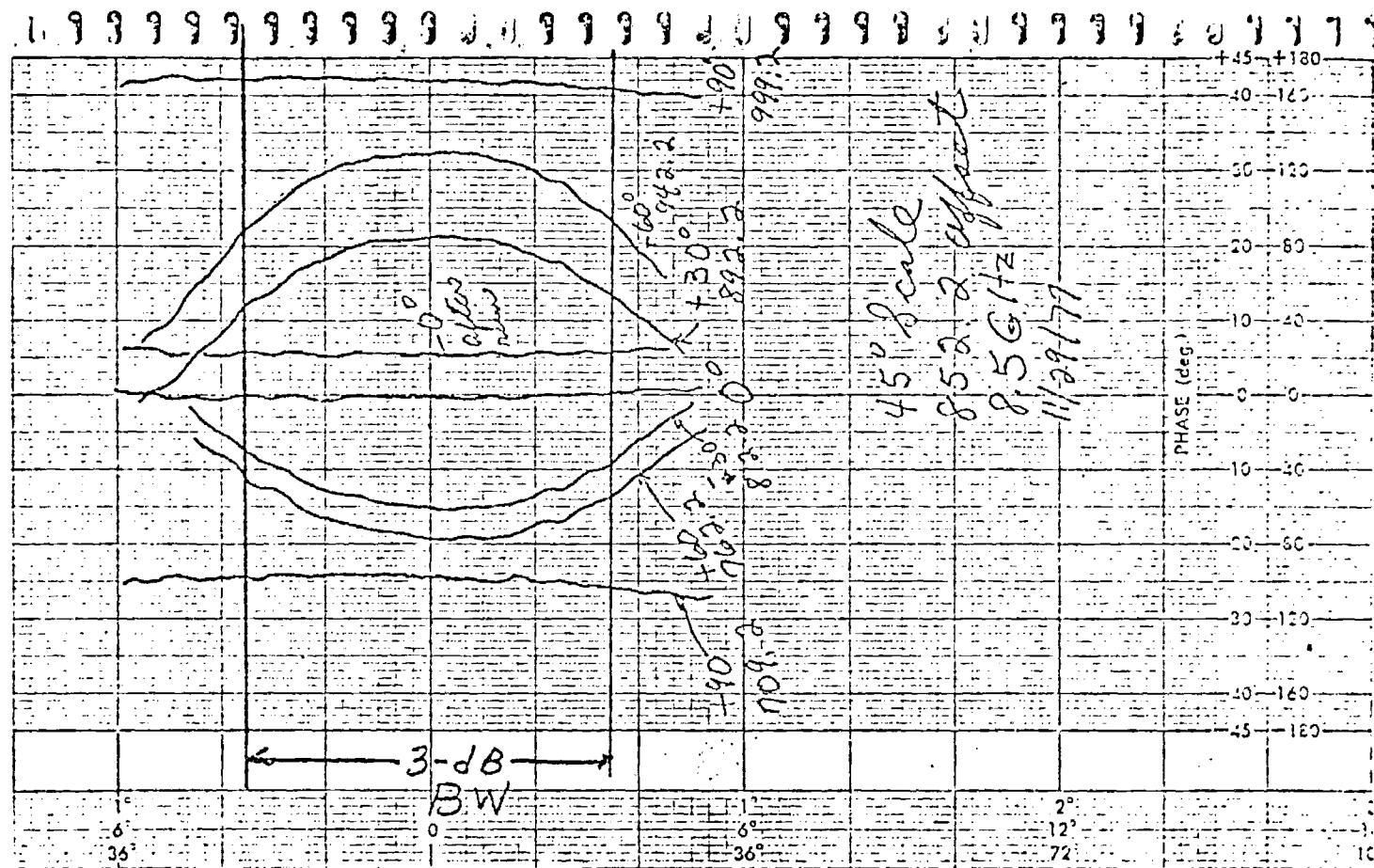


Figure 40. Auxiliary Antenna Port-to-Port Phase Tracking at 8.5 GHz

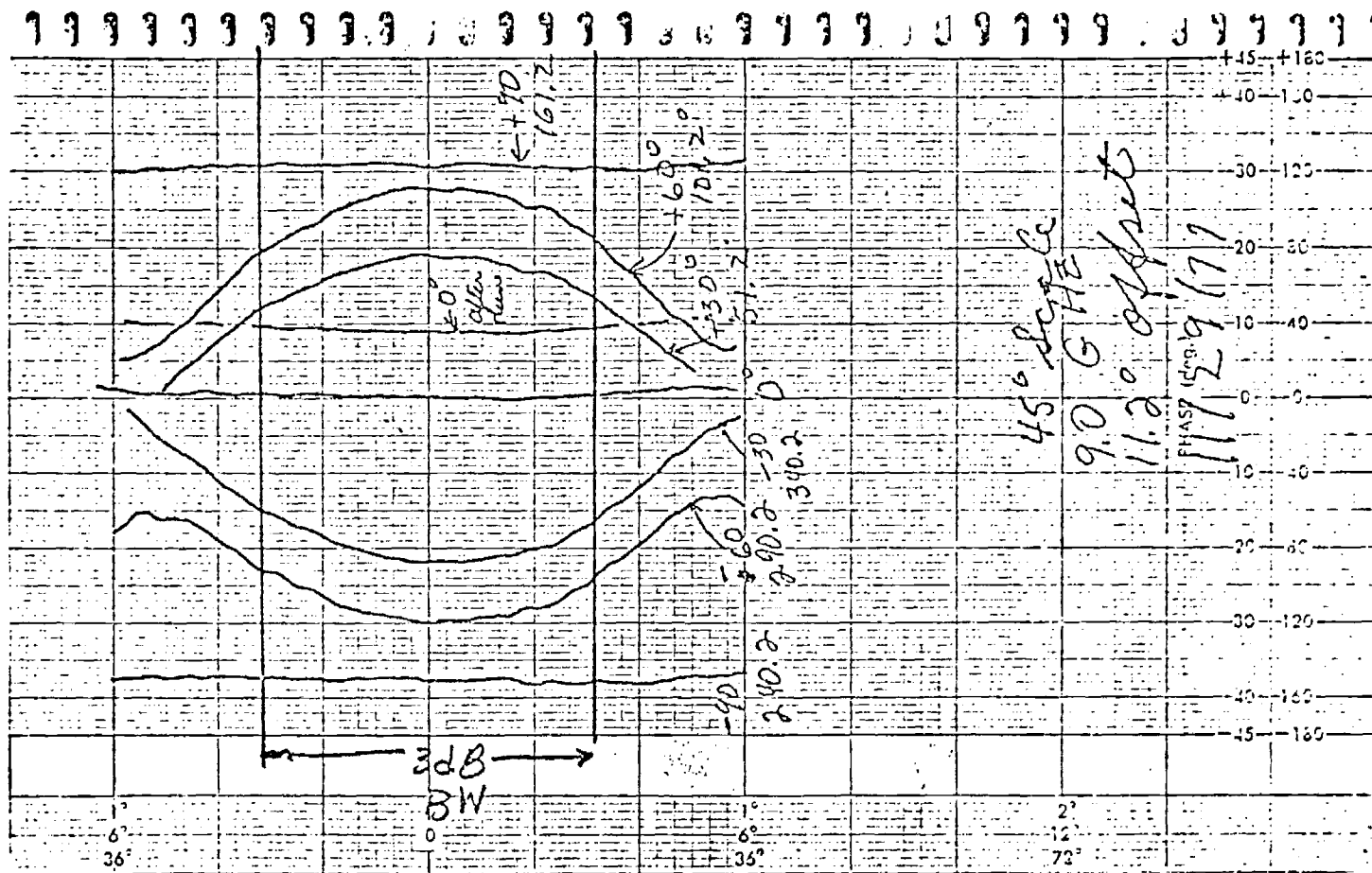


Figure 41. Auxiliary Antenna Port-to-Port Phase Tracking at 9.0 GHz

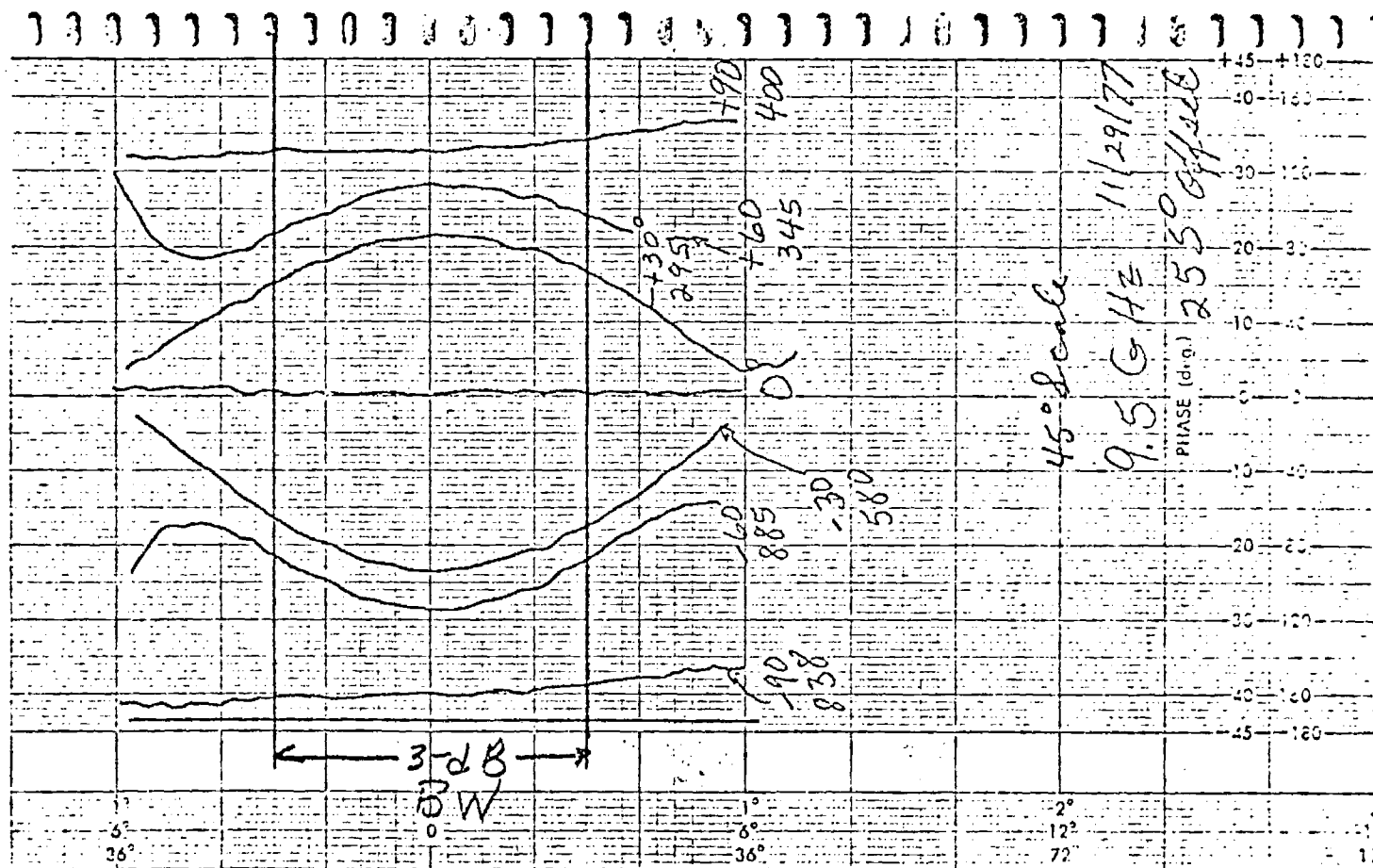


Figure 42. Auxiliary Antenna Port-to-Port Phase Tracking at 9.5 GHz

4.0 APECM/DCECM TRANSMITTER SUBSYSTEM OPERATION

4.1 Initial Set-up and Check-out Procedure

This procedure should be followed when setting up the transmitter for the first time or when the system has not been used for a considerable period of time.

4.1.1 Power On

a) Terminate the RF MON and RF TEST connectors on the driver front panel with 50 Ω , 5W CW, 8-12 GHz terminations (NARDA 370 BNM or equivalent). Terminate the CW and PULSE output connectors on the driver rear panel with similar loads.

b) Set the pin diode SPDT switch to the transponder position. This can be done by placing the RPTR/XPNDR/IIG driver front panel toggle switch to the XPNDR position.

c) Set the A-B toggle switch on the driver front panel to the A position.

d) Disable the LOOKTHROUGH switch on the driver front panel by setting it to the DISABLE position.

e) Set the mechanical DPDT switch to the NORMAL position. This can be done by placing the front panel knob switch labeled L.O. ENABLE to the NORMAL position (pos 1).

f) Set the pin diode SP4T switch to the TEST position. This can be done by placing the front panel knob labeled OUTPUT FUNCTION to the TEST position.

g) Turn both the screw adjustable variable attenuators inside the driver drawer completely counterclockwise. They are accessible only from the inside of the drawer. Turn the variable attenuator mounted on the front panel (labeled RF GAIN CONTROL) completely clockwise.

h) Connect the short semi-rigid cable assembly provided for connecting the SSA PAD and IIG RF connectors in the driver front panel.

i) Set the power switch on the bottom right of the driver front panel to the STANDBY position. Verify the light labeled POWER SUPPLIES and the LED labeled TEST come on.

j) Press the push button switch labeled ALARM RESET on the driver front panel.

k) Using a VTVM verify proper DC power supply operation by checking the appropriate Test Points on the driver front panel for +5V ($\pm .25V$), +15V ($\pm .5V$), and -15V ($\pm .5V$).

4.1.2 Fault Indicators and Safety Circuits

a) Set the pin diode SP4T switch labeled OUTPUT FUNCTION on the driver front panel to the CW position. Verify the LED labeled CW comes on. Connect a VTVM set on the -10V scale to TP2 and adjust R_{49} (of the VSWR protection circuit) until the VTVM reads -5.5 volts DC. Change the position of the OUTPUT FUNCTION switch to PULSE and verify a VTVM reading of -1.45 volts DC ($\pm .2$ VDC). The LED labeled ERROR should come on.

b) Apply a pulse trigger signal with the lowest PRF to be used into the front panel connector labeled PULSE TRIGGER. Adjust potentiometer R_{59} (on the SP4T control circuit) while looking at TP4 with an oscilloscope until this signal remains at a constant high TTL level. Maintain the OUTPUT FUNCTION switch in the PULSE and verify the LED labeled PULSE comes on. Change the OUTPUT FUNCTION switch to CW and verify the LED labeled ERROR comes on.

c) Disconnect the multipin connector on the rear of the driver drawer labeled DC POWER. With the OUTPUT FUNCTION switch in the PULSE position apply a variable DC voltage to TP3 starting at -1V and slowly decrease it. Verify the LED labeled ALARM comes on at approximately -1.45V DC ($\pm .2V$). Change the OUTPUT FUNCTION switch to the CW position, press the ALARM RESET push-button switch on the driver front panel and slowly decrease the variable DC voltage source at TP3. Verify the LED labeled ALARM comes on at approximately -5.5V DC ($\pm .2$ VDC). Remove the variable DC voltage source from TP3, change the OUTPUT FUNCTION switch to the TEST position, and press the ALARM RESET push-button switch. Reconnect the multipin connector on the rear of the driver drawer.

4.1.3 Preliminary Gain Adjustments

a) Disconnect the short cable jumper on the front panel which connects the IIG RF connector to the SSA PAD connector and the pulse trigger signal from the PULSE TRIGGER connector. Terminate SSA PAD output.

b) Connect TP1 (modulator input) to ground.

c) Connect a power meter to the front panel connector labeled RF MON.

Set the meter on the -10 dBm scale.

d) Apply AC power to the driver amplifier by changing the power switch to OPERATE. Verify the ON light comes on.

CAUTION: Before proceeding with step e, verify that the screw adjustable variable attenuator immediately following the driver TWT output is turned completely counterclockwise.

e) Apply a 9 GHz CW signal at -20 dBm to the front panel connector labeled IIG RF. Slowly increase the input power until the power meter on the RF MON output peaks. This should occur at about -4 dBm input power at the IIG RF input connector and -12 dBm RF MON power.

CAUTION: Do not exceed 0 dBm input power at the IIG RF input. Record the input power which was required to saturate the driver TWT (i.e., to reach a peak on the power meter).

f) While applying a 9 GHz CW signal at the power level recorded in step 4.1.3(e) above to the IIG RF connector, set the power meter on the RF MON output to the +10 dBm scale and slowly turn the screw adjustable variable attenuator immediately following the driver TWT clockwise until the power meter reads +6.5 dBm.

g) Return power switch to the STANDBY position and remove the RF signal source from the IIG RF connector.

h) Connect the power meter to the front panel connector labeled SSA PAD. Terminate the RF MON output. Set the meter to the 0 dBm scale. Apply a 9 GHz CW signal at -10 dBm to the front panel connector labeled RCVR RF. Slowly turn the screw adjustable variable attenuator immediately preceding the front panel connector labeled SSA PAD clockwise until the power meter reads the power level recorded for step 4.1.3(e).

i) Set the RF signal source to its minimum RF output level (at least -70 dBm), CW at 9 GHz. Set power meter to the +10 dBm scale and connect it to the RF MON connector on the driver amplifier front panel. Reconnect the semirigid cable assembly between the front panel connectors SSA PAD and IIG RF. Return power switch to the OPERATE position. With the RF signal source connected to the RCVR RF input connector, slowly increase input power, not to exceed +10 dBm. Verify meter reading approaches +6.5 dBm as input power increases and levels off at this level. With the RF input at 0 dBm, fine-tune the screw adjustable variable attenuator preceding the SSA PAD connector until the power meter peaks.

4.1.4 Modulator Calibration

a) Change the power switch to the STANDBY position. Disconnect the RF signal source from the RCVR RF input. Remove the ground from TP1 and connect a VTVM DC probe to TP1. Set the SW₁ switch (on the O/S circuit) on the large printed circuit board to obtain the desired signal polarity. Adjust potentiometer R₄₄ to obtain the desired DC offset voltage on the meter scale. Apply a known DC voltage at the EXT MOD input on the front panel and adjust potentiometer R₄₇ to obtain the desired scaling factor (gain) as shown on the meter.

b) Disconnect the short semirigid cable assembly from the SSA PAD and the IIG RF connectors on the driver front panel. Terminate the SSA PAD connector. Set the RF signal source for 9 GHz CW at a level of -25 dBm and connect it to the IIG RF input on the front panel. The power meter should remain connected to the RF MON connector on the front panel and the VTVM should remain connected to TP1. Change power switch to the OPERATE position. Vary the DC voltage at the EXT MOD connector on the front panel as indicated below. The power meter should decrease linearly at 10 dB/volt as the voltage on the VTVM increases.

<u>VTVM</u>	<u>PWR MTR*</u>
0V DC	- 5 dBm
1V DC	-15 dBm
2V DC	-25 dBm
3V DC	-35 dBm
4V DC	-45 dBm
5V DC	-55 dBm

* If the power levels are too low to make accurate readings, follow the following procedure:

- a) Return the power switch to the STANDBY position.
- b) Connect the power meter to the RF TEST connector, and connect a 50 Ω load to the RF MON connector. Readings should be approximately 20 dB higher than indicated in the above table.
- c) Return power switch to the OPERATE position and take readings.
- d) Return power switch to the STANDBY position, remove power meter, and reconnect 50 Ω load to the RF TEST connector.

c) Return the power switch to the STANDBY position and reconnect the cable assembly between the SSA PAD and IIG RF connectors. Reconnect the 50 Ω load to the RF MON connector and connect TP1 to ground.

4.1.5 Lookthrough Verification

Connect the power meter to the CW output in the rear of the driver drawer. Change the OUTPUT FUNCTION switch to CW. Set the RF source for 9 GHz CW at a level of -60 dBm and connect it to the RCVR RF connector on the driver front panel. Change the power switch to the OPERATE position and increase the input power until the power meter reads +10 dBm. Disconnect the cable on the LOOKTHROUGH connector and change the appropriate toggle switch on the driver front panel to the LOOKTHROUGH position. Verify the power output has dropped to below -40 dBm. Change the power switch to the STANDBY position, remove the RF source from the RCVR RF connector, change the OUTPUT FUNCTION switch to the TEST position, remove the power meter from the rear panel on the driver drawer, and return the LOOKTHROUGH switch to the DISABLE position.

4.1.6 Repeater Mode Operation

Connect the power meter to the RF MON connector on the driver front panel. Change the mode of operation to the repeater mode by setting the RPTR/XPNDR/IIG toggle switch to the RPTR position. Apply a 9 GHz CW at -50 dBm to the AUX ANT connector on the driver front panel and change the power switch to the OPERATE position. Slowly increase input power, and verify the power meter approaches +6 dBm and levels off at that point as input power continues to increase.

CAUTION: Do not exceed ± 10 dBm input power. Return the power switch to the STANDBY position.

4.1.7 Auxiliary Receiver Calibration

a) Disconnect the ground from TP1, change the front panel toggle switch from the repeater mode (RPTR) to the instantaneous inverse gain mode (IIG). Connect one of the probes of a dual trace oscilloscope to TP1. Connect the L.O. signal from the APECM receiver to the driver front panel connector labeled L.O. Change the L.O. ENABLE switch to the IIG position (pos 2).

b) Reduce the input power into the AUX ANT connector to -50 dBm. Adjust variable resistor R_{19} (on the IIG circuit) so that TP1 reads 0 volts DC. Increase the input power to 0 dBm and record the voltage at TP1. Reduce the input power to -10 dBm and record the voltage at TP1. If the difference in the two readings is not approximately one volt, then adjust R_{18} on the IIG circuit accordingly. Step 4.1.7(b) should be repeated several times as there is interaction between the two adjustments.

c) Amplitude modulate the 9 GHz CW RF signal at -10 dBm with a 25 Hz signal at between 30% and 50% modulation. Connect the other probe from the dual trace oscilloscope to TP5 on the driver front panel. Adjust variable resistor R_{17} until both signals are exactly in phase. Repeat steps 4.1.7(b) and 4.1.7(c) to verify settings of R_{17} , R_{18} , and R_{19} .

d) Disconnect the RF signal source from the AUX ANT connector, replace the 50 Ω load at the RF MON connector, remove the oscilloscope probes, and shut off the AC power at the front panel switch.

4.1.8 CW Plumbing Drawer Adjustments

a) Follow the manufacturer's instructions for zeroing the two power monitors inside the CW/PLUMBING drawer.

b) Adjust potentiometer R_3 in the panel meter connection circuit (CW/PLBG drawer) while using the manufacturer's audio calibration procedure for the power monitors. R_3 should be adjusted so that a -10 V/mA of meter current relation exists.

4.2 Periodic Check-out Procedure

This procedure should be followed only when the operator is certain that the initial set-up and check-out procedure (part A) has been performed recently and he is confident of the validity and currency of its results. The following procedure must be followed when changing from PULSE to CW operation and vice versa or when switching to the IIG mode.

4.2.1 General Checks

4.2.1.1 Driver Front Panel Connections

a) Terminate the RF MON and RF TEST connectors with 50 Ω , 5 W, CW, 8-12 GHz terminations (NARDA 370 BNM or equivalent).

b) Connect the short semi-rigid cable assembly provided for connecting the SSA PAD and IIG RF connectors.

- c) Connect the RCVR RF connector to the RF OUT connector on the RF receiver.
- d) Connect the AUX ANT connector to the auxiliary antenna.
- e) Connect the L.O. connector to the auxiliary L.O. connector on the RF receiver.
- f) Connect the PULSE TRIGGER BNC connector to the XMIT GATE connector on the PROCESSOR-CONVERTER drawer.
- g) Connect the LOOKTHROUGH BNC connector to the CW XMIT connector on the PROCESSOR-CONVERTER drawer.

4.2.1.2 Driver Front Panel Switch Selections

- a) RPTR/XPNDR/IIG to XPNDR.
- b) A-B to A.
- c) LOOKTHROUGH to DISABLE.
- d) OUTPUT FUNCTION to TEST.
- e) L.O. ENABLE to NORMAL.

4.2.1.3 Driver Rear Panel Connections

- a) Connect the CW output connector to the CW input on the CW/PLUMBING drawer.
- b) Connect the PULSE output to the INPUT connector on the PULSE TWT drawer.
- c) Connect the PULSE TRIGGER BNC connector to the TRIGGER connector on the PULSE TWT drawer.
- d) Connect the multipin signal connector to the CW/PLUMBING drawer.
- e) Connect the PULSE TWT OUTPUT connector to the PULSE connector on the CW/PLUMBING drawer.

4.2.2 Pulse/CW Set-up Procedure

4.2.2.1 CW Operation Set-up Procedure

- a) Ensure the OUTPUT FUNCTION switch on the driver front panel is on the TEST position.
- b) Change the waveguide switch in the CW/PLUMBING drawer so that the CW TWT output signal is directed to the front panel and out (through the waveguide filter, etc.).
- c) Replace the power 50 Ω load from the waveguide switch to the bulk-head flange assembly on the CW/PLUMBING drawer front panel.

d) Apply AC power to both the driver drawer and the CW/PLUMBING drawer. Place the CW TWT on the STANDBY position.

e) Apply a 9 GHz, CW signal at less than -40 dBm at the RCVR RF input on the driver front panel.

f) Connect a power meter set on the +10 dBm scale to the RF MON output on the driver front panel and slowly increase the input signal power (do not exceed +10 dBm under any circumstances) while watching the power meter. If the power meter level increases beyond +6 dBm, turn the screw adjustable variable attenuator immediately following the driver TWT output counterclockwise until the power meter decreases to +6 dBm once again. Continue increasing input power until 0 dBm input power causes +6 dBm RF MON output power.

g) Decrease the input power to its lowest possible level (< -70 dBm) and change the OUTPUT FUNCTION to the CW position. Press the ALARM RESET button if the ALARM LED comes on.

h) Slowly increase the input power while watching the power meter connected to the RF MON (so it will not exceed +6 dBm) until the input power is 0 dBm.

i) Fine tune the screw adjustable variable attenuator immediately following the driver TWT output so that it will cause the meter on the CW/PLUMBING DRAWER front panel to peak.

CAUTION: Do not exceed +10 dBm out of the RF MON output.

4.2.2.2 PULSE Operation Set-up Procedure

a) Ensure the OUTPUT FUNCTION switch on the driver front panel is on the TEST position.

b) Change the waveguide switch in the CW/PLUMBING drawer so that the PULSE TWT output signal is directed to the front panel and out (through the waveguide filter, etc.).

c) Replace the power 50 Ω load from the waveguide switch to the bulk-head flange assembly on the CW/PLUMBING drawer front panel.

d) Apply AC power to both the driver drawer and the PULSE drawer. Place the PULSE on the STANDBY position.

e) Apply a 9 GHz, CW signal at less than -40 dBm at the RCVR RF input on the driver front panel.

f) Connect a power meter set on the +10 dBm scale to the RF MON output on the driver front panel and slowly increase the input signal power (do not

exceed +10 dBm under any circumstances) while watching the power meter. If the power meter level increases beyond +6 dBm, turn the screw adjustable variable attenuator immediately following the driver TWT output counterclockwise until the power meter decreases to +6 dBm once again. Continue increasing input power until 0 dBm input power causes +6 dBm RF MON output power.

g) Replace the input with a 2% duty cycle pulse source at the lowest possible level (< -70 dBm) and change the OUTPUT FUNCTION to the PULSE position. Press the ALARM RESET button if the ALARM LED comes on. A pulse trigger signal must be present on the PULSE TRIGGER input on the driver front panel.

h) Slowly increase the input power until the input power is 0 dBm.

i) Fine tune the screw adjustable variable attenuator immediately following the driver TWT output so that it will cause the meter on the CW/PLUMBING drawer front panel to peak.

4.2.3 Mode Selection Procedure

4.2.3.1 IIG Operation Set-up Procedure

a) Follow the same procedure as in 4.2.2 for PULSE or CW except that the input signal will be applied at the IIG RF input on the driver front panel at the power level available from the RF receiver.

b) The proper driver front panel status is as in 4.2.1 except:

b.1 No cable connecting SSA PAD and IIG RF

b.2 Connect IIG RF to the RF OUT connector on the RF receiver

b.3 RPTR/XPNDR/IIG to IIG position

b.4 L.O. ENABLE to IIG.

4.2.3.2 Repeater Operation Set-up Procedure

a) Follow the same procedure as in 4.2.2 for PULSE or CW operation.

b) The proper driver front panel status is as in 4.2.1 above, except:

b.1 RPTR/XPNDR/IIG switch to RPTR.

4.2.3.3 Transponder Operation Set-up Procedure

a) Follow the same procedure as in 4.2.2 for PULSE or CW operation.

b) The proper driver front panel status is as in 4.2.1.

APPENDIX

AIRBORNE IMPLEMENTATION OF THE APECM SYSTEM

I. Aircraft Facilities

The APECM system is installed in the GT/EES Airborne Electronics Laboratory for flight testing (see Figure A-1). The aircraft is a T-29B (modified Convair 240) with an enlarged nose radome and a belly radome added. This aircraft, with a wing span of 92 feet, length of 75 feet, and a fully loaded gross weight of 44,000 pounds can safely operate from an airport with a runway length of 4,000 feet or more, depending on altitude and temperature. Since the aircraft is self-starting, operational support is minimal, needing only parking space, fuel and oil vendor, and a small amount of enclosed storage space for operational spares and supplies.

The aircraft carries a useful load (system equipment, operators, mission-related equipment) of 2,000 pounds at an optimum altitude of 10,000 feet above mean sea level (maximum usable altitude of 15,000 feet MSL) and true airspeed of 190 knots (219 MPH). Fuel consumption is approximately 200 gallons of 100/130 AVGAS per hour.

Nose Radome Area (see Figure A-2)

Previous modification of the aircraft installed a larger radome, as used by Convair 340 and 440 models. This allows a large area for mounting test antennas. The APECM antenna (dual circular polarization) is mounted on centerline. Waveguide is installed through the bulkhead, then internally through the pressurized area to the system equipment rack. The antenna is mounted with a droop of 6° from centerline, giving an in-flight droop of approximately 3° from flight path.

Belly Radome Area (see Figure A-3)

The belly radome contains an auxiliary antenna (also dual circular polarized) for use in monitoring and receiving signals. Its location provides good isolation from signals transmitted by the nose antenna. In addition, tracking beacon antennas are mounted within. The signal emitted by these allows precise tracking of the aircraft by a test range reference radar, thus assuring accurate "true position" data for test runs.



Figure A-1. GT/EES Airborne Electronics Laboratory

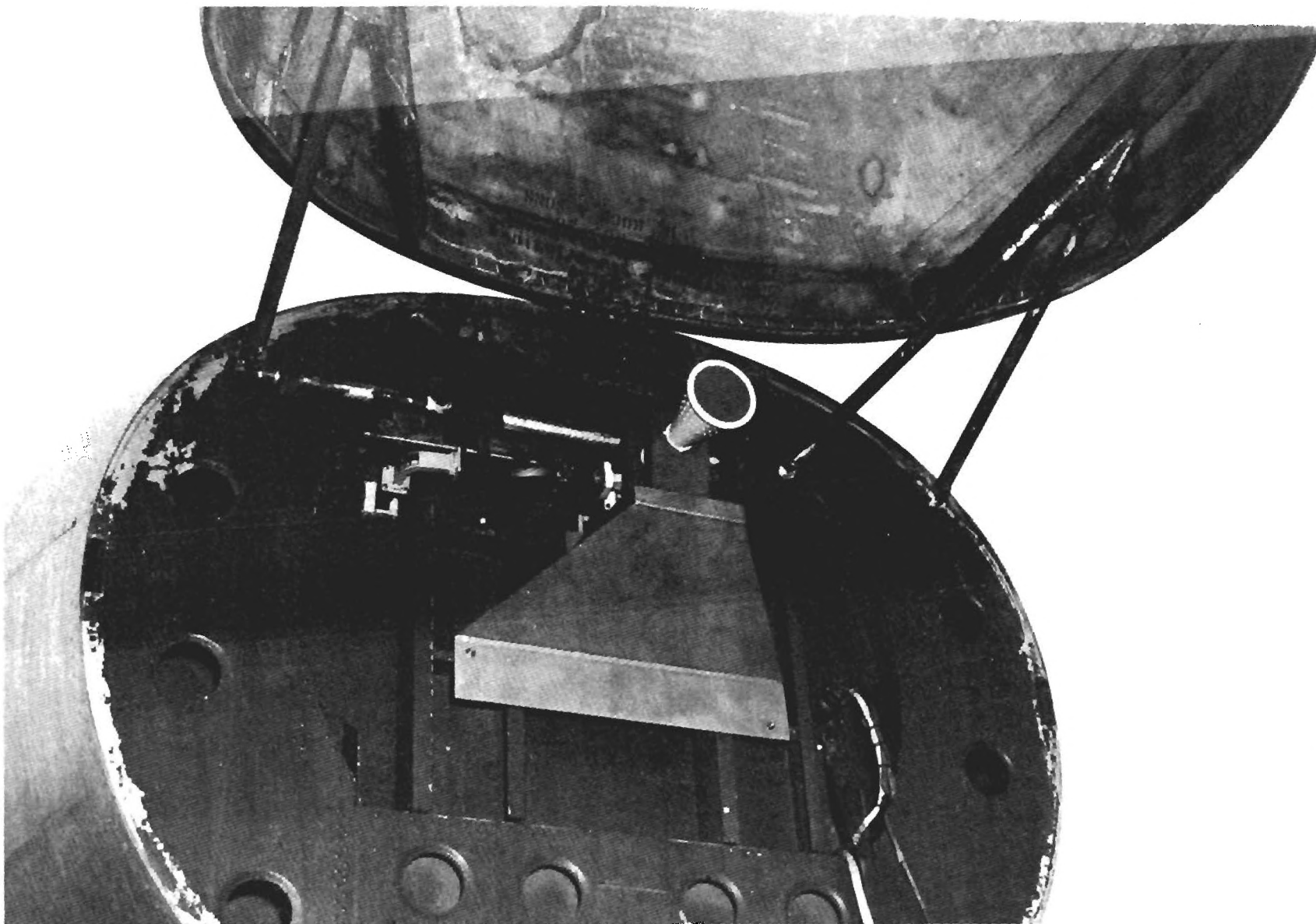


Figure A-2. Nose Radome Area



Figure A-3. Belly Radome Area

Wingtip Antennas (see Figure A-4)

A small circular-polarized antenna is mounted under each wingtip. Each antenna is removable, and can be exchanged as necessary for different test configurations. The mount is installed with a droop of 11° from centerline, giving an in-flight droop of approximately 8° from flight path. Waveguide is installed internally through the wing and fuselage to the system equipment rack.

Auxiliary Power Unit (APU) Installation (see Figure A-5)

A gas-turbine driven generator unit, modified to provide 500 amps of 28 volt DC and 30 KVA of 115 volt, 400 Hz AC (3-phase) is mounted in the aft end of the cabin. Intake airscoop and exhaust outlet are mounted on the outside of the aircraft. The APU has its own batteries for starting. The DC output can be connected to the aircraft DC bus system to provide power for engine starting or as emergency backup DC power. The AC output of the APU provides prime power for the APECM system equipment.

The control console, seen to the right of the large box which contains the APU, is used to control and monitor the APU and its outputs. The tie-in of APU-to-aircraft system is controlled by a switch panel in the cockpit, which also contains an emergency cut-off switch and a control for the fire extinguisher system installed on the APU.

II. Project Equipment Installation

Overall Layout (see Figure A-6)

The prime APECM equipment is mounted in the forward equipment rack on the left side of the cabin. The aft rack contains support and recording equipment (i.e., oscilloscopes, pulse generators, visicorder, etc.). Waveguide from the prime equipment is installed along the left side of the cabin, leading forward to the nose antenna. In addition, waveguide is installed out through the wing (aft of the rear spar) to the wingtip antennas. Coaxial cable is installed from the auxiliary antenna (in the belly radome) to the aft equipment rack, and from the beacon antenna (also in the belly radome) to the beacon transponders (forward of the forward equipment rack).

An operator's chair is positioned at each equipment rack for use during test operations. Passenger seats forward of them are used for take off and landing, as well as for accommodation of other passengers (observers, etc.).

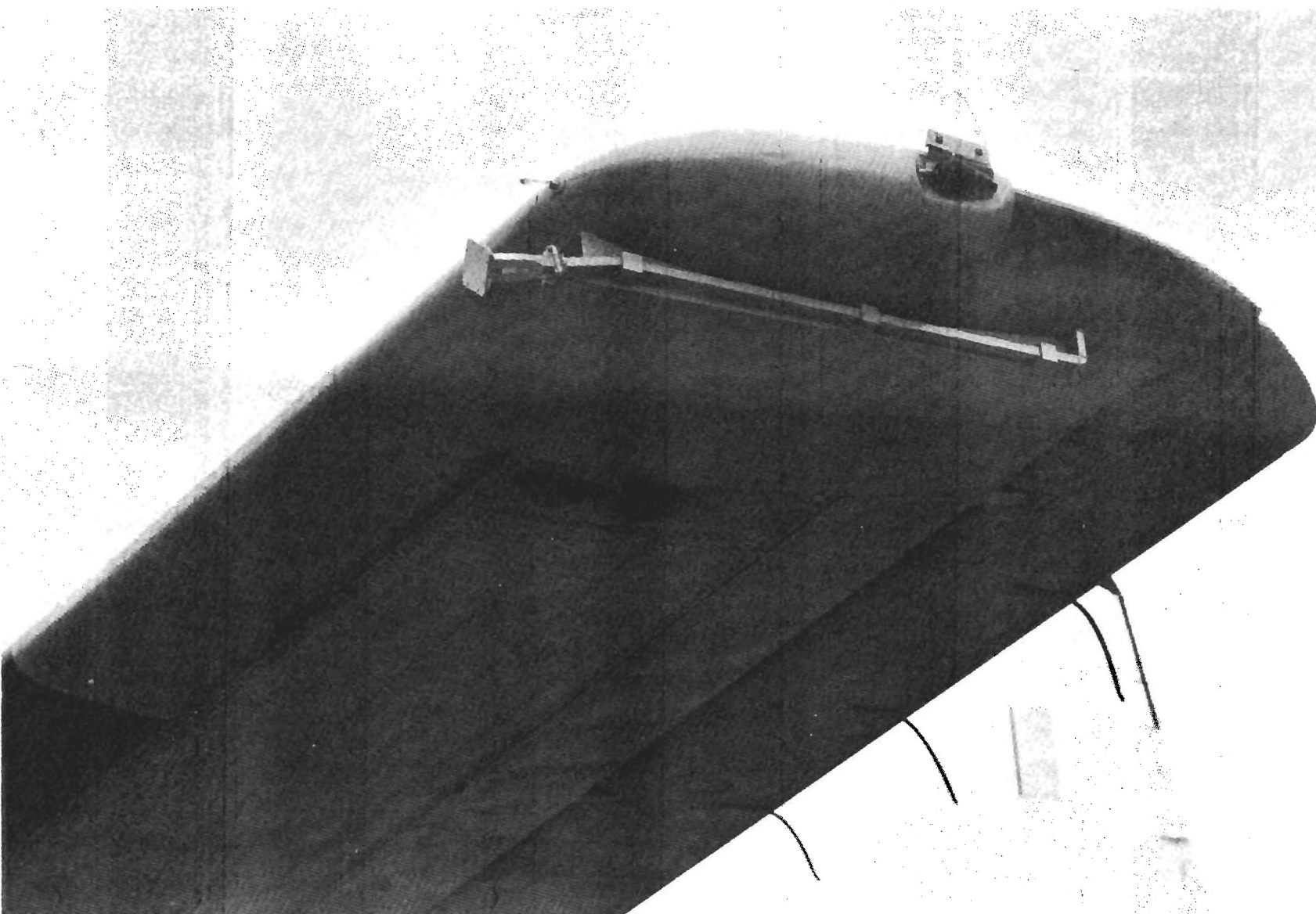


Figure A-4. Wingtip Antenna

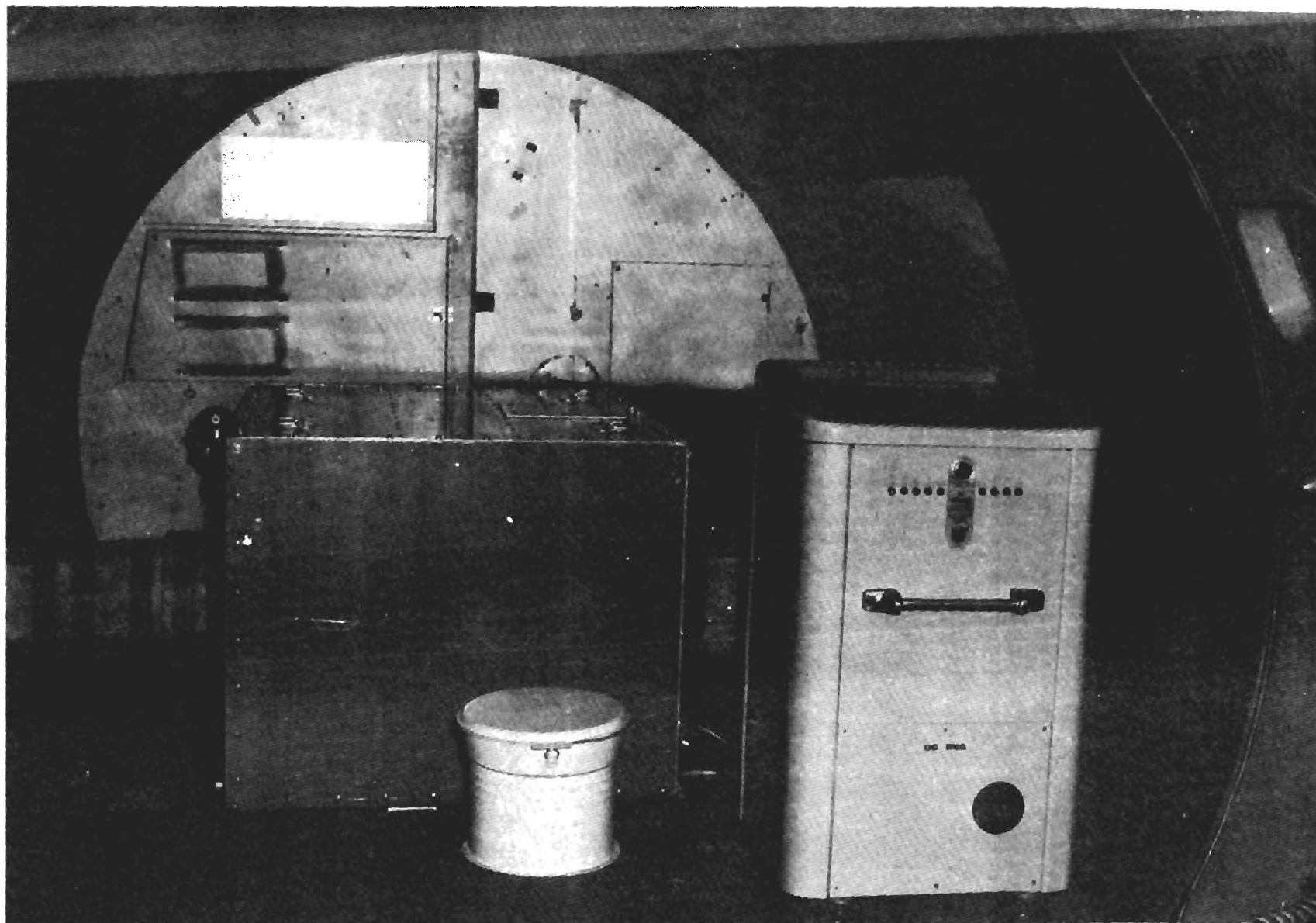


Figure A-5. APU Installation

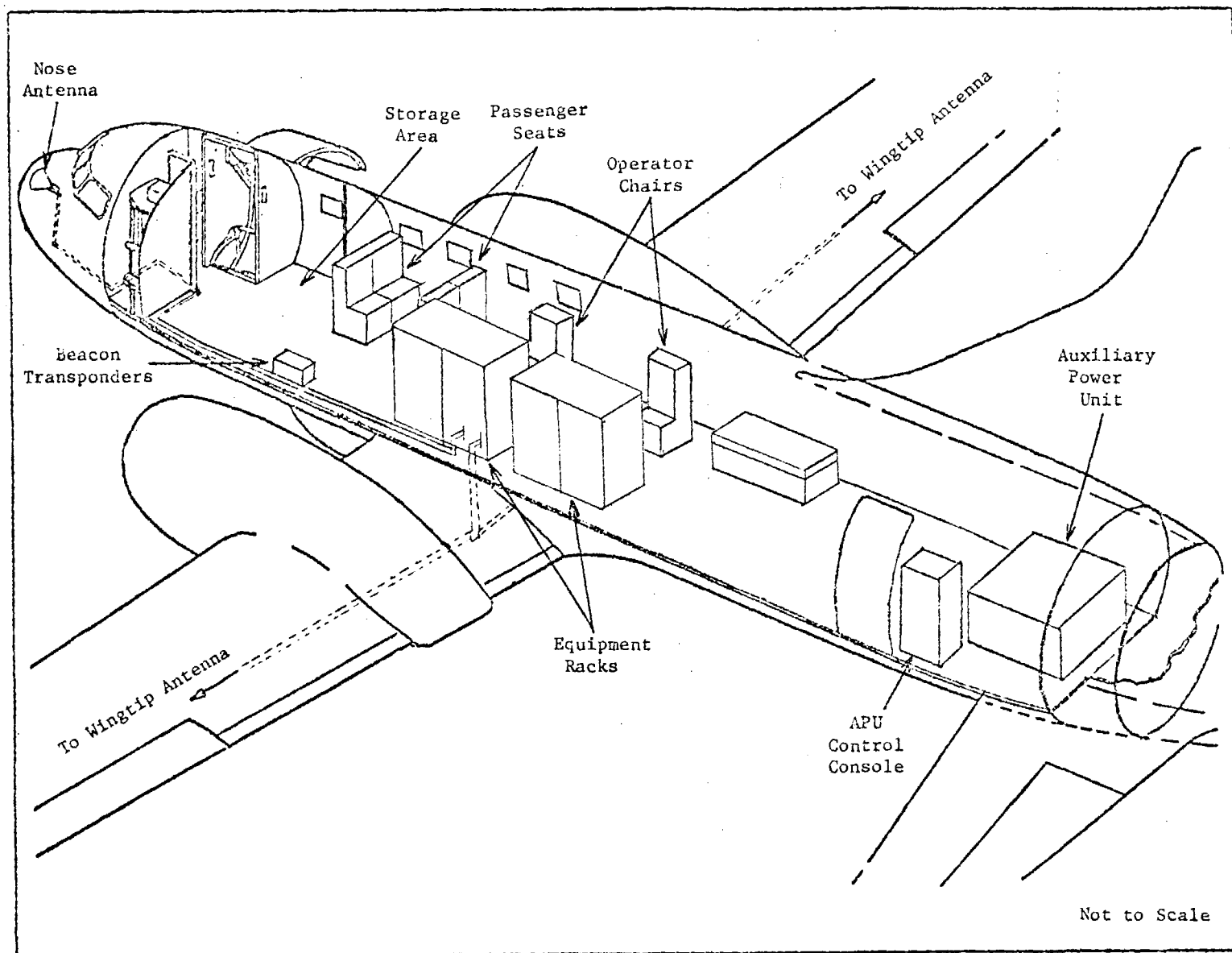


Figure A-6. Overall Layout

Equipment Installation (see Figure A-7)

In the right lower foreground is the mount for the beacon transponders. The waveguide from the nose radar passes under it and goes to the rear of the forward equipment rack. Passenger seats are on the left, and the APU box is in the far background. Some test equipment on top of the rack and on the floor was being used for system maintenance when the photograph was taken.

Prime Equipment Installation (see Figure A-8)

The left side of the forward equipment rack contains (from top down):

- APECM processor-converter: controls system functions and polarizer
- Receiver IF drawer
- APECM receiver: contains receiver tuning and conversion functions
- APECM polarizer: controls polarization of received and transmitted signals.

The right side of the rack contains (from top down):

- Sweeper oscillator for maintenance
- TWT amplifier for maintenance
- Connector panel for visicorder data
- Transmitter driver: controls transmitter modes and modulation, pre-amplifies signal to be sent to TWT amplifiers for output
- Hi-power pulse TWT amplifier: amplifies pulse-mode signals for output through polarization to antennas
- Hi-power CW TWT amplifier: amplifies CW-mode signals for output.

Complete Equipment Rack Installation (see Figure A-9)

Aft equipment rack (to left in picture) contains support equipment. Note oscilloscope and signal generators mounted on top of both cabinets for monitoring and control of system.

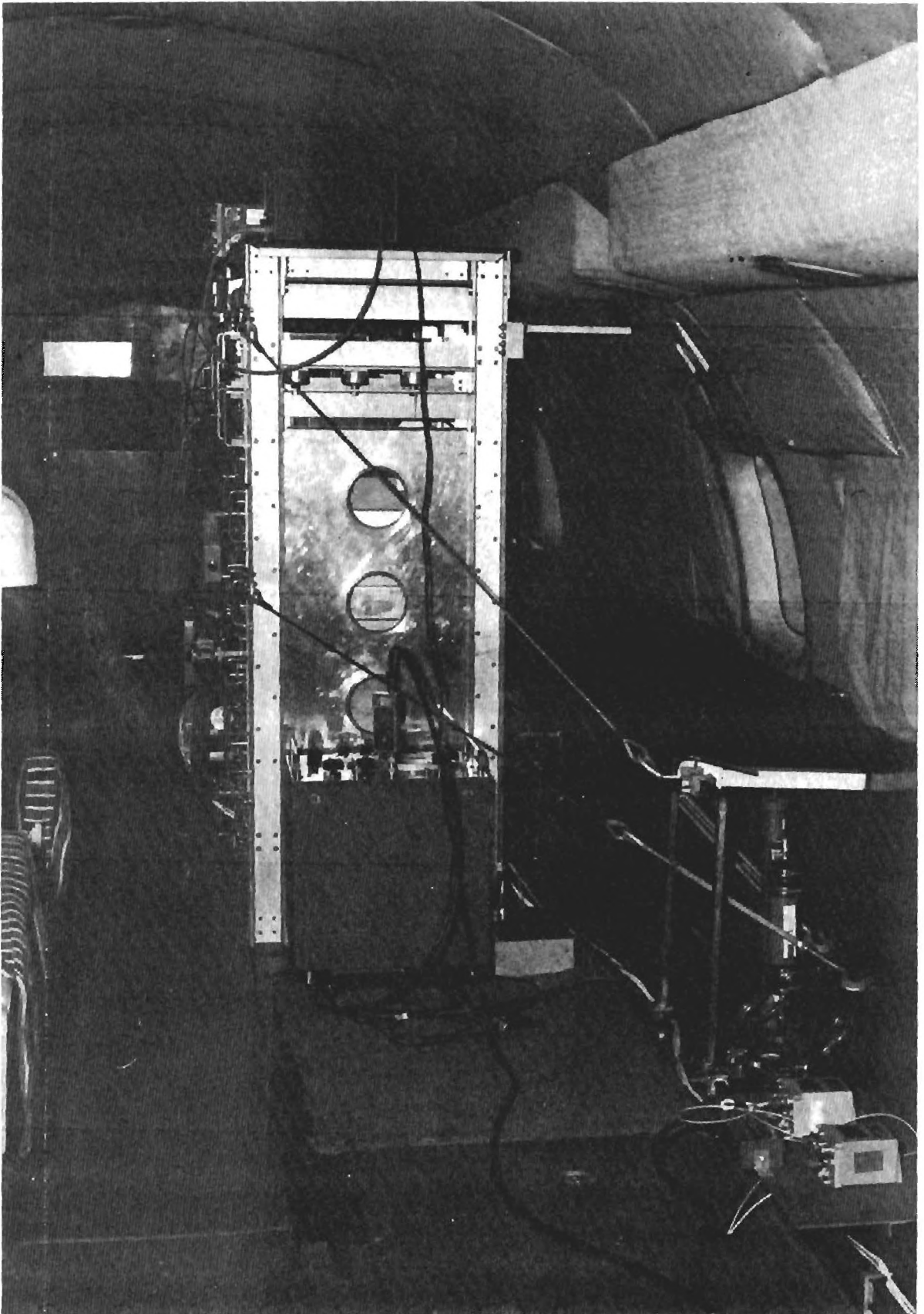


Figure A-7. Equipment Installation

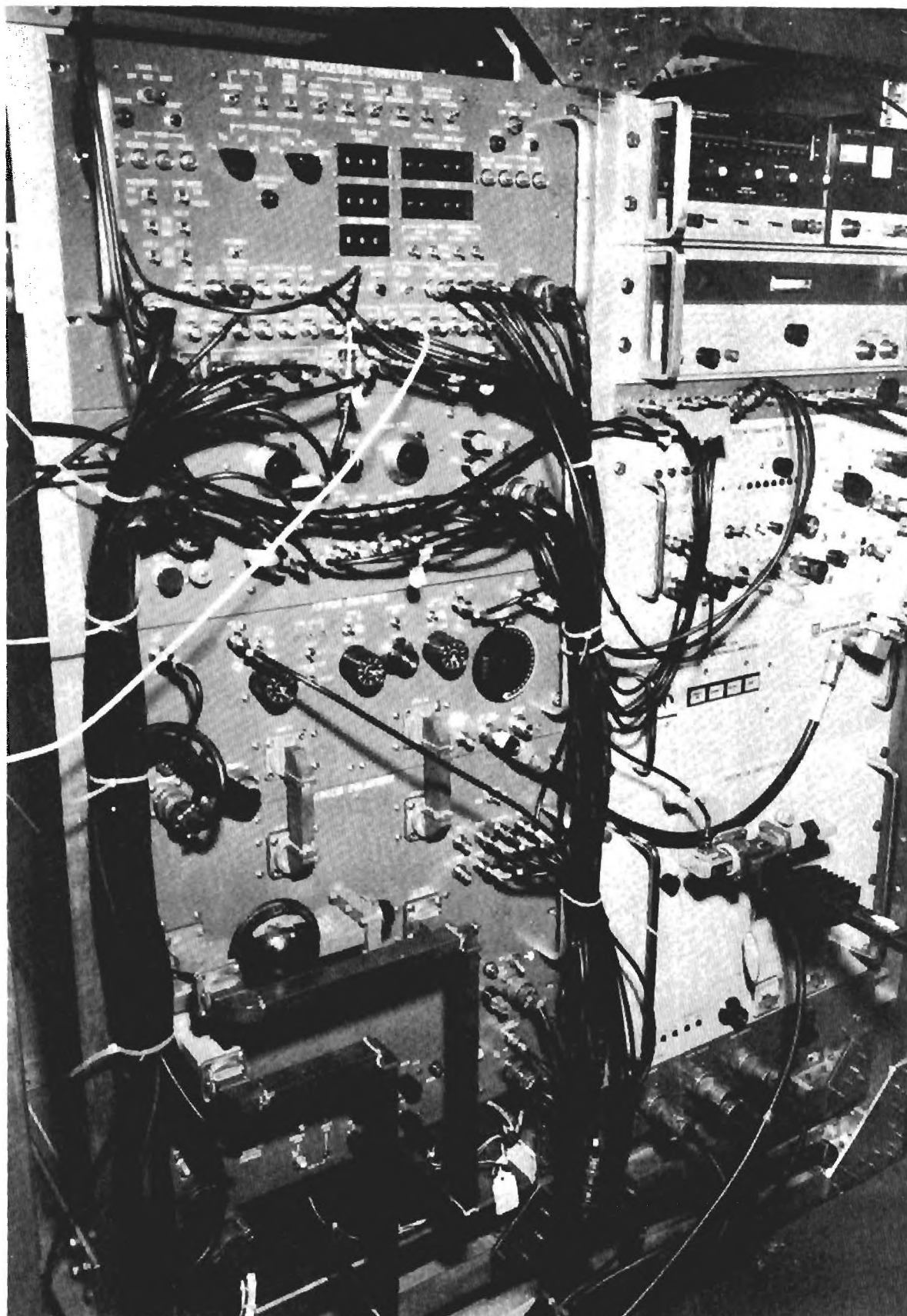


Figure A-8. Prime Equipment

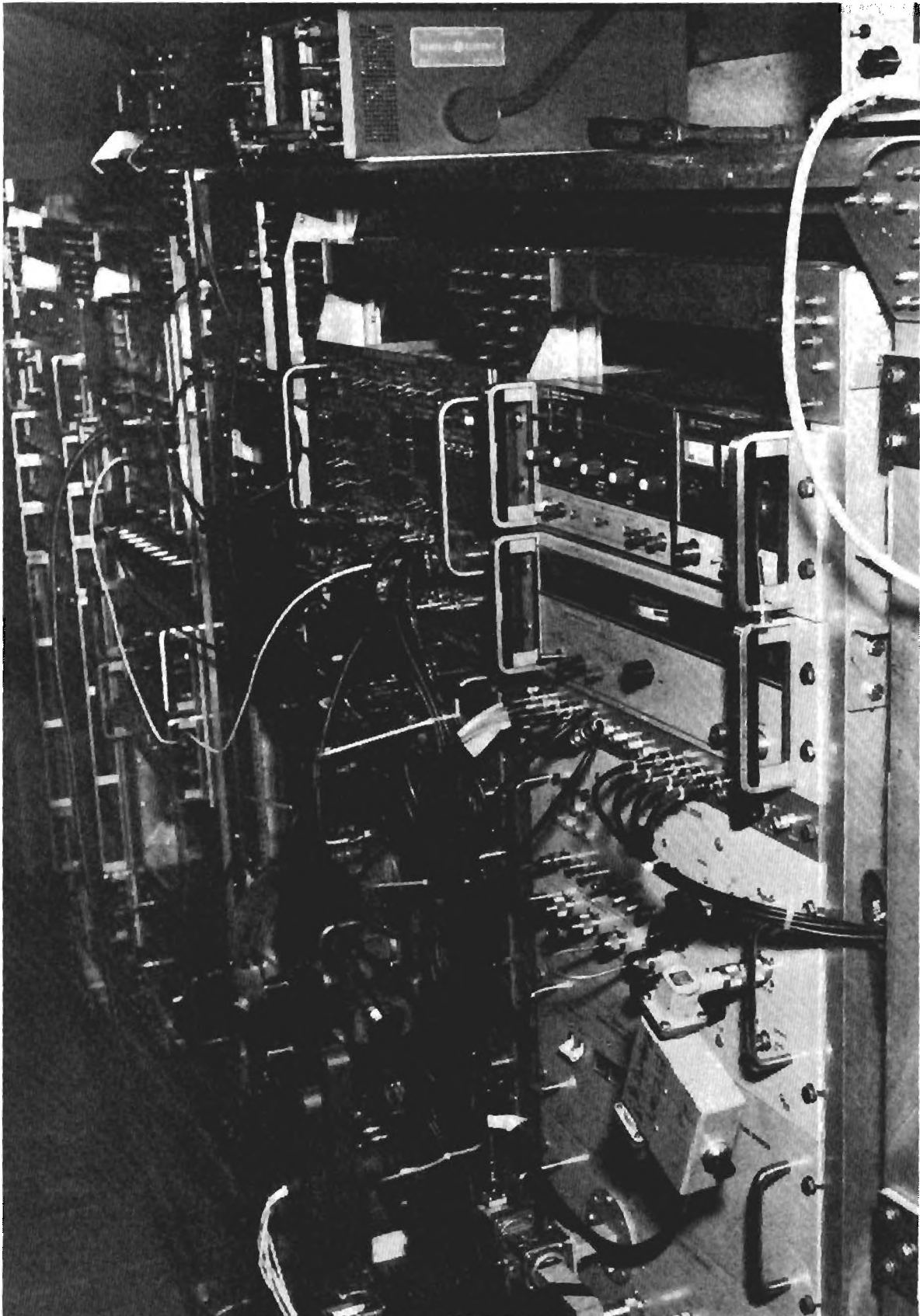


Figure A-9. Complete Equipment Rack

Operation and Maintenance (Volume III of V)
EES/GIT Project A-1871

ADAPTIVE POLARIZATION ECM

Contract Number F33615-76-C-1250
Subcontract Number 1-A-1871

November 1979

Prepared for

U.S. Air Force Avionics Laboratory
Wright-Patterson Air Force Base
Ohio 45433

Prepared by

General Electric Company
Aircraft Equipment Division
Utica, New York 13503

FOREWORD

This is the first of three volumes prepared by GE/AESD covering the operation and maintenance of the Adaptive Polarization ECM system. Functional descriptions of the APECM and test operating procedures are described in this volume.

Volume III covers the functional descriptions of the APECM and its test operating procedures.

Volume IV covers the drawings used in the APECM.

Volume V covers the system specification of the APECM.

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SECTION I

DESCRIPTION OF EQUIPMENT

A. Physical Characteristics

The APECM equipment is contained in seven (7) 19-inch rack mounted drawers. With the exception of the CW TWT amplifier, all of the drawers are attached to the rack with chassis slides. The CW TWT amplifier is supported by aluminum angles.

Table 1-1 tabulates the physical specifications of the equipment.

Table 1-2 lists the interunit cabling.

Figure 1-1 is a complete system interunit cabling and wiring diagram.

The APECM System has the following characteristics:

Figure 1-2 shows the APECM system mounted in its flight qualified racks (less interunit cabling).

Figure 1-3 is a front view of the Processor-Converter.

Figure 1-4 is a bottom view of the Processor-Converter. (cover removed)

Figure 1-5 is a bottom view of the Processor-Converter (cover removed - Pivoted Predictor Subchassis).

Figure 1-6 is a top view of the Processor-Converter (cover removed).

Figure 1-7 is a front view of the APECM IF Receiver.

Figure 1-8 is a front view of the APECM RF Receiver.

Figure 1-9 is a front 3/4 view of the APECM Polarizer Unit.

Figure 1-10 is a top view (cover removed) of the Polarizer Unit.

TABLE 1-1. PHYSICAL CHARACTERISTICS

Unit	Panel Height	Drawer Depth Behind Panel	Weight	Primary Power 400 cps
APECM Processor-Converter	10.5"	21"	56#	None
IF Receiver	7.0"	20"	52#	1 ϕ 520 VA
RF APECM Receiver	7.0"	20"	42#	1 ϕ 115 VA
APECM Polarizer	12.25"	23"	78#	1 ϕ 345 VA
APECM Transmitter Driver	8.75"	18"	55#	1 ϕ 175 VA
Model 624 Pulsed Microwave Amp	7.0"	18"	60#	3 ϕ 565 VA
APECM CW Amplifier	14.0"	20"	103#	3 ϕ 2250 VA
		Totals	446#	3 ϕ 2250 1 ϕ 1720

TABLE 1-2. INTERUNIT CABLE LIST

<u>TO</u>	<u>FROM</u>	<u>COMP TYPE</u>	<u>COMMENTS</u>
<u>RF RCVR</u>	<u>PROCESSOR</u>		
AFC-1 IN	VCO 1	BNC	
AFC-2/3 IN	VCO2	BNC	
SIGNAL	SIGNAL X	MW	
<u>IF RCVR</u>	<u>RF RCVR</u>		
Σ IF IN	Σ IF OUT	BNC	} 50Ω , MATCHED LINE LENGTHS
Δ IF IN	Δ IF OUT	BNC	
<u>RF RCVR</u>	<u>POLARIZER</u>		
Σ RF IN		WG	} MATCHED LINE LENGTHS
Δ RF IN		WG	
<u>AUX RCVR</u>	<u>RF RCVR</u>		
	AUX OUT TO DRIVER	N	
<u>XMIT DRVR</u>	<u>SIGNAL GENERATOR</u>		
MOD IN		BNC	FM INPUT
<u>IF RCVR</u>	<u>PROCESSOR</u>		
VIDEO SYNC	VIDEO SYNC	BNC	
VIDEO	VIDEO SUM	BNC	
IF Δ	IF DELTA	BNC	} 50Ω , MATCHED LINE LENGTHS
IF Σ	IF SUM	BNC	
AGC	AGC	BNC	
SIGNAL	SIGNAL C	MW	
POWER	POWER	MW	
<u>POLARIZER</u>	<u>POLARIZER</u>		
	X-GAMMA	BNC	
	X-PHI	BNC	
	GATE	BNC	
	CLOCK	BNC	
	REC GATE	BNC	
<u>XMTRS</u>	<u>PROCESSORS</u>		
CW	CW XMIT	BNC	
PULSE	XMIT GATE	BNC	
<u>PROCESSORS</u>	<u>SIGNAL GENERATORS</u>		
SAMPLE GATE		BNC, TTL	
POL MOD - PHI		BNC, ±5V, ANALOG	
POL MOD - GAMMA		BNC, ±5V, ANALOG	

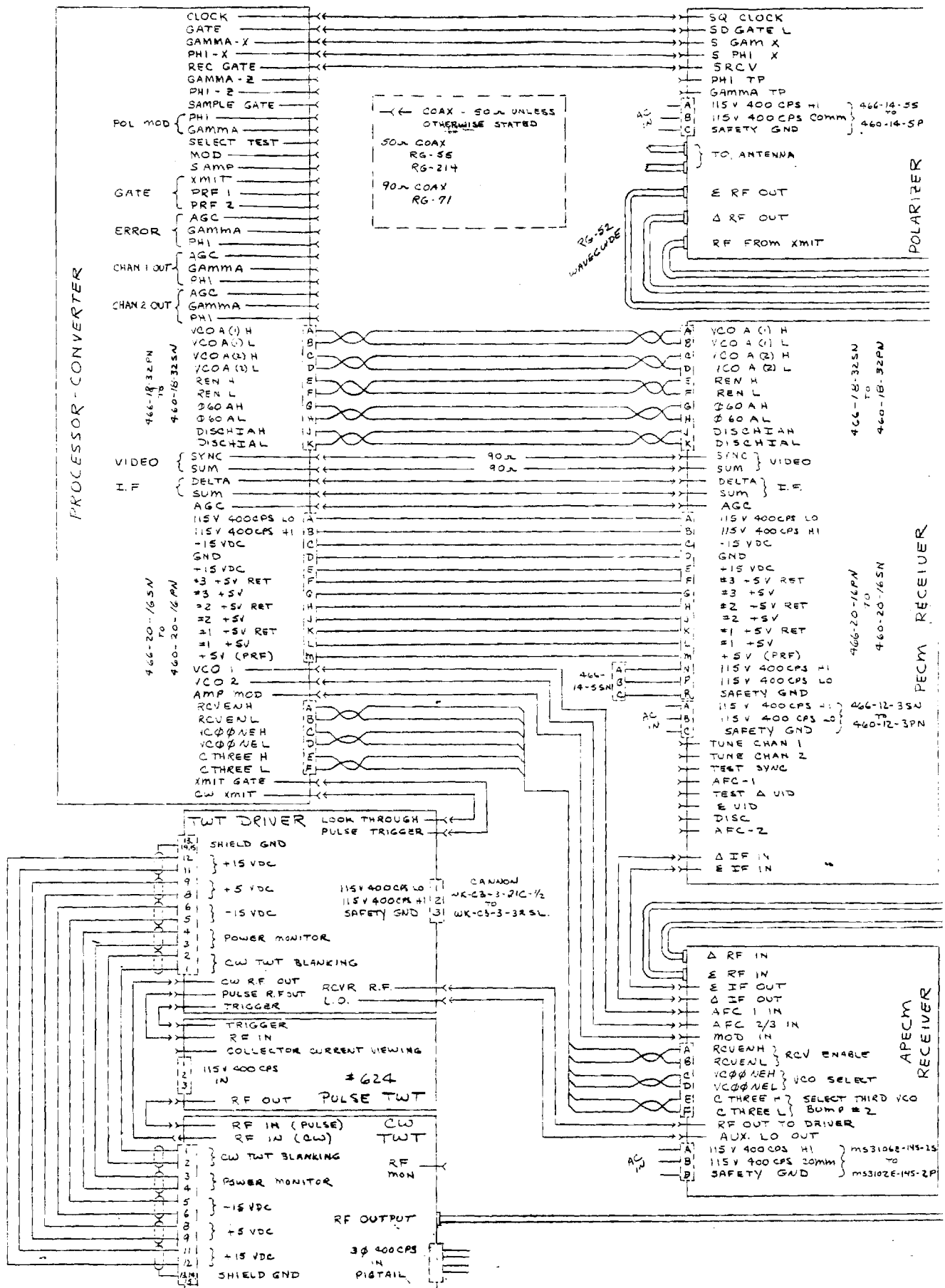


Figure 1-1. APECM Interconnections

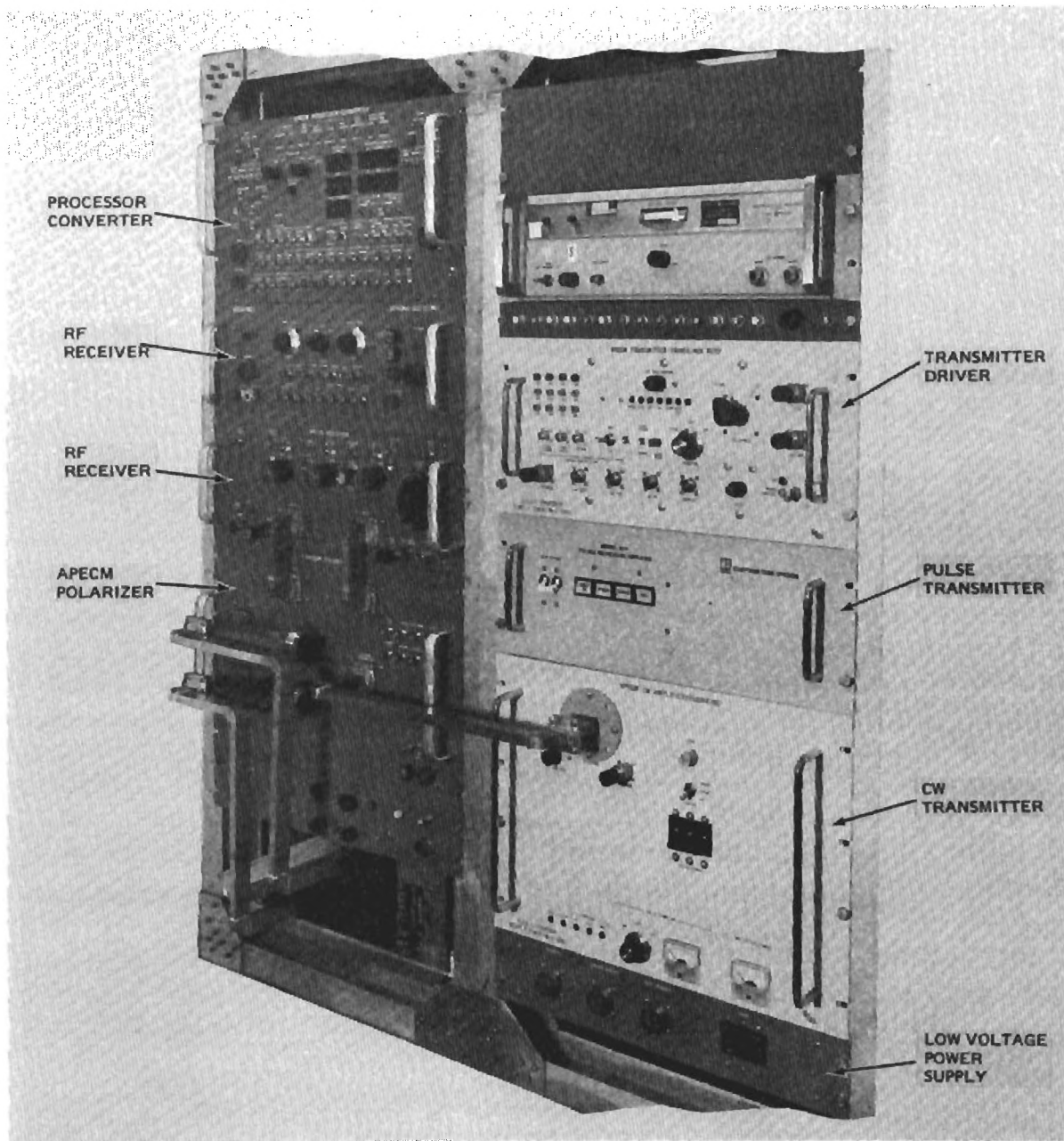


Figure 1-2. APECM System

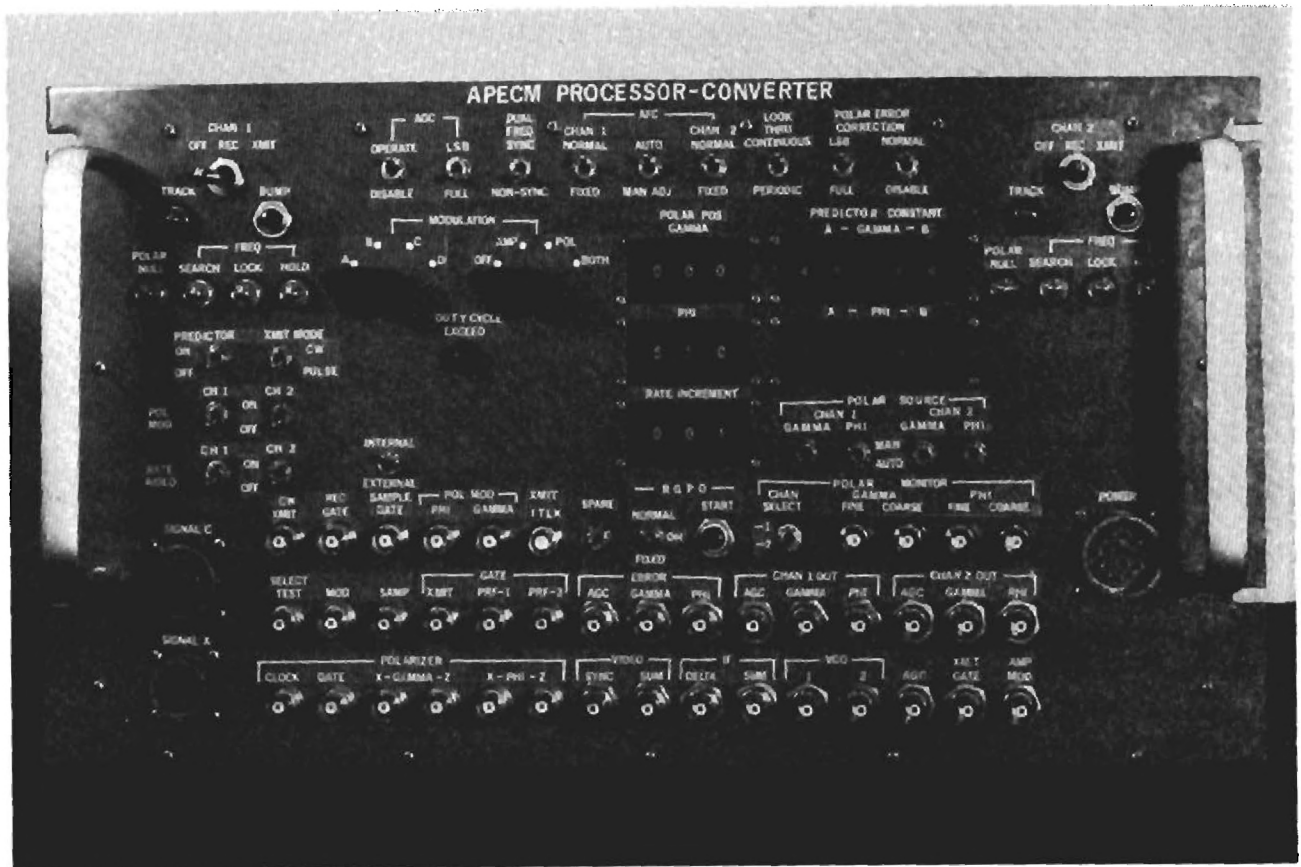


Figure 1-3. Processor-Converter Front View

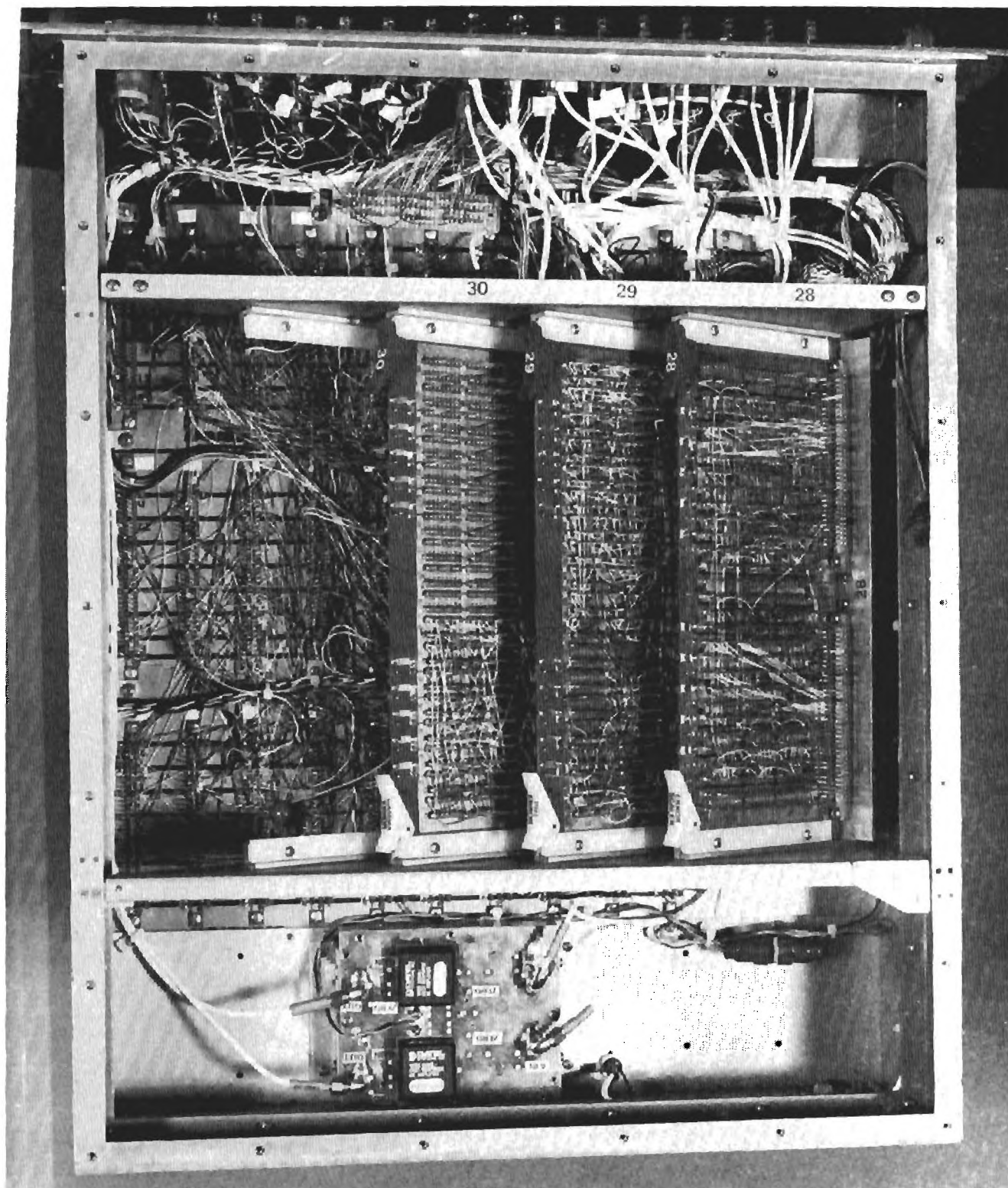


Figure 1-4. Processor-Converter Bottom View
(cover removed)

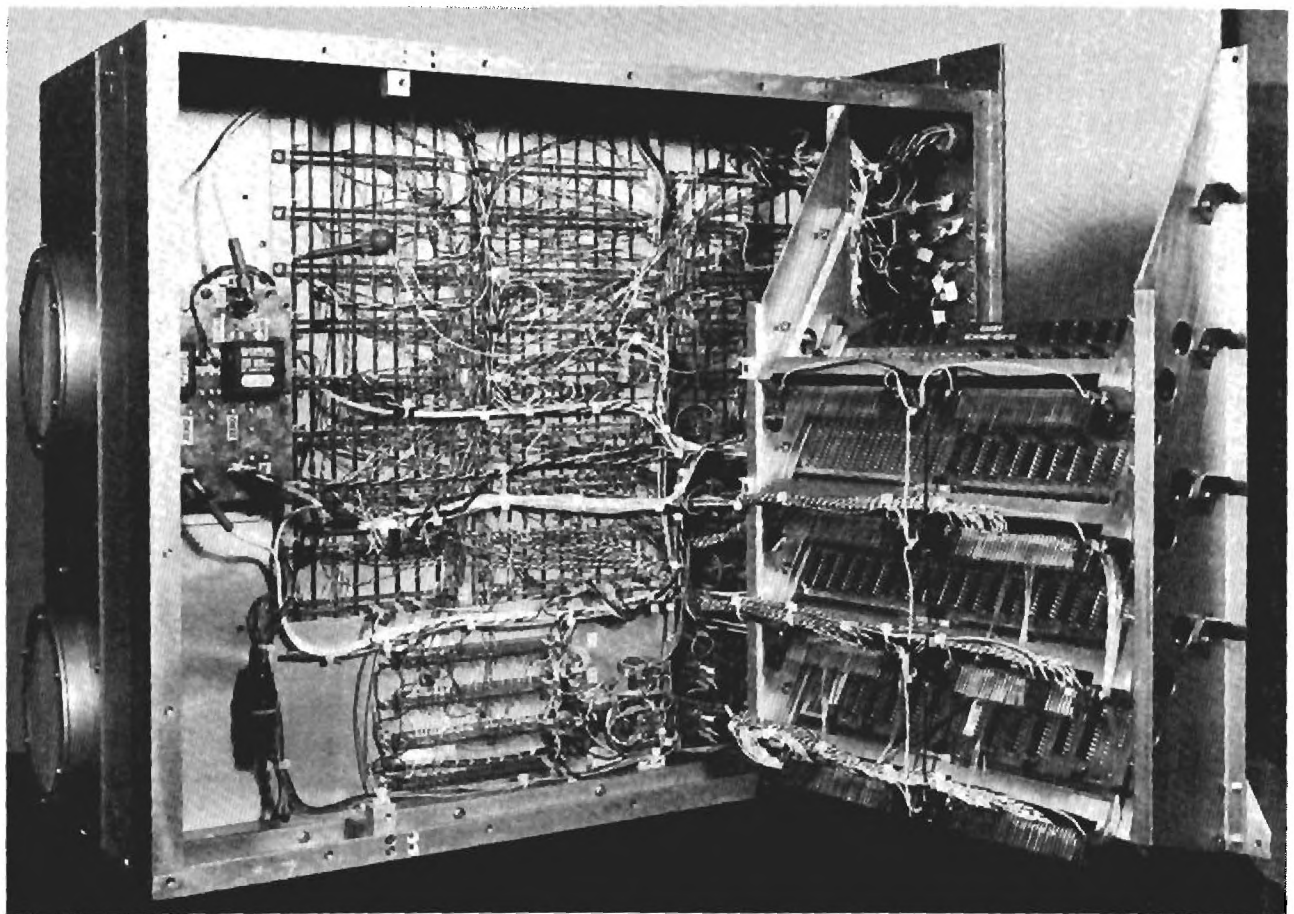


Figure 1-5. Processor-Converter Bottom View - Pivoted Predictor Subchassis (cover removed)

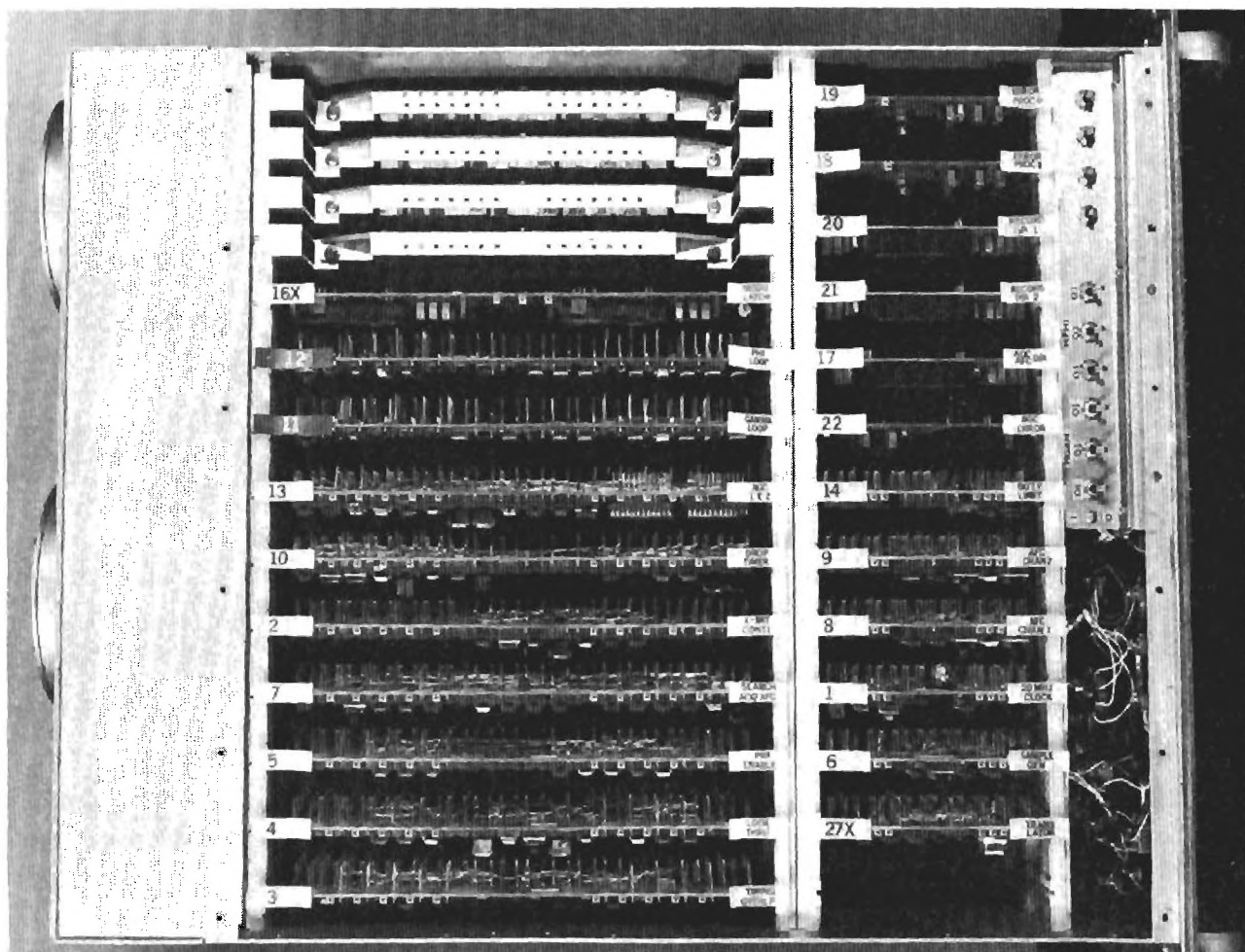


Figure 1-6. Processor-Converter Top View
(cover removed)



Figure 1-7. IF Receiver Front View

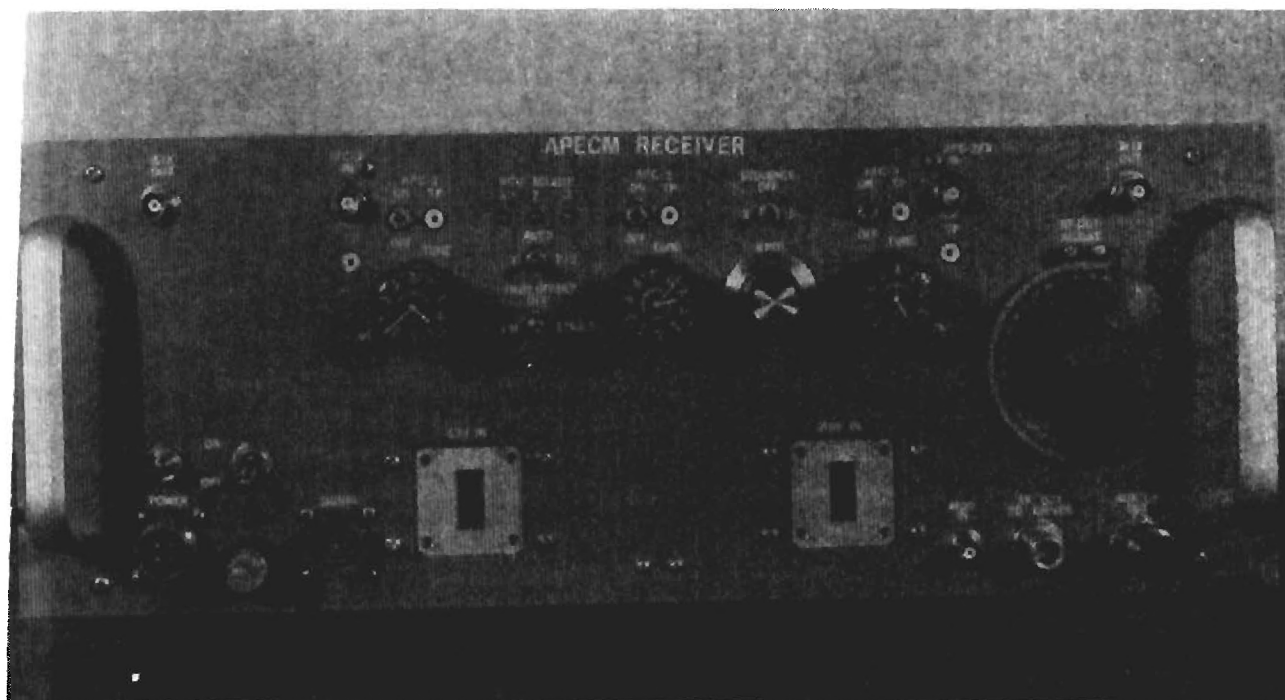


Figure 1-8. RF Receiver Front View

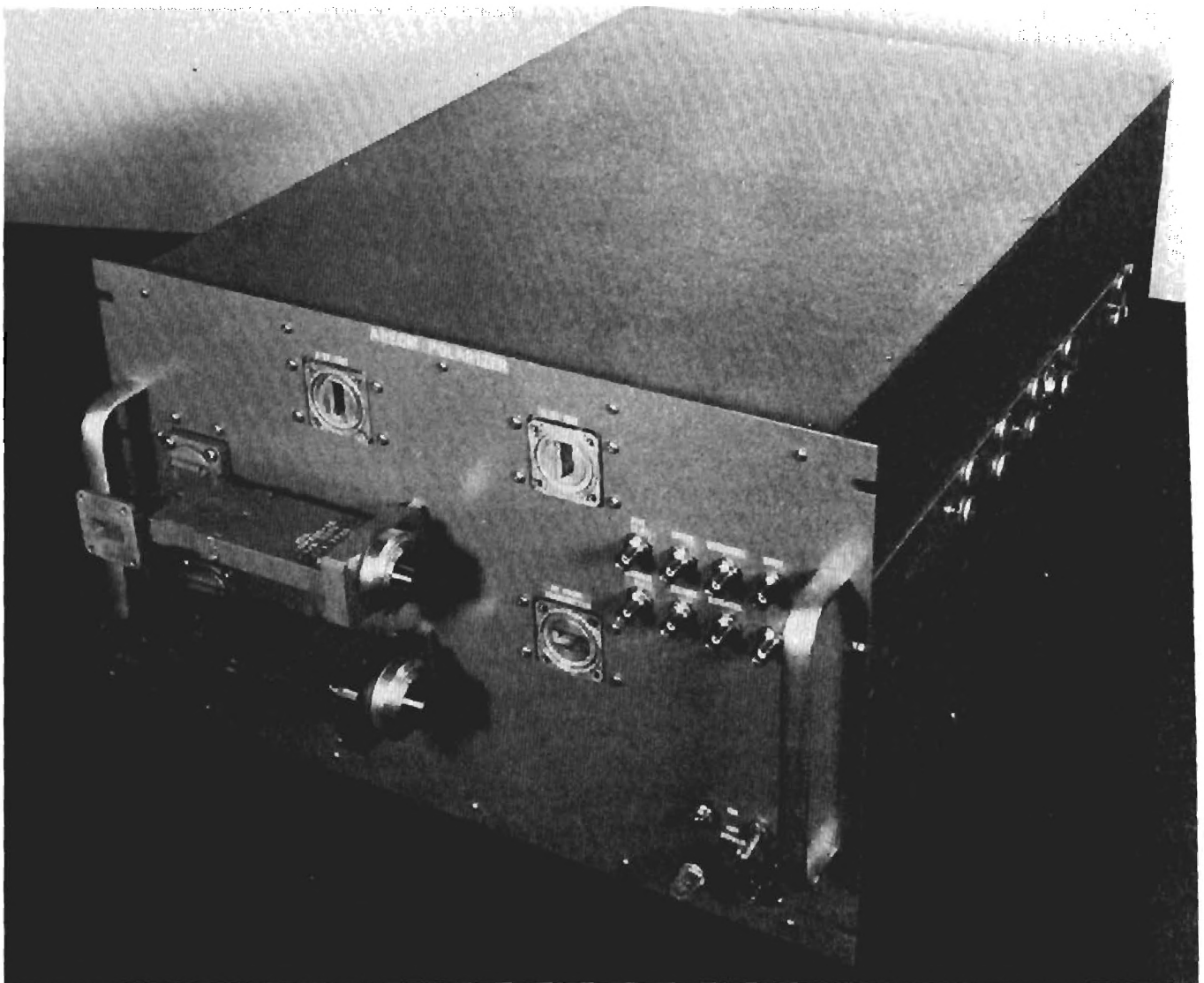


Figure 1-9. Polarizer Unit

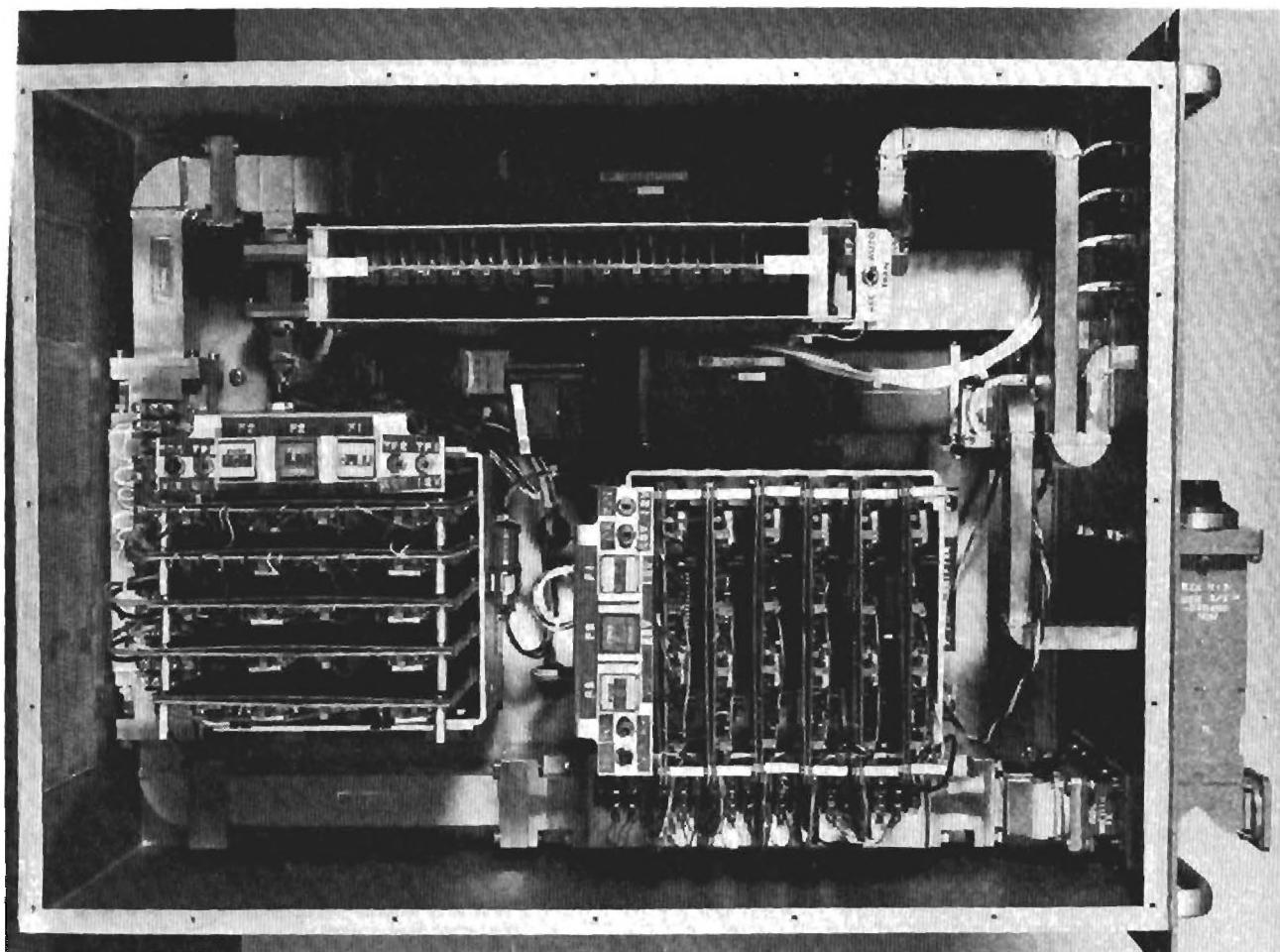


Figure 1-10. Polarizer Unit Top View (cover removed)

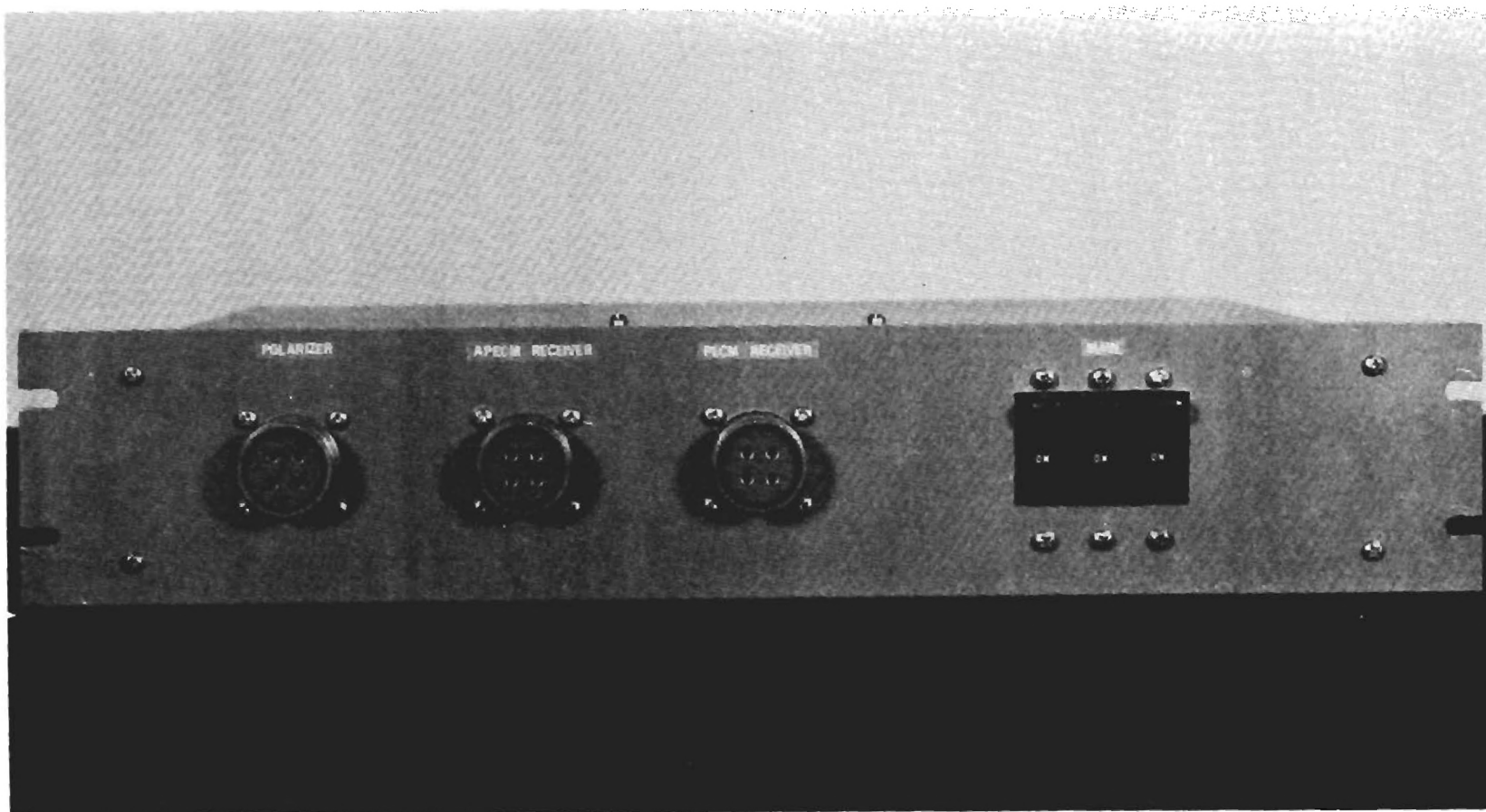


Figure 1-11. APECM LVPS Front View

Figure 1-11 is a front view of the APECM Low Voltage Power Supply.

B. System Description

1. General

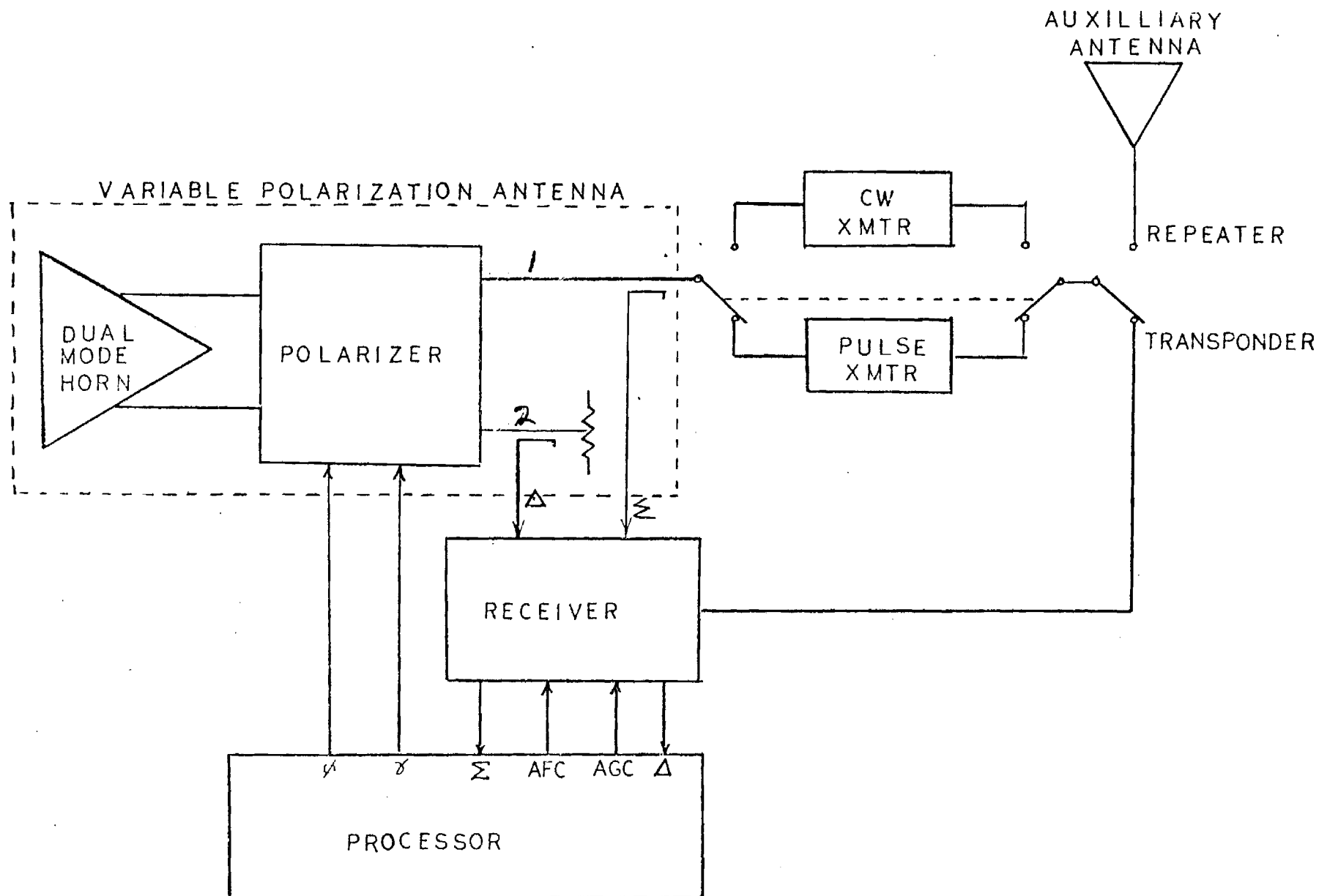
The Adaptive Polarization ECM System (APECM) adds a unique polarization control system to the rejecter/transponder modes of any deception or track-break ECM system. The key to the Adaptive Polarization ECM System, shown in Figure 1-12, is the combination of a dual mode antenna and a polarizer subassembly which is best described as a variable polarization control subsystem.

Very precise polarization measurement of received energy and control of the polarization of radiated energy is possible. Received energy is separated by the orthogonally-coupled dual mode antenna into its two orthogonal components. The polarizer subassembly measures the relative amplitude and phase relationships existing between these two components and permits control of the transmitted energy delivered to these two orthogonal ports such that the desired polarization (relative to the received polarization) can be radiated. Once a signal is being tracked, any error between the polarization of the energy being radiated and the polarization of the energy being received can be measured on a single pulse basis and corrected at electronic speeds.

To measure the received polarization, the polarizer is adjusted so that one of its two output ports (Σ port) is maximized and the other port (Δ port) is nulled. This is accomplished by the dual channel receiver and processor which is coupled to port 1 and port 2 through the transmit/receive couplers. When this condition is realized, port 2 becomes a co-polarized port (energy introduced at port 2 is radiated with the same polarization state as the received energy). Port 1 is a cross-polarized port (energy introduced into port 1 is radiated cross-polarized to the received energy). Since the processor controls the phase and amplitude response of the polarizer, ports 1 and 2 can be programmed to be either (Σ) or (Δ) ports during transmission. Thus either co-polarization or cross-polarization (or other polarization) can be programmed.

Subsequent adjustments of the antenna polarization by the processor will keep this delta signal (Δ) minimized by servo action during receive events. The signal is minimized continuously to compensate for aircraft motion and for received signal polarization changes.

Once the antenna is adjusted so that the (Δ) port has a received signal null, an RF signal transmitted into that port and



on through the antenna subassembly will be precisely cross-polarized to the antenna feed structure emitting the original signal. In the APECM System, the transmitter may be either a pulsed or CW source. One very important property of the APECM antenna system is its reciprocity and its insensitivity to RF power levels. This reciprocity permits the same elements to be employed in the bidirectional operation needed for Receive/Transmit functions.

2. Theory of Operation

a. General

A more detailed block diagram of the Adaptive Polarization ECM (APECM) System is shown in Figure 1-13. The system may be configured for either repeater or transponder operation, depending on the Transmitter Driver input. Cabling changes can also be made so that either the Pulse or CW Transmitter supplies the RF power.

The Polarizer consists of four phase shifter devices, two hybrids, two couplers to supply the receiver, phase shifter driver assemblies, interface logic, and 400 Hz power supplies. The ferrite phase shifters, their drivers, and the hybrids were supplied by Raytheon and subsequently modified by General Electric for required phase accuracy. The interface logic converts the serial phase shifter commands derived in the processor into a parallel form for further use by the phase shifter drivers. The interface logic also contains ultra-violet erasable programmable read-only-memories (UVEPROMs) for code conversion between the processor and phase shifters.

The RF Receiver contains a dual-channel superheterodyne receiver and a frequency offset generator (FOG). The two Voltage-Controlled Oscillators (VCOs) may be manually preset to the threat frequencies, and then switched to automatically track the threats using the automatic frequency control (AFC) system. VCO switching is controlled by the processor so that two interleaved pulse trains from two threats may be countered simultaneously. One of the VCOs may be set to track two different threat frequencies and automatically switched between the two frequencies at a slow rate (approximately 0.1 - 1 Hz). In this manner, three threats may be handled sequentially, with the system responding to threats 1 and 2, then 1 and 3, then 1 and 2, etc. The LO energy is sampled and made available to the Auxiliary Receiver and to a Frequency Offset Generator (FOG). The FOG produces an RF signal at the threat frequency by combining the sampled LO signal and either of two 60-MHz oscillator outputs. One of the 60-MHz oscillators is crystal-controlled, while the other is voltage-controlled and may be driven by an external function generator to produce a frequency modulated output. The

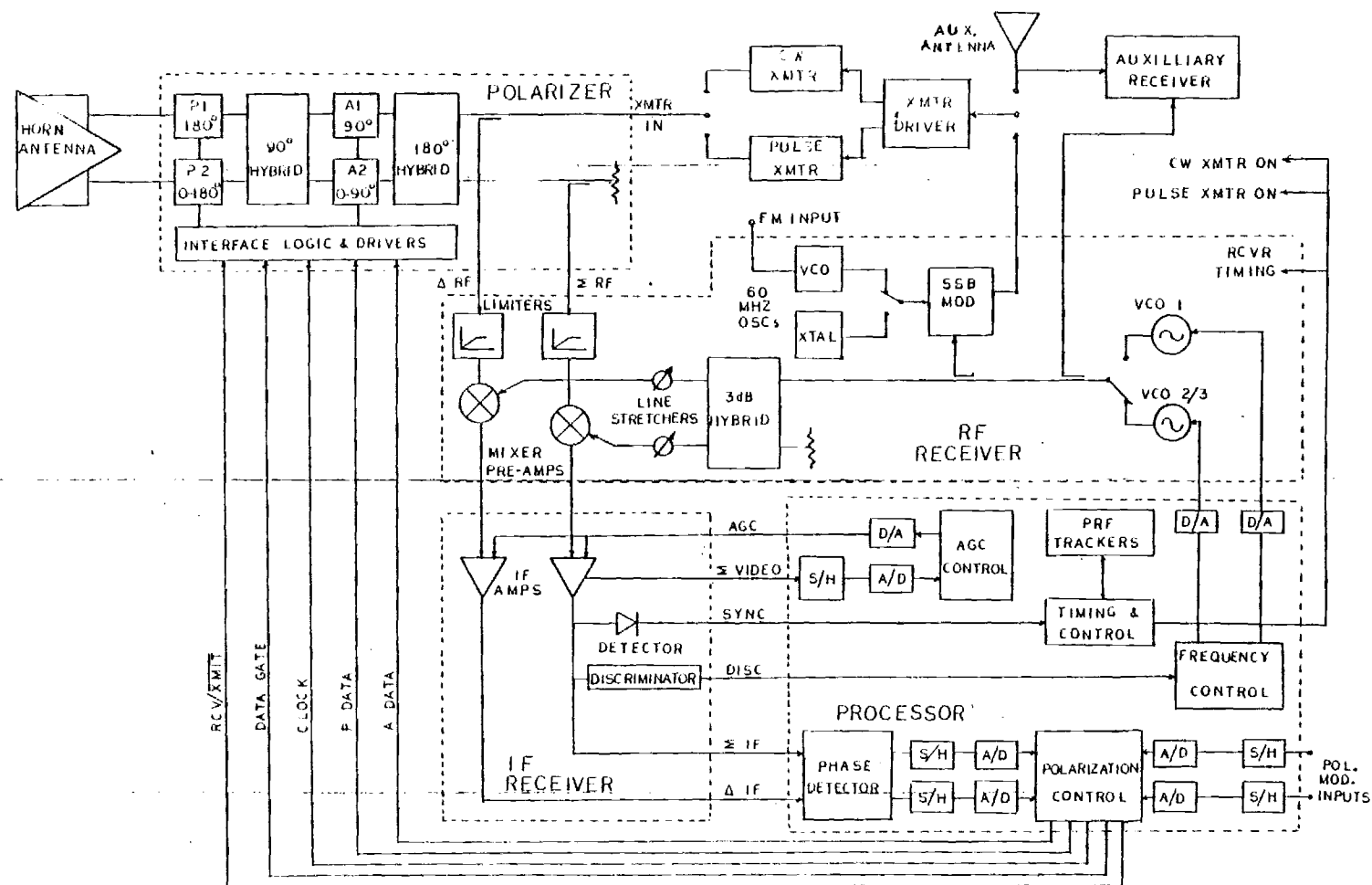


Figure 1-13. Detailed System Block Diagram

mixer-preamplifiers are protected by limiters from excessive RF input levels. Line stretchers provide a means of balancing the phase delays in the LO lines and the sum (Σ) and delta (Δ) IF channels.

The 60-MHz components in the Polarization ECM receiver were developed on a previous polarization contract. IF and video outputs are provided for the polarization control I and Q detectors, the AFC and AGC circuits, and the PRF trackers. The IF Receiver also contains the low voltage power supplies for the Processor-Converter logic.

The Processor-Converter contains all the logic to acquire, track, and respond to two simultaneous threats. The Processor functions include automatic gain control of the IF amplifiers, automatic frequency control of the VCOs, automatic polarization control, PRF (Pulse Repetition Frequency) tracking, transmitter ON/OFF control, and the timing and control required to time-share these functions between two threats.

Once the threats have been acquired, the PRF trackers provide an anticipation pulse prior to the arrival of a radar's pulse. This anticipation pulse is used to time the setting of: the gain of the amplifiers, the polarization of the antenna subassembly, and to select the LO for the mixers. Once the radar pulse arrives, as indicated by the receiver detected video, the information (AFC, AGC, and Polarization error) is sampled and the values to be used on the next pulse are calculated. The receiver gain, frequency, and polarization information is stored in digital registers for both threats being countered and used and updated on an interleaved basis.

Updating of the tracked parameters (receiver gain, frequency, PRF, and polarization) is done on a lookthrough basis. Currently, the hardware samples these parameters on one pulse in three, and transmits on two out of three. Amplitude, frequency, and polarization may be modulated during the transmit events.

b. System Operation

(1) Acquisition

Acquisition is the process of establishing the initial frequency, amplitude, polarization, and PRF of a threat on one of the two threat channels. The parameters of the signals that can be acquired are given in the following paragraphs. Acquisition is initiated by selecting a channel for the threat to be countered and manually tuning its frequency with the appropriate control CHAN 1 TUNE or CHAN 2 TUNE potentiometer) on the RF Receiver front panel. The frequency must be manually tuned to within 16 MHz of the threat frequency.

To handle dual frequency radars or radars which are synchronized in PRF, the APECM Processor-Converter "Dual Frequency" SYNC/NON-SYNC switch must be in the SYNC position which permits sharing a PRF tracker between the two two-receiver channels on an interleaved basis. In this mode, the frequency of each RF Receiver LO must be preset to its assigned frequency using two of the front panel "Tune"(1) controls. For normal operation the "Dual Frequency" switch is left in the NON-SYNC position.

To limit the acquisition process to radar main lobes (to ease the sorting problem and to prevent distant radars from being acquired), the AGC control on the Processor-Converter is set to OPERATE and the GAIN switch on the IF Receiver is set to AUTO. The receiver sensitivity is automatically set to -15 dBm. The LSB/FULL AGC switch selects the mode of AGC to be used. Either position is acceptable for acquisition, although "Full AGC" position should reduce acquisition time.

For normal acquisition, the two "POLAR ERROR CORRECTION" switches should respectively be in the FULL and NORMAL positions.

Acquisition is initialized by placing the switch for the selected channel (CHAN 1 or CHAN 2) located in the upper right or upper left corner of the APECM Processor-Converter in the REC position. Setting the appropriate switch performs several functions: it sets the initial acquisition polarization value into the polarizer and sets the initial or acquisition mode gain setting into the receiver. The logic is also enabled to receive and sample on the channel selected.

Following initialization of the acquisition process, the VCO is swept through a 32 MHz frequency band in search of the received signal. This band is centered about the manually selected frequency. Upon receipt of a pulse, at least 0.25 μ s wide, within 4.5 MHz of the tuned LO value, and above -15 dBm amplitude, the receiver will develop a pulse present sync signal to the processor. The timing control logic of the processor stops the frequency scan and looks for several pulses on which to establish a PRF track. After PRF track is established, it starts the frequency, gain, and polarization servo process.

(1)The three "Tune" controls on the RF Receiver should not be confused with the two tuning controls on the IF receiver labeled "Channel 1 Tune" and "Channel 2 Tune".

With PRF track established, the TRACK light will illuminate. When the received frequency is servoed to the center of the IF strip and has settled there, the FREQ LOCK light will illuminate. When the polarization separation of the antenna assembly and the received signal is within the preset tracking limits, the POLAR NULL light will illuminate, signaling completion of the acquisition process.

Frequency search will be resumed during acquisition under two conditions. The first is when after 14 ms of the receipt of a pulse present sync signal the PRF has not been established. For instance, in the event of a random pulse or noise spike, the tuning would be stopped for a 14 ms period, but start again when a regular PRF is not established. If, after PRF track is established, the frequency servo is unable to tune the signal to the center of the IF passband within a preset time period, the VCO is advanced about 9 MHz and the search and acquisition process resumed. This feature is included so that during acquisition the improper sideband of the receiver can be recognized and rejected. During frequency search, if the image response of the receiver is detected, the normal AFC process will drive the receiver back off the radar signal and the search and acquisition process would never be completed. This special sideband reset circuit allows a limited time period after PRF track is established to obtain frequency lock. If frequency lock is not obtained, the LO is slewed through the image response.

Acquisition can also be reinitialized by pushing the BUMP button on the processor panel. Tracking is dropped when this button is pushed, the frequency advances, and search is resumed from that point.

When three threats are being handled sequentially, the automatic VCO switching between the second and third threats effectively causes a BUMP of processor channel 2. That is, each change from one threat to the other resets all channel 2 tracking information, and the acquisition process is reinitialized on channel 2.

(2) PRF Track and Timing

There are two PRF trackers in the system and a time multiplexer coordinates their functions. All other timing is based on pretriggers generated prior to the arrival of a pulse by the PRF tracker selected by the time multiplexer.

The PRF trackers have the following specifications:

Rates	725 to 3000 pps
Stagger	20% maximum

Number of Steps
of Stagger 2

Stagger implies that the pulses are not equally spaced in their occurrence but that the process is periodic. Two step stagger indicates there are two different step sizes used and that every two pulses a given period repeats.

To accomplish tracking of staggered pulses, each tracker has two "halves". One half tracks every other pulse and the phasing between the tracker determines the stagger. Figure 1-14 shows the "a" and "b" pulse trains of the trackers each interleaved with the other.



Figure 1-14. Stagger Pulses Tracked by Two Halves of a PRF Tracker

The tracker periodically looks to see whether the PRF has been doubled or if it has mistakenly picked up a half rate pulse train. Since there may be stagger on the doubled frequency, the tracker sweeps its gate over the 20% stagger region during the checking process.

The PRF tracker times the pulse arrivals using a 5 MHz clock. The tracker generates a pretrigger 65.8 μ s prior to the next predicted pulse. System timing uses this pretrigger to control subsequent events.

System timing takes this PRF pretrigger and enables the loading of the correct polarization into the polarizer 20 μ s prior to a predicted pulse. The other processes, i.e., loading the gain value in the receiver AGC and selecting the LO, occur about 10 μ s prior to a predicted pulse. 0.8 μ s after all processes are performed the receiver switch is opened and ready to receive a pulse.

The receive gate generated by the system timing logic is available at a test point on the front panel of the Processor-Converter. The test point, labeled GATE PRF 1 (or 2) goes to a logic "1" state whenever the channel is enabled. During tracking, it is enabled about 6 μ s prior to the predicted receipt of a pulse.

When a channel is enabled, the amplitude (AGC) and polarization error analog circuits are placed in a sample mode. The sample pulse for the polarization error measurement is available on the Processor-Converter front panel as a test point labeled SAMP. About 200 ns after a pulse is received, SAMP will return to the hold (logic level 1) state.

If the channel control switch is in the XMIT position, then on two out of every three pulses, the pulse transmitter is enabled about 2 μ s prior to the incident pulse. This transmit mode is obtained when the LOOK THRU switch on the Processor is in the PERIODIC position. The CONTINUOUS position is used during system checkout and forces all pulses or events into the receive mode.

The frequency of update of one in three is referred to as the "lookthrough" rate because the receiver "looks through" the jamming at those times. The lookthrough rate can be changed in the logic, but it must always be set to an odd number. This restriction is due to the fact that only one half of the PRF tracker would be updated if lookthrough occurred on an even numbered pulse count.

If PRF track is lost for any reason, the system maintains a hold on the radar parameters for a 2 μ s period. This function, called dropout timing, prevents the temporary loss of signal from aborting an on-going acquisition or track process and causing the reinitiation of acquisition. During available periods of time when the other channel is not using the system, the last measured values of polarization, gain, and frequency are used with the enabled receiver. If the pulse train reappears, PRF track is reestablished and transmission is resumed.

If PRF track is lost for more than 2 μ s, the gain reverts to the search mode value, and polarization reverts to acquisition value. Frequency control normally reverts to search mode. A mode of operation is optional where the frequency is retained for the initial acquisition sequence. When this mode is selected, the FREQ HOLD light on the front panel lights up along with the FREQ SEARCH light. The BUMP switch can be used to override the FREQ HOLD mode and start frequency search operation again.

(3) Frequency Control

Frequency control for both receive and transmit is provided by a closed loop Automatic Frequency Control (AFC) servo. The controlled variable is a voltage-controlled oscillator. The VCO tuning error is sensed by the IF discriminator during the received pulses. The transmitted signal is derived from the VCO by translating the frequency. It can be

accurately maintained within ± 200 kHz of the received signal frequency.

There are two VCO channels in the system as shown in Figure 1-15. Each one is assigned to a given channel for multiple threat operation. The operating frequency range for each VCO controlled by a multiturn pot on the front panel of the RF receiver. The receiver frequency as a function of the dial reading is given in Figure 1-15. When initiating acquisition, the desired frequency should be set on these potentiometers.

The second VCO line is shared by two VCO's, #2 and #3. Selection of VCO 2 or 3 may be done manually or automatically on a time-shared or sequential basis.

Once a signal present signal is detected automatic control starts, and the VCO frequency is modified by the AFC logic to accurately track the frequency of the received signal.

Upon receipt of a pulse, the receiver discriminator determines whether the VCO frequency is high or low. The discriminator output is available as a test point (AFC-1) on the IF receiver. The calibration curve of this test point is given in Figure 1-16. This data is digitized as a one bit number prior to going to the processor on a signal cable. That is, the only information retained is whether the LO is high or low with respect to the received signal.

The processor multiplexes this signal to the proper one of the two channelized frequency registers by counting the appropriate register up or down one count. Upon receipt of the next pretrigger from system timing, the corrected register value is read into the D/A and the VCO frequencies will be changed approximately 62.5 kHz (mean resolution of one LSB). Thus, for a 4 MHz error, the system requires approximately 64 update pulses to drive the VCO into a no error condition.

The controls for this frequency servo process are on the front panel of the processor. The logic loop readout to the VCO is enabled when the AFC AUTO/MAN ADJ switch is in the AUTO position. MAN ADJ position is used for setting the VCO to the center frequency manually. The AFC CHAN NORMAL position allows the discriminator error to update the internal register. In the AFC FIXED position, the last value in the register is frozen and no updates are permitted.

The values of the correction signals from the processor are available as test points on the RF receiver front panel.

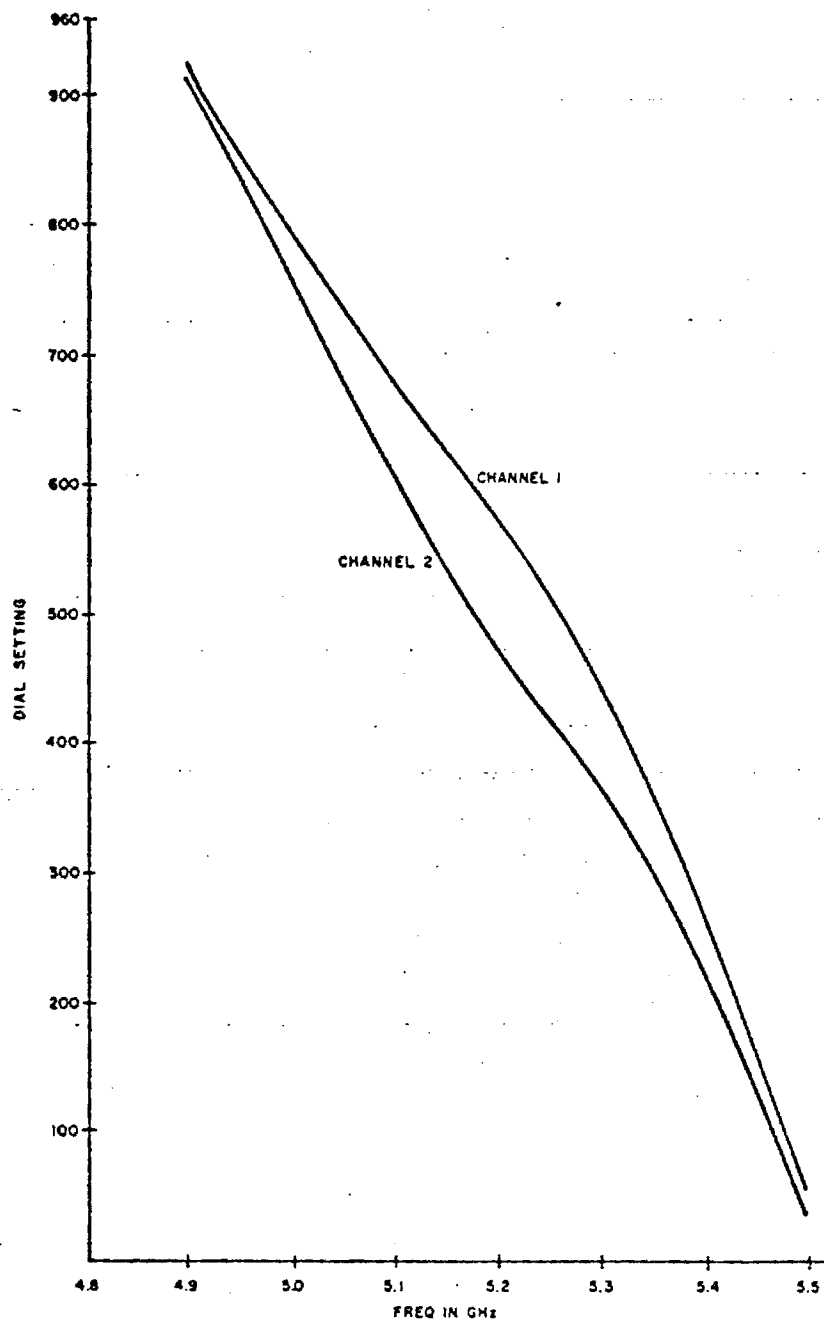


Figure 1-15. VCO Dial Settings

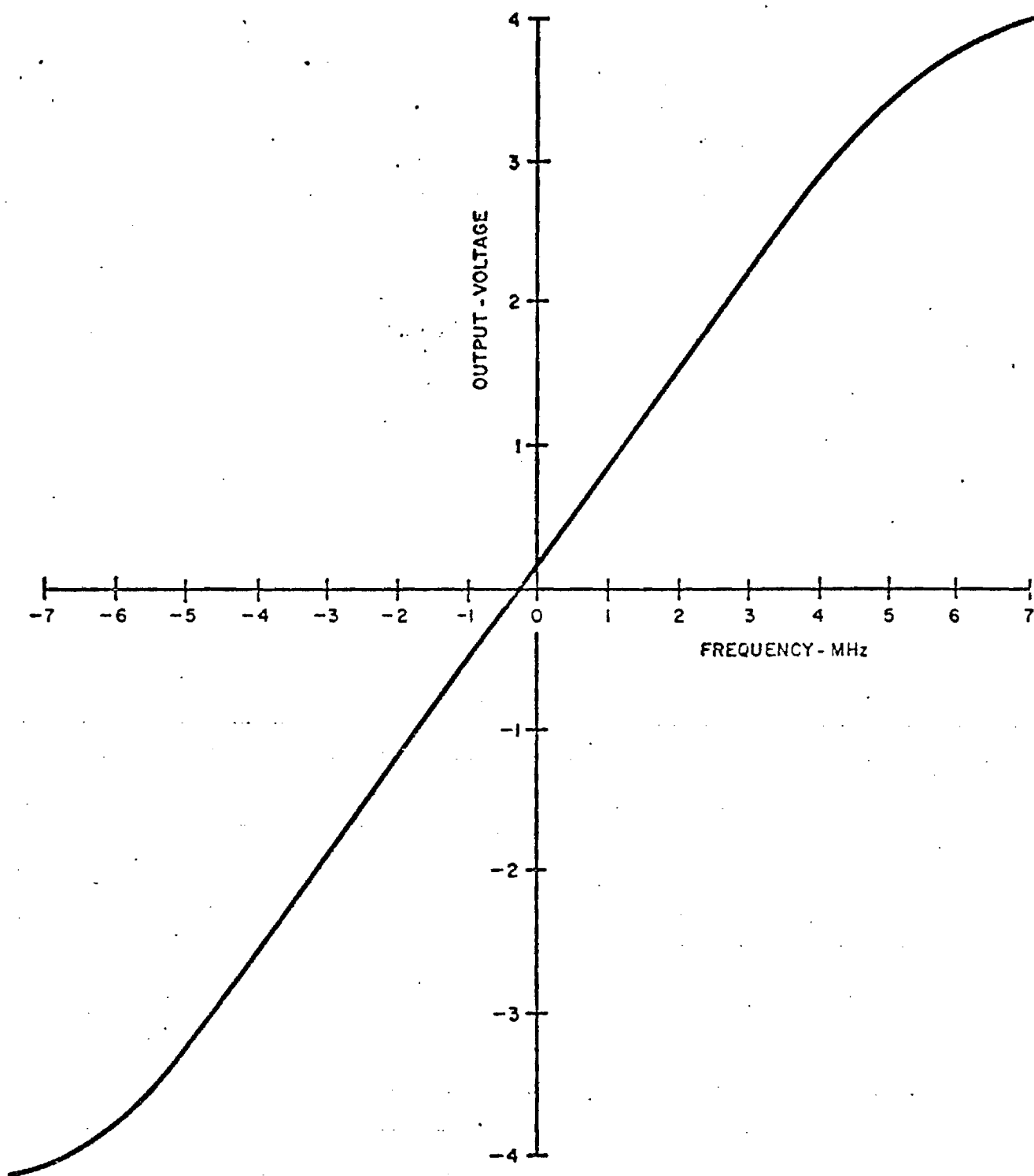


Figure 1-16. Discriminator Test Point Calibration

For multiple threat operation, the logic also selects the correct VCO output signal for the receiver and signal source circuits. Thus, only one VCO at a time is being used during any one event.

During frequency search, the VCO will step 1 (D/A) LSB every 410 μ s. Thus, it takes about 0.2 second to traverse the full 32 MHz search band.

During a transmit event, the correct VCO signal is selected in the same manner as for a receive event. A sample is coupled off and frequency offset by the intermediate frequency to produce the resultant frequency equal to the frequency of the input signal.

In a noise-free analysis, the error in the loop is ± 1 (D/A) LSB or ± 62.5 kHz. In actual operation, the frequency may deviates up to two (D/A) LSB's or ± 125 kHz. The specified ± 200 kHz accuracy allows for ± 3.5 (D/A) LSB variation of the VCO frequency which is adequate for known threats.

(4) Gain Control

The polarization ECM system uses automatic gain control to normalize the polarization error signals. The sum (Σ) channel output is normalized at a fixed level at the receiver output port to simplify the polarization error detection process. Gain control is accomplished via a pair of matched IF gain controlled amplifiers. The gain error is obtained from the sum channel video output, and the processor circuit controls the gain settings of the amplifiers.

Two matched amplifiers are used in the sum (Σ) channel and difference (Δ) polarization channel. Both channels are maintained in gain balance.

The sum and delta video signals are available as test points on the IF Receiver front panel. The Σ video pulse amplitude is given by Figure 1-17.

The Σ channel video signal is cabled to the Processor-Converter, where it is sampled and held and is available as a test point, ERROR AGC. The calibration of this test point is also shown on Figure 1-17. The logic controls the gain to keep this test point voltage at 4.05 V.

The amplitude information is converted to digital form and linearized to compensate for the curve in the data in Figure 1-17. The error of the Σ video signal from the desired level is multiplexed to one of the two channelized gain control registers in the processor and is used to update the gain control register.

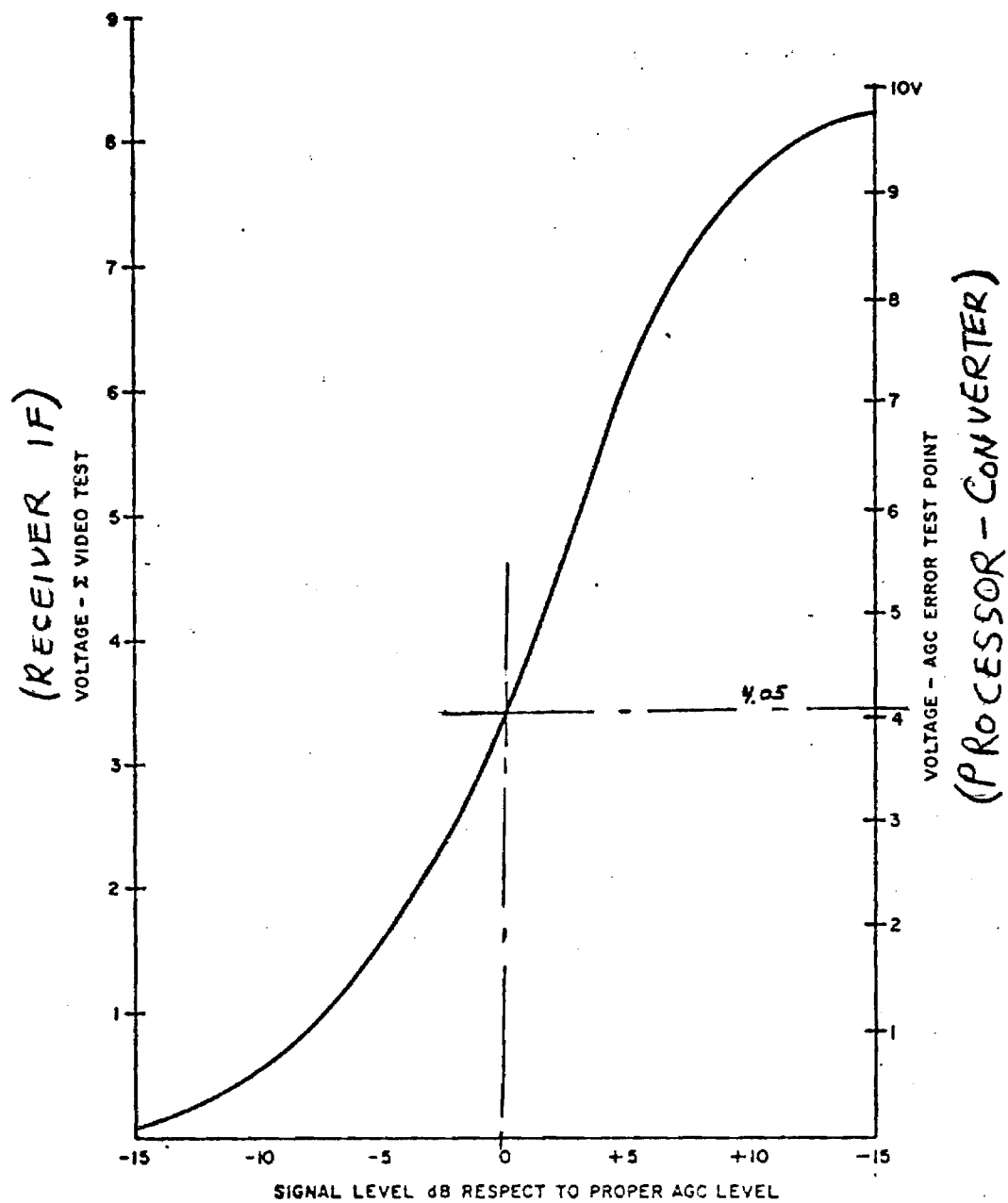


Figure 1-17. Calibration of Sum and Delta Video Test Points

Whenever a receive pulse is due, the gain value in the appropriate register is converted to an analog voltage and applied to the receiver IF amplifiers. The value of gain currently used is available as a front panel test point CHAN OUT AGC. The test signal here is a 0 to 10 V representation of the internal gain register. The calibration is linear with a 6.4 dB per V slope. An AGC signal of 0 V corresponds to a nominal -39 dBm signal received on the antenna terminals of the polarizer. A 10 V signal represents a nominal +25 dBm signal.

Control of the system gain and AGC is performed from the front panels of the equipment. A manual gain control provision (GAIN/MAN or AUTO) is provided on the IF Receiver front panel. This control has both a switch and potentiometer function. In the AUTO position, the potentiometer is out of the circuit and the processor controls receiver gain. In the MAN position, the smaller concentric dial is engaged and manual gain control is available.

Manual gain control is considered a troubleshooting mode and is uncalibrated.

Normal AGC operation is controlled from the processor front panel. In the DISABLE position of the (AGC/OPERATE-DISABLE) switch, the gain setting is frozen at its last value and in the OPERATE position, full AGC functioning is enabled.

The (AGC/LSB-FULL) switch allows two different methods for updating the gain value register. In the LSB position, the gain is corrected by 1/4 dB on each received pulse. For large initial errors in gain, the system will take several pulses to normalize. In the FULL position, a one pulse correction will be made in amplitude using the full error as measured by the receiver AGC error detector.

During acquisition, the gain control loop is opened and a fixed gain inserted into the IF amplifiers to give a pulse present on a -15 dBm or greater signal. Following receipt of five tracking pulses, the gain loop is closed and AGC operation takes over.

When a signal drops below -35 dBm at the input, the AGC value is no longer updated, and the received signal is allowed to drop in amplitude. Following the loss of signal, the AGC will hold its last value for 2 seconds and then revert to the acquisition gain setting.

(5) Two Threat Operation

Operation against two threats is possible by interleaving the transmission against the two threats on a pulse-to-pulse basis. The receiver, processor, transmitter, and polarizer are available to each radar for interleaved 30 μ s segments of time.

In the event that the two threats are pulse synchronized and overlap, an alternate mode of operation is used with special timing enabled by a front panel switch. These two modes, non-synchronized and synchronized, are described below.

(a) Non-Synchronized Threats

Non-synchronized operation is selected on the Processor-Converter front panel by placing the DUAL FREQ switch in the NON-SYNC position. This position can also be used when synchronized radar pulses are separated by 60 μ s or more.

Two-frequency operation is enabled by placing both CHAN 1 and CHAN 2 switches in the REC or XMIT positions.

During acquisition, search alternates between the two channels and the SEARCH light on both channels will be alternately lit, each for about a one-second period. When one channel has acquired, the other will continue to search during all time but the 30 μ s period per pulse in which the first channel is expecting a pulse.

Priority has been assigned in the following order during the acquisition process.

Acquisition

Track

Search

For example, if channel 1 is tracking and channel 2 starts acquisition, the timing will skip a few track pulses until the PRF on channel 2 is established.

When both channels are tracking unsynchronized radars, the two pulses will walk through each other and the 30 μ s track periods will overlap. If two pretriggers occur within about 40 μ s of each other, special overlap timing logic is enabled.

For two 1000 pps threats, the overlap will occur about 8% of the time. The frequency and duration of overlap depends on the difference in PRFs.

The special overlap timing logic selects which channel will be honored for each pulse pair received. The sequence of selection considers that both halves of both trackers must be periodically updated and that lookthrough must periodically occur. During the 8% of the time that overlap occurs, the transmit duty per radar is reduced by 50% due to deleted pulses.

(b) Synchronized Threats

For a radar with a two frequency pulse, or for two radars synchronized together, the DUAL FREQ switch is placed in the SYNC position prior to enabling the channels. This mode of operation solves the problems of initial acquisition of time coincident pulses. During tracking, the operation is similar to being constantly in the unsynchronized but overlapped case as described in paragraph a.

The equipment, as delivered, will not operate optimally against two radars which are synchronized but whose pulses are staggered 2 to 40 μ s from the other. For this case, a wiring change is required in the equipment. An interim solution is to acquire in the synchronized position, but switch to the unsynchronized mode after both TRACK lights are illuminated.

During acquisition in the synchronized mode, the frequency search procedure starts as in the non-synchronized case. However, once one frequency has been acquired and is being tracked, the search procedure is modified. On selected pulses, tracking of the acquired pulse is suspended, and the second frequency is looked for "underneath" the first pulse. That is, an attempt to find the second frequency is made during the 30 μ s interval when the first pulse is normally received.

Once both frequencies have been acquired, the system will alternate between the two channels during successive receive intervals, taking into account the requirements for polarization and PRF updates.

C. Subassemblies

1. RF Receiver

a. Description

(1) Mixer/LO

The RF Receiver contains a dual (Σ and Δ) channel signal conversion superheterodyne receiver. The sum (Σ) and the delta (Δ) channels are nearly identical in gain and phase delay.

The RF input signals enter the unit through a pair of front panel waveguide connections. The RF transmission line is immediately converted from waveguide to semi-rigid coax cable, 0.141 inches in diameter.

Refer to the RF Receiver Functional Block diagram, Figure 1-18. The function of the high power limiters (LIM) (ALPHA MT 3281-C) is to protect the mixers during a system transmit event. Protection is required from the transmitter power reflected into the receiver ports by the Polarizer VSWR. For an expected worst case VSWR of 2:1 the reflected power is -9 dB. The signal is coupled down an additional 10 dB through the receiver/transmit coupler in the Polarizer unit. Assuming an additional -1 dB of transmission line loss, the total attenuation from the transmitter port to the receiver high power limiter is 20 dB. In a pulse mode this results in a 10-30 Watt peak power or a 5 watt CW signal. The limiter reduces this to below 100 mw.

The RF attenuators (RF ATTN) add attenuation prior to the mixers so that received signals up to the +15 dBm linear output level of the limiters may be processed. The RF attenuators are controlled in conjunction with the IF amplifier gain and add 27 dB to the linear operating dynamic range of the receiver system.

The Mixers (RHG DMP10AP92) are special units with high output power and low noise figure, providing a large dynamic range between the noise floor and saturation.

The function of the isolator (Teledyne Microwave T-7543T-6) in the sum (Σ) channel is to prevent any RF signal from getting into the Σ mixer and causing erroneous measurements. The function of the isolator (T-25437T-6) in the delta (Δ) channel is to maintain phase and gain match by keeping the two (Σ and Δ) channels identical.

The purpose of the line stretcher (ALPHA 20160-PJ) is to allow phase compensation for any small line length variations between the two receiver channels.

The 3 dB hybrid (ANARAN 40268) splits the single LO line into two ports to supply the two mixers. A high degree of phase and amplitude balance is required so that the receiver and channels remain balanced.

The combination of the single pole - double throw RF switch (ALPHA MT-3585-84) and the single pole - single throw RF switch (ALPHA MT-3498-H3-I-1) select RF from either VCO #1* (Varian VSX-9080C1) or VCO #2/3*. The combination of three switches is necessary to provide sufficient isolation such that the "OFF" VCO does not interfere with the "ON" VCO. The VCOs are not turned off (power removed) in order to permit long term stability and transient-free operation.

The isolators (Teledyne Microwave T-7543T-6) are used to minimize the VCO tuning due to VSWR effects, especially when the LO single pole - single throw switch is open.

Front panel switches on the RF Receiver allow the selection of:

- VCO #1
- VCO #2/3
- Auto (Auto selection under the control of the processor)

(2) Auxiliary LO Output

An LO signal for an auxiliary receiver is obtained by coupling energy from the main LO line. A 20 dB (ANARAN 1H0618-20) coupler is used for this purpose. The isolator (Teledyne Microwave T-7543T-6) is used to:

- 1) provide a load for the coupler in the event the auxiliary is not used, and
- 2) prevent radar RF from entering the receiver thru the auxiliary LO lines.

* Mounted in the box near each VCO is an ON-OFF switch. These switches are used for unit test only and should be in the "ON" position normally.

(3) Transponder RF

To provide a transponder RF signal source at the frequency of the victim, the LO is offset 60 MHz using a single sideband modulator (SSB) (ANARAN 90338-60).

The RF input to the SSB modulator is coupled from the direct LO line with a 10 dB coupler (ANARAN 1H0618-10). The isolator (Teledyne Microwave T-7543T-6) is used to eliminate the effect on the LO source due to the VSWR variations created by modulating the SSB modulator. It also prevents the offset RF from feeding back into the receiver through the LO lines.

The LO signal is frequency offset by the 60 MHz OSC. input to the SSB modulator. The 60 MHz source can be selected (Receiver front panel) to be either a stable crystal oscillator or frequency modulated VCO source. The stable source is crystal controlled and results in a transponder signal at the victim RF ± 250 /kHz. The 60 MHz source VCO can be externally modulated (Receiver Front Panel BNC) at any rate up to 100 kHz.

The amplitude out of the SSB modulator is controlled by a front panel variable attenuator (ARRA 6684-60AA).

(4) VCO Tuning Control

Figure 1-19 is a simplified block diagram of the VCO tuning control.

Channel #1 (Figure 1-19A) controls VCO #1, the LO for operation against threat #1. Two front panel contacts are provided. A switch (AFC-1/ON/OFF) is used to select VCO #1. The other control is the manual tuning of the LO. Figure 1-20 shows the RF versus dial position curve.

Channel #2/3 (Figure 1-19B) controls VCO #2 and VCO #3 which are the LOs selected for operation (sequentially) against threats #2 and #3. The sequence rate is controlled by the front panel RATE control. Figure 1-21 shows the sequence rate versus dial position. A front panel switch "SEQUENCE" controls the selection of #2 or #3.

The HA-2405 (Figure 1-22) is a four channel operational amplifier. It combines the functions of an analog switch and a high performance operational amplifier.

There are four parallel preamplifier input sections, one of which is selected through the TTL-compatible digital inputs and connected to the output amplifier. The selected analog input terminals and the output terminal form a high performance operational amplifier with four selectable inputs.

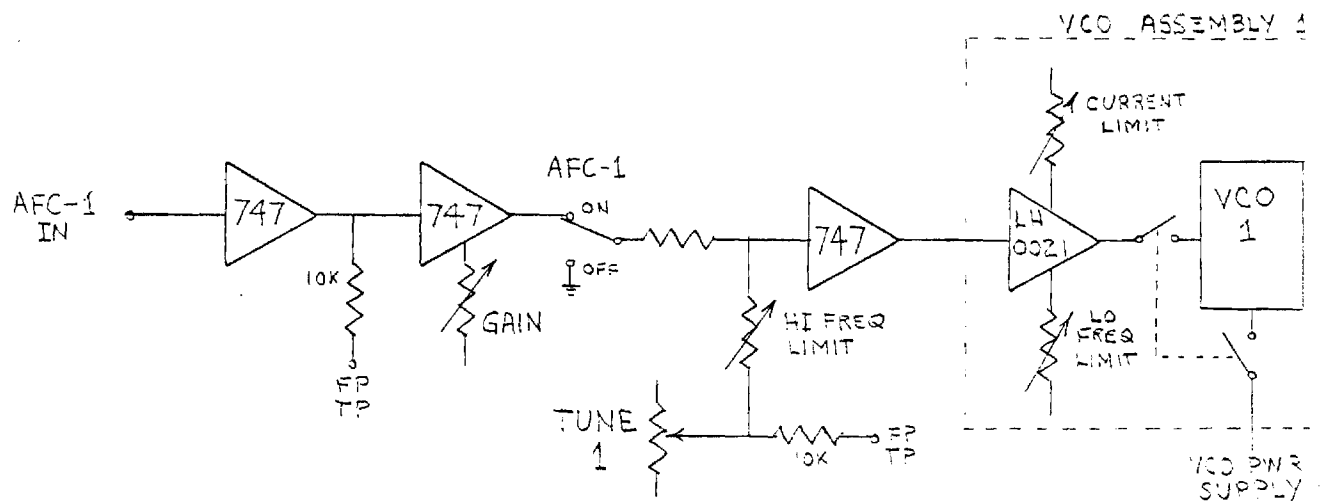


Fig 1-20

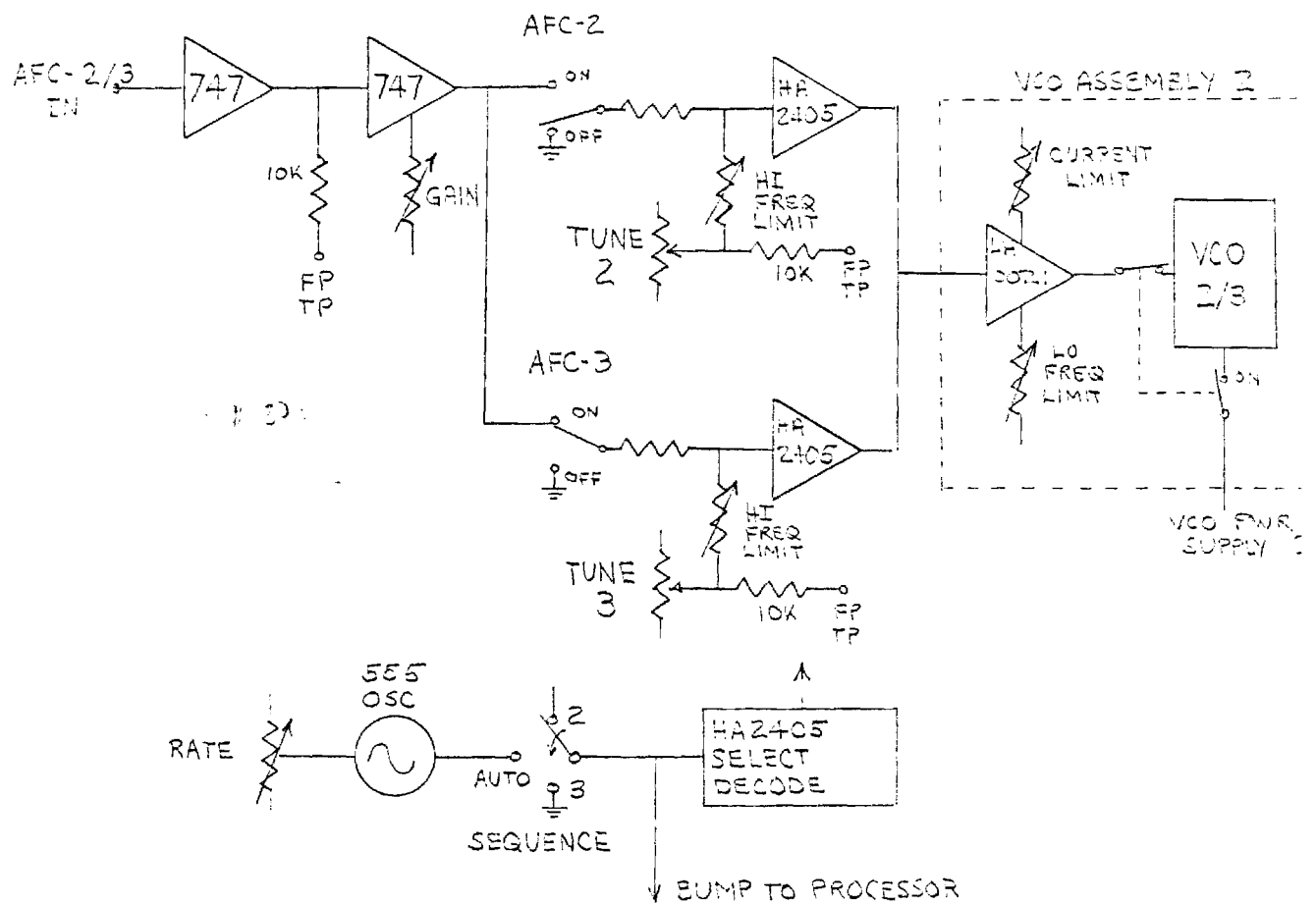


Figure 1-19. VCO Control AFC Chassis Block Diagram

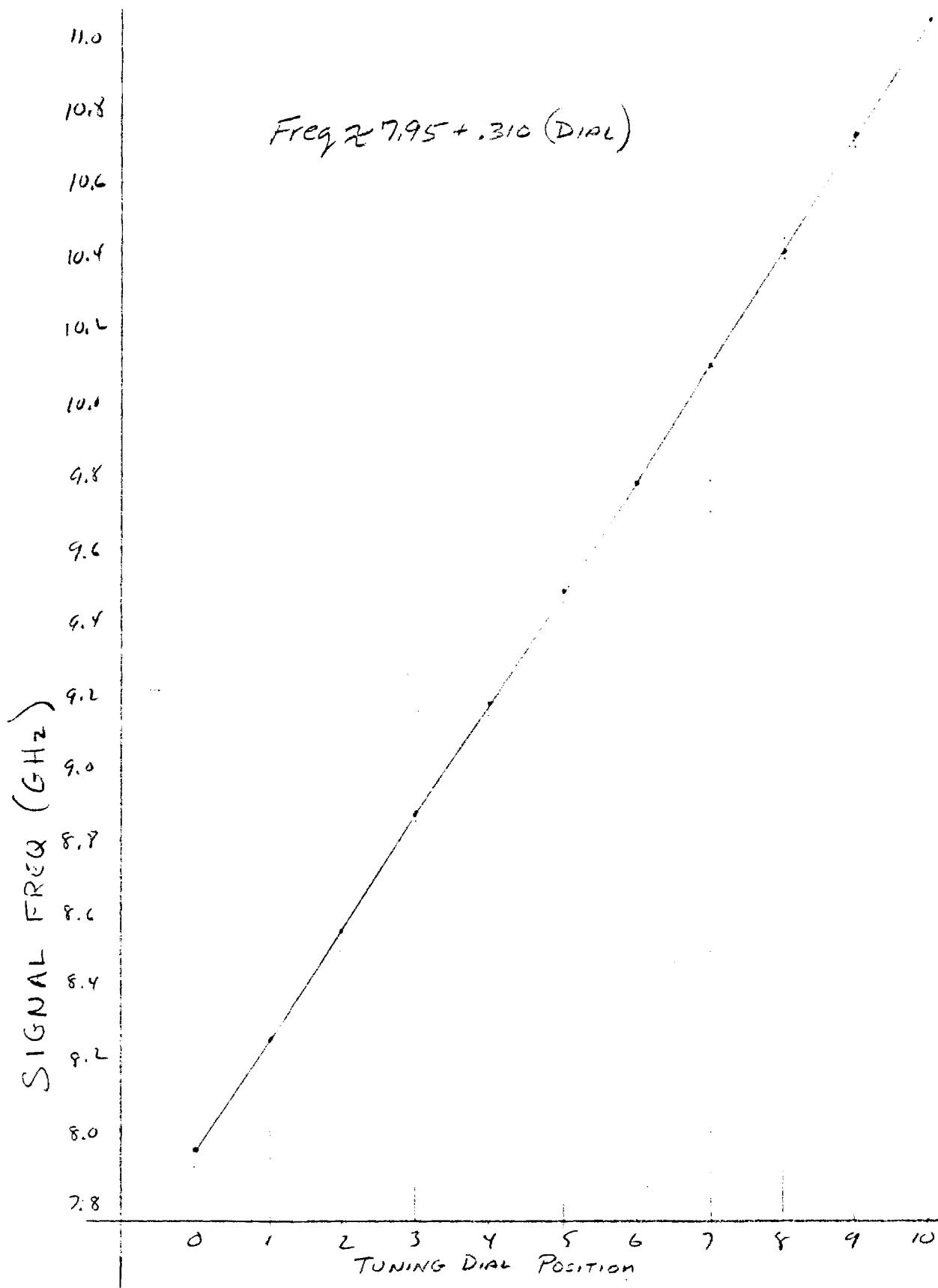


Figure 1-20. Signal Frequency versus Tuning Dial Position

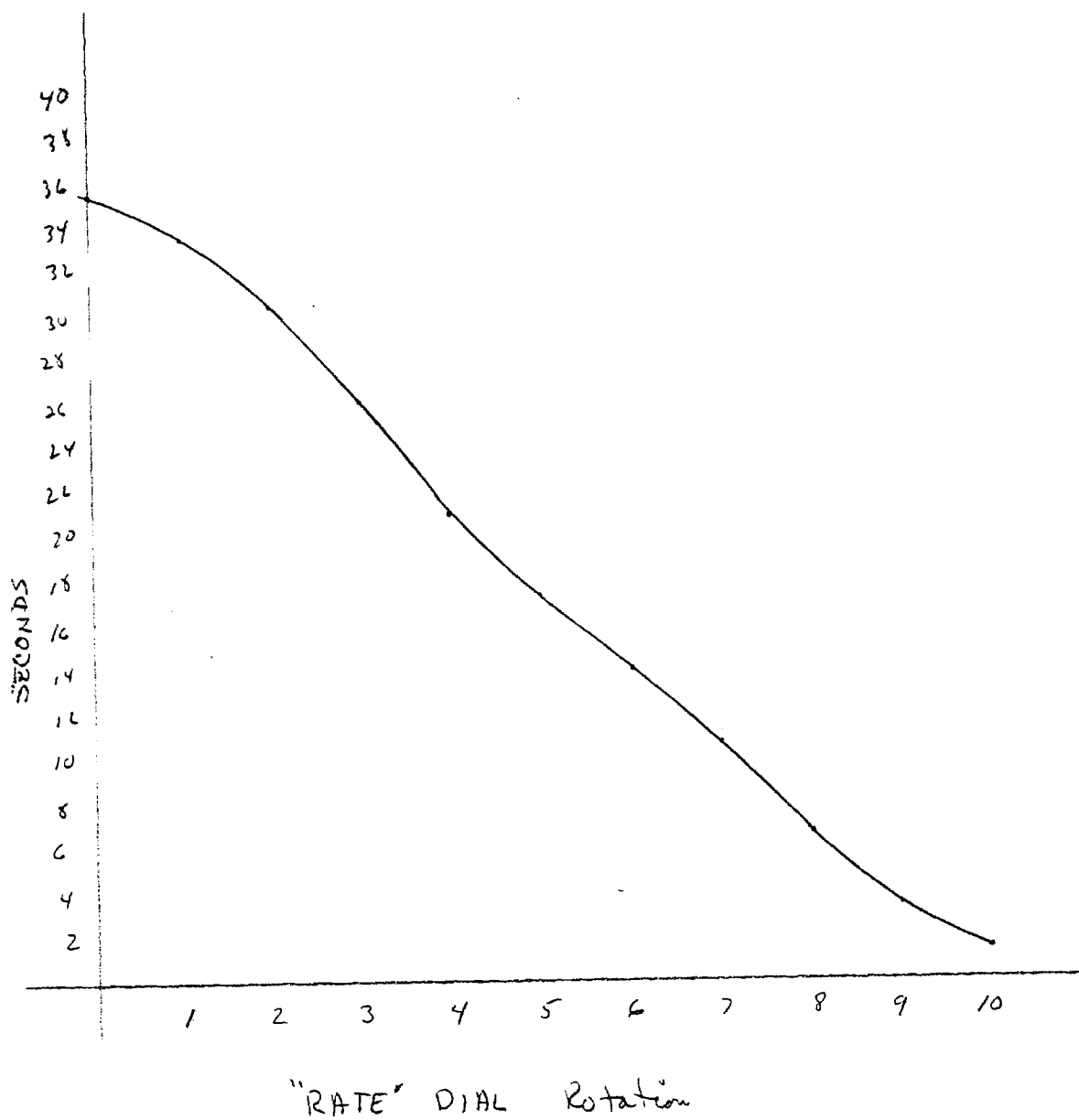


Figure 1-21. Sequence Rate (Time in Seconds)
versus
"RATE" Dial Position

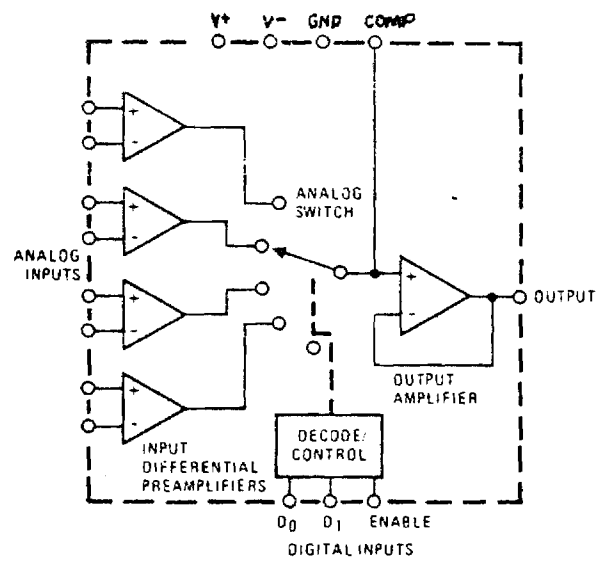


Figure 1-22. HA-2405 Programmable Operational Amplifier

When the command to change from Threat #2 to Threat #3 is generated, a signal "BUMP" is sent to the processor initiating the new acquisition procedure.

The AFC control for channels #1, 2, and 3 can independently be turned on or off.

b. Calibration and Test Points

(1) Mixer/LO

The following data represent measured data. No attempt has been made to establish required limits for normal operation.

Figure 1-23 shows the measured AUX LO output versus frequency for VCO #1 and VCO #2/3.

Figure 1-24 shows the IF power out versus RF power in at 9.2 GHz for both Σ and Δ channels (VCO #1 was used).

Figure 1-25 shows the measured noise figure (front panel input) versus frequency for both the Σ and Δ channels (VCO #1 was used at 9.2 GHz).

(2) Transponder RF

The stable oscillator is crystal controlled. It has been measured to have a frequency of 60.0001291 MHz.

The Frequency Modulated oscillator has the following characteristics:

Figure 1-26 shows the relative amplitude of the largest undesired sideband (to the desired sideband) versus frequency. (VCO #1 and the stable oscillator were used).

Figure 1-27 shows the power out of the desired sideband versus frequency.

(3) VCO Tuning Control

The VCOs have been set to tune from 7.890 to 10.990 GHz as the dial is adjusted from 000 to 100. The LO frequency is offset by 60 MHz. An additional 50 MHz is covered at each RF end to insure the full coverage of 8-11 GHz over temperature and hysteresis.

The following procedure is used to make these adjustments. (See Figure 1-19.)

1. Select VCO #1.

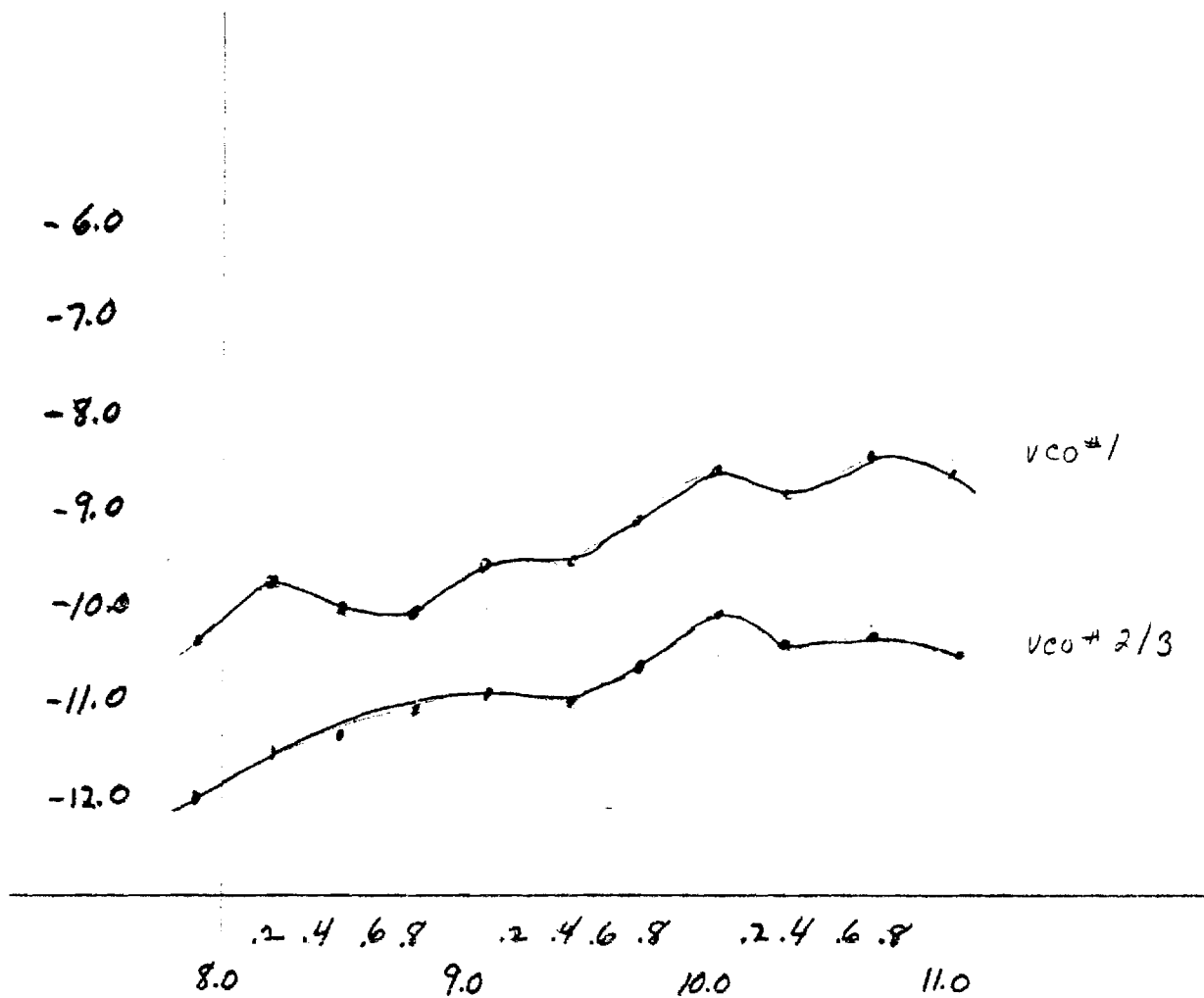


Figure 1-23. Aux. L.O. Output Power
versus
Frequency

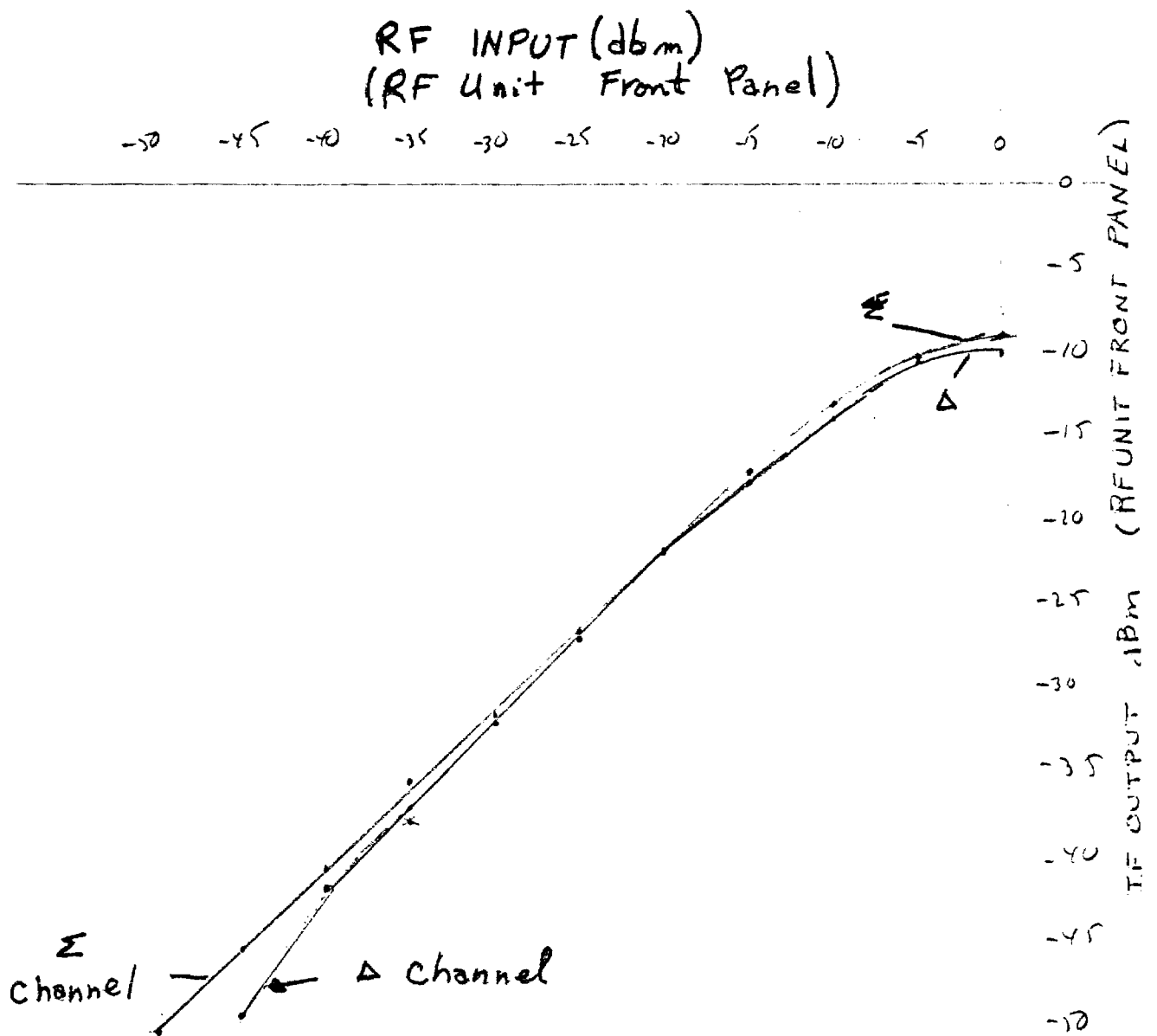


Figure 1-24. IF Output
versus
RF Input

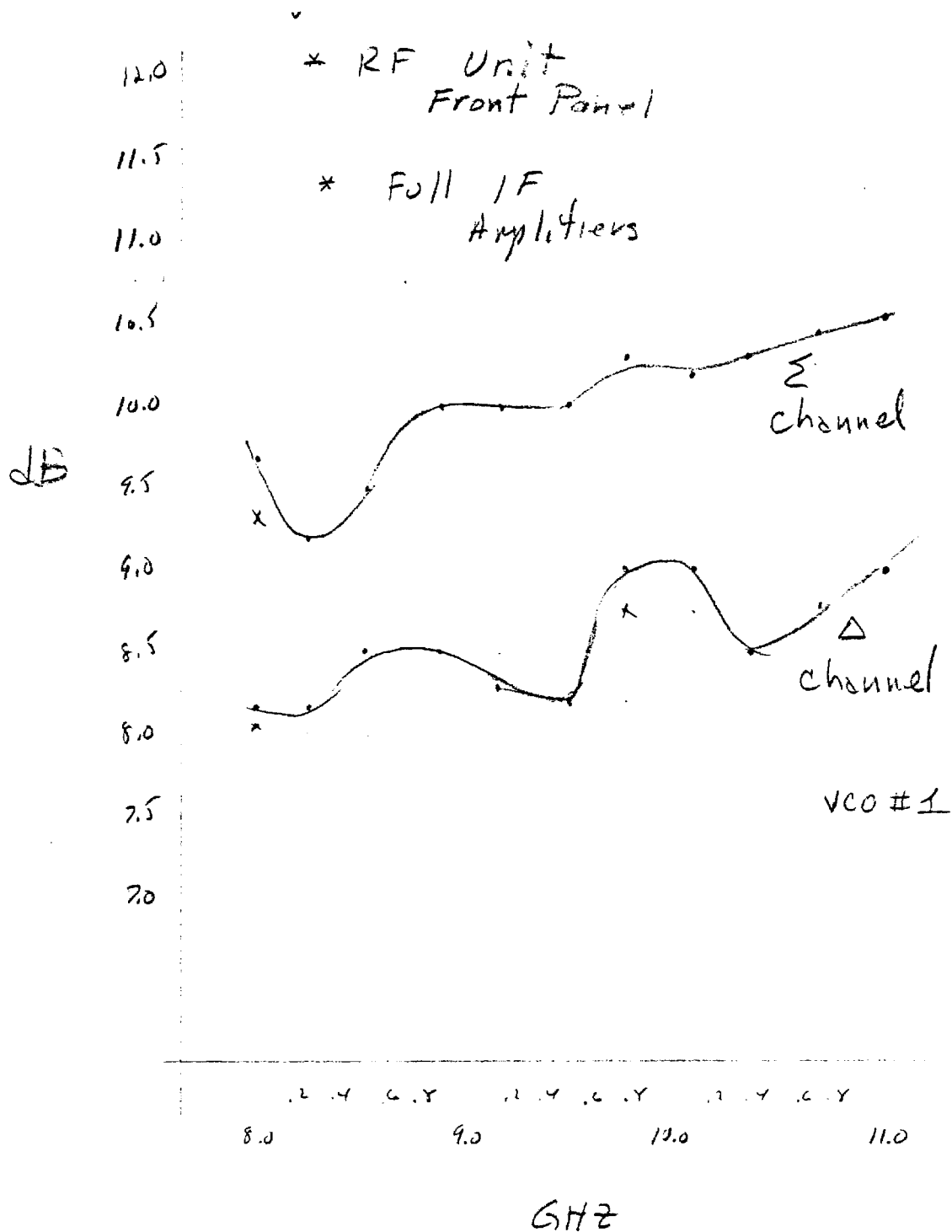


Figure 1-25. Noise Figure
 versus
 Frequency

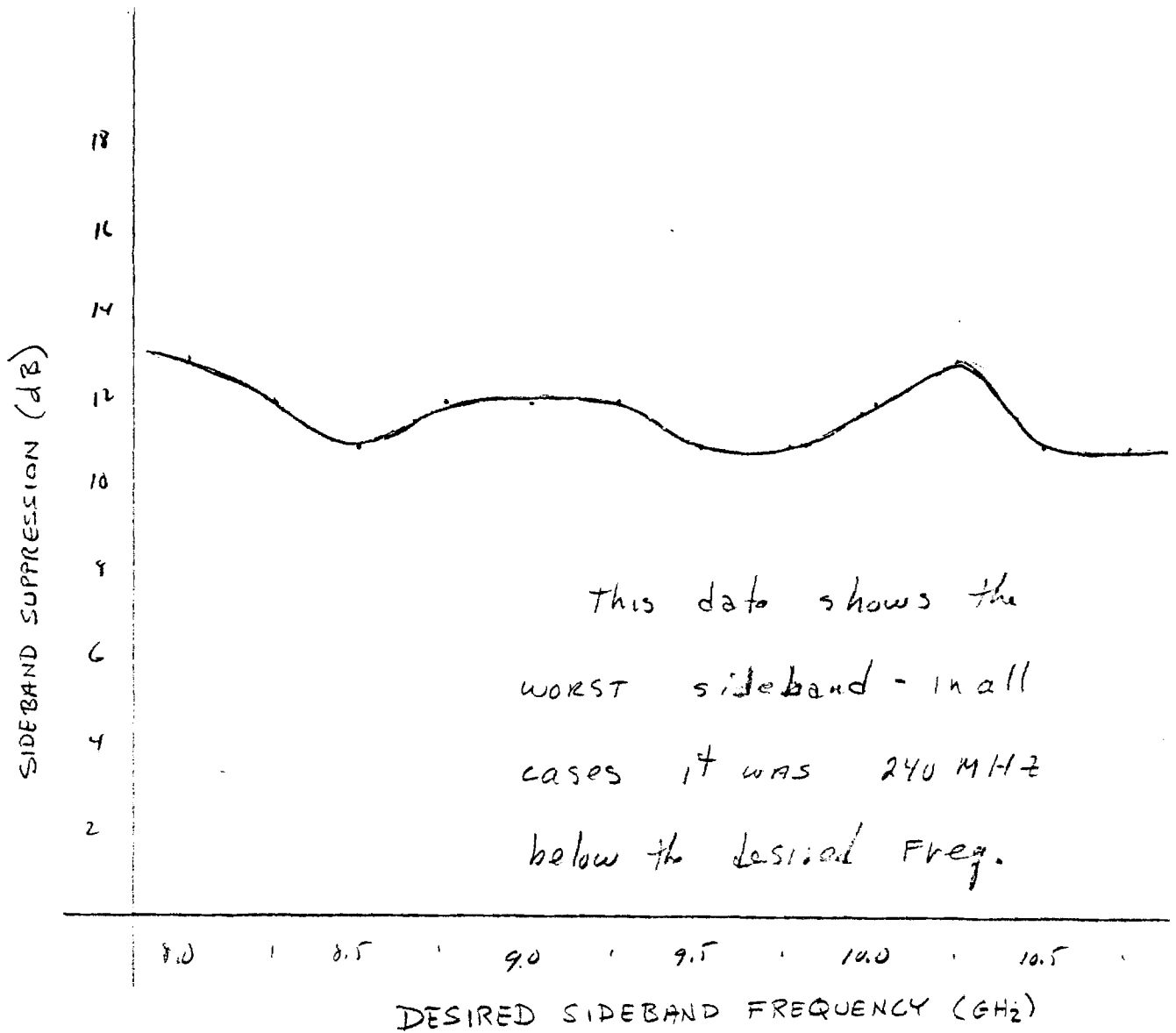


Figure 1-26. Sideband Supression
versus
Frequency

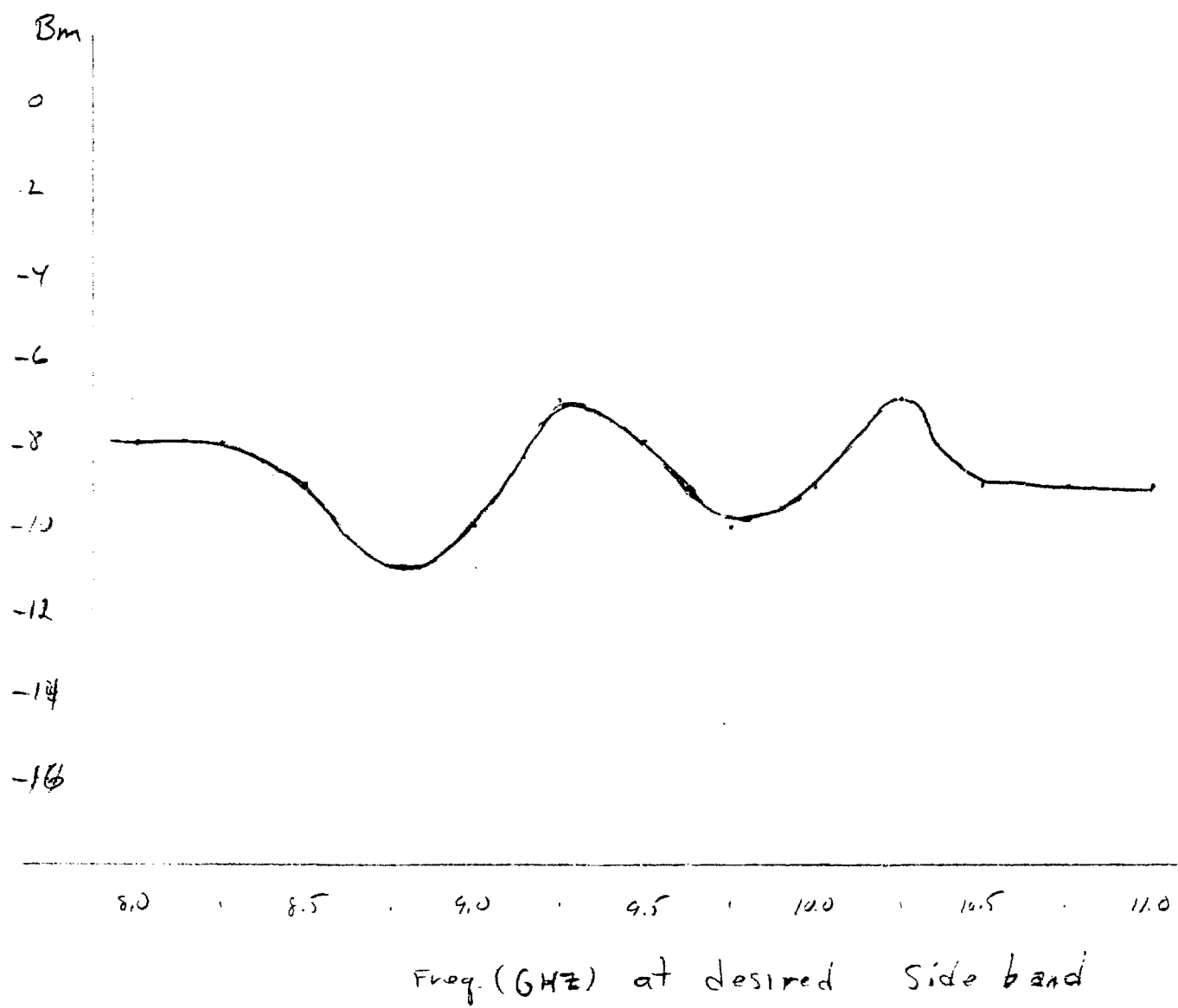


Figure 1-27. RF Output Power
versus
Frequency

2. Turn AFC "OFF".
3. Set 3 ohm (current limit) pot on VCO chassis to zero (full CW).
4. Set Front Panel Frequency Control to 000.
5. Adjust "Low Frequency Limit Adjust" on VCO Chassis so that the RF (AUX LO output) is 7.890 GHz (± 10 MHz).
6. Adjust Front Panel Frequency Control to 100.
7. Adjust "High Frequency Limit" so that the RF is 10.990 GHz ± 10 MHz (Clockwise rotation increases Frequency).
8. Adjust the current limit out put such that it is just beginning (5 MHz) to lower the RF.
9. Repeat steps 6 and 7.
10. Select VCO #2.
11. Repeat Steps 2 thru 9.
12. Select VCO #3.
13. Repeat Steps 2 thru 9.

2. IF Receiver

The IF Receiver unit is configured using the PECM (C Band receiver) GFE from a previous contract. All the C Band components remain in the chassis but only the IF & video circuitry is used in the APECM system. It has been rewired to accept (Σ) and (Δ) IF signals from the IF preamplifiers located in the RF Receiver Unit.

Figure 1-28 is a functional block diagram of the IF/Video portion of the IF Receiver of the APECM system. The two IF amplifiers are phase and gain matched Varian 60-MHz amplifiers type ITM2-239A0. Table 1-3 shows the measured characteristics of the two amplifiers. Figure 1-29 is a plot of the measured phase and gain match of the DELTA channel amplifier referenced to the SUM channel amplifier as a function of IF frequency. Plots are for the extremes of (a) full gain and (b) with gain reduced 55 dB below full gain. Figure 1-30 is the measured gain match at 60 MHz as a function of gain reduction.

Each amplifier has two IF outputs and a video output. The video output of the sum channel amplifier is sent to the receiver processor where a Sample and Hold and A/D conversion is performed for amplitude measurement by the digital AGC control loop.

IF output #1 is passed through a passive 60 MHz filter (K & L #X-4851-60/9) to a MERRIMAC 3 dB hybrid power splitter. One arm of the 3 dB power splitter feeds the 60 MHz discriminator (RHG DT60 PP78). Figure 1-31 is a plot of the output of the discriminator as a function of frequency (relative to 60 MHz). The discriminator output is quantified into a single logic bit which is directed to the processor digital frequency control (ARC) circuits, causing a LSB correction to the frequency control word controlling the appropriate (VCO) local oscillator of the RF receiver. The second arm of the 3 dB hybrid power splitter is coupled to an amplifier detector which produces a Video pulse (Rec. Pulse present) sync signal to the Processor-Converter's timing and control circuits. The number 2 IF output from both Sum and Delta amplifiers is furnished to the Processor-Converter for resolving by the Polarization Error Detector (I & Q detector) into PHI and GAMMA phase error signals.

A local manual gain control is available for test purposes.

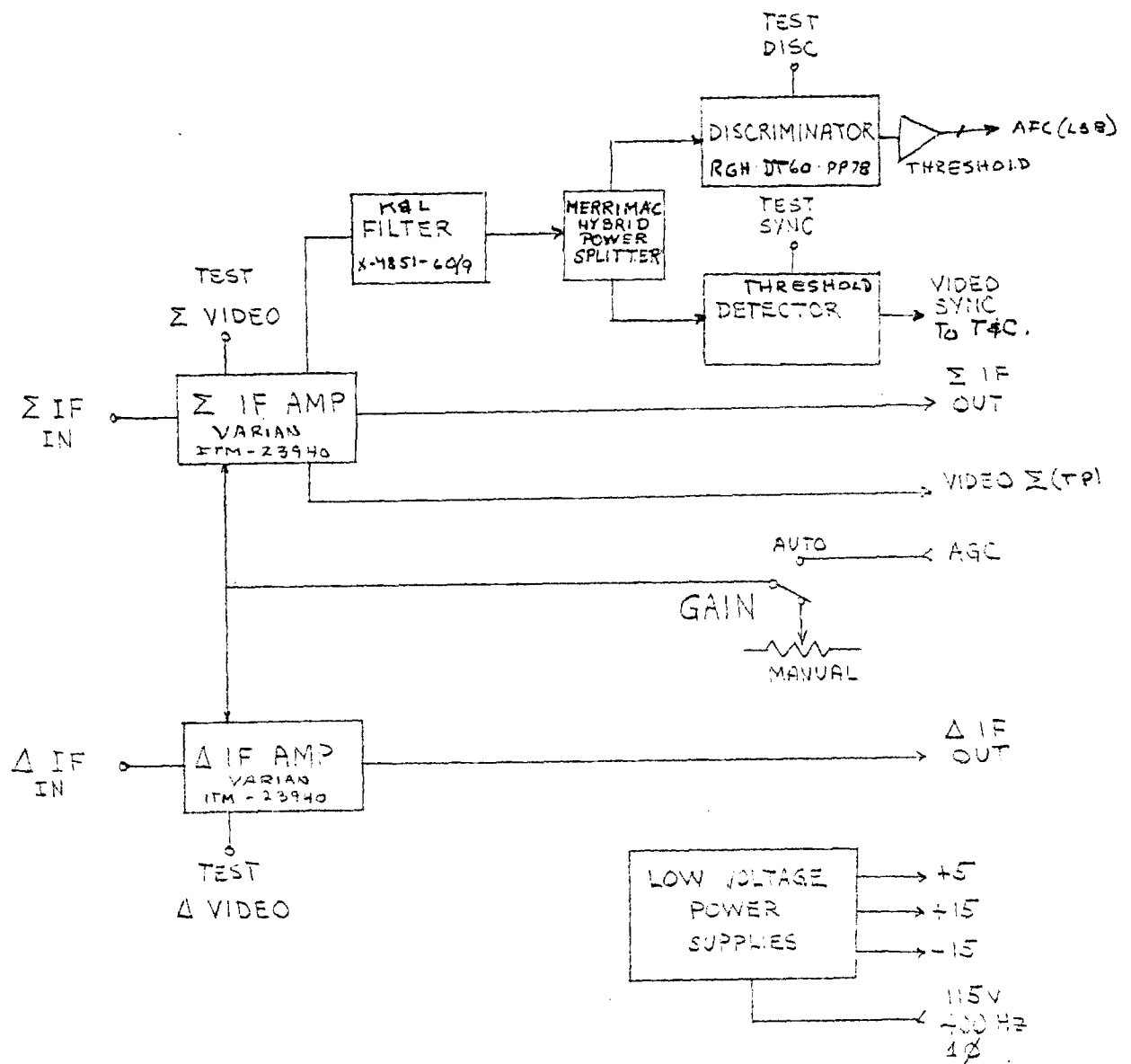


Figure 1-28. IF Receiver Block Diagram

TABLE 1-3. MEASURED CHARACTERISTICS OF
MATCHED IF AMPLIFIERS

	DELTA SN-866B	SUM SN-867B	
F _o	60	60	MHz
BW (3 dB)	13.0	11.5	MHz
NF	3.0	2.8	dB
Rise Time	0.1	0.1	μsec
IF Gain	75.0	75.4	dB
IF Output (1 dB comp.)	>+10	>+10	dBm
Video Output into 93 (0 dBm IF)	0.55	0.55	volts
Input VSWR	1.2:1	1.2:1	at 50 ohms
AGC Switching Time	2	2	μsec
Recovery Time (0 dBm on input)	0.15	0.15	μsec
Auxiliary IF Output (0 dBm output)	-9	-9	dBm
Channel Isolation	>15	>15	dB
Power Required -15 VDC at	80		

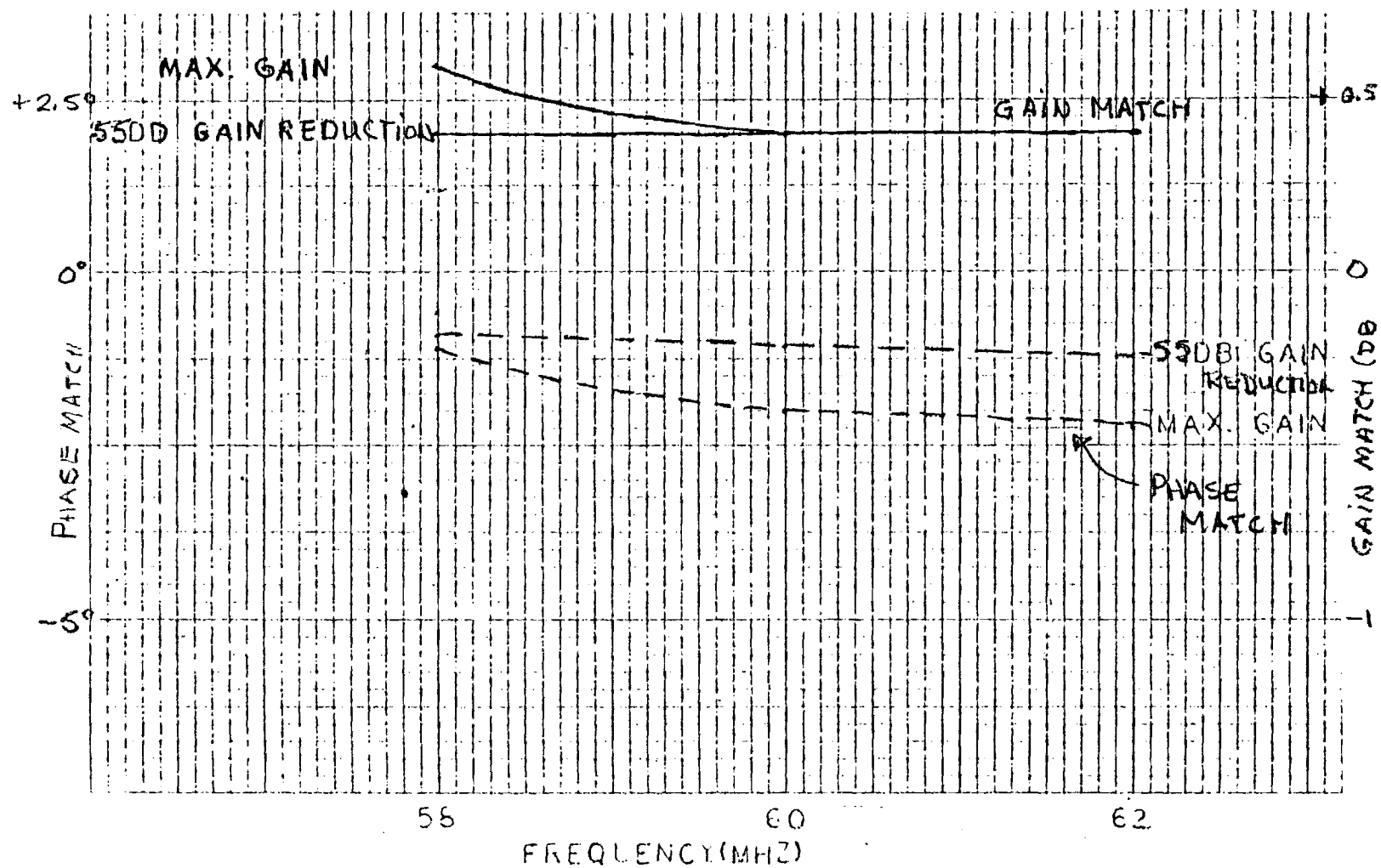


Figure 1-29. IF AMP Phase/Gain Match vs IF Frequency

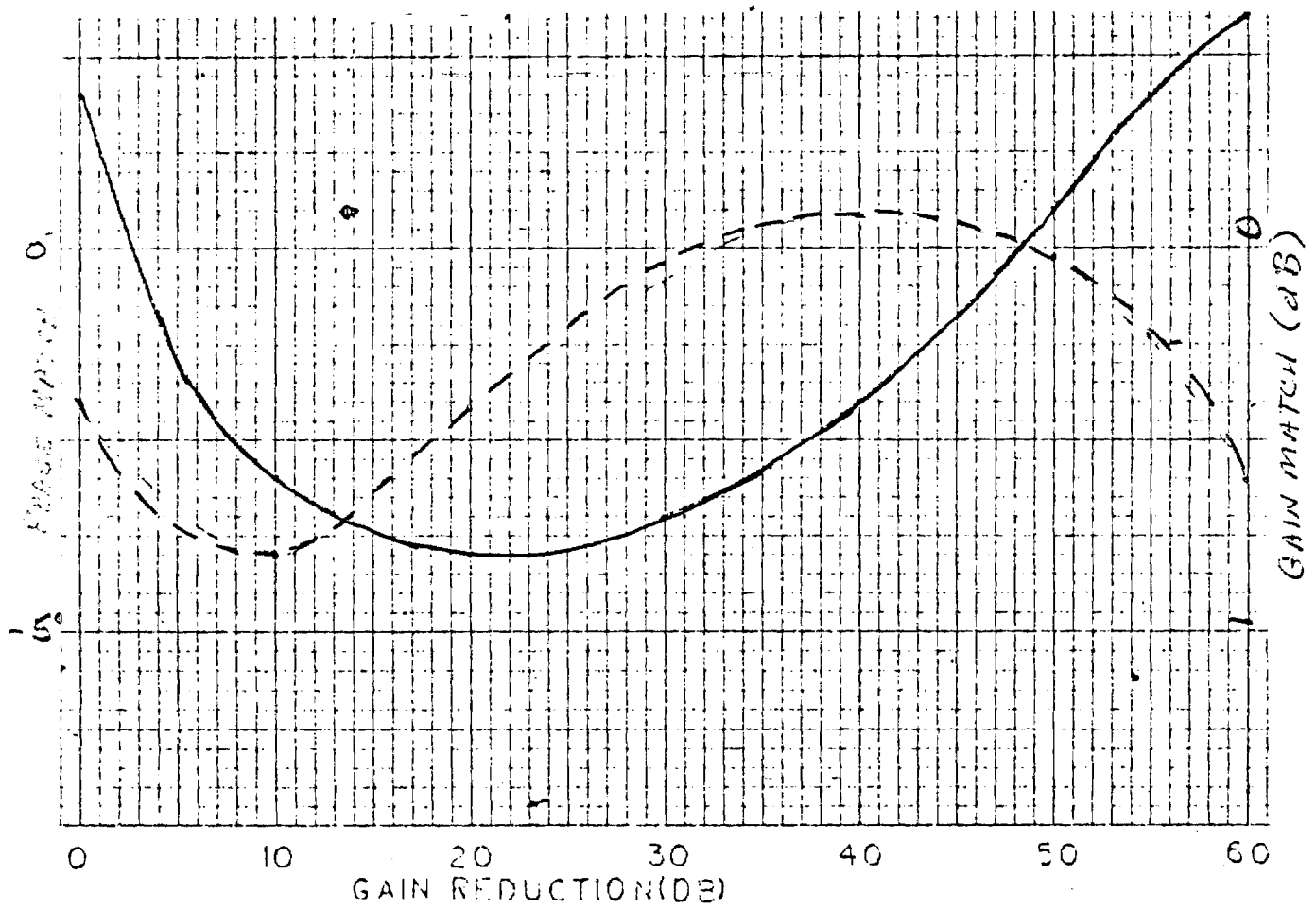


Figure 1-30. Measured Gain vs Gain Reduction

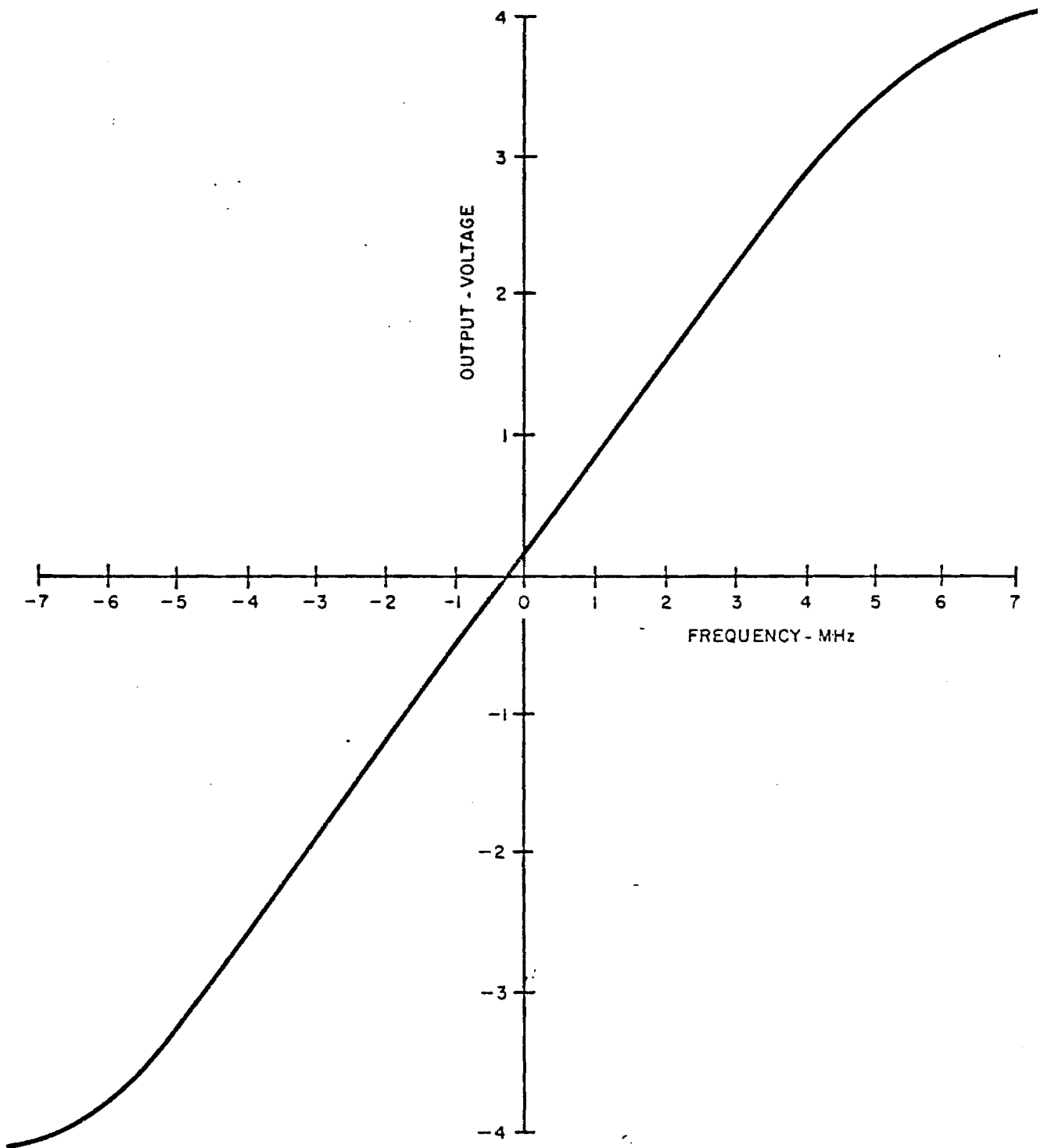


Figure 1-31. Discriminator Output vs Frequency

3. Processor-Converter

a. General

The Processor-Converter performs all the logic, timing, and control functions for the APECM system. The Processor-Controller is a special-purpose hardwired digital processor which performs the functions of PRF track, AGC, and AFC control for both track channels as well as polarization null tracking. All tuning and control of the polarization, receiver control, and transmitter control including Range Gate walkoff and lookthrough programming. Both automatic functions and selective manual control for checkout and test are provided. Table 1-4 and 1-5 describe the front panel controls, their functions, and their locations. Related controls located on other units are consolidated into this discussion for uniformity. In addition the front panel controls, certain auxiliary controls located on subassemblies are also described.

b. Block Diagram

The block diagram of the Processor-Converter is shown in Figure 1-32. By the side of each block is a number keyed to a brief functional description of that block. These descriptions are in Table 1-6. The identity of the circuit board that contains a given function is given by the number in the top right corner of its block on the block diagram. The location of the circuit boards in the Processor-Converter chassis is shown in Figure 1-33.

c. Circuit Board Descriptions

The following paragraphs describe the logic circuits of the Processor-Converter. Sheet numbers refer to drawings in Vol IV of this manual.

(1) Clock Generator Board 1

Schottky logic is used to frequency divide from 20 MHz and to maintain 5-10 MHz phase match. The 5 MHz clocks are 50 ns pulses. Seven 9316's are used to divide the clock frequencies from 5 MHz to 0.019 Hz. All the divided clock edges are close to synchronous with the system 5 MHz clock edge (Q5 MHZAL). 7510's are used as output drivers.

(2) Transmit Control Board 2 (Figure 1-34)

After polarization phase error is below preset limits, and the IF center frequency has been crossed at least twice such that the frequency is centered in the receiver band-pass, ENXMIT can occur with XMITG. XDU is 1 and TCC is 0. The

TABLE 1-4. SWITCH FUNCTION TABLE

CONTROL	RANGE	NOMINAL SETTING	Δ	METHOD OF ADJUSTMENT S=SWITCH, W=WIRE	LOCATION OF ADJUSTMENT FP=FRONT PANEL BD=BOARD
1. CH 1 XMIT/REC/OFF	-	-	-	S	FP-PC
2. CH 2 XMIT/REC/OFF	-	-	-	S	FP-PC
3. CHAN 1 AFC NORMAL/FIXED	-	NORM	-	S	FP-PC
4. CHAN 2 AFC NORMAL/FIXED	-	NORM	-	S	FP-PC
5. CHAN 1 & 2 AFC AUTO/MAN ADJ	-	AUTO	-	S	FP-PC
6. CHAN 1 "CENTER FREQ." TUNE	-	-	-	POT	FP-RFR
7. CHAN 2 "CENTER FREQ." TUNE	-	-	-	POT	FP-RFR
8. CHAN 3 "CENTER FREQ." TUNE	-	-	-	POT	FP-RFR
9. GAIN MANUAL/AUTO	-	AUTO	-	S	FP-IFR
10. AGC OPERATE/OPERATE	ON/OFF	OPERATE	-	S	FP-IFR
11. AGC LSB/FULL	-	-	-	S	FP-PC
12. POLAR ERROR CORRECTION LSB/FULL	-	-	-	S	FP-PC
13. POLAR ERROR CORRECTION NORMAL/DISABLE	ON/OFF	NORM	-	S	FP-PC
14. CHAN 1 BUMP	ON/OFF	OFF	-	S	FP-PC
15. CHAN 2 BUMP	ON/OFF	OFF	-	S	FP-PC
16. POL MOD CHANNEL 1	ON/OFF	-	-	S	FP-PC
17. POL MOD CHANNEL 2	ON/OFF	-	-	S	FP-PC

TABLE 1-4. SWITCH FUNCTION TABLE (Continued)

CONTROL	RANGE	NOMINAL SETTING	Δ	METHOD OF ADJUSTMENT S=SWITCH, W=WIRE	LOCATION OF ADJUSTMENT FP=FRONT PANEL BD=BOARD
CONTINUOUS LOOKTHROUGH	ON/OFF	OFF	-	S	FP-PC
FC-AUTOSEARCH	-	AUTO	-	S	FP-PC
HAN 1 TRACK AFC INHIBIT	ON/OFF	OFF	-	S	BD2,2-PC
HAN 2 TRACK AFC INHIBIT	ON/OFF	OFF	-	S	BD2,2-PC
/2RF SWEEP BANDWIDTH	0-5MHz	15MHz	1/4 MHz	S	BD7,3-PC
SBREVERSE(1))	HI/LO	-	-	S	BD2,2-PC
SBREVERSE(2))	HI/LO	-	-	S	BD2,2-PC
GC ACQ SENSITIVITY	-	-15dBm	-	S	BD13,2
GC MAX TRACK SENSITIVITY	-	-35dBm	-	S	BD13,2
ANUAL AGC ADJUST	-	-	-	POT	FP
GC A/D CONTROL	0-6.4 μ s	1.2 μ s	.4 μ s	W	BD13,4
and ϕ A/D CONTROL	0-102.4 μ s	-	.4 μ s	W	BD13,4
ODCONTROL	-	GND	-	W	BD4,2-33
TRANSMIT PULSE WIDTH	.8 μ s- 12.8 μ s	5.6 μ s	.8 μ s	S	BD2,2
TRANSMIT PULSE POSITION	-4. μ s- +.2 μ s about PRF center	0 μ s	.2 μ s	W	BD3,1&2

TABLE 1-4. SWITCH FUNCTION TABLE (Continued)

CONTROL	RANGE	NOMINAL SETTING	Δ	METHOD OF ADJUSTMENT S=SWITCH, W=WIRE	LOCATION OF ADJUSTMENT FP=FRONT PANEL BD=BOARD
33. REC GATE TO PRF ENABLE DELAY	.2 μ s- 1.2 μ s	.8 μ s	.2 μ s	W	BD5,3&4
34. FREQ JUMP PERIOD	0-52ms	22ms	3.3ms	W	BD7,1
35. ACQ GATEWIDTH	0-13ms	13ms	2ns	W	BD7,1
36. ACQ PRF INTERVAL RESET	0-1.64 ms	1.64ms	102 μ s	W	BD7,1
37. LOOKTHROUGH GATE RATIO	1/1- 1/256	-	1	S	BD4,1
38. LOOKTHROUGH TRANSMIT SELECT	ON/OFF	ON	-	S	BD2,1
39. REC BLANK TIME AFTER TRANSMIT	.2 μ s - 1 μ s	.2 μ s	.2 μ s	W	BD2,1
40. CHAN 1 LOOKTHROUGH MISS COUNTER	1/1- 1/16	1/7	1	W	BD7,2
41. CHAN 2 LOOKTHROUGH MISS COUNTER	1/1- 1/16	1/7	1	W	BD7,2
42. DROP OUT TIME	0 to 13 sec	-	52ms	S	BD10,1
43. -10 dB SUM REFERENCE TRIM	-	-10dB	-	POT	BD10,3
44. -10 dB AUX REFERENCE TRIM	-	-12dB	-	POT	BD10,3
45. LOOKTHROUGH DATA SAMPLING DELAY	0- 51.2 μ s	10 μ s	.2 μ s	W	BD6,1
46. CHAN 1 SELECT START	0- 819 μ s	-	.2 μ s	W	BD3,1

TABLE 1-4. SWITCH FUNCTION TABLE (Continued)

CONTROL	RANGE	NOMINAL SETTING	Δ	METHOD OF ADJUSTMENT S=SWITCH, W=WIRE	LOCATION OF ADJUSTMENT FP=FRONT PANEL BD=BOARD
IAN 1 ENMASTER START	0- 819 μ s	-	.2 μ s	W	BD3,1
IAN 1 ENMASTER END	0- 819 μ s	-	.2 μ s	W	BD3,1
HAN 2 SELECT START	0- 819 μ s	-	.2 μ s	W	BD3,2
HAN 2 ENMASTER START	0- 819 μ s	-	.2 μ s	W	BD3,2
HAN 2 ENMASTER END	0- 819 μ s	-	.2 μ s	W	BD3,2
VERLAP INTERVAL	0- 51.2 μ s	32.8 μ s	.2 μ s	W	BD3,3
VERLAP ALTERNATION RATE	1/1- 7/7	1/1	1	S	BD4,1
UAL FREQ. SYNC/NON SYNC	-	-	-	S	FP-PC
REDICTOR - ON/OFF	$\alpha=\alpha'-1$ $b=b'-0$	ON	-	S	FP-PC
MIT - CW/PULSE	-	-	-	S	FP-PC
GPO - NORMAL/FIXED	-	NORM	-	S	FP-PC
GPO - START	-	-	-	S	FP-PC
OL MON CHANNEL SELECT	1-2	-	-	S	FP-PC

TABLE 1-4. SWITCH FUNCTION TABLE (Continued)

CONTROL	RANGE	NOMINAL SETTING	Δ	METHOD OF ADJUSTMENT S=SWITCH, W=WIRE	LOCATION OF ADJUSTMENT FP=FRONT PANEL BD=BOARD
60. MAN POLAR POS. GAMMA	180°	-	$\approx .35^\circ$	S	FP-PC
61. MAN POLAR POS. PHI	360°	-	$\approx .7^\circ$	S	FP-PC
62. RATE INCREMENT	$\pm .45^\circ/P$	-	$\approx .17^\circ$	S	FP-PC
63. PREDICTOR CONSTANT (GAMMA)					
ALPHA	0- 1-63/64	-	1/64	S	FP-PC
BETA	0- 1-63/64	-	1/64	S	FP-PC
64. CHAN 1 POLAR SOURCE (GAMMA)	MAN/ AUTO	AUTO	-	S	FP-PC
65. CHAN 1 POLAR SOURCE (PHI)	MAN/ AUTO	AUTO	-	S	FP-PC
66. CHAN 2 POLAR SOURCE (GAMMA)	MAN/ AUTO	AUTO	-	S	FP-PC
67. CHAN 2 POLAR SOURCE (PHI)	MAN/ AUTO	AUTO	-	S	FP-PC
68. AFC-1	ON/OFF	-	-	S	FP-RFR
69. AFC-2	ON/OFF	-	-	S	FP-RFR
70. AFC-3	ON/OFF	-	-	S	FP-RFR
71. VCO SELECT - 1/AUTO/2/3	-	-	-	S	FP-RFR

TABLE 1-4. SWITCH FUNCTION TABLE (Continued)

CONTROL	RANGE	NOMINAL SETTING	Δ	METHOD OF ADJUSTMENT S=SWITCH, W=WIRE	LOCATION OF ADJUSTMENT FP=FRONT PANEL BD=BOARD
REQ. OFFSET - FM/STABLE	STABLE	-	-	S	FP-RFR
EQUENCE - 2/OFF/3	OFF	-	-	S	FP-RFR
EQUENCE RATE	See Fig. II-5 1.5- 36 sec	-	CONT	S	FP-RFR

TABLE 1-5. DESCRIPTION OF SYSTEM SWITCH AND
ADJUSTMENT FUNCTIONS

1. CH1 XMIT/REC/OFF - Controls mode of channel 1 operation XMIT (receive and transmit), REC (receive only), OFF (disabled).
2. CH2 XMIT/REC/OFF (CH(2)OFFAL),(2) XMIT) - Same as switch 1 for Channel 2.
3. CHAN 1 AFC NORMAL/FIXED - Fixed Position disables Channel 1 AFC. It remains in last established state.
4. CHAN 2 AFC NORMAL/FIXED - Same as switch 3 for Channel 2.
5. CHAN 1 AND 2 AFC AUTO/MAN ADJ - Manual Position causes Channel 1 and 2 frequency to be entirely controlled by their respective center frequency pots.
6. CHAN 1 "CENTER" FREQ TUNE - Adjusts Channel 1 center frequency.
7. CHAN 2 "CENTER" FREQ TUNE - Adjusts Channel 2 center frequency.
8. CHAN 3 "CENTER" FREQ TUNE - Adjusts Channel 3 center frequency.
9. GAIN MANUAL/AUTO - Allows Rec Gain to be manually or automatically controlled.
10. AGC OPERATE/DISABLE - Disables Channel 1 and 2 AGC. It will remain in last established state.
11. AGC LSB/FULL - Selects AGC mode for CHannel 1 and 2. In full mode the AGC will be corrected by the full value of measured AGC error. In LSB mode, correction is made in indicated direction by only 1 least significant bit for each error sample.
12. POLAR ERROR CORRECTION LSB/FULL - Same functions in polarization servo circuit as switch 11 has in AGC servo circuit.
13. POLAR ERROR CORRECTION NORMAL/DISABLE - Disables Channel 1 and 2 GAMMA and PHI error correction servo. Polarization will remain in last established state.

TABLE 1-5. DESCRIPTION OF SYSTEM SWITCH AND
ADJUSTMENT FUNCTIONS (Continued)

14. CHAN 1 BUMP - When depressed, Channel 1 servos will be reset and will begin searching for a new signal.
15. CHAN 2 BUMP - When depressed, Channel 2 servos will be reset and will begin searching for a new signal.
16. POL MOD CHAN 1 - Permits Polarization Modulation of Channel 1 null using waveform inserted at connectors labeled POL MOD - PHI and GAMMA.
17. POL MOD CHAN 2 - Permits Polarization Modulation of Channel 2 null using waveform inserted at connectors labeled POL MOD - PHI and GAMMA.
18. CONTINUOUS LOOKTHROUGH - When "ON" will cause lookthrough to occur on every received pulse. Intended as a test condition.
19. AFC-AUTO/SEARCH - Will prevent search frequency sweep on return to search condition once a null condition has been established. Effects both channels but only after a channel has nulled. Permits rapid reacquisition of test signal.
20. CHAN 1 TRACK AFC INHIBIT - Will prevent Channel 1 track frequency from changing once a Channel 1 null condition has been established.
21. CHAN 2 TRACK AFC INHIBIT - Will prevent Channel 2 track frequency from changing once a Channel 1 null condition has occurred.
22. 1/2 RF SWEEP BANDWIDTH - Establishes frequency deviation about center frequency established by switches 6 and 7.
23. (S.B. REVERSE (1)) - Selects whether a high or low sideband will contain the frequency to be tracked on Channel 1.
24. (S.B. REVERSE (2)) - Selects whether a high or low sideband will contain the frequency to be tracked on Channel 2.
25. AGC ACQ SENSITIVITY - Establishes AGC level required for acquisition. This is the level automatically selected during search.
26. AGC MAX TRACK SENSITIVITY - Establishes maximum tracking sensitivity. AGC is not allowed to increase receiver sensitivity to more than that level established by this control.

TABLE 1-5. DESCRIPTION OF SYSTEM SWITCH AND
ADJUSTMENT FUNCTIONS (Continued)

27. MANUAL AGC ADJUST - Manually adjusts AGC level. Used primarily for testing.
28. AGC A/D CONTROL - Sets delay between end of PRF gate and start of AGC error A/D.
29. γ and ϕ A/D CONTROL - Sets delay between end of PRF gate and start of γ and ϕ error A/D's.
30. MOD CONTROL - Used when operating in dual frequency mode. If lookthrough is called for on one channel while the system is operating at polarization null of the other channel, use of this function will cause lookthrough to wait for the modulator to return to the null polarization of the channel calling for lookthrough. If MOD CONTROL is set to 1 this will happen. If MOD CONTROL is set to 0, a lookthrough call will override the modulation and immediately cause null polarization for the lookthrough calling channel.
31. TRANSMIT PULSE WIDTH - Adjusts transmit pulse width.
32. TRANSMIT PULSE POSITION - Allows transmit pulse adjustment about the center of the expected received pulse.
33. REC GATE TO PRF ENABLE DELAY - Delays PRF enable after start of receive enable to allow spurious pulses to settle.
34. FREQUENCY JUMP PERIOD - Sets gate width which inhibits acquisition while search frequency is scanning a little more than 1 IF bandwidth.
35. ACQ GATEWIDTH - Sets gate width during which time received pulses are examined to establish PRF track.
36. ACQ PRF INTERVAL RESET - Set minimum PRI interval which will cause PRF tracker reset.
37. LOOKTHROUGH GATE RATIO - Sets lookthrough interval; i.e. 1/7 means every 7th received pulse on each channel will be a lookthrough period for the respective channel.
38. LOOKTHROUGH TRANSMIT SELECT - Selects whether a transmission will occur after a pulse is received during lookthrough.
39. REC. BLANK TIME AFTER TRANSMIT - Establishes delay after end of transmit until receive enable turns on. Used to prevent receiver saturation.

TABLE 1-5. DESCRIPTION OF SYSTEM SWITCH AND
ADJUSTMENT FUNCTIONS (Continued)

40. CHAN 1 LOOKTHROUGH MISS COUNTER - Sets number of look-throughs that occur on Channel 1 without receiving a pulse before a PRF tracker reset is generated. Each channel has its own counter, but they should be identically preset.
41. CHAN 2 LOOKTHROUGH MISS COUNTER - Sets number of look-throughs that occur on Channel 2 without receiving a pulse before a PRF tracker reset is generated.
42. DROP OUT TIME - Sets delay between drop PRF track and full channel drop track condition at which time, for example, search frequency turning may resume.
43. -10dB SUM REFERENCE TRIM - System sensitivity vernier. Works in conjunction with AGC ACQ Sensitivity and AGC MAX TRACK SENSITIVITY (Controls 25 and 26).
44. -10dB AUX REFERENCE TRIM - Adjusts sensitivity used for establishing IF bandwidth in conjunction with the auxilliary channel filter and the discriminator.
45. LOOKTHROUGH DATA SAMPLING DELAY- Sets delay between end of PRF gate and strobe which samples lookthrough data. This allows sufficient time for S and H op amps and A/D's to settle.
46. CHAN 1 SELECT START - Determines how far start of phase shifter set up is advanced from expected PRF occurrence for Channel 1.
47. CHAN 1 ENMASTER START - Determine position of start of receive gate for Channel 1.
48. CHAN 1 ENMASTER END - Determines position of the end of the receive gate for Channel 1.
49. CHAN 2 SELECT START - Same as CHAN 1 SELECT START (Control 46).
50. CHAN 2 ENMASTER START - Same as CHAN 1 ENMASTER START (Control 47).
51. CHAN 2 ENMASTER END - Same as CHAN 1 ENMASTER END (Control 48).
52. OVERLAP INTERVAL - Sets a separation interval between a Channel 1 pulse and a Channel 2 pulse that is used to establish an overlap or interference condition.

TABLE 1-5. DESCRIPTION OF SYSTEM SWITCH AND
ADJUSTMENT FUNCTIONS (Continued)

53. OVERLAP ALTERATION RATE - Sets how many times a given channel will be selected during overlap before changing to the other channel during overlap.
54. DUAL FREQ. SYNC/NON SYNC - Selects system mode - whether operating with 2 PRF synchronized RF frequencies (DUAL FREQ SYNC) or independent PRF's and RF frequencies (DUAL FREQ. NON SYNC).
55. PREDICATOR ON/OFF - Disables automatic adaptor mode of Alpha/Beta tracking loop by setting Alpha to 1.0 and Beta to 0.0.
56. XMIT-CW/PULSE - Alters logic to function in nonpulse mode; i.e., back generation etc.
57. RGPO-NORMAL/FIXED - Provides fixed range delayed trigger to transmitter or normal RGPO ramps.
58. RGPO-START - When depressed resets RGPO cycle.
59. POL MON CHANNEL SELECT - Selects polarization error samples to be available at Polarization monitor output connectors.
60. MAN POLAR POS-GAMMA - Establishes digital command (octal word) for manual control of Gamma Phase shifter.
61. MASS POLAR POS-PHI - Same as MAN POLAR POS-GAMMA (Control 60) for PHI phase shifter.
62. RATE INCREMENT - Establishes digital command for rate-aided incremental polarization predictor.
63. PREDICTOR CONSTANT (GAMMA) ALPHA/BETA - Establishes the Alpha and Beta constants for the adaptive polarization predictor, GAMMA loop.
64. PREDICTOR CONSTANT (PHI) ALPHA/BETA - Same as PREDICTOR CONSTANT (GAMMA) ALPHA/BETA (Control 63) for PHI loop.
65. CHAN 1 POLAR SOURCE (GAMMA) - Permits selection of manual or automatic control of Gamma phase shifter.
66. CHAN 1 POLAR SOURCE (PHI) - Same as CHAN 1 POLAR SOURCE (GAMMA) (Control 65) for PHI phase shifter.
67. CHAN 2 POLAR SOURCE (GAMMA) - Same as CHAN 1 POLAR SOURCE (GAMMA) (Control 65) for Channel 2.

TABLE 1-5. DESCRIPTION OF SYSTEM SWITCH AND
ADJUSTMENT FUNCTIONS (Continued)

- 68. CHAN 2 POLAR SOURCE (PHI) - Same as CHAN 1 POLAR SOURCE (GAMMA) (Control 65) for Channel 2 PHI phase shifter.
- 69. AFC-1 - Energizes AFC for Channel 1.
- 70. AFC-2 - Energizes AFC for Channel 2.
- 71. AFC-3 - Energizes AFC for Channel 3.
- 72. VCO SELECT - 1/Auto/2/3-Position "1" locks in VCO 1 position. "Auto" permits tracking of two threats on an interleaved basis (VCO 1 and VCO 2 or 3, whichever has been selected by sequencing.) Position "2/3" - Lock in VCO 2 or 3.
- 73. FREQUENCY OFFSET-FM/STABLE - Selects either the crystal-controlled 60 MHz oscillator for the offset generator or the Frequency Modulated VCO which permits the transmitted signal to be Frequency Modulated.
- 74. SEQUENCE-2/OFF/3 - Position "2" locks in VCO 2 into Channel 2 position. "OFF" permits the selection of 2 or 3 on a time share basis at rate established by the SEQUENCE RATE (Control 75).
- 75. SEQUENCE RATE - The position of this control establishes the sequencing rate between VCO 2 and 3 (See Figure 1-22).

The following switches are accessible from the Front Panel but are not used in controlling the APECM⁽¹⁾.

- | | | |
|---|---|---------------------|
| <ul style="list-style-type: none"> (1) Modulation A/B/C/D (2) Modulation OFF/AMP/POL/BOTH (3) Chan 1 Rate Aided ON/OFF (4) Chan 2 Rate Aided ON/OFF | } | Processor Converter |
| <ul style="list-style-type: none"> (5) Chan 1 Tune (6) Chan 2 Tune | } | IF Receiver |

(1)The APECM equipment was modified from GFE equipment originally built on previous Polarization contracts.

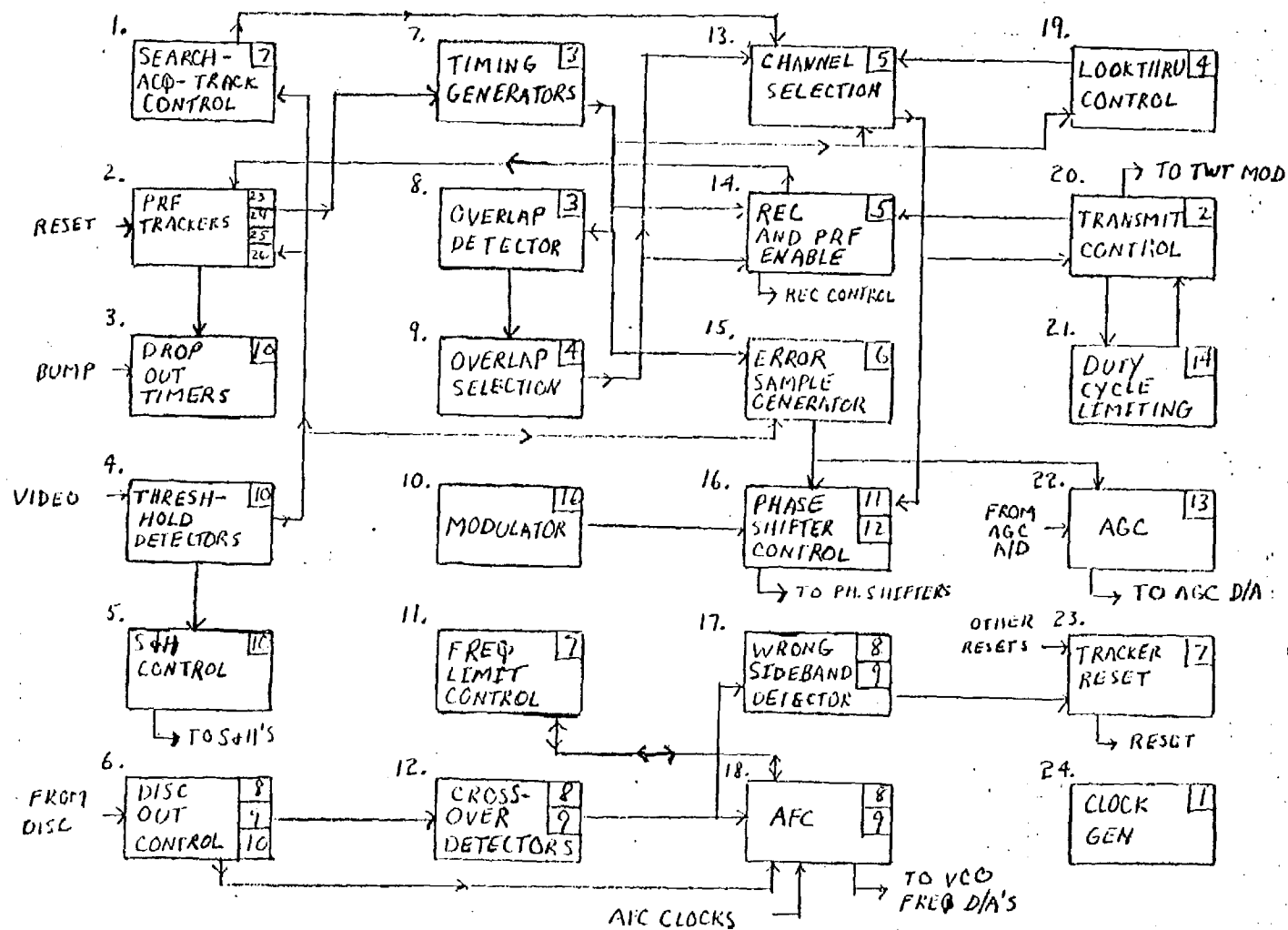


Figure 1-32. Processor-Converter Block Diagram

TABLE 1-6. FUNCTIONAL DESCRIPTION OF PROCESSOR-CONVERTER
BLOCK DIAGRAM

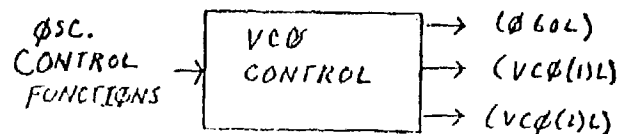
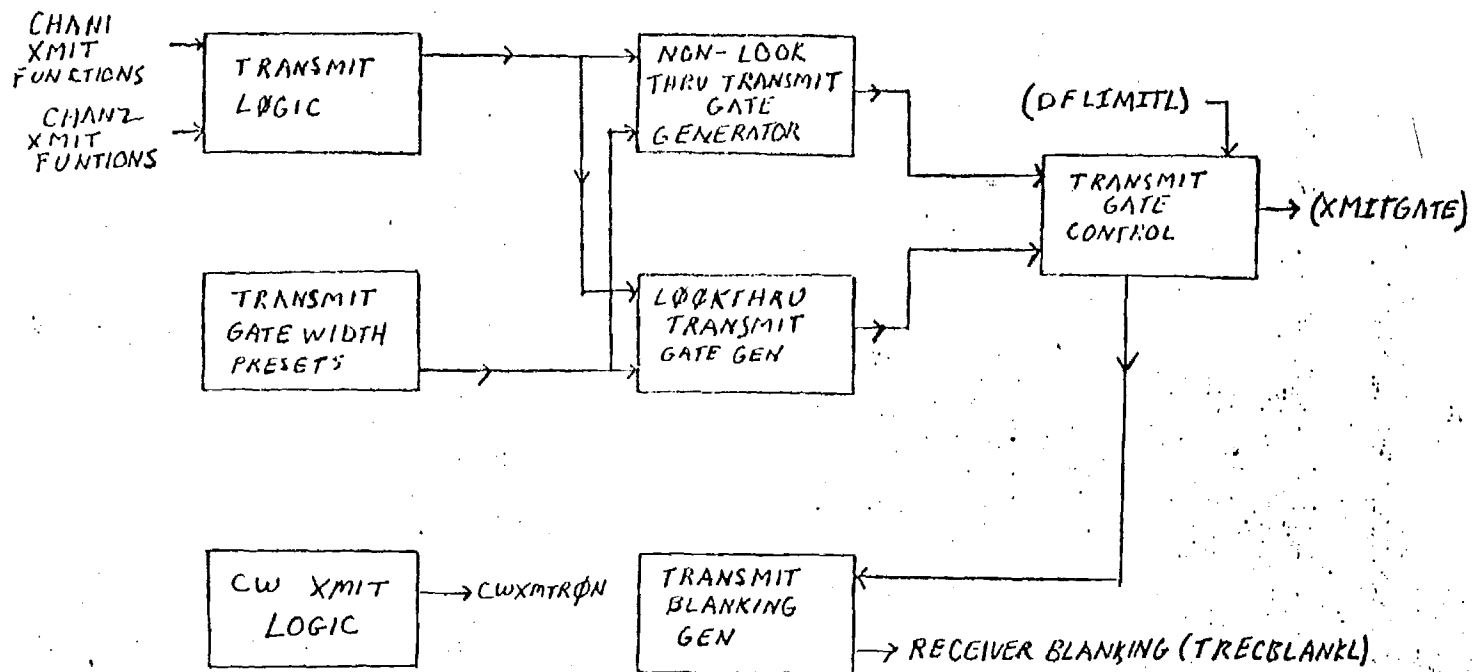
1. SEARCH-ACQ-TRACK CONTROL - Controls search, acquisition, and track modes for each channel.
2. PRF TRACKERS - Tracks PRF signals from 2 different radars and generates pretriggers and PRF gates for each signal.
3. DROP OUT TIMERS - One for each channel. Provides a presettable delay after the PRF trackers drop track and is used to delay search sweep or AGC level adjustment. It is an aid in preventing system instability.
4. THRESHOLD DETECTORS - In conjunction with AGC control establishes minimum signal requirements.
5. S & H CONTROL - Provides the sample and hold (S&H) gates for 3 system samples and hold modules.
6. DISC OUT CONTROL - Provides sampling of discriminator output polarity while a pulse is being received and maintains this on a channelized basis until the next pulse is received for the given channel.
7. TIMING GENERATOR - Provides channelized timing derived from PRF pretriggers to establish phase shifter selection, receiver and PRF gates, and error sampling.
8. OVERLAP DETECTOR - Predicts when channel 1 and channel 2 phase shifter set up periods will interfere with each other.
9. OVERLAP SELECTION - Controls channel selection based on whether or not an overlap is occurring and past history channel selection during overlap.
10. MODULATOR - Provides digital signals for modulation of phase shifter commands.
11. FREQ. LIMIT CONTROL - Provides a plus and minus Δ frequency detector for each channel. When the limit is reached during search, its output causes AFC up/down counter reversal, which in turn reverses the direction of RF tuning.
12. CROSSOVER DETECTORS - One for each channel. Generates an output clock pulse each time the discriminator output changes polarity on a given channel and uses this pulse in establishing IF center frequency tuning criteria.

TABLE 1-6. FUNCTIONAL DESCRIPTION OF PROCESSOR-CONVERTER
BLOCK DIAGRAM (Continued)

13. CHANNEL SELECTION - Selects which channel will receive and/or transmit at any given time.
14. REC AND PRF ENABLE - Provides channelized gates to enable the receiver and PRF trackers at the proper time.
15. ERROR SAMPLE GENERATOR - Controls timing of channelized AGC and phase error sample strobe when conditions for sample generation are met.
16. PHASE SHIFTER CONTROL - Combines and time-multiplexes channelized null and modulation to establish desired phase shifter settings. Phase errors are added to the null reference.
17. WRONG SIDEBAND DETECTOR - Determines whether a signal is being received on the wrong sideband and generates a channelized reset if it is.
18. AFC - Provides channelized control of plus and minus frequency deviation about center frequency.
19. LOOKTHROUGH CONTROL - Establishes all criteria for look-through occurrence.
20. TRANSMIT CONTROL - Establishes conditions for and determines timing and pulse width for transmit pulses during lookthrough and nonlookthrough conditions.
21. DUTY CYCLE LIMITING - Monitors the time that the transmit gate from the TRANSMIT CONTROL is ON and inhibits transmission when the duty cycle factor becomes greater than 2 percent.
22. AGC - Time multiplexes channelized AGC reference to a D/A converter which controls receiver sensitivity. Adds channelized AGC error to its respective reference AGC.
23. TRACKER RESET - Combines channelized resets from several sources to reset the respective PRF tracker for various conditions.
24. CLOCK GEN - Provides several edge-synchronized system clocks.

#3	CHANNEL TIMING OVERLAP DETECTOR	NOT USED
#4	OVERLAP CONTROL LOOKTHRU TIMING	#27 PHASE SHIFT DATA
#5	CHANNEL SELECT REC & PRF ENABLE	#6 SAMPLE GENERATOR
#7	SEARCH-ACQ-TRACK CONTROL AFC CONTROL	#1 CLOCK GENERATOR
#2	TRANSMIT CONTROL	#8 CHN 1 AFC
#10	S&H-A/D-DISC. TIMING DROP OUT TIMER	#9 CHN 2 AFC
#13	AGC CONTROL	#14 DUTY CYCLE LIMITER
#11	γ PHASE SHIFT CONTROL	#22 AGC A/D
#12	ϕ PHASE SHIFT CONTROL	#17 AFC & AGC D/A'S
#16	AMPLITUDE & PHASE MODULATION	#21 RECORDER D/A'S
#23	PRF TRACKER #1	#20 RECORDER D/A'S
#24	PRF TRACKER #2	
#25	PRF TRACKER #3	#18 γ PHASE ERROR A/D
#26	PRF TRACKER #4	#19 ϕ PHASE ERROR A/D

Figure 1-33. Processor-Converter Board Location Diagram



191 starts counting down, having been preset to maximum while ENXMIT was 0. When its count falls below a preset count determined by XGW, (11) LT output = 1, causing XGATEA to go to 1 on the next 5 MHz clock edge. This will produce XMITGATE to the TWT modulator if not inhibited by EXTBLANKL or DFLIMITL. When the 191 reaches minimum count, TTC = 1 disables E. On the next 5 MHz clock edge, XDU goes to 0, TCC goes to 0, and the 191 starts counting up. When XG becomes greater than or equal to XGW, LT goes to 0, and XGATEA goes to 0. This action produces a transmit gate centered about the expected pulse position.

QR2P5MZH is a rephased 2P5MHz clock having a fixed 200ns multiple relationship with SELECT (1) and SELECT (2) so that the transmit pulse will have the same resolution as the PRF (200ns). Using 2P5MHz allows use of a single 191.

By counting the 191 down, a number mating occurs between the XGW at (11) and presets (06) and (13) inputs, since the numbers required for preset are the exact complement 2 of XGW.

The lookthrough transmit gate generator causes a transmit logic pulse to be generated 100 ns after receiving a pulse. The received pulse through (04) sets (05) and (12), and resets (06) and (13). LTTC goes to 0 causing XMITGATE to go to 1 as above. (05) resets on the next clock edge, and (12) resets on the second clock edge, insuring a full clock period for (06) and (13) to preset. When the 9316's time-out, LTTC has produced an XMITGATE = X GATEA width + (0 to 400 ns) (29) and (30) allow only one lookthrough transmit/TG. LOOKTHRUB = 1 during lookthrough and ENPRF = 1 until a pulse is received through (04) and LTTC goes to 0.

When LTBLANKL is switched to 0, no transmission will occur during lookthrough.

LKTC goes to 1 on the next 5 MHz clock edge after LOOKTHRU goes to 1 so that (04) is enabled only during lookthrough.

Lookthrough transmission will never occur until the IF frequency is centered and an error null has occurred on both the γ and ϕ phase servos.

(26) starts receiver blanking and turns off PRF enable immediately when XMITGATE starts. After XMITGATE turns off, the receiver blanking remains on for 0.2 μ sec. and PRF enable remains blanked for 1 μ sec.

(23), (24), (27), (28) and (29) control channel 1 VCO. Flip-flop (27) and (28) functions to hold the VCO on

during lookthrough in the transpond mode, when it is possible for XMITGATEA to last beyond the end of the PRF gate and beyond SELECT (1) going to 0. The function of gate (23) cannot be used without the holding delay of the flip-flop. (25), (26), (30), (31) and (32) provide a similar function for Channel 2.

The CW transmit control is on board two. Although the capability may not be used operationally, a CW response is possible against two threats. As in pulse operation, frequency and PRF track as well as a polarization null are required before the transmitter is enabled. The transmitter is disabled throughout lookthrough and acquisition. In addition, the transmitter is disabled at the pretrigger time preceding the lookthrough event (ACW from board 4), allowing the transmitter output to have time (~ 70 μ sec.) to decay before the threat pulse arrives.

CONECW and CTWOCW indicate which channel is operational (which threat is being countered). CTWOCW selects the polarization control register (1 or 2) on boards 11 X and 12 X which is to be the basis for the phase shifter command.

(3) Timing/Overlap Board 3 (Figure 1-35)

(03), (04), (05) start counting when preset by PRETRIG (1) L and continue to count toward maximum count. 3 decodes are required, each having a fixed relation with the pretrigger. These provide timing gates for the following:

- Start of phase shifter set-up period
- Start of receiver enable
- End of receiver enable.

The following gating pulses are generated:

- Channel selection period
- Receiver enable period
- Transmit enable period

(17) produces the XMITENABLE GATE (XMITG (1)) with the proper 0.6 μ sec. delay from ENMASTER (1) to start the transmission timing leading edge, and with its training edge coincident with ENMASTER (1).

The phase overlap works by having a pretrigger from either PRF tracker preset the counter to the desired overlap criterion interval (see timing information, Figure 1-36). If another pretrig (from the other channel) arrives before the counter times out, the PHOVERLAP flip-flop will be set, indicating overlap.

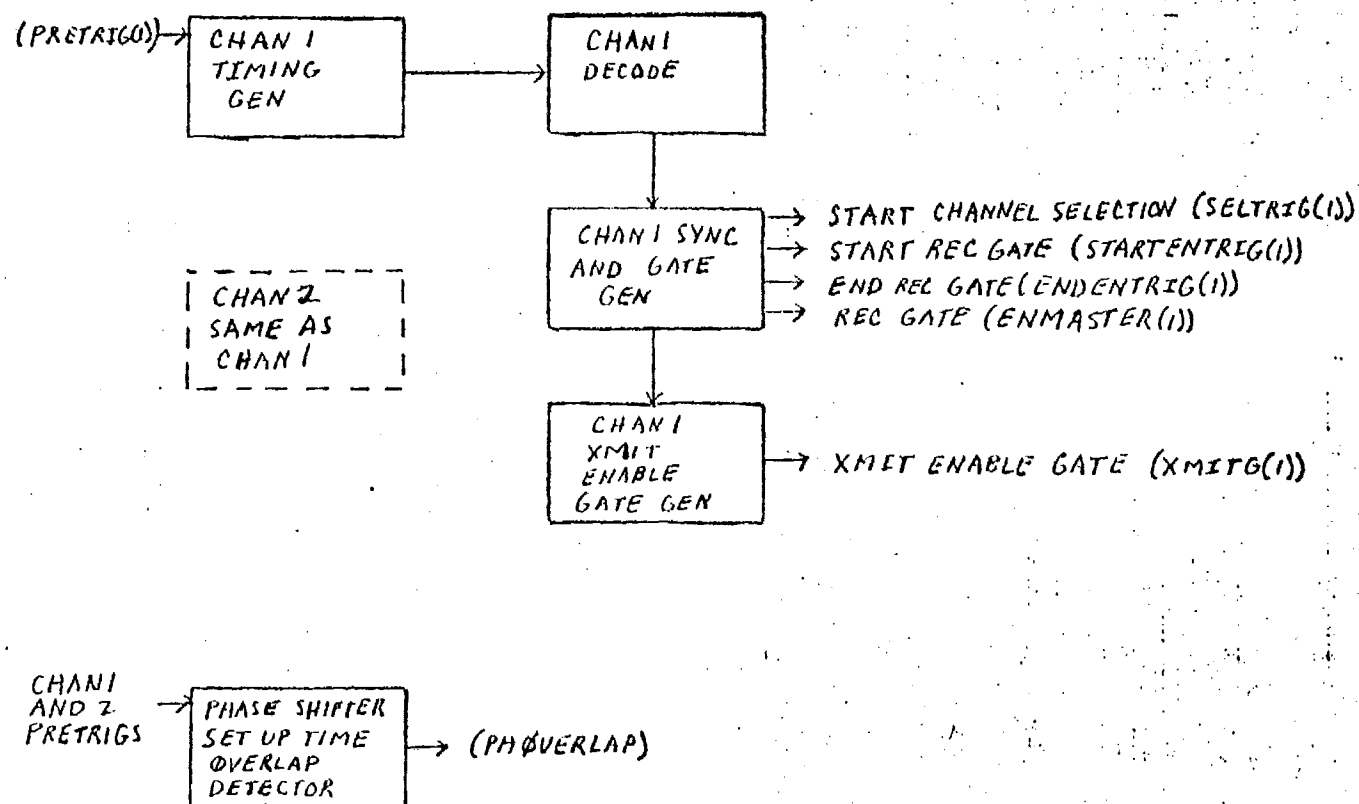


Figure 1-35. Timing/Overlap Board 3 Block Diagram

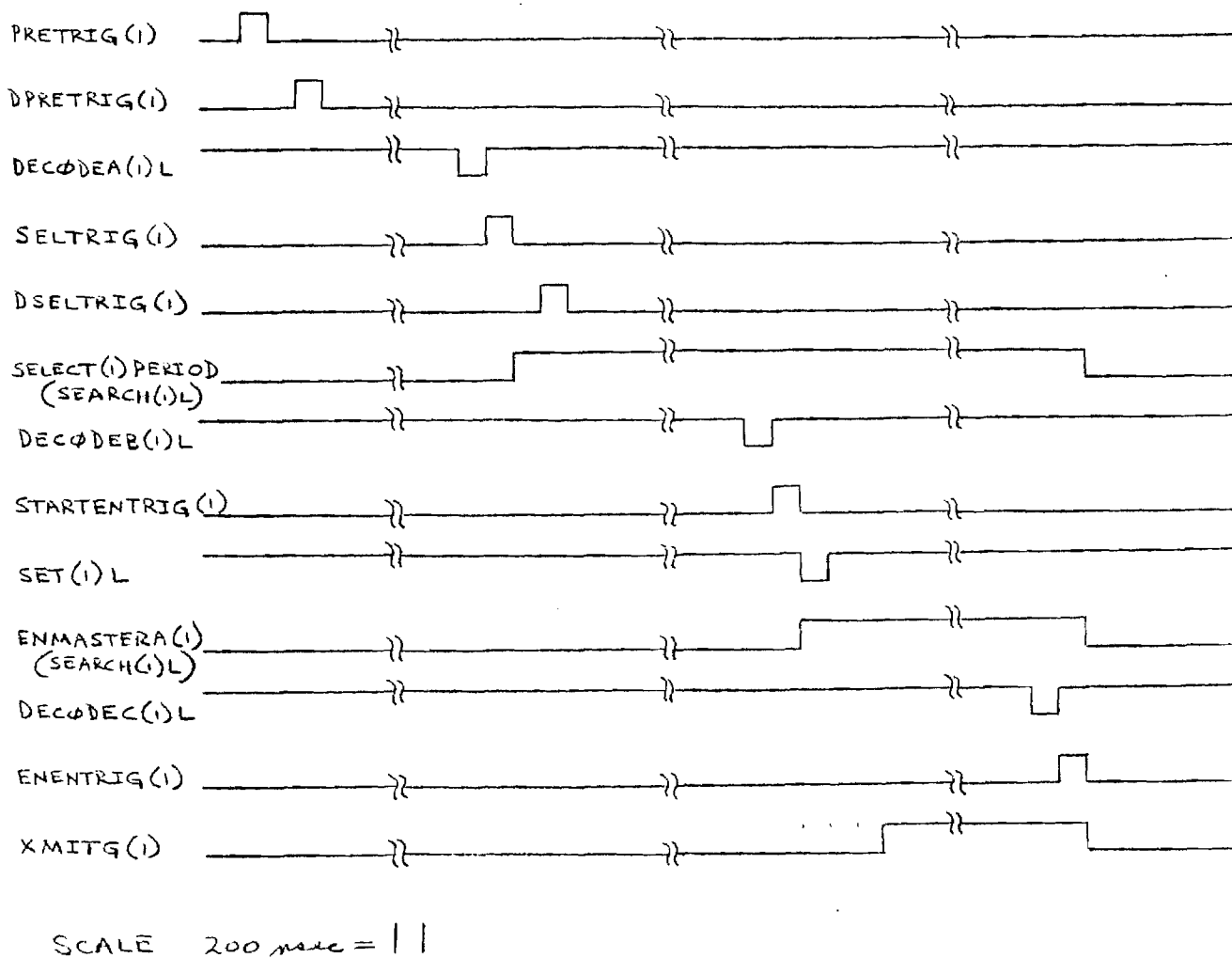


Figure 1-36. Board 3 Timing Diagram

(4) Overlap/Lookthrough Control Board 4
(Figure 1-37)

On sheet 1, the overlap selection circuit determines the alternation rate between the two channels when their phase shifter set-up time is overlapped. (07) is preset by the ALTD signals. A preset to 7 will cause alternation on every other overlap PRF. A preset to 6 will select 2 on one channel then 2 on the other channel, preset 5 will select 3 on one, 3 on the other etc., up to 8 and 8. The following principles are observed:

- (a) When a preset 7 is selected it could mean that one of the phases in the PRF tracker does not get serviced and consequently (03) was added to counter this condition. With it the alternation will be 1212212112122, etc., where 1 and 2 represent channels 1 and 2.
- (b) Only PRF gates occurring during overlap are counted for alternation. This means that:
 - a) when overlap occurs for only 1 PRF, the alternate channel can be selected on the next 1 PRF overlap if the alternation counter so indicates.
 - b) for harmonic PRF's it will insure selection of the one that is at the lowest frequency during long overlap periods.
- (c) (15) provides 200ns delay to allow DSELTRIG(1) to operate on the channel selection circuits before overlap (1) changes.

As shown on sheet 2, channel 1 and 2 lookthrough control are identical. (01) and (02) are preset to the desired lookthrough. Its range is continuous to 1 out of 255 in steps of 1. (01) and (02) are preset when a pulse occurs during lookthrough and they then start to count PRF gates. When terminal count is reached the lookthrough situation is enabled. This lookthrough enable situation will remain until a pulse is received during a lookthrough thereby presetting the counter.

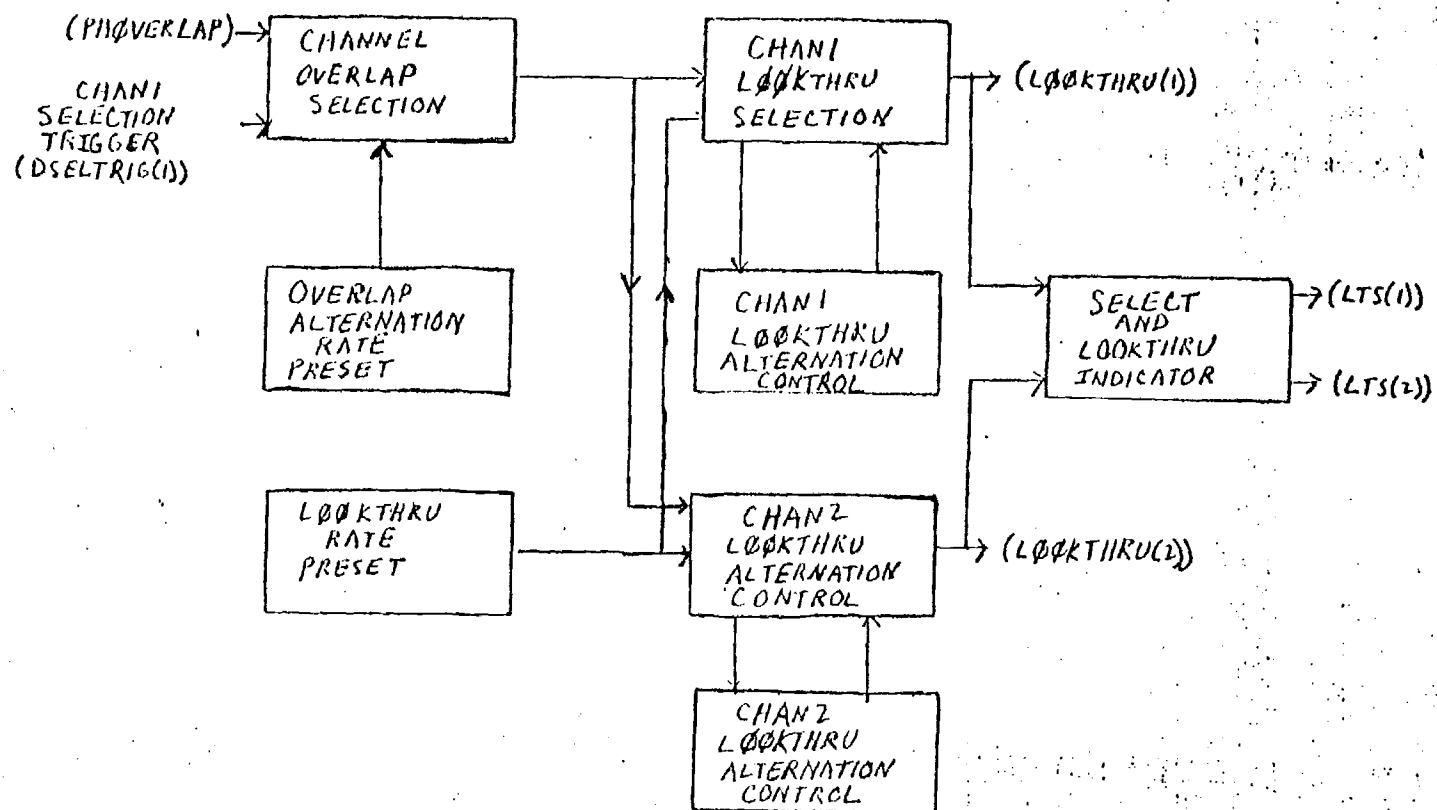


Figure 1-37. Overlap/Lookthrough Control Board 4 Block Diagram

A lookthrough enable does not necessarily mean that a lookthrough will occur, since a lookthrough must also meet the following conditions:

- (a) A lookthrough on a given channel must occur on $2n + 1$ PRF gates following the previous successful lookthrough on the same channel. This is to force rephasing on both PRF tracker phases.
- (b) If overlap is occurring then condition (a) must be met along with the overlap selection control.
- (c) If dual frequency is occurring and the "wait for crosspole" option is used, lookthrough can only occur if the dual F modulation is calling for crosspole on the lookthrough enabled channel and if (a) and (b) are met.

(09) provides (01) and (02) preset synchronization and only allows preset when a pulse is received during an actual lookthrough selection.

PRETRIGA(1) enables (05), causing (05) to alternate with each PRF gate. (14) and (15) are exclusively enabled by setting at F/F (32) and (33). (01) and (02) terminal count enables both (14) and (15), as does (13) output. Then, on the desired PRF gate phase (24) is enabled. DPRETRIGA (1) is delayed 400 ns from PRETRIGA(1). This sets CLT(1) to 1 in F/F (27) and (28) CLT enables (10). The overlap conditions also enable (10 through (03) and (12). (10) output OR's with (11) output in (21), enabling (20). SELTRIG(1) (occurring several μ s after PRETRIG(1)), sets lookthrough indicator (19). At the end of the channel select period (19) is reset by ENDENTRIG(1)L, and CLT(1) is then reset to 0.

A lookthrough is enabled only during the phase shifter set-up time.

During initial acquisition it is desirable to have continuous lookthrough. This is provided by (11) with (34) output control. This will cause continuous lookthrough subject to overlap conditions until both an IF center frequency crossing has occurred and a crosspole null has been achieved.

F/F (32) and (33) is switched when a pulse is received by the PRF tracker during lookthrough as indicated by 200 ns pulses (1)L.

MODSEL (1) forces channel selection during dual frequency. DMOD or a lookthrough will force this, but a lookthrough cannot occur when DMOD = 1 if MODCONTROL into (13) equals 1. DMOD = 1 is the copole condition and lookthrough must await the crosspole condition. This option is turned off when MODCONTROL = 0. CONTL(1) = 0 will force continuous lookthrough (for test purposes), subject to overlap conditions.

SACQ(1)L was added to (19) R input to prevent channel 1 lookthrough during channel 2 acquisition (remember that channel 2 selection is forced during this time, but it is still possible that a tracking channel 1 may try to do a lookthrough during this time unless this change is made).

Also, to force continuous lookthrough starting with the first DSELTRIG(1) during the acquisition period, ACQ(1) was added to (21).

(5) SELECT/REC - PRF Enable Board 5 (Figure 1-38)

This board controls which channel is selected for phase shifter crosspole set up under all combinations of dual frequency, non-dual frequency, search, acquisition, track, one channel on, one channel tracking, both channels on, both channels tracking, etc.

(09) resynchronizes the selection with this clock. F/F (19) and (20) holds a given selection until changed by an opposite channel selection and also provides drive for the select signals.

The cross channel connections in (22) and (24) prevent SELECTC(1)L and SELECTC(2)L from simultaneously going to 1 due to both channels trying to select at once.

This effect can be illustrated in channel 1. With (01) and (02) outputs = 0 and ACQ (1)L = 0, channel 1 should be selected on a priority basis over channel 2. However, if channel 2 is tracking, a DSELTRIG(2)L will be generated. With (26) output = 1, (35) output will hold (30) output at 1. SELTRIG(2)L = 0 would cause (28) to go to 0 for 200 ns (without the cross connection) and both SELECT(1)AL and SELECT(2)AL would simultaneously be 1 for 200 ns. This would result in SELECT(1)AL being 1 for 200ns when it should be 0. Since SELCTC's are used for clocks, (in the phase shifter load strobe generator) the extra edge is not desirable, and it would complicate its usage in other circuits.

Refer to Sheet 2. This circuit provides ENSECFREQ which is used during DUALF to look for the second frequency after the first frequency has been acquired.

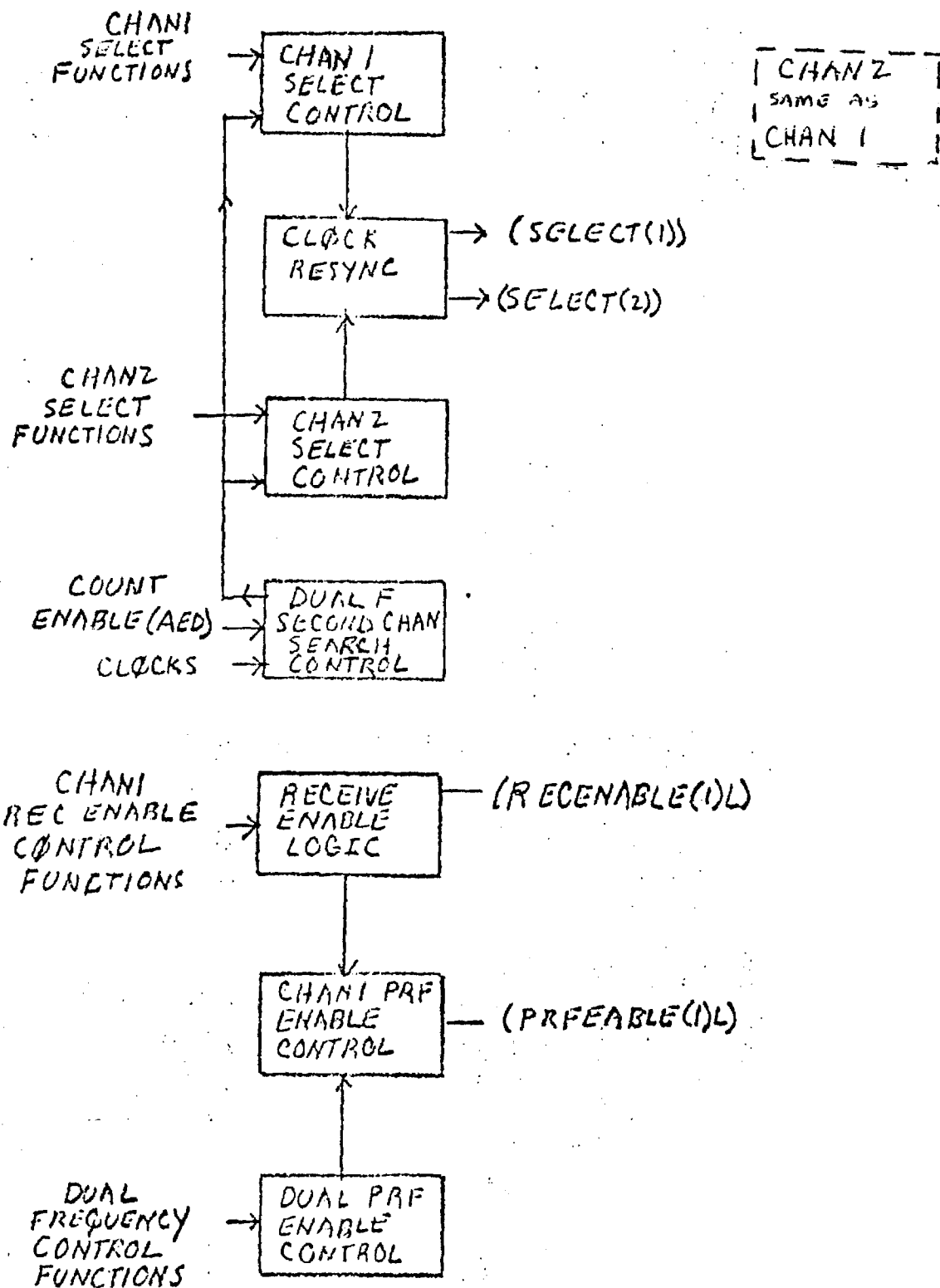


Figure 1-38. Select/REC-PRFENABLE Board 5 Block Diagram

Periodically, once every three seconds (determined by P3HZAL) two or three search sweeps are allowed (as determined by 2.4 HZH) during which time every fourth PRF period of the tracking channel (as determined by the 9316 Modulo 4 counter) is used to enable the nontracking channel during the search sweep. This allows the acquired channel to maintain track while trying to locate the untracked frequency.

The RECENABLE circuit consist of combinational logic to implement the following equation:

$$\begin{aligned} \text{RECENABLEB}(1) = & \text{TRECBLANKL} \cdot \text{EXBLANKL} \cdot \text{SBLANKL} \cdot \\ & \{ \text{SELECT}(1) \cdot \text{ENMASTER}(1) \cdot \text{PRFTRACKA}(1) \\ & + \text{DUALF} \cdot [\text{SEARCH}(1) \cdot \text{PRFTRACKA}(2)\text{L} \\ & + \text{ACQ}(1) \cdot \text{TG}(1) \cdot \text{PRFTRACK}(2)\text{L}] \\ & + \text{DUALF} \cdot \text{ENMASTER}(2) \cdot [\text{SEARCH}(1) \cdot \text{ENSECFREQ} \\ & + \text{ACQ}(1) \cdot \text{PRFTRACK}(2)] \\ & + \text{DUALFL} \cdot [\text{SEARCH}(1) \cdot \text{ENMASTER}(2)\text{L} \\ & + \text{ACQ}(1) \cdot \text{TG}(1)] \} \end{aligned}$$

PRFENABLE is a combination of RECENABLE and some other factors and is an implementation of the following equation:

$$\text{PRFENABLE}(1) = \text{PPDDR}(1) + \text{RECENABLEB}(1) \cdot \text{DRECEN}(1)$$

The start of PRFENABLE is delayed 0.8 s by DRECEN(1) out of (18) and is inhibited by TRECBLANKL during transmit and for 1 μ s afterwards

(08), (09), and (10) provide logic for coupling the 2 channel PREENABLEs together during dual frequency operation according to the following equation:

$$\text{PDDR}(1) = \text{DUALF} \cdot \text{PRFTRACKA}(1) \cdot \text{PRFTRACKA}(2) \cdot \text{DRECEN}(2) \cdot \text{RECENABLEB}(2)$$

(6) Sample Generator Board 6 (Figure 1-39)

The sample strobe generator operates as follows: If a pulse (HIT) is received during lookthrough (LTS) when the corresponding channel is selected (SELECT) and this is indicated at the end of the PRF gate (ENDENTRIG), then (01) and (02) are preset to a value corresponding to the AGC and phase error settling times. Also (referring to channel 1) (22) is set, indicating the sample select period (SSELECT)(1). (22) enables (30). When (01) and (02) time out, STCTC goes to 1, (27) produces a 200 ns sample (1) pulse through (30). (Note that lookthrough cannot occur until the fifth pulse during the acquisition gate, so that a sample pulse cannot be generated until tracking has started.)

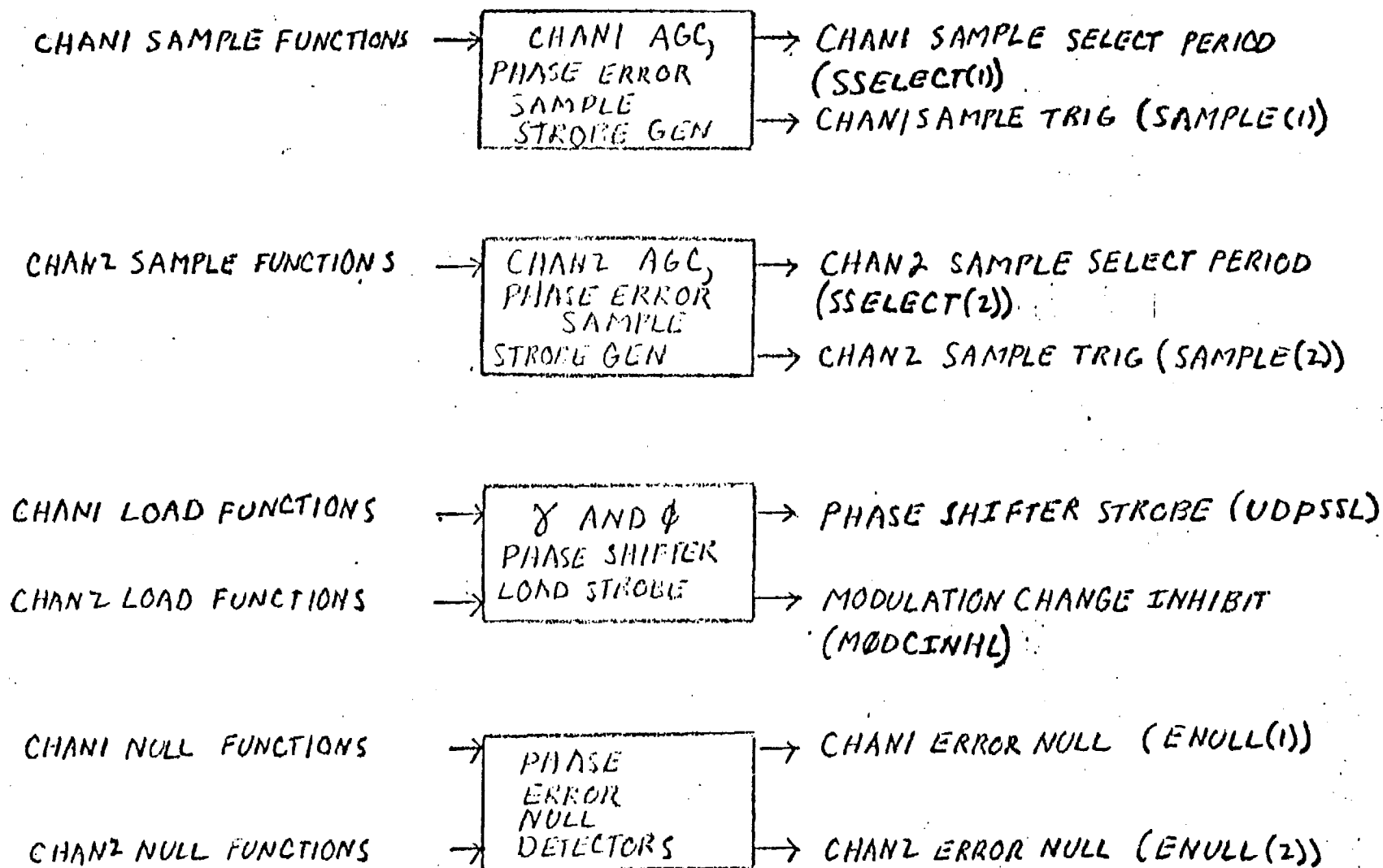


Figure 1-39. Sample Generator Board 6 Block Diagram

The phase shifter load strobe generator works as follows (refer to channel 1 operation, since channel 2 operation is identical): a 1 at (14) output sets F/F (15) and (16); Q2 on (24) goes to 0, because it is reset by (15) zero output. This causes UDPSSL to go to 0, which will set (3). If SELECTC(1) has toggled (03), (14) will go to 0 and (15) and (16) will flip back the other way and (15) out will then be 1.

The continuous 1 applied to (24) D0 will be propagated to (24) Q2 by the clock input. UDPSS will be 0.8 to 1.2 μ s long, depending on how the clock edges line up with the reset. This allows at least 0.6 μ s for phase shifter data set-up time and propagation of modulation changes. A similar action occurs during acquisition when PRF track begins (the DSELTRIGs start). The only difference is that DSELTRIG lasts 200 ns and will delay the reset of (15) and (16) by 200 ns and probably extend the tracking edge of UDPSS by 200 ns. This is not critical. (08) generates a gate to inhibit crosspole modulation changes during phase shifter strobe time. Referring to sheet 2, the error null circuit operates as follows, using channel 1 as an example: When DOT(1)L and HOLD(1)L are 1, as they are after a BUMP or search condition in the automatic search mode, flip-flop (6) and (7) is reset so that ENULL(1) = 0 indicating no phase null.

On two boards (18 and 19), are 2 error threshold detectors, one for γ and one for ϕ . When the error of both and falls below these preset thresholds as SAMPLE(1) strobe occurs, then the ENULL(1) flip-flop will be set. It cannot be reset again until both DOT(1)L and HOLD(1)L go to 1. Significantly, if the search AFC off mode is used, the ENULL(1) cannot be reset except with a BUMP. This is one factor allowing transmission to begin immediately when the track is reestablished. TRACK (1) and TRACK (2) are buffered track indication signals to the front panel indicators, which indicate current null conditions via (10 through (18).

(7) SEARCH-ACQ-TRACK-AFC Control Board 7
(Figure 1-40)

During search activity on either channel as determined by (01) and (02), a received pulse may pass through (20) resetting counter, (29) and starting the acquisition period as indicated by ACQAL = 0. The leading edge of ACQB clocks (14) or (15) depending on which one is enabled thus starting a channelized ACQ gate. (03) is enabled by ACQ(1). When ACQL goes to 1 at the end of the acquisition period, (14) is reset. ACQL leads ACQB by one gate to prevent race. (20) is also enabled by PRFENABLE and inhibited by FREQJUMPL after each acquisition gate. The PRF enable prevents spurious triggering of (29). FREQJUMP prevents acquisition when skipping over an IF band through (24),

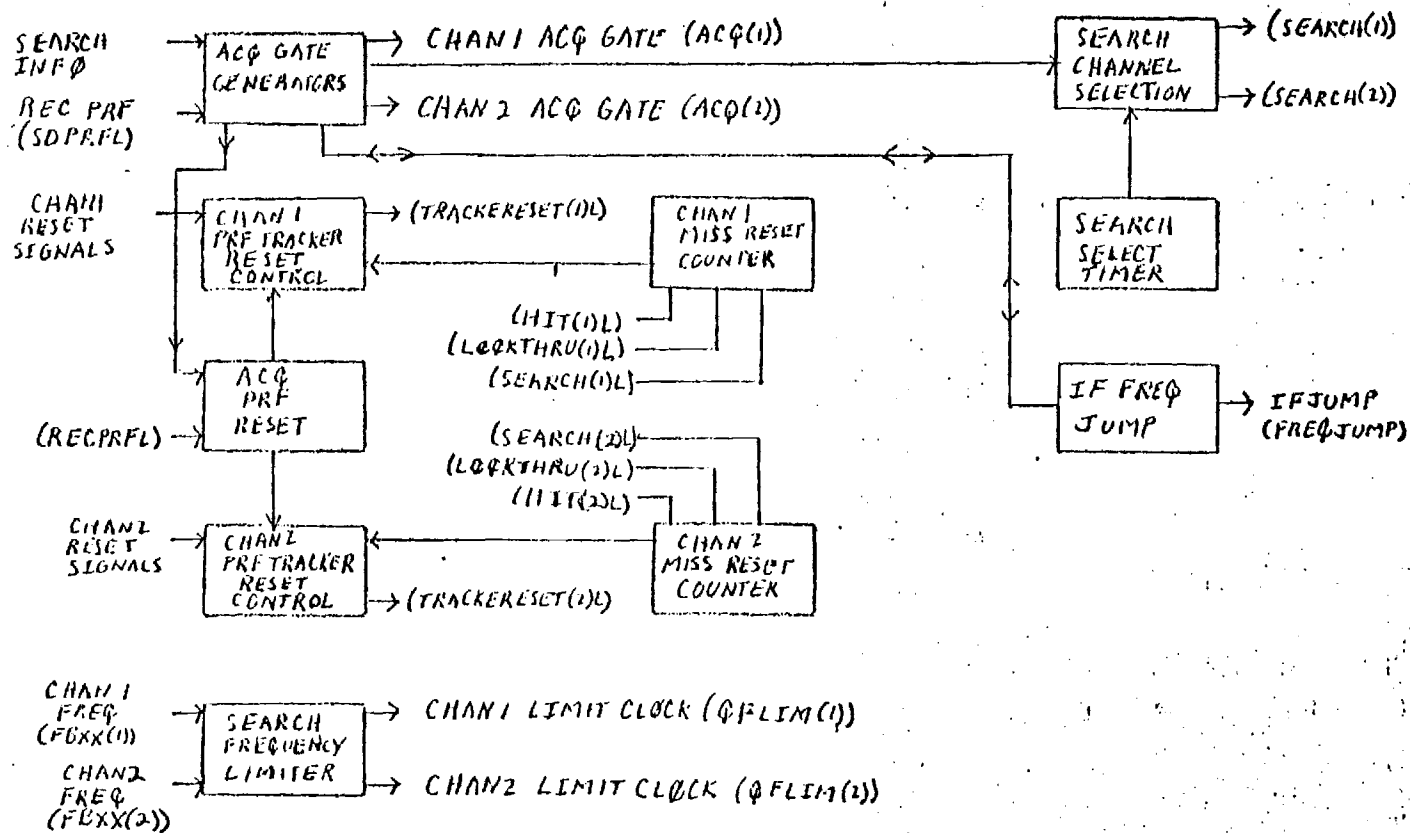


Figure 1-40. Search-ACQ-Track-AFC Control Board 7 Block Diagram

on Sheet 3. (35), (36), (37) and (38) distribute loading of the acquisition gate. (40) and (41) force search to the opposite channel when only one channel is tracking and prevents search in a tracking channel or an off channel.

LIMPRF is derived from the discriminator limiter output. A 10 MHz band pass filter is ahead of the limiter. This insures that an acquisition is started only if the received signal is within the 10 MHz pass band and avoids the problem of putting two filters in a phase sensitive location ahead of the Σ and Δ receivers. This also affects IF center dropout criteria. (21) determines which channel is selected for search. (26) and (27) provide search inhibiting functions.

The LIMPRF function is currently not used and should be tied to true condition.

(16), (17), (22) and (34) combine channel 1 tracker reset functions. Reset occurs:

- (a) Through (16) if (08) times-out during acquisition. (DOT(1)L = 1 during this time.)
- (b) Through (17) if channel is off or a BUMP signal occurs, causing CRESET(1)L to momentarily go to 0; CRESET(1)L also goes to 0 if a sideband reset condition occurs.
- (c) Through (22) if the lookthrough miss counter has timed-out.
- (d) Through (34) during channel 1 search.

(08) will time-out during the acquisition pulse unless continuous PRFs are received during acquisition and no two pulses have a separation greater than about 1.6 ms.

(28) provides timing for FREQJUMP. Its purpose is to inhibit an acquisition cycle while the search frequency sweeps through the 10 MHz IF band. (28) is preset through (02), (see Sheet 2), causing a FREQJUMP whenever CRESET(1)L, CRESET(2)L, or SFLIPA occurs. CRESET(1)L occurs whenever a channel one bump or a channel one sideband reset occurs. SFLIPA occurs at the end of each acquisition period and periodically as a result of (1), from sheet 2.

(01) on sheet 2 will cause search to slowly alternate between channels if no acquisition periods occur. Its purpose is to insure that the system will not lock up on a dead channel.

(1) and (12) count missing pulses during lookthrough. A HIT (received pulse) during lookthrough will reset the counter. If seven consecutive misses occur, MISSRES goes to 1, causing tracker reset.

(03) and (04) provide a high loading capability for PRFTRACKA(2) and PRFTRACKA(2)L. (22) is a buffer to the PRFTRACK recorder decode on board 14.

(20) prevents channel one lookthrough during channel two acquisition and insures channel one lookthrough reset when channel one search occurs. (21) performs identically for channel two.

Sheet three is primarily concerned with search frequency limiting and serves this function for both channels. Channel frequency offset code is selected by multiplexer (01) and (02). This code may represent either a plus or minus deviation from the center frequency established elsewhere. If the frequency code is negative, it is converted to absolute value in multiplexer (10) and (11) by inversion, ignoring the LSB inaccuracy. As many bits are carried as possible, using two packages per stage.

A preset frequency deviation limit (SLIM) is set by the switches and input comparator (13) and (14). When the frequency deviation exceeds the preset limit, GTI goes to 1 from (14), causing QFLIML to go to 0. The timing is as follows:

- (a) Q2P5 MHZBH causes a frequency change.
- (b) GTI goes to 1.
- (c) Q2P4KHZBL goes to 1, clocking (15) and QFLIM goes to 0.
- (d) QFLIM(1) goes to 0 if SEARCH(1)L = 0.
- (e) The rising edge of QFLIM(1) clocks (12) on sheet 1, board 8.
- (f) QFLIM(1) inverts through (26) and LIMRES(1)L goes to 0.
- (g) FQJUMP goes to 0, preventing an acquisition period from starting through (20) on sheet 1.
- (h) LIMRES(1)L maintains the channel one PRF tracker in the reset condition through (34) on sheet 1.

As long as channel one search is maintained and GTI = 1, QFLIM(1) will remain 1 so that multiple clockings will not occur, since the direction of frequency scan should be changed only once, until GTI goes to 0. This will insure that if the Δ frequency is ever greater than the band limit, for any reason, scanning will continue in the same direction until the frequency is again in the right band. The acquisition cycle is inhibited in search mode and GTI = 1, so that it is not possible to go out of search mode unless the frequency is in the right band. To prevent GTI from fluctuating due to alternate frequency selection by (01) and (02) (such as with one channel tracking and one channel in search mode), SEARCH(1)L is used for frequency selection.

Example: If QFLIML = 0 and SEARCH(1)L = 0 then channel one frequency is selected continuously and QFLIM(1)L = 1 continuously until GTI goes to 0 or SEARCH(1)L goes to 1.

- (a) If both channels are not tracking and a switch to alternate channel search is made and both channel 1 and 2 frequencies are within band limits, an occasional malfunction may cause (15) to switch and clock the corresponding Up/Down control flip-flop on board 8 or 9. This should not matter because the search scan will usually have the opportunity to sweep in the correct direction.
- (b) If SEARCH(1)L = 1, Channel 2 may be in search mode. If it is, frequency comparisons will cause up/down control clocking via QFLIM(2). If it is not, QFLIM(2) will be inhibited because SEARCH(2)L = 1. A channel cannot go out of search and into acquisition while it is outside the Δ band limits.

FQJUMPL from (25) inhibits the acquisition mode.

EXTBLANK comes from a BNC front panel jack. When EXTBLANKL = 0 both the receiver and transmitter function are blanked. The 5.1V Zener provides overvoltage protection for (12). This function has been removed from the front panel.

(22) and (23) provide drive for the Channel 1 and 2 off signals.

(03) through (09) supply frequency complement data to (10) and (11).

(8) Channel 1 AFC Board 8 (Figure 1-41)

This board controls Channel 1 AFC. (12) determines whether Δ frequency counter (5) and (6) counts up or down during search mode, controlled through (1) and (8). The frequency clock, QAFCL(1) is controlled through (10) during search and through (9) when not in search.

AFCDISABLE(1) is a front panel control used during test to prevent any clocks from changing the frequency. During SEARCH(1) the search clock is inhibited by HD(1)L. HD(1)L is described later.

QAFCL into (4) is common to both channels. Whether or not it affects Channel 1 is determined by SELECT(1)L and SSELECT(1)L through (3). These two signals overlap and allow QAFCL to operate slightly after the end of the PRF gate when necessary, as would be the case if a pulse was received very late in the gate.

Frequency counter (5), (6), (7) and (11) is a nine bit up/down counter whose output is used to determine, in 2's complement form, the frequency deviation from the center frequency set on the front panel. The FB outputs go to a PROM, then to a bipolar D/A converter and thence to a 741 op amp which adds the center frequency to the offset frequency.

AFCZEROL is a front panel switch which sets the counter to zero offset (all 0's) so that the center frequency can be independently adjusted.

On sheet 2, (1), (2), (9), (10), (19), (20) and (21) comprise an IF center frequency crossover detector. Each time DOWN(1) changes polarity, a 1.6 μ s 0 going clock pulse (QCROSS(1)) is generated, and DOWN(1) flips whenever the channel 1 sampled discriminator output flips. Unless PRF track is established, CR(1)L maintains (8) in the reset condition. After track is established, the 1 at pin D0 propagates on QCROSS(1) command. The second QCROSS(1) after track starts puts a 1 on Q1. This should mean that the IF center frequency has been crossed over twice. This is indicated by IF CENTER(1) = 1. Four crossovers later AGZ(1) goes to 1. If AUTOSEARCHL = 1, AFCINH(1)L goes to 0. This causes HOLD(1)L to go to 0 and therefore HD(1)L goes to 0. HD(1)L prevents search frequency sweep through (10) on sheet 1 as does DOT(1)L = 1 (when the timer is not timed-out). This is probably the most desirable operation mode.

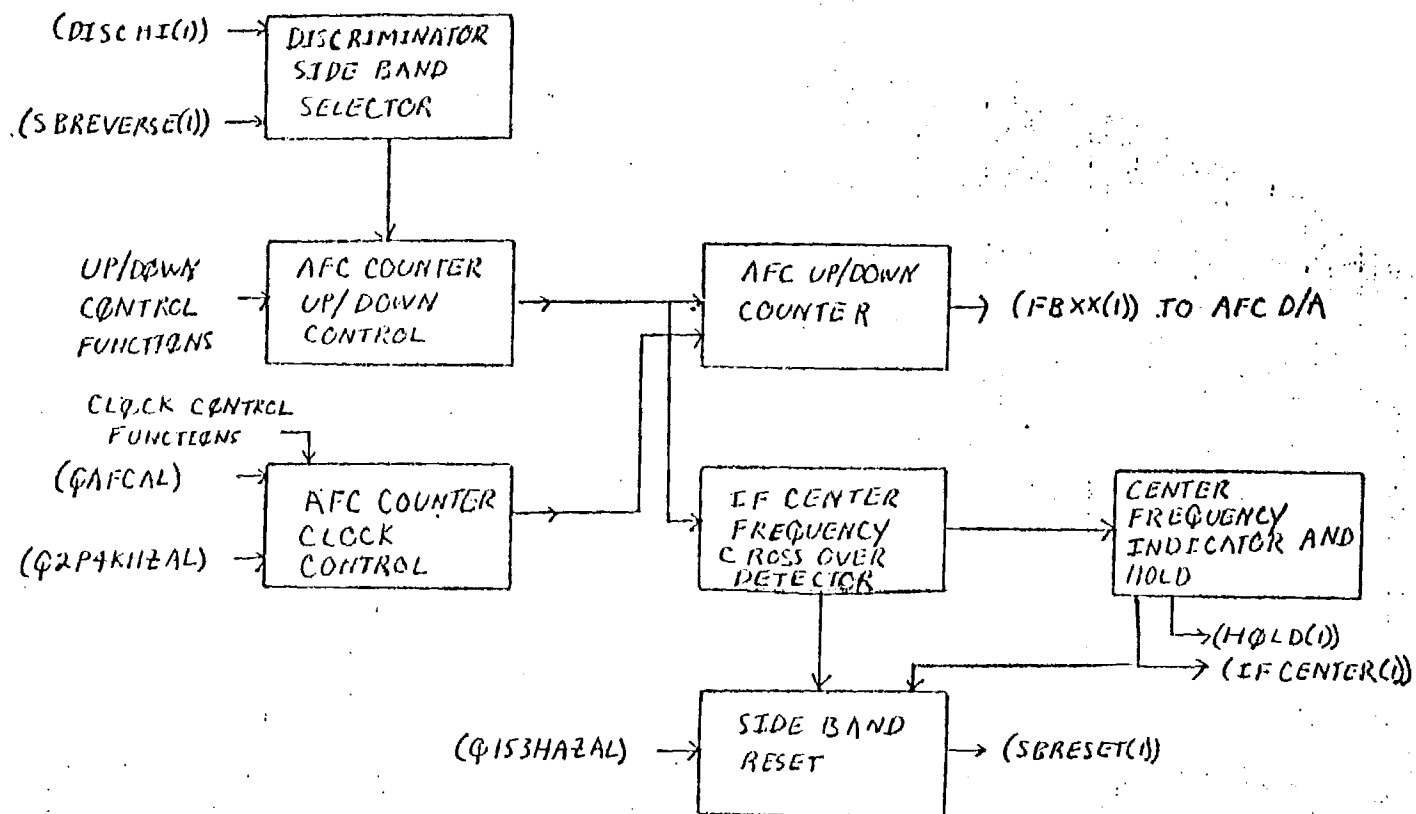


Figure 1-41. Channel 1 AFC Board 8 Block Diagram
(Identical to Channel AFC Board 9 Block Diagram)

If AUTOSEARCHL = 0, (13) has no effect (AUTOSEARCHL is set by an internal switch on board 10) and as soon as DOT(1)L goes to 0 frequency search will resume automatic search frequency sweep. With AUTOSEARCHL = 1, after track is once established search sweep will never again occur, unless the pilot's BUMP switch is depressed. This causes DOT(1) and CR(1)L to go to 0.

To control the track frequency in a way similar to that used in the search frequency, AFCINH(1)L goes through a switch on board 2 and then to (9) and sheet 1 as AFCINH(1)AL.

(6), (7), (11), (12), and (15) select whether the correct signal will be received above or below LO frequency, as determined by SBREVERSE(1) Switch on board 2. (22) will cause a PRF tracker reset if the crossover interval exceeds about .1 sec. It only counts after track is established, when DOT(1)L = 1. If IF CENTER(1) goes to 1 before SBRESET(1), count will stop and no SBRESET(1) can occur after that. ACQBL (acquisition gate) initially resets (22) to 0 as does each QCROSS(1) clock. AFCDISABLE into (20) holds (22) in reset so that there is no change of SBRESET(1) occurring during this time.

For proper operation the DOT timer should be set longer than the time required for the AFC to pull on to center frequency after initial acquisition. (23), (24) and (25) are lamp drivers to front panel indicator lamps.

Normal AFC would be:

AFCINH(1)AL = 1

AUTOSEARCHL = 1

AFCZEROL = 1

AFCDISABLELE = 1

(9) Channel 2 AFC Board 9

Operation of this circuit is identical to that of channel 1 AFC Board 8.

(10) Dropout Timer Board 10 (Figure 1-42)

This board contains the dropout timers (DOT) for both channels. After PRF track is established the DOT is preset as determined by DPRES signals set by the switches. Normally gates (13) through (20) are enabled and PRFTRACKA (1) causes continuous preset to occur through (5). If PRF track is

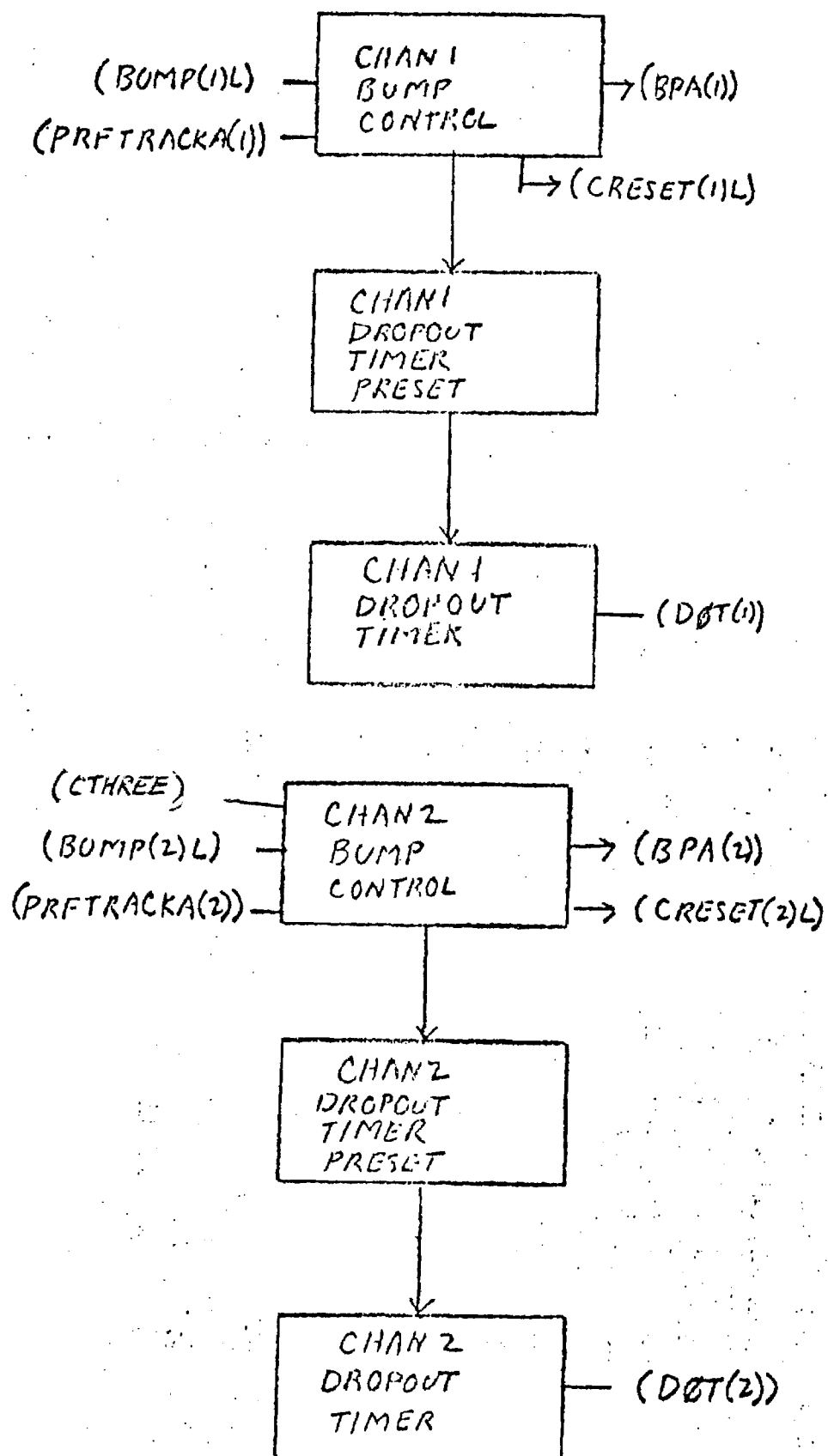


Figure 1-42. Dropout Timer Board 10 Block Diagram

dropped (24) and (25) will count until terminal count, causing dropout timer time-out. Terminal count condition is maintained until another preset occurs.

If it is desired to reset or BUMP Channel 1, a momentary depression of the BUMP (1) button on the Processor-Converter front panel will cause BUMP (1)L to go to 0. All DPs go to 1, DLD(1)L goes to 0 and (24) and (25) are forced to terminal count. BPA(1) and CRESET(1)L are reset functions used elsewhere. When a sideband reset condition occurs, SBRESET(1) goes to 1, forcing (24) and (25) to terminal count.

Channel 2 is automatically bumped if the system is countering three threats. In this mode, CTHREE, from the X band RF receiver, will change state, indicating that the second receiver VCO has changed from frequency 2 to 3 or from 3 to 2. These transitions are caught in flip-flops, and have the same effect as a manual BUMP on channel 2.

(11) Gamma Error Processor - Board 11X (Figure 1-43)

The γ input error from the γ A/D converter, board 18, is buffered and applied to the 8 least significant bits of the error adder. The adder output is multiplexed with the MANUAL GAMMA INPUT switches and applied to the channel 1 and 2 gamma registers. A multiplexer on the output of these registers selects the second input to the error adder when the error loop is to be updated (during lookthrough). Another multiplexer on the register outputs selects channelized data to be applied to the modulation adder.

The error adder logic on sheet 3 controls the error adder function. During lookthrough, ORSSELECT=1, and a Processor-Converter front panel switch controls the extent of the error correction: full count or just one count. When the error loop is not being updated, ORSSELECT=0, and the register contents selected by the error adder multiplexer are passed through to the manual/cross pol multiplexer.

The nine bits from the three octal MANUAL GAMMA switches are applied to the 9 most significant bits of the manual/cross pol multiplexer. This multiplexer is controlled by logic on board 12X. Basically, the manual switch data is loaded into the registers during search or when commanded by the front panel switches.

Input data is strobed into the gamma registers on the rising edge of LOAD. SAMPLE () occurs at the end of SSELECT (after lookthrough) and updates the loop based on error information. RSW loads the manual switch data during search.

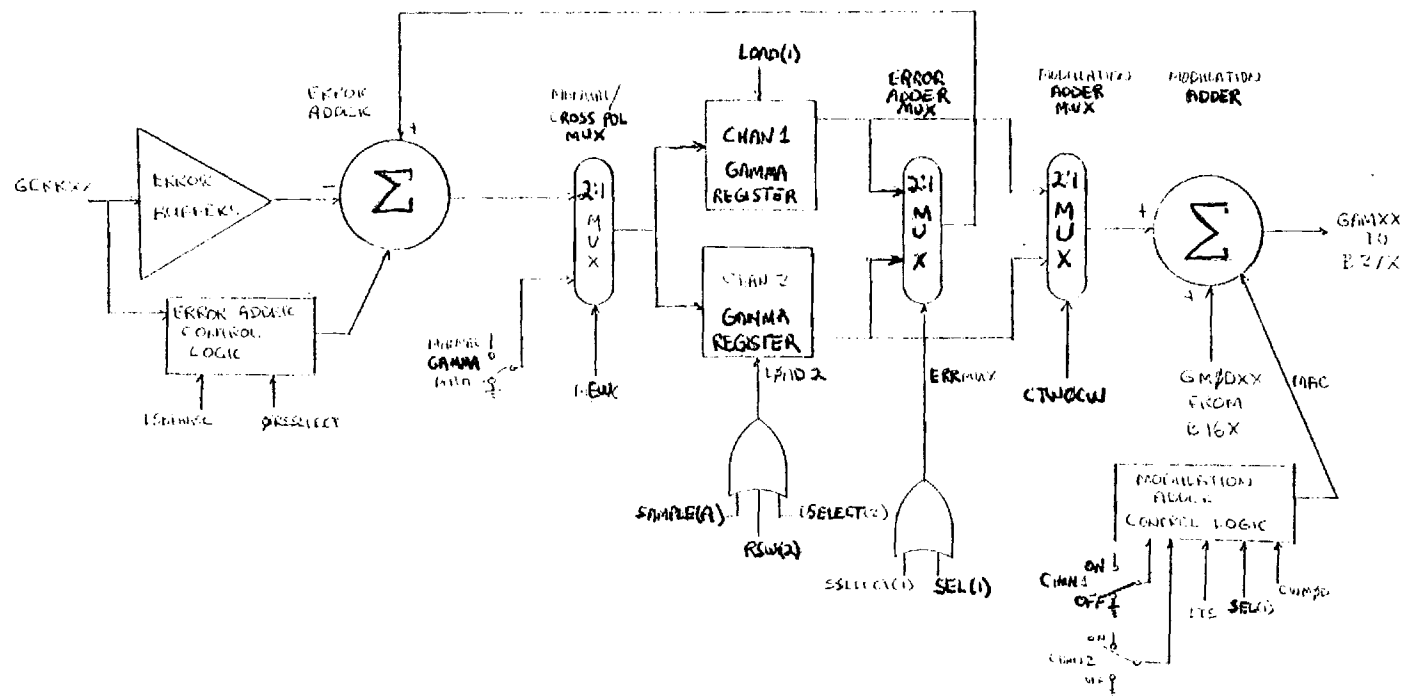


Figure 1-43. GAMMA ERROR Processor Board 11X Block Diagram

DSELECT allows the rate-aided increment to be added into the current register contents. The effect on board 11X is to load the register with itself, since the rate increment is only added to the phase command (board 12X). If enabled, the rate increment is added in before either a transmit or receive event.

The modulation adder control logic controls the function of the modulation adder. The modulation is ignored for a lookthrough event so that the cross pol error loop can be updated. The polarization modulation may be applied to either or both channels. However, if it is applied to both channels, they will have the same modulation. The modulation information is added to the eight most significant bits.

(12) Phi Error Processor - Board 12X (Figure 1-44)

Board 12X is similar to board 11X; however, a rate-aided function has been added. A rate-aided adder adds a fixed amount, determined by the MANUAL RATE INCREMENT switches, before each transmit and receive event, depending on the channelized front panel switches. The 9 rate increment bits are sign extended and added to the middle significant bits in the error loop.

On sheet 2, the most significant phase bit, the sign bit, is changed whenever the signs of the modulated and unmodulated γ data are different.

The table below describes the relationship between various variables in the polarization control servo in terms of the number of bits and interpretation in processor degrees. The basic error loop has 12 bits spanning 360° , so the LSB has a value of 0.088° . The input error data is an eight bit quantity, connected directly to the 8 LSB's of the error loop. The other variables are all less than 12 bits and are not aligned with the LSB.

Servo Loop Variable Relationships

<u>Variable</u>	<u>Bits</u>	<u>LSB Value (Deg.)</u>	<u>Max. Pos. Value (Deg.)</u>	<u>Min. Neg. Value (Deg.)</u>
Error Loop	12	0.088	179.012	-180.0
Error Data	8	0.088	11.162	- 11.25
Manual Gamma, Phi	9	0.703	179.297	-180.0
Gamma, Phi Modulation	8	1.406	178.594	-180.0
Rate Increment	9	0.176	44.824	- 45.0

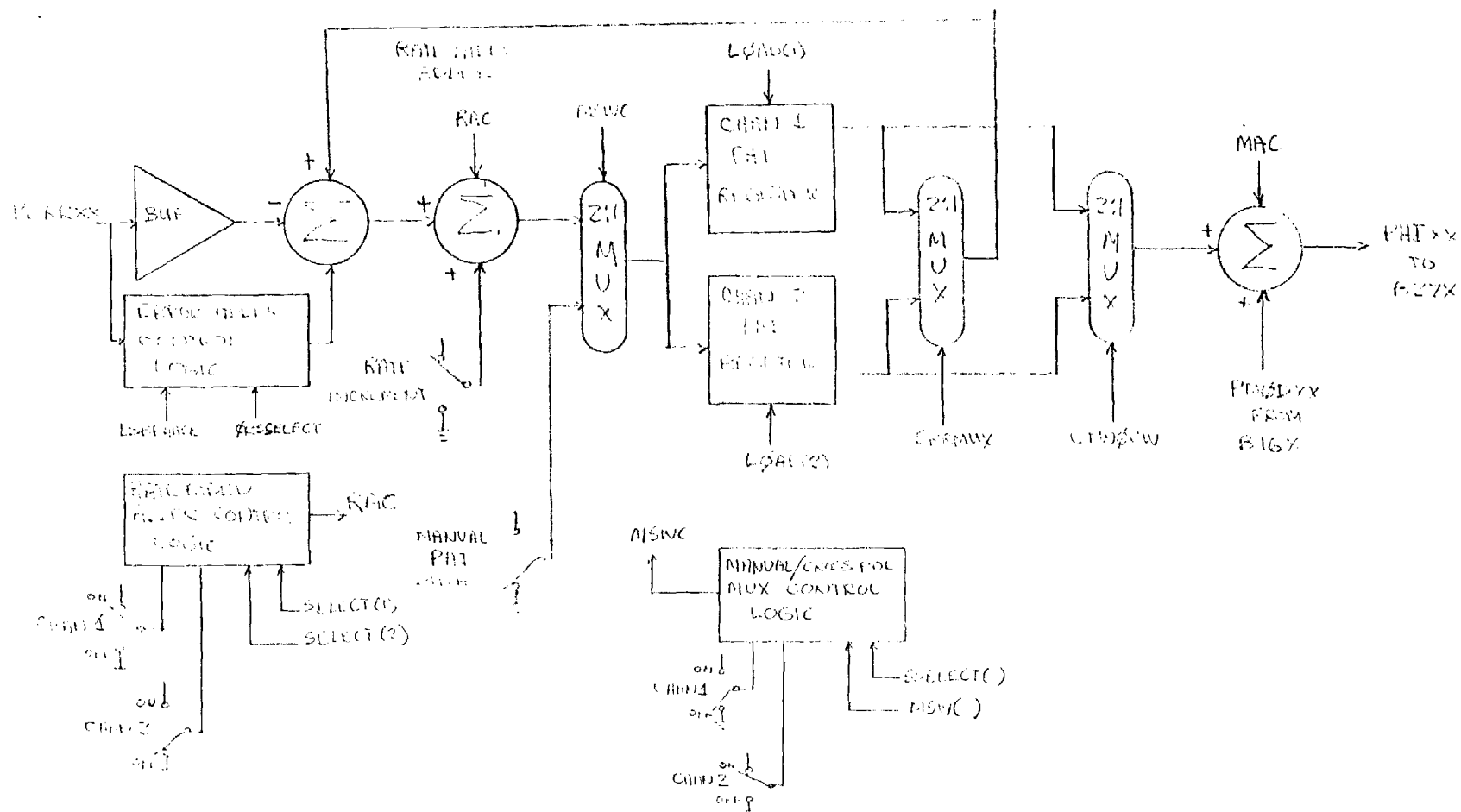


Figure 1-44. PHI Error Processor Board 12X Block Diagram

As a further aid, the table below gives the processor phase for several settings of the front panel octal switches. The data for the gamma and phi switches between the 400 and 777 settings are listed as positive angles greater than 180° , although the processor treats them as negative angles less than 180° ($-135 = 360-135 = 225$).

The processor phase commands are sent to the polarizer where they are translated by ultraviolet PROMS into phase shifter phase commands. The interaction of the polarizer and the incoming RF polarization phase is sensed by a phase detector and converted back into processor phase information.

Switch Settings in Terms of Processor Phase

<u>Switch Setting (octal)</u>	<u>Gamma, Phi (degree)</u>	<u>Rate Increment (degree/PRI)</u>
000	0.0	0.0
001	0.7	0.2
010	5.6	1.4
100	45.0	11.2
200	90.0	22.5
300	135.0	33.7
377	179.3	44.8
400	180.0	-45.0
500	225.0	-33.7
600	270.0	-22.5
700	315.0	-11.2
777	359.3	- 0.2

(13) AGC Board 13 (Figure 1-45)

The AGC control for both channels is on this board, on sheets 1, 2 and 3. Sheet 4 contains part of the S&H and discriminator strobe timing, the rest of which is co-located on board 10 with the Dropout Timer. The AGC is similar to the

Figure 1-45. AGC Board 13 Block Diagram

Phase Shift processor. The AGC error is added to the existing AGC level from the Channel 1 and 2 AGC registers through MUX (10), (11), (12), and (14) on sheet 2, the error channel selector. The REC AGC channel selection MUX selects which channel AGC is applied to the receiver. Its output, AGCB, goes to the AGC PROM LINEARIZER on sheet 3. AGC error is in dB derived from the linear AGC error through the PROMs on sheet 5. The dB vs AGC voltage characteristic is translated in the AGC PROM LINEARIZER. Its output goes to a D/A converter for application to the receiver.

The error channel selection is a 4/1 multiplexer which selects one of the following: current channel 1 AGC, current channel 2 AGC, search AGC, or MINAGC. Search AGC is the preset AGC level used during search and corresponds to a -15 dBm detection level. This is preset by switches (23) and signals SAGC. MINAGC is the minimum allowable AGC voltage (maximum sensitivity) during track. If a signal falls below this corresponding sensitivity, drop track will occur.

Refer to schematic sheet 1. Shortly following the start of the sampling period, which can only occur during track, (see timing diagrams) AGCEOC goes to 1. This is the EOC pulse from the AGC error A/D. When EOC equals 0, the A/D conversion is complete. EOC goes to 1 at start of conversion. AGCEOC is delayed for at least 400 ns and inverted in (13). AGCEOCDL goes to 0, resetting (11). MINAGC goes to 1; this allows the LSB ADDER CONTROL on sheet 2 to generate control signals which set the A+B function in the AGC error ADDER, sheet 1. Also (04) and (05) outputs on sheet 2 control the ERROR CHANNEL SELECTION so that either channel 1 or 2 current AGC is AGCC at the ERROR ADDER.

If AGCA is not less than the MIN AGC (AREF) the current AGC will be updated by changing it to AGCA when sampling pulse AGCSAM(1) or AGCSAM(2) occurs. SAMPLE(1) (sheet 1) is a 200 ns 0 pulse. AKA equals 1 during track. This pulse goes thru (15) and (04) to (17) and (18).

When AGCINHL = 0 (front panel control), it inhibits AGCSAM(1) and prevents the current AGC from changing.

If AGCA is less than AREF (minimum allowable AGC level), after AGCEOCDL goes to 1 (AGC error has settled), then AGCLTR goes to 1, causing (1) to toggle MINAGC to 1. MINAGC is input to (14). If SSSSL=1, as it will during a track sampling period, MINAGCL will go to 0. This causes the error channel selection MUX to pass the AREF (MIN AGC) to the A input of the AGC ERROR ADDER, and control the AGC ERROR ADDER so that AGCC=AGCA. The minimum AGC level is then input to the channel 1 and 2 AGC registers. (14) is necessary because no AGCEOC pulse

occurs during search and (11) may be left with MINAGC=1 during this time, when MINAGC should be inoperative. The AGC error is 2's complement, either positive or negative. Sign conversion is done in the AGC input PROM. The AGC itself is always a positive number.

Search AGC level is set up as follows: During channel 1 search (Channel 2 search is identical), SSS(1) from (15) (sheet 1) is a 2.5 MHz clock which continuously strobes (17) and (18). SSSS from (07), sheet 2 equals 1, and SSELECTL = 1. Under these conditions SGL will equal 0, MUXS0 will equal 0, MUXS1 will equal 1, causing AGCC to equal SAGC and AGCA to equal AGCC. Search AGC (SAGC) is then continuously strobed into channel 1 AGC register.

(09) on sheet 2 is required because SELECT (1) can overlap SELECT (2) and vice versa when one channel is in search while the other is tracking. MUX and adder control must return to normal during the SSELECT period. MUXS0 and MUXS1 are controlled according to the following truth table. SSELECT (1) or SSELECT (2) cannot be used directly at (04) input since SSELECT(1)L \neq SSELECT (2) and vice versa.

SGL	SSELECT (2)	MINAGCAL	S1	S0	
0	0	0	1	1	MIN AGC
0	0	1	1	0	SEARCH AGC
0	1	0	1	1	MIN AGC
0	1	1	1	0	SEARCH AGC
1	0	0	1	1	MIN AGC
1	0	1	0	0	CHAN 1 AGC
1	1	0	1	1	MIN AGC
1	1	1	0	1	CHAN 2 AGC

On sheet 2 the LSB AGC ADDER CONTROL controls the AGC ERROR ADDER as previously described, and also controls the adder when the AGC is operating in the LSB mode. In this mode AGC is always changed $\pm 1/4$ dB, (corresponding to the AGC LSB) unless the AGC is at the minimum level. (27) and (28) cause LSB override during acquisition to aid in achieving a stable AGC condition quickly.

The following table shows the behavior of the AGC ERROR ADDER CONTROL and the control functions under all operating conditions.

LSBAGC	MINAGCAL	SGL	AGCDS	AGCSOS2	AGCS1S2	AGCCN	
0	0	0	0	0	0	1	A
0	0	0	1	0	0	1	A
0	0	1	0	0	0	1	A
0	0	1	1	0	0	1	A
0	1	0	0	0	0	1	A
0	1	0	1	0	0	1	A
0	1	1	0	1	0	1	A+B 2's complement error
0	1	1	1	1	0	1	A+B so always add
1	0	0	0	0	0	0	A+1 A-B
1	0	0	1	1	1	1	A-1 A+B
1	0	1	0	0	0	0	A+1 A-B
1	0	1	1	1	1	1	A-1 A+B
1	1	0	0	0	0	0	A+1 A-B
1	1	0	1	1	1	1	A-1 A+B
1	1	1	0	0	0	0	A+1 A-B
1	1	1	1	1	1	1	A-1 A+B

(04) through (09) on sheet 3 is the INITIAL SEARCH RECEIVER BLANK. Its purpose is to blank the receiver for 24 μ s immediately after a channel selection is made and the channel is in the search mode. This allows time for the search AGC to set up. If AKP=1 and SSSS goes to 1, as it will when one of the channels is selected in the search mode, SBLANK will equal 0 until (05) times-out and TC goes to 1. SSSSL always holds (05) on reset while neither of the channels is selected in the search mode. If AGCB=SAGC, (04) causes AKN to go to 1 allowing (05) to time-out. The set-up time for AGCB when switching to search does not matter since SBLANKL will go to 0 as soon as search is selected. (04) insures that when a channel operates in search for the first time after acquisition or tracking that AGCB must be set to SAGC before (05) time-out starts. The worst case of this occurs if search starts during an SSELECT period; up to about 15 μ s may be required to initiate search AGC, and SBLANKL will be extended for this extra time.

Note the entire search blank function is now not used. It has been negated by a change which replaced SELECT(1) and SELECT(2) inputs on (06) and (09), sheet 1, with DOT(1) and DOT(2) respectively. This change maintains current AGC level for reacquisition until DOT time-out.

(14) Threshold Detector, Sum and Hold and A/D Control Circuits (Figure 1-46 and 1-47)

This circuit generates timing to strobe the discriminator output, the sample and holds, and the A/D converters. Refer to Board 10 sheets 3 and 4 and Board 13 sheet 4.

The SUMVID signal derived directly from the Σ IF's is input to the threshold detector which is nominally set to detect a signal level corresponding to 10 dB below the Σ reference level. This setting is calibrated during test and should only rarely need adjustment. This level, in conjunction with AGC control, provides threshold detection levels for controlling the SAMPLE and HOLD circuits under various conditions. During track the AGC is adjusted to nominally maintain the incoming signal to the Σ reference level. This will probably correspond to +6 dBm receiver output. Using a level that is 10 dB below reference threshold would allow linear detection in the range of -10 dB to +4 dB about the +6 dBm reference level.

Detection from the Σ generates EAW only. AUXVIDEO detection generates SUMPRFA, SUMPRFC, and SDPRFL. SDPRFL is used for establishing initial track, which must be done before any phase or AFC corrections are made. Similarly, AFC control is initiated by the passage of SUMPRFA through (03) on Sheet 4. (03) through (08) accommodate loading and inversion requirements. (09) provides two delays. The SUMHOLD signal is used as timing for the S&H circuit which captures the received signal level for use in determining AGC error. The SDHOLD is used on the γ and ϕ error S&H's and will probably be slightly delayed from SUMHOLD.

On sheet 4 SUMPRFA is delayed in (03) and used to clock (02), when SENL=0. If this condition exists, EBR goes to 0, causing an approximately 30 ns strobe on EBC, setting (02) again and clocking (22). This causes EBQ to go to 0. (23) clocks at 625 kHz. EBQ is delayed for 2 clock edges to insure that QAFCAL is always delayed at least 1 clock interval, since EBO occurs asynchronously, having been initiated by the received pulse. EBN goes to 0 on the first clock edge causing EBQ to also go to 0. EBQ remains 0 until the next received pulse so QAFCAL will be a 1.6 μ s clock pulse equal to 1 period of the 625 MHz clock.

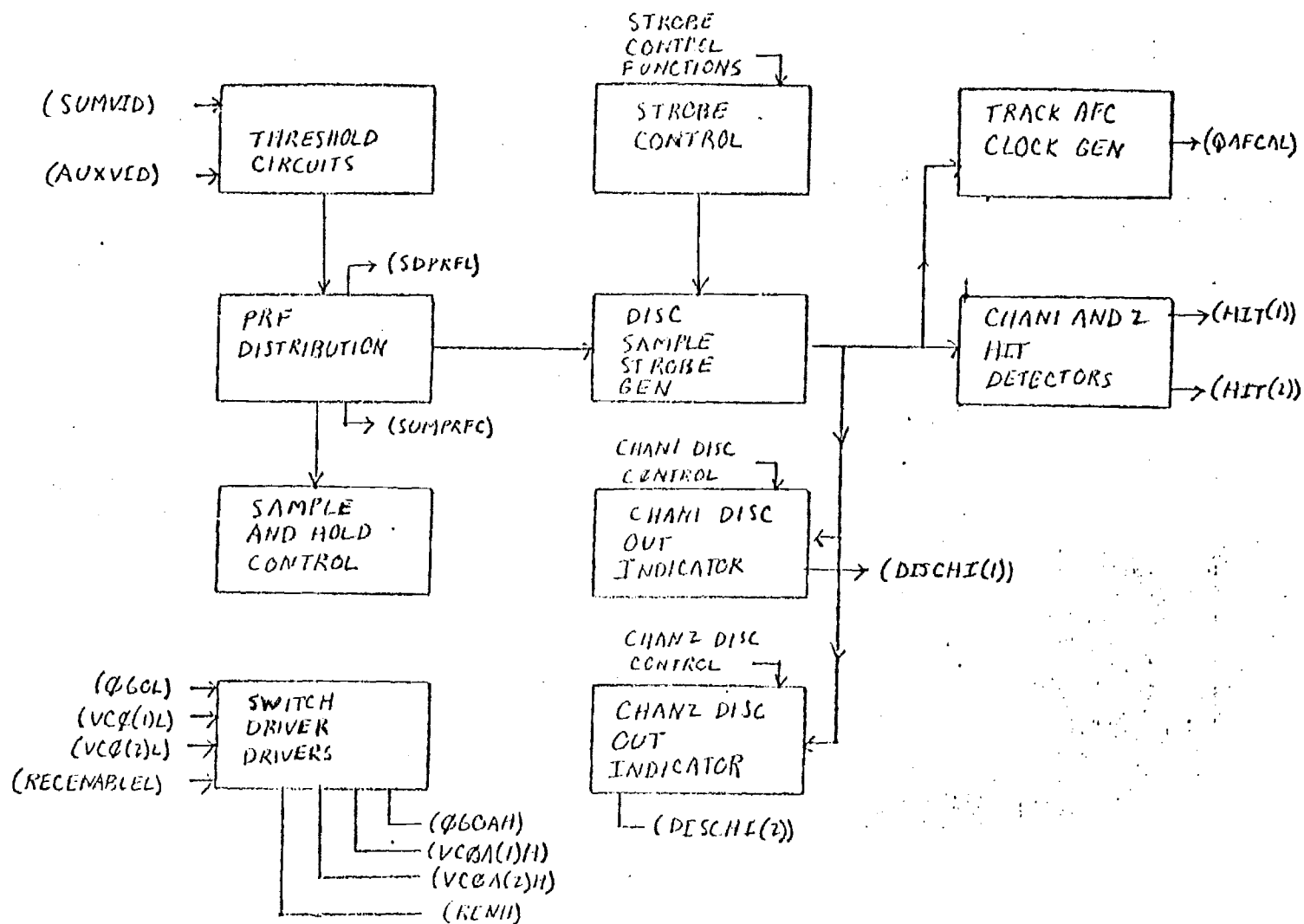


Figure 1-46. Dropout Timer Board 10 Threshold Detector, Sum and Hold, and A/D Control Block Diagram

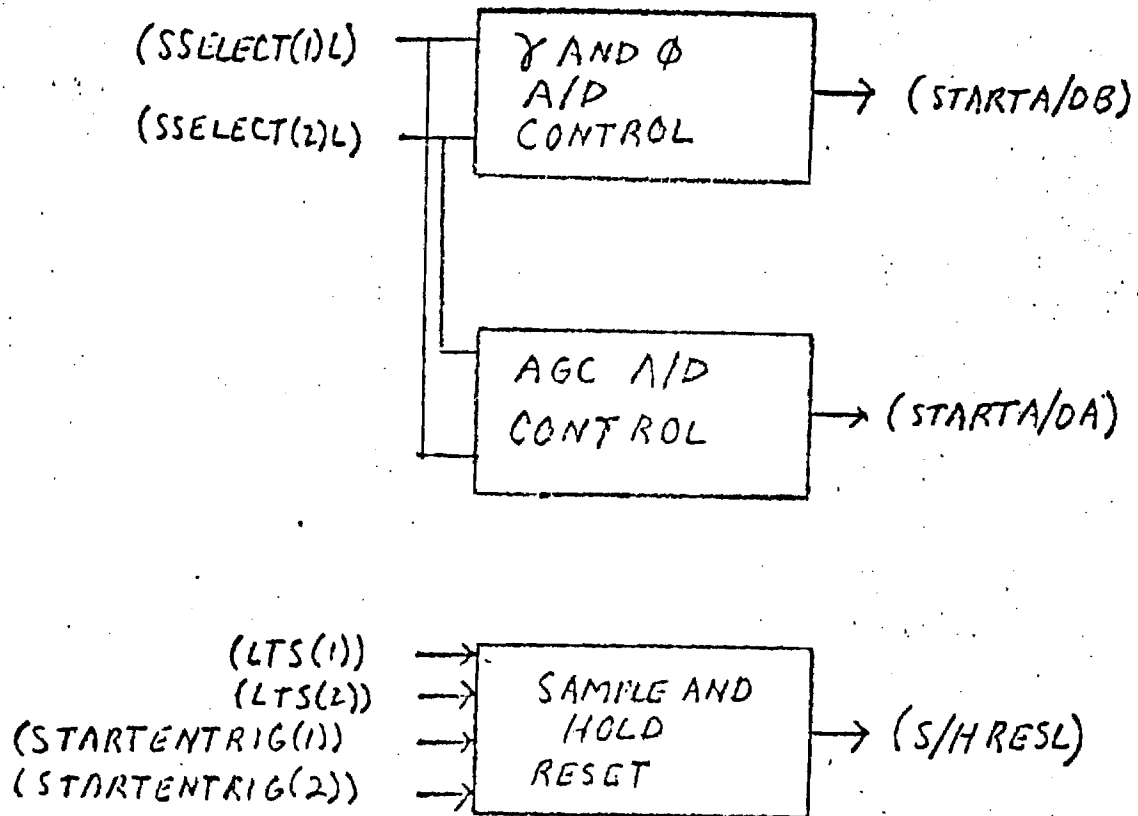


Figure 1-47. AGC Board 13 Threshold Detector, Sum and Hold, and A/D Control Block Diagram

The approximately 30 ns DISCSAMPLE will go to 1 when (02) is clocked, causing either EBK or EBL to go to 0, setting flip-flop (20), (21) accordingly. DISCHIBL is the logic output from the discriminator indicating whether the received frequency is above or below the IF center frequency. SELECT (1) enables (10) and (11) for channel 1 while SELECT (2) enables (04) and (05) for channel 2.

LIMPRFAH

LIMPRFAH is currently not used, its function having been superseded by the AUXVIDEO circuit on sheet 3. The following discussion is included for documentation purposes only. LIMPRFAH enables both channels; this signal is derived from the auxiliary channel. Its purpose is to prevent discriminator sampling when the received signal is at the IF band edge.

A sharp 10 MHz BW, 60 MHz center filter is located ahead of the discriminator limiter. The filter output goes to the discriminator limiter. The limiter output goes to the discriminator and to a video detector. The video detector output goes to a threshold detector which is set to about 1/2 of the limit level.

In order for a signal to be detected during search, it must be detected by this threshold detector. All levels above the threshold must cause the discriminator to reliably provide polarity information (amplitude is not required in conjunction with the purpose of this detector). This arrangement causes the following to happen: (The four following items also apply the AUXVIDEO functions.)

1. A signal will only be detected within the filter bandwidth instead of relying on the very poor IF skirt selectivity.
2. If the signal is in the right sideband the tuning will walk it toward the IF center.
3. If the signal is not in the right sideband the tuning will walk it out of the filter passband to where it is below the threshold and the discriminator operating level, which will cause the signal to be rejected (bumped) and search will resume in the same direction as before.

4. Inserting the filter in the auxiliary channel eliminates phase shift and sensitivity problems which might occur if two filters were inserted ahead of the dual IF. (See further discussion of AUX-VIDEO operation.)

Signal SENL is applied to the KB input of (02) sheet 4 and (10) and (11) sheet 3, enabling these flip-flops when PRFENABLE and LTS (lookthrough) occur for either channel. This allows error updating to occur only during lookthrough. PRF tracking update will occur during lookthrough, but may also occur during PRFENABLE and when not transmitting as indicated in Figure 1-48.

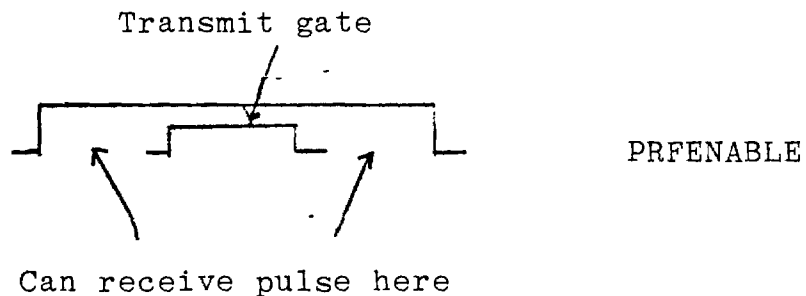


Figure 1-48. PRF Tracking Update

System timing will have to be set up so that when a pulse is received SENL will remain at KB's until the delayed received pulse has time to clock the respective flip-flops. There are about 15 delay devices between SUMPRFA, EAW and SENL. If this is not enough time some delay can be added to SUMPRFC to delay transmit blanking, which will in turn delay PRFENABLE turnoff. There should be no problems with differential delays between receive enable and PRFENABLE since receive enable turnoff should occur slightly after PRFENABLE turnoff and no receive enable switching transient will occur as a result.

S/HRSEL, a 200 ns pulse generated just prior to the start of the receive enable gate sets (10) and (11) sheet 3. (24) and (25) are hit detectors for channel 1 and channel 2. These indicate whether or not a pulse has been received during a lookthrough.

ENMASTER timing spans the receive enable gate timing and enables (24) and (25) so that an EBC strobe will cause a hit indication. If a hit is indicated at the end of the ENMASTER GATE a -7 preset will be clocked into a lookthrough hit/miss counter (see board 7), if not, the lookthrough gate trailing

edge will advance the counter by 1. Seven consecutive misses will cause the PRF tracker to reset. The lookthrough implementation requires that lookthrough be done on alternate PRFs of the same channel and will not select the alternate time unless a hit has occurred on the non-alternate time slot. This provides a means of causing a tracker reset to occur whenever it appears that one of the PRF tracker phases has skewed off center position. This is necessary to prevent faulty tracking condition.

BD 13 sheet 4 shows the timing controls for starting the AGC and the phase error A/D's. The AGC only needs to wait for the AGC S&H to settle. EAF, (09), TC output goes 1 about 1.2 μ s after AKR goes to 1. This allows (12) and (13) to generate a 400 ns pulse which starts the AGC A/D conversion. Similarly (02) and (03) provide timing for starting the γ and ϕ error A/Ds: A longer time is required than for the AGC. (Figure 1-49).

AKR presets (02), (03) and (09) whenever there isn't a sample select period occurring (SSELECT), so that the counters are ready for the succeeding sample period.

Note that because of the way S/HRESL is generated, if only one channel is tracking, SUMHOLD will = 1 all the time except for a few microseconds during each PRF gate when lookthrough occurs. This means that the γ and ϕ error signals will be almost continuously present and can be measured by the recorder. The sample and hold signals are always held until just before a new one is to be read. This assumes, however, that no calibration is needed in the phase error preprocessor loops. If it is, then the S&H's should be reset at the end of each sampling period. The sampling pulses are used for this.

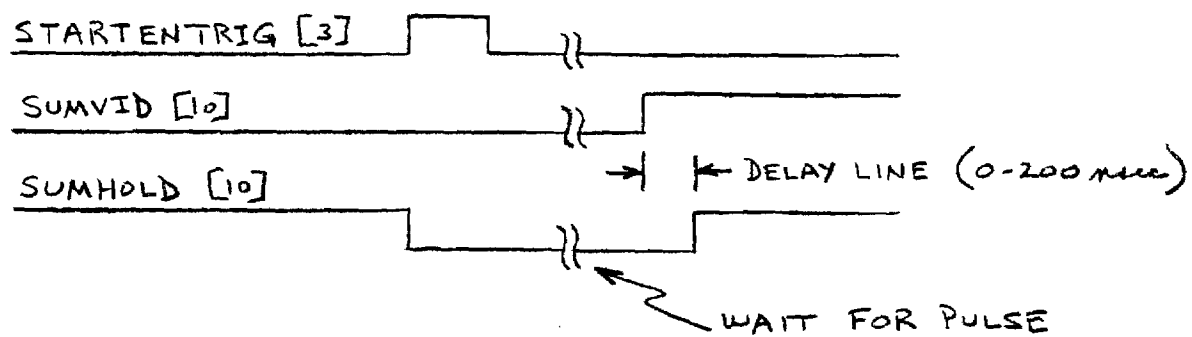
Duty Cycle Limiter Board 14 (Figure 1-50)

This circuit inhibits TWT on GATE whenever XMIT GATE Duty cycle exceeds 2%.

Polarization Modulation Converters - Board 16X

This board contains the analog to digital converters to convert the external modulation waveform into eight-bit digital words. The digital outputs are applied to the modulation adders on boards 11X and 12X. The input buffer has provision for some gain ($0.5 < \text{Gain} < 5.5$) to accommodate signal generators with a limited output range ($0.9 < V_{in} < 10$).

The falling edge of MADSTARTL starts the conversion process. This signal resets the A/D converter, whose status line, EOC, is then used to set the S/H in a HOLD state.



SCALE 200 nsec =

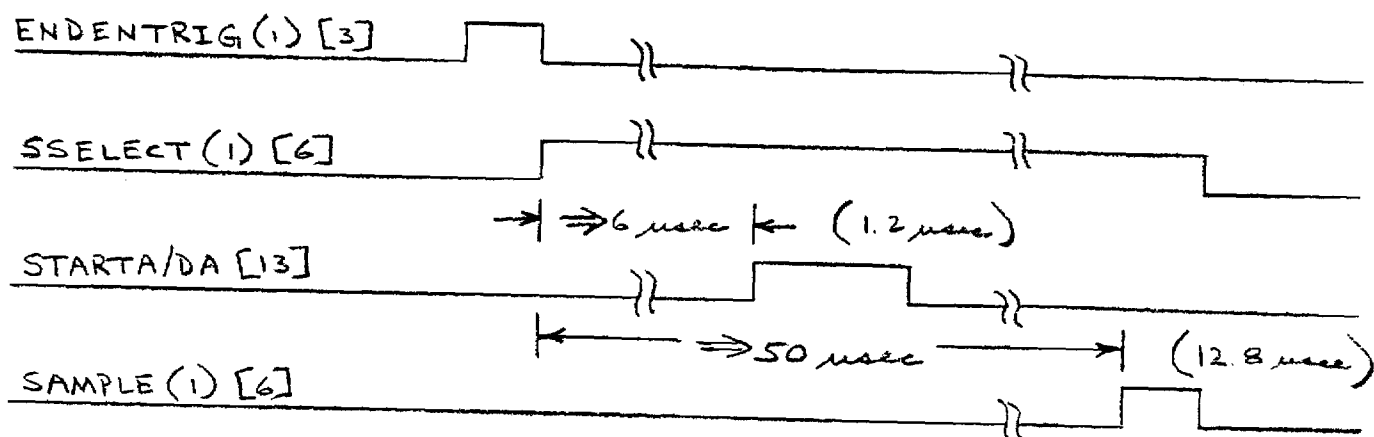


Figure 1-49. AGC Timing

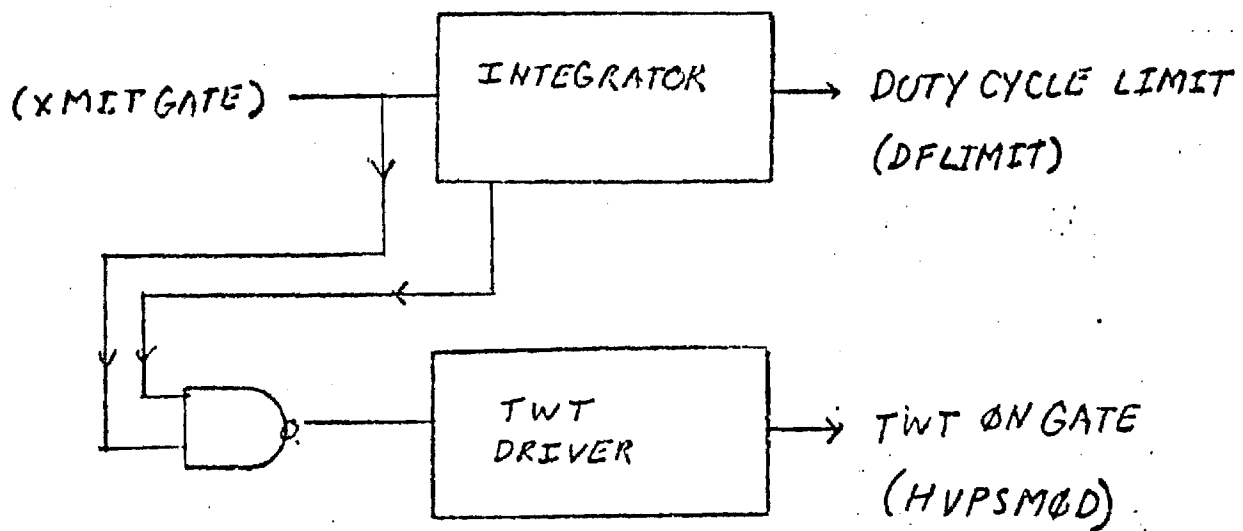


Figure 1-50. Duty Cycle Limiter Board 14 Block Diagram

At the end of the conversion, the S/H reverts to a SAMPLE mode, and the digital data (PMODXX or GMODXX) is held for further use until the next MADSTARTL transition. The A/D input is bipolar ($\pm 5V$) and the output coding is in two's complement.

Parallel to Serial Polarizer Interface - Board 27X (Figure 1-51).

This board converts the parallel gamma and phi data to serial form for transmission to the polarizer. It also contains logic to control the polarization modulation A/D converters.

The gamma and phi data is strobed into U19, 20, 21, and 22 on the 0 to 1 transition of MUDPSSL, which also allows U15 to start counting. The data is shifted out serially through the line drivers to the polarizer. GATE = 1 while the shifting is in progress, allowing the formation of DGATEL and QCLOCKL. DGATEL goes to 1 800 ns after the last QCLOCK edge. This DGATEL transition is used as a register strobe on P1, Polarizer Interface board, and the 800 ns allows a plentiful margin for the 450 ns maximum access time on the 2780 uV PROMS. Transmit/receive information is also sent to the polarizer by RCV, the OR of channel 1 lookthrough and channel 2 lookthrough. This same signal is sent to the X-band RF receiver to shut off the 60 MHz source during lookthrough (to avoid tracking the ECM transmitter). VCO ON is also sent to the RF receiver to turn on the appropriate VCO for the expected receive events.

U11 Synchronizes the EXTERNAL SAMPLE GATE to the processor clocks. When the SAMPLE GATE SOURCE switch is at INTERNAL, the polarization modulation A/D converter start command, MADSTARTL, occurs at pretrigger time, allowing more than sufficient time for the conversion (UDPSSL occurs at the start of SELECT). In the EXTERNAL position, MADSTARTL is controlled by the EXTERNAL SAMPLE GATE, which may occur at rates higher than the threat PRF. This mode is intended for use with the CW transmitter, to enable the output transmit polarization to be changed within the interpulse period. (Figure 1-52).

Polarizer Interface - Board P1

The Polarizer Interface board contains the serial to parallel conversion, the ultraviolet PROM's, and D/A converters to interface the processor with the phase shifter assembly. The inputs to the board are the serial data streams for phi and gamma, and the outputs are parallel data phase shift commands to the phase shift bit drivers. The A/D converters allow observation of the commands which are given to the phase shifters. (Figure 1-53.)

Figure 1-51. Polarization Modulation Timing Sample Gate - External Board 27X

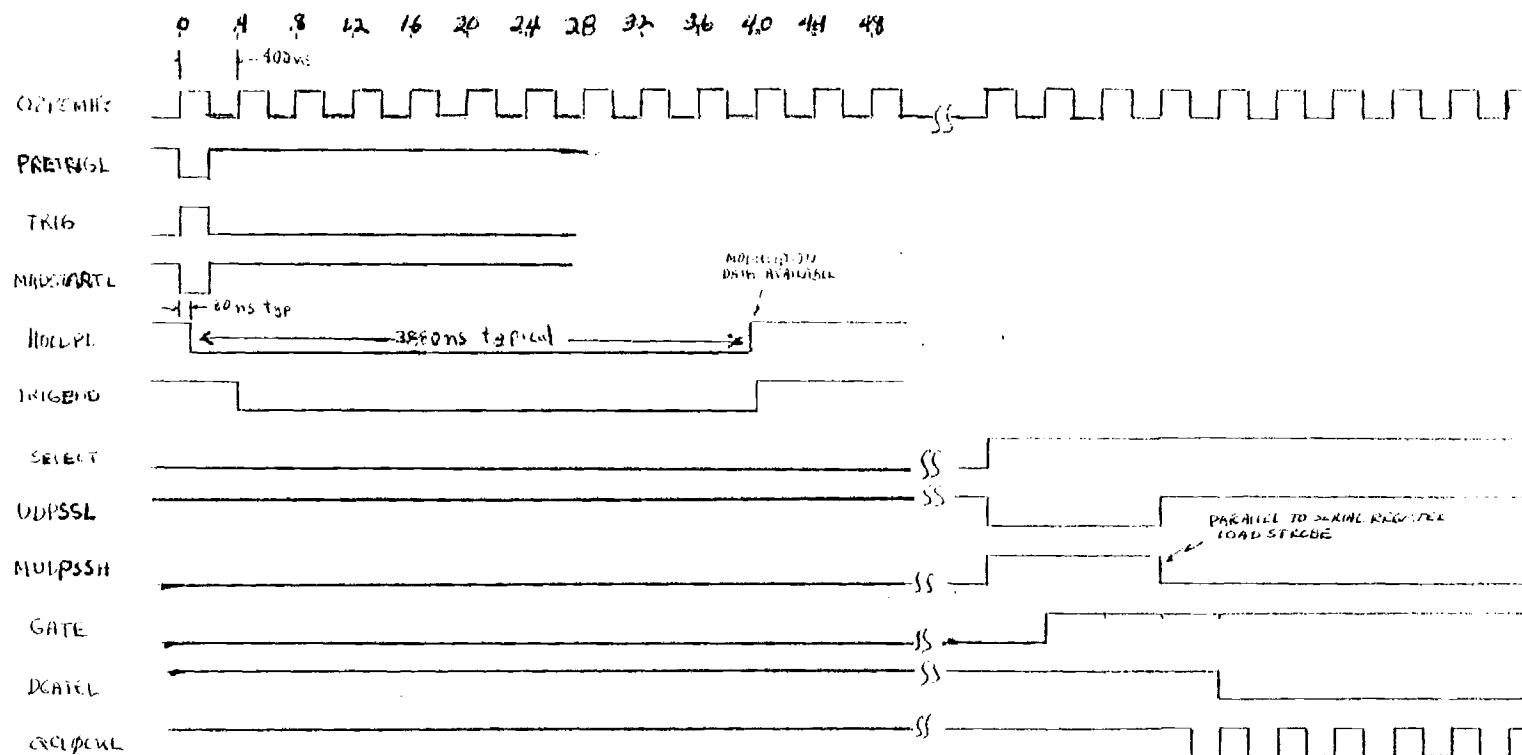


Figure 1-52. Polarization Modulation Timing
Sample Gate - Internal

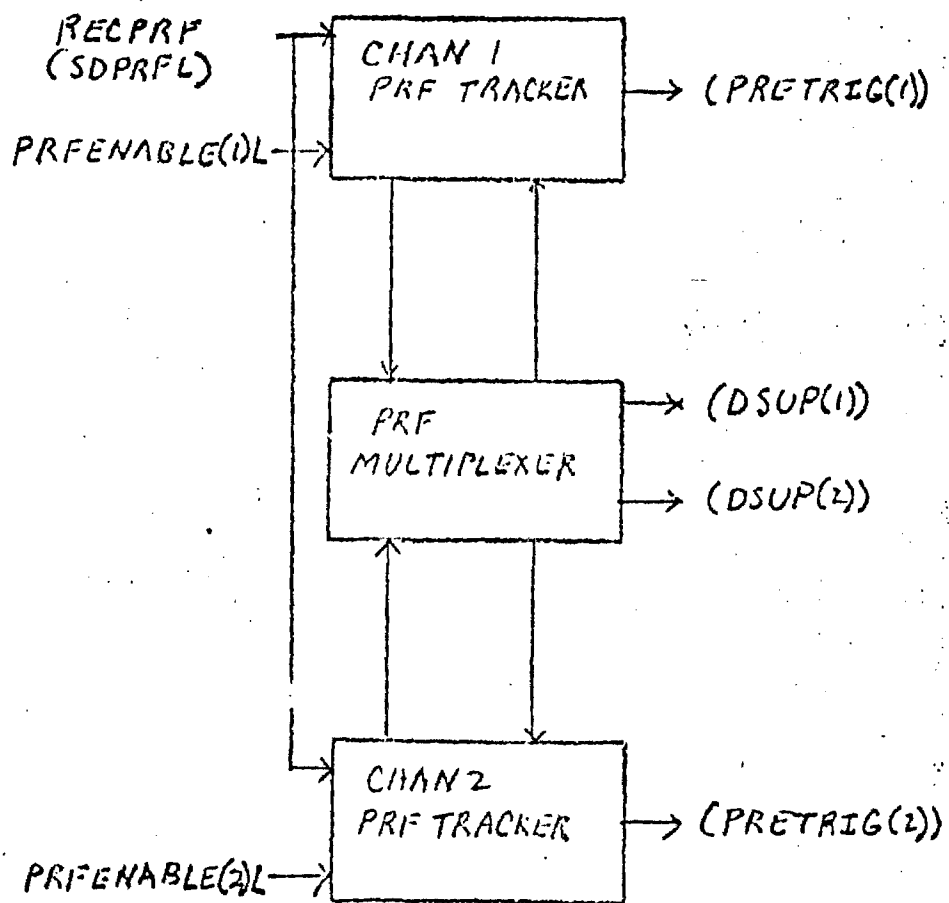


Figure 1-53. PRF Tracker Boards

4. Polarization Control

Figure 1-55 is a simplified block diagram of the APECM polarization control system. Several system components have been omitted to reduce the complexity of the drawings; those items which are germane to the following discussion have been included.

The polarizer contains four phase shift elements:

- 1) P1, a one-bit phase shifter, with two phase states: 0 and 180°
- 2) P2, a ten-bit phase shifter, with many phase states between 0 and 180°
- 3) A1, a one-bit phase shifter, with two phase states: 0 and 90°
- 4) A2, a nine-bit phase shifter, with many phase states between 0 and 90°

The polarizer also contains ultraviolet PROMs that provide a table lookup function to translate the processor data to phase shifter state commands.

The A2 and P2 phase shift elements do not have the resolution implied by the number of bits supplied to them. Both the A2 and P2 elements contain phase shift "bits" of 45° , 22.5° , and 11.25° . The P2 element also has a phase shift bit of 90° . Each of these "bits" is controlled by one digital bit from the PROM output. In addition, both A2 and P2 contain an "analog bit," which is controlled by six digital bits from the PROM output and which provides many distinct phase shift states in the range 0 to 20 degrees. The 64 (2^6) states of the analog bit are not linearly distributed over the 20° ; the count command versus phase may have the form shown in the sketch in Figure 1-55.

Each phase shifter element consists physically of several sections of ferrite. Reducing the required phase shift proportionately reduces the physical length of the ferrite.

The analog bit consists of one length of ferrite, whose phase shift is determined by the amount of time during which a current is passed through it. The six-bit digital word is loaded into a down counter which terminates current flow when the end of count is reached. At this time the current has driven the device along its hysteresis curve to a remnant magnetization, and a resulting phase shift.

Thus, the phase shifter resolution is not 0.088° , ($360^\circ 2^{12}$). If its phase shift vs input count characteristic shown in

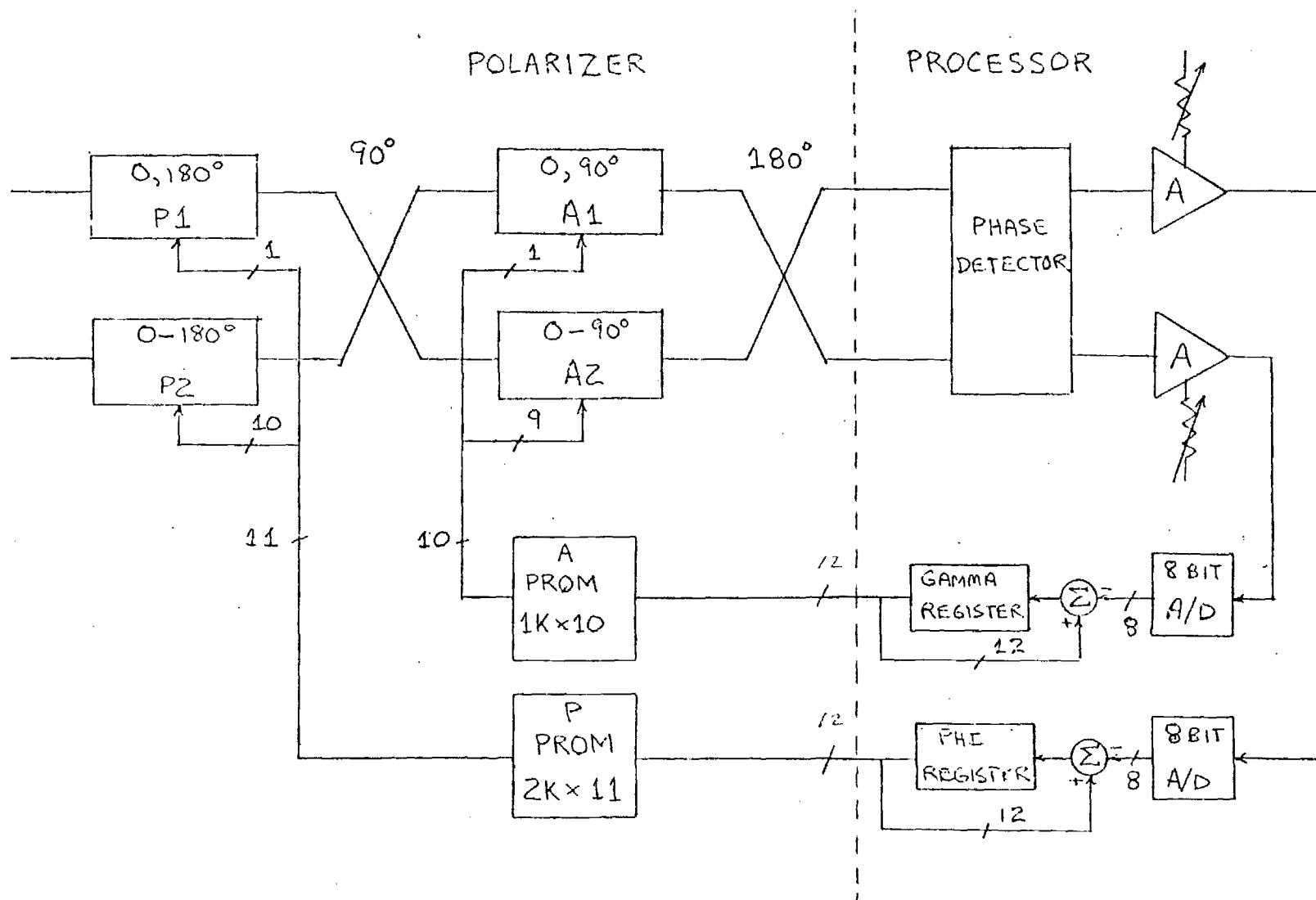


Figure 1-54. Polarizer Control Block Diagram

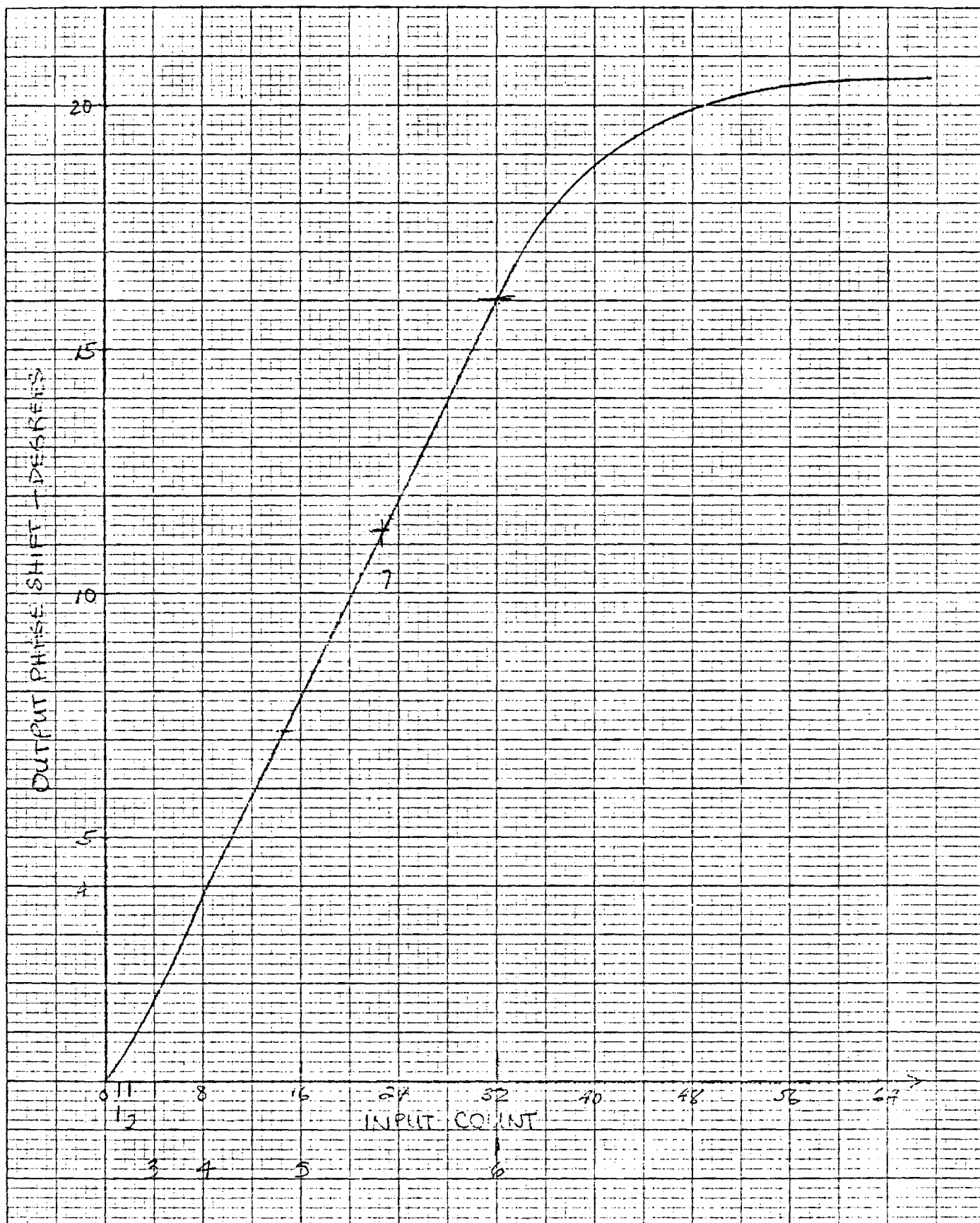


Figure 1-55. Analog Phase Shift Bit

Figure 1-55 were linear, its resolution would be $1/3^\circ$ ($20/2^6$). However, the realized resolution nominally $1/2^\circ$ ($20^\circ/40$).

The phase detector located in the processor provides two outputs: one proportional to $\sin \theta$ and the other to $\cos \theta$, where θ is the phase angle between the two input signals. These outputs are amplified to a value within a range of $\pm 5V$ and applied to an 8-bit analog to digital converter (A/D). The apparent dilemma of providing 8-bit error data to a 12-bit loop is resolved by the video amplifier.

The gain of the video amplifiers can be adjusted in the following manner. It is required that the input to the A/D span its entire full scale range when the phase difference in the two inputs changes from -11.25° to $+11.25^\circ$, a 22.5° (0.088×2^8) range. The situation is shown graphically in Figure 1-56 for both the gamma and phi channels. The A/D inputs are available on the processor front panel: ERROR GAMMA and ERROR PHI. The inputs to the phase detector may be supplied at 60 MHz at the processor front panel. Due to amplifier saturation effects, the outputs may not be at the full scale limits at the corners of the curves in Figure 1-56. However, near the zero crossings or null, the slope is 0.444 volts/degree.

The P1 and P2 phase shifters provide a maximum relative phase shift of 360° . Together they contain six phase shift bits: 180° , 90° , 45° , 22.5° , 11.25° and the 0 to 20° analog bit. Each phase bit requires one digital bit to determine its state, with the exception of the analog bit, which requires six. Thus, the PROM data word must be at least 11 bits long. Although two 8-bit PROMS are used in the hardware, only 11 bits are significant.

Due to nonlinearities in the phase shifter/phase shift driver transfer function a translation between the processors phase shift request and the input to the phase shifter driver is required. UV prompts provide the linearizing and format translation.

One of the functions of the PROMS is translation of the 12-bit processor word to the 11-bit P1, P2 and 10-bit A1, A2 commands. In the case of the P phase shifters, there are only 2^{11} or 2048 distinct output states possible (1024 for the A phase shifters). An address is made available for each possible output state. Thus, the P PROM is 2048 words of 11 bits, and the A PROM is 1024 words of 10 bits.

The data in the PROMs provides the translation from the processor phi and gamma values to the required phase shift. This process is illustrated in Figure 1-57. The PROMs essentially close the servo loop by determining the required phase shift states based on the current values of phi and gamma in the

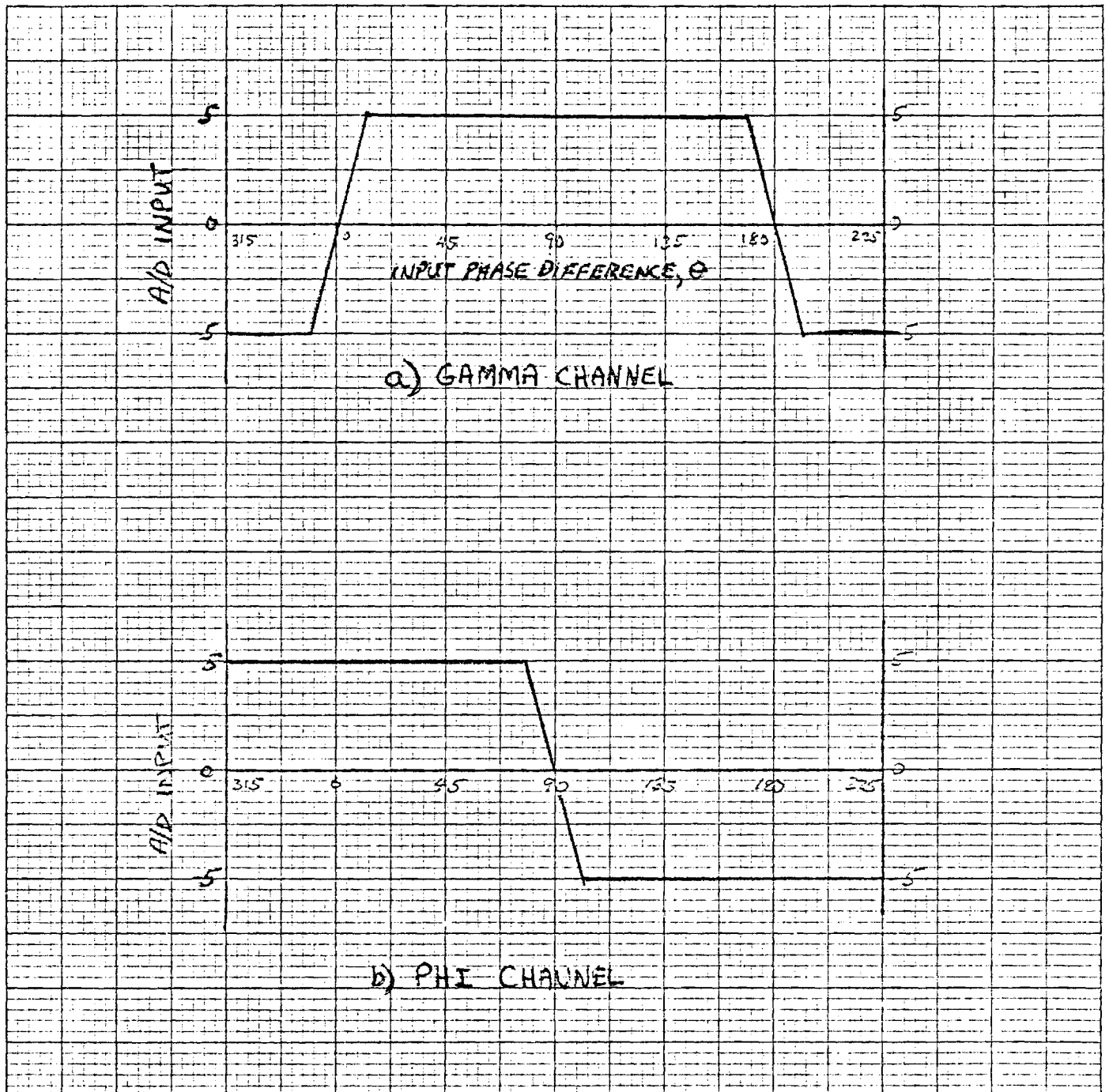


Figure 1-56. Video Amplifier Gain Adjustment

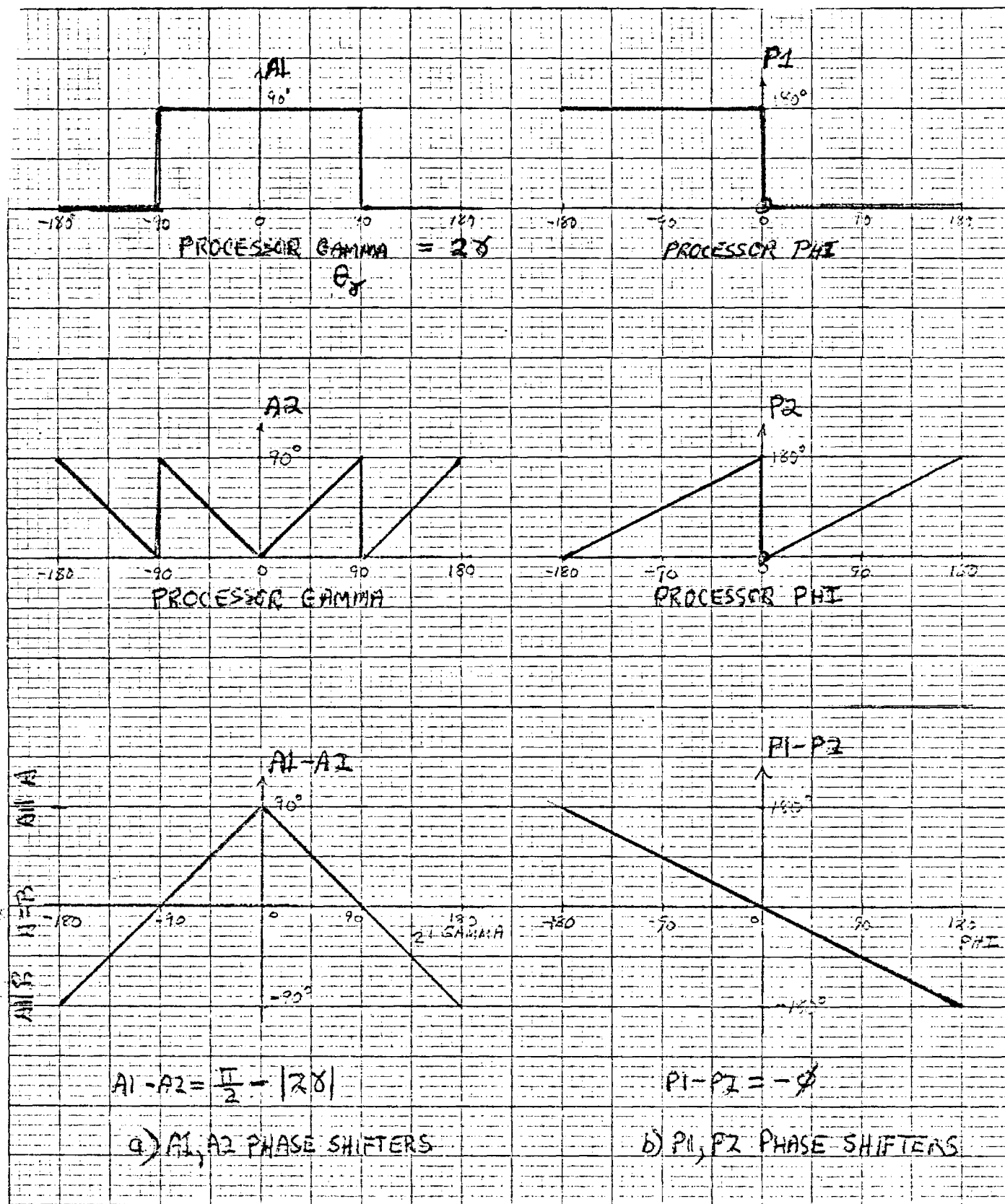


Figure 1-57. PROM Data Translation

processor. The processor data is interpreted in degrees in Figure 1-57. The data is actually a 12-bit word which is used as the PROM address.

If the phase shifters were perfect devices, the A PROM would contain the data illustrated in Table 1-7. The ten highest bits of the processor word are used for the PROM address. The LSB out of the PROM is disregarded. The second bit is the logical complement of the MSB, which controls the A1 phase shift.

The second bit, rather than the MSB, is used in the input word to the D/A. This produces a continuous output waveform as the PROM address is stepped. The D/A output is given the Table 1-7 and is also illustrated in Figure 1-58.

The PROMs could be used to linearize the phase shift command versus output phase relationship, however the commands are reasonably linear over the 0 - 11.25° range of the analog shifter and the servo permits reading any desired phase shift. PROMs are used to reduce the perturbations caused by the hysteresis effect when digital controlled shifters' states are altered causing the analog shifter to reset to zero.

5. Transmitter

The APECM Transmitter consists of a high-power, high gain, TWT chain with, optional Pulse or CW output. The output Amplifier(s) is driven by a low-noise TWT driver. The following is a functional description only; for details, refer to Volume II.

A signal flow block diagram of the APECM Transmitter TWT chain is shown in Figure 1-59.

Two drive signals may be selected by switch S1 (RPTP/Transponder). For Repeater operation the RF source is the direct radar signal received on the auxiliary receive antenna. For Transponder operation the RF source is the output of the FOGs of the LO assy in the APECM RF Receiver. Switch S-1 is a remote control coaxial switch operated by the control (RPTR-Trans.-IIG) located on the front panel of the APECM Transmitter Driver/AUX RCVR Unit.

The output of the Driver Amplifier is directed to the selected transmitter by remote control coaxial switch S2. S-2 is controlled by the manually operated selector switch (APECM-FUNCTION/CW-TEST-PULSE) located on the front panel of the APECM Transmitter Driver/AUX RCVR Unit.

The output of the Pulse Transmitter is routed via waveguide from the back of the Pulse Transmitter to the backside of

TABLE 1-7. EXAMPLES OF A PROM CONTENTS

PROCESSOR		PROM		D/A		
<u>se</u> <u>g)</u>	<u>Digital Word</u> (hex)	<u>Address</u> (decimal)	<u>Data Out</u> (hex)	<u>A1</u> (deg)	<u>A2</u> (deg)	<u>Output</u> (volts)
0.0	000	0	800	90	0	10.0
2.5	100	64	A00	90	22.5	7.5
5.0	200	128	C00	90	45.0	5.0
7.5	300	192	E00	90	67.5	2.5
10.0	400	256	002	0	0	0
12.5	500	320	202	0	22.5	- 2.5
15.0	600	384	402	0	45.0	- 5.0
17.0	700	448	602	0	67.5	- 7.5
20.0	800	512	7FE	0	89.8	-10.0
25.0	A00	640	402	0	45.0	- 5.0
30.0	C00	768	002	0	0	0
35.0	E00	896	C00	90	45.0	5.0

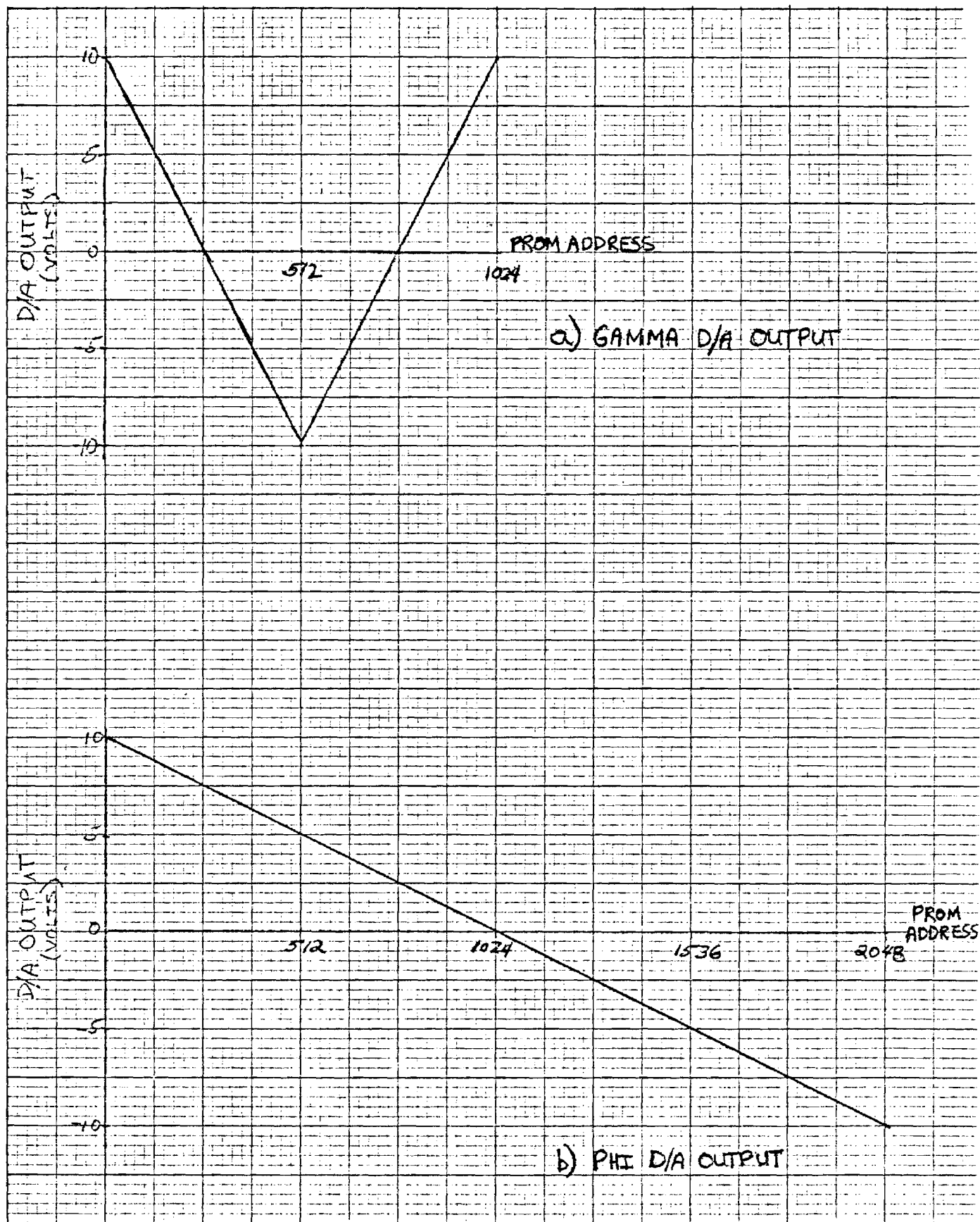


Figure 1-58. Phase Shift Command Test Points

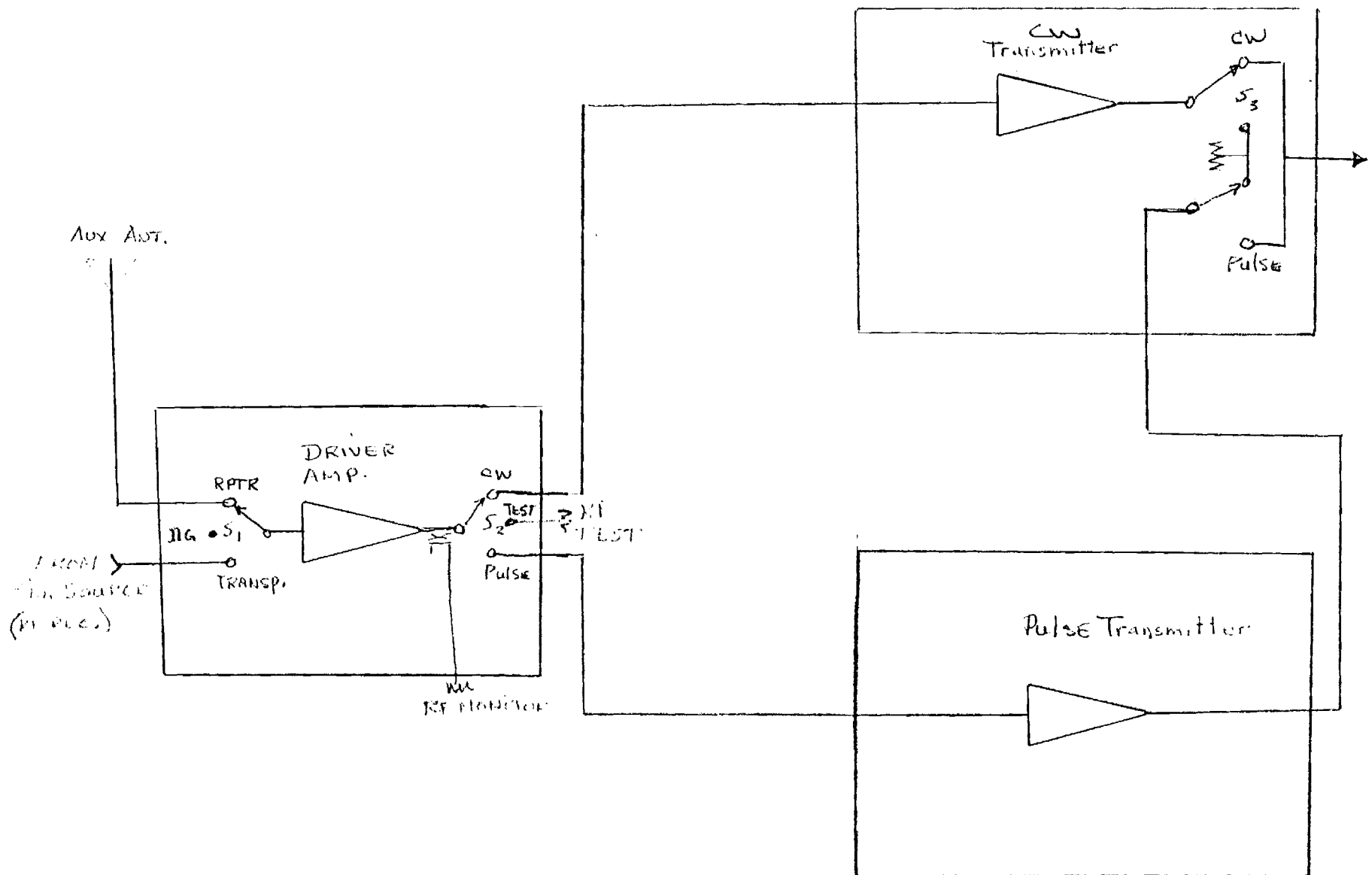


Figure 1-59. Signal Flow Block Diagram of APECM TWT Chain

the CW Transmitter Unit. A manually operated Waveguide Switch S3, accessible from the rear of the CW Transmitter Unit, selects the required transmitter signal which is available at the front panel of the CW Transmitter Unit. A high power dummy load is always connected to the transmitter unit not connected to the output port. The output port at the front panel of the CW Transmitter is connected by waveguide to the waveguide port on this front panel of the Polarizer Unit labeled RF FROM TRANSMITTER.

Figure 1-60 is a photo of the APECM Transmitter Driver/Aux. Rec. (Front View)

Figure 1-61 is a photo of the APECM Pulse Transmitter (Front View) which is a Litton model 624 Pulsed Microwave Amplifier.

Figure 1-62 is a photo of the APECM CW Amplifier/Plumbing Unit. (Front Quarter View)

6. Antenna

The antenna is a dual mode horn supplied by NVRAD. The two ports are (1) Right Circular (RC) and Left Circular (LC).

For details and descriptions see Volume I.

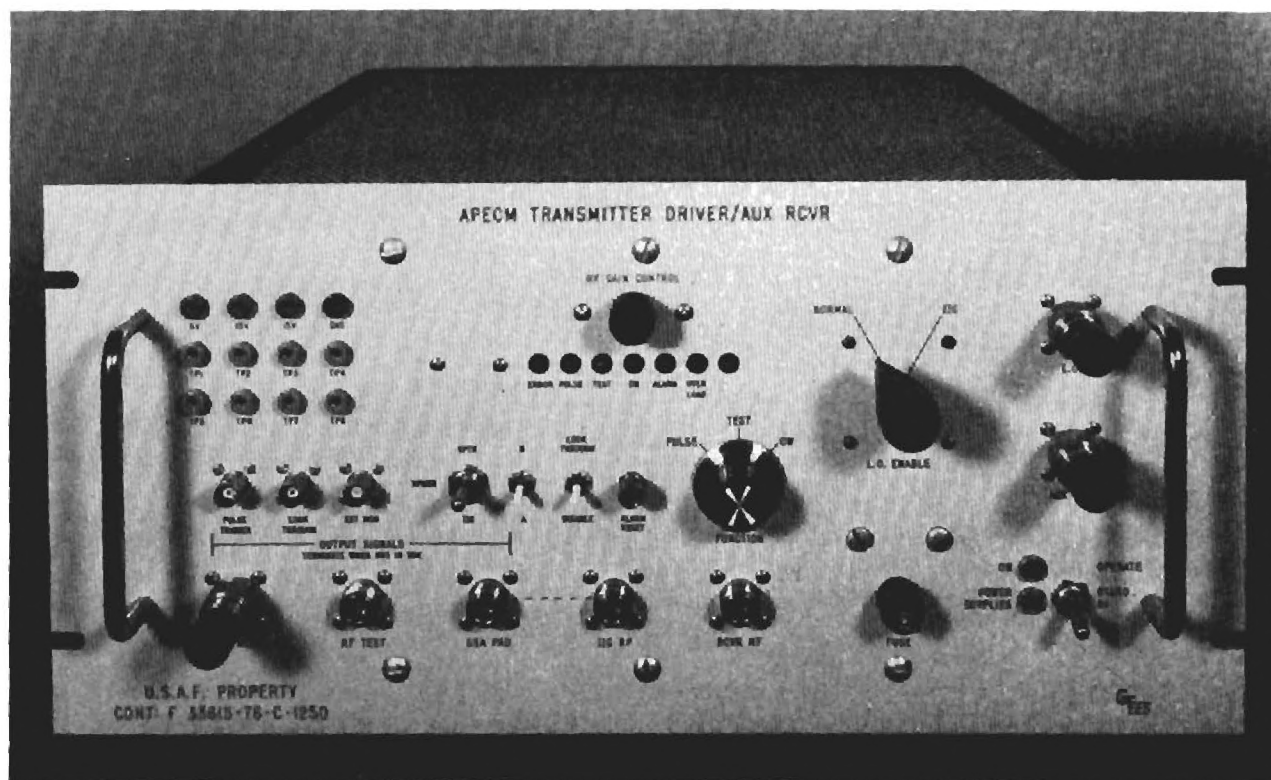


Figure 1-60. APECM Transmitter Driver/Aux Rec
(Front View)

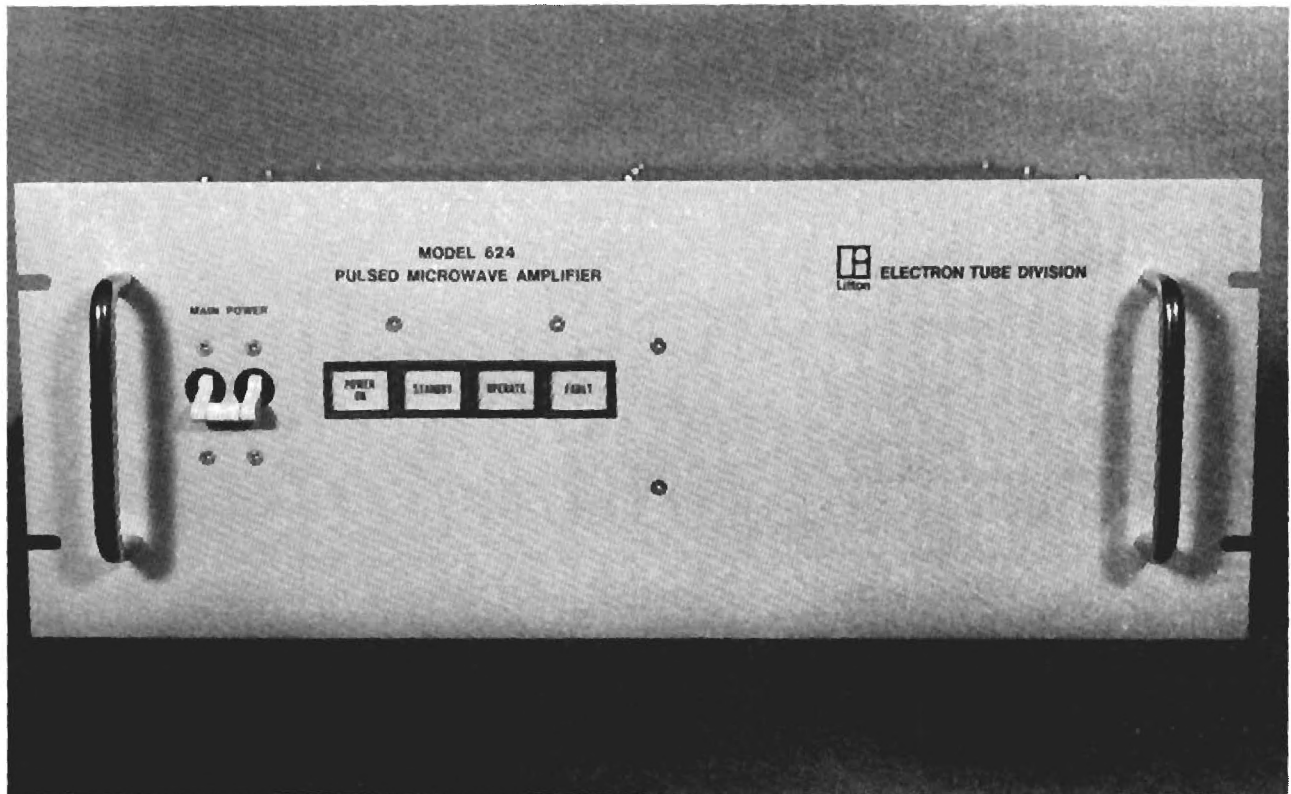


Figure 1-61. APECM Pulse Transmitter (Front View)

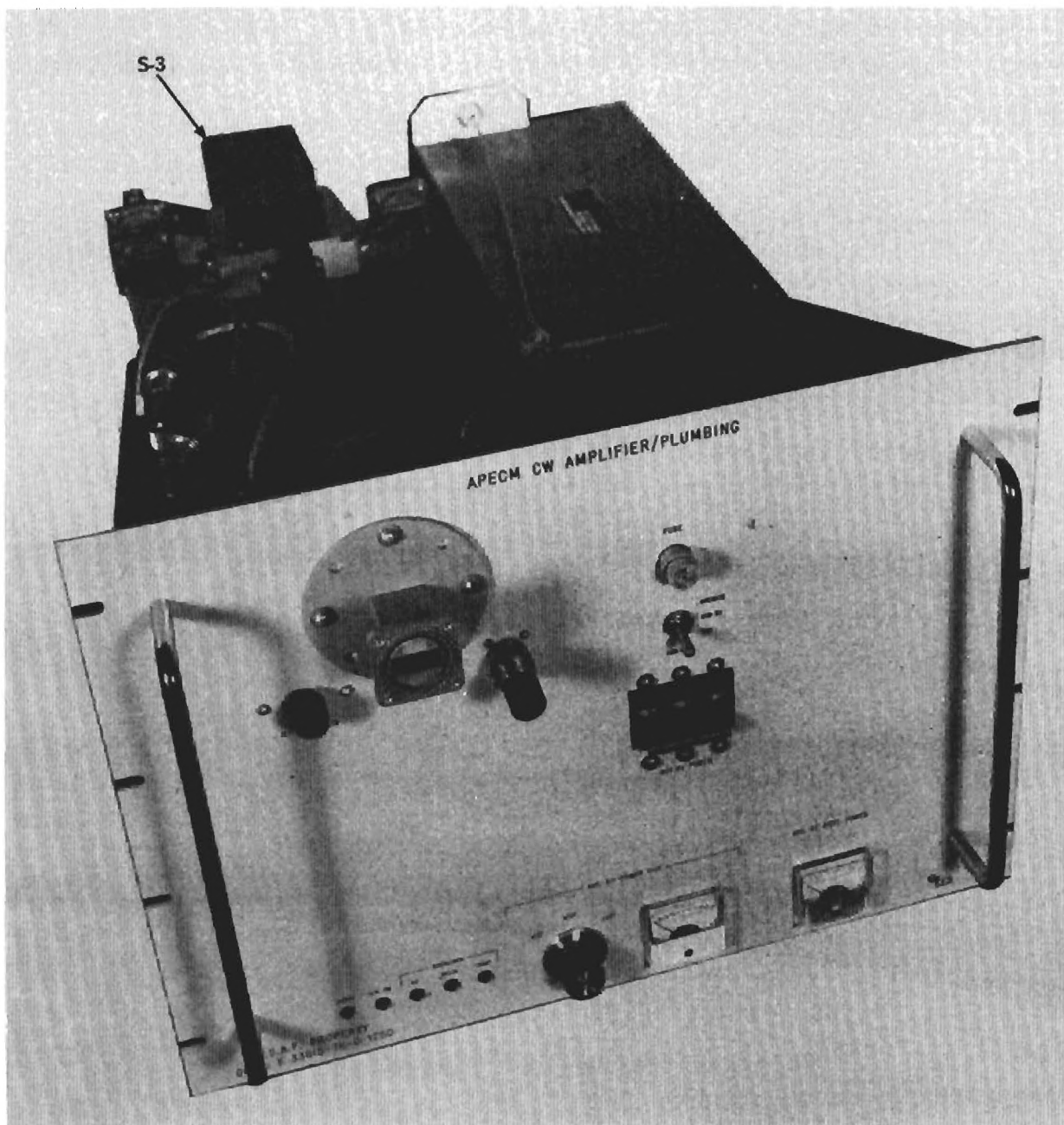


Figure 1-62. APECM CW Amplifier/Plumbing Unit
(Front Quarter View)

SECTION II

TEST OPERATION

A. Introduction

1. Objective

The intent of this section is to outline the test procedures and measurements to be made to verify the system performance of the Adaptive Polarization ECM equipment. The tests to be described are intended to measure the system operating parameters, rather than specific subsystem operating parameters.

2. Test Environment

The system will be tested in a flight ready mechanical configuration in a laboratory environment.

3. Auxiliary Test Equipment

Auxiliary test equipment, such as oscilloscopes, counters, power meters, RF sources, pulse and waveform generators, and miscellaneous, X-Band, RF components, will be required .

B. General Test Information

1. System Configuration

The basic system configuration, shown in Figure 2-1, consists of the following assemblies:

- A1 - Polarizer Antenna
- A2 - Polarizer
- A3 - Pulse Transmitter
- A4 - CW Transmitter
- A5 - Driver Amplifier
- A6 - Auxiliary Antenna
- A7 - Auxiliary Receiver
- A8 - RF Receiver
- A9 - IF Receiver
- A10 - Processor Converter

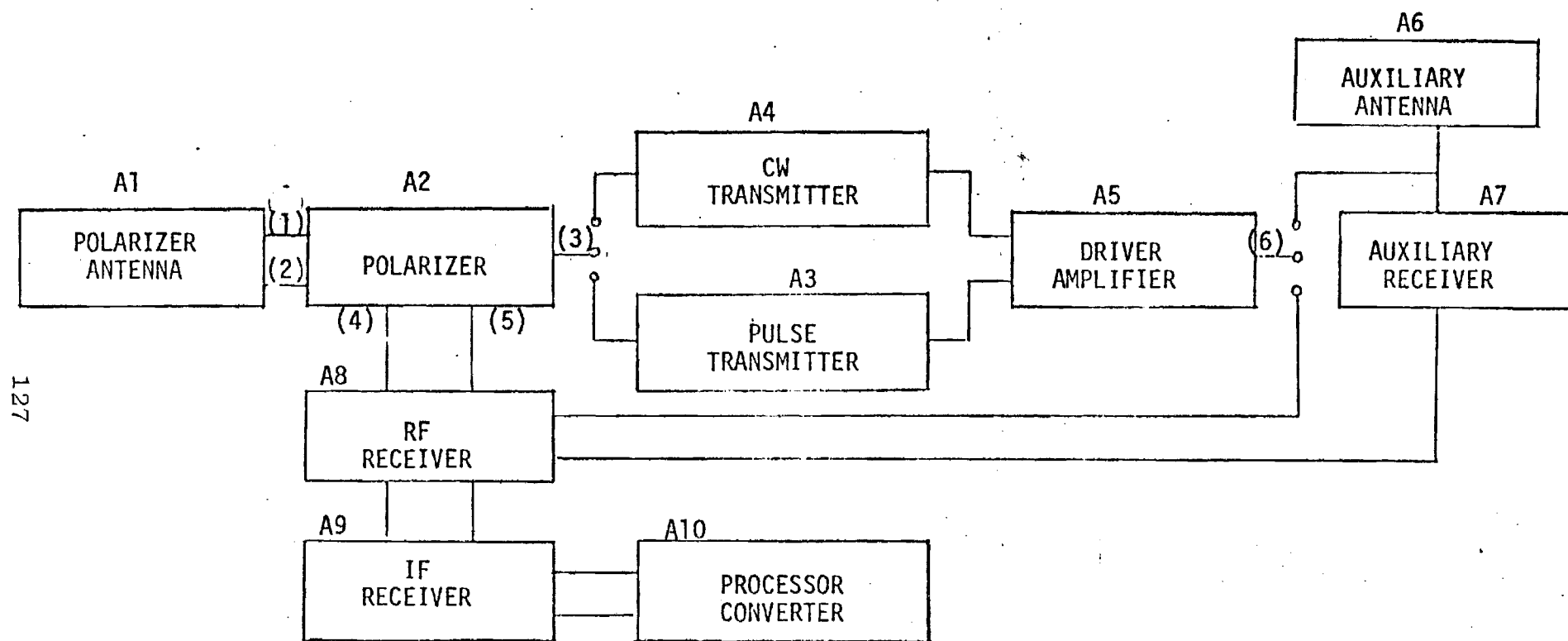


Figure 2-1. Basic System Configuration

All assemblies are not required in each test procedure. For example, direct coupling to the polarizer ports may be used rather than observing the free space output of the polarizer antenna.

2. System Modes

The connections of points (3) and (6) in Figure 2-1 determine the system modes which are defined in Table 2-1.

TABLE 2-1. SYSTEM MODES

<u>MODE</u>	<u>POLARIZER INPUT(3)</u>	<u>DRIVER INPUT(6)</u>
Pulse Transponder	Pulse XMTR	RF RCVR
CW Transponder	CW XMTR	RF RCVR
Pulse Repeater	Pulse XMTR	Aux. Antenna
CW Repeater	CW XMTR	Aux. Antenna

3. Nominal Source Parameters

Three X-Band sources will be used during the Acceptance Test. The recommended, nominal parameters for each of these sources is given in Table 2-2.

TABLE 2-2. NOMINAL SOURCE PARAMETERS

	<u>SOURCE 1</u>	<u>SOURCE 2</u>	<u>SOURCE 3</u>
FREQ (GHz)	8.5	9.5	10.5
PRF (Hz)	700	1500	2800
PW (s)	0.5	1.0	2.0
AMP (dBm)	-10	-5	0

4. Manual Polarization Settings

The Processor front panel contains three sets of thumbwheel switches which determine the manual polarization reference state, and the polarization increment which is added to

the polarizer phase shifter commands when the rate-aided mode is enable. The manual polarization reference state is always used in threat acquisition, and may be selected for open loop operation by the Channel 1 and 2 Threat Source switches on the processor front panel. The correspondence between the reference thumbwheel settings and major polarization states should be recorded as illustrated in Table 2-3.

TABLE 2-3. MANUAL POLARIZATION SETTINGS

<u>POLARIZATION</u>	<u>GAMMA</u>	<u>PHI</u>
Left Circular	1	
Right Circular		
Horizontal		
Vertical		To be recorded during test.
45° Linear		
135° Linear		
Nominal		

5. Normal Switch and Control Settings

The normal system configuration is described by the switch and control settings listed in Tables 2-4 and 2-5. These switch settings should be verified at the start of each test procedure. Changes in switch and control settings to achieve specific test configurations are described in the test procedures.

6. Test Configurations

a. Source Configuration

Three X-Band RF sources are required to simulate a three threat environment. The outputs from three sources can be combined as shown in Figure 2-2 and amplified to a 1 watt level by a TWT. The function generator can be used for source FM and PRI variations.

TABLE 2-4. NORMAL CONFIGURATION PROCESSOR FRONT PANEL CONTROLS

<u>SWITCH</u>	<u>POSITIONS</u>	<u>SETTINGS</u>
1. Ch 1	OFF-REC-XMIT	XMIT
2. AGC	OPERATE-DISABLE	OPERATE
3. AGC	LSB-FULL	LSB
4. Dual Frequency	SYNC-NONSYNC	NONSYNC
5. AFC	CH 1 NORMAL-FIXED	NORMAL
6. AFC	AUTO-MAN ADJ	AUTO
7. AFC	CH 2 NORMAL-FIXED	NORMAL
8. LOOKTHROUGH	CONTINUOUS-PERIODIC	PERIODIC
9. POLAR ERROR	LSB-FULL	LSB
10. POLAR ERROR	NORMAL-DISABLE	NORMAL
11. Ch 2	OFF-REC-XMIT	XMIT
	<u>CH 1</u> <u>CH 2</u>	
12. THREAT SOURCE	MANUAL - XPOLE	XPOLE
13. POL MOD	ON - OFF	OFF
14. RATE AIDED	ON - OFF	OFF
15. SAMPLE GATE	INTERNAL- EXTERNAL	INTERNAL
16. MODULATION	A-B-C-D	ANY
17. MODULATION	OFF-AMP-POL-BOTH	ANY
18. GAMMA	000-777	TBD
19. PHI	000-777	TBD
20. RATE INCREMENT	000-777	000

TABLE 2-5. NORMAL CONFIGURATION X-BAND RF RECEIVER CONTROLS

<u>CH</u>	<u>POSITION</u>	<u>SETTINGS</u>	<u>COMMENTS</u>
AFC-1	ON-OFF	ON	OFF for manual acquisition only
VCO SELECT	1-AUTO-2/3	AUTO	Selects VCO output
FREQ OFFSET	FM-OFF-STABLE	STABLE	Applies power to either stable or FM-able 60 MHz oscillators
AFC-2	ON-OFF	ON	OFF for manual acquisition
SEQUENCE	2-OFF-3	2	2-AFC2 TUNE pot controls VCO #2 3-AFC3 TUNE pot controls VCO #2 OFF-Automatic switching between 2 and 3
AFC-3	ON-OFF	ON	OFF-for manual acquisition
MOD SELECT (AFC Chassis)	OFF-ON-AUTO	AUTO	Controls 60 MHz oscillator Select switch
SEQUENCE RATE	POT	MID RANGE	Controls threat 2 and 3 dwell time.

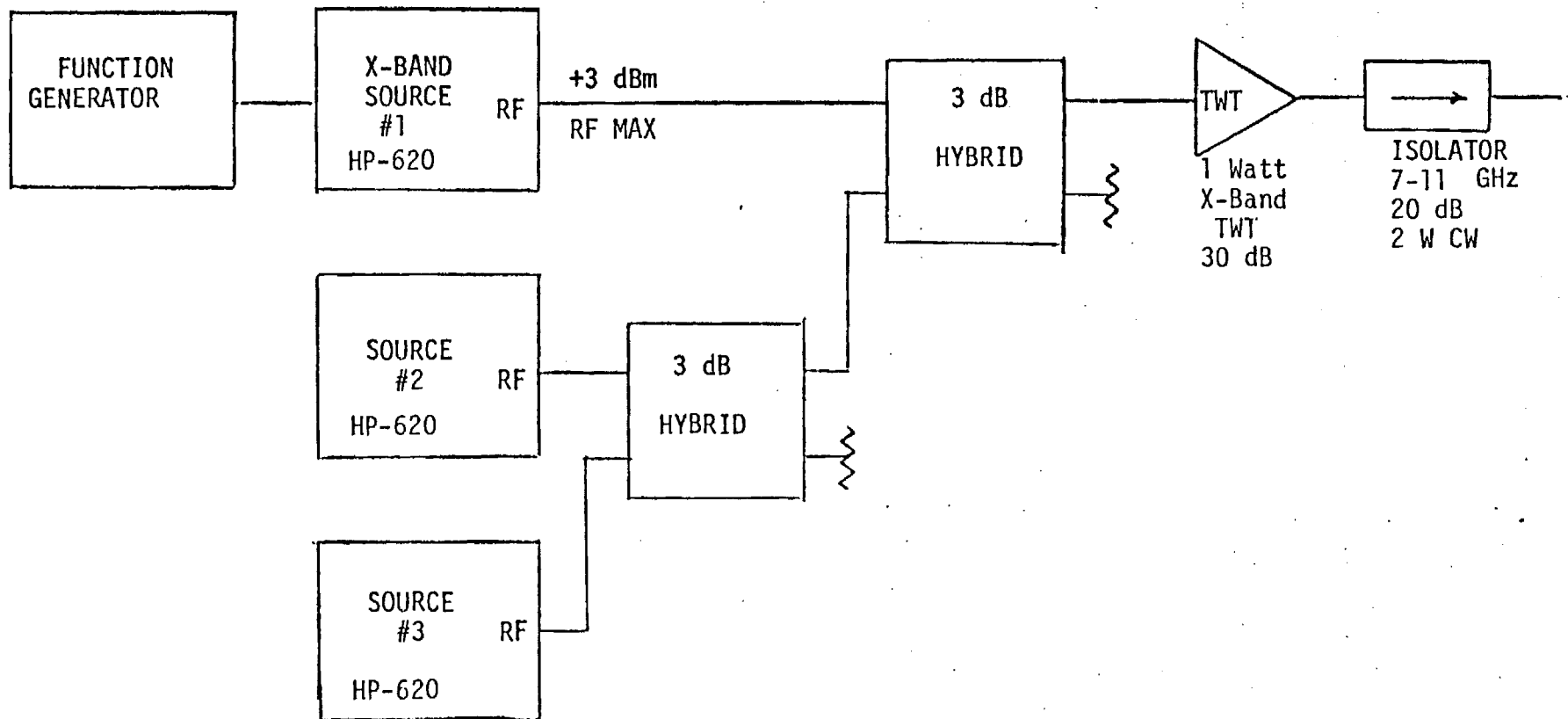


Figure 2-2. Source Configuration

b. Mechanical Polarizer Networks

Two mechanical polarizer networks will be used during the Tests as shown in Figures 2-3 and 2-4. The network in Figure 2-3 is used in the receive only parts of the tests. These tests include threat acquisition and track verification, threat parameter (PRF, pulsewidth) limit verification, and multiple threat capability demonstration. The more complicated network in Figure 2-4 is used for transmitter testing and closed loop system operation. The network in Figure 2-4 could be used in the receive only tests, however, the network in Figure 2-3 will provide a greater signal level to the system.

C. Test Instructions

1. Receive Tests

a. Frequency Acquisition

(1) PURPOSE: Verify ability to manually acquire three threats. Verify AFC tracking ability.

(2) SET UP:

- (a) Set up test equipment as in Figure 2-2 and 2-3.
- (b) Verify all normal switch and control settings.
- (c) Power on system.

NOTE: Transmitter output power is not required in this procedure. The transmitters should be left in a stand-by condition.

(3) PROCEDURE:

(a) Source 1 Acquisition

1. Turn on Source 1 and set up nominal Source 1 parameters. Turn off Source 2 and 3.

2. Processor FP switches:

Chan 1	REC
Chan 2	OFF
Lookthru	CONTINUOUS

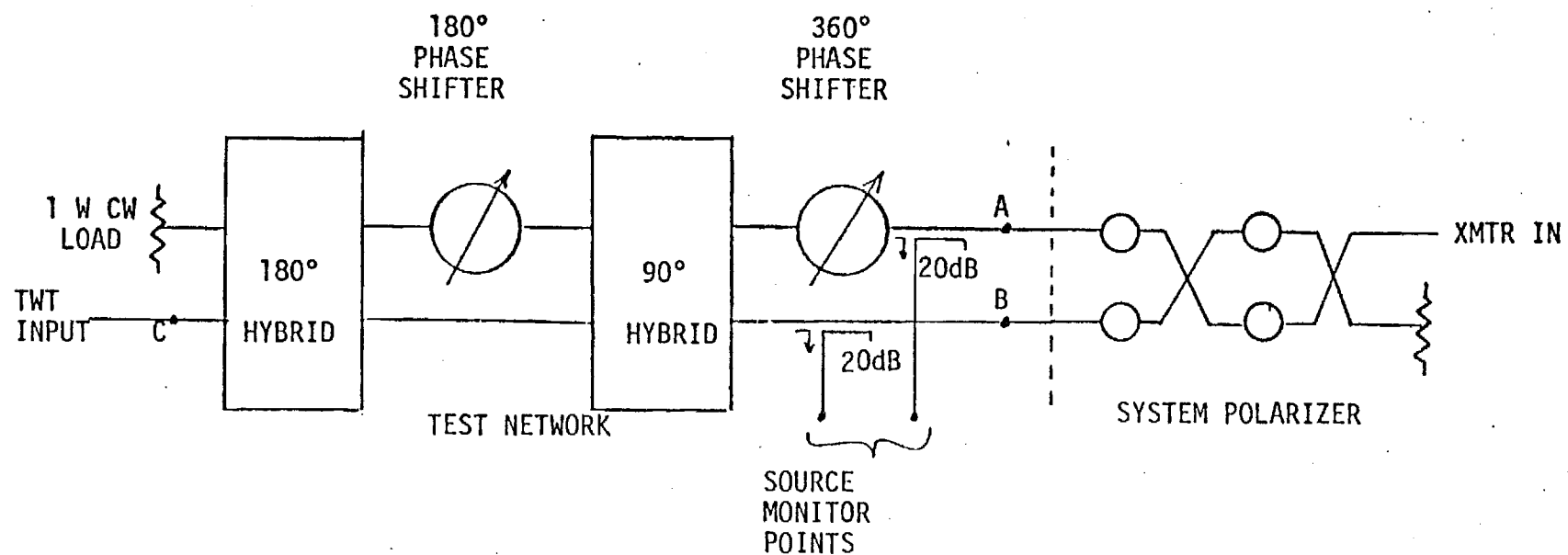


Figure 2-3. Mechanical Polarizer Network - Receive Only Configuration

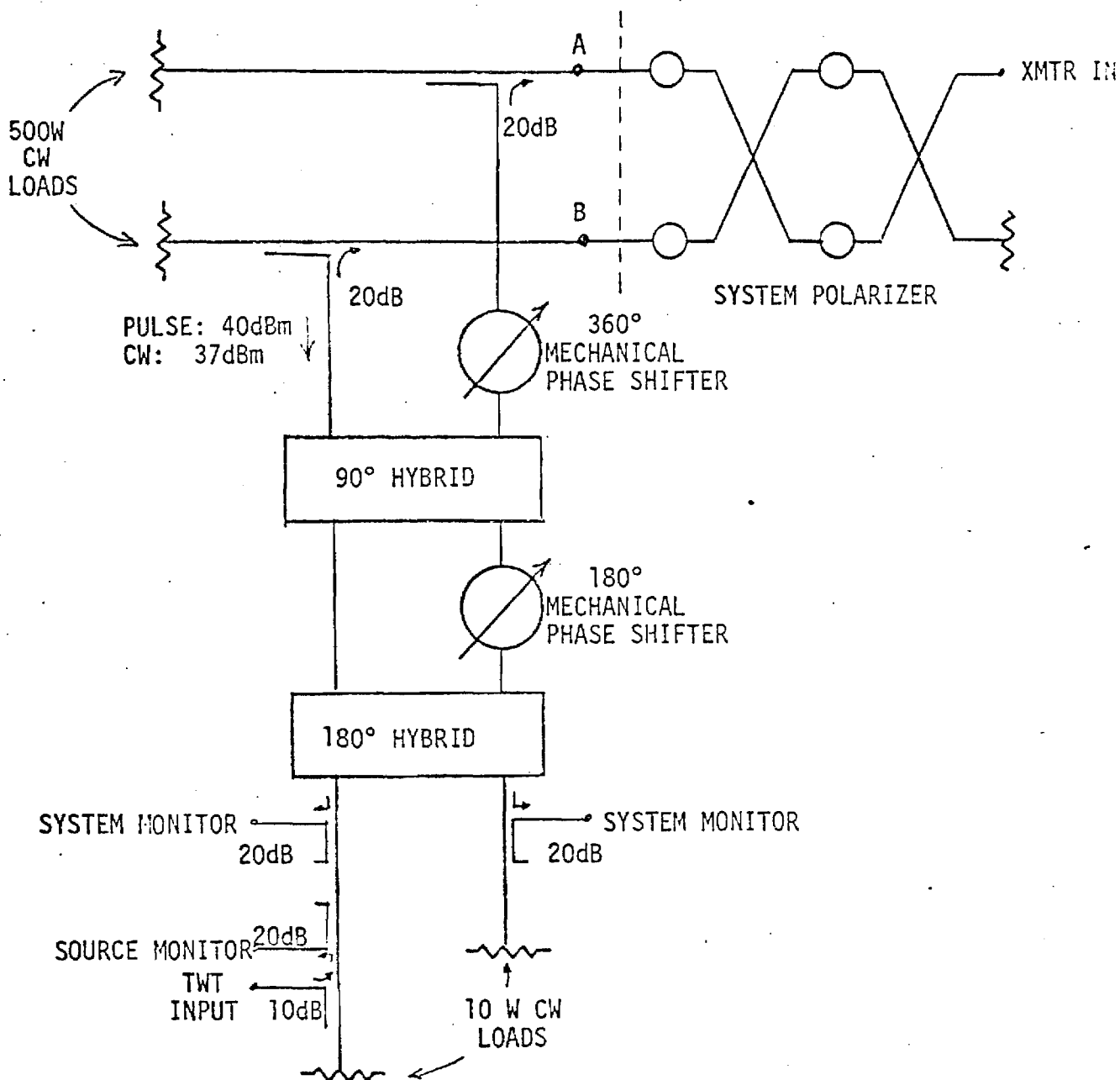


Figure 2-4. Mechanical Polarizer Network - Transmit/Receive Configuration

3. X-Band RF RCVR FP switches:

AFC-1 OFF
VCO SELECT 1

4. Adjust AFC-1 TUNE on RF RCVR FP, while observing TEST SYNC, IF RCVR RF, on an oscilloscope.

5. When threat has been acquired manually, set

AFC-1 ON
VCO SELECT AUTO

FREQ LOCK indicator, Processor FP, should indicate AFC tracking

6. Record Source 1 spectrum, AUX. LO. OUT spectrum, RF OUT TO DRIVER spectrum

7. With frequency counters, simultaneously record Source 1 and AUX. L.O. OUT frequencies. Difference between measurements should be 60.0 MHz \pm 200 KHz. Record data every 30 seconds for 5 minutes.

8. Turn off Source 1.

(b) Source 2 Acquisition

1. Turn ON Source 2 and set up nominal Source 2 parameters

2. Processor FR:

Chan 1 OFF
Chan 2 REC

3. X-Band RF RCVR RF switches:

AFC-2 OFF
SEQUENCE 2
VCO SELECT 2/3

4. Adjust AFC-2 TUNE, RF RCVR FP, while observing TEST SYNC, IF RCVR FP, on a scope.

5. After threat has been acquired, set

AFC-2 ON
VCO SELECT AUTO

FREQ LOCK indicator, Processor FP,
should indicate AFC tracking.

6. Repeat 6 thru 8 in Source 1 acquisition above, substituting "Source 2" for "Source 1".

(c) Source 3 Acquisition

1. Turn ON Source 3. Set up nominal Source 3 parameters.

2. RF RCVR switches:

AFC-3 OFF
SEQUENCE 3

3. Adjust AFC-3 TUNE, while observing TEST SYNC.

4. After threat has been acquired, set

AFC-3 ON
VCO SELECT AUTO

FREQ LOCK indicator should light.

5. Repeat 6 thru 8 in Source 1 Acquisition, substituting "Source 3" for "Source 1".

b. Acquisition/Track Level

- (1) PURPOSE: Verify acquisition signal level and signal level range for full polarization tracking accuracy.

- (2) SET UP:

- (a) Set up test equipment as in Figure 2 and 3.

- (b) Verify normal switch settings.

- (c) Turn ON Source 1. Turn OFF Source 2 and 3.

(d) Set system RF power input at -25 dBm.

NOTE: Transmitters are not required.

(3) PRODEEDURE:

(a) Processor FP:

Chan 1	REC
Chan 2	OFF
AGC	LSB
POLAR ERROR	LSB

(b) Increase system RF power input until POLAR NULL indicator comes on.

(c) Record system RF power input (spec -15 dBm) and GAMMA and PHI ERROR, Processor FP.

(d) Increase input power. Record GAMMA and PHI ERROR at -10, -5, 0, +5, +10, +15 dBm.

(e) Decrease input power. Record GAMMA and PHI ERROR at -15, -20, -25, -30, -35 dBm.

(f) Processor FP:

AGC	FULL
POLAR ERROR	FULL

(g) Repeat steps (b) - (e).

c. Threat Parameters

(1) PURPOSE: Verify ability to track PRF and pulsewidth variations.

(2) SET UP:

(a) Set up test equipment.

(b) Verify normal switch settings.

(c) Turn ON Source 1. Turn OFF Source 2 and 3.

(d) Verify Source 1 parameters.

NOTE: Transmitters are not required.

(3) PROCEDURE:

(a) Processor FP:

Chan 1	REC
Chan 2	OFF

(b) Verify Source 1 acquisition and track.

(c) Decrease Source 1 PRF until PRF track is lost. Record PRF value (spec minimum = 630 Hz).

(d) Increase PRF until PRF track is lost, or until > 10 KHz. Record PRF (spec maximum = 3000 Hz).

(e) Set PRF at 1000 Hz.

(f) Decrease pulsewidth until track is lost. Record pulsewidth (spec minimum = 0.25 μ s).

(g) Increase pulsewidth until track is lost or until > 10.0 μ s. Record pulsewidth (spec = 4.0 μ s).

d. Threat Capabiltiy

(1) PURPOSE: To verify the ability to track two threats simultaneously, and three sequentially.

(2) SET UP:

(a) Set up test equipment.

(b) Verify normal switch and control settings.

(c) Turn on all three sources. Acquire all three sources as described in the Frequency Acquisition procedure.

NOTE: Transmitters are not required.

(3) PROCEDURE:

(a) Processor FP:

Chan 1	REC
Chan 2	REC

(b) Verify TRACK and POLAR NULL indicators ON for each channel.

(c) RF RCVR FP:

SEQUENCE	OFF
----------	-----

(d) Verify that Channel 2 alternately acquires and tracks Source 2 and Source 3.

(e) Adjust SEQUENCE RATE, RF RCVR FP, which controls the dwell time on each threat. Within the limits of the control, record the minimum dwell time for which track and polar null can be obtained. At the control limit, record the maximum dwell interval.

2. Pulse Transmitter Tests

a. Power Out/Null Depth

(1) PURPOSE: Measure system power output and two-way polarization null.

(2) SET UP:

- (a) Set up test equipment as in Figure 2-2 and 2-4.
- (b) Set up Source 1 with nominal parameters.
- (c) Establish Source 1 tracking and polarization null.
- (d) Allow transmitter to warm up.

(3) PROCEDURE:

(a) Processor FP:

Chan 1	XMIT
--------	------

- (b) Measure the peak power out of the system at the test points in the mechanical network. Add the coupling values and calibrated network loss figures to determine the RF levels in the high power network arms. Subtract these latter values to determine the two way null depth.
- (c) Vary both mechanical phase shifters over their full range. Record the maximum and minimum power level difference between the value found in 2 (e.g.: +2.3 dB, -1.7 dB), as each phase shifter is separately varied.
- (d) Repeat (b) and (c) at 500 MHz increments over the band.
- (e) Record the output spectrum at 9.0 GHz.

b. AM Test

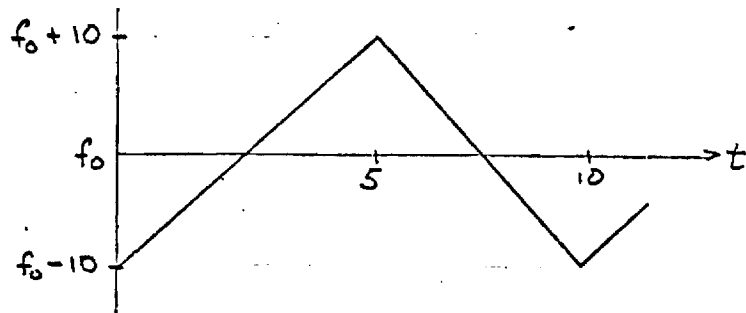
- (1) PURPOSE: Verify the AM capability of the pulse transmitter.
- (2) SET UP: (Same as a. Power Out/Null Depth)
- (3) PROCEDURE:
 - (a) Processor FP:

Chan 1 XMIT
 - (b) Record peak power out and RF output spectrum.
 - (c) Apply a DC level to the AM input on the Driver. Adjust the DC level to that specified to produce minimum power out. Record peak power out and RF output spectrum.
 - (d) Apply a 0.01 Hz sinewave from a function generator of sufficient level to cause 100% modulation. Record peak-to-peak sinewave input value, average power out, RF output spectrum, and detected output.
 - (e) Increase the source PRF to a maximum while maintaining track and polarization null. Decrease the source pulsewidth so that the duty cycle is $\leq 2\%$.

- (f) Increase the generator frequency to a value of $1/4$ of the PRF found in (e). Record the average power out, RF output spectrum and detected output.

c. FM Test

- (1) PURPOSE: Verify the FM capability of the pulse transmitter.
- (2) SET UP: (Same as a. Power Out/Null Depth Test)
- (3) PROCEDURE:
 - (a) Enable the transmitter.
 - (b) Measure the output RF frequency.
 - (c) Apply a DC source to the MOD IN BNC on the RF RCVR RP. At the specified minimum input level, measure the RF frequency. Record the input level and frequency.
 - (d) Adjust the DC source to the specified maximum input level. Record the level and the RF frequency.
 - (e) Remove the DC source and apply a 0.01 Hz triangle wave from a function generator. The output value should be adjusted to produce ± 10 MHz output RF frequency excursions.



Record the input level and observe the output spectrum.

- (f) Increase the triangle wave frequency to $1/2$ the maximum trackable PRF rate. Record the generator frequency and output RF frequency spectrum.

d. Polarization Modulation

(1) PURPOSE: Verify the polarization modulation capability.

(2) SET UP: (Same as a. Power Out/Null Depth Test)

NOTE: The polarization modulations will be observed at the PHI and GAMMA test points on the Polarizer front panel. These test points are analog representations of the actual phase shifter commands. Since the polarization modulations will be observed at this point, rather than detecting and processing the RF output, the transmitters are not required for this test. The transmitters will be enabled during the test procedure; however, the cables carrying the ON/OFF information should be disconnected from the processor front panel.

(3) PROCEDURE:

(a) Enable Chan 1 XMIT.

(b) Observe

PHI TEST	POLARIZER FP
GAMMA TEST	

GATE PRF-1	PROCESSOR FP
GATE XMIT	

On four channel oscilloscope. Record the data. (PHI and GAMMA Test will be switching between co-pole on receive and cross-pole on transmit).

(c) Apply a 0.001 Hz sine wave from a function generator to the POL MOD PHI BNC on the Processor FP. Adjust the generator for $\pm 5V$ output.

(d) Processor FP:

SAMPLE GATE	INTERNAL
POL MOD CH 1	ON

(e) Observe and record:

PHI TEST
GAMMA TEST
GATE PRF-1
FUNCTION GENERATOR

- (f) Increase the generator frequency to 1000 Hz. Increase the source PRF to the maximum track limit. Repeat (e).
- (g) Transfer the function generator output to the POL MOD GAMMA BNC on the Processor FP. Lower the generator frequency to 0.001 Hz and repeat (e) and (f).
- (h) Adjust the generator for 0.0 to 5.0 volt square wave at 1/2 the source PRF. Repeat (e).
- (i) Change THREAT SOURCE CH1 to MANUAL (Processor FP). Repeat (e).
- (j) Remove generator input. Record the PHI and GAMMA TEST point voltages and the existing manual PHI and GAMMA thumbwheel switch settings. Record the test point voltages at the following PHI, GAMMA settings: (000,000); (100,100); (200,200); (300,300); (400,400); (500,500); (600,600); (700,700).
- (k) Processor FP:
- | | |
|-------------------|----------|
| THREAT SOURCE CH1 | X-POLE |
| POL MOD CH1 | OFF |
| SAMPLE GATE | EXTERNAL |
- (l) Apply 15 KHz, 1.0 μ s, 0-4 pulse train to SAMPLE GATE BNC, Processor FP.
- (m) Apply ± 5 V 1 KHz sine wave to POL MOD PHI BNC, processor FP. Enable POL MOD CH1. Repeat (e).

3. CW Transmitter Tests

a. Power Out/Null Depth

- (1) PURPOSE: Measure system power output and two-way polarization null.

(2) SET UP:

Configure the system for CW transmitter operation: turn OFF pulse XMTR, connect CW XMTR output to Polarizer, connect CW XMIT ON/OFF cable from processor, turn ON the CW XMTR. Repeat the set-up in 2.a.(2).

(3) PROCEDURE:

- (a) Repeat the procedure in 2.a.(3). Substitute "Average power" for "Peak power".

b. AM Test

- (1) PURPOSE: Verify AM capability of CW Transmitter.

- (2) SET UP: Same as 2.a.(2).

- (3) PROCEDURE:

- (a) Repeat (a) through (d) in 2.a.(3).
 - (b) Increase the generator frequency to 100 KHz. Record power out, output spectrum, detected output and input AM waveform.

c. FM Test

- (1) PURPOSE: Verify the FM capability of the CW transmitter.

- (2) SET UP: Same as 2.a.(2).

- (3) PROCEDURE:

- (a) Repeat (a) through (e) in 2.a.(3).
 - (b) Increase the generator frequency to 100 KHz. Record the power out, output Spectrum, input waveform and detected output.

4. Repeater Test

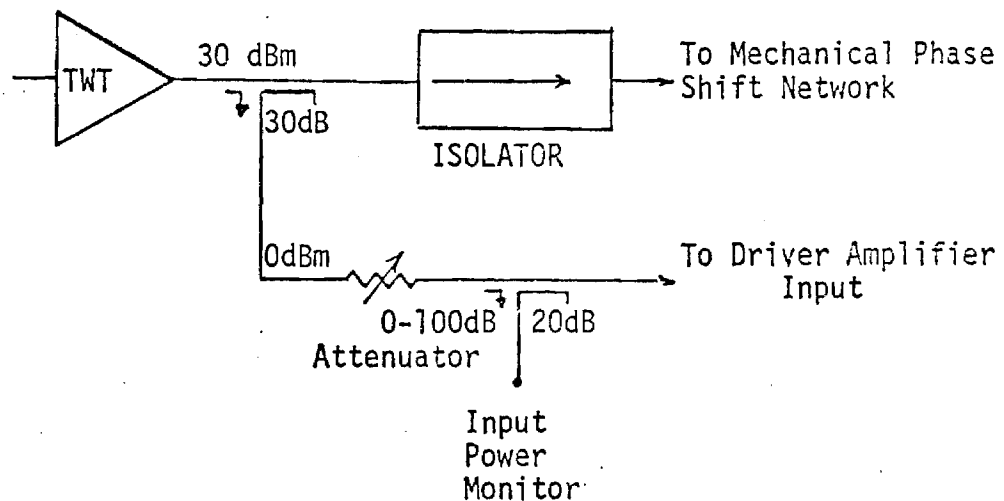
a. CW Transmitter Loop Gain

(1) PURPOSE: Verify repeater operation and determine system power gain in the CW Repeater mode.

(2) SET UP:

(a) Set up test equipment as in Figure 2-2 and 2-4.

(b) Configure the additional components as shown at the source TWT output:



(c) Establish CW Repeater system configuration.

(d) Establish Source 1 nominal parameters and verify Channel 1 tracking.

(3) PROCEDURE:

(a) Insert maximum attenuation at tWT attenuator pad. (Power input \leq -90 dBm)

(b) Enable Chan 1 XMIT.

(c) Record power in and system power out.

(d) Repeat (c) at approximately 5 dB increments of increasing input power.

- (e) Measure and record input and output RF power spectrums at a -10 dBm input power level.
- (f) Measure and record input and output RF power Spectrums at a -60 dBm inpt power level.

b. Pulse Transmitter Loop Gain

- (1) PURPOSE: Verfiy repeater operation and determine system power gain in the Pulse Repeater mode.
- (2) SET UP: (Same as 4.a.(2), except: (c) Establish Pulse Repeater system configuration.)
- (3) PROCEDURE: (Same as 4.a.(3)).

5. Auxiliary Receiver

a. Receiver Performance

- (1) PURPOSE: Verify auxiliary receiver operation.
- (2) SET UP: (Same as 4.a.(2)).
- (3) PROCEDURE:
 - (a) Insert maximum attenuation at the TWT attenuator pad.
 - (b) Insert a 10 dB coupler at the Auxiliary Receiver LO Input. Measure and record the input power and spectrum.
 - (c) At approximately 5 dB input power increments, record the input power and receiver output.

System Specification (Volume V of V)
EES/GIT Project A-1871

ADAPTIVE POLARIZATION ECM

Contract Number F33615-76-C-1250
Subcontract Number 1-A-1871

November 1979

Prepared for
U.S. Air Force Avionics Laboratory
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FOREWORD

This is the third of three volumes prepared by GE/AESD covering the operation and maintenance of the Adaptive Polarization ECM system. The system specification is described in this volume.

Volume III covers the functional description of the APECM and its test operating procedures.

Volume IV covers the drawings used in the APECM.

Volume V covers the system specification of the APECM.

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SECTION I

OVERVIEW

A. Document Objective

The intent of this document is to define the adaptive polarization ECM brassboard built for the Georgia Institute of Technology (GT).

B. Specification Outline

Section II is a summary of the overall system performance requirements; these requirements form the basis for the system and subsystem specification presented in Sections III and IV. Section III contains a block diagram of the system identifying the subsystem assembly discussed in Section IV. Section IV provides detailed specifications for the individual subassemblies.

C. Acceptance Tests

This document provides the basis for the system and subsystem acceptance tests, but does not provide detailed directions for testing.

SECTION II

SYSTEM PERFORMANCE REQUIREMENTS

A. Program Scope

The Adaptive Polarization ECM brassboard consists of an ECM equipment suitable for flight testing in T-29 or other cargo type aircraft.

Under this contract, General Electric has modified the existing Polarization ECM hardware developed under AFAL contract F33615-73-C-1123, and has incorporated an RF chain (driver, CW and pulse transmitters), a dual polarization antenna, and an auxiliary antenna and receiver provided by Georgia Tech.

This document applies only to the ECM brassboard system.

B. Program Objective

The primary objective was the development of a flyable brassboard to investigate the effects of various polarization modulations and techniques. In this regard the functions of the equipments are:

1. To provide suitable polarization tracking and modulation for flight test evaluation.
2. To allow AM and FM modulation to provide the baseline capabilities of a nonpolarization controlled ECM system.
3. To allow AM and FM capability to be used in conjunction with the polarization controlled ECM techniques.

C. Experimental Capability

1. Platforms

The experimental ECM airborne platform is a T-29 type aircraft.

2. Victims

Victims are understood to consist primarily of tracking radars employing monopulse or pseudo-monopulse angle tracking techniques.

3. Functional Requirements

The experimental ECM performs the following functions (the indicated parameters are nominal values):

- Angular Track Degradation - The ECM, through the utilization of polarization control of the transmit jamming signal (augmented by AM and/or FM as required), will degrade the performance of target tracking radars. The goal is to produce enough angular errors to create an acceptable computed miss distance against the automatic modes of the victims. Ideally, enough error shall be induced so that tracking lock-on will be broken and the associated weapon cannot be fired.
- Re-Acquisition Confusion - Polarization control is to be used to evaluate its potential for confusion of the tracking radar operator during the target search and acquisition process.
- Threat Capability - The ECM is able to acquire (following initial manual set-up) and track two interleaved victim signals. A third victim may be tracked and countered on a sequential basis.

D. Parameter Requirement Summary

The following list of system parameter requirements is based on the functional requirements listed in Section C. This is a summary of the system parameters only; a more detailed description of these and other parameters is contained in Section IV.

1. System Type

The system shall be capable of operation in either a transponder or repeater mode.

2. RF Coverage

Receiver	8-11 GHz
Polarizer Network	8-11 GHz
Pulse Transmitter	8-11 GHz
CW Transmitter	8-11 GHz

3. Transmitters

Two transmitters (one pulsed and one CW) are provided. These are constructed in such a manner that only a short time (30 minutes) is required to change from one to the other.

a. Pulse Mode Output Power

Peak Power	1800 W
Average Power	50 W
Pulse Width	10 μ s maximum

b. CW Mode Output Power

Average Power	500 W
---------------	-------

The transmit powers shall be measured as the sum of the two polarizer output ports.

4. Cross Polarization Tracking Accuracy

Static	$\pm 1^\circ$
Rotating Linear	$\pm 5^\circ$

5. Transmit Polarization Accuracy

a. Cross Polarization

Static	$\pm 1^\circ$
Rotating Linear	$\pm 5^\circ$

b. Modulation

Static	$\pm 20^\circ$
Rotating Linear	$\pm 20^\circ$

6. Polarization Modulation Waveforms

Source	External Generators
Waveform	Any
Rotation Rate	0.001 to 1000 Hz
Dither Rate	0.001 to 1000 Hz
Switching Rate	0.01 to 15,000 Hz
Major Axis	Yes
Ellipticity	Yes

7. Polarization Reference States
- The above polarized modulation shall be made relative to:
- The tracked cross polarization, or
 - A polarization (major axis and ellipticity) state which can be manually controlled.
8. Threat Capability
- | | |
|--------------------------|---|
| Interleaved Pulse Trains | 2 |
| Sequential | 3 |
9. Amplitude Modulation
- | | |
|-------|--------------------|
| Depth | 0 to 40 dB |
| Rate | 0.01 Hz to 100 kHz |
10. Frequency Modulation
- | | |
|-----------------|--------------------|
| Deviation (p-p) | 20 MHz |
| Rate | 0.01 Hz to 100 kHz |
11. Threat Pulse Width
- 0.25 to 4.0 microseconds
12. Threat PRF
- | | |
|---------|-------------------------|
| Range | 630 to 3000 Hz |
| Stagger | Single Stagger, 20% max |
| Jitter | 5 microseconds max |
13. Receiver Sensitivity (Referenced to the Antenna Terminals)
- | | |
|---------------------------------------|------------------|
| Acquisition Level | -15 dBm |
| Signal Strength for Full Polarization | |
| Tracking Accuracy | -25 dB to +5 dBm |
14. Frequency Acquisition
- Manual, observing Pulse Present AFC to ± 200 kHz
15. Transponder Transmit Frequency Accuracy
- ± 250 kHz

16. Threat RF Drift

1 MHz/minute ± 10 MHz max total drift.

17. Polarizer Antenna

Elevation Beamwidth	$\pm 15^\circ$
Azimuth Beamwidth	$\pm 15^\circ$
Gain	15 dB
Polarization	See IV.A

18. Auxiliary Antenna

Elevation Beamwidth	$\pm 15^\circ$
Azimuth Beamwidth	$\pm 15^\circ$
Gain	15 dB
Polarization	Circular

SECTION III

ECM SYSTEM DESCRIPTION

A. Functional Block Diagram

Figure 3-1 is a functional block diagram of the experimental ECM System. The units shown in this figure and itemized below are provided for the purpose of identifying the various subsystems and components and to clarify subsequent discussion.

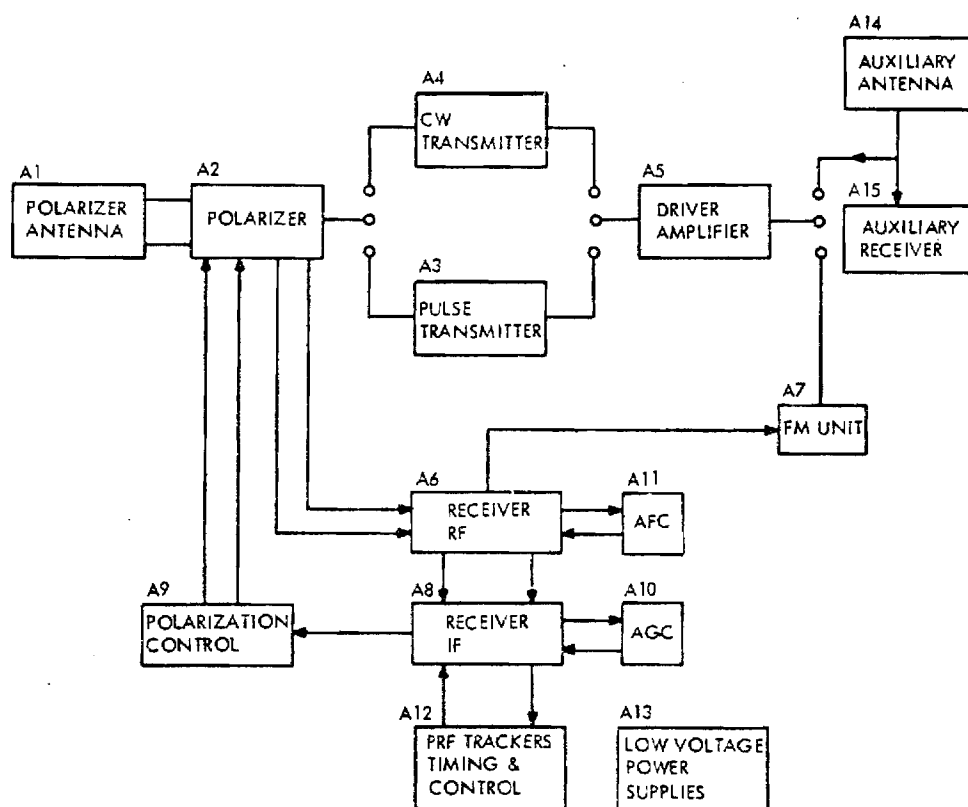


Figure 3-1. System Block Diagram

- A1 Polarizer Antenna
 - Dual polarization antenna
- A2 Polarizer
 - Hybrids and Phase Shifters
 - Phase Shift Drivers
 - Receiver/Transmitter Couplers
- A3 Pulse Transmitter
 - High Power TWT
 - TWT Power Supply
 - TWT Modulator
 - TWT Protection Circuits
- A4 CW Transmitter
 - CW TWT/Power Supply
 - TWT Modulator
 - TWT Protection Circuits
- A5 Driver Amplifier (RF)
 - Amplitude Modulator (See II.D.9)
 - Gain (manual) Control Attenuator
 - Amplifier(s) and Power Supply
- A6 RF Receiver
 - Transmit Protection
 - Mixer/Preamplifier
 - Local Oscillator
- A7 FM Unit
 - SSB Modulator
 - 60 MHz Oscillator(s)
- A8 IF Receiver
 - IF Amplifiers
 - Phase Detectors
- A9 Polarization Control
 - Tracking Loops
 - External Modulation Interface

- A10 Automatic Gain Control
- A11 Automatic Frequency Control
 - Discriminator
 - Sequential Timing for Third Threat
- A12 PRF Trackers Timing and Control
 - System Timing
 - Operator Interface
- A13 Low Voltage Power Supplies
- A14 Auxiliary Antenna
- A15 Auxiliary Receiver
- A16 RF Waveguide

B. Environmental Considerations

1. Mechanical

The ECM system is constructed as a flyable brassboard. The antenna units (A1 and A14) are compatible with installation in test aircraft radomes. The remaining hardware, including necessary test equipment, is suitably rack mounted.

a. Size and Weight

The antenna unit (A1) design goal is found in Vol. I. The remaining hardware uses no more than 6 feet of vertical rack space. The minimum or maximum weight of the equipment is not specified.

2. Altitude

The system shall be capable of operation from 0 to 35 thousand feet above sea level.

3. Vibration

The ECM system, when mounted in the provided shock-mounted racks, operates satisfactorily in the following vibration environment.

± 0.01 inch double amp 5 Hz to 32 Hz
 ± 2 g's from 32 Hz to 500 Hz

4. Temperature

The ECM system components inside the test aircraft are designed to operate over the temperature range of 0°C to 50°C. This equipment is not damaged by storage (nonoperation) at temperatures from -30°C to +55°C. The external components such as the antenna units are designed to operate at a range of -30°C to +55°C.

5. Humidity

All system components operate over the range of 0 to 95% relative humidity.

6. System Prime Power

The system uses 400 Hz 3 phase. The total input prime power shall not exceed 5 kw.

SECTION IV
SUBSYSTEM PARAMETER SPECIFICATION

A. Polarizer Antenna (A1)

This specification describes the antenna which provides the interface between freespace and the polarizer. The antenna uses dual polarization ports, and is both passive and reciprocal. It is used for both transmit and receive.

1. Description

The Polarizer Antenna is to be supplied by GT. (See Vol. I.)

2. Antenna Gain

The antenna gain is compatible with the required azimuth and elevation coverage and the RF band (15 dB nominal DG).

3. Antenna Beamwidth (3 dB point):

Elevation	$\pm 15^\circ$ (DG)
Azimuth	$\pm 15^\circ$ (DG)

4. Antenna Polarization

The antenna has a dual polarization capability. Each polarization is to be coupled to its corresponding antenna port. One antenna port is right circularly polarized; the other is left circularly polarized.

5. Gain Match

Over the RF band and at any point within the beamwidth stated above, the gain of the two ports is the same within ± 2 dB. The gain of each port is measured using the nominal polarization of the specific port; that is, right circular is used for one port and left circular for the other (DG).

6. Phase Match

Over the RF band at any point within the beamwidth stated above, the phase match of the two ports is held within $\pm 14^\circ$ (DG).

7. Polarization Match

Over the RF band and at any point within the beamwidth stated above, the polarization accuracy, as defined below, shall be within $\pm 10^\circ$.

Using equal amplitude, in-phase RF signals as the inputs to the two ports, the resulting far-field polarization shall be vertical $\pm 10^\circ$ ($2\delta = 20^\circ$ on the Poincare sphere). Both major axis and ellipticity errors are included.

8. Antenna Sidelobes

No direct specification.

9. Polarization Purity

Over the RF band and the beamwidth of each port (independent), the polarization shall be within $\pm 10^\circ$ of the nominal design; that is, $\pm 10^\circ$ of right circular and $\pm 10^\circ$ of left circular (10° corresponds to a 3.4 dB ellipticity).

10. Port Isolation

A signal into either port shall appear at the other down at least 20 dB.

11. Frequency

The antenna shall meet all specifications over the 8-11 GHz band.

12. VSWR

$\leq 2.0:1$

13. Antenna Mounting

See Vol. I.

14. Connectors

UG-39/U or UG-125/U, small "x" (1" x 1/2") cover flange.

15. RF Power

The antenna shall be capable of handling 4.0 KW peak power, 10 μ s pulsewidth, at a 4% duty cycle or 600 watt CW RF at an altitude of up to and including 35 thousand feet.

B. Polarizer (A2)

1. Scope

The polarizer provides digital control of phase and amplitude characteristics of transmitted and received signals. When configured in a system, the polarizer allows transmission of energy which can be controlled in polarization.

2. Configuration

a. General

The Polarizer consists of RF subassemblies, digital interface circuits, and power supplies as shown in Figure 4-1. The Digitally Controlled Phase Shifter Assembly is a separate subassembly which is included in the Polarizer.

b. Size

The polarizer is contained in a 19-inch rack-mounted drawer.

c. Connectors

The RF connectors are UG-39/U or UG-135/U. The digital connectors are BNC.

d. Input Power

The input power is 115 V, 400 cycle, single phase AC.

3. Specifications

a. RF Specifications

Frequency	8-11 GHz
Peak Power into Port 5	5.0 kW max 1.8 kW min
Average Power into Port 5	600 W max 500 W min

Insertion Loss (5 to sum 1 + 2)	2.7 dB max
Phase Control between 1 and 2 for input to 5	Range Resolution
	0 to 360 degrees <u>≤</u> 1.4 degrees
Amplitude Control between 1 and 2 for Input to 5	0 to 30 dB
VSWR (All Ports)	2.0:1 from 8-10.5 GHz 3.0:1 from 10.5-11 GHz
Duty Cycle/Time Interval Limits for Peak Power Input	100%/10 μ s 50%/60 μ s 2%/1.5 ms or

more

b. Digital Interface Specifications

Shift Clock Rate	2.5 MHz (min)
Transmission Line Impedance	93 ohms
Amplitude Control Bits γ_x, γ_z	9 bits each
Phase Control Bits ϕ_x, ϕ_z	10 bits each
Signal Levels	TTL

c. Driver Specifications

Switching Speed	10 μ s max
Switching Rate (Changes/ Interval)	1/20 μ s 3/60 μ s 3/200 μ s
Switching Rate - Average	15 kHz

d. Transmitter/Receiver Couplers

(1) Coupling

The nominal coupling is 10 dB.

(2) Directivity

The directivity is at least 15 dB.

(3) RF Power

Peak RF power 5.0 kW

CW RF power 600 W

(4) Isolated Arm Termination

Shall be able to dissipate:

- 500 W peak

- 60 W CW

(5) Connectors

UG-39/U or UG-135/U are used throughout.

(6) Coupler Match

(a) Coupling

A coupling match of ± 1.5 dB is maintained across the RF band (DG).

(b) Phase

A phase match of $\pm 5^\circ$ is maintained across the RF band (DG).

e. Σ Port Load

(1) Power

TBD

(2) VSWR max

TBD

C. Pulse Transmitter Unit (A3)

The function of the pulse transmitter is to amplify the RF energy to an effective level.

This unit consists of a TWT, power supplies, modulator (grid pulse drive) and protection circuits.

1. Peak Power

Transmitter Unit

a. TWT

Over the 8-11 GHz band, the minimum saturated peak power output shall be 1.8 kW. The maximum peak power output shall be 3.0 kW.

b. Output Losses

The RF losses from the TWT output to unit front panel connectors shall be less than 0.7 dB.

2. Pulse Width and Duty

The maximum pulse width requirement is 10 microseconds. Two pulses may occur with a leading edge to leading edge spacing of 30 microseconds. However, in any 350 μ s time period, a maximum of two 10 μ s pulses will be required. The long term maximum duty cycle required will be 4 percent.

3. TWT Pulse Control

The input control pulse is a TTL pulse, the width of which corresponds to the pulse width desired.

4. Pulse Delay and Rise Time

A CW signal is input to the TWT with the tube being pulsed on.

a. Rise and Fall Time

The maximum RF rise or fall time (10% to 90% or 90% to 10%) shall be 50 nanoseconds.

b. Turn-on Delay

The maximum delay from 90 percent of the input control pulse leading edge to 90 percent of the RF pulse shall be less than 100 nanoseconds.

c. Turn-off Delay

The maximum delay from 10 percent of the input control pulse trailing edge to 10 percent of the RF shall be less than 500 nanoseconds.

5. Gain (Saturation)

Total gain from the Driver TWT unit (A5) input to Polarizer (A1) unit output is 90 dB or more. This includes all the losses.

6. Saturation Characteristics

A RF overdrive of 10 dB causes no more than a 3 dB reduction of output power (DG).

7. Gain Variation

The gain varies less than 3 dB (± 1.5) over the 8-11 GHz band (DG).

8. Feedthrough

With maximum RF (+6 dBm) applied to the Driver TWT unit (A5) and with the final TWT off, the RF output of unit A3 shall be less than -80 dBm.

To accomplish this, an RF switch prior to the final TWT input may be required. This switch would probably be in the Driver A5 unit. See Section IV.E.2.

9. Operating Load VSWR

The above requirements are to be met while operating into any load which has a VSWR of 2:1 or less.

10. TWT Protection

TWT protection shall be provided to prevent tube damage due to:

- Load VSWR (2:1 to ∞)
- High duty cycle (or even CW) control command
- Environmental heat

A manual reset is permissible if any of the above occurs.

D. CW Transmit Unit (A4)

The function of the CW transmitter is to amplify the RF energy to an effective level.

This unit consists of a TWT, power supplies, modulator (grid pulse or gated power supply), and protection circuits.

1. Output Power

- a. TWT

Over the 8-11 GHz band, the minimum saturated output power is 500 watts. The maximum output power 600 watts.

- b. Output Losses

The RF losses from the TWT output to the front connector are less than 0.7 dB.

2. Noise Output

With no RF drive applied, the output noise density is less than -90 dBm/MHz at all points across the 8-11 GHz band. To accomplish this, the TWT can be gated off or a high power switch following the TWT can be used if necessary.

3. Feedthrough

With an RF level of up to +6 dBm applied to the Driver (A5) unit, but with the system in the receive mode, the RF output of unit A4 shall be less than -80 dBm. To accomplish this, an RF switch prior to the final TWT input may be required. This switch would probably be in the Drive (A5) unit. See Section IV.E.2.

4. Turn-off Time

The time from the turn-off command to the time at which IV.D.2 is met is to be no more than 65 microseconds.

5. Turn-on Time

The time from the turn-on command to the 90 percent point of the external RF output power is to be no more than 150 microseconds.

6. Duty Cycles

The maximum average rate of turn-offs shall be 2 kHz.

7. Gain (Saturation)

Total gain from the drive unit (A5) input to the Polarizer (A1) unit output is 90 dB or more. This includes all the RF losses.

8. Saturation Characteristics

An RF overdrive of 10 dB shall cause no more than 3 dB reduction of output power (DG).

9. Gain Variation

The saturation gain shall vary less than 1.2 dB \pm 0.6 over the 8-11 GHz band (DG).

10. Operating Load VSWR

The above requirements are to be met while operating into any load which has a VSWR of 2:1 or less.

11. TWT Protection

TWT protection is provided to prevent tube damage due to:

- Load VSWR (1.8 to ∞)
- Environment Heat

A manual reset is permissible if any of the above occur.

E. Driver Amplifier (A5)

The primary function this unit is to provide RF drive for the transmitter units. It also contains the amplitude modulation capability.

It also contains the RF switch if one is needed to meet the requirements of Sections IV.C.8, IV.D.2, IV.D.3.

1. Output Power

Sufficient output power to drive either unit A3 or A4 into saturation is required.

2. Dynamic Range

The driver amplifier should have a saturation characteristics compatible with the final TWT drive requirements. The final amplifier output power should be reduced by no more than 3 dB due to overdrive when the driver amplifier input signal level varies from +7 dBm to -33 dBm. This performance should be met without a manual attenuation change.

3. RF Switch and Driver

a. Background

A RF switch is assumed to be used to help meet Sections IV.C.8 and IV.D.3 and this switch will be after the driver TWT (so that driver TWT noise need not be considered).

b. RF Maximum Power

Refer to Section IV.E.1.

c. Switching Speed

(1) Turn-on Delay

The maximum RF delay from the 90 percent point of the input control pulse leading edge to 90 percent of the RF output is less than 5 microseconds.

(2) Turn-off

The maximum delay from 10 percent of the input control pulse tracking edge to 10 percent of the RF is less than 5 microseconds.

(3) Duty

The RF switch is capable of operating continuously in either the ON or OFF position and capable of a switch rate of up to 15 kHz.

(4) Isolation

Isolation is sufficient to allow the requirements of Section IV.C.8, IV.D.2 and IV.D.3 to be met.

4. Amplitude Modulation

a. Depth

The depth of modulation requirement depends on the saturation characteristics of the final TWT. Therefore, no specification can be made at this time. See Section II.D.9.

b. Rate

The rate shall be 0.01 Hz to 100 kHz. This implies that for a given voltage swing, the modulation depth will vary no more than ± 3 dB (DG) as the frequency is changed through the above limits.

c. DC Offset

A manual DC offset should be incorporated in the Unit (A5) so that a bipolar (noise) waveform can be used.

d. Modulation Source

All modulation waveforms shall be provided by external test equipment.

5. Gain

Refer to requirements in Section IV.C.5 and IV.D.7.

6. Saturation Characteristics

A RF overdrive of 10 dB shall cause no more than a 3 dB reduction of output power.

7. Gain Variation

The saturation gain shall vary less than 3 dB (± 1.5) over the 8-11 GHz band.

8. TWT Protection

TWT protection shall be provided to prevent tube damage due to:

- Load VSWR (1.8 to ∞)
- Environment Heating

A manual reset is permissible if any of the above occur.

F. RF Receiver (A6)

The RF Receiver consists of a matched pair of receivers. It includes the local oscillators, mixers, IF preamplifiers, and any additionally required switches, couplers, and isolators.

The receiver input is defined to be at the connector to the 10 dB arm of the transmitter/receiver coupler. The output is defined to be the IF preamplifier output.

1. RF Coverage

The RF coverage is 8-11 GHz.

2. Multiple Threats

The receiver is capable of switching RF between two relatively fixed frequencies. It is capable of changing frequency to the other threat in 4 microseconds with an accuracy of ± 200 kHz. This assumes that each threat has been acquired and the AFC is operating with each threat.

3. Match

The RF receiver provides accurate signals to the IF for processing. The receiver does not change the relative amplitude of the Σ and Δ signals by more ± 3 dB (DG) and does not change the related phase of the Σ and Δ signals by more than 10 degrees.

4. Dynamic Range

a. Signal

The input signal is between -40 and -10 dBm.

b. Transmit RF

The transmit RF does not cause receiver burnout. Following a transmitter RF signal, the receiver recovers rapidly.

The maximum transmit RF power at the input to the receiver is:

50 watts pulsed (10 μ s max), 4% maximum duty cycle,
or 5 watts CW

The receiver recovers its full sensitivity and accuracy in 10 microseconds (DG).

5. Noise Figure

A signal-to-noise ratio (S/N) of 0 dB is required for a signal level of -85 dBm.

6. IF Interface

a. Drive

The RF receiver (A6) is capable of driving a pair of 50-ohm matched RG-55 cables.

b. Center Frequency

The IF center frequency is 60 MHz.

c. Bandwidth

The IF bandwidth is nominally 10 MHz.

7. SSB Modulator (A7) Interface

The RF receiver unit supplies an RF output at -10 dBm or more. This port is capable of driving a 50-ohm matched line.

8. Auxiliary Receiver (A15) LO

An LO signal is provided at nominally -20 dBm to the auxiliary receiver. It is the same frequency as that supplied to the mixers in the RF Receiver (A6).

9. Spurious

All spurious response shall be identifiable by the operator during manual acquisition.

10. Local Oscillator Linearity

It is desired that the tuning curve be monotonic and that it not have a slope change of more than 2:1.

G. FM Unit (A7)

The FM unit provides a transponder signal capability. It will generate this signal by offsetting in frequency (60 MHz) the receiver LO. By the selection of a stable or modulated 60 MHz source, the resulting RF can be accurate and stable, or FMed.

1. Stable Mode Stability

The stable 60 MHz oscillator shall contribute less than ± 50 kHz to the transponder RF instabilities (DG).

2. FM Mode

In this mode the oscillator (a different oscillator from the stable one) is capable of being FMed over a peak-to-peak deviation of 20 MHz (± 10 MHz) at rates from 0.01 Hz to 100 kHz.

3. Modulation Source

The modulation signal will be an external source with at least a 10-volt p-p (± 5 volt) amplitude capability.

4. Spurious RF

All spurious RF outputs (taken one at a time) are at least 10 dB below the desired frequency.

5. Output Power

The power output is sufficient to drive the amplifier chain to saturation (estimated to be -27 dBm).

6. Spurious 60 MHz

During the receive mode, the 60 MHz oscillator(s) are turned off or switched off to prevent interference to the receiver.

H. IF Receiver (A8)

The IF receiver consists of dual IFs, called the Σ and Δ channels, and a pair (I and Q) of phase detectors.

1. AGC

The Σ IF provides a video pulse from which the AGC function can be derived.

2. Pulse Present

A filtered and detected Σ IF output provides the "Pulse Present" function.

3. AFC

An IF output is provided to the FM discriminator, from which AFC error information can be derived.

4. Center Frequency

The nominal center frequency is 60 MHz.

5. Bandwidth

The nominal bandwidth is 10 MHz.

6. Match

The receiver provides accurate Σ and Δ signals to the phase detectors. The receiver does not change the relative amplitude of the Σ and Δ signals by more than +3 dB. The relative phase of the Σ and Δ signals are not changed by more than 5 degrees.

7. Phase Detector

The Phase Detector provides two outputs: one proportional to $\sin \theta$ and the other proportional to $\cos \theta$, where θ is the phase angle between the Σ and Δ IF signals.

I. Polarization Control (A9)

The Polarization Control is comprised of digital servo loops and polarization modulation interface circuits which control the digital phase shifters in the Polarizer assembly. The Polarization Control consists of two essentially identical error loops, called the Gamma Processor and the Phi processor. The Polarization Control has the ability to track the polarization of two threats.

1. Polarization Modulation

Each Processor provides analog-to-digital interface elements so that the output polarization command to the Polarizer can be externally modulated.

The external polarization modulation signal source bandwidth is 0.001 Hz to 1 kHz. The input source is -5 to +5 V.

The polarization modulation is with respect to a manual setting or the cross-polarized tracking state.

Polarization modulation will be disabled when the reference state is cross-polarization, and the threat is not being tracked.

Polarization modulation will be disabled during any receive event (lookthrough). During lookthrough, the polarization command will be the reference state, except when the rate-aided mode is enabled.

2. Modes

The operator may select either the cross-polarized or manually determined reference state for either threat channel. The manually determined reference state will be the same for each threat channel.

The operator may select a rate-aided mode, in which a manually determined increment is added to the polarization command. The manually determined increment will be the same for either threat channel.

The rate-aided mode may be enabled independently of the reference state selection.

3. Interface

The inputs to the Gamma and Phi Processors are the respective analog outputs of the receiver phase detector.

The modulation inputs to the Gamma and Phi Processors are externally supplied analog voltages.

The output polarization commands to the Polarizer are serial digital bit streams. Updated polarization commands will be sent to the Polarizer before each threat signal arrival.

J. AGC (A10)

The sum (Σ) channel IF output level is maintained at a fixed level to simplify the polarization error detection process.

The Δ channel is given the same gain level, but its signal level is typically 35 to 50 dB below that of the Σ channel.

1. Input Dynamic Range

The system must operate correctly (accurate polarization) over an RF dynamic range (at the antenna terminals) of +5 to -25 dBm.

2. Output Level

The output level is the maximum which is consistent with:

- a. The maximum IF gain
- b. The maximum allowable input to the phase detector

3. Output Variations

The sum IF output variation is less than ± 0.5 dB (DG).

4. Response Speed

The response speed is such that the system is able to track a 12 dB per second amplitude change (DG).

K. AFC (A11)

The receiver is tuned in frequency both manually and automatically. The manual adjustment sets the receiver frequency ± 16 MHz (DG). The frequency is updated by a 62.5 kHz frequency step shortly after each receive event. During a received pulse, the frequency error is measured. A decision to either increase or decrease the LO frequency is then made.

1. Frequency Acquisition

The frequency acquisition circuits are included in the AFC. The acquisition process is started by manually tuning a VCO (LO) to the correct frequency (± 16 MHz).

The VCO sweeps slowly (125 kHz/ms) in a ± 16 MHz band around the manually set frequency. This sweep is continued until such time as a "pulse present" is received.

PRF tracking is then attempted. If it is successful, the AFC begins to operate.

2. Image Rejection

Provision is included in the acquisition procedure to insure the AFC does not track an image.

3. Accuracy

A LO frequency accuracy of ± 200 kHz or better is required.

4. Stability

The AFC provides an accurate LO for a fixed signal frequency. Stability of 1 MHz/minute is estimated to be adequate.

L. PRF Trackers Timing and Control (A12)

The system contains a PRF Tracker which updates on a periodic basis and which is used to generate system timing based on the arrival of victim radar pulses. The Tracker has the capability to track two interleaved pulse trains. Pretrigger outputs from the tracker are used for receiver and transmitter sequencing.

1. Lookthrough

Either the pulse or CW transmitter will normally be on, except when a lookthrough event occurs. During a lookthrough event, the transmitter is turned off and the receiver is enabled, allowing the tracked parameters (frequency, PRF, gain, and polarization) to be updated. The lookthrough rate is expressed as the number of actual receive events out of a total number of possible receive events. For example, a lookthrough rate of one in five corresponds to one receive event every five pulses. The transmitter is enabled for four out of five pulses. When countering two threats, the lookthrough rate is the same for each threat.

2. Threat Selection

When countering two threats, in most cases the PRFs will be unsynchronized. In this case, at certain times the two threat events will occur at the same time or be close enough so that the system cannot respond to both threats. When this overlap condition occurs, system response is made by alternate selection in a regular way.

When the threats are synchronized, this regular alternate selection will also occur.

The overlap process and response will only occur during tracking. During search, each channel will be enabled for approximately one second intervals. During acquisition, a given channel will be enabled until PRF track is established (up to 14 ms). For example, if channel 1 is tracking and channel 2 starts acquisition, the timing will skip a few track pulses until the PRF on channel 2 is established.

3. Drop Out Timers

In the event that PRF track is lost, a Drop Out Timer (DOT) is enabled, permitting the system to hold the radar parameters for a 2 second time period. This function prohibits the acquisition process from being reinitiated needlessly. If PRF track is lost for over 2 seconds, the gain reverts to the search level, the polarization setting reverts to its acquisition value, and the frequency control normally enters the search mode.

4. PRF Pretriggers

Once the PRF track has been established in a given channel, the PRF Tracker will issue a Pretrigger prior to the expected arrival of the threat pulse. Subsequent receiver and transmitter switching will be based on the Pretrigger:

<u>Event</u>	<u>Time</u>
Pretrigger	+66 μ s
Polarizer Update	+20 μ s
Gain Update	+10 μ s
LO Switch	+10 μ s
Receiver Enable	+6 μ s
Transmitter Enable	+2 μ s

5. PRF Tracker Performance Parameters

PRF Range	650-3000 Hz
PRI Resolution	200 ns
Pretrigger	66 μ s
Stagger	20% max
Jitter	5 μ s max
Update Rate	1/29 min

M. Low Voltage Power Supplies (A13)

The low voltage power supplies generate all required voltage levels for system operation. Prime power is three phase, 400 Hz, 115 V.

N. Auxiliary Antenna (A14)

1. RF

The antenna operates over the 8 - 11 GHz band.

2. Polarization

The polarization is circular.

3. Spatial Coverage

$\pm 15^\circ$ of elevation and $\pm 15^\circ$ of azimuth coverage (DG).

4. Gain

15 dB (DG).

5. Output Connectors

Standard small "x" waveguide.

O. Auxiliary Receiver (A15)

The Auxiliary Receiver is used to derive scan rate information from threat signals. The unit consists of a directional coupler, mixer, IF amplifier, and detector.

1. Specifications

RF Coverage	8-11 GHz
Dynamic Range	-33 to +7 dBm
Noise Figure	17 dB
LO Driver	-20 dBm
IF Frequency	60 MHz
IF Bandwidth	20 MHz
Antenna to Mixer Losses	36 dB min

2. LO Injection into Repeater Amplifier

The LO signal level at the input to the repeater amplifier shall be less than -85 dBm.

3. Transmitter Injector into Auxiliary Mixer

Signal path losses from the RF Receiver (A6) mixers to the Auxiliary Receiver mixers shall be at least 90 dB.

P. RF Waveguide

The antenna will be located in a radome while the polarizer is located in the cargo/passenger area. This requires a pair of low-loss matched waveguide runs. The phase match required is equivalent to 0.1 inch of line length difference.

This is not a realistic goal; therefore, a waveguide line length adjustment will be provided. This adjustment compensates for line length differences of up to ± 2 inches.

During initial set-up in the aircraft, it is necessary to have access to the antenna ends of these waveguide runs. It is necessary to input a test RF signal at these points to provide a source for measurement during the line matching.