Mixed-source Charger-Supply CMOS IC

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Mixed-source Charger-Supply CMOS IC

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Summary

With the advances in the silicon integration technologies, self-powered microsystems, such as wireless sensors, are widening their application areas in military reconnaissance, biomedical implants and smart grids, where they can greatly enhance human capabilities in gaining important information. One of the greatest technological challenges in such volume-constrained systems is the limited on-board energy, which translates into the operational lifetime. Another challenge comes from the limited power capability from the on-board source, which will also constrain the functionality of the microsystems. However, as it is difficult for a single source to be both energy-dense and power-dense, using two complementary energy sources together can achieve a higher level of integration than single-source-based solutions. The power conditioner for such dual sources should not only be power-efficient, but also have the control intelligence that can adaptively select a suitable source for time-varying loads, to be able to fully benefit from using mixed energy sources.

Therefore, in this research, a mixed-source charger-supply CMOS (complementary metal-oxide-semiconductor) IC (integrated circuit) is investigated and developed to validate the benefit of using mixed sources and the load-dependent, source-selecting control in supplying loads with high peak-to-average ratios. This converter selectively draws low powers from an energy-dense source to supply light loads, while engaging a power-dense source only for high, peak loads. When the load is light, the converter recharges the power-

dense source with the remnant energy from the energy-dense source. As the converter adaptively selects a suitable source for its load levels, the system can avoid over-sizing either the energy source or the power source for its conflicting demands in the operational lifetime and the peak power, and therefore can reduce the volume of energy sources.

Two mixed-source charger-supply CMOS ICs were designed, developed, and validated using 0.5-μm and 0.18-μm BiCMOS processes, respectively. The first prototype proved the functionality of the load-dependent, source-selecting control, but the maximum efficiency was low at 32%, due to excessive power losses in highly-switching operations. The second prototype improved the maximum efficiency to 81% by operating in discontinuous conduction mode and eliminating the current-sensing control. This prototype had two functional modes: the ESR-derived nested-hysteretic mode and the low-ESR (equivalent series resistance) PWM (pulse width modulation) mode. The former shows a faster response and a more compact circuit by utilizing an ESR-dominant hysteretic control, but it requires a high ESR for the stability. The latter is based on the PWM control, showing a slightly better efficiency than the former, without any constraints on the ESR. Both designs from the second prototype showed more than 68%'s volume reductions in the required energy sources to supply an example load, when compared to the state-of-the-art power supplies.

Chapter 1. Microsystems and Miniaturized Energy Sources

1.1 Applications

Rapid advances in IC and MEMS (micro-electro-mechanical system) technologies enabled handheld consumer products such as smart phones and tablets, integrating more functionalities within a smaller device' volume than ever imagined. Partly inspired by these successes or partly by insightful pioneers, there have been numerous predictions about more convenient futures that human societies can evolve into, benefiting from using wireless sensors in various fields, which enhance man's ability to gain more useful information in a lot easier and smarter ways [1]-[4]. Especially, sensing and actuating functionalities, which have originally been done in off-chip sensors and actuators, are now migrating onto silicon die, reducing the size of systems tremendously to a chip's level, eventually leading into the developments of wireless sensor units, called "motes" [1].

A mote refers to an autonomous, compact sensor unit having the capability of processing information and communicating in wireless channels [1]. The major advantage of motes is that they can form networks and co-operate each other to collect and process lots of data quickly, and even make a decision about how to respond to the given information quickly. Therefore, wireless sensor networks have been extensive research foci in vast areas including communications (in selecting robust and efficient communication channels and protocols,) electronics (in pursuing higher energy efficiency and higher level of miniaturization of each individual motes,) and network controls (in designing a robust,

fault-tolerant network control system in consideration of lower reliability issues in wireless sensor networks.) These small electronic sensors can be extremely useful in the sense that they can be placed to gain important information where human access is very dangerous, expensive, or even impossible, as in military reconnaissance [2], environment monitoring [3], and utility distribution applications [4]. The positions of sensor nodes do not have to be determined before the deployment, because their network protocol and algorithms can have self-organizing capabilities [5]. Each sensor node can be either a data originator or a data router, and the sensed raw data can be pre-processed locally by each sensor utilizing its computing power, before forwarding the pre-processed data to the data sink or the user [5]. In other words, sensors in the network work in a cooperative way to distribute the sensing and processing power to individual sensors to achieve wider coverage and reach a higher level in information's quality effectively.

The requirements on these wireless sensor networks can be more demanding than those on the existing ad hoc networks. First of all, the number of engaging nodes can be a lot more, anywhere from 10 to 100, 1000 and even to a million, making the network routing even harder and complicated [5]. The local density of the sensors can also be a lot higher, because the nodes are tiny and the deployments are not tightly controlled in general. This type of network is prone to any types of failures in small and numerous individual nodes, requiring the ability to quickly identify and exclude bad nodes from the network, and continue its task by reconfiguring its topology with no serious degradation in its output. Communication paradigm is in many cases broadcasting-based rather than point-to-point communications, because the latter is not guaranteed when the topology may change

frequently in time. And most of all, the total production cost of individual sensors and the network deployment should be lower than that of the traditional sensors. For example, the price of a piconode should be lower than US1$ to be profitable, in order to replace existing state-of-the-art Bluetooth radio system in [5].

1.1.1. Military

Wireless sensor networks can have huge merits in military applications in the sense that these moats can replace human labors in dangerous battlefields or other-than-war situations [1]-[2]. Fig. 1.1 shows an example of the deployment of a wireless sensor network detecting enemy vehicles in battlefields. Individual sensor nodes detect the location and movement of enemy vehicles in real time and broadcast the information to the sink node, which collects the information and eventually forward it to the command center. This technology can therefore reduce lots of risks and costs in information collection, enemy tracking, battle field surveillance and target classification [2].

One of the most important requirements on military sensors is that communications should be resistant to jamming, direction finding and electronic turbulence, while providing end-to-end security [2]. In addition, requirements on deploying wireless sensor networks can vary from battle field scenarios where manual placements of individual sensors are practically hard and dangerous, to other-than-war (OTW) scenarios where peacekeeping or disaster relief are the main objectives and therefore sensor deployment can be better controlled. In either case, having wireless sensor networks can provide a cost-effective method of gathering information, which reduces uncertainty over where the opponents will be deployed or which roles they will fulfill [2].

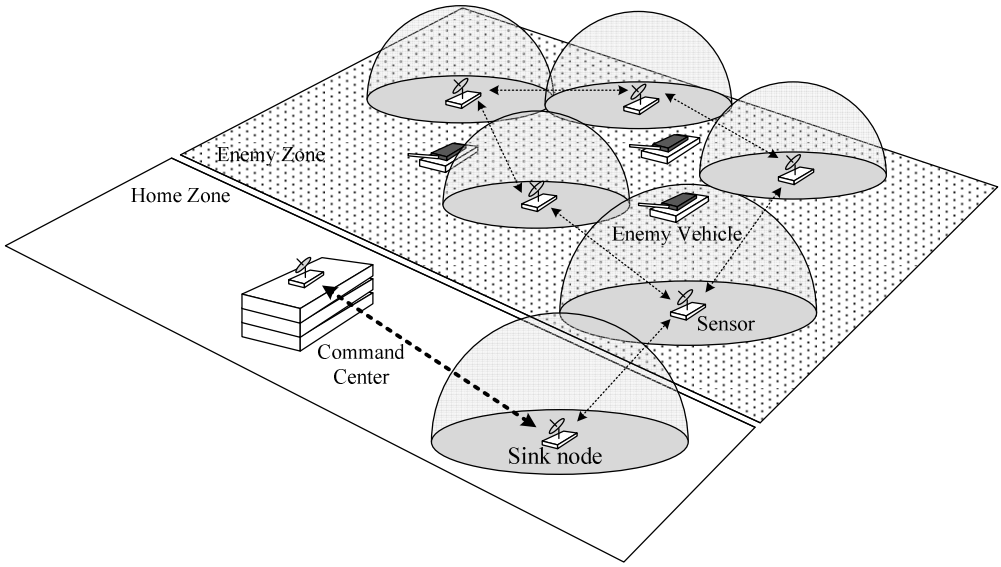


Figure 1.1. An example of the deployment of a wireless military sensor network detecting enemy vehicles in battlefields.

Different sensor types can be used to perform various roles better in each scenario. Battle-field sensors can measure electromagnetic waves, light and sound from gunfire and explosions, and also sense presence of toxic chemical and biological vapors. Detecting the presence of people or objects is of great interest in enemy-tracking, battlefield surveillance or target classification [2]. For example, a research team in University of Virginia presented an energy-efficient surveillance system using wireless sensor nodes, replacing dangerous mines with much safer thousands of motes to detect the enemy units [6]. Another demonstration showed that wireless sensor networks helped pursuers locate their enemies by multi-vehicle tracking methods, informing about the relative locations and movements of targeted vehicles so that pursuers can locate them a lot easier [7]. “A line in the sand” research conducted in Ohio State University [8] shows a similar example of tracking

vehicles and armed soldiers, from 90 nodes deployed to detect metallic objects. All of these results are meaningful because this critical information can reduce uncertainties about the opponents' position and deployment of their weapons so that it can help reduce the unintended casualties during the war with the least human power and the cost.

The challenges of military wireless sensor networks mainly come from the fact that the information should be correct and secure, even though the available power should be a lot lower on each sensor node. For data integrity, reliable correlation of information from adjacent sensor nodes is important to maximize cooperative effects from using multiple sensors. And the networks should be able to classify objects or events in addition to just detecting them, requiring data-processing in individual sensors. Gateways then will provide a higher level of data fusion, additional data processing, or reach-back capability to the command center [2]. Therefore, the power and energy assigned to these gateways should be greater than those to individual nodes, because their functionality is more important and critical from the network management's view point.

In addition, the improved integration of different types of sensors are required considering the various types of sensors needed in battle fields: for example, (1) presence / intrusion tasks using infrared, photoelectric, laser, acoustic, and vibration sensors, (2) chemical, biological, radiological, nuclear and explosive and toxic industrial material detectors, (3) ranging tasks using Radar or ultrasonic sensors, (4) imaging sensors, and (5) noise detection using acoustic sensors [2]. From a communications' perspective, a common, energy-efficient standard of data communication protocols would be economically feasible,

but again the end-to-end security should be never overlooked. And above all, to ensure that all their operations not be interrupted by power failure for a reasonable operational time is the most important, requiring reliable and compact power supplies.

1.1.2. Utility Distribution

The main role of power distribution networks is to provide uninterrupted power service without degradation in power quality, to customers whose demands may dynamically change in time [4]. The power grids today are showing gradual transitions into smart grids, which enable localized sensing of individual power demands and controlling power flow from that, eventually reaching a more efficient power-utilization level and reducing lots of costs and human labors as well. Wireless sensor networks deployed in smart grid applications can help assess the real-time electricity needs from users and therefore make the electricity distribution more efficient and fast (Fig. 1.2.)

Other than smart grids, wireless sensor networks can be also utilized in asset-monitoring applications, for example, (1) to physically monitor the status of power distribution networks to prevent cable and lattice thefts, or (2) to check conductor's temperature and placement to avoid potential hazards, or (3) to sense partial discharges and leakage currents to prevent breakdown of cable insulation [4]. In all cases, the task of monitoring and controlling power distribution networks becomes challenging, because of the huge number of assets distributed in wide geographic areas [4]. In addition, monitoring and managing power distribution need to be done in real time, to diagnose problems early and reduce person hours to locate faults, and therefore to control service outages in a timely manner.

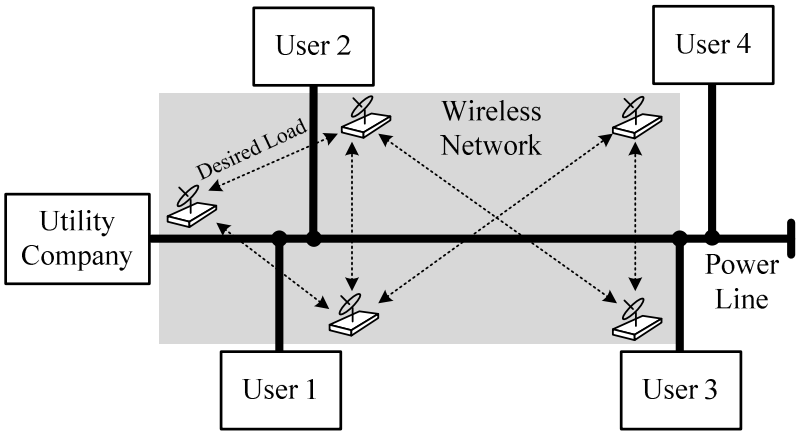


Figure 1.2. An example of the deployment of a wireless sensor network in smart meter applications.

Developing reliable sensor nodes that need low maintenance and operational cost with harsh environment conditions (i.e., high humidity levels, highly corrosive environments, dirt and dust, etc.) is one of the major challenges in this application area [4]. Network integration with a low cost, highly secure wireless communication method presents another big hurdle for this network to be profitable. The architectures and protocols should be also flexible and scalable in a modular and hierarchical way, to ensure the system's robustness and reliability. The latency and network throughput should be fast enough to ensure real-time requirements so that time-sensitive sensor data are processed and proper actions are activated in a timely manner. Considering the large number of sensor nodes, the system should be fault-tolerant so that local failures in sensor networks do not lead into failures and malfunctions in wider area.

1.1.3. Environment Monitoring

Wireless sensor networks can be utilized to monitor indoor environments and condition them more efficiently, or to prevent indoor emergency situations ahead in time. As one example, researchers at CITRIS (Center for Information Technology Research in the Interest of Society) installed 50 Smartdust motes in U.C. Berkeley to monitor light, temperature, status of frames, air streams and indoor air pollution, to ensure optimal control of the indoor environment, preventing unnecessary heating or cooling of buildings [9]. In another indoor application, motes deployed inside the walls periodically monitor the robustness of building structures in earthquake-prone areas [10]. Outdoor-environment-monitoring applications cover a wider scope, from ecology and environmental protection to disaster warnings (Fig. 1.3.) One representative example is the wireless sensor network deployed on Great Duck Island for habitat monitoring of a bird (storm petrel), consisting of 32 sensor nodes to sense temperature, pressure and humidity [11]. This application utilized a heterogeneous multi-level network to process data aggregated by sensor nodes and passed to a gateway.

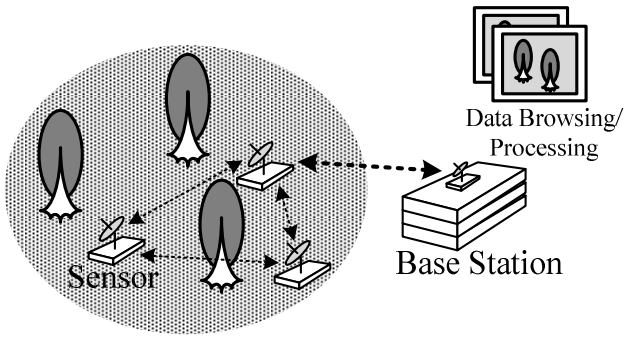


Figure 1.3. An example of the deployment of a wireless sensor network for environmental monitoring applications.

Underwater wireless sensor networks show another good example of outdoor environment monitoring. Underwater sensors can collect oceanographic data and assess water quality for preventing sea water pollution, and also can monitor seismic waves to avoid natural disasters [3]. Traditionally these sensors were deployed underwater to record data on board and collected afterwards to retrieve data. However, this off-line, open-loop method had lots of overheads with retrieving them, also making it harder to diagnose and replace failed sensor nodes quickly. To avoid these difficulties, underwater wireless sensor networks with reconfigurable and fault tolerant sensing nodes have been introduced, benefitting from similar merits that the terrestrial WSNs (Wireless sensor networks) have [3]. They suffer from different issues than the terrestrial ones, because they have to interface with the worse medium: water. For example, their architecture suffers from network problems including large propagation delays, limited link capacity (bandwidth), and greater number of packet losses, to mobility problems because of floating sensor nodes. However, most importantly, limited battery lifetime is one of the greatest concerns, because all these above-mentioned problems aggravate energy consumptions of sensor nodes, which mostly depend on the initial on-board energy they had at the time of deployment [3]. In other words, among all the challenges, the technique that extends the operational lifetime of micro sensors given a limited small volume is one of the most demanding hurdles to overcome. And before going into deeper discussions, the usage of the term “lifetime” and the definition within the context of this dissertation need to be clarified.

1.2 Lifetime

Lifetime of a wireless sensor network is one of the important metrics that define the ability and sustainability of the network, and also justify the cost of deployment [12]. There are various definitions about the lifetime of a sensor network in the literature. For example, the most common definition is based on the number of alive nodes in the network, but sometimes the number of nodes only does not tell whether the network is still functional or not. Other definitions specify the time during when the region of interest is covered by sensor nodes (sensor coverage), or the minimum time until the size of the largest connected network decrease below a certain threshold (connectivity) [12]. Regardless of how it's defined, however, the lifetime of a network heavily depends on the lifetime of a single sensor node that constitutes the network.

The lifetime of a single node also needs to be carefully defined, because this term often refers to two different notions, for example, in a battery's case. A lifetime of a battery can either mean (1) how long a mobile device can work on a single charge of a rechargeable battery, or (2) the duration of a rechargeable battery, generally specified by the number of charge/recharge cycles until its performance degrades significantly and cannot supply a useful output [13]. The former is closely related to the energy-density characteristic and also the efficiency of power generation, while the latter is related to the sustainability of a rechargeable battery. And these two characteristics do not usually correlate each other, as shown in various battery technologies in Fig. 1.4 [14].

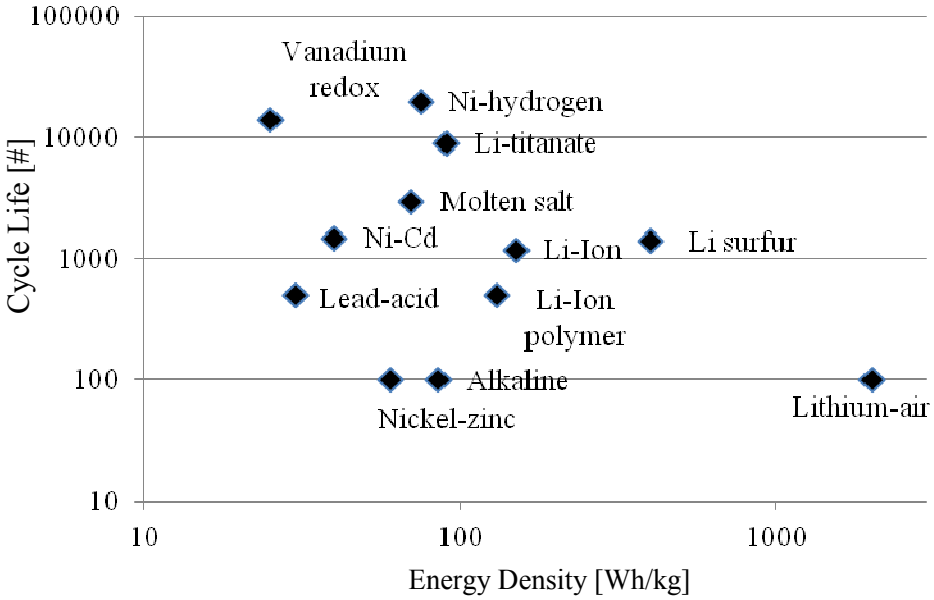


Figure 1.4. Energy density and cycle life of various battery technologies.

In this dissertation, this term will be more generally applied to energy sources including fuel cells, batteries, and capacitors, etc. The term "operational lifetime" will refer to the operational time of a sensor device powered by a finite energy source on a single charge, until it cannot sustain the output level that the device needs. The term "cycle life" will refer to the energy source's durability with multiple charge/discharge cycles, which is only applicable to rechargeable energy or power sources.

1.3 Challenges: Limited Power and Limited Energy

Wireless micro sensors usually require different power levels in performing various tasks as sensing, processing, transmitting and receiving. Fig. 1.5 illustrates the different components that constitute a typical wireless micro sensor [5]. For example, a sensing circuitry samples

the real-world information to electrical analog signals, and an analog-to-digital converter (ADC) converts them to digital signals. Then the micro processor pre-processes the raw digital data and either forward it to transmitter circuits or store in the memory. And all these powers are coming from the power/energy source, through the power-conditioning systems.

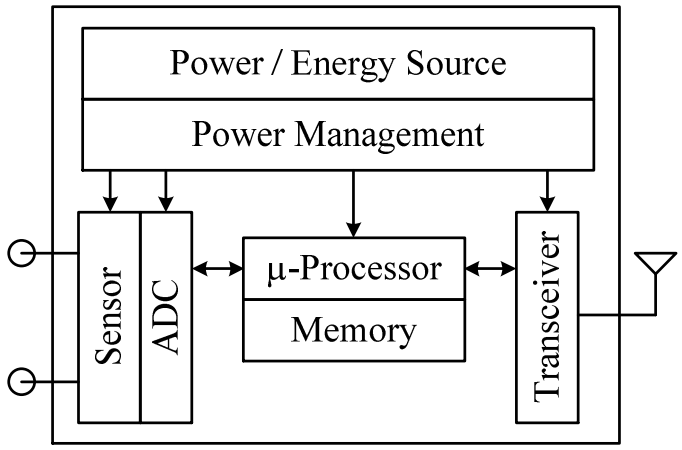


Figure 1.5. Components of a wireless micro sensor node.

One important point to notice is that the system's volume limits the power level it can supply, because the power output from power sources generally scales with their area or volume. For example, high-frequency RF (radio frequency) transmissions requiring over 50 mW's power cannot be supported by direct methanol fuel cells (DMFC), which is the most promising micro-scale fuel cell technology but can only generate about 12.5 mW's power per a square centimeter [16]. Similarly, the same fuel cell cannot be utilized in the Smart Dust project conducted by U.C. Berkeley, where a StrongARM microprocessor consumes over 100 mW's power even in its sleep mode [16]. Especially in applications where sensor

nodes' volume shrinks down to a few cubic millimeters, the power constraints on sensor functionalities will severely limit the allowed distance between RF-communicating sensors and the sensor network's coverage.

The operational lifetime is also limited by the volume of a sensor node. And replacing the energy source is not an economically feasible or even possible option in hostile or hard-to-reach environments. In most energy sources, a bigger volume means a higher energy and therefore a longer operational lifetime. Energy harvesting techniques will be the only exception from this, under the assumptions that the excitation source is steady and always there, which are not guaranteed every time in most applications [17].

Most micro sensors have an expected operational lifetime, which may vary from a few days to even several years, and this mainly determines the choice of energy sources. In Smart Dust project, to sustain a lifetime of only one day, the power consumption of an always-on sensor mote should be less than 10 μW, even when supplied from the best available battery technology fitting into the specified volume [16]. This example shows that all circuits, architectures, and network protocols on such energy-constrained nodes should be consuming the least energy possible to perform their required tasks.

1.4 Power and Energy Characteristics of Sources

Energy sources are characterized by the amount of energy and power available given a specific load [18]-[19]. The energy capability of an energy source at a specific power can be represented as a whole, unique curve in the power-energy plane, varying from source to source due to the different internal losses and leakage, as shown in Fig. 1.6. The so-called

Ragone plots [18], usually presented in a log-log scale, provide the limit in the available power and energy of an energy source given a unit volume. The dotted line, which is the ratio of the energy and power densities, thus indicates a constant time, which is increasing in the direction of the arrow. Since originated in a paper by D. V. Ragone [18] in 1968, Ragone plots have been empirically drawn for various energy storage devices. As they offer easy comparison of different energy sources of different technologies, they have been frequently used in selection of energy sources for many applications, especially in hybrid electric vehicles. The importance of the Ragone plot lies in its intuitive visualization of the operational lifetime of an energy storage device, from an energy viewpoint.

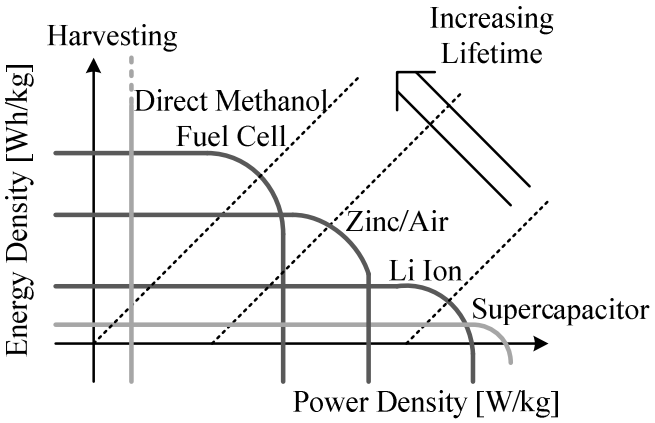


Figure 1.6. Ragone plot.

Although Ragone plots were usually drawn empirically, they can also be plotted analytically with some mathematical definitions [19]. First, a simple test system consisting of an energy source and a load is set up, and a constant power is assumed to be drained by the load (Fig. 1.7). Then, an analytic equation about the electrical dynamics of the system can be derived and solved for the load current or charge transfer. From this the operational

lifetime can be found, and the available energy from the energy source to the load is just the product of this lifetime and the constant load power. Finally, the relationship between the available energy and load power are plotted in log-log plane, and that's the Ragone plot of this energy source.

If the power losses are ignored, Ragone plot looks like a horizontal line, because all the energy from energy sources will be available regardless of the load power. In reality, however, because of the inevitable losses, the curve has usually a hooked shape (Fig. 1.6). The general shape of the curve depends on whether the energy source gives potential energy or inductive energy to the system [19]. When an energy device supplies potential energy (e.g., battery, capacitor), it can be modeled as an ideal voltage source and a series resistance (Fig. 1.7a). The available energy then becomes vanishingly small in high load power, because the power loss in series resistance increases significantly with high load current (Fig. 1.8a). On the other hand, an energy source supplying inductive energy (e.g., inductor) is modeled as an ideal current source and a parallel resistance (Fig. 1.7b). In this case the available energy decreases significantly with lower load current, since the current through the leakage resistance increases and therefore the power loss becomes significant (Fig. 1.8b).

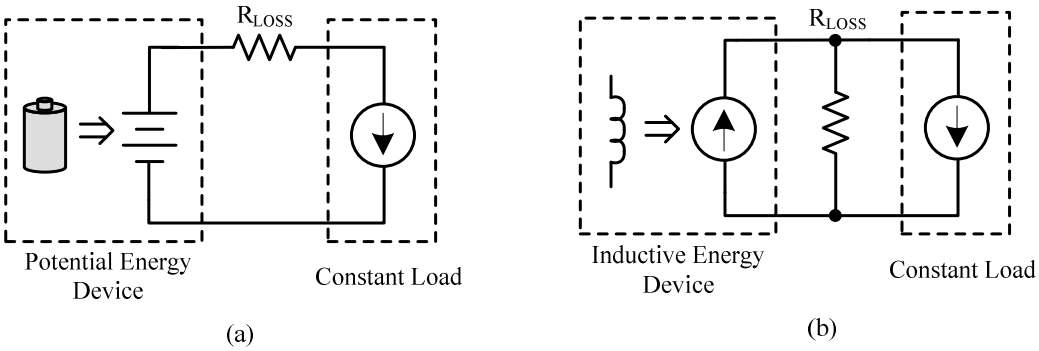
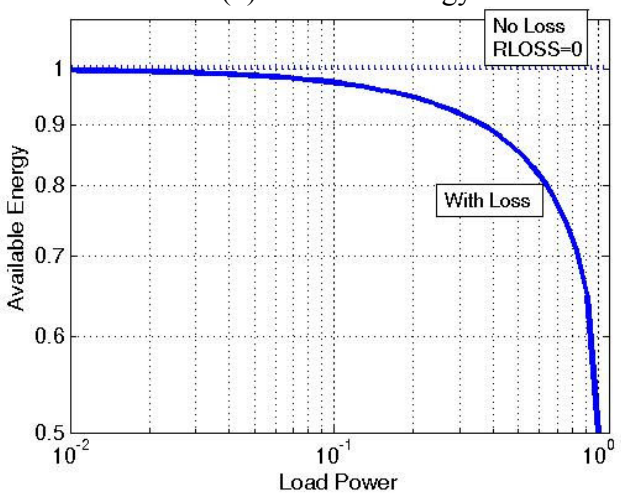
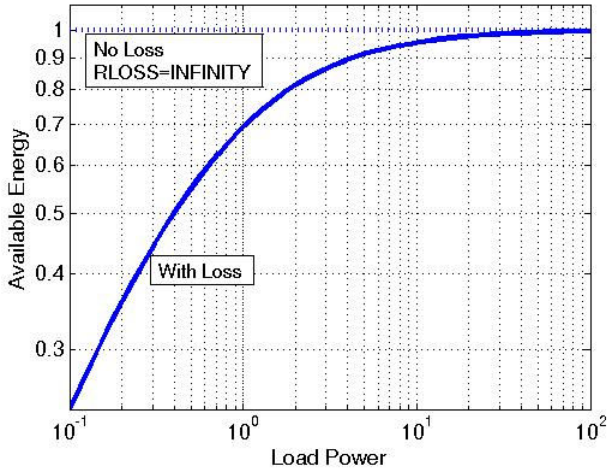


Figure 1.7. Modeling of an energy storage device for Ragone plot for (a) potential energy device and (b) inductive energy device.



(a)



(b)

Figure 1.8. Ragone plots of energy storage devices: (a) ideal battery, and (b) inductor.

As seen from Ragone plots from the various energy sources (Fig. 1.6 and 1.8), the energy and power characteristics do not correlate in general. For example, the fuel cells have higher energy densities (1000Wh/kg) than Li Ion batteries (200Wh/kg), meaning that they can last a longer operational lifetime [20]-[27]. However, the power density of fuel cells are a lot lower (10W/kg) than that of Li Ion batteries (200W/kg), making them unsuitable for supplying higher power levels. Therefore, this means that in applications where both the peak power and operational lifetime are important, two energy sources with complementary characteristics can be used together to satisfy both power and energy requirements, minimizing the sources' volume [28].

1.5 Energy-Dense Sources

1.5.1. Energy Harvesting Sources

All kinds of energy harvesting sources including light, thermal gradient, electromagnetic waves, and vibrations, etc., can be considered to have a virtually infinite energy density, assuming the presence of the energy source. The photovoltaic energy under the outdoor sunlight can generate the highest power density (0.15 – 15 mW/cm^3) among the known energy harvesting sources [29]-[30]. As the photovoltaic power is largely influenced by the solar insolation and temperature, a maximum power point tracking control should be usually accompanied for maximum efficiency. The thermoelectric generators can harvest about 15 $\mu W/cm^3$ from 10 °C's gradient, converting heat flows directly into an electrical power via the Seebeck effect [31]-[32]. Mechanical vibrations also provide a plentiful

source of kinetic energy, from which piezoelectric materials (~200 $\mu W/cm^3$) [33]-[34] or electrostatic capacitors (50 - 100 $\mu W/cm^3$) [35]-[36] can harvest. The major weakness of these ambient energy sources though is that their power levels are usually susceptible to any kind of disturbances in energy-generation mechanisms, requiring a secondary energy source or energy storage for stable power generation.

1.5.2. Direct Methanol Fuel Cell

Fuel cells (FC) are electrochemical devices that convert the chemical energy of a reaction directly into electrical energy [37]. The fuel cell technology has been widely recognized as a key energy source in a variety of application areas including power stations, transportations, and small-scale electronic systems, because of its high efficiency and environmentally-clean byproducts [38]-[40]. In a typical fuel cell, highly-reactive gaseous fuels are fed continuously to the anode, generating electrons to drive electronic loads, while an oxidant (i.e., oxygen) is fed to the cathode, where the electrochemical reduction takes place to produce an electric current. These conventional fuel cells, however, cannot be used for small-scale applications, because they usually require reformer systems and heaters to expedite chemical reactions [39].

The direct methanol fuel cell (DMFC) is considered to be the ideal fuel cell system because it operates on a liquid fuel, which can be easily stored and distributed [20]-[25]. In addition, the DMFC is inherently simpler and more attractive as portable power sources than the conventional indirect fuel cell, which relies on expensive and bulky reformer systems to convert the fuel into hydrogen gas. However, the commercialization of the

DMFC has been impeded by its poor performance compared to the H_2-based PEMFCs (proton exchange membrane fuel cells), mainly due to the slow dynamics of the anode, where efficient electro-oxidation catalysts, i.e., Pt-Ru catalysts, are needed.

Fig. 1.9 shows the operating principle of the DMFC employing a solid polymer electrolyte membrane. Methanol and water electrochemically react at the anode to produce carbon dioxide, protons, and electrons (Eq. 1-1). The protons produced at the anode migrate through the proton exchange membrane to the cathode where they react with oxygen to produce water (Eq. 1-2). The electrons produced at the anode travel through the external circuit where they can be made to run an electronic load.

$$CH_3OH + H_2O \rightarrow CO_2 + 6H^+ + 6e^- \quad \text{(anode reaction)} \quad (1\text{-}1)$$

$$3/2O_2 + 6H^+ + 6e^- \rightarrow 3H_2O \quad \text{(cathode reaction)} \quad (1\text{-}2)$$

$$CH_3OH + 3/2O_2 + H_2O \rightarrow CO_2 + 3H_2O\,CH_3OH \quad \text{(full reaction)} \quad (1\text{-}3)$$

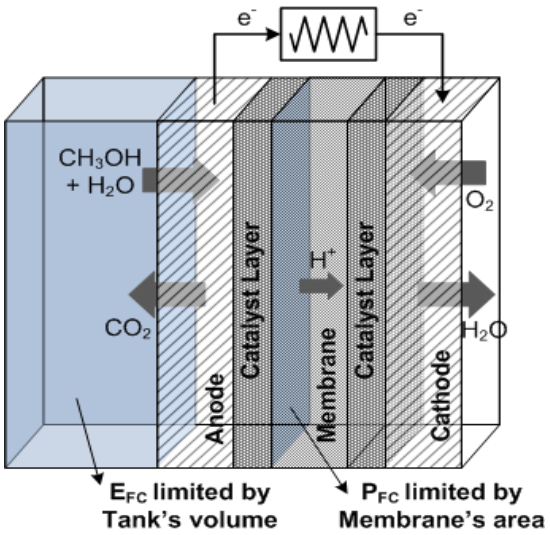


Figure 1.9. Schematic of a DMFC employing a solid polymer electrolyte membrane.

Fig. 1.10 shows a polarization curve of a typical fuel cell, showing that the fuel cell voltage gradually decreases as the current increases, due to various loss mechanisms. The voltage drop in the activation polarization, which includes open-circuit and low-current conditions, results from overcoming electronic potential barriers due to parasitic electrochemical processes and methanol crossover effects [39]. When the fuel cell current becomes higher enough to overcome internal potential barriers, it enters the Ohmic polarization region, where the voltage decreases linearly with the increasing current due to the internal resistance. Finally, when the fuel cell current increases further so that the mass transport effects such as a lack of reactant gases or a blocking of gas access happen, this results in additional voltage drops in the concentration polarization region. This current-voltage characteristic gives a maximum fuel cell's output power that can be generated from a specific fuel cell (Fig. 1.10). Therefore, the power-conditioning system can draw a maximum power from a fuel cell by properly regulating its output current or voltage to its optimal value.

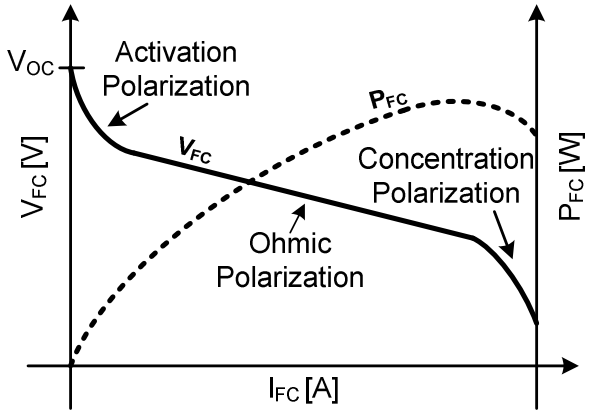


Figure 1.10. Polarization curve of a typical fuel cell.

The major challenge in the DMFC is the performance degradation due to the methanol crossover effect, a phenomenon by which the methanol diffuses through the membrane without reacting, severely impacting the fuel utilization and lowering power and energy density of the fuel cell [20]. The research towards reducing the methanol crossover focuses mainly on improving the membranes. The other important challenge is the sluggish anode dynamics, which require expensive catalysts (i.e., Pt-Ru catalyst) and high operational temperatures (i.e., 80°C). However, recent progresses in direct-methanol fuel cell researches show that they can achieve power densities ranging from 12.5 to 50 mW/cm^2 [20]-[25], making this technology more viable for portable applications.

1.5.3. Zinc/Air Cells

Zinc/air cells generate electrochemical energy from ambient oxygen [26]. Oxygen gas diffuses through the opening into the cell and works as the cathode reactant. The air goes thorough the cathode and reach at the interior cathode active surface, which is in contact with the electrolyte. Then the air starts to work as the air cathode, and promotes the reduction of oxygen in an aqueous alkaline electrolyte [26]. Since the air electrode is not consumed in the process (working as a catalyst) and the other active component zinc fills the entire cell's volume, zinc/air batteries generally have a higher energy density than those technologies where both active components should share the cell's volume [26].

In many applications, the zinc/air technology has the highest energy density of all primary battery technologies. In addition, it shows almost flat discharge voltages throughout its cycle life, and it has a long shelf life if properly sealed. Another advantage of

this technology is that its capacity is independent of load and temperature within its operating range. However, the fact that it depends on ambient air flowing through a small hole leads to some disadvantages. For example, once opened, it gradually dries out and this limits its shelf life. Designing the air hole to the minimum size might help this problem, but this creates another problem called "Flooding", where the produced gases (H_2O) blocks part of this air passage and prevents air from coming into the cell, eventually limiting its power output [26]. Fig. 1.11 shows how the service life and limiting current of a zinc/air cell are affected by maximum gas-transfer rates through the air hole. When the hole allows a lower gas-transfer rate, the service life would be longer, but the maximum current would be limited. If the hole is designed to allow a higher gas-transfer rate, it will increase a maximum power, while the service life would be shorter. In short, there is a tradeoff between the power and energy capability in designing this cell.

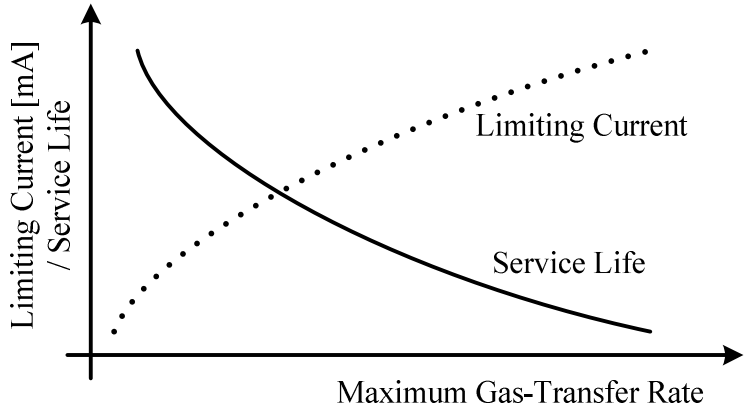


Figure 1.11. The effect of maximum gas-transfer rate in limiting current and service life of zinc/air cells [26].

The chemical reaction within the zinc/air cell is similar to that in primary alkaline systems, such as the zinc/manganese dioxide, zinc/mercuric oxide, and zinc/silver oxide batteries, where the overall discharge reaction can be described as the following expression [26]:

$$MO + Zn \rightarrow M + ZnO \tag{1-4}$$

The metal oxide (MO) is reduced to the metal or a lower oxide form during the discharge, and zinc is oxidized to ZnO in the alkaline electrolyte. In zinc/air cells, the air cathode, which acts as a reaction site, has almost infinite life because it is not consumed. The reactions of the air cathode and anode are given as the following expressions:

$$1/2O_2 + H_2O + 2e^- \rightarrow 2OH^- \text{ (cathode reaction)} \tag{1-5}$$

$$Zn \rightarrow Zn^{2+} + 2e^- \text{ (anode reaction)} \tag{1-6}$$

$$Zn^{2+} + 2OH^- \rightarrow Zn(OH)_2 \tag{1-7}$$

$$Zn(OH)_2 \rightarrow ZnO + H_2O \tag{1-8}$$

$$Zn + 1/2O_2 \rightarrow ZnO \text{ (overall reaction)} \tag{1-9}$$

Zinc/air button and coin cells come in various sizes with various power and energy characteristics. Table 1-1 shows the volume, weight, rated capacity and standard / maximum output current level of the various kinds of zinc/air cells. Their capacity ranges from 70 to 600 mAh, and their limiting currents vary from 2 to 22 mA with their respective sizes. The service life is one to three months limited by the leakage through their air hole.

The smaller sizes are generally used in hearing aid devices, while the bigger ones find their applications in pagers or telemetry devices [26].

Type	Diameter / Height (mm)	Weight (g)	Capacity (mAh)	Standard / Limiting current (mA)	Service life (months)
10	5.7 / 2.5	0.3	70	0.4 / 2	1-2
312	7.7 / 2.9	0.6	134	0.8 / 7	1-2
13	7.7 / 5.2	0.9	260	0.8 / 12	1-2
675	11.4 / 5.2	1.8	600	2 / 22	2-3

Source: Duracell, a Gillette Company

Table 1-1. Characteristics of zinc / air button and coin cells.

The output voltage and current characteristics of a zinc/air cell is determined by the degree of oxygen access to the cathode and the catalytic activity of the cathode [26]. As the higher access to air means the higher output power, the power output generally increases with the number of air access holes. Fig. 1.12 shows the voltage - current profiles of various zinc/air cells. The nominal open-circuit voltage for a zinc/air cell is 1.4 V, and the discharge voltage with the load is relatively flat, with a typical end voltage of 0.9 V. When the continuous currents exceed the limiting current, then the cell becomes oxygen-starved, consuming more oxygen than the amount entering the cell, and the output voltage rapidly decreases until the cell finds another equilibrium condition for the output current.

The zinc/air cells can supply a higher pulse load than the limiting current, because during the normal operation, a reservoir of oxygen is created within the cell when the load is lower than the limiting current [26]. If the duration of the pulse load is long so that the cell becomes oxygen-starved at the end of the pulse, the output voltage will start to fall

down. In addition, the average current of the pulse load should not exceed the rated limiting current, because it will also cause the output voltage to decline. In order to prevent this phenomenon, it is better to use this cell in parallel with a power device that can support pulse loads and absorb transient currents better, i.e., a capacitor.

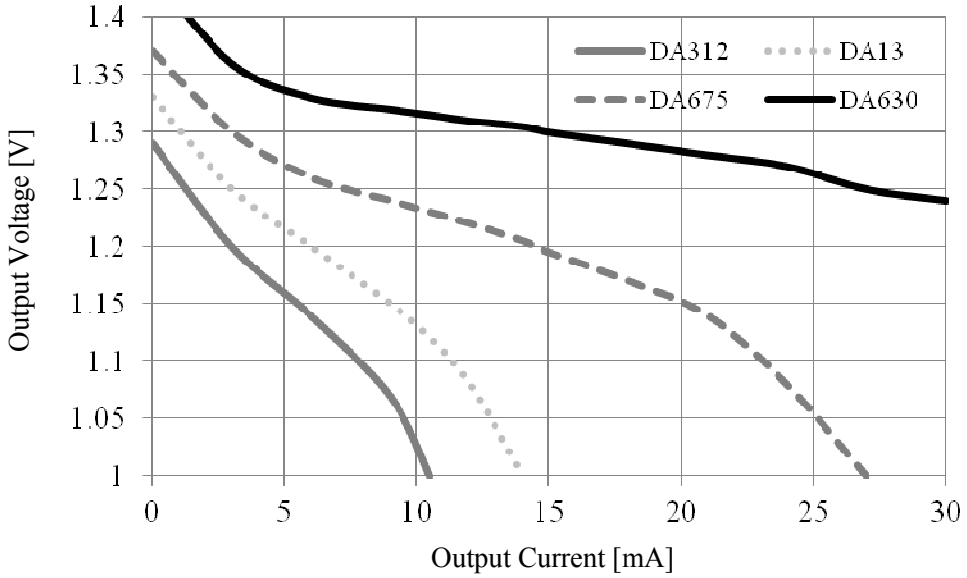


Figure 1.12. Voltage-current profiles for various zinc/air button cells [26].

1.6 Power-Dense Sources

1.6.1. Lithium Ion Batteries

A battery is a device that converts chemical energy directly into electrical energy through a reaction that transfers electrons from its anode to its cathode across an electrolyte material [26]. They are different from the fuel cells in the sense that they are energy storage devices, and the maximum energy available is determined by the amount of chemical reactant stored within the batteries. Conventional batteries such as nickel metal hydride (NiMH) and nickel

cadmium (NiCd) suffer from short cycle life and memory effects, while offering high power densities and high discharge rates. Lithium-ion batteries (Li Ion), when compared to other batteries, show superior energy and power density, discharge rate, longer cycle life, and less memory effects [26].

$$LiCoO_2 \leftrightarrow Li_{1-x}CoO_2 + xLi^+ + xe^- \quad \text{(cathode reaction)} \tag{1-10}$$

$$xLi^+ + xe^- + 6C \leftrightarrow Li_xC_6 \quad \text{(anode reaction)} \tag{1-11}$$

$$Li^+ + LiCoO_2 \leftrightarrow Li_2O + CoO \quad \text{(full reaction)} \tag{1-12}$$

A lithium-ion battery is a secondary, rechargeable battery in which lithium ions move from the negative electrode to the positive electrode during discharge, and back when charging. They are one of the most common types of rechargeable batteries for portable electronics, due to their high energy density, no memory effect, and low self-discharge rate. Their disadvantages are a relatively short shelf life and a high internal resistance due to deposits inside the electrolyte from charging operations, which diminishes the cell's capacity and reduces the cell's ability to deliver current. Also, Li-Ion batteries are not as durable as nickel-based batteries, and can be dangerous if overheated or overcharged. However, thin-film technologies make Li Ion batteries attractive by enabling the integration into power-intensive wireless micro systems, where fast and high burst power demands cannot be satisfied by only energy-dense sources such as micro fuel cells [27],[41]-[42].

Fig. 1.13 shows a typical Li Ion-battery charging scheme [43]. Li Ion-battery chargers generally extract unregulated dc power from an ac outlet or a dc power source and use it to

charge batteries with linear regulators or switching converters. To quickly and safely charge a battery, charger circuits usually start by sourcing a constant current (I_{CONST}) into the battery and end by sourcing whatever decreasing current necessary to regulate the battery's full-charge voltage. When the battery is deeply discharged below the minimum charging limit, the pre-conditioning phase starts to source a constant pre-conditioning current (I_{PRE}) to charge the battery back to the constant-current charging phase. However, this typical battery-charging scheme may not apply for the case when the system's main priority is to supply a load efficiently, rather than to charge a battery.

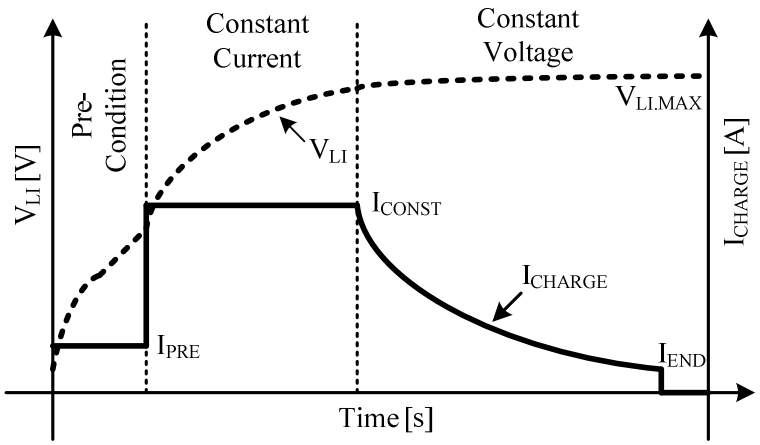


Figure 1.13. A typical Li ion-battery charging scheme.

1.6.2. Supercapacitors

Supercapacitors are electrical double layer capacitors with a large surface area of porous carbon electrodes, and a very small separation in Angstroms between positive and negative charges [44]. The capacitance increases with the surface area and the volume of the carbon

electrodes, while being inversely proportional to the separation distance between electrodes. Therefore, having highly-dense porous electrodes with a very small separation between them makes supercapacitors have a lot higher capacitance compared to normal capacitance technologies. The equivalent series resistance, which should be low to supply a very high output current, depends on the active surface area, conductivity of the electrolyte, and the porosity and thickness of the separator [44]. The mechanisms they store and release charges are completely reversible, which enables this technology undergo a huge number of charge/discharge cycles without any performance degradation [44]. They can also store and release energy very quickly over a wide temperature range.

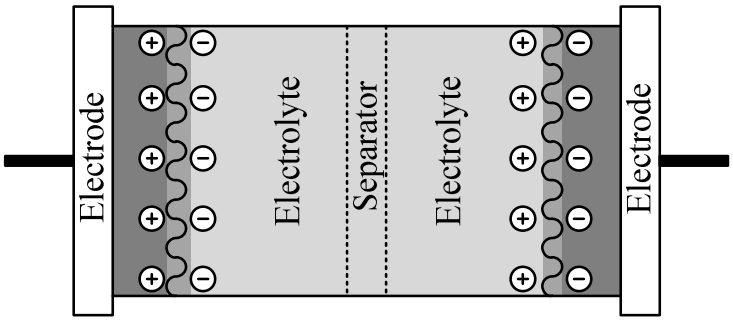


Figure 1.14. Charge storage mechanisms in a supercapacitor.

A conventional capacitor stores its energy in electrical charge, typically consisting of two conducting plates separated by a dielectric. The capacitance becomes proportional to the conductor's surface area and the dielectric constant of the dielectric, and inversely proportional to the thickness of the dielectric. The supercapacitor stores electrical charges in a similar manner, but the charge accumulates on the interface between the conductor's

surface and an electrolytic solution (Fig. 1.14, [45]). The accumulated charge forms an electric double layer, with its separation being on the order of a few Angstroms. According to the estimate of the capacitance from the double-layer model proposed by Helmholtz in 1853, the specific capacitance of a double-layer structure is given by

$$\frac{C}{A} = \frac{\varepsilon}{4\pi\delta}, \tag{1-13}$$

where C is the capacitance, A is the surface area, ε is the dielectric constant, δ is the distance between the two layers [45]. As the supercapacitor consists of two electrodes, there are two double layers present, and an ion-permeable separator blocks the electrical contact between the two electrodes, but allows ions to move through. Because of a high interface surface area made of porous carbon or carbon aerogels and a very small charge-layer separation, the supercapacitor can have a high capacity and energy density compared to conventional capacitors [45].

When compared to battery technologies, supercapacitors have superior power capabilities than batteries: power density and speed [46]. Batteries rely on redox reactions in the electrode, and therefore have a higher energy density, but their kinetics are slower. Supercapacitors, however, show a lot faster response, because they store energy in electrostatic charges at the electrode surface and the transport of ions in the aqueous solutions is rapid [46]. Unlike the batteries, no electron transfers are needed between the electrodes, and therefore can be charged and discharged quickly without damaging or altering their structures. This leads to almost infinite cycle life of supercapacitors, and there

are no restrictions in charging/discharging currents, making the charging circuits much simpler than battery technologies [46].

1.7 Hybrid Sources

The hybrid concept to utilize the complementary characteristics of energy sources is not new. In automotive applications, for example, electric vehicles using a Polymer Electrolyte Membrane Fuel Cell (PEMFC) as the main generator need to employ a battery or a supercapacitor as a secondary source, to generate or absorb a higher power in a short time and also to compensate the warm-up time of a fuel cell, because fuel cells cannot supply fast, high loads due to slow dynamics and fuel starvation phenomena [47]-[49]. Another prevalent application is Start-Stop systems [44]. In city driving where cars frequently start and stop at traffic lights or due to heavy traffics, about 15% of fuels can be saved by stopping the engine when the car is idling. And when the engine needs to start again, a supercapacitor cranks the engine instead of a car battery, because supercapacitors can supply instant, high power more efficiently and quickly than batteries, even at sub-zero temperatures [44]. These technologies have been applied to Peugot Citroen diesel cars, utilizing Continental supercapacitors for this Start-Stop system [44]. Supercapacitors can reduce the overall size of power generation systems, because they have a higher power density than batteries. As an example, they are used to boost power in HEV (hybrid electric vehicle) buses in Shanghai to boost power while improving fuel efficiency. In addition, they can be easily recharged from regenerative braking as well as charging stations at bus stops in a short period of time, unlike other battery technologies [44].

In energy-generation applications where renewable energy sources (solar, wind, etc.) provide an intermittent, time-varying power, the fuel cell or batteries are often integrated together to ensure continuous, constant power generation regardless of the main sources' conditions [50]-[52]. In [50], for example, an energy system comprising solar, wind, and fuel cells has been suggested to deliver the maximum power to a fixed DC voltage bus. Maximum power tracking methods are used for solar and wind energies to supply the load, while the excess energy is directed to fuel cells to generate hydrogen for running them. Another example shows a remote area power generation system utilizing a hybrid energy system of solar and diesel energy, to achieve economically viable and efficient energy-generation solutions in rural households in less developed countries [52]. In short, hybrid mixing technologies in renewable energy generation are vital, because of the low reliability of individual energy-generation sources.

The concept of using both an energy-dense fuel cell and power-dense batteries (or supercapacitors) becomes very attractive to small-scale portable electronic systems, because they usually require an immediate, burst delivery of power and also a long operational lifetime [53]-[55]. Especially in volume-limited standalone systems, using both an energy-dense and power-dense source can lead into an optimal volume to perform a specific power task and to meet the operational lifetime (Fig. 1.15). For example, to meet the lifetime target in Fig. 1.15, only one energy-dense source (marked as "E") will be enough, and for the power target, only one power-dense source (marked as "P") will do. However, in order to meet the power target, four energy-dense sources will be needed, if only energy-dense sources are available. Similarly, if only available sources are power-

dense sources, then four of them will be needed to meet the lifetime target. However, if both energy-dense sources and power-dense sources are available, then using each one from both sources will suffice to satisfy the power and lifetime target, requiring the least volume compared to single-source-based solutions. These hybrid-source techniques will play an important role in optimizing the system's volume especially in wireless sensor applications where spaces for energy sources are severely limited and any additional space means a room for a longer operational lifetime and also for more functionalities that a sensor can perform.

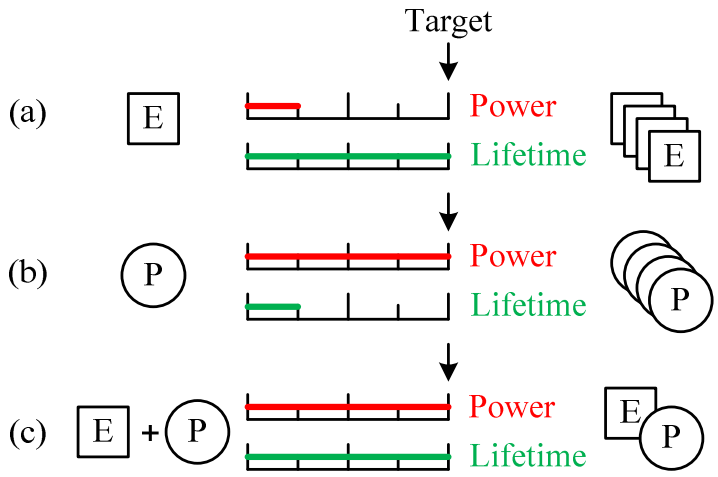


Figure 1.15. Comparison of required volumes to meet the power and operational lifetime targets using (a) only energy-dense sources, (b) only power-dense sources, and (c) a hybrid combination of energy-dense sources and power-dense sources.

1.8 Summary

Emerging micro-scale wireless sensors have vast application areas in military, utility distribution and environment monitoring applications, mostly to enhance human abilities to reach information more safely, effectively, and easily with a lot lower cost and man power.

Many challenges come from harsh environment conditions the sensors should face and the development of efficient and robust networks that the sensors should employ for information collection and processing. However, the most important premise of all these is that these sensors should be provided with uninterrupted power and energy from reliable energy sources, to be functional throughout their operational lifetime.

The amount of energy and power that each energy source can generate given a unit volume is of great importance in a portable, stand-alone system, because it will eventually determine the system's operational lifetime and feasible functionalities that the system can perform. Using an energy source with a highest energy density and power density will therefore lead into the smallest optimal solution. However, energy-dense sources such as fuel cells and zinc / air cells cannot generate as much power as power-dense counterparts can do, as clearly seen in Ragone plots of various source technologies. Similarly, power-dense sources such as lithium ion batteries and supercapacitors cannot provide high energy and long operational lifetime, while they are more optimized in generating a higher and instant power. Therefore, to satisfy a specific power and operational lifetime target of a system, using both an energy-dense source and a power-dense source can lead into a smaller optimized volume than that of single-source-based solutions. The next problem then becomes how to choose a power management system to efficiently condition power and energy between hybrid energy / power sources and the load.

Chapter 2. Power Conditioning Systems

The power conditioning system for hybrid sources should be able to interface with more than one inputs and more than one outputs, requiring a multiple-input, multiple-output topology. As the inputs and outputs may have different voltage ranges, the power conditioner should be able to generate a wide range of outputs with high efficiencies, from a wide range of inputs. The power conditioner itself should be also compact, because its own area should not invalidate the benefit of using mixed complementary sources. Therefore in this chapter, three different power conditioning systems – linear regulators, switched-capacitor circuits, and switched-inductor converters, - are compared and analyzed in terms of aforementioned requirements, to decide which is the most compact, efficient power conditioner for multiple-input, multiple-output systems.

2.1 Linear Regulators

A linear regulator is a circuit that generates a regulated output voltage (v_{OUT}) by controlling the conductance of a pass device, which connects the unregulated input voltage (v_{IN}) and the output voltage (v_{OUT}), as shown in Fig. 2.1 [56]. The output voltage is sensed by a resistor divider, and a fraction of it is fed into the negative terminal of the error amplifier, whose output controls the conductivity of the pass device to regulate v_{OUT}'s fraction to the reference voltage V_{REF}. The gain of the error amplifier affects the output's accuracy, and the compensation network determines the linear regulator's speed to respond to load variations. As the output current equals to the input current, the power efficiency becomes

the ratio between the input and output voltage. Therefore, the dropout voltage across the pass device, which is the minimum voltage drop required to maintain the output regulation within 2% in general, determines the efficiency of a linear regulator [57]-[58].

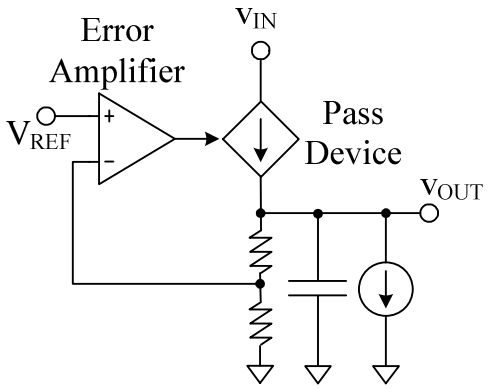


Figure 2.1. Linear regulator.

In a standard Bipolar linear regulator, the pass device is made up of an NPN Darlington driven by a PNP transistor [58]. This configuration has the high dropout voltage, which amounts to $2V_{BE}+V_{CE}$, while it has the lowest ground pin current due to its high current gain in the pass device [58]. To reduce the dropout voltage, a single transistor can be used to allow a voltage drop of V_{CE} in low-dropout (LDO) regulators, but its ground pin current to sustain a higher load increases by much. The pass device can be either NPN transistor or PNP transistor. NPN pass transistors usually are in follower types, so the output impedance is low and the bandwidth is high, making the compensation network immune to the load capacitance [57]. PNP pass transistors, on the other hand, are in inverter configurations with high output impedance, so they generally have a narrower bandwidth and are also

sensitive to the load capacitance [57]. In all cases, bipolar pass devices require a fraction of load current to drive base, which lowers efficiency when compared to CMOS devices [56].

CMOS LDO regulators do not require current to drive their pass devices, and therefore require less supply currents than their Bipolar counterparts. The gate of the pass device is mainly controlled by the error amplifier to regulate v_{OUT}. By utilizing a single CMOS transistor as a pass device, the dropout voltage can be decreased, but if the difference between v_{IN} and v_{OUT} is large, then the maximum efficiency cannot be more than the ratio of v_{IN} and v_{OUT}. This fact limits the application of LDO regulators to where the difference between input and output voltages is not big. However, the bandwidth of LDO regulators can be a lot higher than that of switching regulators, because LDO regulators do not have low-frequency poles due to LC filters in switching converters [56]. Another advantage of LDO regulators over switching regulators is that the number of off-chip components can be reduced even to zero, if their output capacitor is integrated on die. However, due to the inherent limitations in the range of acceptable input / output and efficiency, LDO regulators do not have much advantage over switching regulators in multiple input/output converters.

2.2 Switched-Capacitor Circuits

Switched-capacitor circuit is an electronic circuit that charges capacitors from available voltage sources and discharges them into the output so that it can produce an output voltage with a predetermined ratio by periodic switching operations. As switched-capacitor circuits require only capacitors and switches that can be easily integrated on silicon die, they have been frequently used in fully-integrated, low-power, DC-DC conversion applications [59].

Fig. 2.2 shows one example of switched-capacitor circuits, a voltage doubler. During phase 1, two switches marked as "1" turn on to charge the pump capacitor to the input voltage v_{IN}. During phase 2, the other two switches marked as "2" turn on to discharge the pump capacitor into the output capacitor and load, raising v_{OUT} to two times of v_{IN}.

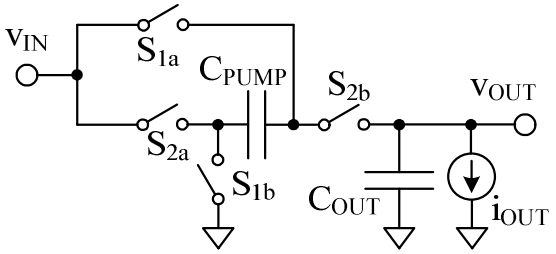


Figure 2.2. Switched capacitor voltage doubler circuit.

Switched capacitor circuits usually employ negative feedback to regulate the output voltage at the desired level. Fig. 2.3 shows a simplified model of a regulated switched capacitor circuit, which has two control loops – an inner loop and an outer loop. In the inner loop, an error amplifier senses the output voltage v_{OUT} and controls the duty cycle of the switch connecting the output of the ideal transformer to v_{OUT}. In other words, the inner loop controls the output resistance for tight regulation of v_{OUT} [59]. The outer loop generates an output voltage with a conversion ratio n:1, modeled as an ideal transformer with the same turn ratio. As practical switched-capacitor circuits cannot have a very high resolution of the turn ratio n, this ratio is usually predetermined by the topology and switching patterns, designed for the highest efficiency in specific output ranges [59].

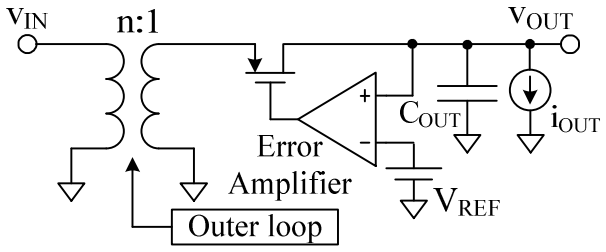


Figure 2.3. Model of a regulated switched capacitor circuit.

This fixed turn ratio affects the efficiency performance of switched capacitor circuits for a wide range of output voltage. As the turn ratio is determined by its topology and switching patterns rather than feedback-loop operations, the ratio of the output current to the input current is also pre-determined, unlike the switched-inductor converters where the level of the output current is dynamically adjusted according to the output voltage's level. Although the efficiency of a switched capacitor circuit can be high at a specific output voltage determined by the turn ratio, the efficiencies at other output voltages cannot be as high as those of a switched-inductor converter. Another drawback of a switched-capacitor circuit is a large number of switches. A simple doubler circuit in Fig. 2.2 requires four switches to generate two times of input voltage at the output, while an inductor-based boost converter only requires two switches or even one (in asynchronous control) to do the same job. The increased number of switches also affects the efficiency adversely, because conduction losses occur when constantly charging and discharging each capacitor. Especially in systems such as hybrid-sourced micro sensors where multiple inputs and multiple outputs are required, the number of switches and also capacitors should increase by a lot, worsening the power conversion efficiency and system complexity.

2.3 Switched-Inductor Converters

Switched-inductor converters use an inductor as an energy-transfer medium, and periodically apply either positive or negative voltage on the inductor to control its current and eventually the system's output voltage v_O [60]. As they use a quasi-lossless inductor as an energy-transfer medium, they can be very efficient in voltage-to-voltage conversion than linear regulators and switched capacitors allowing a wide range of output and input voltages than linear regulators and switched-capacitor circuits [60]. However, as inductor-based converters have various sources of power losses that are affected by the selection of passive components or the converter design, understanding the root mechanism and characteristics of individual losses is important in designing an efficient inductor-based converter.

Fig. 2.4a shows an example synchronous buck converter and its parasitics. Power losses in switched-inductor converters can be generally categorized into conduction, switching, and quiescent losses [61]. Conduction losses refer to the Ohmic power dissipated in the parasitic series resistances and diodes present in the power-conducting switches (e.g., switch-on resistances and diodes in M_P and M_N), inductors (e.g., $R_{L.ESR}$ in L), and capacitors (e.g., $R_{C.ESR}$ in C_O). Switching losses describe the energy needed to charge and discharge gate-drive capacitors (e.g., current i_C used to charge and discharge C_{GS} and C_{GD} in M_P and M_N), the energy lost due to the voltage-current overlaps across the switches (e.g., drain-source terminal voltages across M_P and M_N) and all other energy lost due to the switching actions of the converter. Finally, quiescent power refers to the steady-state

current the controller in the feedback loop requires (e.g., I_Q) to function and operate at the prescribed switching frequency.

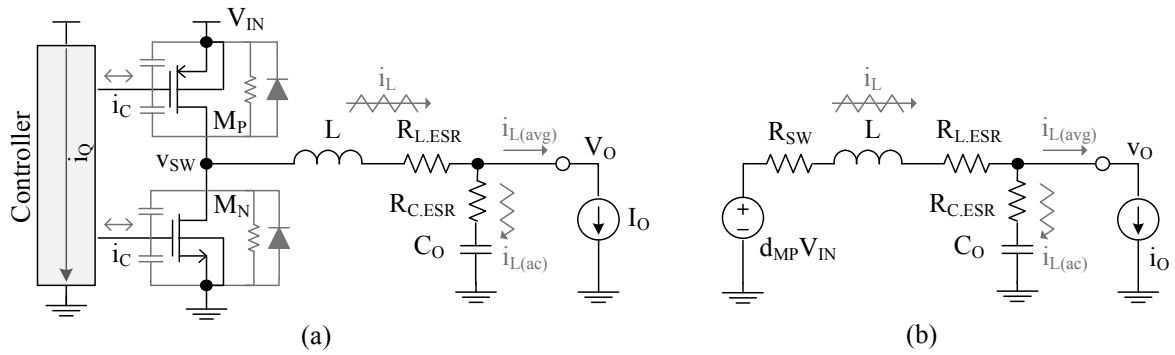


Figure 2.4. (a) A synchronous buck dc-dc converter and parasitic devices, and (b) an equivalent conduction-loss model.

2.3.1. Conduction Losses

To start, it is worth noting high- and low-side switches M_P and M_N conduct almost all of inductor current i_L in alternate phases, which means their respective duty cycles d_{MP} and d_{MN} roughly complement one another; that is, d_{MN} is approximately 1-d_{MP}. Collectively, as a result, they present a single resistance R_{SW}, as shown in Fig. 2.4b, that is equivalent to the sum of their respective turn-on resistances R_{MP} and R_{MN} multiplied by their corresponding duty cycles:

$$R_{SW} \approx R_{MP}d_{MP} + R_{MN}d_{MN} \approx R_{MP}d_{MP} + R_{MN}(1-d_{MP}) \tag{2-1}$$

Although not necessarily the case, R_{MP} is normally on the same order as R_{MN} so R_{SW}, R_{MP}, and R_{MN} are all about the same value (i.e., $R_{SW} \approx R_{MP} \approx R_{MN}$).

Decomposing inductor current i_L into its average and ac (or ripple) components $i_{L(avg)}$ and $i_{L(ac)}$ helps highlight the relative impact of the various Ohmic losses in the circuit. For instance, $i_{L(avg)}$ in the case of the buck converter shown in Fig. 2.4a and modeled in Fig. 2.4b does not flow continuously through C_O's $R_{C.ESR}$, but it does through L's $R_{L.ESR}$ and M_P and M_N's collective series resistance R_{SW}. As a result, $R_{L.ESR}$ and R_{SW} dissipate a dc conduction power $P_{C.DC}$ that is in direct proportion to $i_{L(avg)}^2$, in other words, to I_O^2:

$$P_{C.DC} = i_{L(avg)}^2 \left(R_{SW} + R_{L.ESR}\right) = I_O^2 \left(R_{SW} + R_{L.ESR}\right) \equiv I_O^2 R_{C.DC} \tag{2-2}$$

where $R_{C.DC}$ represents the converter's equivalent dc-conduction resistance.

Similarly, i_L's ripple $i_{L(ac)}$ also flows through R_{SW} and $R_{L.ESR}$, but instead of reaching the load, C_O and its parasitic $R_{C.ESR}$ steer $i_{L(ac)}$ to ground. Resistors R_{SW}, $R_{L.ESR}$, and $R_{C.ESR}$ therefore dissipate ac conduction power $P_{C.AC}$ that is in direct proportion to the square of $i_{L(ac)}$'s root-mean-square (RMS) value $i_{AC.RMS}^2$:

$$P_{C.AC} = i_{AC.RMS}^2 \left(R_{L.ESR} + R_{C.ESR} + R_{SW}\right) \equiv i_{AC.RMS}^2 R_{C.AC} \tag{2-3}$$

where $R_{C.AC}$ is the converter's equivalent ac-conduction resistance. Note that in continuous-conduction mode (CCM), i_L is triangular in shape so $i_{AC.RMS(CCM)}$ depends on i_L's peak-peak value Δi_L, which means $i_{AC.RMS(CCM)}$ is directly proportional to the voltage across the inductor when M_P conducts (i.e., V_{IN}-V_O during d_{MP}) and inversely proportional to L's impedance Ls or Lf_{SW}, where f_{SW} is the switching frequency:

$$i_{AC.RMS(CCM)} = \frac{\Delta i_L}{\sqrt{12}} = \frac{\left(V_{IN} - V_O\right) d_{MP}}{Lf_{SW}\sqrt{12}} = \frac{V_{IN}\left(1 - d_{MP}\right) d_{MP}}{Lf_{SW}\sqrt{12}} \tag{2-4}$$

and ac conduction losses in CCM $P_{C.AC(CCM)}$ is

$$P_{C.AC(CCM)} = i_{AC.RMS(CCM)}{}^2 R_{C.AC} = \frac{[V_{IN}(1-d_{MP})d_{MP}]^2}{12L^2 f_{SW}{}^2} R_{C.AC} \quad (2\text{-}5)$$

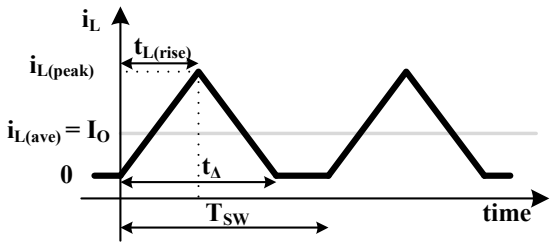


Figure 2.5. Inductor current in DCM.

When I_O drops below half ripple current Δi_L, i_L momentarily reverses direction (i.e., i_L becomes negative) and flows back to ground through R_{SW}. Allowing the converter to remain in CCM and sink this current constitutes an unnecessary power loss so, to avoid this loss, the controller normally shuts M_N off when i_L reaches zero, as shown in Fig. 2.5, allowing the converter to enter discontinuous conduction mode (DCM). Under these conditions, i_L is no longer triangular and the expression for $i_{AC.RMS}$ consequently changes. To extrapolate the mean-square fraction of ac current flowing into $R_{C.ESR}$ in DCM, the output current component is subtracted from the total mean-square inductor current $i_{L(RMS)}$, just as the load subtracts power from what is available in L:

$$i_{AC.RMS(DCM)}{}^2 = i_{L(RMS)}{}^2 - i_{L(avg)}{}^2 = \left(\frac{i_{L(peak)}{}^2}{3}\right)\left(\frac{t_\Delta}{T_{SW}}\right) - I_O{}^2 \quad (2\text{-}6)$$

where $i_{L(peak)}$ is the peak inductor current and t_Δ is M_P and M_N's combined conduction period, which is now a fraction of switching period T_{SW} in DCM. Since I_O is essentially the

dc current i_L produces, that is, $i_{L(avg)}$ is I_O, $i_{L(peak)}$ increases with I_O and decreases with conduction period t_Δ:

$$i_{L(peak)} = 2i_{L(avg)}\left(\frac{T_{SW}}{t_\Delta}\right) = \frac{2I_O T_{SW}}{t_\Delta} \quad (2\text{-}7).$$

The fraction of time M_P conducts with respect to conduction period t_Δ in DCM is the same as the fraction of time M_P conducts with respect to switching period T_{SW} in CCM, which is simply another way of referring to duty cycle d_{MP}, or equivalently, V_O/V_{IN}. This is true because L continues to be a dc short between switching node v_{SW} and v_O (i.e., $v_{SW(avg)}$ equals V_O) so M_P must therefore connect L to V_{IN} and ground at the same duty cycles it did in CCM. As a result, conduction duty-cycle d_{MP} is the ratio of conduction rise time $t_{L(rise)}$ to conduction period t_Δ:

$$t_\Delta = \frac{t_{L(rise)}}{d_{MP}} = \frac{i_{L(peak)}L}{d_{MP}(V_{IN} - V_{OUT})} = \frac{\left(\frac{2I_O T_{SW}}{t_\Delta}\right)L}{d_{MP}(V_{IN} - V_{OUT})} = \sqrt{\frac{2I_O T_{SW} L}{d_{MP}(1 - d_{MP})V_{IN}}} \quad (2\text{-}8)$$

Substituting $i_{L(peak)}$ and t_Δ in $R_{C.ESR}$'s extrapolated RMS current $i_{AC.RMS(DCM)}$ for the above-derived equations yields:

$$i_{AC.RMS(DCM)}{}^2 = \left(\frac{i_{L(peak)}{}^2}{3}\right)\left(\frac{t_\Delta}{T_{SW}}\right) - I_O{}^2 = \frac{4}{3}I_O{}^{1.5}\sqrt{\frac{d_{MP}(1 - d_{MP})V_{IN}}{2Lf_{SW}}} - I_O{}^2 = \frac{4}{3}I_O{}^{1.5}\sqrt{I_{OB}} - I_O{}^2 \quad (2\text{-}9)$$

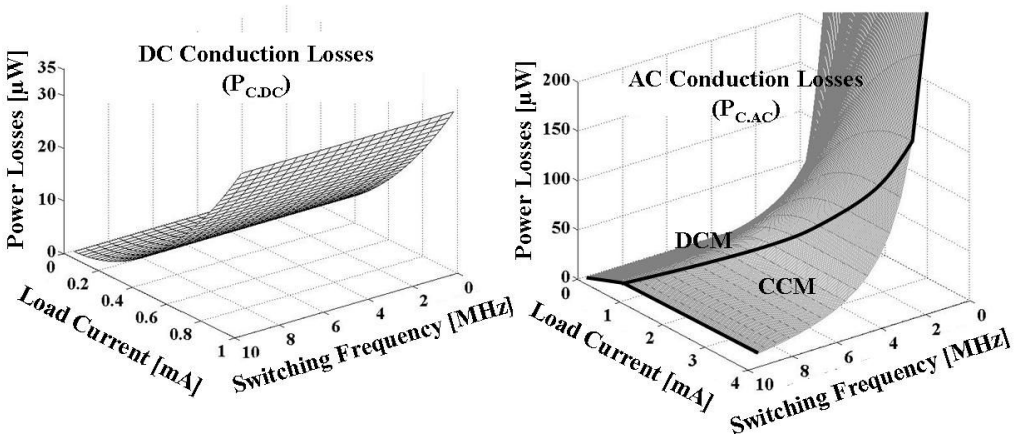
where I_{OB} represents I_O's value at the boundary of CCM and DCM operation (i.e., I_{OB} equals $0.5\Delta i_{L(CCM)}$) and ac conduction losses in CCM $P_{C.AC(CCM)}$ reduce to

$$P_{C.AC(DCM)} = i_{AC.RMS(DCM)}{}^2 R_{C.AC} = \left[\frac{4}{3}I_O{}^{1.5}\sqrt{\frac{d_{MP}(1 - d_{MP})V_{IN}}{2Lf_{SW}}} - I_O{}^2\right]R_{C.AC}. \quad (2\text{-}10)$$

Under deep DCM conditions, when I_O is substantially below I_{OB}, the I_O^2 component in $i_{AC.RMS(DCM)}$ becomes negligibly smaller with respect to its counterpart, reducing $i_{AC.RMS(DCM)}$ and $P_{C.AC(DCM)}$'s dependence on I_O and f_{SW} to $I_O^{1.5}/f_{SW}^{0.5}$:

$$P_{C.AC(DCM)}\Big|_{I_O<<I_{OB}\equiv 0.5\Delta_{\cdot L}} = i_{AC.RMS(DEEP\ DCM)}{}^2 R_{AC} \cong \left(\frac{4}{3} I_O{}^{1.5}\sqrt{I_{OB}}\right) R_{AC} \propto \frac{I_O{}^{1.5}}{f_{SW}{}^{0.5}} \qquad (2\text{-}11)$$

What is perhaps most important about this conclusion is that ac conduction losses in DCM depend on $I_O^{1.5}$ and $f_{SW}^{0.5}$, whereas in CCM, they depend on f_{SW}^2 alone. Fig. 2.6 summarizes the DC conduction losses and AC conduction losses across load currents and switching frequencies.



(a) (b)

Figure 2.6. (a) DC conduction losses and (b) AC conduction losses across load currents and switching frequencies.

2.3.2. Switching Losses

Switching power losses are all the losses attached to M_P and M_N's parasitic capacitors and diodes. The fact the converter incurs these losses every switching event, as capacitors

charge and discharge and diodes temporarily conduct, is critical because their negative impact on efficiency increases with switching frequency f_{SW}. The eddy currents and core saturation in the inductor, as it turns out, also induce power losses every switching cycle, except they are negligibly small when compared against capacitor-derived losses. Similarly, skin effects, which are pronounced in conductors with multi-layer windings at high frequency under high currents, are normally insignificant at micro-Watt levels [60].

2.3.2.1. Gate-Drive Losses

The fundamental loss in the gate capacitors is the energy required to charge them through a resistive switch: capacitor energy E_C is $C_{PAR}\Delta V_C^2$, where ΔV_C is the voltage variation in parasitic capacitor C_{PAR}. Gate-source capacitors C_{GSN} and C_{GSP} in M_N and M_P, for instance, require energy E_{GSN} and E_{GSP} to charge from zero to supply V_{IN} (i.e., $\Delta V_{GS} \approx V_{IN}$):

$$E_{GS} = E_{GSN} + E_{GSP} = C_{GSN}\Delta V_{GS}^{\ 2} + C_{GSP}\Delta V_{GS}^{\ 2} \approx (C_{GSN} + C_{GSP})V_{IN}^{\ 2} \qquad (2\text{-}12)$$

Likewise, M_P's gate-drain capacitor C_{GDP} requires energy E_{GDP} to charge from $-V_{IN}$ (when M_N is off, M_P is on, and switching node v_{SW} is at V_{IN}) to $V_{IN}+V_{DN}$ (after M_P shuts off and M_N's diode pulls v_{SW} to a diode voltage below ground V_{DN} -during dead time-); in other words, ΔV_{GDP} is approximately $2V_{IN} + V_{DN}$. After dead time, M_N's gate-drain capacitor C_{GDN} charges from V_D (before M_N conducts) to V_{IN} (when M_N is fully engaged); that is, ΔV_{GDN} is roughly $V_{IN} - V_D$ and total gate-drain energy E_{GD} is

$$E_{GD} = E_{GDP} + E_{GDN} = C_{GDP}\Delta V_{GDP}^{\ 2} + C_{GDN}\Delta V_{GDN}^{\ 2} \approx C_{GDP}(2V_{IN} + V_D)^2 + C_{GDN}(V_{IN} - V_D)^2$$

$$\approx (C_{GDN} + 4C_{GDP})V_{IN}^{\ 2} \qquad (2\text{-}13)$$

assuming V_D is considerably below V_{IN}. The average gate-drive power losses that result therefore reduce to

$$P_{SW.GD} = (E_{GS} + E_{GD}) f_{SW} \approx \left[(C_{GSN} + C_{GSP}) V_{IN}^{\ 2} + (C_{GDN} + 4C_{GDP}) V_{IN}^{\ 2} \right] f_{SW} = C_{GEQ} V_{IN}^{\ 2} f_{SW} \quad (2\text{-}14)$$

where C_{GEQ} is the equivalent switching capacitance present at the gates of M_N and M_P, the total value of which depends on the size of M_N and M_P.

2.3.2.2. IV-Overlap Losses

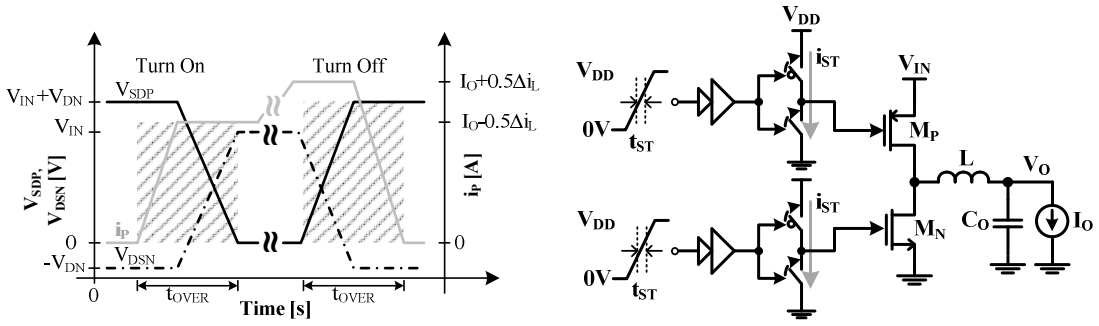


Figure 2.7. IV overlap power losses in MP and MN and shoot-through losses in MP and MN's driver chains.

As gate capacitors charge and discharge, while M_N or M_P conducts inductor current i_L, the conducting switch is temporarily exposed to a transitioning non-zero drain-source voltage v_{SW}, the current-voltage overlap of which induces an $i_L v_{SW}$ power loss across the conducting switch. In CCM, just before M_P turns on, for example, M_N's body diode conducts i_L's negative peak I_O-0.5Δi_L, switching node v_{SW} is below ground by a diode voltage V_{DN}, and M_P's source-drain voltage v_{SDP} is high, as illustrated at time equal zero in Fig. 2.7a, and as M_P engages, M_P's current i_P rises to i_L all the while v_{SDP} is high at $V_{IN}+V_{DN}$ – the overlap area constitutes part of M_P's IV power loss $P_{IVP(CCM)}$. A similar

event occurs when M_P disengages, as v_{SW} decreases and i_P decreases, which is why $P_{IVP(CCM)}$ reduces to

$$P_{IVP(CCM)} = (V_{IN} + V_{DN})t_{OVER} I_O f_{SW} \tag{2-15}$$

where t_{OVER} is the IV overlap time. Although the model used and Fig. 2.7 neglect the clamping effects parasitic bond-wire inductances induce, their influence is minimal when using multiple bond wires, as is typical in practice, with little to no performance trade-offs.

Power switch M_N also undergoes similar IV losses during CCM, except its drain-source voltage v_{DSN} is only exposed to diode voltage V_{DN} because dead time forces its body diode to conduct i_L and pull v_{SW} to $-V_{DN}$ when M_N and M_P are both off, just before M_N is engaged and allowed to pull v_{SW} from $-V_{DN}$ to zero:

$$P_{IVP(CCM)} = (V_{IN} + V_{DN})t_{OVER} I_O f_{SW} \tag{2-16}$$

which means CCM IV losses combine to

$$P_{SW.IV(CCM)} = P_{IVP(CCM)} + P_{IVN(CCM)} \approx (V_{IN} + 2V_{DN})t_{OVER} I_O f_{SW}. \tag{2-17}$$

In DCM, switching conditions are softer because i_L is zero just after M_N disengages and immediately before M_P engages, allowing M_N's v_{DSN} and M_P's v_{SDP} to transition with little-to-no current during M_N's turn-off and M_P's turn-on transitions, which means $P_{IVP(DCM)}$ and $P_{IVN(DCM)}$ reduce to

$$P_{IVP(DCM)} = 0.5(V_{IN} + V_{DN})i_{L(peak)} t_{OVER} f_{SW} = 0.5(V_{IN} + V_{DN})\left(\frac{2I_O T_{SW}}{t_\Delta}\right)t_{OVER} f_{SW}$$

$$= t_{OVER}\left(V_{IN} + V_{DN}\right)\sqrt{\frac{d_{MP}\left(1-d_{MP}\right)V_{IN}}{2L}} \cdot \sqrt{I_O f_{SW}} \tag{2-18}$$

$$P_{IVN(DCM)} = 0.5 V_{DN} i_{L(peak)} t_{OVER} f_{SW} = t_{OVER} V_{DN} \sqrt{\frac{d_{MP}\left(1-d_{MP}\right)V_{IN}}{2L}} \cdot \sqrt{I_O f_{SW}}, \tag{2-19}$$

$$P_{SW.IV(DCM)} = P_{IVP(DCM)} + P_{IVN(DCM)} \approx t_{OVER}\left(V_{IN} + 2V_{DN}\right)\sqrt{\frac{d_{MP}\left(1-d_{MP}\right)V_{IN}}{2L}} \cdot \sqrt{I_O f_{SW}} \tag{2-20}$$

where $i_{L(peak)}$ is the peak inductor current in DCM.

2.3.2.3. Dead-Time Losses

During dead-time, when switches M_N and M_P are both off, because the inductor has energy and continues to demand current to flow to the output, M_N's parasitic diode forward biases and conducts i_L, pulling v_{SW} below ground by a diode voltage (V_{DN}). The diode therefore incurs a conduction loss during this time interval that is proportional to the product of V_{DN} and i_L. In CCM, for instance, i_L is at either its positive ($i_{L(+peak)}$ is I_O+0.5ΔI_L) or negative peak ($i_{L(-peak)}$ is I_O-0.5ΔI_L) during its transitions, giving an overall average value of I_O. The dead-time losses ($P_{SW.DT}$) in CCM are therefore proportional to V_{DN} and I_O, given $i_{L(+peak)}$ exceeds I_O by the same amount $i_{L(-peak)}$ falls below I_O:

$$P_{SW.DT(CCM)} = V_{DN}\left(i_{L(+peak)} + i_{L(-peak)}\right)\left(\frac{t_{DT}}{T_{SW}}\right) = 2V_{DN} t_{DT} I_O f_{SW}. \tag{2-21}$$

In DCM, however, dead-time conduction effectively occurs only when i_L is at its positive peak because its negative-peak counterpart is essentially zero, which means the negative

peak experiences softer switching conditions. As a result, the expression for dead-time losses in DCM is similar in form to $P_{SW.DT(CCM)}$, but its dependence on I_O is less pronounced:

$$P_{SW.DT(DCM)} = V_{DN} i_{L(peak)} t_{DT} f_{SW} = V_{DN} t_{DT} \sqrt{\frac{2d_{MP}(1-d_{MP})V_{IN}}{L}} \sqrt{I_O f_{SW}} \qquad (2\text{-}22)$$

2.3.2.4. Driver Shoot-Through Losses

The drivers, because they do not normally incorporate dead-time features, incur shoot-through power losses when their respective supply and ground switches momentarily conduct shoot-through current i_{ST} at the same time. These Ohmic power losses are directly proportional to the square of V_{IN}, inversely proportional to combined switch-on resistances $R_{SW.DST}$, and the fraction of time they both conduct with respect to switching period T_{SW} or $1/f_{SW}$ (i.e., ratio of shoot-through time t_{DST} and switching period T_{SW}). Considering the size of each inverter in the driver chain is normally tapered, the inverter that drives the power switches, that is, the last inverter in the chain, incurs the most shoot-through losses:

$$P_{SW.DST} = \frac{2V_{IN}^{\ 2} t_{DST} f_{SW}}{R_{SW.DST}} \qquad (2\text{-}23)$$

Fig. 2.8 summarizes the trends of all switching losses with respect to load currents and switching frequencies.

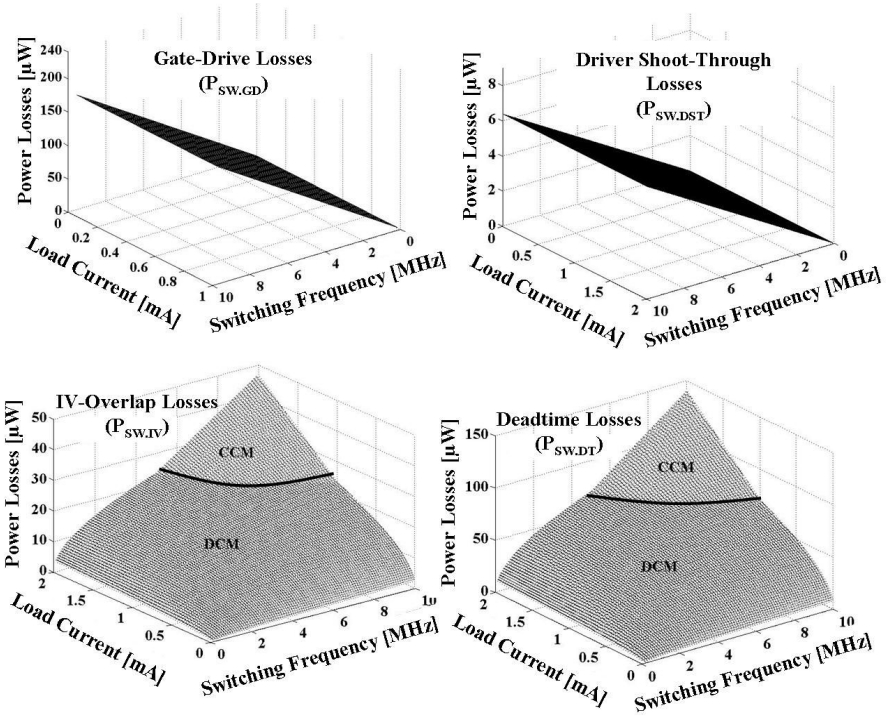


Figure 2.8. Switching losses across load currents and switching frequencies.

2.3.3. Quiescent Losses

Feedback control, protection, and other vital functions require quiescent current to operate, and because input voltage V_{IN} normally supplies this current, the controller dissipates a quiescent power P_Q that is proportional to input supply V_{IN} and quiescent current I_Q:

$$P_Q = V_{IN} I_Q = E_Q f_{SW} + V_{IN} I_{Q0} \approx E_Q f_{SW} \tag{2-24}$$

where E_Q refers to the quiescent energy required in each switching cycle and I_{Q0} to the frequency-independent quiescent current. As it turns out, quiescent power losses usually become strong functions of switching frequency because higher speeds demand more quiescent current. The fact is dominant and parasitic poles in the control loop shift to higher

frequencies when I_Q increases because the effective resistance at each node in the circuit decreases with quiescent current (e.g., small-signal output resistance r_o or $1/\lambda I_Q$ in MOSFETs and V_A/I_Q in BJTs). In other words, higher bandwidth f_{BW} demands f_{SW} and lower parasitic resistance r_o, which means higher quiescent current I_Q and power P_Q (as shown in Fig. 2.9):

$$P_Q \propto I_Q \propto \frac{1}{r_O} \propto f_{BW} \propto f_{SW}. \tag{2-25}$$

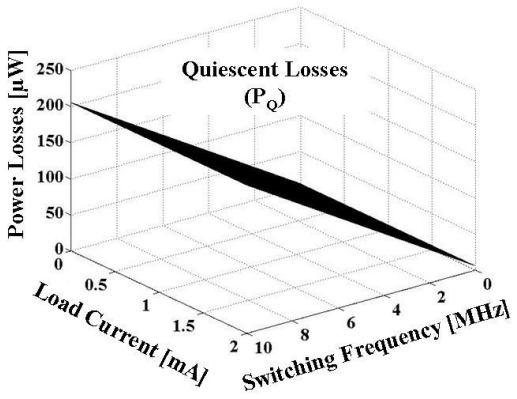


Figure 2.9. Quiescent losses across load currents and switching frequencies.

2.4 Power Losses across Process Nodes

2.4.1. Process Parameters

As the individual power losses are strong functions of various process parameters, understanding the trends of power losses with varying process parameters helps in determining which process to use to achieve a higher converter's efficiency. The driving motivation behind scaling semiconductor technologies is increasing the number of transistors that can fit in one silicon chip. Minimum channel length L_{MIN} is therefore an

important measure of integration. Reducing L_{MIN}, however, requires other modifications in the process. Oxide thickness T_{OX}, for example, decreases [62], which means oxide capacitance per unit area C_{OX}" and transconductance parameter K' increase. Electric fields also intensify as a result of reductions in T_{OX}, so gate- and drain-source breakdown voltages $|V_{GS(MAX)}|$ and $|V_{DS(MAX)}|$ drop, and therefore, so does supply voltage V_{DD} [63]. The 0.18-, 0.35-, and 0.5-µm CMOS nodes in Table 2.1 show these trends.

L_{MIN}	0.18 µm	0.35 µm	0.5 µm
	N/P-MOS	N/P-MOS	N/P-MOS
$\|V_{GS(MAX)}\|$ and $\|V_{DS(MAX)}\|$	1.8 V	2.3 V	4.5 V
$\|V_{TH}\|$	0.65/0.58 V	0.5/0.6 V	0.86/0.8 V
C_{OX}"	7.7 fF/µm^2	4.5 fF/µm^2	2.3 fF/µm^2
T_{OX}	45 Å	74 Å	151 Å
K'	135/35 µA/V^2	89/33 µA/V^2	47/12.5 µA/V^2

Table 2-1. Process parameters across process nodes.

Process engineers typically offset reductions in gate drive, which result from lower $|V_{GS(MAX)}|$ values, with lower threshold voltages ($|V_{TH}|$). An implant step in the fabrication process adjusts V_{TH} for this purpose [64]. The objective is to keep gate-drive voltages (i.e., $V_{GS} - V_{TH}$) as high as possible. Unfortunately, reducing V_{TH} increases leakage currents and decreases noise margins in digital gates [65]. As a result, V_{TH} does not fall linearly with L_{MIN}.

2.4.2. Switch Power Losses with Process Technologies

Conduction: As already mentioned, the equivalent resistances of the power switches in a switching converter therefore consume conduction power P_C when engaged. As such, the power that their combined equivalent resistance R_{EQ} dissipates increases quadratically with i_L's root-mean-squared value $i_{L(RMS)}$:

$$P_C = R_{EQ} i_{L(RMS)}^{\ 2} \propto \frac{L_{MIN}}{W_{EQ}}. \tag{2-26}$$

Since conducting switches only drop millivolts, MOSFETs operate in triode. As such, their resistances increase linearly with minimum channel length L_{MIN} and decrease linearly with maximum gate-drive $|V_{GS(MAX)}| - |V_{TH}|$:

$$R_{EQ} \approx \frac{L_{MIN}}{\mu_M C_{OX}'' W_{EQ}\left(\left|V_{GS(MAX)}\right| - \left|V_{TH}\right|\right)}$$

$$= \frac{L_{MIN}}{\mu_M C_{OX}'' W_{EQ}\left(V_{DD} - \left|V_{TH}\right|\right)} \propto \frac{L_{MIN}}{W_{EQ}}, \tag{2-27}$$

where μ_M is charge-carrier mobility and W_{EQ} the equivalent channel width of the MOSFET. In a buck converter, for example, M_P and M_N's equivalent resistances R_{MP} and R_{MN} combine in R_{EQ} to conduct L_O's $i_{L(RMS).CCM}$ in CCM and $i_{L(RMS).DCM}$ in DCM [61]

Drive: Although capacitors do not dissipate power, the switches that charge and discharge them do. In fact, V_{DD} loses all the charge it supplies to drive gates to V_{DD}, as set by $|V_{GS(MAX)}|$. In other words, when combining gate capacitors into an equivalent

capacitance C_{EQ}, V_{DD} supplies $C_{EQ}V_{DD}$ across each switching period T_{SW} to lose drive power P_D:

$$P_D = \left(\frac{C_{EQ}V_{DD}}{T_{SW}}\right)V_{DD} = \left(C_{OX}"W_{EQ}L_{MIN}\right)V_{DD}{}^2 f_{SW} \propto W_{EQ}L_{MIN}{}^2. \quad (2\text{-}28)$$

Because C_{OX}" drops with L_{MIN} and V_{DD} rises, C_{OX}" offsets L_{MIN} but not $V_{DD}{}^2$, so P_D increases quadratically with L_{MIN}.

2.4.3. Quiescent Power

The circuit blocks in the controller require current to operate, so they too dissipate power. When heavily loaded, a converter typically operates in CCM and switches at a moderately high f_{SW}. So, in CCM, most, if not all, circuit blocks function and consume power continuously across T_{SW}. Under light loads, however, the supply can save power by operating in DCM and switching at a lower f_{SW}. Still more, T_{SW} in microwatt applications can be long enough to allow system components to momentarily disengage, so as to save additional power.

Irrespective of the mode and f_{SW} of the converter and the duty cycle of its components, circuits in the feedback loop require sufficient quiescent current $I_{Q(BW)}$ to process information within one T_{SW}. Generally, the quiescent power $P_{Q(BW)}$ that bandwidth-critical circuits consume reduces to

$$P_{Q(BW)} = K_{DC}I_{Q(BW)}V_{DD} \propto L_{MIN}{}^3, \quad (2\text{-}29)$$

where K_{DC} is a correction fraction that accounts for duty-cycled elements in the feedback loop. Because the unity-gain frequency of the loop f_{0dB} is ultimately proportional to transistor transconductances g_m over parasitic capacitors C_{PAR}:

$$f_{0dB} \propto \frac{g_m}{C_{PAR}} \propto \frac{\sqrt{I_{Q(BW)}}}{C_{PAR}}, \tag{2-30}$$

$I_{Q(BW)}$ should be proportional to C_{PAR}^2 (and as a result, to L_{MIN}^2), to maintain the same f_{0dB}. That means $P_{Q(BW)}$ increases with L_{MIN}^2.

Converters also include another class of circuits that need not process information within one T_{SW}, like the bias-current generator, protection circuitry, and monitoring blocks. These subsystems require sufficient bias current $I_{Q(B)}$ to remain operational in the presence of substrate and supply noise. For these circuits, their quiescent power $P_{Q(B)}$ is

$$P_{Q(B)} = K_{DC} I_{Q(B)} V_{DD} \propto L_{MIN}, \tag{2-31}$$

which roughly increases with V_{DD}, and therefore, with L_{MIN}.

2.4.4. Other Losses

Like the power switches, L_O's and C_O's parasitic resistances $R_{L.ESR}$ and $R_{C.ESR}$ also conduct part or all of $i_{L(RMS).CCM}$ and $i_{L(RMS).DCM}$. These resistances and currents, however, do not change with L_{MIN}. As a result, their corresponding conduction losses are independent of L_{MIN}.

Because power switches can conduct substantial current, converters normally introduce a dead time T_{DT} between the conduction times of adjacent power transistors. i_L cannot drop to zero instantaneously, however, so diodes in the circuit engage during T_{DT} to conduct i_L. As a result, these diodes dissipate dead-time power P_{DT} across T_{DT} of every T_{SW}:

$$P_{DT} = V_D i_{L(DT)} \left(\frac{T_{DT}}{T_{SW}} \right) = V_D i_{L(DT)} T_{DT} f_{SW}, \tag{2-32}$$

where V_D is the diode voltage and $i_{L(DT)}$ L_O's current during T_{DT}, which is practically a constant across T_{DT} because T_{DT} is a small fraction of T_{SW} − $i_{L(DT)}$ is roughly $2i_{L(AVG)}$ in CCM and $i_{L(PK)}$ in DCM [61]. Note none of these terms relate to L_{MIN}.

The switch that engages after T_{DT} conducts slightly more than i_L to lower the voltage across its terminals from V_D + V_{DD} to millivolts. During this transition, the transistor's current i_D and drain-source voltage v_{DS} overlap (T_{IV}) and therefore dissipate power P_{IV}:

$$P_{IV} = (V_{IN} + V_D) i_{IV} \left(\frac{T_{IV}}{T_{SW}} \right) = (V_{IN} + V_D) i_{IV} T_{IV} f_{SW}, \tag{2-33}$$

where i_{IV} is practically constant across T_{IV} because T_{IV} is a small fraction of T_{SW} and equal to $i_{L(AVG)}$ in CCM and $0.5i_{L(PK)}$ in DCM [61]. Again, none of these terms are functions of L_{MIN}.

2.4.5. Minimizing Losses

Comparing efficiency across process nodes is only valid after optimizing the design for minimum losses. Off-chip losses, however, such as in L_O's $R_{L.ESR}$ and C_O's $R_{C.ESR}$, do not

vary with process. Although diodes can be on chip, diode voltages change little with process. As such, dead-time losses P_{DT} are similarly independent to process. Because overlap time T_{IV} depends on how fast transistors drive parasitic capacitances, overlap power P_{IV} changes with W_{EQ} (design). Still, when compared to other switch losses, P_{IV} and P_{DT} are usually insignificant. So, only switch and quiescent losses remain.

Switch: Because both conduction and drive power P_C and P_D generally rise with channel length, L_{MIN} is the optimum channel length for all switches in the power stage. However, while P_C falls with channel width W_{EQ}, P_D increases. As such, combined losses are lowest when P_C equals P_D [61], which results at an optimum width W_{OPT}. Equating the sum of P_C and P_D's respective derivatives with respect to W_{EQ} to zero in CCM and DCM and solving for W_{EQ} reveals that

$$W_{OPT.CCM} = \frac{i_{L(RMS).CCM}}{V_{DD}\sqrt{\mu_M C_{OX}{}'' f_{SW}\left(V_{DD} - |V_{TH}|\right)}} \propto \frac{1}{\sqrt{L_{MIN}}} \tag{2-34}$$

and

$$W_{OPT.DCM} = \frac{i_{L(RMS).DCM}}{V_{DD}\sqrt{\mu_M C_{OX}{}'' \left(V_{DD} - |V_{TH}|\right)}} \propto \frac{1}{\sqrt{L_{MIN}}}. \tag{2-35}$$

which the analytical results in Fig. 2.11 of the buck converter in Fig. 2.10 corroborate. Note that, since V_{DD} rises with L_{MIN} and C_{OX}" falls, W_{OPT} drops with the square root of L_{MIN}.

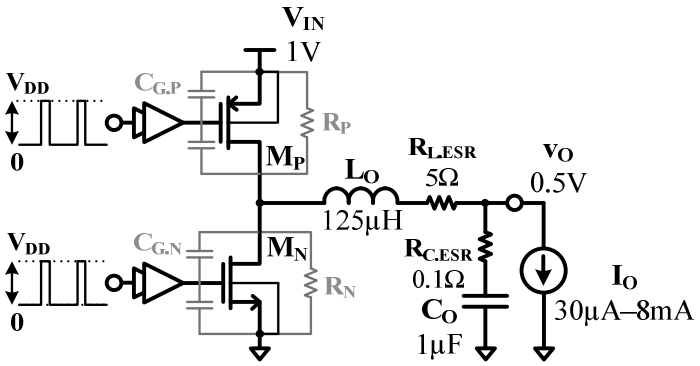
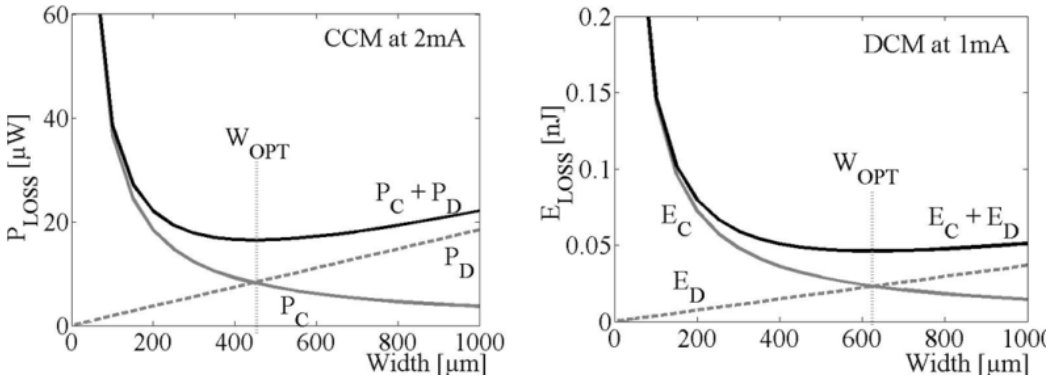


Figure 2.10. An example switching DC-DC buck converter.



(a) (b)

Figure 2.11. Switch conduction losses and drive losses across channel widths, and the optimum channel width for minimizing losses in (a) CCM and (b) DCM.

Combined Losses: Because W_{OPT} drops with $L_{MIN}^{0.5}$, both P_C and P_D rise with $L_{MIN}^{1.5}$, so their sum also rises with $L_{MIN}^{1.5}$ in both CCM and DCM, as the analytical results in Fig. 2.12 show. Therefore, since bias and bandwidth-critical quiescent losses increase with L_{MIN} and L_{MIN}^{3}, all losses in an optimized design rise with coarser process nodes. In other words, finer pitched technologies yield higher efficiencies, as the simulated results in Fig. 2.13 of

the converter in Fig. 2.10 with optimized 0.18-, 0.35-, and 0.5-µm CMOS switches show. The driving reason for this trend is V_{DD}'s quadratic and linear effects on drive and quiescent losses P_D and P_Q, respectively. Notice that derived theory follows simulations closely.

Simulation Notes: V_{IN} is 1 V to keep the terminal voltages of 0.18 µm transistors within their breakdown limits – stacking techniques would circumvent this limitation [67]-[68]. For maximum gate drive, V_{DD} is 1.5, 3, and 4 V for 0.18-, 0.35-, and 0.5-µm switches, respectively. With 125 µH and 1 µF for L_O and C_O, the converter transitions from DCM to CCM when load current I_O is 2 mA. For ease of implementation, a comparator ensures $i_{L(PK)}$ is 4 mA and a clock changes f_{SW} to ensure the converter can sustain I_O. W_{EQ} is optimum at W_{OPT} (by design) for 0 – 2mA loads in DCM, and for 2mA load in CCM.

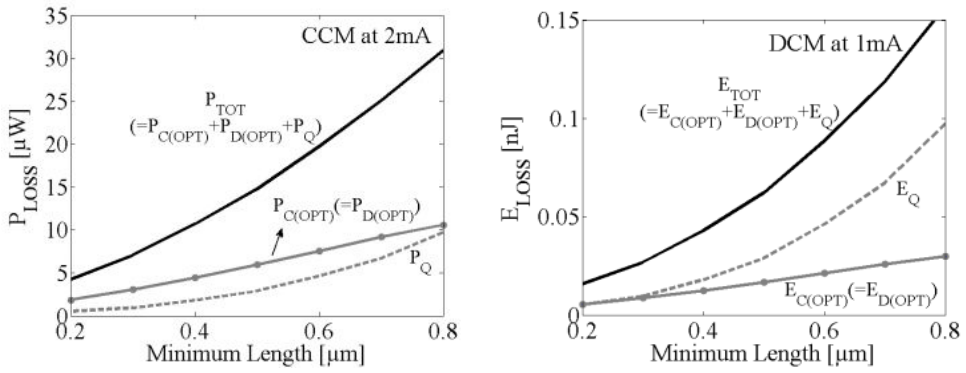


Figure 2.12. Losses of optimized design across L_{MIN}.

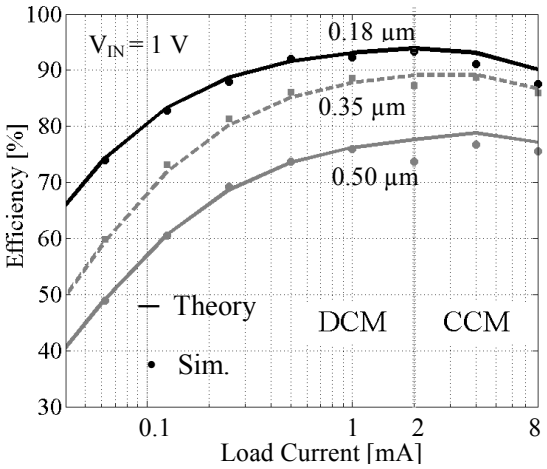


Figure 2.13. Efficiency of optimized design across process nodes.

2.4.6. Maximum Gate Drive vs Input Supply

Designers conventionally select the process so that its breakdown voltages match the application's input supply V_{IN}. With this approach, choosing the lowest L_{MIN} that can sustain V_{IN} yields the highest efficiency (e.g., 0.5-µm switches for a Li Ion's 2.7 – 4.2 V). Higher efficiency is possible, however, if L_{MIN} were lower. For this, stacking transistors in series can limit the voltage each switch receives to a fraction of V_{IN} [67]-[68].

Although series components add resistance, the quadratic fall in drive power P_D that results from a lower gate-drive voltage V_{DD} more than offsets the linear rise in conduction power P_C. The challenge here is designing dedicated gate-drive circuits whose losses do not negate P_D's quadratic savings. Assuming this is not an issue, differentiating P_D and P_C with respect to V_{DD} and equating their sum to zero reveals that switch losses are lowest when V_{DD} is $2|V_{TH}|$, as the analytic results in Fig. 2.14 corroborate.

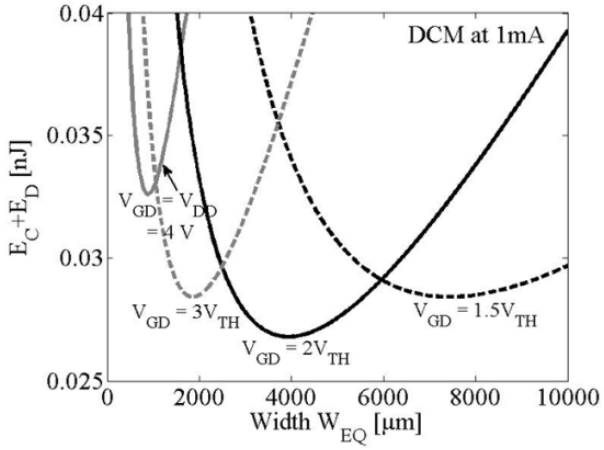


Figure 2.14. Losses across width and gate-drive voltages in DCM.

2.5 Summary

The power conditioning systems should be both power-efficient and compact so that they do not burden the miniaturized systems' limited space. In linear regulators where the efficiency is determined by the ratio of the input and output voltage, it cannot be efficient when the voltage conversion ratio is high. The switching converters are generally more efficient than linear regulators, because the feedback loop adjusts their output currents, allowing a more flexible input and output voltage range. Especially, the inductor-based switching converters can be inherently more efficient by using a quasi-lossless inductor, than the switched-capacitor regulators that is only efficient at specific output voltage levels and always consumes a half of energy in charging (and discharging) the capacitors.

When looking into individual power losses of a general inductor-based switching converter, the conduction losses, switching losses, and quiescent losses all become strong functions of the process parameter. For example, Theory and simulations presented for

optimized 0.18-, 0.35-, and 0.5-μm CMOS switching buck dc–dc converters in CCM and DCM show that lower minimum channel lengths (L_{MIN}) yield higher efficiencies with peaks at 93%, 89%, and 79%, respectively. The fundamental reason for this trend is gate drive increases with L_{MIN}, which causes a quadratic rise in drive losses and a linear rise in quiescent power that more than offset the resulting linear drop in conduction power. Therefore, irrespective of application, converter topology, and mode of operation, finer pitched technologies yield higher efficiency, as long as leakage current, which has a tendency to rise with reductions in L_{MIN}, do not become a considerable fraction of the load. However, all these advantages of an inductor-based switching converter become valid only when the converter limits the number of off-chip high-Q inductors to one for system integration, especially for miniaturized systems such as wireless micro sensors.

Chapter 3. Single-inductor Converters

3.1 Multiple Inputs

Multiple-input converters are circuits that have more than one input sources to accommodate and provide one or more outputs [69]. Multiple sources are required when the amount of power or energy from a single source is not enough or reliable to satisfy the application's demand. By using multiple sources, the reliability and utilization of each source can be improved, selecting the most readily available sources at a time and location [69]. The power conditioning circuits interfacing with more than one input source should be i) energy-efficient, ii) compact, and iii) consider each source's optimal operating conditions (given by voltage-current characteristics or energy-generation mechanisms.) Multiple-input converters, which have originally found usefulness in automotive and residential applications, are now gaining new attentions in renewable energy generations, where the intermittent nature of such sources needs more than one source for reliable energy generation [69]-[70]. More importantly, as the characteristics of each energy source can vary, they often require a dedicated control mechanism or even a dedicated converter, which may significantly increase the number of parts and therefore the cost.

One example of multiple-input converters in renewable energy generation is the hybrid photovoltaic / wind power system introduced in [70]. The photovoltaic and wind energies can be considered as complementary, because in general the photovoltaic source – the sun - provides enough energy during sunny days, but when the sun is gone, strong winds are

more likely to occur [70]. To store energy from these intermittent sources, battery banks have been used to supply a reliable power. However, due to the limitations of batteries such as toxic chemicals, huge size, and the limited cycle life, supplying the ac mains directly from the photovoltaic and wind energy sources by using inverters has become a common way of utilizing these renewable sources [70]. Fig. 3.1 shows the schematic diagram of the hybrid photovoltaic / wind inverter. This circuit consists of a buck / buck-boost fused multiple-input dc-dc converter to store the energy in the capacitor C_{bus}, and a full-bridge dc/ac inverter to supply power to the ac mains [70]. Maximum power point tracking (MPPT) methods are used in drawing energy from both photovoltaic and wind sources individually and simultaneously, with the help of pulse-width modulation (PWM) control schemes.

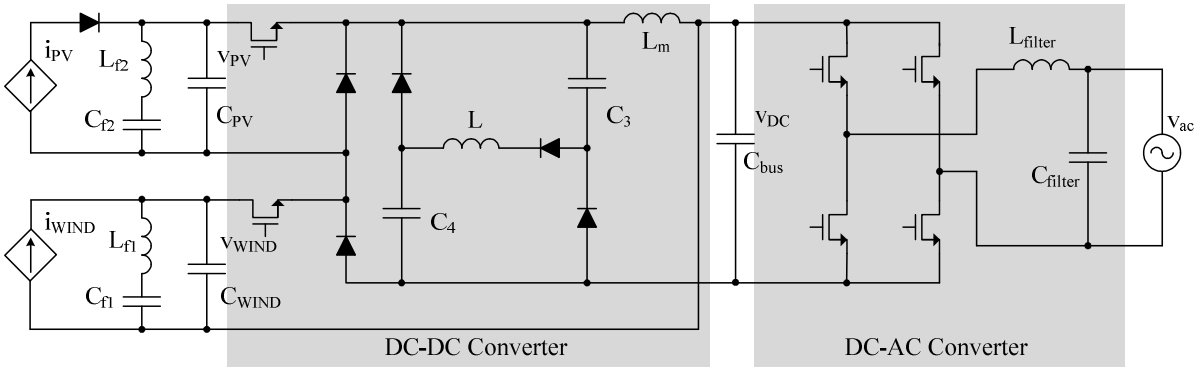


Figure 3.1. Schematic diagram of the hybrid PV/wind inverter.

In automotive applications, multiple-input converters are frequently adopted in hybrid or electric vehicles [47]-[51]. Fuel cells have a high energy density and can be more efficient than the conventional engines, although a cost-effective and safe storage for hydrogen is yet to be developed [47]. Fig. 3.2 shows an example of the hybrid fuel cell / supercapacitor sources and a simplified schematic [47]. As fuel cells generate a lower voltage (12.5 V in

this application), a boost converter is used to generate a higher DC output bus (42 V). A diode in the fuel cell model indicates that the energy flow from the fuel cell is unidirectional: it only generates energy, and cannot be recharged in the reverse direction. Therefore, the converter is also unidirectional, having an asynchronous diode switch to the DC bus. The main power switch S_1 is controlled by a pulse width modulation for average current control, and the clock frequency is constant at 25kHz for the fuel cell's current. The switch S_2 is a shut-down switch to protect the fuel cell from accidental destructions of S_1 during short-circuit events [47].

The supercapacitor also supplies power to the DC output bus with a boost converter, as shown in Fig. 3.2b. However, it can be recharged from the DC bus in the reverse direction in a buck converter's configuration unlike the fuel cell's case, utilizing the same inductor and capacitor during regenerative breaking events (Fig. 3.2b.) The power switches S_3 and S_4 are driven by complementary pulses generated from a hysteretic comparator. The fact that supercapacitors can be easily recharged without much constraints on the charging circuitry and for some hundreds of thousands of cycles, and that they can also generate a sudden high power load reliably and safely make this technology extremely appealing to the automotive applications.

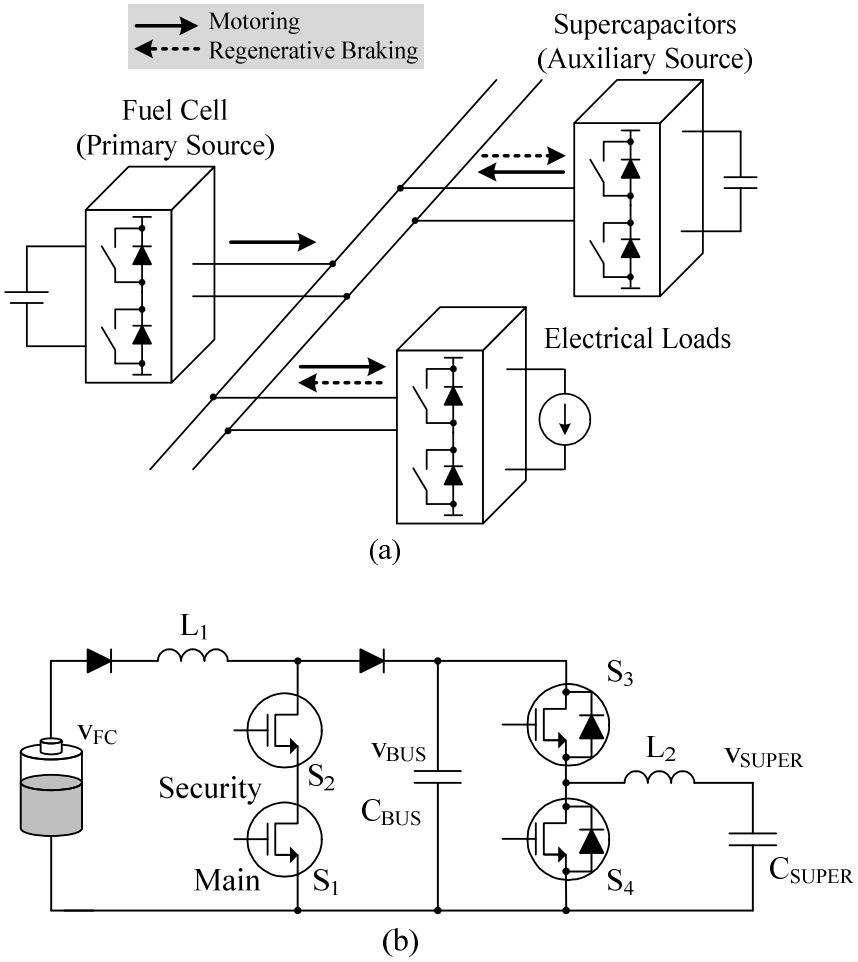


Figure 3.2. (a) Fuel cell / supercapacitor hybrid power sources and a (b) multiple-input converter schematic.

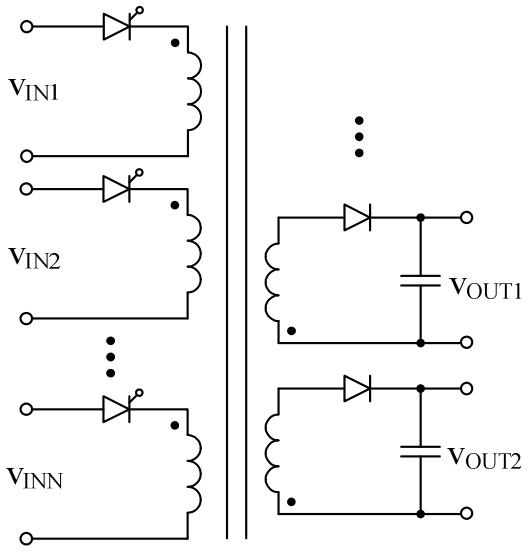


Figure 3.3. Multiple-input multiple-output converter using a transformer core with multiple windings.

In order to accommodate a higher number of multiple inputs, a transformer can be used in general, with a separate winding for each input [71]. The multiple outputs can be also managed by using multiple secondary windings. As the transformer's core is shared in multiple inputs and outputs, the volume is saved when compared to the case when multiple flyback converters are used in parallel [71]. One additional advantage of using a transformer with multiple windings is that it provides good electrical isolation between all inputs and outputs. However, although one core is shared, the transformer core itself requires a large volume to have all the secondary windings, and the benefit will become smaller as the number of inputs and outputs are smaller.

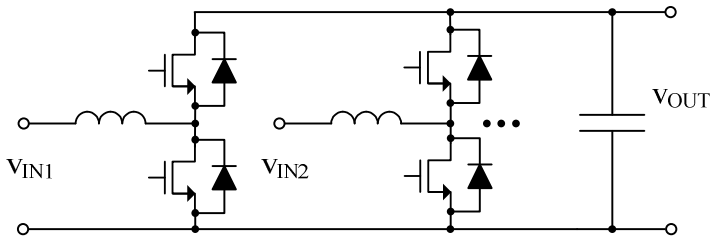


Figure 3.4. Multiple-input boost converters with multiple inductors for each input.

Fig. 3.4 shows another example of a multiple-input boost converter, where multiple inductors are used for each input [72]. This topology has a separate inverter phase leg for each input, and all inputs provide power to the shared DC output bus. The number of inputs can be increased simply by adding more inverter phase legs. The switches can be implemented by bidirectional-conducting, forward-blocking insulated gate bipolar transistors (BCFB IGBTs) or power MOSFETs with an anti-parallel diode [72]. The switches are controlled to condition input power from each input source, and the DC output bus drives an inverter and motor drive. When the inputs supply power, the converters work as boost converters, providing power to the output DC bus. When the inputs receive power in the negative direction, the converters work as buck converters. One of the drawbacks of this converter is that the number of inductors and power switches should add up linearly as the number of inputs increases [72]. In addition, malfunctions in one inverter phase leg can negatively impact the operations in the other legs.

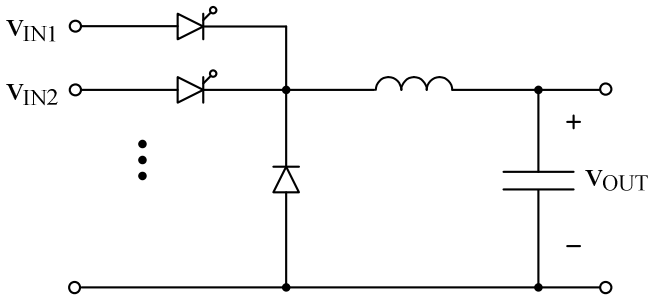


Figure 3.5. Multiple-input buck converters using FCBB switches.

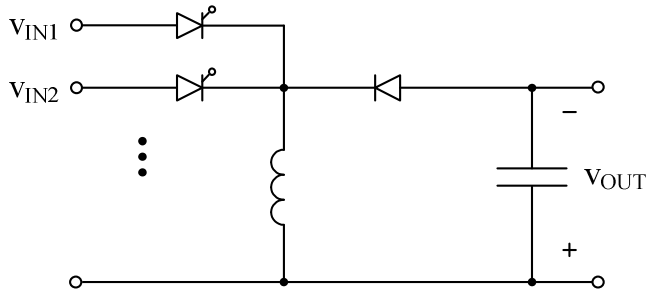


Figure 3.6. Multiple-input buck-boost converters using FCBB switches.

The disadvantages of the converter in Fig. 3.4 can be improved by sharing a single inductor in delivering power from multiple inputs, as shown in Fig. 3.5 and [73]. The number of both semiconductor switches and passive components has been reduced and therefore the cost also. This converter has a forward-conducting, bidirectional-blocking (FCBB) series switch from each energy source, and also has an asynchronous diode shared for all input sources during de-energizing events. One of the limitations of this converter is that it can only provide buck output, and a similarly-designed buck-boost converter in Fig. 3.6 can overcome this limitation.

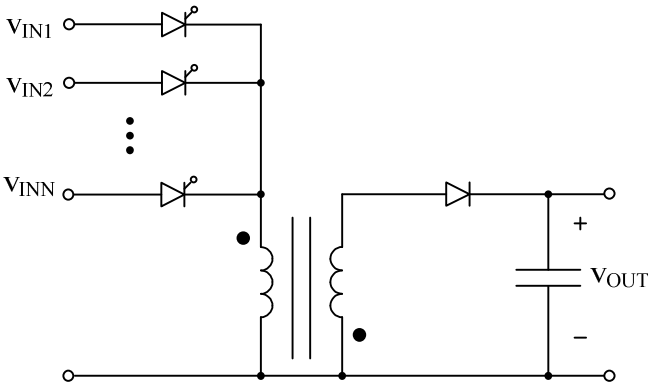


Figure 3.7. Multiple-input flyback converter with a coupled inductor.

Fig. 3.7 shows one variation from multiple-input buck-boost converters introduced in [73] by using a coupled inductor, to provide an isolation between inputs and the output and to provide the non-inverted output voltage [74]. The topology resembles that of a flyback converter, and the power switches are again forward-conducting bidirectional-blocking switches, which can be implemented by gate turn-off thyristors (GTO) or a transistor in series with a diode [74]. However, although this topology shares one coupled inductor in all power transfers from multiple inputs and one output which reduces the device counts and the cost, one coupled inductor can still be too large for a micro-scale systems where an additional save in volume means a prolonged operational lifetime or an extended functionality that it could not have when it was using a bulky energy-transfer medium. More importantly, most of the state-of-the-art multiple-input converters only concern about the availability or the amount of energy that each source can provide in power budgeting, while in hybrid-sourced applications, how to distribute the output's power requirements to

each source from the load's perspective can be more important to prolong the operational lifetime of such systems.

3.2 Multiple Outputs

Multiple-output converters are circuits that provide power and energy to more than one output. This concept has been popular in applications where the system has more than one kind of loads, each having a different current and voltage characteristic. Recently, this idea has broaden its application area deeper into the system's internal operations, where a power converter provides a set of different internal voltages to supply different internal blocks at each optimal voltage, to achieve a higher efficiency using a dynamic voltage scaling [75]. In such systems, a transformer can be used to provide multiple outputs, as already discussed in the previous section. Especially for the applications where the volume is not much constrained and the electrical isolation between the inputs and outputs are important, transformers still can be cost-effective solutions in automotive or residential applications [71].

In smaller-scale, handheld applications, however, transformers are oftentimes not welcomed because their core itself is bulky, not to mention the additional volume of the multiple secondary windings that need to be added to accommodate more inputs and outputs. Instead, single-inductor multiple-output converters can provide a much compact and efficient solution in interfacing with multiple outputs with a single quasi-lossless inductor in battery-operated standalone electronics and even smaller wireless sensors [76]. In such systems, one of the most important issues is how to allocate the single inductor to

various power paths so that all the outputs get the sufficient power from the input sources in a timely manner.

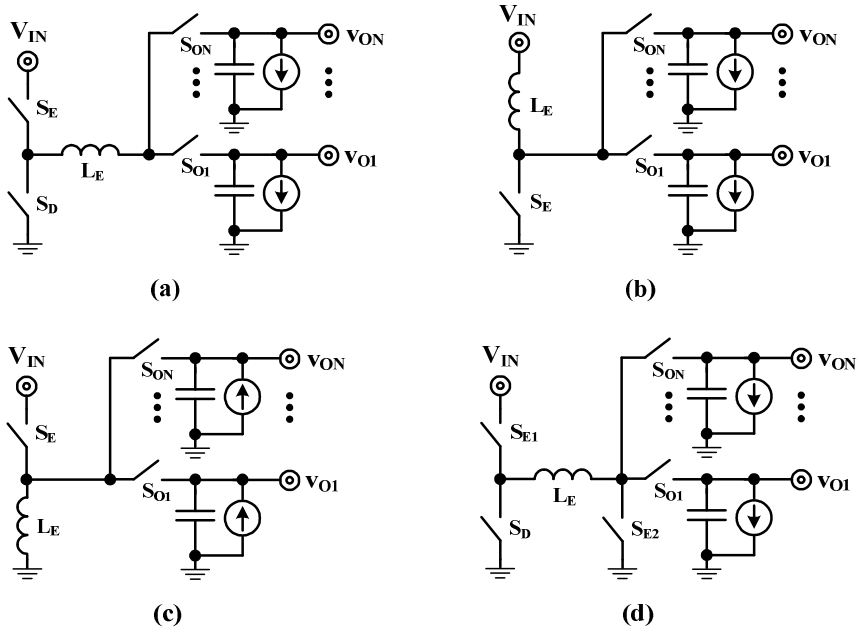


Figure 3.8. Single-inductor multiple-output converters in (a) buck, (b) boost, (c) inverting buck/boost, and (d) non-inverting buck/boost configurations.

The topologies of single-inductor multiple-output (SIMO) converters are generally circuit extrapolations of single-inductor single-output power stages, except for the energy flow and feedback [77]. Fig. 3.8 shows buck, boost, inverting buck/boost, and non-inverting buck/boost configurations of SIMO converters, where the inductor current is distributed into N outputs by N output switches S_{O1}, S_{O2}, …, S_{ON}. The inductor current is time-shared by the N outputs, and each output switch must conduct the inductor current for only a fraction of the time without overlap, to avoid short-circuiting the outputs. In a buck converter's case (Fig. 3.8a), S_E and one of the output switches are closed to charge the

inductor, while closing S_D discharges the inductor's energy into one of the outputs at a time. As the average voltage across the inductor is zero in steady state, then the averaged switching node voltage $v_{SW(AVG)}$ becomes the averaged output voltage [77]:

$$v_{SW(AVG)} = D_{IN} V_{IN} = \sum_{k=1}^{N} D_{O(k)} V_{O(k)} \,. \tag{3-1}$$

For a boost converter's case, the switch S_E is closed to energize the inductor, and one of the switches from S_{O1} to S_{ON} turns on to de-energize the inductor's energy to the corresponding output (Fig. 3.8b). In steady state, as the average voltage across the inductor is zero, the input voltage becomes the averaged output voltage of the switching node:

$$V_{IN} = v_{SW(AVG)} = \sum_{k=1}^{N} D_{O(k)} V_{O(k)} \,. \tag{3-2}$$

In an inverting buck-boost configuration, the inductor is energized similarly by closing the switch S_E, but in this case the direction of the inductor current is opposite, drawing the current from the outputs in de-energizing phases to provide negative output voltages (Fig. 3.8c). In steady state, as the one terminal of the inductor is connected to the ground, the average voltage of the switching node becomes equal to the ground:

$$v_{SW(AVG)} = \sum_{k=1}^{N} D_{O(k)} V_{O(k)} + D_{IN} V_{IN} = 0 \,. \tag{3-3}$$

Fig. 3.8d shows a non-inverting buck-boost configuration, where the converter provides positive voltages while it can still provide both a higher or lower output voltage than the input voltage. This topology is frequently adopted due to its versatility – which can provide

a wide range of non-inverted outputs, but it requires one additional power switch to energize the inductor (the switches S_{E1} and S_{E2} engages in energizing events.) Similarly in this case, the averaged switching nodes become the same, and therefore:

$$D_{IN}V_{IN} = \sum_{k=1}^{N} D_{O(k)}V_{O(k)} \ . \tag{3-4}$$

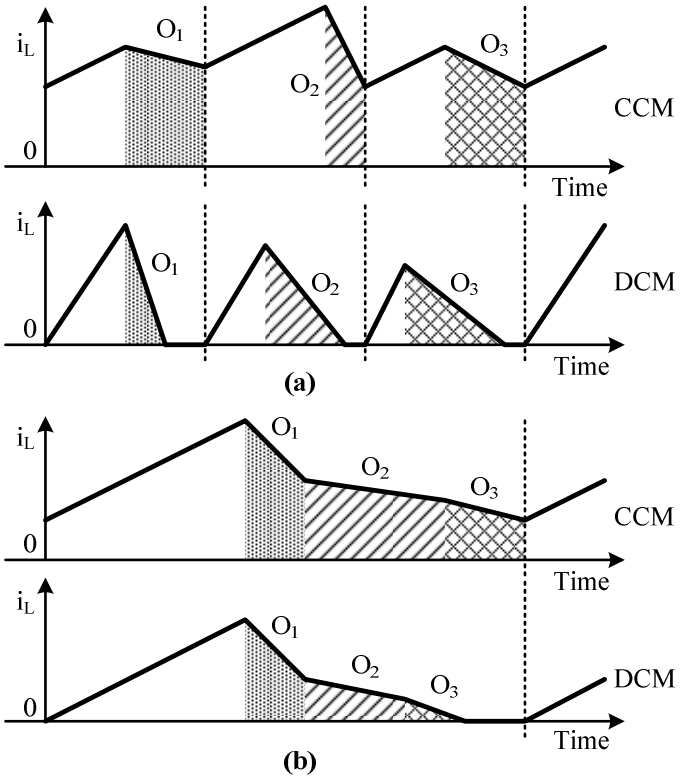


Figure 3.9. Inductor-current waveforms for SIMO converters with
(a) dedicated energize/de-energize sequences and
(b) one shared energize followed by de-energize sequences.

The resulting inductor current waveforms become different with the energy flow and conduction modes, as shown in Fig. 3.9. The converters in [78]-[82] dedicate an

energize/de-energize sequence to each of N outputs by a time-multiplexing switching period, as shown in Fig. 3.9a. The feedback control individually regulates each output, and the inductor can conduct either continuously (continuous conduction mode, CCM) or discontinuously (discontinuous conduction mode, DCM) according to the load level. The pseudo-continuous conduction mode emulates DCM in CCM to reduce the cross-regulation problem in multiple-output converters, which occurs when the regulation of one output affects that of the other, leading to poor regulation or stability problem.

The converters in [83]-[91], on the other hand, energize the inductor only once in the switching period, but with enough energy to supply all loads (Fig. 3.9b). In other words, the energizing time is determined to cover the collective demand of all the outputs, while the de-energizing time is set by each output's individual demand. Similar to the previous case, the converters can operate in CCM or DCM (Fig. 3.9b), but the cross-regulation problem can be more severe than the dedicated energize/de-energizing schemes, because each output's conduction time affects the others. The accuracy performance of this single-energizing control for multiple outputs is generally better than that of the dedicated energizing/de-energizing control, because each output gets some of the inductor's energy in every switching period more frequently, resulting in smaller voltage ripples at each output. In all SIMO cases, the most important consideration is how to energize the inductor and distribute its energy to the multiple outputs so that each regulated output shows good accuracies and does not suffer from serious cross-regulation problems.

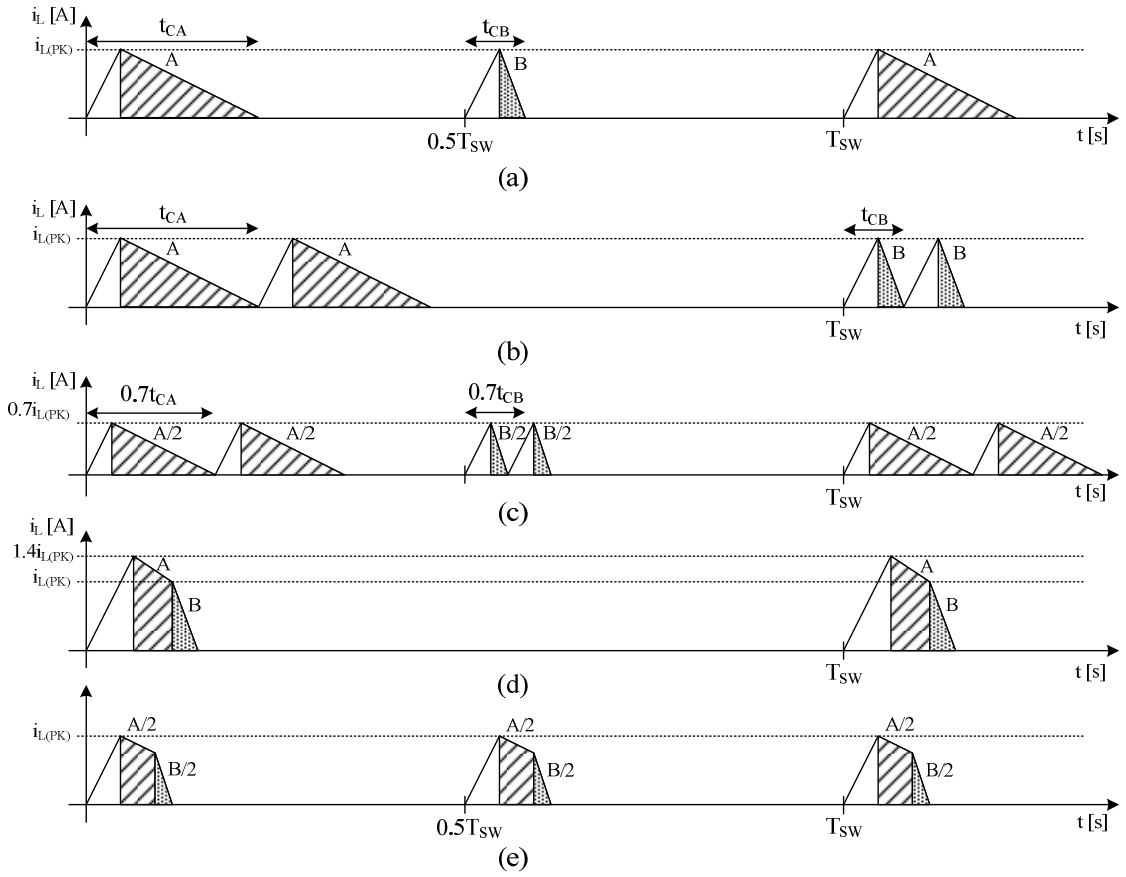


Figure 3.10. Inductor current waveforms of five different single-inductor dual-output switching sequences delivering the same output powers.

More analytic comparisons between the dedicated energizing/de-energizing sequences and the shared energizing event followed by de-energizing sequences can be possible. For example, Fig. 3.10 shows the five different switching sequences in delivering the output power to the dual output A and B respectively. The purpose of this comparison is to compare the trends of the important power losses in these five different sequences in delivering the same amount of power and eventually decide which sequence incurs the least power losses of all and therefore the most efficient. For fair comparisons, below are the

premises that needs to be applied: (1) the output power delivered to A (or B) should be the same in five sequences, (2) the converter works in discontinuous conduction mode, (3) the converter uses the same inductor, input voltage, and output voltages (so that the inductor currents have the same slope in all sequences), (4) the peak current $i_{L(PK)}$ is the same in all sequences.

The parameters that are to be compared are output voltage ripple Δv_O, gate-drive losses P_{GD}, IV-overlap losses P_{IV}, and AC-conduction losses P_{AC}. The output voltage ripple becomes proportional to the amount of charge per one energy packet times the number of packets per a switching cycle, divided by the output capacitor (assuming the load current is small). As the energy packet's charge is proportional to the inductor's peak current and the de-energizing time, the ripple becomes proportional to the square of $i_{L(PK)}$,

$$\Delta v_O = \frac{\Delta q_O N_{EP}}{C_O} \propto \frac{i_{L(PK)} t_{DE} N_{EP}}{C_O} \propto \frac{i_{L(PK)}{}^2 N_{EP}}{C_O} \tag{3-5}$$

where Δ_{qO} is the amount of charge to the output and N_{EP} is the number of energy packets per one switching cycle. The gate-drive losses are the product of the energy loss in driving the power switches and the switching frequency, and the former is not a function of the choice of energizing and de-energizing sequences. Therefore, the only important relation here is with the switching period and the number of gate-drive events N_{GD}:

$$P_{GD} = E_{GD} f_{SW} N_{GD} \propto \frac{1}{T_{SW}} N_{GD}. \tag{3-6}$$

The IV-overlap losses are proportional to the energy loss and the number of energy packets N_{EP} and the switching frequency, and the energy loss itself increases with the inductor's peak current:

$$P_{IV} = 0.5 i_{L(PK)} (V_{IN} + V_D) t_{OVER} N_{EP} f_{SW} \propto i_{L(PK)} N_{EP} \frac{1}{T_{SW}} \quad . \tag{3-7}$$

The ac conduction losses are proportional to the energy packet's size and the average number of energy packets, and as the conduction time t_Δ linearly increases with $i_{L(PK)}$,

$$P_{C.AC} = \frac{1}{3} i_{L(PK)}{}^2 t_\Delta N_{EP} f_{SW} R_{C.AC} \propto i_{L(PK)}{}^3 N_{EP} \frac{1}{T_{SW}} . \tag{3-8}$$

The first sequence in Fig. 3.10a is the reference sequence, delivering an energy packet 'A' to one output A with a switching period of T_{SW}, and another energy packet 'B' to the other output B with the same T_{SW}, but in alternating cycles. All the parameters and losses of the other sequences (b)−(e) will be compared against the parameters of this sequence (a). The second sequence (b) delivers twice the energy packet 'A' and 'B', but with a switching period of $2T_{SW}$, so that it still delivers the same overall output power to A and B. As this delivers two energy packets within one cycle, the output ripple Δv_O increases by two. The gate drive losses (P_{GD}) remain the same, because the average switching times do not change, and so is the iv overlap losses P_{IV}. The ripple conduction losses P_{AC} also remain the same, because the increase in Δv_O is cancelled by the decrease in the switching frequency. Therefore, in overall, the total power losses of the sequence (b) become similar to those of the reference sequence (a) (Table 3-1.)

The switching pattern of the sequence (c) is similar to that of the sequence (b), but the difference is the reduced size of an energy packet by half, and the increased switching frequency by two. The inductor's peak current should decrease by 0.7 times to reduce the size of an energy packet by half, and because of this, the output ripple reduces by half compared to (b). P_{GD} also increases by two, because the average number of gate-drive events increases by two. P_{IV} becomes 1.4 times regardless of the decreased $i_{L(PK)}$, because of the increased number of energy packets per switching period. P_{AC} becomes smaller than the other sequences, because $i_{L(PK)}$ is the smallest of all. Overall, due to the increased switching times, the total power loss of the sequence (c) becomes higher than that of the reference case.

The switching pattern of the sequence (d) is different from all the other preceding sequences in the meaning that one energy packet is being split into the two outputs. The inductor's peak current therefore has to increase to hold the total energy to output A and B in one energy packet, and because of that, Δv_O increases by 1.4. The switching frequency can be the same as the total energy packet per switching cycle stays the same. But as the number of gate-drive switching events per one switching cycle is decreased from 4 to 3, P_{GD} decreases by 0.75. P_{IV} increases slightly due to the increase in $i_{L(PK)}$. P_{AC} becomes the highest of all sequences, because the peak current is at its maximum of all. Although this sequence has lower gate-drive losses, it leads to higher overall losses if the ac resistance is not negligible.

The last switching sequence (e) is similar to the sequence (d), except that the overall frequency is increased by two and the peak current should therefore be decreased. As the equivalent peak current decreases, it has the lowest output ripple of all sequences. P_{GD} increases by 2 times compared to the sequence (d) because of the increased switching frequency. Although this sequence has a lower $i_{L(PK)}$ than the sequence (d), P_{IV} actually increases due to the increased number of energy packets by two, similarly in P_{AC}. In short, although the voltage ripple is at the minimum, all the individual losses has increased because the reduced peak current could not compensate for the increased numbers of energy packets and gate-drive events.

Sequences	$i_{L(PK)}$	N_{EP}	N_{GD}	T_{SW}	Δv_O	P_{GD}	P_{IV}	P_{AC}	P_{TOT}
(a) 1 Cycle / 1 Out	1	1	1	1	1	1	1	1	1
(b) 2 Cycles / 1 Out (1)	1	2	2	2	2	1	1	1	≈
(c) 2 Cycles / 1 Out (2)	0.7	2	2	1	1	2	1.4	0.7	>>
(d) 2 Outs / 1 Cycle (1)	1.2	1	0.75	1	1.4	0.75	1.2	1.7	>
(e) 2 Outs / 1 Cycle (2)	0.85	1	0.75	0.5	0.7	1.5	1.7	1.2	>>

Table 3-1. Comparisons of Parameters and Power Losses in Five Different Single-Inductor Dual-Output Switching Sequences.

3.3 Single-Inductor Dual-Input Dual-Output Systems and Limitations

As the hybrid sourcing and charging techniques as well as dynamic voltage scaling techniques become popular, the converters combining the benefits of both multiple-input converters and multiple-output converters are frequently adopted in wide application areas. Especially in micro-scale electronics where the demand for the further miniaturization and

longer operational lifetime is high, a compact and efficient converter using a single high-Q off-chip inductor is becoming a dominant solution. As single-inductor multiple-input multiple-output converters should interface with various sources and outputs with different voltage-current characteristics, they should be able to i) distribute the multiple sources' energy to more than one output, and ii) to assign the output's energy requirements to each source efficiently.

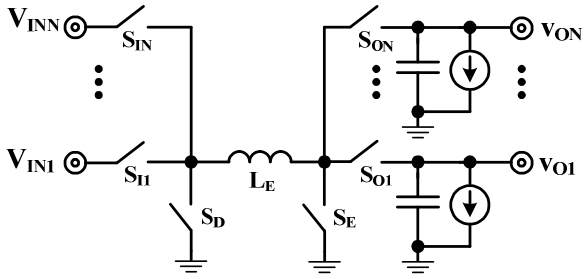


Figure 3.11. General topology of a SIMIMO non-inverting buck/boost converter.

Fig. 3.11 shows a general topology of a single-inductor multiple-input multiple-output (SIMIMO) non-inverting buck/boost converter, where power multiplexing is achieved by input and output switches [92]. During energizing events, one of the input switches from S_{I1} to S_{IN} and the switch S_E turn on, and during de-energizing events, one of the output switches from S_{O1} to S_{ON} and the switch S_D turn on. As there is only one inductor in various power paths, the inductor should be shared in a time-multiplexed control that decides from which input to draw the energy and to which output to direct the inductor's energy.

Like in SIMO converters, the multiple-input converters can either have dedicated energizing sequences for each source or share one energizing event between multiple

sources. Fig. 3.12 shows the examples of (a) dedicated energizing sequences for each source and (b) one shared energizing sequence between dual sources, operating in discontinuous conduction mode. In the dedicated energizing sequence, one energy packet is entirely supplied by either source A or B, while in the shared energizing sequence, one energy packet is supplied sequentially by source A and B. Different inductor peak currents $i_{L(PK).A}$ and $i_{L(PK).B}$ are to emphasize the fact that the maximum or optimal current from each source can be different.

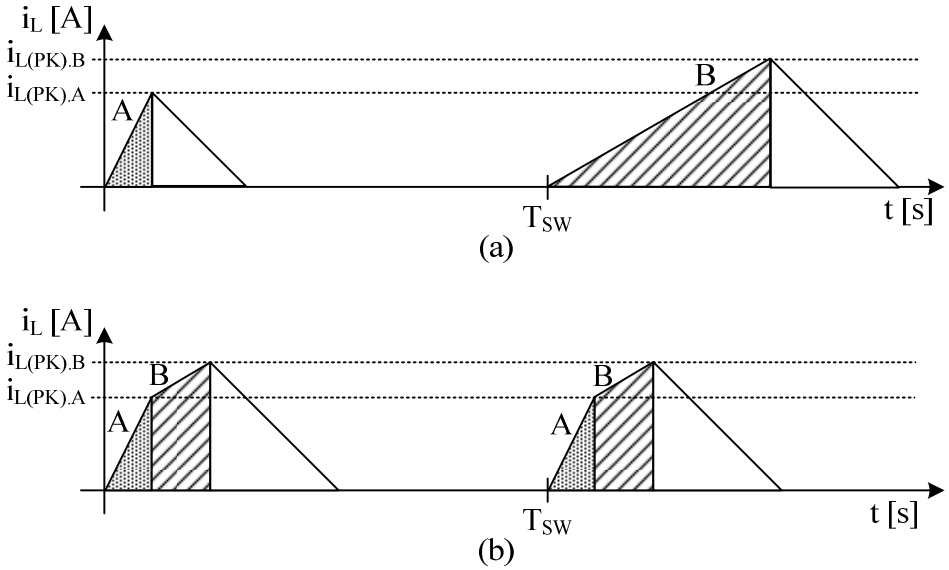
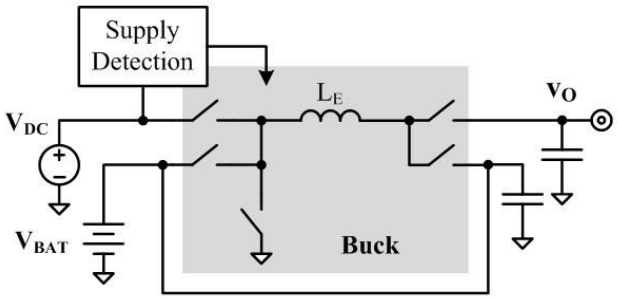
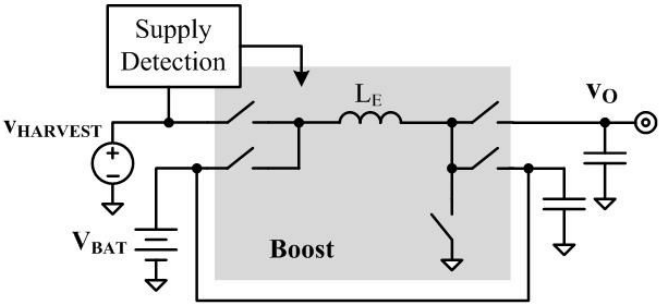


Figure 3.12. (a) Dedicated energizing sequences for each source and (b) one shared energizing sequence between multiple sources.



(a)



(b)

Figure 3.13. Single-inductor dual-input dual-output topologies for (a) an integrated-battery-charging application and (b) an energy-harvesting application.

In [93], a single-inductor dual-input dual-output (SIDIDO) switching converter having an external DC power source and a rechargeable battery as an offline power source is introduced. Unlike the conventional battery power management system, this converter uses a single inductor in time-multiplexing the external DC power to the system's load and charging up the battery in DCM, while the battery supplies the load when the main external source is removed (Fig. 3.13a). In [94], an integrated single-inductor dual-input dual-output boost converter for energy harvesting applications was designed. Similar to [93], this

system has a charge storage device as its secondary input, to deliver the load power when the intermittent energy harvesting source is not available. The direct energy path from the energy harvesting source to the load is better in terms of efficiency, than the cascaded energy path from the harvesting source to the battery and then to the load, because the latter passes through two converters. These SIDIDO converters forego compensating for battery non-idealities in favor of accommodating for a possibly disconnected dc source and an intermittent harvester. However, the functionality of selecting an optimal source from a hybrid combination of a high-energy source and a high-power source for a load's level is largely absent in the state of the art.

3.4 Summary

Single-inductor converters have all the benefits of inductor-based switching converters including high efficiency and wide range of inputs and outputs, but allow only one high-Q inductor to be used in volume-constrained micro-scale electronic systems. As various power paths should share a single inductor, the converter with multiple inputs and multiple outputs generally use a time-multiplexed control in discontinuous conduction mode to avoid any interference between different power paths. Especially, when the system has multiple inputs, the converter should try its best to condition each source at its optimum operating region, generally defined by the voltage – current characteristics of it. When the system needs to recharge one of its input sources, or has more than one output, then the converter should be able to allocate the available energy to outputs in a smart way so that

each output gets the required power sequentially with the order of their priorities without any systematic failure.

In hybrid-sourced micro-scale electronic systems, single-inductor dual-input dual-output converters can efficiently draw energy from the hybrid sources and oftentimes recharge one of them if needed, while supplying one or more outputs in the most compact solution. In drawing the energy from a hybrid combination of power-dense and energy-dense sources, choosing an appropriate energy source for the characteristic of the load at each time can lead to the most compact and efficient sourcing solution. Therefore, an adaptive control scheme to select an appropriate energy source with respect to the load's level is a key to achieve the real benefits of using hybrid sources, while the state-of-the-art SIDIDO converters generally focus more on the sources' condition and availability rather than the load.

Chapter 4. Nested-Hysteretic Dual-source Charger-Supply System

From the previous chapters, it is concluded that a single-inductor dual-input dual-output converter is a both compact and efficient solution in dealing with hybrid sources. Then the question becomes how to share this quasi-lossless inductor in a time-multiplexed manner in more than one power path. Therefore, the first IC prototype - the nested hysteretic dual-source charger-supply system - focuses on implementing the single-inductor time-multiplexing control and verifying the functionality of the control. The target functionality of this control is to draw a low, average power from an energy-dense source and a higher, peak power from a power-dense source to supply a load and to recharge the power-dense source from the energy source.

4.1 Energy Flow and Power Stage

The objective of the fully hysteretic charger-supply system is to draw the optimum amount of power the FC can supply for its size from the FC and channel all or a fraction of it to the load, using the excess to recharge a battery. The system designer therefore allocates just enough FC area to supply the average power needed by the system, tank space for the fuel to last the lifetime needed, and package volume for the Li Ion to ably source power bursts. The system must consequently transfer energy from the FC to both the load and the Li Ion and from the Li Ion to the load. As a result, the converter (with one inductor only) must boost a FC's 0.5 – 0.7 V to a Li Ion's 2.7 – 4.2 V (via the FC-Li Ion path in Fig. 4.1) and a

load at possibly 1 V (via the FC-load path) [95] and buck a Li Ion's 2.7 – 4.2 V to a load at 1 V (via the Li Ion-load path).

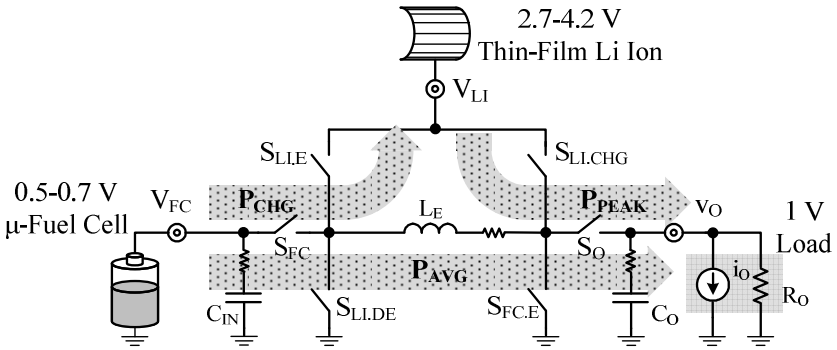


Figure 4.1. Energy-flow (path) diagram of the proposed power stage.

Note that eliminating the FC-load path (and allowing the Li Ion to supply all load levels) is possible but not optimal because (*i*) the FC outlasts the Li Ion during light loads and (*ii*) the converter incurs more power losses when conditioning FC power to charge the Li Ion and Li-Ion power to supply the load. The integrated switches of the converter therefore energize inductor L_E from either the FC or the Li Ion and subsequently de-energize it into either the load or Li Ion via separate and alternating energy-flow paths, according to the needs of the load.

The converter regulates L_E's current i_L with hysteretic control to one of two predefined targets (Fig. 4.2) : I_{FC} or I_{LI}, depending on the source from which L_E draws energy. I_{FC} is sufficiently small (at 0.5 mA) to avoid stressing the FC's membrane electrode assembly beyond its rating (for overload protection) and high enough to reduce the percentage of fuel lost through the membrane as leakage (for load matching) [96]-[98]. I_{LI} is higher at 2.5 mA

to supply the heavier loads that the small fuel cell cannot. In other words, L_E practically functions like a 0.5 or 2.5 mA current source. From a mechanical perspective, the FC's membrane should be just wide enough to supply the load's average needs (as I_{FC}) and the Li Ion large enough to never fully charge. If the Li Ion fully charges and i_O is zero, the charger-supply must shut down; but for proof of concept, the prototype does not include this form of protection.

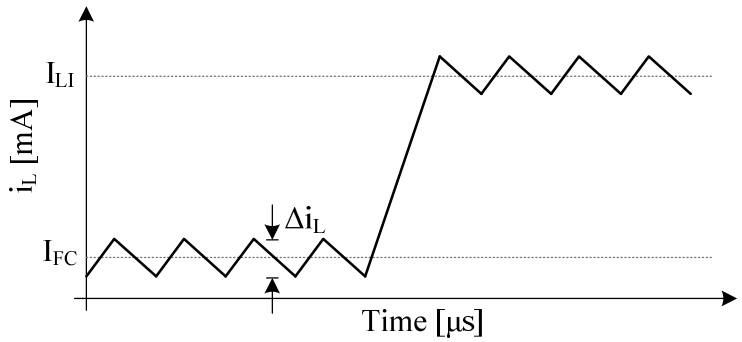


Figure 4.2. Hysteretic-controlled inductor current and the two targets I_{FC} and I_{LI}.

During light loads, the system derives power from the FC only so the circuit regulates i_L to reference I_{FC} and average FC power P_{FC} equals $I_{FC}V_{FC}$. Because P_{FC} exceeds output power P_O in the light-load mode (LLM), the controller partitions (i.e., time-divides) P_{FC} to supply the load and charge the Li Ion, with load level i_O determining what fraction of P_{FC} to steer into the battery. Graphically, the solid line in Fig. 4.3 indicates the fraction of P_{FC} delivered to the load (as load-FC ratio $r_{LD/FC}$), which equates to the fraction of time the FC supplies the load, or said differently, how often the FC connects to the load. As a result, $r_{LD/FC}$ is zero when i_O is zero (Fig. 4.3) so the system disconnects from the load and directs

all of P_{FC} into the battery. As i_O increases, the converter raises connectivity ratio $r_{LD/FC}$ to channel an increasing fraction of P_{FC} into the load (and a decreasing share into the battery):

$$P_O|_{LLM} \approx r_{LD/FC} P_{FC} \approx r_{LD/FC} I_{FC} V_{FC}, \tag{4-1}$$

and

$$P_{LI}|_{LLM} \approx (1 - r_{LD/FC}) P_{FC}. \tag{4-2}$$

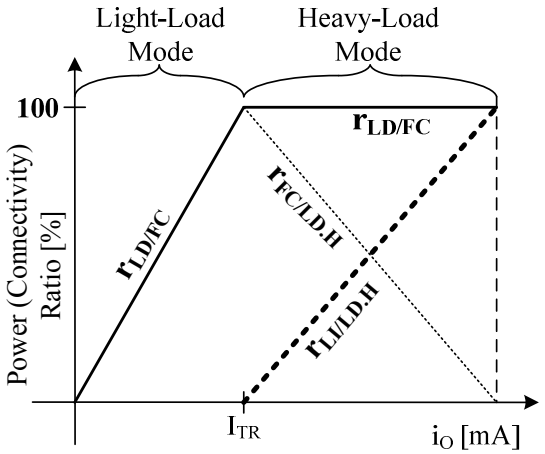


Figure 4.3. Power (connectivity) ratios across load.

When i_O's power P_O surpasses P_{FC} (past transition threshold I_{TR}, after $r_{LD/FC}$ reaches one), the converter enters the heavy-load mode (HLM) by augmenting P_{FC} with average Li-Ion power P_{LI}. Because the aggregate sum of average power levels P_{FC} and P_{LI} must sustain P_O in HLM, the supply draws energy more often from the battery (so average power P_{LI} increases) as i_O increases past I_{TR}. Accordingly, Li Ion-load (and connectivity) ratio $r_{LI/LD.H}$ (illustrated by the dotted line in Fig. 4.3) increases with i_O (as FC-load ratio $r_{FC/LD.H}$ decreases):

$$P_O\big|_{HLM} \approx r_{LD/FC} P_{FC}\big|_{HLM} + P_{LI} = P_{FC} + P_{LI}$$

$$= r_{FC/LD.H} I_{FC} V_{FC} + r_{LI/LD.H} I_{LI} V_{LI}$$

$$= (1 - r_{LI/LD.H}) I_{FC} V_{FC} + r_{LI/LD.H} I_{LI} V_{LI}. \quad (4\text{-}3)$$

Raising $r_{LI/LD.H}$ decreases the FC's connectivity to the load so FC-load ratio $r_{FC/LD.H}$ is $r_{LI/LD.H}$'s complement. Notice instantaneous power $I_{LI}V_{LI}$ sets the converter's maximum output power, which happens when the converter only draws energy from the Li Ion, when $r_{LI/LD.H}$ is one.

4.2 Feedback Control

Hysteretic comparator CMP_V in Fig. 4.4 senses and regulates v_O to $V_{O.REF}$ by steering what amounts to a current source (L_E) into or away from v_O at $f_{O.SW}$, the system's switching frequency. To CMP_V's feedback loop, L_E is practically a current source because comparator CMP_I regulates i_L at a switching frequency $f_{I.SW}$ that is higher than $f_{O.SW}$. Depending on the level of the load, mode comparator CMP_M dictates whether to draw i_L from the FC or both the FC and the Li Ion. R_S and $V_{I.REF}$ ultimately set i_L's regulation target to I_{FC} (when drawing energy from the FC) and I_{LI} (when deriving i_L from the Li Ion). Note I_{FC} is lower than I_{LI} because the FC cannot source the power the Li Ion can.

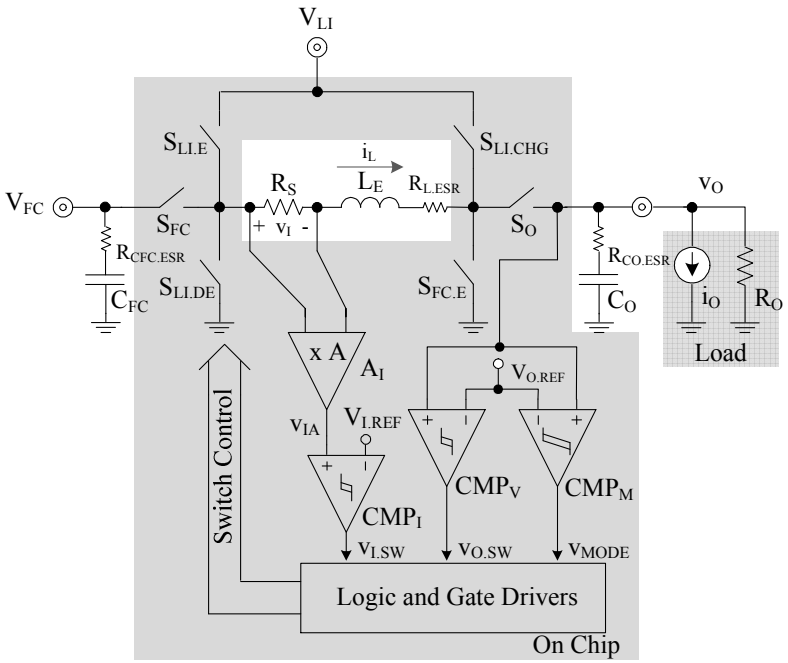


Figure 4.4. System-level schematic of the proposed charger-supply system.

In light loads, switch S_{FC} in the power stage shown in Fig. 4.4 remains closed and $S_{FC.E}$ energizes inductor L_E from the FC while S_O and $S_{LI.CHG}$ de-energize L_E into v_O and the Li Ion. Similarly, when heavily loaded and drawing energy from the FC, S_{FC} stays closed and $S_{FC.E}$ energizes L_E with the FC while S_O de-energizes L_E into v_O. When drawing energy from the Li Ion, S_O remains closed and $S_{LI.E}$ energizes L_E from the Li Ion and $S_{LI.DE}$ de-energizes L_E into v_O.

4.2.1. Hysteretic Current Loop

The LC filter introduces a complex conjugate pair of poles in the frequency response that, if not properly handled, compromises the stability of the system. A conventional means of reducing the pair into a single dominant pole is to regulate inductor current i_L past the

system's switching frequency $f_{O.SW}$ so that inductor L_E functions like a current source below $f_{O.SW}$ [60]. In like manner, the proposed converter uses hysteretic control to regulate i_L to I_{FC} and I_{LI} when drawing energy from the FC and the Li Ion, respectively, at a switching frequency $f_{I.SW}$ that exceeds the system's $f_{O.SW}$.

To regulate i_L, series resistor R_S senses i_L to produce v_I, amplifier A_I then amplifies v_I to generate v_{IA}, and hysteretic comparator CMP_I compares v_{IA} against current reference $V_{I.REF}$ to regulate v_{IA} within CMP_I's hysteretic window (Fig. 4.4). CMP_I's output $v_{I.SW}$ then determines the connectivity of the switches, which the control logic implements. CMP_I's hysteresis and i_L's rising and falling rates (as set by L_E, V_{FC}, V_{LI}, and V_O) establish the switching frequency of the current loop ($f_{I.SW}$) and i_L's peak current $i_{L(PEAK)}$, where $f_{I.SW}$ exceeds $f_{O.SW}$ and $i_{L(PEAK)}$ falls below the FC's rated limit. CMP_I establishes the hysteresis in Fig. 4.5 with its inherent propagation delay. In other words, CMP_I senses when i_L surpasses target I_{FC} (when connected to the FC) and, after rising delay $t_{P.R}$ (~ 0.1 μs), its output $v_{I.SW}$ prompts the controller to end the energizing cycle, allowing i_L to peak at $I_{FC(MAX)}$. Similarly, CMP_I senses when i_L falls below I_{FC} and, after falling delay $t_{P.F}$ (~ 0.1 μs), when i_L reaches $I_{FC(MIN)}$, CMP_I trips. If $t_{P.F}$ is so long that i_L falls below zero, C_{FC} sinks the reverse current and the system continues to operate normally, provided i_L's average stays above zero. Notice that while using $t_{P.R}$ and $t_{P.F}$ to set current ripple Δi_L is not accurate, doing so establishes a small ripple, which is important to keep P_{FC} steady.

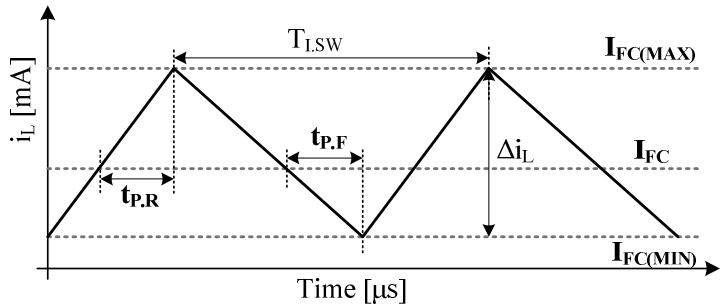


Figure 4.5. Inductor current ripple through the FC-load path.

4.2.2. Nested Hysteretic Voltage Loop

4.2.2.1. Output Regulation

Each mode of operation steers inductor energy to regulate output voltage v_O to reference $V_{O.REF}$ within a hysteretic window (ΔV_O). In LLM, v_O rises to the upper window limit when the converter directs P_{FC} to v_O and droops to the lower limit when L_E disconnects (and the system charges the Li Ion). Similarly, v_O rises in HLM when the converter supplies the load with Li-Ion power P_{LI} and falls when using FC power P_{FC} (because P_{FC} is lower than P_{LI} by design). Hysteretic comparator CMP_V senses and regulates v_O to $V_{O.REF}$ within CMP_V's hysteretic window ΔV_O (Fig. 4.6). For that purpose, CMP_V's output $v_{O.SW}$ sets how often L_E de-energizes into v_O in LLM (as load-FC power and connectivity ratio $r_{LD/FC}$) and energizes from the Li Ion in HLM (as Li Ion-load power and connectivity ratio $r_{LI/LD.H}$).

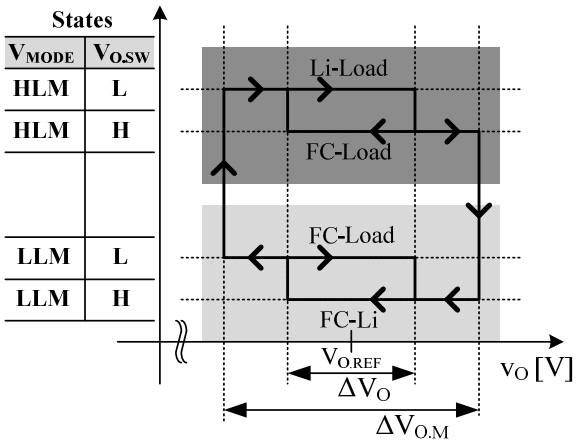


Figure 4.6. The nested hysteretic windows that regulate the output in light- and heavy-load modes.

4.2.2.2. Mode Control

With a wider hysteretic window $\Delta V_{O.M}$, CMP_M senses v_O to determine which mode of operation to assert. If P_{FC} is insufficient to satisfy the load, i_O pulls v_O to CMP_M's lower limit, prompting the converter (with v_{MODE}) to enter HLM. Conversely, when the converter sources more power than needed, the excess power pulls v_O to CMP_M's upper limit, triggering v_{MODE} to force the converter into LLM. Note v_O remains within smaller hysteretic window ΔV_O in steady state and only extends beyond ΔV_O to $\Delta V_{O.M}$ when i_O surpasses boundary limit I_{TR}, resulting in the nested hysteresis shown in Fig. 4.6 and v_O's response to 0.1 – 1-mA load transitions in Fig. 4.7.

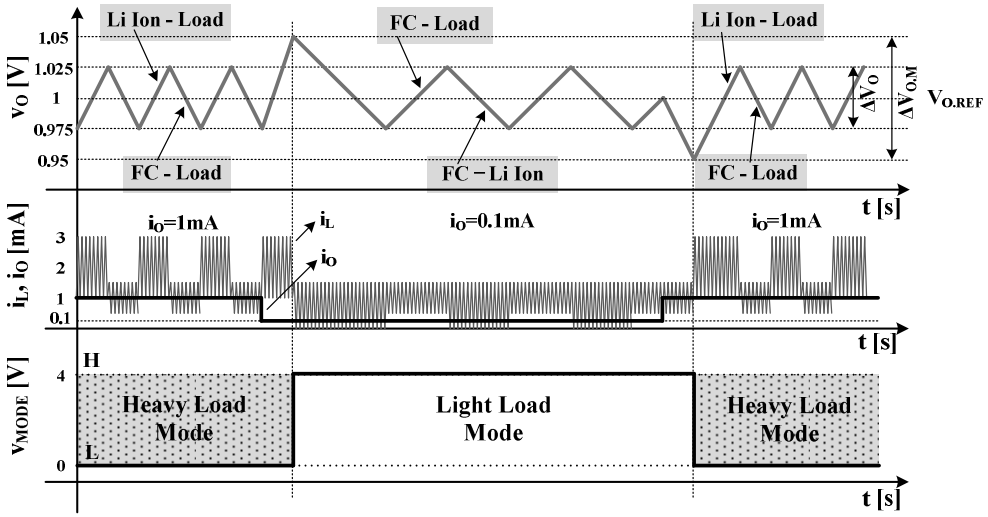


Figure 4.7. Time-domain output-voltage, load-current, and mode-voltage waveforms in light- and heavy-load modes and across rising and falling load-dump transitions.

4.2.3. Stability

4.2.3.1. Light Loads

In LLM, when the system steers FC power P_{FC} into v_O and V_{LI}, CMP_I regulates i_L to I_{FC} at $f_{I.SW}$, so L_E is practically a $D_O I_{FC}$ current source at and below $f_{O.SW}$ (because $f_{I.SW}$ is higher than $f_{O.SW}$), where D_O is the switching duty cycle that the current loop sets for S_O. CMP_V, as a result, regulates v_O by determining how often to direct FC-derived current $D_O I_{FC}$ to v_O, as Fig. 4.8 shows, where CMP_V's $v_{O.SW}$ sets load-FC connectivity ratio $r_{LD/FC}$. Since V_{LI} is an unregulated low-impedance source, V_{LI} and its connectivity to L_E have no impact on the dynamics of the loop controlling v_O. Accordingly, in LLM, the MIMO system reduces to a single-input (V_{FC}), single-output (v_O) converter, where cross regulation does not apply.

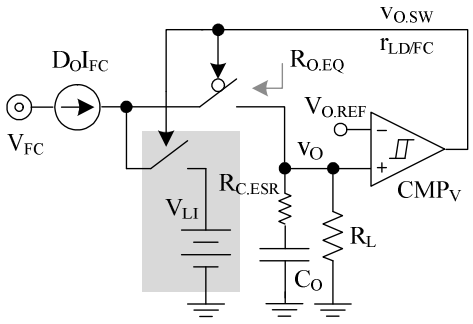


Figure 4.8. Small-signal equivalent circuit in LLM.

4.2.3.2. Heavy Loads

In HLM, the converter directs FC and Li-Ion power P_{FC} and P_{LI} into v_O in alternate switching cycles according to CMP_V's $v_{O.SW}$, which defines FC-load connectivity ratio $r_{FC/LD.H}$ and its complement Li Ion-load connectivity ratio $r_{LI/LD.H}$ (or $1 - r_{FC/LD.H}$). Again, because CMP_I regulates i_L at $f_{I.SW}$ to I_{FC} or I_{LI}, depending on the source used, L_E is a current source equal to boost-equivalent $D_O I_{FC}$ in the FC cycle and buck-equivalent I_{LI} in the Li-Ion counterpart, as Fig. 4.9 illustrates.

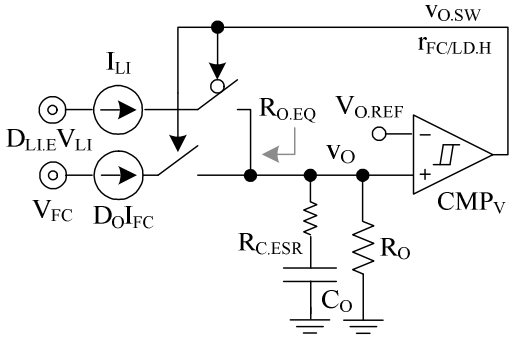


Figure 4.9. Small-signal equivalent circuit in HLM.

Note that boosting V_{FC} to v_O does not introduce a right-half-plane (RHP) zero like a conventional boost converter would because $r_{FC/LD.H}$ is the only control variable to v_O. The reason a RHP zero exists in boost converters in the first place is because the system modulates L_E's de-energizing duty cycle (D_O) to regulate v_O [27], and the current loop in this case switches S_O to regulate i_L to I_{FC} or I_{LI} irrespective of v_O, which means variations in v_O do not affect S_O's duty cycle D_O.

4.2.4. Switch-Control Logic

CMP_I, CMP_V, and CMP_M's binary outputs $v_{I.SW}$, $v_{O.SW}$, and v_{MODE} determine the state of all the NMOS (S_{FC}, S_O, $S_{FC.E}$, $S_{LI.DE}$) and PMOS ($S_{LI.E}$, $S_{LI.CHG}$) switches in the power stage. In regulating i_L, for example, CMP_I toggles $v_{I.SW}$ up and down at $f_{I.SW}$ to energize and de-energize L_E. CMP_M and CMP_V switch at lower frequency $f_{O.SW}$ to determine from which source L_E should draw energy and to which output L_E should direct it. To this end, CMP_M transitions v_{MODE} high to place the system in LLM, which means L_E draws energy from the FC (and S_{FC} remains closed). In this mode, a low state for CMP_V's $v_{O.SW}$ prompts boost-like switches $S_{FC.E}$ and S_O to energize and de-energize L_E (at $f_{I.SW}$) from the FC into v_O. A high state similarly commands boost-like switches $S_{FC.E}$ and $S_{LI.CHG}$ to energize and direct L_E's energy (at $f_{I.SW}$) from the FC into the Li Ion. When CMP_M's v_{MODE} is low, the system enters HLM, where a low state for CMP_V's $v_{O.SW}$ prompts S_O and buck-like switches $S_{LI.E}$ and $S_{LI.DE}$ to energize and de-energize L_E (at $f_{I.SW}$) from the Li Ion into v_O. A high state here induces S_{FC} and boost-like switches $S_{FC.E}$ and S_O to energize and de-energize L_E (at $f_{I.SW}$) from the FC into v_O. Table 4.1 summarizes the operation just described in Boolean form.

Switch	Equations
S_{FC}	$v_{O.SW} + v_{MODE}$
S_O	$\left(\overline{v_{O.SW}} \cdot \overline{v_{MODE}} + v_{I.SW}\right) \cdot \left(\overline{v_{O.SW}} + \overline{v_{MODE}}\right)$
$S_{LI.E}$	$v_{I.SW} + v_{O.SW} + v_{MODE}$
$S_{FC.E}$	$\left(v_{O.SW} + v_{MODE}\right) \cdot \overline{v_{I.SW}}$
$S_{LI.CHG}$	$\overline{v_{O.SW} \cdot v_{MODE} \cdot v_{I.SW}}$
$S_{LI.DE}$	$\overline{v_{O.SW}} \cdot \overline{v_{MODE}} \cdot v_{I.SW}$

Table 4-1. Switch-control logic equations.

Generally, before control signals reach their respective gate terminals, an 8 kΩ-75 fF delay block and logic introduce dead time between the transitions of interconnecting switches to avoid shoot-through power. During this time, when all switches are momentarily off, body diodes conduct i_L and, in so doing, ensure L_E's conduction path is never disrupted. Once $S_{LI.E}$'s gate-control signal $G_{LI.E}$ trips low, for example, $S_{LI.E}$ does not engage until after a delay after S_{FC} and $S_{LI.DE}$'s gate-control signals G_{FC} and $G_{LI.DE}$ transition low, during which time $S_{LI.DE}$'s body diode conducts.

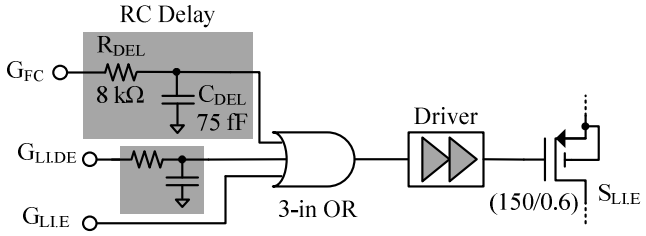


Figure 4.10. Dead-time control circuit.

4.3 IC Implementation

To validate the proposed charger-supply, an IC prototype was designed, fabricated, and tested using AMI's 0.5-μm CMOS process. As depicted in Fig. 4.1, power inductor L_E, fuel-cell capacitor C_{FC}, output capacitor C_O, and current-sense resistor R_S are off chip while power switches S_{FC}, $S_{LI.DE}$, $S_{LI.E}$, $S_{LI.CHG}$, $S_{FC.E}$, and S_O; logic and dead-time-control drivers; current, voltage, and mode comparators CMP_I, CMP_V, and CMP_M; current sensing amplifier A_I; and a biasing block are on chip (and supplied from Li-Ion voltage V_{LI}). Since the FC is more efficient when supplying dc current, the controller was designed to operate in continuous-conduction mode (CCM) [15]. In addition, to mitigate design risk (and noise) and concentrate on functionality, R_S senses i_L, rather than a noisier but less lossy sample-and-hold sense-FET circuit.

4.3.1. Power Stage

Given V_{FC} and v_O are relatively low at 0.5 – 0.7 V and 1 V, NFETs implement switches S_{FC}, S_O, $S_{LI.DE}$, and $S_{FC.E}$ (Fig. 4.11); PFETs implement $S_{LI.E}$ and $S_{LI.CHG}$ because they link to the highest voltage: V_{LI}. In sizing the switches, consideration for parasitic capacitances outweighed those for resistances because gate-drive losses at low power levels (below 1 mA) and higher switching frequencies (at roughly 2.5 MHz) dominate over conduction losses. As such, the aspect ratios for S_{FC}, $S_{LI.DE}$, $S_{FC.E}$, and S_O are 75/0.6 μm/μm and $S_{LI.E}$ and $S_{LI.CHG}$ are 150/0.6 μm/μm.

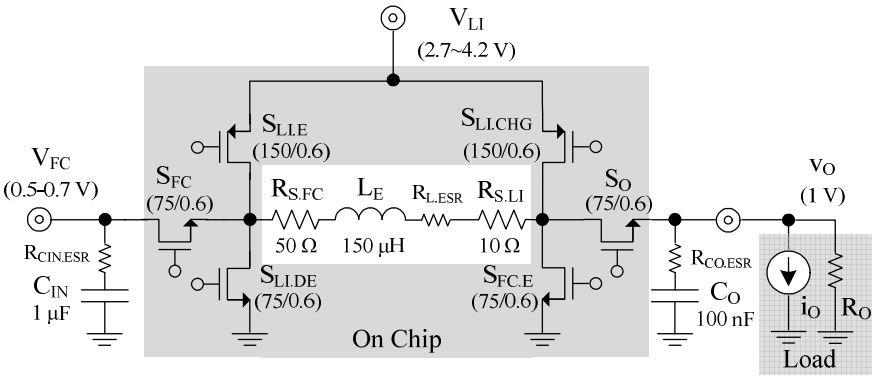


Figure 4.11. Prototyped power stage.

Because the FC has limited power range and response time, the circuit keeps ripple Δi_L low with a large L_E. Considering co-packaging L_E with the IC is important, L_E should also conform to a small footprint, which is why L_E is a 6.6 mm × 4.5 mm × 2.9 mm 150-μH surface-mount ferrite-core power inductor with 2 Ω of ESR. Because switching losses dominate, the design favors high L_E over low ESR because a lower ESR would only be possible with a lower L_E when constrained in volume. With L_E, V_{FC}, V_{LI}, and V_O set and CMP_I's hysteresis down to its lowest possible level, the current loop switches at roughly 2.5 MHz ($f_{I.SW}$). Δi_L is nevertheless considerable at 1 – 2 mA so the system uses a 1-μF tantalum capacitor (C_{FC}) to suppress the power variation the FC experiences on a cycle-by-cycle basis. At v_O, 100 nF (2 mm × 1 mm × 1 mm) slows v_O sufficiently to ensure $f_{I.SW}$ stays well above the system's $f_{O.SW}$. Recall that keeping v_O's regulation $f_{O.SW}$ below i_L's $f_{I.SW}$ allows the converter to perceive L_E as a current source.

4.3.2. Hysteretic Current Loop

The prototype splits current-sensing resistor R_S into $R_{S.FC}$ and $R_{S.LI}$ (and connects one or the other into A_I with M_{NFC1}-M_{NFC2} and M_{NLI1}-M_{NLI2}, as shown in Fig. 4.12) to ease A_I's ICMR requirements and keep noise injection low. When drawing energy from the FC, $R_{S.FC}$ remains attached to V_{FC} so $R_{S.FC}$'s terminal voltages hover at 0.5 – 0.7 V, which also means $R_{S.FC}$'s terminals do not generate switching noise for A_I to amplify. Placing $R_{S.LI}$ on the other side of L_E accomplishes similar results when deriving power from the Li Ion because $R_{S.LI}$ remains attached to v_O, keeping $R_{S.LI}$'s terminal voltages at 1 V (with a small ripple). A side benefit of splitting R_S in two is flexibility because $R_{S.FC}$ and $R_{S.LI}$ can independently and flexibly define i_L's regulation targets I_{FC} and I_{LI} with only one reference voltage $V_{I.REF}$:

$$V_{I.REF} \approx I_{FC}R_{S.FC}|A_I| = I_{LI}R_{S.LI}|A_I|, \tag{4-4}$$

so a 5-to-1 ratio between $R_{S.FC}$ and $R_{S.LI}$ sets I_{LI} to $5I_{FC}$. In other words, an $R_{S.FC}$ of 50 Ω, $R_{S.LI}$ of 10 Ω, A_I of –25 V/V, and $V_{I.REF}$ of 625 mV set I_{FC} and I_{LI} to 0.5 and 2.5 mA, respectively. This design flexibility was important to test the prototype fully.

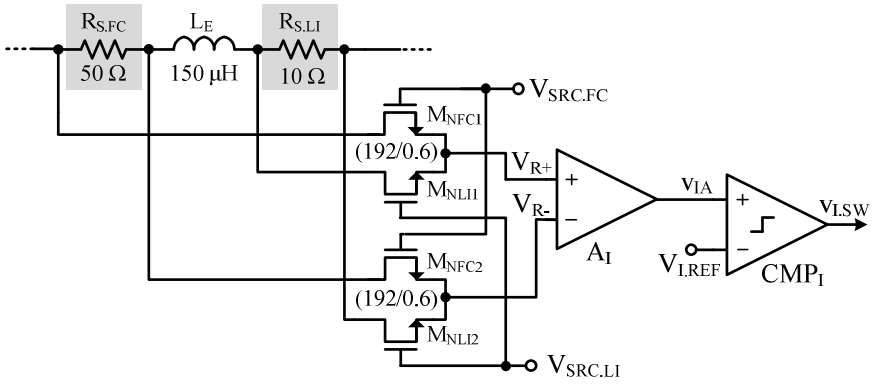


Figure 4.12. Inductor current-sensing circuit.

Differential amplifier A_I consists of a p-type differential pair loaded with an n-type mirror and cascaded with a Miller-compensated second stage (Fig. 4.13). The operational amplifier is in an inverting configuration where resistor ratio R_B/R_A sets the gain to –25 V/V. External tuning voltage V_{TUNE} connects to A_I's non-inverting input to attain a gain of one and raise A_I's output v_{IA} high enough to keep v_{IA} within the ensuing comparator's ICMR:

$$v_{IA} \approx (v_{R-} - v_{R+})A_I + V_{TUNE}\left(\frac{R_A}{R_A + R_B}\right)\left(\frac{R_A + R_B}{R_A}\right)$$

$$= (v_{R-} - v_{R+})\left(-\frac{R_B}{R_A}\right) + V_{TUNE}. \qquad (4\text{-}5)$$

To follow L_E's fast changing current i_L, which switches at roughly 2.5 MHz, A_I needs 875 μA. A_I feeds a comparator (Fig. 4.13) whose p-type mirror-loaded input drives a common-source amplifier. The amplified current-sense voltage v_{IA} is compared to the reference $V_{I.REF}$ fed from the outside, and the comparator CMP_I generates $v_{I.SW}$ to decide either to energize or de-energize the inductor. As CMP_I should also be fast to track the fast i_L, it was designed with relatively smaller transistors, sacrificing the accuracy for the speed.

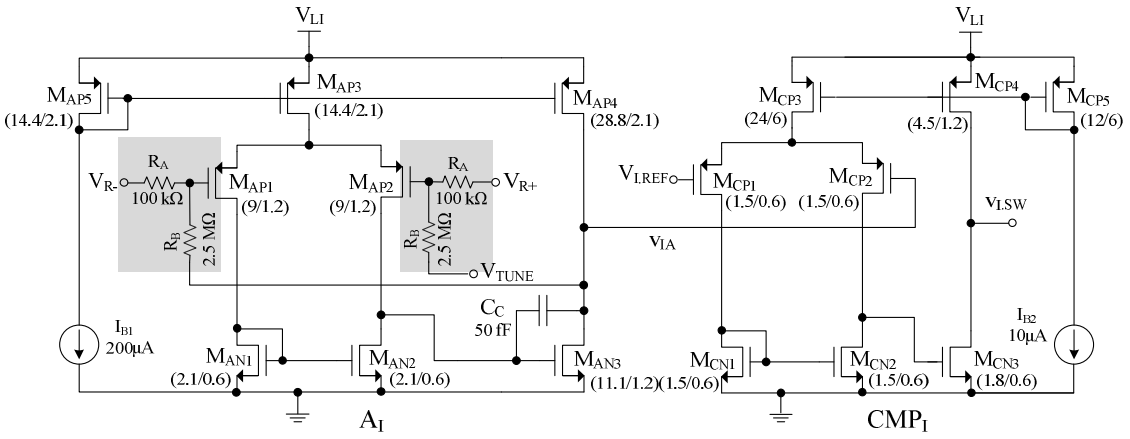


Figure 4.13. Current-sense amplifier A_I and the regulating comparator it drives.

4.3.3. Nested Hysteretic Voltage Loop

Since both voltage-loop comparators CMP_V and CMP_M produce hysteresis and sense v_O, they share ICMR and bandwidth requirements, which is why their circuit topologies resemble. In particular, p-type input pairs feed a latching load whose positive feedback gain determines the circuit's hysteresis (Fig. 4.14). A folding class-AB gain stage follows to produce the rail-to-rail (binary-like) signal that feeds the switch-control logic. CMP_V and CMP_M only differ in that the latter produces a wider hysteretic window so CMP_M's positive feedback gain exceeds CMP_V's. As a result, mirror ratios M_{CN3}/M_{CN1} and M_{CN4}/M_{CN2} are greater in CMP_M at 2.1/1.2 µm/µm than in CMP_V at 2.1/1.65 µm/µm, producing hysteretic windows of 100 and 50 mV, respectively. Incidentally, these two nested hysteretic windows must, by design, correlate so the layout implementations of M_{CN1} – M_{CN4} must match accordingly (i.e., be close and surrounded by dummy devices in a common-centroid and cross-coupled configuration).

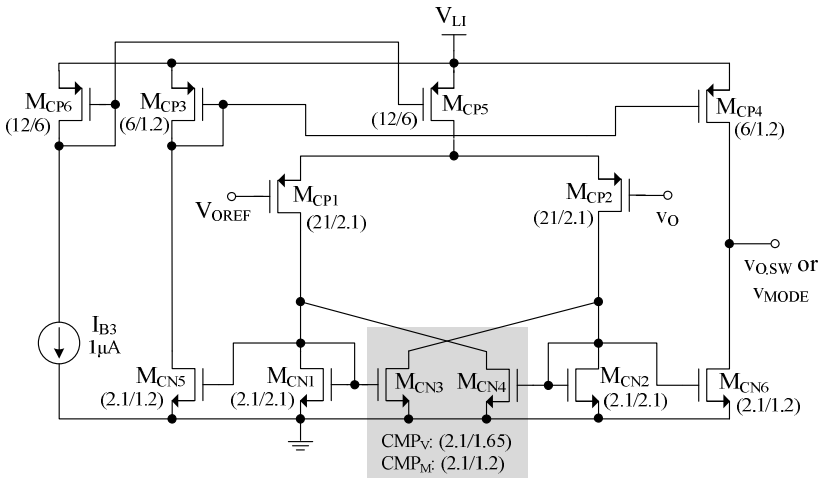


Figure 4.14. Schematic for output-voltage and mode-controlling comparators CMP_V and CMP_M.

4.3.4. Bias Circuit

A PTAT (proportional to absolute temperature) current bias generator is used to generate 1 μA and 10 μA's bias currents to run the comparators and the amplifier. Fig. 4.15 shows the schematic of the current bias circuit, where a PTAT current is generated by the voltage difference between the two differently-sized diodes D_1 and D_2:

$$I_{BIAS} = \frac{1}{R_{BIAS}} \frac{kT}{q} \ln \frac{1}{N} \tag{4-6}$$

N is the ratio of the size of two diodes, which is 8 in this design, and a 100 kΩ resistor is used to generate the seed current of 1 μA. A long-channel PMOS transistor M_{BPS} feeds a small current to start up the circuit correctly for the case when the positive feedback loop latches the circuit to the undesired state.

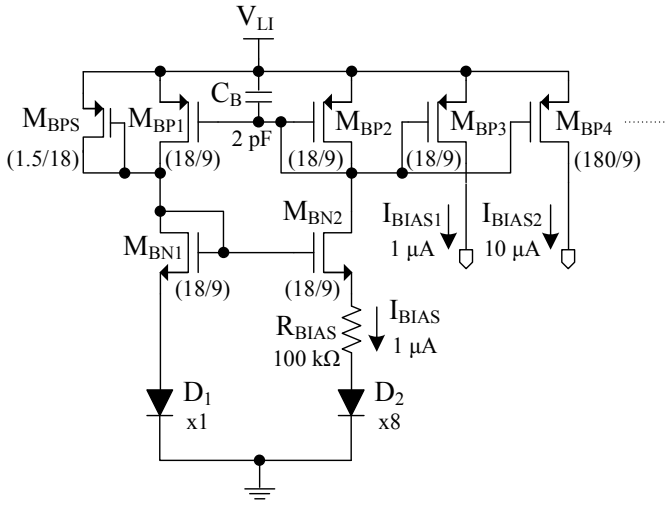


Figure 4.15. PTAT Current Bias Circuit.

4.3.5. Startup

When the system first starts, v_O is zero so both voltage-loop and mode comparators CMP_V and CMP_M in Fig. 4.1 force their respective outputs $v_{O.SW}$ and v_{MODE} to start at a low state, prompting the converter to enter HLM and to source power from the Li Ion. In this state, the circuit continually sources Li-Ion power so v_O necessarily rises. Once v_O surpasses CMP_V's upper threshold, the system downshifts to FC power. If the load exceeds this power, v_O falls to CMP_V's lower threshold and ripples about $V_{O.REF}$ in steady state (in HLM). Otherwise, if the load is light, v_O continues to rise with FC power to CMP_M's upper threshold, at which point the system enters LLM and allows CMP_V to steer FC power away from v_O until v_O reaches steady state. Although starting a power supply with its maximum-rated power is typically not advisable (because the sudden inrush of i_L may damage the power stage), power levels in this design are always low so the devices were able to accommodate all relevant power levels.

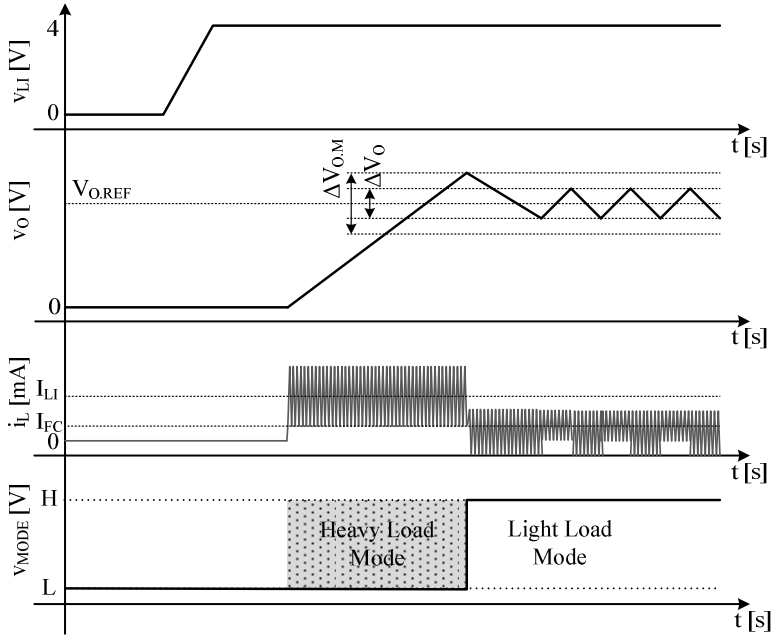


Figure 4.16. Startup waveforms.

4.4 Performance and Limitations

Fig. 4.17 shows the die photograph of the 0.5-μm CMOS (AMI) IC fabricated and its accompanying printed-circuit-board (PCB) prototype. The die occupied 1.0 mm × 0.5 mm of silicon area with the power devices using roughly 12%. To focus on proof of concept, the IC did not include short-circuit protection or battery-charging functions and two external supplies at 0.5 – 0.7 V and 2.7 – 4.2 V emulated the FC and the Li Ion, respectively.

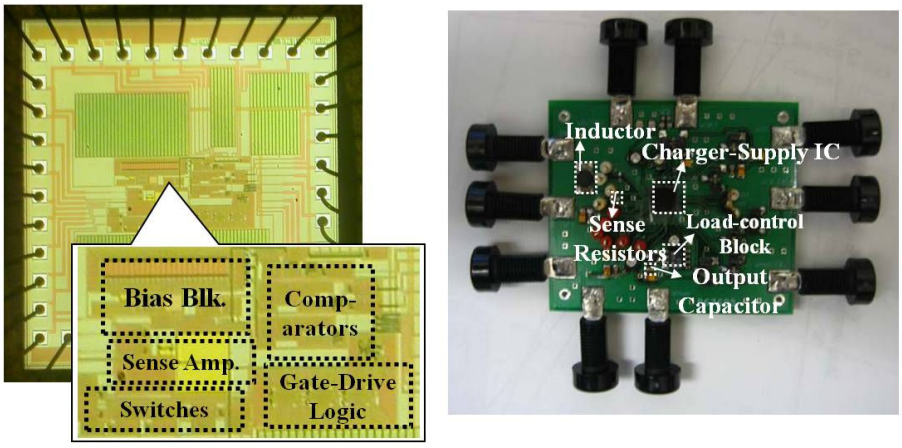


Figure 4.17. 0.5-µm CMOS IC die photograph and corresponding PCB.

4.4.1. Current Regulation

Fig. 4.18a-c shows that the converter switches at roughly 2.5 MHz ($f_{I.SW}$) to regulate i_L through all energy-flow paths. When drawing energy from the FC and directing it to v_O, i_L ripples at 1 ± 0.5 mA, and when channeling current into the Li Ion, i_L ripples at 0.25 ± 0.75 mA, off its 1 ± 0.5 mA target. The reason for the disparity is i_L's falling rate when connected to the Li Ion is faster at $(V_{FC} - V_{LI})/L_E$ than its counterpart at $(V_{FC} - V_O)/L_E$ (when attached to the load) so the propagation delay across CMP_I produces a larger hysteresis (and offset) for the faster rate. This is a drawback because the momentary negative current that results (which peaks at –0.5 mA) discharges the battery. When steering power from the Li Ion into v_O, i_L ripples at 2 ± 1 mA, which is slightly off its 2.5 ± 1-mA mark because of, again, delay mismatches. Since fig. 4.19 demonstrates v_O is stable, integrated substrate and signal-propagation noise through the IC and PCB probably accounts for the ringing in the Li Ion-load path's i_L in Fig. 4.18c. Fig. 4.18d further

illustrates the converter in dual-output mode (in LLM) as it switches from supplying the load at 1 ± 0.5 mA to charging the battery at 0.25 ± 0.75 mA. (These waveforms were extracted from $R_{S.FC}$ and $R_{S.LI}$'s terminal voltages.)

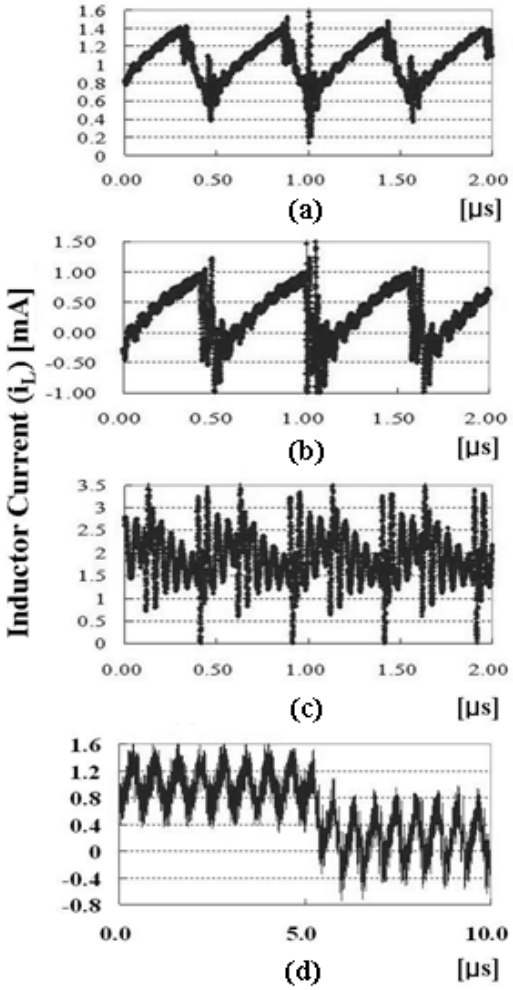


Figure 4.18. Measured inductor-current waveforms through the (a) FC-load (b) FC-Li Ion, and (c) Li Ion-load energy-flow paths and (d) while transitioning from the FC-load to FC-Li Ion paths in dual-output mode (in LLM).

4.4.2. Voltage Regulation

4.4.2.1. Steady State

The prototype regulates v_O within ±25 mV of its target (1 V) with CMP_V in both LLM when i_O is 0.1 mA and HLM when i_O steadies at 1 mA (Fig. 4.19, Table 4-2). Since CMP_M's v_{MODE} determines the converter's mode, a high state indicates the system is in LLM and a low state in HLM. In LLM, the light load discharges C_O slowly so v_O ripples at about 11 kHz. In HLM, the higher i_O discharges C_O faster so v_O ripples at 50 kHz, well below $f_{I.SW}$.

Parameter		Value
Process		AMI 0.5 μm CMOS
Die Area		1.0 x 0.5 mm^2 (342 transistors)
Open-Circuit Fuel-Cell Voltage V_{FC}		0.5 – 0.7 V
Li-Ion Battery Voltage V_{LI}		2.7 – 4.2 V
i_L's Switching Frequency $f_{I.SW}$ [+]		2.5 MHz (nominally)
v_O's Switching Frequency $f_{O.SW}$ [+]		11 kHz (LLM) , 50 kHz (HLM)
Output Voltage v_O (and Δv_O) [+]		1 V ± 25 mV (±2.5 %)
v_O's 0.1 → 1 mA Load-Dump Response [+]		–50 mV (20 μs)
v_O's 1 → 0.1 mA Load-Dump Response [+]		+60 mV (30 μs)
Supply Power P_{DD} at 4 V	A_I [*]	3.5 mW
	CMP_I [*]	242.8 μW
	CMP_V & CMP_M [*]	28.8 μW
	Current Bias [*]	133.1 μW
	Control Logic [*]	1.0 nW
	Gate Drive	1.1 mW
	Total [+]	5.0 mW

[+] Measured [*] Simulated

Table 4-2. IC performance summary.

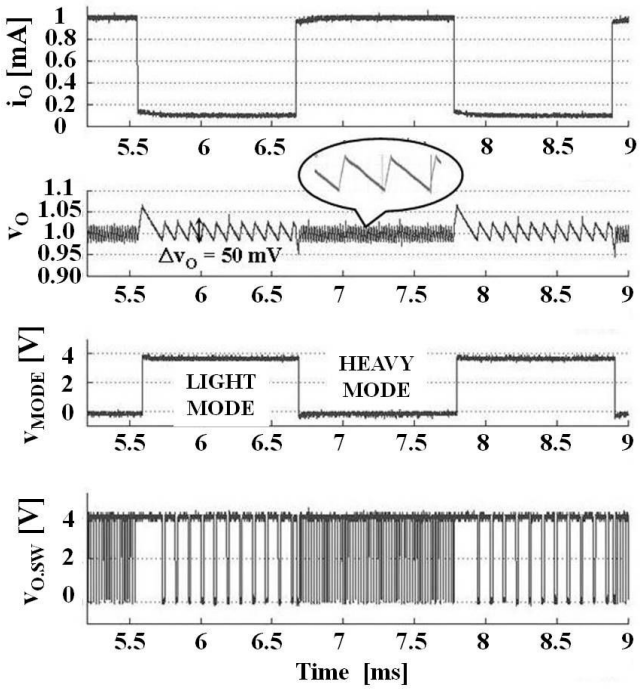


Figure 4.19. Measured output, mode, and path-control voltages in light- and heavy-load modes and across rising and falling loads.

4.4.2.2. Load Dumps and Mode Transitions

During a rising load dump, when i_O suddenly increases from 0.1 to 1 mA, v_O falls to 0.95 V (CMP_M's lower threshold), prompting the system to enter HLM and source Li-Ion power (Fig. 4.20). Similarly, in response to a falling load dump from 1 to 0.1 mA, the converter sources more power than needed and v_O rises to 1.06 V, pushing the converter into LLM, where it draws FC power to both supply the load and charge the Li Ion. These single-cycle response times t_{LH} and t_{HL} (being only functions of i_O, C_O, and CMP_M's delay) are generally faster than those of PWM-based converters, which typically require several switching cycles to recover from severe load dumps [99]. CMP_M's asymmetrical delay, incidentally,

accounts for the slight difference between CMP_M's measured (1.06 V) and expected upper threshold (1.05 V), which represents 1% of V_O. Overall, the system regulates v_O within 2.5% (±25 mV) of its target in steady state and within +6% and –5% (+60 and –50 mV) when subjected to load dumps. The results also show the prototype transitions between LLM and HLM automatically and seamlessly, indicating feedback control is reliable and stable.

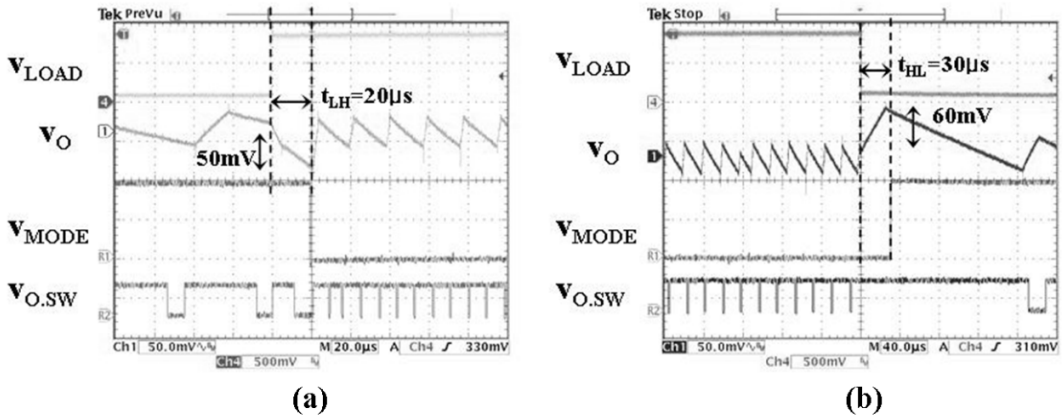


Figure 4.20. Measured close-ups of the output when subjected to (a) rising and (b) falling load dumps.

4.4.3. Efficiency

To understand and decouple the power losses in the system, a separate source (V_{DD}) supplied the controller (i.e., the IC) in these experiments. To this end, Fig. 4.21 shows the simulated input power that the battery and V_{DD} supply as P_{LI} and P_{DD} along with output power P_O and conduction losses P_C up to 10 mA, well above the target of 1 mA. (Fig. 4.21 shows simulation results because decoupling and measuring conduction losses are difficult in practice.) P_{DD}, which represents quiescent and switching gate-drive losses, is constant

across the entire range and dominant below 3 mA because quiescent power and i_L's switching frequency f_{LSW} are independent of i_O (by design) and v_O's switching frequency in HLM is constant at 50 kHz. P_C's contribution and related voltage drops are negligible below 1 mA (because $P_C \propto i_O^2$), which means conduction power is less important than quiescent and switching losses in the targeted load range.

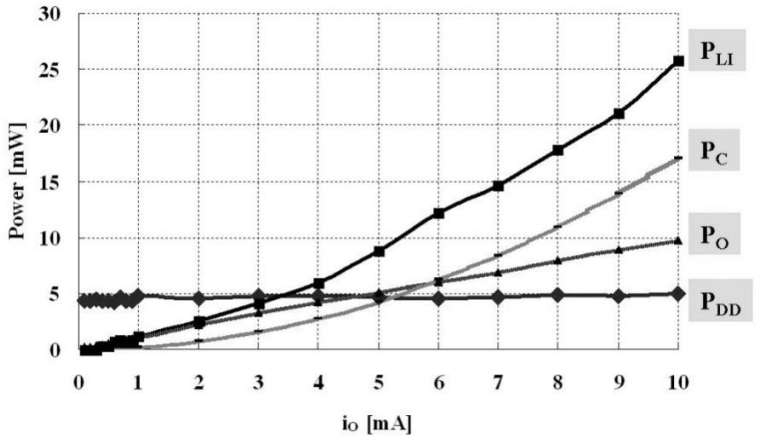


Figure 4.21. Simulated Li Ion-, supply-, output- and conduction-power levels across load.

Fig. 4.22 shows the measured and simulated efficiency results of the converter in LLM (below 0.35 mA) and HLM (above 0.35 mA). While efficiency in LLM (η_{LLM}) is the ratio of the power that reaches v_O (P_O) and charges the battery (P_{CHG}) to the power the FC and V_{DD} deliver:

$$\eta_{LLM} = \frac{P_O + P_{CHG}}{P_{FC} + P_{DD}} = \frac{P_O + P_{CHG}}{I_{FC}V_{FC} + P_{DD}}, \tag{4-7}$$

HLM efficiency η_{HLM} is the ratio of P_O to the power the FC, the battery, and V_{DD} deliver on average as $r_{FC/LD.H}I_{FC}V_{FC}$, $(1 - r_{FC/LD.H})I_{LI}V_{LI}$, and P_{DD}, respectively:

$$\eta_{HLM} = \frac{P_O}{r_{FC/LD.H} I_{FC} V_{FC} + (1 - r_{FC/LD.H}) I_{LI} V_{LI} + P_{DD}}. \quad (4\text{-}8)$$

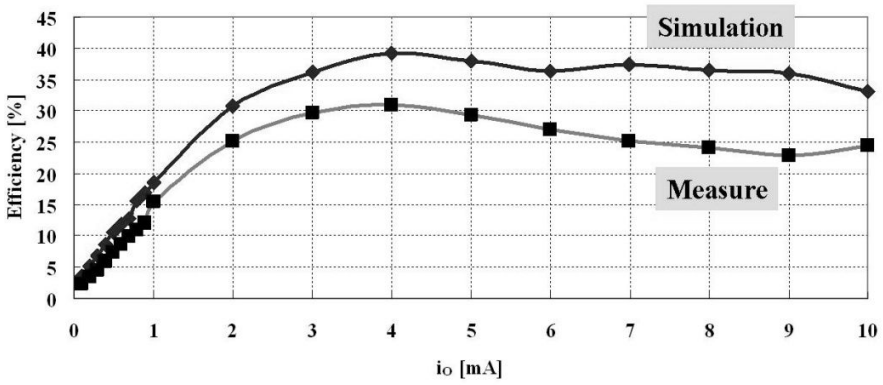


Figure 4.22. Simulated and measured efficiency performance across load.

Experimentally, power losses balance at 4 mA (in HLM), where efficiency peaks at 32%, and as i_O decreases to 0.35 mA, when the converter starts to recharge the battery, efficiency falls below 7%. Efficiency is relatively low because the effects of quiescent and switching losses (P_{DD}) in this region are profound. The design also favored flexibility and testability over converter efficiency to validate functionality (as proof of concept), choosing to operate in CCM for the sake of the FC and sense i_L with lossy sense resistors $R_{S.FC}$ and $R_{S.LI}$ (so P_{DD} exceeds P_{FC}). The efficiency simulated is generally higher than the one measured because the ringing currents observed in Fig. 4.18c dissipate additional power.

While $R_{S.FC}$ and $R_{S.LI}$ increase power losses by about 0.5% in LLM and 3.6% in HLM, the impact of current-sense amplifier A_I (which operates continuously) is worse at 3.5 mW (of the total 5 mW reported in Table 4.2). Replacing $R_{S.FC}$ and $R_{S.LI}$ with sample-and-hold sense FETs [86] would decrease conduction losses and, more importantly, eliminate the

need for A_I, improving efficiency considerably, even if the sense FETs generate switching noise. Additionally, allowing L_E to conduct discontinuously (in DCM) reduces switching losses [91] and the time that the current-sensing network is operational, which combined should advantageously offset the conduction losses a higher peak current ($i_{L(PEAK)}$) would incur. Another benefit of DCM is that L_E can be smaller, which is better for integration. Forcing DCM operation with multiple inputs and outputs is not straightforward, however, especially considering pseudo-DCM techniques are often inefficient [81] and FC peak power would have to increase.

4.5 Summary

The objective of the first IC prototype - the nested hysteretic dual-source charger-supply system – was to implement the single-inductor time-multiplexing control and verify the functionality of the control, which is to deliver a low, average load power from the energy source and a high, peak power from the power source while regulating the output and recharging the power source. The prototype built regulates its output to 1 V within ±25 mV with 150 μH, 100 nF, and 1 μF of off-chip inductance and output and fuel-cell capacitance and responds to rising and falling load dumps of 0.1 – 1 mA within 30 μs, without surpassing a +60/–50-mV window. This precise output voltage control and the tight current control were possible because of the nested hysteretic control, where the faster inner loop regulates the inductor current and the slower voltage loop manages the output voltage within the hysteresis window. Although the functionality of the control has been verified, the prototype suffered from the low efficiency which peaked at 32%, mainly due to high

switching losses and quiescent losses coming from the continuous-conduction-mode operations and series current sensing methods, respectively. Therefore, the objective of the next prototype is to overcome these deficiencies of the first prototype, in the direction that reduces or even eliminates the most dominant power losses by the improved control and circuit designs.

Chapter 5. ESR-derived Nested-Hysteretic Dual-source Charger-Supply System

The fully-hysteretic charger-supply system introduced in the previous chapter was able to draw a low, average power from an energy-dense source and a high, peak power from a power-dense source, and to mix them to either supply a load at 1 V or to recharge the power-dense source with the remnant energy. One important limitation of this system is the low efficiency due to the fact that the converter operates in continuous conduction mode with a high switching frequency and it consumes too much quiescent power in sensing the inductor current. By operating the converter in discontinuous conduction mode and changing the current-control method can greatly save the power and boost the efficiency. In addition, the response time to load variations should be reasonably short so that the converter recovers its output quickly even with high peak-to-average loads. Considering all these, managing the inductor current by hysteretic-controlled, ESR-dominated output in discontinuous conduction mode is both an efficient and compact way of achieving these goals.

5.1 Using ESR in Regulating Inductor Current

The current-sensing method in the fully-hysteretic charger-supply system, which was to use a series sense resistor with an amplifier, claimed substantial power and therefore efficiency. The most common way to sense inductor current is to use a sense FET, which senses a mirrored replica current through a sense FET with a large ratio from a power switch

conducting the inductor current. This method usually needs an additional resistor, a feedback loop and a comparator to convert the inductor current into a voltage and generate a control signal. However, considering the fact that the ESR in the output capacitor already has the inductor current information converted into a voltage, the hysteretic output-voltage control can be an easy and simple way of controlling the inductor current, not requiring any error amplifier or sense resistors and therefore greatly reducing the circuit complexity.

In order to directly control the inductor current from the output voltage, there should be assumption that the converted inductor current dominates the variations in capacitor voltage. The output capacitor can be modeled as a series connection of a resistor and a capacitor. Through this output capacitor, only the ac portion of the inductor's output current flows, while the dc portion flows into the load. Then the ESR and the capacitor portion of the output voltage become

$$v_{ESR} = \Delta i_O R_{ESR}, \tag{5-1}$$

$$v_C = \frac{1}{C_O}\int i_O dt = \frac{1}{8}\frac{\Delta i_O T_{SW}}{C_O}, \tag{5-2}$$

where v_{ESR} and v_C are the ESR and capacitor's portion of the output voltage, Δi_O is the ripple of the load current, R_{ESR} is the ESR, C_O is the output capacitor, and T_{SW} is the switching frequency. Then, the condition for ESR-dominant inductor-current control becomes that v_{ESR} should dominate v_C :

$$R_{ESR} > \frac{1}{8}\frac{T_{SW}}{C_O}. \tag{5-3}$$

To force this condition under parameter variations, an additional series resistor is often required.

The idea to control inductor current from the output voltage's ripple is the basis of all ripple-based switching regulators, which include hysteretic regulators and constant-on-time ripple regulators [100]. Other than the merit of reduced circuit complexity, the ripple-based switching regulators have in general fast response to transient perturbations, when compared to PWM-controlled switching regulators, because they do not require error amplifier and feedback compensation related to it. However, their switching frequencies usually show high dependency on the parameters such as output capacitor, propagation delay, and input / output voltages. In addition, due to the variations in parameters, their dc output regulation performances are sometimes lower than those of PWM counterparts. High susceptibility to noise and jitter is another shortcoming of the ripple-based converters, because the ESR can easily catch the ambient electromagnetic noise and directly affect the feedback node.

5.2 Power Stage and Energy Flow

The switched-inductor charger–supply in Fig. 5.1 is similar to the system introduced in the previous chapter in the sense that it draws power from both an energy-dense source v_{ED} and a power-dense rechargeable device v_{PD} to supply a load. Also, when lightly loaded, the system recharges v_{PD} with excess v_{ED} power. For this, the network connects inductor L_O so it can energize from either v_{ED} or v_{PD} and drain into either the load at v_O or v_{PD}. L_O essentially transfers energy packets between v_{ED}, v_{PD}, and v_O in discontinuous-conduction

mode (DCM), draining L_O fully before re-energizing it from another source (Fig. 5.2.) To list important differences from the previous fully-hysteretic charger-supply system, (1) this system operates in the discontinuous conduction mode, (2) the peak inductor current is controlled by a ESR-dominated hysteretic control, and (3) the switching frequency has been also reduced to less than 2% of the previous system to save switching power.

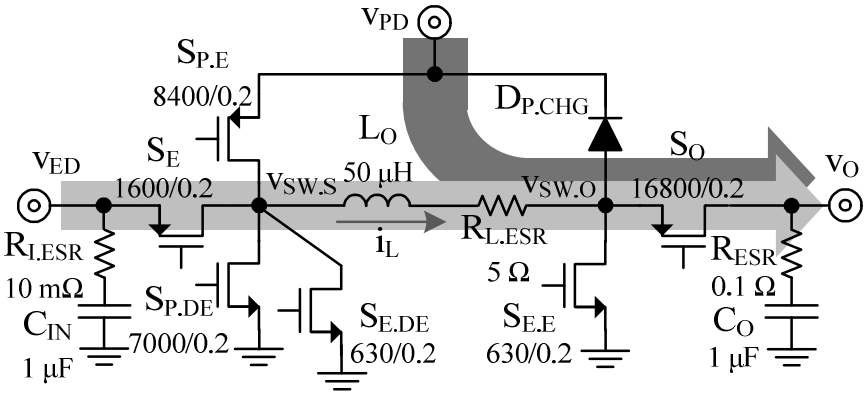


Figure 5.1. Simplified dual-source hysteretic charger–supply system.

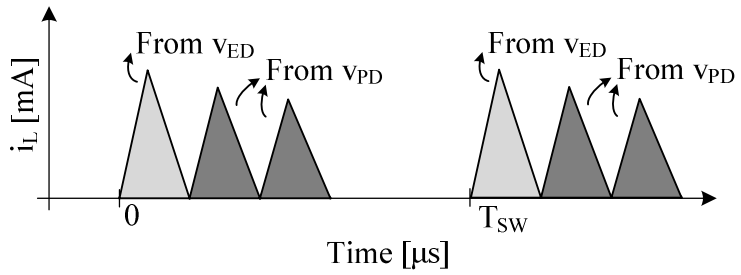


Figure 5.2. Inductor current waveform in heavy loads.

5.3 Switching Sequence

5.3.1. Energy-Dense Phase

The rising edge of an internal 40-kHz clock f_{CLK} starts every switching cycle by drawing and delivering one energy packet E_{ED} from v_{ED} to v_O. For this, switches S_E and $S_{E.E}$ close to energize L_O from v_{ED} across fixed energizing time τ_{EN} to peak L_O's current at $i_{L(PK).ED}$ in Fig. 5.3. S_E and $S_{E.E}$ then open and $S_{E.DE}$ and S_O close to drain L_O into v_O until CP_{IOZ} in Fig. 5.4 senses when S_O's voltage nears zero, which corresponds to L_O's current i_L reaching zero. To save energy, CP_{IOZ} operates only when needed, from $v_{E.E}$'s falling edge, after L_O's τ_{EN}, until CP_{IOZ} trips, whose output shuts both $S_{E.DE}$ and CP_{IOZ}.

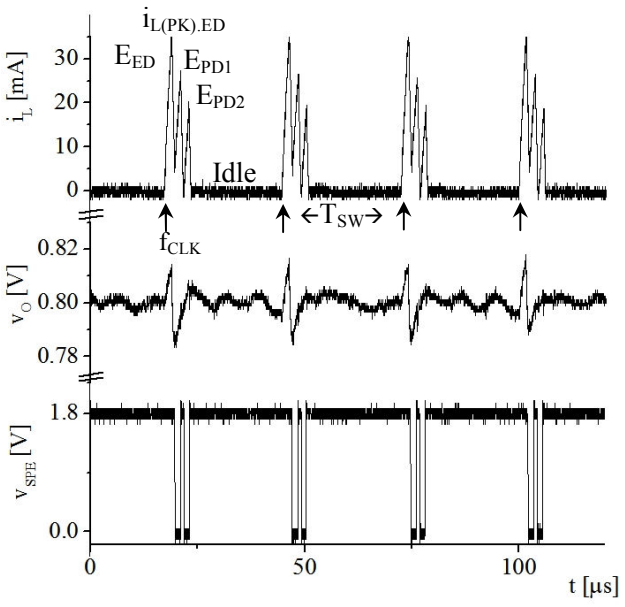


Figure 5.3. Measured current and voltage waveforms when heavily loaded.

5.3.2. Power-Dense Phase

If E_{ED} does not raise v_O above CP_O's upper threshold (above V_{REF}), CP_O's output remains low. This commands the network to energize L_O from v_{PD} immediately after L_O drains E_{ED} into v_O. With S_O already engaged, $S_{P.E}$ closes to energize L_O from v_{PD} to v_O until CP_O trips.

After this, $S_{P.E}$ opens and $S_{P.DE}$ closes to drain L_O into v_O until CP_{IOZ} again senses that L_O's current nears zero. This way, L_O delivers v_{PD} energy E_{PD} to v_O.

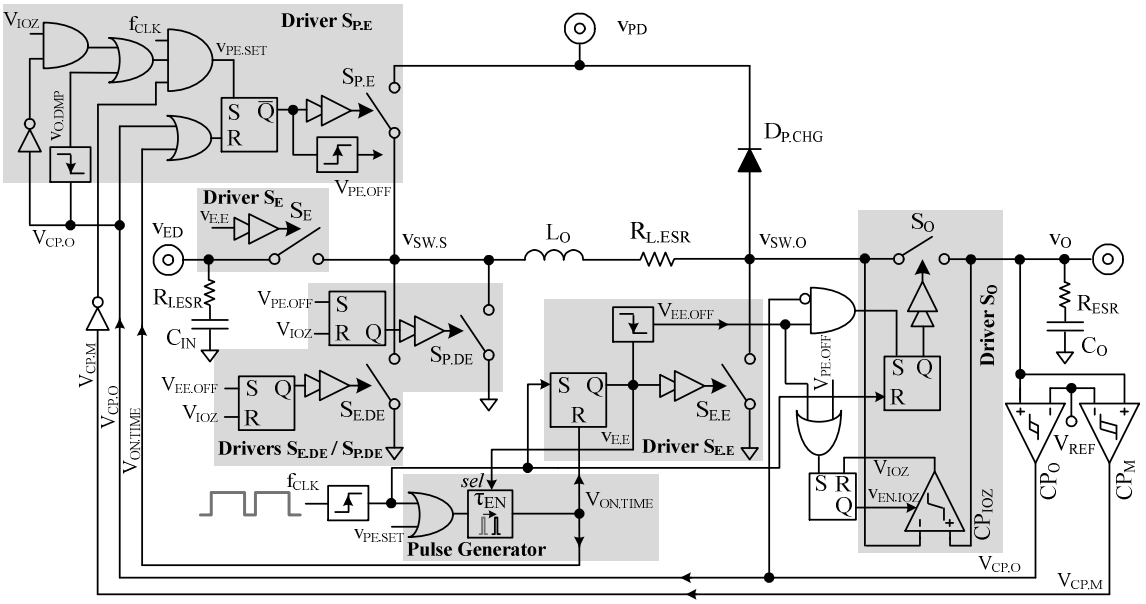


Figure 5.4. Detailed dual-source hysteretic switched-inductor charger-supply system.

If v_O does not rise above CP_O's higher threshold or again drops below CP_O's lower threshold before f_{CLK} rises again, L_O energizes from v_{PD} again and delivers another E_{PD} to v_O, as Fig. 5.5 shows when load current i_O is 2 mA. The system then delivers consecutive packets until it satisfies the load. Once satisfied, v_O does not droop below CP_O's lower threshold and, as a result, the system idles until f_{CLK} rises again to start another sequence. If the system cannot satisfy the load, to avoid conflicting commands, f_{CLK}'s high state keeps the system from initiating additional E_{PD} packets. If this happens, the system is, in essence, sourcing as much power as it can. Note, however, the system waits for i_L to be zero before energizing L_O another time.

5.3.3. Charge Mode

When v_{ED}'s energy packet E_{ED} exceeds the needs of the load, as in Fig. 5.5, v_O rises and reaches CP_O's higher threshold, which disconnects L_O from v_O by shutting S_O. As a result, L_O's remnant energy raises $v_{SW.O}$ until $D_{P.CHG}$ forward-biases and drains L_O into v_{PD}. The system continues to send packets of energy to v_{PD} across cycles until i_O discharges C_O below CP_O's lower threshold. At this point, CP_O trips low to prompt the network to send another E_{ED} to v_O.

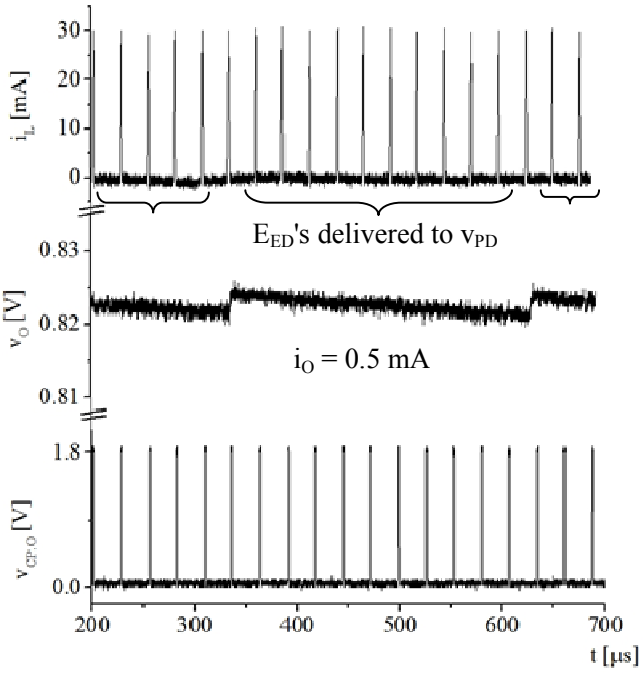


Figure 5.5. Measured current and voltage waveforms in charge mode.

5.4 Feedback Control

Every clock cycle prompts L_O to draw an energy packet E_{ED} from v_{ED} (Fig. 5.6.) CP_O determines where to drain L_O (to v_O if below CP_O's lower threshold or to v_{PD} otherwise) and

whether or not L_O should draw supplementary power from v_{PD} (if v_O remains low after E_{ED}). Comparator CP_M determines which mode to engage: supply v_O if v_O falls below CP_M's lower threshold or charge v_{PD} if v_O rises above CP_M's upper threshold. Therefore, when v_O falls below both lower thresholds, L_O draws energy from v_{ED} and v_{PD} to supply v_O. When v_O rises above CP_O's upper threshold, L_O stops drawing energy from v_{PD}, and when above CP_M's upper threshold, L_O recharges v_{PD} with part or all of E_{ED}. In other words, the system adjusts L_O's connectivity to regulate v_O.

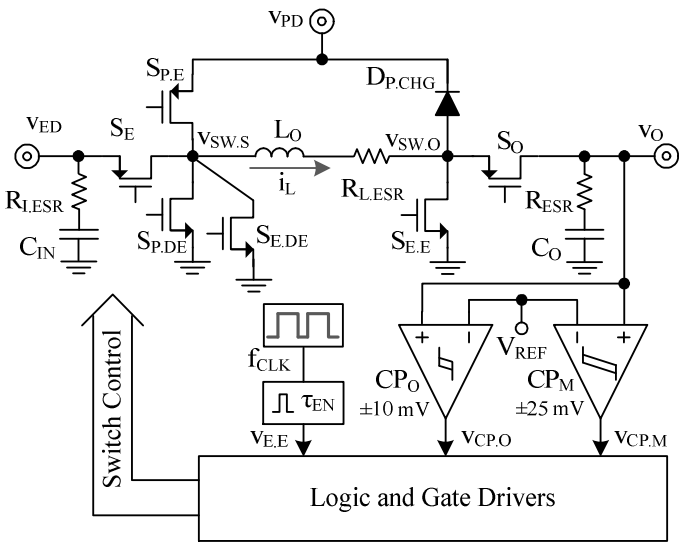


Figure 5.6. Simplified control circuit.

Transfer inductor L_O and output capacitor C_O in dc–dc converters introduce two poles p_L and p_C to the feedback loop that regulates v_O, and if L_O disconnects from v_O at any time, also a right-half-plane zero z_{RHP}. Here, however, energizing and draining L_O from and to 0 A in discontinuous conduction ensures the average voltage across L_O is zero across L_O's conduction time, so L_O's p_L disappears [101]. Plus, fully draining L_O into v_O keeps feed-forward signals from inverting v_O, so z_{RHP} also disappears [101]. And because R_{ESR} limits

how much current C_O can shunt, R_{ESR} eventually cancels the effects of p_C, which means R_{ESR} introduces a left-half-plane zero z_{LHP}. This system is therefore widely stable, because the power stage includes no other low-frequency poles than p_C and z_{LHP} recovers phase.

In this case, L_O supplies E_{ED} from v_{ED} and supplementary energy E_{PD} from v_{PD} to v_O when heavily loaded. Because L_O draws the same energy E_{ED} from v_{ED} every switching cycle T_{SW}, v_{ED} supplies a fixed amount of charge across T_{SW}. This means v_{ED} supplies a "constant" current to v_O, so neither v_{ED} nor its E_{ED} affect the feedback dynamics of the system.

5.4.1. Heavy Loads

In heavy mode, the system regulates v_O by adjusting the number of E_{PD} energy packets that L_O draws from v_{PD}. Several E_{PD}'s across T_{SW} amount to a variable current source i_l whose peak $i_{l(pk)}$ CP_O controls. If the voltage across R_{ESR} overwhelms that of C_O, v_O rises with i_l after each E_{PD} until i_l satisfies the current that produced Δv_O in the first place: $\Delta v_O/R_{ESR}$, so i_l rises until it peaks at v_o/R_{ESR} or $i_{l(pk)}$ in peak-current mode [102].

Since the current v_O receives as i_o across T_{SW} is the charge several E_{PD}'s supplied across conduction time t_C over T_{SW}, i_o is $i_{l(pk)}t_C/T_{SW}$. In other words, L_O supplies i_o to C_O and its R_{ESR}, load R_O, and L_O's equivalent output impedance in discontinuous-conduction mode Z_{LO} [101], as Fig. 5.7a depicts. As the signal-flow graph of Fig. 5.7b further illustrates, R_{ESR} sets $i_{l(pk)}$; t_C determines i_o; R_{ESR}, R_O, and C_O establish p_C; and R_{ESR} and C_O introduce z_{LHP} in loop gain A_{LG}:

$$A_{LG} = \left(\frac{1}{R_{ESR}}\right)\left(\frac{t_C}{T_{SW}}\right)\left\{\frac{(R_O \parallel Z_{LO})(1+sR_{ESR}C_O)}{1+s\left[(R_O \parallel Z_{LO})+R_{ESR}\right]C_O}\right\}. \quad (5\text{-}4)$$

Here, t_C is the conduction time across one energizing and de-energizing sequence of L_O times the number of packets drawn, neither component of which introduces poles or zeros. Z_{LO} represents how much L_O's current i_L changes in response to variations in v_O when excluding the effects of the feedback loop, which reduces to $2L_OT_{SW}/(D't_C)^2$, as [101] demonstrates, where D' is $(1\text{-}V_O/V_{PD})$.

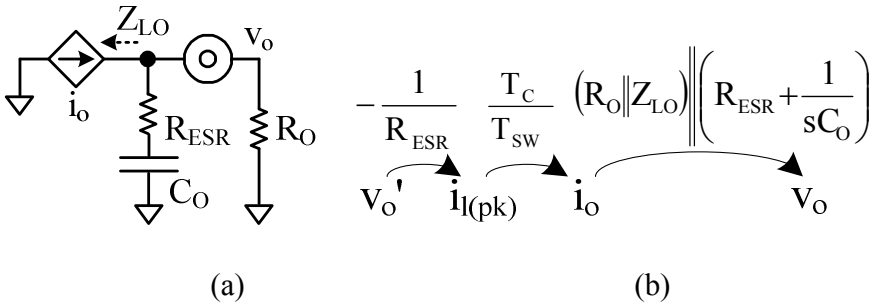


Figure 5.7. Equivalent small-signal (a) circuit and (b) signal-flow graph.

5.4.2. Light Loads

When lightly loaded, CP_O determines which output should receive v_{ED}'s energy packet E_{ED}. As such, L_O delivers E_{ED} to v_O whenever v_O falls below CP_O's lower threshold and to v_{PD} otherwise. In delivering one E_{ED} across T_{SW}, L_O supplies constant current. In other words, L_O is a current source that CP_O directs into either v_O or v_{PD}. This means, like before, that C_O establishes the dominant low-frequency pole of the system and its R_{ESR} is a phase-saving zero. Note v_{PD} is an unregulated low-impedance output that absorbs excess v_{ED} power.

5.4.3. Mode Transitions

When i_O changes so that v_O goes out of the steady-state regulation range and reaches CP_M's thresholds, the converter changes its mode. For example, when the converter is in Light mode and the load power p_O increases over P_{ED}, v_O continues to decrease until it hits the CP_M's lower limit. Then with the next clock's rising edge, the system enters Heavy mode, where the power source v_{PD} starts to supply v_O to bring it back to V_{REF}. When the converter is in Heavy mode and p_O suddenly decreases below P_{ED}, then v_O starts to rise even without v_{PD} and it does not trigger additional energizing event from v_{PD}, and goes into Light mode where v_O automatically settles in the regulation window defined by CP_{LT}, sharing P_{ED} into v_O and v_{PD}. These mode transitions are synchronized with either the clock's rising edge or i_L's zero current conditions to avoid overlaps in energizing sequences.

5.5 IC Implementation

5.5.1. Power Stage

The proposed single-inductor charger-supply IC was designed in 0.18-µm BiCMOS process. Switch S_{PE} and S_{PCHG} were chosen to be PMOSs as they interface with the system's highest voltage V_{PD} (Fig. 5.1.) S_{ED} and S_O are also PMOSs for lower losses with the higher gate drive voltages, and S_O has a back-to-back diode to block any reverse current. S_{DE} and S_E are NMOSs as they connect to ground and are easier to drive with the system's supply voltage – v_{PD}.

5.5.2. Output Hysteretic Comparator

The hysteretic comparator CP_O regulates v_O by deciding where to put i_L's energy, either to v_O or v_{PD} from v_O's level in Light mode, and also effectively regulates the inductor current

by ESR-dominant output (Fig. 5.8.) $v_{EN.LT}$, the enable signal of CP_O, becomes high only for τ_D-shifted S_{ED}'s energizing duration, to save power. The first stage of CP_O consists of a NMOS input pair with latched PMOS loads to generate hysteresis (±10 mV), the amount of which depends on the relative strength of the latched and diode-connected transistors on the first stage.

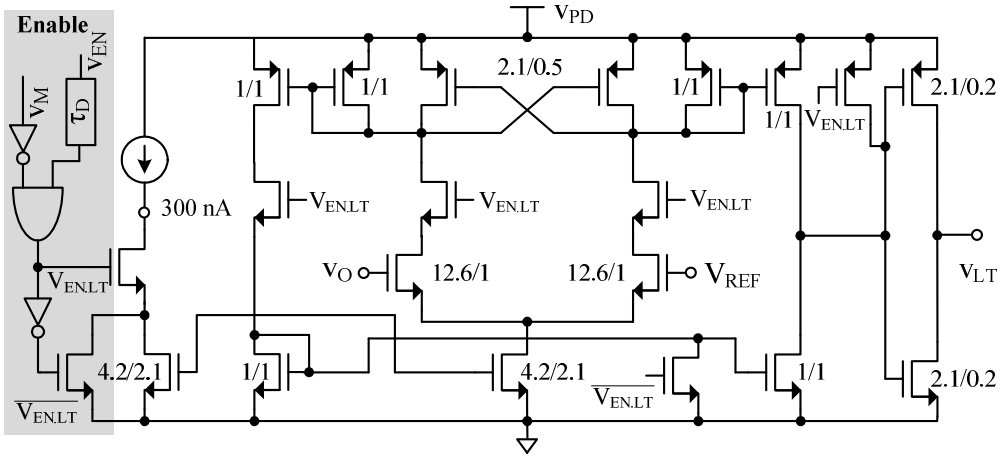


Figure 5.8. Output Hysteretic Comparator CP_O.

5.5.3. Diode-emulating Circuits

The comparators CP_{IOZ} and CP_{IPZ} block the negative i_L by comparing both terminals of the switch S_O and S_{PCHG}. CP_{IOZ} turns on with S_O's control signal, and at that moment, v_{IOZ} is low because v_{SWO} is higher than v_O. As i_L decreases below zero, v_{SWO} goes below v_O, flipping v_{IOZ} to high. When v_{IOZ} goes high, it turns off S_O and disables its own comparator CP_{IOZ} by SR latch and waits for the next energizing cycle. To avoid deglitch during turn-on transients, v_{IOZ} activates after 100 ns' deglitch time with 50-fF capacitor.

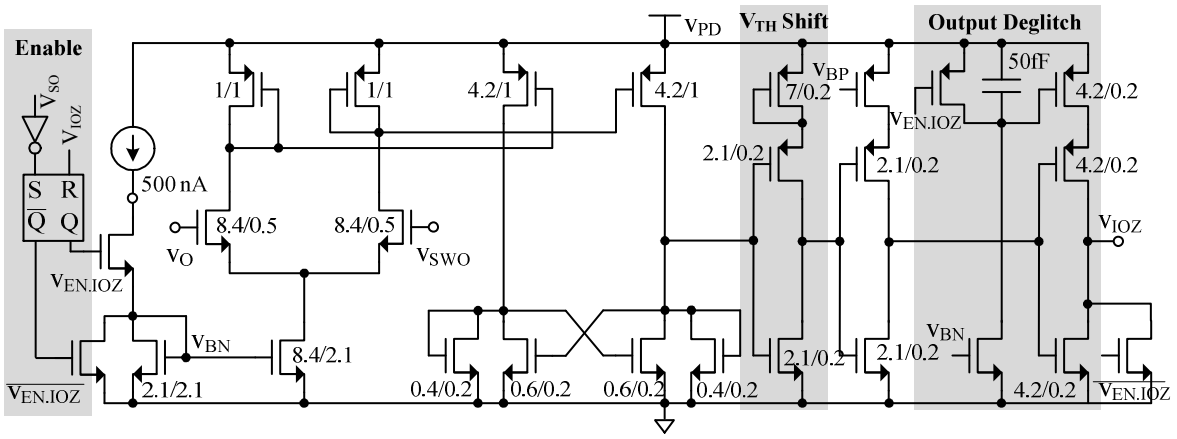


Figure 5.9. Zero-Current-Detecting Comparator CP_{IOZ} for the Output v_O.

Another comparator CP_{IPZ} detects zero i_L to v_{PD} through the switch S_{PCHG} (Fig. 5.10.) This has common-gate PMOS inputs with different dimensions to create an intentional offset and therefore be more effective in blocking faster negative i_L. This comparator turns on with S_{PCHG}'s control signal, and similarly turns off with its output v_{IPZ} going high when v_{SWO} falls below v_{PD} as S_{PCHG} starts to conduct negative i_L.

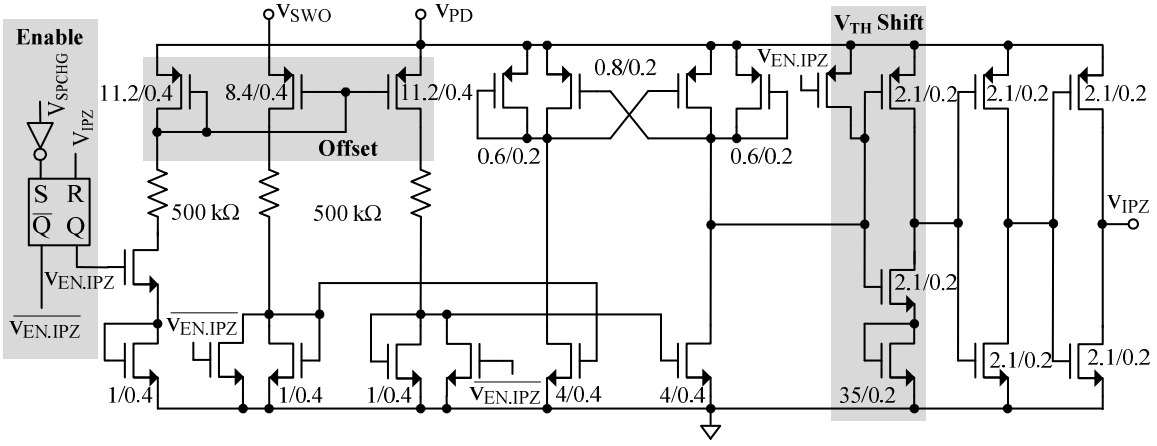


Figure 5.10. Zero-Current-Detecting Comparator CP_{IPZ} for the Supply v_{PD}.

5.5.4. Mode Control

The mode comparator CP_M shares the similar topology with CP_{LT}, but it has 4x-sized latched transistors to create a wider hysteresis (±25 mV) than CP_{LT}. In order to make sure CP_{LT} and CP_M's hysteretic thresholds are well aligned, the latched transistors and diode-connected loads should be physically close to each other and well matched on layout. CP_M uses a smaller bias current (100 nA) than CP_{LT}, because it should be always on to detect load dumps and respond to them at any time. The actual mode transitions, however, happen in synchronous with the clock or zero-i_L signals so that they do not interfere with switch controls.

5.5.5. Bandgap Reference Circuit

The resistor-less bandgap core generates a $PTAT^2$ current (10nA nominal) by biasing $M_{P.RES}$ in linear region [103]-[104] (Fig. 5.11.) The voltage difference in V_{GS}s of sub-threshold PMOS pairs falls on $R_{DS.ON}$ of the transistor $M_{P.RES}$ to conduct I_{BIAS},

$$I_{BIAS} = \frac{V_T}{R_{DS.MPRES}} \ln N , \tag{5-5}$$

where V_T is thermal voltage, $R_{DS.MPRES}$ is on resistance of $M_{P.RES}$, and N is the ratio of the input PMOS pairs $M_{P.I1}$ and $M_{P.I2}$ (4 in this design). Considering $R_{DS.MPRES}$ is inversely proportional to $\sqrt{I_{BIAS}}$, I_{BIAS} becomes proportional to the square of the absolute temperature ($PTAT^2$). Then the current is mirrored with multiplication factor (60) into two series diode-connected NMOSs to generate a reference voltage V_{REF} (1.02V from nominal simulations). Transistors $M_{P.B}$ and $M_{N.B}$ make sure that the bandgap core starts up in a desired state by initially charging up C_{BS} to turn $M_{N.B}$ on so that it can pull down the common gate of $M_{P.I1}$

and $M_{P.I2}$. As the bandgap circuit settles in a desired state, the gate of $M_{N.F}$ goes up shorting C_{BS} to ground. v_{BRDY} signal, which goes high in about 1.4 ms after the start-up when the rising v_{PD} charges up the capacitor C_{SS} with the long-channel PMOS $M_{P.S}$, indicates that the reference voltages and bias currents are now ready.

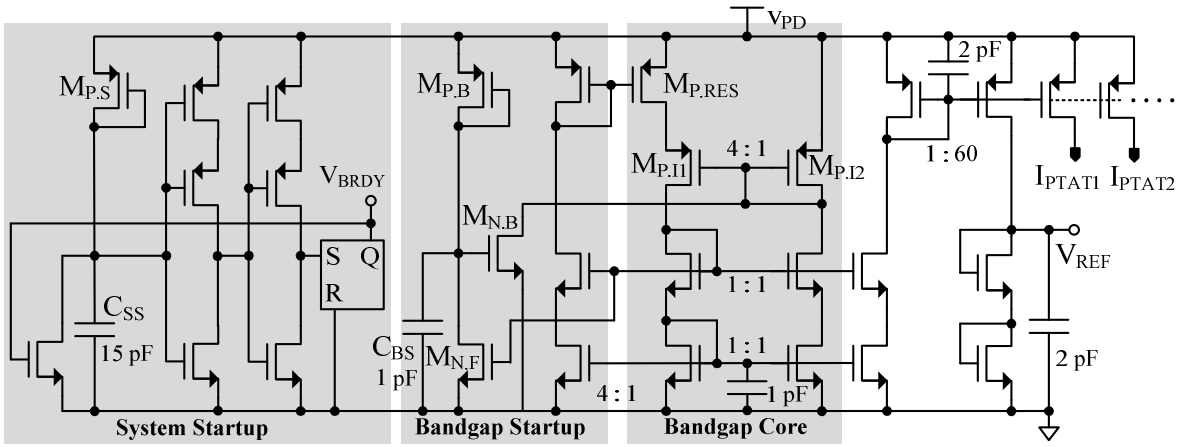


Figure 5.11. Bandgap Reference Circuit.

5.5.6. Clock and Pulse Generators

The system clock f_{CLK} is generated by a comparator-controlled oscillator, constantly charging up and down the capacitor C_{CLK} with constant current sources to generate 40 kHz clock (Fig. 5.12.) The clock generator is enabled after the bias block is ready, turning on the current source I_{BR} with v_{BRDY} signal going high. When CP_{CLK}'s output goes high for the first time, the output of SR latch $v_{EN.PW}$ goes to high to enable power stage, because now the clock is ready. The clock's frequency is determined by the current sources, capacitance, and the hysteresis of CP_{CLK}.

The v_{ED}-energizing event always starts with the rising f_{CLK}, triggering v_{EN} to high to turn on S_{ED} and S_E. At the same time, $I_{B.ED}$ starts to charge up C_{ED}, and when the capacitor voltage reaches the threshold of the following cascaded inverter, v_{RESET} pulse goes to high to end the energizing time and turn off the switches.

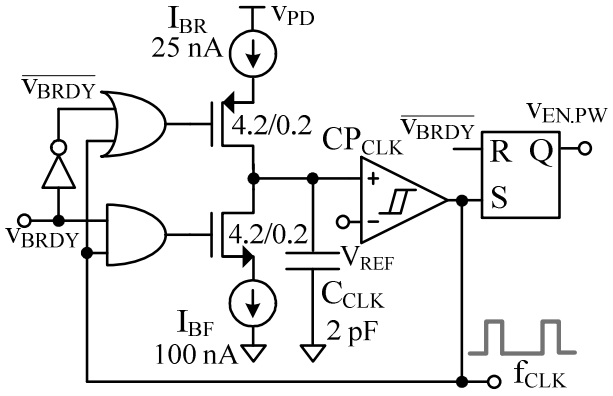


Figure 5.12. Clock Generator Circuit.

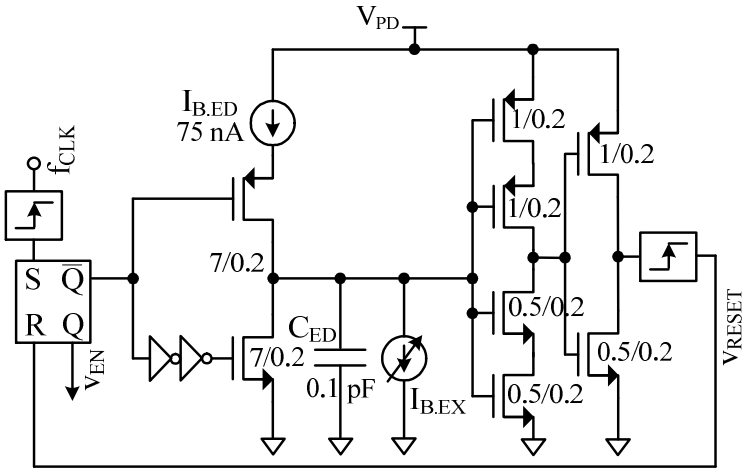


Figure 5.13. Pulse Generator Circuit.

5.5.7. Start Up.

The system starts with the v_{DD} rail ramping up, which is connected to the power source v_{PD}. For sequential start-up or duty-cycled operations, every block including analog and power switches except the bias block has its own enable signal. The bias block turns on automatically as v_{DD} goes up, and the reference voltage and bias currents become ready before v_{BRDY} signal goes high. Then the clock generator starts to charge up C_{CLK} to its desired value, and when v_{CLK} goes from low to high for the first time, the enable signal for power switches $v_{EN.PW}$ goes high to enable the power stage. As initially v_O is low, the system starts with heavy-load mode charging up C_O, with the v_{PS}-energizing time limited by the maximum-time pulse from the pulse generator, because PWM control's output becomes too high due to low v_O. When v_O has risen to the regulation limit of the mode comparator CP_M, then the converter automatically settles into one of the two modes according to the load level at that time.

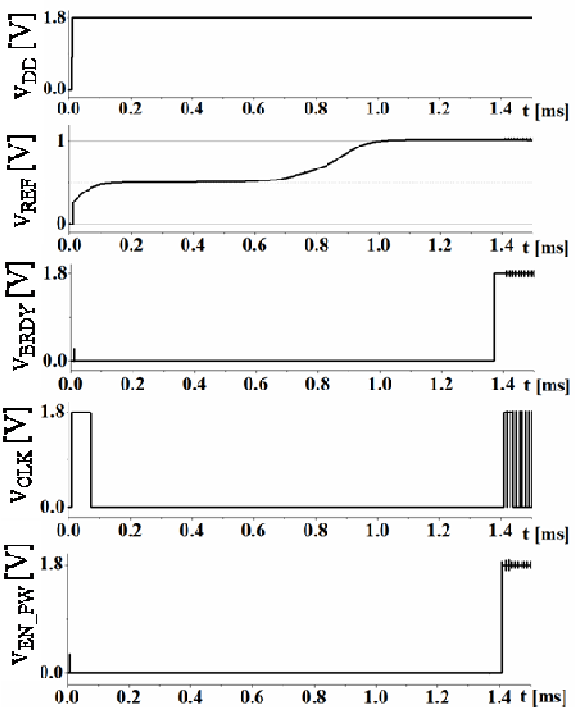
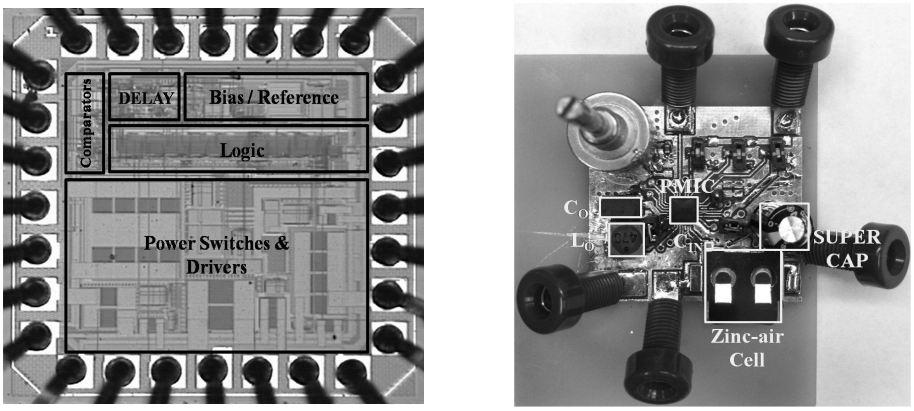


Figure 5.14. System Start Up.

5.6 Performance and Limitations

The 840 × 840-μm^2 0.18-μm CMOS die photographed in Fig. 5.15a and two-layer board in Fig. 5.15b implement the system. A 11×11×5-mm^3 600-mAh zinc-air battery together with a 2×1×1-mm^3 1-μF tantalum capacitor comprise the energy-dense source and a 8×8×12-mm^3 1-F supercapacitor charged to 1.8 V the power-dense counterpart. The power stage uses a 6×6×2-mm^3 50-μH inductor with 4 Ω of ESR to supply power and a 7×4×1-mm^3 10-μF capacitor with 0.1 Ω of ESR to suppress ripples in the output v_O. The clock frequency of the system is 40 kHz.



(a) (b)

Figure 5.15. Prototyped (a) 0.18-μm CMOS die and (b) printed circuit board.

5.6.1. Regulation Performance

In Fig. 5.3, when the load demands 2 mW, the converter delivers about1.5 mW from the zinc-air cell with one energy packet E_{ED} and 0.5 mW from the supercapacitor with two

energy packets E_{PD}. L_O's inductor current peaks at different points when delivering E_{PD} because v_O rises with E_{PD} and CP_{IOZ}'s input-referred offset keeps L_O from fully de-energizing before the subsequent cycle. As a result, E_{PD1} differs slightly from E_{PD2}. Still, v_O ripples 15 mV about V_{REF}, which is 0.80 V. In addition, when lightly loaded, as Fig. 5.5 shows, the system delivers ten of eleven packets of energy to the supercapacitor and v_O ripples roughly 5 mV about 0.823 V.

The output includes perceptible noise with respect to its ripple mainly because the hysteretic window is small at 15 mV. With such tight hysteresis, noise in the board can easily couple into the output, which can not only trigger inadvertent transitions but also affect other components in the system like the reference and bias generator. With over 30 mA of peak current, C_O's R_{ESR} of 0.1 Ω and board resistances also contribute over 3 mV of noise into the 15-mV window.

In response to the rising and falling 1–4-mA load dumps of Figs. 5.16 and 5.17, v_O shifts 12 mV or 1.5% between 0.803 and 0.815 V. Under hysteretic control, the converter responds within one clock cycle and adjusts the number of energy packets it delivers from v_{PD} automatically according to the load. The steady-state shift in v_O is load regulation, which is the result of finite gain across the feedback loop.

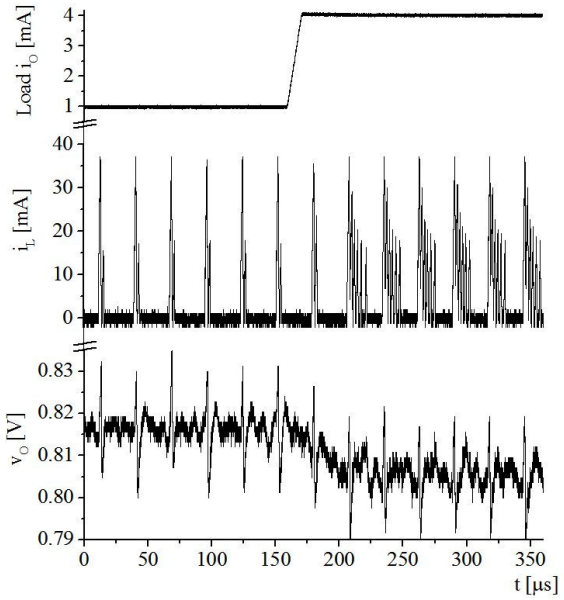


Figure 5.16. Rising 1–4-mA load-dump response.

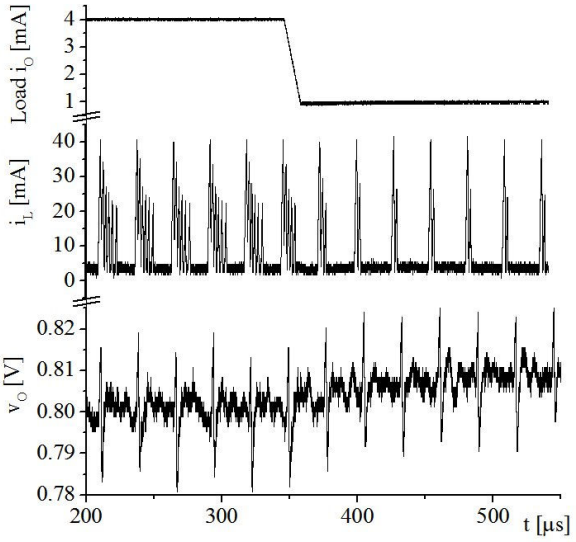


Figure 5.17. Falling 4–1-mA load-dump response.

5.6.2. Power-Conversion Efficiency

The system consumes conduction, gate-drive, and quiescent power. Power switches in the conduction path dissipate 310 μW of Ohmic conduction power when supplying 2 mW to

the load. Of those, as Table 5.1 shows, output switch S_O consumes 280 µW. Parasitic gate capacitances also require 17.4 µW and bias and comparators in the system another 16.8 µW. Considering S_O loses more than 50% of all the 514 µW lost, increasing $S_{O.HV}$'s width–length ratio by5× would have saved, at the expense of increased silicon area, about 200 µW.

Category	Block	Power Losses
Conduction	Power Switches	310µW (280µW in S_O)
	L_O's $R_{L.ESR}$: 4Ω	170 µW
	C_O's R_{ESR}: 0.1Ω	2.9µW
Gate-Drive	Power Switches	16µW
	Logic Gates	1.4µW
Quiescent Losses	Reference/Bias	6.1µW
	Clock/Delay Gen.	3.8µW
	CP_{IOZ}	3.9µW
	CP_O and CP_M	3.0µW
Total Losses		**514 µW when P_O is 2 mW**

Table 5-1. Simulated power losses in the system

Power-conversion efficiency η_C is how much input power P_{IN} from v_{ED} and v_{PD} reaches v_O as P_O:

$$\eta_C \equiv \frac{P_O}{P_{IN}} = \frac{P_O}{P_{ED} + P_{PD}}, \tag{5-6}$$

where P_{ED} and P_{PD} refers to the power that v_{ED} and v_{PD} supply, respectively. In this case, η_C peaks to 73% when supplying 1 mA to the load, as Fig. 5.18 demonstrates. Overall, η_C

remains above 65% across the0.5-to 8-mA load range. η_C does not rise above 73% because, as Table 5.1 shows, output switch S_O and L_O's $R_{L.ESR}$ consume substantial power. In fact, increasing S_O's width–length ratio would raise η_C. Similarly, reducing $R_{L.ESR}$ would also raise η_C, but at the expense of volume because L_O would have to be physically larger. In other words, larger systems outperform their miniaturized counterparts.

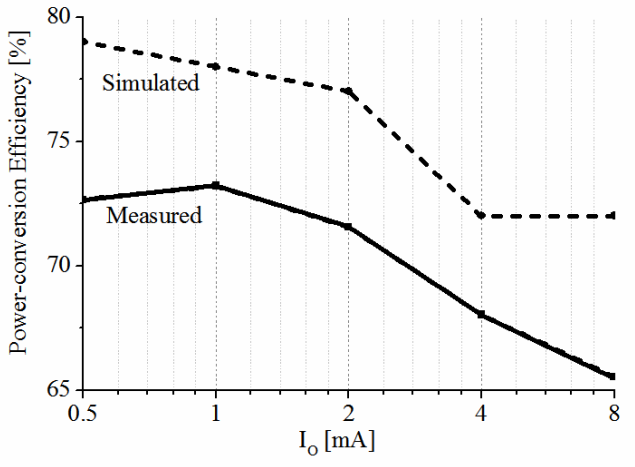


Figure 5.18. Power-conversion efficiency across load-current I_O.

Generally, measurements were roughly 7% to 8% lower than simulations predicted. This discrepancy is more than likely the result of several factors. For one, basic CMOS models do not emulate well the parasitic series resistances and substrate currents that power transistors typically incorporate. Secondly, the printed circuit board introduces parasitic series resistances to ground, the output, and both zinc-air and supercapacitor supplies that, again, simulations do not account well. In this respect, a multi-layer board can expand the supply and ground planes and reduce their resistive effects.

5.6.3. Tradeoffs

Since accommodating larger power switches and a larger inductor reduces Ohmic losses,

one tradeoff in this system, as in other dc–dc converters, is efficiency for size. Another tradeoff is stability and response time for noise and power losses. This system is stable because v_O rises when the system supplies more current in peak-current-mode fashion, which results because the voltage across C_O's R_{ESR} overwhelms that of C_O [102]. Plus, hysteretic converters [102][105] respond more quickly than pulse-width modulated supplies [106]. In other words, control and speed hinge on the presence of R_{ESR}.

Unfortunately, peak inductor currents across R_{ESR} produce noise ripple in v_O. R_{ESR} also dissipates Ohmic power, so R_{ESR} reduces efficiency. Plus, R_{ESR} limits the extent that C_O rejects coupled noise in v_O. At high frequency, for example, when loop gain is negligible, feedback is unable to counter the effects of noise coupled from the supplies and other circuits that v_O powers. Considering all these effects, the optimal C_O introduces no more R_{ESR} than necessary to guarantee stability.

	[88] TCAS-II 09	[90] JSSC 09	[107] ISSCC 13	[108] ISSCC 11	[109] TCAS-II 12	This work
Topology	MO Buck-Boost	SIMO Buck-Boost	SIDITO Buck-Boost	SISO Boost	SIMO Boost	SIDIDO Buck-Boost
Efficiency at 0.1mW	80%	80%	83%	83%	60%	72%
Peak Efficiency	83%	93%	83%	87%	81%	73%
Output Voltage	2 ~ 12	1.25	1, 1.8, 3	1.5, 3, 5	2.5, 3.0	0.8
Load Dump	20 mV	25 mV	–	–	50 mV	30 mV
Output Capacitor	10 µF	33 µF	–	–	10 µF	1 µF
Load Range	0 – 450 mW	0 – 125 mW	0 – 10 mW	0 – 10 mW	0 – 150 mW	0 – 8 mW
Inductor	4.7 µH x 2	10 µH	–	1000 µH	1 µH	50 µH
Process Technology	0.5 µm	0.25 µm	0.18 µm	0.25 µm	0.5 µm	0.18 µm
Source required to sustain the 0.01 – 4-mW load in Fig. 1	480-mg DMFC Or 330-mg Li Ion	430-mg DMFC Or 320-mg Li Ion	480-mg DMFC Or 310-mg Li Ion	460-mg DMFC Or 310-mg Li Ion	490-mg DMFC Or 430-mg Li Ion	73-mg DMFC + 27-mg Li Ion Tot.: 99 mg

Response Time	< 10 clock cycles*	< 10 clock cycles*	N/A (Open-loop)	N/A (Open-loop)	< 12.5 clock cycles	< 2 clock cycles
Switching Frequency	1 MHz	660 kHz	10/20 kHz	100 kHz	500 kHz	40 kHz

Table 5-2. Summary of the ESR-derived charger-supply system and comparison against the state of the art

5.6.4. Performance Comparison

Table 5-2 summarizes the performance of the prototyped single-inductor multiple-input multiple-output (SIMIMO) charger–supply and those of similar, though not exactly alike state-of-the-art systems. The driving advantage of the prototyped system over the state of the art is the feedback intelligence with which it determines when to derive power from a power-dense source and when to steer excess energy from an energy-dense source into the rechargeable power-dense battery. The ultimate benefit here is the space savings that results when supplying a system whose peak power is substantially above its average, which is typical in wireless microsensors.

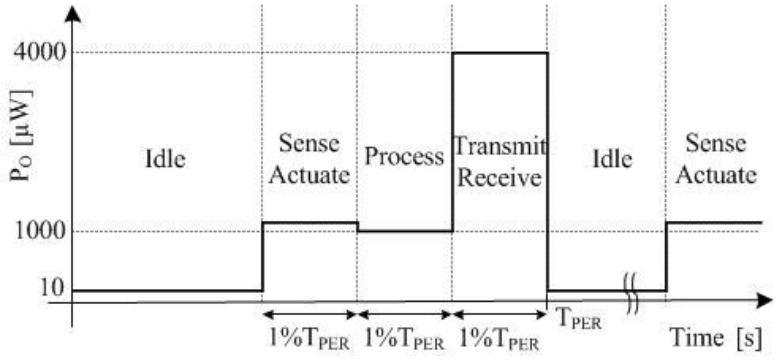


Figure 5.19. Sample load profile of a wireless microsensor

Fig. 5.19 shows a suggested sample load profile of a wireless microsensor to compare performance metrics with other works, and this has a similar energy profile given in [110]. In this load profile, the system mostly idles at 10 μW and peaks to 4 mW to dissipate 72 μW on average. For this, first consider that the weight W_{FC} of the direct-methanol fuel cell (DMFC) required to supply the power $P_{IN(PK)}$ that a converter with a power-conversion efficiency $\eta_{C(PK)}$ demands when delivering peak output power $P_{O(PK)}$ depends on the fuel cell's power density PD_{FC}:

$$W_{FC} = \frac{P_{IN(PK)}}{PD_{FC}} = \frac{P_{O(PK)}}{\eta_{C(PK)} PD_{FC}}. \tag{5-7}$$

Similarly, the energy density ED_{LI} of a lithium ion determines the weight W_{LI} of the battery required to sustain the power $P_{IN(AVG)}$ that a converter with a power-conversion efficiency $\eta_{C(AVG)}$ demands when outputting average output power $P_{O(AVG)}$ for one month is

$$W_{LI} = \frac{P_{IN(AVG)} t_{1\text{-MONTH}}}{ED_{LI}} = \frac{P_{O(AVG)} t_{1\text{-MONTH}}}{\eta_{C(AVG)} ED_{LI}}. \tag{5-8}$$

So, to sustain the aforementioned load, the MO buck–boost converter in [88] requires a 480-mg direct-methanol fuel cell (DMFC) to supply the 4-mW peak load or a 330-mg lithium-ion battery to sustain 72 μW for one month. [90],[107-109] must similarly oversize the DMFC to 460 – 480 mg to supply the 4-mW peak or the lithium ion to 310 – 430 mg to sustain 72 μW for one month. Since the system presented here draws average power from the energy-dense source and burst power from the power-dense counterpart, W_{FC} depends on $P_{O(AVG)}$ and W_{LI} on $P_{O(PK)}$:

$$W_{FC} = \frac{P_{IN(AVG)} t_{1\text{-MONTH}}}{ED_{FC}} = \frac{P_{O(AVG)} t_{1\text{-MONTH}}}{\eta_{C(AVG)} ED_{FC}}, \tag{5-9}$$

$$W_{LI} = \frac{P_{IN(PK)}}{PD_{LI}} = \frac{P_{O(PK)}}{\eta_{C(PK)} PD_{LI}}, \tag{5-10}$$

and $$W_{TOT} = W_{FC} + W_{LI}. \tag{5-11}$$

As a result, the prototyped converter requires a 27-mg lithium ion to supply 4-mW peaks and a 73-mg DMFC to sustain 72 μW for one month. When combined, the proposed technology requires 99 mg, which is 68% less weight than what the lightest state-of-the-art counterpart requires.

Other features here are the speed and ease of compensation that result from operating under nested hysteretic loops. For one, the feedback comparators CP_O and CP_M react to load dumps as soon as they detect changes in v_O, so the system responds within one or two clock cycles, as opposed to the several clock cycles needed under pulse-width-modulation (PWM) schemes. And the system remains in regulation without the aid of off-chip compensation components as long as the voltage across the equivalent series resistance (ESR) of the output capacitor C_O overwhelms that of C_O. This means this solution can be both fast and compact, both of which are critical in micro-scale applications whose loads vary vastly across time.

5.7 Summary

The hysteretic dual-source single-inductor 0.18-µm CMOS switching charger–supply supplies 0.5 – 8 mA and regulates the output to 0.8 V within 1.5% with peak and average efficiencies of 73% and 70%. When heavily loaded, the system draws constant power from an energy-dense source and supplementary peak power from a rechargeable power-dense battery. Otherwise, when lightly loaded, the system recharges the battery with excess power from the energy-dense source. This way, when loaded with a microsystem that idles at 10 µW and peaks to 4 mW, the system requires sources that weigh 68% less than those of the state of the art. The dual-source system also responds to load dumps within one switching cycle by redirecting power from the energy-dense source and adjusting the number of energy packets the power-dense battery delivers. The charger–supply is fast and widely stable without off-chip compensation components because the voltage across C_O's equivalent series resistance (ESR) dominates over that of C_O. While higher ESRs reduce efficiency and raise noise, responding quickly to load dumps is imperative in miniaturized applications. Microsensors, to cite a driving example, which cannot afford large capacitors and inductors, suffer from vast load dumps when they wake and transmit data wirelessly. In these cases, response time and overall size are paramount.

Chapter 6. Low-ESR Variant of PWM-Hysteretic System

The ESR-dominant PWM-hysteretic system introduced in the previous chapter showed an improved efficiency performance and a fast response time to load dumps, compared to the fully hysteretic charger supply system in Chapter 4. Although this ESR-dominant hysteretic control is simple and efficient in regulating the inductor current and the output voltage, it relies on the ESR of the output capacitor, and the magnitude of the ESR determines whether the system is stable or not, narrowing the converter's application. The PWM control, which may require a longer response time than the fully-hysteretic counterpart, does not have such constraints on the ESR of the output capacitor and therefore can be more widely applicable.

The low-ESR variant of PWM-hysteretic single-inductor charger-supply IC has a similar energy flow and power stages with the previous systems, as shown in Fig. 6.1. In the low-power supplying path from v_{ES} to v_O, the converter works as a non-inverting buck-boost converter by energizing L_O with S_E and $S_{E.E}$ closed, and de-energizing L_O into v_O with $S_{E.DE}$ and $S_{O.LT}$ closed. In the other low-power recharging path from v_{ES} to v_{PS}, the energizing operation is exactly the same as v_{ES}-v_O path, but in the de-energizing operation, $S_{P.CHG}$ is closed instead of $S_{O.LT}$ to deliver L_O's energy into v_{PS}. In the higher-power supplying path, the converter works as a buck converter, with $S_{P.E}$ and $S_{P.DE}$ turning on and off alternately, and with $S_{O.HV}$ closed all the time to supply v_O. The pairs of $S_{E.DE}$/$S_{P.DE}$ and $S_{O.LT}$/$S_{O.HV}$ are two sets of power switches sized differently for low-power and high-power supplying paths

respectively, for higher efficiency. In addition, $S_{O.LT}$ and $S_{P.CHG}$ are comparator-controlled active switches to block negative currents more efficiently than actual diodes (Fig. 6.1.)

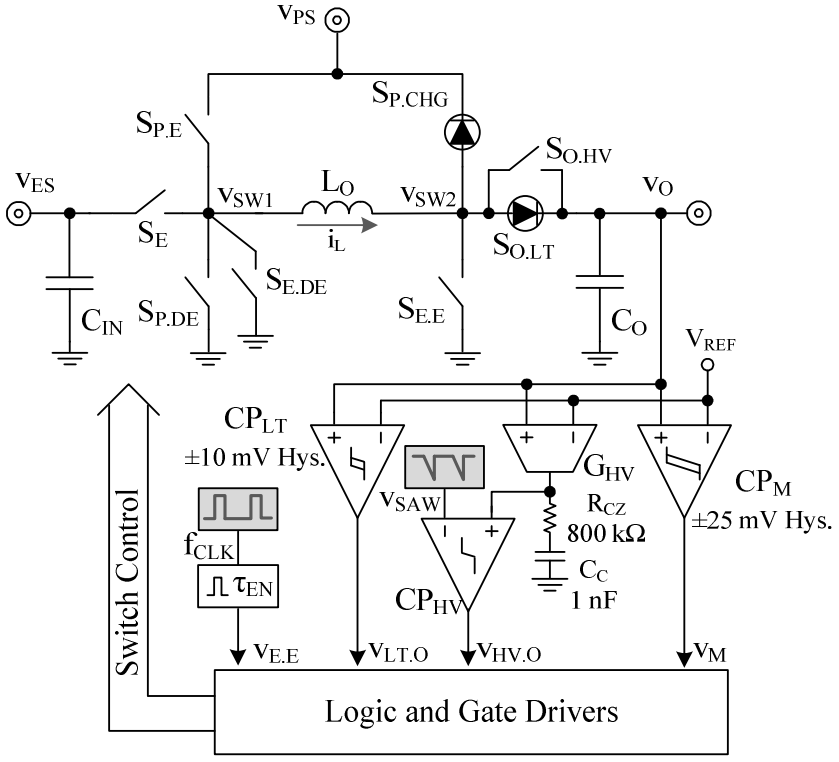


Figure 6.1. Low-ESR Variant of PWM-Hysteretic System.

The control of power switches are basically synchronized with the internal system clock f_{CLK}, and L_O is shared in discontinuous conduction mode, which can efficiently deliver the system's load of up to 8mW (Fig. 6.1). f_{CLK} and the pulse generation block generates constant on-time pulse $V_{E.E}$ to draw the constant power P_{ES} from v_{ES}. The load power p_O's level with respect to P_{ES} determines the operational mode of this system. For example, if p_O is lower than P_{ES}, then the converter operates in light-load mode (LLM), and otherwise it operates in heavy-load mode (HLM). The mode decision is made by comparing v_O to the

reference V_{REF} by the mode comparator CP_M, not by sensing and comparing the actual currents, to avoid complexity.

6.1 Control and Stability

6.1.1. Light-load Mode (LLM)

Control: All power switches are controlled by their own SR latches, with S_E and $S_{E.E}$ sharing the same latch (Fig. 6.2). The switch operations start with the rising edge of f_{CLK}, by turning on S_E and $S_{E.E}$ to energize L_O from v_{ES}. After the pre-defined energizing time τ_{EN}, those two switches turns off by the output of the pulse generator (v_{PUL}), and then the turn-off pulse $v_{EE.OFF}$ turns on the de-energizing switch $S_{E.DE}$ and either of the two switches $S_{O.LT}$ or $S_{P.CHG}$, depending on CP_{LT}'s output $v_{LT.O}$: if $v_{LT.O}$ is low, $S_{O.LT}$ is turned on (to supply v_O), and otherwise $S_{P.CHG}$ is turned on (to recharge v_{PS}). When i_L starts decreasing through $S_{O.LT}$, zero-current-detect comparator CP_{IOZ} turns on, and when i_L reaches zero, its output v_{IOZ} goes high. Then $S_{O.LT}$ and $S_{E.DE}$ turns off, and all switches are kept open until the next rising f_{CLK} comes. The other comparator CP_{IPZ} similarly detects zero currents through the switch $S_{P.CHG}$, when i_L is being directed to v_{PS}. Fig. 6.3a shows the measured waveforms of i_L, v_O, and $v_{LT.O}$ in light-load mode, showing that 1 out of 10 energy packets are delivered to v_O, with 9 others going to v_{PS}. Fig. 6.3b captures the multiple triggering moments showing both de-energizing paths: to v_O and to v_{PS}.

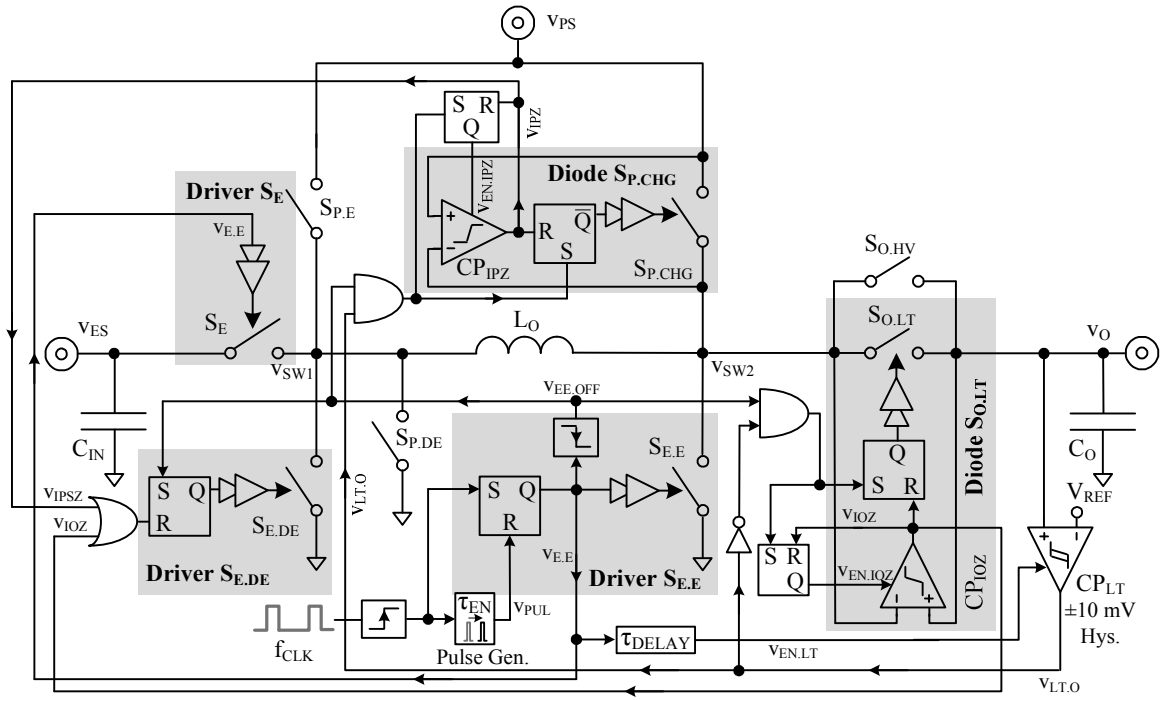
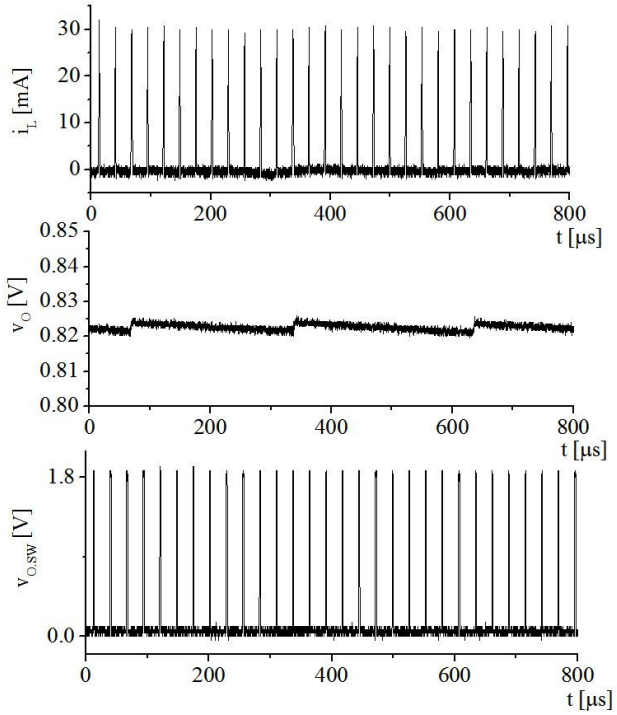


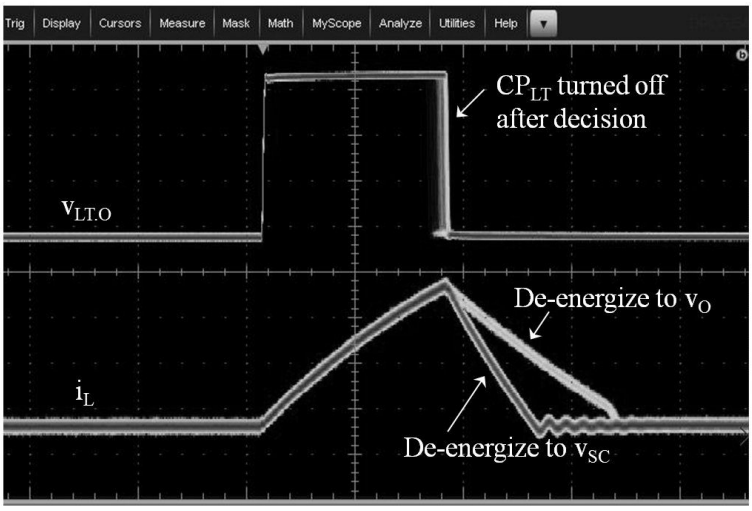
Figure 6.2. Light-Load Mode.

As the inductor current stays at zero for a large portion of the switching period and comparators do not need to be on during the entire time, control power can be significantly saved by duty-cycling the comparators CP_{LT}, CP_{IOZ}, and $CP_{IPZ.}$ For example, CP_{LT} only needs to be on at the end of energizing time, because that is when $v_{LT.O}$ is needed to decide where to direct L_O's energy. Therefore, the enable signal $V_{EN.LT}$ is derived from delaying $v_{E.E}$ signal by τ_{DELAY}, to cover the moment and the required setting time (Fig. 6.3b.) The zero-current detecting comparators CP_{IOZ} and CP_{IPZ}, however, need to stay on only during $S_{O.LT}$ or $S_{P.CHG}$ is on. Therefore, their enable signals $v_{EN.IOZ}$ and $v_{EN.IPZ}$ goes high with the de-energizing event starts, resetting comparators' outputs to zero. When the comparators detect the zero currents, their outputs go high, turning themselves off and finishing their

duties in that clock period. This duty-cycled operations result in the reduction of about 90% of the comparators' static control power in light-load mode.



(a)



(b)

Figure 6.3. (a) Inductor Current, Output Voltage, Comparators' Output Signals in Light-Load Mode, and (b) Zoomed-in Inductor Current and Comparators' Output's Fast-Acquisition Screen Capture

Stability: The small-signal model for hysteretic-controlled light-load mode becomes the averaged inductor current flowing into the main output v_O and the power source v_{PS}, with the averaged connection duty cycle $\overline{d_O}$ defined by the averaged ratio of the number of cycles v_O connects to L_O over entire switching cycles (Fig. 6.4). As the inductor's peak current is a pre-defined constant, the inductor becomes an averaged constant current source which does not have ac variations with respect to v_O, and therefore it does not present any RHP zero. The transfer function from $\overline{d_O}$ to v_O presents a single-pole response with C_O, and the rest of the comparator's describing function make sure that the closed-loop system shows sustained oscillation at the switching frequency, as in any hysteretic controlled DC-DC converters [111]. The other output v_{PS} is not a feedback-controlled output, absorbing any remnant energy after supplying v_O.

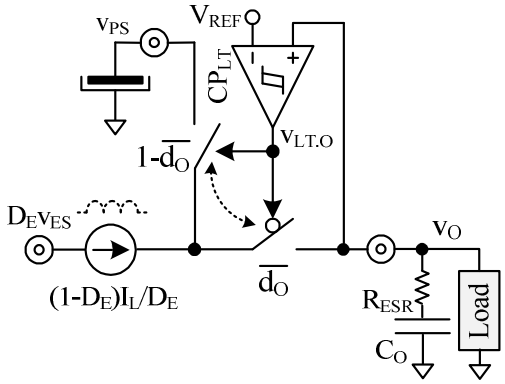


Figure 6.4. Small-Signal Model for Light-Load Mode.

6.1.2. Heavy-load Mode (HLM)

Control: The switch operations in heavy-load mode also start from energizing L_O from v_{ES} by closing S_E and $S_{E.E}$ for the same duration τ_{EN}, but then de-energize it only to v_O by closing $S_{E.DE}$ and $S_{O.HV}$, because now the load requires more than P_{ES} in this mode (Fig. 6.5.) After i_L reaches zero (V_{IOZ} goes high) and v_O still needs more power, then the converter turns on $S_{P.E}$ with $S_{O.HV}$ kept on, and starts energizing from v_{PS} as in a buck converter. And at the same time, the saw-tooth signal V_{SAW} starts to ramp down (Fig 6.6.) During this v_{PS}-energizing, i_L keeps increasing until the PWM comparator CP_{HV}'s output goes high. However, to limit the i_L's peak value, the pulse generator throws a separate reset pulse to Driver $S_{P.E}$, for the case when v_O needs too much power so that i_L increases by too much. If either of these signals go high, $S_{P.E}$ turns off and $S_{P.DE}$ turns on to deliver L_O's energy to the load (v_O). When i_L reaches zero, V_{IOZ} turns off $S_{P.DE}$ and then the rest of the switches are kept off until the next clock comes. The control can be made to allow more than one energizing instance per clock from v_{PS} to reduce v_O's ripple, but the number is limited to one for this IC for simplicity. As the zero-current detection comparator CP_{IOZ} are needed during de-energizing events in both v_{ES}' and v_{PS}' periods, its enable signal $v_{EN.IOZ}$ goes high with either of the switch-turn-off signals: $v_{EE.OFF}$ or $v_{PE.OFF}$., and comes back to low when the current crosses zero.

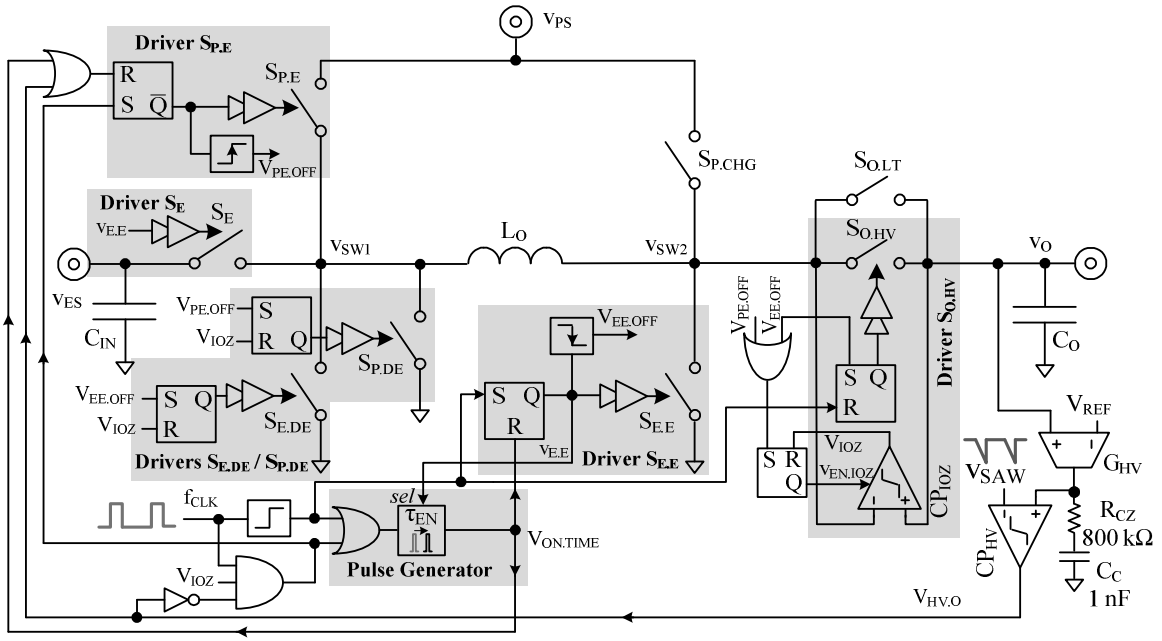


Figure 6.5. Heavy-Load Mode.

The pulse generator makes two different pulse signals for (1) setting v_{ES}-energizing time $\tau_{E.E}$ and for (2) limiting v_{PS}-energizing time to $\tau_{P.EMAX}$, respectively (Fig. 6.5.) This block starts counting the time with either of the starting pulses of V_{ES}-energizing or V_{PS}-energizing, and then generates a time-shifted pulse to finish the V_{ES}-energizing, or to finish the v_{PS}-energizing if PWM control output $v_{HV.O}$ has not already ended it. $\tau_{E.E}$ and $\tau_{P.EMAX}$ are pre-defined so that the former is at the energizing time for optimum P_{ES}, and the latter is to make sure that i_L's peak current is well-limited so that there's no overlap between the adjacent clock cycles. $v_{E.E}$ selects which delay to be generated ($\tau_{E.E}$ or $\tau_{P.EMAX}$.)

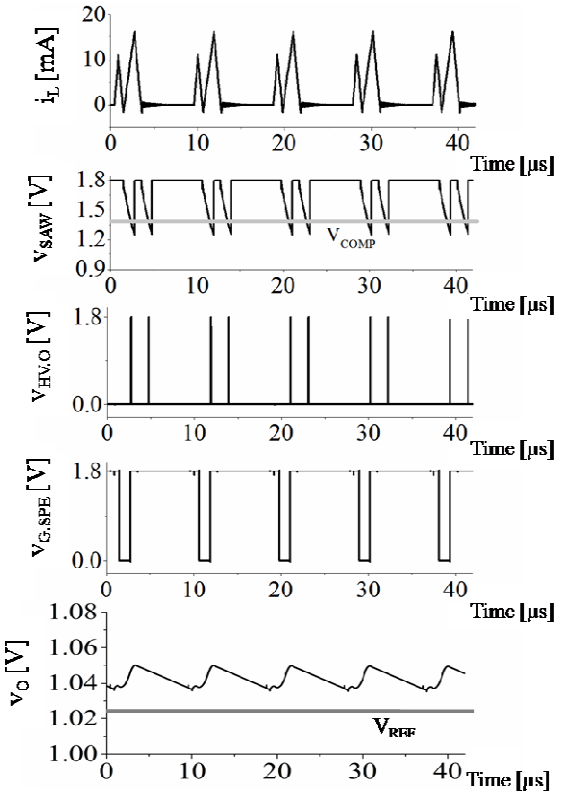


Figure 6.6. Simulated Inductor Current, Saw Tooth, PWM Comparator's Output, gate signal of $S_{P.E}$, and Output Voltage in Heavy-Load Mode.

Stability: The small-signal model for heavy-load mode is shown in Fig. 6.7. Unlike in light-load mode, v_O's small-signal variation does propagate through L_O, because now the inductor's peak current $i_{L(PK).PS}$ propagates the small-signal perturbation from the error amplifier G_{HV}'s output v_{go} (Fig. 6.8.) Therefore, the open-loop gain can be expressed from Eq. 1 with each stage's small-signal gain drawn from Fig. 6.7 and Fig. 6.8,

$$A_{HV} = \frac{v_{go}}{v_o}\frac{t_{en}}{v_{go}}\frac{i_o}{t_{en}}\frac{v_o}{i_o} = \left(\frac{G_M R_{GO}(1+sR_{CZ}C_C)}{1+2(R_{GO}+R_{CZ})C_C}\right)\left(\frac{T_{EN}}{V_{SAW}}\right)\left(\frac{I_{L(PK)}}{T_{SW}}\right)\left(Z_{LO}\left\|(R_{ESR}+\frac{1}{sC_O}\right.\right) \quad (6\text{-}1)$$

where R_{GO} is the output impedance of G_{HV}, Z_{LO} is the output impedance of L_O when conducting current in DCM ($\frac{2T_{SW}V_O^{\ 2}}{I_{L(PK)}^{\ 2}L_O}$), and other variables defined in Fig. 6.7 and 6.8. The Bode plot of A_{HV} was drawn (Fig. 6.9) with the actual components' values used in the circuit, showing the stable response with the low-frequency gain of 43dB and phase margin of about 90 degrees.

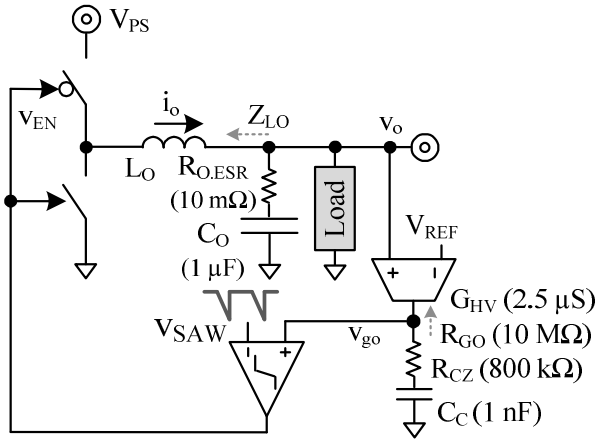


Figure 6.7. Small-signal Model in Heavy-Load Mode.

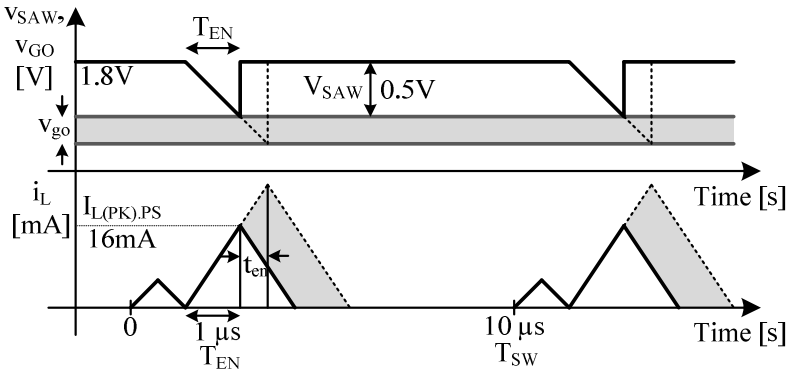


Figure 6.8. Small-signal Variations in Error Amplifier's output and Inductor Current in Heavy-Load Mode.

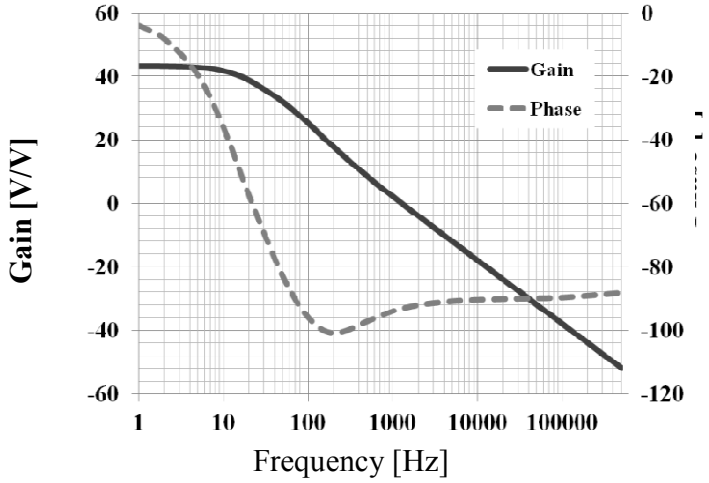
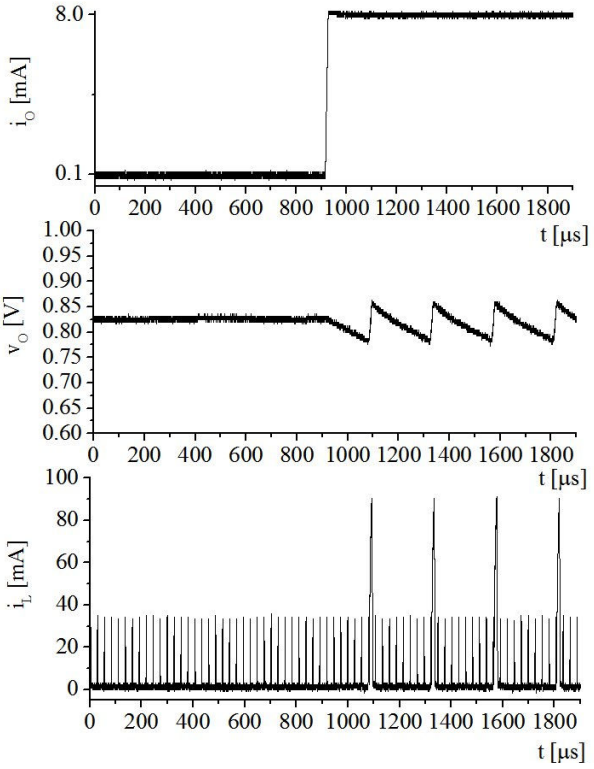


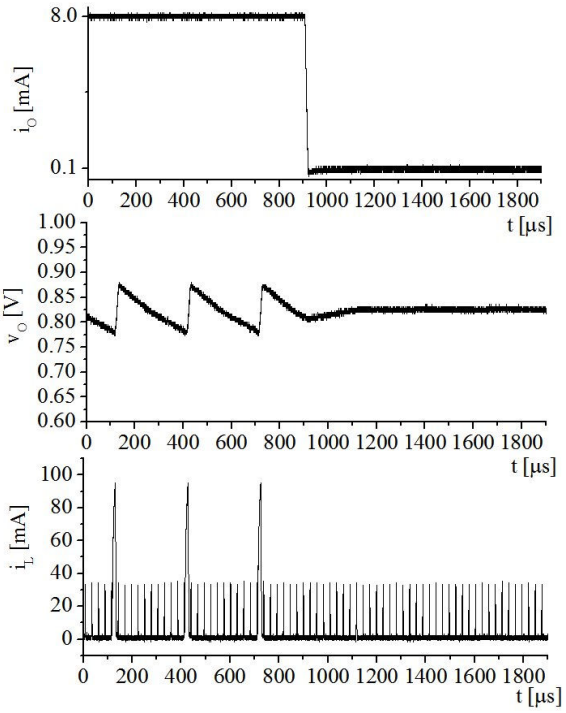
Figure 6.9. Loop Gain and Phase in Heavy-Load Mode.

6.1.3. Mode Transitions

The converter's mode is determined by the load power p_O: if p_O is lower than P_{ES}, then the converter operates in light-load mode, and in heavy-load mode otherwise. Instead of directly sensing p_O, the converter senses v_O with the mode comparator CP_M, and when v_O goes out of the steady-state regulation range and reach the wider hysteretic limits of CP_M, it changes its mode, because it indirectly shows that power delivered to the load is a lot bigger (in heavy to light transitions) or smaller (in light to heavy transitions) from what the load actually needs. For example, when the converter is in light-load mode and p_O increases over P_{ES} (Fig. 6.10a), v_O continues to decrease, until it hits the lower hysteretic limits defined by CP_M. Then the output of CP_M goes low, and with the rising edge of the next clock, the system enters to heavy-load mode, where the power source v_{PS} starts to supply its own power to load (Fig. 6.10a). With the higher total input power, v_O starts to increase back near to the reference value.


8.0
0.1
i_O [mA]
0 200 400 600 800 1000 1200 1400 1600 1800
t [µs]
1.00
0.95
0.90
0.85
0.80
0.75
0.70
0.65
0.60
v_O [V]
0 200 400 600 800 1000 1200 1400 1600 1800
t [µs]
100
80
60
40
20
0
i_L [mA]
0 200 400 600 800 1000 1200 1400 1600 1800
t [µs]

(a)


8.0
0.1
i_O [mA]
0 200 400 600 800 1000 1200 1400 1600 1800
t [µs]
1.00
0.95
0.90
0.85
0.80
0.75
0.70
0.65
0.60
v_O [V]
0 200 400 600 800 1000 1200 1400 1600 1800
t [µs]
100
80
60
40
20
0
i_L [mA]
0 200 400 600 800 1000 1200 1400 1600 1800
t [µs]

(b)

Figure 6.10. (a) Light to Heavy Mode Transition and (b) Heavy to Light Mode Transition.

When the converter is in heavy-load mode and p_O suddenly decreases below P_{ES}, then v_O starts to rise even without v_{PS} and the control does not initiate v_{PS}-energizing event (Fig. 6.10b). v_O keeps increasing over the steady-state regulation window, because now the load level is even lower than P_{ES}. Then v_O automatically settles in the regulation window defined by the hysteretic comparator CP_{LT}, sharing P_{ES} into v_O and v_{PS}. These mode transitions are synchronized with either the clock's rising edge or i_L's zero current condition, to start a new switch energizing sequence with no overlaps.

6.2 IC Implementation

The proposed single-inductor charger-supply IC was designed in 0.18μm TI LBC8 process. Each power switch was sized to balance the conduction and gate-drive energy losses to minimize total switch losses, with 1.8V V_{PS} driving the switches. Switch $S_{P.E}$ and $S_{P.CHG}$ were chosen to be PMOSs as they interface with the highest voltage V_{PS}. S_E and $S_{O.HV}$ are also PMOSs for lower losses with the higher gate drive voltages, and $S_{O.HV}$ has a back-to-back diode to block any reverse current. $S_{O.LT}$, however, was chosen to be NMOS, because of lower power level and therefore less benefits from using two large PMOS switches.

6.2.1. Mode Comparators.

The light-load-mode comparator (CP_{LT}) regulates v_O in light-load mode by deciding where to put i_L's energy, either to v_O or V_{PS}, according to v_O's level (Fig. 6.11.) The first stage consists of a NMOS input pair with a latched PMOS load for generating hysteresis (±10 mV), the amount of which depending on the relative strength of the latched and diode-

connected transistors. CP_{LT} is on only during the time-shifted V_{ES}-energizing duration in light-load mode, because the decision about where to direct i_L's energy is only required at the end of energizing time. The mode comparator (CP_M) shares the similar topology with CP_{LT}, but it has differently-sized latched and diode-connected transistors for wider hysteresis (±25 mV), as shown in Fig. 6.11 (values in parenthesis are for CP_M.) In addition, CP_M is always on with a smaller tail current (100 nA) than CP_{LT}.

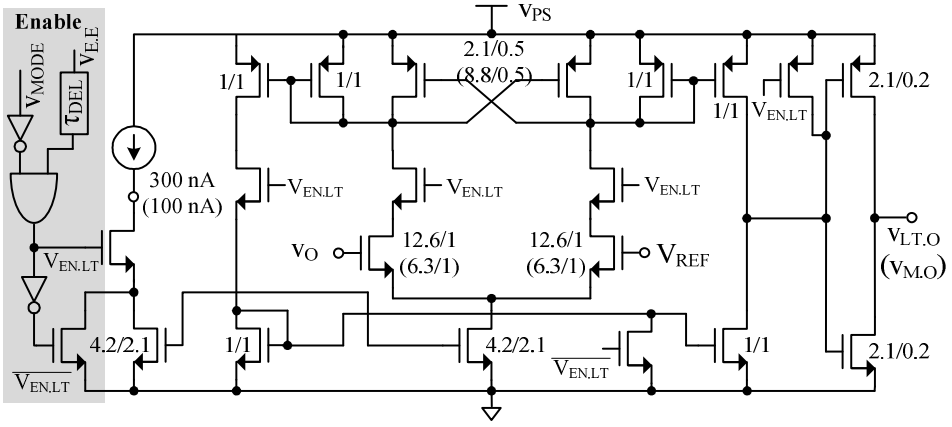


Figure 6.11. Output comparator CP_{LT} and Mode comparator CP_M.

6.2.2. Voltage-PWM Converter and Transconductor.

To regulate v_O at a varying load in heavy-load mode, power from v_{PS}, which translates into the v_{PS}-energizing time, should be adaptively changing, unlike the constant power P_{ES} from v_{ES}. For that purpose, a voltage-mode PWM control is used to determine v_{PS}-energizing time in heavy-load mode (Fig. 6.12.) After the v_{ES}-energizing and de-energizing events end with i_L reaching zero, then the v_{PS}-energizing switch $S_{P.E}$ is turned on (with $S_{O.HV}$ already on), and at the same time a 100nA current source I_B is enabled to start to discharge C_{SAW} to generate a saw-tooth signal v_{SAW} (Fig. 6.6.) When v_{SAW} goes below the compensated error

transconductor G_{HV}'s output v_{GO} by a certain threshold, the output $v_{HV.O}$ of CP_{HV} goes high to end and set the v_{PS}-energizing time. This signal also resets C_{SAW} to zero and disables I_B, waiting for the next clock. Then the de-energizing switch $S_{P.DE}$ turns on and starts de-energizing i_L to v_O, eventually reaching zero and generating another pulse in v_{IOZ} and v_{SAW}. For simplicity, however, the number of v_{PS}-energizing events per one clock period is limited to only one time in this IC.

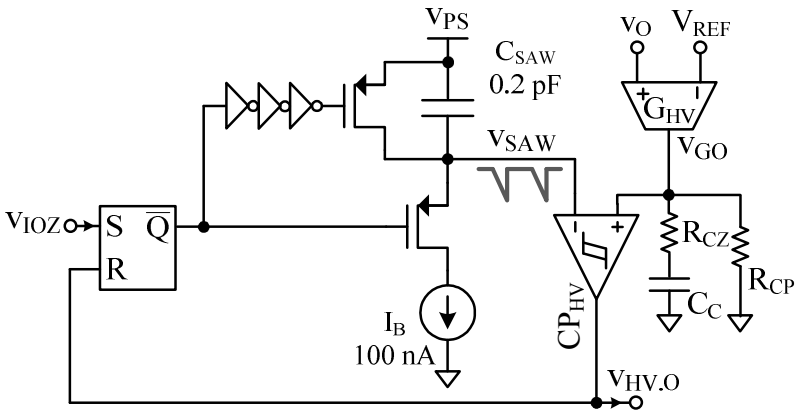


Figure 6.12. Voltage-PWM Converter.

The feedback transconductor G_{HV} has a transconductance of 2.5 μS so that the total low-frequency loop gain in heavy-load mode is as high as 43 dB. G_{HV} has a high-gain folded cascode structure (Fig. 6.13), and putting a dominant pole at the output and inserting a zero to cancel the second pole at v_O stabilizes the system, as shown in II. B. The saw comparator CP_{HV} shares the similar design with the hysteretic mode comparator CP_M to prevent a too-short pulse than the control's response time.

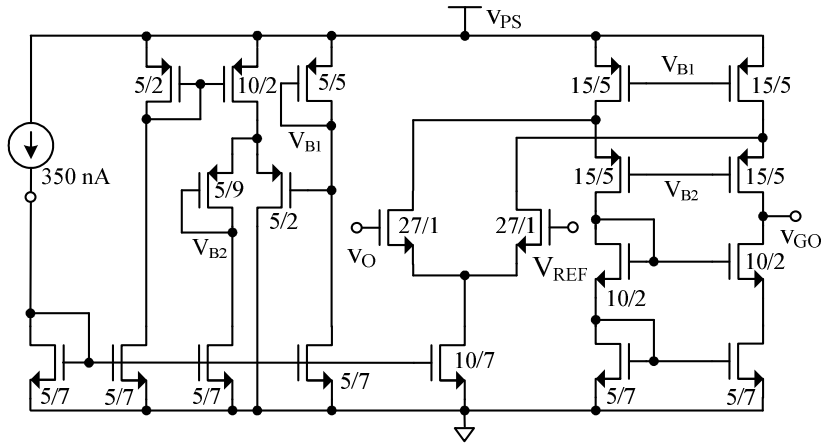


Figure 6.13. Feedback Transconductor G_{HV}.

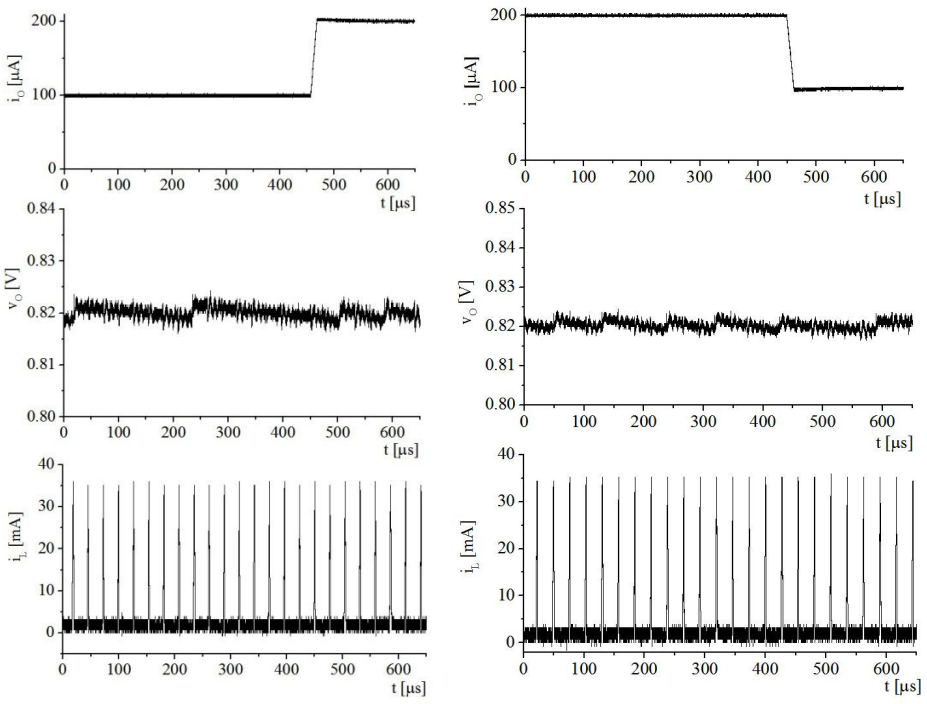
6.3 Performance and Limitations

This prototype shares the same die and board with the ESR-derived nested hysteretic charger-supply system, as shown in Fig. 5.15. As the energy source, a 675-size Energizer Zinc Air battery is used, to provide the rated capacity of 600 mAh with 2 mA drain current [112]. The zinc-air battery starts up on its own when the air-blocking tape is removed, generating about 1.1-1.4 V from a single cell. In order to absorb ripples from discontinuous conduction operations, 1 μF tantalum capacitor is connected in parallel with the energy source [113]. To supply a higher load power beyond the zinc air battery's, a 30mF super capacitor is used, which has a much smaller capacity (10 μAh), but can provide much higher power in a short duration [114]. The super capacitor, which also supplies the system's control power, is pre-charged to 1.8 V outside the IC. A 50 μH off-chip inductor and 1 μF output capacitor are used to deliver power from dual sources to a 0.8 V, 0.1 -

8mA load in 100 kHz, discontinuous conduction mode operations (the measured V_{REF} was about 20% lower than the simulated value – 1.02 V.)

6.3.1. Regulation Performance.

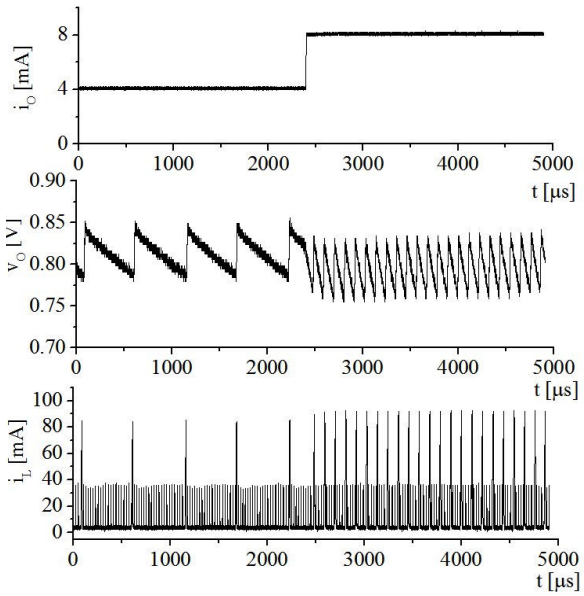
Light-load Mode: During the light-load mode, the output voltage stays within the regulation window (±10 mV) of CP_{LT}, as shown in Fig. 6.3a. The inductor draws a constant power of about 1.5 mW from the zinc air battery, and delivers part of it to the load, and the rest of it to the super capacitor. When the load changes within the range of light-load mode (from 100 µA to 200 µA), v_O remains within the regulation window, showing about 0.2% DC variation in v_O (Fig. 6.14).



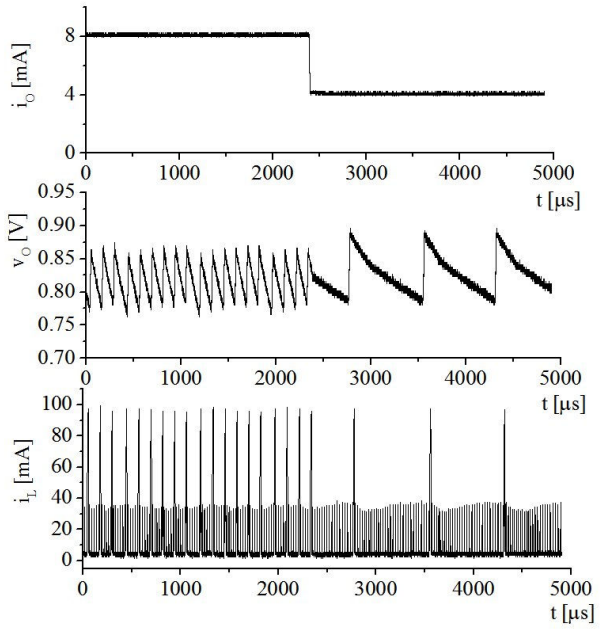
(a) (b)

Figure 6.14. Load regulation performance within Light-Load Mode in (a) rising and (b) falling load dumps.

Heavy-load Mode: In heavy-load mode, the energy source first engages to supply its entire power to load, and then the power source engages using the rest of the period to supply an additional power, as shown in Fig. 6.6. In measurements, the energy packet from v_{PS} was established at a much higher value than simulation, which was enough to satisfy v_O for several consecutive cycles, and therefore led to pulse-skipping operations from v_{PS} (Fig. 6.15) Therefore, the voltage ripple in v_O during heavy-load mode was higher at about ±25 mV than that of light-load mode. However, the converter showed only about 2.5% (20 mV) DC variations in v_O when the load changes from 4 mA to 8 mA and back to 4 mA.



(a)



(b)

Figure 6.15. Load regulation performance within Heavy-Load Mode in (a) rising and (b) falling load dumps.

Mode Transitions: Fig. 6.10a shows the mode transition from light-load mode to heavy-load mode, when the load changes from 0.1 mA to 8 mA and back to 0.1 mA. During the first cycle in heavy-load mode, because v_O is low, v_{PS} starts to engage and v_O comes back near to the reference value. When the load decreases back to 0.1 mA in heavy-load mode, v_O starts to increase and v_{PS}-energizing event is not triggered because the output of CP_{HV} is high all the time (Fig. 6.10b.) Then v_O settles within the regulation window of light-load mode with the power from the energy source only. This method reduces the system's complexity by not directly sensing the load, but the response time can be longer (about 200 µs in both transitions), being a function of output capacitor, load current, and the mode transition limits.

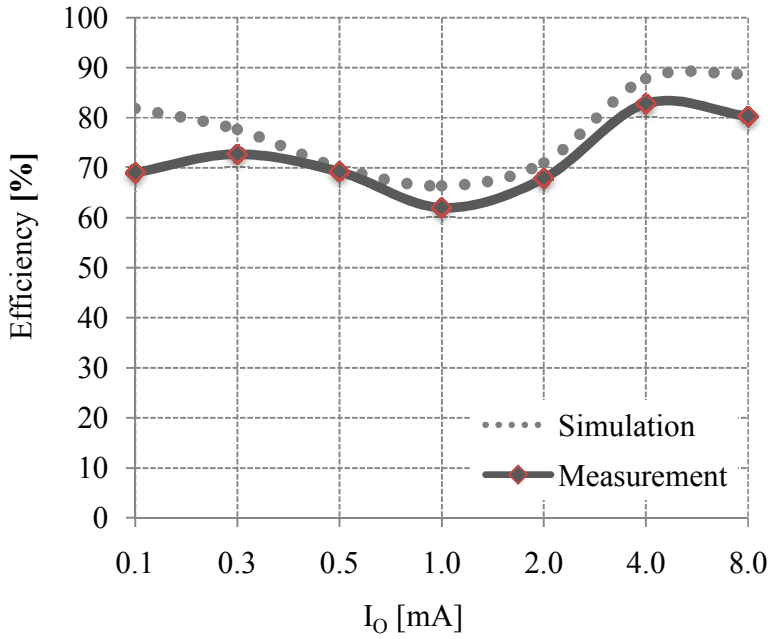


Figure 6.16. Efficiency of the converter across i_O.

6.3.2. Power-conversion Efficiency.

In Light mode, as the input power P_{ED} is divided into v_O and v_{PD}, the efficiencies to v_O and to v_{PD} becomes

$$\eta_{LM.O} = \frac{P_O}{P_{ED} + P_{VDD}}, \tag{6-2}$$

$$\eta_{LM.PD} = \frac{P_{O.PD}}{P_{ED} + P_{VDD}}, \tag{6-3}$$

where P_{ED} is v_{ED}'s input power, P_{VDD} is v_{PD}'s control power, P_O is the output power to v_O, and $P_{O.PD}$ is the power delivered back to v_{PD}. In Heavy Mode, as v_{PD} participates as another source, the power efficiency becomes

$$\eta_{HM.O} = \frac{P_O}{P_{ED} + P_{PD} + P_{VDD}}, \tag{6-4}$$

where P_{PD} is v_{PD}'s input power. Fig. 6.16 shows the measured and simulated converter's efficiencies across 0.1 ~ 8 mA's loads, peaking at 83% at 4 mA's load. The efficiency dip around 1 mA's load is due to high gate-drive losses, being optimized at higher current levels. The converter consumed 19.3 µW and 56.4 µW's control power in Light and Heavy modes, with more gate-drive powers needed to drive larger switches in Heavy Mode.

	[90] JSSC 09	[107] ISSCC 13	[108] ISSCC 11	First prototype	ESR-derived Hysteretic prototype	PWM-Hysteretic prototype
Topology	SIMO Buck-Boost	SIDITO Buck-Boost	SISO Boost	SIDIDO Buck-Boost	SIDIDO Buck-Boost	SIDIDO Buck-Boost
Efficiency at 0.1 mW	80%	83%	83%	4%	72%	70%
Peak Efficiency	93%	83%	87%	32%	73%	83%
Output Voltage	1.25	1, 1.8, 3	1.5, 3, 5	1.0	0.8	0.8
Load Dump	25 mV	–	–	60 mV	30 mV	40 mV
Output Capacitor	33 µF	–	–	0.1 µF	1 µF	1 µF
Load Range	0 – 125 mW	0 – 10 mW	0 – 10 mW	0 – 1 mW	0 – 8 mW	0 – 8 mW
Inductor	10 µH	–	1000 µH	150 µH	50 µH	50 µH
Process	0.25 µm	0.18 µm	0.25 µm	0.5 µm	0.18 µm	0.18 µm
Sources required to sustain the 0.01 – 4 mW's load for 1 month (72 µW Ave.)	430-mg DMFC Or 326-mg Li Ion	482-mg DMFC Or 314-mg Li Ion	460-mg DMFC Or 314-mg Li Ion	1.3-g DMFC + 63-mg Li Ion Tot.: 1.37 g	72.5-mg DMFC + 27.4-mg Li Ion Tot.: 99.9 mg	74.5-mg DMFC + 24.1-mg Li Ion Tot.: 98.6 mg

Table 6-1. Performance Summary of the Low-ESR Variant of PWM-Hysteretic System and comparison against the first prototype, the ESR-derived charger-supply system, and the state of the art

6.3.3. Performance Comparison

The main idea of this converter is to draw low, average power from an energy-dense source and engage a power-dense device only for higher power so that it can avoid the situations where a single source should be oversized to meet conflicting power and energy

requirements in high peak-to-average loads. Although the state-of-the-art converters in [90],[107]-[108] have good efficiency performances, they cannot avoid oversizing either the energy-dense source or power-dense source to meet peak power or lifetime demands, because they lack the load-dependent source-selection controls. For example, [90] needs 430-mgs of DMFC to be able to supply the peak load at 4 mW, or 326-mgs of Li Ion to support 72 μW's average load for one month, and the converters in [107]–[108] requires similar amount of sources (Table I.) On the other hand, the converter in [115], which is the first prototype discussed in Chapter 4, was able to selectively draw low power from the energy-dense source and high power from the power-dense counterpart. Yet it required total of 1.37g of sources to sustain the same load due to low efficiency performance, not being able to fully exploit the benefits of the control. The low-ESR variant of PWM-Hysteretic converter, however, requires only 74.5 mgs of DMFC to sustain the load for one month and 24.1 mgs of Li Ion to supply the peak load, the total of which is less than 31% of that required in the converters in [90],[107]-[108]. This number is still lower than that of the hysteretic converter in [116], because the peak efficiency of [116] is lower due to higher switching losses in hysteretic-controlled heavy loads.

6.4 Summary

The low-ESR PWM-Hysteretic system replaces the hysteretic output control in Heavy mode with PWM output control, to make the control less dependent on the parameter of the output capacitor and therefore more efficient in wider application areas. This IC similarly draws a pre-defined constant power from an energy source all the time and controls the

output power adaptively to loads, either by re-directing the excess power to the power source at light load, or by increasing power from the power source to supply heavier loads. This converter uses a single, 50μH off-chip inductor in three different power paths by sharing it at different times, achieving the maximum efficiency of 83%, which is more efficient than the ESR-derived nested hysteretic charger-supply system. This difference comes from the fact that the number of switching events to deliver the same load is reduced to one in this IC, while the ESR-derived charger-supply system had to energize three to four times to deliver the same load because the peak current is the function of the ESR of the output capacitor. This benefit leads to the reduction in the sources to sustain the suggested load profile, requiring only 23% of the sources that the state-of-the-art converters need, which is also 1.3%'s reduction from what the ESR-derived system requires. However, the transient response of this PWM-Hysteretic system is still slower than that of the ESR-derived charger-supply system, which can respond to load dumps within one or two switching cycles due to hysteretic control.

Chapter 7. Final Summary and Conclusions

7.1 Research Objective

Micro-scale electronic systems have a vast application area emerging in military, utility, biomedical, and environmental monitoring fields where they can greatly enhance human's ability to gather information with lower cost and better security. Of all the technological challenges that such systems encounter, one of the most demanding issue is the severely limited space that ultimately constrains the operational lifetime and the functionality. Taking into account the fact that there is no perfect single energy source that promises both high energy and power density at the same time as given by the Ragone plots, using a hybrid mixture of one energy-dense source and the other power-dense source can provide the smallest optimum solution given the specific targets in the operational lifetime and the maximum power of a micro-scale electronic system. The power supply circuit interfacing with the hybrid sources should be able to condition power and energy from them to supply the output and redirect the unused energy back to a power cache efficiently, without burdening the system's area. Although the state-of-the-art converters addressed the issues regarding sharing one inductor in multiple power paths and selecting the active input from its availability, the idea to select the input sources with respect to the loads and mix the power efficiently to supply the load is largely absent in literature, which is why this research is focusing on the subject.

7.2 Conclusions

The first prototype, the single-inductor fully-hysteretic charger-supply system, was designed and fabricated in the 0.5-μm CMOS technology, to prove the functionality that it can draw a low, average load power from an energy source and a higher, peak load power from a power source, while supplying a time-varying load of 0.1 – 1 mA. This converter demonstrated an intelligent, load-dependent, and dynamically adaptive feedback control which automatically selects the optimum source from a hybrid combination of an energy-dense source and a power dense source based on the load's needs. However, the converter consumed too much switching powers and control powers while operating in continuous conduction mode with a high switching frequency of 2.5 MHz. In addition, although the current-sensing method that directly senses the inductor current with a series resistor was effective in controlling the average inductor current, it consumed too much power in the fast amplifier, limiting the measured efficiency of the converter at 32% across the load range and 4% at 0.1 mW. To supply the example load profile in Fig. 5.19 for one month, this converter required 1.3-g DMFC with 63-mg Li Ion, 1.37 g in total, which is given by (7-1.) This number exceeds those required by the state-of-the-art converters in [90],[107]-[108] (from 314 mg to 482 mg) by far, because this converter was not able to benefit from the load-dependent source-selecting control mainly due to low efficiencies (Table 7-1.)

$$W_{TOT} = W_{FC} + W_{LI}$$

$$= \frac{P_{O(AVG)} t_{1\text{-MONTH}}}{\eta_{C(AVG)} ED_{FC}} + \frac{P_{O(PK)}}{\eta_{C(PK)} PD_{LI}} \tag{7-1}$$

	[108] ISSCC 11	First Prototype	Second Prototype	
			ESR-derived Hysteretic	PWM-Hysteretic
Topology	SISO Boost	SIDIDO Buck-Boost	SIDIDO Buck-Boost	SIDIDO Buck-Boost
Efficiency at 0.1 mW	83%	4%	72%	70%
Peak Efficiency	87%	32%	73%	83%
Output Voltage	1.5, 3, 5	1.0	0.8	0.8
Load Dump	–	60 mV	30 mV	40 mV
Output Capacitor	–	0.1 µF	1 µF	1 µF
Load Range	0 – 10 mW	0 – 1 mW	0 – 8 mW	0 – 8 mW
Inductor	1000 µH	150 µH	50 µH	50 µH
Process	0.25 µm	0.5 µm	0.18 µm	0.18 µm
Sources required to sustain the 0.01 – 4 mW's load for 1 month (72 µW Ave.)	460-mg DMFC Or 314-mg Li Ion	1.3-g DMFC + 63-mg Li Ion Tot.: 1.37 g	72.5-mg DMFC + 27.4-mg Li Ion Tot.: 99.9 mg	74.5-mg DMFC + 24.1-mg Li Ion Tot.: 98.6 mg

Table 7-1. Performance Summary of the tested prototype ICs.

The next step in this research was therefore to investigate the origin and the characteristic of each power loss in a general inductor-based switching converter, and to apply the information in building an improved control to achieve a better performance – efficiency. For that purpose, all important power losses are first characterized and grouped together with respect to their relations with the important parameters – the switching frequency and the load current. It was shown from the analyses that in micro-power regions where the frequency-dependent switching losses dominate the load-dependent conduction losses, operating the converter in discontinuous conduction mode with a lower switching frequency can greatly reduce the overall power losses. In addition, the conduction losses and the gate-drive losses of an integrated power transistor, being the two most important loss contributors in general switching converters, can be optimized by selecting the size of the transistor to achieve the minimized sum because the former is inversely proportional to

it while the latter is proportional to it. Then, the question becomes how the process technology and parameters affect these individual losses and efficiency, because optimizing the process parameters can overcome the efficiency limit, which cannot be achieved just by the proper design of the power switches.

The various process parameters such as the maximum voltage, the threshold voltage, the oxide capacitance, the thickness of the oxide, and the transconductances individually affect the power losses. However, as all these process parameters are strong functions of the minimum channel length, all important power losses can be characterized with respect to this most important process parameter – the minimum channel length. Under the assumptions that the power switches are optimally designed to balance the conduction and gate-drive losses, and the leakage losses are not pronounced compared to the switch-related losses, the sum of the conduction and drive losses become proportional to $L_{MIN}^{1.5}$, meaning that the efficiency can be always higher in shorter channel-length technologies. The discussion goes further to the point that using series power switches to overcome the lower voltage ratings with the shorter channel length can be more efficient than using a single switch with a longer channel, because the quadratic fall in drive power resulting from a lower gate-drive voltage more than offsets the linear rise in conduction power.

The next prototype designed with 0.18-µm CMOS technology applied the findings from the power loss and efficiency analyses to address the performance issue raised in the first prototype. This new converter operates in discontinuous conduction mode with a lot lower frequency of 40 kHz, and the direct current-sensing technique that led to a high quiescent

power has been eliminated. Instead, the peak current from the energy source is set by the fixed energizing time, and the peak current from the power source is indirectly set from either by ESR-dominant hysteretic control, or PWM control. Therefore, the new converter had two different variations in terms of control, the ESR-dominant hysteretic variant and the low-ESR variant of PWM-hysteretic system.

The former system is a single-inductor fully-hysteretic converter, which effectively regulates the inductor's peak current by controlling the ESR-dominated output voltage with the hysteretic control in discontinuous conduction mode. One important merit of this hysteretic control over the PWM-based control is the fast response time to load variations within a clock cycle. As this method does not require an error amplifier and resulting compensation networks, the circuit complexity is greatly reduced, as long as the output voltage is dominated by the ESR portion of the output capacitor as explained in Chapter 5.

This hysteretic dual-source single-inductor supplies 0.5 – 8 mA and regulates the output to 0.8 V within 1.5%'s ripple, with peak efficiency of 73%. With 72%'s efficiency at 0.1 mW's load and 73%'s peak efficiency, this converter requires 72.5-mg DMFC along with 27.4-mg Li Ion, in total 99.9 mgs, to supply the example load. Although this converter shows lower efficiencies when compared to the state-of-the-art converters in [90][107]-[108], this converter needs less than only 31.8% of the sources that they require, because it can selectively draw a low power from the energy source and engage the power source only for the higher loads, and therefore can avoid oversizing the energy source for the peak

power or the power source for the lifetime. Another benefit of this hysteretic converter is the fast response time, which can respond to load dumps within one switching cycle.

One weakness of this system, however, is that the stability and control heavily relies on the ESR of the output capacitor, which may limit the application of this technology. From the control's perspective, the high ESR directly limits the peak current from the power source, which will also limit the size of the individual energy packet. Then the system needs to draw multiple numbers of energy packets from the power source to supply a heavy load, which will increase switching power losses and make the system less efficient. For example, this converter, with 0.1 Ω's ESR, required two to three energy packets per one clock period in Heavy mode, resulting in increased switching losses. Therefore, this shows the inevitable trade-off between the stability and performance in ESR-dominant hysteretic converters.

The latter system, low-ESR variant of PWM-hysteretic system, overcomes the constraints on the ESR of the output capacitor by using the PWM voltage control in discontinuous conduction mode. The converter still draws a constant power from the energy source with the fixed peak current, but it draws a variable energy packet with the PWM voltage controller to supply a higher load. This converter reached the efficiency of 70-83% in delivering 0.1 to 8mW loads from dual sources, showing a steady-state ripple of 25 mV and 20 mV's voltage regulation under the load transients of 4 to 8 mA. With these numbers, this converter can support the same example load for one month with 74.5-mg DMFC and 24.1-mg Li Ion, in total 98.6 mgs of sources. This is about 1.3%'s reduction

from the ESR-dominant hysteretic-mode converter, because the PWM control allowed only one energy packet from the power source per one switching period, and therefore had lower switching losses than the ESR-dominant hysteretic converter. By using the efficient load-dependent source-selecting control, this converter can supply the same load in Fig. 5.19 with only 31.4% of the sources that the state-of-the-art converters require.

7.3 Contributions

7.3.1. Main Contribution

The main contribution of this research is an area- and energy-efficient power-mixing technique for mixed sources, which will reduce the required sources' volume and eventually extend the operational lifetime of self-powered miniature systems. This technique shows significant reduction in sources' volume especially when the load has a high peak-to-average power ratio, which is frequently seen in many electronic systems. The reduction ratio becomes higher for mixed sources with complementary energy and power characteristics: the farther they are placed in the Ragone plot, the higher reduction ratio this technology can achieve.

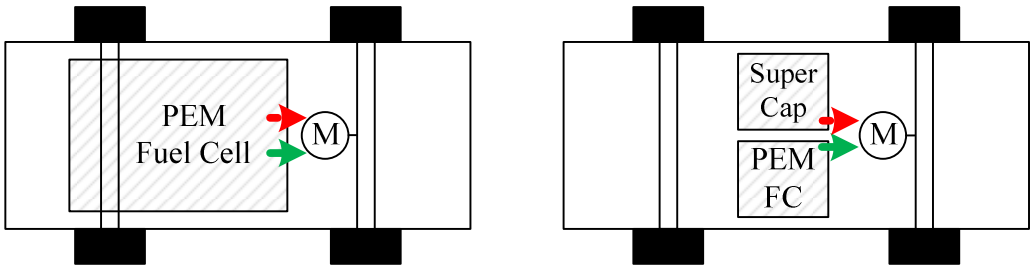
The original motivation of this research was to optimize the volume of a micro-scale electronic system which is powered by micro sources, and therefore the direct methanol fuel cell was introduced as the energy source, because it is suitable for portable power applications (Table 7.2.) However, other fuel cell technologies with higher power outputs can also benefit from this research. For example, Proton exchange membrane (PEM) fuel cells are good candidates for powering fuel cell electric vehicles, generating from 1 to 100

	Electrolyte	Catalyst	Fuel	Typical Power	Temperature	Application
Direct Methanol Fuel Cell (DMFC)	Polymer membrane	Platinum-Ruthenium / Platinum	Methanol	< 250 W	60-130C	Portable power applications
Proton Exchange Membrane Fuel Cell (PEMFC)	Acidic polymer membrane	Platinum-based on both electrodes	Hydrogen	1 kW – 100 kW	< 100C	- Fuel cell electric vehicles - Backup power
Alkaline Fuel Cell (AFC)	Alkaline solution	Nickel	Hydrogen + Oxygen	10 kW –100 kW	70C	- Military - Space program
Phosphoric Acid Fuel Cell (PAFC)	Liquid Phosphoric acid	Platinum	Hydrogen	100 kW – 400 kW	180C	Stationary power generation
Solid Oxide Fuel Cell (SOFC)	Solid ceramic	Not needed	Methane	1 kW – 2 MW	800-1000C	Stationary power generation
Molten Carbonate Fuel Cell (MCFC)	Molten Carbonate salt	Not needed	Methane	300 kW – 3 MW	650C	Fuel cell power plant

Table 7-2. State-of-the-art Fuel Cell Technologies and Applications

kW's output power. The electric motor in an electric vehicle shows a time-varying load profile, as the engine accelerates and brakes in real-time road conditions. The required torque of the motor, which is proportional to the current through it, also changes fluctuates with roads, requiring wide range of currents from the energy source. If the vehicle relies only on a PEM fuel cell, then the fuel cell should be oversized so that it can also sustain the peak power and torque of the motor, as shown in Fig. 7.1a. And the huge volume and high price of the PEM fuel cell has been the serious bottle neck in commercializing fuel cell vehicles. However, if a PEM fuel cell is only used for lower powers while a super capacitor

is adopted to supply high powers, then the required sources' volume to sustain the same load will be reduced by much, as shown in Fig. 7.1b. The control ability to directly draw low loads from the PEM FC can increase the overall fuel efficiency, because it removes the efficiency penalty in recharging the super capacitor from the PEM FC.



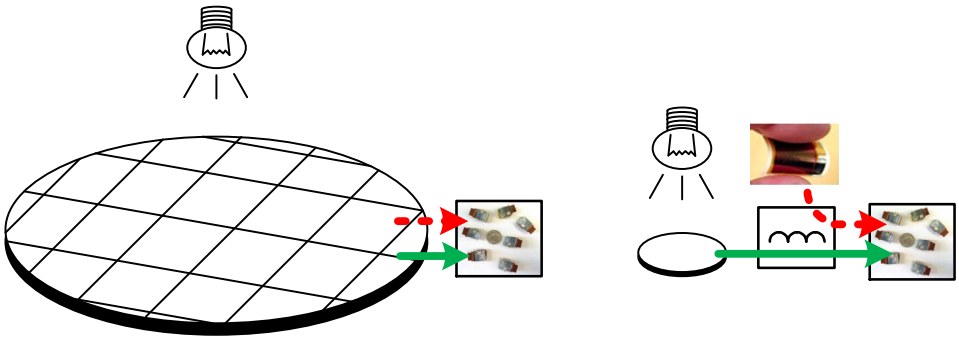
(a) Oversized PEM Fuel Cell in Fuel Cell Car

(b) Hybrid Fuel Cell Electric Car

Figure 7.1. Expected Contribution of this Technology in Hybrid Electric Vehicles

This technique can contribute to volume reductions in energy-harvesting applications as well. As the Ragone plot in Fig. 1.6 indicates, the harvesting sources have virtually unlimited energy densities, provided that the source of excitation is there. Although these sources are relatively free from the concerns about the operational lifetime, their power densities are generally less than those of fuel cells and batteries. For example, an indoor light can source less than 10 μW per 1 cm^2, and therefore needs to be oversized to 400 cm^2 to successfully supply the peak load of 4 mW. However, if this technology is applied to utilize the Li Ion battery for the power source, then only 10 mg's Li Ion battery will suffice to the same peak load, as shown in Fig. 7.2. The thermal harvesting sources and piezoelectric sources can similarly benefit much from using this technology, because they

lie very close to the y axis of the Ragone plot – the energy axis - and have complementary energy / power characteristics to power-dense sources.



(a) Oversized Solar Panel (b) Hybrid Solar Panel – Li Ion

Figure 7.2. Expected Contribution of this Technology in Indoor Light Harvesting Applications

7.3.2. Other Contributions

7.3.2.1. Nested-Hysteretic Voltage Control

A nested-hysteretic voltage control by using two hysteretic comparators with different regulation windows is proposed in this research to implement the power-mixing technique. This technique provides a very compact solution in regulating a voltage output, because it only needs two hysteretic comparators with different hysteretic windows. In addition, this does not need an external compensation network. Therefore, this technique can be very useful in applications with severe volume constraints, such as biomedical implants, where additional external component significantly burdens the compactness of the whole system. This technique also shows a fast one-cycle recovery from using hysteretic controls, which make it more suitable for biomedical implants, where they consume a dynamic, fast power in sensing, actuating, transmitting and receiving, etc.

7.3.2.2. Automatic Mode-Transition Control

This technique senses the output voltage with a hysteretic comparator to change energy flows so that the converter supplies just enough power to a time-varying load. Instead of directly sensing the load for mode transitions, the converter waits until the integrated effect of the load changes appear on the output voltage, and then automatically changes its mode. As the converter does not change its mode with respect to rapid changes in the load itself, it can avoid false transitions for load transients, which can be safely taken care by the output capacitor, without having to switch between the two modes consuming unnecessary power. Therefore, this technique can be beneficial for electronic systems where the loads are fast and unpredictable. For example, the motion sensors which detect random vibrations from the environment, can stay in a low-power mode even with a few sporadic vibrations, while changing into a high-power mode only when the high vibrations start to appear continuously.

7.3.2.3. Analyses on Power-Loss Mechanisms in a Switching DC-DC Converter

The detailed exposition of various power loss mechanisms in a switching DC-DC buck converter with respect to the switching frequency and the load current will be another contribution of this research, because this can provide a starting point in the analytic studies in any high-efficiency switching converter designs. The loss analyses cover most of the important power loss mechanisms that affect the overall efficiency of general switching DC-DC converters, including the conduction losses, the gate-drive losses, the IV-overlap losses, the dead-time conduction losses, the shoot-through losses, and the control quiescent losses. The relationship of each loss with the load current and the switching frequency,

which is detailed in this research, will be useful in designing power switches and gate drivers, control blocks, and in deciding the switching frequency to achieve high efficiency in the interested load range. Switching converters in micro-watt regions can benefit more from this analysis, because that is where the control and switching powers become a bigger portion of the entire losses and therefore should be balanced with the conduction losses.

7.3.2.4. Analyses on how the Selection of Process Technology Affects Efficiency

Selection of a process technology impacts all the important power loss mechanisms in switching DC-DC converters, and sometimes limits the maximum achievable efficiency. Therefore, knowing how the process affects the converter's individual losses and efficiencies in the early period of design is important, because it will save a lot of design time by not having to go back and change the process technology in the later stage so that the design can achieve a higher efficiency. The result of the analyses implies that a finer channel-length technology can achieve a higher efficiency, as long as the other parameters are optimized and the leakage portion of losses is not dominating. The analyses further suggest using series stacked power switches to overcome the low voltage ratings of a finer process technology for high efficiencies. These results can contribute to the design of fully-integrated switching DC-DC converters with digital cores, where all digital blocks and power converters share the same die and technology. This integration effort has been made especially in the design of power management units for application processors for smart phones and tablet PCs, where the finest process technology is used to build power converters as well as the digital cores.

No.	Major Contribution
0	An area- and energy-efficient power-mixing technique for hybrid sources.
	Related Contributions
1	A nested-hysteretic voltage control by using two hysteretic comparators with different regulation windows.
2	A load-dependent, automatic mode-transition control between light- and heavy-mode operations.
3	A detailed exposition of various power-loss mechanisms in a switching DC-DC buck converter and their relations with the switching frequency and the load current in both CCM and DCM.
4	A detailed exposition of how the selection of process technology affects the various power-loss mechanisms and the efficiency in a switching DC-DC converter.

Table 7-3. Contributions of the research.

Below is the list of peer-reviewed journal publications and conference publications that this research has generated so far. This contains two published journal papers and two submitted journal papers, and five published conference papers.

Peer-Reviewed Journal Publications

[1] S. Kim and G.A. Rincón-Mora, "Achieving High Efficiency under Micro-Watt Loads with Switching Buck DC-DC Converters," *Journal of Low Power Electronics (JOLPE)*, vol. 5, no. 2, pp. 1-12, August 2009.

[2] S. Kim and G.A. Rincón-Mora, “Single-Inductor Fuel Cell-Li Ion Charger-Supply IC with Nested Hysteretic Control,” *Analog Integrated Circuits and Signal Processing (AICSP)*, vol. 70, no. 1, pp. 33-45, Jan. 2012.

[3] S. Kim and G.A. Rincón-Mora, “Dual-source Hysteretic Switched-inductor 0.18-µm CMOS Charger-Supply System,” *Submitted to IET Circuits, Devices & Systems*, April 2014.

[4] S. Kim and G.A. Rincón-Mora, “83% Efficient 0.1-6.4-mW PWM-Hysteretic Dual-Source 0.18-µm CMOS Charger-Supply,” *To be submitted*, May 2014.

Peer-Reviewed Conference Publications

[1] S. Kim and G.A. Rincón-Mora, “Single-Inductor dual-input dual-output buck-boost fuel-cell-Li-ion charging dc-dc supply,” in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 444-445.

[2] Rajiv Damodaran Prabha, G.A. Rincón-Mora, and Suhwan Kim, “Harvesting Circuits for Miniaturized Photovoltaic Cells,” *IEEE International Symposium on Circuits and Systems*, pp. 309-312, May 2011.

[3] S. Kim, G.A. Rincon-Mora, and D. Kwon, "Extracting the frequency response of switching DC-DC converters in CCM and DCM from time-domain simulations," *IEEE International Systems-on-Chip Design Conference (ISOCC)*, Jeju, Korea, Nov. 17-18, 2011.

[4] S. Kim and G.A. Rincon-Mora, "Efficiency of Switched-Inductor DC-DC Converter ICs Across Process Technologies," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Seoul, Korea, May 20-23, 2012.

[5] S. Kim and G.A. Rincón-Mora, "Dual-source single-inductor 0.18-µm CMOS charger-supply with nested hysteretic and adaptive on-time PWM control," accepted to *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 9-12, 2014.

7.4 Technological Limitations

7.4.1. Performance

One of the most important performance metrics is the efficiency, because this directly affects the operational life and functionality. And the efficiency performance is basically limited by the selection of the silicon process technology, as discussed in the chapter 3. For example, an inductor-based switching DC-DC converter from 1 V's input to 0.5 V's output supplying 30 µA – 8 mA's loads, showed that it can achieve a higher maximum efficiency as the channel length of the technology decreases, as shown in Fig. 2.13. In other words, the charger-supply ICs that have been designed in the 0.18-µm technology could have actually resulted in a higher efficiency if designed in a finer technology, as long as the breakdown voltage have been properly addressed in the design. The breakdown voltages of the silicon technologies tend to decrease as the minimum channel length becomes shorter, as shown in Table 2-1. To overcome this, stacking power transistors in series can be a good solution, as the linear increase in the conduction losses can be compensated by the quadratic decrease in the drive losses, under the assumption that the additional losses in the

dedicated gate-drive circuits do not nullify the benefits. However, the leakage losses, which become worse in finer technologies but were not dominant in 0.18 μm technology, will ultimately limit the minimum channel length that can be used in the design.

There is also an inherent trade-off which limits the maximum efficiency in designing an integrated power switch in every dc-dc switching converters: the conduction losses and the drive losses. As the former is inversely proportional to the width of the power switch while the latter being proportional to the same width, the sum of two losses should have a minimum achievable value that are fixed by process parameters regardless of the design. This limitation comes from the basic operation of every switching converter: the converter should periodically make a low-resistive power path to flow the inductor's current by turning power switches on, which inevitably requires energy every time it switches, unlike linear regulators. One way to reduce the on resistance of power switches without increasing the size is to always use NMOS transistors, because they have lower resistance due to high mobility, given by

$$R_{ON} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_T)}, \tag{7-2}$$

where μ_n is electron's mobility, C_{OX} is the unit oxide capacitance, W and L are the width and length of the power switch, V_{GS} is the gate-to-source voltage, and V_T is the threshold voltage. In this converter, the PMOS switches S_{PE} in particular, can be converted into NMOS transistors and be driven by the bootstrap gate-drive circuits shown in Fig. 7.3, because they conduct the highest currents in heavy mode. The negative terminal of the

boot-strap capacitor C_{BST} is always connected to the switching node. The positive terminal of C_{BST}, however, is connected to V_{PD} when the switching node is at ground (i.e., when S_{DE} is conducting in the de-energizing event), and when S_{PE} is about to turn on, it connects to v_{GD} to provide the sufficient gate-drive voltage of V_{PD} when S_{PE} is on. This technique can reduce the on resistance of the switch S_{PE} to about 1/3, without increasing the size of the power switch and therefore the related switching losses.

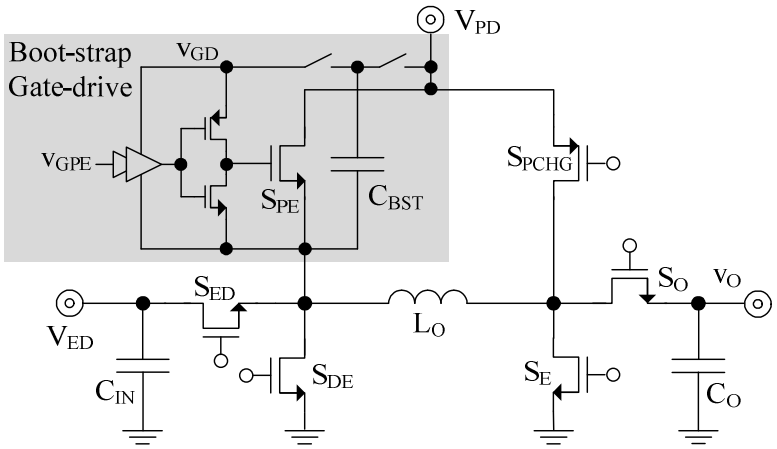


Figure 7.3. Boot-strap Gate-Drive Circuit for the NMOS switch S_{PE}.

From the control's perspective, there is another inherent trade-off in a switching converter's performance: a switching frequency and a ripple. As the individual switching operations require a fixed amount of energy, reducing the average number of switching events will result in the reduction of the switching losses. However, as the amount of energy should increase to deliver the same amount of power with a slower latency, the ripple in the output, which translates into the accuracy of the converter, will inevitably become worse. Therefore, the optimized design of a switching converter will choose the

maximum amount of energy delivery per a switching event that meets the output-ripple requirement, which will reduce the switching frequency down just to be enough to deliver the load demand. For the ESR-dominated hysteretic converter, the ripple may not increase as the function of the switching frequency, because the ripple is tightly regulated by hysteretic control. Instead, a higher ESR means a lower peak current and therefore a smaller energy packet, increasing the number of switching events and degrading the efficiency.

7.4.2. Functionality

The main functionality of this technology is to supply a low, average load from an energy-dense source and recharge a power cache with remnant energy, and mix power from both the energy-dense source and the power cache to supply a high, peak load. The main output voltage is tightly regulated by either hysteretic or PWM control, as explained in the previous chapters. The second output – the power-dense device – is not being regulated and operates as a low-impedance power sink for remnant inductor's energy after satisfying a low load. However, as the second output needs to supply the system's internal rail being the highest with the nominal value of 1.8 V, it needs to be controlled within a range where the control circuits do not fail due to either under voltage or over voltage conditions. One simple solution is to monitor the voltage of the power cache by a hysteretic comparator. Then, another question arises: what needs to be done in case the voltage of the power cache fails?

This question is also valid at the start-up conditions. Unlike the energy-dense sources, the power caches are more likely to carry much less energy on them before the system is up and running, and therefore cannot provide an enough output voltage to power the system during the startup. For example, the super capacitors will always start from zero when the system is starting. Therefore, the system should have a functionality that it can use the energy-dense source as its internal supply and charge the power cache until it is ready to power the system at its optimum condition. Fig. 7.4 shows such implementation of the supply-voltage selector. For example, when the power source's voltage v_{PD} is low during the start-up or due to the excessive discharge, then the comparator's output goes to low and connects the energy source's voltage v_{ED} to the system supply voltage v_{DD}. When v_{PD} is recharged from the energy source and becomes ready, then the comparator's output goes to high and v_{PD} connects to v_{DD} again to function as a system's supply. As the higher v_{DD} means less resistance in power switches, the use of v_{ED} as a system's supply should be limited only to the cases where v_{PD} is discharged lower than v_{ED}.

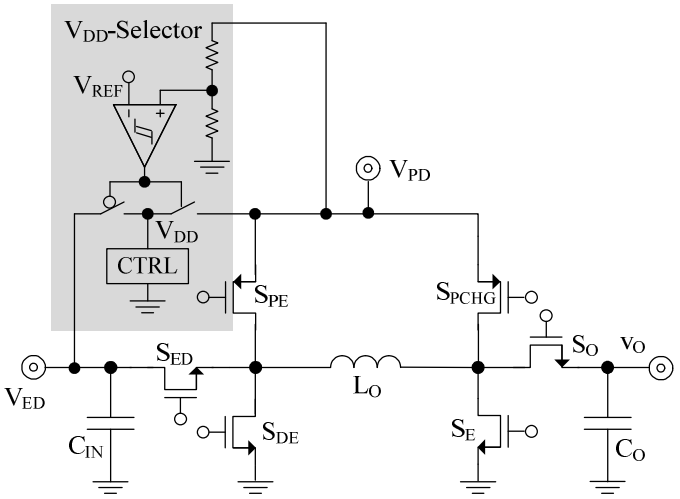


Figure 7.4. Supply-voltage selector between the energy source and power source.

In this research, however, the more important question to focus was how to mix energy from the dual sources, supply the output, and charge the power cache in steady-state conditions. Therefore, the power source has been pre-charged to 1.8 V using an external circuit, assuming that it has a valid voltage at start-up. In a complete hybrid-supply system, however, the functionality that the energy source replaces the power cache's role and provides the control power should be addressed.

Another functional limitation comes from the fact that this converter continuously draws power from the energy source all the time, even when the load at v_O or the power source does not need additional power. The current control scheme for the Light mode is that whenever the load at v_O is satisfied, the control redirects all the inductor's remnant energy to the power source to recharge it. And this becomes problem when the power source is already fully charged and should not accept more energy.

In this case, there are two general ways of approaching this problem. First one is to keep drawing a constant power all the time, and discard it when not needed. This can be easily done by adding a free-wheeling switch in parallel with the inductor and burning the remnant energy by shorting the inductor. The problem of this approach is that when the load is kept light for a long period of time, then the converter will drain the energy continuously for nothing. Second one is to shut down the energy source when not needed, and to turn on only when the system needs the power. The problem of this approach is that in some energy sources, the time constants in turning on and off are high on the order of

minutes and even hours. Considering all these, the ideal approach would be a mixture of these two solutions, based on the estimated load profiles in a long-time period: activating the energy source when the load is active, but shutting it down when a long inactive period is expected.

7.5 Future Research Directions

7.5.1. Adding an Optimum-Power-Tracking Loop for the Energy Source

One of the important assumptions of this technology is that the system draws a constant, optimum power from the energy-dense source continuously. This optimum power point has to be at the most efficient point or the maximum power point from the energy source, because it will ultimately extend the system's operational lifetime (Fig. 7.5.) In this technology, it was assumed that the optimum point of the energy source is pre-determined by its voltage-current characteristic and it is not changing with time, and the converter is conditioning the source at the desired power point by periodically drawing a constant-peak energy pulse. However, in many cases, the optimum power point does change with time, temperature, state-of-charge, etc. Therefore, designing a dedicated control loop to track the optimum operation point of the energy source would be an important research path, because it will result in better utilization of the given energy.

Fig. 7.6 shows a conceptual control to condition the output voltage of the energy source to the desired optimum voltage that the energy source requires. The current from the energy source can be effectively controlled by adjusting the energizing time τ_{EN} and therefore the peak current from the energy source, which is set to a fixed value in this research so far.

When the output voltage of the energy source is higher than the optimum value, the control should increase the energizing time from the energy source, which will bring the voltage down near to the target value, and vice versa. Regulating the output power at its optimum point will impact the overall efficiency in power generation from the energy source, and investigating the power converter's role in improving the overall efficiency will be a good research direction from this work.

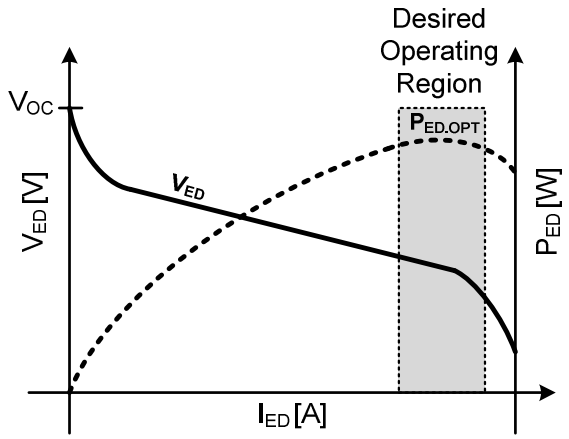


Figure 7.5. Desired operating region of an energy source from IV characteristics.

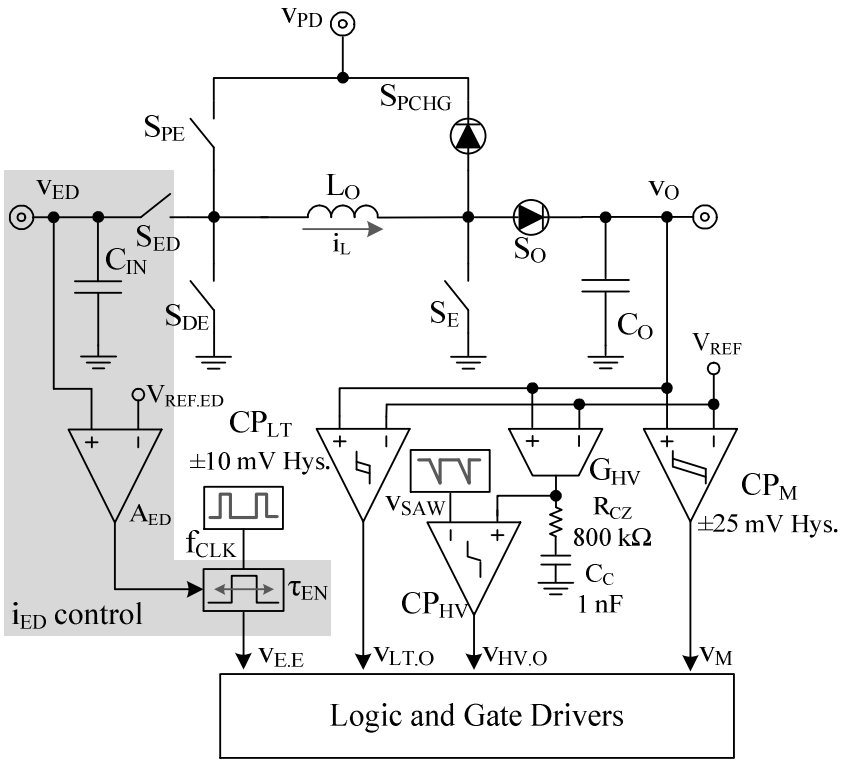


Figure 7.6. Dedicated Control Loop to Condition the Energy Source

7.5.2. Adding a protection / regulation control for the power source

The power source v_{PD} in this research is a low-impedance output which absorbs the remnant energy from the energy source, and it is neither protected nor regulated. However, maintaining the power source's voltage within the minimum and the maximum allowed value is important, because it powers the system's control and should not be overcharged or undercharged. The protection circuit against overcharging events is needed both for the power source itself and for the control circuits with the maximum rated voltage. In such situations, the control needs to decide whether to burn the inductor's energy in the inductor, or to stop drawing additional power from the energy source.

For this purpose, a hysteretic comparator to sense v_{PD} can be added, and when its output goes high, the control needs to decide either (a) to stop drawing additional power from the energy source, or (b) to start burning the inductor's energy by the free-wheeling switch S_{FW}. The selection of the method (a) is based on the assumption that the light-load condition should last long so that turning off the energy source should be more efficient even after considering the long time constants of the energy source. The selection of the method (b) should be taken when the load can come back anytime so the converter cannot wait for the long restart of the energy source. The overall efficiency of each method and the implementation of the control can be an interesting research path.

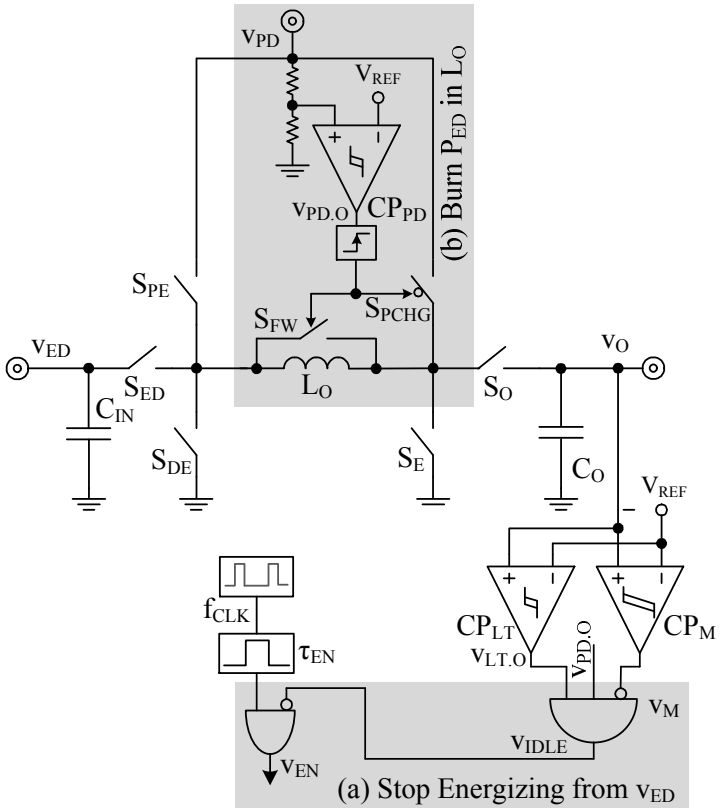


Figure 7.7. Over-Charge Protection Control for the Power Source

7.5.3. Low-Voltage Self-Start from an Energy-Harvesting Source

The energy harvesting source is the best candidate for the energy-dense source, because it has virtually unlimited energy density, provided that the source of excitation is always on. Considering the intermittent nature of a general harvesting source, having multiple input harvesting sources will enhance the reliability. In such systems, the initial startup from zero energy is not a trivial issue, because some harvesting inputs generate only a fraction of a threshold voltage of an enhancement–mode transistor, unlike in fuel cells or batteries. To overcome this, a low-voltage charger consisting of depletion-mode devices can be used to initially charge up the power source. After the power source is fully charged and it is ready to supply the system's control, then the low-voltage charger can turn off and the system can start its normal operations. When the system loses the power source's voltage due to excessive load dumps to the level where it cannot supply the control block, then the low-voltage charger turns on again to bring v_{PD} back. Designing the low-voltage charger with proper on/off controls for the initial start up and recovery operations can be one research path, which will widen the application of this technology to harvesting sources.

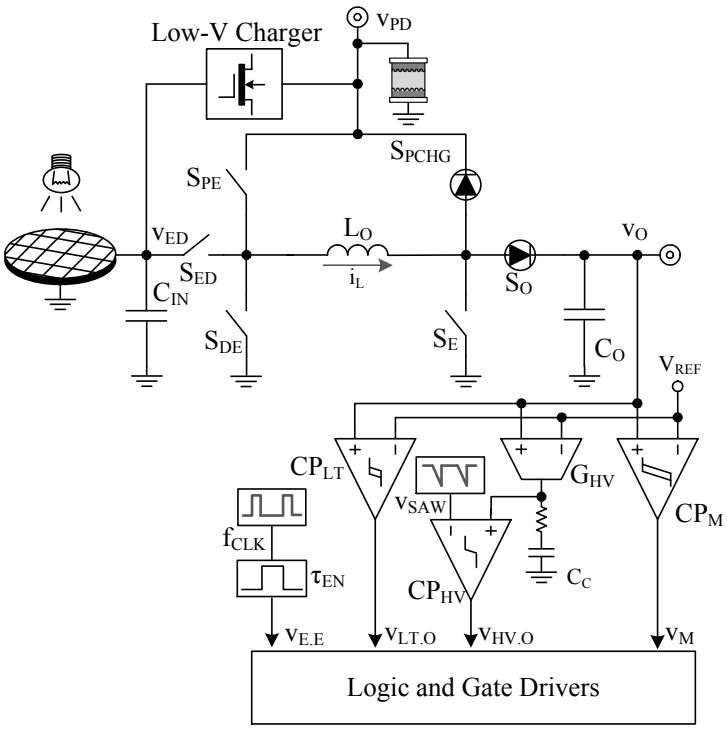


Figure 7.8. Low-Voltage Self-Start from an Energy-Harvesting Source

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