ADVANCES IN PANEL GLASS PACKAGING OF MEMS AND SENSORS FOR LOW STRESS AND NEAR HERMETIC RELIABILITY

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
Of the Requirements for the Degree
Master of Science in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2018

# ADVANCES IN PANEL GLASS PACKAGING OF MEMS AND SENSORS FOR LOW STRESS AND NEAR HERMETIC RELIABILITY

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To my beloved sister

ACKNOWLEDGEMENTS

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

MEMS based sensing is gaining widespread adoption in consumer electronics as well as the next generation Internet of Things (IoT) market. These applications serve as primary drivers towards miniaturization for increased component density, multi-chip integration, lower cost and better reliability. Existing MEMS packaging techniques like silicon wafer level packaging and laminate/ceramic substrate packaging either limit package level integration and miniaturization, are fabricated on small wafers or panels, or use materials that fail to decouple system level stress on the device, thereby risking its long-term reliability at board level. Besides, application specific packages take up the largest fraction of the total manufacturing cost. Therefore, advanced packaging of MEMS sensors for HPI plays a critical role in the short and long run towards the SOP vision.

This dissertation demonstrates a low stress, reliable, near-hermetic glass cavity MEMS package as a solution that combines the advantages of LTCC substrates and silicon wafer level packaging while also addressing their limitations. These glass based cavity packages can be scaled down to 2x smaller form factors (<500µm) and are fabricated out of large panel fabrication processes thereby addressing the cost and form factor requirements of MEMS packaging. Flexible cavity design, advances in through-glass via technologies and dimensional stability of thin glass also enable die stacking and 3D assembly for sensor-processor integration towards sensor fusion. The following building block technologies were explored: (a) reliable cavity formation in thin glass panels (b) low stress glass-glass bonding, and (c) high throughput, fully filled through-package-via metallization in glass. Three main technical challenges were overcome to realize the

objectives: (a) cavity corner cracking, side wall taper, side wall roughness and defects, (b) interfacial voids at glass-polymer-glass interface and (c) electrical opens and high frequency performance of copper paste filled through-package-vias in glass.

The first objective was to achieve cavities in thin glass panels with a focus on three main design metrics: a) side wall roughness for high reliability, b) side wall taper for RDL co-planarity and better electrical performance and c) surface roughness of cavity base for die pad-pad co-planarity and high assembly yield. Two types of cavity structures were explored: a) laminated glass cavities for excellent base surface smoothness, and b) blind cavities for easier integration of TPVs to enable 3D integration. These design metrics were optimized with the help of advanced, proprietary micromachining techniques from supply chain partners to achieve rounded cavity corners (100 µm corner diameter) to mitigate corner cracks, smooth side walls, low taper (< 2 µm) and smooth cavity base surfaces.

The second objective was low stress glass-to-glass bonding below 250ºC, to achieve high reliability using ultra-thin 5-10 um special polymer adhesives. Glass to silicon or glass to glass bonding has been reported using anodic bonding which requires alkali-based glass with sufficient electrical conductivity, or by high temperature or high cost direct glass to glass bonding. This research explored low moisture uptake and ultra-thin polymers to achieve near-hermetic glass to glass bonding of alkali-free glasses with low stress due to the low modulus of the polymer materials. The interfacial bond strength was characterized by die shear testing, and bonding efficiency was enhanced by process variations. Bond reliability was demonstrated by characterizing bond strength degradation after thermal cycling.

The third objective was to achieve fully-filled through-package-vias with low stress and yet high enough electrical conductivity in thin glass. Via filling has been achieved in the past by electrolytic copper plating requiring thin polymer stress buffer liners for high reliability, especially for larger vias. Sintering pastes (Ag, Pt) and conductive adhesives have also been widely used for through-via metallization, requiring high temperatures and long curing cycles. This research explored and demonstrated a high-throughput, low stress through-via metallization process using screen printing of conductive paste cured at less than 200°C, as an alternative to copper plating. Direct copper plating on glass results in thermomechanical reliability failures due to CTE mismatch between glass (3-9 ppm/°C) and copper (17ppm/°C). The CTE of copper paste can be modified by binders and additives for reduced CTE mismatch with glass. Moreover, the transition alloys that partially re-melt in the copper paste matrix act as stress sinks during thermal cycling, thereby mitigating reliability issues like interfacial delamination and cohesive cracking that are posed by copper plating. The via fill process parameters were optimized to demonstrate void-free filling for small (30 µm) as well as large (100 µm) vias. Conductive paste filled vias have higher electrical resistance compared to copper filled vias, and via design rules were established using electromagnetic modeling (ANSYS HFSS^{TM}) targeting Cu-via like performance at high frequencies. A hybrid structure involving conformal copper metallization followed by paste filling is being evaluated to achieve copper via like performance at high frequencies.

The following key engineering contributions were identified:

i)   Reliable, low defect, low taper cavity formation techniques in ultra-thin glass panels were explored, demonstrated and characterized.

ii)   Panel glass-glass bonding was demonstrated using ultra-thin, low moduli dry film polymer adhesives with low interfacial stress, ultra-high shear strength values and 100% bonding efficiency.

iii) Thermal cycle reliability of polymer adhesives based glass-glass bonding was demonstrated and shear strength degradation was monitored and characterized.

iv)   A novel, low temperature cured conductive copper paste was used to fill small (30 µm) and large (100 µm) through-glass vias in 130 µm and 300 µm thick glass panels for lower stress and higher throughput compared to electroplated copper through-package-vias in glass.

v)   A hybrid through-package-via structure comprising of conformal coated sidewalls with copper paste filled via was explored and modeled using ANSYS HFSS^{TM} to achieve copper-via like high frequency performance.

CHAPTER 1

INTRODUCTION

The objective of this dissertation is to model, design and demonstrate a near-hermetic glass package for low cost, highly reliable, ultra-thin ($< 500 \, \mu m$) MEMS and sensor device packaging at panel scale. Existing packaging schemes like panel laminate/ceramic cavity packaging and silicon wafer level packaging either limit package level integration and miniaturization, are fabricated on small wafers or panels, or use materials that fail to decouple system level stress on the device, thereby risking its long-term reliability at board level. Hence, there is a cost, reliability and form factor gap between existing MEMS and sensor packaging solutions and future heterogeneous package integration (HPI) requirements. This dissertation aims to bridge this gap by exploring ultra-thin panel glass embedding using low-cost materials and processes to enable low stress package structures with high system-level reliability.

MEMS and sensing electronics are seeing unprecedented growth, driven by smartphones as well as emerging IoT devices. Sensing devices need to be interconnected with RF connectivity, high bandwidth computing and analog/mixed signal processing ICs to form smart systems. MEMS devices are widely used for sensors due to existing CMOS fabrication infrastructure used to form 3D out-of-plane structures. There are several challenges in the packaging of MEMS sensors, especially when are co-packaged with logic, memory, RF and analog ICs to form heterogeneous systems. The main packaging challenges are cost, hermetic/near-hermetic sealing for board level stress decoupling and low stress through-package interconnections to enable miniaturization, all of which form

1

the focus of this dissertation. Current approaches to MEMS and ASIC integration in a package include wafer-level packaging in 2D and 3D stacking with TSV, and multi-chip system in package (SiP) in ceramic cavity substrates. Wafer level packaging involves expensive TSVs for 3D interconnections and anodic bonding of silicon-silicon or silicon-glass wafers at high temperature and voltages which not only result in high residual stresses at the interface, but also fail to buffer external system level stresses. Ceramic cavity packages are limited by their high cost coming from small panel sizes, CTE mismatch induced stress on sensitive MEMS devices, and thick and bulky form factors. In contrast to these wafer or small ceramic substrates, this dissertation for the first time demonstrates a new cost-effective and low-stress, near-hermetic or hermetic package for MEMS devices using ultra-thin glass panel substrates and stacking multiple layers of thin glass with and without cavities.

1.1 Current Approaches to MEMS packaging and Their Limitations for Heterogeneous Package Integration (HPI)

MEMS sensors are currently packaged using a combination of two approaches: zero level packaging and first level packaging. Silicon Wafer Level Packaging is a necessary zero level packaging method used in which the fabricated MEMS and sensors devices are packaged before they are diced into individual coupons. These individual packaged dies are then further packaged on laminate/LTCC substrates with cavities for integration with other devices like ASICs.

1.1.1   *Silicon Wafer Level Packaging*

Silicon wafer level packaging (WLP) refers to the practice of encapsulating MEMS structures fabricated on silicon chips between bonded wafers prior to the dicing step. WLP is a zero-level packaging technique or foundry based process which is low cost, high yield, provides protection from dust and water in saw dicing processes, shows superior long-term stability and reliability and provides robust mechanical protection, all of which are critical for fragile MEMS structures. Two main methods are used for wafer level encapsulation: (a) use of bonded cap wafer and (b) deposition of encapsulation layer. Since thin film deposition involves complex processing steps, wafer level lids are more commonly used at the cost of increased form factor.
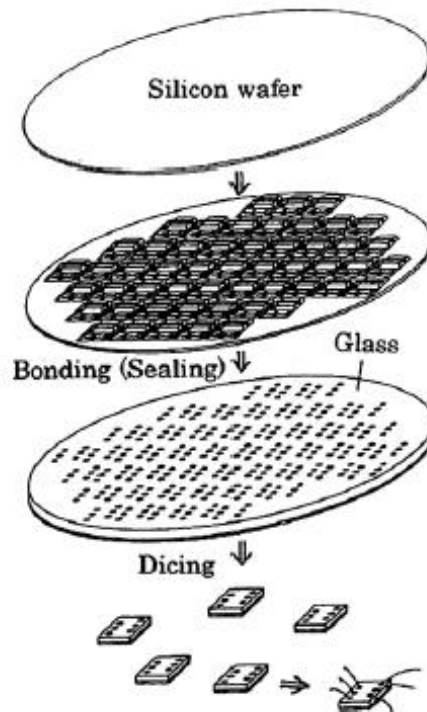
Figure 1: Typical silicon wafer level packaging process flow [5]

Figure 1 above shows the simplified process flow used in silicon wafer level packaging. MEMS devices with metallization and bond pads are fabricated using standard CMOS processing steps on a silicon wafer. Next, cavities are sacrificially etched on a lid wafer (silicon or Pyrex glass) which is then bonded to the device wafer using direct or indirect bonding techniques (anodic bonding, glass frit bonding and adhesive bonding). Finally, the devices are singulated to form packaged MEMS chips, cross section of which is shown in Figure 2 below.
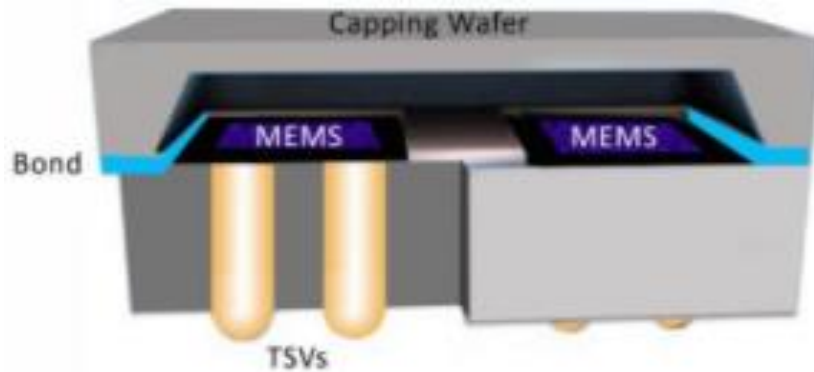
Figure 2: Typical cross section of a silicon wafer level packaged MEMS device [6]

Recently, vertical feedthroughs to establish interconnections from inside the sealed cavity have gained popularity over complicated planar interconnections, leading to increased interest in through-silicon and through-glass via (TSV/TGV) technologies. Vertical feedthroughs can be used to assemble package on package (PoP) architectures which enable integration of the MEMS sensor with its ASIC circuitry in 3D fashion, thereby conserving silicon real estate for 2D miniaturization.

1.1.1.1 Limitations of Silicon Wafer Level Packaging for HPI with MEMS

While wafer level packaging is gaining increased adoption due to its ability to provide hermetic vacuum encapsulation at foundry level that protects the delicate, sensitive device from dust, shocks, air dampening and humidity exposure, several challenges associated with WLP expose the technology gaps that need to be addressed. Wafer level packaging does not allow MEMS-ASIC integration. Cost scaling is limited due to lack of large panel availability and expensive processing steps like TSV formation and metallization. Form factor reduction made possible by back grinding the wafer to desired thickness may impart mechanical damage to the MEMS and high temperature anodic bonding techniques conventionally used to bond the lid wafer to device wafer generate residual stresses and stiction issues.

Despite these limitations, wafer level packaging is an essential part of the MEMS manufacturing process and cannot be avoided. To overcome the primary challenge of heterogeneous integration, first level packaging becomes critical and is the focus of worldwide research.

1.1.2 *Low Temperature Co-Fired Ceramic (LTCC) Substrates and Laminates*

Low temperature co-fired ceramic (LTCC) substrates have been widely used for the last two decades to produce multi-chip ceramic modules, used as a multilayer substrate for IC packaging.
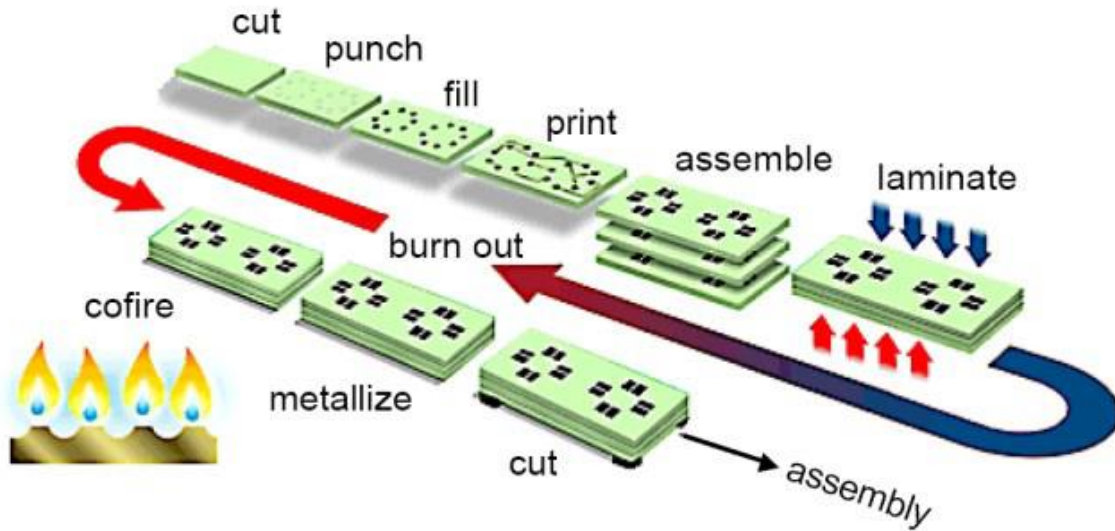
Figure 3: Manufacturing process of LTCC substrates [1]

A typical process flow for manufacturing LTCC substrates is shown in Figure 3 above. The starting point is the ceramic green tape sheets (usually >50 µm thick, 6 x 6 inch sheets) produced by tape casting method. Micromachining techniques are used to form through vias and other structures like cavities in the tape after which conducting material is screen printed to form vertical feedthroughs and horizontal traces that enable 2D and 3D integration. Successive green tapes are then registered, laminated using uniaxial or isostatic laminators (typically at 200 atm, 70°C for 10 minutes) and cofired in a single step in air at high temperatures, typically up to 875°C, simultaneously sintering the conductive ink to form interconnections, after which devices are assembled.
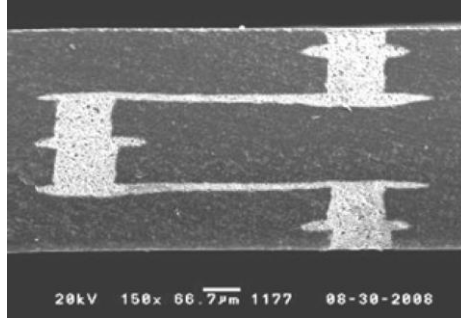
Figure 4: Sintering pastes used to form vertical and planar interconnections in LTCC substrates [2]

Figure 4 above shows the cross section of vertical and lateral electrical connections in an LTCC substrate and Figure 5 below shows the typical structure of a multilayer LTCC package with MEMS devices assembled and sealed in cavities.
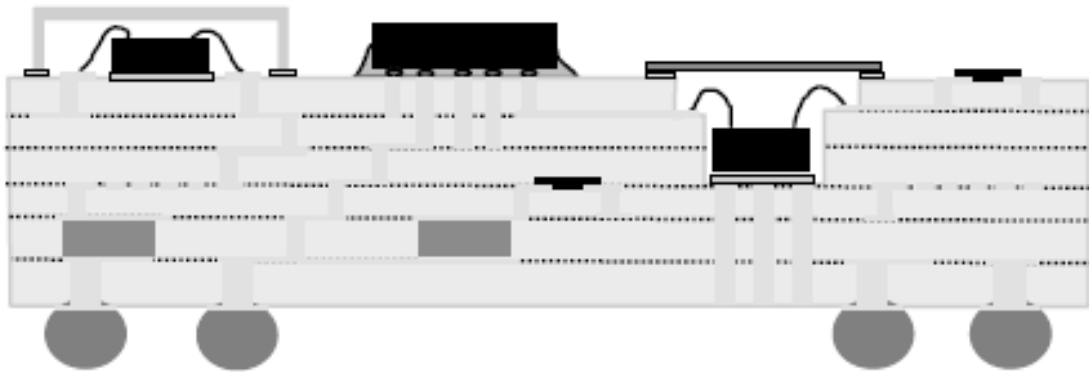
Figure 5: Concept image of a MEMS System-in-Package (SiP) using LTCC technology [3]

Additionally, MEMS-ASIC integration is also made possible by die assembly in 2D or 3D stacked fashion using die attach followed by wire bonding/flip-chip assembly on laminate substrates, as shown in Figure 6 below. Once devices are assembled, metal/plastic lid structures, laminate based cavities and epoxy molding compound (EMC) are used for encapsulation and mechanical protection. Through-silicon-vias and face-to-face stacking

7

is used to interconnect stacked dies while through-mold-vias are used in cases where molding compounds are used.
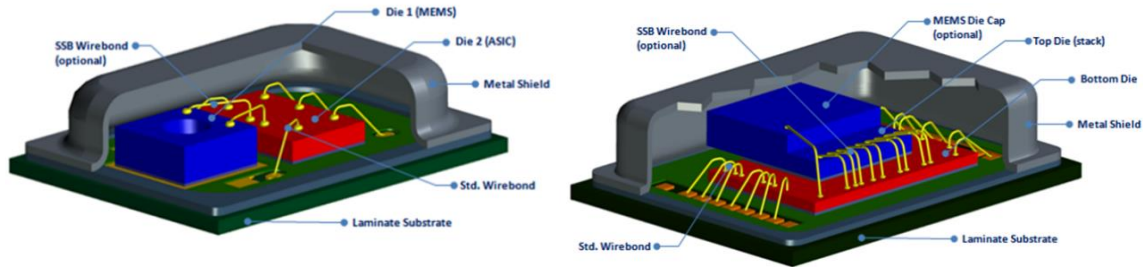
Figure 6: Amkor's laminate substrate based packaging to enable MEMS-ASIC integration

1.1.2.1 Limitations of Low Temperature Co-Fired Ceramic (LTCC) Substrates and

Laminates for HPI with MEMS

While LTCC substrates offer robust mechanical protection, high reliability through silicon CTE matching, device embedding and integration capabilities, there are several challenges that can limit its potential as an advanced MEMS packaging substrate. Since each green tape is at least 50 µm thick [4], high density, multilayer packages often exceed hundreds of microns in thickness. High density, fine line interconnections require smooth surfaces and precision micromachining capabilities but LTCC substrates are rough and are limited to a line width and via diameter of 50 µm and pitch of 150 µm, which may be insufficient for high density interconnections between MEMS and ASIC [2, 3]. Further, expensive processing tools and conductor materials typically used, like silver, gold and platinum pastes limit cost scaling. Finally, high temperature processing is often incompatible with certain MEMS whereas unequally distributed post-firing-shrinkage may lead to warpage induced stresses. Laminate based packaging enables MEMS-ASIC

8

integration in a system-in-package (SiP) fashion. Further, the large CTE mismatch between the dissimilar materials (EMC~30 ppm/^{o}C, Silicon = 3 ppm/^{o}C, die attach ~ 40 ppm/^{o}C and laminate substrate = 17 ppm/^{o}C) leads to reliability issues, particularly from molding compounds that impart compressive stresses often of the order of thousands of psi on the MEMS. Use of cavities and metal caps instead eliminates a source of stress. However, interfacial stresses at die-die attach-substrate interfaces and lid-substrate interface persist. Metal caps are also expensive and lead to bulky, heavy packages.

1.2 Panel Glass Embedding for HPI with MEMS

In this dissertation, glass panel substrates are explored and demonstrated for first-level embedded packaging of MEMS sensors, scalable to heterogeneous integration with logic and other devices in the same package. Panel glass embedding combines the benefits of LTCC substrate and silicon wafer level packaging while addressing their limitations. There are several compelling reasons for the use of glass substrates for MEMS packaging:

i) Large availability of **ultra-thin glass substrates** in panel form, engineered to thicknesses between 30 – 300 μm to reduce form factor, eliminating the need for back grinding.

ii) Affordability to form high-density through-package-vias in glass to enable **3D integration** and high density planar traces due to high modulus (50 – 90 GPa) and excellent surface finish with < 1 nm roughness.

iii) Low package-induced stresses due to tailored CTE and high dimensional stability leading to **higher reliability**.

iv)   Large area panel processing as opposed to wafer processing and use of inexpensive materials and processes for **lower cost**.

This dissertation demonstrates a new concept of low stress, reliable, near-hermetic ultra-thin glass based cavity packages for MEMS devices. These glass cavity packages can be scaled down to 2x smaller form factors (<500µm) and are fabricated out of large (up to 12 x 12 inch), ultra-thin (50 µm thick) glass panel based processes, thereby addressing the form factor and low-cost requirements of MEMS packaging. Flexibility in cavity design, advances in low temperature, low stress through-glass-vias (TGVs) and substrate bonding technologies, better CTE matching and dimensional stability of thin glass enable 3D integration with improved reliability. Figure 7 shows the conceptual representation of the glass cavity MEMS package.

ULTRA-THIN GLASS CAVITY PACKAGE
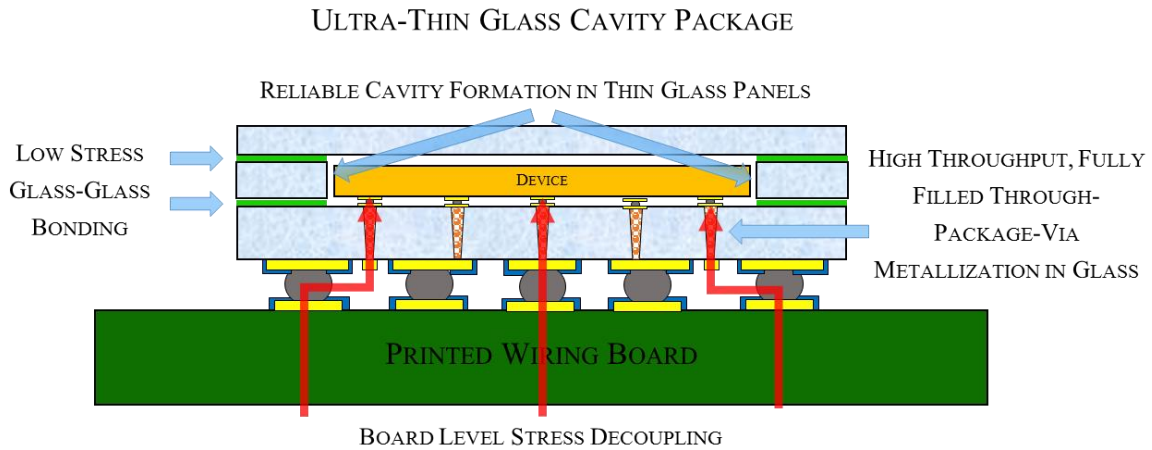
Figure 7: Conceptual cross-sectional image of glass cavity package

1.3 Research Objectives, Unique Approach and Technical Challenges

The specific objectives of this dissertation research are to address the fundamental technical challenges in three key panel glass cavity MEMS package building blocks,

(a) reliable cavity formation in thin glass panels, (b) low stress glass-glass bonding, and (c) high-throughput, fully filled through-package-via metallization in glass. The fundamental challenges to achieve these objectives are: (a) cavity corner cracking, side wall taper, side wall roughness and defects, (b) interfacial voids at glass-polymer-glass interface and (c) electrical opens and high frequency performance of copper paste filled through-package-vias in glass.

The specific objectives, prior art, unique approach and associated technical challenges are summarized in Table 1, which forms the basis of this research.

Table 1: Table showing research objectives, recent prior art and technical challenges

Objectives	Prior Art	Unique Approach	Technical challenges
1. Reliable Cavity Formation in Thin Glass Panels	• Wet etch • Sandblasting	• Advanced machining technologies for laminated/blind cavities	• Cavity corner cracking, side wall taper, side wall roughness and defects
2. Low Stress Glass-Glass Bonding	• Anodic bonding (400V-1000V, 300 °C -500°C) • Glass welding • Glass frit bonding	• Glass-glass near hermetic adhesive bonding @ <250°C using ultra-thin polymer adhesives	• Interfacial voids at glass-polymer-glass interface

3. High Throughput, Fully Filled Through-Package-Via Metallization in Glass	• Copper plated fully filled through-vias • Electrically conductive adhesives and high temperature sintering pastes	• Low temperature, low stress conductive paste filled through-vias	• Electrical opens and high frequency performance of paste filled through-package vias in glass

1.4 Research Tasks and Thesis Organization

The research tasks are consistent with the objectives and technical challenges mentioned above in. They are listed below:

Task 1: Process development, demonstration and examination of reliable, defect free, low taper cavities in thin glass panels.

Task 2: Shear strength characterization, void reduction and reliability studies of polymer adhesives against thermal cycling.

Task 3: Process optimization and demonstration of metallization process for fully filled through-package-vias in glass using copper paste for high yield.

Task 4: Evaluation of a novel hybrid via structure for improved high frequency performance of copper paste filled through-package-vias in glass.

This thesis is organized into six chapters. This chapter discussed the drivers for advanced MEMS packaging in the IoT era, reviewed the status of MEMS packaging and established a compelling case for the use of glass as a MEMS packaging substrate. Chapter 2 reviews published literature that studies glass cavity formation, glass-glass bonding and through-glass-via metallization technologies. In Chapter 3, various design considerations in formation of glass cavities in thin glass panels are discussed followed by process, characterization and analysis of reliable, defect free and low taper glass cavities. Chapter 4 discusses the theory of glass-glass bonding using ultra-thin polymer adhesives along with experimental characterization of bond strength, void reduction and bond reliability studies. Chapter 5 discusses the fundamental working principle of low temperature copper paste, process demonstration and optimization to achieve fully filled through-package-vias in glass. Hybrid via structures that exploit process versatility are explored for improved high frequency performance.

CHAPTER 2

LITERATURE REVIEW

The previous chapter described the dissertation objectives, technical challenges, and research tasks to address these challenges. The unique approach of panel scale device embedding in glass substrates for MEMS sensor packaging has three main challenges and tasks to achieve the research objectives, namely, (a) reliable cavity formation in thin glass panels, (b) low stress glass-glass bonding, and (c) high-throughput, fully filled through-package-via metallization in glass. This chapter will review published literature in addressing these challenges. The final section in this chapter will summarize these advances.

2.1 Prior work in reliable cavity formation in thin glass

This section describes the prior work on cavity formation in glass using a variety of techniques. Due to its chemical inertness and brittleness, high throughput, defect free glass structuring is difficult. While cavity formation in glass has been demonstrated using a number of expensive, specialized techniques like deep reactive ion etching (DRIE) [7] , glass reflow [8] and hot-forming [9], two main techniques are most widely used: wet etching and sandblasting (powder blasting).

2.1.1 *Wet etching*

Wet etching is a method commonly used to machine structures in glass and silicon for MEMS wafer level packaging applications [7, 10] where HF based solutions of varying concentrations are used in combination with masking materials. Some of the main

drawbacks of this method are (a) isotropic nature of etching leading to irregular shapes, large taper and high surface roughness, (b) low etch rates and (c) selection of masking material. HCl and H_3PO_4 used in appropriate ratios with HF are known to mitigate the challenge of roughness [11]. Etch rates can be controlled by varying the HF concentration and by controlling the temperature of the solution as shown in Figure 8 [12].
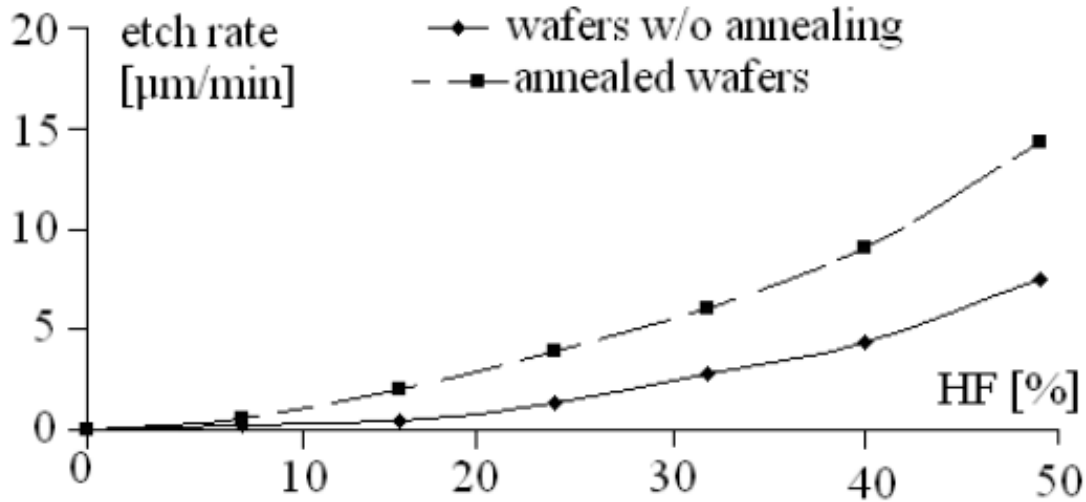
Figure 8: Variation of etch rates in glass with HF concentration [12]

Masking options and alternative solutions to overcome the roughness problem have been investigated in [11, 13, 14] and by the use of photosensitive glass [15-18]. Despite all these efforts, wet etching is limited by the fundamental challenge of isotropic etching resulting in tapered/curved side walls, as shown in Figure 9 below.

15
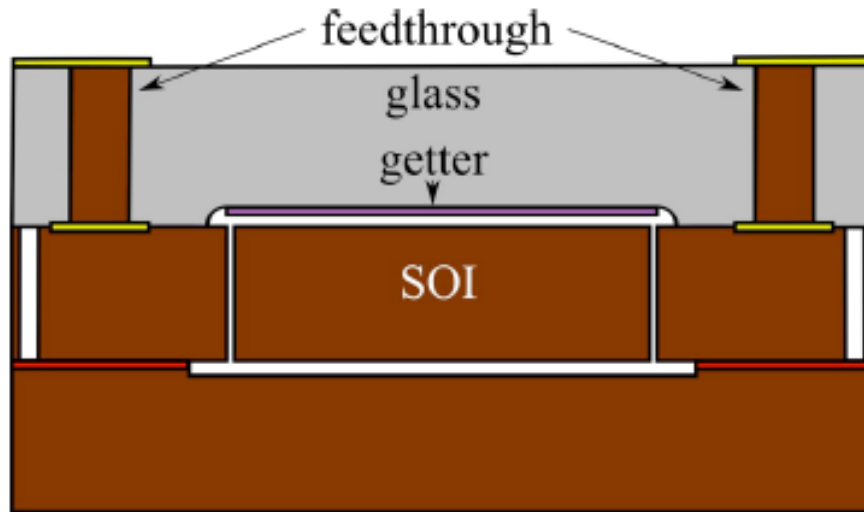
Figure 9: Wet etched glass cavity for hermetic packaging of resonators [10]

2.1.2 *Sandblasting/powder blasting*

Sandblasting is one the earliest methods used for glass machining. Commonly used to fabricate large, coarse-pitched feedthroughs, this method, illustrated in Figure 11, has been recently extended to form glass cavities used as capping structures in MEMS packages, shown in Figure 10. [19]
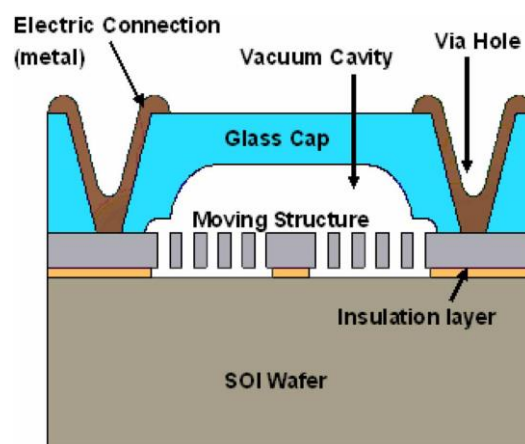
Figure 10: Glass cavities formed by sandblasting technique [19]
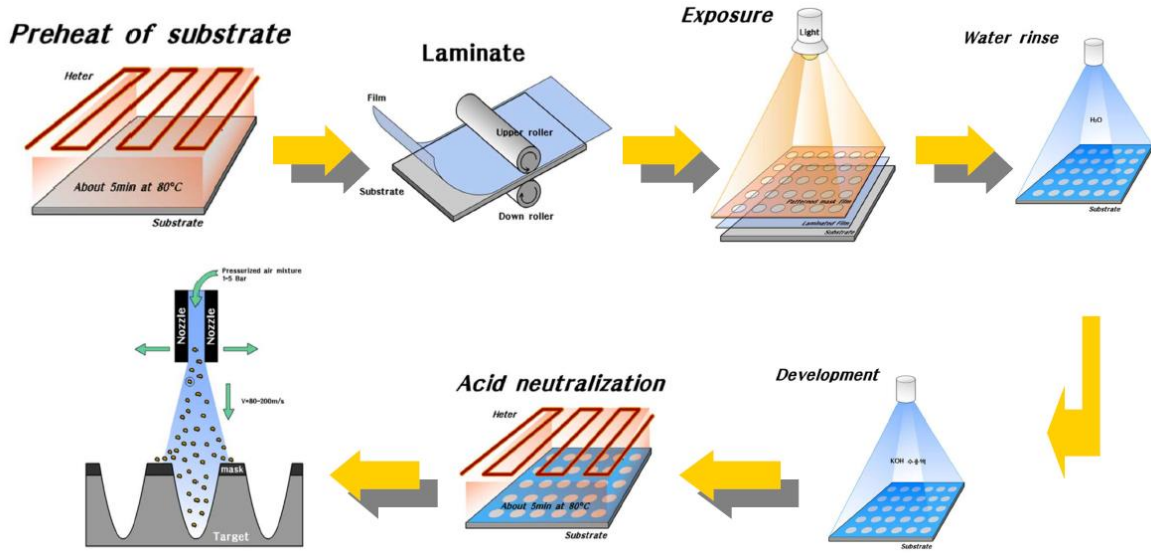
Figure 11: Image showing typical steps involved in sandblasting process [11]

Table 2 summarizes the techniques used for glass cavity formation in the prior art. None of the existing methods meet all the requirements to achieve the research objectives and there is a need to explore and develop new processes to form high quality cavities in thin glass to match the throughput, reliability and form factor requirements of ultra-thin glass embedded packages.

Table 2: Comparison of various glass cavity formation techniques

Parameter	Sandblast	Wet etch	DRIE	Glass reflow
Lateral etching	No	Yes	No	No
Taper	V shaped taper	U shaped taper	Vertical walls	Vertical walls
Aspect ratio	Low	Low	High	High
Surface quality	Rough	Rough	Smooth	Smooth
Process time	Short	Long	Long	Long

2.2 Prior work in glass-glass bonding

Silicon-glass and glass-glass bonding have been developed for wafer level packaging of MEMS devices. Capping structures fabricated out of glass or silicon wafers are bonded to the MEMS wafer for mechanical protection, in the wafer fab and not in the package foundry, to prevent device contamination. While most of the published literature relates to glass-to-silicon wafer bonding, there has been a limited amount of prior work on glass-glass bonding. Bonding techniques can be broadly classified into two types described in this section: direct and indirect. Direct bonding uses no additional material at the interface whereas indirect bonding uses materials like polymer adhesives, frit paste and thin film metals.

2.2.1   *Direct Glass-Glass Bonding*

2.2.1.1 Anodic Bonding

Silicon-silicon, silicon-glass and glass-glass anodic bonding has been used extensively for hermetic sealing and protective encapsulation of various MEMS devices like accelerometers, RF switches, pressure sensors and gyroscopes [20]. In this technique, illustrated in Figure 12, alkali rich glass (borosilicate) is bonded to other borosilicate glasses, metals or semiconductor substrates, most commonly silicon by application of high temperatures ($300^{o}C - 500^{o}C$) and high voltages ($400V - 1000V$). A robust, permanent hermetic bond is achieved through formation of interfacial SiO_2. Glass-glass anodic bonding has been demonstrated in [21] by use of thin film aluminum that acts as a common anode, illustrated in Figure 13. Other interfacial materials like silicon with similar CTEs can also be used as the common anode for more reliable bonding.

18
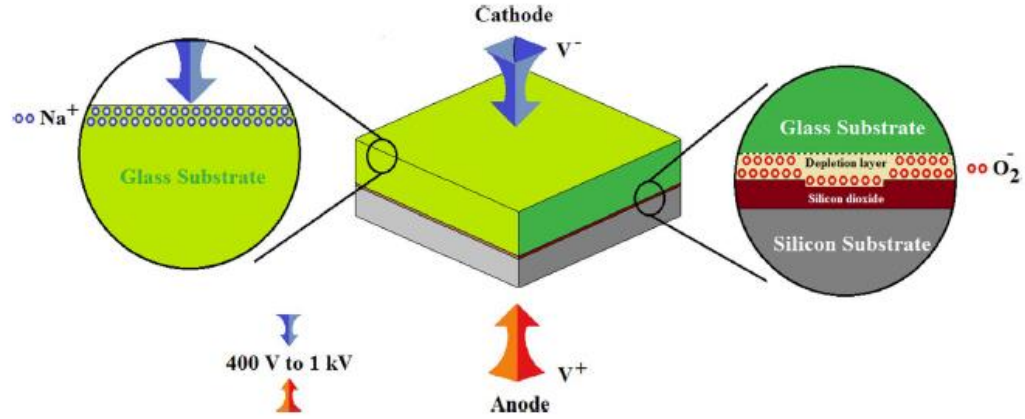
Figure 12: Conceptual image showing mechanism of Si-glass anodic bonding [22]
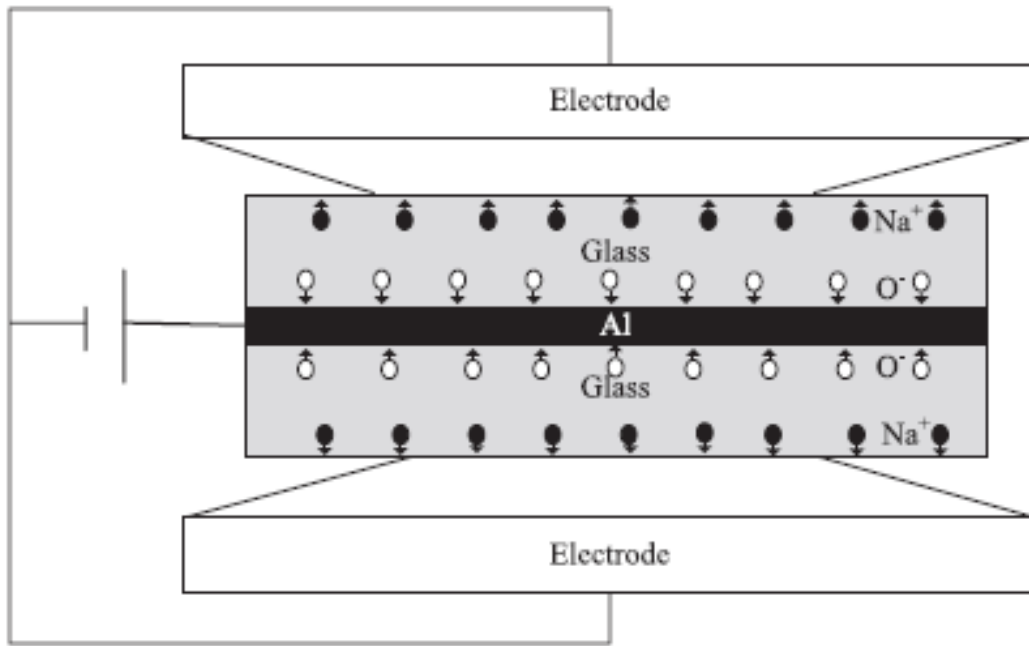
Figure 13: Conceptual image showing mechanism of glass-glass anodic bonding using common interfacial anode (here, Aluminum) [21]

Despite all its advantages, anodic bonding is only applicable to high-alkali content glasses with customized compositions. High voltages used in anodic bonding have shown to cause stiction between movable MEMS structures and the lid [2]. Additionally, the high temperatures involved in anodic bonding result in high residual thermal stresses [20],

which can be controlled by slow cooling resulting in increased processing time. Low temperature anodic bonding can result in weaker bonds and requires longer bonding times. A potential solution is to modify the glass composition to increase the bulk charge carrier density. This technique was employed in [23] and [24], where low temperature anodic bonding at 180°C was demonstrated using Li-containing glass-ceramic in which spodumene (β-LiAlSi$_2$O$_6$) provided mobile Li-ions at elevated temperatures. Another technique to achieve low temperature anodic bonding at 200°C - 300°C was demonstrated using plasma based surface activation techniques [25]. Most recently, electrode modifications have been shown to help reduce bonding temperatures to as low as 250°C with shorter bonding times [22].

2.2.1.2 Low Temperature Direct Bonding

D. Hutt [26] and X. Cui [27] presented a preliminary process to fabricate laminated multilayer glass substrates built up from 50 µm - 100 µm thin glass sheets to address the demand for high density interconnect (HDI) packaging substrates. Glass sheets were micromachined to form vias, metallized to form electrical interconnections and then bonded using a Pressure Assisted Low Temperature Bonding method (PALTB) in a sequential process using metal plates and a clamping system which imparted high tensile stress and risk of glass cracking. M.M.R. Howlader's group [28] also explored direct bonding at room temperature using surface activation techniques, namely reactive ion etching O$_2$ RF plasma followed by nitrogen radical microwave plasma. The glass wafers were then bonded in a cold rolling process under a load of 20 kilograms.

2.2.2   *Indirect Bonding*

2.2.2.1 Adhesive Bonding

Adhesive bonding has been previously explored to bond silicon to silicon [29, 30] and silicon to glass [31-35] for MEMS WLP packaging applications but there is limited published work in detailed analysis of glass to glass adhesive bonding. Jourdain et al. demonstrated silicon-silicon bonding using BCB as the adhesive material for wafer level packaging and sealing of RF MEMS structures inside cavities fabricated in silicon to achieve low leak rates, high bond strength and reliability against harsh conditions [29]. Niklaus et al. used BCB, a photoresist (S1818) and two polyimides to investigate influence of process parameters on interfacial void formation to successfully demonstrate void-free silicon wafer-wafer interface [30]. In S. Ma's [31] and Polyakov's [33] work , BCB was explored to bond glass to silicon wafers where its photosensitivity and patternability was leveraged to avert MEMS intra-cavity contamination. Finally, adhesive bonding using a β-stage epoxy was explored in Kim's work [32] where temperatures as low as 150ºC with 30 to 60-minute cure times were shown to form robust silicon-glass bonds. However, since epoxies are weak in water, bond strength degradation was observed after a 40-hour water soak.

2.2.2.2 Laser Assisted Glass Frit Paste Bonding

Glass frit pastes have been used as an alternate to anodic bonding to for hermetic seals in MEMS packaging, especially gyroscopes. Detailed investigations on thermomechanical properties, process optimization, bond quality, bond reliability and hermeticity have been published in [36-38]. More recently, alternative techniques like laser

assisted frit bonding [39-44] have been explored to overcome the limitations of the traditional thermocompressive glass frit bonding, which cannot be applied for hermetic packaging of MEMS sensitive to high temperatures. Impact of laser processing on bond quality has been studied in [45] with a focus on further reduction of residual thermal stresses that initiate and propagate micro-cracks.

2.2.2.3 Ultrashort and Nanosecond Laser Welding with Interfacial Thin Films

Glass welding is a relatively new technology that is still under development. Many methods have been developed to bond glass substrates through use of expensive femtosecond [46], picosecond [47] and CO_2 lasers [48] while relatively cheap nanosecond lasers have also been explored [49]. A. Horn and A. de Pablos-Martin [49-53] have published detailed studies of glass-glass bonding mechanisms with and without intermediary absorber thin films like titanium, fresionite (BaSn0.15Ti0.85O3), and $BaTiAl_6O_{12}$ using femto-, pico- and nanosecond lasers with research work in laser parameter dependence, interfacial microstructural analyses, bond strength and bond quality characterization.

2.3 Prior work in fully filled through-glass-via metallization

Metallization of through via interconnections in glass substrates is essential to enable x-y-z miniaturization and 3D integration. This section discusses the approaches that have been successfully used to demonstrate fully filled through vias metallized with different conductor materials.

22

2.3.1   Copper Filled Through-Glass Vias

Fully filled copper vias offer improved electrical performance in 2.5D silicon and glass interposers. Lee et al. described an innovative approach which involves bottom-up plating of Cu into TGVs made by a wafer-level packaging approach (Figure 14) [54]. In this process shown in Figure 14, borosilicate glass is reflowed at 1025 °C into a silicon mold that contains inverse pillar structures formed by deep reactive ion etching (DRIE). The inverse pillar structures in the Si mold are etched by DRIE to reveal vias in the reflowed glass, which are filled with electroplated copper and then planarized by CMP. Finally, the bottom of the vias are revealed by CMP and then metallized.
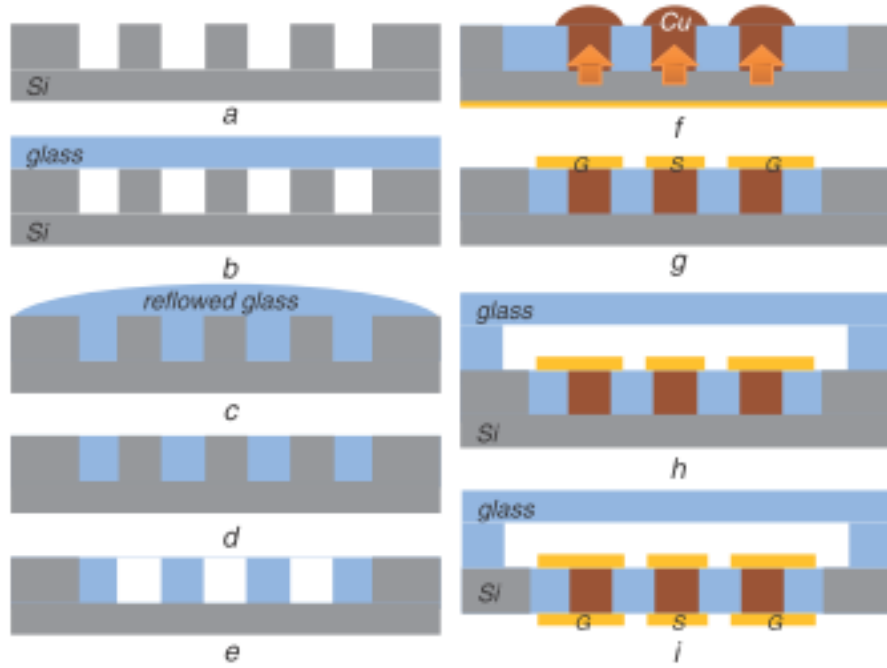
Figure 14. Fabrication process flow of a wafer-level RF MEMS package [54].

A more manufacturable approach was demonstrated by Corning Inc. in 2013 [55]. The process is similar to what is typically used for fabricating Si interposers. The process

begins with blind vias formed in a thick glass substrate (Figure 15a). The blind vias are drilled to a depth greater than the desired final substrate thickness. Ti/Cu is then deposited by physical vapor deposition (PVD), forming a seed layer for subsequent bottom-up filling of Cu and planarization (Figure 15b). Next, the glass substrate undergoes back grinding to reveal the bottom of the blind vias, and then another Cu metallization step is used to complete the metallized glass substrate (Figure 15c).
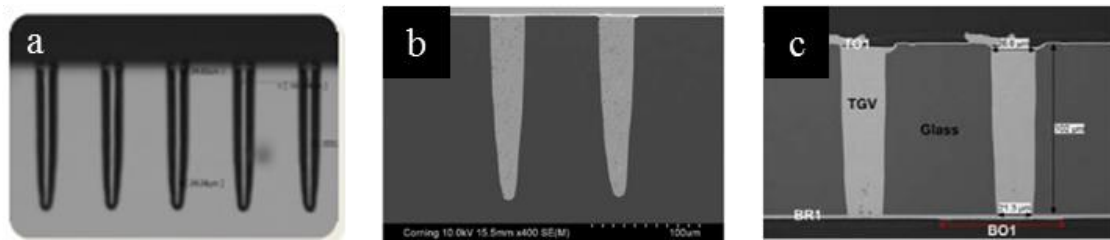
Figure 15. SEM cross sections showing various stages of a Si interposer-type fabrication process of filling glass vias with copper [55].

In 2016, Corning demonstrated an improved process for copper filled vias known as Advanced Lift-off Technology (ALoT) [56]. This technique obviates the back-grinding step and is also designed to be high temperature compatible. A carrier glass and a bonding layer is used to support thin glass wafers or panels with pre-drilled vias, as shown in Figure 16, followed by bottom-up metallization of vias using the standard process described in [57]. Finally, instead of back grinding, the carrier structure is mechanically debonded to release the metallized wafer/panel, shown in Figure 17. Chemical-mechanical-planarization (CMP) is required for planarity on top side, but no additional polishing is required on the bottom side.
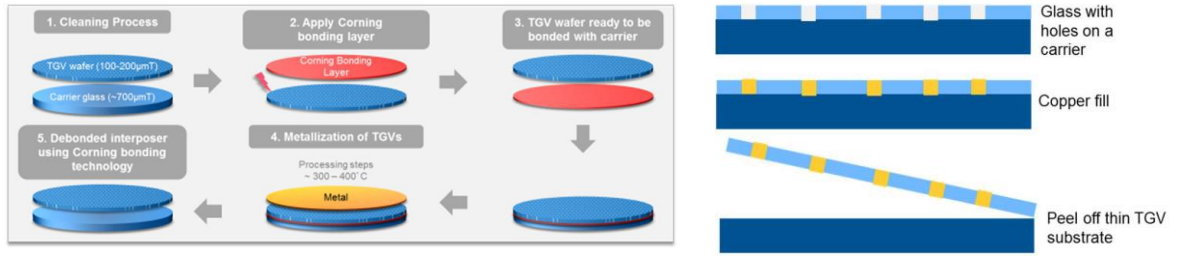
Figure 16: ALoT process for through-glass-via metallization [56]

(a)	**(b)**
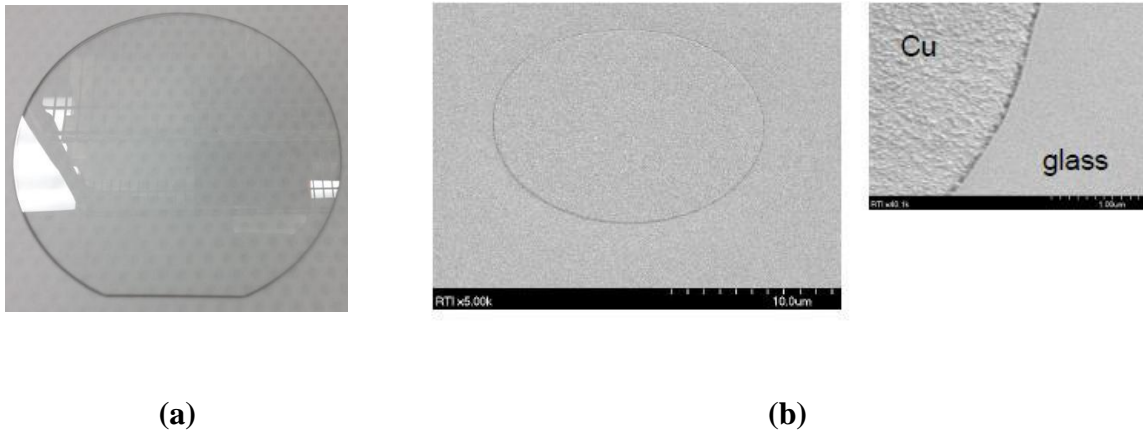
Figure 17: (a) Debonded metallized glass wafer after Corning's a lot process and (b) SEM image showing good planarity [56]

As discussed earlier, fully filled copper plated vias are highly beneficial for high frequency applications due to the high conductivity of copper. However, the fundamental challenges associated with copper plated through glass vias is the high CTE mismatch that lead interfacial stresses and subsequent thermomechanical reliability issues like interfacial delamination. Demir et al [58] proposed an alternative to fully-filled copper plated through

vias in bare glass by using thin polymer liners as barrier layers to buffer the stresses originating from glass-copper CTE mismatch for higher reliability.

2.3.2   *Alternate Through Via Metallization Techniques*

Asahi Glass Company reported on a process to metallize through vias in glass with copper paste filling for 2.5D and 3D glass interposers. TPVs with a minimum via pitch of 60μm in 100μm thick glass substrates were metallized using conductive metal paste, e.g., Cu paste shown in Figure 18. The study also reported that the CTE of the Cu-paste could be adjusted to match the CTE of the glass substrate to achieve higher reliability [59].
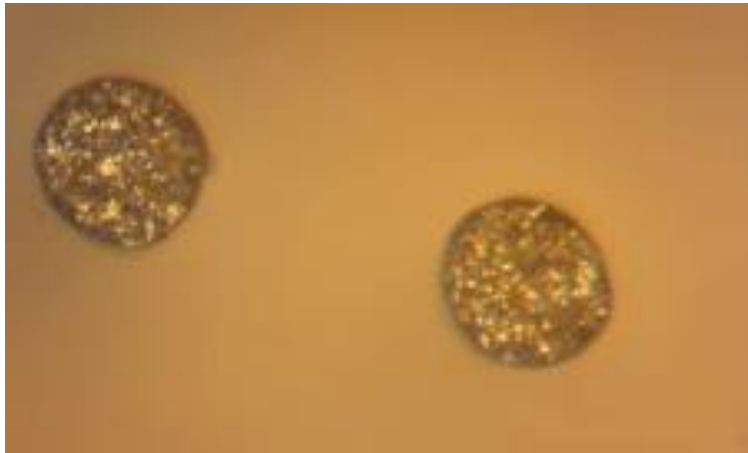
Figure 18: Asahi Glass' copper paste filled hermetic through vias [59]

Another hermetic TGV filling technology named HERMES[TM] has been demonstrated by Schott/NEC [60] in which Tungsten (W) or FeNi is used as conductor materials in through glass vias for MEMS packaging applications. Glass is reflowed over W or FeNi plugs in an additive process to achieve hermetic, void free through glass vias 80 μm in diameter at 200 μm pitch in 350μm thick glass wafers. Nomura's work [61] demonstrated through glass via metallization with bumps using gold particles for hermetic sealing. Standard lithography steps were used to define bump patterns around the through-

via opening, followed by vacuum-assisted stencil printing of Au slurry which comprises of submicron Au particles suspended in an organic solvent and surfactant. A pre-bake step at 110°C followed by a 200°C sintering step resulted in fully filled Au vias, shown in Figure 19 and Figure 20.
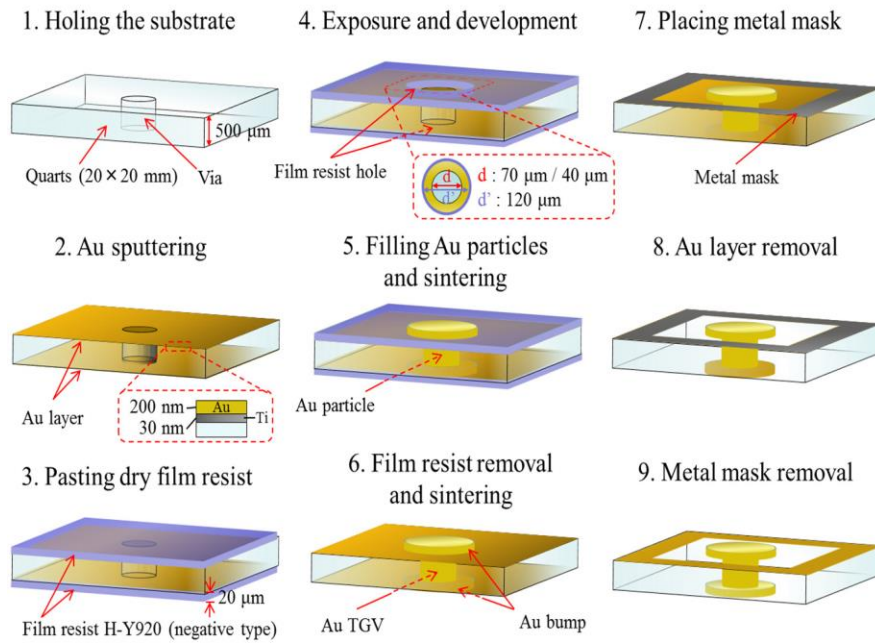
Figure 19: Process flow for through glass vias filled with gold particles [61]
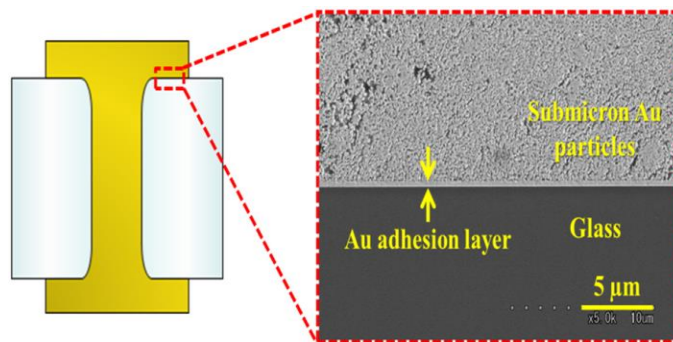
Figure 20: Cross section showing interface between glass substrate and sintered gold particles [61]

2.4 Chapter Summary

This chapter discussed in detail the advances in addressing the three main technical challenges and tasks in this dissertation to enable miniaturized, low stress and near hermetic panel glass embedded packages: (a) reliable cavity formation in thin glass panels, (b) low stress glass-glass bonding and (c) high throughput, fully filled through-package-via metallization in glass. The table below summarizes published research discussed in previous sections of this chapter and highlights their technical contributions towards addressing challenges associated with each.

Table 3: Summary of published literature in relevant tasks with references and technical contributions

Task		References	Technical contributions
Glass Cavity Formation	Wet Etching	[11-12]	Cavity sidewall roughness control by H_3PO_4 addition and etch rate control by temperature variation
		[15-18]	Use of photosensitive glass to overcome mask selectivity issues
	Sandblasting	[19]	Fabrication of tapered glass cavity for MEMS package capping structure for mechanical protection
Glass-Glass Bonding	Anodic bonding	[22-25]	Low temperature processing by electrode modification, increasing

			glass carrier concentration and surface activation
	Low temperature direct bonding	[26-28]	Low temperature bonding using pressure and surface activation techniques
	Adhesive bonding	[29-35]	Silicon silicon/silicon-glass bonding for higher reliability
	Glass frit bonding	[39-45]	Laser assisted bonding for localized heating
	Laser welding	[49-53]	Laser welding using interfacial absorber thin films
Through glass via metallization	Copper Filled TGVs	[54-58]	Fully filled copper TGVs
		[58]	Thin polymer liners for interfacial stress buffering and enhanced reliability
	Schott HERMES©	[60]	Hermetic fully filled tungsten TGVs
	Paste filled TGVs	[59], [61]	Cu and Au paste hermetic TGVs

CHAPTER 3

RELIABLE CAVITY FORMATION IN THIN GLASS PANELS

The previous chapter reviewed literature describing recent approaches to address the three main research challenges. This chapter describes the dissertation research on the first task, namely, cavity formation in thin glass panels. The sections in this chapter discuss two main packaging architectures, metrics used to evaluate the formed cavities, methods to realize cavity structures with advances in micromachining processes and finally, the characterization results.

3.1 Glass Panel Embedding Architectures

Glass cavities can be integrated into two different device embedding architectures: (a) chip last embedded glass cavity package, and (b) chip first embedded glass panel fan-out package, shown in Figure 21 and Figure 22 below. The basic difference between the two is in the sequence of RDL formation and die placement in the cavity.
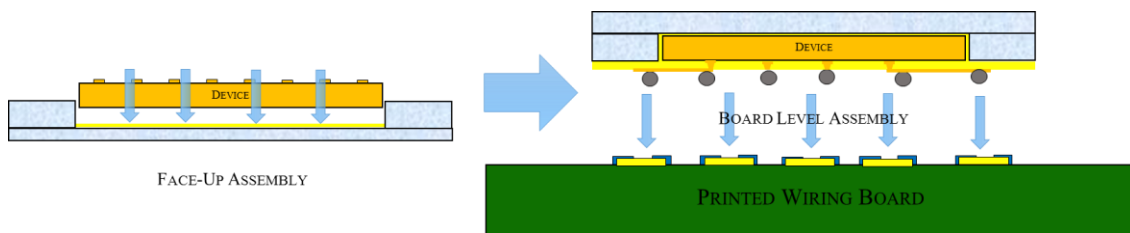
Figure 21: Concept image showing chip-first packaging architecture involving face-up die bonding followed by RDL fabrication and board level assembly
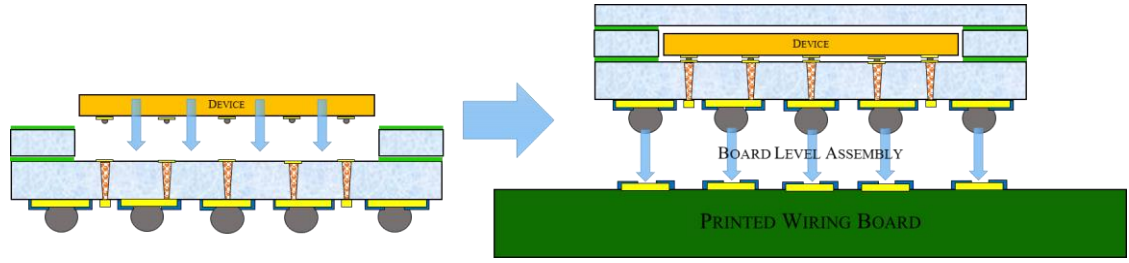
Figure 22: Concept image showing chip-last packaging architecture involving TGV metallization and RDL fabrication followed by die assembly and board level assembly

The chip-first packaging architecture shown in Figure 21 involves face up assembly of the device using ultra-thin polymer adhesives or standard die-attach films (DAFs) for die bonding to the base of the cavity, after which RDLs are fabricated directly on the die to form ultra-short die-to-package interconnections for the best possible electrical performance. The chip-last packaging architecture shown in Figure 22 is the main focus of this dissertation, since it enables the decoupling of board-level stresses from wafer level packaged MEMS devices, and provides ease of integration with other ICs.

3.2 Design Considerations for Glass Cavities

One of the fundamental barriers in realizing the above two packaging architectures is the formation of smooth and defect-free, small and large cavities with low taper angles in thin glass panels (50 µm – 300 µm). For device capping in MEMS WLP applications, the specifications for these metrics are not very aggressive as these applications involve thick glass wafers, typically 100 µm - 500 µm [62] which are more stable and intrinsically more reliable to machine. Besides, their main role is to seal and protect the device from contamination and direct mechanical shocks. However, for device embedding in ultra-thin glass panels the demands on these metrics are relatively more aggressive to ensure high

31

reliability, small form factor (in the X, Y and Z domains) and provide planarity for RDL fabrication. The significance of each of these metrics is described below:

3.2.1 *Sidewall roughness and defect size*

Glass is a brittle material, and can fail under the influence of small elastic strains, especially in the presence of defects. The inherent strength of glass deteriorates during various processing steps as microcracks and other defects are introduced, especially during micro-structuring. Griffith's equation, stated below, states that the critical stress value for brittle failures is related to defect size.

$$\sigma_f = \sqrt{\frac{2E\gamma}{\pi a_c}} \tag{1}$$

Where σ_f is the failure stress, E is the Young's Modulus, γ is the specific free surface energy and a_c is the critical defect length for brittle failure. Small defects present on rough glass surfaces, illustrated in Figure 23 below, act as stress concentration sites which are vulnerable to crack initiation and propagation. Therefore, defect free cavity side walls are essential for reliability.
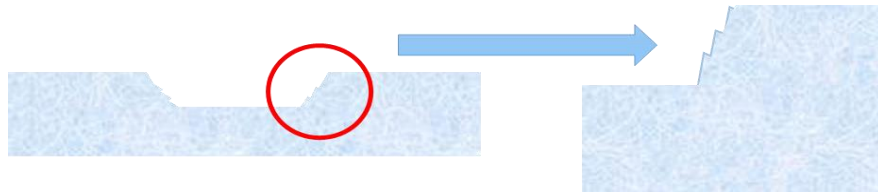
Figure 23: Microdefects on rough glass sidewalls

3.2.2   Sidewall taper

Side wall taper is an important design consideration while forming glass cavities. Cavities with straight side walls enable overall package miniaturization in the x and y dimensions. Additionally, a low taper angle is desirable for the following reasons:

a) RDL surface co-planarity

In the case of chip first glass embedded packages, redistribution layer circuitry is fabricated on top of the die that is assembled face-up. A high degree of planarity is needed to form small RDL traces and vias landing on die pads with good alignment accuracy. During fabrication, the inter-layer dielectric tends to flow into the gap between the die and cavity side wall, which creates micro-depressions on the top surface, as illustrated in Figure 24 below. Although these depressions can be planarized by further lamination steps or by planarization tools, this increases processing steps, complexity and cost. Therefore, a 90-degree cavity wall angle is desirable to reduce the gap volume.
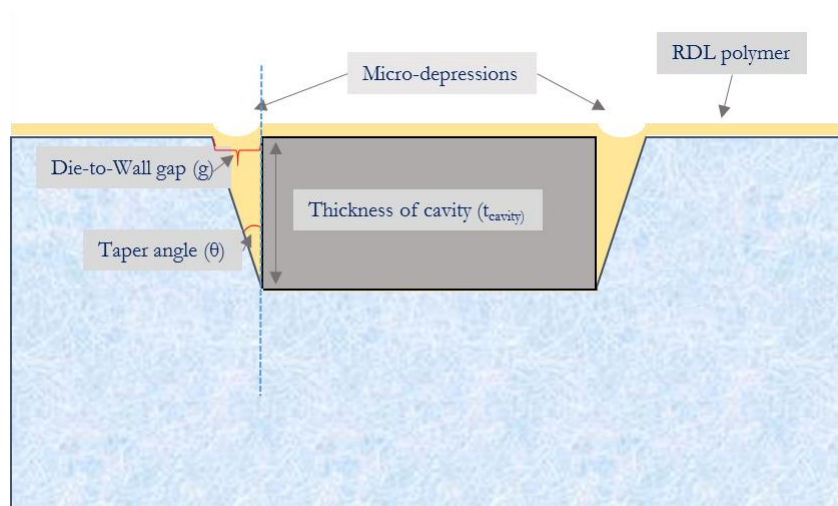
Figure 24: Cavity taper induced micro-depressions top RDL surface

As illustrated in Figure 24 above, the die-cavity wall gap volume can be calculated by first calculating the two-dimensional gap area and then extending it in the third dimension. The gap area can be approximated as a triangle having base length equal to the thickness of the glass cavity (t_{cavity}) and a height equal to the maximum die-to-cavity wall gap (g). If the taper angle is θ, the gap area is defined by the following equation:

$$Gap\ Area = \frac{1}{2}\ x\ t_{cavity}\ x\ g$$

$$= \frac{1}{2}\ x\ t_{cavity}\ x\ (t_{cavity} x \tan \theta)$$

$$= \frac{1}{2}\ x\ t_{cavity}{}^2\ x\ \tan \theta$$

Therefore, a relationship can be drawn between the gap volume and taper angle as shown below.

$$\boldsymbol{Gap\ Volume \propto (taper\ angle\ (\theta))^2}$$

To conclude, formation of micro-depressions and non-planarity on the cavity surface after die embedding can be controlled be minimizing the cavity side wall taper.

b) *Increased I/O density for 3D integration*

Low taper angle is also desired for chip last glass embedded cavity packages to allow the integration of through-glass via structures in close vicinity to the active device placed in the cavity, thereby reducing total interconnect length in the x-y directions leading to

better electrical performance for 3D packages. The taper-induced increase in lateral interconnect length is illustrated in the Figure 25 below.
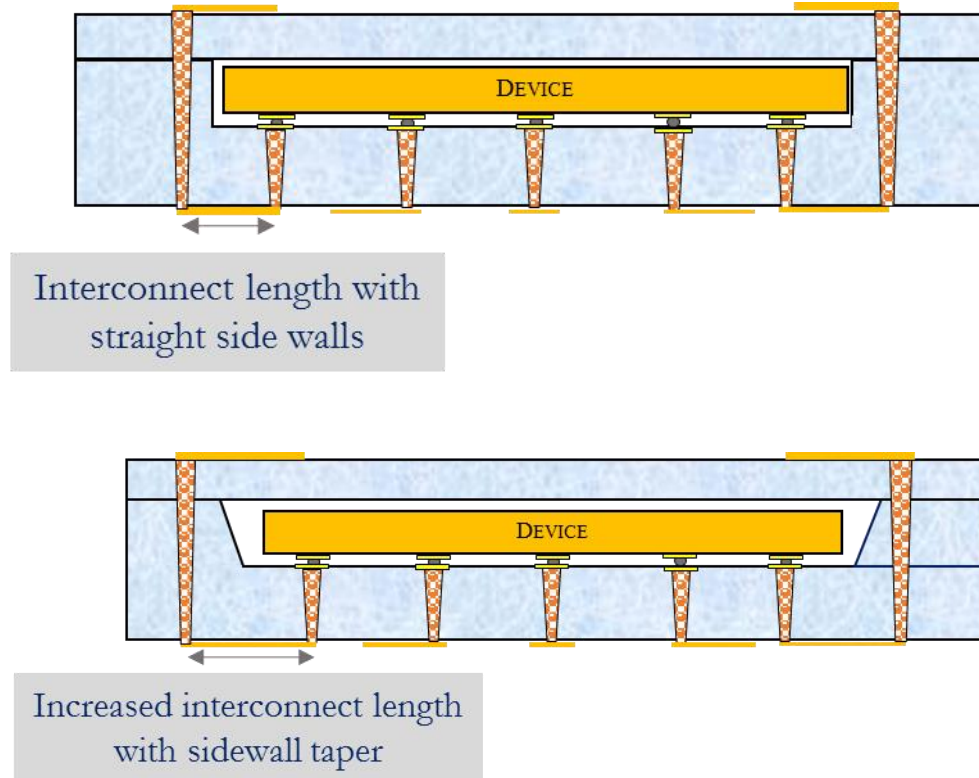
Figure 25: Image showing increased interconnect length from die to TGV due to tapered cavity sidewalls

3.2.3 *Cavity Base Surface roughness*

Surface roughness of the cavity base is an important metric because the die is placed on the base of the cavity. Non-co-planar surfaces can lead to voids, unreliable contact between die bump and pad and other defects, as illustrated in Figure 26 below, and a smooth and planar surface is required to achieve high assembly yield.
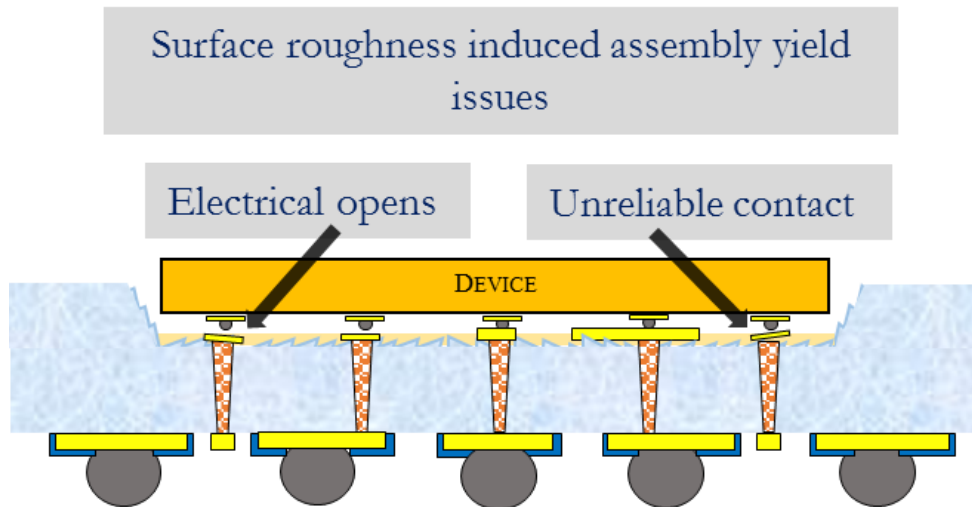
Figure 26: Cavity base surface roughness induced assembly yield challenges

Surface roughness also impacts die pad-to-pad co-planarity in the case of panel glass fan-out packages, as illustrated in Figure 27. Landing of micro-vias on non-coplanar die pads/bumps can result in electrical opens and affect panel scale interconnection yield. Moreover, angular tilting of the die due to the non-uniform surface can lead to x-y axis misalignment.
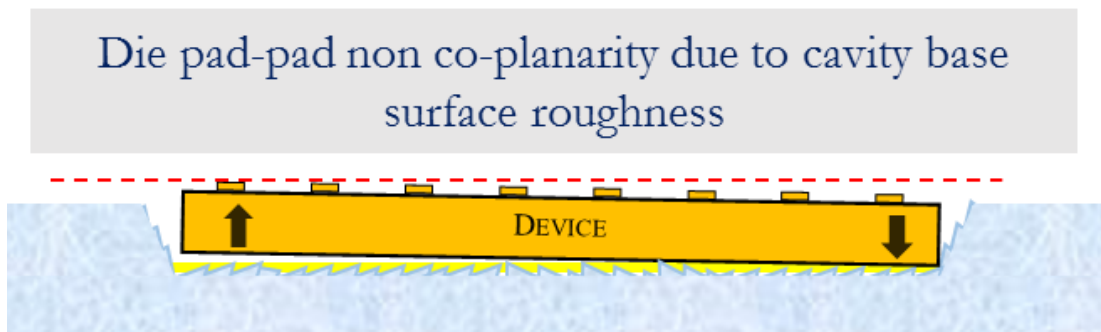
Figure 27: Die pad-pad non-co-planarity due to cavity base surface roughness

3.3 Laminated Glass Cavities vs Blind Cavities

Based on the cavity quality evaluation metrics discussed in the previous section, two glass cavity structures were explored: (a) forming through cavities in one layer of glass followed by glass-to-glass bonding to a base glass carrier, and (b) blind cavities formed in a one-step process.

3.3.1 *Laminated Glass Cavities*

Cavity structures formed using a combination of through glass holes and a carrier substrate have numerous benefits and are the focus of this dissertation. Through-holes are micromachined through glass panels in a flexible process that allows custom designs in a range of glass thicknesses (50 µm – 500 µm). Next, the carrier glass panel is bonded to the cavity panel to form the desired cavity structure. This two-step technique is used in cases where TGVs and RDL must be fabricated separately on the carrier glass before bonding of through-hole glass panel and chip assembly. Therefore, in this dissertation carrier glass is to demonstrate embedded glass cavity packages. Figure 28 below illustrates the concept of cavity formation using through glass holes and metallized carrier glass.
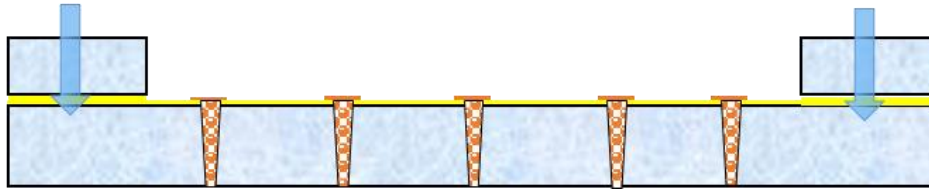
Figure 28: Process for formation of laminated glass cavities

This process enables cavity structures with excellent surface smoothness at the base, ensuring high yield during assembly. Step 3 shown in Figure 28 above involves formation of through-glass holes in glass panels which are then bonded to the carrier glass. To improve reliability of these through-holes, modifications in geometric design are needed. Cavity corners formed at right angles are vulnerable crack initiation sites due to stress concentration. Therefore, it is beneficial to have rounded corners as illustrated in Figure 29 below.
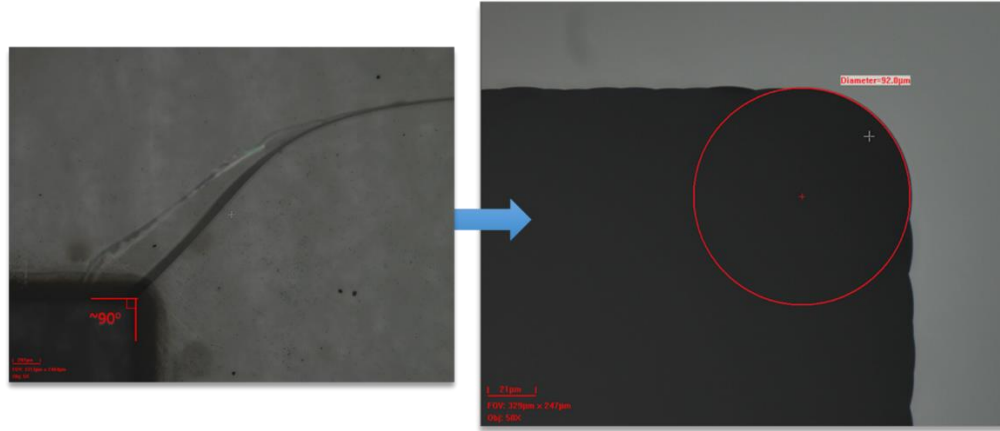
Figure 29: Cavity corners at right angles (left) vs rounded corners for reliable design (right)

Additionally, advancements in micromachining techniques enable formation of low taper, defect-free through glass holes which help meet the design metrics discussed in the previous section. Some of these advanced processes are described below:

a) *Advanced laser processes*

Laser processes typically involve use of certain wavelengths of light (deep UV: <266 nm or IR: > 9µm) that glass absorbs. Photons of higher wavelength (IR regime) cannot break chemical bonds in glass due to insufficient photon energy; however, since absorptivity of glass is high at these wavelengths, the kinetic energy of photons is converted to vibrational energy, leading to thermal ablation by local melting and vaporization. Alternatively, low wavelength photons in the UV regime (<266nm) break chemical bonds in the glass matrix due to high incident energies. UV lasers avoid thermal damage and thus eliminate residual stresses. Ultra-short pulse lasers operating in the visible region are also used, where ablation is triggered by multi-photon initiated avalanche ionization [63]. These conventional laser processes lead to micro-cracking, glass chipping and rough surfaces.

Subsequent processing steps like grinding and polishing increase costs, reduce throughput and lead to low yields [64]
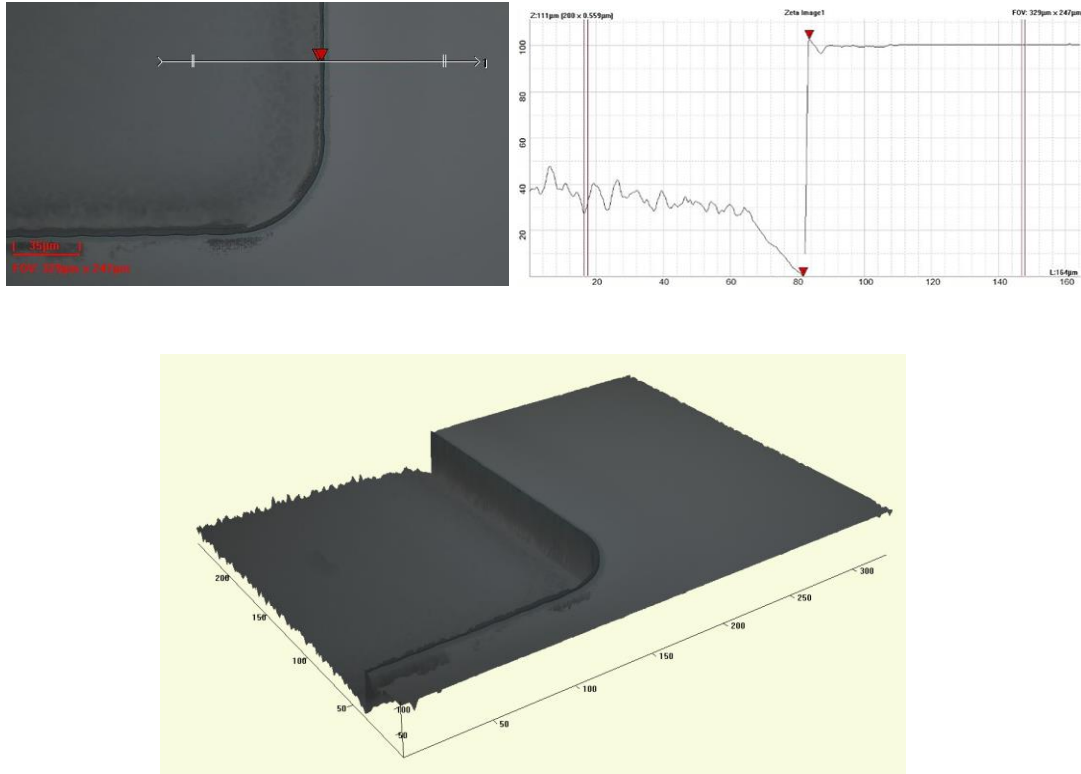
Figure 30: Advanced micromachining processes used to achieve low taper (<2µm)

In this research, two novel methods are explored. In the first approach, glass is machined in a non-linear process where specially tuned lasers using ultra-short pulses in the picosecond range perforate the brittle glass and separate it through its thickness to form through-holes with low taper values of < 2 µm, as shown in Figure 30 above [65]. Since the process relies on dissociation rather than ablation, pristine, defect free side walls are achieved as seen in the Figure 31 below. The combination of low taper and smooth, defect-free side walls gives high dimensional accuracy. High throughput is achieved using high-scan speed lasers cost is reduced as post processing needs are eliminated.
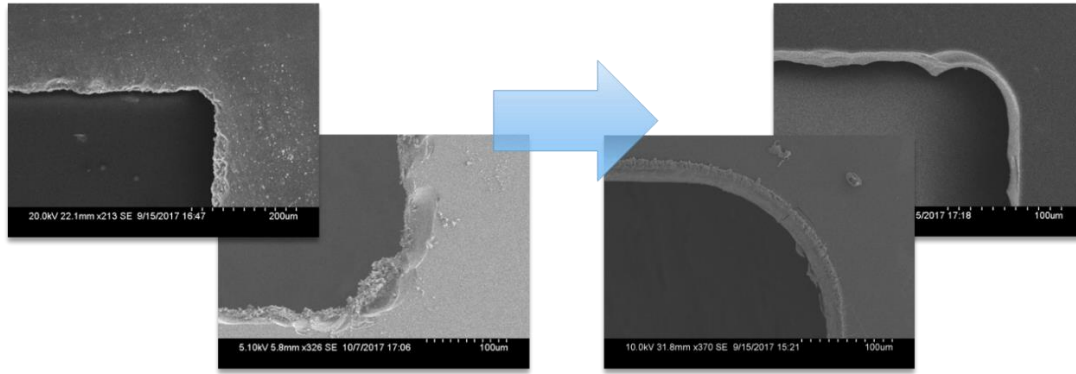
Figure 31: Advanced micromachining processes used to achieve defect-free, smooth cavity sidewalls

In another novel approach [66], thermally induced, high-precision fissures are introduced in glass. Laser heating is followed by rapid cooling using a cold jet of air or air-liquid mixture. The thermal shock induces super-fine fractures resulting in cut edges with high precision and no microcracks or glass chipping. The cleanliness of the cut also eliminates processing steps like washing, grinding and polishing. Figure 32 below shows through-glass cavities micromachined in 300 µm glass using advanced laser drilling processes.

Figure 32: Cavities micromachined in 300 µm thick glass

b) Wet etch processes

As described in chapter 2, wet etching is a common micromachining technique used to form cavity structures in silicon or glass wafers used as caps in MEMS wafer level packaging. In this research, material and process innovations in the wet etching technique at Applied Materials, Inc. are used to form reliable, smooth-walled, low taper cavities in thin glass panels. Figure 33 below shows an SEM image of a crack-free corner of cavity formed in 100 µm thin glass panels. Compared to typical wet etching processes, the proprietary process at Applied Materials resulted in smooth sidewalls and a relatively low taper length of about 60 µm – 70 µm.
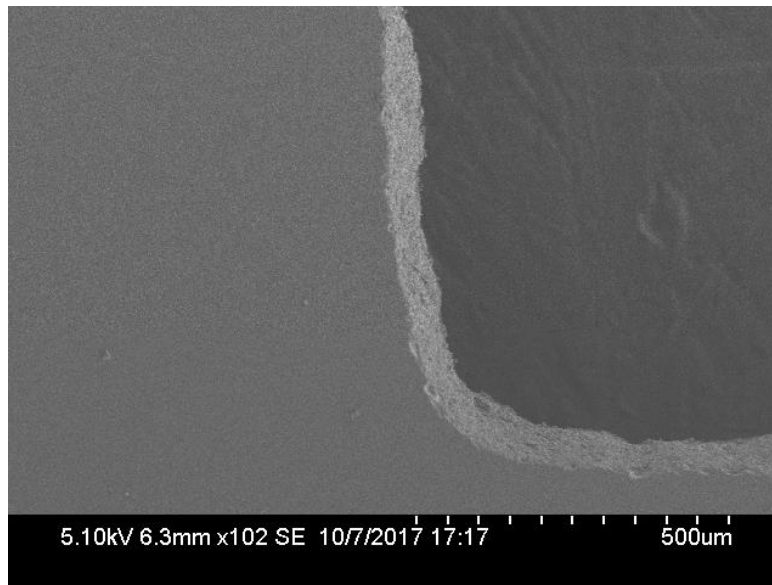
Figure 33: 60-70 µm taper in Applied Materials' proprietary wet etch process to form cavities in thin glass panels

To test the reliability of cavities formed using the two processes described above, glass cavity panels of varying thicknesses - 100 µm, 300 µm and 700 µm - were subjected to thermal cycling between -55ºC and 125ºC. Samples were visually inspected for crack

initiation after every 100 cycles. No failures have been observed so far after completion of 1000 cycles.

3.3.2 *Blind cavities*

A blind cavity is an opening micromachined midway through the thickness of a substrate. Blind glass cavity structures are commonly used in Wafer Level Packages as MEMS caps as described in Chapter 2, but their use as an active carrier substrate has not been reported.

There are two main advantages of this structure:

a) Elimination of glass-glass interface, thereby reducing the risk of interfacial bond failure and enhancing hermetic/near-hermetic encapsulation reliability, and

b) Through-glass-via (TGV) integration in blind cavities is much easier than in laminated glass cavities, which pose challenges like:

-   differential etch rates through glass and interfacial bonding material

-   panel level layer to layer via registration and

-   reliable contact between metallized through vias
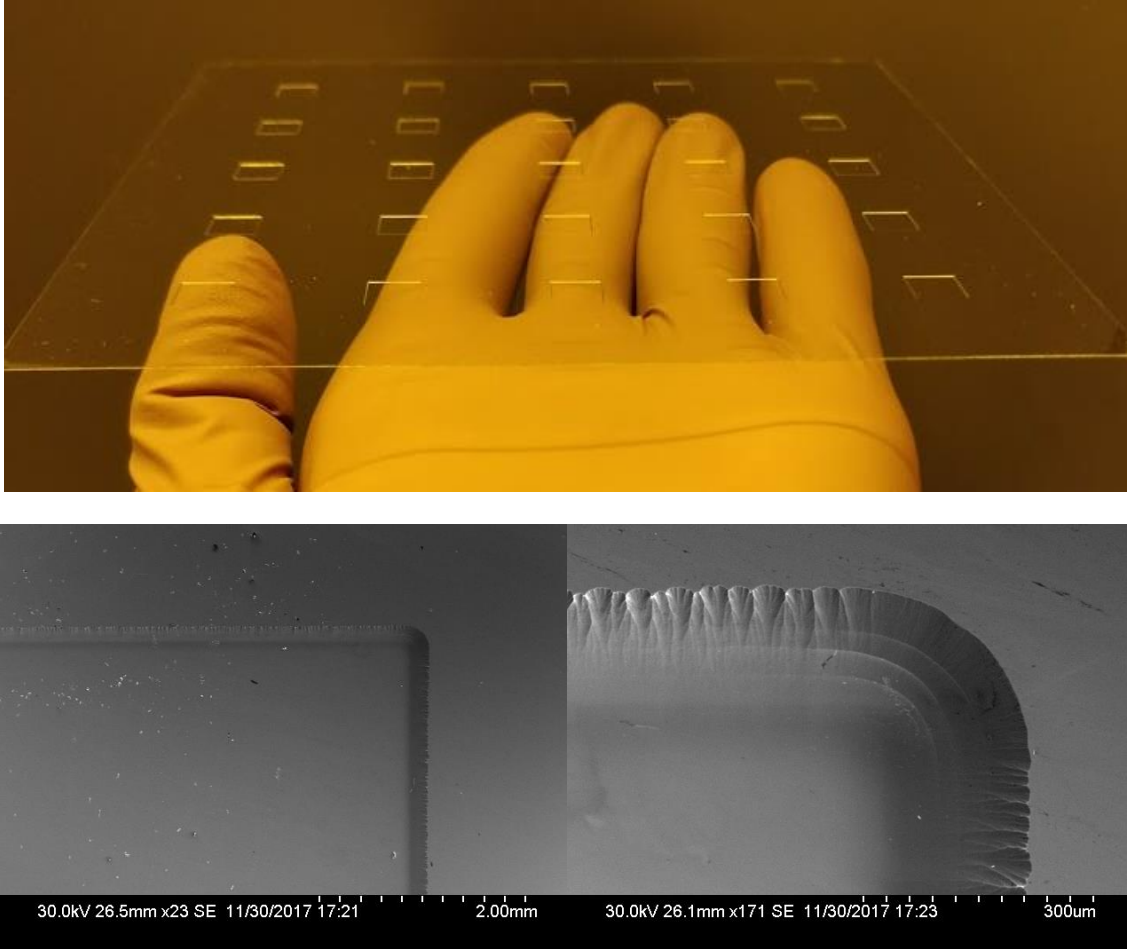
Figure 34: Blind cavities formed using advanced hybrid wet etch processes

Figure 34 above shows the preliminary demonstration of blind cavities machined in 200µm thick, four-inch glass panels. Cavities measuring 7.7 mm x 7.7 mm were wet-etched to an average depth of 101.8 µm using appropriate HF concentration and process temperatures. Process induced taper was observed to be between 155 µm - 175 µm and profilometry results showed fairly smooth cavity base, with an average roughness of about 0.5 µm, as illustrated in Figure 35 and Figure 36 below.
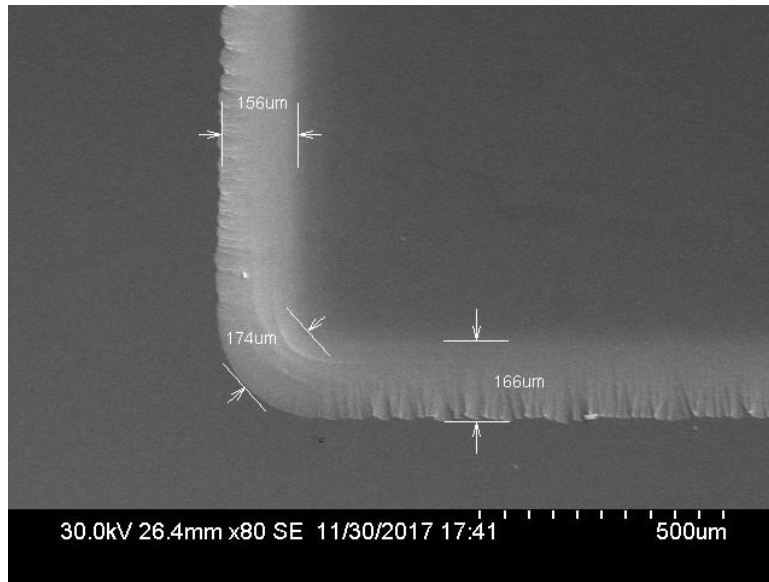
Figure 35: SEM image showing process induced taper of 155 μm – 175 μm
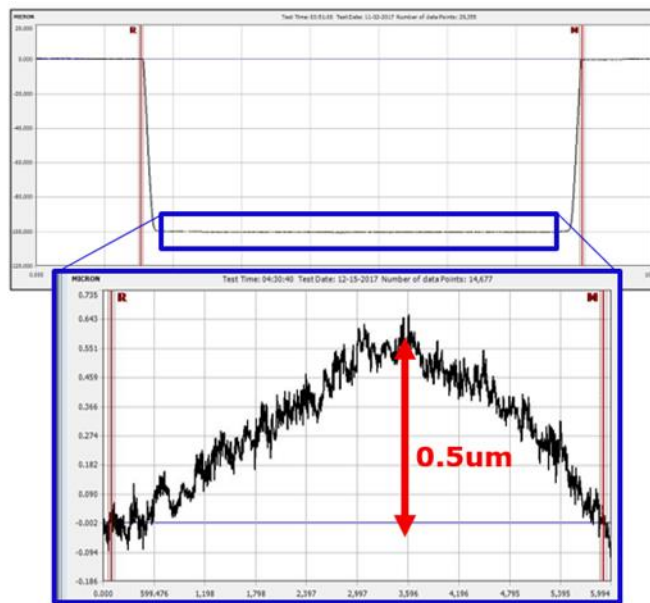
Figure 36: Cavity base surface roughness profile shows roughness of about 0.5 μm

CHAPTER 4

LOW STRESS GLASS-GLASS BONDING

This chapter discusses the advances in low stress bonding technologies for bonding ultra-thin glass panels along with discussion of bonding interface material selection, bonding mechanisms and processes, characterization and reliability results.

4.1 Adhesive bonding

As discussed in Chapter 2, anodic bonding is the most prevalent direct bonding technique that ensures hermetic and robust bonds when used for glass wafer-wafer bonding. However, it poses challenges such as material restrictions, high temperature induced residual thermo-mechanical stresses and potential damage to MEMS structures due to high electromotive forces. Alternatively, indirect bonding techniques that employ eutectic metal bonds or intermediate materials like glass frit pastes, metallic thin films involve high processing temperatures which may lead to critical failures, especially in thin glass panels with vulnerable, stress concentration sites like cavity corners. While adhesive bonding has been pursued at wafer level for silicon-silicon and silicon-glass bonding, there is a lack of detailed research on glass-glass bonding using polymer adhesive thin-films and its reliability in humid environments.

Polymer adhesives were chosen as the interface bonding material for bonding thin glass substrates for a variety of reasons. Most importantly, adhesive bonding occurs at significantly lower temperatures without the use of any voltages as compared to anodic bonding. Due to their elastic properties, polymer adhesives act as stress buffers between

46

the substrates to be bonded, and therefore, are very effective in decoupling package induced stress from the device. Materials and processes involved are simple, low cost and can tolerate surface non-uniformities, thereby achieving high bonding yield with robust adhesion to a variety of dissimilar substrates. Adhesives can be patterned by dry etching, laser ablation or by lithography in case of photosensitive versions which is important in case of area selective bonding. Finally, adhesive bonding processes are compatible with existing packaging foundry tools and mature infrastructure.

In this dissertation, two thin film polymer adhesives were evaluated for their glass-to-glass bond strength and bond reliability. Variations in process parameters were studied to achieve optimal bonding efficiency and to eliminate interfacial voids. Preliminary thermal cycle reliability was demonstrated, and the results also demonstrate the near-hermetic reliability of adhesive seals in corrosive environments.

4.2 Adhesive bonding mechanism, material selection and process advances

Proper bonding requires that the two substrates be brought in sufficiently close contact. In case of indirect bonding using polymer adhesives, close contact is enabled by mechanical compliance (deformability) and wettability of the polymer on the substrate surfaces under influence of external forces like temperature and pressure. These properties help compensate for the glass surface roughness that would otherwise prevent large-surface-area contact, as illustrated in the Figure 37 below.

47
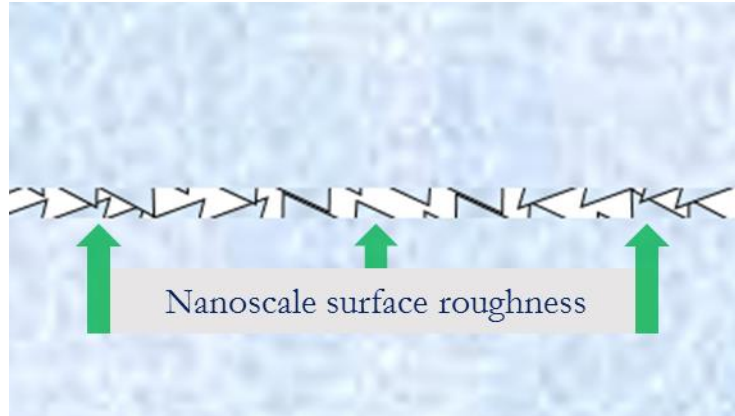
Figure 37: Concept image showing close up view of glass-glass contact interface with nano-scale roughness

Figure 38 shown below highlights the properties of polymer adhesives that help in glass-glass bonding. At elevated temperatures, the viscosity and modulus of polymer adhesives reduces, resulting in improved wettability and deformability. For any polymer in the semi-liquid/liquid phase to sufficiently wet the substrate, the substrate's surface energy must exceed that of the adhesive. Surface contaminants like dust, organic particles and moisture reduce the surface wettability by reducing the surface energy. Therefore, wettability of the liquid-like adhesive on substrate surfaces can be further improved by adequate surface modification steps like surface cleaning and use of adhesion promoters to increase the surface energy of the substrate. Adhesion promoters that are tailored to the adhesive-substrate combination result in stronger, more robust chemical bonds. Additionally, optimized curing processes to appropriately harden the liquid like polymer into a material that can hold the substrates together by mechanical interlocking further ensures strong bonds. Therefore, it follows that to achieve high quality substrate bonding, material selection and process optimization steps are critical.
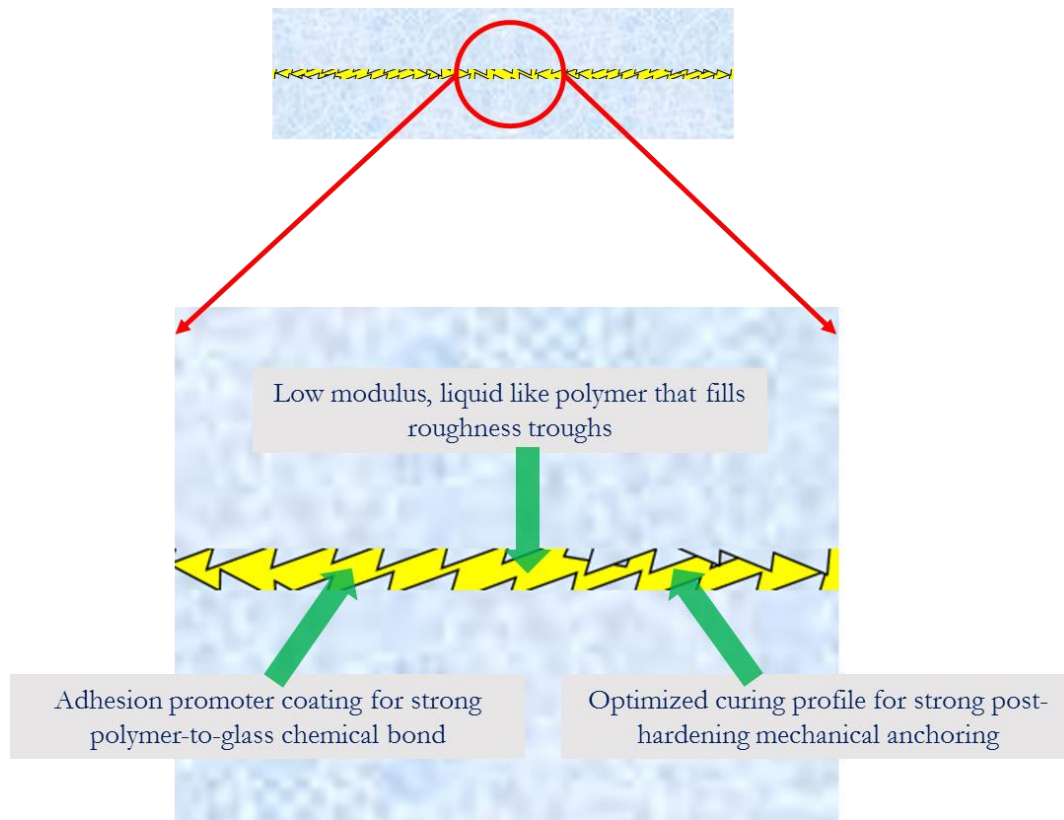
Figure 38: Concept image highlighting role of polymer adhesive dry films in glass-glass bonding

Figure 39 below shows the process flow for panel bonding of ultra-thin glass substrates, with and without cavities, using polymer adhesive dry films. The process begins with a standard IPA/acetone cleaning step to remove organic impurities, dust and other contaminants, followed by an O_2 plasma clean step for 10 minutes with a flow rate of 100 sccm, RF power of 400W at 30°C in a dry etch plasma tool by PlasmaEtch, Inc. Next, the glass panels with through cavities formed as described in chapter 3 are coated with adhesion promoters in the liquid or vapor state followed by vacuum lamination of the dry film polymer adhesive according to prescribed temperature-pressure-time parameters. The glass panel and polymer adhesive dry film stack-up is sandwiched between two metal hotplates in the Meiki MVLP-300 vacuum laminator, as shown in Figure 40. Next, these

panels are bonded to the carrier glass panels containing metallized through-package vias (TPVs) and fabricated RDL in a lamination step which is identical to the previous polymer lamination step. Finally, the bonded panels are cured in an appropriate atmosphere and temperature.
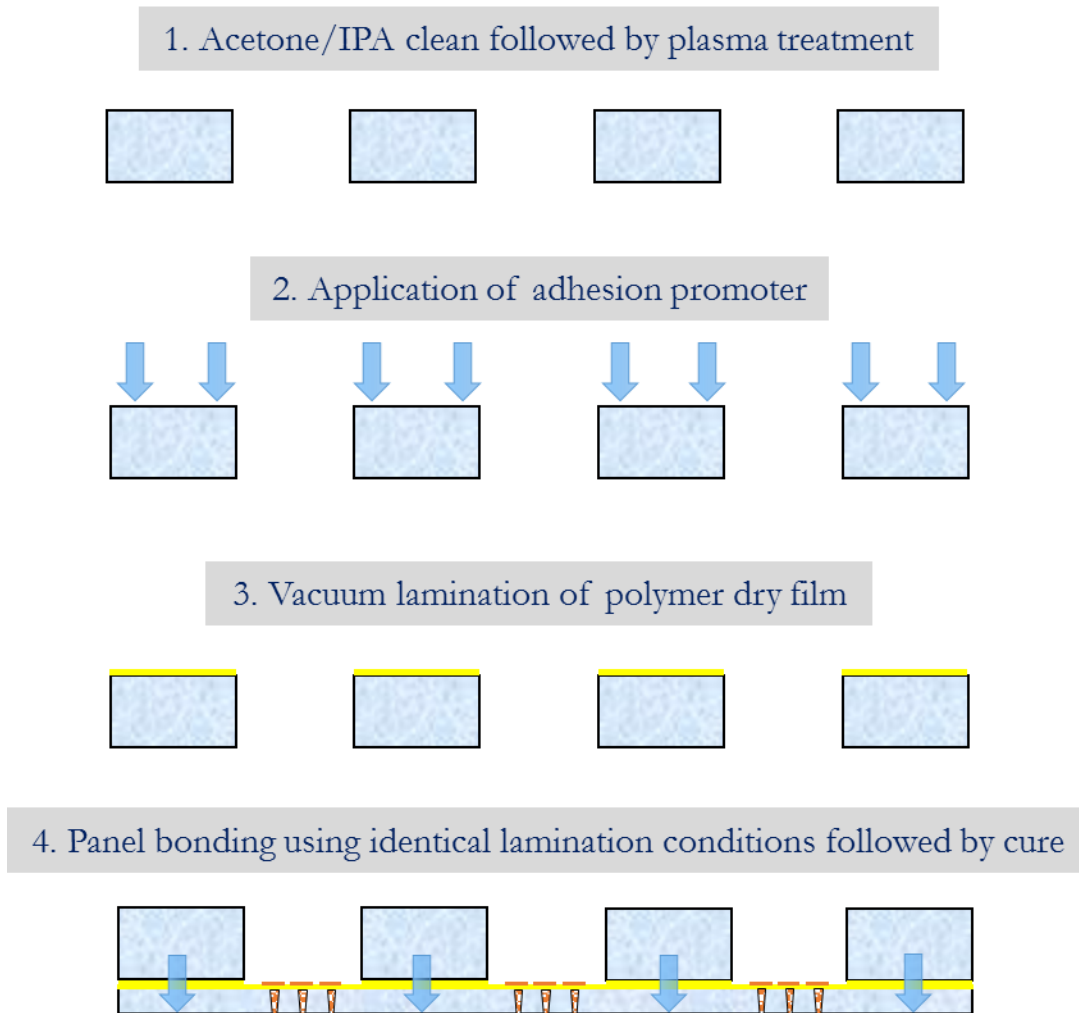
Figure 39: Process flow for glass-glass panel bonding using polymer adhesive dry films
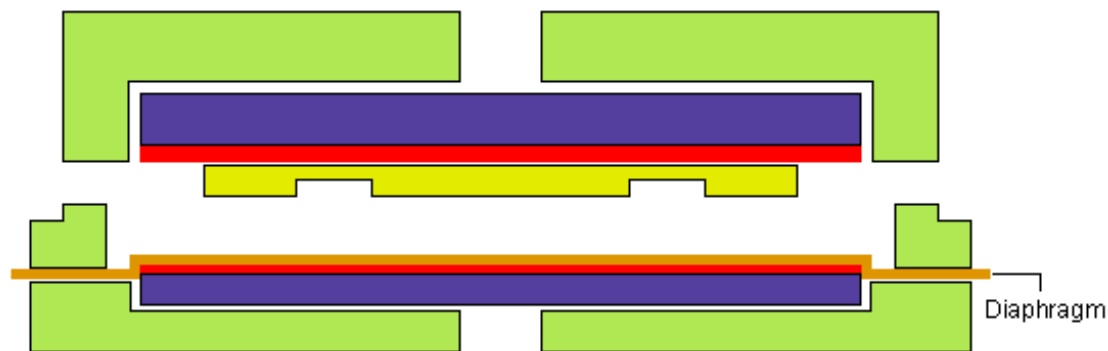
Figure 40: Image showing sample sandwiched between two metal hotplates in the Meiki Laminator

Two dry film thermosetting polymer adhesives were selected for evaluation of glass-glass bonding: (a) ABF GX-92 (hereafter referred to as ABF) from Ajinomoto Fine Tech Co., Inc. and (b) Benzocyclobutene (BCB) from Dow Chemical Co., properties of which are listed in the Table 4 below.

Table 4: Properties of polymer adhesive dry films used

Supplier	Trade Name/Type	Thickness (μm)	Young's Modulus (GPa)	T_g (°C)	CTE (10^{-6} K^{-1})
Ajinomoto FineTech Co. Inc.	ABF GX-92	5/10/15/25	5	153	39
Dow Chemical Co.	BCB	9/19	2.8	>350	42

51

For ABF, 0.9% (3-aminopropyl) triethoxysilane vapors (99%, Sigma-Aldrich) was used as the adhesion promoter, where self-assembled-monolayers (SAM) of silane molecules were deposited when cured at 70°C for 20 minutes. For BCB, the recommended adhesion promoter was AP3000, which is an organosilane coupling agent in an organic solvent. These silane molecules form strong chemical bonds through hydrolysable alkoxy groups on the glass surface side and strong physical bonds with the polymer on the other side through polarizable side groups, as illustrated in the Figure 41 below.
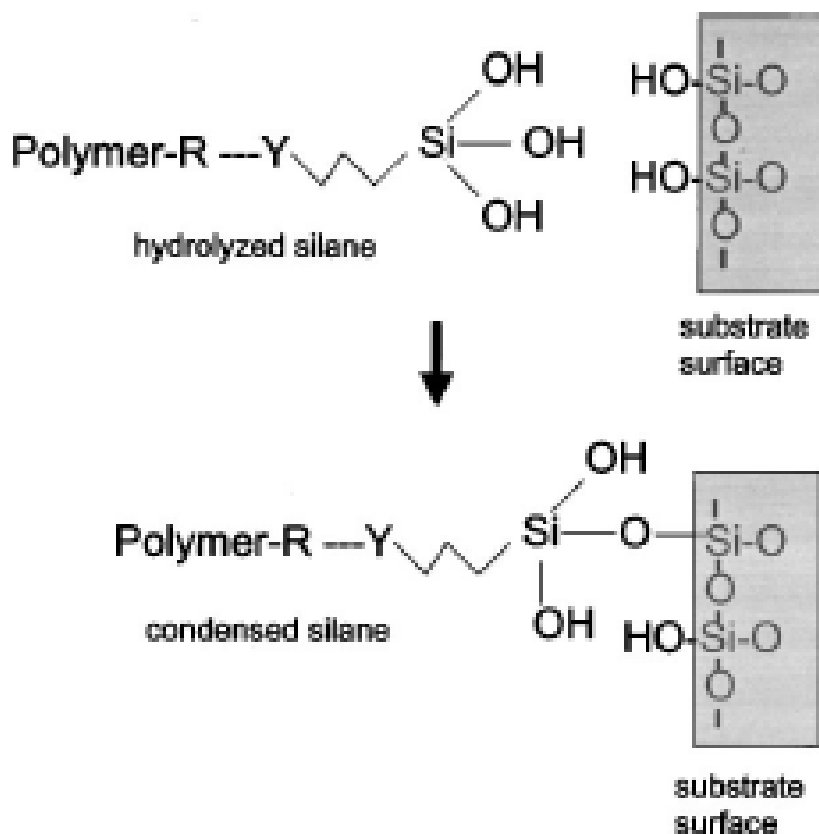
Figure 41: Image showing role of silane-based adhesion promoter to enhance adhesion of polymer adhesive dry films to glass [67]

Next, the respective dry film polymer was laminated on the glass substrate using the Meiki MVLP-300 vacuum lamination tool. The substrate with the overlying dry film was

placed between the tool's hot plates, followed by lamination at the recommended conditions, shown in Table 5 below.

Table 5: Lamination conditions used to polymer adhesive dry film lamination as well as glass-glass panel bonding

Dry Film Polymer	Temperature (ºC)	Pressure (MPa)	Vacuum Dwell (s)	Pressure Dwell (s)
ABF GX-92	90	0.3	90	30
BCB	120	0.6	90	30

After polymer lamination, the carrier glass substrate was placed underneath the laminated glass substrate such that the polymer faces the carrier and similar conditions as listed in Table 5 were used to bond the two glass substrates together in a pre-cure step.

Table 6: Cure conditions for the polymer adhesive dry films used for glass-glass panel bonding

Dry Film Polymer	Ambient	Cure Temperature (ºC)	Cure Time (minutes)
ABF GX-92	Air	180	30
BCB	N_2	250	60

Finally, the bonded samples were cured at conditions given in Table 6 above. It is important to note that BCB requires an inert atmosphere during the curing step, as it oxidizes at temperatures > 150ºC.

4.3 Glass-glass Bonding Characterization and Void Reduction

Dry film polymer adhesives used for wafer/substrate bonding often give rise to interfacial defects like voids, cracks and delaminated areas. These defects propagate easily to form continuous cracks at the bonded interface during temperature excursions that occur over its lifetime, which leads to total bond failure. Besides, voided areas directly result in bond strength reduction, as experimentally observed and reported in the later sections. Therefore, defects must be eliminated for maximum bond strength and bond reliability. Three main factors that give rise to such defects are:

a) Surface roughness/non-planarity of polymer coating,

b) Volatile impurities that outgas and get trapped at the interface between the substrates,

c) Volume shrinkage during cure leading to stresses that cause interfacial delamination

Therefore, it is evident that the material properties are the important factors that impact void formation. The dry film polymers selected for use in this study have specific characteristics to minimize interface defect formation: ABF GX-92 has low surface roughness while BCB shows little to no outgassing from volatile components and <5% shrinkage.

This section discusses the characterization of interfacial defects and resulting bonding efficiency and process advances to mitigate the defects to achieve ~100% bonding efficiency.

4.3.1   Void characterization

Figure 42 below shows the test samples used for characterizing interfacial voids. Commercially available thick glass slides were used as carriers on which 300µm thick square glass pieces measuring ¼ inch x ¼ inch were bonded using the same materials and processes discussed in the previous section, with optimized bonding parameters. These samples were also used for the die shear test for bond strength characterization, discussed in the next sub-section.
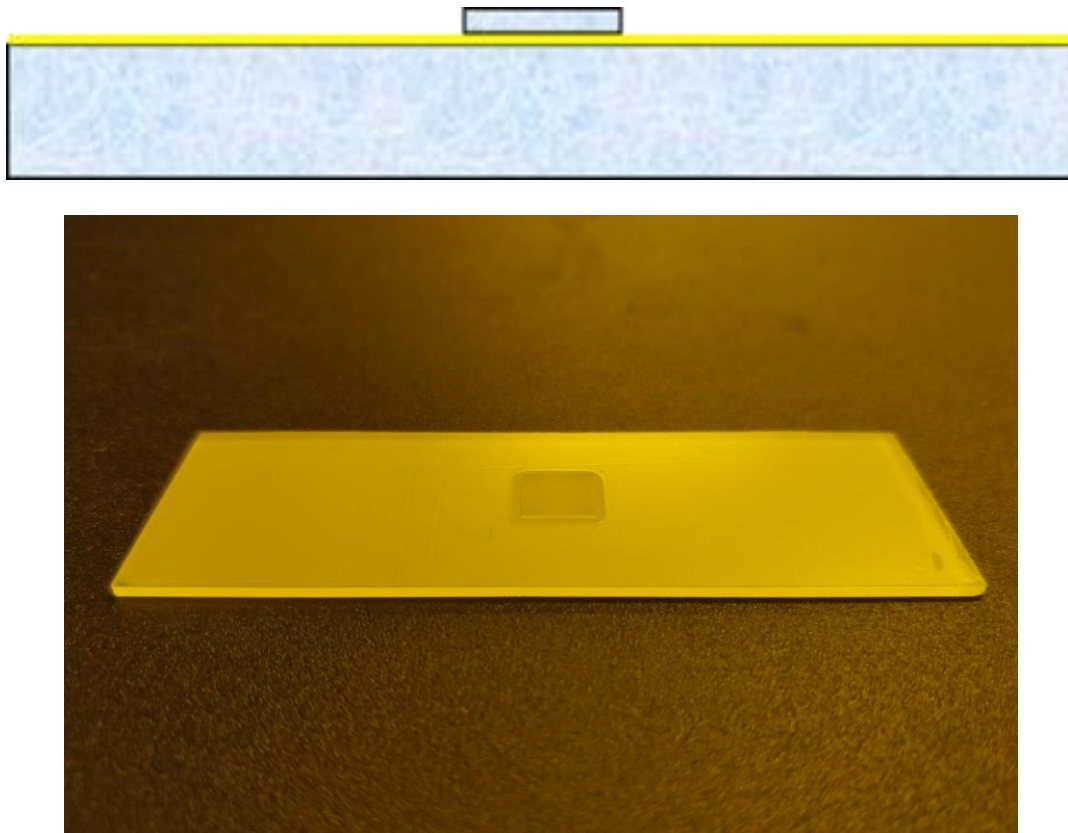
Figure 42: Cross section (top) and actual sample used for characterization of interfacial voids

The samples shown in Figure 42 above were characterized for void formation using the non-destructive Confocal Sonic Acoustic Microscopy (C-SAM) tool provided by

Sonoscan, Inc. By adjusting the z-height of the transducer, varying the time of flight of the sound waves through water and the sample and based on the echo peaks, the interface of interest between the small glass piece and polymer adhesive was identified and imaged.

a) *ABF GX-92 bonded samples*

The bonding parameters for ABF-bonded samples were recommended by Ajinomoto Co., Inc and were identical to ABF lamination conditions. Figure 43 below shows the CSAM image of the sample interface, where the grey square indicated the bonding interface. The absence of brighter white spots within the bonded area indicate that no voids, cracks or edge/corner delamination was observed, indicating a bonding efficiency of ~100%.
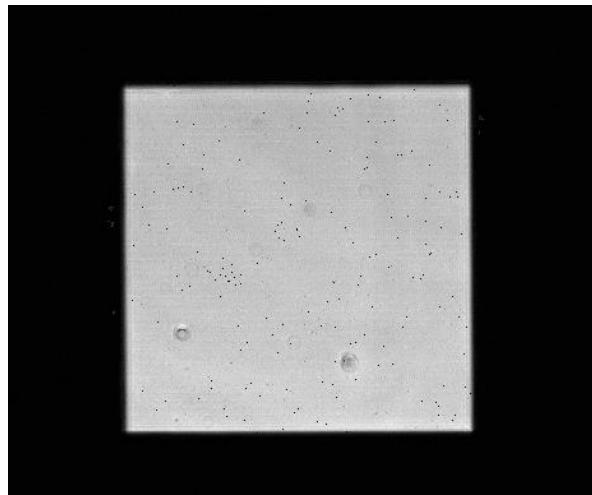
Figure 43: CSAM image of ABF GX-92 bonded sample showing ~100% bonding efficiency

b) *BCB bonded samples*

Two approaches were explored to optimize the bonding parameters for BCB bonded samples:

i) Pressure assisted bonding

Increased bonding pressure helps eliminate voids by closing non-uniformity induced interfacial gaps that create the voids. In this method, the bonding temperature was fixed at 120°C, vacuum and pressure dwell times were fixed at 90 seconds and 30 seconds respectively whereas the bonding pressure was varied from 0.2 MPa to 0.8 MPa. Table 7 below shows the percentage voided area for each set of conditions, computed using a commercial image processing software.

Table 7: Impact of pressure on voided area and corresponding CSAM images
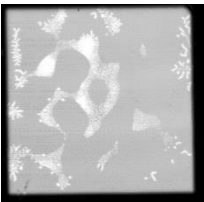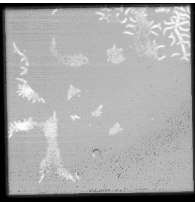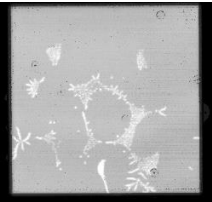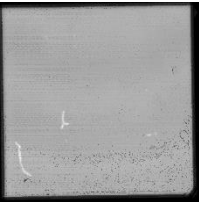
Pressure	0.2 MPa	0.4 MPa	0.6 MPa	0.8 MPa
No. of Samples	3	3	3	3
Average Voided Area	17.7%	10.48%	8.39%	4.55%
CSAM Image of bonding interface				

Figure 44 below shows that pressure assisted bonding enhances bonding efficiency by 16%, reducing the percentage voided area from 17.7% to 4.55%.
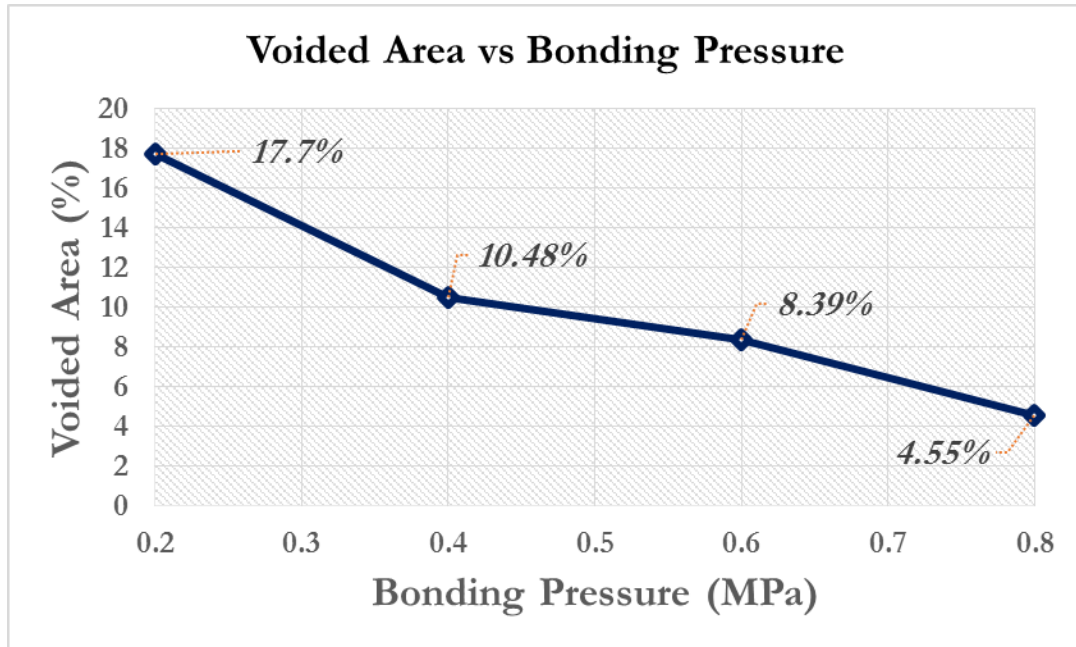
Figure 44: Graph showing reduction in voided area with an increase in bonding pressure

ii) **Variation in BCB lamination conditions for reduced pre-cure surface roughness**

Pressure assisted bonding enhanced the bonding efficiency up to ~95% but did not eliminate voids. It is hypothesized that unavoidable shear components that arise from higher pressures prevent complete elimination of voids by causing localized non-uniformities at the glass-polymer-glass interfaces. Therefore, further process improvement was necessary to minimize waviness and surface roughness to eliminate the need for higher pressures during bonding. Table 8 below shows the optimized lamination process parameters.

Table 8: Optimized lamination conditions to reduce pre-cure surface roughness

Dry Film Polymer	Temperature (°C)	Pressure (MPa)	Vacuum Dwell (s)	Pressure Dwell (s)
BCB	110	0.25	30	60

Next, a new set of BCB laminated samples were prepared using these optimized process parameters and the pre-cure surface roughness was measured and compared to that of the samples laminated using previous set of parameters, the results of which are shown in Table 9 below.

Table 9: Impact of optimized lamination conditions on pre-cure surface roughness

Roughness parameter	Old conditions (μm)	New conditions (μm)	Roughness reduction (%)
Average R_a	0.0539	0.0423	21.5
Average R_z	0.3344	0.5356	37.6

Finally, BCB bonded samples were prepared with bonding parameters identical to the optimized BCB lamination conditions shown in Table 8. As seen in the CSAM image below in Figure 45, full area void free bonding was achieved.
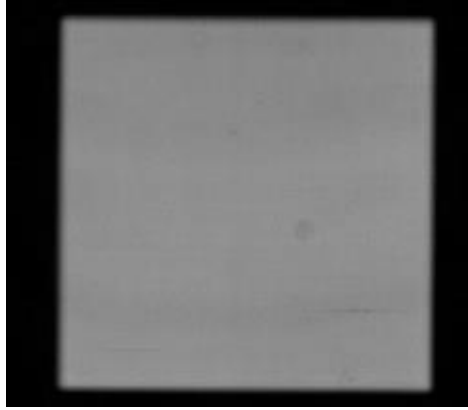
Figure 45: CSAM image of sample bonded using optimized conditions to achieve ~100% bonding efficiency

4.4 Bond shear strength characterization

Using the optimized bonding processes described in the previous section, ABF and BCB bonded samples were prepared and die shear tests were conducted to characterize bond strength, as illustrated in the schematic below. By subjecting the samples to a stress parallel to the plane of the polymer adhesive, shear forces are introduced at the two polymer glass interfaces. The die contact tool applies an increasing load on the glass edge till the shear stress overcomes the bond strength at which point failure occurs and the glass piece is chipped off, as shown in Figure 46 below.
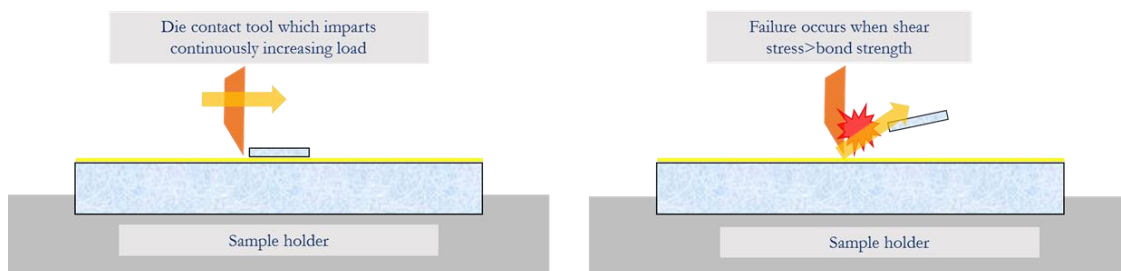
Figure 46: Bond strength characterization technique using die shear test tool

The shear strength was measured using the industry standard CONDOR from XYZTECH and Nordson Dage die shear test tools. Shear height was set as 15µm for the sample of thickness 300µm and a maximum load of 200 kilograms was applied. Results of the test for ABF and BCB bonded samples are summarized in Table 10 below.

Table 10: Shear strength of glass-glass samples bonded using ABF GX-92 and BCB

Dry Film Polymer	Bonded Area (mm^2)	Number of Samples tested	Average Shear Force (Kgf)	Average Shear Stress (MPa)
ABF GX-92		10	71.14	17.29
BCB (conditions as listed in Table 5)	40.3225	10	89.39	21.73
BCB (conditions as listed in Table 8)		10	91.83	22.32

It was observed that shear strengths for samples bonded using both ABF and BCB well exceeded the requirements of MIL-STD-883 method 2019.5 which states that for areas larger than 4 mm^2 the shear force must exceed 2.5kgf/25N. ABF bonded samples sustained an average force of 71.14 Kgf corresponding to a shear stress of 17.29 MPa. BCB-bonded samples using conditions listed in Table 5 and Table 8 respectively failed under a shearing force of 89.39 Kgf and 91.83 Kgf, corresponding to 21.73 MPa and 22.32 MPa respectively. This marginal increase in bond shear strength observed in the BCB bonded samples can be attributed to the improved bonding efficiency that results from

optimized BCB conditions. The recorded shear strength values are also greater than those observed in previous work involving BCB and SU-8 [68-70].

4.4.1 *Impact of BCB bonding process selection on shear strength*

As part of the studies to analyze the impact of pressure on interfacial defects, the corresponding shear strengths were also analyzed. As illustrated in Figure 47 below, the decrease in interfacial voids corresponded to a rise in the shear strength values. With an increase in contact area between polymer and glass, bond efficiency increases and a higher shearing force was needed to cause failure. This is confirmed by a distinct rise in shear strength from 19.67 MPa corresponding to 82.3% bonding efficiency to almost 22 MPa corresponding to > 95% bonding efficiency.
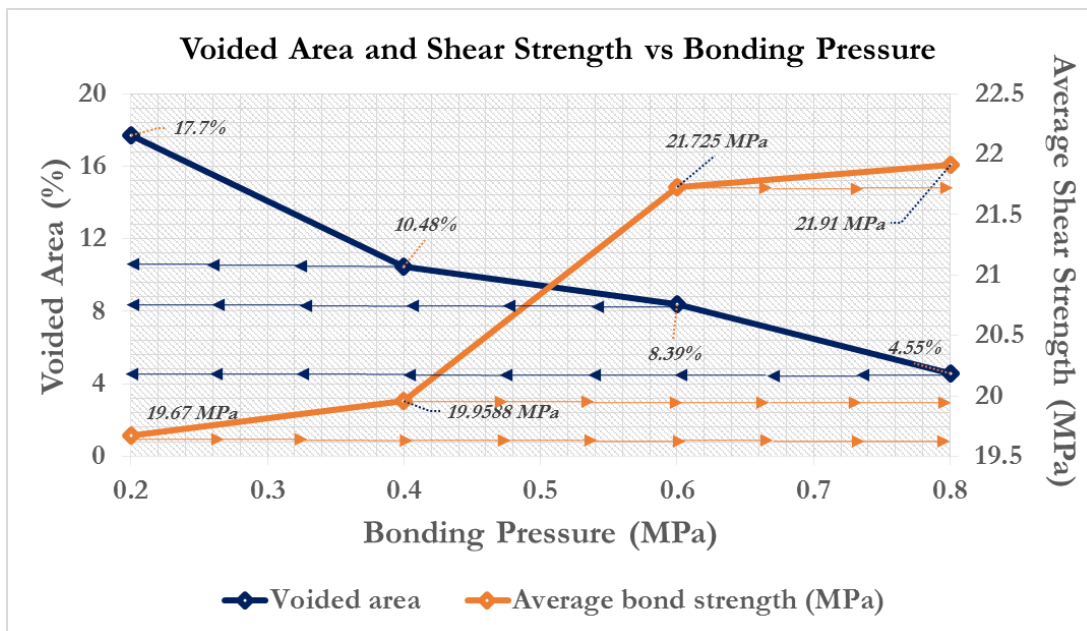
Figure 47: Impact of pressure assisted bonding on bonding efficiency and corresponding impact on bond strength

62

Despite the obvious improvement in bond quality in terms of efficiency and robustness, increased bonding pressure puts ultra-thin glass panels at higher risk of cracking due to the brittle nature of glass. Therefore, an optimal solution that mitigates interfacial defects and maintain robustness of the bond while requiring low values of bonding pressure is desired. This was achieved through optimization of BCB lamination conditions to minimize pre-cure roughness, as discussed in section 4.3.1 (b) (ii).

4.5 Reliability studies

An initial investigation of the thermo-mechanical reliability of adhesively bonded glass-glass samples was undertaken. Samples fabricated using optimized bonding process conditions were tested for shear strength degradation after thermal cycling between temperature extremes to accelerate failures. The samples were first subjected to a 24-hour bake at 125°C, followed by accelerated moisture sensitivity level 3 (MSL-3) preconditioning (60°C, 60% RH for 40 hours), and three times reflow at a peak temperature of 260°C, to simulate the lead-free board assembly processes. These preconditioning steps identify early failures like delamination, cracking, voiding and swelling due to moisture absorption and CTE mismatch with glass. The samples were then subjected to thermal cycles between -55°C and 125°C with a dwell-time of 15 minutes at each temperature extreme, as described in JEDEC JESD22-A104 condition B test standard, with shear strength measurements after 100, 300, 500, 700, 1000 cycles. Degradation of average bond shear strength to 2.5 Kgf and below is chosen as the failure criteria.

As plotted in Figure 48 below, samples bonded using original ABF GX-92 conditions and the optimized BCB conditions showed no degradation in bond strength over 1000 thermal cycles. In fact, the bond shear strength for ABF GX-92 and BCB improved to about

21 MPa and 25 MPa respectively, which can be attributed to greater extent of thermally-induced cross-linking that occurs within the polymers over successive thermal cycles.
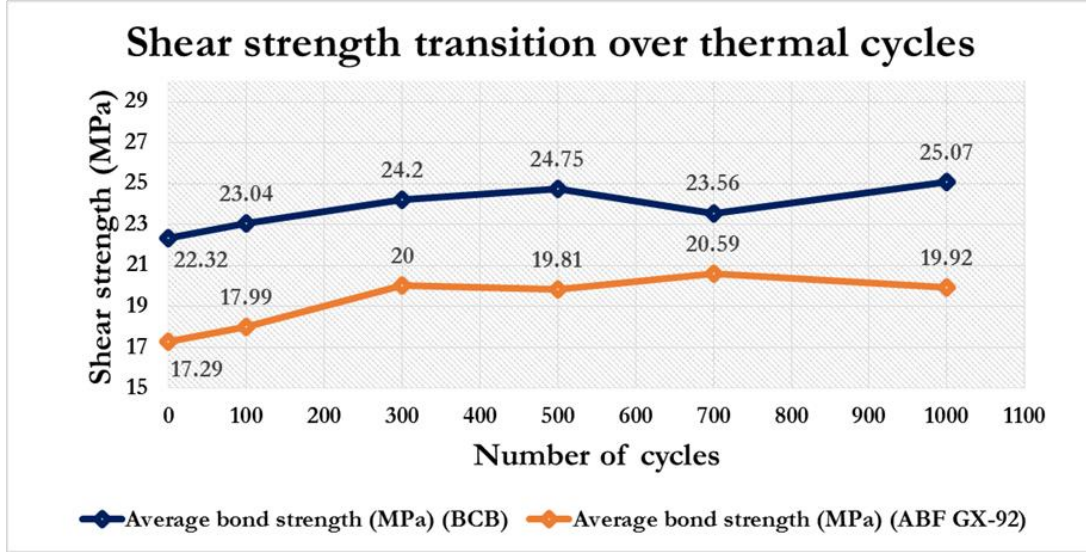
Figure 48: ABF GX-92 and BCB bond shear strength transition over 1000 thermal cycles

4.6 Summary

In this chapter, adhesive bonding of ultra-thin glass panels was explored and demonstrated as a low stress bonding technique. The case for adhesive bonding was established by discussing its advantages over anodic bonding on various fronts. Next, the theory and mechanism of adhesive bonding was discussed together with details on bonding process and material selection. ABF and BCB dry film polymer adhesives were evaluated and characterized for bonding efficiency as well as shear strength, with a detailed discussion of two different approaches undertaken to improve the two metrics: a) use of added pressure and b) optimization of process parameters. Impact of pressure assisted bonding on shear strength was studied. Finally, thermo-cycling reliability of the two polymer adhesives was characterized. Results of this study were used to bond a carrier

64

glass panel to a glass panel with through holes to form a cavity structure described in Chapter 3, as shown in Figure 49 below.
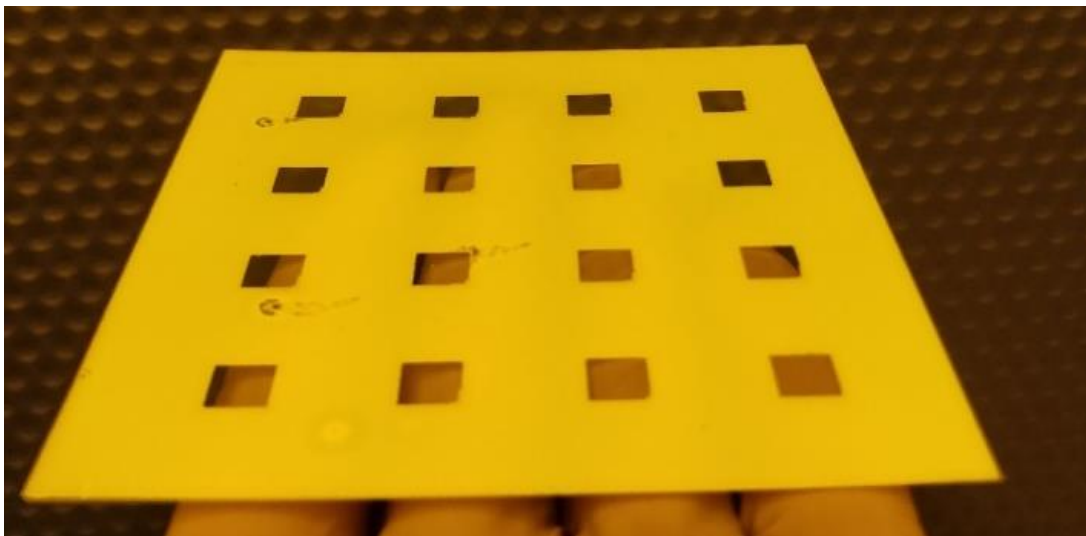
Figure 49: Glass cavity panel bonded to a glass carrier using BCB and ABF GX-92

CHAPTER 5

HIGH THROUGHPUT, FULLY-FILLED THROUGH-PACKAGE VIAS IN GLASS FOR CAVITY PACKAGES

Through-package-vias (TPVs) are used for vertical interconnections between ICs to reduce the interconnection length compared to lateral interconnects and improve electrical performance. This research explores and demonstrates a high-throughput, low temperature through-via metallization process using stencil printing of conductive copper paste, cured at less than 200ºC. In contrast to prior work on copper plated fully filed TPVs, the paste filled vias offer several advantages including short processing times leading to higher throughput, better yield and better stress management. The copper paste material properties, curing mechanism and process yield studies are discussed in this chapter. Further, a hybrid TPV design to improve the high frequency performance of copper paste filled TPVs is proposed and initial modelling results to verify this hybrid TPV concept are presented.

5.1 Need for Alternate Metallization Process for Fully Filled TPVs

As discussed in Chapter 2, via filling has been achieved in the past by electrolytic copper plating, use of tungsten/FeNi plugs and high temperature sintered paste filling (Au particles/Cu pastes). Direct copper plating on glass creates potential risk of thermomechanical reliability failures due to the CTE mismatch between glass (3-9 ppm/ºC) and copper (17ppm/ºC) and hence requires thin polymer stress buffer liners for high reliability, especially for larger diameter vias. Additional challenges for fully filled TPV copper electroplating include void formation leading to reliability failures, and long

processing times leading to increased cost. Use of sintering pastes often require long sintering cycles at high temperatures (>500C), which induces stress in ultra-thin glass substrates. While copper paste filled through-glass-vias have been previously demonstrated [59], further research is needed in this area to develop scalable processes that achieve hermetic through-glass vias at high yield with high frequency performance and thermomechanical reliability comparable to electroplated copper filled TPVs.

5.2 Transient Liquid Phase Sintering (TLPS) Pastes

Sintering in general refers to the phenomenon where metal particles fuse together under the influence of thermal energy to form a bulk metallic phase. Transient Liquid Phase Sintering in contrast involves two components, one of which is a low melting point alloy and the other is a high melting point metal. Further, at least one of the components in the alloy is highly soluble or reactive with the metal particle, resulting in formation of intermetallic species with special properties like high re-melt temperature and electromigration resistance.

The concept of TLPS has been exploited by Ormet Circuits, Inc. /Merck KGaA to formulate pastes that comprise of copper particles as the high melting point metal and a tin alloy as the low melting point alloy, mixed in specific proportions in an adhesive-flux polymer binder. The post-cure composition of the paste is shown in Table 11.

Table 11: Post-cure matrix components of TLPS copper paste with their melting points and proportions

Matrix components	Melting Point (°C)	Percentage of Matrix
Cu	1085	
Cu_6Sn_5	415	>85%
Cu_3Sn	640	
Bi	271	<15%

As shown in Figure 50 below, a line scan performed on a tin-alloy particle for elemental analysis using energy-dispersive x-ray spectroscopy (EDX) in a scanning electron microscopy (SEM) tool shows the presence of a tin-bismuth intermetallic.
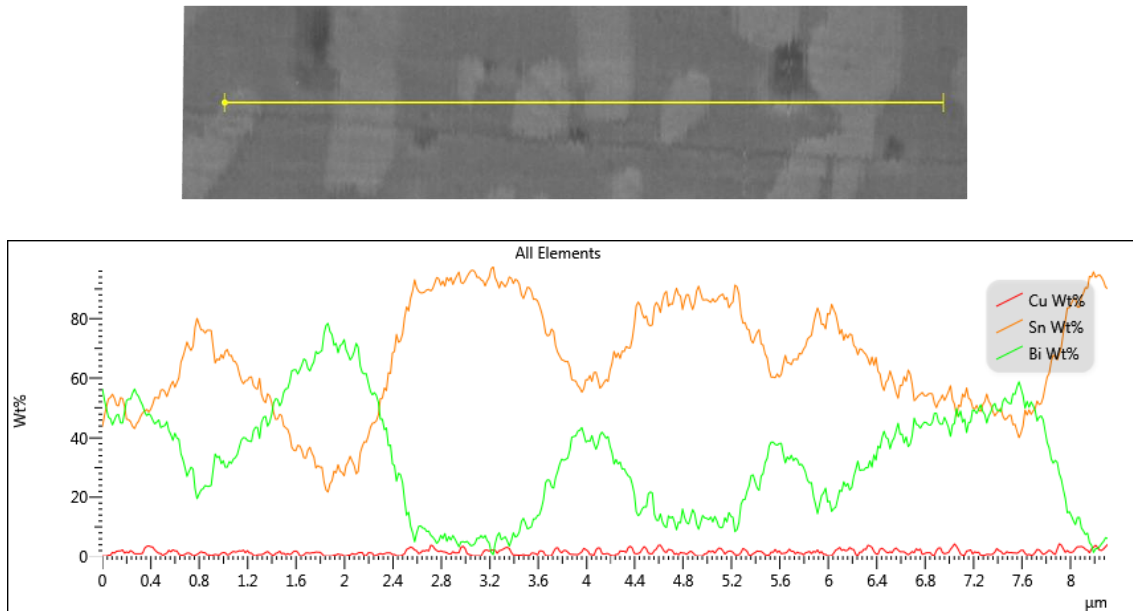
Figure 50: Line scan along a tin alloy particle showing presence of bismuth fillers

As the temperature is raised to near the melting point of the tin alloy (160 °C -190°C), the molten alloy particles flow and form a web of interconnections between the adjacent bulk copper particles to form intermediate species in-situ, listed in Table 11 above. The melting point of these intermetallics is greater than that of the original alloy. Therefore, they solidify instantaneously to form a matrix of interconnects with high metal loading of 97%. Figure 51 (a) shows partially melted tin alloy encapsulating the visible copper particles at 160 °C whereas Figure 52 shows the complete web of intermetallics formed when cured at 191°C.
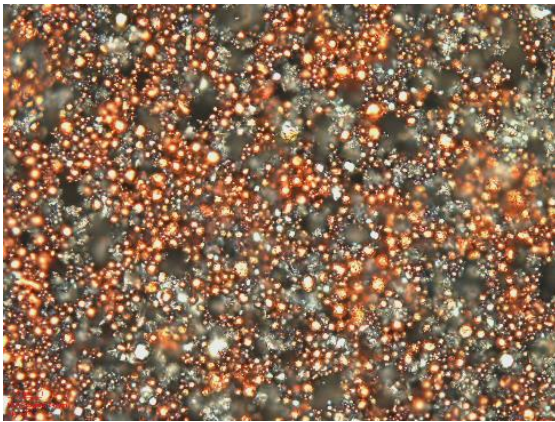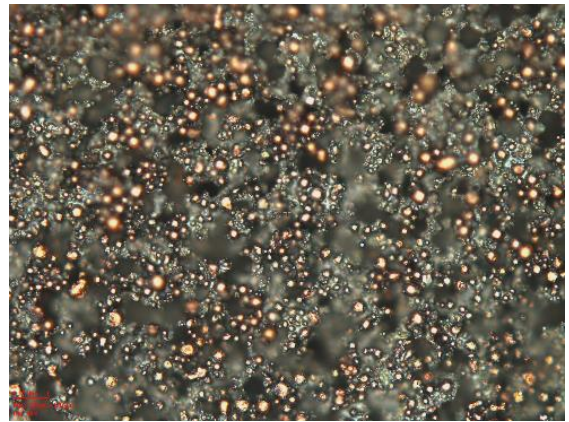
(a) (b)

Figure 51: Paste cured at (a) 160 °C & (b) 175ºC
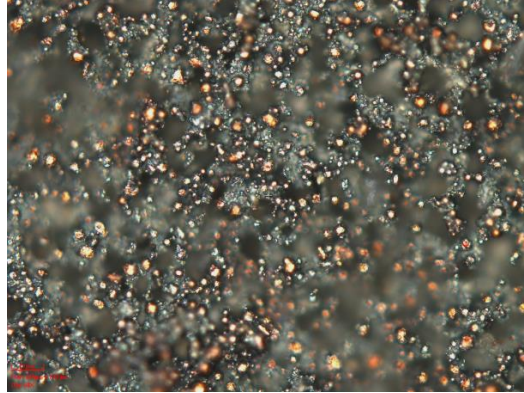
Figure 52: Paste cured at 191ºC

The metallurgical mesh formed provides a robust electrical interconnection. Further, the unconsumed fraction of tin alloy located interstitially re-melts partially through thermal cycles and acts as a stress buffer, thereby providing stability against mechanical shocks and thermal cycling. Lastly, since the interpenetrating metallurgical network undergoes reactions in a polymer matrix, it is also resistant to oxidative degradation, provides good adhesion to different substrate materials and has a low bulk modulus compared to copper.

Table 12: Properties of TLPS copper paste vs bulk copper

Property	Bulk Copper	TLPS Copper Paste
Young's Modulus (GPa)	117	<10
CTE (10^{-6} K^{-1})	17	22
Volume Resistivity (μohm-cm)	1.7-2	20-40

A major drawback of the polymer based binder is the increased resistivity of the paste, which degrades electrical performance, especially at higher frequencies. Relevant properties of the copper paste are shown in Table 12 above.

5.3 TPV paste fill process

This section discusses the process flow for TLPS copper paste filling in bare glass TPVs as well as TPVs with copper plated side walls. The via-fill process employs simple and low cost process tools to achieve high throughput, high yield metallized vias as described below.

A metal plate with a vacuum inlet was used for mounting the substrate. The sample substrate was placed on a piece of bleeder paper conducive to vacuum suction and the setup was taped down as shown in Figure 53 below. It is critical to place the sample substrate next to the vacuum suction hole instead of directly over it to avoid glass cracking.
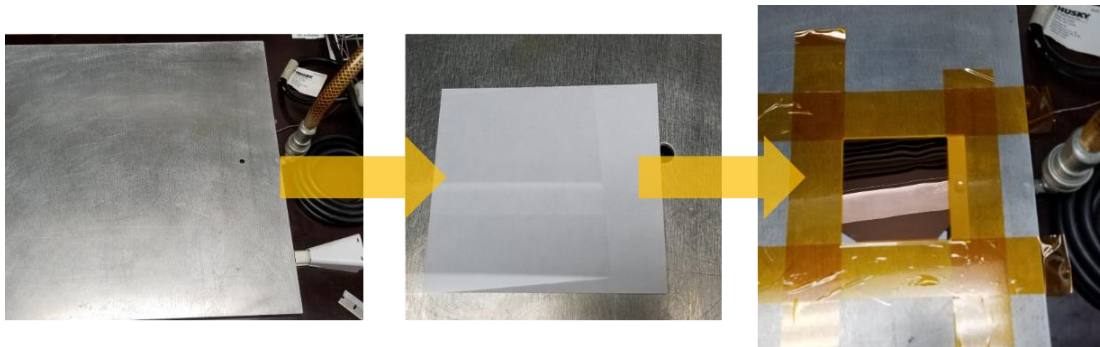
Figure 53: TPV paste fill process showing metal hotplate, bleeder paper and mounted substrate

Next, the metal plate was heated to 55°C and vacuum was applied to the setup. As shown in Figure 54, thick layer of copper paste was dispensed, lightly squeegeed entirely over the substrate area and allowed to rest for 30 seconds to allow the paste to completely

fill the TPVs with the help of the vacuum suction force. The squeegee was pressed over the substrate area with higher pressure repeatedly about 6-8 times to ensure complete fill. Finally, the vacuum was released and after a final squeegee press to clean the surface, the fill process was completed.
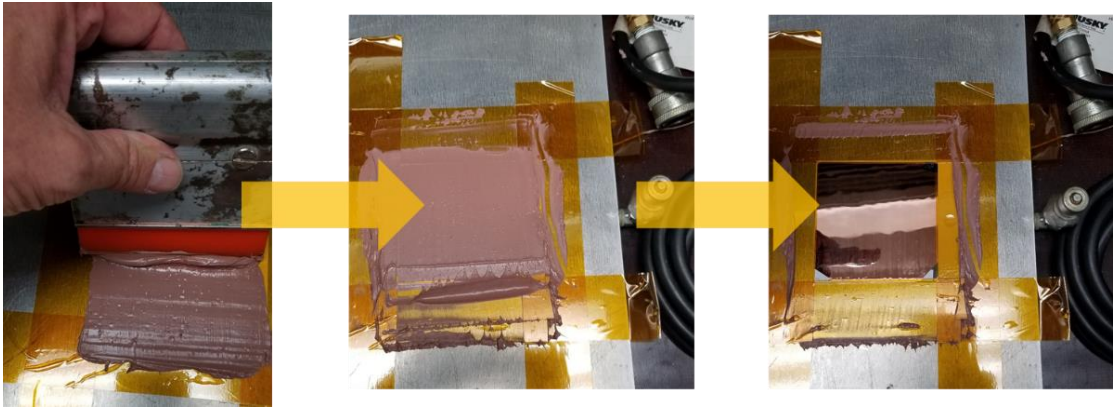
Figure 54: TPV paste fill process showing copper paste dispensed using squeegee followed by surface cleaning

The substrate was then released from the metal plate after carefully pulling the tape at a sharp angle. A blade was used to level paste fill on the top and bottom openings of the TPVs. Next, the bleeder paper was slid from underneath the substrate causing a shearing action as opposed to lifting or peeling, to avoid pulling the paste out of the TPV. As seen in Figure 55 below, the existence of paste marks on the bleeder paper indicate complete TPV fill. The substrate was pre-dried in a convection oven for 30 minutes at 95°C.

Figure 55: TPV paste fill process showing release of substrate and levelling the TPVs

After the pre-drying step, the substrate was allowed to cool down before it was prepared for the hard-curing step. A stack-up was prepared consisting of metal plates, Pacothane™ release sheets and Pacopads™, between which the paste filled glass substrate was sandwiched, as illustrated in Figure 56 below.
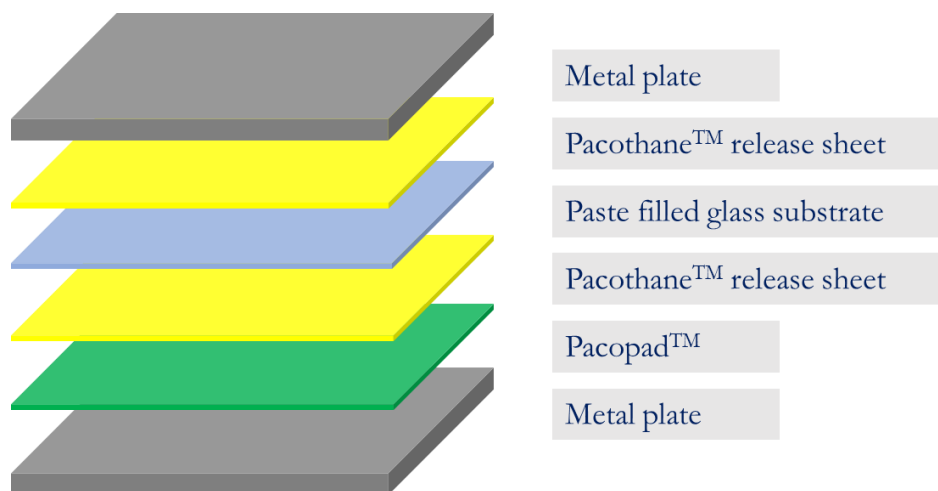
Figure 56: Stack-up used for paste curing step in lamination press

This stack-up was cured in a lamination press at 200ºC for 20 minutes under a pressure of about 50-75 psi followed by a cooling step before dismantling the stack-up and releasing the substrate. It is important to ensure that the metal plates are clean and free of debris to prevent cracking of the glass substrate.

The TPV fill process was demonstrated for small 30 µm diameter TPVs at 120 µm pitch in 130 µm thin glass as well as large 100 µm diameter TPVs at coarse pitch in 300 µm thick glass, as shown in in Figure 57 (a), (b), (c) and (d) below.

(a)

(b)

(c)

(d)
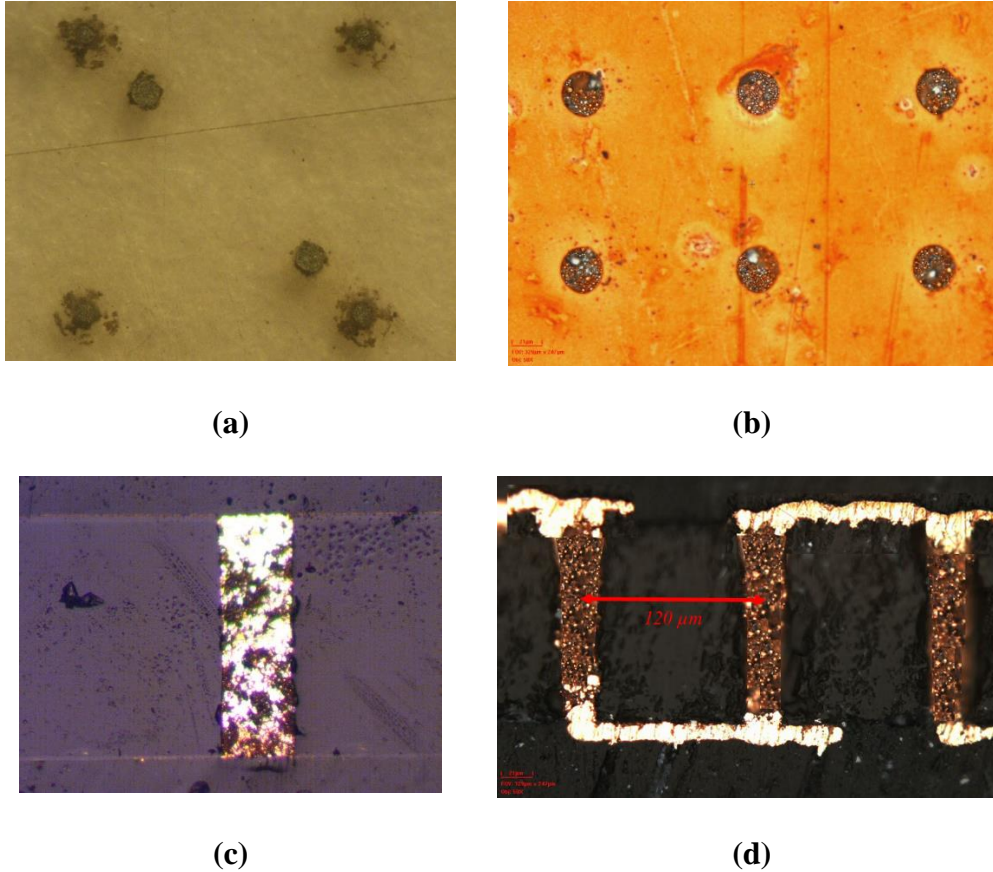
Figure 57: Top ((a) and (b)) and cross-sectional view ((c) and (d)) of paste filled TPVs of diameter 100 µm and 30 µm respectively

The paste fill process was tested on five glass panels with the 30 µm diameter TPVs and x-ray analysis was used to characterize the process yield. Each panel consisted of 16 arrays, each consisting of 16 x 16 TPVs at 120 µm pitch. X-ray images showed 100% yield, confirmed by the absence of white spots which signify voids in the metallized via arrays. Figure 58 below shows an x-ray image of one of the 16 x 16 arrays.
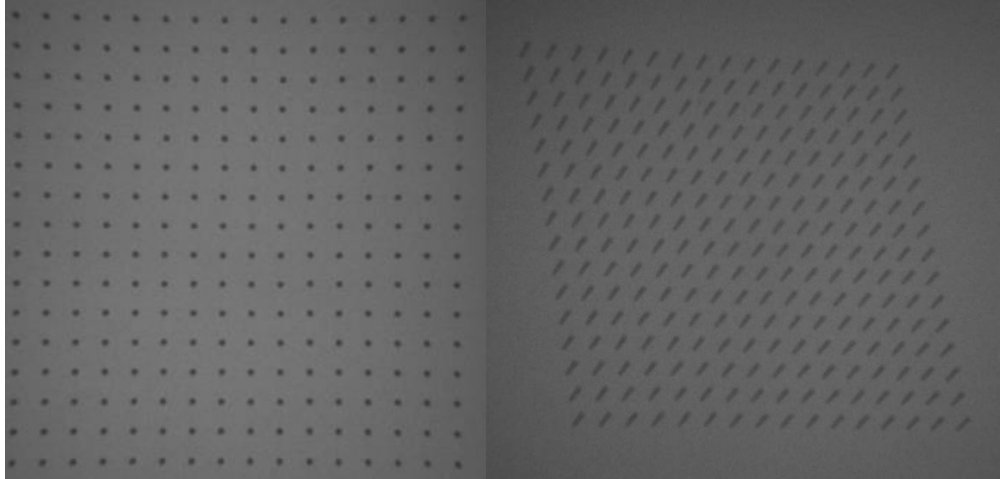
Figure 58: Top and 3D angular x-ray images of 30 μm paste filled TPVs in glass

5.4 Hybrid TPV for improved electrical performance

For low I/O count/low power applications like MEMS sensing electronics, the higher electrical resistivity of the copper paste (20-40 μohm-cm) as compared to bulk copper (1.7-2 μohm-cm) is not of great significance. However, for high speed and high bandwidth communication applications with signal data rates or carrier frequencies in the GHz range, it leads to significant performance degradation. This section addresses the high frequency performance challenges of paste filled TPVs in glass through preliminary evaluation of a hybrid TPV structure and validating the concept using ANSYS HFSS™ modeling.

A dual via chain structure illustrated in Figure 59 below was used to model the interfacial losses when a high frequency signal transitions from a planar transmission line to a through via.
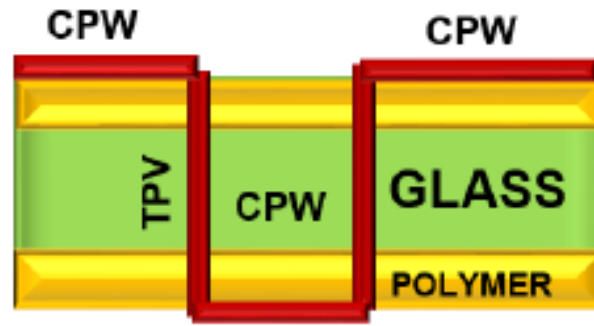
Figure 59: Dual-via chain structure

A simple 3D model, shown in Figure 60, originally built for modelling and design of TPVs for interposer applications was used to compare the performance of electroplated copper filled TPVs and copper paste filled TPVs.
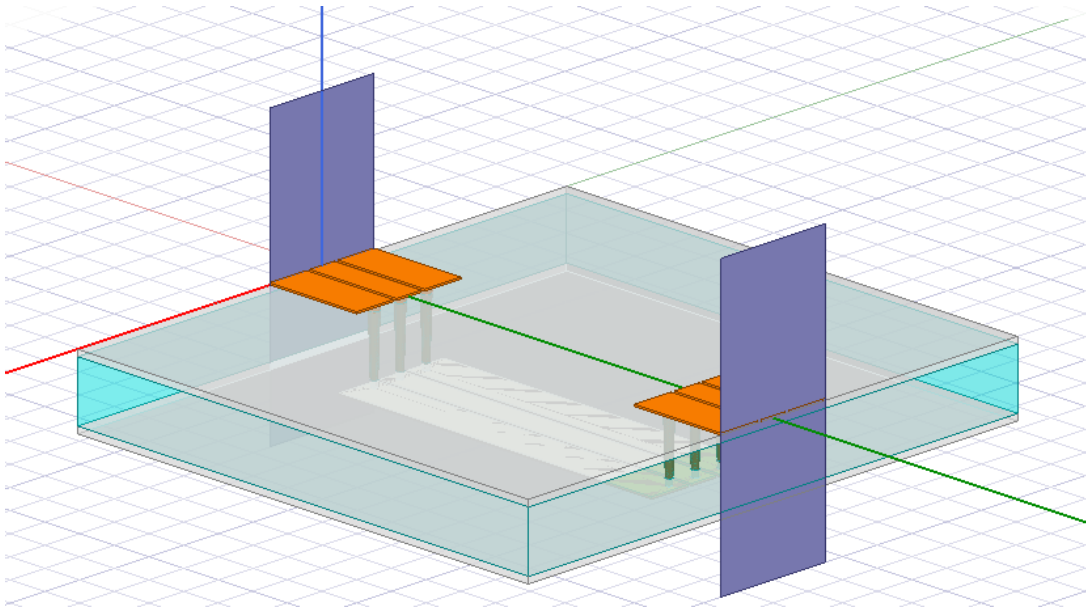
Figure 60: A dual-via chain model consisting of 2 sets of GSG vias and transmission lines

The model consisted of CPWG-CPWG (coplanar waveguide) structures enabled by two sets of GSG via transitions, shown in Figure 60 above. Model specifications are as shown in Table 13 below.

Table 13: Specifications of 3D model of dual via chain structure built in ANSYS HFSS^{TM}

Parameter	Value (μm)
Glass core thickness	300
TPV entry/exit diameter	55/34
Polymer thickness	33

Insertion loss (S_{21}) values at 20GHz were recorded for electroplated copper filled TPVs and Ormet paste filled TPVs and are shown in Table 14 below.

Table 14: Comparison of S$_{21}$ parameters at 20GHz for electroplated copper TPVs and copper paste TPVs in glass

Parameter	Electroplated Copper TPVs	Copper Paste TPVs	Performance gap
Insertion Loss S_{21} (dB) @ 20 GHz	-0.32	-0.41	28.125%
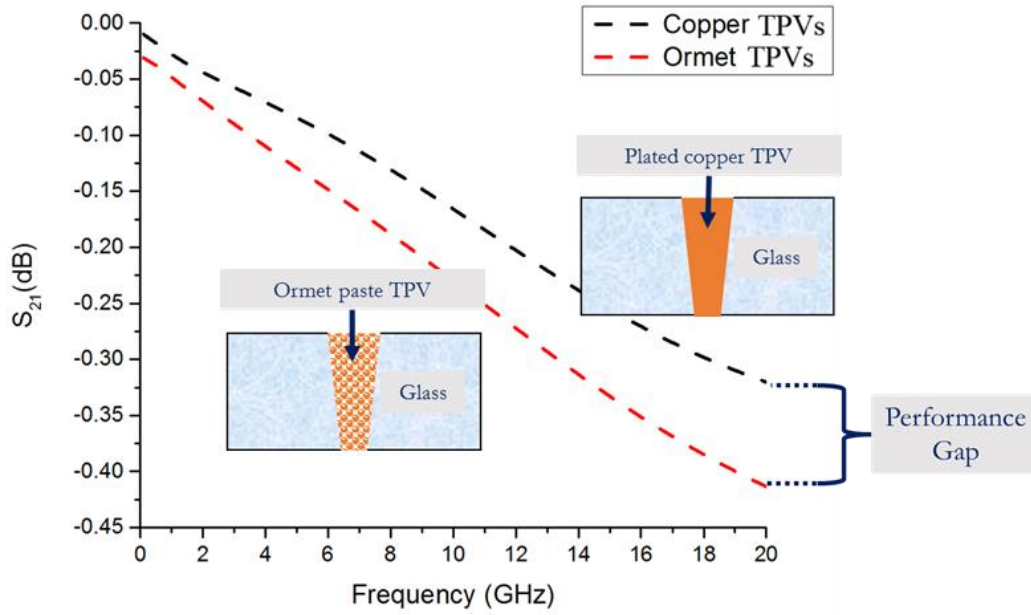
Figure 61: S_{21} plot showing performance gap between electroplated copper TPVs and copper paste TPVs in glass

As seen in Figure 61 above, there is a performance gap in the S_{21} parameter at 20 GHz between the two TPVs. To bridge this gap, a hybrid via structure was proposed, as shown in Figure 62 below.
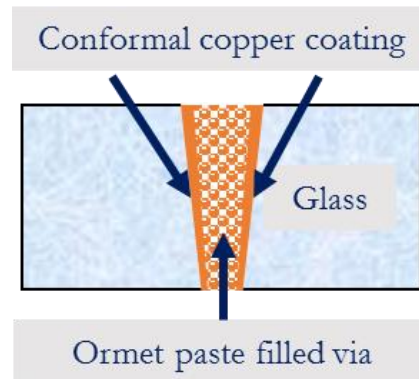
Figure 62: Concept image showing cross sectional view of hybrid TPV in glass

The hybrid via consists of a conformal coating of copper deposited along the TPV sidewalls by means of PVD/electroless plating processes as well as the copper paste to fill the via using the printing process described earlier. The hybrid TPV model was built in ANSYS HFSS^{TM} with a range of conformal copper coating thicknesses starting from 0.2 µm (typical thickness of copper seed layer in semi-additive processing for fabrication of traces) and the corresponding S_{21} values at 20 GHz were observed as shown in Table 15 below.

Table 15: Impact of conformal copper on S_{21} parameters of hybrid TPVs in glass

Parameter	Hybrid TPVs						
	0.2 µm	0.25 µm	0.5 µm	1 µm	1.5 µm	2µm	2.5 µm
Insertion Loss S_{21} (dB) @ 20 GHz	-0.41	-0.39	-0.33	-0.31	-0.31	-0.31	-0.3

As the conformal copper thickness was increased beyond 1 µm, the insertion loss asymptotes to a value of -0.3 dB which is comparable to that of copper TPVs. As shown in Figure 63 below, the performance of copper paste TPVs becomes comparable to that of copper TPVs over the same frequency range by introducing a conformal copper coating in the thickness range of 0.5 µm – 1.5 µm.
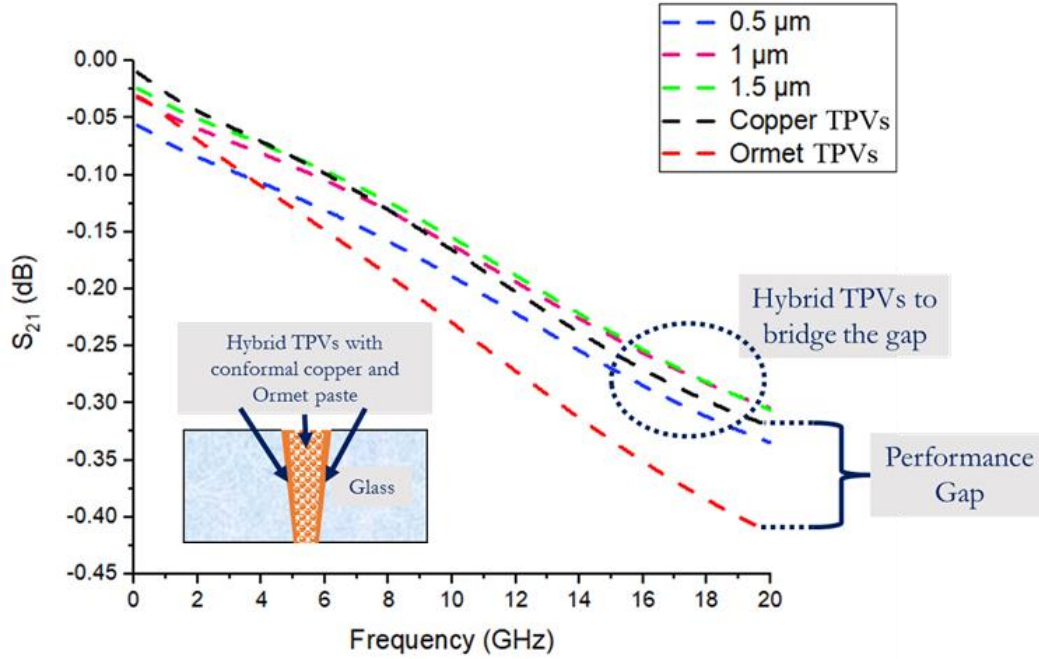
Figure 63: S$_{21}$ plot showing impact of conformal copper in hybrid TPVs to improve high frequency performance of paste filled TPVs

5.5 Summary

In this chapter, a high throughput and low temperature cured paste filled TPV metallization process was explored and demonstrated. The need for an alternatives to copper plating and high temperature sintering pastes was established followed by detailed discussion of Transient Liquid Phase Sintering pastes, the theory and mechanism of metallic mesh formation, material properties and its advantages. Next, the process to achieve paste filled TPVs was demonstrated using a simple, scalable, high throughput process with characterization of process yield using x-ray imaging. Finally, a hybrid TPV structure was evaluated and verified using preliminary electrical modeling using ANSYS HFSS^{TM} to provide design guidelines for future research. The process developed for TPV paste filling was extended to fill:

a) Large 100 µm diameter TPVs in 300 µm thick, 6-inch glass panels for a sensor glass cavity package (Figure 64)
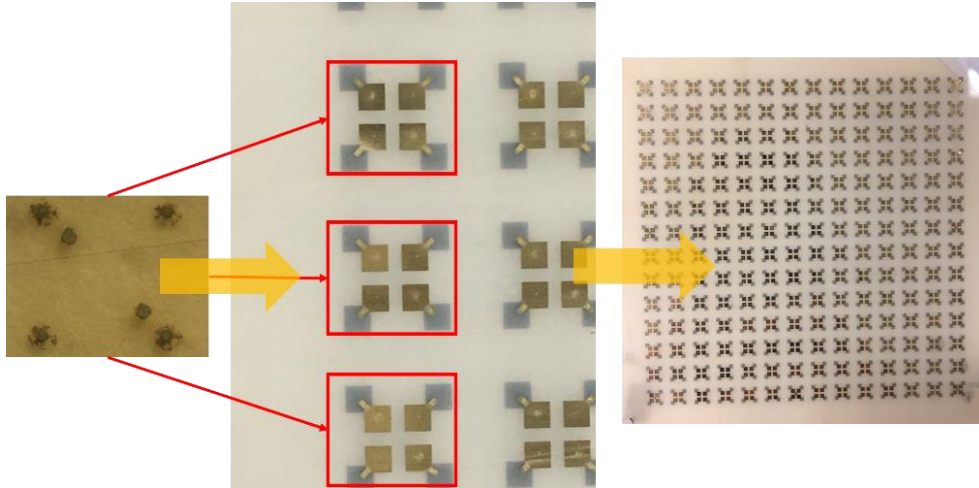
Figure 64: Test structures consisting of large paste filled TPVs in glass for sensor glass cavity package

b) Small 30 µm diameter TPVs in thin 130 µm thick 3-inch glass panels used for reliability test vehicles. These TPVs form daisy chain structures to study the thermomechanical reliability of paste filled TPVs in bare glass as shown in Figure 65, as part of future research.
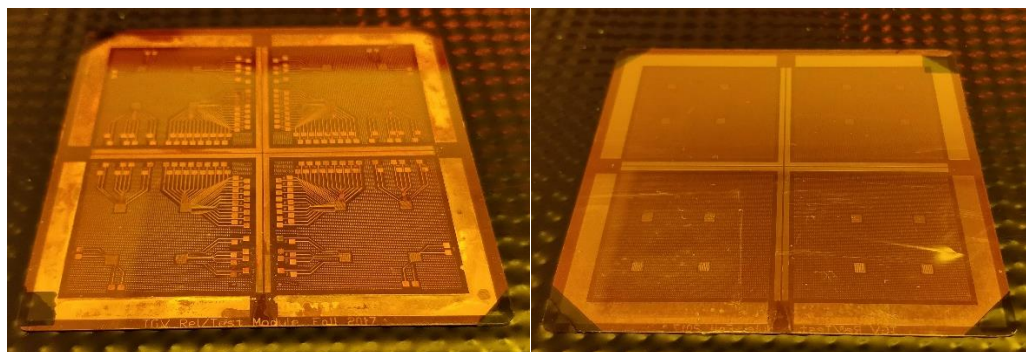
Figure 65: Test vehicle with daisy chain structures to study thermomechanical reliability of small paste filled TPVs in bare glass

CHAPTER 6

SUMMARY AND FUTURE WORK

This chapter summarizes the current trends and challenges in MEMS sensor packaging as well as the research tasks carried out to explore the following key technologies that enable an ultra-thin glass cavity MEMS package: a) reliable cavity formation in thin glass panels, (b) low stress glass-glass bonding and c) high throughput, fully filled through-package-via metallization in glass. Key contributions are highlighted and recommendations for future work related to this research are provided.

6.1 Summary

MEMS based sensing is gaining increased adoption in smartphones as well as the next generation Internet of Things (IoT) market. Such applications serve as primary drivers towards miniaturization for increased component density, multi-chip integration, lower cost and better reliability. State-of-the-art MEMS packaging techniques like silicon wafer level packaging and laminate/ceramic substrate packaging lag in terms of standardization, heterogeneous package integration and form factor miniaturization and take up the largest fraction of the total manufacturing cost. These limitations are a barrier against large scale adoption of MEMS devices. Therefore, advanced packaging of MEMS sensors for HPI plays a critical role not only in the shorter term by serving the needs of these nascent markets, but also for system scaling towards the System-on-Package (SOP) vision in the longer run.

This dissertation demonstrates a low stress, reliable, near-hermetic ultra-thin glass cavity MEMS packages as a solution that combines the advantages of silicon wafer level packaging, LTCC substrates and laminates while also addressing their limitations. This approach offers the potential of 2x reduction in form factor and the promise of higher integration capabilities at reduced costs. The following building block technologies were explored: (a) reliable cavity formation in thin glass panels (b) low stress glass-glass bonding, and (c) high throughput, fully filled through-package-via metallization in glass. Based on the objectives defined in Chapter 1, three main technical challenges were overcome to realize the objectives: (a) cavity corner cracking, side wall taper, side wall roughness and defects, (b) interfacial voids at glass-polymer-glass interface and (c) electrical opens and high frequency performance of copper paste filled through-package-vias in glass.

6.2 Reliable Cavity Formation in Thin Glass Panels

Three main design metrics were defined for glass cavities: a) side wall roughness for high reliability, b) side wall taper for RDL co-planarity and better electrical performance and c) surface roughness of cavity base for die pad-pad co-planarity and high assembly yield. Two types of cavity structures were explored: a) laminated glass cavities for excellent base surface smoothness, and b) blind cavities for easier integration of TPVs to enable 3D integration. These design metrics were optimized with the help of advanced, proprietary micromachining techniques from supply chain partners to achieve rounded cavity corners (100 µm corner diameter), smooth side walls, low taper (< 2 µm) and smooth cavity base surfaces.

6.3 Low Stress Glass-Glass Bonding

Two ultra-thin polymer adhesives: ABF GX-92 from Ajinomoto FineTech Co., Inc. and BCB from Dow Chemical Co. were used to achieve near-hermetic, low stress glass to glass bonding. Void reduction was achieved using two approaches: pressure assisted bonding and parametric variation for reduced surface roughness. Due to increased deformability of low-modulus polymers at elevated temperatures, pressure assisted bonding improved bonding efficiency to > 95% but did not eliminate voids. It is hypothesized that the shear components arising from higher pressures leads to localized non-coplanarity that generates voids. However, 100% bonding efficiency was achieved through variations in bonding conditions for reduced pre-cure surface roughness. Next, bond strength was characterized by die shear testing. The shear strength significantly exceeded the requirements of MIL-STD-883 method 2019.5 with an average shear strength of 17.29 MPa and 22.32 MPa for ABF and BCB bonded samples respectively. Finally, test samples were tested for bond reliability by subjecting them to 1000 thermal cycles between -55°C and 125°C. Shear strength was recorded at intervals to monitor bond quality degradation and it was observed that all ABF and BCB bonded samples survived 1000 cycles without failure.

6.4 High Throughput, Fully Filled Through-Package-Via Metallization in Glass

High throughput fully filled through-package-vias were achieved in ultra-thin glass using screen printed conductive copper paste cured at less than 200°C, as an alternative to copper electroplating. Via fill process parameters were optimized to demonstrate void-free

filling for small (30 μm) as well as large (100 μm) vias using conventional PCB hole filling tools as well as simple, scalable, lab based process using rudimentary tools including metal plates, vacuum suction pumps and Kapton tape. 100% yield was observed through x-ray imaging. Conductive paste filled vias show inferior high-frequency performance compared to electroplated copper filled vias. Therefore, a hybrid via structure with conformal coated copper in combination with copper paste was evaluated and via design rules were established using electromagnetic modeling (ANSYS HFSS^{TM}) targeting Cu-via like performance at high frequencies up to 20 GHz. Simulation results showed that the performance of copper paste filled through-package-vias in glass improves to closely match to that of electroplated copper through-package-vias in glass over the same frequency range by introducing a conformal copper coating of thickness 0.5 μm – 1.5 μm.

6.5 Key Contributions

This research presents the first set of advances in building block technologies that enable ultra-thin panel glass embedding of electronic components, with a focus on MEMS sensors. In particular, the following key engineering contributions are identified:

vi) Reliable, low defect, low taper cavity formation techniques in ultra-thin glass panels were explored, demonstrated and characterized.

vii) Panel glass-glass bonding was demonstrated using ultra-thin, low moduli dry film polymer adhesives with low interfacial stress, ultra-high shear strength values and 100% bonding efficiency.

viii)   Thermal cycling reliability of polymer adhesives based glass-glass bonding was demonstrated and shear strength degradation was monitored and characterized.

ix)   A novel, low temperature cured conductive copper paste was used to fill small (30 µm) and large (100 µm) through-package-vias in 130 µm and 300 µm thick glass panels for lower stress and higher throughput compared to electroplated copper through-package-vias in glass.

x)   A hybrid through-package-via structure comprising of conformal coated sidewalls with copper paste filled via was explored and modeled using ANSYS HFSS^{TM} to achieve copper-via like high frequency performance.

6.6 Recommendations for Future Work

This research, through reliable cavity formation processes, feasibility studies of panel glass bonding using ultra-thin polymer adhesives and process development of a novel through-package-via metallization technology, led to the demonstration of ultra-thin glass cavity MEMS package with fully filled through-package-vias that connect the embedded device to the external environment, as shown in Figure 66 below.
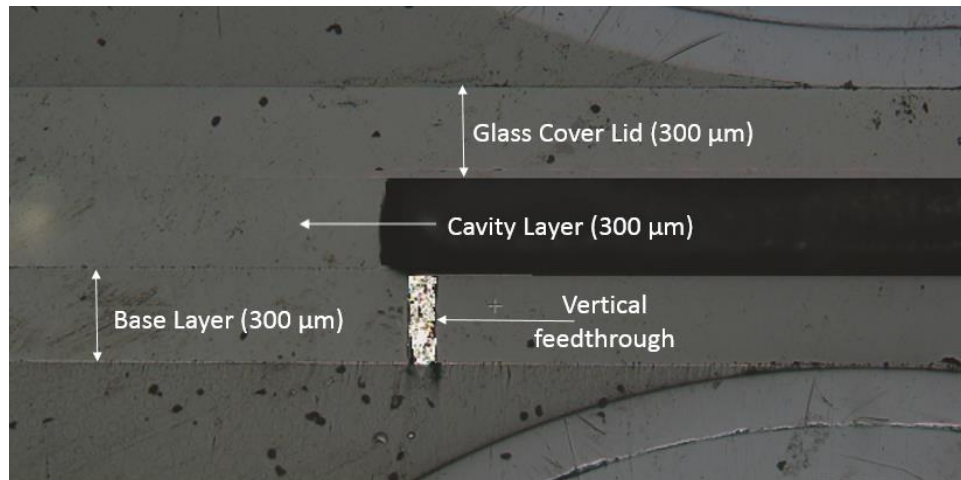
Figure 66: Cross sectional image showing glass cavity MEMS package with polymer-adhesive based glass-glass bonding and fully filled through-package-vias

The focus of the next stage of research in panel glass embedding is suggested below:

i)   Scaling down of ultra-thin glass cavity package form factors to < 300 µm and beyond.

ii)   A scalable method by which shear strength of large bonded areas can be characterized.

iii)   Hermeticity characterization of glass cavity packages in a helium leak rate detector using ultra-thin dry film polymer adhesive based panel glass bonding.

iv)   Process development of a low stress, ultra-thin metal-glass sealing technology and hermeticity characterization of the same.

v)   The feasibility of using ultra-thin dry film polymer adhesives as a die attach material needs to be explored by studying impact of assembly parameters and curing profile on die shift and die pad-pad co-planarity. These studies will contribute to development of chip-first panel glass embedded packages as described in chapter 3.

vi)   Electromigration tests, detailed studies of electrical and thermo-mechanical reliability of novel copper paste filled through-glass-vias

vii)   Detailed electrical modelling, design, fabrication and characterization of hybrid through-glass via structures described in chapter 5.

6.7 Journal and Conference Publications

i)   Buch, Chintan, et al. "Design and Demonstration of Highly Miniaturized, Low Cost Panel Level Glass Package for MEMS Sensors." Electronic Components and Technology Conference (ECTC), 2017 IEEE 67th. IEEE, 2017.

ii)   Buch, Chintan, et al. "Ultra-thin wireless power module with integration of wireless inductive link and supercapacitors." Electronic Components and Technology Conference (ECTC), 2016 IEEE 66th. IEEE, 2016.

iii)   Shi, Tailong, Buch, Chintan et al. "First demonstration of panel glass fan-out (GFO) packages for high I/O density and high frequency multi-chip integration." *Electronic Components and Technology Conference (ECTC), 2017 IEEE 67th*. IEEE, 2017.

iv)   Struk, Daniel, Buch, Chintan et al. "Thermal and Mechanical Analysis of 3D Glass Packaging for Automotive Cameras." Electronic Components and Technology Conference (ECTC), 2017 IEEE 67th. IEEE, 2017.

v)   Buch, Chintan, Sundaram Venkatesh et al "Advances in panel glass embedding for low stress, near hermetic reliability of MEMS towards heterogeneous package integration (HPI)" *To be submitted*

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