

# Development of High Performance Interfill Materials for System Chips Technology

Jiali Wu, Swapan Bhattacharya, Courtney Lloyd, C. P. Wong, *Fellow, IEEE*, H. Bernhard Pogge, and Rao R. Tummala, *Fellow, IEEE*

**Abstract**—An innovative precisely interconnected chip (PIC) technology is currently under development at IBM to seek more effective means of creating system chips. The objective of this research is developing fabrication methods to permit the realization of high yielding large area chips, as well as chips that may contain very diverse technologies. This paper reports the use of a high-performance interfill material based on epoxy resin, which is used to connect the different chip sector macros that make up the system chip. This novel interfill material remains thermally stable through the subsequent processing temperature hierarchies during the interchip interconnection fabrication. Spherical SiO<sub>2</sub> powders are incorporated into the epoxy resin to improve its mechanical properties, reduce coefficient of thermal expansion, and increase thermal conductivity. Adhesion and rheology of the formulated interfill materials are evaluated. Microstructure of SiO<sub>2</sub> filled epoxy system is also investigated to confirm the reliability of the composite before and after thermal aging. Initial results indicate that the formulated EPOXY A resin composite is qualified for the system chip manufacturing process in terms of the dispensing processability, structural and mechanical integrity, and reliability.

**Index Terms**—Interfill material, microstructure, rheology, system chips, thermal stability.

## I. INTRODUCTION

WITH ever-faster clock rates, the propagation delays between chips constitute a significant portion of the clock cycle. It is expected that mounting both active and passive devices in close proximity will boost the system performance. An approach referred to as embedded technology with chip-first or chip-last processing can realize the direct interconnection between active and passive components without soldering or wire bonding [1]–[6]. The active and passive components are embedded on silicon substrates to achieve a common planar surface. The interconnection is realized using thin-film technology on the planar chip/substrate surface. The major advantages of such configuration are the short interconnection lengths between chip and the substrate, no chip bumping preparation, planar topography, high integration density, and low interfacial thermal resistance. Additionally, all transmission lines on the

substrate and from the substrate to the active or passive components can be realized with controlled impedance for high frequency applications. Therefore, this embedded technology provides the possibility of employing a three-dimensional (3-D) stacking—the highest package density, which tends to be the core technique for the system on chip (SOC) technology for the next generation of electronic packaging.

An innovative precisely interconnected chips (PIC) technology developed by IBM attempts to simplify the embedded technology further by minimizing feature size and reducing manufacturing cost. Based on this innovation, active and passive components are placed facedown onto predetermined sites on ceramic or Si substrates that are used as guide carriers. The gaps formed between functional chips can vary in a range from 50 to 300  $\mu\text{m}$  and are to be filled with a suitable high performance and low shrinkage interfill material. A surface with good planarity is achieved by chemical and mechanical polishing. An intermediate manufacturing step is the assembly of a sandwich of the chip tops (the other side attached to the guide carrier) attached to a ceramic or silicon supporter plate. The supporter plate is sized to serve as a thermal spreader. After the supporter plate is attached, the guide carrier is removed. A multilayer thin-film process is subsequently used for interconnection. In the course of system fabrication, a kind of polymeric composite is required to freeze the active and passive components in place. This composite is expected to hold the chips in their predetermined positions as accurately as possible for the subsequent photolithography. High temperature stability of the candidate composite is another key requirement to ensure the system's reliability during the high density interconnection (HDI) processes, such as dielectric cure, thin film metallization, and laser-drilled via formation. The interfill material also has to meet the requirements such as low shrinkage, high modulus, low viscosity, good wetting, thermal conductivity and adhesion to the substrates.

Based on these challenging requirements, fourteen different formulations of thermoset polymers were selected for the initial evaluation. They were obtained either from commercial markets or home-made formulations. In-house formulated interfill materials are epoxy based polymers, including high temperature adhesives EPCO, EPCU (with low viscosities), HTAI, and HTA2 [7], [8]. Commercially available materials evaluated in this project are listed in Table I.

## II. EXPERIMENT

Most of these fourteen candidates failed for either high volume shrinkage or poor thermal stability. However, only

Manuscript received December 1, 2001; revised January 7, 2002. This work was supported by IBM. This work was recommended for publication by Associate Editor D. N. Donahoe upon evaluation of the reviewers' comments.

J. Wu, S. Bhattacharya, C. Lloyd, C. P. Wong, and R. R. Tummala are with the School of Materials Science and Engineering, Packaging Research Center, Georgia Institute of Technology, Atlanta, GA 30332-0560 USA (e-mail: cp.wong@mse.gatech.edu).

H. B. Pogge is with the IBM Microelectronics, Hopewell Junction, NY 12533 USA.

Publisher Item Identifier S 1521-3331(02)02319-X.

TABLE I  
COMMERCIALY AVAILABLE AND HOME-MADE INTERFILL MATERIAL  
CANDIDATES

Sample ID	Supplier	Components
A	Epoxy Technology	Epoxy resin
B	Epoxy Technology	Epoxy resin
C	Hitachi Chemical	Carbon black filled epoxy
D	Ablestick Electronics	Low stress epoxy
E	Ablestick Electronics	Low stress epoxy
F	Hitachi Chemical	Silicone modified polyimide-amide, 28% NMP
G	Sumitomo Chemical	Polyimide-amide, 20% DMSO, 68% NMP
H	Sumitomo Chemical	Polyimide-amide, 89% NMP
I	BF Goodrich	Polynorborene, 77% Mysitylene
EPCU	House-made	Epoxy resin
EPCO	House-made	Epoxy resin
HTA1	House-made	Epoxy resin
HTA2	House-made	Epoxy resin

EPOXY A (from Epoxy Technology, Inc.) with different SiO<sub>2</sub> filler loading was characterized using differential scanning calorimeter (DSC), thermogravimetric analyzer (TGA), dynamic mechanical analyzer (DMA), thermal mechanical analyzer (TMA), Rheometer, thermal conductivity analyzer (TCA), die shear tester, and scanning electron microscope (SEM). Results based on the above mentioned studies are discussed in this paper.

#### A. Sample Preparation

Candidate interfill materials reported in this paper include the following. Epoxy A, B (Epo-Tek, epoxy base, two components, part A:part B = 10:1), HTA1, HTA2, EPCO, EPCU (Home-made, epoxy base, low viscosity). LE-03 SiO<sub>2</sub> (JCI USA Inc.) powder with average diameter of 3–4 μm was selected as filler to reduce coefficient of thermal expansion and increase thermal stability of the candidate polymer resins. Specified amounts of SiO<sub>2</sub> were blended (Blender, Model 22 305A, Warning Products Division, Dynamic Corporation America) with candidate epoxy resins with stirring rate from 0 to 15 000 rpm at the beginning, hold at that rate for 20 s, then turned down. This step was repeated five times. The blended samples were degassed in a vacuum oven for 60 min under –711.2 mm (–28 in) Hg gage pressure. All prepared samples were stored in freezer at –40 °C. Curing temperature for EPOXY A, HTA1 and HTA2 was 150 °C for 60 min, for EPCU and EPCO was 250 °C for 30 min.

#### B. Thermal Property Evaluation

Thermal stability of the candidate interfill materials was evaluated by thermal scanning analysis and isothermal analysis using a thermal gravimetric analyzer (TGA), Model 2940 from TA Instruments. Temperature for thermal scanning analysis ranged from 25 °C to 400 °C at a heating rate of 5 °C/min in a nitrogen atmosphere. For the isothermal analysis, the temperature of sample was raised to 350 °C with a heating rate of 5 °C/min, then held at 350 °C for 2 h, and the whole experiment proceeded under nitrogen protection. Sample size for the TGA

test is about 20 mg. Sample shape was also controlled, since the sample preparation was done by putting an approximately equal amount of liquid epoxies into an aluminum pan with a diameter of 6 mm. Therefore, the deviation due to the area of sample exposed to the atmosphere can be ignored.

#### C. Rheology Study

Rheometer model AR 1000N (TA Instruments) was used for viscosity test. A flow experiment mode was selected to measure the viscosity of the samples changed with shear rate. Geometry of the shear head is a pair of 4 cm diameter parallel stainless steel plates with a gap of 80 μm in between. Shear rate was ramped from 0.2 to 20 m/s · m with a deviation of 5% at 25 °C. For the viscosity versus temperature test, a flow experiment mode was selected and the geometry is a pair of 2 cm diameter parallel plates with a gap of 80 μm in between. The measurement was done under shear rate control with a temperature range of 40 to 80 °C and a shear rate of 1 m/s · m.

#### D. Mechanical Property Characterization

Dynamic moduli of the interfill materials were measured using a dynamic mechanical analyzer (DMA), Model 2980 from TA Instruments. The specimen for DMA testing were prepared by placing the filler contained and degassed liquid candidate materials into an 1.5" diameter aluminum pan, and then cured according to the *mentioned* procedures in a convection oven. After curing, samples were peeled out from aluminum pans and diced into strips (about 32 × 11 × 2 mm) using a diamond saw. DMA test was conducted in a single cantilever mode under 1 Hz sinusoidal strain loading, and the test temperature was raised from 30 to 250 °C at a heating rate of 3 °C/min. Storage modulus  $G'$ , loss modulus  $G''$ , and loss angle  $\tan \delta$  of a sample were obtained from a *single* experiment.

Coefficient of thermal expansion (CTE) of the candidate interfill materials was determined by using thermal mechanical analyzer (TMA), Model 2940 from TA Instruments. The specimen preparation was the same as that for DMA testing, but the size was about 5 × 5 × 2 mm. Testing temperature ranged from room temperature to 180 °C at a heating rate of 3 °C/min in a nitrogen atmosphere.

Adhesion between interfill materials and adherents (Si substrate) was also tested. 2 × 2 mm (80 × 80 mil) dies were directly attached to the 25.4 × 25.4 mm (1 × 1 in) Si substrate using interfill material as adhesives. Adhesion test was performed with an adhesion analyzer (Royce Instruments System 552) at room temperature before and after thermal aging at 350 °C for 2 h. During the test, shear speed was controlled at 0.1 mm/s (0.004 in/s) with a vertical offset of 49 μm (0.002 in).

#### E. Thermal Conductivity Evaluation

A thermal conductivity analyzer (Holometrix C-MATIC, Model TCA-200, Guarded Heat Flow Meter, from Holometrix Inc. was used for measuring the thermal conductivity of *candidate* materials by the guarded heat flow meter method. A test sample was placed between two plates controlled at different temperatures, resulting in a flux of heat running through the

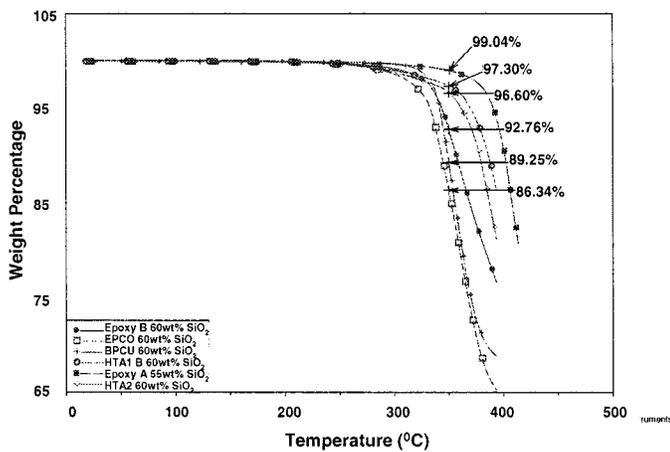


Fig. 1. Thermal gravimetric analysis on the interfill candidates (heating rate = 5 °C/min).

tested material from the hotter plate side to colder plate side. The amount of heat flow was measured with a thin heat flux transducer attached to one of the temperature-controlled plates. Sample preparation was the same as that for DMA test, but sample size was 25.4 × 25.4 × 1.0 mm, and the two sides of the sample must be parallel to guarantee the intimate contact to both plates of upper thermal sink and lower thermal heater. During the test, low thermal conductivity materials (foaming springe, Dow Corning 340 silicone heat sink compound) were used as thermal insulators to prevent heat flow going out through the surrounding cylinder wall.

#### F. Reliability Analysis

Interfill materials were dispensed into 200 μm wide and 400 μm deep grooves Cu on Si substrates using a automated dispenser Model 403 from Asymtek. After curing, the filled substrates were mounted in a epoxy mold for a cross-sectional specimen preparation. Dispensing quality was observed with SEM.

Microstructural variations of samples before and after thermal aging at 350 °C for 2 h in a nitrogen oven were studied with a scanning electron microscope (SEM), Model S-800 from Hitachi. Both fine polished samples and fractured samples were gold sputtered for 5 min before SEM analysis.

### III. RESULTS AND DISCUSSION

#### A. Interfill Materials Screening

Adding SiO<sub>2</sub> filler into polymer resin is a common way to increase the thermal stability and mechanical property of polymer resin itself. In this study, thermal stability comparison on the candidate interfill materials was conducted on the SiO<sub>2</sub> filled samples. The results could ignore the discrepancy due to the incompatibility of SiO<sub>2</sub> filler and polymer matrix. Fig. 1 shows a change in weight remainder of the potential interfill materials versus temperature scanning from 25 to 400 °C at a heating rate of 5 °C/min. EPOXY A with 55% SiO<sub>2</sub> shows the best thermal stability with 99.04% weight remainder at 350 °C. HTA1 with 60% SiO<sub>2</sub> shows the second best thermal stability with 97.3% weight remainder. The Results of isothermal stability analysis on these candidate interfill materials are illustrated in Fig. 2.

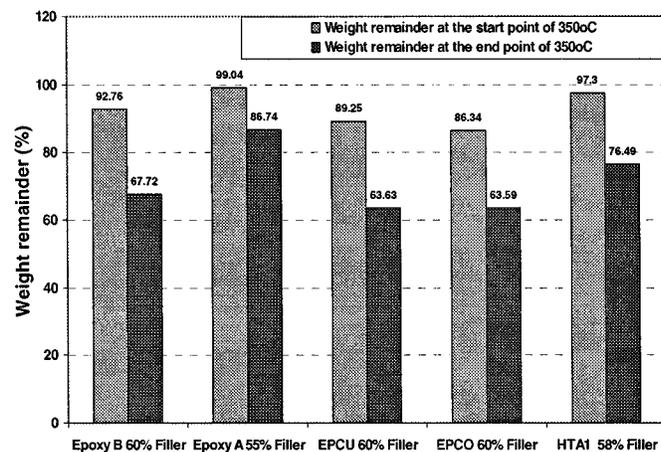


Fig. 2. Isothermal stability comparison on the interfill candidates (isothermal at 350 °C for 2 h).

EPOXY A with 55% SiO<sub>2</sub> shows the highest weight remainder for isothermal test at 350 °C for 2 h, and the difference between the starting and ending points of isothermal temperature also shows the smallest weight loss, i.e., EPOXY A with 55% SiO<sub>2</sub> has the best performance during isothermal test at 350 °C for 2 h. HTA1 ranks the second in isothermal stability.

#### B. Mechanical Property Characterization

Mechanical properties of the interfill material play an important role for the reliability of system chips. In general, storage modulus ( $G'$ ), loss modulus ( $G''$ ), and  $\tan \delta$  ( $\tan \delta = G''/G'$ ) [7] are the key parameters that affect the material's stiffness, energy dissipation and damping property. Coefficient of thermal expansion (CTE) is associated to system chips' structural stress due to the thermal mismatch between interfill materials and relative adherents [8], [9]. Adhesion between interfill materials and Si substrates acts as a critical factor to the interfacial behavior during swift temperature increasing or decreasing. Generally, a 50 MPa shear strength is considered as the lowest adhesion margin for qualified MCM systems [10].

DMA was used to measure the modulus change of materials with temperature. Fig. 3 illustrates the storage modulus, loss modulus,  $\tan \delta$  of EPOXY A with 50% SiO<sub>2</sub> changed with temperatures. With temperature increases, storage modulus of the sample first gradually decreases, dramatically decreases when the temperature reaches glass transition point, and finally falls down to almost less than 10 MPa due to the complete softening of the epoxy structure. Fig. 4 is a summary of storage moduli, loss moduli,  $\tan \delta$ , and  $T_g$  changed with SiO<sub>2</sub> filler loading percent in EPOXY A epoxy matrix at room temperature. As the filler loading percent increases, storage modulus, loss modulus and glass transition temperature increases, but  $\tan \delta$  decreases slightly. This trend indicates that the stiffness and damping property of the material increase with filler loading percent at room temperature. The toughness of the material remains almost constant. The temperature point (related to  $T_g$ ) of initial movement of large polymer segment increases with the increase of filler loading percent, because the existence of filler acts as an inhibitor to the mobility of polymer segments.

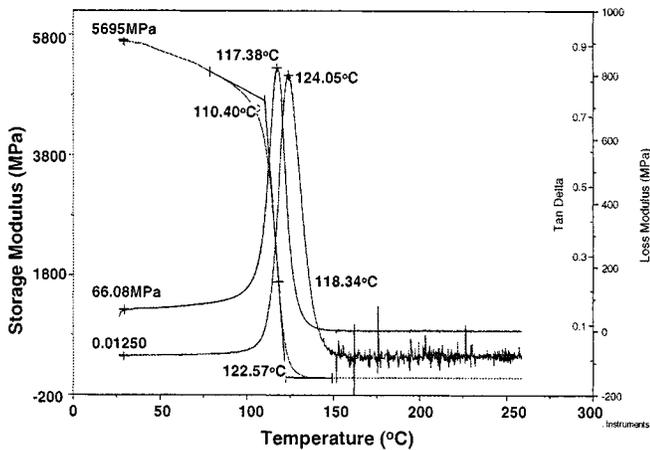


Fig. 3. Storage modulus, loss modulus and  $\tan \delta$  of Epoxy A with 50%  $\text{SiO}_2$  versus temperature.

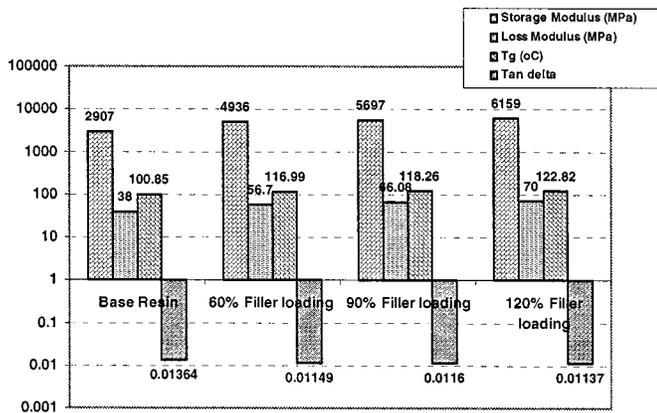


Fig. 4. Comparison on storage moduli, loss moduli  $\tan \delta$  and  $T_g$  of Epoxy A series.

CTE is another essential parameter to evaluate the mechanical property of interfill materials. For the purpose of reducing the CTE of polymers, high percent of filler loading had been applied to the EPOXY A matrix. The  $\text{SiO}_2$  fillers are amorphous silica spheres with an average diameter of 3–4  $\mu\text{m}$ . The relation between CTE and filler loading percent is shown in Fig. 5. CTE shrinks quickly at low filler loading percent compared to the pure EPOXY A resin, then the reduce trend slows down with the increase of filler loading percent. As  $\text{SiO}_2$  filler loading percent varied from 0 to 55%, CTE's below  $T_g$  decreased from 62.8 to 35.3 ppm, CTE's above  $T_g$  decrease from 243 to 112 ppm.

Adhesion change before and after thermal aging at 350°C for 2 h was evaluated with EPOXY A with 55%  $\text{SiO}_2$  used as adhesive between Si substrates. The adhesion from shear test decreases from the starting 77.42 MPa to 58.02 MPa after thermal aging, approximately 20% difference. But it is still above the strength limitation of 50 MPa. The die shear fracture mode observed through microscope could somehow explain what happened to the material during the thermal aging. Fracture surface of die sheared sample showed a mix-mode failure before aging, while it showed an adhesive failure after 350 °C for 2 h aging. This may be caused by the CTE's mismatch between Si substrate and epoxy, which produced residual stress after the

sample cooled down from 350 °C and resulted in the delamination easily propagating at the weakest interface. In addition, outgassing may also affect the interfacial adhesion and cohesion of polymer composite itself.

### C. Rheology Study

Rheological property of the interfill materials is directly related to the processing feasibility. In general, viscosity is referred to as an internal resistance to the movement of molecules and often used to evaluate the fluidity of liquids or pastes.

In this study, the viscosities of EPOXY A series with various filler loading percents were tested over time and temperature. The initial viscosities of EPOXY A series were tested with shear rate changed from 0.2 to 20  $\text{m/s} \cdot \text{m}$  right after samples were prepared at 25 °C. The samples were stored in freezer at –40 °C. The same batch samples were taken out 24 h later and warmed up to room temperature, and re-tested. After the test, all the samples were stored into the freezer for another 24 h, and repeated the former steps. The whole measurement lasted 72 h. Fig. 6 shows the average viscosity and shear stress of EPOXY A with 55%  $\text{SiO}_2$  changed with storage time within the shear rate range from 0.2–20  $\text{m/s} \cdot \text{m}$ . Viscosity dramatically increased with storage time. Shear stress at the same shear and storage time also increased correspondingly. The viscosity change indicates that the pot life of Epoxy A composite greatly depends on its viscosity change and manufacture processing feasibility.

Correlation between viscosity and filler loading percent and storage time are illustrated in Fig. 7. The trend of viscosity against time and filler loading percent is very obvious. It can be intuitively observed that the rate of change in viscosity accelerated over each 24 h period, which was mainly due to the auto-catalyzed polymerization between part A and part B of EPOXY A once they were put together. It appears that after the first 24 h, viscosity data of the samples begin to separate into three groups. The EPOXY A with 65%  $\text{SiO}_2$  and 60%  $\text{SiO}_2$  samples have the highest level viscosities. Next, the EPOXY A with 55%  $\text{SiO}_2$ , 50%  $\text{SiO}_2$ , and 45%  $\text{SiO}_2$  samples have viscosities less than the first group, but not the lowest. And the EPOXY A with 40%  $\text{SiO}_2$ , 30%  $\text{SiO}_2$ , and 0%  $\text{SiO}_2$  samples have the lowest level of viscosities. After 72 h storage time, the viscosities of all the samples were from 75 times to 300 times of their original viscosities. However, the EPOXY A resin was not fully cured at this time as its major molecules are dimers, trimers, or oligomers. Once the samples were heated to certain high temperature, the dimers, trimers, or oligomers would absorb some energy to freely move around and approach enough low viscosity for dispensing operation.

### D. Thermal Conductivity Evaluation

Thermal conductivity is defined that the amount of heat flux diffused through the unit cubic material with a unit temperature differential between both sides of the sample. With semiconductor feature size deep down to submicron, heat dissipation from IC device becomes one of the pressing issues of the electronics packaging. Thermal conductivity of epoxy resin itself is pretty low. Filler loading is a common way to improve the thermal conductivity of polymer base.  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , BN, AlN

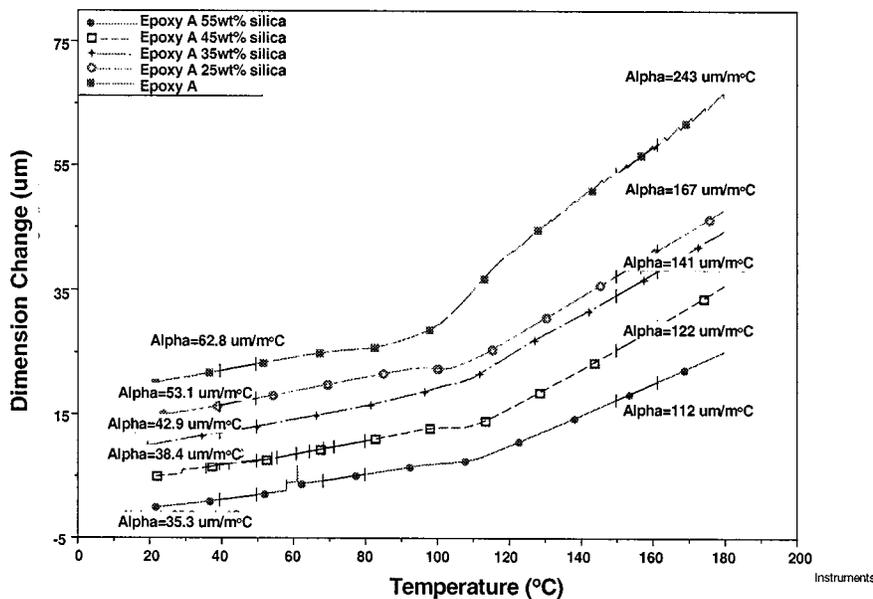


Fig. 5. TCE's of Epoxy A series changed with silica filler loading percents.

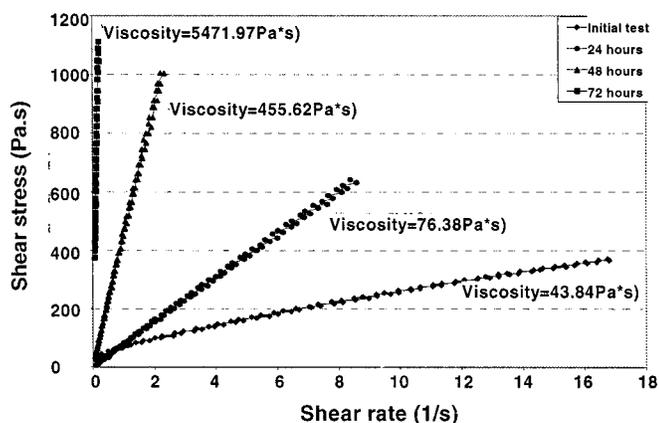


Fig. 6. Viscosity and shear stress of Epoxy A with 120% SiO<sub>2</sub> versus shear rate over 72 h storage period.

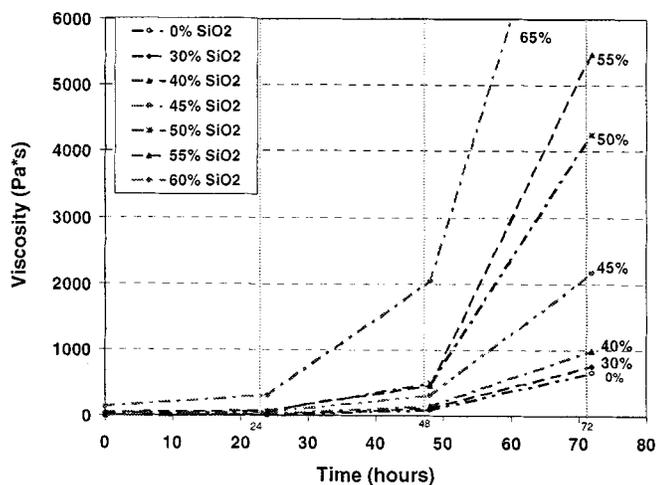


Fig. 7. Viscosity versus storage time and SiO<sub>2</sub> filler loading percentage.

and SCAN (silica coated AlN) spherical or flaky powders with various sizes are often used for that purpose. Although BN, AlN

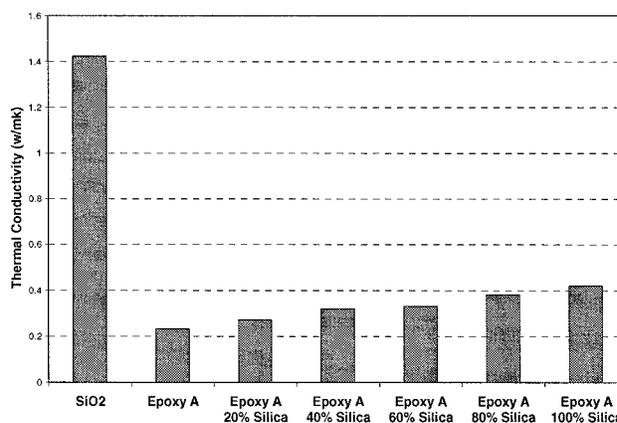


Fig. 8. Thermal conductivity versus SiO<sub>2</sub> filler loading percentage on Epoxy A base.

and SCAN have higher thermal conductivity compared to the other two fillers, they will greatly increase the viscosity of the filled polymer system even with lower loading percentage [11]. Flexibility of filler size of these three powders is also limited and high manufacture cost is another disadvantage. In this study, we selected spherical SiO<sub>2</sub> with average size of 3–4 μm as fillers to improve the thermal conductivity of the EPOXY A composite as well as CTE. Fig. 8 shows the thermal conductivity values of EPOXY A series with different percent filler loading tested around an average temperature of 75 °C. Thermal conductivity of EPOXY A series shows a good linear relation to the filler loading percent. Thermal conductivity of EPOXY A with 60% SiO<sub>2</sub> is 43.5% higher than that of base EPOXY A.

### E. Reliability

TGA test provides the information of material's thermal stability changed with temperature in nitrogen atmosphere. While optical microscope and SEM can intuitively display the material's interfill quality and intrinsic change of microstructure occurred before and after thermal aging. Fig. 9 illustrates the im-

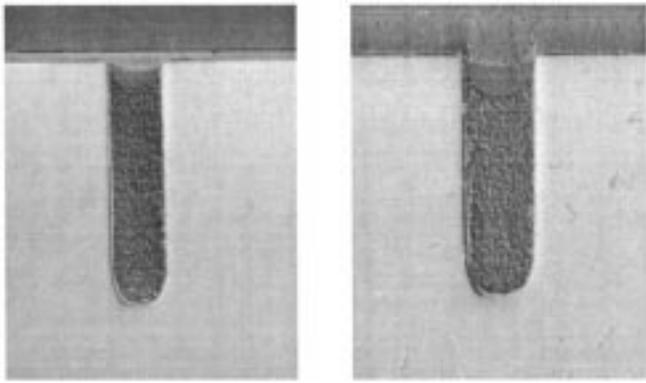


Fig. 9. Cross section images of filled trenches with  $400\ \mu\text{m}$  depth and  $200\ \mu\text{m}$  width (samples cured at  $150\ ^\circ\text{C}$  for 60 mins, filler 45% silica).

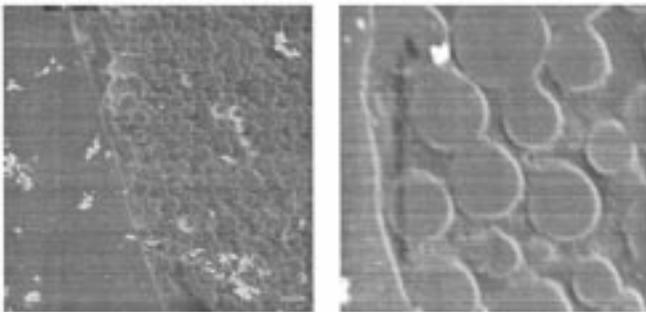


Fig. 10. SEM cross section images on a well-polished sample with interfill material filled in the trench after thermal aging at  $350\ ^\circ\text{C}$  for 2 h (epoxy A with 45% silica filler loading).

ages of cross section cut from dummy substrates with  $200\ \mu\text{m}$  width and  $400\ \mu\text{m}$  depth trench filled by EPOXY A with 55%  $\text{SiO}_2$ . Fig. 9(a) is a  $90^\circ$  cutting and Fig. 9(b) is a  $45^\circ$  cutting, but both from the same specimen. Materials filled the trench pretty well. Good fill indicates the EPOXY A with 55%  $\text{SiO}_2$  has a good wetting on the Si of the trench side-wall. SEM high magnification images were shown in Fig. 10(a) and (b) after specimen exposed to  $350\ ^\circ\text{C}$  for 2 h. Interfaces show a good contact between EPOXY A matrix and Si substrate without any defects appearing and fillers homogeneously distributed in the EPOXY A. High magnification image of Fig. 10(b) displays that the  $\text{SiO}_2$  filler was structurally encompassed by EPOXY A matrix. No fatal cavities appeared inside the polymer matrix. In addition, a further morphology study was done on the topographies of fractured specimens of EPOXY A with 45%  $\text{SiO}_2$ .

#### IV. CONCLUSION

EPOXY A based interfill materials, selected from fourteen candidates, can meet the thermal stability requirement according to the manufacture process. High percent  $\text{SiO}_2$  loading can greatly increase the stiffness of the EPOXY A composite system and provide a storage modulus on the order of GPa.  $T_g$ s were increased from  $105$  to  $115\ ^\circ\text{C}$  and CTE was reduced to 35 ppm with filler loading percent increases from 0 to 55%. Viscosity changed with storage time and filler loading percent accordingly. Adhesion of the specimen still remains reliable value after  $350^\circ\text{C}$  for 2 h. Results from optical microscope

and SEM analysis indicates that EPOXY A itself can keep thermally stable at  $350\ ^\circ\text{C}$  for 2 h and higher filler loading benefits thermal stability improvement as well as mechanical properties enhancement.

#### REFERENCES

- [1] R. Fillion, R. Wojnarowski, T. Gorczyca, E. Wildi, and H. Cole, "Plastic encapsulated MCM technology for high volume, low cost electronics," *Circuit World*, vol. 21, p. 28, 1995.
- [2] J. Wolf, F. J. Schmuckle, W. Heinrich, M. Topper, K. Buschick, A. Owzar, O. Ehrmann, and H. Reichl, "System integration for high frequency applications," *Int. J. Microcirc. Electron. Packag.*, 2002.
- [3] M. Topper, J. Wolf, V. Glaw, K. Buschick, A. Dabek, L. Dietrich, O. Ehrmann, and H. Reichl, "Embedding technology—A chip-first approach using BCB," in *Proc. Int. Symp. Adv. Packag. Mater.*, 1997.
- [4] —, "MCM-D with embedded active and passive components," in *Proc. ISHM'96 Conf.*, 1996.
- [5] J. T. Butler, V. M. Bright, and H. Comtois, "Advanced multichip module packaging of microelectromechanical system," in *Proc. Int. Conf. Solid-State Sensors Actuators*, Chicago, IL, 1997, p. 261.
- [6] R. Boudreau, P. Zhou, and T. Bowen, "Wafer scale photonic-die attachment," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 21, p. 36, Feb. 1998.
- [7] I. M. Ward and D. W. Hadley, *An Introduction to the Mechanical Properties of Solid Polymers*. New York: Wiley, 2001.
- [8] E. Suhir, "Calculated thermally induced stresses in adhesively bonded and soldered assemblies," in *Proc. 1986 Int. Symp. Microelectron.*, 1986, pp. 383–392.
- [9] S. P. Timoshenko, "Analysis of Bi-metal thermostats," *J. Opt. Soc. Amer.*, vol. 23, pp. 233–255, 1925.
- [10] M. Edwards, "Some factors that affect performance of capillary flip chip underfills," in *Proc. Int. Symp. Adv. Packag. Mater.*, 1998, p. 21.
- [11] C. P. Wong and R. S. Bollampally, "Mixed filler combinations for enhanced thermal conductivity of liquid encapsulations for electronic packaging," in *Proc. 1999 Int. Symp. Advanc. Packag. Mater.*, 1999, p. 113.

**Jiali Wu** received the B.S. degree from Zhejiang University, China, and the M.S. and Ph.D. degrees from the Shanghai Institute of Metallurgy, Chinese Academy of Sciences, Shanghai, all in chemistry.

From 1991 to 1997, her major research work focused on microsensor fabrication and application in the electrochemistry field and die bonding with Au/In bi-alloy isothermal solidification technique. She has been with the Electronics Packaging Research Group as a Postdoctoral Fellow in the School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, since 1997. She is currently working on polymer development for the application of various electronics packaging, mainly including multilayer conformal coatings for reliability without hermeticity encapsulation, reworkable high temperature adhesives for advanced MCM-D processing, underfills, and parylene interfacial adhesion enhancement on low- $K$  polymer passivated substrates.

**Swapan Bhattacharya** received the M. S. and Ph.D. degrees from the Indian Institute of Technology, Kharagpur.

He is a Senior Research Scientist at the Packaging Research Center, Georgia Institute of Technology (Georgia Tech), Atlanta. His primary research interests are integral passives and low-cost large area packaging in HDI substrates. Prior to joining Georgia Tech in 1996, he was with Systran Corporation, American Cyanamid Company, and Amoco Corporation. He has published 40 journal papers and edited a book on polymer composites.

**Courtney Lloyd**, photograph and biography not available at the time of publication.



**C. P. Wong** (SM'87–F'92) received the B.S. degree in chemistry from Purdue University, West Lafayette, IN, and the Ph.D. degree in organic/inorganic chemistry from Pennsylvania State University, University Park.

After his doctoral study, he was awarded two years as a Postdoctoral Scholar at Stanford University, Stanford, CA. He joined AT&T Bell Laboratories, in 1977 as Member of Technical Staff. He was elected an AT&T Bell Laboratories Fellow in 1992. He is a Regents Professor with the School of Materials

Science and Engineering and a Research Director at the NSF-funded Packaging Research Center, Georgia Institute of Technology, Atlanta. He holds over 40 U.S. patents, numerous international patents, has published over 400 technical papers and 300 key-notes and presentations in the related area. His research interests lie in the fields of polymeric materials, high T<sub>c</sub> ceramics, materials reaction mechanism, IC encapsulation, in particular, hermetic equivalent plastic packaging, electronic manufacturing packaging processes, interfacial adhesions, PWB, SMT assembly, and components reliability.

Dr. Wong received the AT&T Bell Laboratories Distinguished Technical Staff Award in 1987, the AT&T Bell Labs Fellow Award in 1992, the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society Outstanding and Best Paper Awards in 1990, 1991, 1994, 1996, and 1998, the IEEE Technical Activities Board Distinguished Award in 1994, the 1995 IEEE CPMT Society's Outstanding Sustained Technical Contribution Award, the 1999 Georgia Tech's Outstanding Faculty Research Program Development Award, the 1999 NSF-Packaging Research Center Faculty of the Year Award, the Georgia Tech Sigma Xi Faculty Best Research Paper Award, the University Press (London, UK) Award of Excellence, and was elected a member of the National Academy of Engineering in 2000. He is a Fellow of AIC and AT&T Bell Labs. He served as the Technical Vice President (1990 and 1991), and the President (1992 and 1993) of the IEEE CPMT Society.

**H. Bernhard Pogge** received the B.S. degree in chemistry from Siena College, Loudonville, NY, in 1963 and the M.S. and Ph.D. degrees in physical chemistry from the Stevens Institute of Technology, Hoboken, NJ, in 1965 and 1967, respectively.

He is an IBM Fellow at the IBM Microelectronics Division, East Fishkill, NY. He is also a member of the IBM Academy. His research and development interests have been in material processes and the fabrication of electronic device structures. He is the inventor of the Sidewall technology and the Trench technology, both of which have become integral structure elements in modern electronic device products-worldwide. He continues to concentrate on uniquely new technology direction efforts in these development areas. He is also the author or coauthor of 37 U.S. patents and over 25 professional presentations and publications. He has authored two book chapters, and has edited *Electronic Materials Chemistry* (New York: Marcel Dekker, 1996).

Dr. Pogge received two IBM Corporate Awards, three Outstanding Innovation Awards, a Patent Portfolio Award, and the Texaco Research Award. He is a member of the American Chemical Society and the Electrochemical Society.



**Rao R. Tummala** (F'94) received the B.S. degree in physics, mathematics, and chemistry from Loyola College, India, the B.E. degree in metallurgical engineering from the Indian Institute of Science, Bangalore, the M.S. degree in metallurgical engineering from Queen's University, Kingston, ON, Canada, and the Ph.D. degree in materials science and engineering from the University of Illinois, Urbana.

He joined the faculty at the Georgia Institute of Technology (Georgia Tech), Atlanta, in 1993 as a Pettit Chair Professor in electronics packaging and as Georgia State Research Scholar. He is also the Director of the Low-Cost Electronic Packaging Research Center (funded by NSF as one of its Engineering Research Centers, the state of Georgia, and the U.S. electronics industry). Prior to joining Georgia Tech, he was an IBM Fellow at the IBM Corporation, where he invented a number of major technologies for IBM's products for displaying, printing, magnetic storage, and multichip packaging. He is co-Editor of the widely-used *Microelectronics Packaging Handbook*. He published 90 technical papers and holds 21 U.S. patents and 44 other inventions. His current research interests include packaging materials (metals, ceramics, and polymers) and processes, mechanical properties of materials, thin and thick MCMs, thermal and electrical designs, and integrated passive components.

Dr. Tummala received the David Sarnoff award, the IEEE Sustained Technical Achievement award, the ISHM John Wagnon's award, the Materials Engineering Achievements award from ASM, the Distinguished Alumni award from the University of Illinois, and the Arthur Friedberg Memorial award from the American Ceramic Society. He is a fellow of the American Ceramic Society, a member of the National Academy of Engineering, 1996 General Chair of IEEE-ECTC, and 1996 President of ISHM. He was recently named by *Industry Week* as one of the 50 Stars in the U.S., for improving U.S. competitiveness.