

**RELIABLE FINE-PITCH CHIP-TO-SUBSTRATE COPPER
INTERCONNECTIONS WITH HIGH-THROUGHPUT ASSEMBLY
AND HIGH POWER-HANDLING**

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The Academic Faculty

by

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**RELIABLE FINE-PITCH CHIP-TO-SUBSTRATE COPPER
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AND HIGH POWER-HANDLING**

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Dedicated to my parents, Makarand and Seema

And to my love, Damini

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LIST OF SYMBOLS AND ABBREVIATIONS

<i>AC</i>	Alternating current
<i>AFM</i>	Atomic force microscope
<i>BEI</i>	Backscattered electron image
<i>BGA</i>	Ball grid array
<i>BSE</i>	Backscattered electron
<i>BMVs</i>	Blind micro-vias
<i>BNUF</i>	B-stageable nonflow underfill
<i>C4</i>	Controlled collapse chip connection
<i>CTE</i>	Coefficient of thermal expansion
<i>C-SAM</i>	C-Mode Scanning Acoustic Microscopy
<i>CSP</i>	Chip scale package
<i>D/B</i>	Die bonding
<i>DBC</i>	Direct bond copper
<i>DC</i>	Direct current
<i>DIP / DIL</i>	Dual in line package
<i>DOE</i>	Design of experimental
<i>EM</i>	Electromigration
<i>ENIG</i>	Electroless Ni, immersion Au
<i>EPAG</i>	Electroless Pd, autocatalytic Au
<i>FC</i>	Flip chip
<i>FEM / FEA</i>	Finite element method / Finite element analysis
<i>FIB</i>	Focus ion beam

<i>FT-IR</i>	Fourier transform infrared spectroscopy
<i>IMC</i>	Intermetallic
<i>PECVD</i>	Plasma-enhanced chemical vapor deposition
<i>PGA</i>	Pin grid array
<i>SEM</i>	Scanning electron microscope
<i>SLID bonding</i>	Solid-liquid interdiffusion bonding
<i>SMT</i>	Surface mount technology
<i>SoC</i>	System on chip
<i>SoP</i>	System on package
<i>TC / TCB</i>	Thermocompression bonding
<i>TCT</i>	Thermal cycling test
<i>TIM</i>	Thermal interface material
<i>TLP</i>	Transient liquid phase
<i>TM</i>	Thermomigration
<i>TSMC</i>	Taiwanese Semiconductor Manufacturing Company
<i>TSVs</i>	Through silicon vias
<i>TPVs</i>	Through package vias
<i>NP</i>	Nanoporous
<i>NCP</i>	Nonconductive paste
<i>NCF</i>	Nonconductive film
<i>OSATs</i>	Outsourced semiconductor assembly and test providers
<i>VM</i>	Von Mises
<i>WLUF</i>	Wafer-level underfill
<i>XEDS</i>	X-ray Energy-dispersive spectroscopy
<i>XPS</i>	X-ray photoelectron microscopy

<i>XRF</i>	X-ray fluorescence
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SUMMARY

Emerging high-performance computing systems have been driving advances in packaging solutions such as high-density 2.5D interposer packages with escalating pitch, performance, and reliability requirements for off-chip interconnections. The objective of the proposed research is to design and demonstrate Cu-based interconnections without solders scalable to 20 μ m pitch and below for power handling at current densities exceeding 10⁵A/cm² with high-throughput manufacturability and thermomechanical reliability of the chip and interconnection system.

Solder-based interconnections have been the interconnection technology of choice in chip-to-package substrate applications for close to 60 years because of their electrical properties, thermomechanical reliability, ease of fabrication, self-alignment characteristics, and high-throughput reflow assembly manufacturing. While currently being a manufacturable high-speed assembly process, resulting in high throughput and low cost, solders are now reaching fundamental limits in pitch scaling to below 30 μ m, current handling capacity exceeding 10⁴A/cm², operating temperatures above 85°C, and thermomechanical reliability at small stand-off heights, that are required for fine pitch. As a complete elimination of solders is desirable, all-Copper interconnections are viewed as next era in interconnections and assembly.

Copper interconnections; however face many challenges of their own in meeting high-volume assembly manufacturing with high throughput and high reliability. These challenges are: 1) inadequate deformation of stiff Cu bumps to accommodate non-coplanar and warped surfaces 2) room-temperature oxidation; 3) low diffusivity of Cu below 300°C

assembly temperature and 4) low compliance of short Cu joints to absorb thermal expansion stresses potentially resulting in cracking in either the joint or in the low-K on-chip dielectrics. While many solutions have been proposed, and studied, such as the use of chemical-mechanical planarization (CMP) to eliminate non-coplanarities and vacuum bonding, none have addressed all the challenges mentioned above.

This thesis addressed these two major challenges of high-throughput assembly, involving handling of noncoplanarities and enhancements in reactivity, and high thermomechanical reliability by two different innovative approaches.

In the first approach, ultra-thin Au-based metallic thin films were introduced to circumvent copper oxidation and yet maintain enhanced reactivity of the bonding interfaces. The Au bonding layers provide soft, oxide-free bonding interfaces, enabling assembly at lower temperatures and in air. Low-cost fly-cut planarization of non-coplanar bumps is proposed to lower bonding pressure and this, combined with low temperature assembly, is expected to result in higher assembly throughput. Thermal stability of such planarized interconnections is demonstrated to 1000 hours under ageing at 200°C.

In the second approach, a low-modulus Cu cap made of nanofoam is formed onto bulk Cu micro-bumps to act as a compliant layer to accommodate noncoplanarities at low bonding pressures and as a reactive bonding interface for assembly at low temperatures. Nanocopper foams have a 20-40GPa modulus compared to 130 GPa for pure Cu. Nanofoams also benefit from an ultra-high surface area, providing sufficient reactivity to enable low-temperature, high-speed bonding. During assembly, the foam sinters and

densifies to achieve bulk Cu-like properties post assembly, enabling high-throughput assembly.

In both approaches, the final joints are composed mostly of Cu, forming stiffer interconnections than solders, and unable to absorb thermal expansion stresses through plastic deformation. Such rigid interconnections bring unprecedented thermomechanical reliability concerns, with aggravated stresses on the brittle semiconductor devices as well as on-chip low-K dielectric layers. To address this new challenge, interconnection geometry, particularly their aspect ratio, is optimized, given the existing CTE mismatch in the package assembly, and process innovations are introduced, such as the use of pre-applied underfills, to form reliable low-stress joints. Automotive-graded thermomechanical reliability of solid-state Cu interconnections was demonstrated at pitches down to 50 μ m pitch on 100 μ m-thick organic and glass substrates. Finally, excellent electromigration resistance of Cu-EPAG interconnections at 3×10^5 A/cm² was demonstrated with the high power-handling capability, beyond that of traditional solder-based interconnections.

CHAPTER 1. INTRODUCTION

Transistor scaling has been aggressively pursued since the 1950's, resulting in rapid performance improvements as well as miniaturization of semiconductor devices such as microprocessors. However, transistor integration has recently slowed down, taking a longer time to reach the next technology node than predicted by Moore's Law. As transistor scaling reached its limits in performance and cost, on-chip integration towards higher functionality through the means of 'System-on-Chip (SoC)' technologies were pursued. However, electronic systems concurrently increased in complexity and required co-integration of many heterogeneous functions such as digital, analog and power, which could not be achieved through silicon integration only. These challenges spurred the growth of 'More-than-Moore' technologies such as horizontal integration through Multi-chip-module (MCM) and 3D vertical chip stacking in the form of 'System-in-Package (SiP)' technologies, aimed at miniaturization and heterogeneous integration of logic and memory. However, this integration accounted for only 10% of the system and faced several challenges in terms of logic-memory design complexity, electrical and yield losses and reliability of logic dies. This forced the semiconductor industry to rethink their system integration strategy and turn to packaging to meet the functional density requirements of emerging electronic systems. The 3D Systems Packaging Research Center at Georgia Tech is pioneering the 'System-on-Package (SoP)' scaling approach to address these challenges and enable complete heterogeneous system integration through miniaturization of device, package and system board into a single package including all system functions. As digital systems require bandwidths in excess of 1TB/s for ultra-fast communication and high-

performance computing, high I/O packages enabling the interconnection of individual logic and memory chips on silicon, organic or glass substrates with high-density wiring has been extensively pursued. This so-called 2.5D integration aims at interconnecting the chips as if they were one single piece of silicon, pushing off-chip interconnections towards the required back-end-of-line pitches. An alternative to this was recently proposed with the advent of embedded packaging in RF and power modules, where I/Os from embedded chips fan out into the package without requiring assembly. However, current fan-out technologies face many challenges in achieving high I/O densities and interconnecting large dies so are not yet considered for advanced logic-memory integration. While Georgia Tech is pushing both technologies in parallel, this research focuses on bridging the off-chip interconnection gap with silicon. Conventional solder-based interconnection technologies are incompatible with such pitch scaling requirements, bringing the need for solid-state all-copper interconnections that have a high CTE and elastic modulus. Copper is notoriously a hard material to bond with due to its high melting point, room-temperature oxidation and low compliance. Therefore, Cu-Cu bonding presents unprecedented throughput, reliability and process challenges that are being addressed in this work.

1.1 Research Motivation and Strategic Need

1.1.1 Pitch scaling for emerging systems

High-performance computing systems have been driving advances in device, packaging and interconnection technologies over the last several decades to meet their escalating performance, miniaturization and cost requirements. Transistor scaling, following Moore's Law, has been the basis of all these advances in logic and memory

integrated circuits (ICs) with increasing transistor densities and optimized performance. However, transistor scaling has recently been slowing down, with only incremental improvements in performance as the Si-based CMOS technology reaches its physical limits and the complexity of integrating non-digital technologies in CMOS escalates. Further, there is no longer a cost reduction in moving to the next node. These challenges in realizing Moore's Law's predictions have compelled the semiconductor industry to turn to packaging as the next platform for system integration [1]. The International Technology Roadmap for Semiconductor (ITRS) has recently modified their system integration roadmap to reflect this trend with "More of Moore" aiming at miniaturization of digital functions with new transistor concepts, and "More than Moore" targeting heterogeneous integration on Silicon with advances in Si-packaging technologies and architectures [2]. Under this roadmap, System-on-Chip (SoC) technology, consisting of monolithic co-integration of digital, analog or RF circuitries in a single IC, was later pursued to further increase the functional density of electronic systems with the homogeneous 'More of Moore' approach. SoC basically integrates computing, communication and consumer components onto a single Si chip. However, design complexities involved in such integration, high manufacturing costs and IP issues plagued further advances towards a single SOC-based Si system. To concurrently achieve miniaturization and higher functional densities, the industry explored module-level integration, ushering in the trend of 'More than Moore' technologies through horizontal stacking of Si chips (Multichip Module (MCM) technology) as well as more recently 3D vertical stacking of thinned logic and memory chips with through-silicon vias (TSVs). However, the presence of TSVs in logic dies have created several challenges such as complex co-design between logic and

memory, large thermomechanical stresses on logic dies from TSVs as well as yield losses due to lack of testability for known-good-dies (KGD). Furthermore, 3D-ICs still face design limitations in terms of thermal management and power delivery of logic IC [3]. Although SoC, MCM and SiP seek to ultimately increase functionality while following Moore's Law, they fail to achieve miniaturization at system level. The gap between transistor scaling (based on the gate length of a transistor) and system scaling (based on off-chip interconnection pitch) illustrated in Figure 1.1 is becoming quite acute.

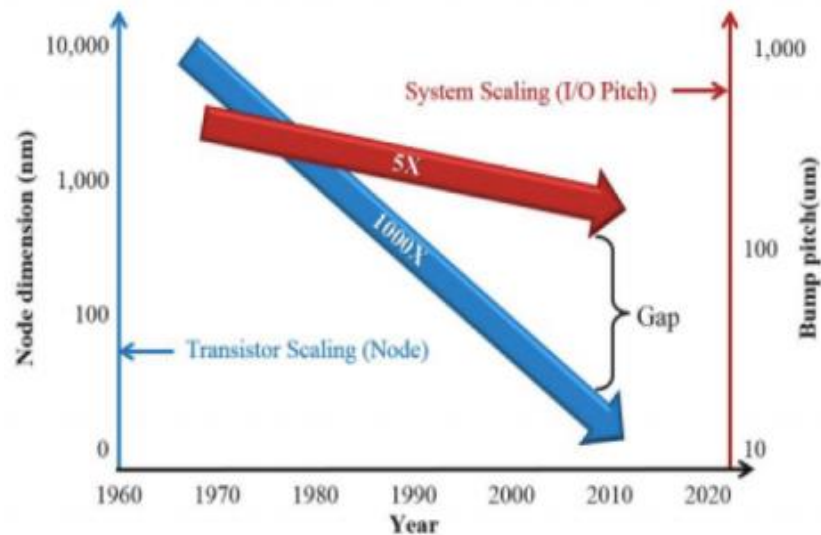


Figure 1.1 Gap between transistor and system scaling (Courtesy Dr. S. Iyer, IBM)

To bridge the gap between transistor scaling and system scaling, a new paradigm for system miniaturization and integration has been proposed by the 3D Systems Packaging Research Center at Georgia Tech with the pioneering System-on-Package (SoP) technology. In the SoP approach, heterogeneous functions are directly integrated on the package substrate. Packaging is now a key enabler to reduce the overall system cost and size, and, therefore, adds value to the system. The SoP vision has rapidly gained

momentum in high-performance computing, giving rise to advanced packaging technologies as demonstrated in Figure 1.2. One such technology is that of 2.5D integration. In 2.5D integration, a single, costly SoC die is split into multiple dies that can be fabricated with different, more cost-effective technology nodes. An interposer package with high-density wiring is then introduced for high-speed, high-bandwidth die-to-die communication. This approach was first demonstrated in production by Xilinx Inc. in 2011 [4].

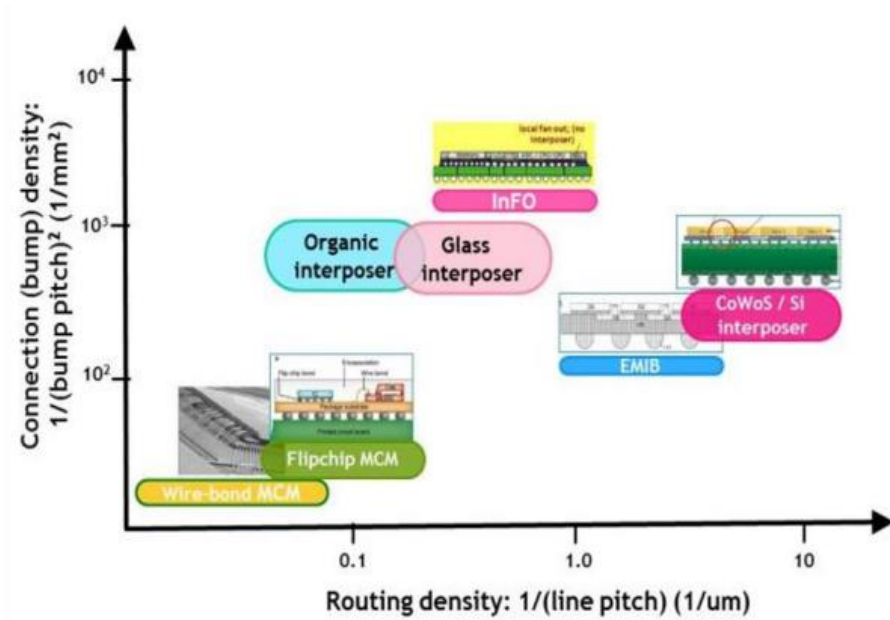


Figure 1.2 Comparison of advanced packaging technologies: I/O density v/s routing density

While 2.5D integration has heavily relied on expensive and lossy Si interposers, advances in substrate technologies have enabled development of panel-level ultra-thin organic and glass interposers with fine-wiring capability and are competing with Si interposers for performance and cost. With a tailorable CTE between 3.8-9.8 ppm/°C, glass substrates have been shown to provide design flexibility for chip- and board-level

reliability. Such heterogeneous integration at package level is becoming more and more critical with the emergence of cloud computing, optical communications and ‘Internet-of-things (IoT) systems to achieve ultra-high bandwidth (1TB/s) at lower power consumption.

In parallel, a chip-last approach to system integration using embedding technologies has been developed in recent years, primarily applied to RF and millimeter-wave modules. Embedded packages rely on fan-out of on-chip I/Os using back-end-of-line (BEOL) and packaging re-distribution layer (RDL) tools without the need for assembly, thus driving down cost and improving throughput. An example of such embedded wafer-level packaging in production is TSMC’s Integrated fan-out (InFO) package, used in the Apple iPhone 7 as shown in Figure 1.3 [5]. While both chip-last and chip-first configurations have been demonstrated in embedded packaging, it still is a nascent technology with critical challenges in: 1) die placement accuracy and coplanarity with increasing I/O density and fine-pitch RDL scaling; 2) limited RDL scaling due to molding compound shrinkage and die warpage; 3) limited to small-to-medium sized ICs and packages with high cost for packages beyond 20mm size; and 4) concerns of yield loss with high-value chips in chip-first configurations.

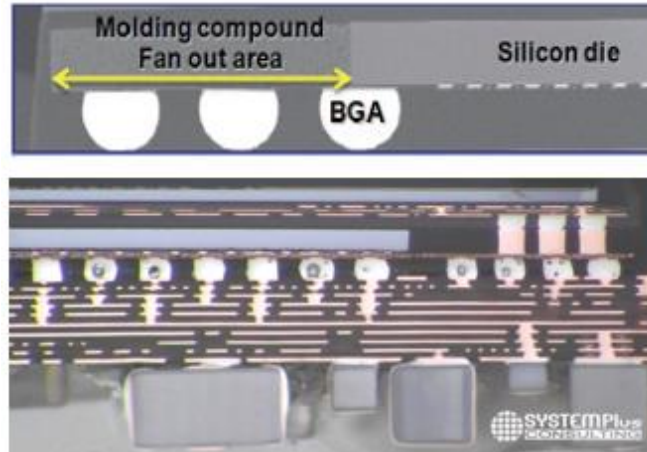


Figure 1.3 (Top) TSMC's InFO package for processors and (bottom) TSMS processor-memory stacking

These new approaches to system scaling utilizing advanced substrate technologies with interconnect pitches and densities close to BEOL dimensions subsequently require scaling of off-chip interconnection pitches with unprecedented performance and reliability requirements.

1.1.2 Evolution of interconnection and assembly technologies

Modern-day graphics processor units (GPUs) require high bandwidths ranging from 512 GB/s to 1 TB/s for data transmission. In high-performance computing, processors carry out trillions of floating operations per second to produce high-resolution data or do deep learning. To meet this calculation capacity, silicon dies are fabricated with transistor densities in excess of 10 billion/mm², with die sizes exceeding 1,000 mm². An example of this is Advanced Micro Devices Inc. (AMD)'s next-generation Fiji Chip, which is a GPU in the Radeon™ Fury product line, providing a bandwidth of 512 GB/s. Furthermore, according to ITRS roadmap predictions, high-performance computing is expected to drive the off-chip interconnection pitch to 20μm and below in the next 5 years, with bump

diameters of 10 μm or less. Concurrently, an increase in power density is expected from 0.6W/mm² currently to 1.15W/mm² by 2020. At interconnection level, this translates into higher current densities, exceeding 0.5 $\times 10^6\text{A/cm}^2$, and operating temperatures above 100°C. These requirements are highlighted in Figure 1.4 and exceed the fundamental material limitations of traditional solder-based interconnections in scalability, electromigration and thermomechanical reliability performances [1]. A new interconnection and assembly technology node, beyond solders, is, therefore, required to address this grand challenge. High-performance computing has historically been driving the evolution of interconnection technologies to achieve higher I/O densities from wire-bonding to flip-chip technologies, as illustrated in Figure 1.5.

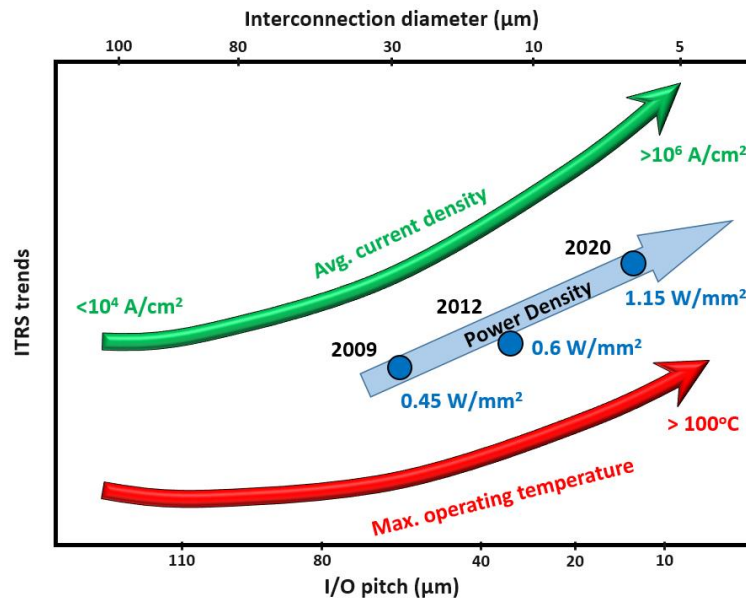


Figure 1.4 ITRS roadmap predictions (arbitrary units) vs I/O pitch for high-performance interconnections

Ever since IBM's invention of the C4 (Controlled Collapse Chip Connection) technology [2], numerous advances have been made in solder-based interconnection technologies to keep up with increasing I/O densities on one hand, and IC size reduction

on the other, necessitating pitch scaling. Pitch scaling, however, requires a reduction in solder volume to prevent bridging, thereby increasing thermomechanical strains in solder joints and limiting scalability of conventional C4 bumps to $\sim 80\mu\text{m}$ pitch. Copper micro-bumps were introduced to increase the interconnection standoff height and mitigate strains in the solder caps. As logic-memory packages moved to MCM and SiP technologies, the Cu pillar technology, utilizing mass reflow, was subsequently pursued for further pitch scaling [6], with high throughput of 40,000 units per hour (UPH). At pitches below $\sim 60\mu\text{m}$, application of pressure in assembly was found necessary to control warpage and subsequently achieve uniform joints across the chip. Thermocompression bonding (TC) is, however, a sequential chip-to-substrate strip process as opposed to batch processing in mass reflow, degrading assembly throughput by $\sim 40\text{X}$ to around 1,000 UPH. To improve assembly yield and throughput, Amkor developed the now standard TC-NCP (thermocompression bonding with non-conductive paste) process, combining high-speed assembly and snap-cure underfilling [3]. The use of pre-applied underfills enabled a better control of the joint shape for high yield and reliability. The industry standard TC-NCP process is illustrated in Figure 1.6 where the solder caps form a liquid phase during assembly at $<250^\circ\text{C}$ to accommodate chip and substrate non-coplanarities. After assembly, the solder joints form a relatively compliant interface that can absorb thermal expansion stresses and strains. This technology has been demonstrated at pitches down to $40\mu\text{m}$ in production and $25\mu\text{m}$ in R&D [1], but faces many fundamental limitations in achieving finer pitches.

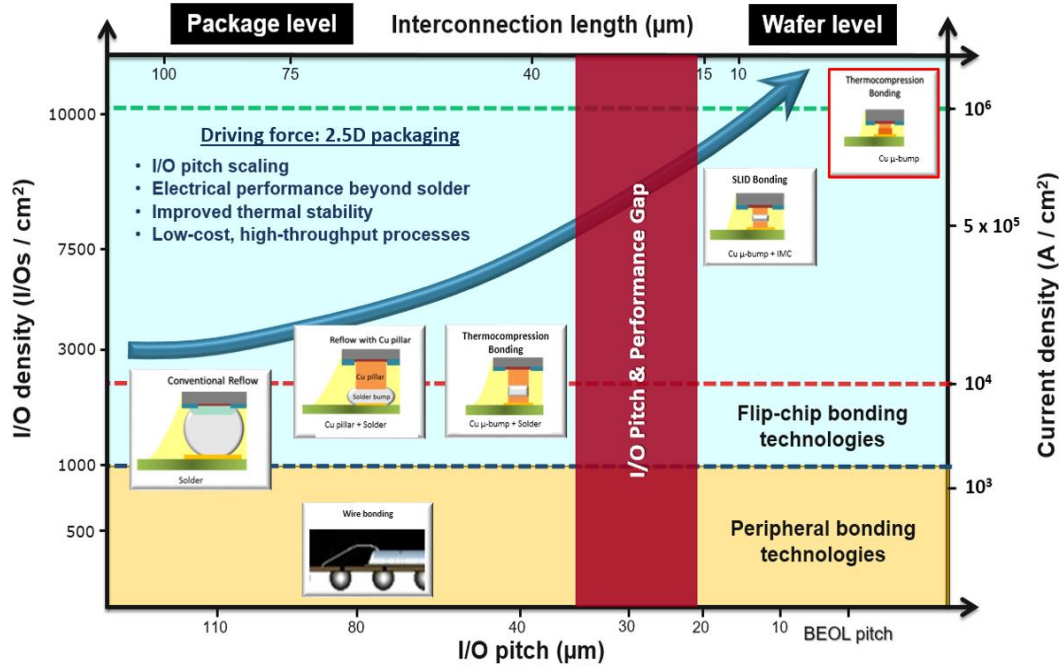


Figure 1.5 Evolution of off-chip interconnection technologies for pitch and performance scaling

The projected reduction in solder volume from 15-30μm solder heights in current Cu pillars to less than 10μm at 20μm pitch is bringing unprecedented challenges in control of interfacial reactions, intermetallic growth and subsequent joints' microstructure, properties and reliability. Conventional Sn-based solders are also reaching their fundamental limits in current carrying capability at 10^4 A/cm^2 and operating temperatures, with massive creep and fatigue failures expected from temperatures as low as 70°C.

All-intermetallic joints formed by solid-liquid interdiffusion bonding (SLID) have been proposed as a natural next step for further pitch scaling. SLID interconnections retain the processability of solders with low-temperature assembly and a low-modulus liquid-phase (molten solder) to accommodate non-coplanarities, coupled with the improved thermal and electrical stability of intermetallics. Intermetallics can typically sustain current densities up to 10^5 A/cm^2 , an order of magnitude higher than solders, and have much higher

melting points, improving microstructural stability. While SLID bonding has already seen some adoption in niche applications such as memory chip stacking and 3D ICs, wide acceptance of this technology in chip-to-substrate (C2S) applications, i.e. in package structures with thermal expansion mismatch, is limited by its relatively low assembly throughput, giving high cost, and reliability concerns primarily due to voiding [7]. Solid-state interconnections, without solders, have, therefore, been identified as the ultimate goal for high-performance computing applications. In particular, copper has excellent power-handling capability, high-speed signal transmission and high thermal conductivity [8, 9], thus making it the ideal choice to build RDL layers directly on-chip. However, Cu-Cu bonding faces its own set of challenges that are discussed in the next section

1.1.3 State-of-the-art in all-Cu interconnections – the ‘holy grail’

Though highly sought after by the semiconductor industry for decades, direct Cu-Cu bonding faces many fundamental material and process challenges that have hindered technology development, including: 1) room-temperature oxidation; 2) low diffusivity at temperatures below 300°C; and 3) low tolerance to non-coplanarities and warpage due to relatively high elastic modulus. Comparing this with the standard Cu Pillar technology, these fundamental challenges are addressed through: a) fluxing under assembly to prevent oxidation; b) high diffusivity of solder in molten form at 260°C; and c) high compliance and fatigue life due to low elastic modulus of solders, respectively. But such solutions cannot apply to direct Cu-Cu bonding because: (a) of the incompatibility of fluxing in typical direct Cu-Cu bonding conditions; (b) Cu has a melting point of 1081°C and undergoes comparatively slower kinetics under solid-state diffusion, and (c) Cu has a relatively high modulus of 120-130GPa as compared to that of solders.

Consequently, existing technologies rely heavily on selective activation of the bonding surface to ensure perfect contact and high diffusivity across the Cu-Cu interface for metallurgical bonding [10], as well as involve expensive planarization steps to eliminate non-coplanarities [11-15]. Essentially, current state-of-the-art technologies in direct Cu-Cu bonding require high bonding forces, assembly in vacuum, inert or reducing environments with temperatures far greater ($>300^{\circ}\text{C}$) than that used for solder-based reflow, and long annealing times with expensive chemical-mechanical polishing steps. This limits their adoption to wafer-level packaging (WLP) as bonding pressures and temperatures exceed current substrate material limitations for chip-to-substrate (C2S) assemblies. The most widely used Cu-Cu bonding technology is described in Figure 1.6 in comparison with the standard Cu pillar process.

Chemical-mechanical planarization is first applied on both surfaces so the Cu pads are then embedded in the silicon oxide layer. Oxide bonding is achieved in vacuum at temperatures exceeding 300°C for 1-2 hours followed by a post-bond high-temperature anneal step in the range of $250\text{-}350^{\circ}\text{C}$ to allow for the thermal expansion of Cu and form bonds. This greatly reduces the throughput of direct Cu-Cu bonded assemblies, and limits adoption in high-volume manufacturing. Furthermore, bonding and post-bond anneal temperatures exceed the material limits for substrate technologies other than silicon (ex: organic substrates) and are a detriment for wide-spread adoption. The trade-offs between performance and assembly throughputs are also highlighted in Figure 1.6.

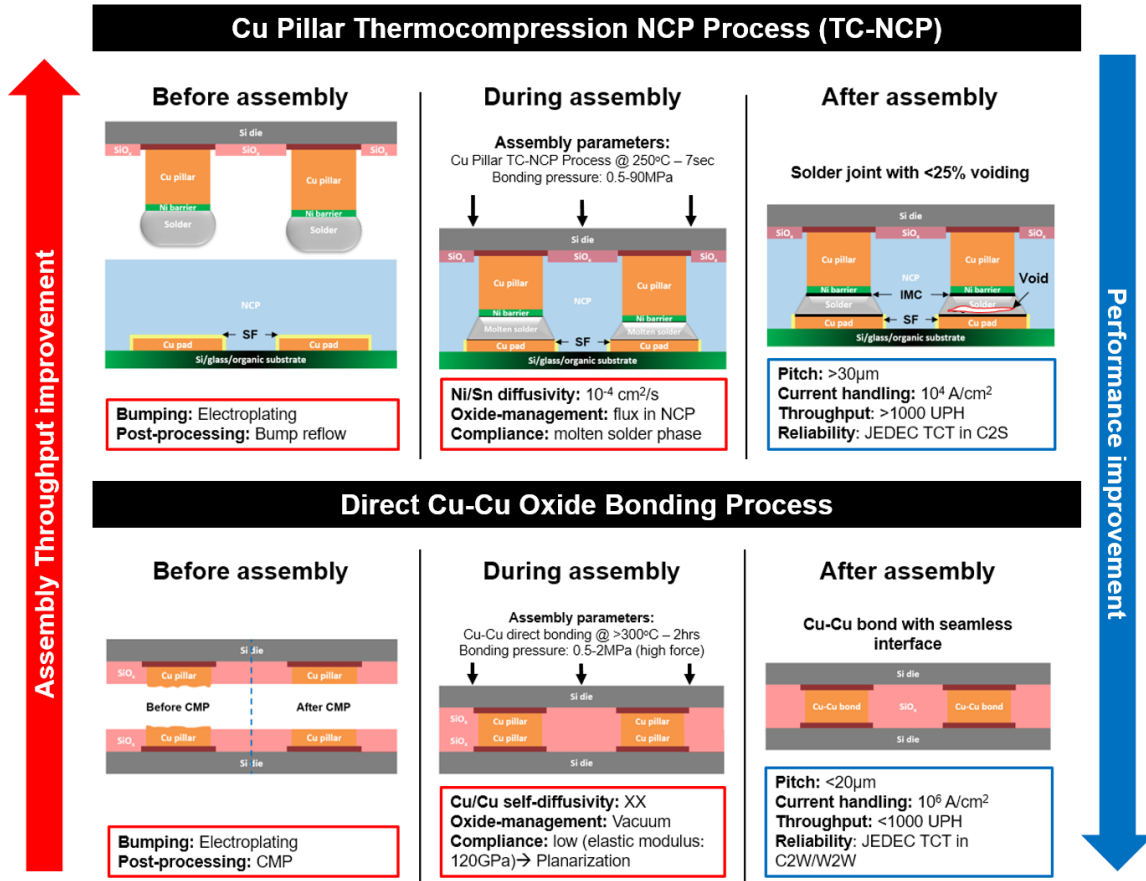


Figure 1.6 Comparison of the most advanced industry-wide compatible technologies between the C2S and WLP applications

While all-Cu interconnections meet the pitch and performance requirements highlighted by the ITRS roadmap, existing technologies are only applicable to CTE-matched wafer-level packaging, resulting in the off-chip interconnection gap. This is because Copper makes very stiff joints, resulting in a different distribution of thermal expansion-related stresses. With such interconnections, the failure mode is expected to shift from fatigue failures experienced in solders to stress build-up in the chip, particularly in the ultra-low-K (ULK) dielectric layers [16]. As a result, there is a need for low-modulus interconnections that can absorb the strain and protect the integrity of the low-K layers underneath. To this effect, interconnections based on capillary bridging of Nano-Cu ink under evaporation were demonstrated by IBM Zurich to form interconnected necks [17].

Nano-pastes and inks benefit from high surface area and can, therefore, sinter at low temperatures to achieve strong joints with high electrical and thermal performances after densification. Inks and pastes also provide a viscous phase which, like molten solder, can accommodate non-coplanarities, extending applicability of this technology to C2S applications. While this technology is promising, there are challenges with respect to: 1) high retained porosity post-sintering; 2) agglomeration of particles causing adhesion issues; 3) risks of bridging with pitch scaling due to viscous binder phases; 4) expensive surface treatments to prevent oxidation etc.

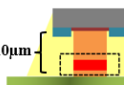


As a result, a new class of solid-state Cu interconnections is required to bridge the off-chip interconnection gap with improvements in assembly throughput compared to direct Cu-Cu bonding and in pitch scaling and reliability as compared to conventional solder-based approaches.

1.2 Research Objectives and Technical Challenges

The objectives of this research are to design and demonstrate chip-to-substrate solid-state Cu interconnections scalable to 20 μ m pitch and below, with power handling at current densities exceeding 10⁵A/cm² and thermal stability at temperatures above 100°C, while retaining processability and assembly throughput to meet high-volume manufacturing (HVM) requirements, and achieving high reliability in presence of thermal expansion-mismatch. The fundamental properties, reliability and manufacturability objectives are reported in Table 1 and benchmarked against prior art in interconnection technologies. Two fundamental challenges were identified in realizing the research objectives: 1) high-throughput assembly including considerations of the interconnection

system design with a) reactivity of the bonding interface and b) accommodation of noncoplanarities; and of the assembly process with c) high-speed bonding; and 2) high reliability in a chip-to-substrate package architecture with thermal expansion (CTE) mismatch. These two fundamental challenges are detailed in the following subsections.

Table 1 Research objectives beyond prior art and associated technical challenges

Parameters		Objectives	State of the Art		Technical Challenges	Research Tasks
			Cu pillar – solder cap	Direct Cu–Cu bonding		
Performance characteristics	Package configuration	 10µm	 25-35µm	 <10µm	High-throughput assembly: a) Energy barrier to diffusion b) Managing non-coplanarities c) Short assembly cycle time	Task 1: Modeling and design of interconnection system for improved reactivity and accommodation of non-coplanarities Task 2: Design and demonstration of high speed assembly of Cu interconnections
	Pitch	<20µm	>35µm	<10µm		
	Power handling	>10 ⁵ A/cm ²	<10 ⁴ A/cm ²	>10 ⁶ A/cm ²		
	Shear strength	>40MPa	40 – 60MPa	30 – 180MPa		
Assembly manufacturability	Throughput	>1000 UPH	>1000 UPH	<1000 UPH	High reliability in a chip-to-substrate (C2S) system with CTE mismatch	Task 3: Modeling, design and demonstration of reliability at interconnection and IC level
	Bumping	Standard, low cost	Standard, low cost	Expensive		
	Tolerance to noncoplanarities	High	High	Low		
	Bonding temp	< 250°C	230-260°C	RT – 400°C		
	Bonding time	3sec + anneal	3sec	>30min		
	Bonding pressure	<40 MPa	0.5-40 MPa	0.1 – 300 MPa (pre-annealing)		
Reliability		JEDEC standard TCT and thermal ageing				

1.2.1 High-throughput assembly

Throughput is qualified as the number of units-per-hour (UPH) that can be produced through an assembly process and essentially is an integral function of the bonding temperature, time, pressure and environment. Formation of metallic joints fundamentally relies on: a) thermodynamic diffusion mechanisms across bonding interface that require energy to be activated, and b) atomic-scale contact at the bonding interface. The energy barrier to diffusion is known to increase in presence of surface oxides, roughness and non-coplanarities among other factors. External energy in the form of heat, force or reducing

atmospheres is, therefore, necessary to reduce this energy barrier to diffusion and thereby, reduce the time for interface bonding. Under ideal atomic contact, metallurgical joining becomes a function of temperature and time with higher temperatures giving higher diffusion rates, thus lower assembly times. The thermal budget is, however, limited by the maximum admissible temperatures of package substrates, in particular the organic materials they are made of, and the development of severe thermal expansion stresses. Temperatures below 250°C, as applied in conventional reflow, are desired for assembly on existing substrate technologies.

However, under non-ideal atomic contact such as with presence of non-coplanarities that are typical in chip and substrate fabrication processes, application of force may be required to achieve sufficient atomic contact area at the bonding interface to promote diffusion and grain growth. In legacy solder-based interconnection systems, above ~60µm pitch, the solder height was sufficient to accommodate non-coplanarities and warpage solely through melting, collapse and wetting of the solder. No external force was then required to achieve adequate yield, leading to the batch process known as “mass reflow” with highest throughput exceeding 40,000UPH. At finer pitches, limited solder heights led to yield loss and reliability concerns as the joint shapes varied across the chips due to warpage. Pressure was, therefore, added to control assembly warpage and solder spread. Pressure application became even more critical when using pre-applied underfills to ensure penetration of the bumps in the viscous underfill layer and contact between bumps and pads. However, thermocompression bonding is inherently a serial process, where chips are assembled individually on a substrate strip. Force application in assembly also requires complex and expensive tooling to ensure planarity. As mentioned before, this

results in a dramatic drop in throughput down to ~1,000UPH. In the typical Cu pillar TC-NCP process, metallurgical bonding is typically achieved in 3s at peak temperature of 250°C in the joints, and pressures in the 40-90MPa range.

As application of pressure seems unavoidable to achieve such fine pitches, current industry focus is on improving the throughput of thermocompression bonding through gang, collective or laser-assisted bonding. Two-step processes in which pre-applied underfill is first used to tack the chip on the substrate, then followed by a batch thermal aging process to form the metallurgical joints, are also highly desirable as they limit the time spent under the compression tool. To achieve high-throughput assembly, bonding temperatures should not exceed 250°C, bonding times 3s (under compression) and bonding pressures 40MPa. Compliance of the interconnection system is critical to overcome at least 3 μ m of non-coplanarities with reasonable bonding pressures. Copper, being such a stiff material with a high yield strength (>170MPa), does not provide such compliance, and requires much higher pressures to achieve adequate contact and subsequent formation of a metallurgical joint. Copper is also prone to room-temperature oxidation and has low self-diffusivity at temperatures below 300°C. These challenges are addressed in this work through design of solid-state Cu interconnections with engineered-bonding interfaces for assembly throughput and manufacturability.

1.2.2 Reliability of chip-to-substrate system (C2S) with CTE mismatch

Solder interconnection systems work well even in presence of thermal expansion mismatch between chip and substrate as they form soft, deformable interfaces. While accumulation of plastic strains ultimately results in fatigue failures of the joints, it helps

reduce the stress on the fragile and expensive ICs. Alternatively, copper is a much stiffer material which is not expected to experience a lot of plastic strains in the operating temperature range of computing applications. This results in failure modes not only at the interconnection level, but also brittle shear-failures in the low-K on-chip dielectric layers, with aggravated risks of crack propagation with larger CTE mismatch between chip and substrate. While it has been demonstrated that the use of pre-applied underfills such as non-conductive pastes or films (NCP or NCF) in solder-based assembly can effectively reduce the energy release rate and prevent crack propagation through development of compressive stresses [18], such approach has never been demonstrated on a non-CTE matched chip-to-package substrate assembly with direct Cu-Cu bonded interconnection systems and, therefore, needs to be verified.

1.3 Proposed Unique Approach

To realize these objectives and address the technical challenges, the two unique approaches described in Figure 1.7 were developed in parallel. . The first approach enhances assembly throughput with the following two key innovations in interconnection design and a high-speed 2-step assembly process: a) ultra-thin metallic coatings deposited on Cu bumps and pads to provide oxide-free and more reactive bonding interfaces, while the overall interconnection retains of the key properties of Cu, and b) a low-cost fly-cut planarization technique used to eliminate bump non-coplanarities. This material system has been so designed to meet the assembly throughput and reliability challenges of direct Cu-Cu bonding. Bimetallic coatings were considered in this work with Au used as reacting layer on account of its nobility, high ductility and softness and improved bondability as compared to Cu. Bump planarization and metallic coatings were applied as post-processing

steps after wafer bumping with standard Cu pillars, and leverage package-level processes for HVM compatibility. The metallic coatings, planarization and assembly processes were co-designed to meet performance, manufacturability and reliability objectives before, during and after assembly. From the joining process viewpoint, a pre-applied underfill was introduced to mitigate thermal expansion stresses in assembly and achieve high thermomechanical reliability. Two-step processes including a high-speed TC-NCP process followed by a batch-type thermal aging step were considered for highest assembly throughput ($>1,000$ UPH) possible in chip-to-substrate packaging architectures.

The second approach advances assembly throughput by replacing the standard solder cap applied on Cu pillars by a solid-state, low-modulus nano-copper foam cap with the following attributes addressing the abovementioned throughput challenges: a) highly-reactive nano-surfaces enabling low-temperature densification to achieve bulk-like properties after assembly, b) sub-20GPa Young's modulus as synthesized to provide high tolerance to surface roughness, non-coplanarities, and warpage. In addition, nano-copper foams benefit from low-cost fabrication processes through electrodeposition and chemical dealloying, compatible with standard lithography processes and have outstanding pitch scalability given by solid-state bonding. While nano-Cu foams do not possess the wettability of solders, their low modulus enables, for the first time, formation of all-Cu joints within the thermal and force budget of package-level processing, without any additional post-processing step.

This document highlights the research and progress carried in both approaches and positions them fundamentally in contrast to the state-of-the-art in Cu bonding technologies.

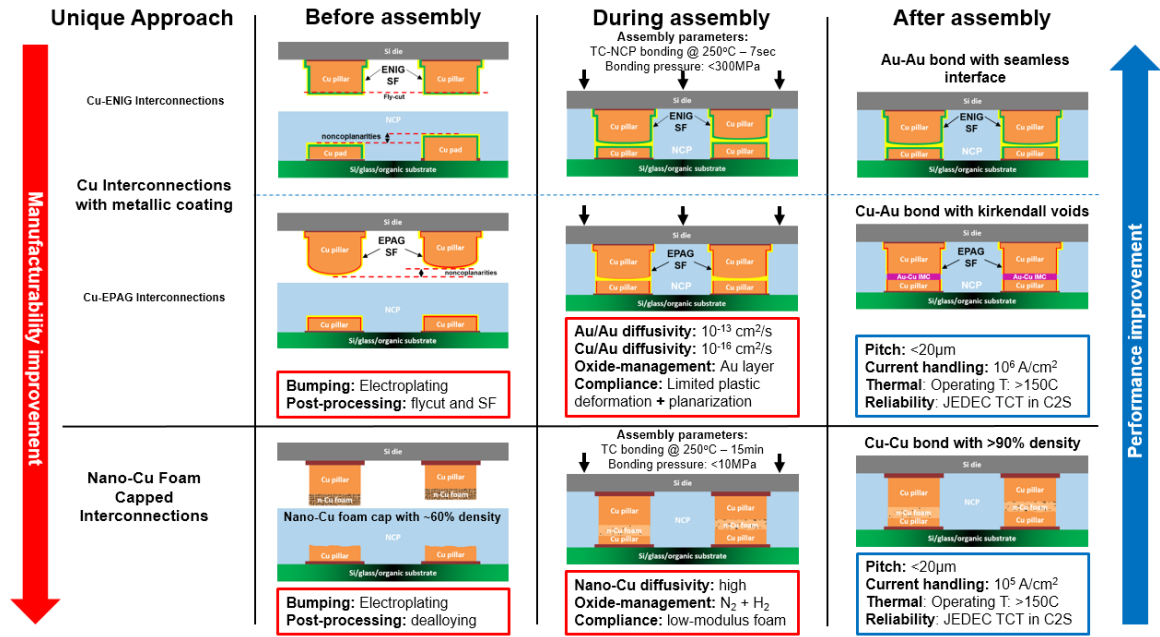


Figure 1.7 Unique approaches beyond the current prior art for Cu interconnections without solders

1.4 Research Tasks

Two main research tasks were defined to overcome the above-mentioned challenges, as shown below for both unique approaches:

1.4.1 Research Task 1: Modeling, design, and demonstration of copper interconnection system for improved reactivity and accommodation of non-coplanarities

The objective of this task is to design and demonstrate novel Cu interconnection systems for high-throughput manufacturing assembly. Two approaches were pursued in parallel to address this grand challenge and provide options for implementation by the semiconductor industry. In the first approach, conformal ultra-thin metallic coatings were introduced on Cu bumps and pads to prevent copper oxidation as well as enhance plasticity of the bonded interface. They were designed from 1st principles utilizing theoretical and kinetic diffusion models to ensure: a) a long shelf-life time at 25°C; b) formation of stable

and reliable metallurgical interfaces through low-temperature, low-pressure and high-throughput assembly; c) ease of post-processability through electroless deposition of metallic coatings; d) high reliability under temperature and current stressing. Thermomechanical finite-element modeling (FEM) was carried out to optimize the bonding parameters as well as assess the need for planarization towards high-throughput assembly.

In the second approach, low-modulus nano-copper foam caps, akin to solder caps, are fabricated on Cu pillars to enhance interface reactivity and improve tolerance to non-coplanarities. Analytical and finite-element models were utilized to design the interconnection system, dealloying and patterning-based strategies for ease of fabrication were demonstrated. Sintering studies were carried out to understand fundamentals of densification within the foam structures. Alloying and patterning processes were developed to ensure ease of fabrication within the CMOS infrastructure. Lastly, assembly of patterned nano-copper foam interconnections was demonstrated using a low-temperature, low-pressure process. The Cu pillar with nanocopper caps technology was conceptualized, developed and demonstrated for the first time in this work, and was, therefore, not subjected to optimization of the assembly process for highest throughput and thermomechanical reliability, focus of Tasks 2 and 3. After densification, the Cu pillar interconnections with nanocopper caps essentially behave like bulk-like joints and are expected to face similar reliability challenges as in the first approach, except for potential technology-specific failure modes at interconnection level.

1.4.2 Research Task 2: Design and demonstration of high-speed assembly of Cu interconnections

The objective of this task is to demonstrate high-speed assembly of Cu interconnections using a optimized bonding parameters. Preliminary compression tests were carried out to validate the findings of the thermomechanical modelling from Task 1. Assembly parameters of as-plated and planarized Cu interconnections were compared to develop a low-pressure, low-temperature bonding process. high-temperature stability was assessed through die shear tests after thermal ageing for 1000 hours at 200°C with microstructural analysis of the aged to study interfacial reactions and confirm modeling predictions. Furthermore, a novel 2-step approach involving thermocompression bonding with pre-applied non-conductive paste material (TC-NCP) was applied to improve the assembly throughput of chip-to-substrate Cu interconnections.

1.4.3 Research Task 3: Design and demonstration for reliability at interconnection and IC level

The objective of this task is to demonstrate high-reliability of proposed unique approaches at the interconnection and IC levels. Regardless of the approach used, it is imperative that the joints formed achieve bulk-Cu like properties after assembly. As a result, reliability of the interconnect joints need to be evaluated first before applying a more system-level approach to reliability of the package. An FEM model featuring a C2S package assembly was built to model the effect of thermal cycling on reliability of stiff Cu interconnections with underfill. Design rules of the interconnection system were established as a function of the interconnect aspect ratio and substrate CTE to design reliable Cu interconnections. Furthermore, a C2S model with a low-K dielectric stack-up was developed to understand the effect of pre-applied underfill on the stress redistribution and IC-level reliability for Cu-Cu interconnections. Electromigration testing at high current density of 3×10^5 A/cm² at 150°C was

carried out to demonstrate high power-handling capability of this system. To validate the predictions from the model, the proposed Cu interconnections were assembled onto organic and ultra-thin 100 μ m glass substrates in a chip-to-substrate configuration using the 2-step TC-NCP process to demonstrate thermomechanical reliability down to 50 μ m pitch.

1.5 Thesis Organization

This document first reviews the state-of-the-art of Cu interconnections with respect to technical challenges of high-throughput assembly from both design of the interconnection system and bonding technology, and system reliability in Chapter 2, highlighting how the identified technical challenges have been addressed in academic research and industry. Chapters 3 focus on the design and demonstration of Cu interconnections with ultra-thin metallic coatings and their assembly process for highest throughput. Chapter 4 then focuses on the reliability assessment of this technology in chip-to-substrate package assemblies in presence of CTE mismatch. Chapter 5 presents the design, fabrication, assembly and preliminary characterization of the novel Cu pillar with nanocopper caps technology with a fundamental focus on understanding sintering kinetics in nanoporous metal systems. Chapter 6 provides a brief summary, key conclusions and intended future work to fully demonstrate the proposed technologies.

CHAPTER 2. LITERATURE REVIEW

All-Cu interconnections are highly sought after by the semiconductor industry as the next interconnection node, beyond conventional solders, for chip-to-substrate applications. While Cu interconnections overcome the shortcomings of solders in pitch scalability, electrical and thermal performances, direct Cu-Cu bonding is hindered by material limitations of Cu itself: room-temperature oxidation, low self-diffusivity and relatively high elastic modulus hindering intimate contact at the bonding interfaces. These barriers were addressed head-on through expensive planarization steps such as chemical-mechanical polishing (CMP) to eliminate non-coplanarities, and use of high bonding pressures and temperatures, as well as vacuum or inert environments in assembly, giving rise to the “Oxide Bonding” process that is currently used in wafer-level packaging (WLP) [11-15]. Such processes are not scalable to the packaging world due to limitations on allowable process temperature for organic substrates ($<200^{\circ}\text{C}$). Cu pillar technology utilizing reduced solder volumes is the most standard process used for C2S assembly on account of the compatibility of solders with substrate processing conditions as well as its ability deform plastically to absorb stress and relieve non-coplanarities. However, the trend towards system scaling in advanced computing applications through 2.5D, 3D and embedded assembly has required the package in itself to be more integrated with high-performance requirements. This has necessitated the scaling of off-chip interconnect pitches to follow that of on-chip scaling, thus increasing I/O density with pitches $<20\mu\text{m}$. As current solder-based assembly technologies do not scale below $30\mu\text{m}$ pitch on account of solder bridging and voiding challenges, the need for solid-state Cu-Cu bonding in chip-to-substrate (C2S) applications is growing. This brings in two new major challenges: 1) assembly throughput and 2) reliability with CTE mismatch. This chapter dives into the

details of the latest technologies based on solid-state Cu-Cu bonding being developed in academia and industry to address the challenges above.

2.1 High-throughput Assembly

The main parameters of a high-throughput assembly are bonding temperature, environment, bonding pressure and assembly time. While process parameters affect the quality of the final metallurgical bond, it is imperative to understand the material limitations as well to develop innovative assembly technologies. Unlike conventional solder, solid-state materials such as copper have high melting points (1081°C) and have low self-diffusivity at bonding temperatures <250°C. The thermodynamic barrier to diffusion is quite high, giving low self-diffusion rates and high transition times for stable phase formation as compared to molten phase diffusion. Moreover, the self-diffusion coefficient of copper is 5 orders of magnitude less than that of molten solder at 250°C [19], thus requiring an external driving force for faster diffusion kinetics. Furthermore, copper oxidizes in ambient conditions and the rate of oxidation increases at 250°C leading to the formation of stable CuO and Cu₂O oxides that are very hard to break. This oxidation behavior of copper is shown under ambient air conditions as well as at 240°C in Figure 2.1. Thus, to achieve metallurgical bonding in solid state necessitates clean and oxide-free surfaces and the use of an external driving force such as ultrasonic energy or pressure under an inert / vacuum / reducing environment. The bonding parameters of time, temperature and pressure are not mutually exclusive and it is imperative to find a solution that satisfies all three in terms of the objective to achieve a throughput exceeding 1,000 units per hour (UPH). The following sub-sections detail the prior-art in improving assembly throughput through a) enhancing reactivity with innovations in low-temperature bonding technologies, b) achieving contact by accommodation of non-coplanarities, and c) developing high-speed assembly processes. Furthermore, novel emerging technologies that focus on high-throughput and reliability are detailed in the final section.

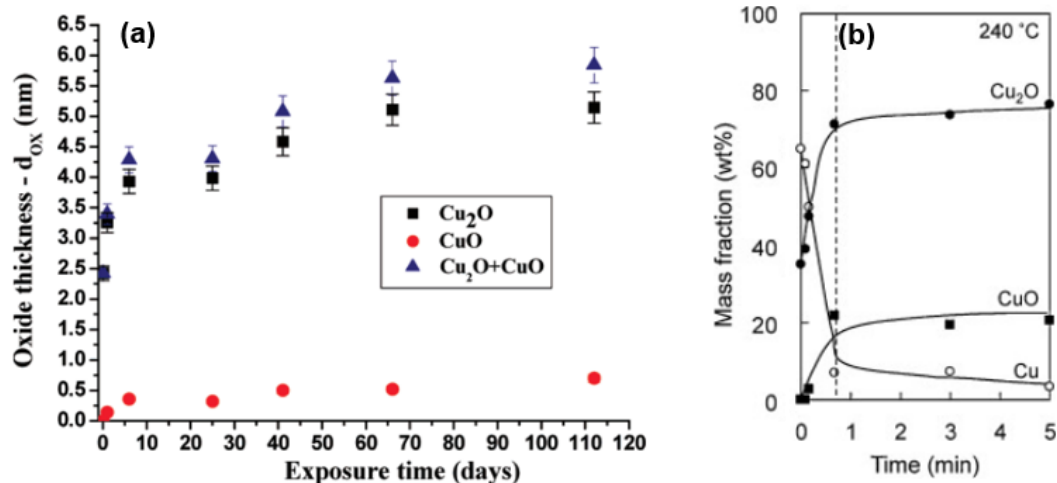


Figure 2.1 Oxidation of copper at (a) ambient temperature [20] and (b) at 240°C [21]

2.1.1 Improving interfacial reactivity

Reactivity of the mated Cu surfaces is a key parameter in forming strong bonds through grain growth and recrystallization within the thermal budget of the package-level assemblies. Since Cu is readily oxidized by O_2 and H_2O when exposed to air, Cu surface modification as well as passivation with organic layers, noble metal-capping layers and plasma-induced surface activation processes have been studied to protect Cu surfaces from oxidation and to improve the Cu–Cu bonding quality, thereby decreasing the time required to break oxide scales and improve assembly throughput.

2.1.1.1 Surface Modification

Diffusion of Cu under TCB conditions is also microstructure dependent. Because of a larger surface diffusivity on (111) plane than (100) or (110) planes, the energy barrier for Cu–Cu bonding can be reduced by using (111)-oriented Cu surfaces. C.M. Liu et. al. [22] showed Cu–Cu bonding using highly (111)-oriented nano-twinned Cu films under TCB at

150-200°C for 10-60 min. Figure 2.2 shown below presents a cross-sectional TEM image of such films bonded at 200°C – 30min with a void-free bonding interface. Room-temperature Cu-Cu bonding using (111)-oriented sputter-deposited Cu film has also been shown under ultra-high vacuum (UHV) condition on account of the rapid self-diffusion of Cu along the twinned (111) orientation.

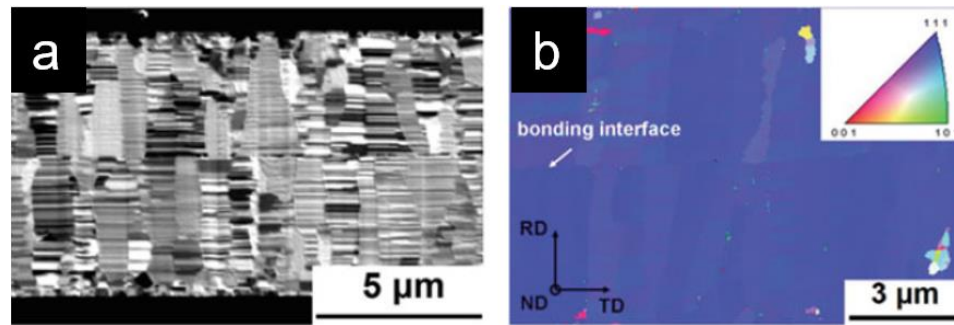


Figure 2.2 Bonding between two electroplated (111)-oriented Cu films at 200°C – 30min: (a) TEM cross-sectional image and (b) electron backscatter diffraction (EBSD) orientation image of the same

2.1.1.2 Organic passivation

Self-assembled monolayers (SAM) are used as temporary capping layers for passivating Cu film surfaces. SAMs of alkane-thiol have been studied by C.S. Tan et. al. [23-25] for Cu-Cu bonding at 250-300°C. Citric acid / microwave plasma cleaning is carried out before the SAM-adsorption process to clean Cu of surface oxide layers. The Thiol (-SH) head groups bind to the surface of Cu and form a densely-packed SAM cap while the methyl (-CH₃) group ensure hydrophobicity. This temporary organic film ‘sits’ for 3-5 days for complete coverage before it is desorbed with annealing at 250°C under inert or vacuum environment to expose the Cu surfaces. These exposed Cu surfaces are then bonded to form strong interfaces with shear strengths of 60 MPa. A schematic of this bonding technology is shown in Figure 2.3.

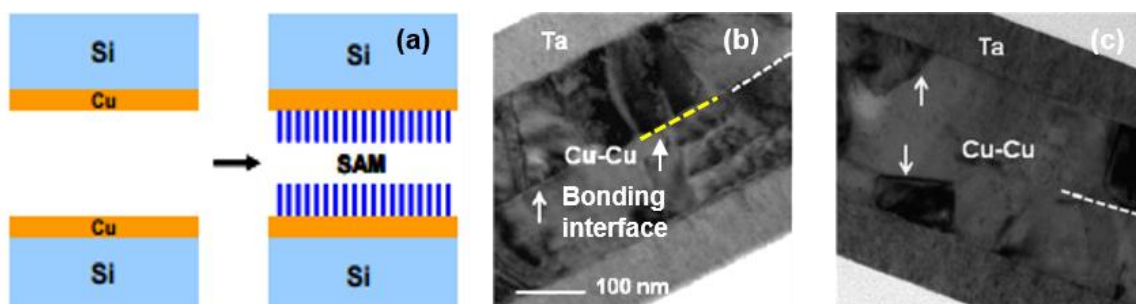


Figure 2.3 (a) A schematic of SAM capped Cu surfaces with SEM images (b) prior to desorption and (c) after bonding

2.1.1.3 Thin-film metal passivation

While SAM-enabled bonding does prevent oxidation of copper it requires time-consuming extra steps for complete coverage of SAM as well as a desorption stage under assembly conditions which lower the throughput of the process. Furthermore, the organic monolayers may not be compatible with the underfill material and could result in non-intentional voiding across the interface. Unlike SAMs that desorb before bonding, metal capping layers are present and involved in interfacial reaction during the bonding. Y.-P. Huang et al. studied Cu–Cu bonding by using sputtered ultra-thin Ti and Pd capping layers (<10nm) [26, 27]. Due to lower activation energy at the surface, Cu has a tendency to diffuse toward the bonding interface. In contrast, Ti(TiO_x) diffuses toward Si substrate [27]. This diffusion behavior results in a Ti(TiO_x)/Cu–Cu/Ti(TiO_x) bonded structure. Similar behavior was also found by using a Pd capping layer. Panigrahi et al. [28] also investigated the influence of the thickness of the Ti capping layers on passivation and bonding results. They demonstrated that a sputtered 3nm Ti capping layer is effective for passivation of Cu surface with small surface roughness and low TiO_x content [29] as shown in Figure 2.4(a). However, the bonding conditions are still very similar to that of direct Cu-Cu bonding with no tolerance to non-coplanarities. IMEC has also demonstrated a new technology involving

non-noble capping layers (e.g., electroless NiB and CoB) to passivate Cu surfaces and enable better bonding [30]. The boron in the non-noble capping layers fits into the spaces in the Ni or Co lattices and acts as an interstitial element thereby preventing oxidation of the Ni or Co present in the capping layer. Thus, CoB or NiB alloy with an atomic concentration percentage of B from 10 to 50% behaves as a noble metal for surface passivation but at a lower cost. Similarly, Georgia Tech – Packaging Research Center (GT-PRC) has demonstrated low-temperature chip-to-substrate Cu interconnections using thin-ENIG layers at temperature below 200°C using pre-applied underfill [31]. Figure 2.4 shows cross-sections of Ti-capped and ENIG-capped Cu-Cu bonding technologies. However, most of these capping technologies are expensive from the point of view of low throughput, cost-intensive sputter-based processes, high thermocompression bonding (TCB) force and thermal budget.

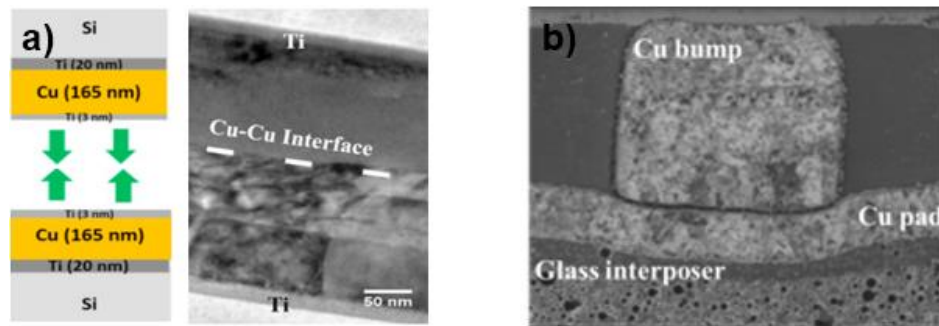


Figure 2.4 (a) Schematic and TEM cross-section of Cu-Cu bonding with 3nm Ti passivation layers and (b) Cu interconnections with ENIG surface finish on glass substrates

A metallic surface passivation that ensures protection of Cu from oxidation while providing soft metallurgical interfaces for low-temperature (<250°C) and high-speed assembly would be ideal to improve throughput.

2.1.1.4 Surface Activation

Surface contaminants such as adventitious organics and oxides are always present on the surface of copper during fabrication. It is imperative that these barriers to diffusion are removed to ensure unhindered interfacial diffusion. Surface-activated bonding (SAB) method is carried out by using a pre-bonding surface activation treatment under ultra-high vacuum (UHV) conditions. This method removes surface oxides and contaminants like organics by Ar⁺ ion beam bombardment under UHV conditions which prevents rapid re-oxidation and recontamination of surfaces prior to bonding [10, 32]. Figure 2.5 shows TEM cross-sections of a Cu-Cu bonded interface formed after SAB at room temperature under UHV conditions. Modified SAB-based diffusion bonding has also been demonstrated with dry-O₂ and humid N₂ environments at 150°C with void-free interfaces albeit with higher oxide content in the interfaces. While SAB is exceedingly effective in forming seamless interfaces, the application of UHV or plasma-induced pre-treatment limits its applicability to low-volume wafer-level packaging (WLP) and micro-electromechanical systems (MEMs) packaging.

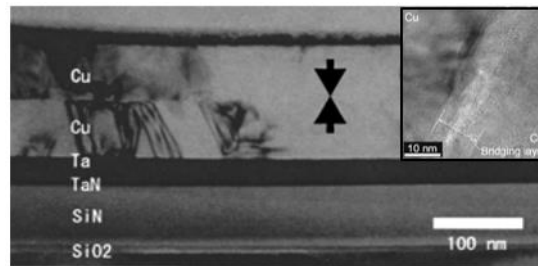


Figure 2.5 TEM image of Cu-Cu bonding by surface-activated bonding at room temperature; inset figure represents HRTEM image of Cu-Cu bonded interface

2.1.2 Achieving planar contact

Metallurgical bonding requires atomic level contact of the mated itnerfaces. However, non-coplanarities and asperities are introduced on the surfaces of Cu pillars / thin films during

various fabrication process steps. To create planar atomic contact during Cu-Cu bonding, these non-coplanarities need to be eliminated through either planarization processes or through extensive plastic deformation, to ensure recovery, recrystallization and grain growth occurs at the bonded interface. However, due to the high elastic modulus of Copper, the throughput of the assembly process is greatly reduced as significant energy is required to ensure a perfect contact. This also necessitates the introduction of a low-modulus compliant phase that can absorb the stresses under assembly and improve tolerance to non-coplanarities. In the sub-sections below, the current state-of-the-art in direct- Cu-Cu bonding to accommodation of non-coplanarities is discussed.

2.1.2.1 CMP-enabled hybrid bonding

Direct Cu-Cu bonding or Cu/dielectric hybrid bonding promises high-density vertical electrical interconnections with short lengths between stacked 3D-ICs or wafers [33, 34]. This technique involves bonding the Cu-Cu interfaces as well as the dielectric-passivated areas to enhance bond strength, heat dissipation and corrosion protection of Cu with seamless interfaces. One of the most common techniques in improving the Cu-Cu bonding strength is through chemical-mechanical polishing (CMP). CMP physically erodes and polishes the copper to an extremely low-roughness ($R_a \sim 0.5\text{nm}$) flat surface to improve contact in bonding. This improves contact and forms a seamless bond-line after thermal treatment due to ease of Cu diffusion across the interfaces. This concept is illustrated in Figure 2.6.

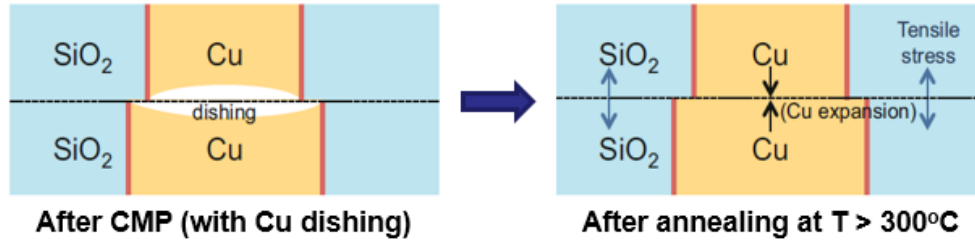


Figure 2.6 Schematic of non-thermocompression Cu/SiO₂ hybrid bonding

Direct Bond Interconnect (DBI) is a famous Cu/SiO₂ (or SiN_x) hybrid bonding technique developed by Ziptronix Inc [35], where, after surface activation processes (to activate Si-O and Si-NH₂ groups), wafers are contacted and bonded at room temperature without any applied pressure, followed by a post-bond anneal at 400°C. The bonding at ambient air helps form strong Si-O-Si / Si-N-Si bonds while high-temperature anneal form a strong Cu-Cu bond facilitated by internal compression induced by Cu thermal expansion [32, 36]. Furthermore, an optimized bonding process was developed by researchers at CEA-LETI with an additional CMP step to remove dished Cu surfaces to form ultra-smooth hydrophilic Cu and SiO₂ interfaces for hybrid oxide-oxide bonding [37, 38] as shown in Figure 2.7. T. Suga and co-authors [32] have also demonstrated improved bonding strength by the combination of Ar⁺ plasma-induced SAB with Cu/SiO₂ hybrid bonding under a 10⁻² Pa vacuum environment with a post-bonding anneal step at 200°C. However, voids at the Cu-Cu bonding interface have been found in each of the abovementioned technologies on account of Cu diffusion under high temperature post-anneal and high bonding time conditions leaving behind vacancies akin to Kirkendall voiding.

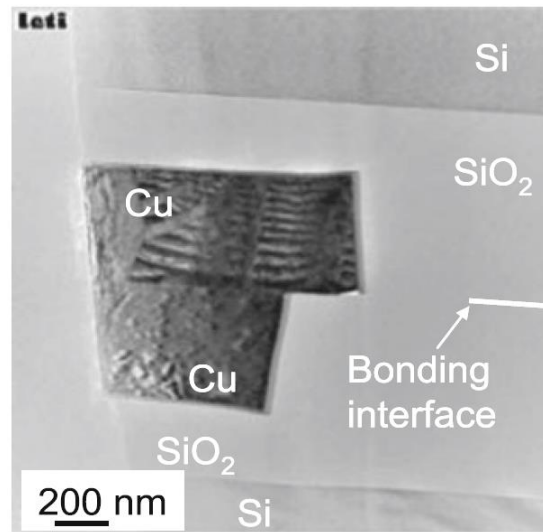


Figure 2.7 TEM image of the Cu–Cu bonded interface obtained by CMP treatment

2.1.2.2 Cu-Cu bonding with thermocompression assembly

The basis of Cu–Cu thermocompression bonding (TCB) is interdiffusion and self-diffusion at elevated temperatures and under an external compression force, which magnitude depends on the cleanliness of the mating Cu surfaces and potential presence of additional passivation or capping layers. Thermocompression bonding brings about significant plastic deformation at the mated interfaces, thus providing enough energy to break through the oxide scales and form a metallurgical bond. However, since there is application of high pressure along with significant time constraints in fine-pitch alignment, the throughput of conventional TCB assembly is very low (<1000 UPH) as compared to solder-based mass reflow technologies. Depending on the surface topology and roughness, a direct Cu-Cu TCB ‘diffusion’ bonding is carried out at a bonding pressure of 100-350MPa [11, 32, 39, 40] for as-plated Cu pillars/films and can also be <3MPa for W2W bonding with extremely low-roughness Cu films. The bonding is carried out at a high temperature of 300-400°C under a vacuum / inert gas environment followed by a post-bonding anneal step at 300-

400°C to improve the bond strength [8, 11, 14, 41-43]. In order to lower the bonding temperature, surface treatments such as wet chemical cleaning and gas/vapor-phase thermal treatments have been studied. Direct Cu-Cu bonding via thermocompression bonding at 175°C in forming gas ($H_2 + Ar$ or N_2) and reducing formic acid vapor ($HCOOH$) has been demonstrated with good quality bonding strength [43]. The H_2 molecules / H radicals chemisorb onto the native surface oxide layers, thus reducing them and enable Cu-Cu bonding without the need for a post-bonding anneal step.

Cu/adhesive hybrid bonding using polymer adhesives instead of SiO_2 has also been investigated for 3D integration. This type of bonding is generally ‘adhesive-first’, where the adhesive is TC-bonded and cured at low temperature (250°C for BCB) before a high-temperature Cu-Cu TCB at 350-400°C. TCB-based Cu/adhesive bonding using lock and key structures [44], benzocyclobutene (BCB) [36] and polybenzoxazole (PBO) prepared by CMP has been reported and an example of this bonding technique is shown in Figure 2.8. However, this method has limitations in terms of throughput of TCB as well as high thermal stresses on account of the high Cu-Cu bonding temperature.

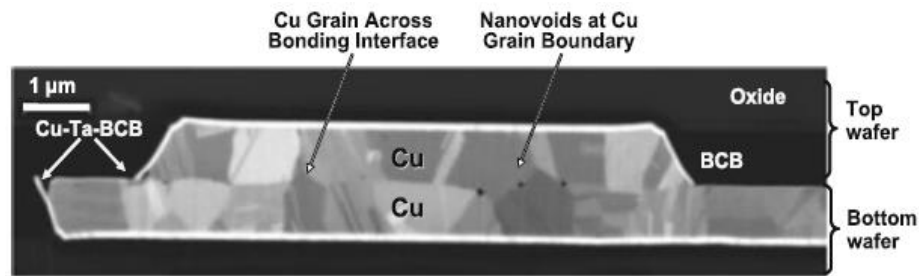


Figure 2.8 SEM cross-sectional image of Cu/BCB hybrid bonded structure

Cu-Cu insertion bonding is a fairly novel TCB approach for low-temperature bonding applied to copper through-Si vias (TSV) bonding structures. The method relies on applying

high shear stresses through TC-bonding on sloped sidewall landing pads (instead of a usual flat pad) to yield large plastic deformation when a Cu pillar is inserted into the sloped pads under high pressure (Figure 2.9). IMEC has demonstrated this process under bonding temperatures of 100°C to form seamless bond interfaces [45].

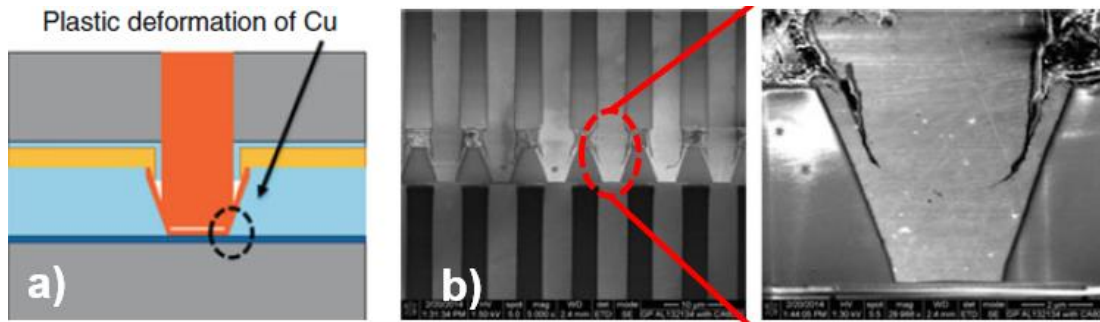


Figure 2.9 Cu-Cu insertion bonding: a) Schematic and b) X-section after 3D-stacking with TSVs

2.1.3 High-speed assembly

Currently, solder-based interconnections down to 80 μm pitch are assembled at a throughput exceeding 40,000 units per hour (UPH) using batch reflow processes. However, as the interconnection pitch shrinks further to 30 μm and below, thermocompression becomes necessary to manage warpage in assembly (due to CTE-mismatch), control the solder collapse and reaction, and achieve joint uniformity. This application of pressure requires complex and expensive capital investments as well as change in infrastructure and sequential assembly processes that further reduce the throughput and increase assembly time considerably. Pitch scaling and corresponding reduction of die-to-substrate gap to below 50 μm also introduces difficulties in flux cleaning and capillary underfilling. While recent research efforts have been made towards the use of plasma-assisted dry soldering to

address the flux residue problem [46], capillary underfill (CUF) is fundamentally limiting by extended filling times with reduced gap and increased package sizes. This filling time is given by equation 1:

$$t = \frac{3\eta L^2}{h\gamma \cos \theta} \quad (1)$$

where η is the underfill's viscosity, γ is the surface tension, θ is the contact angle, h is the die-to-substrate gap, and L is the package size. In addition, to maintain a maximum solder volume, pitch scaling is aggressively driving reduction of the interconnection gaps, causing slower meniscus velocity of the underfill [47]. Recently, the use of pre-applied underfills was proposed [3] as an effective solution to control solder spread and relieve strains in the solders from the formation of the joints, while combining assembly and underfill processes to improve throughput. The use of thermocompression using no-flow non-conductive pastes (TC-NCP), first developed in 1996 [48], with self-fluxing and snap-cure capabilities is one such process where uniform solder joints are formed under a bonding pressure of 40-90MPa for about 7sec at a joint temperature of 250°C. This has considerably increased the throughput to ~1,000 UPH. Further optimization of the assembly tooling with rapid heating and cooling rates (400K/s) has increased the throughput of solder-based TC-NCF (non-conductive film) bonded interconnections to 1,500 UPH. However, the TC-NCF technology is still quite nascent and faces challenges of: (a) voiding through film lamination, (b) degradation of film under dicing' (c) post-bond voiding due to over-cure shrinkage [49] etc. However, a compromise has to be found between performance and cost, as the throughput of thermocompression processes is inherently limited by their serial nature in opposition to batch reflow. Alternatively, Amkor [50] have demonstrated that

gang-bonding of at least 8 dies in parallel with a TC-NCF process (non-conductive film) can compete with the cost of mass-reflow processes through increasing the size of the gang-bond head and bonding time optimization (Figure 2.10(a)). Recently, Cu-Cu bonding for CoW 2.5D integration was demonstrated using a 2-step gang-bonding process where (a) the chips were first diced and populated onto the substrate wafer using a tacky underfill, and (b) in the second step, the chips were gang-bonded under formic acid to form joints, as shown in Figure 2.10(b).

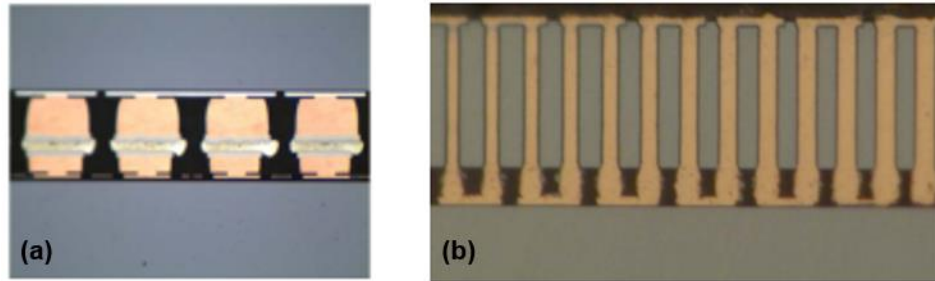


Figure 2.10 Gang bonding of (a) Cu pillar interconnections at 30um pitch [51] and (b) Cu-Cu interconnections at 6um pitch for CoW 2.5D integration [52, 53]

In addition, the laser-assisted bonding (LAB) in replacement of direct heating of TC-bonding was recently introduced by Amkor to improve throughput. A specialized near infrared (IR) laser was implemented to heat the Si die with high directionality, uniformity and selectivity. This caused localized heating and melting of the solder leading to bond formation. It has been confirmed that the bonding time could be shortened to 1-2s, while all the benefits granted from localized heating are kept [54]. Another potential technology to improve the throughput of assembly is ultrasonic or thermosonic (heat-assisted) bonding. This technology has been used quite extensively in wire-bonding assembly modules and is currently being applied to the flipchip packaging world. Under the action of ultrasonic vibrations, localized high energy cavitation bubbles are created which can

melt solder in a fraction of a second and cause metallurgical bonding. As compared to TC-bonding which can form a 1 μ m thick Cu/Sn intermetallic (IMC) layer in 10seconds, an IMC thickness of 10 μ m has been demonstrated using ultrasonic bonding [55], significantly reducing the cycle time. However, the scalability of these technologies for HVM adoption is still questionable.

While the throughput of fine-pitch solder-based interconnections has been improving through process innovations and novel bonding techniques, it is evident that no such high-speed bonding technology exists for direct-Cu-Cu bonded interconnections for chip-to-substrate applications with CTE-mismatch.

2.1.4 Nano-sintering at low-temperature

All applications seem to converge toward nanomaterials acting as a key enabler to achieve strong, reliable joints with high current-carrying capability and thermal stability at low bonding temperatures. Nanoscale materials can be sintered at lower temperatures and pressures due to their large surface energy to form joints by solid-state diffusion, typically at temperatures and pressures of 250°C and in the 1-5MPa range, respectively [56-58]. The following sections highlight nanoparticle-based and nanofoam-based systems for high-throughput assembly.

2.1.4.1 Fundamentals of nano-sintering

In order to understand the intertwined processes of densification and grain growth, we turn to the fundamentals of sintering, and examine whether the same principles and rules that

govern sintering micron-sized particles apply to nano-sized particles. The thermodynamic driving force σ for sintering can be expressed using the following equation:

$$\sigma = \gamma\kappa = \gamma\left(\frac{1}{R_1} - \frac{1}{R_2}\right) \quad (2)$$

where γ is specific surface energy, κ is curvature, and R_1 and R_2 are the principle radii of curvature of a particle surface. It can easily be shown that the driving force for sintering would be two magnitudes higher when the particle size is decreased from 1,000 nm to 10 nm, which enhances the sinterability of nanopowders. In addition, it has also been shown that the specific surface energy γ increases with decreasing particle size in the nanometer scale [59], which further contributes to enhance the sinterability of nanopowders. The particle size also plays a role when considering lowering the sintering temperature in the attempt to reduce grain growth, since melting point is a function of particle size, as given by,

$$\sigma T_m(d) = T_m(\infty) \exp\left(\frac{-S_m(\infty)}{3R} \frac{1}{(d/d_0 - 1)}\right) \quad (3)$$

where $T_m(\infty)$ is the bulk melting temperature; $S_m(\infty)$ is bulk melting entropy; R is the gas constant; d is particle diameter; d_0 is the minimum particle diameter at which all atoms locate on the surface. Along with a decrease in melting temperature, there is also a concurrent decrease in the temperature at which these high-surface area materials sinter, thus requiring lower assembly temperatures to convert into bulk-phase.

The kinetics of sintering are enhanced due to the presence of curvature and can occur through a host of pathways as outlined in Figure 2.11. Thus, by optimizing the

particle size, density as well as the thermal conditions, it is possible to reduce the sintering time and improve throughput of this process. Furthermore, it is possible to achieve low elastic modulus properties akin to that of solders in pre-sintered nanomaterial compacts on account of their inherent porosities. However, a key drawback under sintering conditions is agglomeration of nanomaterials and retention of these porosities after conversion to bulk material, which could be detrimental to the electrical, thermal and reliability characteristics of the interconnections. Therefore, carefully optimized morphologies and assembly protocol is required, along with additional steps to realize oxide-free homogeneous nanomaterials. The following sections go into the details of nano-material based interconnections technologies.

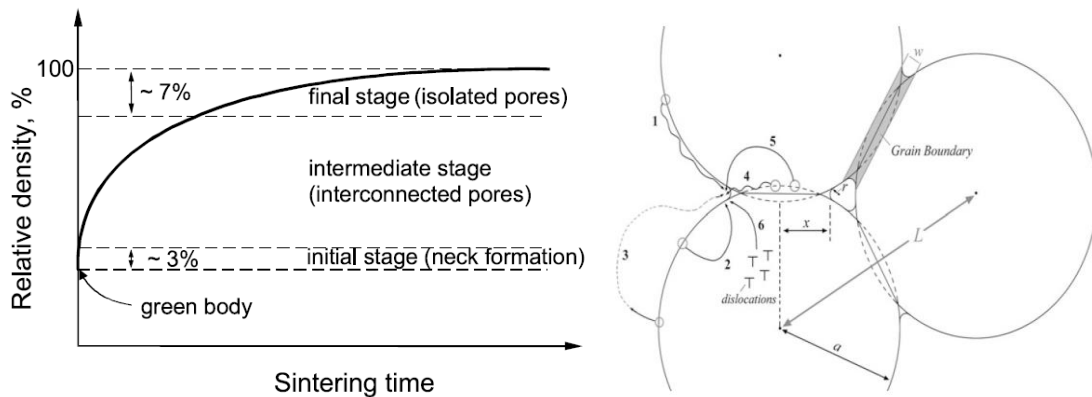


Figure 2.11 Illustration of the sintering mechanisms in a three particles array. The numbers represent the different mechanisms and sources of material. (1) from surface by surface diffusion; (2) from surface by bulk diffusion; (3) from surface by evaporation/condensation; (4) from grain boundary by boundary diffusion; (5) from grain boundary by bulk diffusion; (6) from bulk by bulk-diffusion (through dislocations)

2.1.4.2 Nano-Cu ink based sintering

While most of the above bonding technologies are for wafer-level packaging (WLP) only, IBM Zurich recently demonstrated chip-to-substrate Cu-interconnections dipped in nano-

Cu inks through capillary bridging of nano-Cu particles under evaporation to form interconnected necks [17]. This resulted in the formation of highly porous necked Cu interconnections with elastic modulus an order of magnitude lower than that of electroplated bulk Cu. An example of such joints is shown in Figure 2.12. Presently, low resistance (1.2 m Ω) dip-based Cu interconnections were obtained under a bonding pressure of 50MPa at 200°C with compatibility with standard ENIG and ENEPIG surface finishes applied on substrate pads [60]. However, these interconnections also face a major challenge of limited pitch scalability due to risks of bridging, as well as low shear strengths because of retained porosity from non-uniform densification.

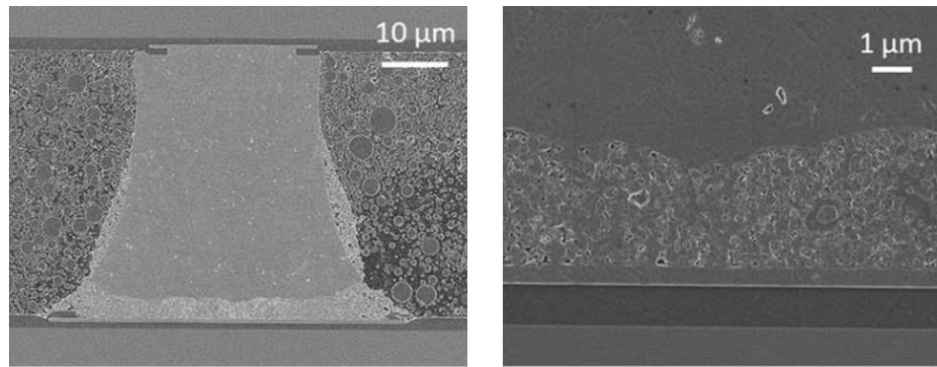


Figure 2.12 SEM cross-section of all-Cu interconnection formed by capillary bridging under TC bonding at 76MPa – 160°C with a high-magnification image of the bonded interface

2.1.4.3 Nanoparticle-based paste sintering

Nanoparticles of Cu, Ag and Au with radii below 100nm show depression in their sintering temperatures and can be used for low-temperature (<250°C) assembly. These nanoparticles are generally in the form of pastes with an organic binder component that ensures homogeneity and stability with respect to oxidation and shelf-life. On heating these pastes to 250°C, the organics get evaporated, leaving behind reactive nanoparticles that

fuse together, form necks and undergo coarsening and densification. The resulting sintered joints have relatively good thermal and electrical conductivities as well as high-temperature stability. For instance, commercial Ag nanopastes can be sintered at as low as 250°C [56, 58, 61, 62]. Copper has comparable electrical, thermal and mechanical properties than silver, and is relatively inexpensive which makes it an ideal candidate (Figure 2.13(a)). Although nano-Cu sintering pastes are actively being developed, with, for instance, Lockheed Martin’s “reflowable” Cu paste (Figure 2.13(b)) at 200°C [63], they have not reached an acceptable cost point due to the expensive surface treatments required to prevent oxidation of Cu particles at micro- and nano-scales. Further, Cu-sintered joints inherently suffer from the same drawbacks as their Ag counterpart: 1) retained porosity after densification and 2) inherent stiffness hindering scalability to large die sizes. No resin-assisted Cu sintering process has been proposed to date to address microstructure stability, nor stress management.

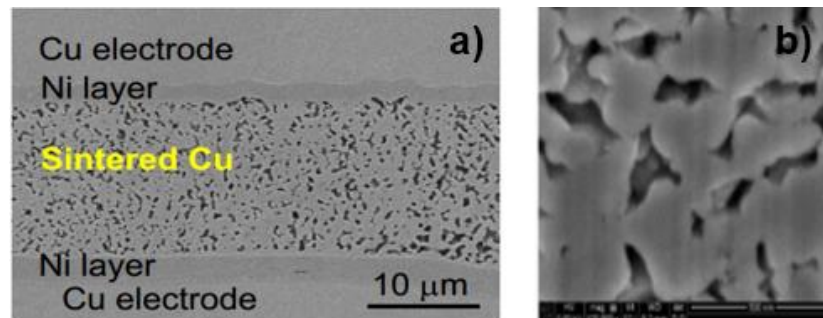


Figure 2.13 Nano-Cu paste systems from a) Hitachi Ltd. and b) Lockheed Martin [63]

2.1.4.4 Nanofoam sintering

Metal nanofoams can be thought of as sponge-like materials with nanoscale feature sizes, and, therefore, can also be sintered at low temperatures [64]. In addition, they have the

following advantages over sintering of nanopastes: 1) low-cost synthesis, compatible with standard lithography processes; 2) high design flexibility to control bondline thickness and final microstructure; 3) absence of organic additives, minimizing risks of voiding due to volatiles; 4) sub-20GPa modulus pre-sintering to compensate for lack of wettability [65]. A representative image of a metal nanofoam and its constitutional cellular model with ligaments and nodes is shown in Figure 2.14(a). While metal nanofoams are a relatively new class of materials, their use as interconnections is recently being explored. Ag nanofoam was proposed as a new high-temperature die-attach technology [66], while Au and Cu nanofoams were demonstrated for direct Au-Au [64, 67] and Cu-Cu bonding [68-70] for 3D packaging respectively (Figure 2.14(b-d)).

Chemical dealloying is the most commonly used method to synthesize metal nanofoams. An initial alloy system having two or more elements is synthesized, and then selectively etched of one or more reactive element(s). During that step, the remaining nobler element self-assembles itself into a 3D interconnected network of nanoscale ligaments and pores [71]. This condition imposes restrictions on the choice of alloying elements available for Cu, since Cu itself is quite reactive. Most commonly used alloying elements are Zn, Mn, Al, Ti and Si [70-76].

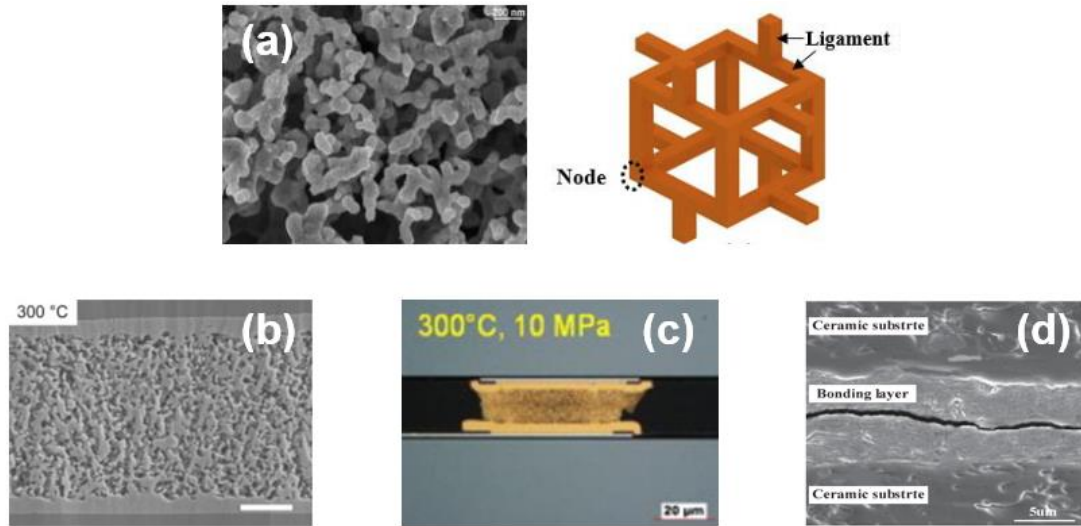


Figure 2.14 (a) Ni nanofoam with a cellular open-cell model from [77] representing metal nanofoams; (b) nanoporous Ag-sheet bonding at 300°C; (c) Au-Au nanoporous interconnection; and (d) nanoporous Cu interconnection after TCB at 20MPa – 250°C – 2hours

The initial alloy can be synthesized in sheets or ribbons, or build on wafer or substrate using different techniques: 1) arc or furnace melting 2) electrodeposition 3) sputtering [68, 75, 78-82]. These alloy sheets can then be dealloyed to fabricate film or patterned Cu nanofoam. The working model for porosity evolution during dealloying was introduced by [83] about 16 years ago, and has been further modified through kinematic Monte-Carlo simulations (KMC) and other numerical solutions of the interface evolution [84]. A key requirement of dealloying is that there should be a significant electrochemical potential difference between the phases in the initial binary/ternary alloy system. Under the action of a suitable etchant above a composition-defined critical electrochemical potential V_c , selective solvation and dissolution of the more reactive elements takes place from the alloy surfaces sites. The more noble element atoms tend to diffuse to these surface sites via an uphill diffusion (low-concentration to high-concentration area), thus passivating them. This dissolution of the more reactive elements further proceeds from the base of these sites

downwards giving undercutting and bifurcation of pores. This apparent increase in surface area further provides the driving force for the dealloying front to proceed deeper into the bulk of the alloy and gives rise to a three-dimensional network of connected ligaments and pores. A schematic of the perceived dealloying mechanism is given in Figure 2.15.

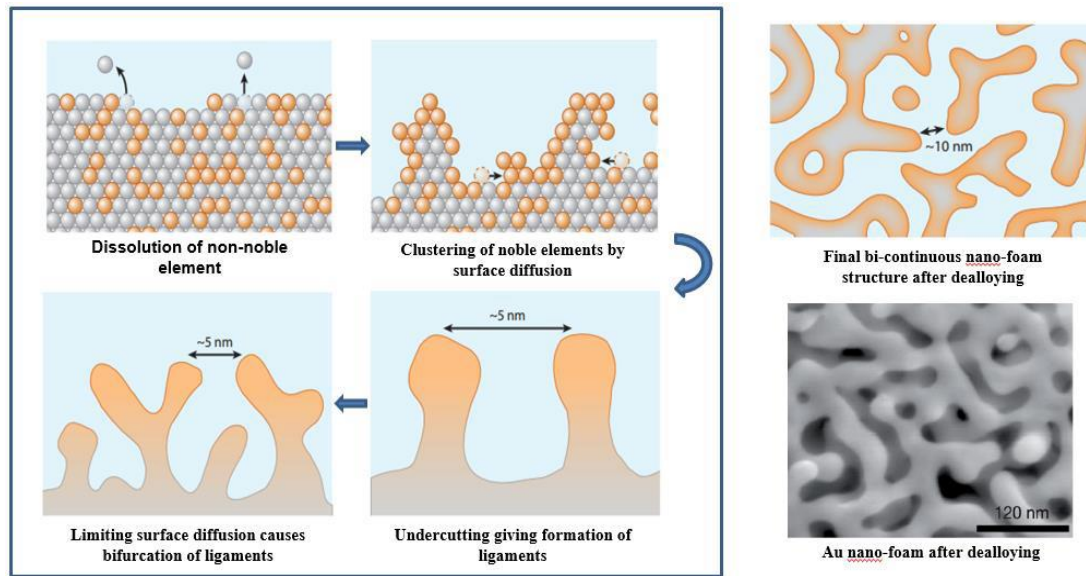


Figure 2.15 Schematic of dealloying process at the atomic scale

Dealloying processes can be classified as either free dealloying in which the alloy is simply immersed in the etchant or electrochemical dealloying where an additional external potential is also applied [73, 85-89]. Longer passive dealloying duration results in coarsening of ligaments and non-uniform morphology. Alternatively, electrochemical dealloying, due to the additional driving force, can reduce the dealloying time by an order of magnitude, resulting in finer ligament and pore sizes as well as providing uniform control over the evolution of the nanofoam morphology [74, 90]. Pre-dealloying parameters such as alloy composition and phase formation as well as dealloying conditions such as electrolyte chemistry, time and temperature play an important role in governing the subsequent structure and morphology of the synthesized nanocopper foams.

2.2 Reliability in chip-package architecture

2.2.1 Failure modes in Cu pillar flip-chip packages

The most common packaging architectures have a large thermal expansion (CTE)-mismatch between the stiff Si die (3ppm/K) and organic substrates (17ppm/K). This CTE-mismatch can cause challenges of warpage and failures under operating conditions. Solder-based interconnections can accommodate this CTE-mismatch on account of the high plasticity of solders due to their low modulus and low melting point (T_m). However, due to their low melting point, this plastic strain accumulates under continuous operation at $0.3T_m$ and can cause creep-enabled fatigue failures and cracks within the solder thus causing open failures. An example of this process of crack propagation and eventual failure is shown in Figure 2.16 [91]. There are two major components to fatigue failures/ fractures: the initiation of fatigue cracks and the propagation of these cracks under cyclic loading. The direction of crack propagation is generally orthogonal to the direction of the principal stress. The Coffin-Manson fatigue model, based on plastic strain, is perhaps the best known and most widely used approach today. The total number of cycles to failure, N_f , is depicted as being dependent on the plastic strain amplitude, $\Delta\epsilon_p$, the fatigue ductility coefficient, ϵ'_f , and the fatigue ductility exponent, c . The relationship among these variables is shown as follows:

$$\frac{\Delta\epsilon_p}{2} = \epsilon'_f (2N_f)^c \quad (4)$$

Here, the fatigue ductility coefficient, ϵ'_f , is approximately equal to the true fracture ductility, ϵ_f while the fatigue ductility exponent, c , varies between -0.5 and -0.7 for most metals. Further improvement to the prediction of solder fatigue was provided by

Engelmaier who assumed that the in-plane (shear) steady-state strains dominated low-cycle fatigue behavior, given by,

$$N_f = \frac{1}{2} \left[\frac{\Delta\gamma_t}{2\varepsilon'_f} \right]^{\frac{1}{c}} \quad (5)$$

Where, $c = -0.442 - 6 \times 10^{-4} T_s + 1.74 \times 10^{-2} \ln(1 + f)$. Here, T_s is the mean cyclic solder joint temperature in °C, and f is the cyclic frequency in cycles/day.

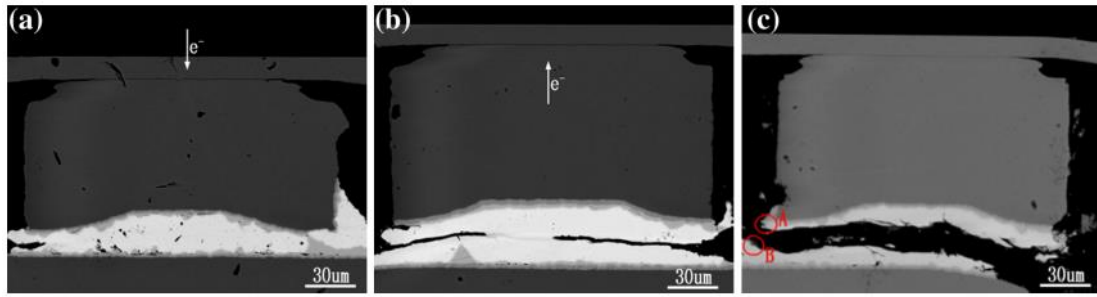


Figure 2.16 Fatigue failure in Cu pillar interconnections under coupled thermal cycling and current stressing with (a) crack initiation; (b) crack extension; and (c) open failure

2.2.2 Reliability challenges in stiff-interconnections

With pitch scaling to 30µm and below, there is also a significant reduction in solder volume, which causes loss of mechanical compliance from the conventional Cu-solder micro-bump. This can cause detrimental stress release in the ultra-low-K (ULK) dielectric layers within the back-end-of-line (BEOL) layers on the Si die, resulting in delamination. Such failures have been demonstrated during assembly of stiff SLID bonded interconnections where the brittle intermetallic layers transfer the stress upwards to the low-K layers on the die causing delamination. Furthermore, in the case of stiff solid-state interconnections, with high melting points as in the case of copper, the strain accumulation occurs in the elastic strain range and the stress is almost completely transferred to the ULK

dielectric layers causing delamination via shear. Similarly, thermocompression bonding with high bonding load can generally lead to high plastic deformation and stress within the interconnected system and can lead to a shift in the failure mode to these stress-sensitive ULK layers beneath the Cu μ -bumps. Normally, these joints fail right after assembly. As a result, there is a need to protect these ULK layers during assembly along with a fundamental understanding of chip-package thermomechanical interactions (CPI). Recently, pre-applied underfill materials such as NCP and NCF have been developed to combat this shift in failure mode. These pre-applied materials cure during thermocompression assembly and apply compressive stresses on the ULK layers to prevent crack propagation.

In the TC-NCP process, a temperature gradient is built between bonding heat and stage that enables the substrate to remain at lower temperature while reaching the melting point of solder. Thus, the stress or strain induced by mismatch in coefficients of thermal expansion (CTE) between silicon and high-density substrates, in particular laminates, can be significantly reduced. Global Foundries recently reported that the normal stress built in ULK layers could be reduced by approximately 85% with TC-NCP assembly as opposed to mass reflow [18], as showed in Figure 2.17(a). In 2016, Shinko also found that the plastic strain in solder could be reduced by 25-30% as comparing to mass reflow, as showed in Figure 2.17(b) [92]. Through optimization of the force and thermal profiles, stage temperature and NCP material, post-assembly warpage can be finely controlled and minimized by managing the timing of coupling die and substrate [93]. Improved yield and reliability were consequently demonstrated with TC-NCP through unbiased highly accelerated stress test (uHAST), temperature cycling, and high-temperature storage (HTS)

[18, 94]. The direct challenge here is to apply such a pre-applied underfill material to direct Cu-Cu bonding for chip-to-substrate applications to improve the reliability and stress distribution across the interconnection.

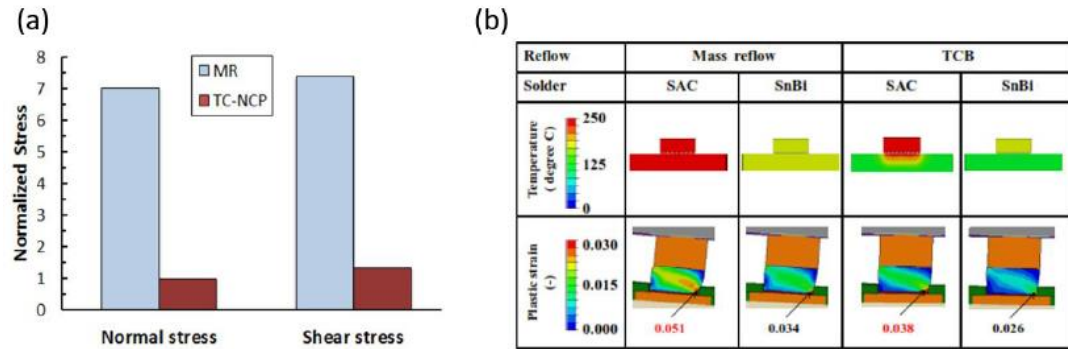


Figure 2.17 (a) Reduced stress in ULK-layer, and (b) reduced plastic strain in solder, benefited from thermocompression bonding

In summary, a comprehensive study of the current state-of-the-art in Cu-Cu bonding has been carried out keeping in mind the fundamental challenges of high-throughput assembly and reliability in chip-to-package architectures. Novel surface-modified direct Cu bonding technologies tackling the challenges of low-temperature bonding were discussed. To overcome the low tolerance to non-coplanarities, pressure-less and TCB hybrid bonding techniques were detailed. A current outlook on high-speed assembly processes was detailed and novel nanomaterials-based bonding technologies were introduced with an emphasis on low-modulus, highly reactive materials that can solve both the challenges simultaneously. In the end, an outlook of reliability has been illustrated with focus on TC-NCP based processes to improve reliability of fine-pitch interconnections. The following sections will discuss the preliminary results towards meeting the objectives.

CHAPTER 3. CU INTERCONNECTIONS WITH METALLIC COATINGS

The primary objectives of this chapter are to develop a methodology for designing reactive bimetallic interfaces for improved assembly throughput and reliability, followed by assembly demonstration and characterization of Copper interconnections with the designed ultra-thin metallic coatings. Sections 3.1 and 3.2 discuss the diffusion behavior and deformation behavior under thermocompression of Cu interconnections with novel electroless Pd – autocatalytic Au (EPAG) finishes. Section 3.3 describes the design and fabrication process flow of the test vehicles used in this thesis down to 50 μ m I/O pitch. Finally, section 3.4 focuses on the experimental validation of the design methodology as well as the design and demonstration of a high-speed TC-NCP process.

3.1 Materials Design

3.1.1 Design Methodology

To design Cu interconnections meeting aforementioned research objectives, novel metallic coatings are required that satisfy the following constraints of assembly manufacturing:

3.1.1.1 Material design before assembly

It is well known that copper oxidizes in ambient conditions to form native surface oxides that degrade its thermal, electrical and metallurgical properties. To achieve oxide-free bonding interfaces, a noble metal coating is subsequently required around the Cu bumps. Post Cu-bumping steps like deposition of a noble layer are generally considered ‘post-

processing' in a typical wafer fabrication cycle and are required to be fairly low cost and with the minimum number of process steps. Similarly, the Cu pads on substrate also require application of the noble metallic layer to prevent oxidation of Cu on substrate side. Since solid-state interconnections are typically stiffer than solders, the use of pre-applied underfills in assembly is generally recommended to protect the fragile ICs by creating compressive stresses that effectively prevent crack propagation in the low-K on-chip dielectric layers. This requires a conformal coating of the noble metallic layers around the Cu pillars and pads to prevent sidewall oxidation of Cu during assembly and improve adhesion of the Cu – underfill interfaces. Since electrolytic deposition does not give conformal coatings, there is a need to use novel electroless-, immersion- or autocatalytic-based processes to form conformal metallic coatings. Finally, the wafers and substrate panels are required to have a high shelf-life between fabrication and assembly. This can be achieved by preventing room-temperature diffusion of Cu to the surface of the metallic coatings in ambient conditions.

3.1.1.2 Material design during assembly:

In assembly, we require material systems that have a high interdiffusivity rate at temperatures below 250°C to form void-free, stable metallurgical interfaces after assembly. Since assembly is cost sensitive, and, therefore, ideally a high-throughput process, it is also required that metallurgical bonding across the interfaces is achieved in a short time, implying fast reaction kinetics. To ensure fast reaction kinetics, the coating film thickness should be nanoscale to ensure rapid diffusion along the large network of grain boundaries in the nanocrystalline films. During fabrication, copper electrodeposition processes can introduce statistical variations in heights and surface roughness of Cu bumps and pads, thus

forming micron-scale non-coplanarities within a single 200/300mm wafer due the micro-etch and electrodeposition processes. Such asperities and hillocks can cause non-uniform contact between two mated surfaces under thermocompression, thus forming voids at the bonded interfaces. As a result, significant bonding pressures inducing plastic deformation and subsequent bump collapse or additional surface planarization steps like CMP are required to create contact between the mated surfaces, all within the process design box of lowest bonding pressures that give seamless bonding interfaces.

3.1.1.3 Materials design after assembly

The bonded interfaces so formed are required to be stable under operating conditions. This involves exposure to possible high currents causing current crowding and electromigration risks, thermal shock due to varying operating temperatures as well as humidity, all of which fatigue and degrade the bonded interfaces and reduce reliability. To ensure formation of robust interfaces that do not fail over the lifetime of the device, it is required to consider standard reliability testing such as thermal stability and accelerated electromigration tests to qualify this technology for product implementation. This detailed design methodology has been illustrated in Figure 3.1. The following sections go into the details of each of the design phases.

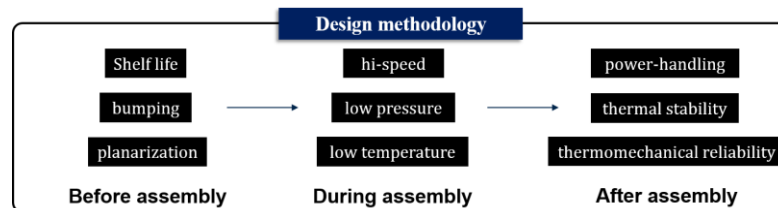


Figure 3.1 Materials design methodology

3.1.2 *Design before assembly*

Based on the manufacturability objectives mentioned above, a novel interconnection system was conceptualized with the following metal layers:

3.1.2.1 Noble bonding interface:

Gold (Au) was chosen as the noble bonding interface on account of its oxidation resistance, softer elastic modulus (70GPa) and lower yield strength as compared to Cu giving easy plastic deformation as well as a higher diffusivity than Copper at $T < 250^{\circ}\text{C}$. Gold (Au) can be deposited using either electroplating, electroless plating or stud bumping at pitches as low as $50\mu\text{m}$ [95]. Au-stud bumps and Au-Au interconnections (GGI) have been demonstrated using ultrasonic and thermocompression bonding at bump pitches as low as $20\mu\text{m}$ [96-98]. However, despite their outstanding electrical, thermal, and reliability performance, GGIs are not extensively used in high-volume manufacturing (HVM) due to the prohibitive cost of Au. Nevertheless, thin-film deposition of Au can be cost-effective as well as provide the soft interfaces required to mitigate effects of surface roughness. There are, however, some processing concerns with the direct deposition of Au on Cu pillars. Since we require conformal films around the Cu, direct immersion gold (DIG) surface finish is a good option for film thicknesses $< 50\text{nm}$ without the performance being compromised by skin effect [99]. However, the control of plating thickness is unstable, leading to over-plating and non-uniform thin-film thicknesses. To overcome these challenges, other innovative techniques like autocatalytic and electroless deposition processes are considered in this work for easily processable and cost-effective deposition of Au on Cu. This leads us to the requirement of another interfacial layer between Cu and Au to enable deposition of Au and prevent conformal oxidation of copper.

3.1.2.2 Reactive layer:

The metallic interlayer between Cu and Au should be easily processable for Au deposition and can act as either: i) diffusion barrier to prevent migration of Cu atoms and isolate Au-Au interfaces for bonding or ii) dissolvable layer under bonding temperatures leading to interdiffusion between Au and Cu and leading to the formation of Au-Cu intermetallics. The Au-Cu system forms 3 intermetallic compounds (IMCs): Cu_3Au , Au_3Cu and the stable CuAu (50 atomic % each) [100]. More importantly, these IMCs are ductile phases with the ability to accommodate large amounts of plastic strain despite being ultra-thin. Thus, the interfaces that form are not brittle and can improve the longevity of the interconnections. Thus, we end up in an interconnection system with 2 options: either have a diffusion barrier layer (Cu-X-Au) or have a sacrificial layer that extends the shelf-life of Cu in ambient conditions, but dissolves (diffuses rapidly) under assembly temperatures ($<250^\circ\text{C}$) to form an IMC (Au-Cu) layer. The chosen configuration of stack-up should also satisfy the reliability testing conditions after assembly.

Now, Au is a common surface metallurgy that is routinely applied on a panel-level in substrate manufacturing. Since Au can only interact with and be deposited on a limited number of metals, we have to choose the interlayer within the scope of existing materials like Ni and Pd. Nickel-based metallic finishes such as electroless Ni immersion Au (ENIG) and electroless-Ni(P) electroless-Pd immersion Au (ENEPIG) are today industry's technologies of choice, owing to their superior properties such as ideal solder wettability, excellent joint strength and reliability performance [101, 102]. Also, $3\text{-}5\mu\text{m}$ Ni(P) is an excellent barrier layer to Cu-Au interdiffusion, thus is the element of choice for the interlayer which acts as a diffusion barrier. In addition to standard ENIG, a novel electroless palladium – autocatalytic gold (EPAG) surface finish, recently developed by

Atotech GmbH, allows electroless deposition of 50-200nm of Pd directly on Cu, followed by deposition of 40-400nm thick Au layers via an autocatalytic process. This Ni-free surface finish has been shown to be particularly suited for high-performance applications, with high-density routing at sub-10 μ m interconnect pitches, thus meeting the needs of ultra-fine pitch architectures without bridging concerns [103]. Furthermore, a thin Pd layer (<100nm thick) can easily dissolve and diffuse into the Cu pillar under assembly temperatures and result in the outwards migration of Cu into Au and formation of Au-Cu intermetallic phases [104, 105]. Since Ni and Pd satisfy the requirements of either a diffusion barrier preventing Cu diffusion and a dissolvable layer allowing IMC formation respectively, as well as satisfying the requirement of easy processability with respect to Au deposition, Ni/Au and Pd/Au-based ENIG and EPAG surface finish layers were considered in this study, as shown schematically in Figure 3.2.

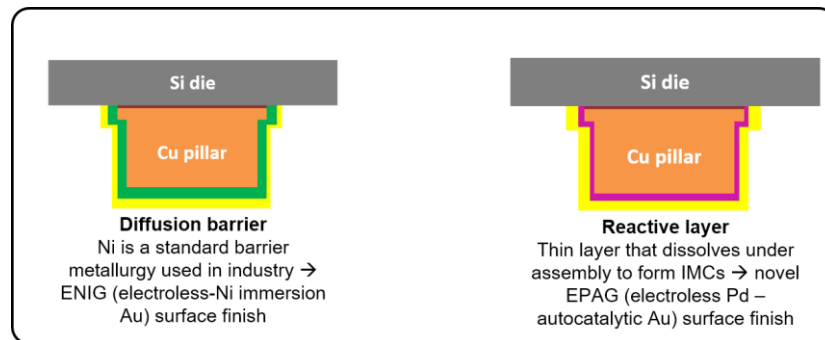


Figure 3.2 Schematic of Cu interconnections with Au-based bimetallic thinfilm coatings

3.1.2.3 Preventing oxidation pre-assembly

Since Cu is so easily prone to oxidation even under ambient conditions, it is imperative to ensure that the design of the Cu-Ni/Pd-Au layers prevent diffusion of Cu to the surface of the Cu bumps and pads at 25°C. Towards this, an analytical model was setup between Cu/Ni, Cu/Pd and Cu/Au metallic couples to understand their interdiffusion characteristics.

The model determined the time required for Cu atoms to diffuse to the surface of the diffusion barrier and increase surface concentration by 1 atomic %. The following assumptions were considered for analyzing ideal microstructures: (i) grain-boundary diffusion coefficients at 25°C are considered for Cu/Pd and Cu/Au binary couples due to their thin-film nature, while volume diffusion is considered for Cu/Ni couple; (ii) the microstructure of the layers consists of columnar grains separated by grain boundaries oriented perpendicular to the film surface/interface; (iii) diffusion can be described by time and position, while being independent of grain-boundary diffusion coefficients. (iv) a semi-infinite layer of copper is considered, coupled to a finite layer of the surface finish; and (v) 1-D diffusion flux is considered omitting the effect of lateral diffusion fluxes from adjacent grain boundaries. These assumptions are shown in Figure 3.3 and the semi-infinite equation is given by:

$$C = \frac{C_0}{2} \left(\operatorname{erfc}\left(\frac{2l-x}{2\sqrt{Dt}}\right) + \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \right) \quad (6)$$

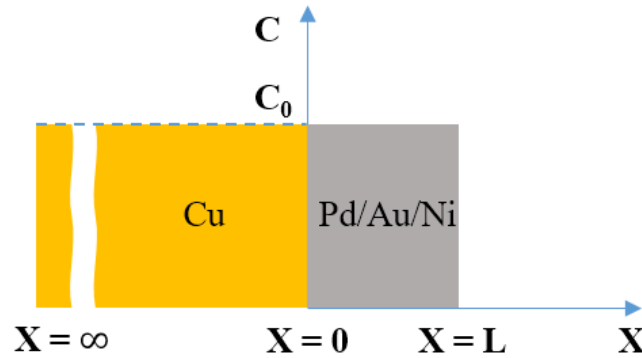


Figure 3.3 Schematic of diffusion model

Where C represents the concentration of Cu atoms across the binary couple, C_0 represents the bulk-concentration of Cu normalized to 1, l is the total thickness of the metallic coating, D is the diffusion coefficient, t is the time, and x is the displacement variable for the

concentration of Cu atoms. After sufficient optimization, it was shown that 3 μ m of Ni and 250nm of Au are enough to inhibit the surface diffusion of Cu for a reasonable shelf-life at 25°C. While Cu and Ni form a solid solution and have comparable sizes, the Ni layer is invariant to Cu diffusion under homologous temperatures ($T/T_M < 0.5$), giving a shelf-life that vastly outnumbers the device lifetime. A lower thickness of Ni can also act as an effective diffusion barrier to Cu migration. However, there are manufacturability concerns with issues of black-pad (Cu corrosion) from thin-Ni deposits on accounts of high porosity and defect paths for Cu diffusion. While Cu and Au atoms have a vast difference in radii, there is no significant interdiffusion in this system, provided that there are no defect / vacancy pathways for Cu atoms to migrate. Cu/Au does not start forming intermetallics until 250°C and thus show promising shelf life with the assumption that assembly takes place soon after fabrication cycles are complete. On the other hand, Cu diffuses to the surface of the thin 100-200nm Pd layers within 10 hours. Previous studies [106], have reported a formation of Cu-Pd intermetallics on the Pd-rich side through diffusion-induced grain boundary migration (DIGM) mechanism between diffusion of Cu atoms into fine-grained Pd at room temperature. As the Cu atoms diffuse into the fine-grained Pd, a Cu-rich phase Cu₃Pd is formed epitaxially on the Pd-rich side and continues to grow all the way across the thin-film layer. Such a migration of the grain boundaries can create extremely fast diffusion pathways with low activation energies [107]. These results are shown in Table 2.

To validate these results, X-Ray photoelectron spectroscopy (XPS) was carried out on Silicon substrates deposited with 10 μ m of Cu and 250nm of autocatalytic-Au and 100nm of electroless-Pd (EP) coatings respectively, to emulate the diffusion couples. XPS was

carried out 12 hours after receiving the EP samples and after 2 months on the EAu samples. Strong signals of Cu^{2+} were recorded around the binding energy of 935 e.V. along with the presence of a satellite peak in the 940-947 e.V. range for Pd-finished samples, suggesting the formation of Cu_2O and CuO oxides [108, 109]. This can also be validated from the formation of oxide islands on the surface of the EP sample as shown in Figure 3.4(a). In case of the Au-finished samples, there was no coherent Cu^{2+} or Cu signal across the surface after 2 months of receiving the sample, thus validating their protection against copper oxidation pre-assembly. These results are shown in Figure 3.4(a)-(b).

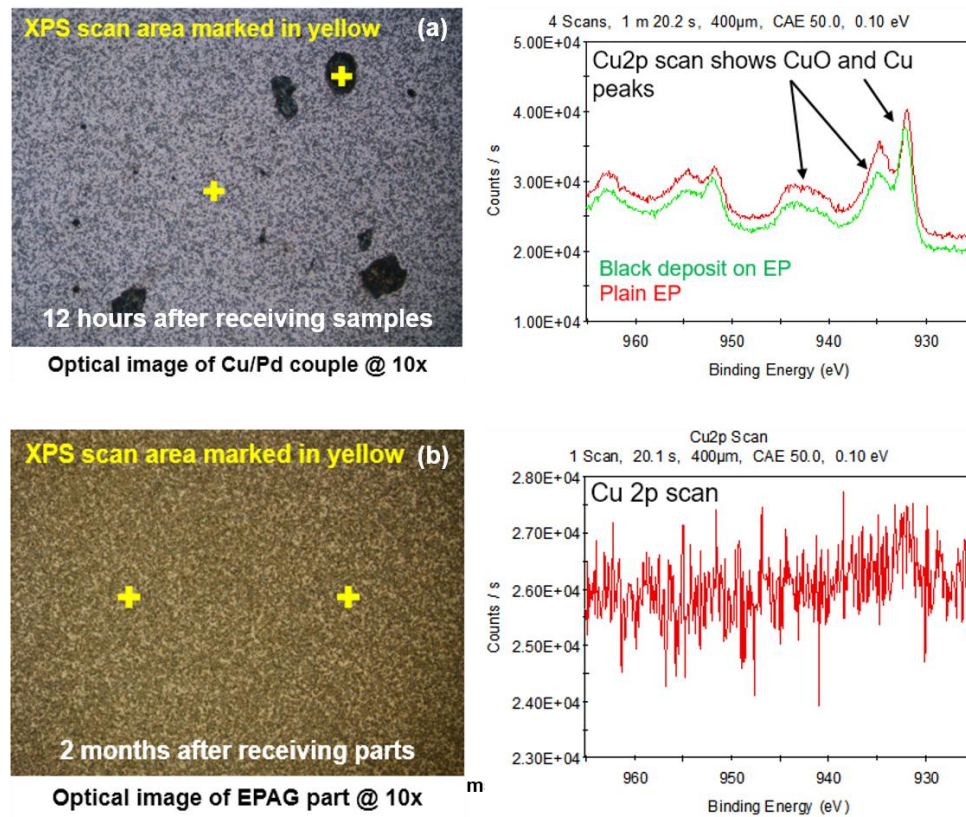


Figure 3.4 XPS analyses of electroless-Pd and electroless-Au finished copper films on Si substrate

3.1.3 Design for assembly

While it is well-known that the self-diffusivity of Cu is quite low [19] in ambient conditions, thus leading to processability challenges in direct Cu-Cu bonding, Cu atoms have a relatively high diffusivity into an Au matrix [100] at bonding temperatures exceeding 250°C. This is generally mediated through defect paths via grain boundaries in nanoscale grains, surface paths on account of curvature of the asperities and through the lattice, thus giving grain boundary, surface and bulk diffusion paths, respectively. Once the instantaneous plastic deformation forms the contact interface, the differences in the curvatures of the void neck and the contacted interface activate diffusion pathways around the free surface of the voids. It is known that this diffusion occurs via 3 different stages: 1) surface diffusion via stress gradients setup due to the differences in curvatures of the void necks and interface in order to close the voids; 2) grain boundary and interface diffusion due to chemical potential difference setup by concentration gradients across the grain boundaries and interfaces to reshape the grain boundaries and decrease interfacial surface energy; 3) lattice diffusion and power-law creep being activated at high temperatures. The analytical diffusion model from Equation 4, is re-used to study low-temperature assembly conditions keeping the modeled thicknesses of Ni, Au and Pd at 3µm, 250nm and 100nm respectively (results shown in Table 2).

3.1.3.1 Cu-Ni-Au System

It can be seen that diffusion of Cu atoms through the diffusion couple of Cu/Ni/Au (3µm Ni/250nm Au) at 250°C would take 65,000 years. Thus, Cu atoms are effectively not able to diffuse through the 3µm-thick Ni layers, providing pure Au-Au interfaces for low-temperature bonding. The low interdiffusion coefficients between Ni/Au also ensure that the self-diffusion of Au is the only driving force to form the metallurgical joints. The self-

diffusion coefficient for Au follows an Arrhenius relation and activation energies are 1.71 eV [110] for lattice diffusion, 0.88 eV [111] through grain boundaries, and 0.40 eV [112] for surface diffusion respectively. Tong et. al. [113], showed that the activation energy for low-temperature (25°C – 250°C) Au-Au bonding is ~0.41 eV, thus correlating well with the surface self-diffusion of pure Au across the interface. Considering assembly conditions for 250°C, the diffusion distance $x = \sqrt{Dt}$ for Au-Au surface self-diffusion increases from 1.5nm after 3s bonding at 250°C to 15nm after bonding for 5 min with a diffusion coefficient of $7.69 \times 10^{-19} \text{ m}^2/\text{sec}$ [110, 111]. This indicates an increased interpenetration of Au interfaces by 1000% (considering initial thickness), thus improving the quality of the metallurgical bond formed, provided that a planar contact is ensured.

3.1.3.2 Cu-Pd-Au System

From the same diffusion model, it is observed that 100nm Pd allows Cu to diffuse through defect paths to the Pd surface within 30sec at 250°C while Cu diffuses through 250nm of Au within 4 hours to form CuO at its surface. Formation of a surface oxide of Cu can seriously degrade the bonding interface as well as interconnection reliability under operating conditions, thus stressing the need for high contact area and lower surface roughness at the bonding interface to prevent formation of Cu oxide in the voids. On the other hand, having perfect contact can initiate formation of Cu-Au intermetallic compounds at the interface [100, 114-116] due to the dissolution of the thin-Pd layer under DIGM mechanism. Such observations have been reported with the increase in resistivity beyond 250°C for Cu/Au diffusion couples, where lattice transformations bring about the formation of Cu₃Au and Au₃Cu intermetallics [100, 115, 117]. Therefore, using 100nm-Pd layers can initiate Cu-Au IMC formation. Under prolonged ageing conditions at 200°C, a

stable intermetallic AuCu (50-50 at%) is also formed [116] while other studies have reported that AuCu is ductile in nature on account of its lattice structure (L1o) [117] in contrast to brittle solder-based intermetallics (Cu_3Sn and Cu_6Sn_5) and can thus stabilize the microstructure at the bonding interface while also absorbing more strain and providing adequate reliability [118-120]. Again, considering assembly conditions at 250°C , the diffusion model predicted the formation of a very thin layer of Cu-Au IMCs (1 – 10nm) under the conditions of 3-300sec, as the Cu/Au diffusion coefficient ($6 \times 10^{-19} \text{ m}^2/\text{s}$) is comparable to that of the Au-Au self-diffusion coefficient. Thus, in both Cu-ENIG and Cu-EPAG interconnections, a predominantly Au-Au bonded interface was predicted to form. With this understanding of the material design before and during assembly, the Ni/Au and Pd/Au layer thicknesses were fixed to $3\mu\text{m}/250\text{nm}$ and $100\text{nm}/250\text{nm}$ respectively for assemblies considered in the further sections of the thesis. In the next section, a critical understanding of power-handling and high-temperature thermal stability of the designed interfaces is provided.

Table 2 Analytical diffusion modeling data

Diffusion Couple	Thickness (μm)	Diffusion Path	Time reqd. to increase surface concentration C_L to 1% C_0		
			25°C	200°C	250°C
Cu/Pd	0.1	Grain boundary	10 hrs	3 min	34 secs
Cu/Au	0.25	Grain boundary	1400 hrs	22 hrs	4 hrs
Cu/Ni	3	Volume	Very High	65000 yrs	6 yrs

3.1.4 Design after assembly

3.1.4.1 Power-handling capability

After assembly, an important characteristic of the electrical performance of an interconnection system is its power-handling capability. It is thus necessary to design the

thickness of the Cu-Ni-Au and Cu-Pd-Au layers to limit electromigration and improve current-carrying capability. An electromigration-induced model of diffusion is developed to ascertain the threshold current densities across the Cu-Ni-Au and Cu-Pd-Au thinfilm systems. It is necessary to consider the electromigration behavior into two types, substitutional diffusion and interstitial diffusion. The concept of critical product is normally used for describing the self-diffusion process, in which the atoms are forced to move within the same type of matrix atoms accompanied with a counter-diffusion of vacancies, such as Sn diffusion in solder joints or Al diffusion across BEOL metal layers and vias. A void gradually formed at the cathode interface and results in localized cracking, leading to failure through this accelerated self-diffusion process. In our scenario, under prolonged current stressing during operating conditions, the electron wind force can effectively drive diffusion of copper atoms across the gold interface, leading to large Kirkendall void formation and an open failure. Normally, the critical product derived from the balance between current stressing and backward mechanical stress can be used for estimating the threshold current density with a given migration distance. Equation 5 describes the critical product of electromigration [121] as

$$j\Delta x = \frac{\Delta\sigma\Omega}{z^*|e|\rho} \quad (7)$$

where j is the threshold current density, Δx is the migration distance, $\Delta\sigma$ is the hydrostatic stress, Ω is the atomic volume, z^* is the effective charge, e is the charge of electron, ρ is the electrical resistivity. The $\Delta\sigma$ could be considered proportional to the young's modulus of matrix material, and the radius of diffusant is corresponding to the Ω term. The effective charges (z^*) referred to the literature [122]. Comparing the structure between a 10 μ m Cu-

Cu interconnection, a Cu microbump with 15 μ m solder cap, and the designed Cu-ENIG and Cu-EPAG interconnections, the threshold current density for each is 1.8×10^6 A/cm², 10^4 A/cm², 5×10^5 A/cm² and 1.2×10^5 A/cm², respectively. Thus, at least a 10X improvement was predicted by replacing the Cu-pillar microbump with the designed Cu-ENIG and Cu-EPAG interconnections, and the failure mechanism related to void propagation under current stressing thus could be effectively prevented.

The interstitial diffusion relates to the dissolution of under bump metallization (UBM). The main difference is that the diffusants would not build the backward mechanical stress to balance the electron wind force, and a differential intermetallic growth rate can be observed between cathode and anode interface. The diffusion flux of these diffusates can be described as in Equation 6:

$$J = C \frac{D}{KT} z^* |e| \rho - D \frac{d\mu}{dx} \quad (8)$$

where C is the concentration of the element of interest, D is the diffusivity of atoms through the matrix, Z^* is the effective charge number, ρ is the resistivity, J is the current density, e is the charge of electron and μ is the chemical potential. The driving force from electron flow is generally two orders of magnitude higher than that from the concentration gradient. The overall diffusion flux is consequently dominated by electromigration. In solder interconnections, Cu atoms can easily be driven from the cathode to the anode through the solder which provides higher interstitial diffusivities of about 10^{-12} to 10^{-13} m²/s at 25°C. The Cu atoms accumulated on the anode interface results in enormous intermetallic precipitation, and this diffusion flux keeps dissolving the Cu pads on the cathode interface to replenish the Cu concentration of solder. With Cu-ENIG and Cu-EPAG configurations,

the diffusion of Cu is comparatively limited as the interdiffusivity coefficients through Ni and Cu-Au IMCs, are $5 \times 10^{-22} \text{ m}^2/\text{s}$ and $6 \times 10^{-20} \text{ m}^2/\text{s}$ respectively. This significantly reduces the diffusional flux for such solid-state interconnections and prevents over-dissolution of the cathode interface. Thus, under the same current densities, a 4X increase in lifetime could be expected with Cu-ENIG and Cu-EPAG interconnections as compared to solder interconnections. However, in the particular case of Cu-EPAG interconnections, the thin-film nature of the deposited Pd/Au layers can create defect pathways for accelerated diffusion of Cu atoms under current stressing and care must be taken to ensure that such layers are defect-free and non-porous.

3.1.4.2 Thermal stability after assembly

From previous sections, we understand that Cu-ENIG interconnections form pure Au-Au interfaces after assembly that are thermally stable beyond the lifetime of devices at 250°C. However, Cu-EPAG interconnections lead to the formation of variable AuCu IMCs across the bonded interface. Under high-temperature operating conditions (80-200°C) as demanded by emerging high-performance applications, the thermal stability of such IMC phases is highly desirable. To study this, a diffusion model was setup using the Laplacian method for binary metallic systems to understand the diffusion of Cu atoms across the Au interfaces under a rigorous thermal boundary condition of 200°C. For ease of modeling, the thin-Pd layer was considered as dissolvable and therefore did not impede the diffusion of Cu through the Au layers. The model consisted of a finite Au layer of 500nm thickness sandwiched between double semi-infinite layers of Cu. All the previous boundary conditions and assumptions from Equation 3 were applied here as well. Figure 3.5 shows the diffusion model as a function of isothermal ageing conditions across 0-1000 hours.

Under 250+ hours of thermal ageing, the model predicted the formation of Cu-rich Cu_3Au phases on the Cu side with a concurrent formation of Au-rich Au_3Cu across the 500nm-thick Au layer. Indeed, islands of such phases forming between Cu/Au diffusion couples at 250°C have been previously reported. Furthermore, a 50-50 at% AuCu IMC phase started forming as we approach 1000 hours thus proving the continued stability of these interfaces even under ageing conditions provided that there is ideal contact.

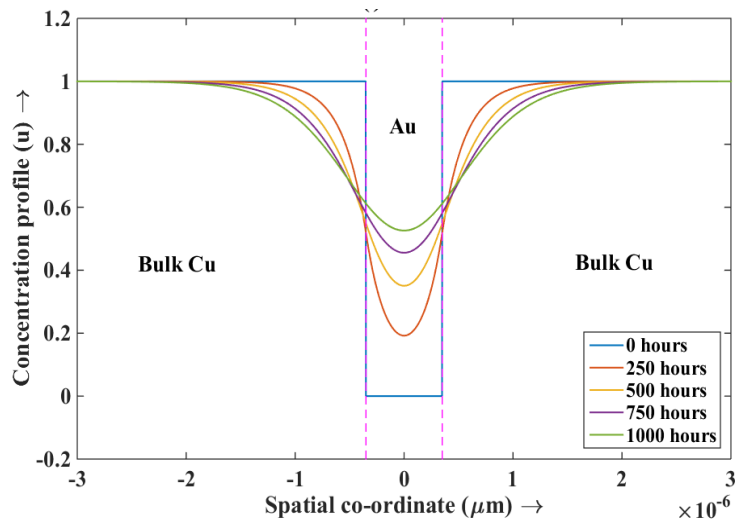


Figure 3.5 1-D diffusion model for Cu/Au binary couple under ideal contact at 200°C

3.2 Thermomechanical Process Modeling

While the design rules for performance were developed, it is necessary to understand the thermomechanical effect of assembly parameters on the throughput of the technology in parallel. In the proposed technology, plastic deformation of the interconnection system is considered instead of cost-intensive CMP-based planarization processes to address bumps and pads non-coplanarities, and create intimate contact at the mated interfaces, critical for diffusion and metallurgical bonding [123]. Thermocompression bonding under the action

of applied pressure, temperature and time brings about atomic contact of mated interfaces to initiate solid-state diffusion. When the Cu bump and pad surfaces are brought together, the surface asperities from roughness or waviness form a ridge-to-ridge like contact as is shown with a sine-wave geometry [124] in Figure 3.6.

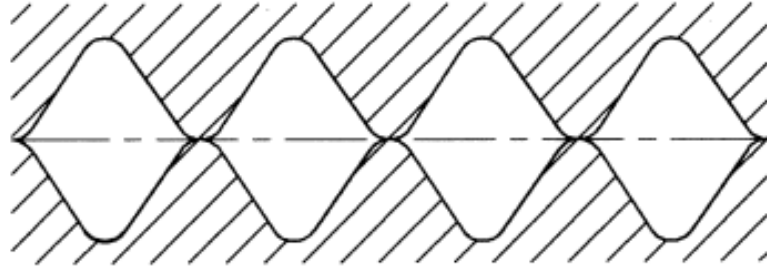


Figure 3.6 Sine wave-like asperities forming interfacial voids

When the applied pressure exceeds the yield strength of Au, the dislocation density increases across the interface and the surface asperities deform plastically to form interfacial voids. The contact area is increased till it is large enough to support the applied bonding pressure, i.e. the localized stress drops below the yield strength of the material. This deformation occurs instantaneously and does not account for time-dependent power-law creep mechanisms. Sharp et al. [125] studied the deformation behavior of an indenter in fully plastic regime and his equation is as:

$$P_k = \frac{1}{3} \sqrt{2a\pi\sigma_y \left(2a + a \ln \left(\frac{aE}{3\sigma_y R} \right) \right)} \quad (9)$$

where ' P_k ' is the bonding pressure, ' σ_y ' is the yield strength of the material at room temperature, ' a ' is the contact width of the void ridge, ' R ' is the radius of curvature of the sine wave, and ' E ' is the Young's modulus of Gold. An increase in the bonding pressure P_k will increase the contact width ' a ' and thus bring about a decrease in the volume of the

void leading to its eventual collapse. Although this model generally overestimates the contacted area due to the stochastic nature of the asperities, it is a fair approximation of the actual bonding conditions. The surface condition thus determines the driving force required to create intimate contact at the mated interfaces, necessary to initiate metallurgical bonding. The essential closure of interfacial voids marks the completion of metallurgical bonding. The following sections will consider the effect of applying surface finish coatings and the geometry of the Cu bump shape on assembly parameters through thermomechanical modeling.

3.2.1 Effect of surface finish

To evaluate the effect of the surface finish composition on the deformation behavior of the interconnection system during thermocompression bonding, the 3D quarter-symmetric finite element model (FEM) of Figure 3.7 was built in ANSYS. The modeled stack-up consisted of a Cu bump, 10 μ m in height and diameter, plated up from a 5 μ m-thick Cu redistribution layer pad on the Si die side, assuming a 10 μ m-thick Cu landing pad on the substrate. A half-pitch design rule was used to scale the bump diameter to 20 μ m pitch, ultimate target of next-generation high-performance systems. All-Cu interconnections were used as reference to compare the different surface finishes, including an ENIG film of 3 μ m-thick Ni(P) and 250nm Au, and an EPAG film of 100nm-thick Pd and 250nm Au layers. The model considered a B-stageable, no-flow, filler-free, epoxy-based pre-applied underfill material (BNUF) surrounding the Cu bumps. All materials were assumed with an elastic-plastic mechanical behavior (Table 3 [126]) with plasticity represented by a bilinear kinematic hardening law. The load was applied on the die side, while the model was constrained along the sides and the bottom to imitate full symmetry. Uniform heating and

cooling was applied, and the model was solved in five steps using the birth-and-death method to simulate as accurately as possible the thermocompression assembly process: 1) temperature ramped to bonding peak temperature of 250°C; 2) load ramped up to bonding pressures in the 50-350MPa range; 3) pressure released; 4) underfill activated on cooling to 160°C corresponding to the T_g of the epoxy material; 5) cooling to room temperature, defined at 25°C.

Table 3 Isotropic elastic-plastic material properties for FEM model

Materials	Cu	Ni(P)	Au	Pd	BNUF	NCP
Elastic Modulus (GPa)	117	199	79	120	2.9	6.5
Poisson's Ratio	0.33	0.31	0.44	0.39	0.4	0.4
Yield Stress (MPa)	172.38	1500	100	200	n/a	n/a
Tangent Modulus (MPa)	1034.2	1200	200	13043	n/a	n/a
CTE (ppm/K)	17	12	14	11.8	50	33

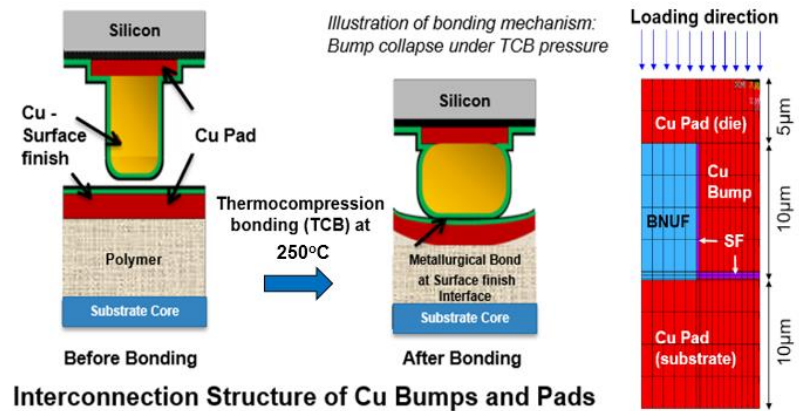


Figure 3.7 Schematic of Cu interconnection structure (left) and finite element model of the thermocompression assembly set-up (right)

On application of a load, compressive forces generate stresses in the Cu bump leading to plastic deformation and collapse while bringing the interfaces into intimate contact. The FEM deformation contours of Cu bumps are shown in Figure 3.8 with (a) Cu bump and

pad without surface finish, for reference; (b) ENIG on bumps and pads; (c) EPAG and ENIG on bumps and pads, respectively; and (d) EPAG on bumps and pads. It has been shown that an interconnection collapse by $3\mu\text{m}$ was necessary to offset non-coplanarities and warpage and achieve reliable interconnections [123]. With all-Cu interconnections, it can be seen from Figure 3.8 that the plastic deformation was almost equally distributed between bumps and pads, with no stress gradients through the underlying low-K on chip dielectric layers.

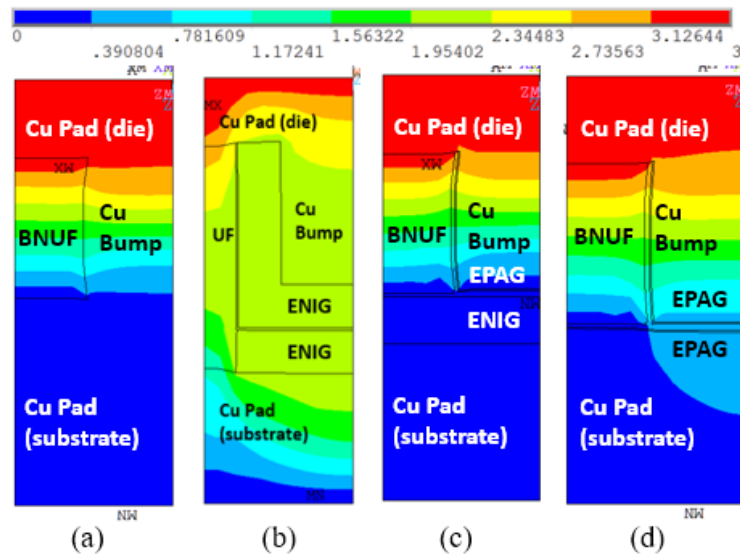


Figure 3.8 Cu bump and pad vertical displacement, resulting in $3\mu\text{m}$ total collapse with (a) Cu-Cu interface at 102MPa, (b) ENIG-ENIG interface at 350MPa; (c) EPAG-ENIG interface at 125MPa; and (d) EPAG-EPAG interface at 110MPa

In the Cu-ENIG system, due to the inherent stiffness of the Ni(P) barrier layer, deformation of the Cu bump and substrate pad was significantly hindered, shifting plastic strains in the Cu pad on the die side. The model predicted a total collapse of the Cu-ENIG interconnections by $\sim 3\mu\text{m}$ at 350MPa. This data correlates closely with compression trials carried out on Cu-ENIG interconnections, $10\mu\text{m}$ in diameter at $30\mu\text{m}$ pitch, at 250°C , with

a pressure of 365MPa applied for 60s [126]. Typical bump and pad deformation contours for all EPAG surface finish configurations are presented in Figure 3.8(b)-(d) with bonding pressures in the 100-125MPa range, varied to achieve the targeted 3 μ m collapse. Such collapse was obtained with a 125MPa, 110MPa, and 102MPa applied pressure in the EPAG-ENIG, EPAG-EPAG and Cu-Cu configurations, respectively. Since the EPAG Pd-Au layers are very thin and ductile compared to Ni(P), plasticity of Cu was mostly retained with a maximum 7% increase in load required to give a comparable interconnection collapse of 3 μ m as in all-Cu interconnections, as can be seen from Figure 3.9.

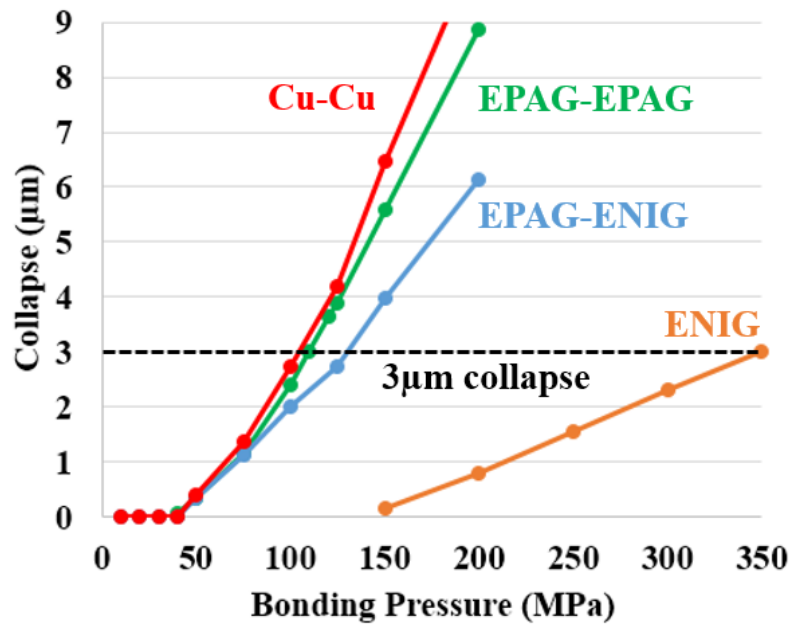


Figure 3.9 Collapse of the Cu bumps and pads with respect to variation in surface finish configurations as a function of applied bonding pressure, obtained by modeling thermocompression at 200°C

As the Ni content is reduced in the surface finish, the pressure required to achieve a 3 μ m total collapse decreases, with plastic deformation being progressively uniformly distributed between bumps and pads for the EPAG-EPAG system, similarly to that for the reference Cu-Cu model. A 3X reduction in bonding pressure was predicted to bring about a total

collapse of $3\mu\text{m}$ at $20\mu\text{m}$ pitch, from 350MPa to 110MPa with ENIG and EPAG configurations respectively. Further, the lateral displacement for all the configurations was found to be less than $1\mu\text{m}$, thus eliminating the risk of electrical bridging. The excessive accumulated plastic strain observed in the soft, ultra-thin interfacial layers in Figure 3.10 should be sufficient to act as a driving force for self-diffusion and subsequent local metallurgical bonding at the Au-Au interface. It is important to note that while a qualitatively high plastic strain is predicted in the thin Au layers, the exact value can be exaggerated due to scale-of-model issues.

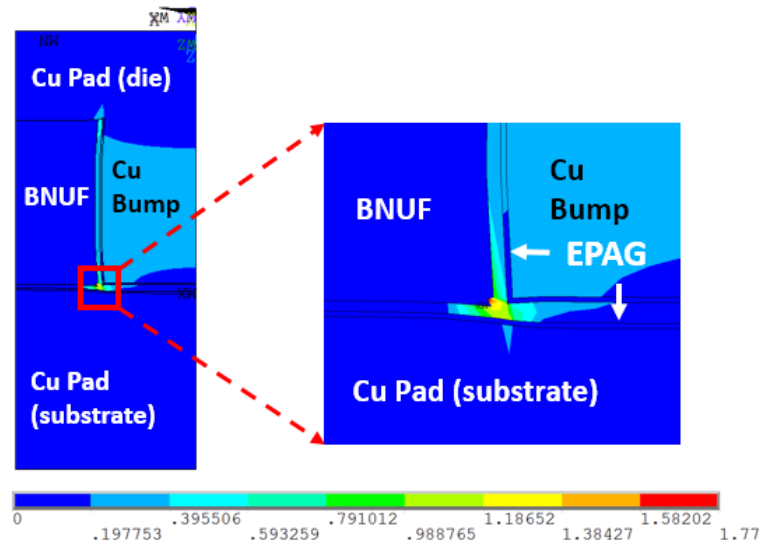


Figure 3.10 Plastic strain at the Au-Au interface on thermocompression of Cu interconnection with EPAG-EPAG configuration at 120MPa

3.2.2 Effect of planarization

A high variation in the Cu bump height can result in poor local contact during thermocompression bonding and a non-uniform distribution of applied pressure across the Cu traces on the substrate. This can cause localized plastic stresses beyond the yield strength of Cu causing a rippling effect as shown in Figure 3.11, and can lead to complete

delamination of the Cu trace from the substrate. A similar result was also reported by [53] in ECTC 2016, wherein, Cu-Cu thermocompression bonding for 3D-IC packages was carried out at 171MPa leading to rippling and buckling of Cu traces beneath the bumps. Such irregularity in the Cu bump heights could also cause stresses on the ULK layers at the active die-side thus causing dielectric cracking and reliability challenges. While such reliability challenges can occur from either non-coplanarities across the substrate or the bump profile, the need for an understanding of the effect of bump profile on stress distribution across the interconnection is acute.

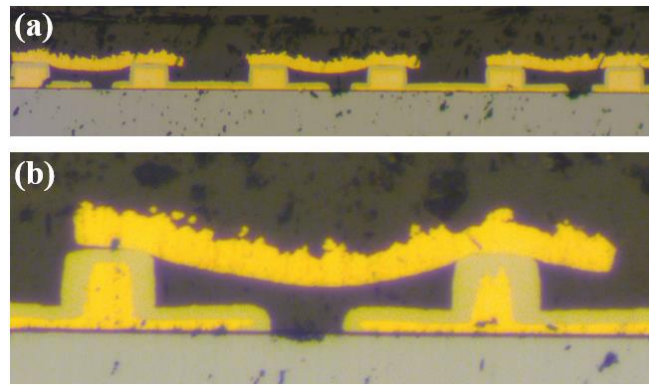


Figure 3.11 (a) Cross-section of Cu-ENIG interconnections at 365MPa – 200°C – 3sec assembly conditions; and (b) magnified image of delaminated Cu trace

Tolerance to non-coplanarities and warpage is a defining characteristic of solder-based interconnections. However, in the case of solid Cu-based technologies, the relatively high elastic modulus limits the compliance and the strain absorbing capability of Cu bumps, thus causing stress concentrations and failures at the interface. To further understand this in the context of planarization, a 2D finite element contact model was developed on ANSYS^{15.5} to simulate the thermocompression bonding of Cu interconnections at 40μm pitch and compare the characteristics of as-plated and planarized bumps. Contact element modeling with rough surfaces in cases of as-plated Cu bumps is a non-linear problem, and

can take up a lot of computational resources. To reduce the processing time, a simple ‘rounded’ geometry was considered for as-plated Cu bumps while a flat geometry was considered for planarized Cu bumps. The model consisted of two half-symmetric Cu pillars (ϕ 20 μ m) at 40 μ m pitch with a bump height of 20 μ m and 15 μ m for as-plated and planarized bumps respectively. The Cu bumps were plated up from a 5 μ m-thick Cu re-distribution layer (RDL) pad on the die side, initiating a single node contact with a 5 μ m-thick Cu trace on the substrate side. ENIG (3 μ m Ni – 0.25 μ m Au) and EPAG (100nm Pd – 250nm Au) surface finish layers were considered on the Cu bumps and RDL pads, while FR-4 and glass were considered for the substrate. All the materials were assumed to be elastic-plastic with a bilinear kinematic hardening law representing the plasticity. An elemental pressure load was applied on the die side with the model being constrained along the vertical axes and the top to simulate complete symmetry. A schematic of the model geometry is as shown in Figure 3.12.

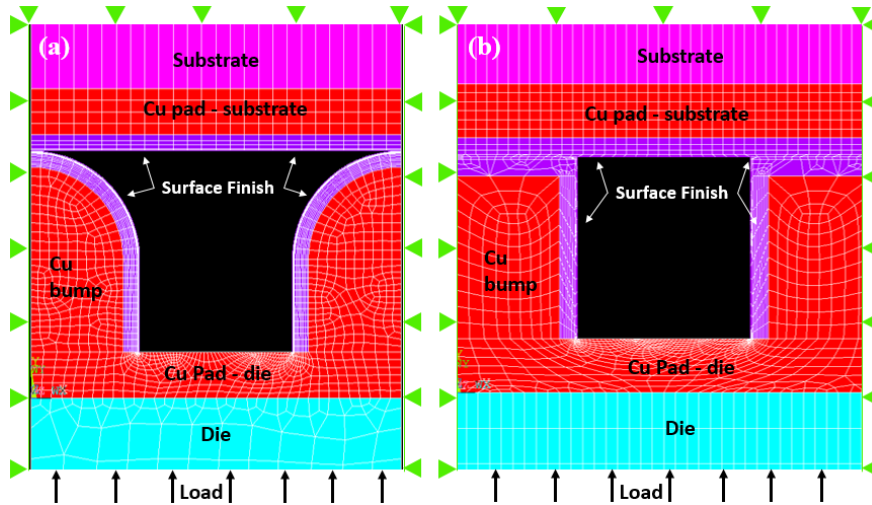


Figure 3.12 FE model of (a) as-plated rounded Cu bump assembly and (b) planarized flat Cu bump assembly

The model was isothermally heated and cooled in 4 steps using the birth-death method to accurately simulate thermocompression bonding: 1) surface load applied; 2) temperature ramped to bonding temperature of 250°C; 3) surface pressure released; 4) temperature ramped down to 25°C. A mesh refinement command was used to improve the accuracy of nodal and elemental results. The substrate and interconnection physical properties for the defined materials are tabulated in Table 4.

Table 4 Properties of materials within the substrate stack-up

Parameters	Si	Glass	FR4	Dielectric
Elastic Modulus (GPa)	130	77	77	6.9
Poisson's Ratio	0.17	0.22	0.22	0.3
CTE (ppm/K)	2.8	3.3	24	23
Reference temperature(°C)	220	160	160	162

The modeled geometry was matched to that of our previous result with assembly conditions of 365MPa – 250°C – 3sec, with ENIG surface finish applied on Cu bump and EPAG surface finish on Cu pad on FR-4 substrate [123]. For ease of modeling across contact

elements, the thin Au layer was ignored and the ENIG surface finish was modeled as 3 μ m of Ni only. It was observed that under 365MPa of loading, there was significant deformation at the bonding interface with a maximum Y-displacement of 4.6 μ m. The copper right under the bump is compressed while the copper trace between the bumps is under tension, thus corroborating strongly with the ripple-like behavior observed earlier. The nodes at the Cu trace – substrate interface showed a maximum tensile Y-stress of 170MPa as shown in Figure 3.13. This is very close to the yield strength of copper (170 – 300MPa).

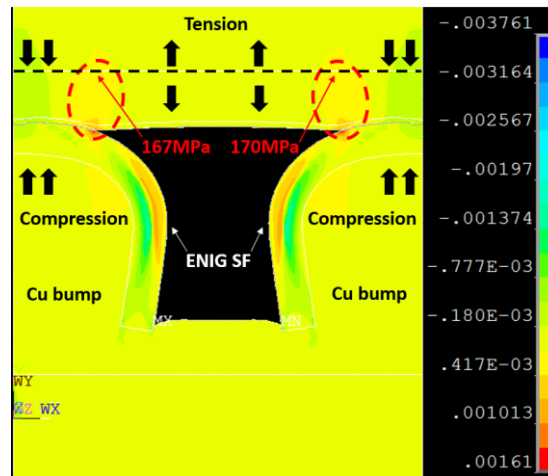


Figure 3.13 Y-stress across the as-plated rounded Cu bump assembly (scale x 10³ GPa) with a maximum stress of 170MPa across the Cu trace-substrate interface

The high stress concentrations under the bump during assembly can cause large amounts of plastic deformation in the Cu trace causing it to compress under the bump and expand in the unloaded free directions giving a rippling effect. Due to the presence of surface defects like voids, cracks or precipitates at the trace-substrate interface, the plastic deformation in the trace triggered crack propagation at the interface to the substrate causing buckling and eventual peeling of the Cu trace.

To understand the effect of planarization on the stress-distribution across the Cu trace-substrate interface, the thick ENIG surface finish is replaced by EPAG surface finish layers across the bumps and pads. As a result of using thin EPAG surface finish, a similar bump collapse of $4.5\mu\text{m}$ can be achieved at $\sim 250\text{MPa}$, which was the initial loading condition used in this simulation. Both flat and rounded geometries were built for the Cu bumps and the thickness of the Cu trace on the FR-4 substrate was varied from $10\mu\text{m}$ down to $3\mu\text{m}$, to accommodate fine-pitch line-space (L/S) design rules. Across all configurations, the maximum Y-stress at the Cu trace – FR-4 substrate interface after cooling to 25°C at every assembly condition was extracted and plotted against the Cu trace thickness. Figure 3.14 shows the Y-stress profile across the Cu trace – FR-4 substrate interface at a trace thickness of $5\mu\text{m}$. It can be seen that the as-plated rounded Cu bumps deform outward under thermocompression and transfer most of the plastic stress across the Cu trace – substrate interface giving a maximum tensile stress of 161MPa in the y-direction. On the other hand, the planarized bumps absorb all the stress, thus reducing the plasticity of the Cu trace and improving the stress distribution pattern across the layers with 40MPa of tensile stress only at the trace-substrate interface. For FR-4 organic substrates, it can be observed from Figure 3.14 that all the planarized assemblies on FR-4 substrates have an approximately constant low stress of $\sim 40\text{MPa}$ at the trace-substrate interface.

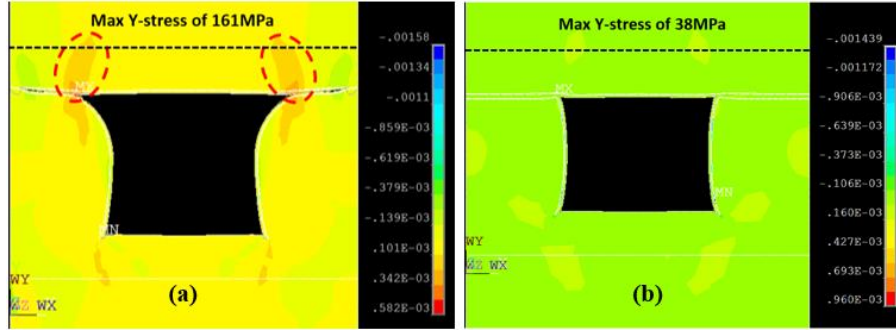


Figure 3.14 Maximum Y-stress profile across the Cu trace – FR-4 substrate interface for the (a) as-plated Cu-EPAG and (b) planarized Cu-EPAG assemblies at 250MPa bonding pressure with 5 μ m Cu trace thickness (scale x 103 GPa)

The maximum y-stress for as-plated assemblies on FR-4 varied in the range of 248MPa to 72MPa when the trace thickness is varied from 3-10 μ m with the interface projected to fail with trace thicknesses less than 5 μ m. Therefore, it can be said that the stress is completely contained within the Cu bump in case of planarized assemblies while as-plated rounded bumps spread the stress to weaker interfaces, thus increasing the stress concentration and consequently the probability of failure at the FR-4 substrate interface. In addition, for verification on glass substrates, the substrate material was changed to glass and a 15 μ m soft dielectric layer between the Cu trace and glass substrate was modeled, to represent a realistic glass substrate package. A pressure of 200MPa was applied to simulate an overall bump collapse of 4.5 μ m for the rounded Cu bumps, similar to that using FR-4 substrate. It can be seen from Figure 3.15 that the stress values for rounded Cu bumps at the trace – dielectric interface with glass substrates ranges from 235 – 130MPa across a trace thickness of 3 – 10 μ m with the minimum of 85MPa at 7 μ m. Furthermore, the stress values for planarized flat Cu bumps on glass substrates range from 66 – 140MPa, with the stress fairly constant at 60MPa from 3 – 7 μ m Cu trace thickness and steadily rising from 7 – 10 μ m. This behavior after 7 μ m Cu trace thickness for both flat and rounded Cu bumps can be attributed to the high deformation of the softer dielectric layer (elastic modulus of 6.9GPa),

buckling under the thicker Cu trace layer and increasing the stress at the trace – dielectric interface.

From the above, it is clear that certain design rules need to be implemented for the safe assembly of Cu interconnections without inducing failures at the Cu trace – substrate interfaces. For organic substrates, the planarized flat Cu bumps gives stress values that are well below the yield strength of Cu, thus giving freedom in choosing the Cu trace thickness, while the as-plated rounded Cu bumps limit the allowable thickness of the substrate Cu trace to $> 6\mu\text{m}$. On the other hand, both the rounded and flat Cu bumps limit the maximum allowable Cu trace thickness to $< 7\mu\text{m}$ for a ripple-free interfacing with the dielectric layer, thus ensuring a higher durability.

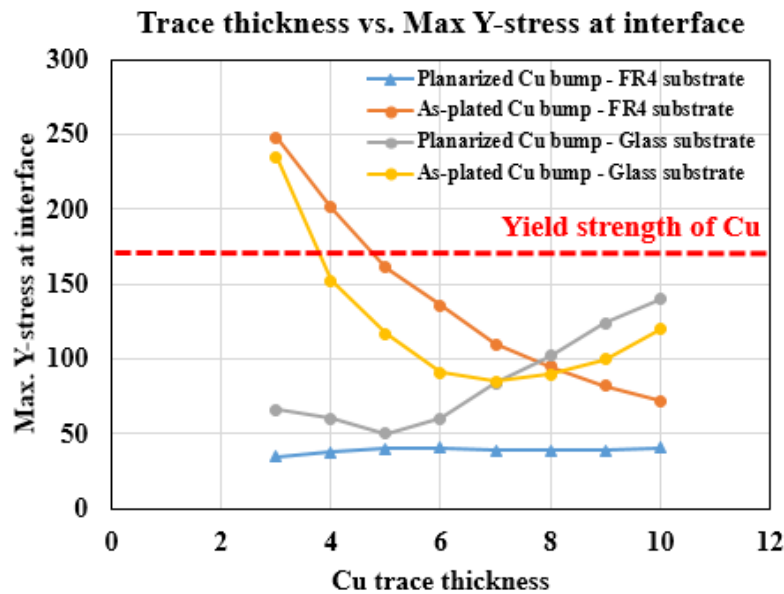


Figure 3.15 Cu trace thickness v/s max y-stress at trace-substrate interface for FR-4 substrates

3.3 Test Vehicle Design

The fabrication details of the four test vehicles (TV) utilized in this study are mentioned below:

3.3.1 Test Vehicle 1 (TV1) at 100 μ m pitch

Test vehicle I, designed to carry out shear strength testing and a preliminary assembly analysis, consisted of 5mm x 5mm and 600 μ m-thick Si dies with 760 Cu μ -bumps, arranged in 3 peripheral rows at 100 μ m pitch and a central area array at 250 μ m pitch. The daisy-chain pattern consists of individual chains, with 4 and 8 two-point probe structures for corners and half-edge chains respectively, while the area array is split into 4 individual daisy chains as shown in Figure 3.16. A 600 μ m-thick 6" Si wafer was utilized to fabricate the Si dies using semi-additive plating processes. A 2 μ m-thick SiO₂ layer was first deposited by Plasma-Therm PECVD, followed by sputtering of a 30 nm Ti – 700nm Cu seed layer. A 3-4 μ m Cu dogbone redistribution layer is then laid out on the wafer by electrolytic plating, followed by bumping photolithography and electroplating of the ~10 μ m height Cu bumps. Test substrates were fabricated from 6" x 6" Cu-clad FR-4 organic laminates for ease of subtractive processing. The Cu cladding on the 1mm-thick FR-4 core was etched down from 50 μ m to 10 μ m, followed by standard photolithography and back-etch processes to build the dogbone Cu patterns without a seed layer. After photoresist and seed-layer stripping, surface finish was applied by Atotech GmbH.

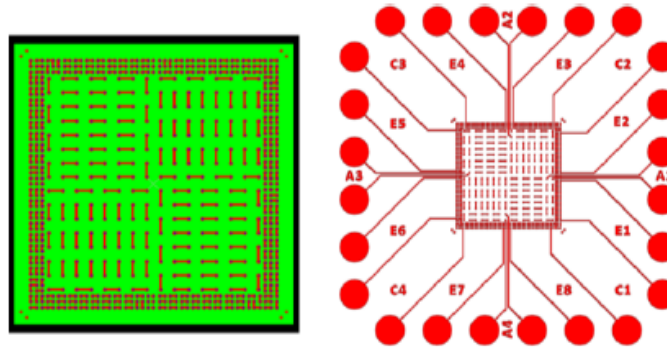


Figure 3.16 Test vehicle 1 layout: 5mm x 5mm Si die and 20mm x 20mm FR4 substrate with probe pads

Design inputs from the previous sections were used to control the thickness of the Au and Pd layers based on: a) bonding pressure reduction while maintaining a $3\mu\text{m}$ bump collapse to compensate for non-coplanarities, and b) metallurgical bonding, confirmed by detailed interfacial characterization, and compared to the ENIG reference. The as-plated Si die with the EPAG surface finish can be observed in Figure 3.17. An XRF measurement of the EPAG surface finish on the dicing mark of the wafer indicates an average thickness of 282nm of Au and 124nm of Pd, which correlate reasonably with developed design rules.

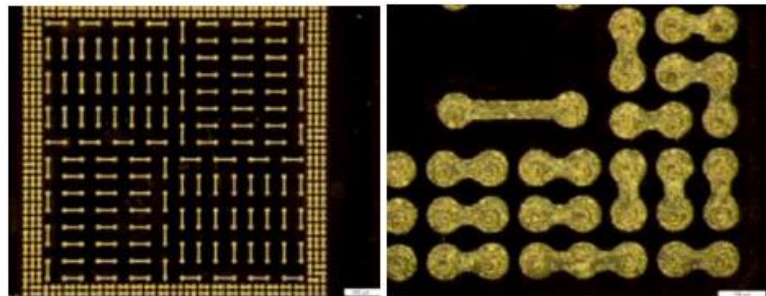


Figure 3.17 Optical micrographs of as-plated Si die with EPAG surface finish

3.3.2 Test Vehicle 2 (TV2) at $40\mu\text{m}$ pitch

A $40\mu\text{m}$ pitch test vehicle was designed and fabricated to investigate and compare the effect of planarized and as-plated Cu bumps on the bonding parameters. The test vehicle

comprises of a 7.1mm x 7.1mm 350 μ m-thick wide I/O single-row peripheral daisy-chain thin-Si dummy die with an I/O count of 1246 bumps at 40 μ m inline pitch. The die was designed, patterned and fabricated by GLOBALFOUNDRIES on a thinned 300mm Si wafer. Further, ASE electroplated 20 μ m diameter Cu bumps to an as-plated height of 17 μ m. The bumped 300mm Si wafers were then shipped to Disco Corporation for mechanical planarization to a set height of 13 μ m.

The electroplating photoresist was stripped off before surface planarization. This process was carried out by DISCO Corporation, our industry partner, and consists of a single diamond bit that is mounted on a spindle rotating at high speeds at the fixed height (shown in Figure 3.18). The surface to be planarized is held in position below the rotating bit on a flat chuck table and is creep-fed slowly under the rotating cutting bit. The diamond tip shaves off excess material at a pre-defined fixed height from the base of the wafer, generally, a few microns just below the sample's original top surface. The speed of the planer is optimized so that cuts made with every rotation overlap while avoiding burr or drag-out metal shavings as much as possible, thus providing an even, smooth surface.

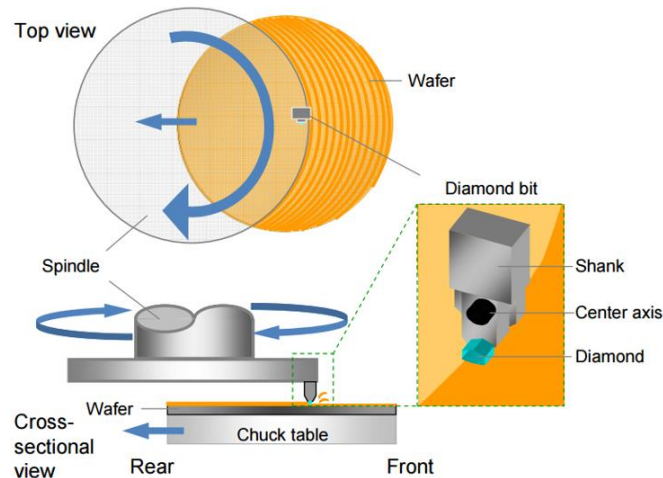


Figure 3.18 Schematic of Disco Corporation's surface planarization process

Figure 3.19 contrasts the appearance of as-electroplated and post-planarized Cu bumps. The planarization process removed all within-feature non-uniformities as well as the rough surface. The planarized Cu bump has a flat and smooth top to an overall surface roughness below $1\mu\text{m}$ across a 300mm wafer. Such precisely controlled removal in a coplanar fashion cannot be achieved with any other existing process.

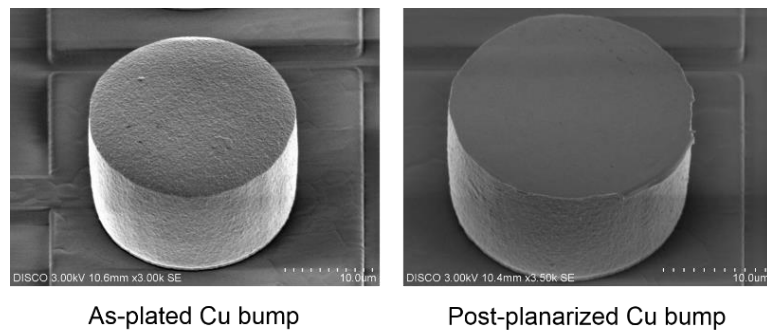


Figure 3.19 SEM images of as-plated and post-planarization individual Cu bump

Once the planarization is complete, surface finish layers of thin-ENIG and EPAG were applied by Atotech GmbH. Finally, the surface finished wafers were singulated and diced by Disco Corporation and shipped to GT-PRC for thermocompression bonding assembly. Si square coupons, 10mm x 10mm in size, with a blanket Cu layer were used as substrates to eliminate thermal expansion mismatch and subsequent warpage in the shear strength

evaluation. Further, the test vehicle was designed to understand interfacial reaction kinetics under low-temperature bonding. The substrates were fabricated using a semi-additive process: a SiO₂ dielectric layer was deposited, followed by sputtering of a Ti-Cu seed layer. Standard lithography and plating tools were then used to pattern a blanket Cu layer of 5µm thickness in 10mm x 10mm square coupons. On stripping the photoresist and etching the seed layer, ENIG and EPAG surface finish layers were deposited courtesy of Atotech GmbH and the wafer was finally singulated into individual substrate coupons.

3.3.3 Test Vehicle 3 (TV3) at 50µm pitch

The TV3 was designed with a bump-on-trace (BoT) structure and composed of a single peripheral daisy chain at 50µm pitch. Figure 3.20 shows the design of TV3, which contains 544 I/Os. The die itself was fabricated at GT-PRC using the standard SAP steps mentioned above. Planarization was carried out and Disco Corporation and EPAG / ENIG surface finish was applied at Atotech GmbH. Two different core materials were used in this study, one is a 200µm-thick Hitachi E679FG-S organic material and another is a 100µm-thick low-CTE glass from Asahi Glass Corporation. The organic substrates strips were supported by Walts Corporation, as shown in Figure 3.21(a), and then singulated in GT-PRC with the DISCO Automatic Dicing Saw DAD3360. Figure 3.21(b) shows the build-up structure of those organic substrates, which contains two dummy mesh layers and two Cu routing layers. An industry standard ABF-GX series build-up material and solder resist were applied. The organic TV3 substrate design was used as baseline for the design of the TC-NCP process as well as studying the reliability using the EPAG surface finish.

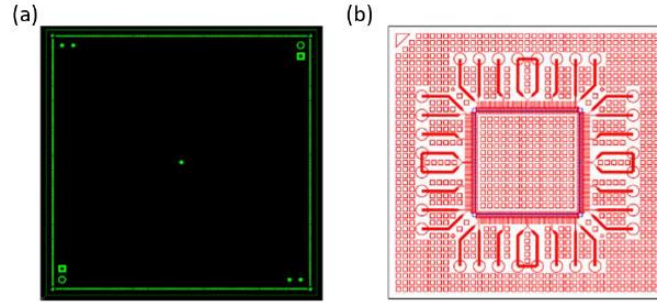


Figure 3.20 TV2 design of (a) die and (b) substrate

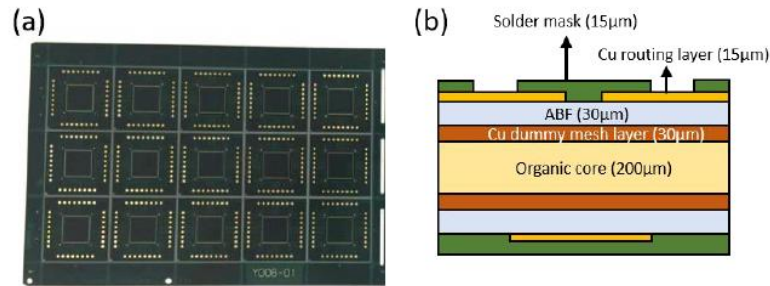


Figure 3.21 (a) Top view, and (b) build-up structure of organic substrate for TV3

GT-PRC has been dedicated for years to developing ultra-thin glass interposers for next-generation high-performance electronics, driven by the potential of high-density wiring with reduced electrical loss, tailorable mechanical properties, and panel-level processing at low cost. As part of this activity, 100 μ m-thick glass substrates with TV2 design were fabricated in-house with the technical support of NGK Spark Plug Corporation. First, an O₂ plasma and silane treatment were applied on bare glass to enhance the adhesion of build-up dielectric layers. An ABF-GX92 film from Aginomoto Corporation was vacuum laminated with Hi-Vac-600 Drawer Vacuum Laminator, and then cured with hot pressing. The seed layer was then deposited on the ABF film with a Printoganth MT electroless Cu chemical. A similar semi-additive process was used to form the Cu wiring, including lithography and Cu electrolytic plating, as described for TV1. After the Cu seed layer removal, a Finelise-JCU chemical was applied to eradicate the Pd atoms adhering to the

ABF in case of Pd contamination. Before applying the Hitachi SR-FA solder resist, a BondFilm process developed by Atotech GmbH was introduced to enhance Cu-polymer adhesion. Finally, an ENEPIG surface finish was deposited onto the exposed Cu traces. The process flow and the fabricated glass substrate after singulation are shown in Figure 3.22.

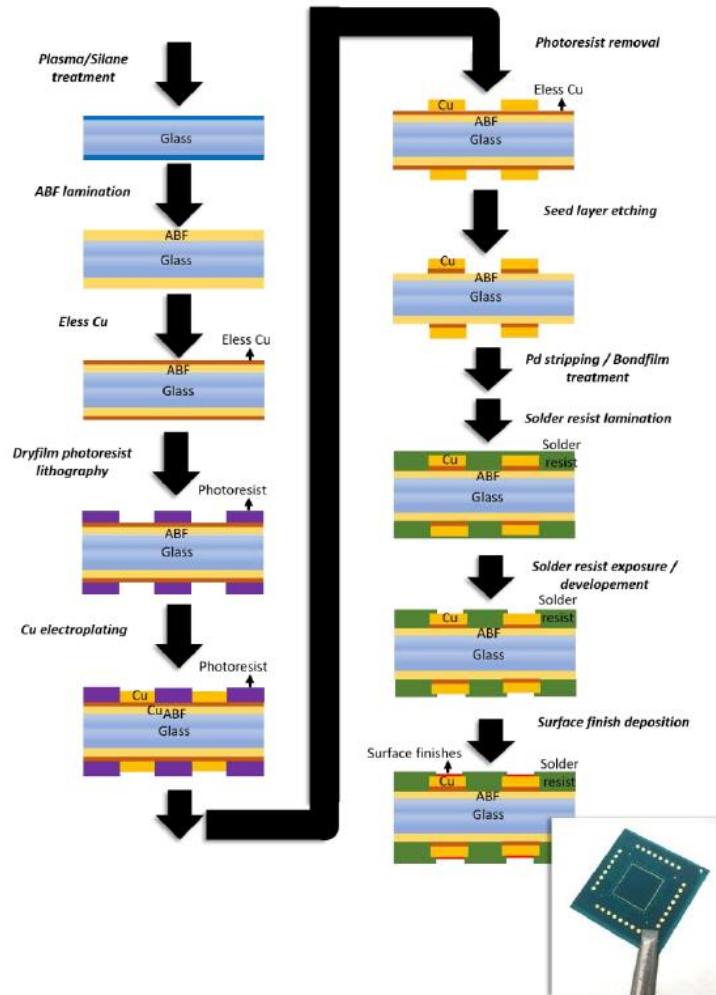


Figure 3.22 Process flow for fabrication of TV3 glass substrates

3.4 Assembly Demonstration and Characterization

3.4.1 Material Characterization

The impact of planarization of Cu bumps is similar to that of cold working. Immediately on being processed by a surface planer tool, surface defects such as grain hardening, grain-size reduction and twinning grain boundaries could occur [127], thus changing the mechanical properties of the surface, and further affecting bonding parameters during assembly. To verify this, a parallel series of experiments were performed, where the as-plated and planarized Cu bumps with bare-Cu, EPAG and ENIG surface finish layers were subjected to micro-mechanical hardness and texture characterization supported by Atotech GmbH. A Picodentor HM500 was used to characterize the surface hardness with a maximum applied force of 25mN over an indentation depth of 0.9 μ m. It can be seen from Figure 3.23 that the as-plated and planarized Cu bumps have similar Martens Hardness values over an indentation depth range, thus suggesting no significant effect of planarization. The red markers in Figure 3.23 indicate hardness values for Cu bumps with EPAG surface finish, with the effect of a hard Pd layer being visible for the first 100nm indentation depth, while a similar response to that of bare-Cu is observed throughout the rest of the indentation depth. However, in the case of Cu bumps with ENIG surface finish (blue markers in Figure 3.23), the electroless Ni is so thick that up to 400nm depth, the response of the Cu bump is much harder, thus substantiating the non-compliance of 3 μ m-thick Ni barriers as surface finish layers. Further, as has been reported before [127], bump shear testing on as-plated and planarized Cu bumps showed a similar cohesive shear failure through the bulk of the bumps, with a shear strength value of 190MPa.

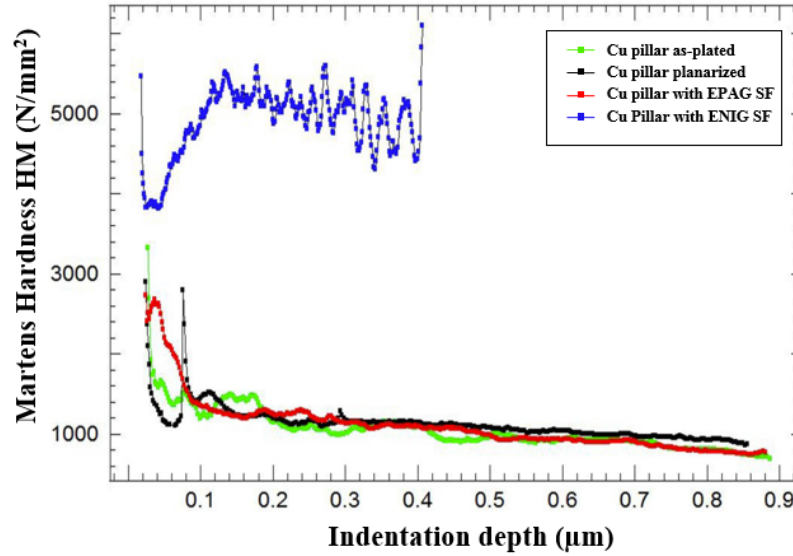


Figure 3.23 Martens Hardness (HM) v/s indentation depth for as-plated and planarized Cu bumps with bare-Cu, ENIG and EPAG surface finish layers

Grain-mapping of the Cu-EPAG bumps was carried out using an FEI Helios 660 FESEM tool with the experiment performed at a 70° tilt angle, 20kV of accelerating voltage and 3.2nA electron beam current. The electron backscatter diffraction (EBSD) texture pattern was obtained with a 10ms dwell time at a step size of 40nm and an indexing rate of 85% was achieved. Figure 3.24 shows the mapped EBSD inverse pole figure (IPF) patterns for the planarized and as-plated Cu bumps with the colors of the grains representing the different crystallographic orientation with regards to the inverse pole figures shown in the inset. The EBSD maps for both the as-plated and planarized Cu bumps are characterized by large Cu grains in the 1-10 μ m size range with a fine-grained thin capping layer which is attributed to the EPAG surface finish. No observable difference is perceived in the grain orientation maps of the as-plated as well as the planarized Cu-bumps, suggesting the absence of a preferred crystallographic directionality to the grains in case of the planarized bumps. It has been shown from previous work that electroplated Copper self-anneals at

room temperature with low activation energy [128]. Thus, any high strain energies stored in the form of hardening defects such as twinning, surface voids, grain hardening etc. after planarization are released over a matter of days. This release of the strain energy is triggered through the recovery and recrystallization of the cold-worked grains on the surface, and promotes grain growth, therefore reverting back to the as-plated mechanical properties. As a result, the hardness values through nano-indentation as well as the grain orientation of the Cu bumps before and after planarization process remain the same.

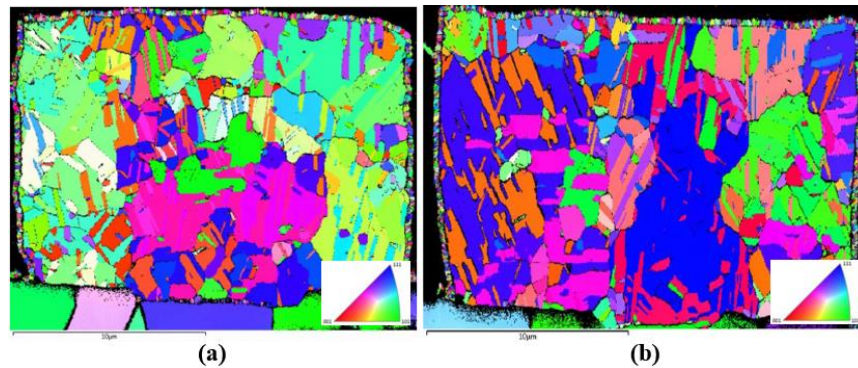


Figure 3.24 Z direction IPF grain orientation maps from EBSD characterization of (a) as-plated Cu bumps and (b) planarized Cu bumps respectively; inset shows the inverse pole figure color key

3.4.2 Validation of FEM models through assembly demonstration

3.4.2.1 Effect of surface finish

Due to force-limitations of the bonder (400N), it was not possible to carry out thermocompression assembly of the Cu-ENIG interconnections. Thus, only Cu-EPAG interconnections were considered in this study and in further sections. To verify the results from the finite element model on plastic deformation of the Cu bumps and pads, compression tests were also performed on TV1 with EPAG surface finish at 120MPa-250°C-3s to confirm the trends in collapse of the Cu bumps as a function of bonding

pressure. All assemblies were carried out with a semi-automatic Finetech Fineplacer Matrix flip-chip bonder with a placement accuracy of $\pm 3\mu\text{m}$. A $2.9\mu\text{m}$ collapse of the bump after thermocompression at 120MPa was measured at room temperature using the Olympus LEXT 3D Confocal Microscopy tool, as shown in Figure 3.25, matching the predictions of the FEM model from section 3.2.1. This was in contrast to the process-of-record (PoR) conditions of 365MPa bonding pressure established for Cu-ENIG interconnections and verified the predictions of the finite element analysis. This confirms the benefits of thin and soft Pd-Au layers in retaining compliance of Cu and enabling $3\mu\text{m}$ plastic deformation with 3X decrease in bonding pressure for improved throughput.

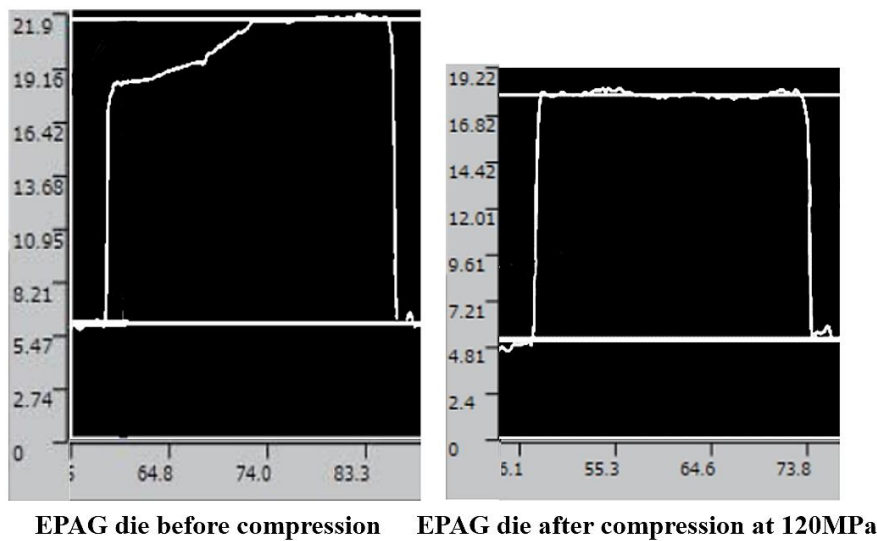


Figure 3.25 Confocal microscopy image of Si dies with EPAG surface finish at $t=0$ (left) and after thermocompression at 200°C -120MPa-3s (right).

3.4.2.2 Effect of planarization

To validate the predictions of contact modeling for as-plated v/s planarized assemblies, the $40\mu\text{m}$ pitch TV2 with planarized and as-plated Cu bumps was utilized. Flip-chip thermocompression bonding was carried out using the same Finetech Matrix bonder. To

ensure strong metallurgical bonding of the Au interfaces, standard GGI assembly temperature and time of 250°C and 5min, respectively, were applied, while the bonding pressure was varied from 100-300MPa. In total, 30 assemblies were built, 15 for each TV with as-plated and planarized Cu bumps. The quality of this bonding was assessed through die shear testing on a Dage Series-4000PA Shear Tester. A range of 10kgf was selected on the die shear cartridge according to the MIL-STD-883G Method 2019.7 standard used for bonding strength evaluation of bumped interconnection technologies. The shear speed was set at 15µm/s while the shear height was set at 6µm above the top of the substrate surface. The shear tester gave a maximum load reading in kgf before failure, which was converted to MPa for ease of benchmarking. It can be observed from Figure 3.26 that the shear strength values steadily increase for both as-plated and planarized assemblies with a maximum shear strength of 190MPa achieved for planarized assemblies at 300MPa – 250°C – 5min bonding conditions, while that of as-plated assemblies shows a maximum of 120MPa at similar bonding conditions. It is important to note that the maximum shear strength of 190MPa correlates well with the cohesive shear strength of Cu bumps at 190MPa, thus providing an established benchmark for the bonding strength.

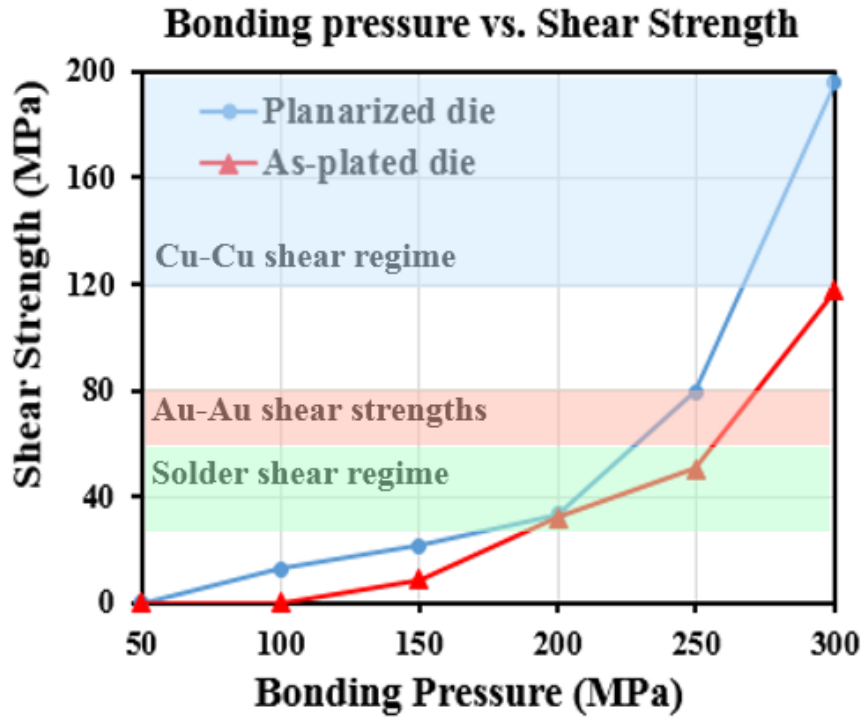


Figure 3.26 Shear strength v/s bonding pressure at 250°C – 5min for planarized and as-plated assemblies

The cross-sections of the assembled test vehicles were observed using a Zeiss Ultra-60 FESEM tool to carry out interfacial analysis. Figure 3.27 shows the SEM imaging of assembled planarized Cu-EPAG interconnections along with SEM-EDS elemental mapping of the individual metallic coating layers after assembly. In section 3.1.1.2, it was shown that bonding conditions of 5min-250°C, under ideal contact, would lead to a diffusion of 15nm across the bonded Au interface. This was verified using SEM-EDS scanning across planarized interconnections, as shown in Figure 3.28. The bonded interface is seamless due to: a) plastic deformation across atomistic flat interfaces coming into contact because of planarization of the Cu bumps; and b) quick self-diffusion of Au across the interface within 300s as predicted by the analytical model. The SEM-EDX scans do

show a broadened distribution of Copper across the interface while the Pd layer appears to be significantly dissolved in the Cu matrix.

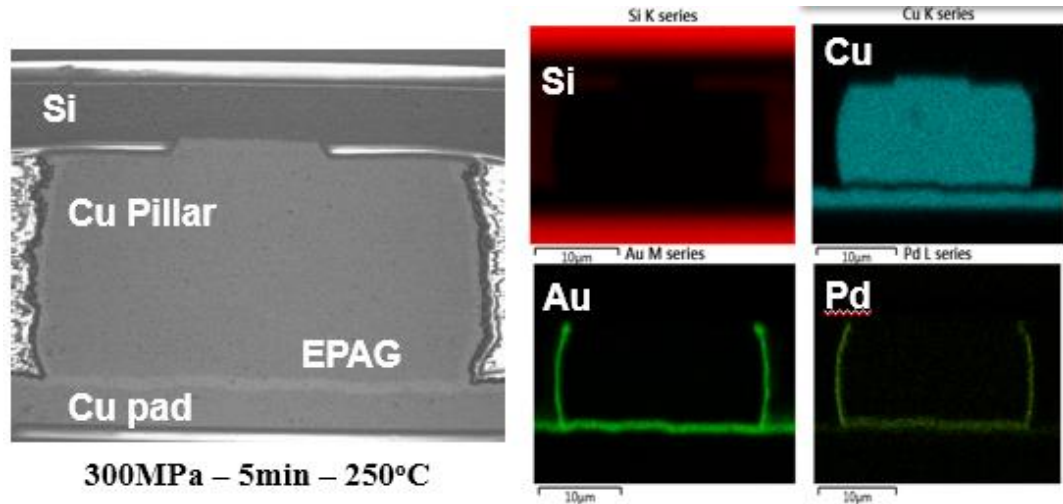


Figure 3.27 SEM cross-section of assembled as-plated Cu-EPAG interconnection with SEM-EDS elemental mapping of the interface

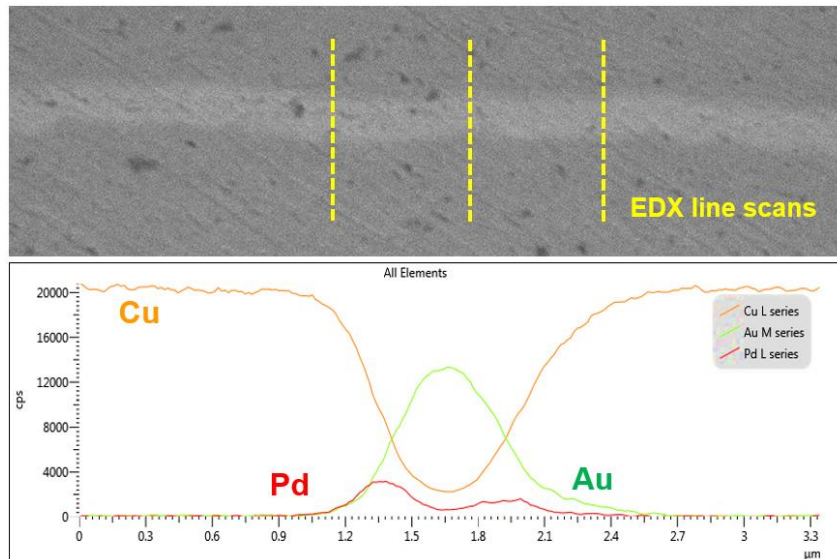


Figure 3.28 SEM-EDX mapping of as-bonded interface for Cu-EPAG planarized interconnections

3.4.3 Hi-speed assembly with TC-NCP

This section aims at understanding the basics of thermocompression bonding (TC-bonding) with pre-applied underfill, considering interactions between process, materials, bonder for process design in production conditions. From the previous results, we know that under appropriate bonding time, temperature and pressure, Cu-EPAG interconnections have been shown to form stable Au-Cu IMC phases with high bonding strength. However, the time required to form these stable IMCs is quite high from a manufacturing standpoint. To improve assembly manufacturability, a 2-step process is proposed with: 1) a quick thermocompression bonding step (<1min) with pre-applied underfill to create plastic deformation and initiate the bonding; followed by 2) a post-annealing step in a batch process that can coincide with the post-cure of the pre-applied underfill, bringing high throughput to the assembly process.

The general TC-NCP process recipe and corresponding evolution at each time step is described in Figure 3.29. The NCP is first dispensed on the bonding area with accurate volume control. After alignment under the bonder, a low-pressure step is applied until the low-viscosity point of the NCP material is reached, to ensure that the NCP spreads uniformly across the chip-substrate volume. An increased pressure is then applied when reaching the NCP's low viscosity point (t_1) to enable the ideal contact between Cu bumps and pads. With increasing temperature, the NCP is projected to be partially-cured at its gelation point (t_2) and applies hydrostatic compressive stresses on the now-formed Cu interconnections. Since the gelled NCP could contribute to the strength of bonding and confine the Cu bumps after t_2 , the evolution of high interest can be expected to happen mainly within the timeframe between t_1 and t_2 . A major difficulty in accurately predicting the right temperature – pressure – time profile is the deviation of the actual temperature

distribution from the nominal temperature set in the recipe depending on the thermal conductivity across the chip-substrate stack-up. Further, the gelation point of NCP is highly dependent on heating rates and shifts to higher temperatures as the heating rate is increased. By modifying the time between t_1 and t_2 , the behavior of the NCP's gelation point was optimized.

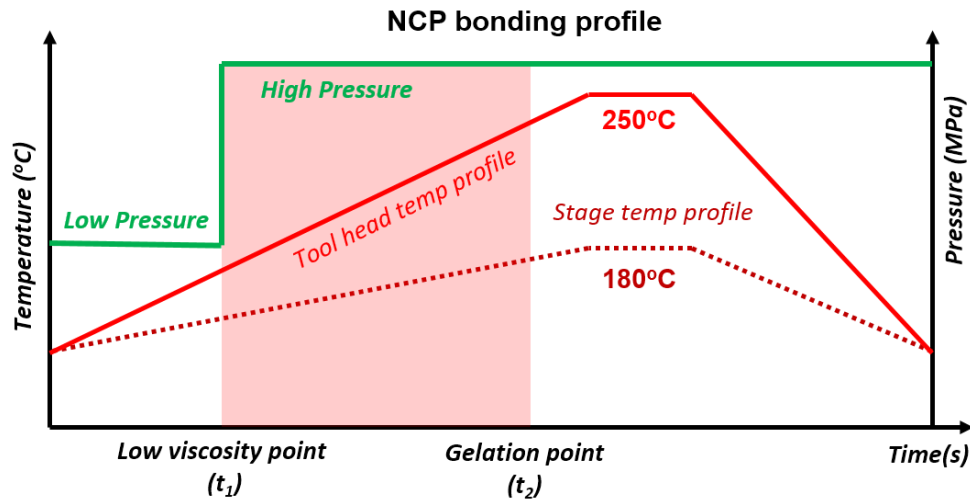


Figure 3.29 TC-NCP general bonding profile

A modeling of this curing kinetics behavior, carried out by Namics Corporation is presented in Figure 3.30 to illustrate this. A jump in gelation point from around 150°C to 230°C was observed by increasing the ramp rate from 2K/s to 200K/s. Such conditions correspond to the typical heating rates with lab-scale and production tools, respectively, showing the criticality of using production equipment to qualify pre-applied materials from their development phase.

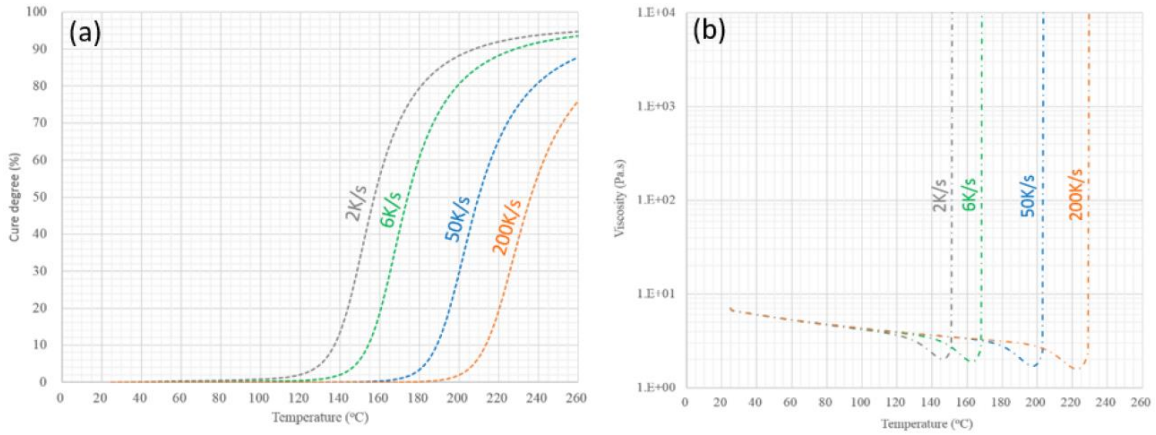


Figure 3.30 Simulation of (a) cure degree, and (b) viscosity with different heating rates (courtesy of Namics Corporation)

As we are limited to a lab-scale bonder with a maximum heating rate of 6K/s, co-design of the TC-NCP curing kinetics and thermocompression bonding process was carried out by varying the peak-temperature hold time and time of application of high pressure t_1 (low viscosity point). A differential scanning calorimetry (DSC) characterization was carried out on the NCP material provided by Namics Corp. at a heating rate of 10°C/min to ascertain the curing range between t_1 and t_2 (as shown in Figure 3.31). It was observed that the NCP reached its low-viscosity point at about 140°C, while reaching gelation by 225°C. TC-NCP assembly trials were conducted on TV3 test vehicle at 50μm pitch with CTE-matched Si substrates as well as 2-metal-layer 100μm-thick glass substrates with EPAG surface finish. The tool head peak temperature and stage temperatures were set at 300°C and 180°C respectively to enable assembly at 250°C within the Cu bumps. A force profile of 2MPa and 120MPa was used to ensure uniform spread as well as adequate contact between the Cu bumps and pads. All assemblies were then heat treated at 165°C for 1 hour to fully cure the NCP as well as create robust metallurgical bonds through diffusion ageing. Assemblies were carried out with variation in the peak-temperature hold time from 30sec

– 10sec to ensure high throughput. As a reference, assemblies were also carried out with previously established bonding conditions of 250°C – 5min to verify contact as well as the formation of a strong metallurgical bond at the interface.

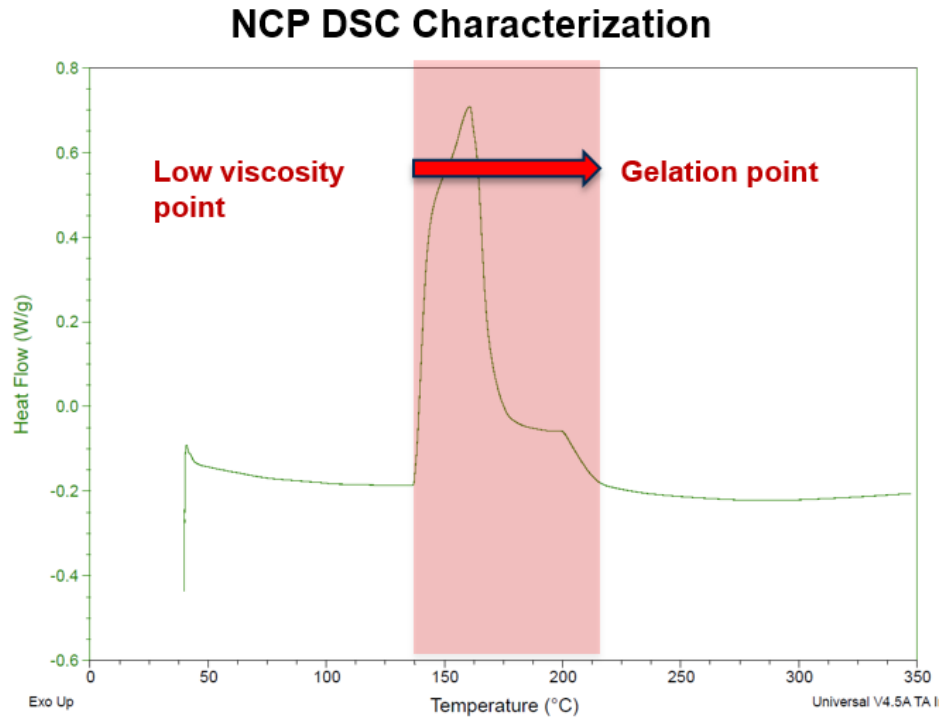


Figure 3.31 DSC characterization of NCP material

Scanning acoustic microscopy (C-SAM) was utilized to map voiding within the assemblies as a function of the peak-temperature hold time. It was observed, that under 5min, there was a significant amount of voiding in the assembly (as shown in Figure 3.32(a)) most likely due to the over-curing of the NCP material under-assembly causing non-uniform shrinkage across the assembled area. While a peak-hold time of 30 sec gave the most uniform spread of underfill across the bonded interface, subsequent cross-section of the assembly showed no contact due to the premature curing of the NCP before sufficient contact was created between the Cu bump and pads (Figure 3.33).

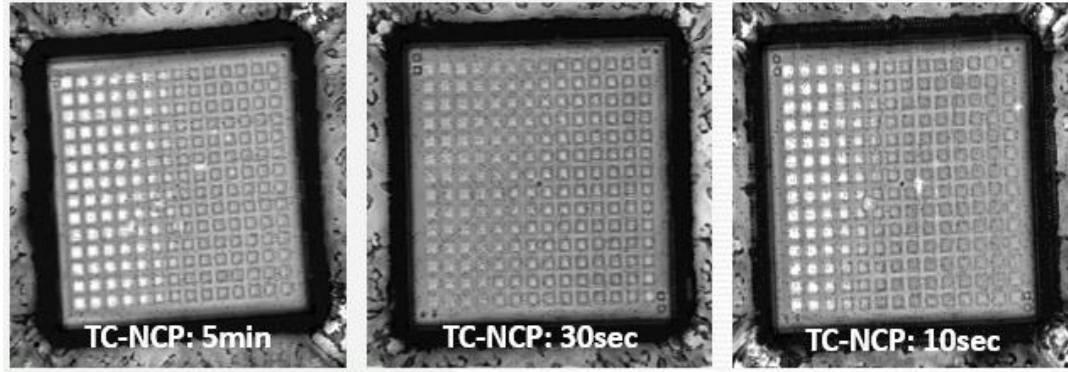


Figure 3.32 CSAM imaging of TC-NCP bonded assemblies with peak temperature hold times of (a) 5min, (b) 30sec, and (c) 10sec

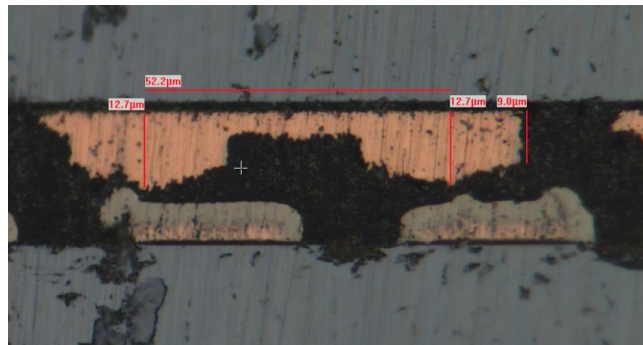


Figure 3.33 Cross-section of prematurely-cured TC-NCP bonded assembly with 30 sec hold time at peak temperature

Further optimization was carried out by varying the time to low-viscosity point (t_1) to ensure that the NCP material would begin curing only after sufficient contact was created between the Cu bumps and pads. This has been depicted in the bonding profile schematic of Figure 3.34(a). Figure 3.34(b)-(d) shows C-SAM images of assemblies with t_1 varying from 30sec – 5sec, with a t_1 of 20sec giving the most uniform coverage of NCP with sufficient contact. A comparison of the SEM cross-sections is shown in in Figure 3.35(a) for assemblies with previous thermocompression process with capillary underfill and the new optimized TC-NCP process with a t_1 of 20s and peak temperature hold time of 30s. The self-diffusion of Au atoms under the 2-step TC-NCP process (250°C-30sec + 165°C-60min) is verified to be very close to that observed with a 250°C-5min process with an

$X_{\text{self-diffusion}} \sim 10\text{nm}$, thus bringing about parity in joint strength and interfacial composition across both the approaches.

Thus, a significant improvement of 20X in the total cycle time for assembly was obtained using the TC-NCP process. Further improvements in throughput can be obtained by using production assembly tools with heating rates in the range of 100-200K/s. SEM-EDS studies across the TC-NCP bonded interfaces demonstrated the formation of a stable Au interface akin to the results in the previous section. This further validated the 2-step TC-NCP process for high-throughput manufacturing, while forming strong metallurgical bonds. There are still some concerns regarding filler entrapment from the NCP material under thermocompression assembly that can potentially increase the contact resistance and bring about early failure of the joints through crack initiation and propagation. A detailed study is required to ascertain the interaction of filler – bonding interface as a function of the bump geometry.

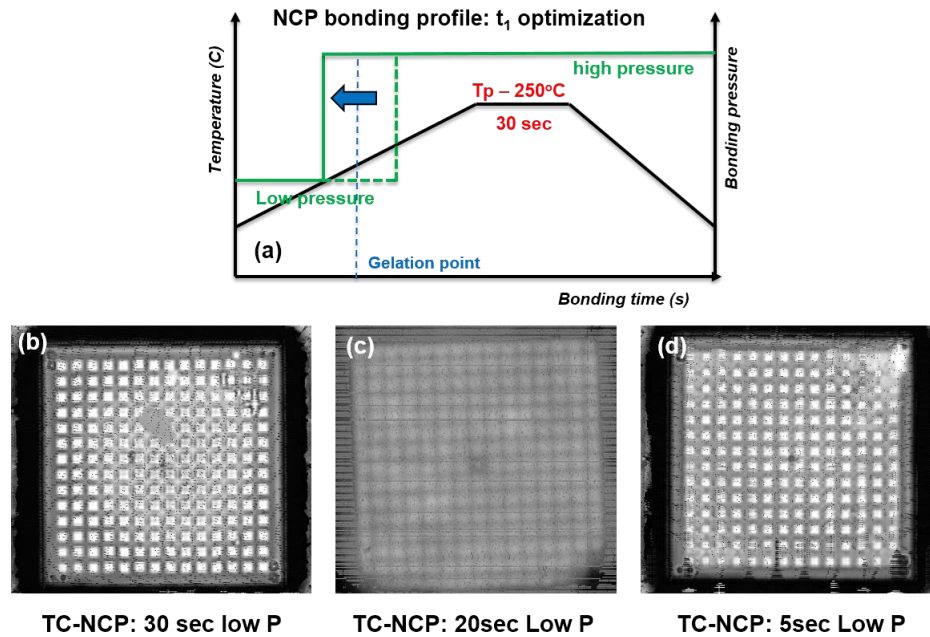


Figure 3.34 (a) Bonding profile with optimization of t_1 , and CSAM imaging of assemblies with t_1 of (b) 30sec, (c) 20sec, and (d) 5sec

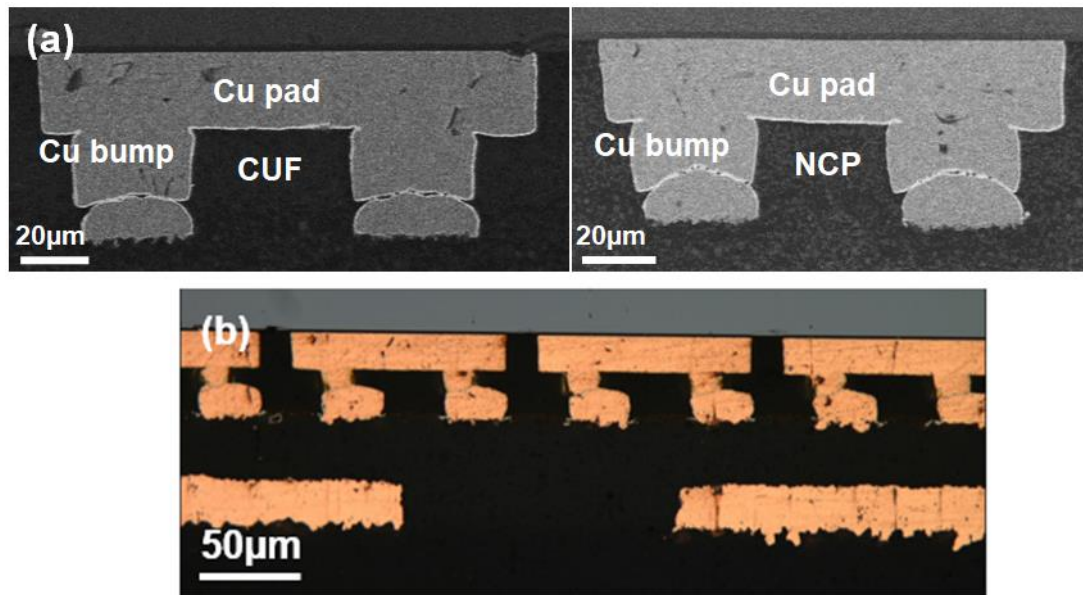


Figure 3.35 (a) SEM images comparing Cu-EPAG assembly with traditional CUF and new TC-NCP process; and (b) TC-NCP assembly on 100µm thick organic substrate with EPAG surface finish.

3.5 Thermal Ageing Test

A total of 52 assemblies for as-plated and planarized Cu-EPAG interconnections were built using the CTE-matched TV2 for thermal ageing test. A shear-strength based analysis was carried out as a function of bonding pressure under the bonding conditions of: a) Joint temperature – 250°C; b) 5min dwell time at peak temperature to create plastic deformation with adequate contact and promote diffusion; and c) bonding pressure varied from 100-300MPa. Results of thermal ageing studies on 26 as-plated interconnect assemblies, carried out at 200°C for 1,000 hours are shown in Figure 3.36. A continuous drop in shear strength to 26 ± 6.2 MPa at 1,000 hours was observed for the as-plated assemblies. A further SEM-EDS analysis of the sheared substrate interface shown in Figure 3.37 indicated the presence of CuO formed by thermal oxidation of the non-contacted areas as well as AuCu intermetallic at the contacted surfaces, thus validating the predictions of the diffusion model presented in section 3.1.3.2. The presence of CuO was further confirmed through high resolution XPS point scans of the failed interfaces. Insufficient contact caused Cu to diffuse through defect paths and form brittle CuO which further degrades the strength of the interface, ultimately causing failure at the Au – CuO interface. The presence of a highly deformable Au surface finish definitely improves diffusivity and ambient bond strength of the proposed technology. Furthermore, it was shown that the need to improve the contact area in bonding to decrease the surface asperities and prevent diffusion of Cu to the Au surface and its subsequent oxidation was acute.

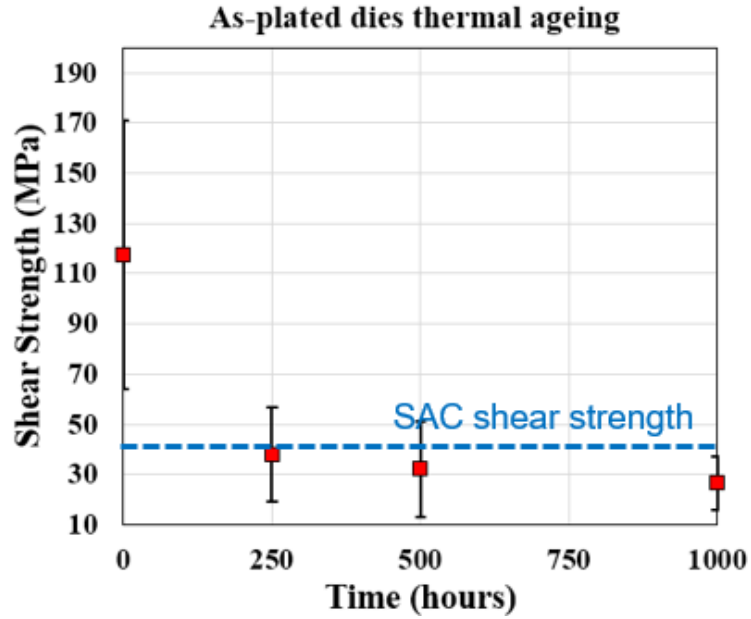


Figure 3.36 Variation in shear strength of as-plated Cu-EPAG assemblies as a function of thermal ageing time

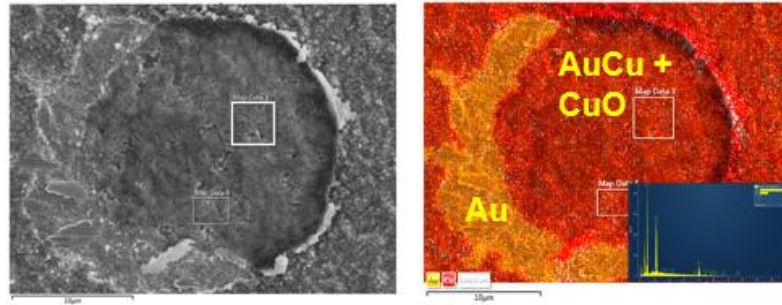


Figure 3.37 Interfacial failure across Au / Cu oxide interface after 1,000hours of thermal ageing at 200°C for as-plated Cu-EPAG assemblies with SEM-EDS enabled elemental mapping

As-bonded, the test vehicles with planarized Cu-EPAG bumps showed a maximum shear strength of 196 ± 2.6 MPa. On this account, 26 more test vehicles with planarized Cu bumps were assembled in the same conditions and subjected to thermal ageing studies at 200°C – 1,000 hours to compare with the previous results using as-plated Cu bumps. A sudden drop in shear strength to 62 MPa was observed at 250 hours after which the shear strength

stabilized to 40MPa (comparable to Sn-Ag solders) at 1,000 hours. This comparison between the thermal ageing performance of the assemblies with as-plated and planarized Cu bumps has been shown in Figure 3.38. SEM imaging of the sheared substrate interface confirmed a ductile failure at the bonding interface evident from the dimpled morphology while SEM-EDS established the presence of only Au and AuCu intermetallic at the bonding interface as shown in Figure 3.39. Thus, formation of a stable ductile AuCu phase through Cu-Au interdiffusion caused the observed degradation in shear strength and failure at the Au-AuCu interface at 250 hours. However, the presence of a stable AuCu phase and the absence of the brittle CuO phase due to better contact area enabled stabilization of the microstructure and improved reliability of the bonding interface under thermal ageing over 1,000 hours.

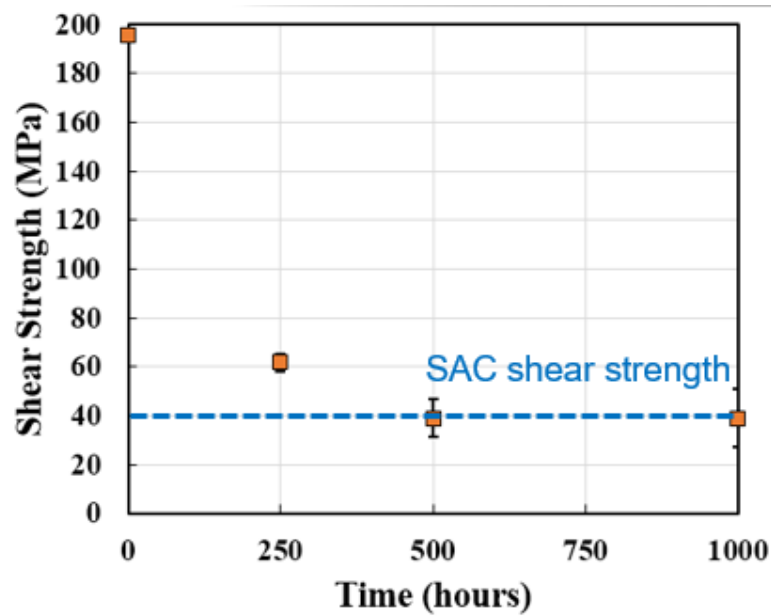


Figure 3.38 Variation in shear strength of planarized Cu-EPAG assemblies as a function of thermal ageing time

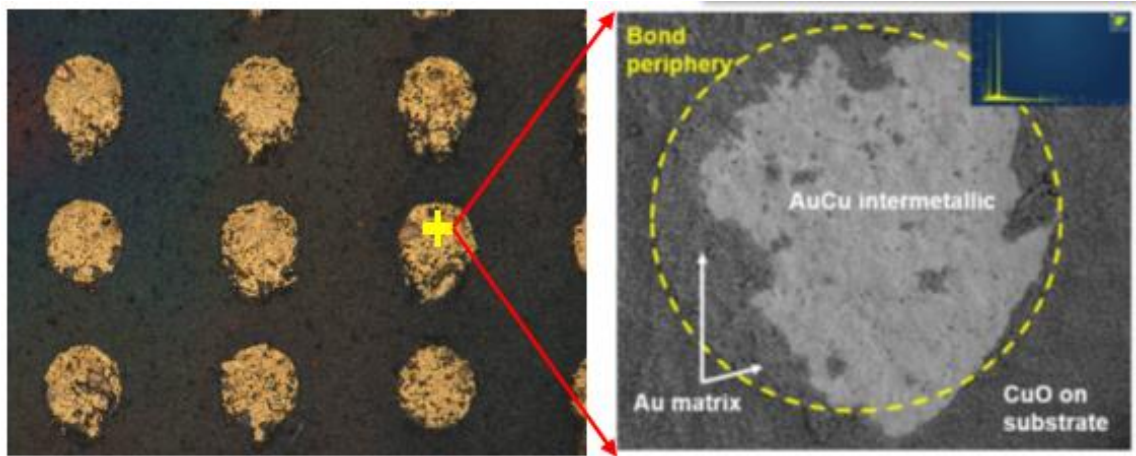


Figure 3.39 Interfacial failure across AuCu / Au oxide interface after 1,000hours of thermal ageing at 200°C for as-plated Cu-EPAG assemblies with SEM-EDS enabled elemental mapping

On comparing the SEM-EDS line scans across the bonded interfaces for as-bonded and parts thermally aged for 1,000 hours, it can be seen from Figure 3.40, that, initially, while the Pd layer instantaneously diffuses into the Cu bump during bonding, there is not enough driving force for the Cu to diffuse completely through the outer Au layers to form stable AuCu IMC phases. However, after 1,000 hours of thermal ageing, a uniform AuCu IMC interface is formed across the ~500nm of bonding interface, thus also verifying the diffusion model from section 3.1.4.2 Thus, fly-cut planarization helps in improving contact across bonded interfaces by removing surface asperities and increasing the true contact area under assembly.

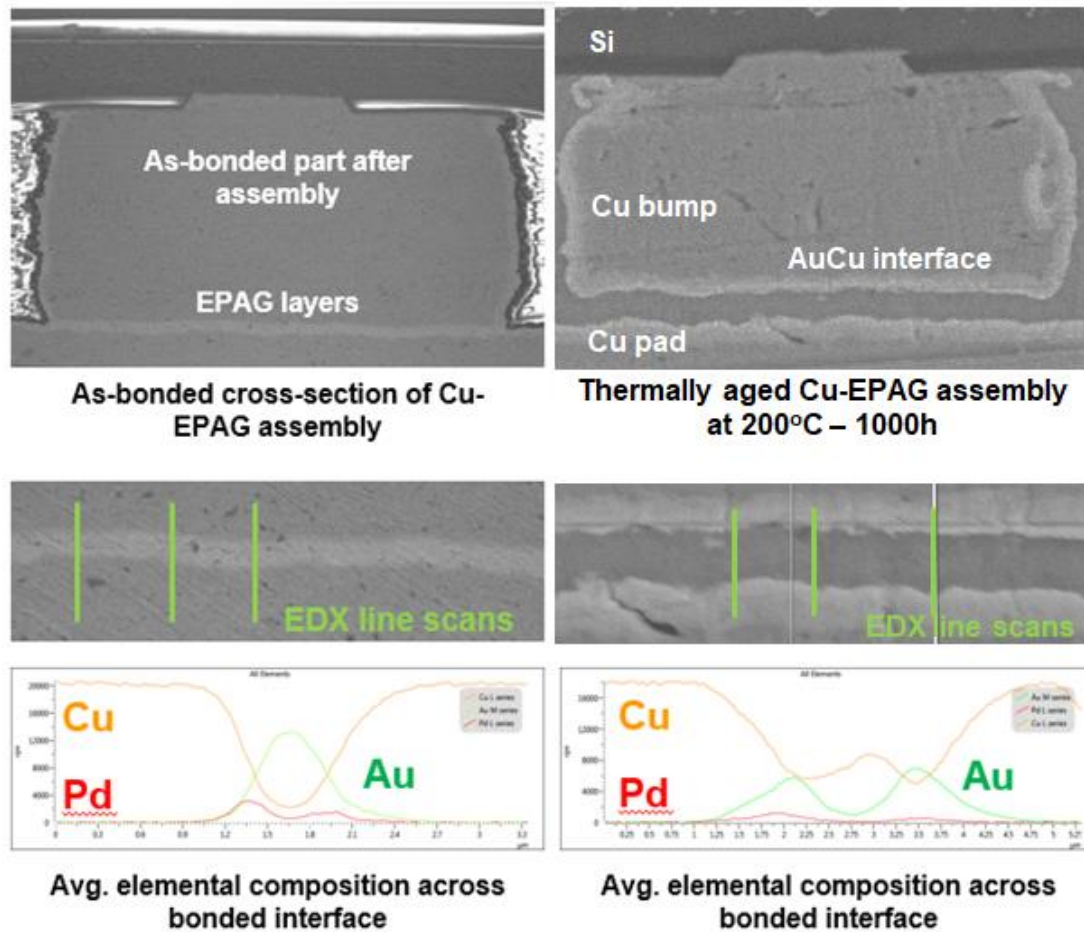


Figure 3.40 Average SEM-EDS elemental composition from line scans across the cross-sections of as-bonded and thermally aged Cu-EPAG assembly

3.6 Chapter Summary

This chapter went into the details of the material design and assembly demonstration of Copper interconnections with ultra-thin metallic coatings. Standard ENIG (Ni/Au) and novel thin-film EPAG (Pd/Au) surface finishes were considered in this study, leveraging autocatalytic processes traditionally reserved for substrate processing for low cost. Both interconnection systems were designed based on diffusion analysis and thermomechanical modeling to provide sufficient shelf life, and form strong and reliable metallurgical joints

at temperatures below 250°C, with stable microstructure through thermal aging at 200°C and power handling at 10⁵A/cm². Based on the diffusion and thermomechanical modeling, an optimized EPAG surface finish was utilized with minimum 250nm of Au to ensure improved shelf-life, low-temperature bonding profile with a 3X reduction in bonding pressure and reliable post-assembly performance. Furthermore, through rigorous contact modeling, the need for planarized Cu pillars with low stress-distribution profile was established. Concurrently, design rules were developed for as-plated and planarized Cu bumps to limit the substrate pad thickness to below 7µm to prevent buckling and rippling of the traces under assembly. Proof-of-concept bump compression tests verified the 3X reduction in pressure on using EPAG surface finish. High-strength planarized Cu-EPAG interconnections were demonstrated with bonding parameters of 250°C – 5min, under varying bonding pressure with a maximum strength of 195MPa. To improve throughput, a hi-speed 2-step TC-NCP process is introduced with a snap-cure assembly step and a full-cure batch-anneal step at 165°C – 1hr. The bonding parameters are further refined to 120MPa – 250°C – 30sec peak hold time, bringing about a 20X improvement in the entire cycle throughput as compared to previous assemblies. Finally, a successful demonstration of the thermal stability of planarized Cu-EPAG interconnections was demonstrated through high temperature storage testing was carried out at 200°C for 1000h. The failure mechanisms for as-plated joints were attributed to Cu diffusion and detrimental surface oxidation under non-contact areas, while that for planarized Cu-EPAG joints was attributed to a stable bulk-failure through a stiff IMC phase. The formation of 50-50 at% AuCu IMCs with ductile properties at the bonded interface was identified as the primary reason for this stability.

CHAPTER 4. RELIABILITY OF CU-EPAG INTERCONNECTIONS

In this chapter, the reliability of solid-state Cu interconnections is experimentally evaluated based on the objectives defined at the beginning of this thesis. A comprehensive finite element modeling of the interconnection system is provided to evaluate thermomechanical reliability in a chip-to-substrate architecture with potentially significant CTE-mismatch. This analysis is extended to understand the stress behavior of on-chip low-K layers under TC-NCP assembly conditions. Thermal stability of Cu-EPAG interconnections is tested through high temperature storage tests up to 1000h at 200°C. Thermomechanical reliability of ultra-thin glass packages assemblies using novel Cu-EPAG interconnections is demonstrated up to 1,000 cycles. Finally, a superior power handling capability is shown with an electromigration testing at a current density of 3×10^5 A/cm² for 1,000 hours.

4.1 Reliability Modeling

4.1.1 Thermomechanical reliability of Cu-EPAG interconnection system

The main concern of thermomechanical reliability when designing new interconnection systems is maintaining acceptable product life, in package architectures with CTE-mismatch and considering finer pitch interconnections with shorter stand-off heights and smaller diameters. While solder-based interconnections built using a thermocompression bonding process still retain the ability to accommodate thermal expansion stresses and strains, solid-state interconnections have a relatively high modulus and melting point, giving a low strain-retention ability. It was shown in Chapter 3 that on application of a 2-

step TC-NCP process, the pre-applied NCP material cures during bonding to create a state of hydrostatic compressive stress around the formed interconnections. While also vastly improving throughput, the aim of this compressive stress is also to protect the bonded interfaces and enhance thermomechanical reliability. To verify this, a FEM model was built to understand the effect of capillary underfill v/s NCP in a chip-to-substrate package design with varying CTE mismatch. A 2D geometry was built using ANSYS15.5 simulating the half diagonal of the assemblies (shown in Figure 4.1(a)), from the neutral axis to the corner. An assumption of plane strain condition was applied since the main deformation was expected to happen in in-plane direction. A total of 20 bumps were populated in this model with a bump diameter of $15\mu\text{m}$ at $30\mu\text{m}$ pitch. Figure 4.1 shows the detailed geometry used in this modeling, in which the proposed Cu-EPAG interconnections was assumed to be bonded on Cu pads with EPAG surface finish. Due to the inability of experimental validation for Cu-ENIG interconnections, ENIG surface finish was not considered in this model. Low-CTE glass and organic FR4 materials are considered for the substrate to understand the effect of CTE mismatch on reliability. The material properties considered in the model as tabulated in Table 3 and Table 4 in Chapter 3.

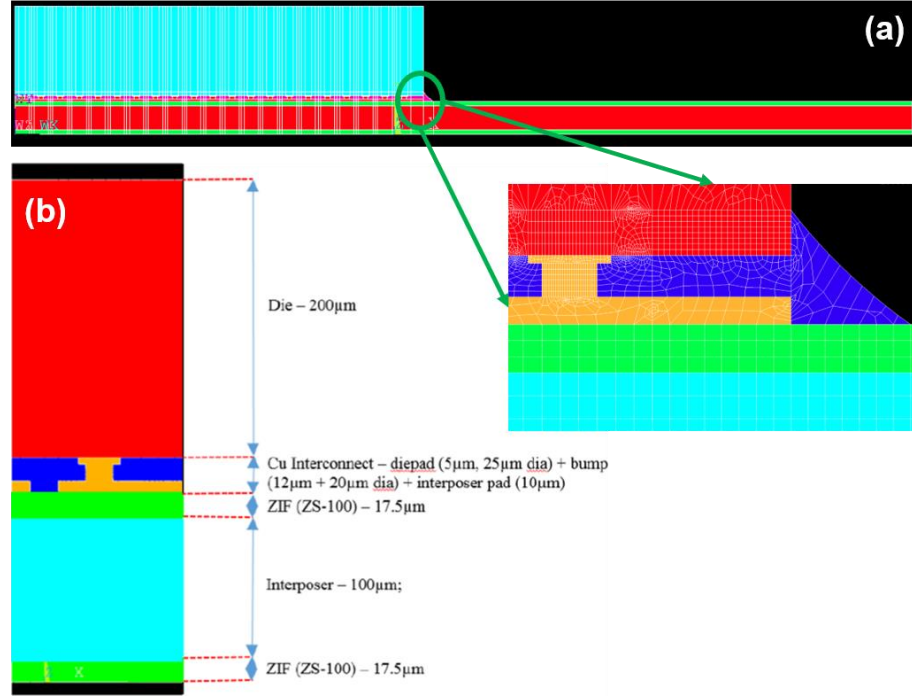


Figure 4.1 2D FEM model with (a) global geometry and (b) local features with modeled components

The material properties for the underfills are as tabulated in Table 3. The temperature of the bottom surface of the interposer is kept constant at 180°C and the heating of the die is modelled by applying a temperature profile to the top surface of the die. The pressure is also applied to the top surface of the die. The temperature and pressure profiles shown are chosen to represent the nominal profile during an actual process. The values of temperature applied to the die side are optimized to get a temperature of close to 250°C in the Copper bumps to simulate experimental bonding conditions. Similarly, the value of pressure is designed to get at least $\sim 1\mu\text{m}$ of displacement at the interface to emulate plastic deformation and planar contact across the entire bonded interface. A birth and death time-step method was used for birthing the capillary and NCP underfill materials during cool down after assembly. Further, the geometry was led through 5 loops of thermal cycling to

ensure that the plain strain range converged. The cycling condition was set referring to the JEDEC TCT Standard - Condition B within the temperature range of -55°C / 125°C with a rate of 2 cycles per hour.

The results of the Von Mises (VM) stress distribution after thermal cycling of Cu-EPAG interconnections assembled on FR4 and low-CTE glass substrates under common underfilling conditions are shown in Figure 4.2. The color map of the images was normalized to the scale bar and the value of stress was $\times 10^3$ times the scale in MPa according to the unit conventions chosen for this model. The maximum stress was observed at the Si – Cu interface on the die with a VM stress value of 289MPa, higher than the yield strength of electroplated copper (170MPa). While the glass assemblies showed a reduced VM stress value of 130MPa, the stress concentration is still along the Cu-Si interface. This suggested a potential failure mode across the die with lift-off of the Si die under fatigue.

Another potential failure mode would be interconnection fatigue by observing the equivalent plastic strain accumulation in both models after thermal cycling. Maximum plastic strain amplitude of 0.064 was observed for the organic package while that for the glass package was significantly lower at 0.008. The strain occurred across the diagonal nodes of the Cu bumps and suggested a shear mode of failure through the bulk of the Cu interconnection.

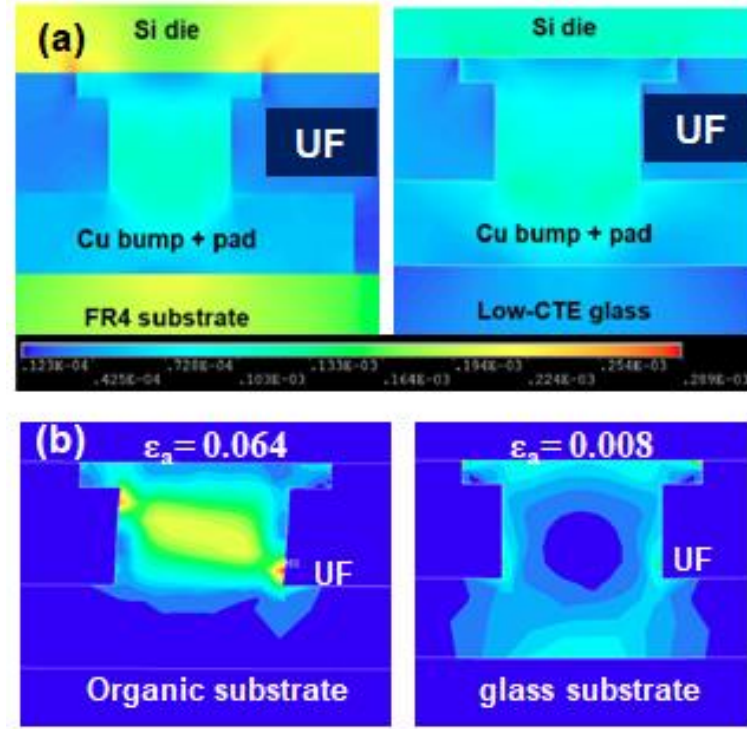


Figure 4.2 (a) VM stress distribution across organic and glass package; and (b) equivalent plastic strain distribution across organic and glass packages under common TC-UF conditions. The contour map for both models is normalized to the scale bar ($\times 10^3$ GPa)

By applying the short lifetime ($<100,000$ cycles) fatigue model given by the Coffin-Manson equation, an estimated lifetime of ~ 350 cycles was predicted for the organic package while a lifetime of ~ 1050 cycles was estimated for the glass assemblies. On using the Engelmaier-Wild equation [129, 130], the estimated lifetime was predicted to be ~ 500 cycles for the organic package and ~ 1200 cycles for the glass package. Table 5 compares these values with those for standard Cu pillar assemblies. The experimental lifetime of the packages generally lie between the estimates provided by these two models. As a result, we can see that there are two competing modes of failure as predicted from a first principle stress-based approximation and a plane strain-based approach. Thus, an experimental

justification and validation of these modeling results is required to determine empirical failure modes as well as design reliable chip-to-substrate packages.

Table 5 Plain strain models for estimation of fatigue life

Plastic strain models	Cu-EPAG assembly		Cu Pillar assembly
	Organic substrate	Low-CTE glass substrate	
Coffin-Manson	351	1050	300
Engelmaier-Wild	528	1230	400

Design of the interconnection geometry is very critical in ensuring that the stress across the interconnected interfaces are within yield-strength limits. Based on the VM stress analysis, a design study was conducted with variation in the aspect ratio of the Cu pillar as well as core substrate CTE, to manage the stress. It can be seen from Figure 4.3 that on variation of the aspect ratio from 0.6-1.5, the VM stress at the Cu-Si interface rises linearly, as the CTE of the substrate increases. To manage this stress below the yield stress of DC plated-Cu across a wide range of Cu pillar aspect ratios, the CTE of the substrate core should at the least be less than 10 ppm/K. Thus material innovations are required on organic and high-CTE glass substrates to ensure that the CTE-mismatch across the interconnections is reduced which, in turn, would improve the reliability performance.

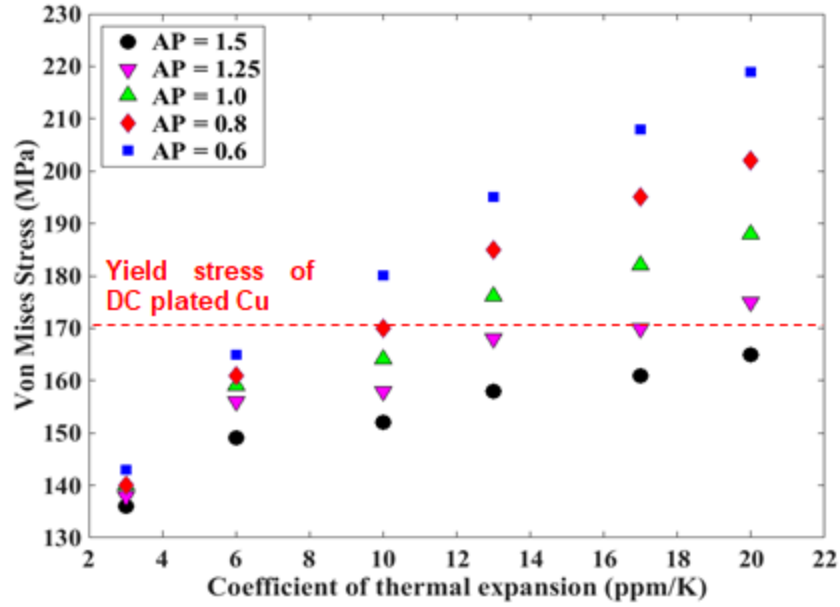


Figure 4.3 Von Mises stress as a function of substrate CTE

4.1.2 Low-K reliability at IC level

The shift from plastic- solder-based systems to rigid-elastic joints can yield potential cracking of on-chip ultralow-K dielectric layers, which is a major reliability concern. To understand this stress redistribution, a finite element model featuring a chip-to-substrate assembly with low-K dielectric stack-up was developed. Based on the inputs from the previous section, a similar interconnection model was built with a stack-up consisting of: a) a 400 μ m thick Si die; b) low-K dielectric layers with three layers of Cu connected to each through-vias; c) Cu bump and pads on both die and substrate side; d) NCP underfill material with a standard fillet size of 260 μ m; and e) organic FR4 and low-CTE glass substrates. The material properties for this model have been tabulated in previous modeling sections. The low-K dielectric considered was SiO_x with standard material properties. A schematic of this model is shown in Figure 4.4 for clarity.

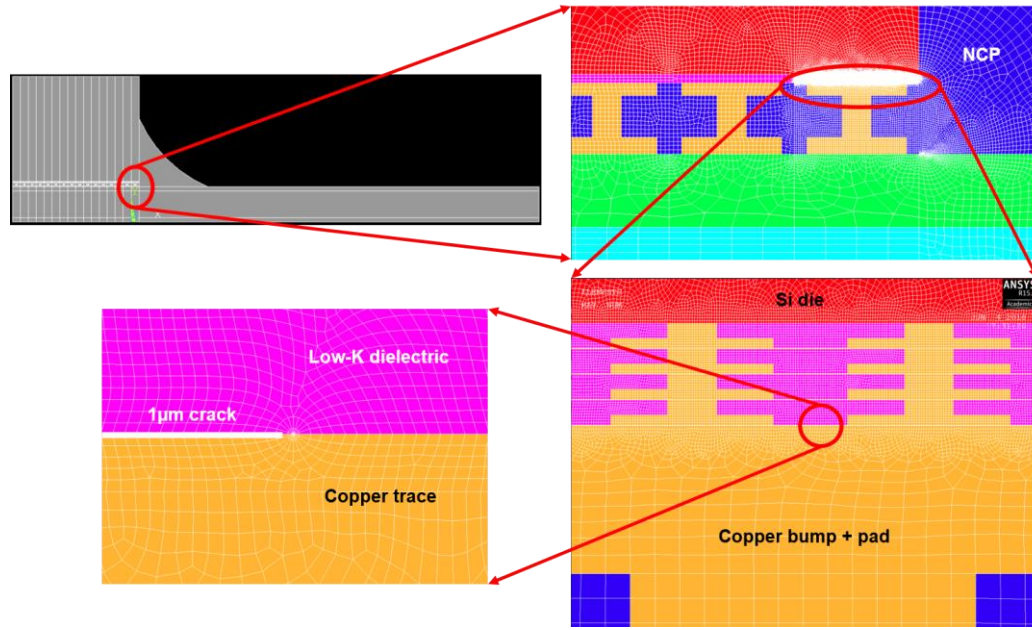


Figure 4.4 2D FEM geometry of chip-to-substrate assembly with low-K layers

A $1\mu\text{m}$ wide crack was initiated at the dielectric / Cu trace interface using crack-tip elements within ANSYS. Using an energy release-rate approach towards fracture modeling, J-integral contours were utilized to calculate the energy required to propagate this crack. This crack propagation was evaluated under the effect of variation in geometry and material property parameters. A critical fracture toughness value of $G_0 = 5 \text{ J/m}^2$ was used as a failure criterion for the opening of the crack at the dielectric / Cu trace interface. Any value above this critical energy would signify crack propagation and subsequent failure across the low-K layers. The assembly was simulated to cool down under a single time step from bonding conditions of 250°C to 25°C . the NCP material was modeled in the fully cured state at 250°C down to ambient conditions. The J-integral values were normalized to the critical fracture toughness of 5 J/m^2 and are plotted against variation of substrate: Silicon, low-CTE glass and organic substrate with a CTE increasing from 2.9 to

3.6 to 17ppm/K respectively. It can be seen from Figure 4.5 that assembly on organic substrates with high-CTE mismatch and without the use of NCP can create significant stress concentrations at the low-K layers with energy release rates higher than that of G_0 . On the birthing of NCP materials, it is seen that there is significant reduction in this G -value on account of the compressive stresses applied by the cured NCP. Even with the application of NCP, the energy release rate is higher than that of G_0 thus giving high risks of crack propagation and low-K failure. On the other hand, since low-CTE glass has a CTE very close to that of Si, the energy release rate is quite low as compared to G_0 and the low-K layers are effectively well protected. Thus, the model predicts that to ensure prevention of low-K failures in a chip-to-substrate architecture, TC-NCP bonding with a low-CTE substrate core is preferred, as expected. Further advances in NCP material characterization are required to modulate the degree of shrinkage and hydrostatic stresses under full-cure for applicability to high-CTE organic laminates.

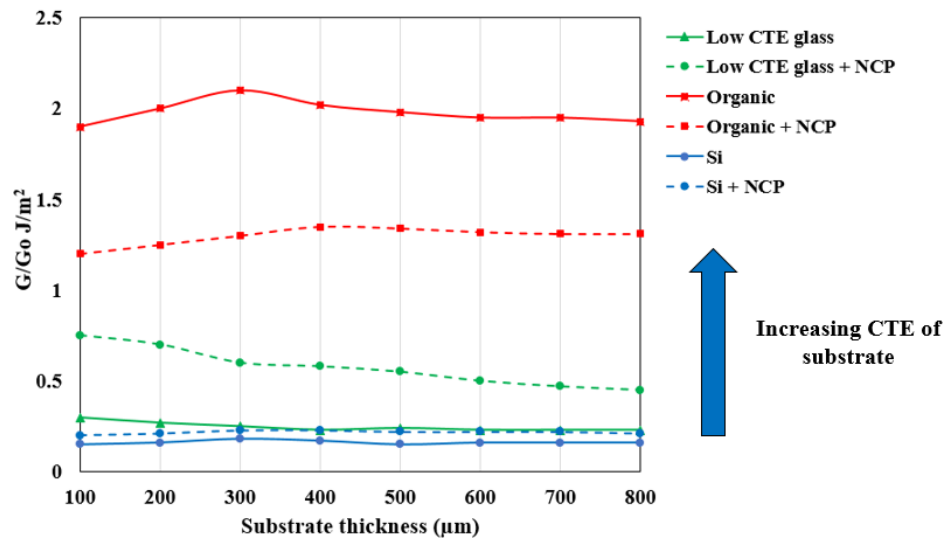


Figure 4.5 Variation of crack energy release rate as a function of substrate thickness for assemblies on Si, low-CTE glass and organic substrates

4.2 Thermomechanical Reliability

The daisy-chain test vehicle of TV1 was used for a preliminary demonstration of thermomechanical reliability of Cu-EPAG interconnections at 100 μ m pitch. A total of 15 samples were built under the assembly conditions of 250°C – 250MPa – 5min as outlined in section 3.4.2.2 towards forming strong metallurgical bonds with shear strengths >75MPa. To emulate the results from the modeling section above, a capillary underfill was used to protect these assembled parts after a full cure at 165°C – 3hrs. A first screening of thermomechanical reliability was carried out by subjecting assemblies to MSL-2 pre-conditioning, followed by thermal shock test from -55°C to 150°C, with a dwell time of 5 min at each temperature extreme and 6 cycle/h in accordance to JEDEC-JESD22-A113F standards. These standards are generally used for automotive grade testing and lie at the most extreme end of the reliability testing spectrum. Each assembled test vehicle comprises 8 daisy chains. The daisy chain resistances were monitored up to 1,000 cycles. The yield of the assemblies has been plotted as a function of test cycles in Figure 4.6.

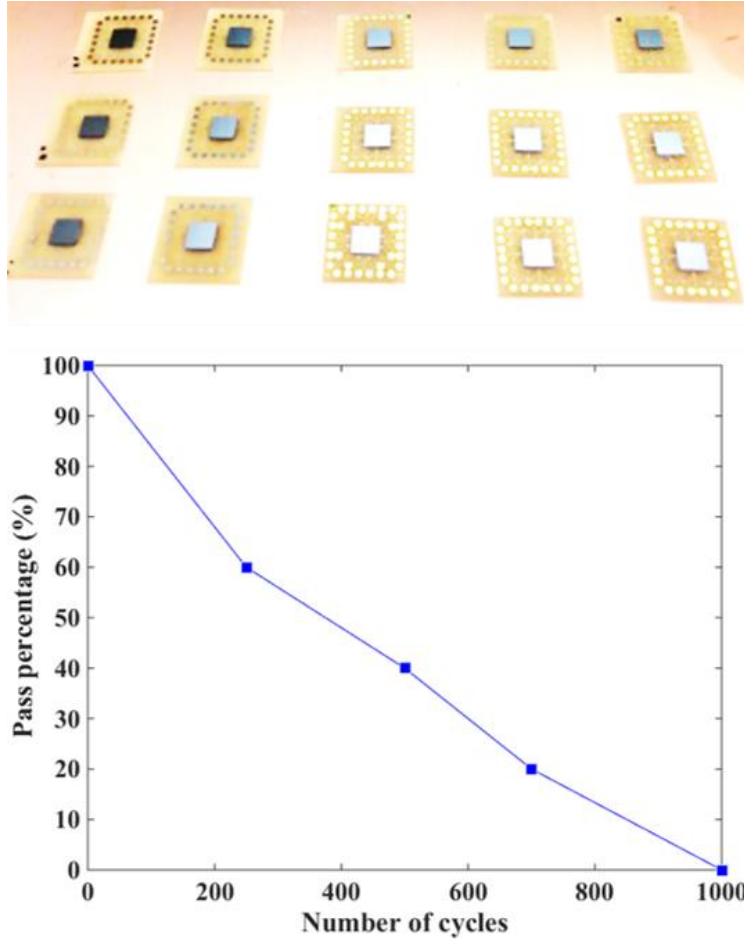


Figure 4.6 Image of the 15 assemblies in TV1 configuration used for thermal shock testing (above) and a graph showing pass percentage / yield as a function of TST cycles (below).

No change in resistance was observed during the pre-screen. However, the yield of the assemblies dropped significantly within 250 cycles under the harsh environments and continued dropping to zero yield at 1,000 cycles. It was observed, that most assemblies had sheared at the Si die - Cu seed layer interface while the Cu-EPAG interconnections themselves were intact. An optical micrograph of these failed samples is shown in Figure 4.7. The die-cracking was presumed to be a result of extremely high strains accumulated at the Si - Cu interface due to CTE mismatch. These results validate the findings of the FEM model in from the previous section.

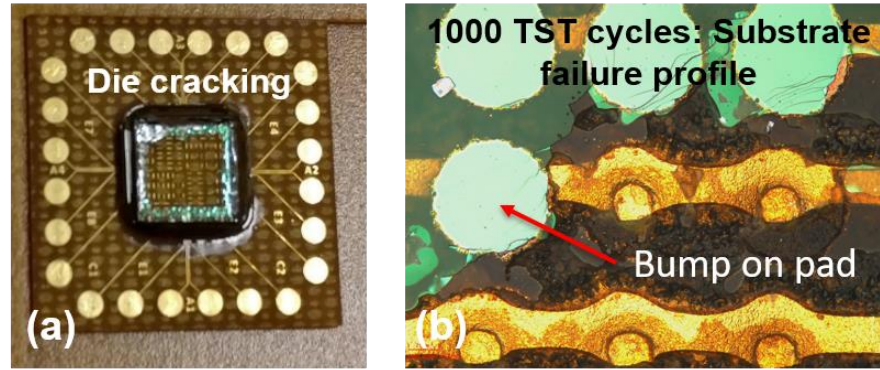


Figure 4.7 (a) Top view of the failed TV1 sample after 1,000 cycles and (b) Optical image of failed interface showing delamination at Si/Cu seed interface, with Cu-EPAG bumps intact on the substrate

To further verify the model, a total of 8 assemblies were built using the TV3 configuration on 100 μ m-thick glass substrates. Si dies with Cu-EPAG bumps planarized using fly-cut planarization were used for this study to improve contact. The fabrication of these glass substrates has been outlined in section 3.3.3. The assembly process was designed based on the TC-NCP bonding results from Chapter 3 with a t_1 value of 20sec to the low-viscosity point of the NCP and a peak-temperature hold time of 30sec at 250°C. After pre-conditioning, the assemblies were subjected to thermal shock testing from -55°C to 125°C with a dwell time of 15 minutes at each temperature extreme at 2 cycles/hr in accordance with JEDEC-JESD22-A104C standards. Each assembled test vehicle comprised of 16 daisy chains and monitoring was carried out until 1,000 cycles as shown in Figure 4.8(a). A change in resistance by 20% was identified as the failure criterion for reliability. Early failures within the samples in the as-bonded condition were attributed to process defects on the glass substrates including undercutting of traces and skip plating of surface finish as outlined in Figure 4.8(b). Only 3 daisy chains were observed to fail between 0-1,000 cycles. These intermediate failures were caused by entrapment of fillers from the NCP material at the bonding interface, leading to non-planar bonded interfaces (Figure 4.8(c)).

Filler entrapment has become a major reliability concern in fine-pitch interconnections with short stand-off heights and along with increase in filler content in advanced pre-applied NCP materials for desired properties. This hurdle has yet to be fully addressed by the semiconductor industry. These fillers act as nucleation points for crack growth due to localized plastic strain at the interface, giving rise to cracks and open failures of the joints.

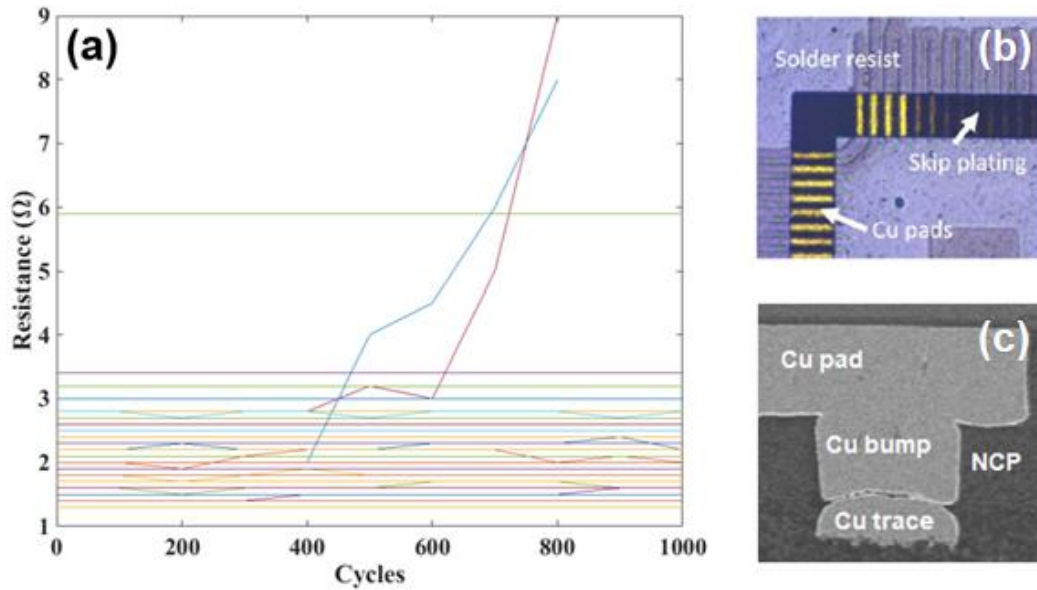


Figure 4.8 (a) Daisy chain resistance monitoring up to 1,000 cycles and (b) early failures through fabrication defects on glass substrates; and (c) TCT failure due to filler entrapment

As diffusion across such bonded interface was hindered, the degradation reliability of these joints was expected. Most of the daisy chains survived the thermal shock test with a final yield of 89% after 1,000 cycles. Thus, thermomechanical reliability of Cu-EPAG interconnections assembled with the 2-step TC-NCP process on low-CTE glass substrates was demonstrated.

4.3 Electromigration Test

For electromigration analysis, a Si-matched test vehicle with TV3 configuration at 50 μ m pitch was utilized planarized Cu-EPAG interconnections were considered in this study. The Si substrate utilized had an ENIG surface finish with 4 μ m-thick Ni and 100nm Au layers. This was used to simultaneously observe the effect of current stressing across Cu-Pd-Au-Ni-Cu layers. The samples were bonded using the developed 2-step TC-NCP process (outlined in section 3.4.3) and with the NCP being fully cured post assembly after thermal treatment at 165°C – 3hrs. The test was conducted through a manual setup using a Keithley 236 Source-Measure Unit. Constant current was supplied to a central daisy chain of area-array test vehicle, which consisted of 15 bumps in series. Based on the bump-to-pad contact area, the maximum allowable current through the source was 1A, providing a current density of 3×10^5 A/cm². The samples were kept in an Espec thermal chamber at a constant temperature of 130°C and voltage measurements were taken manually every 24 hours to calculate the resistance of the corner daisy chain. A 20% increase in resistance was considered as a failure criterion for the electromigration test. A schematic of the EM test vehicle has been shown in Figure 4.9 and SEM cross-sections of the EM assemblies after 500h are shown in Figure 4.10 with labeled current directions. No failures were observed in the samples after 1000 hours of current stressing. The driving force for electron-wind initiated diffusion flux has been shown to be 100X that of thermally-initiated diffusion flux. This was observed in the Cu-Pd-Au thin-film system, where the Pd layers were completely dissolved into the Cu matrix and a continuous layer of CuAu intermetallic (50-50 atomic%) was formed across the bonded interface.

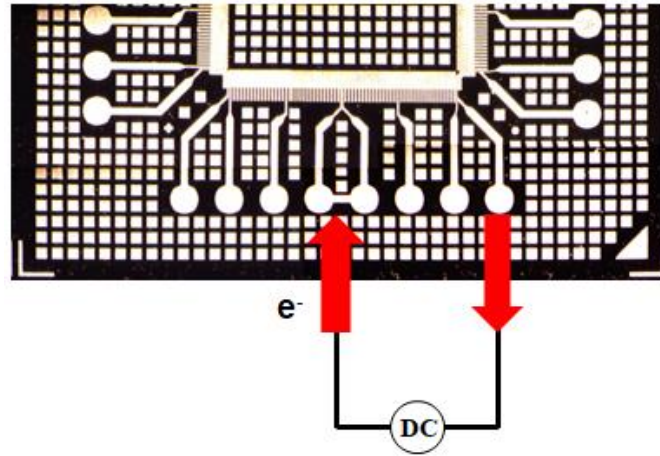


Figure 4.9 TV3 layout showing probed daisy chain and direction of current

Furthermore, massive dissolution of Cu at the cathodes is expected under electromigration testing of solder-interconnections due to the high diffusivity of Cu in the Sn matrix. However, with the presence of an Ni-P barrier and very thin CuAu intermetallic phase, the dissolution of Cu from the electrodes (Cu bump and Cu pads) was not observed with very limited Kirkendall voiding at these current densities across both current flow directions. Thus, the performance is expected to remain the same in the case of a pure Cu-EPAG interconnection without Ni-P barrier. This validated the results of EM modeling from section 3.1.4.1 and demonstrated the high power-handling capability of the proposed Cu-EPAG interconnections under current stressing at $3 \times 10^5 \text{ A/cm}^2$.

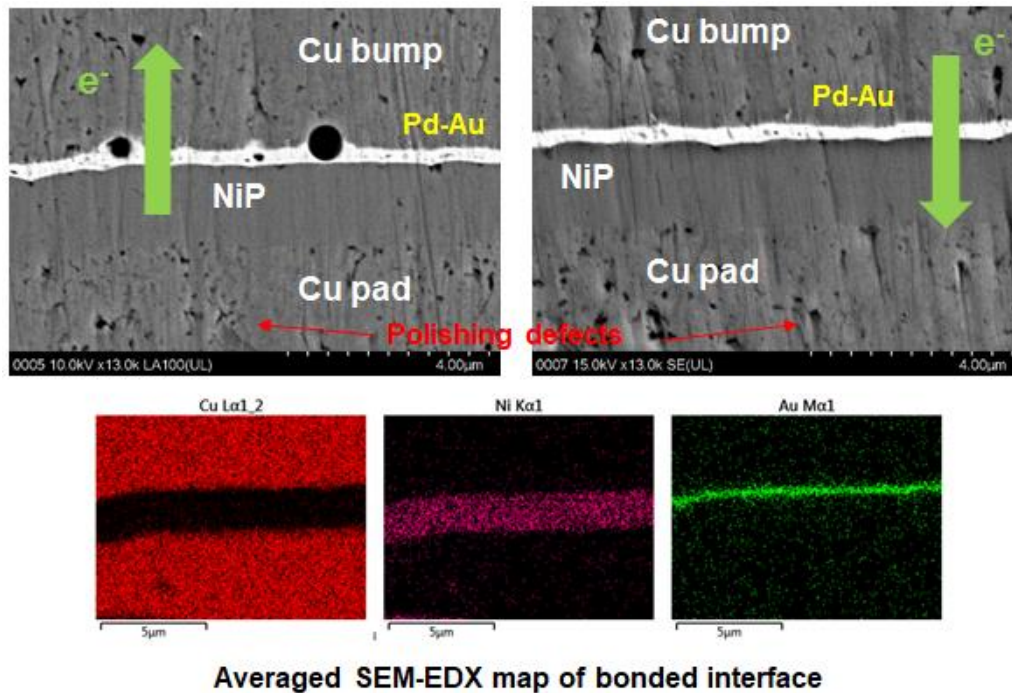


Figure 4.10 High power handling at 3×10^5 A/cm² at 130°C – 500h demonstrated on planarized Cu-EPAG interconnection assemblies at 50μm pitch

4.4 Summary of reliability characterization

A comprehensive analysis of reliability of Cu-EPAG interconnections from modeling, to experimental validation was provided in this chapter. A major concern with solid-state interconnections is their inability to retain strain, thus giving a shift in the failure mode as compared to traditional fatigue failure of solder interconnections. Two competing modes of failure were predicted across organic and glass chip-to-substrate packages. While the VM-stress based approach predicted an adhesion mode of failure, the plane strain approach predicted a shear mode of failure. To validate these predictions, thermomechanical reliability, targeted especially in package designs with substantial CTE mismatch, was preliminary demonstrated with FR-4 organic substrates at assembled conventionally at 100μm pitch, while also successfully scaling down to TC-NCP assembly on 100μm-thick

low-CTE glass substrates at 50 μ m pitch which passed over 1,000 thermal-shock cycles. Furthermore, the predicted failure modes were also validated through experimental results and design rules correlating the aspect ratio of Cu bumps and CTE of substrate core were developed. The shift from plastic solder-based systems to rigid elastic joints can yield potential cracking of ultralow-K dielectric layers on-chip, which is a major reliability concern. To understand this stress redistribution, finite element modeling featuring a chip-to-substrate assembly with low-K dielectric stack-up was developed. It was shown that under assembly, the pre-applied NCP materials applied compressive stresses on curing and brought down the energy release rate at the crack-tip, thus effectively preventing crack propagation in the low-K layers. Under electromigration testing, the Cu-EPAG interconnections showed excellent electromigration resistance under current stressing at 3×10^5 A/cm² – 130°C for 500h, demonstrating high power-handling, beyond the capability of traditional solder-based interconnections. Consequently, the feasibility of novel Cu-based interconnections with the high-performance of copper and compliance, aided by low-cost planarization has been demonstrated for advanced computing applications of the next decade.

CHAPTER 5. CU PILLAR INTERCONNECTIONS WITH NANOCOPPER FOAM CAP

Cu pillars interconnections with nanocopper foam caps are proposed as a novel Cu interconnection technology with improved assembly throughput, manufacturability and reliability. These interconnections have the following attributes: 1) sub-20GPa Young's modulus as-bumped to provide high tolerance to surface roughness, non-coplanarities, and warpage; 2) low-cost fabrication processes through electrodeposition of a Cu-Zn alloy and chemical dealloying, compatible with standard lithography processes; 3) pitch scalability given by solid-state bonding; 4) highly-reactive nano-surfaces enabling low-temperature densification to achieve bulk-like properties after assembly. This chapter first details the motivation and design of nanocopper foams towards novel interconnection systems. Based on a preliminary proof-of-concept bonding demonstration, a more manufacturable fabrication route using co-electrodeposition and patterning is established and demonstrated. A critical understanding of sintering kinetics in nanocopper foams is developed and contrasted to that of nanoparticle-based systems. Finally, assembly of Cu pillar interconnections with nanocopper foam caps is demonstrated.

5.1 Interconnection System Design

5.1.1 Motivation for low-modulus Cu interconnections

FEM modeling of the deformation behavior of bulk Cu interconnection systems during thermocompression bonding highlighted risks of failure in low-K on-chip dielectric layers and of delamination of the Cu traces on substrates. While fly-cut bump planarization was

demonstrated to successfully mitigate these stresses, the results from reliability testing point that even this is not enough to accommodate stress from CTE-mismatch. Thus, a technology with built-in compliance giving similar tolerance to non-coplanarities than solders with high processability, would be highly desirable to address this challenge without the need for any post-processing step. A novel interconnection concept is, therefore, proposed and explored, consisting of a highly compliant, low-modulus Cu bump. During thermocompression bonding, plastic deformation should be mostly confined within the bump to reduce risks of low-K failures and delamination, while still providing a sufficient driving force to enable metallurgical bonding of the mated interfaces. To validate this concept, a finite element model was built considering a low-modulus Cu bump, with the following assumptions: i) the elastic modulus of the Cu bump was scaled down to 20GPa, ~6X lower than that of standard bulk Cu; ii) plasticity within the bump was represented using a bi-linear kinematic hardening model; iii) the yield strength of the low-modulus Cu material was derived from that of bulk Cu using a reduction factor for the same amount of strain; iv) the same reduction factor was applied to the tangent modulus; v) a birth and death method, similar to the standard bulk-Cu models, was applied to simulate deformation and stress contours during the thermocompression assembly process. A metallic coating composed of 100nm of Pd, and 250nm of Au was included in the model to compare the bump collapse with that achieved with a bulk Cu bump in the previous model from section 3.2.1. The isotropic material properties for low-modulus Cu are reported in Table 6. The surface finish layers were chosen to represent the same configuration as that of a Cu interconnection with metallic coatings, albeit with a low-modulus Cu bump.

Table 6 Isotropic elastic-plastic material properties for low-modulus Cu

Materials	Low Modulus Cu
Elastic (GPa)	20
Poisson's Ratio	0.33
Initial Yield Stress (MPa)	14.7
Tangent Modulus (MPa)	88.4
CTE (ppm/K)	17

A collapse of the low-modulus Cu bump by 3.6 μ m was observed with an applied load of only 50MPa, 7X lower than the reference bonding pressure for this process. The lateral spreading of the bump was only of 1.3 μ m, thus confirming compatibility with fine pitches of 20 μ m and below. Further, it can be seen from the Z-deformation plot in Figure 5.1 that the plastic strain was confined to the bump, with less stress concentrated across the Cu traces, thus potentially alleviating risks of trace buckling and delamination on the die and substrate sides. The extent of bonding pressure reduction with the proposed material innovation of low-modulus Cu is well-represented in Figure 5.2, with respect to the reference bulk Cu-ENIG and Cu-EPAG interconnection structures. The low-modulus Copper model shows the highest slope thus indicating an equivalent bump collapse at lower pressure as compared to the EPAG and ENIG models. The slope also highlights a high sensitivity of plastic deformation to changes in bonding pressure.

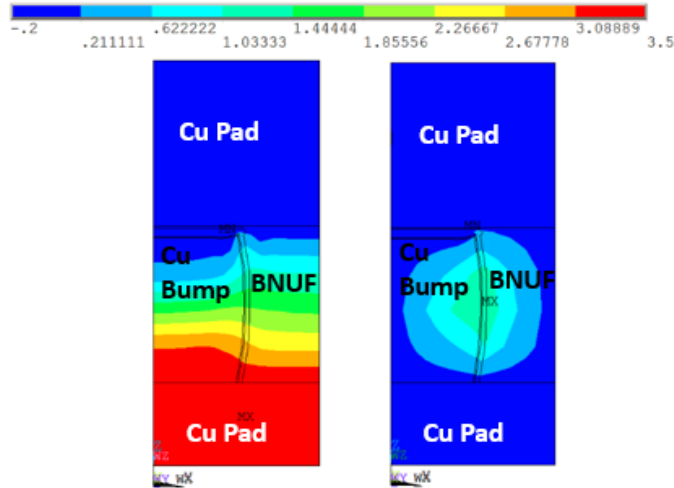


Figure 5.1 Bump collapse deformation contours in the low-modulus Cu bump showing a maximum vertical collapse of 3.6 μm at 50 MPa (left) with a maximum lateral displacement of 1.3 μm (right).

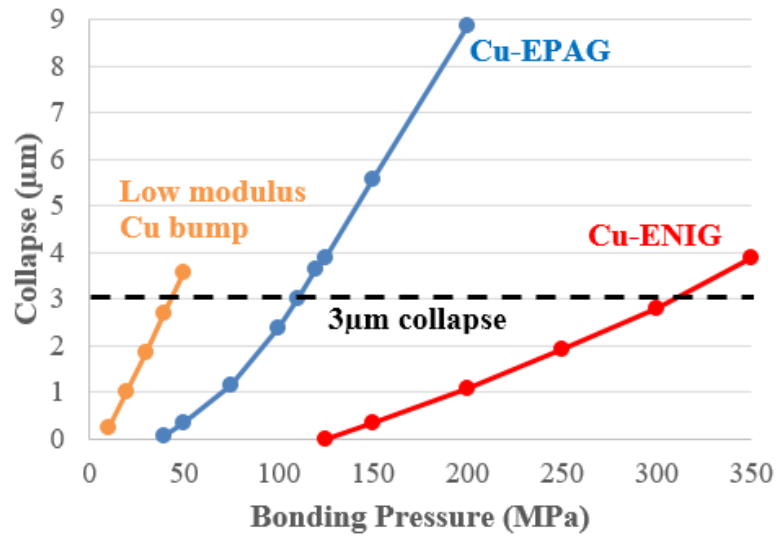


Figure 5.2 Bump collapse as a function of the bonding pressure for bulk Cu-ENIG and Cu-EPAG interconnections in contrast to low-modulus Cu interconnections

In terms of interconnection properties, we need to ensure that such a low-modulus copper interface can be bonded at reasonably low temperatures (<250°C) and be close to the power-handling and thermal stability of bulk copper after assembly. The most effective

method of developing a low-modulus copper material is by introducing porosity. However, porosity is generally detrimental to the performance and stability of the joints, and, therefore, will need to be eliminated in bonding to achieve bulk-like properties after assembly. While abundant information exists on physical properties of porous media with ligaments and porosities in the micron or above range, nanoporous (NP) metals are part of a broader category of porous media or metal-air composites that can extend the range of properties and therefore applications of the parent (solid wall) material. The solid mass fraction (or relative density) for NP metals is typically greater than 30% with open-cell structure, formed by random arrangement of nano-sized ligaments and junctions through the volume. As discussed in Chapter 2, nanoscale copper ligaments are extremely reactive because of higher surface-to-volume ratio, thus can enable sintering and densification of the foam and simultaneous strong metallurgical bonding at temperatures below 250°C to form a bulk-like Cu interface after assembly. In general, open-cell metal nanofoams can exhibit elastic moduli of about an order of magnitude lesser than their bulk counterparts. The value of this modulus and yield strength is strongly correlated to the ligament aspect ratios and relative density [65, 131]. Furthermore, it has been shown [132-134] that nano-Cu foams with ligaments in the size range of 30-40nm have a Young's modulus value of about 25GPa, which is 6X lower than that of bulk-Cu and allows for compensation of non-coplanarities and warpage, thus improving assembly manufacturability. Further, nanofoams show lower thermal and electrical conductivity than the bulk values [135-137]. The conductivity values are dependent on ligament thickness, pore size and defects induced in the ligaments during fabrication. Thicker ligaments increase the conductivity but pores and defects act as scattering centers and are thus, detrimental. Thus, a blueprint of nano-

Cu foams with ligament range of 30-40nm was selected. A comparison of thermal conductivity and electrical resistivity between nanofoam and bulk system is given in Table 7.

Table 7 Comparison of thermal conductivity (κ) and electrical resistivity (ρ) between nanofoam and bulk system (at 300K).

System	Bulk - κ (W/m.K)	Nanofoam - κ (W/m.K)	Bulk - ρ ($\mu\Omega\cdot\text{cm}$)	Nanofoam - ρ ($\mu\Omega\cdot\text{cm}$)
Au	320	8	2.2	70
Cu	385	13.48	1.68	54.5 42.5

It can be seen that as-dealloyed foams have an magnitude of order lesser thermal conductivity than the bulk value. Upon densification of the foams, however, both their electrical and thermal conductivities are expected to increase to values closer to that of the bulk system

5.1.2 Design of precursor system for nano-Cu foams

Choosing the right alloy system (binary / ternary) as well as the correct alloy composition is very important towards achieving key physical properties of the as-dealloyed nanocopper foams. It has been shown in [74, 135, 138] that as the atomic % of Cu decreases within an alloy system, the ligament sizes decrease giving finer length scales as well as changing the isotropy of the structure [132, 133]. The dealloying chemistry also plays an important role in reactivity and dissolution rate of the active element species. In general, Chlorine- and Florine-based acid chemistries are used as etchants because of the tendency of the reactive elements to form salts and dissolve into the solution. Another challenge that needs to be overcome is that of contamination from etchant as well as incomplete dealloying that can

adversely affect the properties of the nanocopper foams. From literature [70], it can be seen that the alloy system of Cu-Zn gives very clean nanocopper foams with less than 1% contamination from the alloying element. From a manufacturability standpoint, etching chemistries such as hydroxides or organic acids need to be considered to eliminate corrosion risks due to Cl⁻ and F⁻ ion contamination. Dealloying time is another major contributor to the kinetics of evolution of nano-Cu foams. Under passive dealloying conditions, coarsening of ligaments proceeds via surface diffusion as dealloying time is increased from 10min to 24hours for the Cu-Zn system in 1% HCl [73]. Conversely, under ‘active’ dealloying conditions, when $V > V_c$ (critical voltage), dealloying is extremely fast and can lead to changes in the structural isotropy [139, 140]. Along with time, temperature also provides the energy to hasten the rate of dealloying causing a large coarsening of the nano-Cu foams, giving coarser porous matrices. Table 8 comprehensively lists the prior art on synthesis of nano-Cu foam from Cu-X alloy systems including the effect of dealloying conditions on the foam morphology and properties.

Table 8 Prior art on synthesis of nano-Cu foams

System	Alloy composition	Fabrication Route	Etchant chemistry	Dealloying time / temperature	Foam Morphology (Ligament size)	Material Properties
Cu-Mn [71, 72]	Mn70Cu30	Arc melting	HCl, Citric acid, (NH ₄) ₂ SO ₄	Passive: 2-10 days RT	45-120nm	Relative density: 30% Hardness: 128±37MPa (120nm ligaments)
			H ₂ SO ₄	Active: 14 hrs (0.11 V _{MSE}) RT	16±4nm	
Cu-Zn [70, 73]	Cu50Zn50, Cu40Zn60, Cu30Zn70, Cu20Zn80	Furnace melting; Electro-deposition; Sputtering	HCl+NH ₄ Cl	Passive: 15-48hrs, 70°C	120±30nm	Relative density: 40% Hardness: 24 – 90MPa
			NaOH & HCl	Passive: 24 hrs (with e-less plating)	150±30nm	
Cu-Al [75, 76]	Cu33Al67, Cu35Al65,	Melt Spinning	HCl+ NaOH	Passive: 2 - 4hrs, RT – 90°C	100-300nm	Cu surface diffusivity: 10 ⁻¹⁰ cm ² /sec

	Cu40Al60, Cu50Al50					Yield strength: 80MPa
Cu-Mg [141]	Cu33Mg67, Cu40Mg60, Cu50Mg50, Cu60Mg40, Cu67Mg33	Melt spinning	5% HCl	Passive 0.5hr 90°C	150±35nm	NA
Mg-Cu- Y [135, 142]	Mg60Cu30Y10 Mg50Cu40Y10	Melt spinning	H ₂ SO ₄	Passive (1.5 hr)	60-100nm Pore Size: 30- 60nm	Relative density: 60%
Cu-Zr- Al [82]	Cu30Zr65Al5 Cu40Zr55Al5 Cu50Zr45Al5 Cu60Zr35Al5 Cu70Zr25Al5 Cu80Zr15Al5	Melt spinning	HF	Passive: 24 hrs @ 0°C and RT	RT: 58nm with pore size – 40nm 0°C: 47nm with pore size of 20nm	180° bendability with 230nm – 1- 3µm nanocopper foam thickness
Cu-Zr [78, 82]	Cu70Zr30	Sputtering	HCl	Active: 10 min (-0.2V _{SCE}) RT	Pore Size: 500nm	NA
Cu-Si [132- 134]	Cu25Si75	Sputtering	HF	Active: 3 - 5 min (- 0.3V _{SCE}) RT	30-45nm	Relative density: 55-60% Elastic modulus: 10-45GPa

5.1.3 Dealloying and pre-assembly characterization

Nano-Cu foams fabricated from a co-sputtered Cu-Si alloy system were used for the first proof-of-concept experiments based on the design knobs listed above as well as the availability and expertise within the team in handling these binary alloys. Nanocopper foams were synthesized through a two-step process. First, thin films of amorphous copper silicide of Cu₂₅Si₇₅ composition by atomic percent were co-sputtered by physical vapor deposition (PVD) on a (100)-oriented Si wafer to a thickness of 2µm. This composition was chosen in order to get uniform and isotropic nano-Cu ligaments across the samples. The composition of the initial alloy was verified through X-ray photoelectron spectroscopy (XPS) analysis. A scanning electron microscopy (SEM) micrograph of the as-deposited Cu₂₅Si₇₅ film is shown in Figure 5.5(a), for reference. The original wafer was cleaved and

each sample was dealloyed in 3% hydrofluoric acid in distilled water, in ambient conditions. Hydrofluoric acid can also react with the Si substrate, potentially causing delamination of the Si substrate-to-amorphous alloy interface during the dealloying process. To prevent this, a thin polymeric film, non-reactive with hydrofluoric acid, was applied on all sides but the top surface of each sample, as shown in Figure 5.3(a). Dealloying initiates from the free top surface and proceeds through the thickness of the foam. As the dealloying front progresses through the thickness, the silicon dissolves in the electrolyte. At the same time, majority of the remnant copper self-assembles into a three-dimensional network of ligaments. The electrochemical dealloying was performed with a three-electrode system consisting of the precursor alloy as working electrode, a saturated calomel electrode (SCE) as reference electrode, and a Pt counter electrode. A schematic of the dealloying experimental setup is shown in Figure 5.3(b).

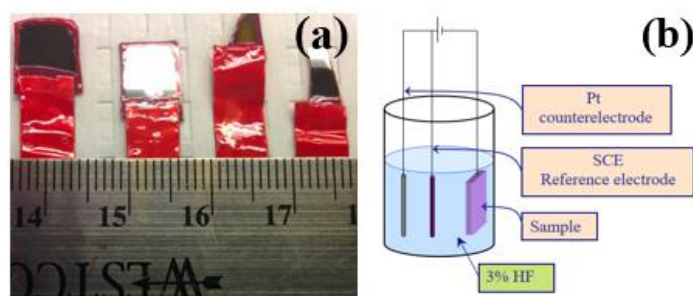


Figure 5.3 (a) Polymeric coating on Cu-Si samples and (b) schematic of dealloying setup

It has been shown that the morphology of metallic foams strongly depends on the applied dealloying potential [84]. As a result, the samples were dealloyed under fixed external voltage of -0.3V for about 300s using charge conservation as a means of quantifying complete dealloying. Figure 5.4 is an I-V graph that demonstrates the optimization trials

on various sets of samples that ultimately led to good repeatability of the dealloying experiments and uniformity in the structural morphology of the nanocopper foams.

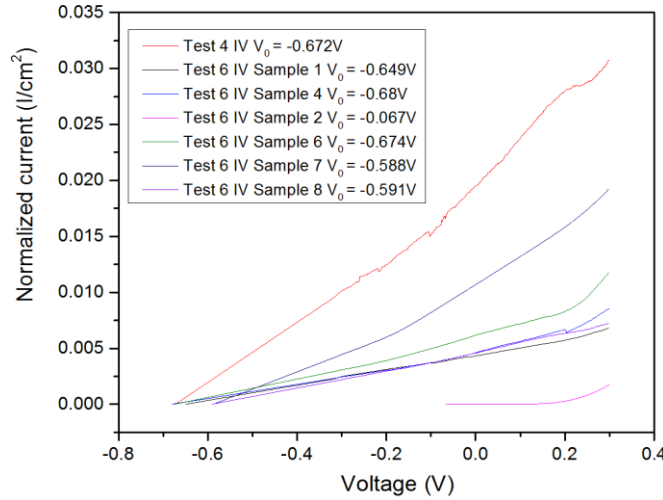


Figure 5.4 Normalized I-V curve with dealloying potential as -0.3V

The samples were characterized with plan and cross-section (90° tilt) SEM views in several locations, and at various magnifications, by Field Emission Scanning Electron Microscopy (FE-SEM) using a Zeiss Ultra60 scanning electron microscope as can be seen in Figure 5.5. The fabricated foams feature an isotropic open cell structure, with an average ligament thickness of 45nm over 25 measurements, as can be seen in Figure 5.5(b). Figure 5.5(c) shows excellent homogeneity and isotropy of the nanocopper foam across the length of the Si substrate. It was confirmed through a combination of XPS and ion milling that the synthesized nanocopper foams contained no remnant silicon to within the resolution limit of the technique (0.1% by atom). A reduction in height of the nanocopper foam films from the initial $2\mu\text{m}$ copper silicide thickness to $1.56\mu\text{m}$ was observed, due to shrinkage during dealloying. Dealloying for longer times results in higher shrinkage of the foams, and brings about coarsening and thickening of the ligaments due to diffusion of Cu atoms across high-curvature surfaces [143].

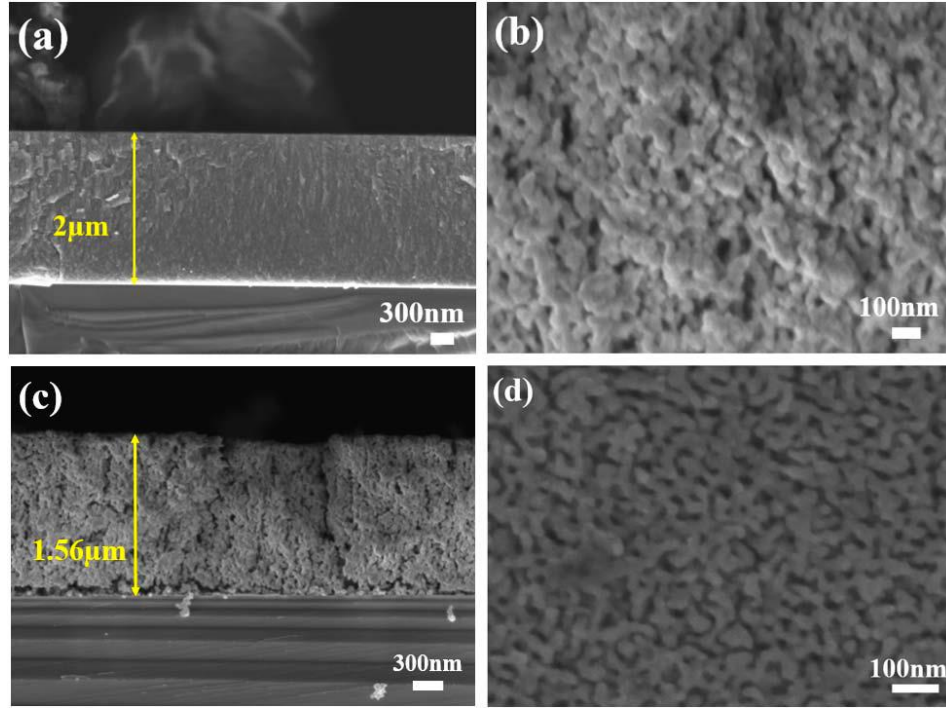


Figure 5.5 SEM micrographs of (a) 90° tilt view of as-sputtered precursor $\text{Cu}_{25}\text{Si}_{0.75}$ thin-film on Si substrate, (b) 90° tilt view of nanocopper foam formed after dealloying, (c) 90° tilt view of the nanocopper foam coverage across the Si substrate, (d) plan-view of nanocopper foams

Image analysis is a fast and attractive technique to extract structural features and trends in length scales from the SEM images. This technique is utilized to find out the relative density of the synthesized foams. The relative density is an important physical property that can alter the mechanical properties of nanofoams. The SEM cross-sectional micrographs were processed using java-based ImageJ software [144]. The images were first converted to 8-bit / 16-bit images and were then passed through a band-pass filter that removed the variation in the brightness for length scales comparable to the image size and also for smaller length scales (few pixels).

Further, these images are then thresholded to an average normalized intensity value selected based on the Otsu thresholding algorithm. This process basically converts it to a

binary image with discernible structural features like pores and ligaments. An area-averaging of this image gives us the relative density of the nanocopper foam cross-section. This analysis technique is illustrated in Figure 5.6. A relative density of 60% was observed on average across the cross-section of the as-dealloyed nanocopper foams.

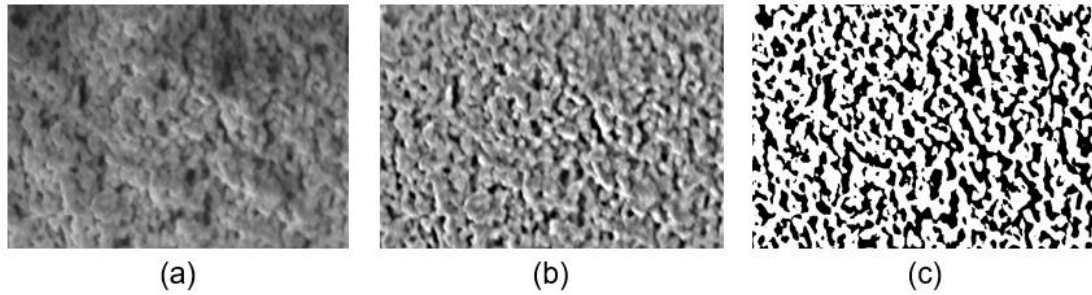


Figure 5.6 SEM image of (a) 30nm sized ligaments on nanocopper foam which is then (b) band-pass filtered and thresholded with an $It = 130$ to form the (c) binary image

5.1.3.1 Oxidation Characterization

Oxidation is a major concern in copper processing. It is well known that on exposure to air, copper oxidizes and forms a mixed oxide film of thermodynamically stable Cu_2O , CuO , $\text{Cu}(\text{OH})_2$, chemisorbed water and carboxylate species [134]. At room temperature, these oxides are self-limiting and form a passive barrier over the Cu surface. Metallurgical bonding typically requires clean and oxide-free surfaces for highest interdiffusion rates. Oxidation kinetics in nano-scale Cu are less understood. It is therefore critical to gain a fundamental understanding of this process in nanocopper foams, and explore solutions to break this layer of surface oxides. Acetic acid has been demonstrated very effective in removing native oxides from the surface of copper thin-films [145]. Acetic acid reacts with copper oxides to form cupric acetate, without reacting with metallic copper. Nanocopper

foams were first characterized five days after dealloying of the copper silicide by XPS analysis, to check for the presence of native oxides. A Thermo Scientific Thermo K-alpha XPS tool having a base pressure of $< 3 \times 10^{-9}$ Torr and fitted with a monochromatic Al K_{α} (1486.6 eV) X-ray source with a hemispherical analyzer was used in this study. Bulk Cu samples were characterized as well, serving as reference to validate the method. XPS analysis detected Cu, O, C and trace Si in the survey spectra, while typical native oxide signature can be identified from the strong satellites (shake-up peaks) characteristic of CuO [109] from the Cu 2p scan spectra in both as-dealloyed foam and bulk Cu samples. The positions of the Cu 2p peaks represent the binding energy required for an electron in the 2p shell of copper to be ejected as a photoelectron. Both samples were then immersed in glacial acetic acid (>99.85% Sigma Aldrich) without any further dilution, at room temperature, for two minutes. Post-acid exposed surfaces were then dried with a N₂ gas gun. Acetic acid has low surface tension (27.8 dyn/cm), allowing for easy removal from the surface. After acetic acid treatment, the pure copper Cu 2p peaks, Cu 2p_{3/2} (932.6 eV) and Cu 2p_{1/2} (952.4 eV), dominated the spectra for both bulk and nanocopper foams as can be seen from Figure 5.7(a)-(b). Carbon contamination is generally unavoidable when dealing with samples in ambient air conditions. For oxidized samples, the C 1s peak generally has two components: the adventitious carbon peak, as well as the carboxylate peak. On comparing the C 1s peak (not shown), it was observed that the carboxylate peak disappears on treatment with acetic acid, thus agreeing with observations from reported studies on copper oxide reduction [20]. In summary, simple method for oxide removal by acetic acid treatment has thus been demonstrated here. Acetic acid treatment had no

discernible effect on the foam nanostructure and resulted in no contamination from residual acid on account of its low surface tension.

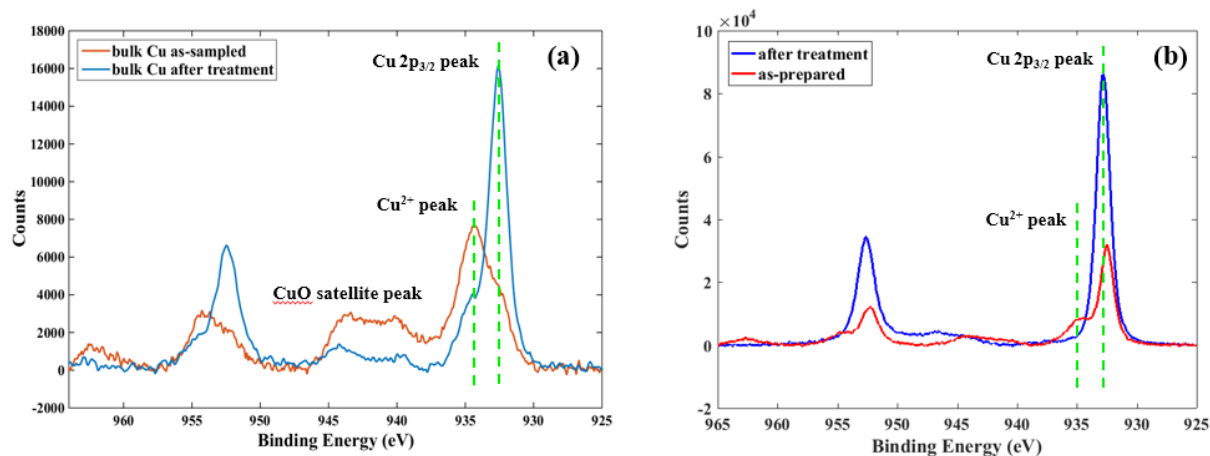


Figure 5.7 Overlaid Cu 2p XPS scans of (a) bulk Cu, and (b) dealloyed nanocopper foams; as fabricated and after acetic acid treatment

5.1.3.2 DSC Characterization

Thermal coarsening studies conducted on nanogold foams revealed that the nano-sized ligaments tended to thicken upon thermal annealing at temperatures much lower than the melting point of Au. This suggests the possibility of a low-temperature solid-state growth mechanism that brings about coarsening of the foams rather than conventional melting to liquid phase. To understand the endo- and exothermic behavior of nanocopper foams, a DSC study was carried out on an as-dealloyed sample on Si substrate in a standard alumina pan using a Thermal Analysis – SDT Q600 DSC instrument. The sample mass was 8.59mg. The heating rate for the experiment was set at 20K/min. The DSC was conducted under constant N₂ flow. Figure 5.8 shows the DSC result for a nanocopper foam. Typically, an endothermic peak is seen for first order melting phenomena, and this peak corresponds to

the melting point of the nanoscale sample. However, in the present case, an exothermal peak is visible at 183°C. The heat released (stored energy) during the exothermal reaction can be calculated as 12.24 J/gm matching closely to that reported for nanoporous gold of 11 J/gm [146]. The presence of this exothermal peak at such low temperature of 0.2 T/Tm indicates that there may be a solid-state strain-release occurring in the nanocopper foam that could be attributed to coarsening of the ligaments. The high surface-to-volume ratio in such foams may have triggered a recovery-like process or recrystallization that initiated coarsening of the foam.

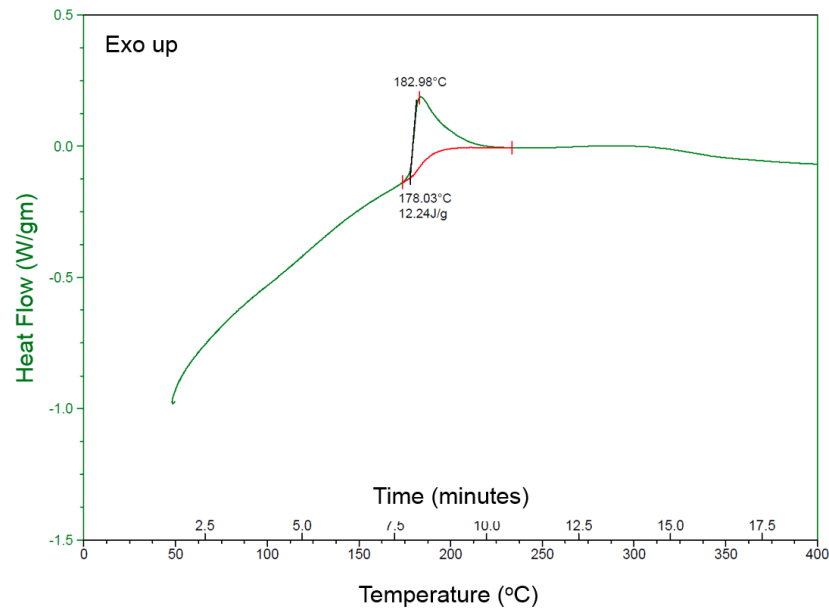


Figure 5.8 Differential scanning calorimetry plot of as-dealloyed nanocopper foam on Si substrate

Further investigation is required to fully understand the nature of recrystallization and hence, explain the sintering mechanisms in nanocopper foams. A preliminary proof-of-concept demonstration was finally carried out to demonstrate assembly of nanocopper foams using the design criteria mentioned in this section.

5.1.4 Proof-of-Concept

The as-synthesized nanocopper foams on Si wafers were assembled onto 5 μ m-thick electroplated Cu on Si substrates. For synthesis of Cu nanofoams, no seed layer was applied to Si wafers before sputtering of Cu-Si. Also, it was assumed that densification of the Cu nanofoams should have minimal impact on the Cu/Si interface adhesion strength. Prior to bonding, the Cu nanofoam samples were treated with acetic acid for 30sec at 25°C to remove native oxides. Assembly was carried out using a Finetech Matrix Fineplacer flip-chip bonder in the conditions listed in Table 9. For Sample A, bonding was carried out at 200°C for 15min under an applied pressure of 6MPa. The bonding pressure and temperature were increased to 9MPa and 250°C, respectively, for sample B. Sample C was bonded for a reduced time of 5min compared to 15min for sample B. All the bonding trials were conducted in 5% forming gas. The mechanical strength of the sintered Cu joints was determined by performing shear test on bonded samples as per MIL-STD-883G Method 2019.7. A Dage die shear tester was used to perform the shear tests. The area of all the samples was greater than 5mm², so the minimum force required for the bond strength to pass the MIL standard is of 2.5kgf. A maximum shear strength of 4.2kgf was measured for sample B at a strain rate of 15 μ m/sec. As expected, a reduction in both bonding temperature and time resulted in a loss of shear strength.

Figure 5.9 shows the cross-sectional SEM images of the fracture surface of sintered Cu joints for samples A and B. A multi-layered morphology was observed after sintering; wherein denser layers were formed at the outer interfaces as compared to the internal region. This kind of morphology upon assembly of metal nanofoams has been reported in [66] and can be explained by pressure-induced collapse of ligaments at the interface. The

deformation leads to greater contact between the ligaments, enabling faster densification at the interface. The internal region, on the other hand, experiences smaller deformation and, therefore, only marginal increment in contact between the ligaments. As the outer layers densify, the densification front moves inward and, if given sufficient time, the internal region also densifies. The gradient in density was very pronounced in Sample A. However, in Sample B the difference in sintered morphology along the thickness was not clearly visible. This could be attributed to faster densification rates at higher temperatures and larger applied pressures, which also resulted into overall higher density of the sintered Cu joint in Sample B.

Table 9 Process parameters for Cu nanofoam-to-bulk Cu bonding

Sample	Temperature (°C)	Time (min)	Bonding pressure (MPa)	Environment
A	200	15	6	5% N ₂ + H ₂
B	250	15	9	5% N ₂ + H ₂
C	250	5	9	5% N ₂ + H ₂

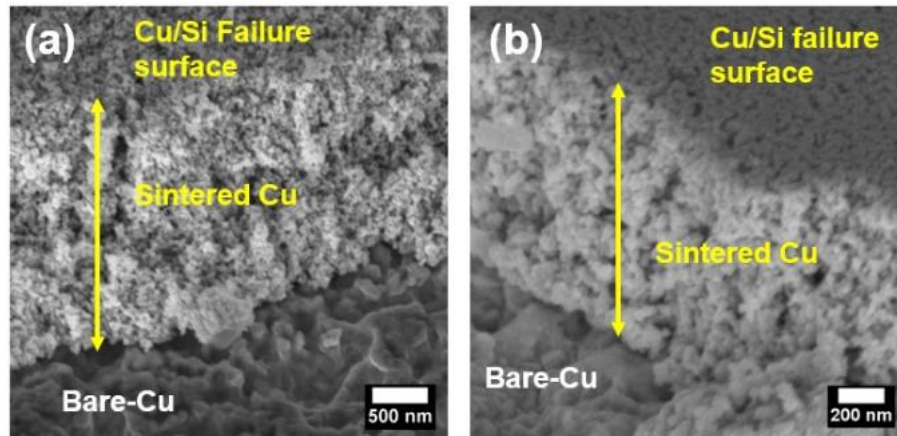


Figure 5.9 Cross-sectional view of fracture surfaces of sintered Cu nanofoam joint: (a) Sample A: 200°C/6MPa/15min; and (b) Sample B: 250°C/9MPa/15min

Figure 5.10 shows the planar view SEM images of the fracture surfaces of sintered Cu joints for samples A and B. At bonding temperature of 200°C, though fracture of the

sintered Cu joint was observed both within the sintered Cu nanofoam and at the Cu nanofoam - to - silicon substrate (Cu/Si) interface, but mainly it occurred within the sintered Cu. On increasing the bonding temperature to 250°C (Sample B), a shift in fracture mode was observed with increase in the fracture area at the Cu/Si interface as compared to sample A.

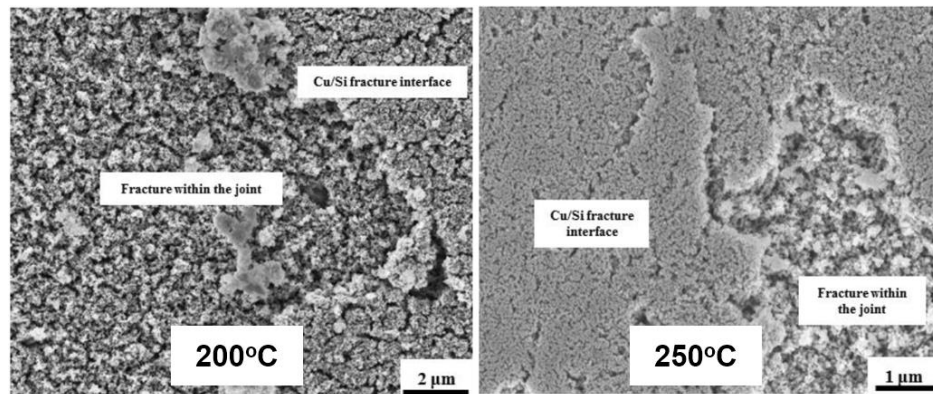


Figure 5.10 Top surface plan-view of fractured sintered nano-Cu joint on bulk-Cu assembly at 200°C and 250°C respectively

Because of higher densification at 250°C, relative density within the sintered Cu was estimated at ~89% in sample B, as compared to 84% for sample A. Lower densification in sample A might have resulted into lower mechanical bond strength in the internal layers, leading to crack initiation within the sintered Cu. Increase in the fracture area at the Cu/Si interface in sample B also suggested that due to higher densification, the Cu/Si interfacial strength became the limiting factor as compared to the strength within the joint. It is to be noted that in both cases, the true bond strength between Cu nanofoams and bulk Cu cannot be estimated. When the bonding time was reduced to 5 min, the fracture profile for Sample C was in between that of Sample A and B. The bonding time needs to be comparable to that of conventional solder-based interconnections for hi-speed assembly. This can be done

using the 2-step TC-NCP based process as discussed in the previous approach with: a) a 30sec bonding time under thermocompression; and b) a batch annealing step at 250°C to sinter the foam under forming gas and densify close to that of bulk-Cu. The activation of forming gas under 250°C was another concern due to the rudimentary setup of our bonder. As a result, in order to ensure the effective activation of forming gas and reduction of copper oxides under assembly conditions, the bonding temperature was raised to 300°C for subsequent assemblies. In the next section, sintering trials were carried out to assess the densification of nano-Cu foams as a metric for their bondability through sintering as a function of assembly environment, temperature, and time.

5.1.5 Sintering kinetics of nanoporous copper

Current understanding of NP metal formation is derived from observed atomic rearrangements at interface under a driving force provided by the electrolyte environment, under the assumption that the crystalline microstructure is preserved [87-89, 147, 148]. Such rearrangement of components across the lattice are at length scales comparable to that of surface diffusion. This mechanism based on Monte-Carlo simulations that does not require nucleation of new crystals or removal of lattice sites was proposed first by Erlebacher [143]. Many other models based on ordering-disordering [149], roughening transition [150], and network restructuring based on plasticity [151] have been proposed over the past years. In the case of dealloying from crystalline precursors, the expectation that the pore fraction reflects the volume fraction of atoms dissolved is erroneous. In addition to dissolution, processes like coarsening, local deformation and capillarity are also active and at nanoscales, can affect macroscopic evolution under different driving forces.

Electrolyte-treated nanoporous Gold (NPG) has been shown to coarsen through surface diffusion without any apparent densification or volume shrinkage [152]. Moreover, electrolyte dealloying under different temperatures has given further give evidence to surface diffusion dominating the evolution of ligaments and pores [153-155]. However, Parida and Detsi et al [148] showed that there was an immense volume shrinkage throughout bulk of NPG material when subjected to catalytic coarsening, giving possibility of a separate mechanism for material redistribution. Moreover, evidence of enclosed voids [156] and remnants of ligament pinch-off, with immense curvature gradients have been observed in experiments [157], in contrary to the predictions of a surface-diffusion model. Though self-similar coarsening behavior is observed for NPG under electrolyte coarsening [158, 159], there have been conflicting reports of both self-similar and non-self-similar coarsening for thermally annealed NPG under various environments [146, 160-163]. Hakamada et.al. [146] reported that recrystallization was responsible for the thermal coarsening of NPG, but the process of recrystallization was not reported, or whether it arises from surface or volume diffusion. While this effect of surface adsorbates on annealed NPG has been explored, such an effect on a more reactive system such as NP Cu is not well understood.

Thermodynamically, this interface coarsening reduces the total interface energy, with a concurrent reduction of surface area per unit volume with time. The total pore volume decreases, and the material densifies with an increase in its relative density. In the field of classical sintering, Coble [164] illustrated the evolution of particle-pore structure schematically, and identified three stages of sintering. The initial stage is characterized as the formation and growth of contact between neighboring particles. In the

intermediate stage, the pore structure evolves into an interconnected channel with cylindrical pores lying primarily along grain edges. The final stage begins when the pinch-off of interconnected pore channel forms closed pores at the relative density of >0.9 . The final stage of sintering of crystalline particles is usually accompanied by coarsening and grain growth. The validity of using final stage coarsening and grain growth models to NP metals with relative densities <0.5 is questionable. However, as-synthesized NP metals with relative densities >0.6 can be thought of as in the intermediate-stage of sintering with necking and network formation, and would thus require intermediate – final stage models to accurately model the mass transport kinetics.

Thus, there is essentially a large gap in the understanding of mass transfer and topology evolution in electrolyte and heat treatment of NP metals. This section aims at providing a critical analysis of the sintering and densification behaviors of electrolyte-treated and thermally annealed foams with experimental evidence and analytical modeling to support distinct mass transport kinetics for each respectively.

5.1.5.1 Experimental protocol for sintering studies

Towards this study, NP Cu was fabricated through dealloying (3% HF) of co-sputtered 2 μ m-thick $\text{Cu}_{0.25}\text{Si}_{0.75}$ (by atomic percent) on Si substrates was utilized for this study. For ease of dealloying, the Si substrate was further sectioned into rectangular pieces with an average area of 0.4 cm² using a diamond scribe to carry out coarsening under thermal and electrolyte environments. Samples were also dealloyed at 5°C and 40°C to observe the change in microstructural variation with dealloying temperature. All these samples are referenced ‘as-prepared’ throughout the further sections and the dealloying temperature

was noted for each. Pre-sintering oxidation inhibition was performed, leveraging our results from section 5.1.3, under 99.7% glacial acetic acid for 30sec. Electrolyte treatment was carried out in 3% HF solution at ambient temperature (25°C) through extended passive dealloying (no potential applied) for 15, 30 and 60 minutes. Similarly, thermal annealing was carried out by subjecting the synthesized NP Cu samples to N₂ gas at 300°C and forming gas (N₂ + 4% H₂) at 250°C and 300°C environments respectively. The thermal annealing was carried out in a rapid thermal annealing furnace (SSI – RTP) with a ramp rate of 30°C/s for fast ramp and uniform temperature control for a time range of 15, 30 and 60 mins. The volumetric flow of N₂ and forming gas was limited to 5 standard liters/min (SLM) to ensure minimal presence of air in the chamber and thus limit the potential high-temperature oxidation of the samples. A Hitachi SU8230 SEM cold-field scanning electron microscope (FE-SEM) was used to observe the variation in morphology of the as-prepared and coarsened samples under plan and 90° tilt views under different magnifications across 5 locations per sample. Charging-induced distortion of the SEM image was prevented by mounting the samples using conductive copper tape. Energy dispersive spectroscopy (SEM-EDS) was employed to verify that no remnant Si was left in the NP Cu after dealloying process to within the resolution limit of the tool (0.1 at. %). ImageJ was utilized to carry out digital image analysis of the SEM images using the technique mentioned in the previous sections. Furthermore, ImageJ is also useful in finding statistical 2-point correlations within binary images through Fast Fourier Transformations (FFT). Radially normalized 2-point correlations were realized by normalizing the radial profile across the inverse-FFT of the SEM binary images. The 1D and 2D 2-point correlations were also

visualized using a custom MATLAB code, based on the inverse of the power spectra of the binary images to corroborate the results from ImageJ.

5.1.5.2 Results of sintering trials

The cross-sectional images of electrolyte and thermal treated samples under various conditions in the ‘as-prepared’ and final states at 60 minutes are shown in Figure 5.12. Both XPS and SEM-EDS characterization of the as-prepared NP Cu confirmed that there was no remnant non-dealloyed silicide to within the resolution limit of the techniques (0.1% by atom). The magnification was set at 200nm across all the images for an eye-to-eye comparison. After dealloying, a homogeneous isotropic open-cell network of NP Cu was formed across all as-prepared samples. While the as-prepared structures might have local variations in foam connectivity, pore and ligament distribution, all the as-prepared samples had effectively the characteristic scale which was verified through 2-point spatial correlation based on pore-density calculations across the binarized as-prepared images for all conditions (as shown in Figure 5.11). The correlation functions for all as-prepared samples appear similar, indicating similarity in microstructure. The critical length-scale, representative of the spatial correlation between the dark (void) and white (NP Cu foam) regions varies in the range of 14-18nm for all the ‘as-prepared’ samples dealloyed at 25°C. Furthermore, the samples dealloyed at 5°C and 40°C show critical radii of 13nm and 16nm, indicative of similar morphology as can be seen from Figure 5.11(d). Thus, any variation in the SEM images is representative of all the as-prepared samples.

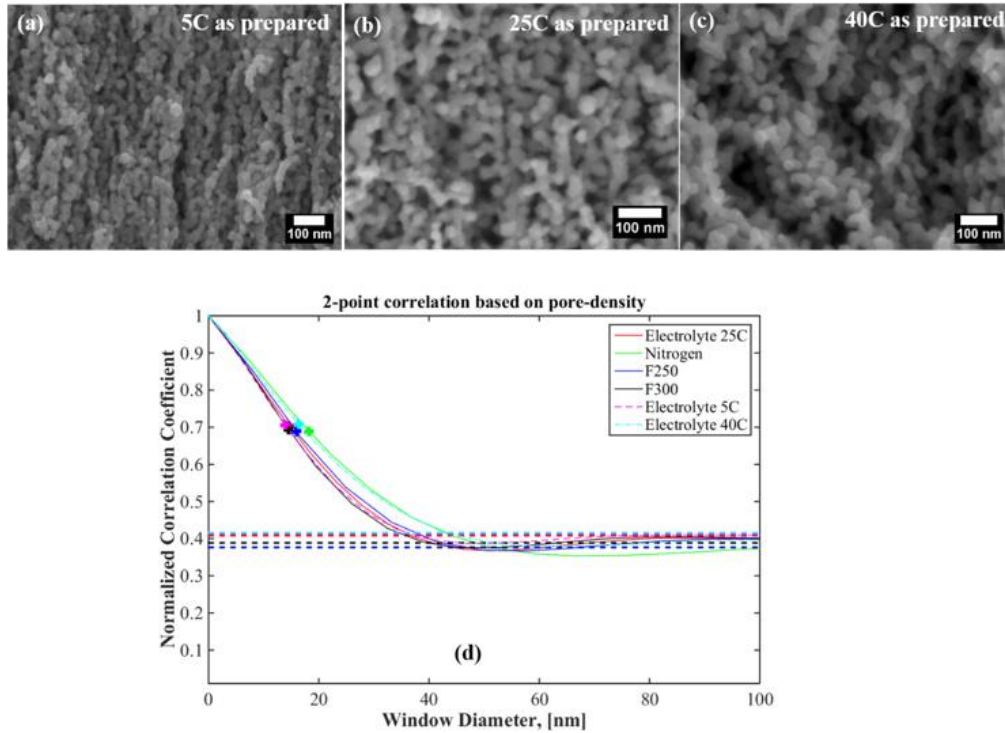


Figure 5.11 Cross-sectional SEM images of NP Cu foam dealloyed at (a) 5°C, (b) 25°C, (c) 40°C; and (d) normalized 2-point correlation function v/s specie radius for all as-dealloyed samples

It has been shown previously that as NP metals are coarsened [131, 134], there is a gradual shrinkage in the through-thickness direction as well as thickening of features during thermal annealing. Significant amount of shrinkage in the Z-direction was observed in the electrolyte- and forming gas-coarsened samples (Figure 5.12(a)-(b) and (e)-(h) respectively) while the nitrogen-coarsened samples showed almost no shrinkage. Furthermore, there was a substantial thickening of the microstructure under electrolyte and forming gas environments, while under Nitrogen, the structure did not appear to have changed drastically after 60 minutes. While self-similar thickening of features was observed in the electrolyte, the environment and temperature played an important role in

shaping the morphology of the thermally treated samples. NP Cu annealed in N₂ atmosphere evolved into an irregular rough microstructure, likely due to the formation of high-temperature oxides at 300°C, while foams coarsened in forming gas at 250°C exhibited denser particle-like morphologies. A noteworthy observation was the large amount of densification and Z-shrinkage exhibited by NP Cu samples coarsened under forming gas at 300°C (Figure 5.12(g)-(h)), where the foam structure had coalesced from an open bi-continuous nanoporous network to form a continuous bulky-Cu layer composed of large faceted agglomerates throughout the substrate. Under forming gas, any high-temperature oxide was reduced instantaneously on the surface of the NP Cu [165] and temperature-based kinetic processes determined the final microstructure of the samples.

Z-shrinkage % values for all as-prepared and coarsened NP Cu samples are represented in Figure 5.13(a). Z-shrinkage % here is defined as the percent change in the thickness of the foam layer under varying coarsening conditions with respect to the as-sputtered free surface of the initial Cu-Si alloy. The shrinkage values were reported across 10 measurements across on 5 different SEM images taken along the observed cross-section of the sample. The standard deviation across the measurements is also reported in Figure 5.13(a). It was observed that the 2µm Cu-Si film shrinks to about 1.55µm on average after undergoing dealloying with a Z-shrinkage value of 19% on average across all as-prepared samples. Furthermore, samples under electrolyte coarsening and under forming gas at 250°C behaved very similarly and the Z-shrinkage gradually increased and varied from 18±1% under as-prepared conditions to 31.5±2% after 60 minutes of coarsening. In case of the N₂-coarsened sample, the Z-shrinkage remained approximately the same changing

from $21\pm1\%$ to $22.5\pm2\%$ after 60 minutes signifying very constricted mass transport even at high temperatures of 300°C .

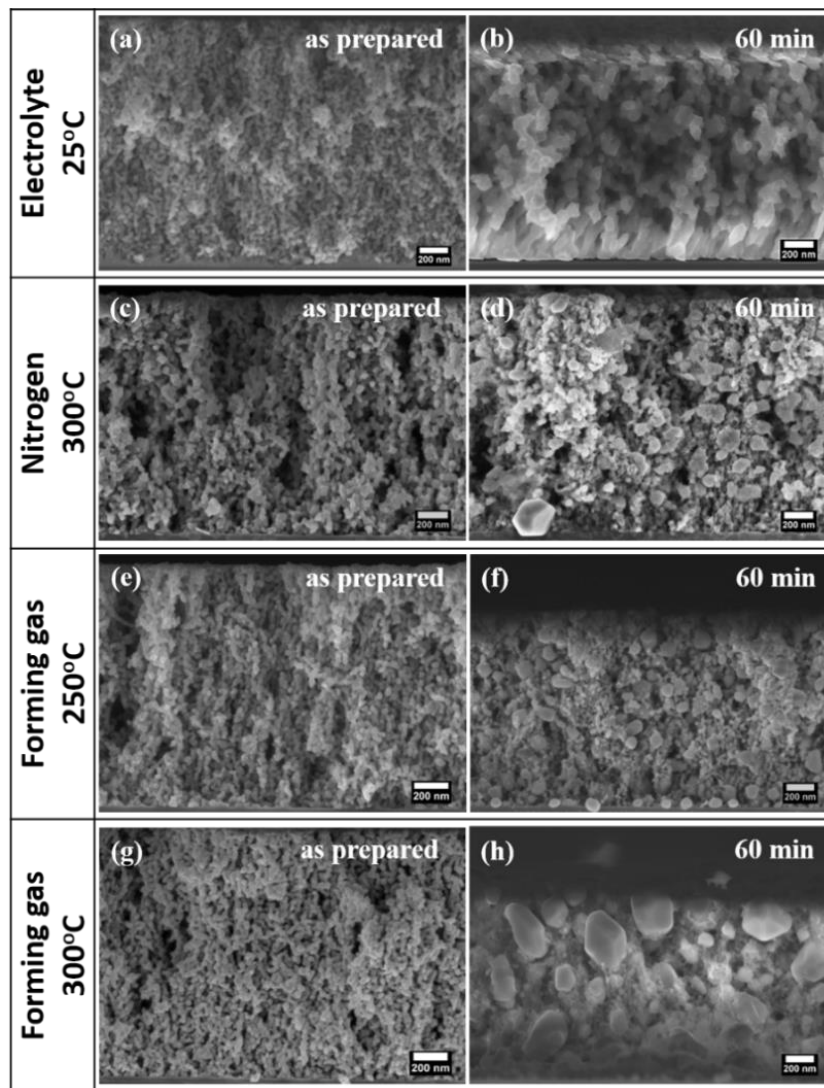


Figure 5.12 Cross-sectional SEM images of NP Cu foam as-prepared and coarsened for 60min under (a)-(b) electrolyte environment, (c)-(d) N_2 gas – 300°C , (e)-(f) forming gas – 250°C , and (g)-(h) forming gas – 300°C respectively

In case of samples under forming gas at 300°C , the shrinkage was significant after only 15 minutes of heating with a Z-shrinkage value of $34\pm2\%$. The shrinkage then steadied to a final value of $34.5\pm2\%$ after 60 minutes of coarsening.

Relative density measurements, made on Image J software using the process outlined in the previous section, across all the as-prepared and coarsened samples are shown in Figure 5.13(b). A standard deviation of $\pm 5\%$ was taken across all the measured samples to account for variation in the chosen threshold intensity as well as the segmentation algorithm. The relative densities for the samples across all the thermal coarsening conditions had similar characteristics, with a large change in density observed in the initial stages of coarsening and a levelling off observed towards the end of the coarsening period at 60 minutes. The relative density for the N_2 -coarsened samples changed sluggishly from $61\pm 5\%$ to $74\pm 5\%$ while for the forming gas coarsened samples, there was a significant change from $63\pm 5\%$ to $86\pm 5\%$ at 250°C and more drastic from $61\pm 5\%$ to $93\pm 5\%$ at 300°C respectively. The electrolyte coarsened samples, however, showed a linear trend in relative density from $62\pm 5\%$ initially, to $82\pm 5\%$ after 60 minutes.

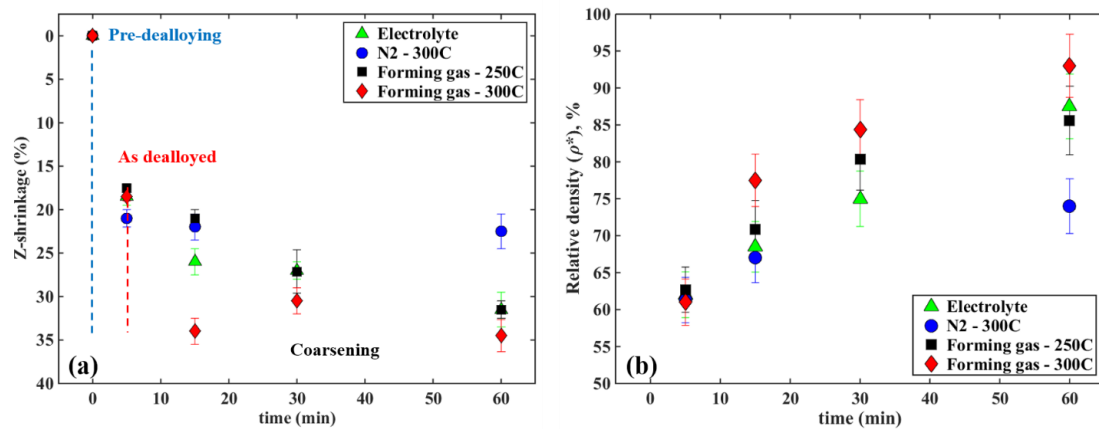


Figure 5.13 NP Cu sample (a) Z-shrinkage (%) and (b) relative density (ρ^*) as a function of processing time in electrolyte – 25°C , N_2 – 300°C , and forming gas environments at 300°C and 250°C respectively

Observing the trends in Z-shrinkage and relative density, we focus on the two extreme conditions within the ones considered: electrolyte-coarsening (electrolyte) and forming gas

coarsening under 300°C (F300). To understand the change in microstructure, high-magnification images of the NP Cu samples as a function of annealing time were considered, as shown in Figure 5.14 and Figure 5.15. Under electrolyte coarsening, the change in morphology is self-similar which is evident through the preservation of the foam microstructure even at 60 minutes of coarsening, even while some densification and thickening of features is observed. This is further accompanied by the gradual change in Z-shrinkage as well as the near-linear increase in relative density of the NP Cu foam from as-prepared condition to 60 minutes. However, in the case of F300 sample, there is a distinct change in the morphology from a porous structure to that of an agglomerated particle-like morphology during thermal annealing. The distribution of these particles is bimodal, with large bulky copper agglomerates coexisting in a matrix of miniscule, almost spherical copper particles. The agglomerates show faceted features evolving from a non-faceted smooth nanoporous network.

To further understand the kinetics of this evolution as well as the differences within electrolyte and F300 samples, we define and track a few features of interest within the foam morphology through the various stages of coarsening. The smallest features of interest within a porous frame are ligament and nodes. Figure 5.16 shows a representative NP Cu structure with three defined features: (a) ligament junction ‘j’ – dimension of nodes within the NP Cu network; (b) ligament width ‘t’ – thickness of the interconnected elements between the junctions; and (c) ligament length ‘l’ – independent length of a ligament.

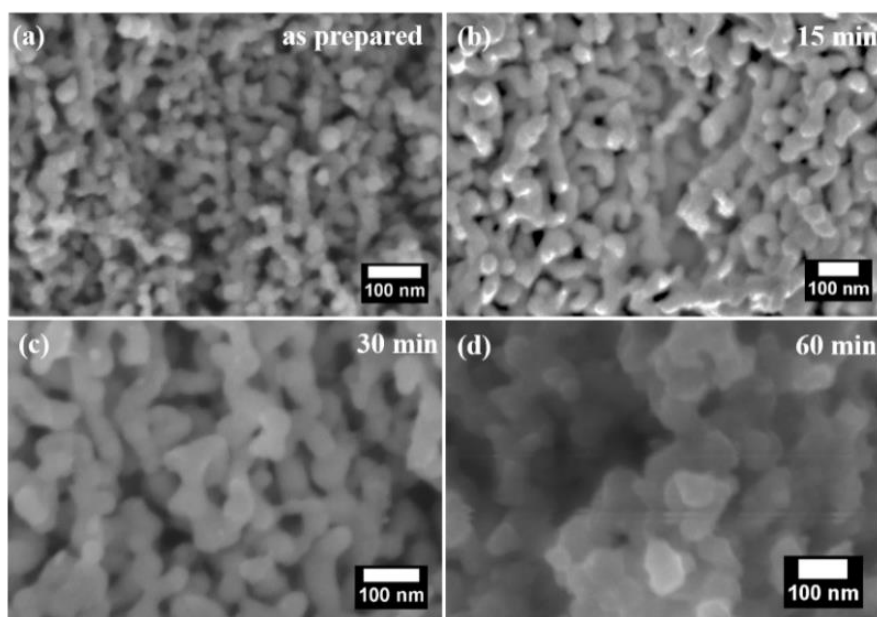


Figure 5.14 Cross-sectional SEM images of as-dealloyed NP Cu samples at (a) as-prepared – 25°C, (b) 15 min, (c) 30 min, and (d) 60 min under electrolyte coarsening

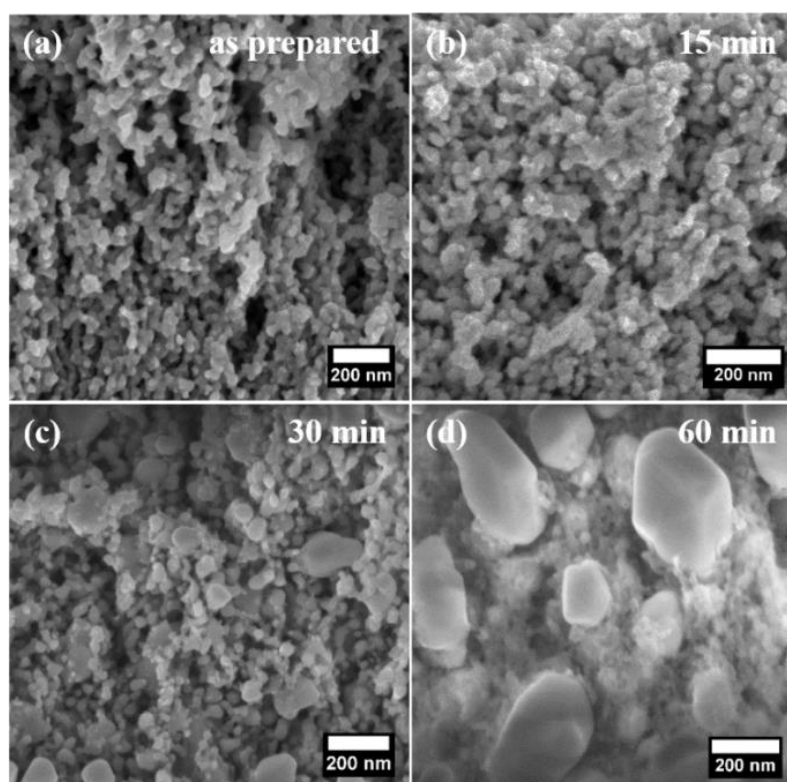


Figure 5.15 Cross-sectional SEM images of NP Cu samples at (a) as-prepared – 25°C, (b) 15 min, (c) 30 min, and (d) 60 min respectively under forming gas at 300°C

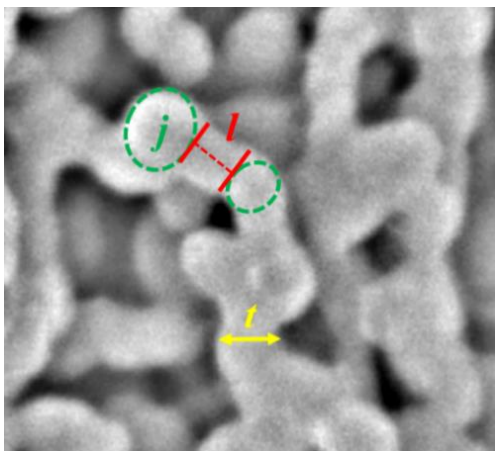


Figure 5.16 Schematic of features of interest: junction dimensions ‘j’, independent ligament length ‘l’ and ligament width ‘t’ in NP Cu

Fifty such measurements of ‘j’, ‘t’, and ‘l’ were manually calculated across 3 binarized SEM images along the cross-section of the NP Cu samples for all processing conditions. These features were tracked as a function of time and the variation in their dimensions and its standard deviations is represented in Figure 5.17(a)-(c). It is strikingly clear that all the tracked features, namely, ligament width, length and junction dimensions increased as a function of time for the electrolyte coarsened NP Cu samples. In the electrolyte coarsened samples, ‘j’ changed from $31 \pm 5 \text{ nm}$ to $55 \pm 10 \text{ nm}$, ‘t’ changed from $25 \pm 4 \text{ nm}$ to $45 \pm 8 \text{ nm}$, and ‘l’ changed from $33 \pm 7 \text{ nm}$ to $49 \pm 9 \text{ nm}$ after 60 minutes of passive dealloying. However, in the case of the thermally coarsened samples, only the junction dimensions increased, while the ligament length and width continually decrease. For the nitrogen-coarsened samples, ‘j’ changed from $32 \pm 4 \text{ nm}$ to $54 \pm 28 \text{ nm}$, ‘t’ changed from $29 \pm 4 \text{ nm}$ to $25 \pm 6 \text{ nm}$, ‘l’ changed from $40 \pm 4 \text{ nm}$ to $26 \pm 5 \text{ nm}$ respectively after heat treatment for 60 minutes. The Nitrogen-annealed samples showed a smaller degree of change in the feature dimensions while the NP Cu sample coarsened in forming gas at 250°C exhibited a larger change in

dimensions with the ligament thickness. For the NP Cu samples coarsened in F250C condition, 'j' changed from $32\pm 5\text{nm}$ to $70\pm 30\text{nm}$, 't' changed from $29\pm 4\text{nm}$ to $17\pm 4\text{nm}$, 'l' changed from $36\pm 7\text{nm}$ to $15\pm 5\text{nm}$ respectively after 60 minutes. The standard deviation for the forming gas coarsened samples at 300°C was high on account of the development of a bimodal distribution of particles. For the NP Cu samples coarsened in this condition, 'j' changed from $32\pm 5\text{nm}$ to $80\pm 70\text{nm}$, 't' changed from $30\pm 3\text{nm}$ to $12\pm 6\text{nm}$, 'l' changed from $35\pm 4\text{nm}$ to $9\pm 6\text{nm}$ after 60 minutes of coarsening respectively. The shift in the ligament width and ligament junction distributions for the two extreme cases of electrolyte and F300 NP Cu samples are detailed in Figure 5.18. Thus, there is a fundamentally different kinetic process for the transport and diffusion of Cu atoms in the case of electrolyte and thermally coarsened NP Cu. Within the thermally coarsened samples as well, the rate kinetics are different in the case of N_2 gas where diffusion is impeded by oxidation and forming gas where, in an oxide-free environment, a higher temperature provides a larger driving force for diffusion and subsequent densification of NP Cu.

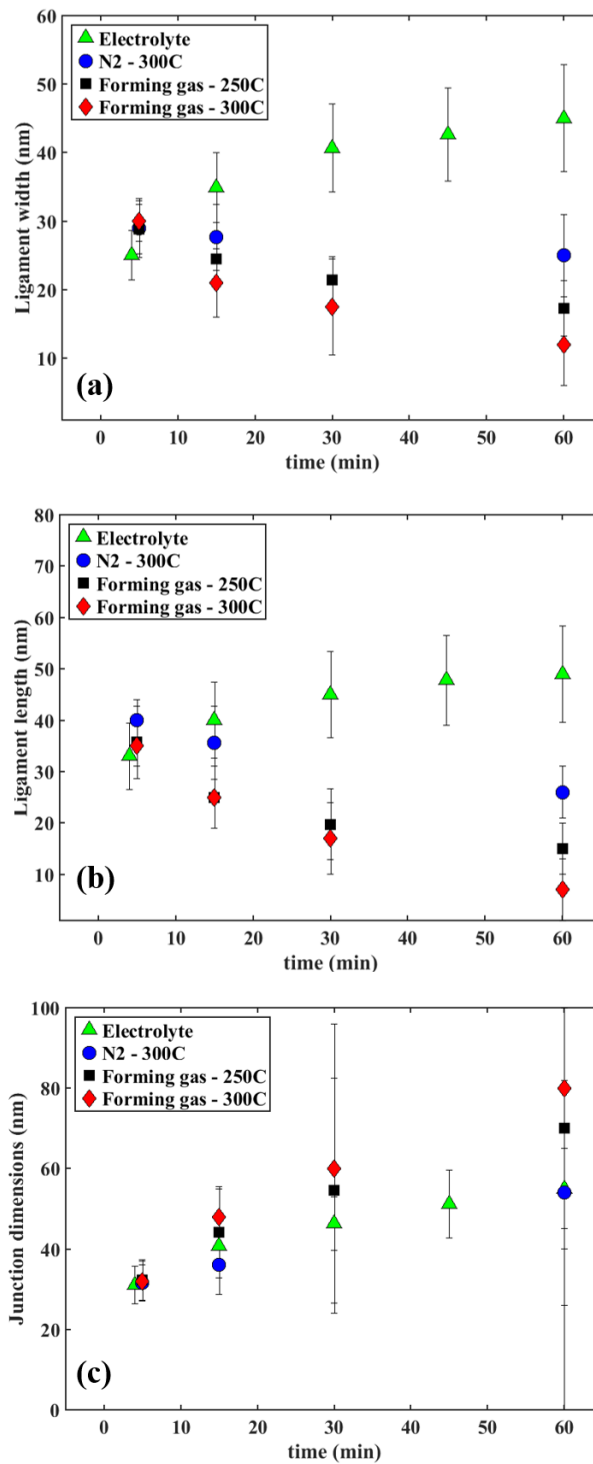


Figure 5.17 Graphs plotting the variation of (a) ligament width ' t '; (b) independent ligament length ' l '; and (c) junction dimensions ' j ' with time across electrolyte, N₂ gas, and forming gas environments

These results were further utilized in plotting histograms of the ligament widths (t) and ligament junctions (j) for the electrolyte and F300 samples in the as-prepared and coarsened to 60 minute conditions. The histograms were normalized to an area of 1 with respect to scaled ligament junctions and widths for each sample, using the mean value as scaling parameter. The mean values for all conditions are given in Table 10. It can be seen from Figure 5.18(a)-(b) that the distribution of the ‘t’ and ‘j’ in the electrolyte coarsened samples about the mean feature size is self-similar for the as-prepared and 60min coarsened case. However, in the case of F300, we can see a sharp contrast in the evolution and hence distribution of t and j as a function of coarsening time. In F300 samples, the scaled ligament widths have a broader distribution after undergoing significant densification over 60 minutes, while the scaled ligament junctions evolve from a narrow Gaussian distribution to a bimodal distribution of extremely small particles co-existing with massive faceted agglomerates that were formed during sintering.

Table 10 Measured average ligament width (t) and junction dimensions (j) for Electrolyte and F300 samples across as-prepared and 60 min coarsened conditions

Condition	Electrolyte Coarsening		F300 Coarsening	
	width (t)	junction (j)	width (t)	junction (j)
as-prepared	25±4nm	31± 5nm	30±3nm	32±5nm
60 min	45±8nm	55± 10nm	12±6nm	80±70nm

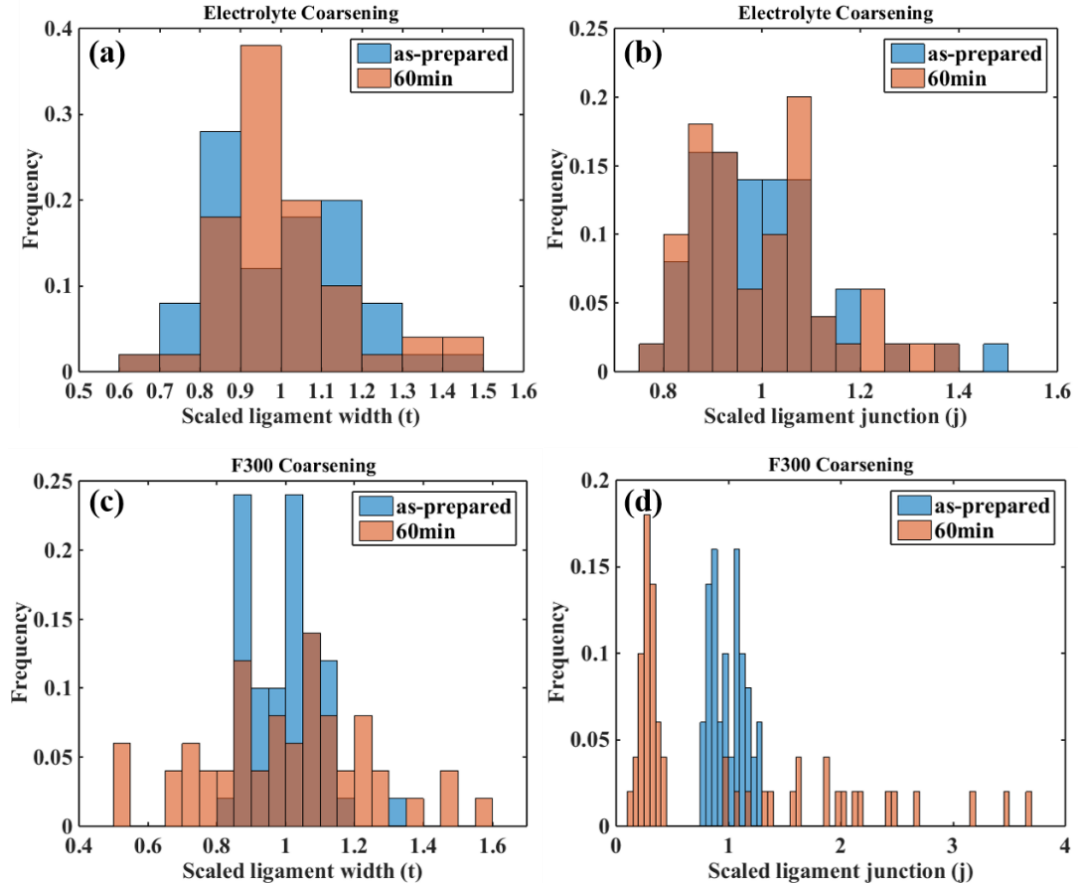


Figure 5.18 Distribution of ligament features across (a)-(b) electrolyte samples and (c)-(d) F300 sample comparing ‘as-prepared’ and ‘60min coarsened’ states.

Furthermore, on plotting the neck-ratio – ligament width to junction size (w/j) against time for the electrolyte- and thermally-treated samples, as shown in Figure 5.19, it is evident that there is very little mass transfer from nodes to the ligaments in the case of electrolyte coarsening. This contradicts the additional ~13% Z-shrinkage observed in electrolyte-coarsened samples post-dealloying. It has been shown that dealloying under potentiostatic conditions causes high tensile stresses to form in NPG foams [166], which could cause the local stresses around ligaments to exceed the yield strength, thus causing ligament collapse

and cracking. Moreover, NP-Cu foams reportedly [133] have a network of grain boundaries and twins that can act as propagation points for the eventual collapse of the ligaments.

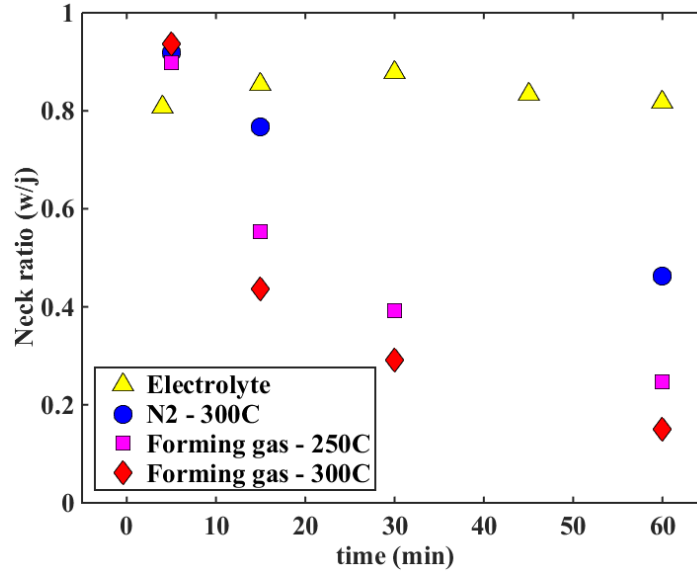


Figure 5.19 NP Cu neck ratio (w/j) as a function of time for all coarsened samples

Furthermore, previous studies have reported that coarsening of constrained films can bring about anisotropic morphologies with void formation in the perpendicular direction to the plane of the substrate [167]. We hypothesize that this effect, combined with the tensile stresses under dealloying causes vertical ligaments to deform plastically and collapse onto the nodes, thus bringing about a mass transfer from the collapsed vertical ligaments to their respective nodes. This would then redistribute mass through surface diffusion between the nodes and non-collapsed ligaments. For the thermally-coarsened samples, the neck ratio (w/j) decreases as a function of time until reaching a plateau. This implies that there is a continuous transfer of mass from the ligaments into the junction nodes, until all the

ligaments are transformed into agglomerated nodes, as is evident from the coarsening and faceting of nodes within the F300 samples in Figure 5.15.

5.1.5.3 Kinetics of Coarsening

In previous studies [160, 161, 163, 168, 169], a temporal power law of grain size evolution has been used to fit coarsening kinetics of nanoporous materials. This is equivalent to the initial stage coarsening and densification within nanoparticles as well as grain growth in polycrystalline materials [59, 170]. The coarsening kinetics are estimated by a log-linear fit of the characteristic length v/s time, i.e.

$$\lambda(t^n) = k_0 t \exp\left(\frac{-E_a}{RT}\right) \quad (10)$$

Where $\lambda(t)$ is the characteristic length evolving at time t , k_0 is pre-exponential constant, n is the coarsening exponent, E_a is the activation energy for sintering, R is the gas constant ($8.314 \text{ J.K}^{-1}.\text{mol}^{-1}$) and T (K) is the annealing temperature. This can also be expressed as:

$$\lambda \log(\lambda) = B - \frac{E_a}{nRT} + \frac{1}{n} \log(t) \quad (11)$$

Where B is a constant, and the coarsening exponent n can be determined by the slope of the $\log(\lambda)$ v/s $\log(t)$ plot. The coarsening exponent n dictates whether the overall sintering in the sample is through surface ($n = 4$), grain-boundary ($n = 3$) or lattice diffusion through the bulk ($n = 3$). In our work, $d(t)$ is the change in size of the junctions (j) on account of mass agglomeration under coarsening conditions. Figure 5.20 shows plots of the variation of ' j ' v/s time for all the environments on a log-log scale. The coarsening exponent is 2.95

– 3.33 for the NP-Cu samples annealed in forming gas at 250 and 300°C, while the coarsening exponent of 4.57 – 4.79 is observed for NP-Cu samples coarsened in nitrogen and electrolyte atmospheres. From this, it is clear that NP-Cu samples coarsen via surface diffusion in electrolyte, and through grain-boundary or bulk lattice diffusion under thermal treatment with forming gas environment. The coarsening exponent of N₂-300C samples is 4.79, implying that surface diffusion plays a more important role as compared to bulk-diffusion modes of transport. Bulk diffusion is hindered in this case due to the formation of rough irregular CuO-based surface-oxides during sintering at 300C [21, 171], thus preventing particle transport across grain boundaries. Studies on coarsening of NPG foams in N₂ atmospheres have also shown that nitrogen atoms adsorb onto the surface of the Au foam and carry out surface transport of adatoms across interface kinks. Finally, in the case of the electrolyte-coarsened samples, the coarsening exponent of 4.57 is corroboration of surface diffusion-controlled coarsening across the NP-Cu / electrolyte interface.

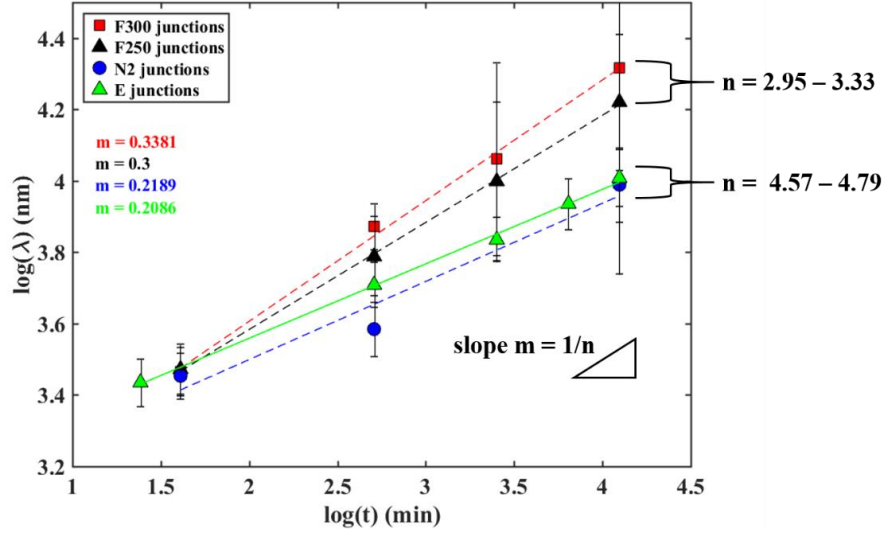


Figure 5.20 log (d) v/s log (t) plot with error bars and fitted lines with slope ($m = 1/n$) values in legend. Dashed fitted lines are for thermally coarsened data while solid fitted lines are for electrolyte coarsened data

In conventional nano-sintering, coarsening and densification occur simultaneously under isothermal sintering conditions and will affect the final microstructural development. Coarsening is associated with aggregate grain growth through mass influx between particle centers. Thus, under pure coarsening conditions, there would be only grain growth through the non-densifying mechanism of surface diffusion. However, under pure densification conditions, there is mass transport away from the particle centers, thus bringing the particles closer to each other, promoting shrinkage and pore-collapse through densifying-mechanisms such as grain boundary diffusion, lattice diffusion, plastic flow, and vapor-phase transport. The microstructural development in such samples is represented by a trajectory from the initial microstructure on a grain size v/s relative sintered density ρ^* plane. Similarly, for our NP-Cu samples, the microstructure can be traced by the normalized average distance between nodes ($\langle N_f/N_o \rangle$) as a function of relative density for all coarsened samples as shown in Figure 5.21. It can be seen that the growth of the NP-

Cu foam in electrolyte environment is governed by coarsening, while that for the Np-Cu foam in thermally-treated environments is governed by densification and eventual pore-collapse and grain growth.

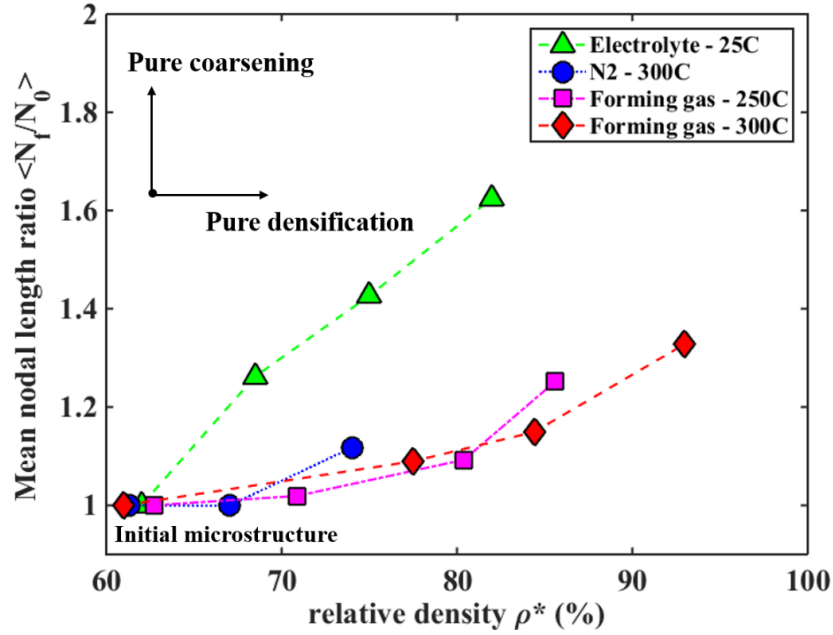


Figure 5.21 Mean nodal length ratio (N_t/N_0) v/s relative density ρ^* for NP Cu foams in various environments

5.1.5.4 Summary of coarsening kinetics

Nanoporous copper synthesized from $2\mu\text{m}$ $\text{Cu}_{25}\text{Si}_{75}$ amorphous thin-film precursors had an average ligament size of 32nm under electrochemical dealloying with 3% HF. Acetic acid treatment of foams resulted in removal of native oxide layers with no discernible change in the nanoporous microstructure. While the as-prepared dealloyed under 5-40°C structures had local variations in NP structure connectivity, pore and ligament distribution, all the as-prepared samples had effectively the same structure as verified through 2-point spatial correlation based on pore-density calculations across the binarized as-prepared

images. The 2 μ m Cu-Si film shrunk to about 1.55 μ m on average after undergoing dealloying with a Z-shrinkage value of 81% on average across all as-prepared samples.

Under thermal and electrolyte coarsening, the F300 samples showed maximum shrinkage from as-dealloyed condition to 65% with a final relative density of 93% after 60 minutes. With time, this microstructure evolved from a smooth porous network to that of a bimodal faceted particle-based morphology. A bulk diffusion-based mechanism was proposed to explain mass transfer from ligaments into nodes, with diffusion of Cu atoms from the ligaments into the nodes, creating agglomeration and bulk-phase formation. A coarsening exponent of $n = 3.33$ for the forming gas-coarsening cases, signifying thermally-activated bulk diffusion validated this hypothesis.

The electrolyte coarsened samples shrunk to 68% while showing a linear increase in relative density from 62% to 82%. This change is evident through the self-similar evolution of the microstructure with time. All the tracked features such as ligament length, nodes and width increased in size under extended dealloying, contradicting the macroscopic shrinkage behavior of the foams. Under extended dealloying, local tensile stresses caused ligaments to plastically deform and collapse, thus causing shrinkage. This excess mass was proposed to be redistributed throughout the porous network in a self-similar manner on account of high surface diffusion rates. The coarsening exponent of $n = 4.55$ for the electrolyte-coarsened foams signifying surface diffusion modes validated this hypothesis. Surprisingly, the N₂-coarsened foams as well showed a coarsening exponent of $n = 4$, which could point to the detrimental effect of oxidation of NP metals. A native oxide layer could prevent thermally activated diffusion modes and promote surface diffusion; more

studies are required to understand the combined effect of oxidation and sintering on nanoporous foams.

In conclusion, it was shown that fundamentally, sintering in electrolyte-treated foams is governed by a non-densifying surface-diffusion driven mechanism of coarsening, while in the case of forming gas-treated samples, particle centers move closer to each other under bulk transport, causing significant densification. This distinction in materials transport mechanism will help create tailored morphologies of nanoporous metals for application as die-attach materials in power electronic packages

5.2 Manufacturable Synthesis with Co-electrodeposition

In the previous section, fabrication of proof-of-concept nano-Cu foams was demonstrated using co-sputtering and dealloying. The sintering behavior of these foams was observed and an initial bonding demonstration of nano-Cu foam interconnections was demonstrated. However, sputtering as a fabrication approach is not feasible in high-volume production. As a result, a cost-effective route utilizing electrodeposition of Cu-X alloys is required in order to build Cu pillar interconnections with nano-Cu foam caps using standard lithography processes. In this section, the advances made in realizing patterned nano-Cu foams onto a bulk-Cu substrate are reported. The general process flow for achieving the patterned foams has been shown in Figure 5.22.

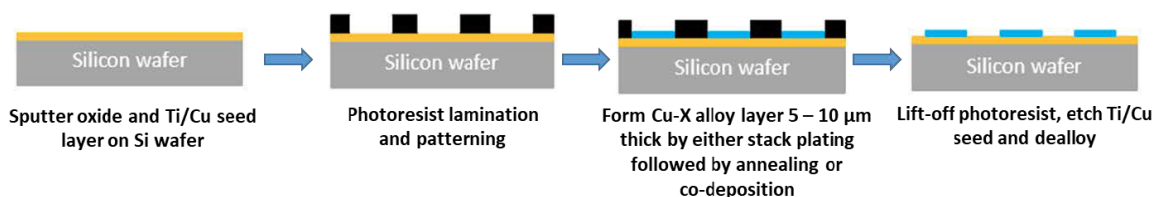


Figure 5.22 Process flow for fabrication of patterned nano-Cu foam films

5.2.1 Choosing precursor alloy system

Broadly, a binary alloy system consisting of copper (less than 50 at. %) and more-reactive element (lower reduction potential) is required to form nano-Cu foams. The Cu-Zn alloy system was selected for this purpose due to the relatively high electrochemical potential of Zn (VSHE = 0.76V) as compared to copper (VSHE = -0.3V) giving stability and uniform structure of the nanocopper foam after synthesis. A close look at the Cu-Zn phase diagram (Figure 5.23) showed that a composition range of Cu from 20-30 atomic % would form a two-phase solid solution system consisting of γ and ϵ phases. Both these phases of Cu-Zn are Zn-rich and would dealloy in a similar manner to form uniform nanoporous Copper.

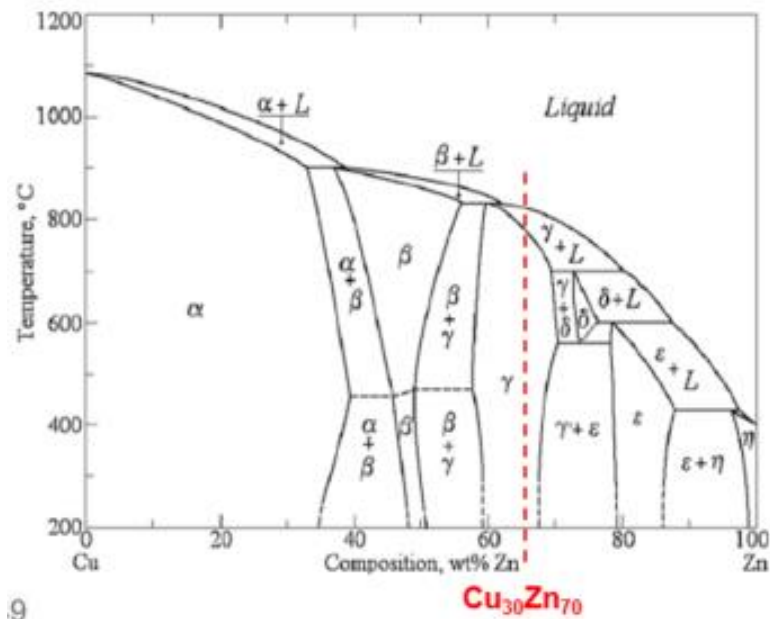


Figure 5.23 Cu-Zn phase diagram

However, the deposition rate of Cu is quite high as compared to Zn from cyanide-free sulfate-based acid electroplating chemistries, thus requiring the aid of organic surfactants to improve the mobility of the Zn ions and enhance the deposition of Zn in the required atomic %. Two different approaches were explored using the Cu-Zn metallurgical system. In the first approach, Zn was stack-plated over Cu substrates, followed by a low-temperature annealing step to form Cu-Zn alloy. In the second approach, both Cu and Zn were co-electrodeposited on Cu substrates to form the Cu-Zn alloy. After the resultant alloy formation, the Cu-Zn films were dealloyed to synthesize nano-Cu foams.

5.2.2 Stack-plating of Cu-Zn and dealloying

To synthesize Cu-Zn alloy, Zn was electroplated on thin sheets of Cu (3cm x 5cm) using a customized 3-electrode setup as shown in Figure 5.24(a). ZnSO_4 (0.1 M) was used as the

electrolyte and the current densities were set between 2-10mA/cm². The plating time was optimized to achieve the desired Cu:Zn ratio of 30:70 by weight. Subsequently, the Zn plated Cu sheets were annealed at 250°C for 8h to form a homogenous Cu-Zn alloy and then dealloyed in 5% HCl to form nanocopper foams, as shown in Figure 5.24(b). While these preliminary results demonstrated the potential of Cu-Zn alloy system to fabricate nanocopper foams, the Cu sheets stack-plated with Zn required a large annealing window to enable diffusion of Zn in Cu and facilitate the formation of Cu-Zn alloy. Solid-state diffusion is fundamentally a slow process, which limited both the thickness and uniformity of the initial Cu-Zn alloy films that could be synthesized. Therefore, going forward, co-electrodeposition of Cu-Zn was chosen as the preferred option to fabricate patterned Cu-Zn alloy films.

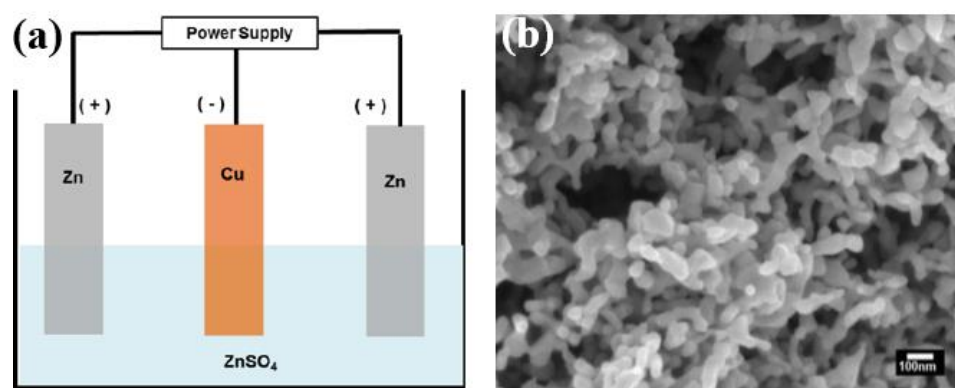


Figure 5.24 Schematic of a 3-electrode cell used to electroplate Zn on Cu sheets; and (b) plan-view SEM image showing nanocopper foam with 30-40nm ligament size

5.2.3 Co-electrodeposition of Cu-Zn and dealloying

5.2.3.1 Preliminary setup for co-electrodeposition of Cu-Zn alloys

In co-electrodeposition, both Cu and Zn atoms are simultaneously deposited over a conducting substrate. The deposited Cu and Zn atoms fuse together even at room temperature to form the Cu-Zn alloy [172]. Furthermore, the Cu:Zn ratio in the deposited films can be varied in a wide range by changing the deposition parameters, giving flexibility in designing the initial alloy films. Co-electrodeposition process is most suitable for fabricating patterned foam architectures for bumped interconnections but can also be extended to fabricate standalone nano-Cu films by using a sacrificial substrate. Based on literature review, it was decided to use potassium pyrophosphate (PP) chemistry-based plating baths, with additions of CuSO_4 and ZnSO_4 in it. From manufacturability perspective, unlike the more established cyanide baths for plating brass (Cu-rich Cu-Zn phases), PP baths are non-toxic, easier to maintain and recycle [173-175]. During electroplating, from only sulfate-based plating baths, the deposition rate of Cu is quite high as compared to Zn which makes it very difficult to obtain zinc-rich alloys. Based on literature review, Cu:Zn composition in the range of 30:70 is the most favorable for dealloying and synthesis of copper nanofoams [73, 80]. Addition of PP to the sulfate-based plating baths stabilizes the Cu^{2+} ions, shifts their reduction potential towards that of Zn^{2+} , making it much more feasible to co-deposit Zn rich alloys. For the preliminary co-plating experiments, the concentration of PP was fixed between 0.7M - 0.8M and the ratio Zn^{2+} and Cu^{2+} was varied to find the best combination. Linear sweep voltammetry experiments were conducted for these different bath compositions and it was found that 0.025M CuSO_4 and 0.25M ZnSO_4 gave a good potential window for co-deposition as shown in Figure 5.25. These experiments were carried out using 3-electrode cell setup with SCE as reference electrode (RE), Cu clad FR4 as working electrode (WE) and Pt as counter

electrode (CE). Based on the potential window, amperometric tests were run to deposit Cu-Zn films at different potentials. The bath chemistry was 0.25M ZnSO₄, 0.25M CuSO₄ and 0.8M PP. It was found that at higher negative deposition potentials, Zn deposition became more favorable: Zn concentration varied from ~40% at -1.65V to ~88% at -2.1V.

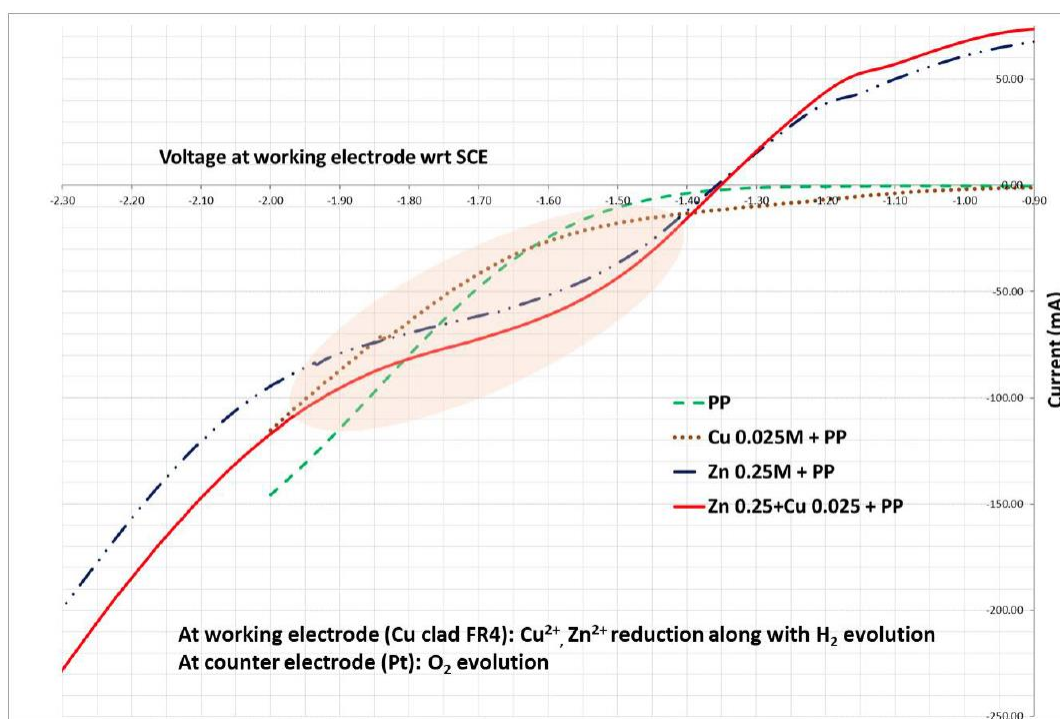


Figure 5.25 Linear sweep voltammetry results for 0.25M ZnSO₄, 0.025M CuSO₄, 0.8M PP with Pt as the counter electrode. The highlighted area indicates the deposition potential region of interest

However, at negative deposition potentials, the deposition current densities also increased rapidly. Higher current densities are known to produce uneven surface morphologies due to very fast deposition rates. Moreover, H₂ evolution at the WE and O₂ evolution at the Pt CE also became more intense at higher negative potentials resulting in higher porosity in

the Cu-Zn films. The observed surface morphology was quite uneven, probably also due to intense bubbling in the bath (Figure 5.26(a)).

The deposited Cu-Zn films were then subsequently dealloyed in 10wt% HCl to form nanocopper foams as shown in Figure 5.26(b). It was observed that the nanocopper foam formation was more favorable for Cu-Zn alloys having Zn concentration greater than 65%. Also, the nanocopper foam surface morphology followed the initial morphology of the Cu-Zn films, resulting in an uneven nanocopper foam surface.

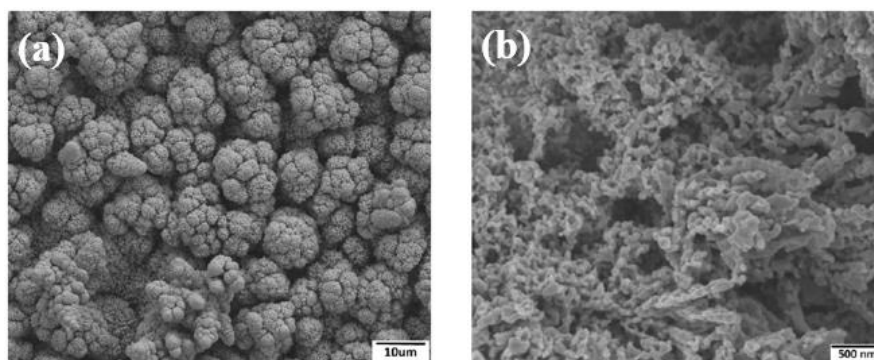


Figure 5.26 (a) Surface morphology of as-plated Cu-Zn film at -1.8V. Cauliflower disjointed morphology can be seen, probably due to intense bubbling of bath and high plating current densities at higher negative potentials; (b) Nanocopper foam formation after dealloying

To potentially improve the surface morphology of the Cu-Zn films, it was decided to replace Pt with Zn sheet as CE. Using Zn as CE, helped get around O₂ evolution which drastically reduced the bubbling in the plating bath. The reaction at CE changed to oxidation of Zn atoms to Zn²⁺. To understand the effect of using Zn CE on co-deposition of Cu-Zn alloy, linear sweep voltammetry and amperometric tests were conducted as mentioned before. The results of linear sweep voltammetry are shown in Figure 5.27. Replacing Pt with Zn CE also reduced the deposition currents significantly in the desirable

deposition potential range. Lower deposition currents are desirable to synthesize plated films with uniform and smooth surface morphologies. Moreover, it was observed that the I-V curves were flatter with reduced slope as compared to the I-V curve with Pt as the CE. This was probably observed because the Zn electrode has a lower catalytic activity for H_2 evolution on its surface as compared to Pt.

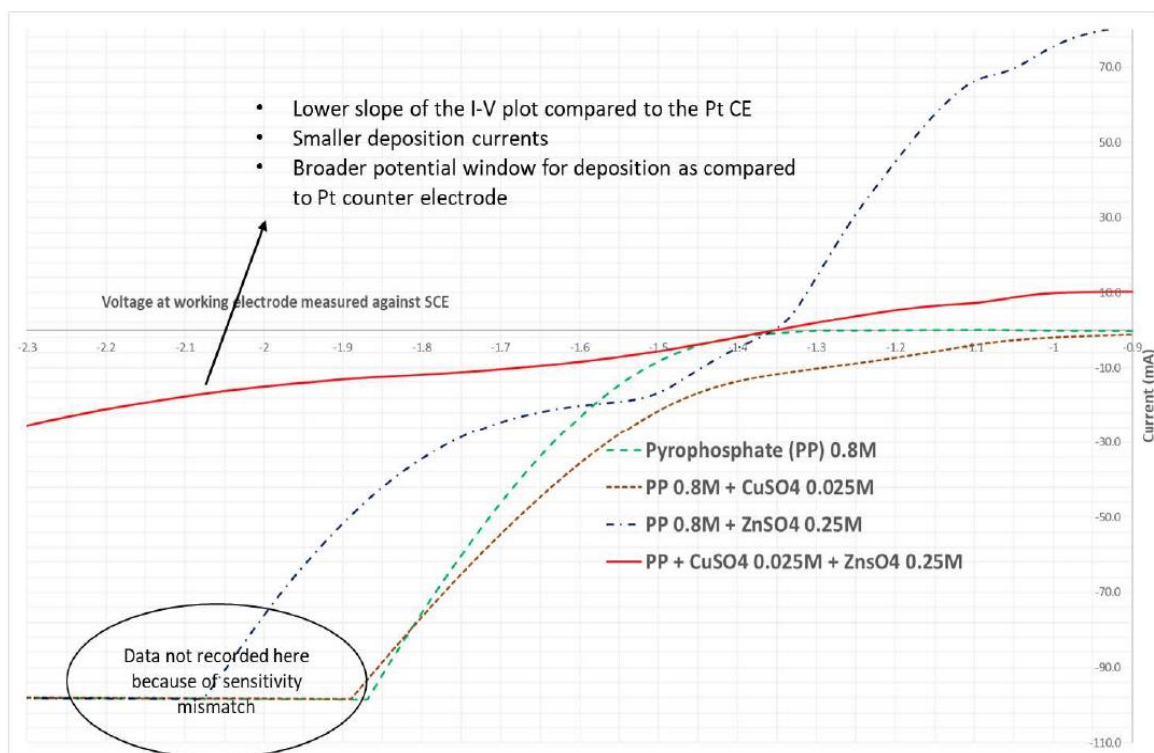


Figure 5.27 Linear sweep voltammetry results for 0.25M $ZnSO_4$, 0.025M $CuSO_4$, 0.8M PP with Zn as the counter electrode

After the positive I-V results with Zn as CE, PP, Zn and Cu concentrations were also optimized based on a parametric study. The Cu concentration was varied from 0.005M-0.025M. It was observed for 0.005M Cu concentration, the reduction potential of Cu^{2+} was slightly more negative as compared to 0.025M Cu^{2+} (-1.36V for 0.005M Cu^{2+} and -1.34V for 0.025M Cu^{2+}). Zn^{2+} concentration was varied from 0.25M-0.3M. As the Zn^{2+} concentration increased, Zn rich alloys could be co-plated at lower negative deposition

potentials, which helped in further reducing the current densities. The surface morphology of the Cu-Zn film plated at -1.7V using 0.015M Cu^{2+} , 0.3M Zn^{2+} and 0.7M PP is shown in Figure 5.28. The Cu:Zn ratio was ~30:70 as determined by EDX analysis. The surface morphology was much more uniform and smooth as compared to plated surface morphologies obtained by using Pt CE. However, at such high concentrations of Zn^{2+} ions, the dealloying was not effective enough to completely remove the Zn impurities post-dealloying. As a result, further optimization of the electrolyte chemistry and dealloying conditions was carried out for the formation of crack-free nano-Cu foams, as outlined in the following sections.

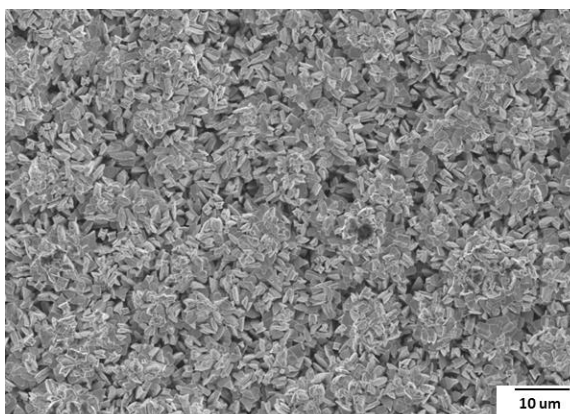


Figure 5.28 Surface morphology of as-plated Cu-Zn film at -1.7V with Zn as CE. Bath composition was Cu^{2+} 0.015M, Zn^{2+} 0.3M and PP 0.7M. The as-plated morphology was more uniform as compared to as-plated morphology obtained with Pt CE.

5.2.3.2 Current density modulation and annealing for crack-free synthesis

For this study, a fixed electrolyte composition of 0.0025M CuSO_4 , 0.15M ZnSO_4 and 0.3M PP was used to co-deposit Cu-Zn films. 4x4 cm² Si wafer coupons with Ti/Cu seed layer were used to deposit blanket Cu-Zn films at different current densities. Scanning electron microscope (SEM) and energy-dispersive X-ray spectroscopy (EDXS) analyses

(Hitachi SU-8230 SEM equipped with EDS) were performed on as-plated samples to understand the effect of current densities on the composition and morphology of the films. The summary of results is presented in Figure 5.29. With the plating time fixed at 90min, the current densities were varied from 1-6 mA/cm². At a plating current density of 1mA/cm², the Cu-Zn alloy films had ~80 atomic % Zn, which increased to ~96% with increase in the plating current densities to 6mA/cm². This was also reflected in the morphology of plated Cu-Zn films. At lower current densities, more spherical grains, typical of α and β Cu-rich phases were observed. As the current density increased, the morphology changed to hexagonal needle and flake-like structures, typical of Zn rich phases. After plating, the samples were dealloyed in 1wt% hydrochloric acid (HCl) for 4 hours at room temperature. All the samples successfully dealloyed to form nanoporous Copper (np-Cu) foams. However, a large variation was observed in the morphology of the foams with change in the composition and morphology of as-plated Cu-Zn films. Samples plated at 1mA/cm² formed np-Cu foams with ligament size in the range of 80-100nm. The residual Zn left after 4 hours of dealloying was ~18%. Macro-scale channel-like cracks, ~0.5 μ m in width, were also observed after dealloying. It was evident that the initial grain structure of the Cu-Zn alloy films was preserved during dealloying. For dealloyed samples plated at an intermediate 2.75mA/cm², the width of the macro-scale cracks increased to 1-2 μ m, while the residual Zn after dealloying decreased to ~10%. Moreover, the foam morphology also became finer with ligament sizes under 60nm. In the samples plated at 6mA/cm² and subsequently dealloyed, cracks in the foam films both at macro and micro-scale were observed. The width of the cracks at macro-scale increased to 3-4 μ m. However, the residual Zn after dealloying decreased to below 4%. These results are summarized in

Figure 5.29. It was surmised that the creation of larger cracks eased the interaction of the Cl⁻ ions with the Zn-rich phases (with higher current densities) and brought about a faster dissolution of said phases, bringing down the residual impurity content post-dealloying.

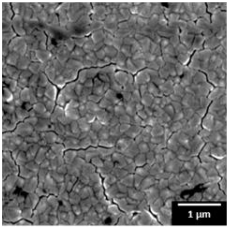
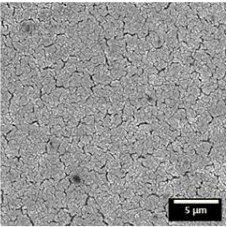
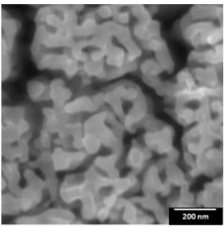
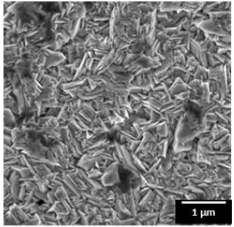
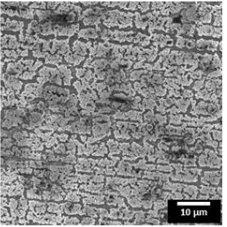
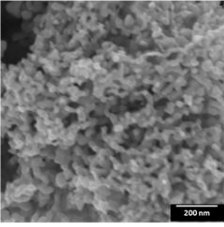
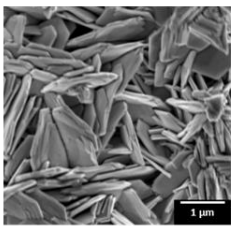
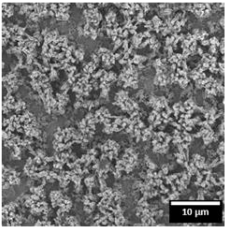
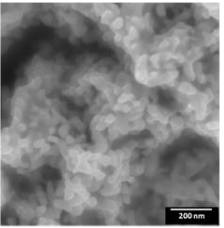
Plating current densities	As-plated morphology	Morphology after dealloying	
		Low-mag	High-mag
1 mA/cm ²	 <i>Zn ~ 80%</i>	 <i>Residual Zn ~18%, Ligament size 80-100nm</i>	
2.75mA/cm ²	 <i>Zn ~ 89%</i>	 <i>Residual Zn ~8%, Ligament size <60nm</i>	
6mA/cm ²	 <i>Zn ~ 96%</i>	 <i>Residual Zn < 4%, Ligament size <60nm</i>	

Figure 5.29 Variation in morphology of as-plated Cu-Zn and dealloyed np-Cu foam films with plating current densities

To address the challenge of cracks in the foam films after dealloying, the Cu-Zn plated films were annealed at 200°C for 30min under Nitrogen (N₂) gas prior to dealloying. Figure 5.30 compares the effect of annealing on as-plated and dealloyed np-Cu foam films morphology for samples plated at 2.75mA/cm². SEM images of the annealed samples

revealed a slight compaction of the surface and smoothening of the edges of the features as compared to the as-plated surface morphology, indicating diffusion-enabled homogenization of the as-plated films. EDXS analysis showed that surface copper concentration increased by 4% after annealing. Annealing, possibly also relieved the stresses in the Cu-Zn film generated during the plating process. However, the observed variations were very subtle and would require more robust analyses to quantitatively conclude on the effect of annealing on surface morphology, composition and plating stresses with certainty. After annealing, the samples were dealloyed in 1wt% HCl at room temperature for 4 hours. The dealloyed foam morphology showed drastic reduction in both the number of macro-scale cracks and the width of the cracks. The morphology was coarser as compared to the morphology of as-plated and non-annealed dealloyed foams, while the ligament size was maintained at less than 60nm.

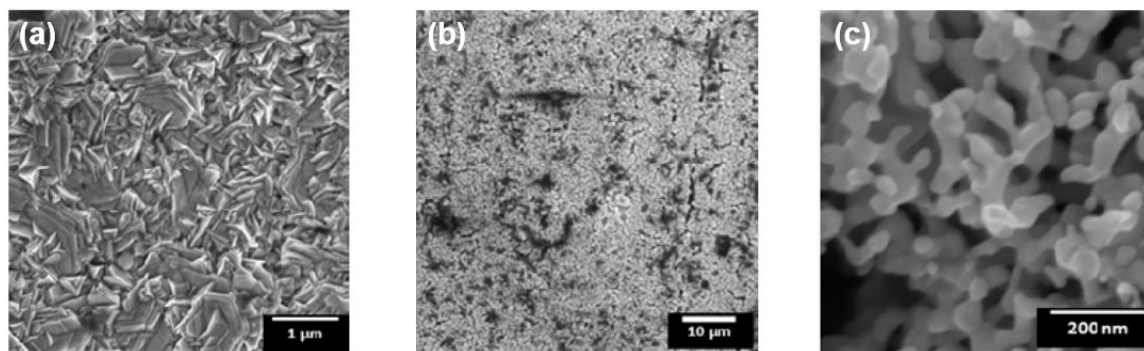


Figure 5.30 SEM images of (a) annealed Cu-Zn samples plated at current density of 2.75 mA/cm²; low-mag (b) and high-mag (c) SEM images of dealloyed nanoporous copper

Based on these trials, the co-electrodeposition process was leveraged for patterning photodefined features, as shown in the next section.

5.2.4 *Fine-pitch patternability*

The next step in demonstrating the applicability of such foams to fine-pitch interconnections and assembly, is the ability to pattern specific features and establishment of a baseline wafer-level bumping process. The TV1 design (section 3.3.1) was utilized to form sub-100 μm RDL dogbone features as a first demonstration of fine-pitch patternability. Si wafers with an SiO_2 barrier and sputtered Ti/Cu seed layer were used as base substrates. A liquid spin-on photoresist from JSR Corporation was coated at 2000rpm to form a 16 μm thick resist layer. This was then exposed and developed to form the desired RDL features. After photoresist patterning, 4-8 μm of Cu was plated on the Cu seed layer and the samples were annealed to relieve the plating stresses in the Cu layer. Annealing was followed by co-deposition of 5-10 μm of Cu-Zn. Plating current densities were maintained in the range of 4-6 mA/cm^2 . Care was taken to ensure that the photoresist would not degrade at such current densities and cause undercutting. Then, the photoresist was stripped and the samples were annealed at 150°C for 30min to relieve the stresses in the Cu-Zn layer and improve the homogeneity of the Cu-Zn alloy. Using a profilometer, the initial thickness of plated Cu and subsequent thickness of plated Cu-Zn were verified at 5 μm and 7 μm respectively. This was followed by singulation of the wafer into individual dice, which were finally dealloyed under 1% HCl to form patterned np-Cu foam features on plated Cu. Optical images after Cu-Zn plating and dealloying are shown in Figure 5.31. The Cu-Zn plated features had sharp boundaries and no bridging was seen after plating. It was observed that dealloyed features maintained the original shape of initial Cu-Zn film in the lateral dimensions, however shrinkage in Z-height was noticed due to etching out of the Zn.

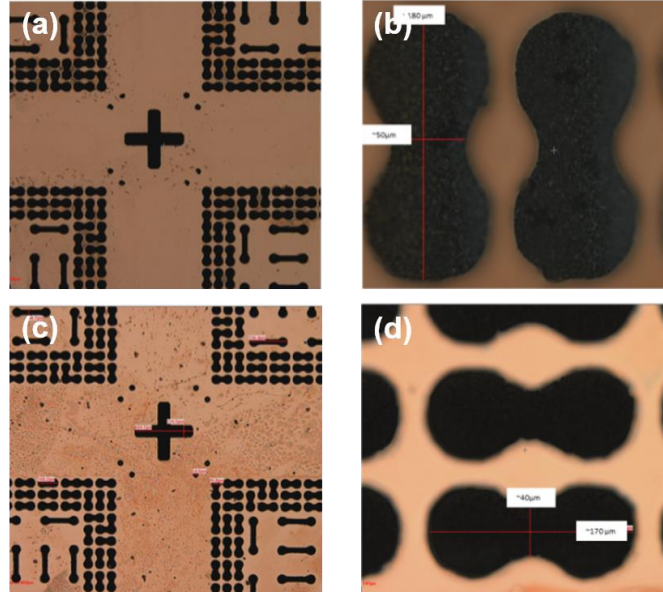


Figure 5.31 Patterned features after (a)-(b) Cu-Zn plating and (c)-(d) after dealloying

5.3 Fine-pitch Assembly Demonstration

To demonstrate nano-Cu foam caps on Cu bumps, the design from TV1 (section 3.3.1) was utilized consisting of 30µm diameter Cu bumps at a pitch of 100µm. Si wafers with sputtered Ti/Cu seed layer were used as base substrates. A 15µm-thick Hitachi 5115 UTEB dry-film resist was exposed under a dose of 180 mJ/cm² and developed to form the patterned 30µm-diameter features. Electroplating of Cu was carried out till an average height of ~7µm across all the bumped features. Then, Cu-Zn plating was carried out (according to the plating parameters discussed in section 5.2.3.2) to an average height of 7-9µm. This was verified using a profilometer as shown in Figure 5.32. SEM images of the as-patterned features are as shown in Figure 5.33(b)-(c) with a SEM-EDX analysis showing Cu:Zn in a 25:75 atomic % ratio (inset). This wafer was then singulated into individual 5mm x 5mm dies which were subsequently dealloyed under 1% HCl for 3 hours. The samples were completely dealloyed, forming a fine-morphology nano-Cu foam with

an average ligament size of 40nm. The SEM images of the as-patterned nano-Cu foam bumps are as shown in Figure 5.34.

Finally, assembly trials were carried out using these fine-pitch Cu pillar interconnections with nano-Cu foam caps bonded to a Si substrate with blanket electroplated copper. Bonding was carried out successfully on the Finetech Fineplacer tool at 300°C – 30MPa – 30min to ensure a complete bond under the active presence of forming gas. A capillary underfill was utilized to protect the formed joints under full cure conditions of 165°C – 3hrs. The SEM cross-section of the bonded interface is as shown in Figure 5.35. The SEM-EDS data across the bonded interface showed a Zn concentration of <0.2 atomic %. However, there were some voids observed at the bonding interface and further optimization of the sintering conditions is required to create void-free interfaces

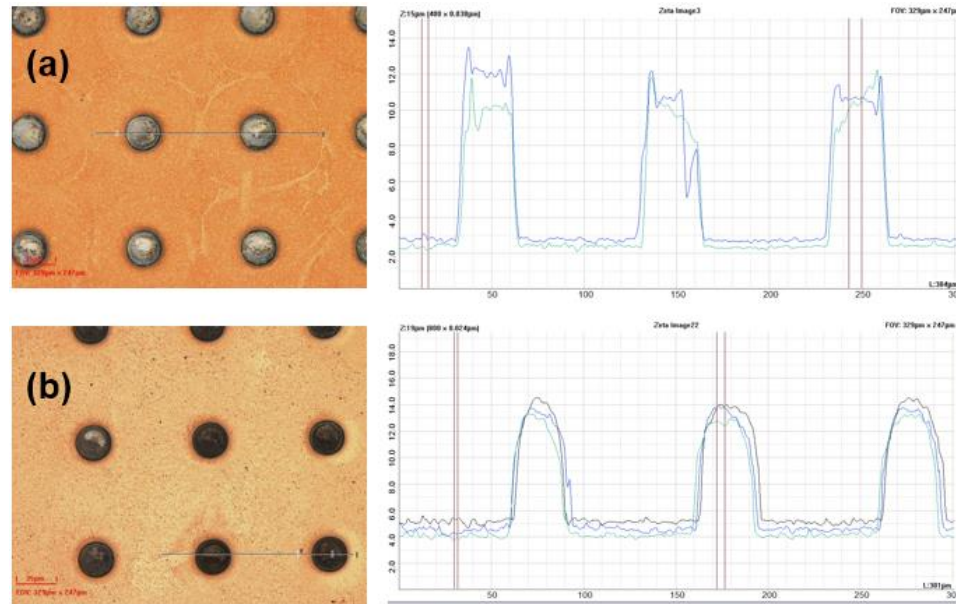


Figure 5.32 Optical images and profile of (a) plated Cu-Zn on Cu bumps and (b) nano-Cu foam caps on Cu bumps

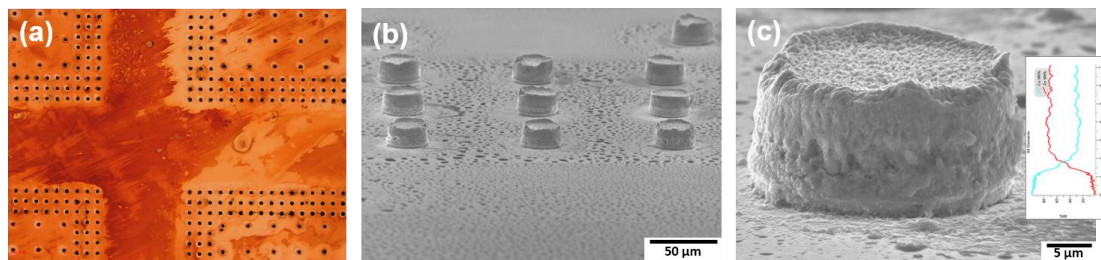


Figure 5.33 (a) Optical image of patterned fine-pitch features; (b) SEM image of Cu-Zn plated on Cu bumps and (c) high-mag image of such a Cu bump with inset SEM-EDS data

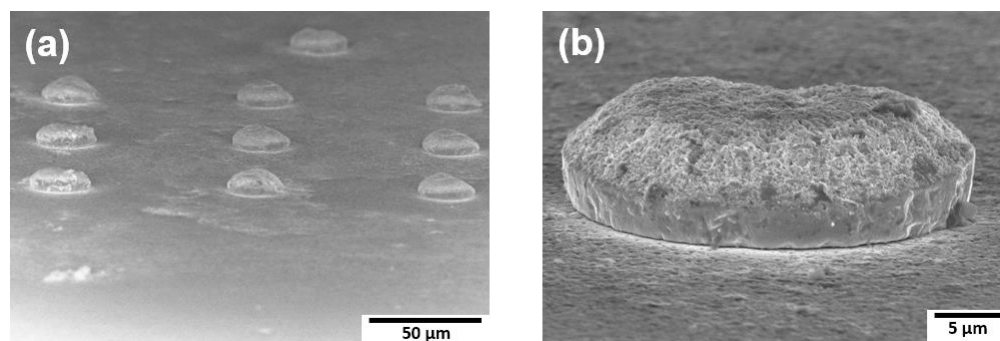


Figure 5.34 SEM images of dealloyed nano-Cu foams caps on Cu bumps at (a) low mag and (b) high mag

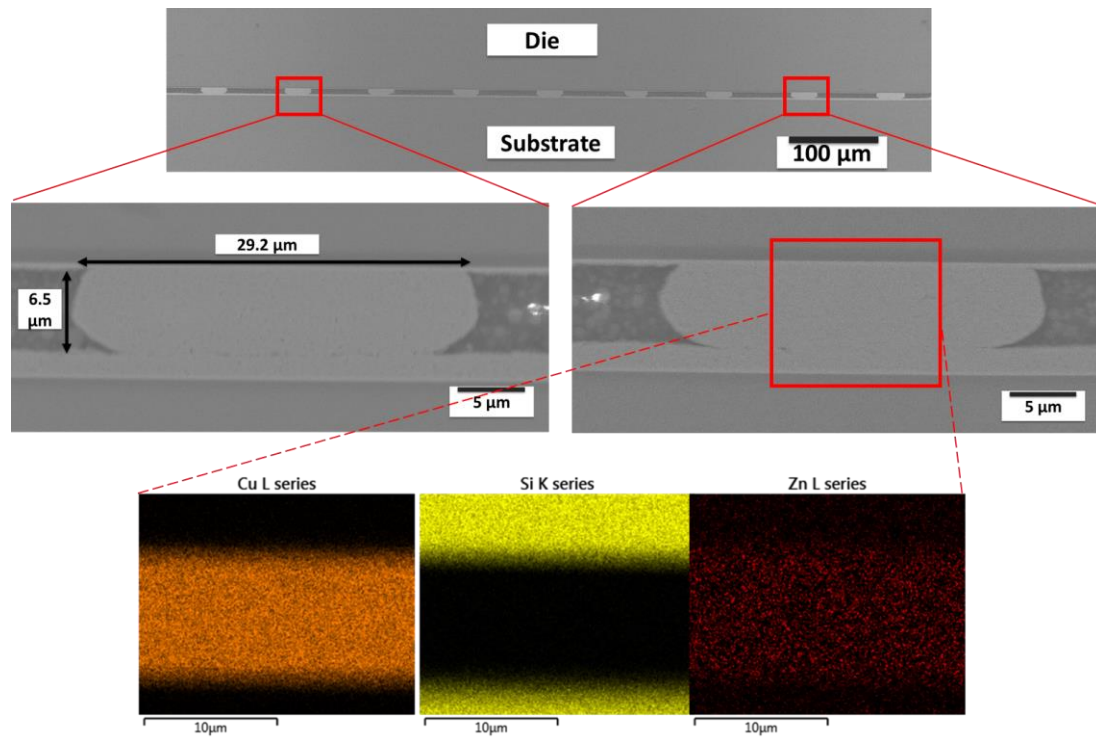


Figure 5.35 SEM cross section of as-bonded Cu pillar interconnections with nano-Cu foam caps with SEM-EDS data across the Cu bumps

Furthermore, shear testing of the as-bonded nanocopper foam parts at a standard 15μm/sec speed gave a maximum strength of 22MPa with shear occurring through the densified Cu foam interface. Figure 5.36 shows the die and substrate profile of the failed interfaces with densified nano-Cu foam visible on both surfaces.

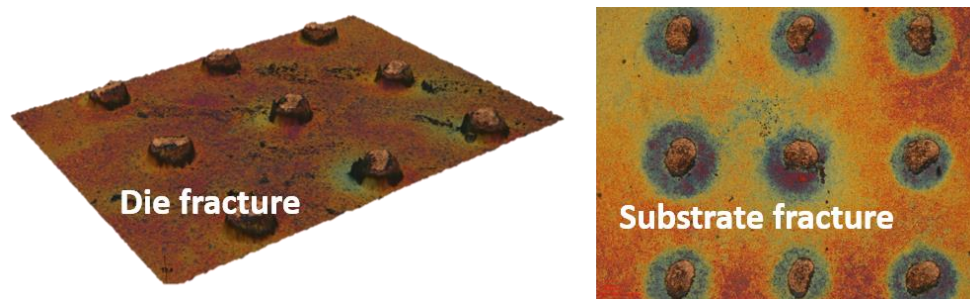


Figure 5.36 Failure profile of sheared nano-Cu foam cap assembly with die and substrate profiles reflecting a failure through the densified foam layer

5.4 Chapter Summary

In this chapter, the use of a solid-state, low-modulus nanocopper foam cap was proposed as compliant bonding interface, akin to solder. The foam morphology, particularly the ligament size and initial relative density, were designed from first principles to achieve the desired elastic modulus in the 20-40GPa range while having sufficient reactivity for low-temperature, high-speed assembly. On account of the high surface area and curvature of these foams, a low-temperature sintering to almost 95% density was demonstrated under forming gas flow, confirming feasibility of metallurgical joint at 250°C, as a first proof-of-concept. Through rigorous optimization cycles, an electroplating-based method involving co-deposition of Cu-Zn layers and subsequent dealloying was employed to assess bumping manufacturability with these foams for large-area interconnections. The electroplating and dealloying processes were optimized to form crack-free foams of the target thickness. Then, a fundamental study of the densification behavior of the foams was carried out concurrently to provide some insight on sintering kinetics with temperature and environment. It was found that the sintering kinetics of foams is similar to the intermediate-stage sintering of nanoparticles, with mass diffusion occurring across preformed necks. Lastly, low-pressure (30MPa) assembly of fine-pitch nano-Cu foam caps, co-electrodeposited and dealloyed on 30 μ m-diameter Cu bumps was successfully demonstrated at 100 μ m pitch with maximum shear strength of 22MPa.

CHAPTER 6. SUMMARY AND CONCLUSIONS

This chapter summarizes the research work carried out in this thesis to improve pitch scalability, assembly throughput as well as reliability of solid-state off-chip all-Cu interconnections. High-performance solid-state Cu interconnections without solders were demonstrated through design and optimization of the bonding interfaces for assembly manufacturability and thermomechanical reliability, with the following two key innovations, pursued in parallel: 1) novel thin-film Pd-Au bilayer metallic coatings applied on Cu micro-bumps and pads; and 2) reactive high-surface area nanocopper foam caps, pioneering the new “Cu pillar with nanocopper caps” technology. By introducing a 2-step assembly process with pre-applied underfill such as NCP, high-throughput assembly was achieved, yielding Cu-like interconnections with superior power handling capability, thermal stability as well as improved reliability. Recommendations for future work are also briefly discussed along with conclusions and scientific contributions.

6.1 Research Summary

The primary objective of this research is to demonstrate reliable, chip-to-substrate Cu interconnections without solders at 20 μ m pitch with superior power handling capability and thermal stability, formed by high-throughput assembly, to meet the needs of emerging high-performance computing applications. Current direct Cu-Cu bonding face two primary challenges in achieving these goals: 1) high-throughput assembly; and 2) high thermomechanical reliability of the joints in a chip-to-package system with mismatch in thermal expansion. Two unique technologies were proposed, designed and demonstrated to address both of these challenges: 1) Cu interconnections with ultra-thin Au-based

metallic coatings and Cu interconnections with nanocopper foam caps. The developed technologies address the shortcomings of current technologies in pitch scalability and performance with power handling at current densities at least an order of magnitude higher than what solders can sustain, and with significant improvements in assembly throughput and manufacturability, as well as reliability, over existing technologies for direct Cu-Cu bonding. To achieve the aforementioned objectives, two research tasks were defined for each individual approach: 1) modeling and design of the bonding interfaces and assembly processes for high-throughput manufacturing; and 2) design and demonstration of the interconnection reliability at interconnect joint and on-chip low-K dielectric levels. This document presented first an extensive review of the state-of-the-art of direct Cu-Cu bonding in research and industry. A summary of the progress made in each of the tasks was then provided. The key novelty and takeaways of this research are highlighted in the task summaries below.

6.1.1 Modelling, design, and demonstration of copper interconnection system for improved reactivity and accommodation of non-coplanarities

This research task aims at designing novel solid-state interconnection technologies and demonstration of high-throughput assembly in a chip-to-substrate architecture with CTE mismatch. Two approaches were concurrently undertaken to address this challenge and provide options for implementation by the semiconductor industry. The first approach relies on the use of ultra-thin Au-based coatings on Cu bumps and pads to prevent room temperature oxidation and provide softer, more reactive bonding interfaces. Due to the inability to deposit Au directly on Cu, standard ENIG (Ni/Au) and novel thin-film EPAG (Pd/Au) surface finishes were considered in this study, leveraging electroless processes

traditionally reserved for substrate processing for low cost. Both interconnection systems were designed based on kinetics and diffusion modeling analysis to provide sufficient shelf life, and form strong and reliable metallurgical joints at temperatures below 250°C, with stable microstructure through thermal aging at 200°C and power handling at 10^5 A/cm^2 . In the Ni/Au system, a 3 μm -thick layer of Ni was designed as barrier layer to inhibit diffusion of Cu so the bonded interface remains unreacted Au throughout the life of the package assembly. In the Pd/Au system, Cu was found to rapidly diffuse through thin Pd interface through defect pathways via grain boundary diffusion, allowing controlled interdiffusion between Cu and Au. The Au reacting layer was then designed to ensure formation of the ductile and stable AuCu intermetallic at the bonded interface. Finite element and stress-strain models were then built to understand the stress distribution and deformation behavior in thermocompression assemblies. In the Cu/Ni/Au system, stiff Ni was found to block deformation of Cu, yielding bonding pressures exceeding 365MPa to achieve 3 μm collapse of the joints, required to achieve good assembly yield considering bumps and pad non-coplanarities and chip and substrate warpage. Such bonding pressures exceeded the force capability of our bonding equipment, preventing conclusive evaluation and demonstration of this technology. The Cu/Pd/Au system was found to mostly retain the compliance of Cu, however limited, yielding a 3X decrease in expected bonding pressures for the same bump collapse, down to 120MPa. The effect of the bump shape on the stress distribution in the on-chip and on-substrate wiring layers was also evaluated, highlighting the importance of bump planarization to prevent stress build-up and subsequent delamination of the Cu traces on substrate.

In the second approach, the use of a solid-state, low-modulus nanocopper foam cap was proposed to reinstate a compliant bonding interface, much like solder was. The foam morphology, particularly the ligament size and initial relative density, were first designed to achieve the desired elastic modulus in the 20-40GPa range while having sufficient reactivity for low-temperature, high-speed assembly. A 2-step fabrication, involving alloying of two elements with vastly different electron affinities and its subsequent dealloying to etch-out the ‘more reactive’ element was employed to form nanocopper foams of various length scales (20-500nm). Ligament sizes in the 30-60nm range were found to give the best performance, resulting in initial relative densities of the foams of ~60%. A fundamental study of the densification behavior of the foams was carried out concurrently to provide some insight on sintering kinetics with temperature and environment. It was found that the sintering kinetics of foams is similar to the intermediate-stage sintering of nanoparticles, with mass diffusion occurring across preformed necks. On account of the high surface area and curvature of these foams, a low-temperature sintering to almost 95% density was demonstrated under forming gas flow, confirming feasibility of metallurgical joint at 250°C, demonstrating as a first proof-of-concept.

An electroplating-based method involving co-deposition of Cu-Zn layers was employed to assess bumping manufacturability with these foams for large-area interconnections. After rigorous optimization of the plating and dealloying parameters, successful assemblies of nanocopper foam-on-bulk Cu with significant pressure reduction to 9MPa at 250°C were also demonstrated, thus validating the sintering kinetics studies.

To demonstrate lithography-compatible patterning that is required for fine-pitch and high-density devices, Cu interconnections with nanocopper caps were then fabricated

through electrodeposition of a Cu-Zn alloy on 30 μ m diameter Cu micro-bumps and subsequently chemically dealloyed to form foam-on-bump structures, similar to the current Cu pillar technology. The novel process involved just one extra step of dealloying compared to conventional solder plating, without the need for reflow, thus avoiding a reflow step. The electroplating and dealloying processes were optimized to form crack-free foams of the target thickness. Lastly, such nanocopper foam-capped interconnections were demonstrated on 100 μ m pitch test vehicles with Pd/Au metallization, thus validating bondability on standard surface finishes.

6.1.2 Design and demonstration of high-speed assembly of Cu interconnections

Based on the design guidelines, daisy-chain test vehicles were fabricated to demonstrate and characterize the as-fabricated Cu/Pd/Au interconnections. A novel, low-cost planarization of the Cu bumps using DISCO Corp's fly-cut tool was also used to validate the modeling predictions. A thin-film Pd/Au metallic coating composed of 100nm electroless Pd and 250nm autocatalytic Au were then applied on Cu bumps and substrate pads. Assembly was successfully demonstrated at 250°C and SEM/EDX characterization confirmed the formation of the expected stable AuCu intermetallic phase. Die shear tests on CTE-matched and non-patterned substrates also confirmed the excellent quality of the metallurgical bonding, with a maximum shear strength of 190MPa observed for the planarized Cu-EPAG interconnections, comparable to that of direct Cu-Cu bonding while much higher than that of traditional solder interconnections. thermal ageing studies were carried out at 250°C for 1000 hours on as-plated (non-planarized) and planarized assemblies. While the as-plated assemblies exhibited a continuous degradation of the bonded interfaces with the average shear strength dropping below 25MPa, the planarized

assemblies stabilized at shear strengths exceeding 40MPa (comparable to solder-based interconnections). XPS and EDS-enabled analysis confirmed the formation of brittle CuO at the interface of non-planarized joints due to the diffusion and oxidation of Cu in the non-contacted areas. This microstructural analysis also confirmed the formation of stable continuous AuCu phases under thermal ageing of planarized interconnections, thus giving higher shear values.

Based on diffusion kinetics across the Cu/Pd/Au layers, a two-step assembly process was demonstrated on non-CTE matched test vehicles at 50 μ m pitch in achieving lower bonding times under compression of less than 3sec. It consists of: a) a high-speed TC-NCP step to “tack” the chip on the substrate and initiate contact and diffusion; and b) a batch post-cure anneal at 250°C to achieve the CuAu IMC formation and metallurgical bonding. Such process involving pre-applied underfills such as NCPs also addresses thermomechanical reliability concerns by protecting the joints and alleviating mechanical stresses on on-chip low-K dielectrics directly from the assembly cool-down step, when cracks can already initiate.

6.1.3 Design and demonstration of reliability at interconnection and IC levels

To ensure bulk-like Cu properties after assembly with improved compliance, this research task aimed at demonstrating reliability of the proposed unique approaches first at interconnection level, and then at system level. Using FEM, two potential failure modes were predicted using VM-stress and plane-strain based modeling across Cu-Si interface and through bulk shear of the Cu bump respectively. Design rules were developed for chip-to-substrate Cu interconnection architectures as a function of VM-stress, Cu bump aspec

ratio and core substrate CTE. It was shown that a substrate CTE below 10 ppm/K could accommodate most bump geometries without exceeding the yield strength of Copper. Furthermore, this shift from plastic solder-based systems to rigid elastic joints can yield potential cracking of ultralow-K dielectric layers on-chip, which is a major reliability concern. To understand this stress redistribution, finite element modeling featuring a chip-to-substrate assembly with low-K dielectric stack-up was developed. A finite crack was introduced in the low-K dielectric layers and the stress-energy release rate was mapped as function of substrate type (Si, organic, glass) as well as bump dimensions. It was shown that under assembly, the pre-applied NCP materials applied compressive stresses on curing and brought down the energy release rate at the crack-tip, thus effectively preventing crack propagation in the low-K layers. Thermomechanical reliability, targeted especially in package designs with substantial CTE mismatch, was demonstrated with FR-4 organic substrates at 100 μ m pitch, with an adhesive failure mode across the Cu/Si interface, thus validating model predictions. This reliability was also successfully scaled down to 100 μ m-thick low-CTE glass substrates at 50 μ m pitch, passing over 1,000 thermal-shock cycles with a yield of over 99.5%. Furthermore, the Cu-EPAG interconnections showed excellent electromigration resistance at 3×10^5 A/cm², demonstrating high power-handling, beyond the capability of traditional solder-based interconnections. Consequently, the feasibility of novel Cu-based interconnections with the high-performance of copper and compliance, aided by low-cost planarization has been demonstrated for advanced computing applications of the next decade.

In conclusion, this work presents novel and manufacturable Cu interconnection technologies with nanoscale bonding interfaces to enable high-throughput assembly and

high thermomechanical reliability in chip-to-substrate (C2S) high-performance computing applications.

6.1.4 Suggested future work

This research work was aimed at improving throughput capability as well as demonstrating reliability of solid-state copper interconnections for advanced high-performance computing applications. From a technology perspective, two such approaches were designed through rigorous diffusion and thermomechanical modelling to improve electrical and thermal performances, while also providing adequate compliance. Based on these designs, optimization of assembly processes was carried out to ensure high-throughput bonding as well as reliability in chip-to-substrate configurations involving CTE-mismatch. A few future directions are suggested to complete this study and fully qualify the proposed technologies as the next-generation interconnection node for high-performance:

- The goal of surface finish layers is to provide oxidation protection to copper as well as improve reactivity at the interface. While Ni/Au and Pd/Au surface finishes both accomplish this task, they have their own limitations. The Ni barrier is extremely hard and causes an increase in the assembly forces, while the Pd barrier allows Cu diffusion to form stable yet weak AuCu interfaces, which degrade the shear strength. There is a need to explore thin-film diffusion barriers that prevent the diffusion of copper while retaining their compliance, thus enabling Au-Au interfaces for bonding and improving the strength of the interconnections. Thin-film Co and Ti-W layers have been shown to prevent Cu diffusion up to 400°C and

concurrent electroless plating technologies need to be developed to apply them for copper interconnections.

- In this research, a 2-step approach to improving the throughput of Cu-EPAG interconnections was demonstrated with a short thermocompression assembly step using pre-applied non-conductive paste (NCP) underfill and a post batch anneal step to improve interfacial bonding. While NCP provides excellent reliability performance and stability, the use of NCP with high filler contents is extremely challenging with flat, ultra-short, high-density bumps that typically result in filler entrapment at the interface. This can degrade performance as well as interconnection reliability. Wafer-level underfills, such as non-conductive films (NCFs) have gained momentum to address this challenge, but NCF materials are still in development and have limited flow, resulting in voiding concerns in die-to-substrate assemblies. Thus, there is a need to optimize the composition of pre-applied underfills with high filler content to ensure limited entrapment under TCB assembly in solid-state interconnections systems. Furthermore, while a 2-step assembly does improve the throughput of solid-state interconnections, thermocompression bonding is limited by traditional force and temperature requirements. As an alternative, ultrasonic bonding is now being explored to not only potentially reduce filler entrapment, but also further improve the diffusion rate across solid-state bonds with high-density bonding capability within milliseconds under thermosonic conditions.
- While initial thermomechanical reliability of Cu interconnections has been proven through modeling and experiments, this reliability assessment was performed on

non-functional wafers. The shift from solder-based interconnections to more rigid solid-state interfaces is known to yield potential cracking of on-chip ultra-low-K dielectric layers, a major reliability concern. Preliminary FEM modeling was carried out that showed promising results, as a result of compressive stresses introduced by pre-applied underfills to prevent crack propagation in the ultra-low-K layers. A new, functional test vehicle with on-chip low-K layers is, however, required to validate these modeling predictions. Such a test vehicle is currently being fabricated by Global Foundries. Furthermore, assembly has to be demonstrated on large die-sizes ($> 10 \times 10 \text{ mm}^2$) with high I/O densities that are standard in today's high-performance computing systems.

The second approach relied on the formation of foam-capped nanocopper interconnections that converted to bulk-copper by densification under thermocompression while providing compliance akin to solders. This work focused on preliminary demonstration of assembly and reliability using these novel materials. However, a more rigorous understanding of the evolution of porosity across these foams must be undertaken through electromigration and thermal cycling reliability experiments to qualify this technology for high-volume production. Furthermore, since these nanofoams are essentially introduced as reactive compliant layers, their applicability extends beyond fine-pitch high-density bumped interconnections and they are also applicable as die-attach layers for high-power applications. Consequently, an understanding of foam densification and stress-buffering on large-area surfaces as well as fabrication of foams with large bondline thicknesses is required to compete with standard die-attach technologies.

6.2 Conclusions

This thesis work was conducted to demonstrate pitch scalability to 20 μ m pitch, assembly throughput and thermomechanical reliability of solid-state copper interconnections to meet the needs of emerging high-performance computing applications. The fundamental focus was on designing Cu-based interconnection systems that prevents copper oxidation, improves interfacial reactivity of copper while also enhancing the compliance of interconnections. This thesis addressed these two challenges: high-throughput assembly and high thermomechanical reliability by two different innovative approaches:

In the first approach, ultra-thin Au-based metallic thin films were introduced to circumvent copper oxidation to maintain enhanced reactivity of the bonding interfaces. The Au bonding layers provided soft, oxide-free bonding interfaces, enabling assembly at lower temperatures and in air. Low-cost fly-cut planarization of non-coplanar bumps was employed to lower bonding pressures and improve high strength interfaces (>190MPa). In the second approach, a low-modulus Cu cap made of nanofoam was proposed and developed on bulk Cu micro-bumps that acted as a reactive and compliant layer to enable assembly at low pressures (<40MPa) and at low temperatures (<250°C) respectively. Nanocopper foams have a 20-40GPa modulus compared to 120GPa for bulk Cu. During assembly, these reactive nanocopper foams densified to achieve bulk Cu-like properties, enabling high-performance joints. Patterned Cu pillar interconnections with nano-Cu caps were demonstrated through co-electrodeposition and dealloying of Cu-Zn layers with a preliminary shear strength of 22MPa.

In both approaches, the final joints are composed mostly of Cu, a stiff interconnection material, to achieve thermomechanical reliability with particular concern

for shear failures in the low-K dielectric layers on-chip. To address this challenge, the use of pre-applied underfill materials and a high-speed 2-step assembly processes was proposed and developed to form reliable, low-stress joints. On utilizing a 2-step assembly approach, involving a fast TC-NCP process followed by a batch anneal step ($<250^{\circ}\text{C}$), high throughput assembly was demonstrated with bonding process time under 3sec. Interconnections formed by both approaches successfully passed preliminary thermal ageing tests at 250°C . Cu-EPAG interconnections showed excellent electromigration resistance at $3 \times 10^5 \text{ A/cm}^2$, passing 1,000 hours without failures while also resulting in good thermomechanical reliability with low-CTE glass substrates under thermal shock testing for 1,000 cycles. The failure modes were attributed to bonded interfaces under accumulated fatigue.

6.3 Technical and Scientific Contributions

This research advances fundamental material science to manufacture reliable, high-throughput and fine-pitch copper interconnections and assembly for high current density applications as follows:

- Design, fabrication and demonstration of cost-effective solid-state interconnection and assembly materials and processes to achieve high power handling, high-throughput assembly, and thermomechanical reliability.
- First approach proposes innovative bimetallic surface coatings that form soft reactive interfaces for bonding. The fundamentals of plastic deformation as well as reaction kinetics at this interface is studied to improve assembly throughput. Furthermore, high throughput planarization process is introduced to prepare planar Cu surfaces to readily bond to each other with minimal surface asperities.

- Second approach proposes synthesis of nanocopper interconnection and assembly with very low modulus and with very high reactivity to achieve bulk-Cu like power handling properties with high throughput and high reliability. The nano-Cu interconnections are explored and developed with nano-foams by co-electrodeposition and dealloying, Fundamental studies include: 1) effect of nanofoam morphology on physical properties, before and after assembly to provide guidelines for material design for power handling, high-throughput assembly and reliability; 2) kinetics of sintering of nanocopper foam as compared to nanoparticle systems; and 3) understanding of plastic deformation in nanocopper foam interconnections.

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