RECONFIGURABLE AMPLIFIERS AND CIRCUIT COMPONENTS FOR BUILT-IN-SELF TESTING AND SELF-HEALING IN SIGE BICMOS TECHNOLOGY

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RECONFIGURABLE AMPLIFIERS AND CIRCUIT COMPONENTS FOR BUILT-IN-SELF TESTING AND SELF-HEALING IN SIGE BICMOS TECHNOLOGY

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To my most cherished teacher,

Mr. Oswin Martineau,

"nothing attempted is nothing gained."

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GLOSSARY

LNA low noise amplifier

BIST built-in-self-test

DUT device under test

PVT process, voltage, and temperature

SMU source measure unit

RF radio frequency

CMOS complementary metal-oxide-semiconductor

FET field-effect transistor

$\mathbf{f_T}$ unity gain frequency

$\mathbf{f_{max}}$ maximum oscillation frequency

DAC digital to analog converter

op-amp operational amplifier

BJT bipolar junction transistor

SiGe HBT silicon-germanium heterojunction bipolar transistor

BiCMOS bipolar-complementary metal-oxide-semiconductor

NF noise figure

$\mathbf{NF_{min}}$ minimum noise figure

ADC analog-to-digital converter

DIP dual-in-line package

I/O input-output

IC integrated circuit

$\mathbf{I_C}$ collector current

$\mathbf{I_B}$ base current

$\mathbf{g_m}$ small-signal gain

$\mathbf{J_C}$ collector current density

$R_{S,opt}$ optimal noise resistance

UWB ultra-wideband

pFET p-channel field-effect transistor

nFET n-channel field-effect transistor

GaN gallium nitride

GaAs gallium arsenide

InP indium phosphide

SoC system on chip

CE common emitter

MIM metal-insulator-metal – A type of on-chip capacitor.

PNA power network analyzer

TID total ionizing dose

DD displacement damage

SEE single event effects

BGR bandgap reference

VCO voltage-controlled oscillator

RHBP radiation-hardening-by-process

RHBD radiation-hardening-by-design

OIP3 output third-order intercept point

ALL amplitude-locked loop

IRR image rejection ratio

LO local oscillator

CPW coplanar waveguide

MLN microstrip line

TEM transverse electric magnetic

quasi-TEM quasi-transverse electric magnetic

MMIC monolithic-microwave integrated circuit

PA power amplifier

SUMMARY

The design of reconfigurable microwave and millimeter-wave circuit components and on-chip testing circuitry are demonstrated. These components are designed to enable the mitigation of process faults, aging, radiation effects, and other mechanisms that lead to performance degradation in circuits and systems. The presented work is primarily based on silicon-germanium heterojunction bipolar transistors (SiGe HBTs) in bipolar-complementary metal-oxide-semiconductor (BiCMOS) technology and harnesses the inherent resilience of SiGe to mechanisms that degrade transistor performance. However, complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs) are also used in limited applications, such as in the design of switches, operational amplifiers (op-amps), and digital to analog converter s (DACs). Individual circuit blocks and circuit systems are characterized with the aim of evaluating their performance under nominal conditions as well as in the context of extreme environments and other deleterious phenomena. The following is a summary of the contributions of this research:

1. Reconfigurable SiGe low noise amplifiers (LNAs) with integrated tuning knobs for built-in-self-test (BIST) and self-healing applications. [35, 36, 37].

2. Investigation of total-dose radiation effects on SiGe reconfigurable LNAs [32].

3. Design and characterization of a self-healing wideband receiver.

4. Investigation of total-dose radiation effects on self-healing wideband receiver.

5. Design of device characterization circuits for self-healing applications [34, 36].

6. Tunable transmission lines and a wideband millimeter-wave balun [31].

CHAPTER I

INTRODUCTION

Perhaps the most seminal moment in the history of semiconductors, after the invention of the transistor itself in 1947, was the advent of integrated circuit (IC) technology in the late 1950s, which made it possible for a number of transistors and associated components to be fabricated on the same silicon die. Early on, it was recognized that collector current (I_C) technology could realize the dream of system on chip (SoC) solutions that would be a game changer in the electronics industry. However, fabrication process problems that had a potential to negatively impact the first ICs with unacceptability low yield were a concern. Fortunately, IC fabrication technology grew rapidly, and it became possible to reliably build integrated systems with tens of transistors on a single die with relatively high yield approaching 99% [80]. The fabrication techniques developed in these early years paved the way for the increased scaling and integration along the trajectory described by Moore's Law in which, the number of transistors in ICs doubles approximately every 18 months. This trend has shown little sign of abating; at the time of writing, it is possible to fabricate in excess of 1 billion transistors on a single memory chip with aggressive scaling down of the transistor's size by reducing its length, commonly known as the transistor's "feature" size. The most advanced transistor technologies have feature sizes less than 70 nm [53]. While progress in the microelectronics industry has been astounding, the aggressive scaling of transistor feature sizes below the sub micrometer level has proven to be a double edged sword; scaling has resulted in increased integration and performance but simultaneously has exacerbated the conditions that adversely affect yield as a result of process variation.

While the first transistor was fabricated from a germanium crystal in 1947, the main semiconductor technology that has benefited from scaling is silicon based CMOS and BiCMOS technologies. The steady progression of silicon IC technology facilitates the use of silicon in advanced microwave and millimeter-wave applications that previously were only the domain of III-V technologies such as gallium arsenide (GaAs), and gallium nitride (GaN), and indium phosphide (InP). The most advanced SiGe HBTs demonstrate unity gain frequency (f_T) values in excess of 300 GHz at 300 K at the 90 nm node [16]. However, as previously mentioned, aggressive device scaling has exacerbated within-die and die-to-die process variations. These variations are often caused by imperfections in the IC manufacturing processes that result in active- and passive-device characteristics varying over a normal distribution, inevitably exacerbating process, voltage, and temperature (PVT) variations and other deleterious phenomena such as aging and some types of radiation effects [7, 58]. For example, the statistical distribution of current gain (β) for two SiGe HBT technology nodes is shown in Figure 1. It shows that the spread in β for the 0.12 μm node is much wider than the 0.25 μm node, meaning that the worst performing transistors (in terms of β value) at the 0.25 μm node are better than the typical spread in β at the 0.12 μm node. Traditionally, circuit designers have factored in parameter variation and environmental effects into their overall design methodology. For example, the use symmetrical layouts and placement of identical dummy devices adjacent to the active components are used to reduce the impact of variation on sensitive circuit components [29]. Similarly in the digital circuit designers have applied a variety of methods, including redundancy and hardening techniques to mitigate the effects of variation and environmental effects such as radiation [30, 42, 70]. While these techniques are somewhat effective in mitigating for PVT variations and environmentally-driven degradation, they add significant overhead in the form of increased complexity, circuit area, and power consumption.

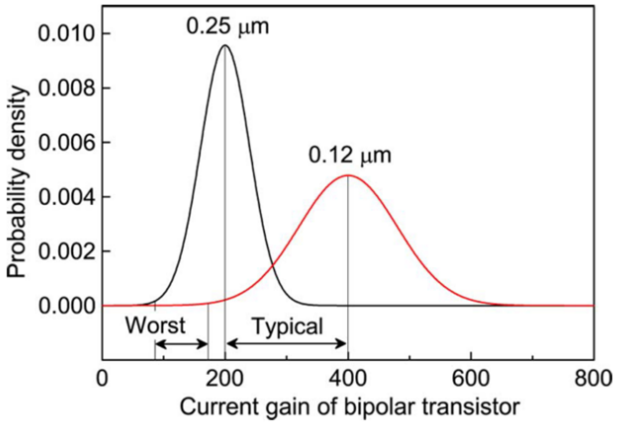


Figure 1: The typical statistical distributions of the current gain (β) of SiGe HBTs in two different technology nodes are compared. The variance of the distribution in 0.12 μm technology is larger than that in the 0.25 μm process (after [66]).

In addition to process-induced variations, other factors can affect circuit performance, such as temperature and radiation. Environments that inherently demonstrate extremes in temperature and radiation, such as low earth orbit and space can be detrimental to circuit performance and even lead to catastrophic failures. The extreme environment of space is subject to temperatures that can vary widely. For instance, the temperatures between the dark and light sides of the Moon can vary from $-180°$C to $+120°$C respectively. Also, space is awash with high energy particles including protons, heavy-ions, and photons, all of which can damage semiconductor transistors in a variety of ways. There are three main classifications of radiation-induced damage to semiconductor transistors: the first is total ionizing dose (TID), that results from damage to the semiconductor-dielectric interface when incident high energy particles produce interface traps and incomplete bonding at surfaces. As a consequence, transistors exhibit increased leakage currents and shifts in quiescent operating points that degrade performance; the second mechanism is displacement damage (DD), in which the incident particles carry enough energy to knock out or displace individual atoms from the semiconductor lattice, resulting in defect states; finally, there are single event effects (SEE), in which high energy particles induce

electron-hole pairs within the semiconductor. These electrons and holes are swept into the terminals of the device by the transistor's built-in electric fields producing, at the circuit level, brief current or voltage transients that can degrade circuit performance. This mechanism affects the performance of digital circuit blocks producing bit errors and corrupts digital information. These effects are transient in nature and are generally described as single event upsets (SEU) [16]. Conventional mitigation strategies for radiation involve protecting sensitive electronics from radiation exposure by using specially designed, shielded and temperature-controlled "warm-boxes" such as those used in NASA's Mars Rovers, illustrated in Figure 2. However, these warm-boxes are bulky, expensive, and add significantly to power consumption. Techniques for hardening of the electronics itself have been increasing in popularity, with the hope that they will eventually obviate the need for these warm-boxes.

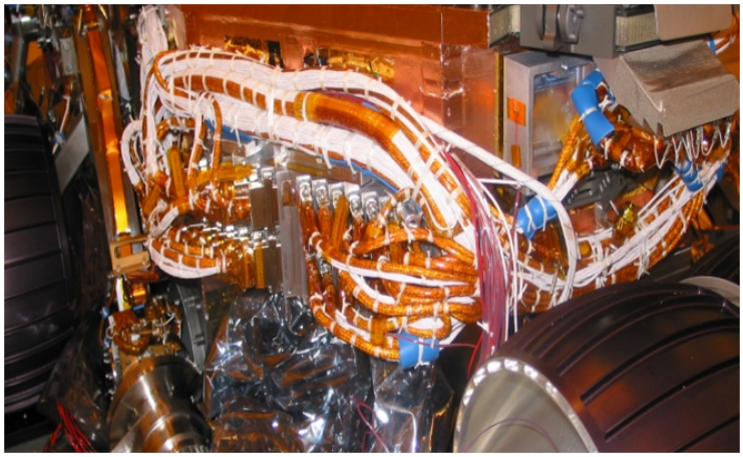


Figure 2: A warm-box typically used in NASA's Mars Rovers.

Approaches to radiation hardening of the circuits themselves fall into two broad categories: 1) Process modifications known as radiation-hardening-by-process (RHBP), and 2) device and/or circuit modifications known as radiation-hardening-by-design (RHBD). It is well established that SiGe HBTs have a tolerance to TID exposure to multi-Mrad levels [17, 74, 78, 79]. SiGe is thus an excellent choice for space-based electronics. Unfortunately, SiGe RF circuits are still susceptible to TID and very

little work has been presented to date on the TID response of SiGe RF circuits. Previous studies on SiGe RF and analog circuits have shown performance degradation as a result of proton fluences in excess of 1.0 x 10^{12} p/cm^2. For example, modest degradation in the output voltage of a bandgap reference (BGR) circuit, as well as an increase in the phase noise of a cross-coupled voltage-controlled oscillator (VCO) has been observed [17]. It is highly desirable for space-based RF SiGe circuits to be capable of autonomously recovering lost RF performance as a result of radiation exposure by employing sensing, feedback mechanisms, and tunable elements to compensate for damage. This concept is not meant to repair the damage to the devices themselves but rather to "tune" circuit performance by adjusting the performance of circuit blocks in the event of non-catastrophic damage at the device level, thereby returning the entire irradiated RF system back into system specification.

These emerging strategies are known as BIST and "self-healing" techniques. These methods incorporate tunable or reconfigurable elements into circuit designs so that parameters can be adjusted *in situ* to regain lost performance as a consequence of non-catastrophic damage. Key to the operation of BIST and self-healing circuits are feedback loops with the ability to assess circuit performance, post fabrication, and respond to degradation by adjusting predefined tuning knobs [9, 28, 39, 49, 55, 69]. A block diagram of a typical self-healing circuit is shown in Figure 3. It shows the typical interconnections between the RF chain, digital circuitry, and tuning knobs, as well as the inclusion of integrated test signal sources.

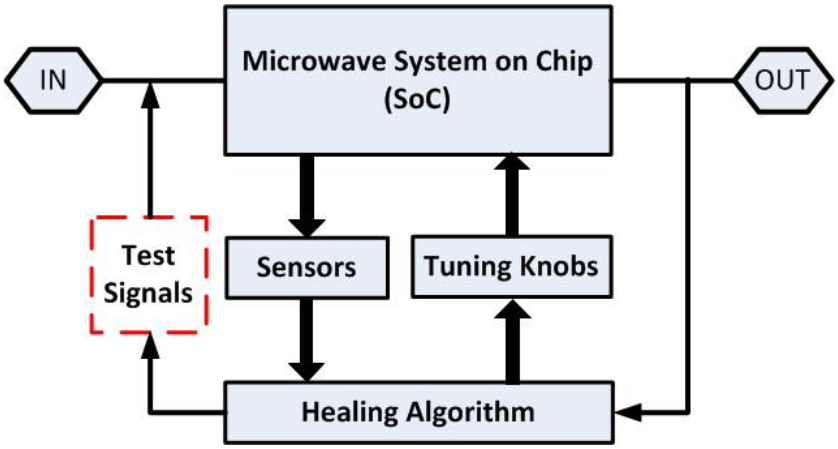


Figure 3: Block diagram of a general self-healing system.

These emerging BIST and self-healing systems require the development of adjustable active and passive circuit blocks to enable the tuning of system performance. As a result, there has been much interest in developing tunable active and passive circuits such as amplifiers, mixers, signal sources, transmission lines, inductors, and capacitors. The body of work presented in this thesis brings these elements together to address the needs of BIST and self-healing systems.

Because most of the work presented was designed in SiGe BiCMOS technology, it is instructive to look into the basic physics governing the operation of SiGe HBTs to shed light on the ways in which extremes in temperature and radiation can impact their performance.

1.1 Silicon Germanium HBT BiCMOS Technology

SiGe BiCMOS technology platforms have garnered much interest within the radio frequency (RF), microwave, millimeter-wave, and mixed-signal communities. This is due to the steadily improving performance of SiGe BiCMOS technology over the years and its manufacturing compatibility with existing CMOS technologies that are highly mature and popular in the semiconductor electronics industry. In particular, SiGe devices are exhibiting peak f_T and peak maximum oscillation frequency (f_{max})

values approaching 500 GHz. The performance of SiGe is approaching that of gallium-arsenide and gallium-nitride semiconductor devices, normally reserved for high performance and high frequency circuits with demanding power and efficiency specifications, while maintaining the cost effectiveness of CMOS technologies [15, 18]. Shown in Figure 4 is an image of the structure of a 3^{rd} generation SiGe HBT device.

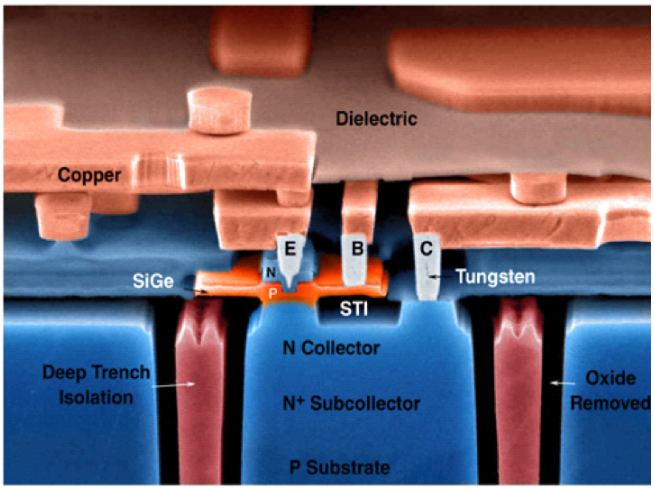


Figure 4: Structure of 3^{rd} generation SiGe HBT (courtesy of IBM).

The impressive performance of SiGe platforms is due to band-gap engineering, in which germanium is incorporated in the base of a standard silicon (Si) bipolar junction transistor (BJT). SiGe devices enjoy improvements in current gain (β), Early voltage (V_A), and f_T over their standard Si BJT counterparts. The ease of integration of germanium in the base of standard Si processes makes it possible to take advantage of the superior performance of SiGe, while leveraging the cost and integration advantages of the best-of-breed CMOS technologies for potent use in mixed-signal application domains. SiGe band-gap engineering is achieved by adding a layer of compositionally graded SiGe alloy in the boron-doped epitaxial layer. The doping and Ge profile as well as the energy band diagram for a typical SiGe HBT is shown in Figure 5 . As seen in Figure 5 (a), there is a position dependent trapezoidal Ge profile in the base. This has the effect of narrowing the bandgap in the base region of the transistor. This

concept is further illustrated in Figure 5 (b), which compares the band diagram of a SiGe HBT and conventional silicon BJT. The valence band of the SiGe HBT in the base region narrows resulting in a smaller bandgap than conventional silicon. Bandgap narrowing, among other things, decreases the transit time of minority carries across the base region and improves the performance of the transistor [6]. The germanium layer is usually grown using epitaxial ultra-high vacuum/chemical vapor deposition (UHV/CVD) techniques discussed in [41]. This step is an easy add-on to the standard Si CMOS process flow, and does not affect the HBT performance and CMOS yield.

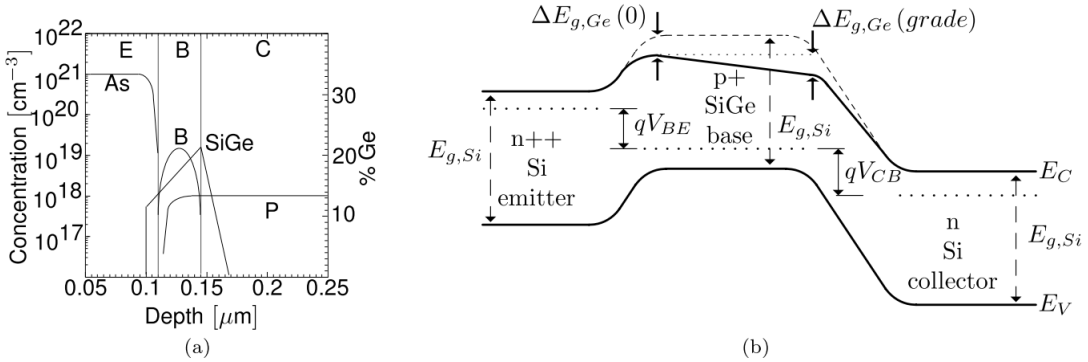


Figure 5: (a) A typical doping and Ge profile for a SiGe HBT (b) Energy band diagram for a SiGe HBT (solid lines) and silicon BJT (dashed lines) along with the bandgap narrowing effect (after [6]).

Further analysis shows that two crucial metrics of transistor RF performance, f_T and f_{max}, are enhanced through reduction of the base transit time (τ_b) through the addition of Ge in the base. Assuming a strong Ge grading scenario, which is true for the current generation of HBT technologies, the SiGe base transit time $\tau_{b,SiGe}$ enhancement is inversely proportional to $\Delta E_{g,Ge}(grade)$

$$\tau_{b,SiGe} \approx \frac{W_b^2}{2D_{nb}} \frac{kT}{\Delta E_{g,Ge}(grade)}, \tag{1}$$

where W_b is the base width and D_{nb} is the minority electron diffusivity. Additionally, the emitter charge storage delay, τ_e, is inversely proportional to the current gain, β.

As a result, the overall transit time is reduced and the maximum f_T increases and is given by

$$f_T = \frac{1}{2\pi}\left[\frac{1}{g_m}(C_{te} + C_{tc}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{tc}\right], \tag{2}$$

where g_m is the transconductance of the SiGe transistor, $C_{te} + C_{tc}$ are the depletion capacitances, W_{CB} is the width of the collector-base junction space charge region, v_{sat} is saturation velocity, and r_c is the small-signal collector resistance. The maximum oscillation frequency (f_{max}) is inversely proportional to f_T, and so follows the same improvement trends as the other RF metrics as a result of the addition of Ge. The f_{max} of a SiGe transistor is given by

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{bc} r_b}}, \tag{3}$$

where C_{bc} is the collector base capacitance and r_b is the intrinsic base resistance. Finally, by adjusting the Ge grading, a higher base doping can be used while still maintaining a high β, yielding a lower base resistance and improved noise performance. This is a marked difference from BJT transistors in which base resistance and β are coupled, limiting the ability of designers to maximize RF performance. For this and the previously mentioned reasons, SiGe technology is emerging as the semiconductor technology of choice for highly integratable, low cost, and high performance electronics.

1.1.1 Temperature and Radiation Effects in SiGe Technology

In traditional CMOS processes, extreme temperature fluctuations, such as those experienced in space, can be detrimental to circuit performance. However, because the SiGe HBT is a minority carrier device, the band edge changes induced by the germanium profile of SiGe produces thermally activated effects beneficial to device performance. The DC current gain (β_{DC}) for a SiGe HBT can be expressed in terms

of the current gain of a Si BJT ($\beta_{DC,Si}$) and other important process characteristics such as the bandgap energy, E_g and the germanium grade, Ge(grade) in equation 4

$$\beta_{DC} \approx \beta_{DC,Si} \left(\tilde{\gamma}\tilde{\eta} \frac{\Delta E_{g,Ge}(grade)}{kT} e^{\Delta E_{g,app}/kT} e^{\Delta E_g(0)/kT} \right). \quad (4)$$

The most important aspect of this equation with regard to temperature effects are the exponentially dependent E/kt terms. These thermally activated terms are inversely proportional to temperature, resulting in an improvement in current gain with a reduction in temperature [6].

Furthermore, it has long been appreciated from the basic physics of the SiGe HBT that cooling favorably impacts all device metrics from a circuit design perspective including RF metrics such as g_m, f_T, f_{max}, and noise figure (NF). SiGe is therefore an attractive technology that can then be used to offset the problems associated with cooling of homojunction bipolar transistors such as bandgap-narrowing induced gain degradation, base freezout, and carrier diffusivity degradation. Moreover, the SiGe HBT represents a transistor that naturally benefits from cooling [16]. At high temperatures, SiGe HBT performance degrades. However, the extent of degradation is not as dramatic as might be expected. SiGe HBTs exhibit a current gain above 100 and f_T values above 75 GHz at 300° C [16]; these are more than adequate numbers for respectable circuit operation under such extreme temperatures.

Unlike the favorable performance of SiGe in response to low temperatures, radiation effects generally lead to degradation of SiGe transistor performance. However, it is well established that SiGe HBTs have a very favorable tolerance to TID exposure to multi-Mrad levels [16, 17, 18]. The main form of TID damage that SiGe HBTs are susceptible to is current leakage, which is shown in the gummel plot in Figure 6. It shows that the SiGe device exhibits base current leakage particularly for proton fluences in excess of 7 x10^{12} p/cm^2. The base current leakage is minimal and leads

to small degradation in device performance. However, these small changes in performance may be problematic for certain applications. Although radiation damage as a result of TID effects are minimal in SiGe HBTs, SiGe devices do not possess any inherent resilience to SEE; in fact, heavy ions can produce bit upsets in SiGe digital circuits. This is because SiGe technology incorporates a reversed biased $n^+ - p^-$ substrate junction that is prone to absorbing the deposited electric charge of an ion strike [16].

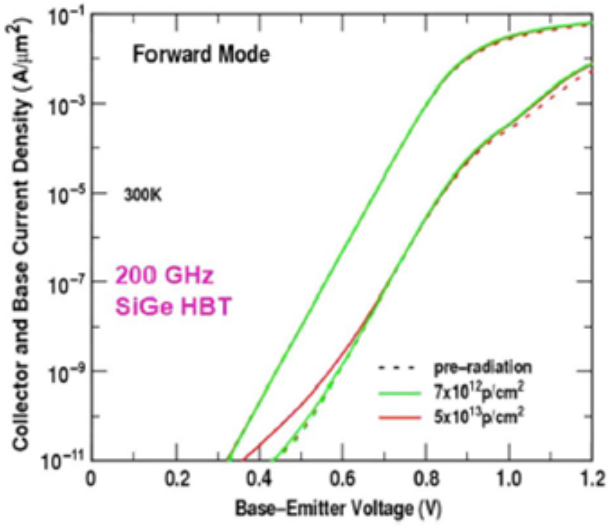


Figure 6: Forward Gummel characteristics of a third-generation SiGe HBT before and after exposure to multi-Mrad total dose (after [16]).

1.2 Research Objectives

The main objective of this research is to leverage the potential of SiGe BiCMOS technologies ti advance the state of the art in microwave and millimeter-wave and monolithic-microwave integrated circuits (MMICs). In particular, the proposed work seeks to leverage silicon-germanium's excellent manufacturing yield as well as temperature and radiation tolerance towards the mitigation of performance degradation as a result of these effects. While work has been done on studying the efficacy of tunable circuits towards the improvement of yield, not enough has been done to explore the

effects of these circuit design techniques when circuits and systems are operating in harsh environments with extreme temperatures and radiation.

In addition, radiation effects in SiGe BiCMOS circuits has primarily focused on analog and digital applications. Much of the high-frequency work in this field has focused on the validation of TID performance degradation as a result of damage to transistor devices. As radiation effects on high-frequency circuits becomes increasingly critical in airborne and space-based systems, such as integrated phased-array radar transmit/receiver (T/R) modules [77], new techniques for mitigating radiation damage are growing in importance.

A major contribution of this work is the design and testing of on chip characterization circuits. These circuits are designed to test SiGe HBT transistors *in situ* and gather vital DC performance information that can be used to adjust the biasing of other circuit blocks on the same die. In this way, it becomes possible to test a separate test transistor, determine its performance in light of changes in PVT or radiation, and then use that information to bias RF circuitry on the same die to regain lost performance. The main advantage of this approach is that it is non-invasive to the sensitive RF electronics blocks and does not add parasitic effects that degrade RF performance.

Additionally, work is presented that explores various techniques for the development of tunable circuits intended for use in BIST and self-healing healing systems. These approaches are investigated via the design of LNAs on chip sensing circuits and tunable transmission lines. Experimental results are presented to show the effectiveness of these techniques in mitigating performance loss as a result of process variation and radiation effects.

Finally, tunable and wideband passives, namely tunable microstrip lines (MLNs) and a wideband millimeter-wave balun are presented. Tunable passive components are key to enabling reconfigurable high-frequency systems.

CHAPTER II

CIRCUIT COMPONENTS FOR SELF-HEALING AND BIST APPLICATIONS

2.1 Introduction

As discussed in the previous section, circuit designers have incorporated reconfigurable elements into their designs so that circuit parameters can be adjusted *in situ* to regain lost performance as a result of non-catastrophic damage. The hallmark of these BIST and "self-healing" techniques is that they enable systems to have the on-die ability to measure their own performance and respond to degradation by tuning predefined knobs according to various algorithms [8, 28, 39].

However, circuits and systems with BIST and self-healing capability must not only incorporate tuning knobs so that the performance of individual circuit blocks can be tuned, but they also require built-in sensors to monitor important metrics. For radio frequency (RF), microwave, and millimeter-wave systems, these metrics include gain, linearity, and NF. Some BIST approaches attempt to directly measure these metrics by incorporating elaborate feedback mechanisms within the system so that the output signal can be analyzed using on-chip analog-to-digital converters (ADCs) [81]. Other strategies attempt to indirectly measure these characteristics by measuring other parameters that impact RF performance. For example, the gain of an LNA can be inferred from the power recorded by a peak detector at the output of the LNA [19, 39, 65].

The circuits presented in this section are the basic building blocks for BIST and "self-healing" systems. They include source measure unit s (SMUs) designed to perform on-chip testing of SiGe HBTs transistors and are geared towards BIST and

self-healing systems that employ the indirect measurement approach for sensing RF performance [37]. The circuits are designed to source a user-specified voltage at one node of a SiGe HBT device and simultaneously monitor the induced current that flows through the same node. This functionality enables these circuits to DC bias a test SiGe HBT device, and by using multiple SMU circuits, it is possible to to extract DC characteristics of the SiGe HBT device under test (DUT) such as, I_C, base current (I_B), β, and small-signal gain (g_m).

Tunable transmission lines are also presented. These lines are based on the MLN architecture and include switching mechanisms to change the voltage potential of the MLN backplane. Switching the voltage potential of the backplane changes key aspects of the transmission line that affect its performance such as the characteristic impedance (Z_0), the electrical length (Φ), and phase between the two ports. These changes make tunable transmission lines suitable for designing tunable matching networks and other tunable microwave elements.

Finally, an asymmetrical broadside coupled wideband balun is presented. Baluns are important components in MMICs because at microwave and millimeter-wave frequencies, it is more desirable to design balanced circuits than it is to design single-ended circuits. This is because at high frequencies, parasitic effects increase, degrading performance. Balanced circuit topologies are robust to these high frequency parasitic effects. However, most systems operate within a single-ended context. Baluns convert unbalanced signals into balanced signals and are an important component in microwave and millimeter-wave systems.

2.2 SiGe HBT Collector Current Source Measure Unit (SMU)

2.2.1 Circuit Analysis and Design

The SMU circuit is shown in Figure 7. Stage 1 consists of an op-amp (OP_1) in negative feedback configuration with device Q_2 at the output. This configuration,

known as a current regulator, allows the input voltage, V_{set}, applied to the positive terminal of (OP_1) to be mirrored onto the positive terminal of the sensing resistor R_S. The collector current of Q_1 induces a voltage across R_S that is proportional to the current. The voltage, V_{set} biases the collector (C) node of the DUT, Q_1.The induced current at the collector (C) node of the SiGe HBT DUT is supplied by transistor, Q_2.

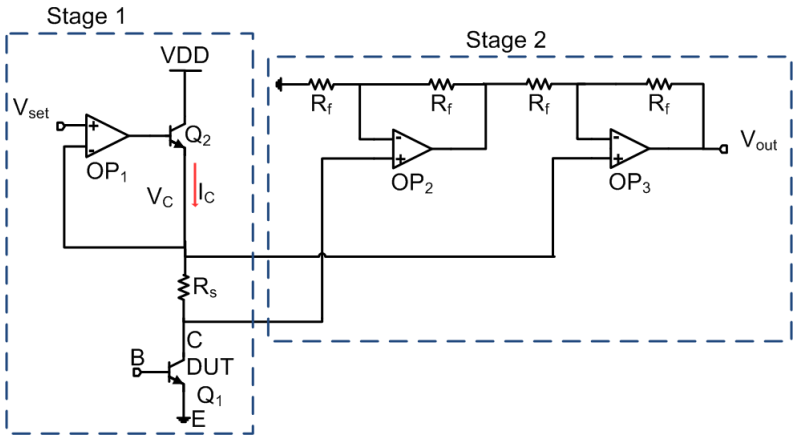


Figure 7: SMU circuit attached to the collector node of the SiGe HBT DUT.

The voltage across R_S is measured by stage 2, which is an instrumentation amplifier comprising of OP_2, OP_3, and four feedback resistors of identical value, R_f. The voltage across R_S is amplified by the instrumentation amplifier and represented by the voltage, V_{out}. The gain of the instrumentation amplifier is given by

$$Gain = 1 + R_f/R_f = 2, \tag{5}$$

where R_f is the feedback resistor used in the instrumentation amplifier. Because all of the feedback resistors have a value of R_f, the gain of the instrumentation amplifier is 2 V/V. The current, I_C at the collector node of the DUT is represented by an output voltage. The collector current I_C is given by

$$I_C = 2V_{out}R_s, \tag{6}$$

where the gain of the instrumentation amplifier (2 V/V) is given by equation (5), R_S,

is the sensing resistance, and V_{OUT} is the instrumentation amplifier output voltage.

2.2.2 Measured Results

To measure the effects of process variation, the collector current I_C of a test device was measured with the on-chip SMU and an Agilent 4155 Semiconductor Parameter Analyzer. In addition, the circuit was simulated at nominal, fast and slow process corners. The measured and simulated I_C at fast and slow corner simulation vs. base voltage, Vb are shown in Figure 8.

The plot shows that the calculated collector current from the SMU agrees closely with the simulated and Agilent 4155 results. However, at low Vb voltages, the SMU measurement diverges from both the simulated and measured results. This is due to the limited range of of the instrumentation amplifier's sensitivity to voltage changes across R_S.

Although the SMU measures I_C of the SiGe HBT DUT with reasonable accuracy, improvements need to be made, especially with its accuracy in measuring low collector current values. This, as well as other improvements is the subject of the subsequent SMU revision.

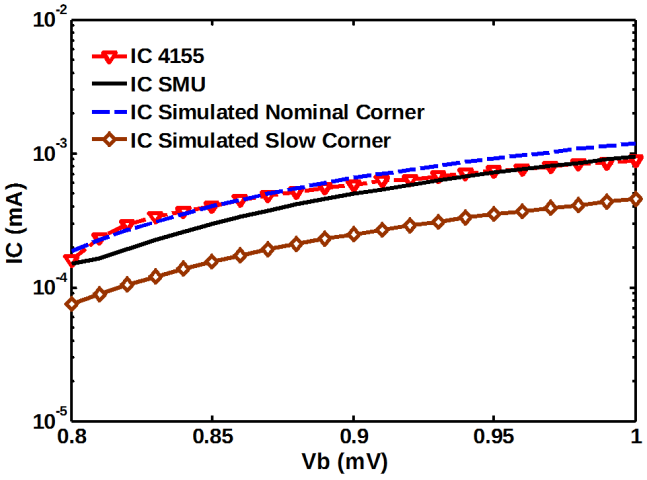


Figure 8: Schematic of SMU attached to the collector node of the SiGe HBT DUT.

2.3 On-chip SiGe Current Gain Characterization Circuit

Building upon the previous design, the SMU was redesigned to measure the current gain (β) of a test SiGe HBT DUT that is representative of the transistors used in RF circuit blocks on the same die. The conceptual application of the SMU in a wider RF system is shown in Figure 9. The circuit reliably sources voltages at the collector and base nodes of the DUT and then measures the currents induced at those respective nodes. These sourcing and measuring features inspire the description of the circuit as a SMU, such as that utilized in precision semiconductor parameter analyzers [1]. The SMU is also designed with temperature compensation so that it can accurately measure the current gain of the DUT over wide temperature ranges.

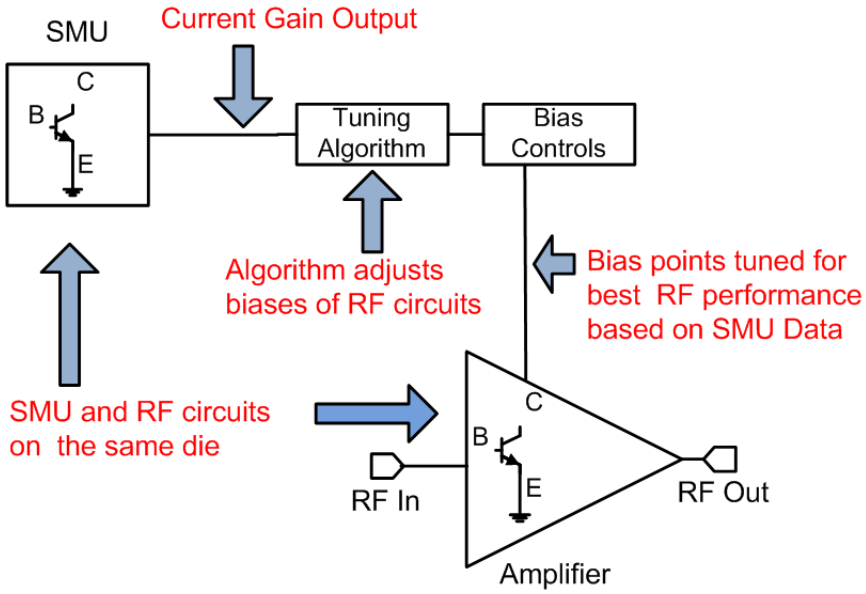


Figure 9: Conceptual diagram of SMU and the RF circuit on the same die.

2.3.1 Source Measure Unit Design

The SMU circuit presented in this work is an extension of the circuit described in [37]. The first two stages of this modified SMU circuit are illustrated in Figure 10. The first stage is a voltage regulator, in which the op-amp, OP_1, is placed in negative feedback around a common drain, voltage-follower, M_1. The op-amp, OP_1, ensures that the

voltage at the collector (C) terminal of the DUT, Q_1, is equal to the test voltage, V_C, which is set at the positive terminal of OP_1. The induced I_C current flowing through the collector is supplied by M_1 and mirrored into the second stage by the cascode current mirror comprised of devices M_2-M_5. Stage 2 is a logarithmic amplifier and consists of an op-amp, OP_3, in negative feedback with a diode-connected SiGe HBT, Q_2, which is placed in the feedback loop. The resistor R_1, is used for stabilizing the circuit.

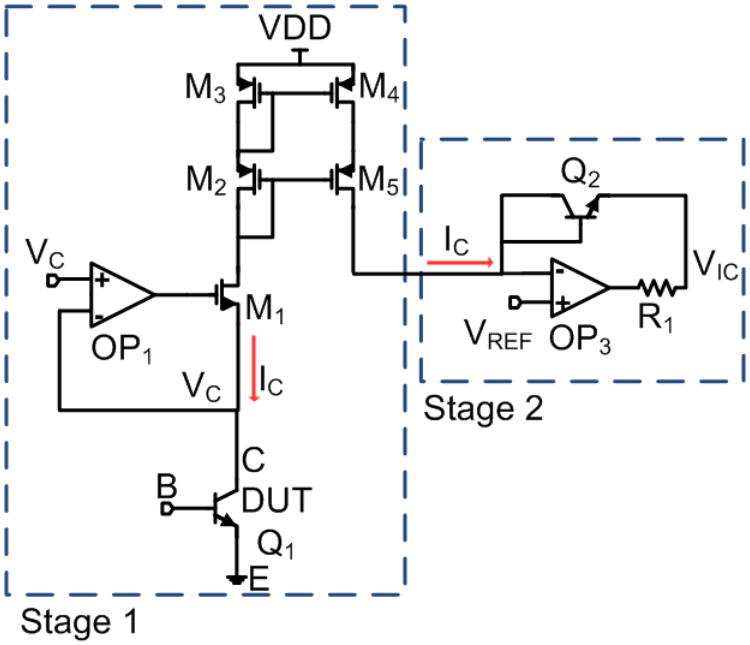


Figure 10: Voltage regulator and logarithmic amplifier stages of the SMU.

The architecture of Stage 2 utilizes the exponential property of the forward-biased, SiGe HBT, Q_2, and results in the output voltage, V_{IC}, being proportional to the natural logarithm of the input current I_C, as given by

$$V_{IC} = V_T \ln\left(\frac{I_C}{I_S}\right) + V_{REF}, \tag{7}$$

where I_C is the collector current through the DUT, I_S is the saturation current of Q_2, V_T is the thermal voltage of Q_2, and V_{REF} is an offset voltage applied to the op-amp because of its single-supply topology.

The full SMU circuit is shown in Figure 11. The DUT, Q_1, is biased using two identical copies of the circuit illustrated in Figure 10, and is connected in a fashion similar to that described in [75]. Half of the circuit biases the collector (C) node and the other biases the base (B) node. The collector and base voltages can be set by V_C and V_B, respectively. The logarithmic voltage outputs of op-amps OP_3 and OP_4 are fed into a difference amplifier formed by the op-amp, OP_5 and feedback resistors $R_{2(Temp)}$ and R_F.

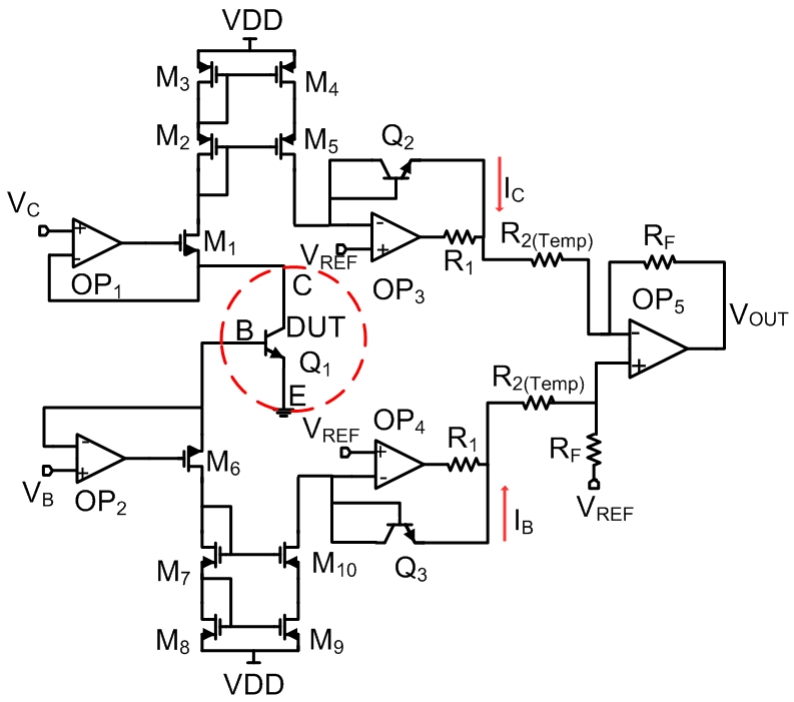


Figure 11: Schematic of complete SMU circuit.

The current gain of Q_1 is calculated from V_{OUT} by the difference of the log outputs of OP_3 and OP_4. Utilizing equation (7), the output voltage, V_{OUT} is given by

$$V_{OUT} = V_T \frac{R_F}{R_{2(Temp)}} \left[\ln\left(\frac{I_C}{I_S}\right) - \ln\left(\frac{I_B}{I_S}\right) \right] + V_{REF}. \tag{8}$$

The saturation current, I_S, is eliminated by simplifying equation (8) to give

$$V_{OUT} = V_T \frac{R_F}{R_{2(Temp)}} \left[\ln \left(\frac{I_C}{I_B} \right) \right] + V_{REF}, \tag{9}$$

where I_C/I_B is the current gain, β of the DUT, Q_1. Rearranging equation (9) to solve for β, and converting from the natural logarithm to base 10 [61], gives

$$\beta = 10^{\left(\frac{\log e}{V_T} \cdot \frac{R_{2(Temp)}}{R_F} [V_{OUT} - V_{REF}] \right)}. \tag{10}$$

The final equation, derived from equation (10) for β using design values for $R_{2(Temp)}$, R_F, and V_{REF} is given by

$$\beta = 10^{1.55(V_{OUT} - 2.0)}. \tag{11}$$

Equation (10) shows that this circuit architecture exhibits inherent temperature compensation in two key ways: first, because both the collector and base currents are measured using the same logarithmic amplifier design and the current gain is measured from the difference of the logarithmic outputs, the saturation current, I_S, which is exponentially dependent on temperature, does not appear in equation (10). Second, compensation for the thermal voltage variations over temperature is provided by the two temperature-dependent resistors with a positive temperature coefficient, $R_{2(temp)}$, as described in [43, 75]. With these temperature compensation features, this SMU circuit can measure the current gain of the DUT across a wide temperature range without the accuracy of the SMU itself being negatively affected by temperature changes.

2.3.2 Measured Results

The SMU was implemented in a six-layer metal, 180 nm, 120 GHz, SiGe HBT BiCMOS platform. The chip area is approximately 1.3 x 0.9 mm^2, including pads. The SMU die was attached to a 28-pin dual-in-line package (DIP) and its input-output (I/O) pads bonded to the package to enable measurement using a DC-cryostat

Dewar. The DIP, with a magnified view of the SMU die micrograph ,is shown in Figure 12. The SMU operates from a 4.0 V supply and a V_{REF} of 2.0 V.

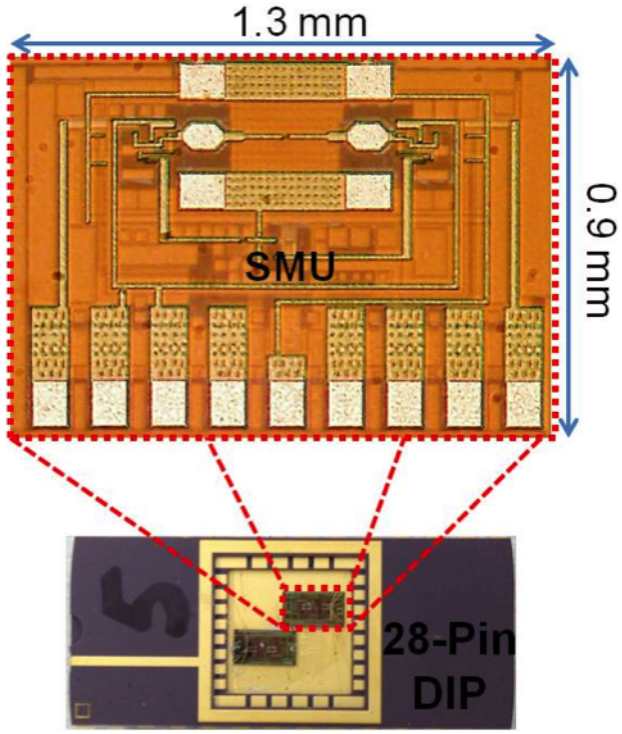


Figure 12: DIP with attached die and magnified micrograph of the SMU.

The measurement setup is illustrated in Figure 13. The DIP with attached SMU is placed in a DC-cryostat Dewar. The SMU DC biases are controlled using an Agilent 4156. The 4156 also has access directly to the device collector and base terminals, in this way the current gain of the device can be measured directly using the 4156. The SMU voltage, V_{out}, is measured using an external voltage meter. Both the Agilent 4156 and the voltage meter are controlled and monitored by a computer running MATLAB. During measurements, the collector and base voltages of the DUT are set by the user using the SMU voltages V_C and V_B, respectively, both ranging from $0 - 1.1$ V. To evaluate the performance of the SMU, the current gain calculated from equation (11) is compared with the current gain measured directly at the device terminals using an Agilent 4156 semiconductor parameter analyzer[1]. The SMU and 4156 were both controlled using MATLAB [54]. For both the 4156 and SMU

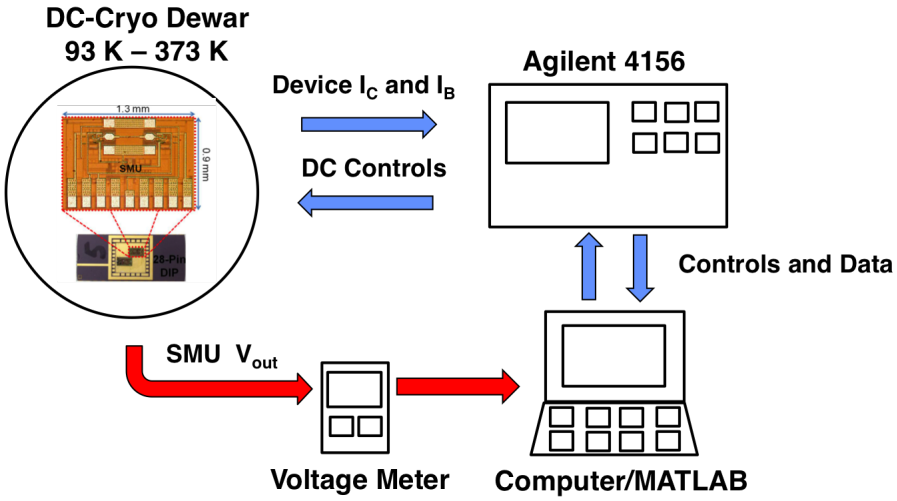


Figure 13: Schematic of measurement setup for the SMU including cryostat, 4156, and MATLAB control.

measurements, V_{BE} and V_{CE} of the DUT were swept to maintain a constant V_{CB} of 0 V. Measurements were conducted across temperatures ranging from -180 °C (93 K) to +120 °C (373 K).

The SMU current consumption over temperature is shown in Table 1. The current drawn from the 4.0 V supply ranges from 14.5 mA at 93 K to 9.1 mA at 373 K. The current is higher at low temperatures because the current gain of the devices within the SMU increases as temperature decreases. While this result means that the DC current consumption of the SMU is high especially when operated at low temperatures, because in self-healing systems, the duty cycle of the healing circuitry is very low, and thus power consumption is of secondary concern.

Table 1: SMU Current Consumption Over Temperature.

Temperature $[K]$	93	143	193	293	343	373
Supply Current $[mA]$	14.5	14.5	14.4	11.6	9.4	9.1

The room temperature (293 K) measurement of current gain vs. V_{BE} of the DUT using the SMU and the 4156 is shown in Figure 14. There is close agreement between

the SMU and 4156 measurements. However, the SMU current gain curve is offset to the right of the 4156 curve by a V_{BE} of approximately 0.1 V. This systematic offset is possibly due to the offset voltage of the op-amps used in the SMU. The current gain measured by the 4156 peaks at 98 for a V_{BE} of 0.75 V, while the SMU current gain measurement peaks at 104 for a V_{BE} of 0.8 V. Moreover, the shape of the SMU β output tracks the 4156 results closely for V_{BE} values ranging from 0.65 to 1.05 V. At $V_{BE} = 1.05\ V$, the headroom of the current mirrors supplying the DUT becomes too small to support current flow, and the data become inaccurate.

Operation at very low temperatures shows a similar agreement between the 4156 and the SMU. The current gain vs. V_{BE} of the DUT at 143 K is shown in Figure 15. The SMU and 4156 β curves agree closely, particularly the rising and failing edges of both current gain curves. However, the SMU curve rises and falls at a slightly steeper slope than the 4156. In addition, the measured β of the SMU peaks at 270 at $V_{BE} = 0.94\ V$, and the 4156 β measurement peaks at 226 at $V_{BE} = 0.97\ V$.

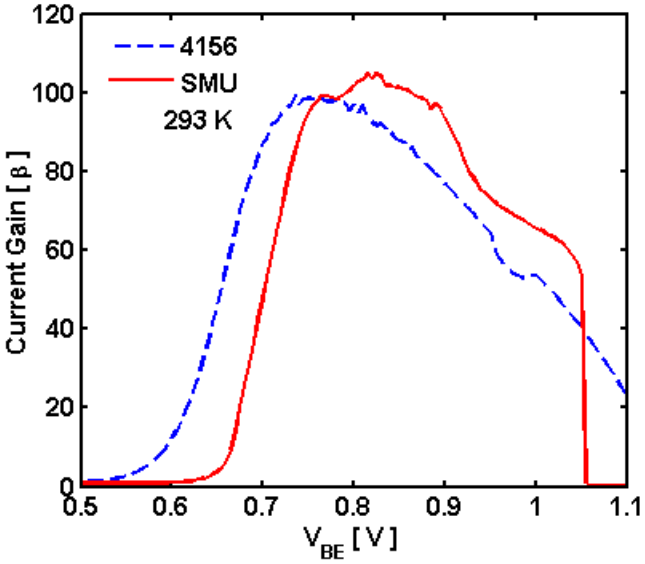


Figure 14: Current gain vs. V_{BE} at 293 K.

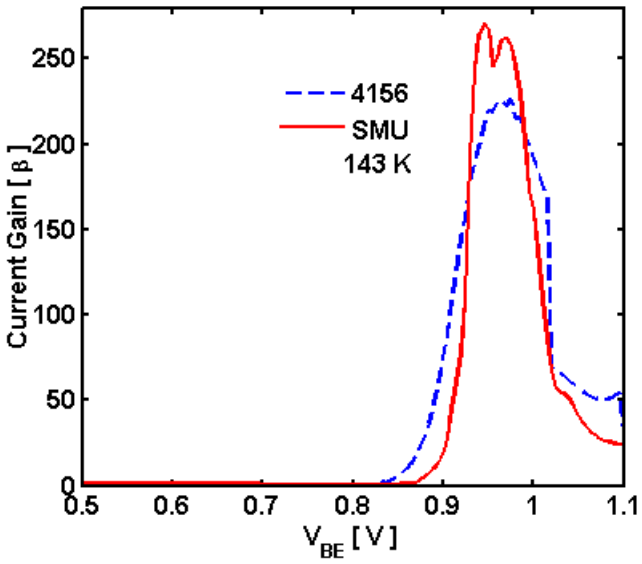


Figure 15: Current gain vs. V_{BE} at 143 K.

The SMU also exhibits good performance at elevated temperatures. The current gain vs. V_{BE} of the DUT at 343 K is shown in Figure 16. As expected, the current gain decreases with increasing temperature. The 4156 current gain measurement peaks at 80 at $V_{BE} = 0.7\ V$, while the SMU current gain peaks at 78 at $V_{BE} = 0.75\ V$. The shape of the SMU β output tracks the 4156 results closely for the V_{BE} range of 0.5 V to 1.05 V.

The measurement of peak current gain vs. temperature for both the SMU and 4156 is shown in Figure 17. There is close agreement between the SMU and 4156 measurements across the entire temperature range from 93 K to 373 K. At low temperatures, the SMU current gain measurement is greater than that of the 4156. At 93 K the measured peak β of the 4156 and SMU are 394 and 448 respectively. Similarly, at 243 K the measured peak β of the 4156 and SMU are 121 and 176 respectively. At higher temperatures, the SMU and 4156 measurements agree more closely. At very high temperatures, the measured β of the SMU is lower than the 4155. For example, at 373 K the measured β of the SMU is 63 while the 4156

measurement is 75. Overall, the differences between the 4156 and SMU measurements are modest across temperature, but can be attributed to the non-ideal behavior of the temperature coefficient of $R_{2(Temp)}$ that should ideally range from 3500 ppm/K to 3700 ppm/K [43].

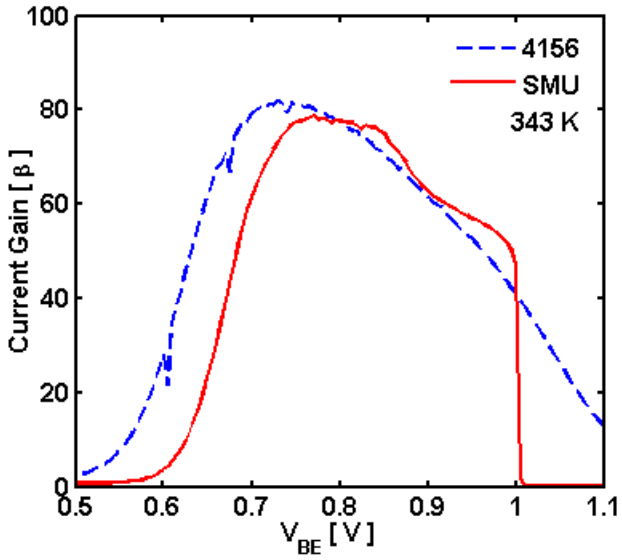


Figure 16: Current gain vs. V_{BE} at 343 K.

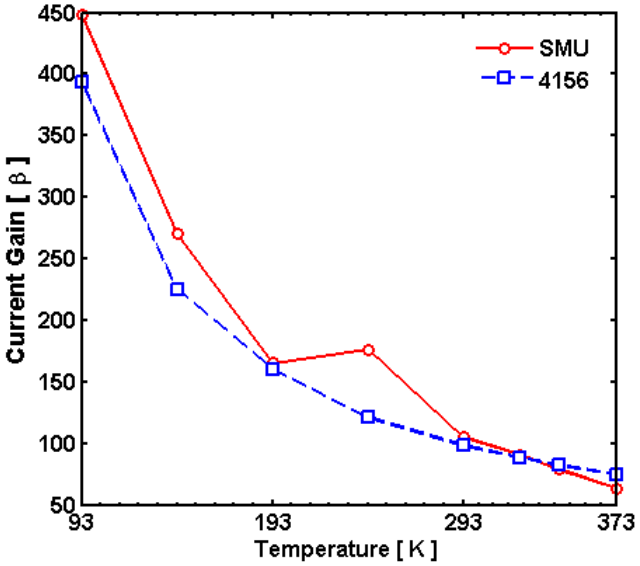


Figure 17: Peak current gain vs. temperature.

2.3.3 Summary

This work presents an on-chip SMU for measurement of current gain of a test SiGe HBT for use in self-healing systems. The SMU accurately measures current gain of the SiGe HBT DUT over a wide temperature range (93 K to 373 K).

The SMU circuit is designed to be applied in closed-looped BIST system where DC characteristic information can be used to infer RF performance metrics. These data can be used to guide the tuning of reconfigurable circuit blocks and thereby "heal" RF performance in response to degradation as a result of either process-induced changes or environmental conditions.

2.4 Tunable Microstrip Lines for Millimeter-wave Applications

The main types of transmission lines found in microwave and MMICs are coplanar waveguides (CPWs) and MLNs. A MLN line simply consists of a planar conductor placed atop the silicon substrate, while a CPW consists of a central signal line placed between a pair of coplanar ground lines placed atop the silicon substrate [63]. In both cases, an additional ground plane is typically added below the planar conductors so that the electric fields generated by the transmission lines are terminated on this ground plane and not in the surrounding substrate, which in silicon processes can exhibit high loss since they have a typical resistivity of 1–20 $\Omega.cm$. In practice however, it is often difficult to attain a solid signal ground which does not experience voltage fluctuations from undesired parasitic effects. The uses of differential transmission line topologies as well as floating shields in the form of either floating metal strips placed underneath the signal line or placed orthogonal to the signal path have been proposed as solutions. The floating shield remains at ground potential with respect to the signal line because no electric field can develop tangential to the strips. In addition, because the floating strips do not develop a net electromagnetic flux over

time, the strips prevent the electromagnetic field from entering the substrate [11, 22]. Floating strips also result in the so-called "slow-wave" transmission line characteristics, in which the speed of the propagating signal is slower than that of a traditional transmission line for a given physical length. The effect of this is to increase the electrical length of the transmission line for a given physical length. Therefore, slow-wave transmission lines can be used to reduce the size of MMIC components such as quarter wave transformers, matching networks, filters, and other structures that may require long transmission lines [11, 68].

Recently, there has been an interest in "tunable" transmission lines, in which the physical or electrical length is manipulated using a switching mechanism, such as switching between different ground planes [14] or the utilization of magnetic materials to change the transmission line characteristics [67]. In this way, the transmission line characteristics can be adjusted *in situ*, enabling tuning of transmission lines and other structures that utilize them. This technique has been used in the design of tunable and reconfigurable microwave circuits such as power amplifiers (PAs) and voltage controlled oscillators VCO, and shows significant potential [20, 44, 45, 46, 47].

2.4.1 Slow-wave-tunable Microstrip Line Design

In this work, the design and performance of novel tunable slow-wave transmission line structures, in which the shield strips are switched between open and ground potentials via nMOS or SiGe HBT devices are investigated. The tunable MLN lines presented here are single-ended, which differs from other designs that employ backplane switching strategies presented in literature [44, 45, 46, 47]. An additional novelty is that the transmission line is made up of sections that can be independently switched between open and ground potentials, resulting in transmission lines that can be programmed to different phase states depending on the combination of switches activated. The electrical length of the transmission lines is adjusted by switching the back plane

of individual sections of the tunable line between open and ground potentials. As a consequence, it is possible to design tunable elements such as phase shifters and tunable matching networks. In addition, the performance of the transmission lines and the effects of using nMOS vs. SiGe HBT switches is investigated for the first time in this context. The tunable transmission lines presented here are based on MLN theory with a grounded backplane, as shown in Figure 18. A grounded MLN line consists of a planar conductor placed atop the silicon substrate, with a grounded metal backplane placed some distance below the conducting line. The electric field (E), passes through the oxide layer and terminates on the ground plane, while the magnetic fields (B) surround the signal line.

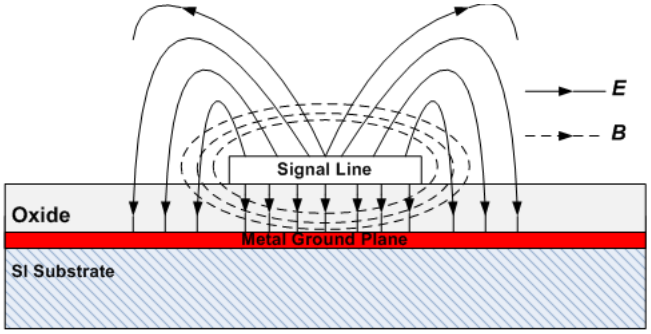


Figure 18: Microstrip cross-section with ground plane and field lines.

MLN transmission lines support a quasi-transverse electric magnetic (quasi-TEM) mode of propagation. In the transverse electric magnetic (TEM) mode, both the electric and magnetic fields are perpendicular to the direction of signal propagation. However, in quasi-TEM mode, there are small E and B field components in the direction of propagation as well. The quasi-TEM nature of the grounded MLN line is due to the fact that the E and B fields exist in different media with different dielectric constants. However, most of the field lines are concentrated in the dielectric region between the signal line and the ground plane. The metal ground plane used is typically patterned with slits to minimize substrate losses. Patterning helps to reduce the formation of eddy currents, which create an electromagnetic field in opposition

to the field created by the propagating signal, and is a source of additional loss.

As previously mentioned, floating the metal strips can result in improved performance and slow-wave characteristics. In this work, the MLN design consists of a signal line with floating metal strips grouped together and connected to an nMOS or SiGe HBT devices that switch the potential on the strips between open and ground. A schematic of a section of the slow-wave MLN line, including important design parameters, is shown in Figure 19. A signal line of width W, with floating metal strips placed on a metal layer below the signal line is shown in Figure 19 (a). The strips are connected together on one side where the nMOS or SiGe HBT device will be connected. Figure 19 (b) is a magnified view of the metal strip backplane in which SS represents the strip spacing and SL represents the strip length.

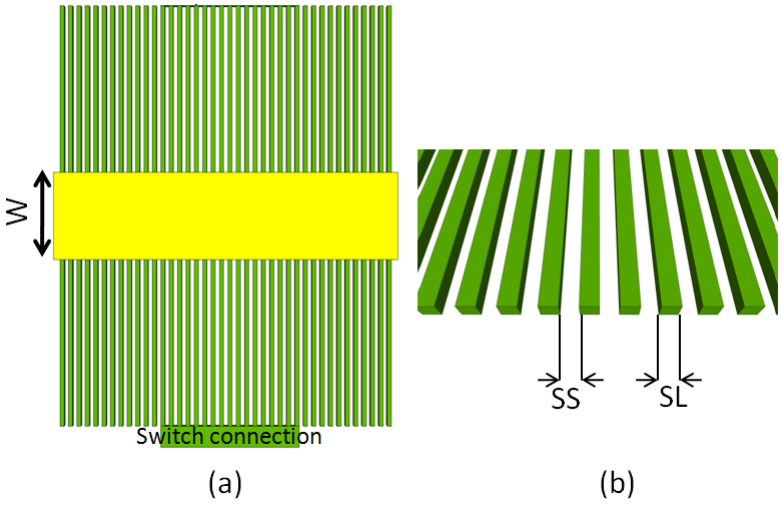


Figure 19: (a) MLN line and (b) Metal strip backplane with design parameters.

The selection of optimal slow-wave transmission line dimensions has been studied extensively in [24]. In that work it was shown that for optimal performance, the transmission line should have a short slit length (SL) and slit spacing (SS). For the transmission lines presented in the current investigation, both SS and SL are made as short as the process design rules permit, which is 1.25 μm for the SiGe BiCMOS

technology utilized. The floating strips were placed on the metal level immediately below the signal trace to maximize coupling and increase the effects of switching the electrical potential between floating and ground on the MLN performance. The vertical distance between the signal line and the floating strips is 2.0 μm.

Because the MLN line supports a quasi-TEM mode, the effective dielectric constant (ϵ_e) can be expressed by a curve fitting approximation [63] given in equation (12),

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12d/W}}, \tag{12}$$

which shows a dependency on the relative dielectric constant (ϵ_r) of the silicon substrate, as well as on the aspect ratio (W/d) of the MLN. The electrical length of the MLN (Φ), in terms of design frequency (ω_o), relative dielectric constant (ϵ_r), and c, the speed of light in vacuum, is given by equation (13),

$$\Phi = \frac{c}{l\omega_o\sqrt{\epsilon_e}}. \tag{13}$$

The effective dielectric constant is adjusted by grounding specific sections of the transmission line backplane using either nMOS or SiGe HBT devices operating as switches. Therefore, the change in electrical length of the transmission line is a function of the change in the effective dielectric constants between the respective switch states. Equation (13) can be rewritten in the form of equation (14),

$$\Delta\Phi = \frac{c}{l\omega_0\sqrt{\epsilon_{e,on} - \epsilon_{e,off}}[\frac{W}{d} + 1.393 + 0.667\ln(\frac{W}{d} + 1.444)]}, \text{ for } \frac{W}{d} \geq 1, \tag{14}$$

where the change in the electrical length, ($\Delta\Phi$) is inversely proportional to the change in effective dielectric constants between the "off" switch state and the "on" switch state. Switching the potential on the backplane between floating and ground also has an impact on the characteristic impedance of the transmission line. The change in

characteristic impedance (Z_0) of a MLN line with ground plane is given by equation (15),

$$\Delta Z_0 = \frac{120\pi}{\sqrt{\epsilon_{e,on} - \epsilon_{e,off}}}, \tag{15}$$

where the ratio of the width of the signal line (W) to its distance from the ground plane (d) is assumed to be much greater than 1, which is the case for the MLN lines presented. This result shows that the characteristic impedance is inversely proportional to the square root of the relative dielectric constant.

The switches were sized to have low insertion loss while maintaining a reasonably high isolation when in the off-state; the area of each nMOS device is 0.18 x 10.00 μm^2 and each SiGe HBT is 0.20 x 20.32 μm^2. Grounding the backplane has the effect of increasing the effective dielectric constant, making the electrical length shorter, in accordance with equations (13) and (14). The MLN lines presented in this work were designed to have a characteristic impedance of 50 Ω. The width of the signal line was chosen to be 20 μm and length to be 400 μm. The floating metal strips were grouped into four 100 μm sections. Each section was connected to an nMOS or SiGe HBT device, as shown in Figure 20. The tunable transmission line with SiGe HBT switches is shown in Figure 20 (a). The SiGe HBTs connected to the backplane of each 100 μm section were diode-connected with the backplane connected to the collector node and biased though a quarter wave (λ / 4) MLN line. The line was designed to be λ / 4 at 94 GHz and used to prevent leakage of RF energy from the backplane through the bias node when the transistor was off. The tunable transmission line with nMOS switches is shown in Figure 20 (b). The backplane of each 100 μm was connected to the drain and the device biased at the gate. In both cases, the change in phase and characteristic impedance of each 100 μm section is independently controlled by an nMOS device. The performance of the transmissions line in terms of phase and characteristic impedance changes across frequency was analyzed with different

combinations of switches activated.

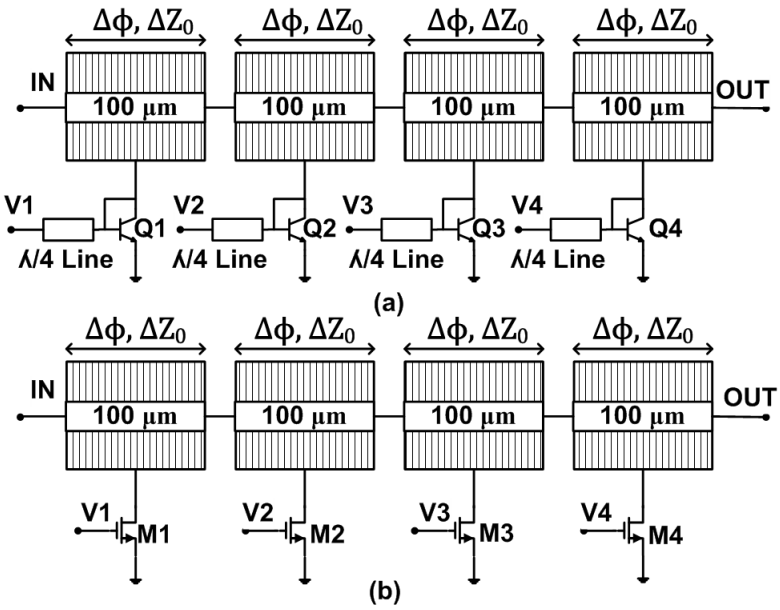


Figure 20: (a) Tunable MLN with HBTs, and (b) tunable MLN with nMOS switches.

2.4.2 Measured Results

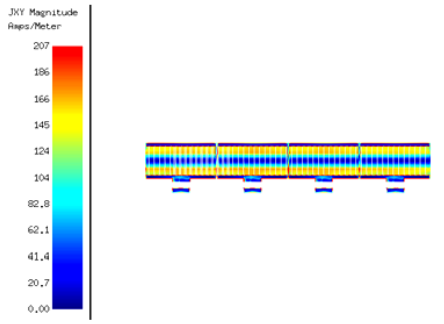
During the design process, the transmission lines were analyzed using an electromagnetic (EM) simulator. The current density distribution on each 100 μm section of the backplane of the 400 μm transmission line at 55 GHz, for different scenarios, are shown in Figure 21. For each scenario, an RF signal is injected from the left end of the signal line. The current density distribution on the backplane when each backplane section is floating is shown in Figure 21(a). The results show that there is almost no current flow at the center of the backplane just under the signal line, but the current density increases towards the edge of each backplane section normal to the direction of signal propagation.

The current density distribution on the backplane changes significantly based on the individual or combination of backplane sections grounded. For instance, the backplane current density distribution when all of the backplane sections are grounded

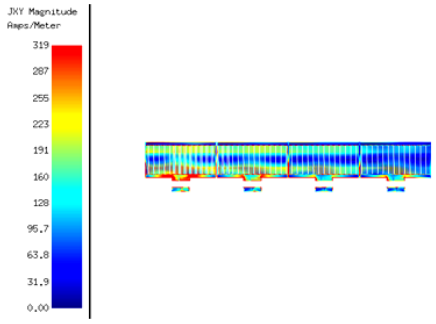
is shown in Figure 21 (b). Like the scenario when all of the sections are open, the current density increases from almost zero at the center to a maximum at the edges normal to the signal propagation, although the pattern is more complex. The results show the current distribution when an RF signal is injected from the left of the signal line. In this case the current distribution on each 100 μm section is not equal, but is at a maximum on the first (left-most) section and then decreases to a minimum on the last (right-most) section. Because of the uneven current distribution, the effects of grounding each section on phase and characteristic impedance of the MLN line is not equal and equal phase changes cannot be achieved from grounding each section in sequence. However, by choosing to ground and open sections in a symmetrical fashion, it is possible to minimize the uneven current density distribution on the backplane and achieve improved phase response. The current distribution on the backplane when the first two (left-most) sections are grounded and the last two are left floating is shown in Figure 21 (c). The current density pattern is more evenly distributed in this case, where the first two sections display the highest current distribution and the last two the lowest. A similar result is observed in Figure 21 (d), which shows the current distribution on the backplane when the first and last sections are grounded and the middle two sections are left floating. Again, the current density pattern is more evenly distributed.

As a result of this analysis, measurements of the 400 μm lines were taken for three cases; 1) the first case where all sections are left floating, 2) where the middle two sections are grounded by turning on the switches attached to them, and finally 3) where all four backplanes were grounded by turning on all switches.

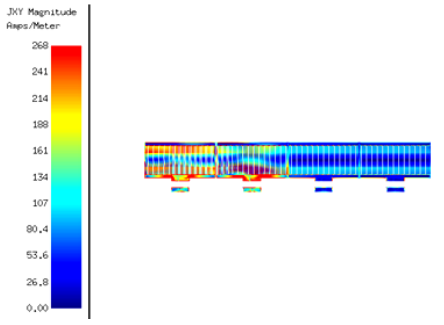
The phase changes and characteristic impedance of the transmission lines under three switch state combinations were measured: 1) "switch state 1", where all four backplane sections floating with switch devices biased off, 2) "switch state 2", where the middle two sections are grounded, and 3) "switch state 3", where all four sections



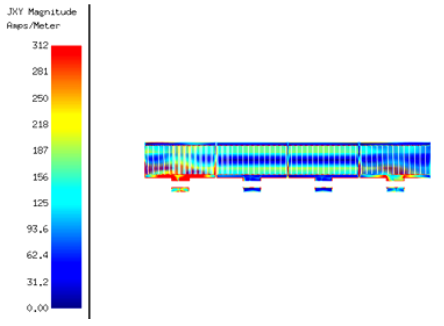
(a)



(b)



(c)



(d)

Figure 21: Backplane current density plots: (a) Backplane sections floating, (b) Backplane sections grounded, (c) First two backplanes grounded and the last two floating, and (d) First and last sections grounded, middle sections floating.

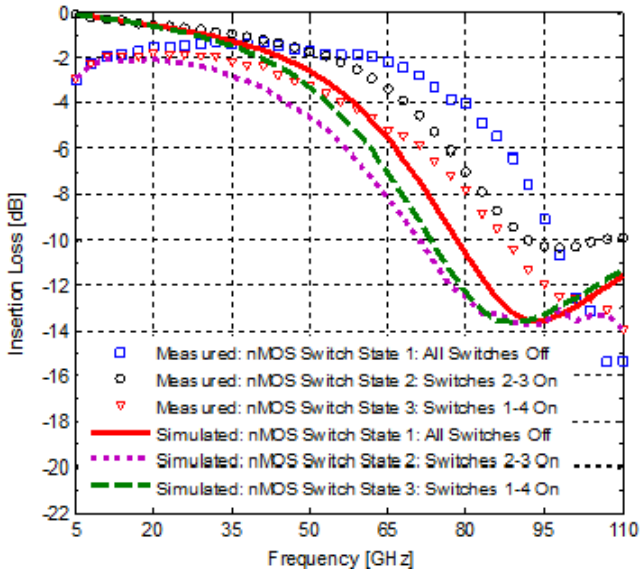
are grounded. The measured de-embedded and simulated insertion loss from 5–110 GHz for the nMOS and SiGe HBT tunable MLN lines are shown in Figure 22. The insertion loss of the MLN line with nMOS switching devices is shown in Figure 22 (a). The measured insertion loss ranges from approximately 2 dB at 10 GHz to 5.8 dB at 55 GHz and ranges from approximately 6 dB at 55 GHz to 14 dB at 110 GHz. Moreover, insertion loss increases for each switch state from 1–3. From 5–10 GHz, the insertion loss for all switch states improves from 3 dB at 5 GHz to 2 dB at 10 GHz. This is attributed to parasitic effects and resonances induced by the RF pads and active devices. The discrepancy in insertion loss between the measured and simulated results, especially from 5–35 GHz, can also be attributed to parasitic effects and resonances that were not captured in the EM simulation. In particular, since the distributed nature of the MLN line can be modeled as cascading series of capacitors and shunt inductors, the active devices, which present shunt parasitic inductance and capacitance, negatively affect the performance of the MLN lines.

The insertion loss of the MLN line with SiGe HBT switching devices is shown in Figure 22 (b). The measured insertion loss ranges from approximately 0.8 dB at 5 GHz to 2.8 dB at 55 GHz, and ranges from a minimum of 1.4 dB at 55 GHz to a maximum of 28 dB at 110 GHz. The insertion loss increases for each switch state from 1–3 from 5–25 GHz and then the slopes of the insertion loss curves for switch states 1 and 3 reverse, resulting in lower loss for switch state 3 than the loss for switch state 1 from 25 GHz and beyond. This can again be attributed to parasitic effects and resonances induced by the RF pads and active devices.

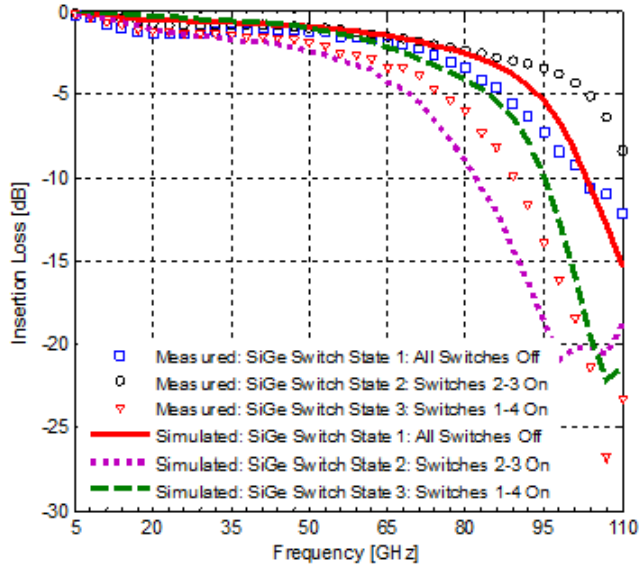
The measured characteristic impedance (the real part) for the tunable MLN lines from 5–110 GHz is shown in Figure 23. The characteristic impedance for each switch state of the tunable MLN line implemented with nMOS devices is shown in Figure 23 (a). The results show that the real part of the characteristic impedance ranges from 39 Ω - 52.5 Ω from 5–55 GHz. The characteristic impedance decreases with the switch

state progression from states 1–3 until approximately 40 GHz, where the impedance for each states begins to increase for switch states 2 and 3, while the impedance for switch state 1 continues to decrease. From 55–110 GHz, the characteristic impedance ranges from 28 Ω - 51 Ω across the frequency band. The characteristic impedance decreases with switch state progression from states 1–2 and then increases for switch state 3. Moreover, from 55–110 GHz, the characteristic impedance of the line for all switch states decreases with increasing frequency.

The characteristic impedance for each switch state for the tunable MLN line implemented with SiGe HBTs is shown in Figure 23 (b). The results show that the real part of the characteristic impedance ranges from 44.8 Ω – 23 Ω from 5–55 GHz. From 55–110 GHz, the characteristic impedance ranges from 28 Ω – 52 Ω. The characteristic impedance decreases with the switch state progression from states 1 to 3 until approximately 45 GHz, where the impedance for each state begins to increase. Unlike for the case of the tunable MLN line with nMOS switches, the impedance increases for all switch states 1 to 3. In addition, the relative change in impedance between each switch state is more constant than the change in impedance between switch states in the tunable transmission lines with nMOS devices.

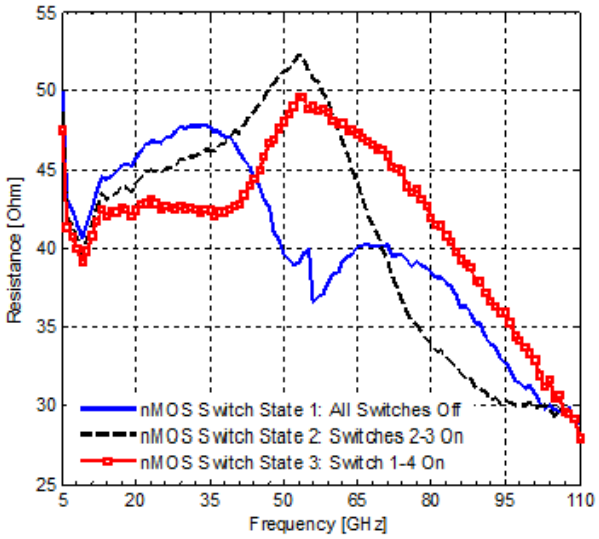


(a)

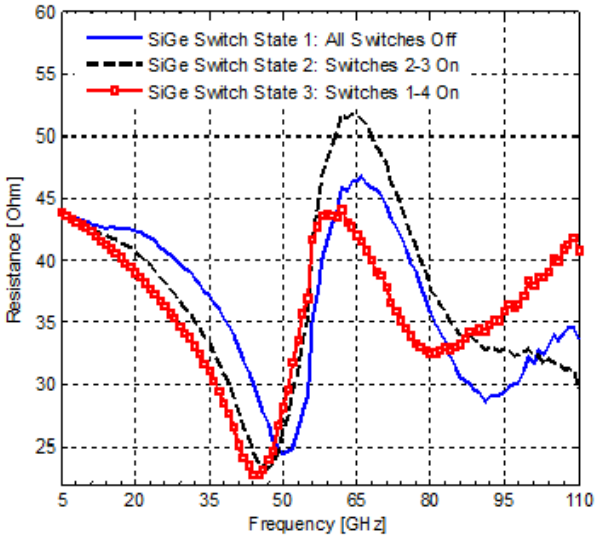


(b)

Figure 22: (a) Insertion loss for tunable MLN line with nMOS devices(b) Insertion loss for tunable MLN line with HBT devices.



(a)



(b)

Figure 23: (a) Characteristic impedance for the tunable MLN line with nMOS devices. (b) Characteristic impedance for the tunable MLN line with SiGe HBT devices.

The phase difference for each switch state between the input and output ports of the tunable MLN line with nMOS switches from 5–110 GHz is shown in Figure 24. The phase difference grows with increasing frequency and increases at a constant rate up until approximately 43 GHz, at which point the phase difference between each state reduces and is less consistent. Specifically, the measured and simulated phase change between switch state 1 and switch state 2, as well as the phase change between switch state 1 and switch state 3 is shown in Figure 24. The measured phase difference between switch states 1–3 increases from approximately 0^0 to a maximum 11^0 at 43 GHz. The measured phase difference between switch states 1–2 increases from approximately 0^0 to 4.9^0 at 38 GHz. Therefore, the phase change between switch states 1–3 is approximately twice that of the phase change between 1–2 and indicates an even phase transition between switch states 1, 2, and 3. However, beyond 43 GHz the phase difference between the switch states decreases and is less consistent. The EM simulated results do not show this behavior, and instead indicate that the phase difference increases at a constant rate for each state. From 55–110 GHz, the measured phase difference between switch states 1–3 increases to a maximum of approximately 62^0 at 95 GHz and the measured phase difference between switch states 1–2 increases to 41^0 at 10^0 GHz. The phase change between switch states 1 and 3 is approximately twice that of the phase change between 1 and 2 and indicates an even phase transition between switch states 1, 2, and 3. However, the phase relationship across frequency is not constant and the phase difference decreased beyond 100 GHz. The simulated results show a similar trend as the measured results, but with less of a phase difference between the switch states. The discrepancy can be attributed to the lack of accurate modeling of these devices in the measured frequency range.

The phase for each switch state between the input and output ports of the tunable MLN line with SiGe HBT switches from 5–110 GHz is show in Figure 25. The phase difference between each switch state grows with increasing frequency and increases at

a constant rate. The results show the measured and simulated phase change between switch state 1 and switch state 2, as well as the phase change between switch state 1 and switch state 3. The measured phase difference between switch states 1 to 3 increases from approximately 0^0 to 14.3^0 at 53 GHz.

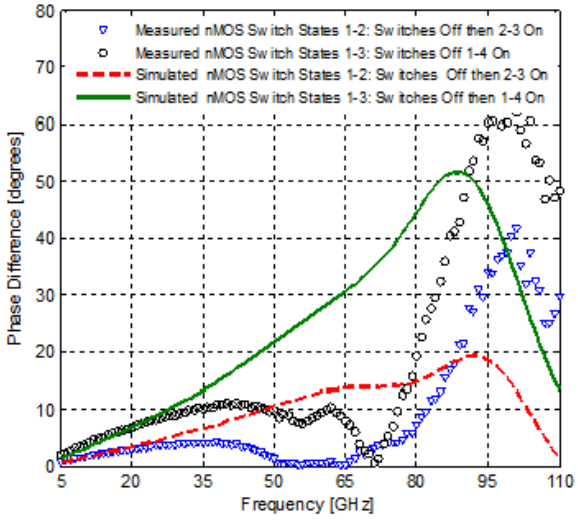


Figure 24: Measured and simulated phase difference of tunable MLN with nMOS devices between switch states 1-2 and switch states 1–3 from 55–110 GHz.

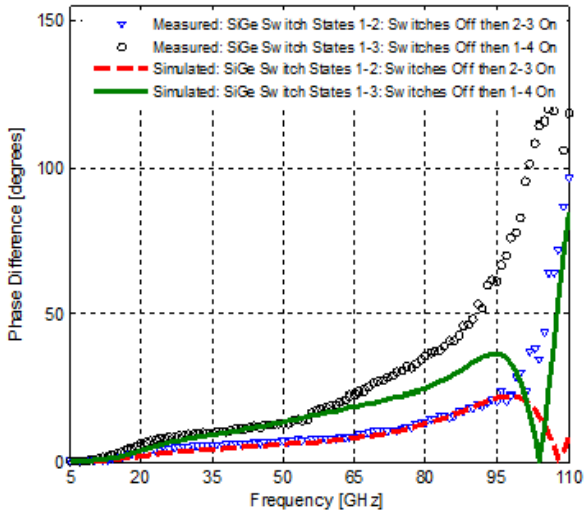


Figure 25: Measured and simulated phase difference of tunable MLN with SiGe devices between switch states 1-2 and switch states 1–3 from 55–110 GHz.

The measured phase difference between switch states 1–2 increases from approximately 0^0 to 7.9^0 also at 53 GHz. Again, the phase difference between switch states 1 and 3 is approximately twice that of the phase change from 1 and 2. The simulated and measured results follow each other very closely and the phase difference between switch states increases for the entire frequency range although the rate of increase is not constant. The measured phase difference between switch states 1 and 3 increases from approximately 8^0 to a maximum 98^0 at 110 GHz. The measured phase difference between switch states 1–2 increases from approximately 18^0 to 120^0 also at 110 GHz. Beyond 100 GHz, however, the phase relationships between the switch states become inconsistent, with the phase difference between switch states 2 and 3 decreasing with increasing frequency. The simulated results follow the measured results closely and also show a reduction in the phase difference at frequencies above 100 GHz.

2.4.3 Summary

In summary, the performance of both tunable MLN structures indicates inherent advantages and disadvantages for each at different frequency ranges. In the 5-55 GHz range, both the nMOS and SiGe HBT MLNs are similar in their performance, with slightly less insertion loss and greater phase change for the line with SiGe HBT devices. However in the 55–110 GHz range, the transmission line with SiGe HBT devices shows a greater difference in phase between switch states and maintains its phase difference for higher frequency range. The transmission line with nMOS devices has better insertion loss at higher frequencies but its phase change performance is not as good at the transmission line with SiGe HBTs. These single-ended MLN lines can be used in the implementation of tunable matching networks, phase shifters and other tunable structures needed in state-of-the-art microwave and millimeter-wave circuits operating at frequencies below 60 GHz where the insertion loss is within a range where it will not significantly affect circuit performance if the tunable MLN is placed

directly in the signal path. However, at higher frequencies, the tunable MLN can still find applications where it is not placed directly in the signal path, such as short and open stubs in matching networks. This method for designing tunable single ended transmission lines appropriate for use in start of the art MMIC and the tunable MLNs are fully compatible with conventional BiCMOS processes.

2.5 Revised Tunable MLN based on nFET Switches

Building upon the work done in the previous section, a second tunable transmission line was designed using n-channel field-effect transistor (nFET) transistors to switch the backplane between floating and ground potential. A schematic of the the tunable MLN is shown in Figure 26. The structure is 150 μm long and the floating backplane is connected to the collector nodes of two nFETs at the ends of the short sides of the rectangular backplane. The gates of the nFET devices were tied together through 5 $k\Omega$ resistors, the voltage at the gates were simultaneously controlled using a control voltage (V_{ctl}) ranging from 0–3 V, and the emitters of M1 and M2 are grounded.

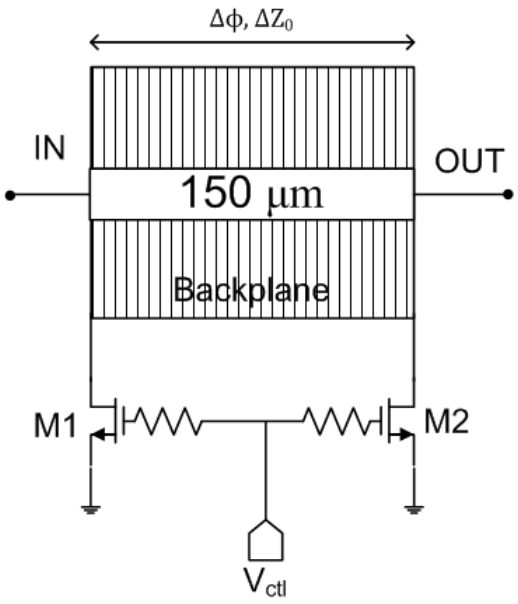


Figure 26: Schematic of tunable MLN with nFET switches.

The control voltage is operated in two states. When V_{ctl}= 0 V, that is when transistors M1 and M2 are turned off, they are modeled as a large shunt resistor to ground (R_{off}) that results in the backplane staying at floating potential. However, when the devices are on ($V_{ctl} > 0V$), there is a significant shunt capacitance to ground of both M1 and M2 and R_{on} is small. This results in the entire structure's behavior resembling that of a typical MLN which is modeled by shunt capacitances and series inductances. Therefore when the switches are turned on, the insertion loss is minimized using the traveling wave concept [10, 50].

A more detailed view of the tunable MLN is given in the 3D model shown in Figure 27. Shown in this model are the signal, backplane ,and ground layers; there is no metal in the area directly below the backplane because otherwise the return current of the tunable MLN would flow on this layer short-circuiting the switches and rendering the MLN tuning inoperable.

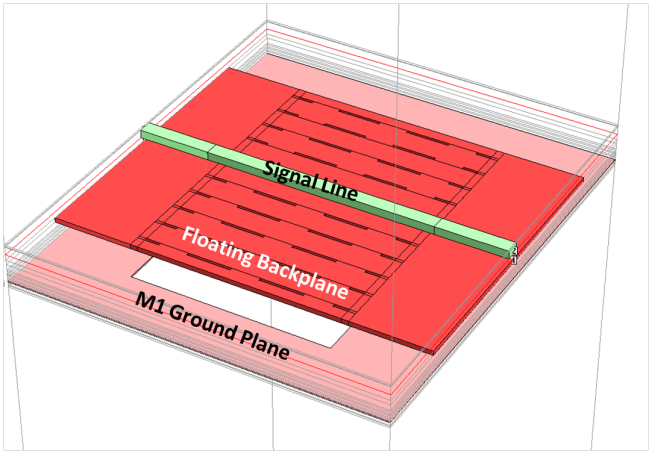


Figure 27: 3D model of tunable MLN.

The ground plane, created from the lowest metal in the metal stack, surrounds the tunable MLN structure. The emitters of M1 and M2 were connected to this ground plane. The nFET devices used in the design were high voltage (3.3 V) devices and were sized to trade-off tuning range with minimum insertion loss; the nFET size selected was 50 x 5 μm^2.

2.5.1 Measured Results

The s-parameters of the tunable MLN were measured using an Anritsu vector network analyzer (VNA) from 10 –110 GHz. A die micrograph of the 150 μm tunable MLN is shown in Figure 28.

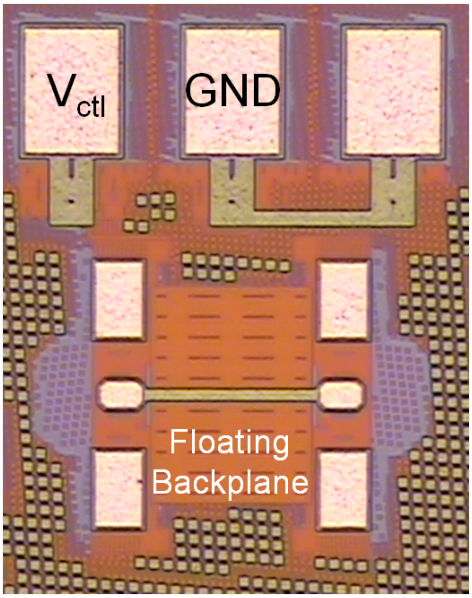


Figure 28: Annotated die micrograph of tunable MLN.

The input impedance and phase between the input and output ports of the MLN were calculated from the measured S-parameters. The bias voltage (V_{ctl}) of the gates of transistors M1 and M2 were varied from 0–3.3 V. The input reflection coefficient of the tunable MLN for two switch states (V_{ctl} = 0 V and 3.3 V) is shown in Figure 29.

As shown in the figure, the input reflection coefficient starts at the center of the Smith Chart (50 Ω point) and curve moves into the capacative region at higher frequencies. It also moves clockwise and becomes more capacative as V_{ctl} increases from 0–3.3 V as a result of the increase in shunt capacitance from the nFET devices.

The insertion loss for V_{ctl} = 0, 0.9, and 3.3 V is shown in Figure 30. It illustrates that the insertion loss when $V_{ctrl} = 0\ V$ ranges from 0.1 dB at 10 GHz to 5.5 dB

at 110 GHz. As V_{ctl} is increased, the insertion loss improves, particularly at higher frequencies. This is because when the transistors are turned on, the transmission line behaves more like a traditional 50 Ω MLN.

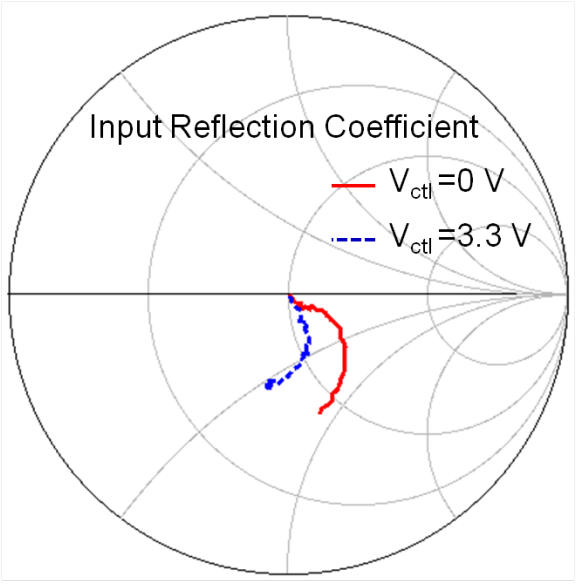


Figure 29: Smith Chart showing input return loss of tunable MLN for V_{ctl} = 0 V and 3.3 V.

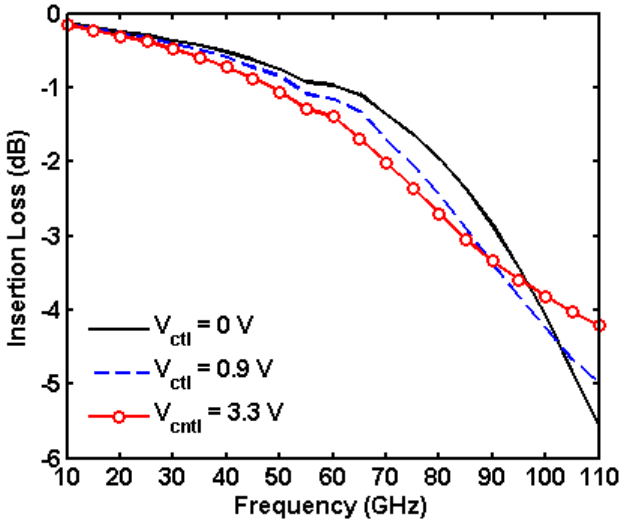


Figure 30: Insertion loss of tunable MLN for V_{ctl} = 0, 0.9 and, 3.3 V.

The real and imaginary parts of the characteristic impedance vs. frequency and V_{ctl} are shown in Figure 31 and 32 respectively. The characteristic resistance, shown in Figure 31, is between 50–55 Ω at frequencies below 65 GHz. However, at frequencies above 65 GHz, the impedance increases sharply as V_{ctl} is increased. This trend continues until 90 GHz when the impedance falls sharply. The opposite behavior is seen with the reactance vs. frequency and V_{ctl} shown in Figure 32. The reactance decreases until 90 GHz. At this frequency the reactance starts increasing with increasing V_{ctl} voltage.

The phase between the input and output ports of the tunable MLN vs. frequency and V_{ctl} is shown in Figure 33. The phase remains relatively constant between each V_{ctl} state from 10–65 GHz. However, the phase decreases as V_{ctl} increases. The maximum phase difference (between the states when $V_{ctl} = 0$ V and 3.3 V) is 13° at 100 GHz.

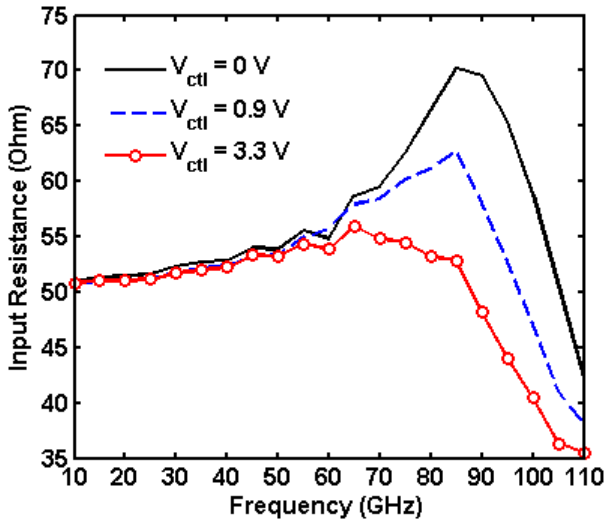


Figure 31: Input resistance of tunable MLN for $V_{ctl} = 0$, 0.9 and, 3.3 V.

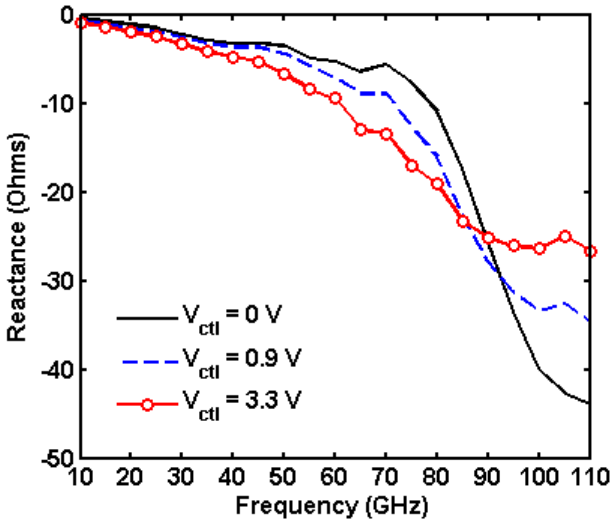


Figure 32: Input reactance of tunable MLN for V_{ctl} = 0, 0.9 and, 3.3 V.

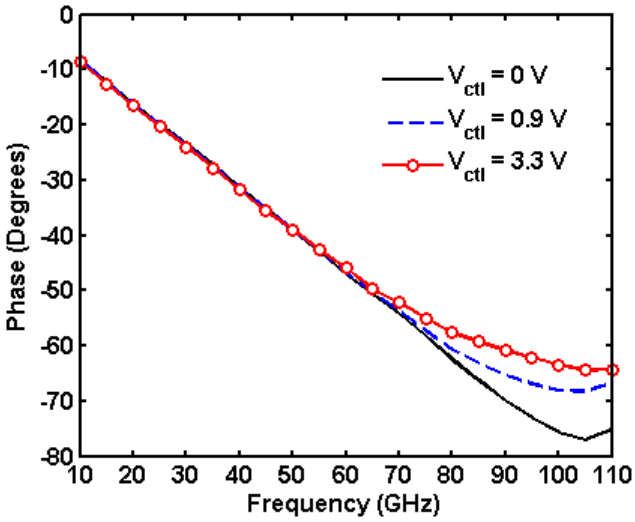


Figure 33: Phase between input and output ports of tunable MLN for V_{ctl} = 0, 0.9 and, 3.3 V.

2.5.2 Summary

In summary, the tunable MLN with nFET switches demonstrates that it can be used to generate variable characteristic impedance, input return loss, and to a lesser extent phase changes at microwave and millimeter-wave frequencies. The 150 μm test MLN

exhibits minimal loss and can easily be integrated into MIMIC systems to facilitate tunable RF circuits.

2.6 A Broadband, Millimeter-wave, Asymmetrical Marchand Balun in 180 nm SiGe BiCMOS Technology

Baluns are important components in many MMICs. They convert single-ended signals into differential or balanced signals, and are used in balanced circuit topologies such as mixers, differential push-pull amplifiers, and voltage controlled oscillators VCOs [84]. A variety of balun designs have been reported in the literature. Originally, baluns were coaxial-based [59]. Later, planar-based structures such as the Wilkinson power divider, and coupled-line-based designs have been developed [3, 13]. The planar Marchand balun consists of two pairs of coupled lines, with appropriate open and short terminations. The Marchand balun is popular in microwave designs for its simplicity and wideband characteristics. Additionally, the Marchand balun can be designed using multiple metal layers to enhance coupling between lines. This has the additional effect of reducing its size, which is clearly of significant benefit in highly integrated solutions. Most research into Marchand balun designs have concentrated on widening the operating bandwidth and reducing the size of the balun. In some cases, novel transmission line structures have been applied, using, metamaterials and slow wave transmission lines or alternative substrates such as Liquid Crystalline Polymer (LCP) [26, 83].

The Marchand balun presented is a two metal layer design utilizing broadside, meandering coupled MLN lines. The width of each MLN line is chosen independently to produce an asymmetrical Marchand balun with enhanced bandwidth characteristics. The Marchand balun was implemented using a commercially available 180 nm SiGe BiCMOS technology. At the time of writing, the results presented here demonstrate the widest operating bandwidth of any Marchand balun in the millimeter-wave frequency range.

2.6.1 Marchand Balun Analysis and Design

The planar Marchand balun consists of two pairs of coupled quarter-wave transmission lines, with open and short circuit terminations at appropriate points. The balun is a three terminal device with two balanced ports and one unbalanced port, as shown in Figure 34. The balun is modeled by the characteristic impedances of the transmission lines: Z_a, Z_b, and Z_{ab}, as well as coupling ratio k, and termination resistances R_S and R_L. In general, R_S is not equal to R_L.

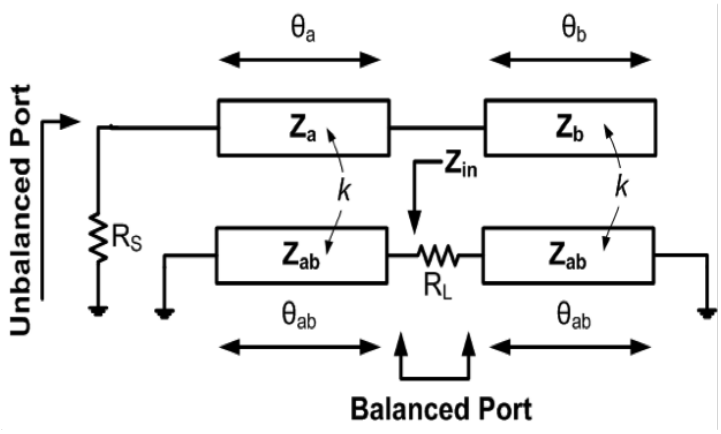


Figure 34: Schematic of the symmetrical Marchand balun.

A symmetrical Marchand balun is one in which all microstrip lines have the same width and characteristic impedance ($Z_a = Z_b + Z_{ab} = Z_o$), and can be analyzed as two sections of coupled lines. The coupled line S-parameters can then be used to derive relationships for the even and odd mode impedances as well as the coupling ratio. These metrics are used to derive the design equations of the balun [2]. However, in an asymmetrical balun, the characteristic impedances of each line are chosen independently and the analysis takes a different form [12]. The Marchand balun can be modeled with the equivalent lumped circuit model shown in Figure 35.

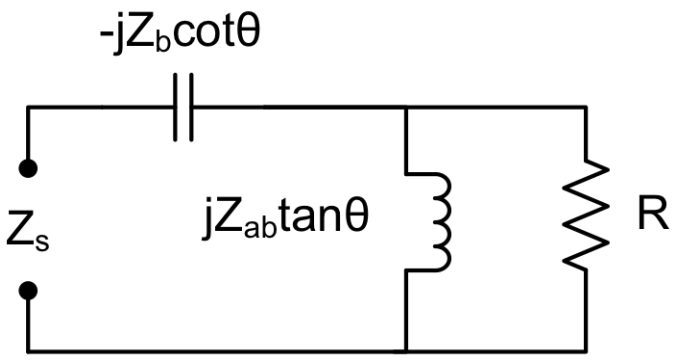


Figure 35: Circuit model of an asymmetrical Marchand balun.

The input impedance seen at the balanced port is given by

$$Z_{in} = r + jx = \frac{R_L Z_{ab}^2 \tan^2\theta_{ab}}{R_L^2 + Z_{ab}^2 \tan^2\theta_{ab}} + j\left(\frac{R_L Z_{ab}^2 \tan^2\theta_{ab}}{R_L^2 + Z_{ab}^2 \tan^2\theta_{ab}} + -Z_b \cot\theta_b\right). \tag{16}$$

The real and imaginary parts of equation (16) can be separated and normalized by the load resistance R_L to generate equations (17) and (18),

$$\frac{r}{R_L} = \frac{Z_{ab}^2 \tan^2\theta_{ab}}{R_L^2 + Z_{ab}^2 \tan^2\theta_{ab}}, \tag{17}$$

$$\frac{x}{R_L} = \frac{\frac{Z_{ab}}{R_L}(R_L^2 - Z_{ab}Z_b)\tan\theta_{ab} - R_L Z_b \cot\theta_b}{R_L^2 + Z_{ab}^2 \tan^2\theta_{ab}}. \tag{18}$$

Analyzing the normalized real part of the input impedance reveals that the input resistance of the balun divided by the electrical length is essentially constant and is mainly dependent on the ratio of Z_{ab}/R_L. Additionally, the normalized reactive part of the input impedance crosses zero when $R^2 > Z_b Z_{ab}$, or when $R^2 < Z_b Z_{ab}$. The derivative of the reactive part of the impedance is given by

$$\frac{dx}{df} = -j\frac{\pi}{2}\frac{R_L^2 - Z_{ab}Z_b}{Z_{ab}}, \text{ for } f = f_0 \text{ and } \theta_{ab} = \frac{\pi}{2}\frac{f}{f_0}. \tag{19}$$

Equation (19) reveals that the slope is negative for $R^2 > Z_b Z_{ab}$ and positive for $R^2 < Z_b Z_{ab}$. It has been shown that in order to achieve the widest possible bandwidth, it is necessary to simultaneously optimize Z_{ab}/R_L by maximizing Z_{ab} and satisfying

the equation $R^2 = Z_b Z_{ab}$ [12, 59].The resulting inequality that optimizes bandwidth is given by

$$Z_{ab} > R > Z_b. \tag{20}$$

In addition to optimizing for bandwidth, it is necessary to select impedances for the desired matching at each port. This is achieved by setting an appropriate value for the voltage standing wave ratio (VSWR). Setting a design goal of VSWR to a ratio of 2:1 is a standard practice for a good low-loss balun [59, 64]. The resulting inequality needed to satisfy the VSWR requirement is given by

$$2Z_a > R > Z_b. \tag{21}$$

The final optimization condition taking into consideration both bandwidth and VSWR is given by

$$2Z_{ab} > 2Z_a > R > Z_b. \tag{22}$$

To satisfy these conditions, the balun presented here was designed with asymmetrical broadside coupling of the MLN lines between the top two metal layers of the SiGe BiCMOS process. The coupling ratio between two metal layers is also enhanced by the relative dielectric constant of the substrate [51]. The coupling between two metal lines on different levels is given by

$$k = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} = \sqrt{\epsilon_r} x k_{air}. \tag{23}$$

In equation (23), Z_{0e} and Z_{0o} are the even and odd mode impedances of the coupled lines, ϵ_r is relative permittivity of the substrate, and k_{air} is the coupling factor of the two lines in air. To satisfy the requirements of equation (22), the metal 5 (second from the top) lines were made wider than the metal 6 (top metal layer) lines. Moreover, the widths of both metal 5 lines were made equal to maintain the same impedance of Z_{ab}. A 3D EM momentum model of the balun is shown in Figure 36.

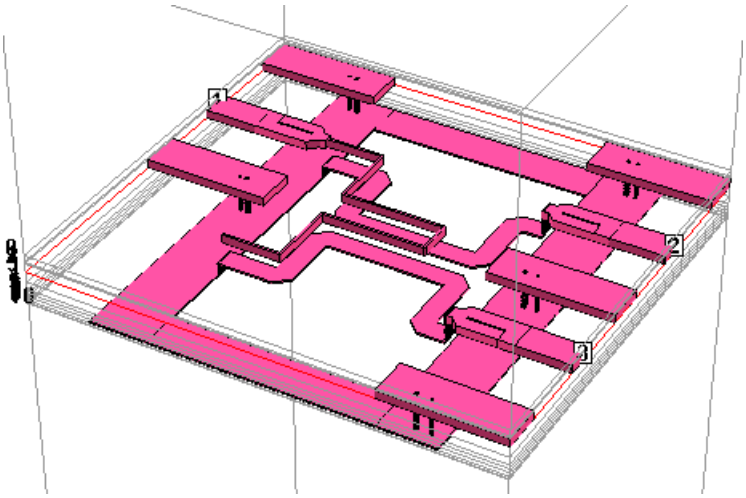


Figure 36: 3D EM model of balun.

2.6.2 Measured Results

The balun was measured using an Agilent VNA, using 110 GHz cables and probes. A die photo of the balun is shown in Figure 37, and it has an overall die area of is 0.80 mm x 0.70 mm.

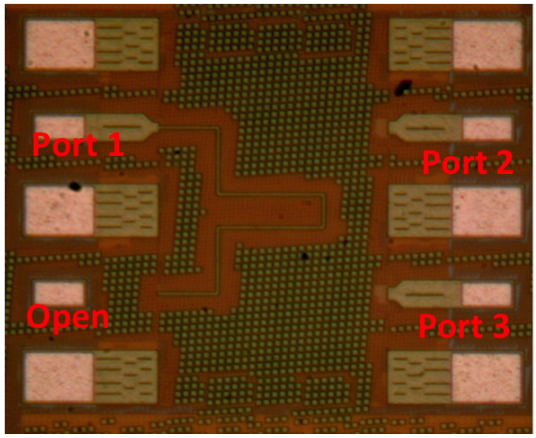


Figure 37: Die micrograph of balun.

The S-parameters from 30–100 GHz were measured by performing a pair of two-port measurements. First, the S-parameters of port 1 and port 2, with port 3 terminated with a 50 Ω, were measured. Then, the S-parameters of port 1 and port 3 were measured in a similar fashion. The pair of two-port files was combined to generate

the three-port balun S-parameters. Figure 38 shows the insertion loss from ports 1 to 2 and ports 1 to 3. The balun has better than 10 dB insertion loss, or better than 7 dB insertion loss when the 3 dB coupling ratio is considered.

The measured isolation at ports 1, 2, and 3 is shown in Figure 39. S_{22} and S_{33} are almost identical and are below 10 dB from 55–100 GHz and S_{11} is below 10 dB from 51–80 GHz.

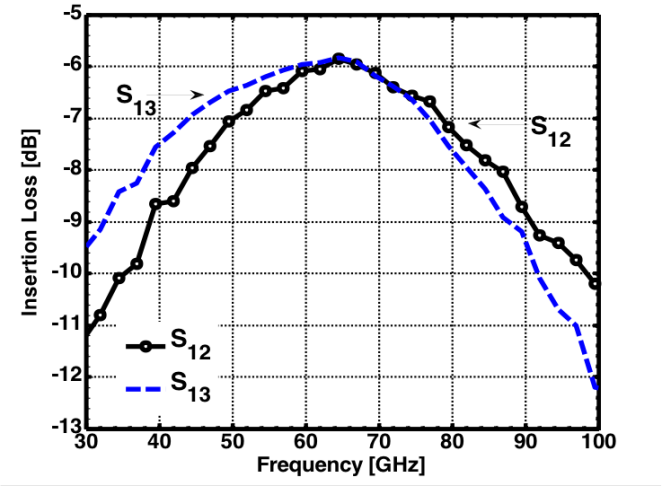


Figure 38: Balun insertion Loss.

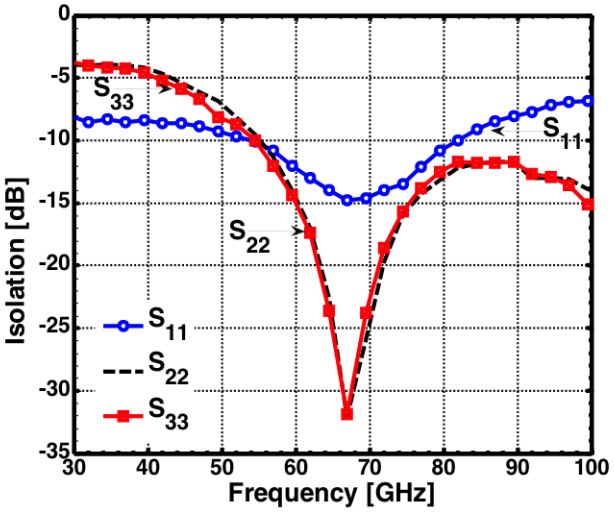


Figure 39: Balun isolation.

The measured phase difference between the balanced ports is shown in Figure 40, with lines indicating ±180° phase for reference. The data indicate that the balun maintains excellent phase balance between ports over a very wide frequency range.

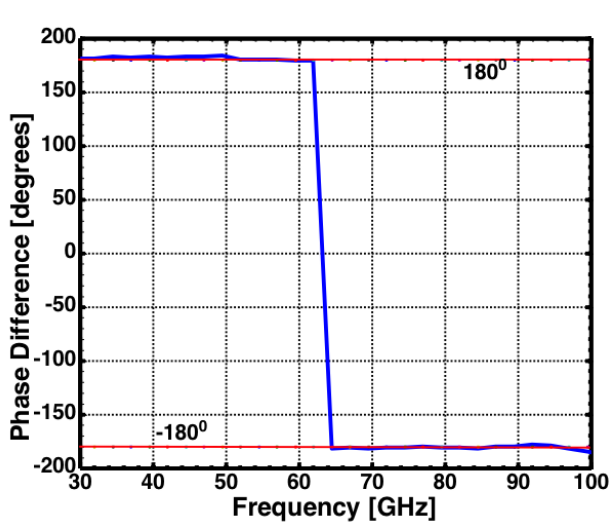


Figure 40: Phase difference between the balanced ports.

To further characterize the balun, additional relevant performance metrics include the amplitude and phase imbalances [23]. The amplitude imbalance is a measure of the difference in amplitude of the signals at the balanced port. The phase imbalance measures the deviation of the phase between the balanced port outputs from the ideal 180°. The phase and amplitude imbalance were calculated from the measured S-parameters using equations (24) and (25) respectively,

$$\phi = ang\left(\frac{S_{31}}{S_{21}}\right), \tag{24}$$

$$A = 20\log\left(\frac{S_{31}}{S_{21}}\right). \tag{25}$$

The amplitude imbalance is shown in Figure 41, and ranges from -1.6 dB at 30 GHz to +0.6 dB at 90 GHz. The measured phase imbalance is shown in Figure 42, and is 5.2°. The measured results demonstrate that the presented balun is suitable for

a wide range of millimeter-wave applications. The performance comparisons of the present results with other published baluns is contained in Table 2, and demonstrate that this new balun achieves the widest operating bandwidth and is very competitive with other baluns operating in similar frequency bands.

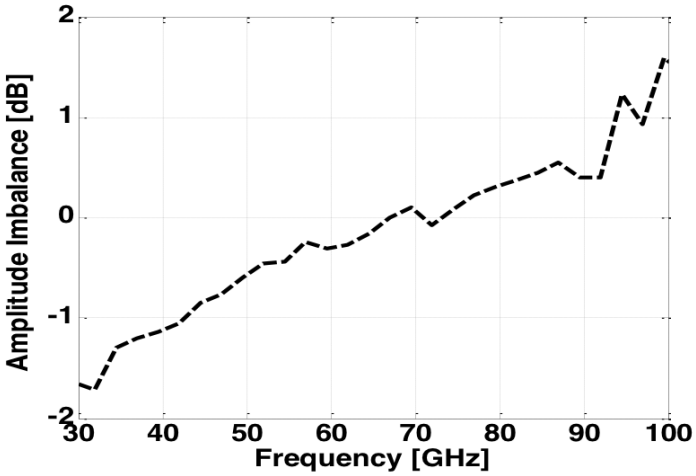


Figure 41: Amplitude imbalance of the balun.

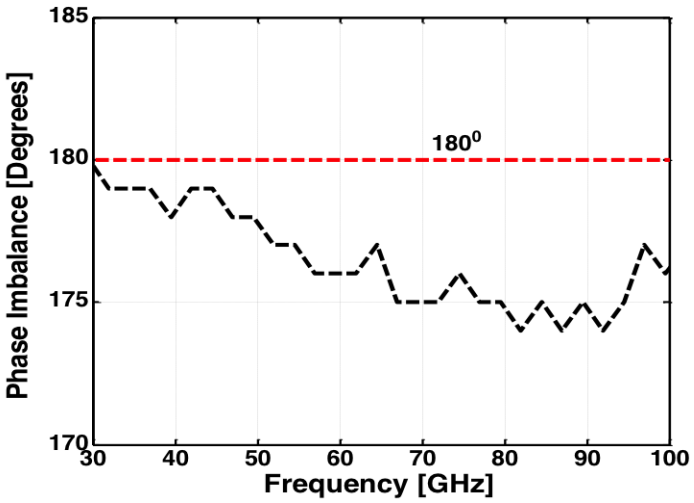


Figure 42: Phase imbalance of the balun.

Table 2: Comparison with Other Baluns Operating in Similar Frequency Bands.

Ref.	Freq. (GHz)	Amplitude Imbalance (dB)	Phase Imbalance (degrees)	Insertion Loss (dB)	Topology	Technology
[51]	25–65	± 1.5	10	<10	Marchand	0.18 μm CMOS
[23]	50–65	3	5	6	Transformer	0.18 μm CMOS
[12]	16–67	1	5	<7	Stacked	0.18 μm CMOS
[38]	40–61	± 1.5	± 15	3.7	Marchand	0.18 μm CMOS
[40]	54–59	± 0.7	± 5	-	Active	0.18 μm CMOS
This Work	30–90	-1.6/+0.6	± 5.2	< 7	Marchand	0.18 μm SiGe

2.6.3 Summary

A 30–90 GHz Marchand balun operating at a center frequency of 65 GHz is presented that features low insertion loss, wide bandwidth operation, and excellent amplitude and phase balance. The balun utilizes multi-layer coupling with the top two layers and optimized layout techniques to reduce area and improve performance. The balun has an amplitude imbalance of -1.6 dB at 30 GHz and +0.6 dB at 90 GHz, and a phase imbalance of $\pm 5.2^{\circ}$, with insertion loss of < 7 dB over the entire frequency range of interest.

CHAPTER III

RECONFIGURABLE LOW NOISE AMPLIFIERS

3.1 Introduction

Reconfigurable, wideband, LNAs can be applied to emerging areas in communication and other wireless technologies. Beginning in the last decade, there has been growing interest in wideband systems, in particular for scientific and military applications. Wideband wireless communications systems such as ultra-wideband (UWB), nominally operating from 3–10 GHz, are attractive because the wide bandwidth enables higher data rates. Wideband systems show promise in the areas of medical imaging, vehicular communications, and other short-range communications needs. In addition, C-Band (4–8 GHz) and X-Band (8–12 GHz), are actively exploited for satellite communications and for a wide variety of radar systems. Thus, wireless transceivers which can simultaneously cover multiple frequency bands are extremely attractive because they potentially enable more efficient spectrum utilization.

Many approaches have been offered for the design of wideband LNAs. For example, the widest bandwidth has been achieved using distributed topologies [85]. However, distributed amplifiers typically take up substantial die area and also suffer from high NF. Other approaches such as common gate and ladder-matched LNAs also suffer from high NF [48, 73]. Additional approaches include staggered compensation and transformer feedback techniques [25, 72]. Both can be used to successfully extend bandwidth, but both suffer from high NF. In addition, shunt-resistive feedback has been used with some success [52].

Reconfigurable LNAs can also be applied space applications in which there is an inherent degradation of circuit performance as a result of exposure to ionizing

radiation.

This chapter presents results relating to the performance of reconfigurable wideband LNAs geared towards BIST and self-healing systems. The LNAs presented incorporate tuning knobs to adjust relevant performance metrics to mitigate for the effects, of PVT, environmental effects, and generally, for the improvement of yield.

3.2 An Ultra-wideband LNA with Gain and Return Loss Control

A central component of any wireless transceiver system is the LNA, and for wideband systems the design of the LNA presents significant challenges, because they simultaneously must achieve broadband impedance matching as well as very low noise figure across the band, all at low power dissipation. The LNA presented here utilizes emitter degeneration, resistive feedback, and inductive peaking to increase bandwidth. A novel varactor-controlled method for the adjustment of input return loss has been developed and included. Additionally, a novel p-channel field-effect transistor (pFET) gain control method is presented [36]. This work presents an ultra-wideband (UWB) LNA with built in gain and return loss control.

3.2.1 Circuit Analysis and Design

The LNA is a three stage design. The schematic of the SiGe LNA is shown in Figure 43. The LNA has a common emitter (CE) input at Q1 with emitter resistive and capacitive degeneration provided by C1, C2, and R1. The capacitive degeneration is implemented by using metal-insulator-metal (MIM) capacitor and a varactor C2. Additionally, an active pFET load, M1, in series with a resistor, R2, is used to provide gain control.

The second stage is composed of a source-follower buffer Q2 which is used in conjunction with a feedback resistor R_f, to provide feedback to the input stage. The use of feedback makes it possible to provide a 50 Ω match at the input without the use

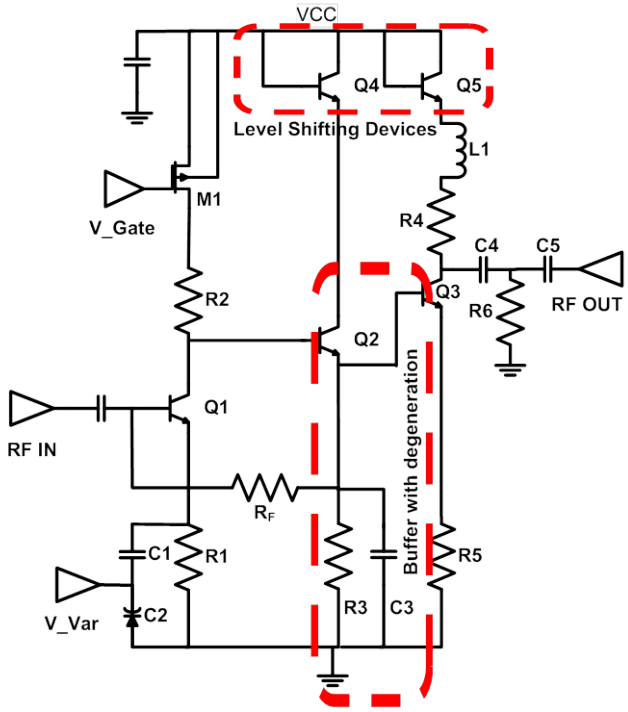


Figure 43: Schematic of reconfigurable UWB LNA.

of a traditional inductor, thus saving valuable silicon die area. Additionally, feedback helps to increase the bandwidth. However, there is a trade-off between the selection of R_f for matching and noise [82]. The input impedance if the LNA is given by

$$Z_i(\omega) = \frac{Z_f(\omega)}{1 + A_v(\omega)}. \tag{26}$$

It can be seen from equation (26), that $Z_i(\omega)$ is proportional to the feedback impedance and inversely proportional to the open-loop gain of the input stage. The input referred current gain of the LNA is given by

$$i_{neq}^2 = i_n^2 + \frac{4kT}{R_f} + \frac{v_n^2}{R_f^2}. \tag{27}$$

From equation (26), it can be seen that the feedback resistor and the gain can be chosen such that the input impedance is low and close to the desired 50 Ω . However, from equation (27), the input-referred current noise is minimized when R_f is large. To achieve the desired match and reasonable NF, a feedback resistance of 170 Ω was

chosen.

The third stage consists of another CE amplification stage, Q3 with shunt peaking provided by an inductor L1 and resistor R4 at the collector node as well as emitter degeneration provided by resistor R5 to further increase bandwidth.

Further details on gain control and input match tuning mechanisms are shown in Figure 44. Specifically, gain control is achieved by controlling the gate voltage (V_Gate) of the pFET device M1. This V_Gate voltage applied to the gate of the M1 is used to adjust the collector current through Q1 and thereby control the gain. Input match (S_{11}) tuning is achieved using capacitive degeneration. As seen in Figure , the capacitive load is generated by a capacitor C1 in series with a varactor C2. Applying a bias voltage to the varactor changes the impedance and shifts S_{11}. This mechanism can be used to fine tune the input matching for matching-sensitive applications.

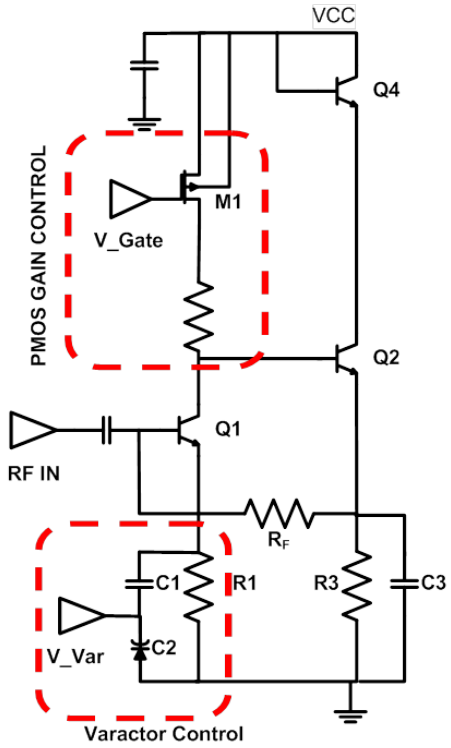


Figure 44: Schematic of the input stage of the reconfigurable UWB LNA.

3.2.2 Measured Results

The SiGeUWB LNA was implemented in a six-layer metal, 0.18 μm, 120 GHz SiGe BiCMOS platform. The chip area is approximately 1.06 x 0.09 mm^2 including pads. A micrograph of the circuit is shown in Figure 45. The LNA was tested was tested using a HP 8510C Network Analyzer, along with 50 GHz cables and probes. The SiGe LNA operates from a 3.3 V supply. The measured current drawn by the LNA was 35.2 mA, resulting in a total power consumption of 116 mW.

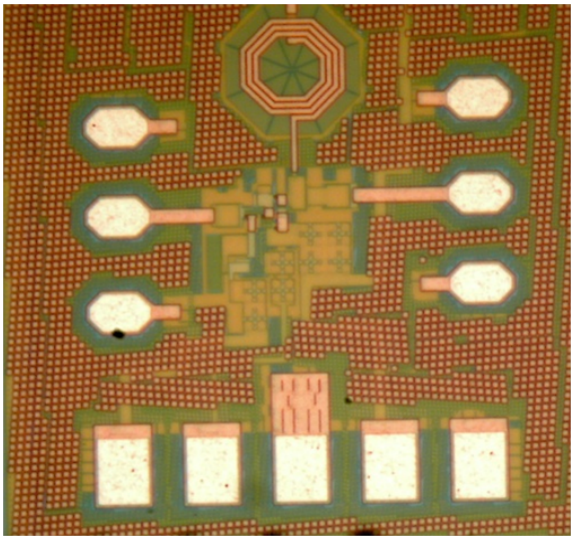


Figure 45: Die micrograph of the reconfigurable UWB LNA.

The S-parameters of the LNA were measured using an Agilent power network analyzer (PNA) along with 50 GHz cables and probes. The measured, nominal S-parameters of the UWB LNA with the control voltages V_Gate and V_var both set to 0 V are shown in Figure 46 . The gain of the LNA is 16.2 dB at 3 GHz and 16 dB at 20 GHz. The LNA demonstrates a maximum gain of 21.3 dB at 5 GHz and a mid-band gain of 19.1 dB at 11 GHz. The 3 dB bandwidth is 12.4 GHz from 3.4–15.8 GHz.

The LNA is well-matched over the frequency range of interest. The input return loss, S_{11}, is less than -10 dB from 5–20 GHz. The input return loss is best matched at 13.4 GHz. The output return loss, S_{22}, is less than -10 dB from 5.0–14.5 GHz and

is -8 dB at 20 GHz. S_{22} is best matched at 5.9 GHz. S_{11} and S_{22} are both less than -4 dB from 3–5 GHz.

The gain control feature of the LNA is illustrated in Figure 47, which shows the step-wise decrease in the gain of the LNA with V_Gate voltage from 0.5–2.5 V. The LNA achieves a very wide gain control tuning range. The gain of the LNA can also be adjusted by varying the V_Var voltage. Figure 48 shows the decrease in gain with the increase in V_Var from 0.5–2.5 V. The gain variation from V_Var is smaller than that for V_Gate, V_Var can be used to make finer adjustments in gain, as needed. However, use of V_Var has a greater impact on the input return loss. Figure 49 plots S_{11} with V_Var voltage ranging from 0-2.5 V. The input match can be moved approximately 3 GHz from 13–10 GHz with V_var set from 0–2.5 V. This demonstrates that the present LNA can be used to adjust the input match to mitigate potential changes as a result of process variation or for dynamic adjustments that may be required based on the specific application or operating environment.

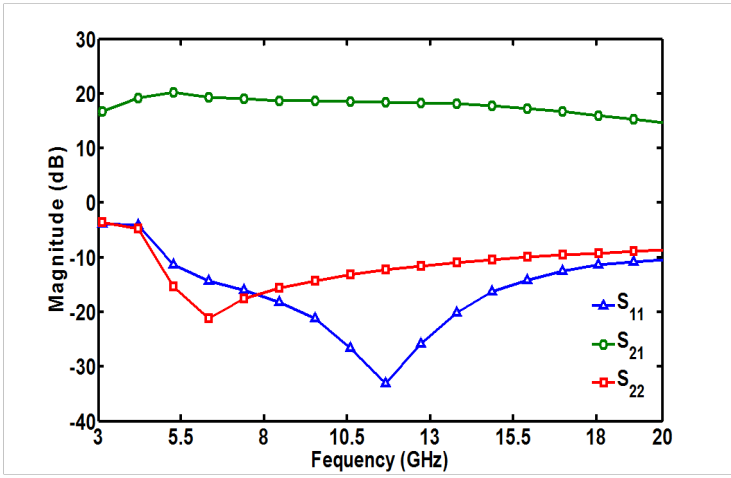


Figure 46: Measured nominal S-parameters of the UWB LNA.

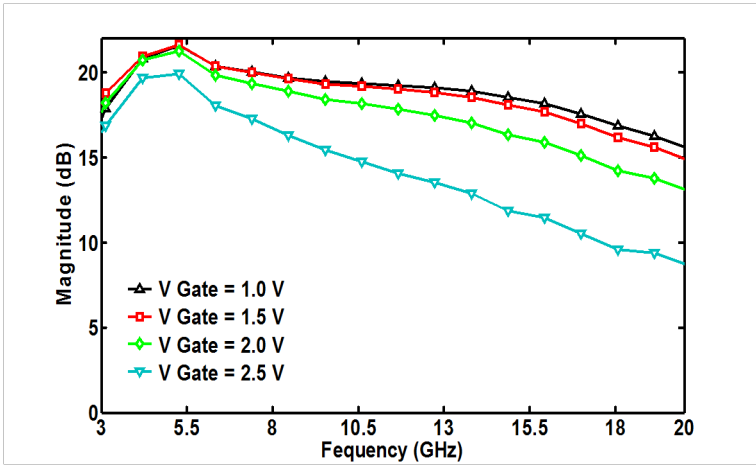


Figure 47: Measured gain with V_{Gate} voltage varying.

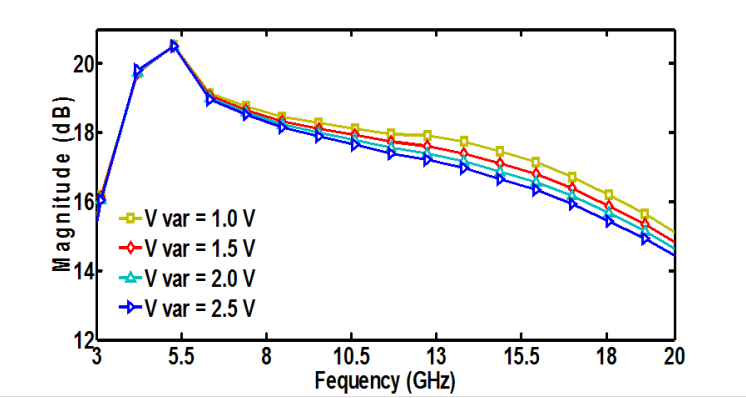


Figure 48: Measured gain with V_{var} voltage varying.

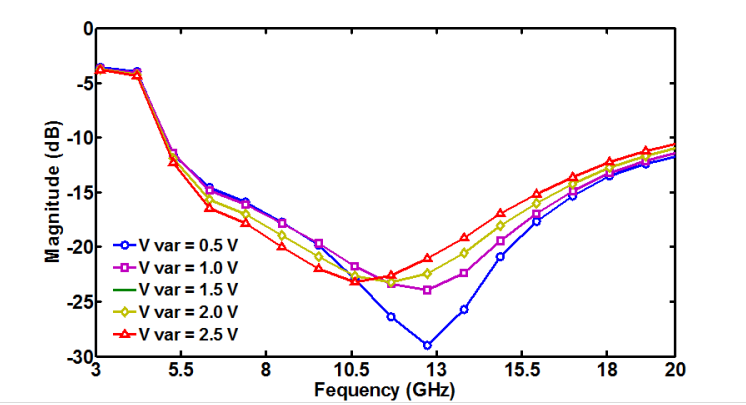


Figure 49: Measured S_{11} with V_{var} voltage varying.

The NF and minimum noise figure (NF_{min}) are plotted in Figure 50 for a frequency range of 8–18 GHz. This frequency range was chosen because it falls within the capabilities of the noise measurement equipment. The measured NF ranges from a minimum of 4.24 dB at 13 GHz to 5.19 dB at 8 GHz and 18 GHz. Also plotted is NF_{min}, which ranges from 4.07 to 4.64 dB, indicating that the LNA is reasonably well noise-matched over the 8–18 GHz frequency band. The linearity (OIP3) of the LNA was also measured. Pout vs. Pin is shown in Figure 51, with an OIP3 of 9.15 dB achieved for an input power of -6.47 dB.

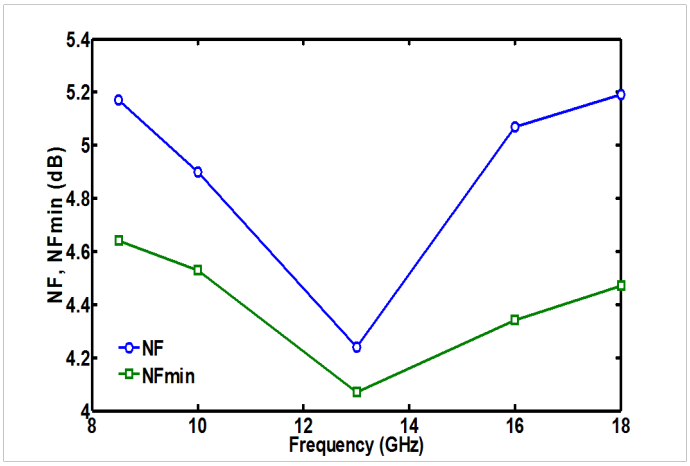


Figure 50: Measured NF and simulated NF_{min} of the SiGe LNA.

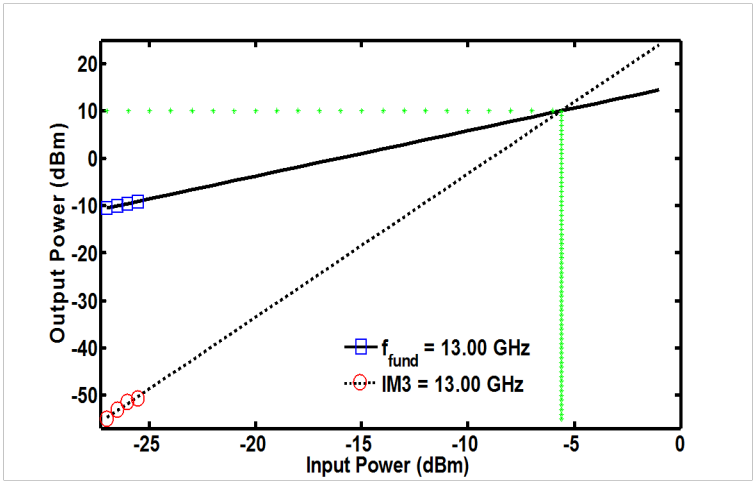


Figure 51: P_{out} vs. P_{in} data for the SiGe LNA.

3.2.3 Summary

A wideband, low power SiGe LNA. The LNA demonstrates a bandwidth of 17 GHz and has a maximum gain of 21.3 dB and a 3 dB bandwidth from 5–17 GHz. The noise figure ranges from 4.2–5.2 dB across the 8–18 GHz band. The LNA consumes 116 mW from a 3.3 V supply. The LNA utilizes novel techniques for gain control and incorporates a means for adjusting the input match that can be used to mitigate for the effects of process variation. This LNA can be used in both X- and C-band applications. The LNA was designed in a commercially-available 0.18 μm SiGe BiCMOS process.

3.3 A SiGe LNA with Mitigating Capability for Radiation-induced Performance Degradation

This work demonstrates for the first time, the efficacy of using performance tuning via circuit tuning-knob adjustments in space-based RF circuits by investigating the proton tolerance of a SiGe, two-stage, wideband (8-16 GHz) LNA. This study shows that radiation-induced changes can affect RF circuit metrics including gain, noise figure, and linearity, but this degradation can be corrected using our proposed performance tuning approach. The LNA presented here was designed using a commercially available 180 nm SiGe BiCMOS technology platform.

3.3.1 LNA Design

The SiGe wideband LNA, was designed to cover an 8–16 GHz band, incorporate circuit tuning knobs, and consume low power. The amplifier, shown in Figure 52, is a two stage design; the first stage is a cascode amplification stage consisting of devices Q1 and Q2, with an output emitter-follower buffer Q4. The LNA operates from a rail voltage of 4.0 V and a nominal cascode and buffer bias current of 4 mA and 5 mA respectively.

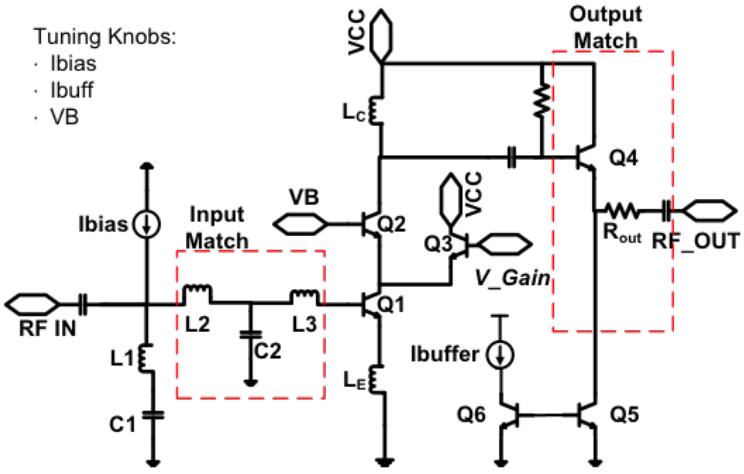


Figure 52: Schematic of SiGe LNA.

The sizing and biasing of the devices in the cascode stage follows the traditional simultaneous matching methodology that has been described in [76]. The nominal cascode bias current was chosen by sweeping the gain and NF_{min} over collector current density (J_C). The value of J_C chosen was based on a compromise between maximum gain and NF_{min}. This choice corresponds to the 4 mA nominal bias current chosen. The device size of Q1 was chosen to bring the optimal noise resistance ($R_{S,opt}$) close to 50 Ω, simplifying input and noise matching by simultaneously matching both. The input impedance of the cascode stage (Z_{in}) with emitter degeneration L_E is given by

$$Z_{in} = \omega_0 L_E + \frac{1}{\omega_0 C_\pi} + \frac{g_m}{C_\pi} L_E, \tag{28}$$

where C_π is the equivalent parasitic base emitter capacitance of the device, g_m is the device transconductance, and ω_0 is the center frequency [52].

The bandwidth of the input section is a function of the quality factor (Q_{in}) of the input network. The relationship between bandwidth (BW) and and the center frequency, is given by,

$$BW = \frac{\omega_0}{Q_{in}}. \tag{29}$$

Additionally the quality factor of the input network given by,

$$Q_{in} = \frac{1}{\omega_0 C_\pi R_S} = \frac{1}{\omega_0 C_\pi R_S (R_S + g_m L_E / C_\pi)}. \tag{30}$$

It can be seen from equation (30) that Q_{in} is inversely proportional to C_π, L_E and the source resistance, R_S. This means that by increasing or by adding additional capacitance to we can increase the input matching bandwidth.

With appropriate biasing, the g_m of the Q4 device can be set to 20 mS, which corresponds to an emitter resistance of 50 Ω for a broadband match across the band of interest. However, as a result of limitations associated with biasing Q4 at 20 mS, including a reduction in linearity, an output resistor R_{out} has been added series to the emitter resistance of Q4 for output matching to 50 Ω. The wideband LNA also incorporates gain control functionality provided by Q3. The gain of the LNA is reduced by increasing the V_Gain voltage, thereby turning on Q3, which steals current away from the common base amplifier. Additionally, the linearity of the LNA is enhanced with the inclusion of the L1-C1 second harmonic impedance termination [4].

3.3.2 Performance Tuning Methodology

Specific bias voltages and currents were identified as tuning knobs to adjust the LNA performance. These knobs were identified as the cascode current bias (Ibias), cascode upper base bias (VB), and the buffer bias (Ibuffer). They are used to control and to regain lost performance in gain, NF, and linearity. The knobs were chosen based on their effect on specific RF performance metrics and for their relative independent action on individual performance metrics. For example, it would be highly undesirable for the Ibuffer control for linearity to greatly affect the LNA gain. In addition, the tuning range of each knob was selected based on its effectiveness of tuning the parameter of interest. It was determined that for each parameter, there should a

primary and/or secondary tuning knob based on the effect of that tuning knob on the metric of interest: the primary knob is used first to attempt to tune the performance. If this knob fails to bring the LNA performance back into specification, the secondary tuning knob is then used. The secondary tuning knob has an effect on more than one parameter, so its tuning range is restricted. For example, VB is used as a secondary tuning knob for both gain and output third-order intercept point (OIP3) because small changes in VB affect more than one parameter.

The measurement set up for the performance tuning system is shown in Figure 53. The LNA is biased by DC power supplies and receives a two-tone RF signal. The RF signal is amplified by the LNA, mixed down to an intermediate frequency (IF), and then processed by a spectrum analyzer. This arrangement allows for the performance of the LNA to be analyzed and tuned using a control algorithm.

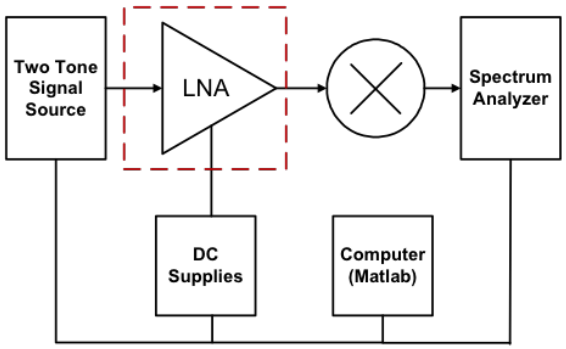


Figure 53: Measurement setup for performance tuning.

The two-tone signal source enables the measurement of both gain and OIP3; to measure gain, the signal source is set to a known power level, and the gain of the LNA is measured as the difference between the amplitude of the signal source and the amplitude of the signal to the spectrum analyzer. The OIP3 is measured by supplying two signals of a specified amplitude and frequency spacing to the LNA. Once the signal is amplified by the LNA and mixer, the inter modulation products of the two tone signal at the output of the mixer are measured to determine the third order intercept points. The NF is determined by first measuring the gain of the

LNA using the mechanism that has been described previously and then turning off the signal source. The noise power at the output of the mixer measured using the spectrum analyzer. The input referred noise figure of the system is determined from

$$NF_{dB} = P_{cold} + 174\ dBm/Hz - 10\log(B) - Gain_{dB}, \tag{31}$$

where P_{cold} is the noise power at the output when the input is terminated with 50 Ω, B is the bandwidth over which the noise power is measured, and dBm/Hz is the thermal noise power of an ideal 50 Ω load at 290 K. This permits noise measurement of the system (LNA and mixer). This method of measuring the noise by first measuring gain and then the noise with the RF source powered off is known as the "cold-source noise measurement method and is described in [60]. It is convenient because other approaches for measuring noise require an accurate on chip noise source. The noise source itself is a difficult component to design and would add performance degrading parasitics.

Measurements were conducted at the wafer level with off-chip power supplies, signal sources, and a spectrum analyzer. Digital control was provided by a computer running the tuning algorithm implemented in MATLAB. The algorithm used to tune the LNA is illustrated in Figure 54.

After evaluating the initial LNA performance, the user must then choose the performance metric that is in need of tuning. Only one metric can be tuned at a time and the ranges for each tuning knob must be determined from prior measurements on a test LNA. Once initial measurements are completed, the algorithm determines if the performance metric of interest meets the required specification. If it does, the algorithm terminates and sets the tuning knobs to the default values. However, if the performance metric fails to meet the required specification, the tuning procedure begins by sweeping the value of the primary tuning knob until the desired RF performance is obtained. The secondary tuning knob is then swept if the LNA performance

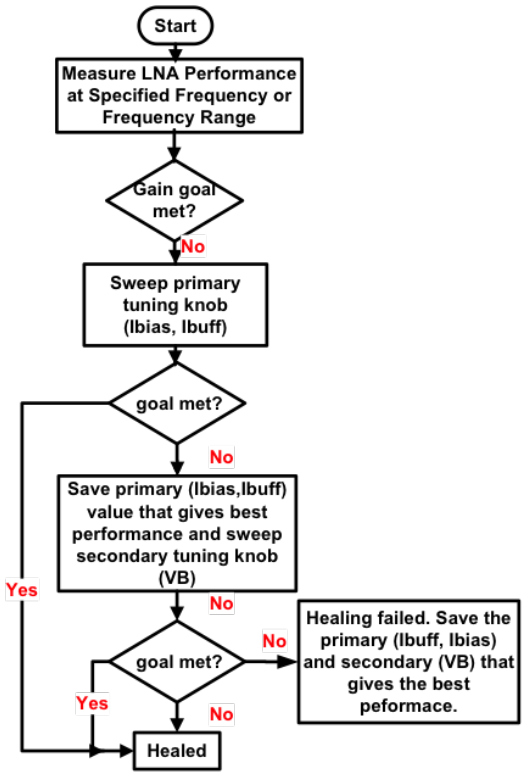


Figure 54: Measurement setup for performance tuning.

has not been tuned. The values of the primary and secondary tuning knobs that bring the RF performance back into specification or the values that result in the best performance, in the case where the LNA is not tuned, are saved.

3.3.3 Measured Results

The SiGe wideband LNA was implemented in a six-metal layer, 180 nm, 150 GHz, SiGe BiCMOS platform. The chip area is approximately 1.3 x 0.9 mm, including pads. A die micrograph of the LNA is shown in Figure 55.

The LNA samples were irradiated with 63.3 MeV protons at the Crocker Nuclear Laboratory at the University of California at Davis. A total of 9 LNA samples were irradiated with 3 samples at each dose. Testing was conducted with proton-equivalent doses ranging from 200 krad(Si) to 2 Mrad(Si). The S-parameters of the pre- and post-irradiated samples were extracted with an Agilent microwave vector network analyzer with 40 GHz cables and probes. All RF measurements were performed

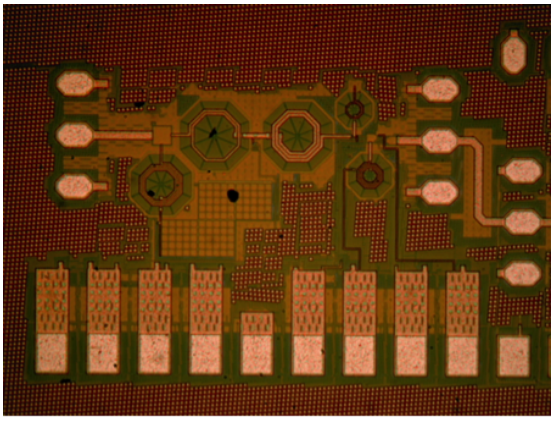


Figure 55: Die micrograph of SiGe LNA.

on-wafer and at room temperature using the measurement test setup previously described. Additionally, the post-irradiated samples were measured soon after exposure to minimize any potential annealing effects.

The SiGe LNA operates from a 4.0 V supply. The nominal measured current draw of the LNA core was 4 mA, and the buffer operates from a 4.0 V supply and draws 5 mA, nominally resulting in a total power consumption of 16.0 mW for the core and 20 mW for the buffer. The measured S-parameters for the LNA at nominal bias are shown in Figure 56. The peak gain is 17.5 dB at 13 GHz. The gain is 6.2 dB at 8 GHz and 3.6 dB at 18 GHz. The input is well matched over the entire frequency range, and the output match is below 10 dB from 10-15 GHz.

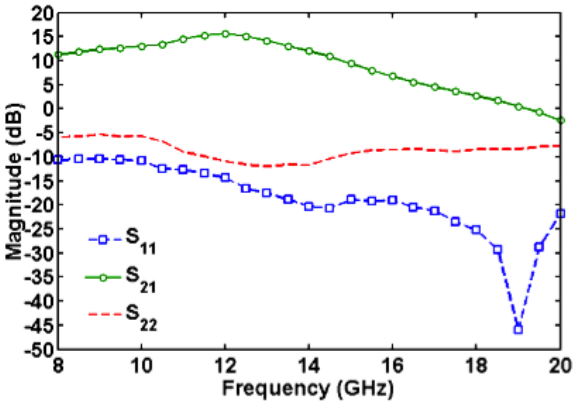


Figure 56: Measured nominal pre-irradiated S-parameters of the LNA.

The LNA incorporates a gain control mechanism. As the V_Gain bias voltage is increased, the RF gain reduces from its nominal value to 0 dB across all frequencies. The slope of S_{21} remains relatively constant for all gain steps, as shown in Figure 57.

The effect of the tuning knobs on gain were also investigated. In particular, the gain of the LNA is affected by the cascode current, Ibias, and the cascode upper base voltage, VB. The effect of ibias on the gain of the LNA vs. frequency is shown in Figure 58. The figure shows that ibias has a modest affect on the LNA gain from 0.5 mA–7.0 mA when VB is set to its nominal value of 3.5 V. However, VB has a strong effect on gain as shown in Figure 59. It shows that VB reduces the gain, to a maximum of 14 dB when VB is 3.0 V and increases the gain to 18.3 dB when VB is 4.0 V while Ibias is set to its nominal value.

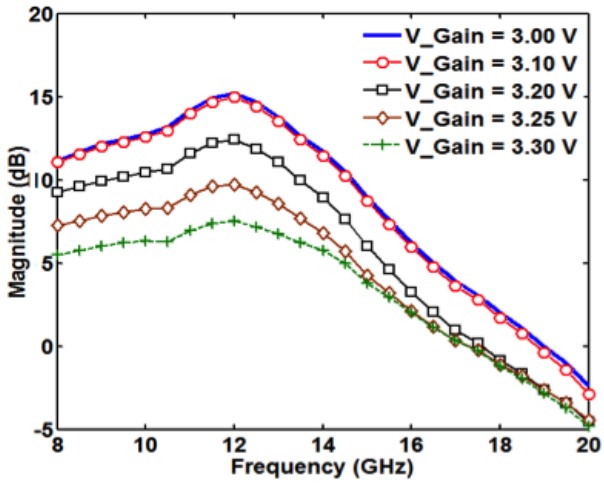


Figure 57: Measured nominal pre-irradiated gain vs. frequency and V_Gain.

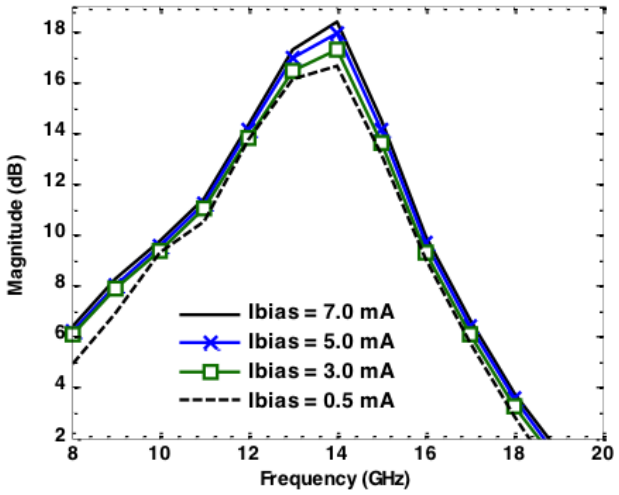


Figure 58: Effect of Ibias on measured pre-irradiated gain.

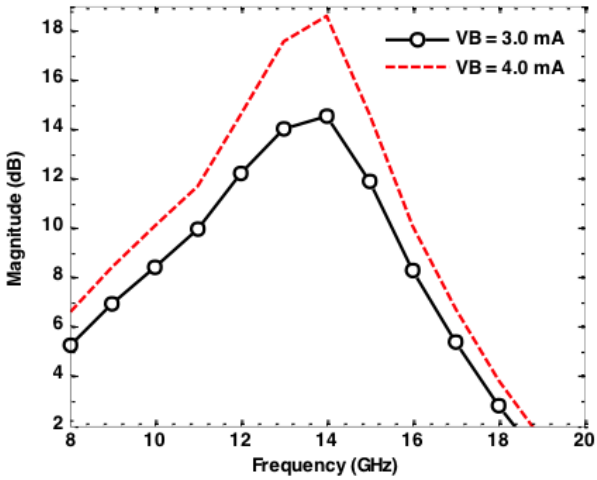


Figure 59: Effect of VB on measured pre-irradiated gain.

The effects of the tuning knobs on the pre-irradiated LNA NF were measured. The plot of NF vs. frequency and ibias is illustrated in Figure 60. This figure shows that there is a strong relationship between NF and Ibias value with the NF increasing with increased bias current. The dependence of NF on VB is shown in Figure 61. There is a strong relationship between VB and NF where the NF increases with decreasing VB voltage. However, the NF also increases once VB is set below 3.0 V.

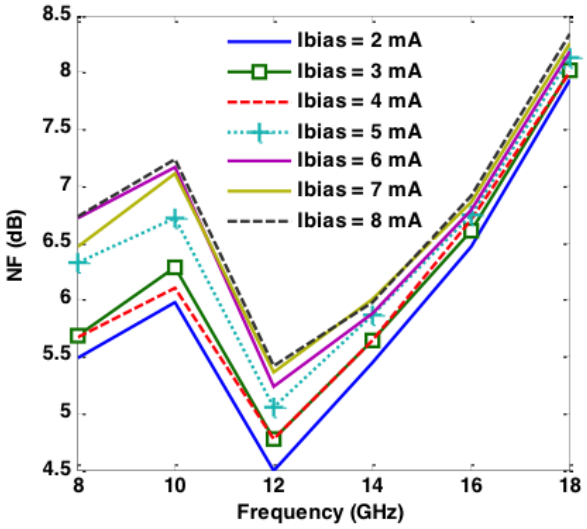


Figure 60: Pre-irradiated NF vs. frequency and Ibias.

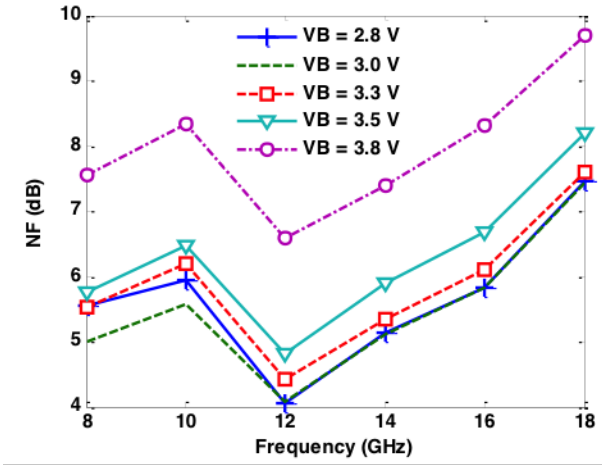


Figure 61: Pre-irradiated NF vs. frequency and VB.

The effect of the tuning knobs on the pre-irradiated OIP3 was also measured. The effect of VB voltage value on the measured OIP3 is shown in Figure 62. OIP3 is strongly dependent on the VB value; increasing VB decreases OIP3 with the best OIP3 measurement across frequency occurring when VB is set to 3.5 V. The effect of Ibuffer on OIP3 is shown in Figure 63, where the OIP3 has the best values across frequency when Ibuffer ranges from 3 mA–5 mA.

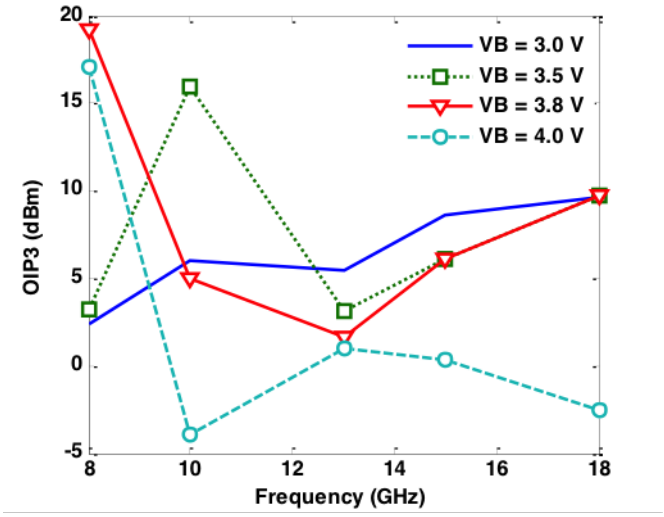


Figure 62: Pre-irradiated OIP3 vs. frequency and VB .

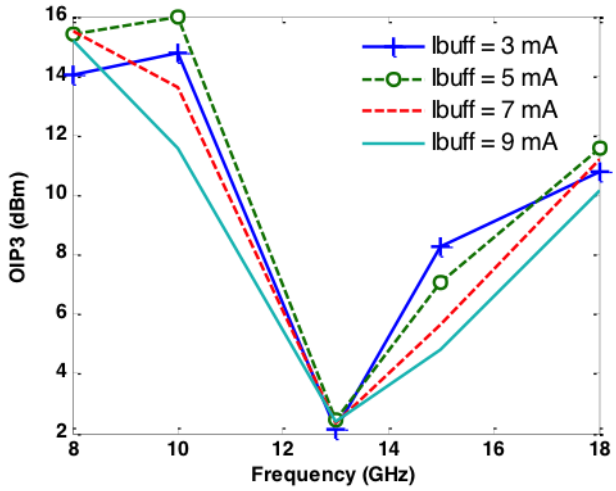


Figure 63: Pre-irradiated OIP3 vs. frequency and Ibuffer.

The nominal pre-irradiated LNA performance occurred with Ibias, Ibuffer and VB set to 4 mA, 5 mA, and 3.5 V, respectively. Specifically, it was found that VB has an effect on OIP3, gain and NF; increasing VB improves gain and to a lesser extent, improves OIP3 but can have a negative effect on other metrics such as NF in the pre-irradiated sample. The Ibuffer tuning knob has a strong effect on OIP3; increasing the Ibuffer current improves OIP3, but Ibuffer has a minimal impact on

other metrics. Finally, Ibias affects gain and NF but has a minimal impact on other metrics. The tuning knob ranges and target specifications determined from initial measurements are shown in Tables 3 and 4 respectively.

Table 3: Maximum Control Knob Ranges

Parameter	Min.	Nom.	Max
Ibias (mA)	2	4	8
Ibuffer (mA)	2	5	8
VB (V)	3.3	3.5	3.6

Table 4: Target Specifications

Gain (dB) 13 GHz	OIP3 (dBm) 13 GHz	NF (dB) 14 GHz	NF (dB) 16 GHz
17.5	2.43	5.6	6.7

The pre- and post-irradiated results for gain, NF, and OIP3 for the LNA samples verses the relevant tuning knob is shown in Figures 64–66. The pre- and post-irradiated LNA gain vs. VB is shown in Figure 64. The figure shows that there is degradation in the LNA pre-radiated gain value of 17.5 dB at 13 GHz with VB set to 3.5 V. The sample exposed to 200 krad shows the most degradation. From initial measurements illustrated in Figure 64, it was determined that VB had the strongest impact on gain. Using the MATLAB algorithm, to achieve a gain value above the 17.5 dB goal VB was set to 3.6 V for the samples exposed to 500 krad and 2 Mrad. The algorithm was not able to tune VB to achieve the gain goal for the 200 krad sample. However, by setting VB to 3.8 V, the 200 krad sample achieves a maximum gain of 17.1 dB.

The pre- and post-irradiated LNA NF vs. Ibias. appears in Figure 65. The figure shows that there is degradation in the LNA pre-radiated NF value with the

post-irradiated NF measuring 5.64 dB at 14 GHz with Ibias set to 4 mA. The sample exposed to 500 krad shows the most degradation. The algorithm is used to achieve a NF value above the 5.64 dB goal. Ibias was set to 3.5 mA in the 200 krad sample and achieves a NF of 5.64 dB. For the 500 krad sample, Ibias was set to 3 mA to achieve a NF of 5.6 dB and for the 2 Mrad sample Ibias was set to 3.5 mA for a NF value of 5.55 dB.

The pre- and post-irradiated OIP3 vs. Ibuffer is shown in Figure 66. The figure shows that there is degradation in the LNA pre-radiated OIP3 value of 2.43 dBm at 13 GHz with Ibuffer set to 5 mA. The sample exposed to 2 Mrad shows the most degradation in this case. The MATLAB algorithm is used to achieve an OIP3 value above the 2.43 dBm goal. Ibuffer was set to 4 mA in the 200 krad sample and achieves an OIP3 2.42 dBm, within 0.01 dBm of the required goal value. For the 500 krad sample, Ibuffer was set to 4.5 mA to achieve an OIP3 of 2.44 dBm. Finally, for the 2 Mrad sample, Ibias was set to 6.5 mA to achieve an OIP3 value of 2.48 dBm.

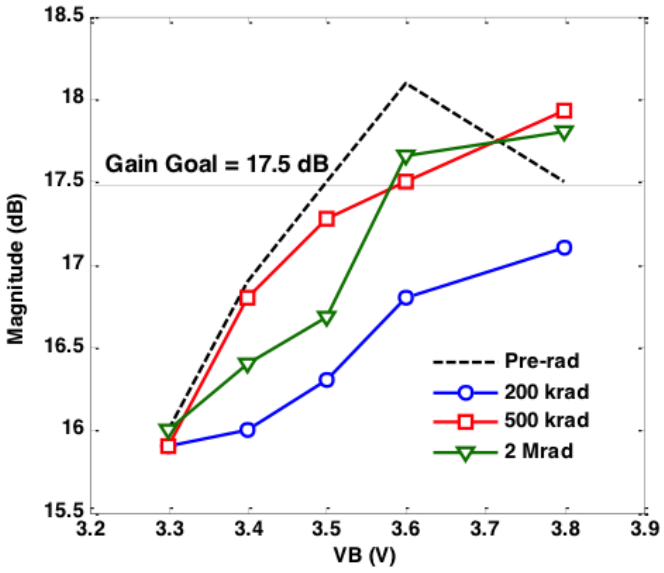


Figure 64: LNA pre- and post-irradiated gain vs. VB.

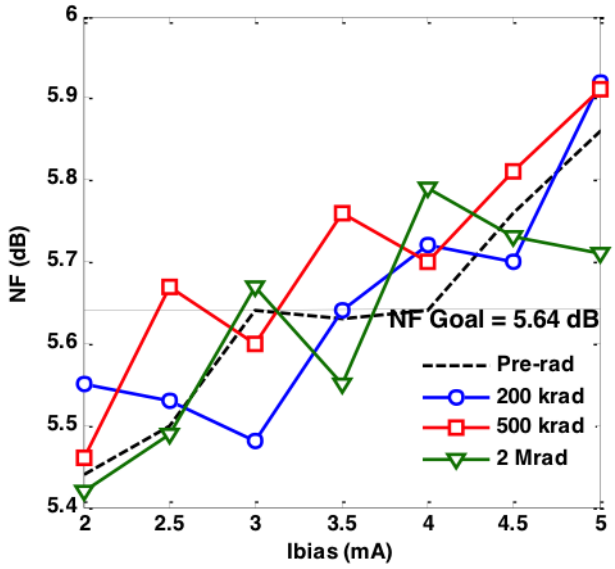


Figure 65: LNA pre- and post-irradiated NF vs. Ibias.

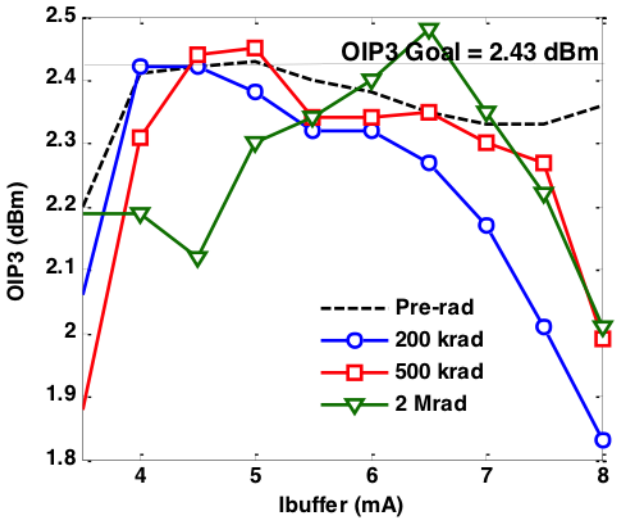


Figure 66: LNA pre- and post-irradiated OIP3 vs. Ibuffer.

A summary of measured results at 13 GHz, 14 GHz, and 16 GHz are shown in Tables 5–8. The tables list the pre- and post-irradiated measured performance values for each die, at each of the three TID values (200 krad, 500 krad, 2 Mrad). In addition, the mean values and standard deviation for each performance metric at

each TID point are listed.

The post-irradiated performance of the LNA shows degradation to gain, NF, and OIP3 performance from proton exposure. The measured pre- and post-tuned gain and OIP3 at 13 GHz of the LNA for each of the three TID points are shown in Tables 5–7. Shown in Table 5 are the results for a TID exposure of 200 krad. The LNA gain degrades, with the lowest measured value being 16.3 dB. The OIP3 however, is not impacted and no tuning is required. The algorithm was able to improve the gain in all cases and restores the gain to its pre-irradiated value in two out of three samples. Shown in Table 6 are the measured results for samples irradiated to 500 krad. The samples suffered degradation in both gain and OIP3. The lowest measured pre-tuned gain was 17.17 dB and the lowest pre tuned OIP3 was 2.05 dBm. The algorithm was able to restore the gain to its pre-irradiated value or greater in all cases. The OIP3 was improved to within 0.01 dBm of the pre-irritated value in two out of three cases. The gain and OIP3 for samples irradiated to 2 Mrad is shown in Table 7. The lowest measured pre-tuned gain was 16.1 dB and the lowest measured pre-tuned OIP3 was 2.19 dBm. The gain was increased in all cases but was improved above the pre-irradiated value in only one sample. The OIP3 was improved above the pre-irradiated value in all but one of the samples. The demonstrated performance tuning of gain and OIP3 was achieved with a tuning range of VB from 3.5 V–3.8 V and a tuning rage of Ibuffer of 4 mA–6.5 mA.

The overall pre-tuned gain for all TID exposures at 13 GHz ranges from 16.1–17.5 dB, with a standard deviation ranging from 0.18–0.52 dB. The average pre-tuned OIP3 ranges from 2.05–2.74 dBm with a standard deviation ranging from 0.13–0.35 dBm. The gain and OIP3 were tuned with small adjustments to VB and Ibuffer respectively.

The measured pre- and post-tuned NF at 14 GHz and 16 GHz of the LNA for each of the three TID points are shown in Tables 8–10. Shown in Table 8 are the

measured results for a TID exposure of 200 krad. The LNA NF degrades, with its highest measured pre-tuned value of 5.7 dB at 14 GHz. The NF degradation at 16 GHz is more severe with the highest measured pre-tuned value of 9.7 dB. The algorithm was able to improve the measured NF by utilizing Ibias as a tuning knob. In all of the samples measured at 14 GHz, the algorithm was able to tune Ibias to achieve a NF value equivalent or better than the pre-irradiated value. The NF of the samples measured at 16 GHz was improved for all samples. However, the three die could not be restored to their pre-irritated value of 6.7 dB.

A similar trend is observed for the samples irritated to 500 krad. The measured results of Table 9 show that the pre-tuned NF at 14 GHz degrades with the worst measured NF of 5.7 dB. The algorithm is able to improve the NF of all samples to the pre-irradiated value or better. The pre-tuned NF measured at 16 GHz could not be restored to the pre-irradiated value but Ibias was used to improve the NF in all three samples at 16 GHz. The NF results for the samples irradiated at 2 Mrad are show in Table 10. The measured pre-tuned NF at 14 GHz showed degradation and was restored to the pre-irradiated value or better by tuning Ibias. The NF measured at 16 GHz could not be restored to the pre-irradiated value but was improved in all cases by tuning Ibias.

In summary, the NF at 13 GHz, of the LNA degrades modestly across all radiation exposures from its 5.64 dB nominal value. The average pre-tuned NF ranges from 5.52–5.79 dB, with a standard deviation ranging from 0.04–0.14 dB for the three samples. The degradation of NF at 16 GHz is more significant; the average pre-tuned NF ranges from 9.48–9.87 dB,with a standard deviation ranging from 0.09–0.13 dB for the three samples. The demonstrated performance tuning of NF achieved with a tuning range of Ibias from 3 mA–3.5 mA.

Table 5: Pre- and Post-tuned Gain and OIP3 for Three Dies at 200 krad, 13 GHz

Rad. Dose	200 krad (Si)									
	Nominal					Tuned				
Die	1	2	3	Mean	Std. dev.	1	2	3	Mean	Std. dev.
Gain (dB)	16.3	16.81	17.34	16.82	0.52	17.1	17.61	17.98	17.56	0.44
OIP3 (dBm)	2.42	2.67	2.53	2.54	0.13	2.42	2.67	2.53	2.54	0.13

Table 6: Pre- and Post-tuned Gain and OIP3 for Three Dies at 500 krad, 13 GHz

Rad. Dose	500 krad (Si)									
	Nominal					Tuned				
Die	1	2	3	Mean	Std. dev.	1	2	3	Mean	Std. dev.
Gain (dB)	17.28	17.5	17.17	17.3	0.18	17.93	17.52	17.74	17.7	0.21
OIP3 (dBm)	2.05	2.31	2.74	2.37	0.35	2.09	2.42	2.74	2.42	0.33

Table 7: Pre- and Post-tuned Gain and OIP3 for Three Dies at 2 Mrad, 13 GHz

Rad. Dose	2 Mrad (Si)									
	Nominal					Tuned				
Die	1	2	3	Mean	Std. dev.	1	2	3	Mean	Std. dev.
Gain (dB)	16.1	16.68	16.47	16.42	0.29	17.08	17.66	17.46	17.4	0.29
OIP3 (dBm)	2.19	2.68	2.34	2.40	0.25	2.48	2.58	2.4	2.49	0.09

Table 8: Pre- and Post-tuned NF for Three Dies at 200 krad at 14 and 16 GHz

Rad. Dose	200 krad (Si)									
	Nominal					Tuned				
Die	1	2	3	Mean	Std. dev.	1	2	3	Mean	Std. dev.
NF (dB) 14 GHz	5.72	5.73	5.66	5.70	0.04	5.64	5.63	5.64	5.64	0.01
NF (dB) 16 GHz	9.58	9.48	9.7	9.59	0.11	8.89	8.76	8.81	8.82	0.07

Table 9: Pre- and Post-tuned NF for Three Dies at 500 krad at 14 and 16 GHz

Rad. Dose	500 krad (Si)									
	Nominal					Tuned				
Die	1	2	3	Mean	Std. dev.	1	2	3	Mean	Std. dev.
NF (dB) 14 GHz	5.55	5.64	5.7	5.63	0.08	5.55	5.64	5.46	5.55	0.09
NF (dB) 16 GHz	9.62	9.65	9.49	9.59	0.09	8.93	9.13	9.11	9.06	0.11

Table 10: Pre- and Post-tuned NF for Three Dies at 2 Mrad at 14 and 16 GHz

Rad. Dose	2 Mrad (Si)									
	Nominal					Tuned				
Die	1	2	3	Mean	Std. dev.	1	2	3	Mean	Std. dev.
NF (dB) 14 GHz	5.52	5.68	5.79	5.66	0.14	5.52	5.62	5.55	5.56	0.05
NF (dB) 16 GHz	9.87	9.72	9.61	9.73	0.13	8.96	9.07	9.23	9.09	0.14

3.3.4 Summary

A 8–16 GHz UWB SiGe LNA is presented. The LNA features low power and low noise performance competitive with other state-of-the-art LNAs operating in this band. The SiGe LNA was designed in a commercially-available 180 nm SiGe technology platform and was designed to cover the 8–16 GHz frequency band. The LNA design incorporates performance tuning knobs for post-irradiation tuning of the key RF metrics. The performance of the LNA tuning knobs were evaluated with radiation proton-equivalent doses ranging from 200 krad(Si) to 2 Mrad(Si). The data demonstrate that it is possible to restore the LNA performance using a tuning algorithm.

CHAPTER IV

SELF-HEALING MICROWAVE SYSTEMS WITH RECONFIGURABLE LOW NOISE AMPLIFIERS

4.1 Introduction

Building upon the results of the previous studies of tunable and wideband circuit components, the next step is to integrate these components to form wideband reconfigurable and"self-healing" systems. The presented work investigates an 8–18 GHz SiGe reconfigurable RF receiver. The receiver incorporates on-chip test signals to provide a reference RF signal to enable on-chip testing, sensors to measure RF performance, and tuning knobs in the form of adjustable biases to tune circuit performance back into specification to mitigate the effects of PVT and radiation.

4.2 A SiGe Receiver with On-chip BIST Capability for Self-healing

This work presents a wideband (8–18 GHz) self-healing receiver in SiGe technology. The receiver chain consists of a LNA, an image-reject mixer, on-chip, amplitude-locked loop (ALL) signal sources that are used to provide test signals of a predefined amplitude, and control circuitry in the form of DAC and data registers. Both the LNA and the mixer circuit blocks incorporate "tuning knobs" to enable "self-healing" in order to ensure consistent performance and mitigate the negative effects of PVT variations, aging, and damage from extreme environments such as ionizing radiation. A maximum post-healed gain greater than 30 dB, an image rejection ratio (IRR) exceeding 30 dB, OIP3 greater than 8 dBm, and NF less than 9 dB are obtained in measurement. An automated self-healing algorithm is developed and shown to be effective for improving the overall performance of the receiver. The receiver was

fabricated in an 0.18 μm SiGe BiCMOS process with a peak f_T of 150 GHz, and consumes 240–260 mA from a 4 V supply.

The goal of self-healing systems is to incorporate all testing and actuation components on die, including feedback loops, data converters, and digital processing. The MATLAB code and spectrum analysis presented in this work are designed to facilitate its implementation with integrated ASIC and ADC blocks.

4.2.1 System Architecture

The system diagram of the 8–18 GHz receiver configured for self-healing is shown in Figure 67. The system is designed to measure and heal gain, IRR, OIP3, and NF. The receiver consists of an LNA, an image-reject mixer, and ALL signal sources. There are a total of four ALLs in the system: a pair at both the input of the LNA and the input of the mixer. The ALL tones are coupled into the RF path via 37 dB couplers at the input of the LNA and via 22 dB couplers at the input of the mixer. These coupling ratios fulfill system specifications requiring the power at the inputs of the LNA and mixer to be -41 dBm and -26 dBm, respectively. The LNA and mixer incorporate built-in turning knobs in the form of pre-identified current and voltage biases. In addition, the LNA, mixer, and ALLs are all controlled using on-chip digital blocks. The system architecture allows for test signals to be applied independently to the LNA input via ALL1 and ALL2, and to the mixer input via ALL3 and ALL4. The pair of ALLs at the input of the LNA and mixer allow for gain and linearity of the system to be measured independently from either the input of the LNA or mixer. Self-healing is accomplished by putting the receiver into an automated healing loop mode.

During the healing process, RF test signals are provided by the on-chip ALL sources. The local oscillator (LO) signal to the mixer is provided by an external source, and the frequency of the source is adjusted so that the IF mixer output is 1.9

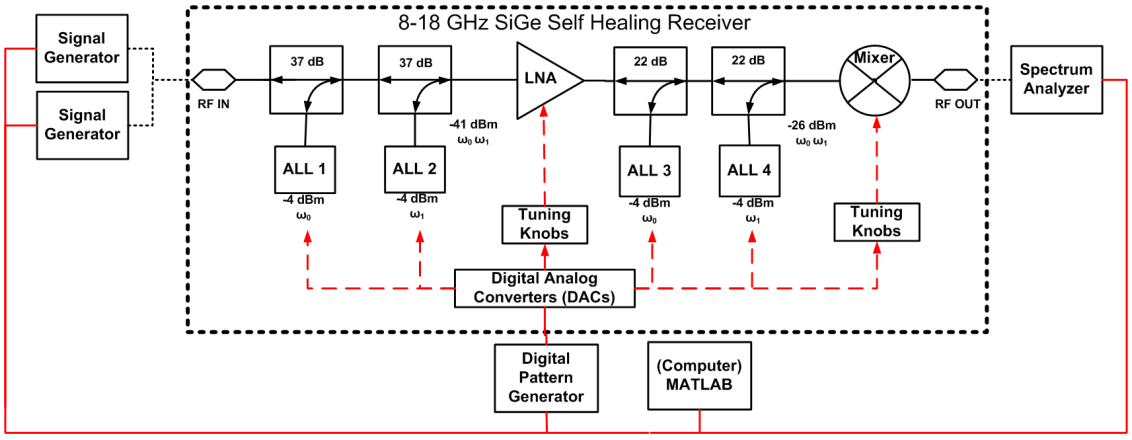


Figure 67: System diagram of the 8–18 GHz SiGe self-healing receiver showing RF and digital control blocks, along with off-chip components used in measurement.

GHz for all input RF frequencies. The IF output is used to ascertain the performance of the receiver and is measured by a spectrum analyzer. NF measurements and healing are accomplished by terminating the receiver input with a 50 Ω load and using the spectrum analyzer to measure the noise power at the output. Upon the completion of healing, the system performance is verified using external RF sources. All of the instruments are controlled through GPIB with the MATLAB healing program running on a computer.

A schematic of the LNA used in the receiver is shown in Figure 68. The LNA is a two stage design; the first stage, Q1 and Q2, is a cascode and the second stage is an output emitter-follower buffer Q4. The nominal cascode bias current was chosen by sweeping the gain and minimum noise figure (NF_{min}) over the collector current density, J_C. The chosen J_C optimizes between maximum gain and minimum NF_{min}. The device sizes of Q1 and Q2 were chosen to bring the optimal noise resistance (R_{Sopt}) close to 50 Ω, simplifying input and noise matching by simultaneously matching both. This is called the simultaneous matching technique and is described in [76]. The cascode bias current, Ibias, the base voltage of $Q2$, V_B, and the buffer current Ibuffer, were used as LNA tuning knobs. The tuning knobs were chosen to have a strong effect on one parameter while having a minimal effect on others; the Ibias tuning

knob tunes gain and NF, V_B tunes linearity and gain, and Ibuffer tunes linearity. A detailed analysis of the effects of these tuning knobs on the LNA performance can be found in [32].

The image-reject mixer used in the receiver is shown in Figure 69. It consists of a quadrature down-conversion stage, two variable gain amplifiers (VGAs) in the in-phase and quadrature (I and Q) paths, a two-stage polyphase filter for image rejection, a three-stage polyphase filter for quadrature signal generation, and another VGA at the output. The mixer is based on the Hartley architecture but uses passive R-C polyphase filters in place of a RC-CR network. Quadrature downconversion is accomplished using a micromixer. The VGAs in the quadrature paths serve the dual purpose of increasing the overall gain and canceling out I-Q imbalances by providing a gain offset. This mixer utilizes various tuning elements, enabling adjustment of its key performance parameters. The IRR of the mixer is tuned by adjusting the VGAs gain of the I and Q paths by making differential adjustments in the biases of the VGAs (ibiasVGAl-ibiasVGA2). The mixer gain is controlled using the bias current of VGA3 (ibiasVGA3). Further details on the mixer design are given in [66].

The schematic of the ALL test signal source is shown in Figure 70, and consists of a three-stage differential ring oscillator, frequency divider, multiplexer, variable-gain amplifier (VGA), and peak detector.The primary oscillation frequencies are generated using a three-stage differential ring oscillator that is capable of generating frequencies between 16–20 GHz. Each stage consists of an emitter-coupled-logic (ECL) inverter with an emitter-follower buffer to maintain signal levels. A frequency divider divides this oscillator signal by the appropriate amount to produce frequencies from 8–10 GHz. The outputs of the divider, as well as the core ring oscillator, are fed into a multiplexer that enables band-select functionality. Frequency tuning is achieved by varying the tail current of the emitter-follower within each delay cell. Changing the tail current changes the capacitance at the output node of each delay cell, which tunes

the delay. To ensure a fixed power level for the signal source across the frequency bands of interest, the amplitude locking is automated using a closed loop consisting of a VGA, a peak detector, and an op-amp. The VGA topology consists of a double-balanced Gilbert cell. Further details on the ALL design can be found in [71].

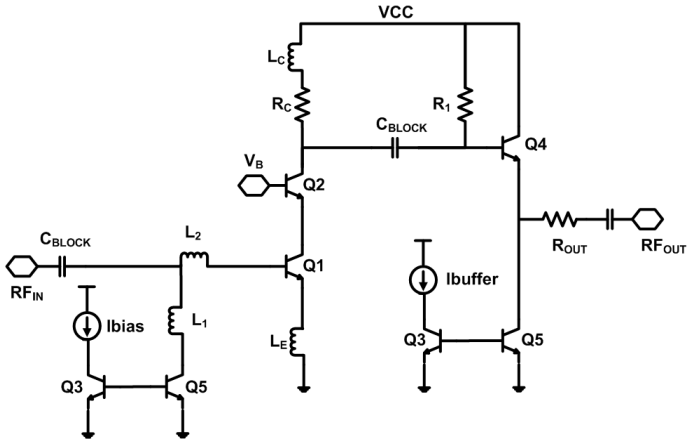


Figure 68: 8–18 GHz tunable SiGe LNA used in the receiver.

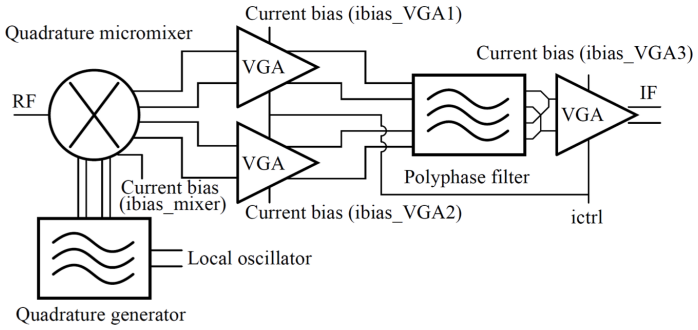


Figure 69: 8–18 GHz tunable SiGe image reject mixer (after [66]).

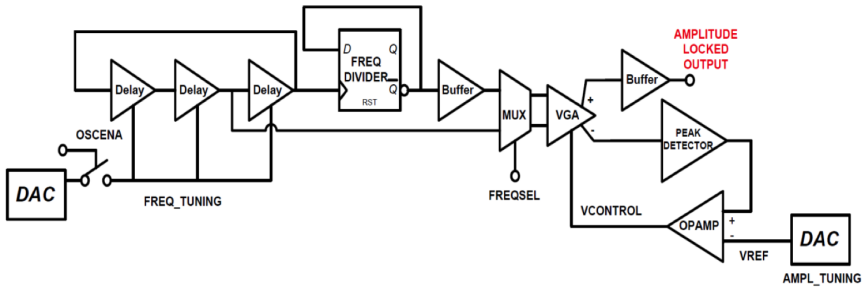


Figure 70: Amplitude Locked Loop (ALL) on-chip test signal source (after [71]).

On-chip, DACs, provide digital control for all of the biases and tuning knobs of the RF blocks. The voltage and current DACs are based on an 8-bit, resistor bridge topology with a thermometer decoder on the front-end. The voltage DAC has a linear output voltage range from 1.1 V to 3.7 V, and the current DAC has a linear output current range from 1.5 mA to 9 mA. Both DACs use an exponentially compensated, temperature stable BGR as their voltage reference. Further details of the DAC and BGR design can be found in [21].

4.2.2 Self-healing Methodology

The main steps of the healing algorithm are shown in Figure 71. The process begins with an initial measurement of the system performance (gain, IRR, OIP3, and NF) using input signal sources ALL1 and ALL2, followed by external sources that are used as signal inputs for verification purposes and are not used during the healing process. The spectrum analyzer is used to the output IF signal of the receiver.

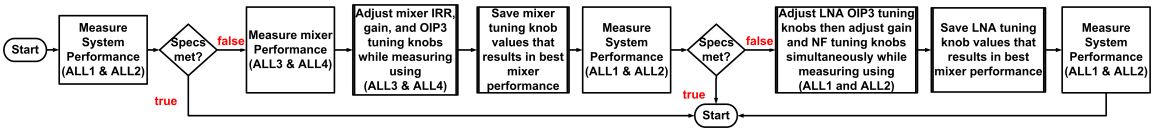


Figure 71: Self-healing algorithm used to tune receiver performance.

Measurement of gain involves feeding in an RF signal of known frequency and amplitude and measuring the corresponding IF power at the output using the spectrum analyzer. To measure IRR, the input signal frequency is changed to the image frequency and gain corresponding to the image is measured. The ratio of gain numbers corresponding to RF and image signals gives the IRR. Measuring the OIP3 requires activation of two ALL sources set to the same power but with a frequency offset ω_0 and ω_1, as shown in Figure 67. The fundamental and third-order tones are measured at the spectrum analyzer and the OIP3 calculated using,

$$OIP3_{dBm} = P_{out} + (P_{out} - P_{out3})/2, \tag{32}$$

where P_{out} is the output power of the fundamental frequency, and P_{out3} is the power of the third-order tone.

The NF is measured by using the gain method. This is accomplished by terminating the input of the LNA with a 50 Ω load and the spectral noise power at the output is measured. The system noise figure is calculated using

$$NF_{dB} = P_{cold} + 174\ dBm/Hz - 10\log(B) - Gain_{dB}, \tag{33}$$

where P_{cold} is the noise power/Hz measured at the mixer output, 174 dBm/Hz is the noise power of an ideal 50 Ω load and B is IF bandwidth of the measurement.

After the initial measurement, if the measurements are within specifications, then the healing process ends. However, if specifications are not met, self-healing begins by measuring the nominal mixer performance. The mixer gain and IRR are first measured by activating ALL3. The mixer linearity is measured using a two-tone measurement by activating ALL3 and ALL4. If the mixer performance does not meet specifications, the algorithm adjusts the mixer tuning knobs. The tuning knob values are swept between pre-defined ranges. Upon completion of the sweep, the tuning knob values that result in the best performance are saved and the mixer is biased with these tuning knob values, as shown in Figure 71. The system performance is then re-measured using ALL1 and ALL2. If system specifications are still not met, the healing algorithm continues and the receiver performance is measured again with the LNA tuning knobs optimized this time. Because the gain and NF of the LNA are related, they are optimized simultaneously. The receiver gain is measured by activating ALL1, then the NF is measured using the method described previously, utilizing Equation (33) with ALL1 deactivated. The algorithm selects the tuning knob settings that result in the optimal trade-off between maximizing gain and minimizing NF, as shown in Figure 71. Two-tone linearity measurements are performed using both ALL1 and ALL2 simultaneously. If the receiver performance does not meet

specifications, the algorithm adjusts the LNA linearity tuning knobs and remeasures the receiver by sweeping the LNA tuning knobs similar to the method used for healing the mixer. At the end of the healing procedure, the algorithm sets all tuning knobs to the values that result in the optimal performance and the system performance is re-measured using the ALL1 and ALL2 as well as with the external signal sources to determine the efficacy of the healing process.

4.2.3 Measured Results

The receiver was fabricated in a commercially available, 180 nm, 150 GHz peak f_T SiGe BiCMOS platform. An annotated die micrograph of the receiver is shown in Figure 72 . The die area is 2.65 x 4.86 mm^2 including bondpads and consumes 240 mA (260 mA post-healed) from a 4.0 V supply. The receivers were tested using a total of six custom test boards that were fabricated. Healing was performed at three discrete frequency intervals (8 GHz, 10 GHz, and 16 GHz).

The measured nominal S-parameters of the LNA for one of the test boards is shown in Figure 73. The peak gain of the LNA is 13 dB at 12 GHz and the gain is above 10 dB from 10–15 GHz. The measured nominal gain of the mixer for one of the test boards is shown in Figure 74. The peak mixer gain is 18.2 dB at 12 GHz and the gain is above 15 dB for entire 6-18 GHz range. At nominal settings for both the LNA and mixer, the system gain is above 10 dB from 6–20 GHz, greater than the bandwidth of interest.

The voltage DAC and current DAC performance were also evaluated by testing separate test structure breakouts. The measured output current and output voltage characteristic curves vs. DAC code programming of the current and voltage DACs are shown in Figure 75. The figure shows that the current and voltage outputs vary linearly with DAC programming. The current DAC outputs approximately 0 mA when the DAC is programmed to 0 and 10 mA when programmed with the maximum

DAC code of 255. The voltage DAC ranges from approximately 1.0 V to 3.8 V when programmed from 0–255 respectively.

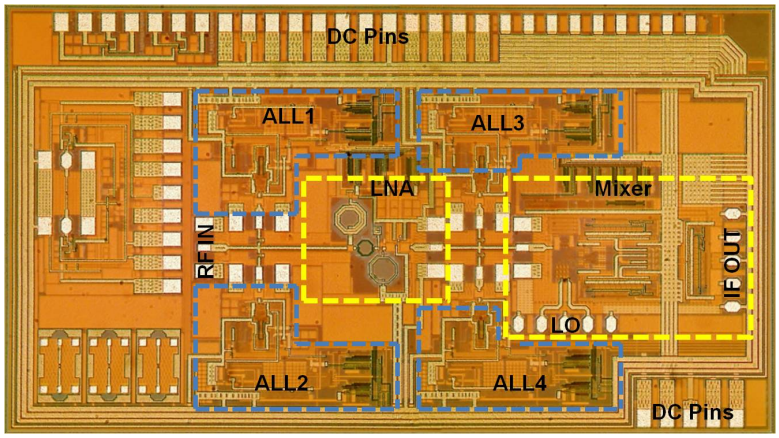


Figure 72: Annotated die photomicrograph of self-healing receiver, showing the RF blocks.

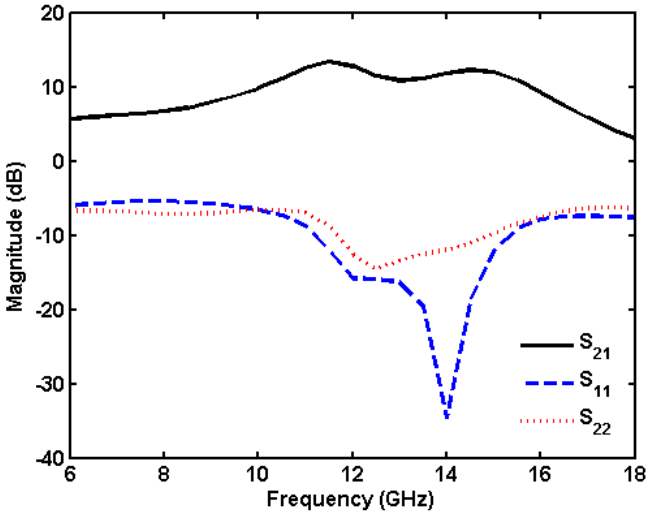


Figure 73: Measured LNA S-parameters at nominal bias settings from 6–18 GHz.

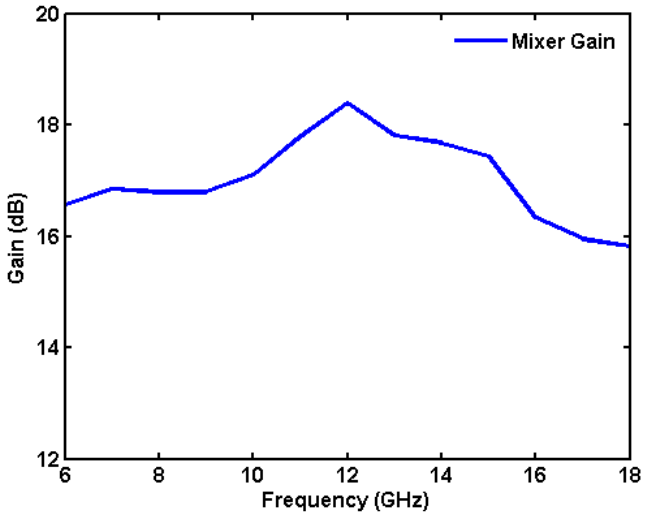


Figure 74: Measured mixer gain at nominal bias settings from 6–18 GHz.

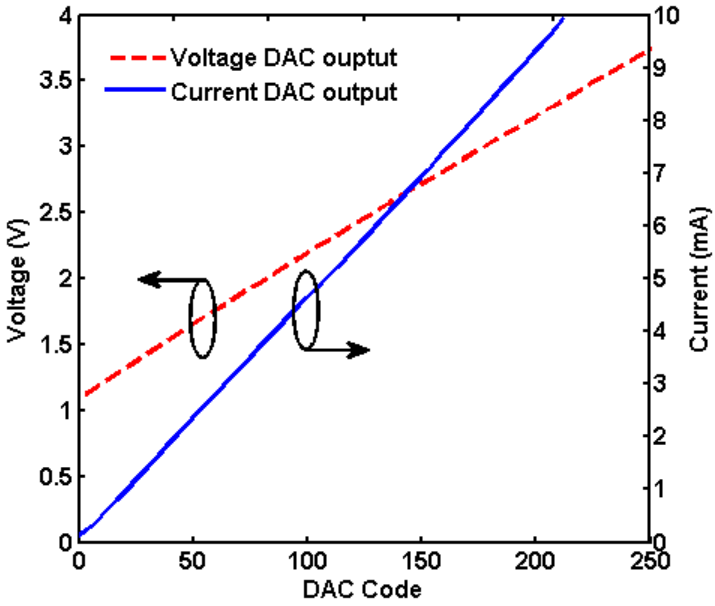


Figure 75: Voltage DAC and current DAC output vs. DAC code programming.

Histograms illustrating gain healing for 8 GHz, 10 GHz, and 16 GHz are shown in Figure 76. The pre- and post-healed gain for each sample at 8 GHz is shown in Figure 76 (a). The pre-healed gain ranges from 23–33 dB. The pre-healed gain is evenly distributed among the six samples for this range. After healing, the gain

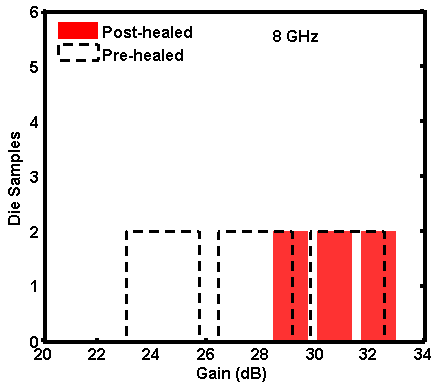
increases for all samples. Moreover, the gain variation decreases significantly, with the minimum and maximum gain at 29 dB and 33 dB, respectively. The results for 10 GHz are shown in Figure 76 (b). The pre-healed gain ranges from 15–35 dB for the six samples. Post-healing, the gain increases for all samples with the majority of samples (four) exhibiting gain values between 26 dB and 30 dB and two samples showing gain values between 36–40 dB. The 16 GHz results are shown in Figure 76 (b). The biggest improvements are seen at this frequency, with the pre-healed gain ranges from 23–30 dB for the six samples. After healing, the gain increases for all samples with the majority of samples with gain values ranging from 30–37 dB.

Similarly, IRR healing results for 8 GHz, 10 GHz, and 16 GHz are shown in Figure 77. The pre- and post-healed IRR histograms for 8 GHz are shown in Figure 77 (a). The pre-healed IRR ranges from 24–32 dB with the IRR of half the samples ranging from 24–25 dB. After healing, the IRR for the six samples increases and the variation for all samples decreases. Moreover, the post-healed IRR ranges from 30–33 dB. The results at 10 GHz are shown in Figure 77 (b). The pre-healed IRR ranges from 22–32 dB for the six samples. After healing, the IRR variation decreases with a minimum post-healed IRR of 25 dB and the maximum IRR remaining unchanged from the pre-healed value. The pre- and post-healed IRR at 16 GHz is shown in Figure 76 (c). The greatest improvements are shown at this frequency with the pre-healed IRR ranging from 25–31 dB for the six samples. After healing, the IRR for all samples increases with the IRR ranging from of 30–37 dB.

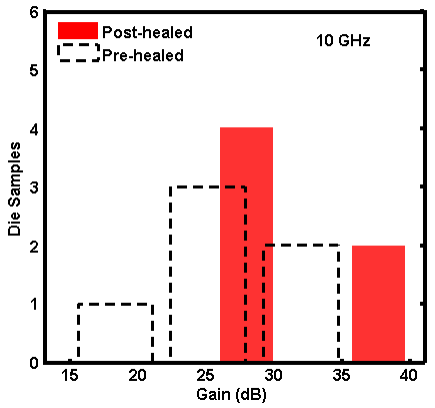
The histograms showing the OIP3 healing results are illustrated in Figure 77. The pre- and post-healed OIP3 at 8 GHz are shown in Figure 77 (a). The pre-healed OIP3 ranges from -1–7 dBm. After healing, half of the samples measured demonstrate OIP3 results that are similar to the pre-healed values. However, the other three samples show an improvement in OIP3 ranging from 8–10 dBm. The results at 10 GHz are shown in Figure 77 (b). The pre-healed OIP3 ranges from -6–7 dBm for the six

samples. After healing, the OIP3 variation decreases and ranges from 8–12 dBm. The pre- and post-healed OIP3 for each sample at 16 GHz are shown in Figure 78 (c). The greatest improvements are shown at this frequency with the pre-healed OIP3 ranging from -8–1 dBm for the six samples. After healing, the OIP3 for all samples increases with the OIP3 ranging from of 2–10 dBm.

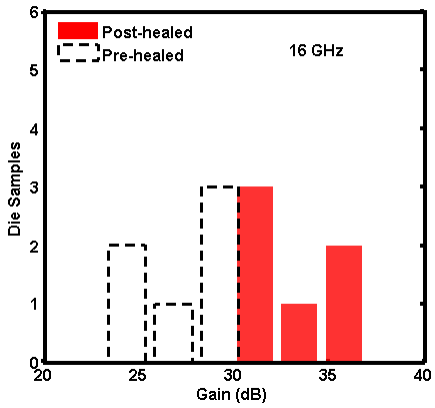
The histograms illustrating the NF healing results are shown in Figure 79. The pre- and post-healed NF at 8 GHz are shown in Figure 79 (a). The pre-healed NF ranges from 6–16 dB. After healing, the NF variation reduces significantly and the post-healed NF varies from 9–13 dB. The pre- and post-healed results at 10 GHz are shown in Figure 79 (b). The pre-healed NF ranges from 6–23 dB for the six samples. After healing, the NF variation decreases and ranges from 5–16 dB. The results at 16 GHz is shown in Figure 79 (c). The greatest improvements are shown at this frequency with the pre-healed NF ranging from 10–17 dB for the six samples. After healing, the NF for all samples increases with the NF ranging from 9–15 dB.



(a) Pre- and post-healed gain at 8 GHz.

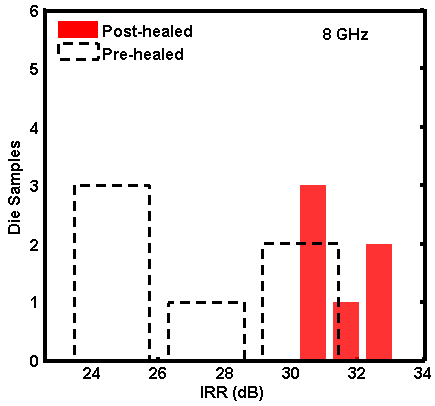


(b) Pre- and post-healed gain at 10 GHz.

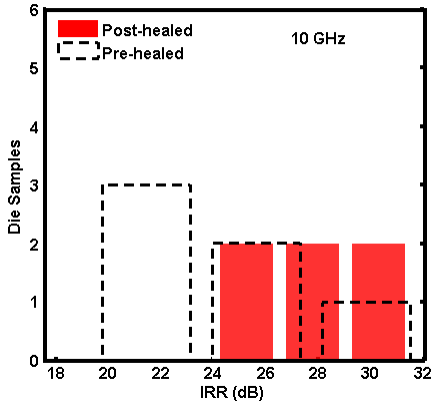


(c) Pre- and post-healed gain at 16 GHz.

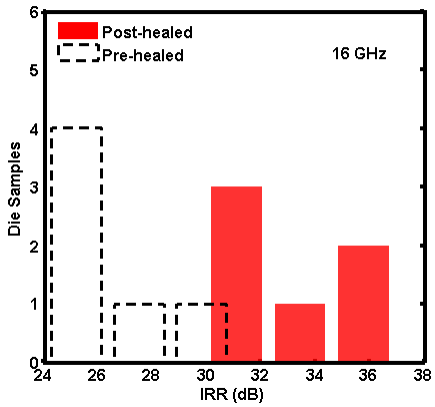
Figure 76: Gain healing at three frequencies: (a) pre-healed and post-healed gain at 8 GHz, (b) pre-healed and post-healed gain at 10 GHz, (c) pre-healed and post-healed gain at 16 GHz.



(a) Pre- and post-healed IRR at 8 GHz.

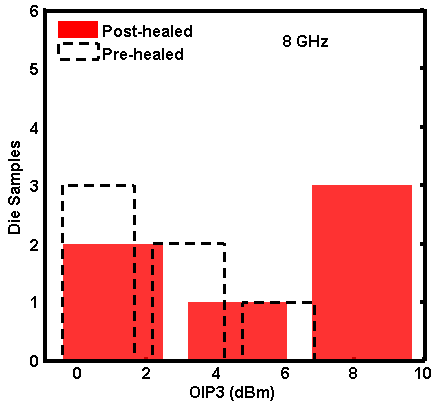


(b) Pre- and post-healed IRR at 10 GHz.

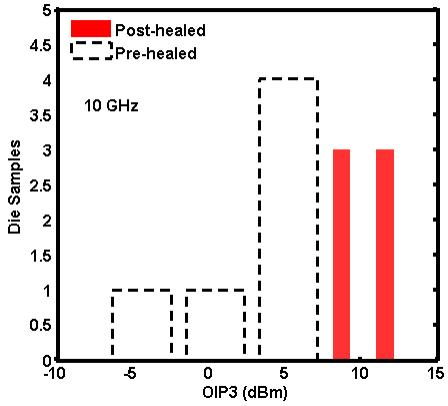


(c) Pre- and post-healed IRR at 16 GHz.

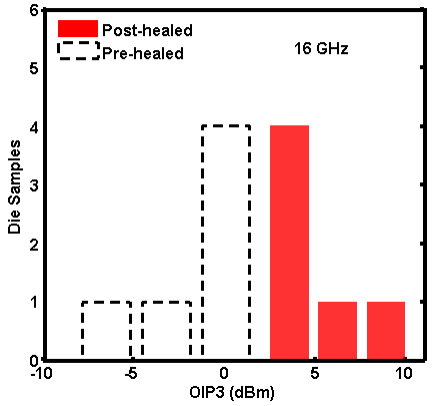
Figure 77: IRR Healing at three frequencies: (a) pre-healed and post-healed IRR at 8 GHz, (b) pre-healed and post-healed IRR at 10 GHz, (c) pre-healed and post-healed IRR at 16 GHz.



(a) Pre- and post-healed OIP3 at 8 GHz.

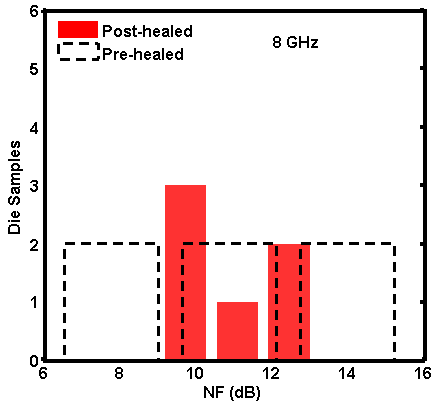


(b) Pre- and post-healed OIP3 at 10 GHz.

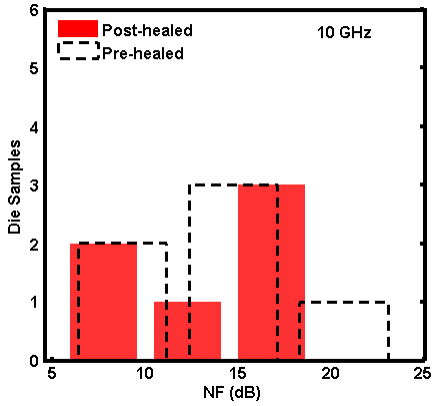


(c) Pre- and post-healed OIP3 at 16 GHz.

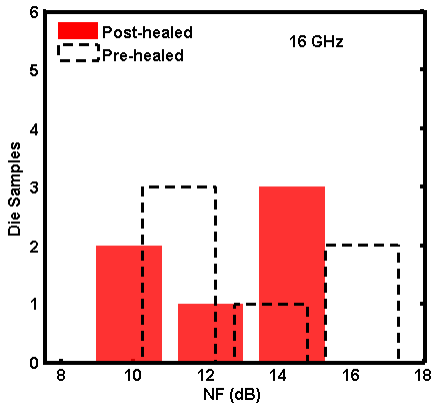
Figure 78: OIP3 Healing at three frequencies: (a) pre-healed and post-healed OIP3 at 8 GHz, (b) pre-healed and post-healed OIP3 at 10 GHz, (c) pre-healed and post-healed OIP3 at 16 GHz.



(a) Pre- and post-healed NF at 8 GHz.



(b) Pre- and post-healed NF at 10 GHz.



(c) Pre- and post-healed NF at 16 GHz.

Figure 79: NF Healing at three frequencies: (a) pre-healed and post-healed NF at 8 GHz, (b) pre-healed and post-healed NF at 10 GHz, (c) pre-healed and post-healed NF at 16 GHz.

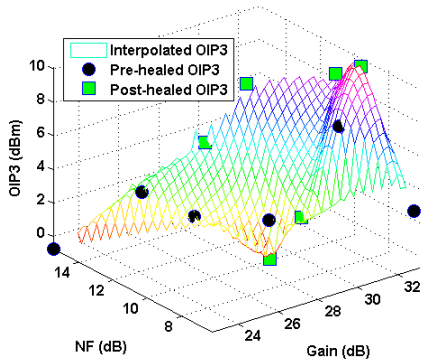
A summary of the measured results with the best overall healing performance of the measured samples of the receiver is shown in Table. 11. The table shows that the post-healed results demonstrate significant improvement in all metrics (gain, NF, IRR, and OIP3). In particular, it shows significant improvements in OIP3 and gain at each of the three frequencies that were used to demonstrate the receiver healing technique. When compared with the target specifications, the healing procedure is able to heal gain in all cases and bring performance near to the target specification for the other metrics.

Table 11: Summary of Best Self-healing Results at 8 GHz, 10 GHz, and 16 GHz.

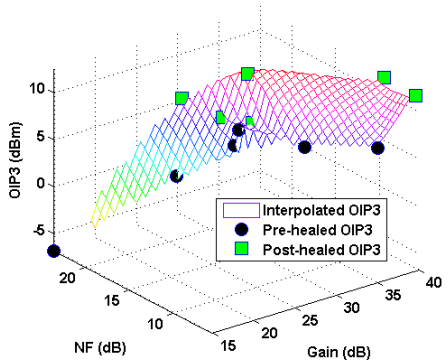
Frequency	8 GHz		10 GHz		16 GHz		Target Specification
	Pre-healed	Post-healed	Pre-healed	Post-healed	Pre-healed	Post-healed	
Gain (dB)	26.9	33.1	30.4	40	29.7	36.8	30
NF (dB)	12.2	11.1	9.5	9.5	10.9	8.7	8
IRR (dB)	26.7	33.1	27.1	30.1	31.0	31.0	20
OIP3 (dBm)	1.5	8.3	7.0	11.7	1.7	10.2	10

Often, maximizing the performance of a single RF metric is not required, but rather, a trade-off between all metrics is required to maximize the overall performance of the system. To further illustrate the effectiveness of this healing methodology, the ability of the algorithm to trade-off related metrics to achieve the best overall performance was investigated. Surface plots showing the trade-offs between OIP3, gain, and NF for pre- and post-healed values are shown in Figure 80. For each plot, the pre-healed results are represented by circles and the post-healed by squares. The surfaces connect show the trajectory for each test board between pre- and post-healed results. The OIP3 vs. gain and NF at 8 GHz is shown in Figure 80 (a). It shows that prior to healing, the six samples produce values for OIP3, NF and gain that are spread randomly across the surfaces. However, after healing, the majority of samples

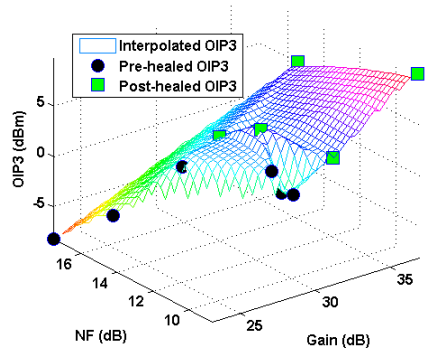
are located in a region that maximizes OIP3 and gain, and minimizes NF. A similar trend is observed for the surface plots at 10 GHz and 16 GHz in Figure 80 (b) and (c).



(a) OIP3 vs. gain and NF at 8 GHz.



(b) OIP3 vs. gain and NF at 10 GHz.



(c) OIP3 vs. gain and NF at 16 GHz.

Figure 80: Surface plots showing the trade-offs between OIP3, gain and NF and the trajectory between pre-healed and post-healed results at 8, 10 and 16 GHz.

4.2.4 Summary

A self-healing 8–18 GHz receiver was implemented in a 180 nm SiGe BiCMOS process. Automated self-healing of gain, NF, IRR, and OIP3 were demonstrated. The flexible nature of this self-healing receiver permits it to adapt to varying performance requirements or which delivers consistent performance despite process variations or environmental changes.

4.3 Mitigation of TID Degradation using the Self-healing Receiver

TID irradiation experiments were performed on the self-healing receiver discussed in the previous section. The receiver die samples, attached to specially designed circuit boards, were irradiated under bias with 10 keV X-rays at Vanderbilt University. The measurement setup is shown in Figure 81. A total of 3 boards were irradiated at X-ray doses of 1 Mrad(SiO_2),3 Mrad(SiO_2), and 6 Mrad(SiO_2). The boards were irradiated while the under nominal DC bias conditions. The receiver samples were

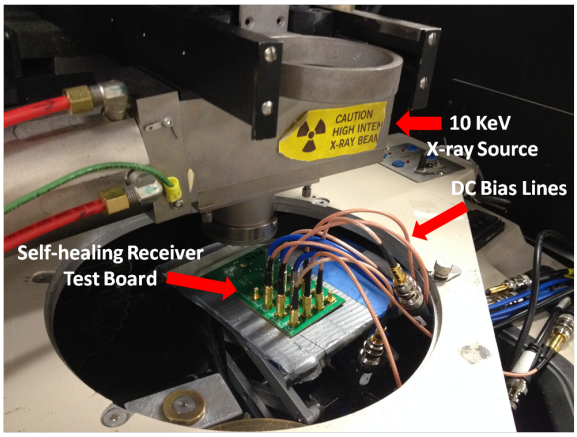


Figure 81: X-ray measurement setup for the self-healing receiver test boards.

RF and DC characterized before and after irradiation. In addition, the voltage and current DACs were characterized as stand alone blocks before and after X-ray, TID exposure (4 Mrad(SiO_2)) to investigate the effect of TID radiation on these blocks which are integral to the operation of the self-healing receiver. Healing of the receiver

was performed pre- and post-irradiation at two discrete frequency intervals (10 GHz, 16 GHz) representing the lower and upper band frequency regimes of the ALL test signal sources.

4.3.1 Pre- and Post-irradiated Nominal Performance

The pre-irradiated voltage and current DACs output characteristics are shown in Figure 75 of the previous section. The current and voltage outputs vary linearly with DAC programming and the DACs are designed to maintain consistent performance over a wide temperature range [21]. However, the DACs, which incorporate many CMOS devices, can exhibit performance degradation caused by X-ray exposure. In particular, CMOS devices suffer from increased gate leakage when exposed to radiation [5]. After TID exposure, the voltage DAC performance is practically identical to its pre-irradiated measurement and the current DAC shows some degradation as illustrated in Figure 82.

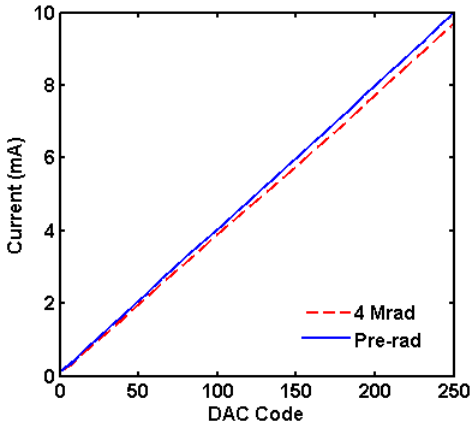


Figure 82: Pre- and post-irradiated current DAC output vs. DAC code.

The figure shows that there is a minor reduction in the current output of the DAC when exposed to 4 Mrad(SiO_2) TID, particularly when programmed to higher DAC codes. The maximum difference between the pre- and post-irradiated current outputs is approximately 0.3 mA. This difference is very small and has a negligible impact on the performance of the RF blocks that the DACs bias.

The pre- and post-irradiated to 1 Mrad(SiO_2) S-parameters of the LNA block are shown in Figure 83. The figure shows that there is significant degradation in the LNA performance.

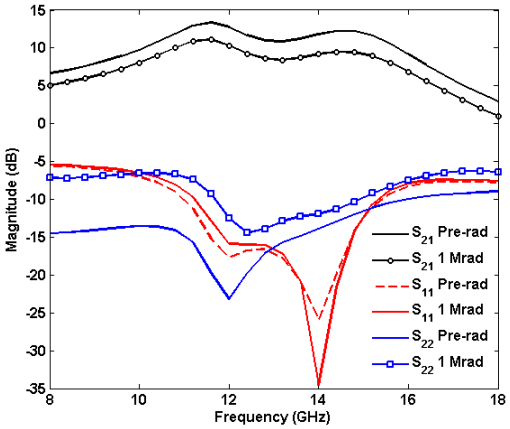


Figure 83: Pre- and post-irradiated LNA S-parameters with TID = 1 Mrad(SiO_2).

Post 1 Mrad(SiO_2) TID exposure, the gain (S_{21}) of the LNA reduces across the band. The gain decreases by approximately 3 dB across the band. Also, the output return loss (S_{22}) degrades severely after TID exposure; pre-irradiation, the output return loss is below 10 dB from 8–18 GHz. However, after the 1 Mrad exposure, the output return loss is above 10 dB across the band of interest. The output return loss is controlled by the output stage of of the LNA which is a SiGe HBT transistor (Q4), in a source follower buffer configuration shown in Figure 68. The impedance looking into the emitter node of Q2 is inversely proportional to the transconductance ($g_{m,Q2}$) of Q2. For the output return loss to be below 10 dB, then $1/g_{m,Q2} \approx 50\ \Omega$ across the frequency band of interest. The transconductance is related to the current gain of Q2 by

$$g_{m,Q2} = \frac{\beta}{r_\pi}, \tag{34}$$

where β and r_π are the current gain and small signal input resistance of Q2 respectively. From previous studies, it has been shown that TID exposure increases base current leakage in SiGe HBTs as a result of the creation of positive changes and an increase in the number of interface traps at the emitter-base (EB) spacer [6, 16]. Also, it has been shown that while base current leakage is usually minimal, it can affect the performance of circuit blocks that are especially sensitive to changes in the value of β of particular SiGe HBT devices within the circuit block [57]. Because, $g_{m,Q2}$ is sensitive to changes in β, the output return loss and subsequently the gain of the LNA is adversely affected by TID X-ray radiation. These changes in the LNA are severe enough to degrade the overall system performance. The mixer also exhibits degradation as a result of TID exposure; the mixer gain from 8–18 GHz pre- and post-irritated to 1 Mrad(SiO_2) is shown in Figure 84. The mixer gain degrades by a similar magnitude as the LNA; the mixer gain degrades by as much as 2.5 dB after a TID of 1 Mrad(SiO_2). The mixer shown in Figure 69, also contains sub-blocks that are depend on the g_m of SiGe HBT transistors namely, the micro-mixer and VGA [66]. Damage to these sub-blocks negatively affect the mixer gain as well as other performance metrics.

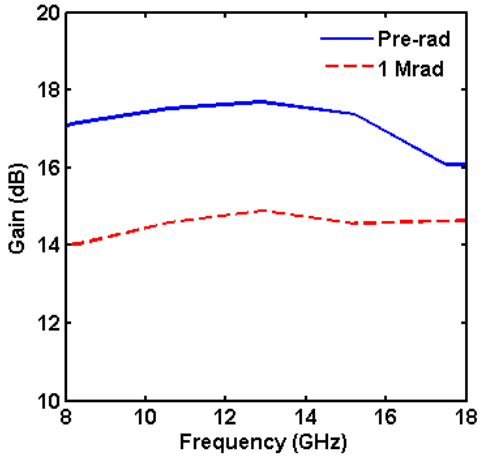
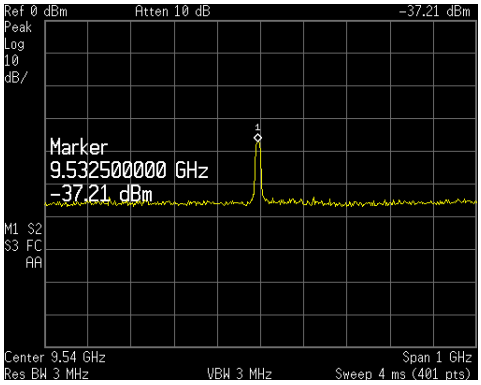
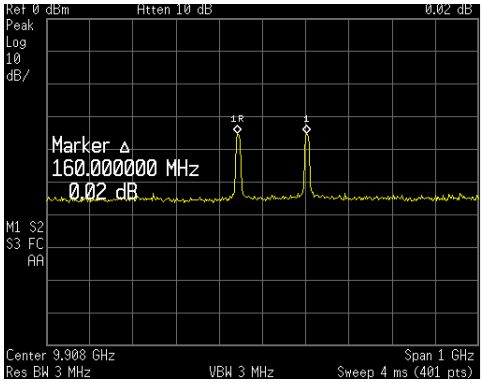


Figure 84: Pre- and post-irradiated image-reject mixer gain with TID = 1 Mrad(SiO_2).

The performance of the ALLs are also degraded by TID exposure. The pre-irradiated frequency and power of ALL3 at nominal DAC programming is -33 dBm (-26 dBm after factoring cable and connector losses) at 10 GHz. After a TID dose of 3 Mrad(SiO_2), ALL3 exhibits decreases in both frequency and power as show in in Figure 85 (a) with the frequency reducing to 9.5 GHz and power reducing to -37 dBm. However, the ALLs can be re-calibrated to recover the lost performance. The re-calibrated ALL3 and ALL4 tones are shown in Figure 85 (b). The figure shows that after re-calibration, the ALL tones are approximately -33 dBm and the spacing is 160 MHz.



(a)



(b)

Figure 85: (a) Post-irradiated (TID = 3 Mrad(SiO_2) ALL3 tone at nominal programming for 10 GHz. and (b) post-irradiated ALL3 and ALL4 tones after re-calibration at 10 GHz

A similar effect was observed with ALL1 and ALL2 and at other TID doses. The ALLs were re-calibrated post-irradiation and could be brought back to the pre-irradiated performance specification in all but the 6 Mrad(SiO_2) case; the ALLs that were exposed to 6 Mrad(SiO_2) could not generate a measurable tone above the noise floor in the lower frequency band (8–10 GHz). This is possibly because the base leakage at 6 Mrad(SiO_2) is high enough to significantly impact the performance of the ring oscillator and frequency dividers that are at the core of the ALL design. However, re-calibration was successful for the upper frequency band as shown in Figure 86. The figure shows that after re-calibration, the ALL tones are approximately -33 dBm and the tone spacing is 205 MHz.

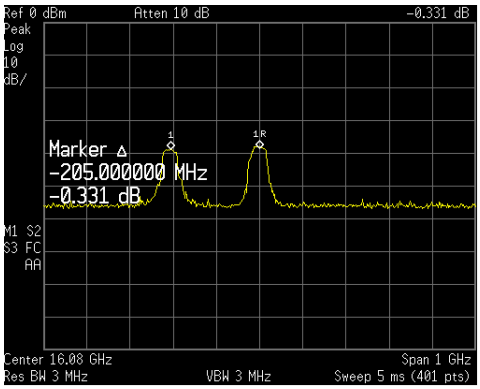


Figure 86: post-irradiated ALL3 and ALL4 tones (TID= 6 Mrad(SiO_2) after re-calibration at 16 GHz.

Changes were also seen in the pre- and post-irradiated DC performance of particular blocks within the receiver. The voltages and currents of the main supplies of the receiver namely the 4.0 V, 3.3 V, 1.8 V, and the two 100 μA current sources, A and B were monitored for each board before and after TID exposures of 1, 2, and 6 Mrad(SiO_2).The results are shown in Table 12. The table shows that the changes in the currents measured from the voltage supplies are relatively stable for the test boards at each TID exposure. The greatest change was observed in the 4.0 V supply in which maximum decrease in current was 5 mA for the board exposed to 6

Mrad(SiO_2). The monitored voltages of the current supplies show greater changes; for the 100 μ A current sources, the voltage developed drops by more than 0.4 V for the board exposed to 6 Mrad(SiO_2). The current sources are CMOS based and TID exposure results in key parameters such as threshold voltage, g_m, and increased current leakage leading to a reduction in V_{BE} across the devices in the mirror, degrading the performance of the current mirrors.

Table 12: Monitored Voltages and Currents of Supplies Pre- and Post-irradiated.

Board	1		2		3	
Supply	Pre-rad	1 Mrad (SiO_2)	Pre-rad	3 Mrad (SiO_2)	Pre-rad	6 Mrad (SiO_2)
4.0 V	242 mA	240 mA	241 mA	237 mA	243 mA	238 mA
3.3 V	37 mA	36 mA	32 mA	32 mA	31 mA	32 mA
1.8 V	14 mA	14 mA	14 mA	14 mA	14 mA	13 mA
100 μ A (A)	1.463 V	1.385 V	1.493 V	1.262 V	1.455 V	1.088 V
100 μ A (B)	1.489 V	1.411 V	1.469 V	1.231 V	1.501 V	1.044 V

4.3.2 Post-irradiated Self-healing Results

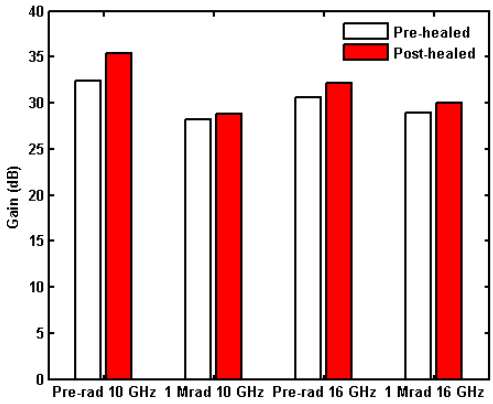
The post-irradiated S-parameters, gain, and DC results show that the the system performance degrades after TID exposure. However, the ALLs can be re-calibrated to meet the pre-irradiated performance specifications in all but the case when the receiver board was exposed to the very high TID of 6 Mrad(SiO_2) in which, the the ALLs failed to produce a 10 GHz tone. However, even at 6 Mrad(SiO_2), the ALLs were able to generate tones at 16 GHz, enabling healing at this frequency. These results demonstrate that it is possible to heal the receiver to mitigate for TID damage that such a receiver will practically be subjected to in space missions. The three boards exposed to 1, 3, and 6 Mrad(SiO_2) were re-measured and the gain, NF, IRR, and OIP3, RF specifications recorded. Then, self-healing method, as described in the previous section.

The pre- and post-healed gain both before and after irradiation to TID = 1, 3, and 6 Mrad(SiO_2) at 10, and 16 GHz are shown in Figure 87. The figure shows that the gain was successfully improved for measurements both before and after irradiation. For the board exposed to 1 Mrad(SiO_2) shown in Figure 87 (a), greater improvements in gain are shown pre-irradiation at 10 GHz than the post-irradiated results at both 10 and 16 GHz. In this case, the pre-healed gain is 31 dB and the post-healed gain is above 35 dB. However, post-irradiation, the gain improves modestly at 10 and 16 GHz after tuning. For the board exposed to 3 Mrad(SiO_2), the greatest improvement is seen at 10 GHz post-irradiated, as shown in Figure 87 (b). In this case, the pre-healed gain is 30 dB and the post-healed gain is above 35 dB. The board exposed to 6 Mrad(SiO_2) shows great improvements in gain after healing pre- and post-irradiated, except for 10 GHz, post-irradiated as shown in Figure 87 (c).

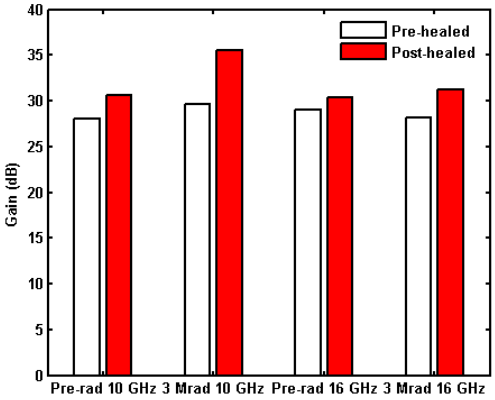
Similarly, pre- and post-healed NF both before and after irradiation with TID = 1, 3, and 6 Mrad(SiO_2) at 10, and 16 GHz are shown in Figure 88. For the board exposed to 1 Mrad(SiO_2) shown in Figure 88 (a), the pre-irradiated NF at both 10 and 16 GHz show the biggest improvements in NF; at 10 GHz the pre-healed NF is 8 dB and the post-healed value is 7 dB. At 16 GHz the pre-and post-healed NF values are 10 and 9.5 dB respectively. However, post-irradiation at 10 and 16 GHz, the NF shows modest improvements or the same performance post-healing. The NF of the boards exposed to TID values of 3 and 6 Mrad(SiO_2), illustrated in Figure 88 (b) and (c) respectively, show that the NF is significantly improved pre- and post-irradiation; the board exposed to 3 Mrad(SiO_2) shows a maximum reduction in NF of 2 dB at 10 GHz and the board exposed to 6 Mrad(SiO_2) shows a maximum reduction in NF of 2.5 dB at 16 GHz.

The pre- and post-healed IRR before both and after irradiation with TID = 1, 3, and 6 Mrad(SiO_2) at 10, and 16 GHz are shown in Figure 89. Improvements are seen in all cases, especially in boards exposed to TID values of 3 and 6 Mrad(SiO_2),

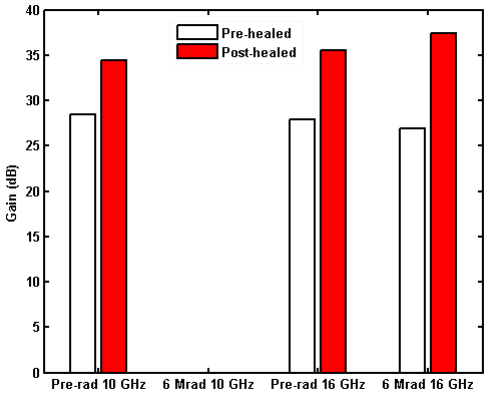
shown in Figure 89 (b) and (c) respectively. Finally the pre- and post-healed OIP3 before and after irradiation illustrated in Figure 90. The OIP3 shows the greatest post-healed improvement of all pre- and post-irradiated RF measurements. In particular, the measured OIP3 of the board exposed to 6 Mrad(SiO_2) shows tremendous improvements at 16 GHz pre-irradiation (0 dBm pre-healed and 7.8 dBm post-healed) and post-irradiation (-5.6 dBm pre-healed and 5.8 dBm post-healed).



(a) Pre- and post-healed gain TID = 1 Mrad(SiO_2)

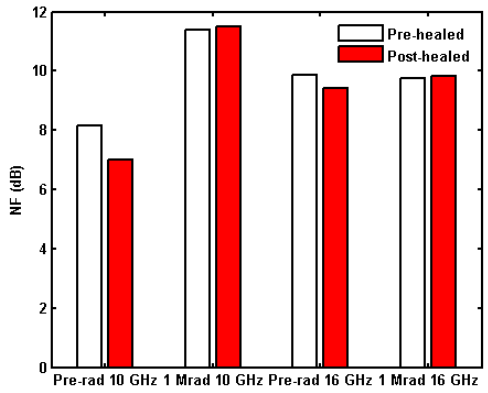


(b) Pre- and post-healed gain TID = 3 Mrad(SiO_2)

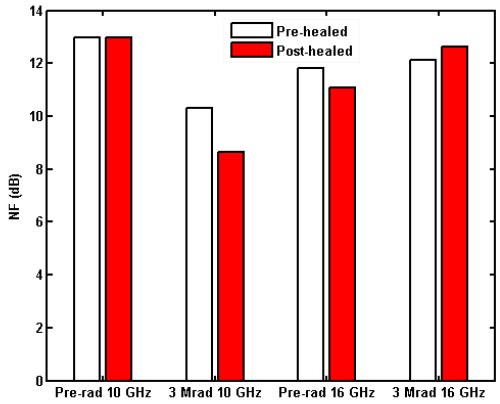


(c) Pre- and post-healed gain TID = 6 Mrad(SiO_2)

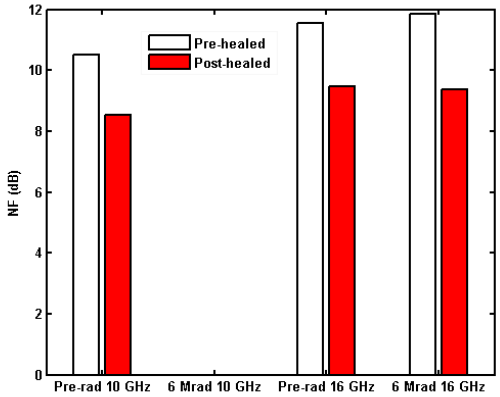
Figure 87: Pre- and post-healed gain before and after irradiation with TID = 1, 3, and 6 Mrad(SiO_2) at 10 and 16 GHz.



(a) Pre- and post-healed NF TID = 1 Mrad(SiO_2)



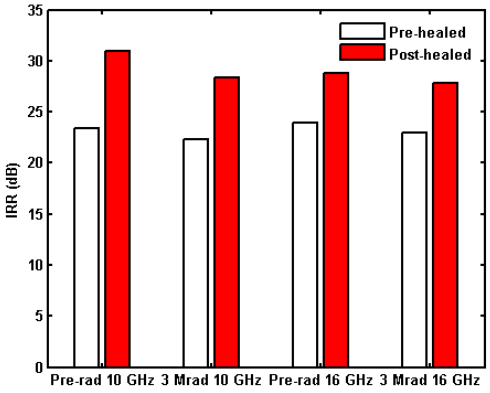
(b) Pre- and post-healed NF TID = 3 Mrad(SiO_2)



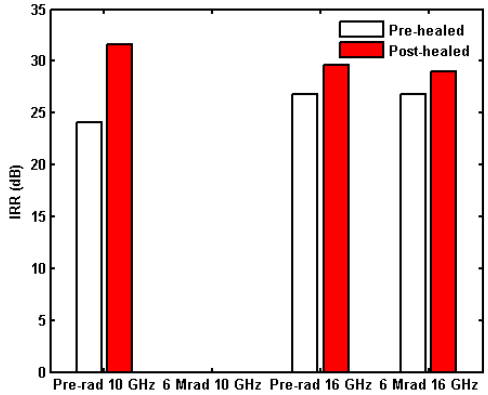
(c) Pre- and post-healed NF TID = 6 Mrad(SiO_2)

Figure 88: Pre- and post-healed NF before and after irradiation with TID = 1, 3, and 6 Mrad(SiO_2) at 10 and 16 GHz.

(a) Pre- and post-healed IRR TID = 1 Mrad(SiO_2)

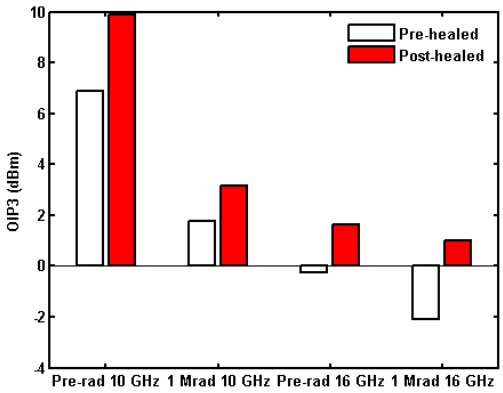


(b) Pre- and post-healed IRR TID = 3 Mrad(SiO_2)

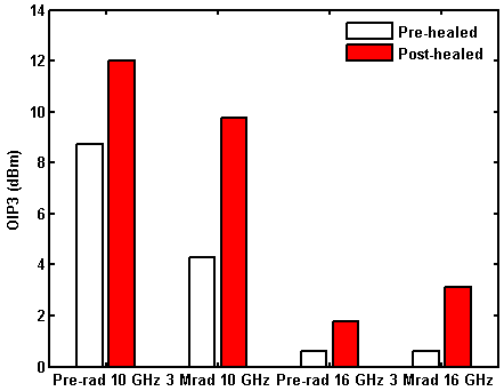


(c) Pre- and post-healed NF TID = 6 Mrad(SiO_2)

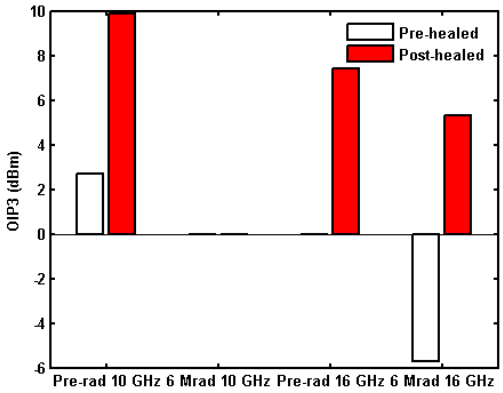
Figure 89: Pre- and post-healed IRR before and after irradiation with TID = 1, 3, and 6 Mrad(SiO_2) at 10 and 16 GHz.



(a) Pre- and post-healed OIP3 TID = 1 Mrad(SiO_2)



(b) Pre- and post-healed OIP3 TID = 3 Mrad(SiO_2)



(c) Pre- and post-healed OIP3 TID = 6 Mrad(SiO_2)

Figure 90: Pre- and post-healed OIP3 before and after irradiation with TID = 1, 3, and 6 Mrad(SiO_2) at 10 and 16 GHz.

4.3.3 Summary

A self-healing 8–18 GHz receiver was implemented in a 180 nm SiGe BiCMOS process. Automated self-healing of gain, NF, IRR, and OIP3 were demonstrated pre-and post-irradiation with TID values of 1, 3, and 6 Mrad(SiO_2). The ability of the receiver to mitigate for radiation damage shows that this system can be used in harsh radiation environments, such as in space based RF, microwave, and millimeter-wave systems.

CHAPTER V

CONCLUSION

5.1 Summary of Contributions

The purpose of this research is to harness the performance of high-frequency SiGe BiCMOS technology towards the development of circuits that are robust to extreme environments and for the mitigation of performance degrading effects such as PVT. Developing these components using commercially available SiGe BiCMOS technologies is advantageous due to SiGe's low-cost, high-performance, and its inherent resilience to multi-Mrad TID radiation exposure. Specifically, tunable components used in radar and wireless communication such as tunable LNAs and tunable transmission lines were designed. Also developed were circuit blocks for on-chip characterization of transistors that can be applied to BIST systems. In addition, RF performance metrics over a wide temperature range were characterized, radiation effects on RF and digital building blocks were examined, and TID mitigation techniques were presented and verified. The specific contributions include:

1. Two on-chip device characterization circuits were designed to extract the current gain of a SiGe HBT test transistor. These circuits are useful in the context of various "self-healing" RF circuits and systems. One of the characterization circuits includes built-in temperature compensation that enables accurate measurement of the current gain of the test device over a wide temperature range.

2. Tunable slow-wave microstrip lines were designed for millimeter-wave applications. The transmission line backplane can either be connected to a ground potential or electrically floated by use of nMOS or SiGe HBT switching devices. The maximum phase changes for the nMOS and SiGe HBT transmission lines

were 62 GHz and 120 GHz, respectively. The maximum insertion loss for the nMOS and SiGe HBT transmission lines were 14 dB and 28 dB, respectively.

3. A tunable microstrip line using two nFET transistors was designed to switch the backplane between floating and ground potential. The tunable MLN design utilizes the shunt capacitances of the shunt nFET devices as well as the series inductance of the backplane to mimic the functionality of a traditional MLN using the traveling wave concept.

4. An ultra-wideband LNA with gain and input return loss control was designed and implemented in SiGe HBT technology. This LNA is broadband, covering the frequency range of 3–20 GHz, and achieves a peak gain of 21.3 dB. The SiGe LNA exhibits a noise figure of 4.2–5.2 dB across an 8-1-8 GHz band and consumes 35.2 mA from a 3.3 V supply.

5. An 8-16 GHz SiGe LNA with tuning capability for mitigation of radiation-induced performance loss was designed. The LNA covers a frequency range of 8-16 GHz and achieves a peak gain of 17.5 dB at nominal bias. It achieves a peak OIP3 of 15.8 dBm at 10 GHz at nominal bias. The noise figure of the LNA is 4.5-8.1 dB across band, and it nominally consumes 4 mA from a 4 V supply. Samples were irradiated with 63.3 MeV proton source to doses ranging from 200 krad(Si) to 2 Mrad(Si). The LNA incorporates bias control "tuning-knobs" to enable bias tuning to mitigate for RF performance loss as a result of total dose exposure and process variation in performance metrics.

6. The use of a tunable LNA within an 8–18 GHz self-healing receiver was implemented in SiGe technology. The receiver chain consists of an LNA, an image-reject mixer, amplitude-locked loop (ALL) signal sources that are used to provide test signals of a pre-defined amplitude and frequency, and finally control circuitry in the form of digital analog converters (DACs) and data registers.

Both the LNA and the mixer circuit blocks incorporate tuning knobs to enable self-healing in order to ensure consistent performance and mitigate the negative effects of process, voltage, and temperature (PVT) variations, aging, and damage from extreme environments such as ionizing radiation. A maximum post-healed gain greater than 30 dB, an image rejection ratio (IRR) exceeding 30 dB, output 3^{rd} order intercept point (OIP3) greater than 8 dBm, and noise figure (NF) less than 9 dB are obtained in measurement. An automated self-healing algorithm is developed and shown to be effective for improving the overall performance of the receiver. The receiver was fabricated in an 0.18 μm SiGe BiCMOS process with a peak f_T of 150 GHz, and consumes 240–260 mA from a 4 V supply.

7. The characterization of an 8–18 GHz self-healing receiver was exposed to 10 keV X-rays exposed to TID doses of 1, 3, and 6 Mrad(SiO_2). The characterization included evaluation the effect of X-rays on the nominal performance of the receiver circuit blocks and on the receiver as a whole. The effectiveness of the receiver's self-healing functionality to mitigate for the TID damage of the X-rays.

5.2 Future Work

The research presented in this thesis included the initial results of investigations using SiGe BiCMOS technology for high-frequency self-healing and BIST circuits. Several opportunities for future research based on these results exist and can serve as follow-on research for this work:

1. Measurement of self-healing receiver systems over temperature to determine the effectiveness of the self-healing blocks and methodology at tuning RF performance over a wide temperature range.

2. The design of a fully integrated self-healing receiver with on-chip calibration for the amplitude-locked loops (ALLs), on-chip RF characterization, and on-chip memory/digital blocks.

3. Development of self-healing blocks and receivers that operate at millimeter-wave frequencies.

4. Inclusion of tunable transmission lines in RF blocks. The tunable MLNs can be used to create tunable matching networks for use in reconfigurable RF amplifiers.

5. Modification of the SMU to directly extract I_C, I_B, and g_m of the test transistor.

6. Integration of the SMU with RF circuits to demonstrate the use of DC characteristic information extracted from the SMU to tune the RF performance of circuit blocks on the same die as the SMU.

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VITA

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