A 1.5V Multirate Multibit Sigma Delta Modulator for GSM/WCDMA in a 90nm Digital CMOS Process

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A 1.5V Multirate Multibit Sigma Delta Modulator for GSM/WCDMA in a 90nm Digital CMOS Process

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To my wife Didem

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Summary

The development of low-voltage and low-power mixed signal CMOS integrated circuits has been one of the key objectives in the last decade. Thus, a significant amount of effort has been devoted for this purpose. There are two main reasons that fuel this need. First reason is the increasing demand for portable battery operated systems. The second one is the ongoing transistor scaling. Analog to digital converters based on $\Sigma\Delta$ modulators are widely used in the analog front ends of various mixed signal integrated circuit. Hence they have to operate from low supply voltages as well as with minimum power dissipation.

This dissertation investigates the use of digital techniques to replace some of the functionalities that were traditionally performed by analog circuits. By doing so, the aim is to increase the share of digital blocks in the $\Sigma\Delta$ system and decrease area and power consumption of the modulator. This dissertation also investigates the design techniques of low-voltage, power efficient analog building blocks which are then used in the design of a $\Sigma\Delta$ modulator for wireless applications (i.e., 200kHz and 1.94MHz for GSM and Wideband CDMA, respectively).

In order to demonstrate the techniques presented here, a prototype $\Sigma\Delta$ modulator is designed and fabricated in a 90nm five metal single poly n-well CMOS process. The presented $\Sigma\Delta$ modulator operates from two different supplies: 1.5V for analog side and 1.3V for digital side. The modulator is realized with fully-differential stray insensitive switched capacitor integrators. Both integrator stages use a fully differential folded cascode operational transconductance amplifier with switched capacitor common mode feedback to set the common mode voltages of the output nodes. Both amplifiers have PMOS input pairs. Simple level shifters are used to increase the voltage level of the clock signals so that the switches that are driven by these clock signals

can be minimized. A careful capacitor scaling is performed in the second integrator stage in order to take advantage of the noise shaping that is due to the first integrator stage. The presented $\Sigma\Delta$ modulator achieves 68.6/42.8dB peak SNDR and dissipates 1.1/1.9mA of current (mostly from 1.5V analog supply) in GSM and WCDMA modes, respectively.

Chapter 1

INTRODUCTION

1.1 INTRODUCTION

The market for mobile radio frequency personal communication devices is rapidly expanding with the development of new services and applications. The variety of applications and devices has led to a proliferation of communications standards with different modulation schemes, channel bandwidths, dynamic range requirements and so forth. In addition, consumers are demanding low-cost, low-power, and small form factor devices to satisfy these communication requirements. As a result, recent efforts in the design of integrated circuits for personal communication transceivers have focussed on increased integration in a low cost technology (e.g. CMOS) as well as adaptability to multiple RF communication standards. This requires research into new architectures and circuit techniques that enable both integration and programmability in RF transceivers [1, 2].

As more and more sophisticated digital signal processing(DSP) functions are implemented on a single IC, the emphasis on the interface circuitry used to convert signals between analog and digital domains increases. $\Sigma\Delta$ A/D converters combine oversampling and feedback to shape the noise and then use a digital lowpass filter to attenuate the noise that has been pushed out-of-band. This way, it is possible to achieve a dynamic range as high as 16 bits or more at relatively modest oversampling ratios [11].

A very significant feature of $\Sigma\Delta$ A/D converters is the transfer of much of the

signal processing into the digital domain where power consumption can be dramatically reduced simply by scaling the technology and reducing the supply voltage [16]. In addition to this, digital systems are easier to implement when moving to a newer technology node since they are generally synthesized by commercial CAD tools. This generally means reduced design cycle and time to market.

This research focuses on bringing more of the digital functionality into the $\Sigma\Delta$ modulator architectures due to the benefits mentioned above. A new idea is explored and it is verified by both behavioral simulation tools and Spice. An experimental prototype design is fabricated using a 90nm digital CMOS process.

1.2 RESEARCH TARGETS

This research seeks to address issues of integration and programmability in RF receivers by investigating the use of multi-rate multi-bit design techniques in the design of a high-speed $\Sigma\Delta$ modulator. A more general goal of this research, which is critical for the RF application, is to develop techniques at both the architecture and circuit design levels to minimize power dissipation in high-speed $\Sigma\Delta$ modulators. In the context of these goals, some key research results are as follows:

- Demonstrated that a multi-rate multi-bit $\Sigma\Delta$ modulator(MMSD) can meet the baseband processing requirements for RF receivers at a reasonable power dissipation. An experimental prototype implemented in a 90nm single-poly, 5 metal CMOS process achieved 68.6dB of Signal-to-Noise and Distortion ratio (SNDR) and required 1.1mA of current across 200kHz signal band. This dual mode modulator also achieved 42.8dB of SNDR across 2MHz signal band and required 1.9mA.

- Showed that scaling integrator sampling capacitors to the minimum value required by kT/C noise at each stage is an effective technique for reducing power dissipation.

- The issues with the ideal multi-rate multi-bit $\Sigma\Delta$ modulators are addressed with a new integrator architecture and a novel clocking scheme. This made the practical implementation of such systems possible.

- Bulky flash A/D converter inside the feedback loop of the $\Sigma\Delta$ modulator is replaced with a single comparator, a very simple digital FIR filter and an up-sampling in the second integrator stage of the modulator. This resulted in significant area and power savings.

1.3 THESIS ORGANIZATION

Chapter 2 provides a brief overview of the fundamentals of $\Sigma\Delta$ modulators.Techniques for improving resolution of high-speed $\Sigma\Delta$ A/D converters are discussed in Chapter 3. In Chapter 4, the specifics of multirate modulators are explained. Chapter 5 describes the system level design of the modulator. The circuit design aspects of the modulator are presented in Chapter 6. An experimental prototype and test results are discussed in Chapter 7. Chapter 8 contains concluding remarks.

Chapter 2

FUNDAMENTALS OF SIGMA-DELTA ($\Sigma\Delta$) Oversampling A/D CONVERTERS

2.1 INTRODUCTION

This chapter reviews some of the fundamental issues in the design of $\Sigma\Delta$ modulators. The discussion begins with a variety metrics used to evaluate modulator performance with emphasis on those which are important for RF applications. Then, the basic concept of how a $\Sigma\Delta$ modulator works is described, and the basic linearized models are reviewed and related to performance issues. Finally, the fundamental power limits for $\Sigma\Delta$ modulators implemented using switched-capacitor circuits are derived. Following this basic introduction, tradeoffs among a variety of sigma-delta architectures suitable for high-speed applications are explored in the next chapter.

2.2 PERFORMANCE METRICS

This section defines the metrics used to evaluate $\Sigma\Delta$ modulator performance. For RF applications, the key requirements for a $\Sigma\Delta$ modulator are dynamic range, Nyquist rate and power dissipation. In addition, $\Sigma\Delta$ designers usually specify peak SNR (signal-to-noise ratio) and peak SNDR (signal-to-noise-and-distortion ratio), which measure the degradation of the signal due to noise alone, and due to a combination of noise and distortion, respectively.

2.3 PEAK SNR/SNDR AND DYNAMIC RANGE

Peak SNR, SNDR and dynamic range are related specifications and will be defined together. Dynamic range is the ratio in power between the maximum input signal level that the modulator can handle and the minimum detectable input signal. SNR is the ratio of the signal power at the output of the modulator to the noise power. SNR includes all noise sources in the modulator, both thermal and quantization. SNDR is the ratio of the signal power at the output of the modulator to the sum of the noise and harmonic distortion powers. Peak SNDR is a useful metric for evaluating the capability of a $\Sigma\Delta$ modulator for handing large in band signals at acceptable linearity and is especially important for applications such as digital audio. Note that peak SNDR is frequency dependent and can be used to measure the degradation of modulator performance as the input signal increases in frequency. Peak SNR, SNDR and dynamic range are typically reported using the type of plot shown in Fig. 2.1. The plot shows SNR and SNDR as a function of input signal power in dB relative to the full scale of the modulator. For small signal levels, distortion is not important implying that the SNR and SNDR are approximately equal. As the signal level increases, distortion degrades the modulator performance, and the SNDR will be less than the SNR. Dynamic range on the plot is the difference between the input level where the SNDR drops 3 dB beyond the peak and the x-intercept of the SNDR curve.

A closely related specification to dynamic range is the resolution of the modulator expressed in bits. The resolution in bits (N) is defined in equation 2.1 where DR is the dynamic range of the modulator expressed in dB. The correspondence is such that each bit of resolution is equivalent to 6 dB of dynamic range.

$$N = \frac{DR - 2}{6} \tag{2.1}$$

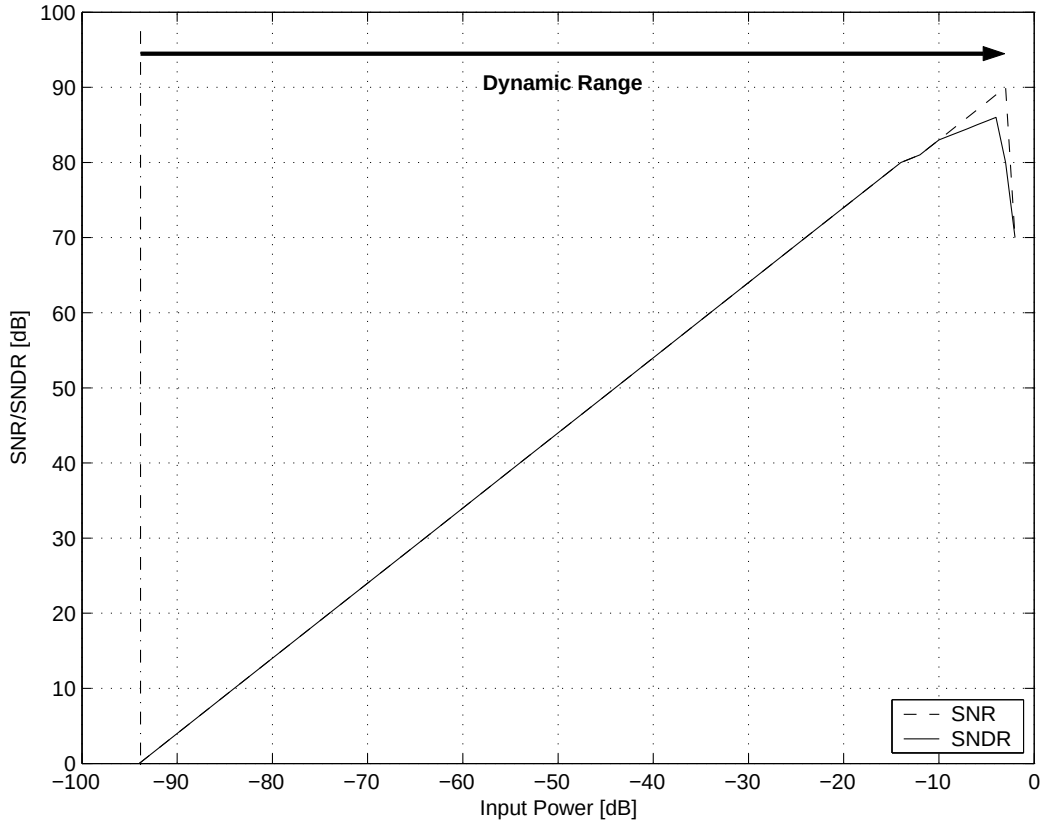

Figure 2.1: SNR and SNDR curves for a $\Sigma\Delta$ modulator.

2.4 NYQUIST RATE

The Nyquist rate is a measure of the speed of a $\Sigma\Delta$ modulator. The Nyquist sampling theorem states that to avoid aliasing, a lowpass signal must be sampled at a rate that is twice its bandwidth. As a result, specifying the Nyquist rate is equivalent to specifying the modulator input bandwidth.

2.5 DYNAMIC RANGE FORMULA

The forward path of a $\Sigma\Delta$ modulator consists of a series of integrators, and a quantizer. Fig. 2.2 illustrates an example modulator. The effect of the feedback loop is to bring the average value at the first integrator input to zero. This implies that the output of the D/A converter is on average equal to the input signal $X(z)$. Since the

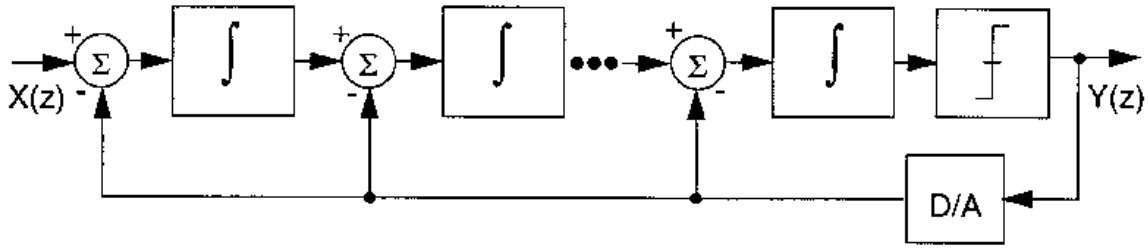

Figure 2.2: $\Sigma\Delta$ modulator block diagram.

output of the D/A converter is merely an analog representation of the digital output $Y(z)$ of the quantizer, it follows that $Y(z)$ on average equals to $X(z)$. If the modulator samples the input signal at a higher rate than required by the Nyquist sampling criterion and multiple samples are averaged to produce a digital output $Y(z)$, the $\Sigma\Delta$ modulator can then be used as an oversampled A/D converter.

Assume that each integrator has the transfer function given by:

$$I(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.2}$$

If we further assume that the quantizer and D/A converter can be modeled as additive error sources, then a linearized transfer function of an Lth order $\Sigma\Delta$ modulator neglecting delays can be expressed as

$$Y(z) = X(z) + (1 - z^{-1})^L E(z) - E_{DAC}(z) \tag{2.3}$$

Equation (2.3) indicates that errors in the D/A converter add directly at the input of the $\Sigma\Delta$ loop. This implies that the D/A converter must be linear to the full resolution of the $\Sigma\Delta$ modulator to avoid degrading the overall modulator performance. One way to ensure that this linearity constraint is met is to use a single-bit quantizer and two-level D/A converter. A two-level D/A converter is inherently linear (it can only result in a dc offset at the input of the modulator [8]). Multi-bit D/A converters need some kind of calibration to meet this linearity constraint [11].

The overall quantization noise power in the baseband $(-f_B, f_B)$ can be found by

integrating the quantization error term in (2.3) evaluated on the unit circle [8].

$$\begin{aligned} S_q &\approx \sigma_e^2 \int_{-f_B}^{f_B} |(1 - e^{j2\pi f/f_S})^L|^2 df \\ &\approx \sigma_e^2 \frac{\pi^{2L}}{2L+1} \frac{1}{M^{2L+1}} \end{aligned} \tag{2.4}$$

σ_e^2 in (2.4) is the variance of the quantization error. If the quantizer has a linear input range $(-\frac{\Delta}{2}, \frac{\Delta}{2})$ and B bits of resolution, it follows that the one least significant bit (LSB) will have a value

$$\delta = \frac{\Delta}{2^B - 1} \tag{2.5}$$

Assuming that the quantization error can be modeled as white and is uniformly distributed between $(-\frac{\delta}{2}, \frac{\delta}{2})$, then from a statistical analysis the quantization noise power can be expressed as

$$\sigma_e^2 = \frac{\delta^2}{12} = \frac{\Delta^2}{12(2^B - 1)^2} \tag{2.6}$$

Combining the results of (2.4),(2.5) and (2.6), the dynamic range of a $\Sigma\Delta$ modulator is calculated as [9]

$$DR = \frac{3}{2} \frac{2L+1}{\pi^{2L}} M^{2L+1} (2^B - 1)^2 \tag{2.7}$$

Equation (2.7) indicates that the dynamic range of a $\Sigma\Delta$ modulator is a strong function of the oversampling ratio and the order of the modulator loop. It is important to note that, especially for single-bit quantizers and two-level DACs, the white noise assumption is not a good one. Furthermore, the stability of $\Sigma\Delta$ modulators is an important concern and in general the practical dynamic range figures significantly deviate from the ideal formula. Thus, (2.7) should be viewed as an upper bound on the dynamic range.

2.6 FUNDAMENTAL LIMITS OF POWER DISSIPATION

In order to design a low-power low-voltage modulator, it is first necessary to understand where the power is going in sigma-delta modulators and what are the fundamental power limits.

The key circuit building block in a sigma-delta modulator is the integrator. Typically implemented using switched-capacitor techniques, the integrators will dominate the power dissipation of the modulator. The minimum achievable power dissipation is set by the need to charge and discharge capacitors of a given size at a given speed. This will be referred to as the dynamic power limit. In practice, switched-capacitor circuits are implemented using amplifiers which have static bias currents and burn significantly more power than the dynamic limit. In this section, both the dynamic and static power limits for switched-capacitor integrators employed in an oversampled system will be investigated.

2.6.1 Dynamic Power Dissipation

The dynamic power dissipation limit assumes that the only power dissipated in a SC integrator is that which is required to charge and discharge the sampling capacitor. This is the absolute lower bound on the achievable power dissipation in an SC circuit. Suppose the amplifier in Fig. 2.3 delivers just the required charge for the sampling capacitor, dissipates no static power and introduces no additional noise into the circuit. Let the system Nyquist rate be f_N and oversampling ratio be M. The maximum voltage swing will be limited by the power supply Vdd. Then, it follows that the integrator power will obey the relationship in 2.8.

$$P \propto C_S V_{dd}^2 f_N M \tag{2.8}$$

Now consider the noise introduced by the sampling process. The circuit in Fig.

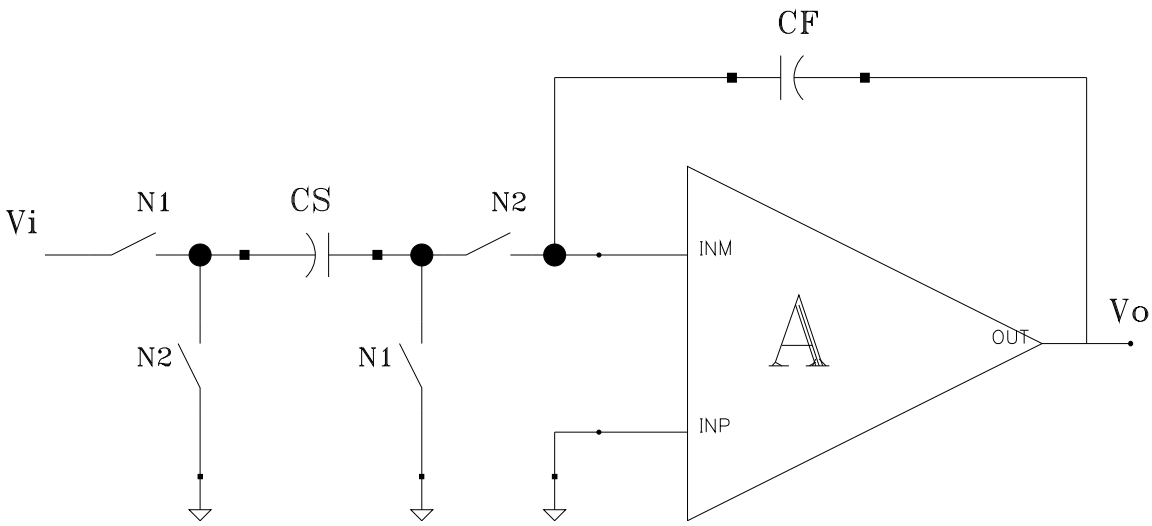

Figure 2.3: Switched-Capacitor integrator

2.4 is a switched-capacitor MOS sample and hold circuit. When the switch is on, the voltage across the capacitor tracks the input voltage. At the instant the switch opens, a sample of both the input signal and the noise due to the switch is held on the capacitor. Since the switch is in the triode region, the single-sided power spectral density of the noise given in 2.9 models the switch by its effective on resistance Ron [46]. The quantity of interest is not the power spectral density but the total inband noise power which can be found by integrating the power spectral density accounting for the bandwidth of the switch and capacitor as in 2.10. Note that $P_{N,TOT}$ represents the

$$\overline{v}^2 = 4kTR_{on}\Delta f \tag{2.9}$$

$$P_{N,TOT} = \int_0^\infty \frac{\overline{v}^2}{\Delta f} \frac{df}{|1 - j2\pi R_{on}C_S f|^2} = \int_0^\infty \frac{4kTR_{on}}{1 + (2\pi R_{on}C_S f)^2} df = \frac{kT}{C} \tag{2.10}$$

total sampled noise in the interval $(\frac{-f_s}{2}, \frac{f_s}{2})$ where f_s is the sampling frequency. Since the sampling process causes uncorrelated noise from higher frequencies to alias into this frequency region, the noise may be modeled as white with the two-sided

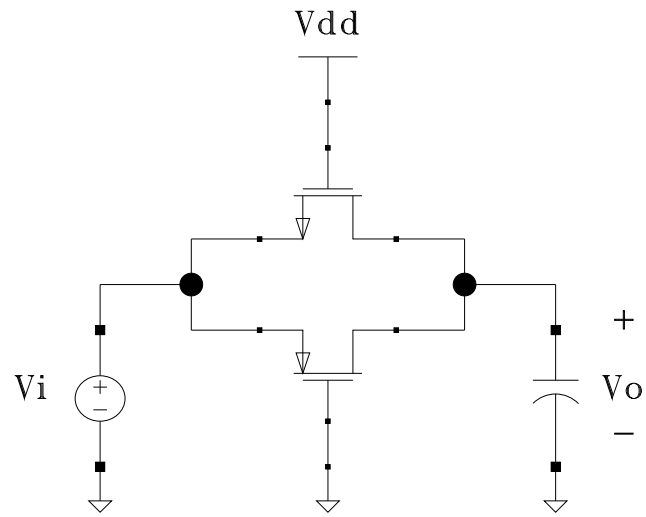

Figure 2.4: CMOS sample and hold circuit

power spectral density in 2.11. Since this is an oversampled system, only noise in the region $(-f_b, f_b)$ corrupts the desired signal.

$$S_N = \frac{kT}{f_s C_S} \tag{2.11}$$

The noise power in the region of interest (P_N) is simply the integral of the power spectral density over the bandwidth in 2.12.

$$P_N = \int_{-f_b}^{f_b} \frac{kT}{f_s C_S} df = \frac{2 f_b kT}{f_s C_S} = \frac{kT}{M C_S} \tag{2.12}$$

Note that the overall noise is independent of the switch resistance and inversely proportional to the sampling capacitance. In addition, the noise is inversely proportional to the oversampling ratio which implies that oversampling ratio and capacitor size trade off for a fixed noise specification.

We also need to relate the thermal noise to the dynamic range requirement for a switched-capacitor integrator. Assume that the maximum signal power is limited by the power supply voltage Vdd. Then, it follows that the dynamic range obeys the relationship in 2.13. Note that the dynamic range is proportional to the capacitor

size, the oversampling ratio and the square of the power supply voltage. This dynamic range expression does not include quantization noise, but for this analysis it is assumed that the modulator is thermal noise limited.

$$DR \propto \frac{MC_S V_{dd}^2}{kT} \tag{2.13}$$

We can now relate power dissipation to dynamic range by combining equations 2.8 and 2.13. This is given in 2.14.

$$P \propto kT(DR)f_N \tag{2.14}$$

As seen in 2.14, the dynamic power limit for an oversampled switched-capacitor circuit is independent of the oversampling ratio and the power supply voltage. Power and speed trade off since power is directly proportional to the Nyquist rate f_N. In addition, power and noise trade off since power is directly proportional to dynamic range.

2.6.2 Static Power Dissipation

In SC integrators, significant static power is dissipated in the operational amplifiers. Fig. 2.5 illustarates the simplest model of an operational amplifier driving a series of capacitors [4]. The amplifier is biased at a current (I) and therefore dissipates static power given by 2.15.

$$P = V_{dd} I \tag{2.15}$$

With a series of simplifying assumptions, it is possible to relate the static power to fundamental parameters of the system:

- Assume the device is biased at fixed $V_{GS} - V_T$ which implies that the device transconductance (g_m) is directly proportional to the bias current (I).

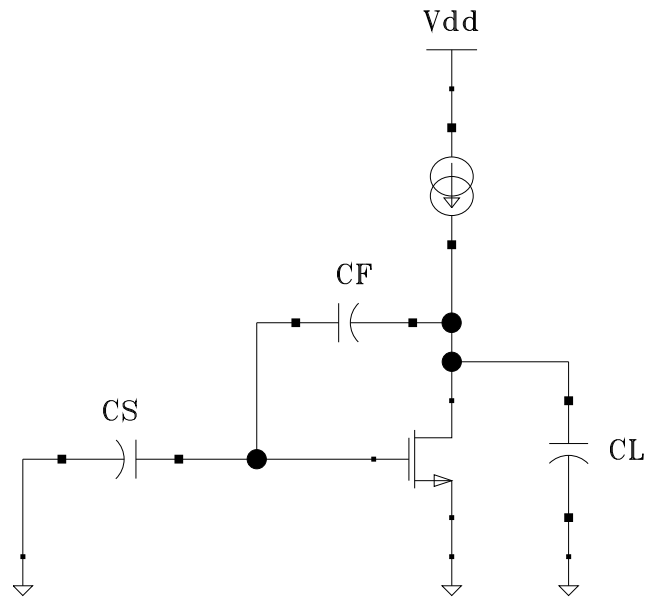

Figure 2.5: Single transistor op amp model of a switched-capacitor integrator

- Assume that the feedback factor (f) given by 2.16 is fixed. This is equivalent to assuming that the gate capacitance C_{GS} of the transistor is small compared to the sampling capacitance.

$$f = \frac{C_F}{C_F + C_S + C_{GS}} \sim \frac{C_F}{C_F + C_S} \tag{2.16}$$

- Assume that the total capacitive ($C_{L,TOT}$) loading on the operational amplifier given by 2.17 is dominated by the sampling network. Note that the device parasitics and any external load capacitance has been lumped into C_L.

$$C_{L,TOT} = \frac{C_F(C_S + C_{GS})}{C_F + C_S + C_{GS}} \sim \frac{C_F C_S}{C_F + C_S} \tag{2.17}$$

A single transistor amplifier has a single pole settling characteristic with time constant given by 2.18. At a given sampling rate and for a given dynamic range the amplifier must settle to a certain accuracy which can be defined by a number of single pole time constants. This implies that the time constant can be related to the sampling frequency though the proportionality in 2.19.

$$\tau = \frac{C_{L,TOT}}{f g_m} = \frac{C_S}{g_m} \tag{2.18}$$

$$\tau \propto \frac{1}{M f_N} \tag{2.19}$$

Using the first assumption above and substituting with the result from 2.18, 2.15 can be rewritten as the proportionality in 2.20.

$$P \propto V_{dd} g_m = \frac{V_{dd} C_S}{\tau} \tag{2.20}$$

Substituting the results from 2.13 and 2.19 into 2.20 yields the static power limit in 2.21.

$$P \propto \frac{(DR) k T f_N}{V_{dd}} \tag{2.21}$$

Like the dynamic power dissipation limit, the static power limit is independent of oversampling ratio. In addition, dynamic range and power trade off as do speed and power. However, the static limit is inversely proportional to the power supply voltage which suggests that the trend toward lower supplies favored by digital circuits and required by deep submicron CMOS processes will have an adverse effect on power dissipation.

Chapter 3

TECHNIQUES FOR IMPROVING RESOLUTION OF HIGH-SPEED ($\Sigma\Delta$) OVERSAMPLING A/D CONVERTERS

3.1 INTRODUCTION

In this chapter, a brief summary of possible approaches to improve the resolution of High-Speed Oversampling $\Sigma\Delta$ ADCs will be presented. A simple observation of the DR equation, (2.7), reveals that there are 3 main ways of achieving higher resolution in a $\Sigma\Delta$ ADC. These are: increasing the oversampling ratio, using a higher order loop filter and increasing the number of bits for the quantizer that is used inside the feedback loop.

3.2 INCREASING THE OVERSAMPLING RATIO

The first look at (2.7) reveals that DR is strongly dependent on the oversampling ratio (M). The expression

$$\Delta(SNR) = 3(2L+1)dB \tag{3.1}$$

in which L is the order of the $\Sigma\Delta$ modulator, describes the increase of the SNR for every doubling of the sampling rate [11]. This translates directly in terms of the resolution as

$$\Delta(Resolution) = (L + 0.5)bits \tag{3.2}$$

In the specific case of a second-order loop ($L = 2$), this improvement is 15 dB or 2.5 bits [12]. Because of this strong dependence, increasing the oversampling ratio is the most attractive method for improving the resolution of $\Sigma\Delta$ modulators.

Although using high oversampling ratios is desirable in a $\Sigma\Delta$ modulator design, it is not always practically possible to increase the clock frequency because the analog circuits may not be able to meet the performance requirements of a very high clock rate. In switched-capacitor (SC) implementations, two non-overlapping clock waveforms are needed. In the first half of the clock period, sampling, the input signal and the signal fed back from the output of the feedback quantizer are sampled onto the sampling capacitors. In the second half, integration, this voltage is integrated. Thus, only 50% of one clock cycle is available for settling to the desired accuracy. As the clock rate is increased, performance of the operational amplifier has to be increased. Specifically, the slew rate (SR) and the gain-bandwidth product (GBWP) of the operational amplifier must be increased in accordance with the clock rate.

Other than the increased performance required from the operational amplifiers, there are two main concerns related with using a high oversampling ratio in a $\Sigma\Delta$ modulator: the sampling jitter and excessive power consumption.

3.2.1 Sampling Jitter

The sampling theorem states that a sampled signal can be perfectly reconstructed provided that the sampling frequency is at least twice the signal bandwidth and that the sampling occurs at uniformly distributed instances in time. An anti-aliasing filter preceeding the sampler ensures that the first of these requirements is fulfilled. Sampling clock jitter results in non-uniform sampling and increases the total error power in the quantizer output. An upper limit for the tolerable clock jitter is derived in [13].

$$\Delta t \leq \frac{1}{2\pi B \cdot 2^b}\sqrt{\frac{2M}{3}} \tag{3.3}$$

The error caused by clock jitter is inversely proportional to the oversampling ratio M and adds directly to the total error power S_N at the output of the A/D converter. The amount of clock jitter that can be tolerated decreases for an increase in oversampling ratio [13].

As an example, if the baseband error power induced by clock jitter to be no larger than the quantization noise resulting from an ideal second-order modulator with 1-bit quantization, then it is necessary that $\Delta t \leq 874ps$ for a 20 kHz bandwidth.

3.2.2 Dependence of Power Dissipation to Clock Frequency

A typical operational-transconductance amplifier (OTA) has a gain-bandwidth product (GBWP) given by

$$GBWP = \frac{g_M}{C} \tag{3.4}$$

where g_M is the transconductance of the input stage and C is the total equivalent loading capacitance in its integrator functionality. When this OTA is implemented in a CMOS technology, the transconductance of the input stage according to a simplified second-order model [14] is given by

$$g_M = \sqrt{2K\frac{W}{L}I_{DS}} \tag{3.5}$$

where K is the gain constant of the transistor, $\frac{W}{L}$ is the aspect ratio, and I_{DS} is the bias current. For most typical SC integrators, if the value of the sampling capacitors is kept constant, doubling the clock frequency requires doubling the GBWP of the op amp. Thus the combined effects of (3.4) and (3.5) show that the bias current has to be quadrupled, or alternatively doubled in combination with the doubling of the transistor ratios [12].

Table 3.1: Theoretical dynamic range of modulators having different loop orders (OSR=32 and single-bit feedback quantization is assumed).

L	SNR (dB)	Resolution (bits)
2	64.1	10
3	85.7	14
4	107	17

3.3 INCREASING THE ORDER OF THE MODULATOR

The DR equation, (2.7), implies that the quantization noise power can be lowered below a desired level by simply inserting more integrators into the forward path of the modulator given in Fig. 2.2. Table 3.1 illustrates the dynamic range predicted by (2.7) for different loop orders (an oversampling ratio of 32 and single-bit quantization in the feedback is assumed in preparing this table).

At first look, increasing the order of noise shaping is a very attractive way of improving the resolution of a $\Sigma\Delta$ modulator. Especially in high-speed applications, where the increase in the oversampling ratio is practically restricted to values of 32 or less, utilizing a more aggressive noise transfer function becomes even more important. But high-order modulators have some practical limitations and because of these limitations, dynamic figures only well below predicted by equation (2.7) can be achieved.

In fact, there are two different ways of implementing an Lth order $\Sigma\Delta$ modulator: single-loop and cascade architectures. Although they are both intended to realize an Lth order noise shaping, they have some advantages and disadvantages with respect to each other. So, a separate treatment of both architectures will be appropriate.

3.3.1 Single-Loop Modulators

A single-loop $\Sigma\Delta$ modulator is the one shown in Fig. 2.2. It is a cascade of integrators and each integrator accepts the output of the previous integrator and the output of the D/A converter in the feedback as its inputs.

In Chapter 2, the $\Sigma\Delta$ modulator is considered as a linear system. However, in reality, a $\Sigma\Delta$ modulator is a highly nonlinear circuit. When more than two integrators are cascaded in the loop filter as shown in Fig. 2.2, the modulator may become unstable [20]. When third or higher-order modulators are excited by a large input signal, the two-level quantizer overloads implying increased quantization noise. In the forward path of the modulator, this large quantization noise is then amplified, resulting in large, uncontrollable, low-frequency oscillations [3]. Even if the modulator is not driven by an input signal, instability may occur depending on the initial conditions of integrators [39]. Clearly, stability is an absolute necessity if a $\Sigma\Delta$ modulator is to be usable [19].

Because of these complicating factors, a designer sorts to simulations for the verification of the stability and the achievable SNR figure out of a $\Sigma\Delta$ modulator architecture. Fig. 3.1 is a result of such simulations for different modulator orders and oversampling ratios.

In addition to single-loop modulators having a noise transfer function (NTF) with all of its zeros at dc, it is also possible to spread the zeros of NTF across the band of interest [10]. By spreading the zeros across the band of interest, the in-band noise power can be reduced.

A detailed derivation of the location of optimum zeros for a modulator order up to 8 can be found in [19]. As a result of this optimum zero placement, significant SNR improvements are achieved when compared to modulators using NTF's with coincident zeros (all zeros at dc). Table 3.2 shows this SNR improvement for modulator orders upto 4. As this table shows, optimized zero placement can yield an improvement amounting to several bits in high-order modulators.

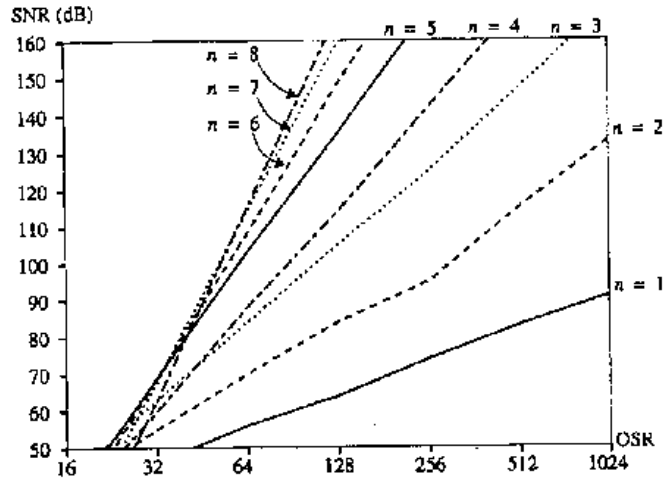

Figure 3.1: Maximum SNR achievable by modulators of order n with coincident zeros, as a function of the oversampling ratio.

Table 3.2: Improvement in SNR of modulators having different loop orders due to the optimum placement of NTF zeros.

L	Δ SNR (dB)
2	3.5
3	8
4	13

3.3.2 Cascade Modulators

A second way of realizing *Lth* order noise shaping is by cascading lower order modulators. In a cascaded architecture, each of the multiple stages is itself a single-stage $\Sigma\Delta$ modulator. As depicted in Fig. 3.2, the quantizer error in each stage serves as the input to the following stage. The output of that following stage is then an approximation of the quantizer error. By subtracting the approximate error from the previous stage's output, most of the quantization error can be canceled, and the performance of a cascaded architecture is approximately equivalent to that of a single-stage architecture having the same total number of integrators. The important thing is that, unlike the single-loop modulators, the instability is avoided because each individual stage is a self-contained first- or second-order $\Sigma\Delta$ modulator with only one or two

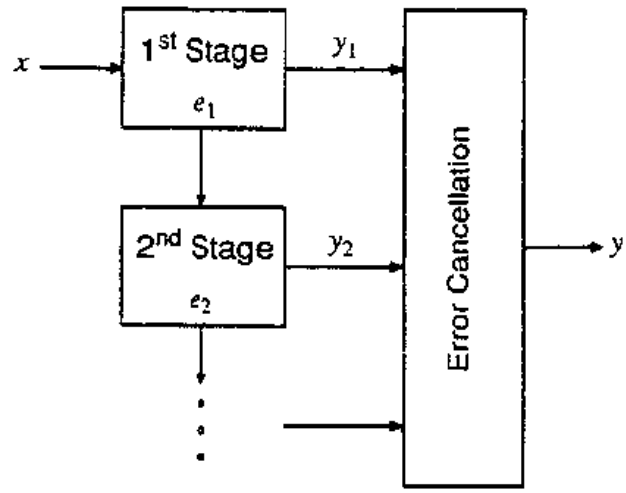

Figure 3.2: Cascaded modulator architecture.

integrators in its forward path.

Because the instability concern is removed, cascade modulators give better performance and their DR figures are much closer to the upper bound defined by (2.7) as compared to single-loop architectures. But there is another problem associated with the design of cascade modulators: the component mismatch problem. The operation of cascade modulators and the importance of component mismatch problem is investigated in detail in [8] on a third-order cascade modulator(implemented by cascading a second-order first stage with a first-order second stage).

3.4 MULTIBIT QUANTIZATION

Multibit quantization can be identified as a third way in order to improve the dynamic range of a given modulator.

The dynamic range equation, (2.7), obtained through the simple linear analysis suggests a 6-dB per bit SNR improvement in a $\Sigma\Delta$ modulator. Especially in high-speed applications, where the oversampling ratio should be kept small, this is pretty important. Fig 3.3 shows the SNR as a function of resolution m, for an m-bit second-order modulator loop [21]. According to this figure, even with a second-order loop

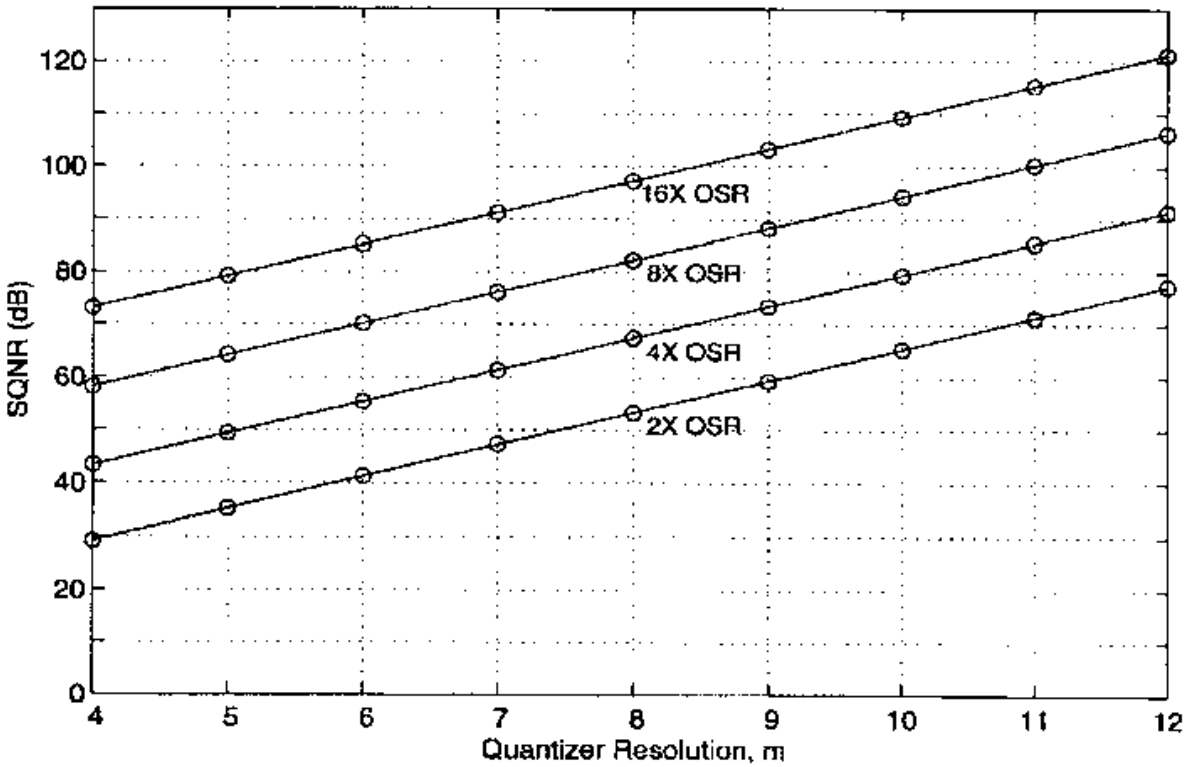

Figure 3.3: Signal-to-quantization noise of a second-order multibit modulator as a function of the number of feedback bits m.

and a low oversampling ratio such as 16, it is possible to achieve more than 80-90 dB of SNR with the use of multi-bit quantizers inside the feedback loop. An additional benefit of multibit quantization is that it enhances system stability. This makes it possible to more closely approach the theoretical SNR through better pole placement [22, 23].

The main problem associated with the use of multi-bit quantization is the non-linearity of the D/A converter, which is used to convert the digital output of the $\Sigma\Delta$ modulator into analog in order to be able to feed that signal back into the first integrator. DACs having only two levels of quantization do not suffer from nonlinearity problems. In fact, it is this property that has been primarily responsible for the popularity of $\Sigma\Delta$ modulation and it is the reason that many $\Sigma\Delta$ modulators employ two-level quantizers. When more than two levels of quantization are used, any

real DAC will have mismatches in the spacing between the levels. Any mismatches in the output level spacing of the internal DAC translate directly to input referred distortion and increased noise [26], which significantly reduces the SNR at the output of the modulator.

As a consequence of this nonlinearity problem, multibit quantization brings less performance improvement than theoretically expected 6-dB per bit improvement. Thus, in order to fully benefit from this technique, it is necessary to alleviate the nonlinearity problem. In order to correct DAC nonlinearity in $\Sigma\Delta$ ADCs, digital self-calibration [27] and dynamic element matching (DEM) [28, 25, 24] have been used. A drawback of digital self-calibration is the added complexity to the system design. The DEM techniques are easier to implement but they are prone to aliasing [24]. Nevertheless, the DEM approach is more popular in the literature. Different DEM techniques have been proposed in the literature. These are: randomization [25], clocked averaging [28], individual level averaging [28], and data-weighted averaging [24].

Chapter 4

MULTIRATE ΣΔ MODULATORS

4.1 INTRODUCTION

All the techniques mentioned in chapter 3 are conventional methods of achieving high performance from ΣΔ modulators. However, as the signal band of interest increases, new methods have to be devised for an efficient design of A/D converters employing such modulators. For example for xDSL and wireless applications, new high performance CMOS A/D converters with high accuracy are required. For these application several modulators have been recently proposed with different topologies [21, 29, 30, 31, 32, 33]. Usually they are high-order cascaded structures of single bit first- or second-order stages, with a multibit quantizer at the last stage of the cascade, showing that selecting the optimal modulator is a compromise between modulator order, oversampling ratio and resolution of internal quantizers.

Conventional first-order analysis shows that, for a given dynamic range (DR), power consumption of ΣΔ modulators does not depend on the oversampling ratio M. For switched capacitor implementations, this analysis assumes that the DR is limited by the kT/C noise of the first integrator. Increasing M has a twofold consequence on the first integrator opamp. On the one hand, the capacitor load can be decreased, as the kT/C noise is inversely proportional to M. On the other hand, the opamp has to settle faster. Both effects counteract so that power consumption does not change. Similar first-order analysis can be done for continuous-time and switched-current implementations [17].

Nevertheless, this simple analysis assumes a one-pole model of the opamp, which

is only valid for low sampling frequencies. Therefore, it does not apply for new high-speed modulators, where opamps are operated near their maximum bandwidth. In that case, power consumption dramatically increases with sampling frequency because 1) parasitic capacitances become a significant fraction of the total capacitance, and 2) clock nonoverlap, and rise and fall times become a significant fraction of the clock cycle. This issue was addressed in [18], where an analysis of three different opamp topologies including first order parasitics, showed a significant increase of the power consumption in the first integrator of a $\Sigma\Delta$ modulator for a high sampling frequency. A recent example can be seen in [30] and [32], where two modulators with similar performances were built in the same technology. The implementation in [30] used $M = 24$, while the implementation in [32] used $M = 16$, achieving more than a 70% of power saving.

In these approaches the oversampling ratio was unique for all the integrators. However, the use of different oversampling ratios along the structure of a $\Sigma\Delta$ modulator can alleviate some of the major problems faced in its design. As the integrators have a considerable amount of gain at frequencies in the baseband, baseband noise and distortion occurring in the integrators succeeding the first one are greatly attenuated when referred back to the modulator input. Therefore, the noise and distortion performance of a $\Sigma\Delta$ modulator is primarily determined by the first integrator, which, in turn, determines the power consumption of the full converter. A reduction in the oversampling ratio of the first integrator(s) of a $\Sigma\Delta$ modulator can be compensated by an increase in the oversampling ratio of the last integrators, whose contribution to power consumption is not so significant. In this sense, the proper selection of the oversampling ratio in each integrator of a single-loop or a cascaded- $\Sigma\Delta$ modulator is another architectural decision to be considered in the design of high-resolution, low-power, high-speed $\Sigma\Delta$ modulators.

In single-loop multirate $\Sigma\Delta$ modulators, the first integrator works at a lower oversampling ratio than the rest of the integrators [34]. The second order version is shown in Fig 4.1. As the modulator output in Fig 4.1 (a) has a high sampling

rate, it has to be down-sampled before being fed back to the first integrator. In order to avoid aliasing a digital filter $H(z)$ and one DAC have to be included in the feedback path. This architecture can be also considered to be a multibit modulator where the multibit quantizer in the forward path has been replaced by a single bit one, operating at a higher frequency, by the increase in the sampling rate of the last integrator; therefore, it is called a Multibit-Multirate (MM-$\Sigma\Delta$) Modulator.

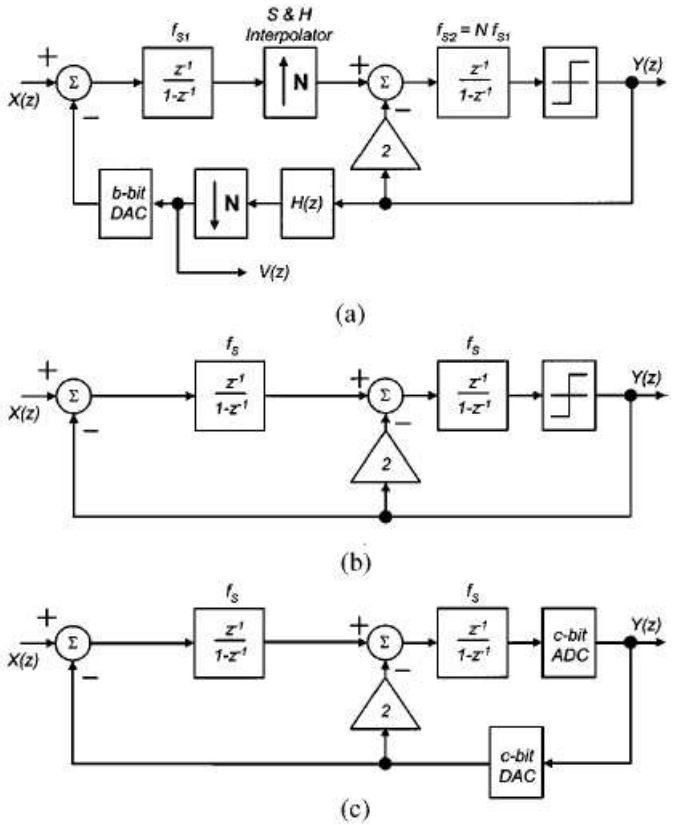

Figure 4.1: Architecture of second-order $\Sigma\Delta$ modulators (a) MM-$\Sigma\Delta$ modulator (b) Conventional single-bit architecture (c) Conventional multibit architecture.

4.2 MM-$\Sigma\Delta$ MODULATOR

Fig 4.1 (b) shows the architecture of a conventional second-order $\Sigma\Delta$ modulator. Let f_S be the sampling rate and let f_N be the input signal Nyquist frequency. The

oversampling ratio is defined as $M = f_S/f_N$. Unlike the conventional $\Sigma\Delta$ modulator of Fig 4.1 (b), in the MM-$\Sigma\Delta$ modulator of Fig 4.1 (a), the first and second integrators are operated at different sampling frequencies. Therefore, this modulator has two different oversampling ratios, $M_1 = f_{S1}/f_N$ and $M_2 = f_{S2}/f_N = N * M_1$, where N is the oversampling ratio increment of the second integrator.

In the MM-$\Sigma\Delta$ modulator, the output y has to be downsampled at rate f_{S1} before being fed back to the first integrator. To avoid aliasing, y is filtered by means of the digital filter $H(z)$, before being decimated. For this purpose, simple comb-type digital filters can be used [11]. In a practical implementation, the modulator output would be taken from v, rather than from y, to benefit from the decimation process done in the feedback path. After decimation, signal v is ($b = 2log_2N$)-bit wide, and a b-bit DAC is required to convert it back to the analog world.

The MM-$\Sigma\Delta$ modulator can be also considered to be a multibit $\Sigma\Delta$ modulator, where the multibit quantizer in the forward path [Fig 4.1 (c)] has been replaced by a single bit one, operating at a higher frequency, by the increase in the clock rate of the second integrator. In the following sections, a relation between the word lengths in the feedback path of a MM-$\Sigma\Delta$ modulator and of a multibit $\Sigma\Delta$ modulator with similar performances will be given.

In a MM-$\Sigma\Delta$ modulator with order higher than 2, every integrator is operated at the high frequency rate f_{S2}, except the first one which is operated at the low frequency rate f_{S1}. Note that other intermediate solutions could be considered, extending the low oversampling ratio to integrators other than the first one.

4.2.1 Analysis of the MM-$\Sigma\Delta$ Modulator

The circuit in Fig 4.1 (a) can be shown to be equivalent to the circuit in Fig 4.2. The first integrator of Fig 4.1 (a), working at the rate f_{S1}, and the sample and hold interpolator have been replaced in Fig 4.2 by an integrator working at the rate f_{S2} and a N-delay.

Using a linear model for the quantizer in Fig 4.2, the expression in (4.1) can be

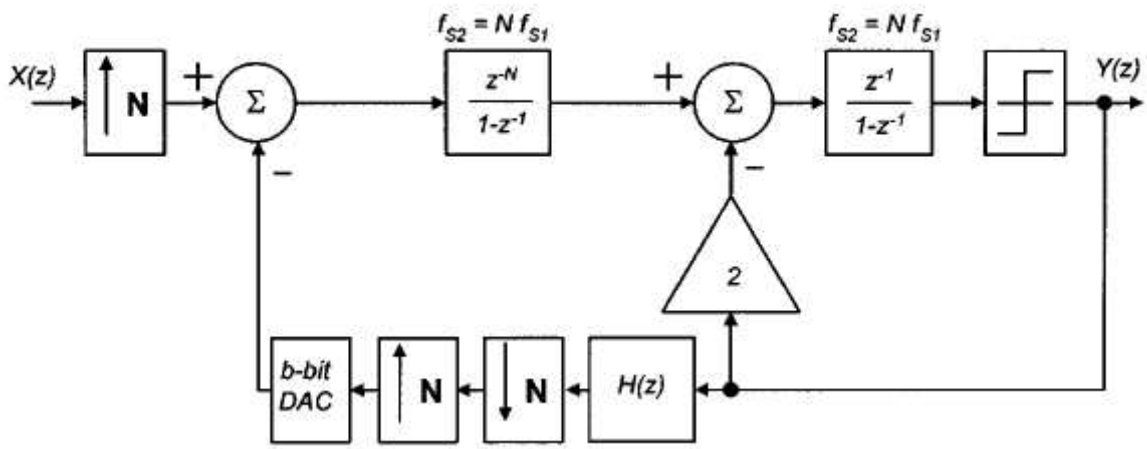

Figure 4.2: Block diagram equivalent to the MM-ΣΔ modulator of Fig 4.1 (a).

obtained where $X(z)$ is the z-transform of the subsampled input sequence and $E(z)$ is the quantization noise.

$$Y(z) = STF(z)X(z^N) + NTF(z)E(z) + W(z) \tag{4.1}$$

The second member of expression (4.1) is the summation of three terms: the input signal filtered by the signal transfer function (STF), the shaped quantization noise, and an error term, $W(z)$, due to aliasing in the decimation process. The $STF(z)$ and the noise transfer function $NTF(z)$ are given by [35]

$$STF(z) = \frac{z^{-(N+1)}}{F(z)} \tag{4.2}$$

$$NTF(z) = \frac{(1 - z^{-1})^2}{F(z)} \tag{4.3}$$

The common denominator $F(z)$ in (4.2) and (4.3) is given in (4.4).

$$F(z) = 1 - z^{-2} + \frac{1}{N} z^{-(N+1)} H(z) \tag{4.4}$$

The error term $W(z)$ is given by

$$W(z) = -\frac{1}{N} STF(z) \sum_{k=1}^{N-1} [H(ze^{-j\frac{2\pi k}{N}}) Y(ze^{-j\frac{2\pi k}{N}})] \tag{4.5}$$

When $H(z)$ is a second-order comb-type filter given by (4.6), it can be shown that for commong values of N, the spectral components of $W(z)$ folded into the signal band $[0, f_N]$ are negligible.

$$H(z) = \frac{1}{N^2} (\frac{1 - z^{-N}}{1 - z^{-1}})^2 \tag{4.6}$$

Fig 4.3 shows the ratio between the inband power of the shaped quantization noise and the contribution of the aliasing term, for different input signal amplitudes, in a MM-$\Sigma\Delta$ modulator with $N = 4$ and $H(z)$ given by (4.6). Fig 4.3 has been obtained by simulation using the model of Fig 4.2.

Based on the results shown in Fig 4.3, the term $W(z)$ can be ignored in the baseband. Besides, as $F(e^{j0} = 1/N$, and $dF/dz(ej0) = 0$, in a first order approach, the denominator $F(z)$ can be replaced by $1/N$. Then, we can write $Y(z)$ as:

$$Y(z) \approx N[z^{-(N+1)} X(z^N) + (1 - z^{-1})^2 E(z)] \tag{4.7}$$

In (4.7), the N factor which multiplies $X(z^N)$ in (4.7) cancels the attenuation introduced by the input interpolator (see Fig 4.2). Proceeding as in [11], the inband quantization noise power (QNP) is given by [35]

$$QNP(\Delta, M_1, N, 2) \approx \frac{\pi^4}{60} \frac{\Delta^2}{M_1^5 N^3} \tag{4.8}$$

where $QNP(\Delta, M_1, N, L)$ is the inband QNP of a Lth-order $\Sigma\Delta$ modulator with quantization step Δ, oversampling ratio M_1 in the first integrator, and $M_2 = NM_1$ in the rest of the stages.

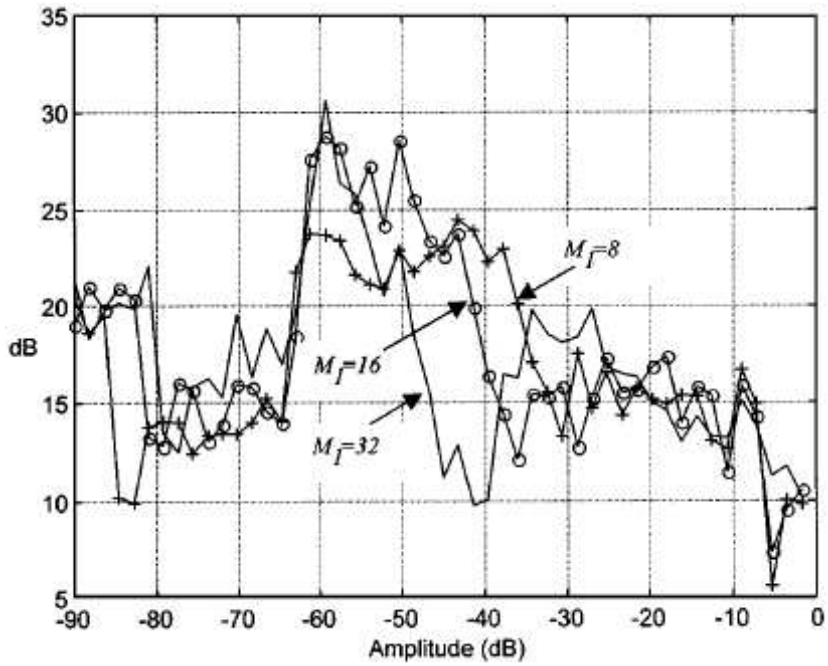

Figure 4.3: Ratio between the inband power of the quantization noise and the contribution of the aliasing terms, in a MM-$\Sigma\Delta$ modulator with $N = 4$, for three different values of the low oversampling ratio M_1.

Following a similar procedure, the inband QNP of high-order MM-$\Sigma\Delta$ modulators can be obtained

$$QNP(\Delta, M_1, N, L) \approx \frac{\pi^{2L}}{12(2L+1)} \frac{\Delta^2}{M_1^{2L+1} N^{2L-1}} \tag{4.9}$$

4.2.2 Relative Performances of MM-$\Sigma\Delta$ Modulators

To evaluate the performances of MM-$\Sigma\Delta$ modulators, the ratio between the inband QNP of a Lth-order MM-$\Sigma\Delta$ modulator with oversampling ratios M_1 and $M_2 = NM_1$, and the inband QNP of a conventional c-bit Lth-order $\Sigma\Delta$ modulator with oversampling ratio M is presented in (4.10) [35].

$$\frac{QNP(\Delta, M_1, N, L)}{QNP(\Delta/(2^c-1), M, 1, L} \approx (\frac{M}{M_1})^{2L+1} \frac{(2^c-1)^2}{N^{2L-1}} \tag{4.10}$$

From (4.10), we shall consider three cases:

- 1-bit Lth-order conventional $\Sigma\Delta$ modulator operating at the low oversampling ratio M_1 (i.e., $c = 1, M = M_1$). In this case, the ratio between the inband QNP's falls by $3(2L-1)dB$, for every doubling of the oversampling ratio increment N.

- 1-bit Lth-order conventional $\Sigma\Delta$ modulator with oversampling ratio M (i.e., $c = 1$), and a MM-$\Sigma\Delta$ modulator with $M_1 = M/2$ and $M_2 = 2M$ (i.e., $N = 4$). According to expression (4.10), the inband QNP of the MM-$\Sigma\Delta$ modulator is $3(2L-3)dB$ smaller than the inband QNP of the conventional $\Sigma\Delta$ modulator. This result shows that a lower oversampling in the first integrator can be favorably compensated by an increase in the oversampling ratio of the rest of integrators.

- c-bit Lth-order conventional $\Sigma\Delta$ modulator operating at the low oversampling ratio M_1 (i.e., $M = M_1$). According to (4.10), the MM-$\Sigma\Delta$ modulator and the c-bit conventional $\Sigma\Delta$ modulator have the same inband QNP when

$$c = log_2(N^{(L-0.5)} + 1) \tag{4.11}$$

  As expected, this result clearly shows that, compared to a multibit structure, the gain in resolution for MM-$\Sigma\Delta$ modulators comes from replacing the multibit quantizer in the forward path by a single bit one, operating at a higher frequency, by the increase in the oversampling ratio of last integrators.

Chapter 5

MODULATOR DESIGN

The objective of this research is to investigate the use of the Multirate Multibit $\Sigma\Delta$ modulator (MM-$\Sigma\Delta$) structure in the design of very low power ADC design. One of the end goals of this research is to design and implement a $\Sigma\Delta$ modulator that is tailored for wireless communications applications. Although the design will be optimized for a GSM receiver, it will be programmable and have a second mode for a wider bandwidth application like wideband CDMA (WCDMA). The modulator will be fabricated in a 90nm digital CMOS technology provided by Texas Instruments Inc.

The sections in this chapter are arranged as follows: First, the conventional implementation of a 2nd order $\Sigma\Delta$ modulator with 5 levels of quantization in its feedback path is described for comparison purposes. Then, the ideal 2nd order MM-$\Sigma\Delta$ structure and its ideal clocking scheme will be given. The practical limitations of this ideal MM-$\Sigma\Delta$ structure will be the topic of the section following this. In section 4, the proposed architecture and the clocking scheme will be explained in detail. Then, a comparison of the proposed modulator system and the modulator designed by using the conventional approach will be given. An extension of this idea into different $\Sigma\Delta$ modulator architectures will be discussed in the appendix with the sole idea of designing higher performance $\Sigma\Delta$ A/D converters in mind.

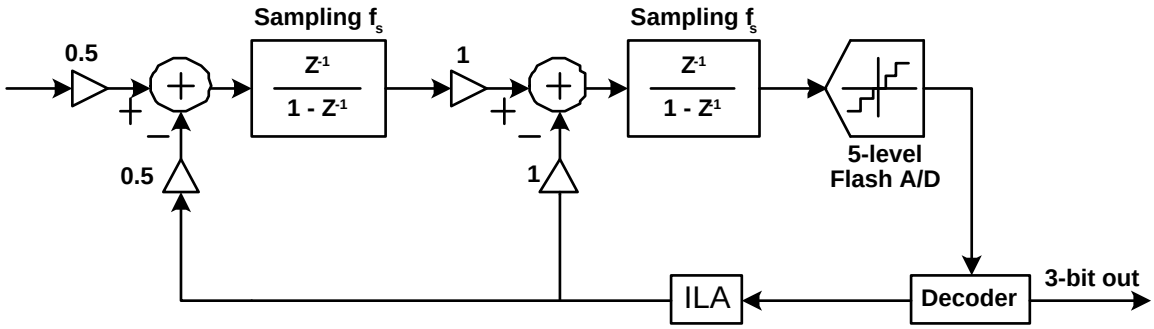

Figure 5.1: Conventional implementation of a Second Order 5-Level $\Sigma\Delta$ modulator

5.1 CONVENTIONAL SECOND ORDER 5 LEVEL $\Sigma\Delta$ MODULATOR

Fig. 5.1 illustrates a conventional implementation of a Second order $\Sigma\Delta$ modulator with 5 levels of quantization in the feedback path [36]. In this structure, both integrators run at the same sampling rate with a frequency of fs. In general, the Switched-Capacitor (SC) implementations of this structure employs two non-overlapping clock phases for the sampling and integration operations performed by the sample-and-hold network and the integrator. Therefore, if the period of the sampling clock is T=1/fs, sampling and integration operations each have T/2 time allocated for them. This means that the voltages at the output of the sampling network and the integrator output must converge to their final values within an acceptable error in T/2 time.

The quantization in the feedback path is usually implemented by employing a flash A/D converter. The main reason for this is stability. The modulator feedback loop is very sensitive to delays in the loop. Other types of A/D converters like pipeline or successive approximations A/D converters provide more accuracy than the flash converters but they also need a delay of a number of clock cycles. Such a delay causes instability. On the other hand, flash converters gives out the output to a certain input almost instantenously and so they found popular use in such modulator structures so far. However, the use of a flash A/D converter is also not without problems. In order to increase the Signal-to-Noise ratio (SNR) of a flash converter by 6dB, we need to

double the number of comparators employed. This means doubling the area and the power dissipation of the flash converter, both of which are very undesirable. Hence, the practical implementations of a flash A/D converter that will be used in such a $\Sigma\Delta$ modulator is limited to a certain number of bits. In the past, 5-bit (or 32 level) flash was sort of the limit for the designers and very few designers actually used such a 5-bit flash A/D converter in their systems [15].

Fig. 5.2 shows the floorplan of the system given in Fig. 5.1. This floorplan shows an accurate partitioning of the area to different sub-blocks. From this floorplan, we observe that the integrators and the 5 level flash A/D converter are almost the same size. Hence, the flash A/D converter consumes one third of the total area of the $\Sigma\Delta$ modulator. This is why it is not practical to use a flash A/D converter which has many levels. Furthermore, that is also why the technique described in this work is important. Because, by means of this technique, we may replace the flash with a much simpler system and save both area and power.

5.2 IDEAL SECOND ORDER MM-$\Sigma\Delta$ MODULATOR

Consider an L-th order MM-$\Sigma\Delta$ modulator with first integrator OSR of M_1 and upsampling of N in the remaining stages. Also, consider a conventional c-bit L-th order $\Sigma\Delta$ modulator with an OSR of M=M_1. These two modulators have the same inband quantization noise power (QNP) provided [35]:

$$c = log_2(N^{(L-0.5)} + 1) \tag{5.1}$$

Equation 5.1 shows the relation between the quantizer resolution in a conventional modulator and the upsampling ratio in a MM-$\Sigma\Delta$ modulator for an L-th order system.

From the theory of conventional $\Sigma\Delta$ modulators, we determine that a 2nd order loop with a quantizer resolution of 2 bits is needed to achieve our design specifications.

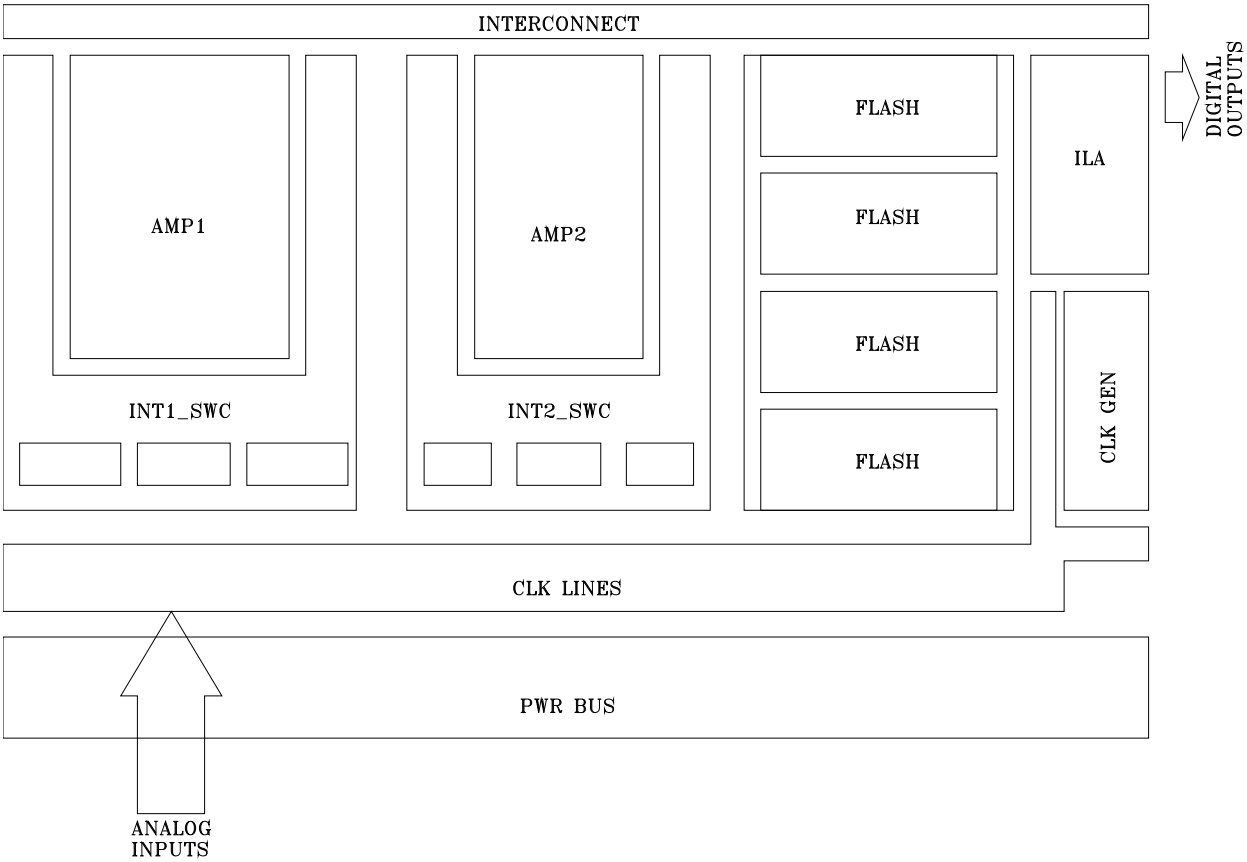

Figure 5.2: Layout floorplan of the 2nd Order 5-Level $\Sigma\Delta$ modulator given in Fig 5.1

The required OSR is 36 and 9 for GSM and WCDMA, respectively. From equation 5.1, with L=2 and c=2, we find the upsampling ratio N of the corresponding MM-$\Sigma\Delta$ modulator is 2. Thus, the modulator in Fig 5.3 is designed for optimum power and area as well as good performance.

In this structure, the quantizer is only a single-bit comparator. Since the second integrator and comparator is running twice as fast as the first integrator, the output needs to be downsampled before it is fed back to the first integrator. A second-order digital FIR filter is used as a low pass filter to avoid aliasing. After this filter, the data is downsampled. Single-bit comparator and the FIR filter along with an upsampling in the second integrator replaces a bulky flash A/D converter if we were to design a second order modulator with conventional multibit quantization. In order to remedy the DAC non-linearity problem, a dynamic element-matching (DEM) block using the

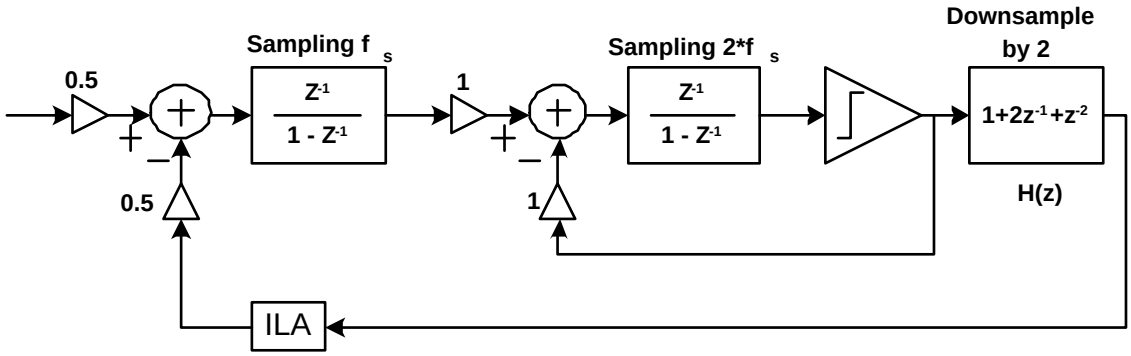

Figure 5.3: Second Order MM-ΣΔ modulator

individual level averaging (ILA) algorithm is included in the feedback.

The transfer function of the comb filter is:

$$H(z) = 1 + 2z^{-1} + z^{-2} \tag{5.2}$$

The comparator preceeding the comb filter can generate only two different outputs 0 and 1. Hence, at the output of the comb filter, we can observe 5 different output values 0,1,2,3,4.

The actual strength of the MM-ΣΔ systems comes from the fact that the flash A/D conveter, which is bulky and consumes significant static power, is replaced by a comparator and a simple FIR filter along with an increase in the sampling rate of the second integrator. Significant area and power savings can be achieved through the use of these systems.

5.2.1 Practical limitations of a MM-ΣΔ modulator

The MM-ΣΔ modulator that is explained in the last section is an idealized system and so it does not take into account the settling limitations of the amplifiers used inside the integrators. In the ideal system, we assume that settling at the output of the integrators happen instantenously. The fundamental problem of MM-ΣΔ modulators shows itself in the practical implementation. Every amplifier is designed with a certain bandwidth and so the amplifier outputs settle to their final values within an acceptable error in a certain time. In order to increase this bandwidth and improve the settling

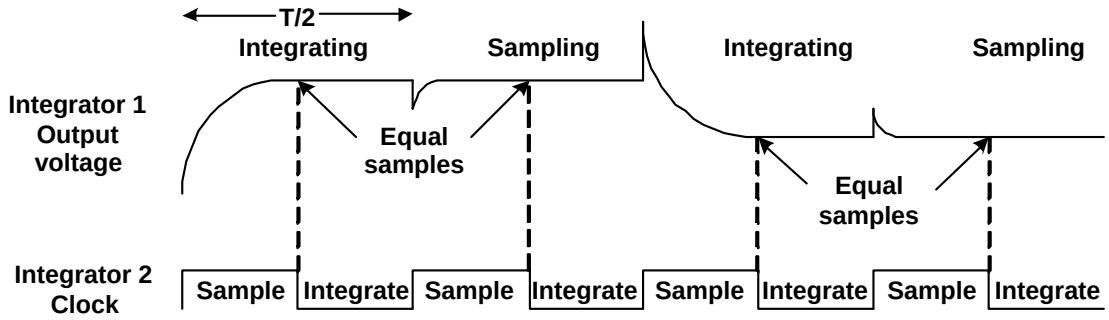

Figure 5.4: Sampling and integration half cycles for the Second Order 5-Level MM-$\Sigma\Delta$ modulator

characteristics, one needs to increase power dissipation of the amplifier. Thus, if amplifiers settle much faster than needed, then they consume more current than is really needed. It is a good practice in terms of saving power to design the amplifier such that it utilizes the whole half period with some margin for slewing and settling of the amplifier output.

Therefore, in the modulator depicted in Fig 5.3, there is an important problem that needs to be addressed for the circuit implementation of this architecture. The second integrator samples the output of the first integrator twice in one clock period T=1/fs. If the first integrator uses the whole half clock cycle T/2 to slew and settle to its final value, then one of the samples that the second integrator is receiving from the first integrator output will not be a valid sample. So, for correct operation, the settling behavior should be such that the first integrator output settles to its final value in about T/4 time. This case is depicted in Fig 5.4. However, then we will have to design an amplifier for the first integrator that is able to run with a 2*fs clock, which means extra current consumption.

Consequently, in its current form, an MM-$\Sigma\Delta$ implementation is not useful. A technique should be devised to get the benefits of an MM-$\Sigma\Delta$ without requiring the first integrator to be as fast as the practical implementations impose.

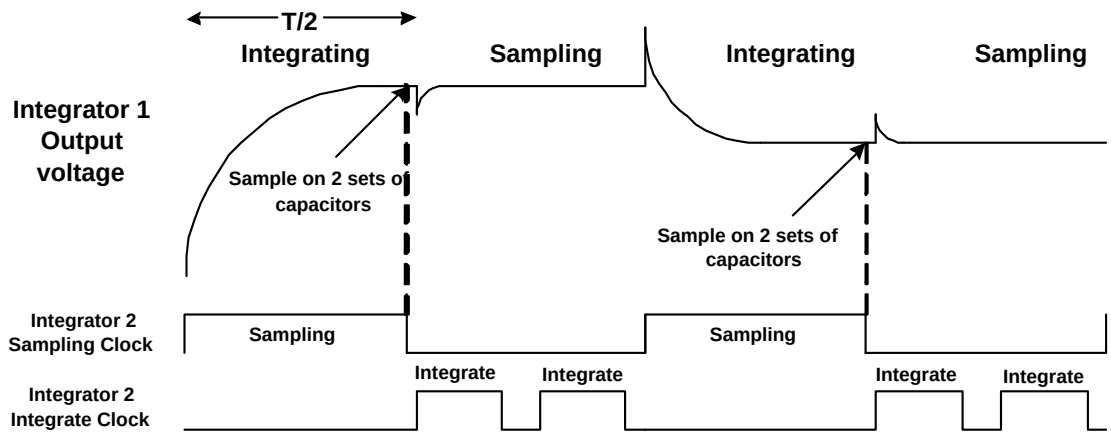

Figure 5.5: Sampling and integration half cycles for the Proposed MM-ΣΔ modulator

5.3 PROPOSED ARCHITECTURE AND CLOCKING SCHEME

A power efficient method is proposed in Fig 5.5 to implement the sampling and integration operations. First note that in the case depicted by Fig 5.4, the two samples received by the second integrator from the output of the first integrator in the same clock period are exactly the same provided the first integrator is designed to settle fast enough. In Fig 5.5, we let the first integrator use the full half clock period for integration (during N2 is high in Fig 5.9). At the same time, the sampling switches of the second integrator are also ON and the sampling capacitors of the second integrator are charging. The second integrator has two sampling capacitors instead of only one. After the first integrator output settles to its final value, we take a sample of the first stage output on to these two sampling capacitors (falling edge of N3 in Fig 5.9).

After the data is stored on the sampling capacitors, we integrate the charge stored on one of these capacitors immediately (during N4 is high in Fig 5.9). After integration, the comparator following the second integrator makes a comparison and determines the new feedback bit. This new feedback bit is used to determine the direction of charge flow when we integrate the charge stored on the second sampling

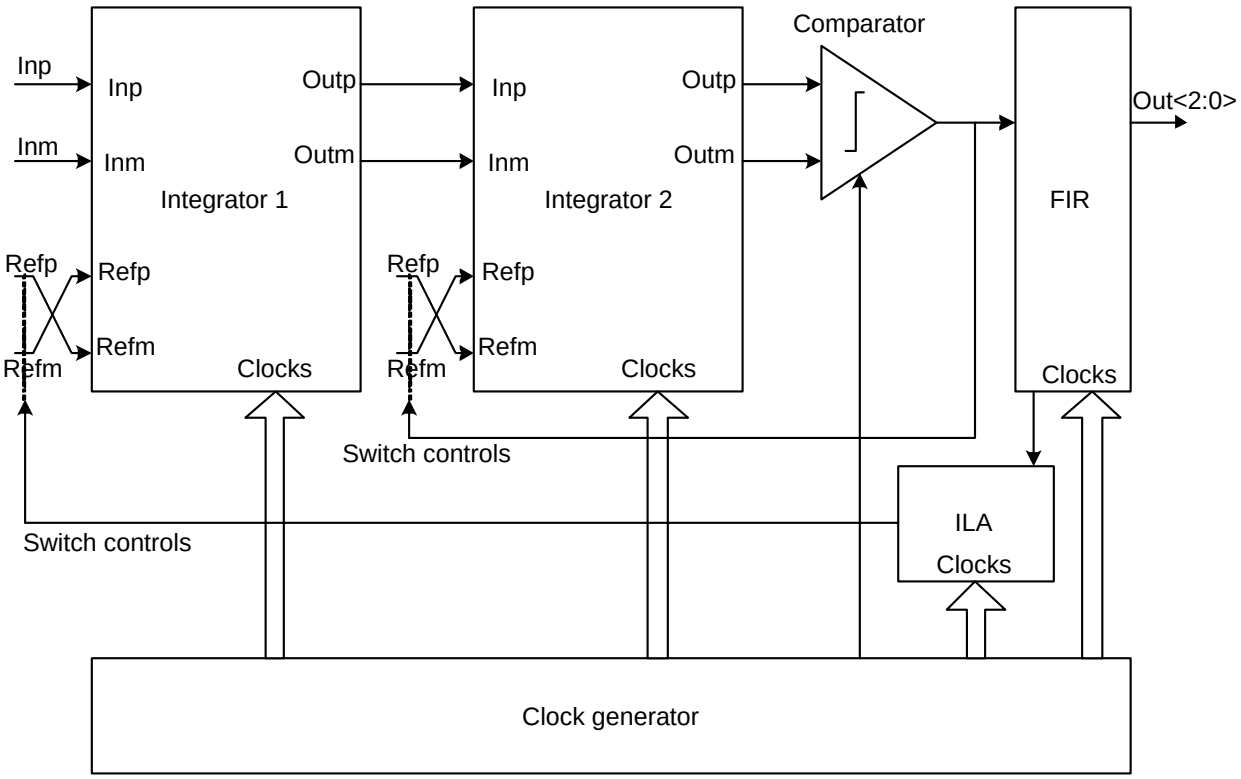

Figure 5.6: Top level implementation of the proposed architecture

capacitor (during when N5 is high in Fig 5.9).

Fig. 5.6 shows the top level implementation of the proposed architecture. In Fig. 5.7 and 5.8 the implementation of the first and the second integrators are given. On these figures, the name of the clock signal that controls a switch is given next to it. N1D is a delayed version of the clock N1 by a few hundred picoseconds. Then in Fig. 5.9, the clocking scheme that is devised and used in this implementation is provided. This clocking is an essential part of the proposed technique for the implementation of a power efficient system. In the next section, the details about the implementation of the digital filter will be given.

As we can see from the discussion above, this clocking scheme allows the 1st integrator to use the whole half clock cycle(T/2) for sampling and integration operations. Therefore, the amplifier does not need to be as fast and so this results in significant power savings in the first integrator.

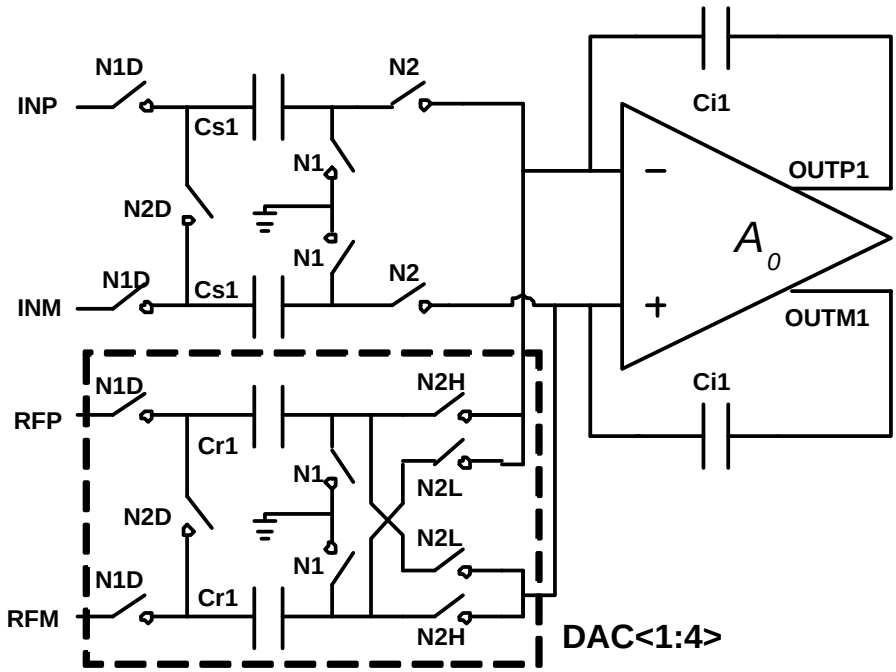

Figure 5.7: Architecture of the 1st integrator in the Proposed MM-ΣΔ modulator. The structure in dashed rectangle is repeated 4 times and connected in parallel, hence the notation $DAC < 1 : 4 >$.

As for the second integrator, with the use of this clocking scheme, it has the whole half clock cycle for sampling. However, it has to be able to integrate twice as fast(at $2fs$) i.e., it has about T/4 time for each integration.

There is still another issue that we need to think about. The second integrator samples the output of the first integrator onto 2 sets of capacitors when the first integrator is integrating. Therefore, the first integrator sees more capacitive load and this may cause additional power dissipation. However, this is really not an issue. Because the output of the second integrator sees just a single comparator. The comparator's decision is only based on whether its input is positive or negative. As long as we keep the C_{s2}/C_{r2} ratio for the second integrator the same, we can use smaller capacitances. The limiting factor is the matching between these capacitances. In other words, we care mostly about the matching between C_{s2} and C_{r2} in the second integrator and not on the matching between C_{s2} and C_{i2}. The gain in front of the comparator does not effect the decision as long as the gain is non-negative.

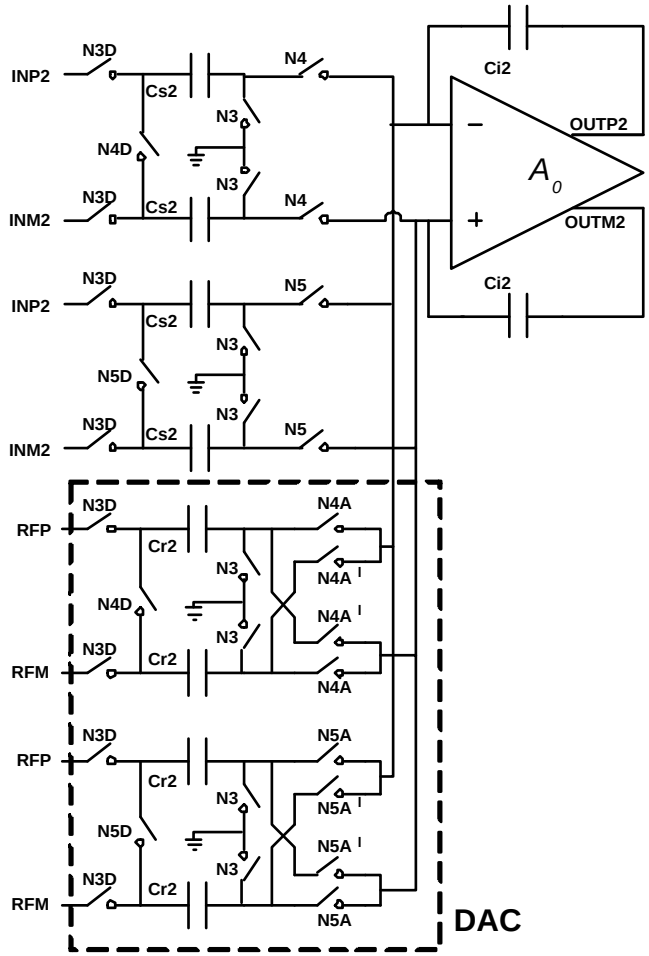

Figure 5.8: Architecture of the 2nd integrator in the Proposed MM-ΣΔ modulator

Consequently, this architecture does not require more power because it is possible to minimize these additional loads easily.

5.4 FIR FILTER

In multirate ΣΔ modulators, the first integrator runs at a slower clock rate than the following stages of the modulator. After the signal goes through the quantizer system, its rate has to be reduced to the rate of the first integrator clock rate. This is simply done by downsampling the signal right after the quantizer. However, just a simple downsampling will cause out-of-band quantization noise to fold into the signal band.

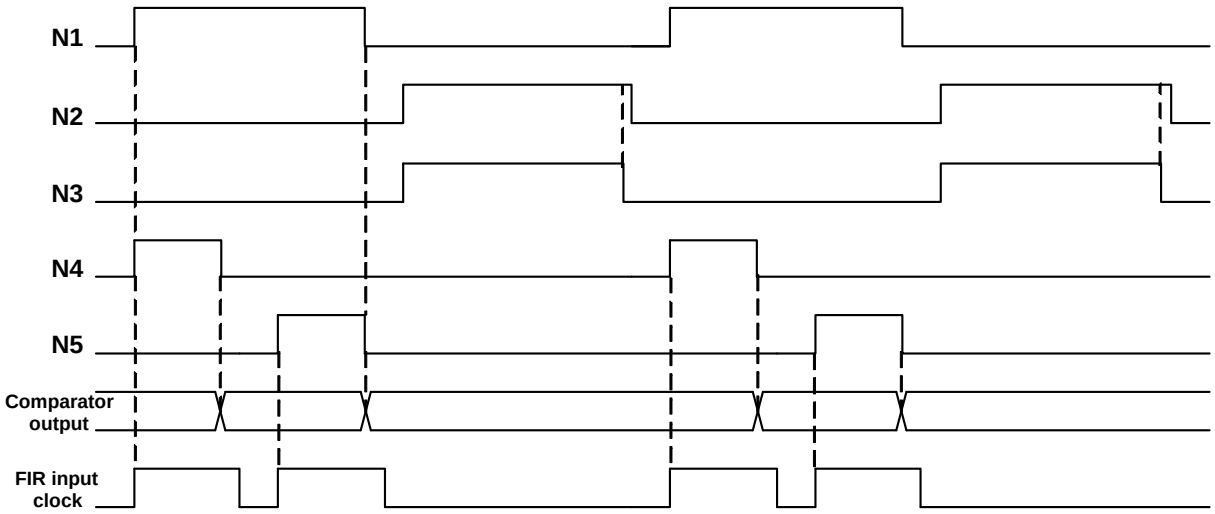

Figure 5.9: Clocking scheme for the Proposed MM-ΣΔ modulator

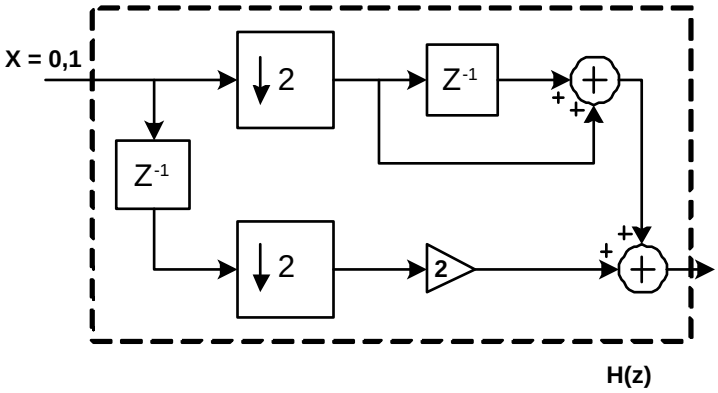

Figure 5.10: Block diagram of the FIR filter structure used in the proposed system

In order to avoid this, the signal has to go through a low pass filter first. Then, it can be downsampled and fed back into the first integrator.

Fig. 5.10 shows the block diagram of the FIR filter structure used in the proposed system. This is a direct implementation of the transfer function given in 5.2. The details of the circuit implementation and the timing of this digital filter will be given in Chapter 6.

5.5 ADVANTAGES OF THE PROPOSED MODULATOR

The proposed modulator is superior to the modulator implemented in conventional means in a variety of fronts. The most important advantage is the area savings as a result of replacing the bulky flash A/D converter in the feedback path of the modulator. This point is investigated in detail in the previous sections of this report. Furthermore, as will be explained in the next section, the idea presented in this report makes it possible to design $\Sigma\Delta$ modulators that makes the most use of multibit quantization. As a result, it will be possible to increase the SNR figures of $\Sigma\Delta$ modulators without having to increase the order of the modulator.

Power savings is another significant advantage point. For example, in order to meet a certain design specification, we will be able to use a low order modulator architecture rather than a high order one. This will be extremely useful because high order modulators will have stability problems. Also, the additional integrators will require more power dissipation that is very undesirable especially in wireless communication systems.

Another advantage is the ease of translating the design to a newer technology node. As the digital portion of the design replaces the analog functions, it is possible to synthesize the digital blocks from VHDL codes by using commercial EDA tools in a fast and efficient way.

5.6 SYSTEM LEVEL SIMULATIONS

The first integrator of a $\Sigma\Delta$ modulator is generally the most critical block in the whole system. This is because all the subsequent blocks benefit from the noise shaping and their nonidealities can be tolerated to a greater extent. A significant portion of the total power consumption also takes place in the first integrator. Therefore, the optimization of the design of the integrator stages, especially the first integrator, is

critical for a proper design. For this purpose, a very detailed non-ideal behavioral model of the system is constructed in Simulink [54] using models presented in [57]. MATLAB [53] routines have been extensively used to post process the modulator output bit stream.

First, we start by determining the OTA requirements of the proposed system. Specifically, it is crucial to know the minimum DC gain requirement, the minimum speed at which the amplifier outputs will settle to their final values (or gain bandwidth (GBW) and the maximum output swing that the amplifier will experience at its outputs.

In Fig 5.11, we find the minimum DC gain required of the OTA by the proposed system. In this experiment, the DC gain of the first integrator amplifier is swept across a range of values and the sensitivity of modulator SNDR with respect to DC gain is presented. From this plot, the minimum required DC gain for the first amplifier is found to be around 45dB. Below 45dB, the rate of SNDR degradation quickly increases whereas the rate of SNDR improvement above 45dB is minimal. A similar experiment is done for determining the DC gain requirement of the second integrator amplifier and it is found that a moderate gain of 40dB is sufficient and does not cause significant degredation to the SNDR of the system.

The second design specification that we need to find about is the GBW required of the first and second amplifiers. Fig 5.12 shows contour plots to determine the gain bandwidth requirement of both amplifiers. Note that first integrator GBW is on the x-axis while the second integrator GBW is on the y-axis. Slew rate of both amplifiers are set to 70V/usec in this experiment. As it is seen from this plot, first integrator amplifier must be designed such that its worst case GBW is more than 40MHz. This minimum GBW for the second integrator amplifier is more than 45MHz to get the best performance out of this system.

The third specification that is extremely important in determining the amplifier topology is the maximum output swing that amplifier will experience at its output nodes when a maximum usable input signal is applied to the modulator input. If a

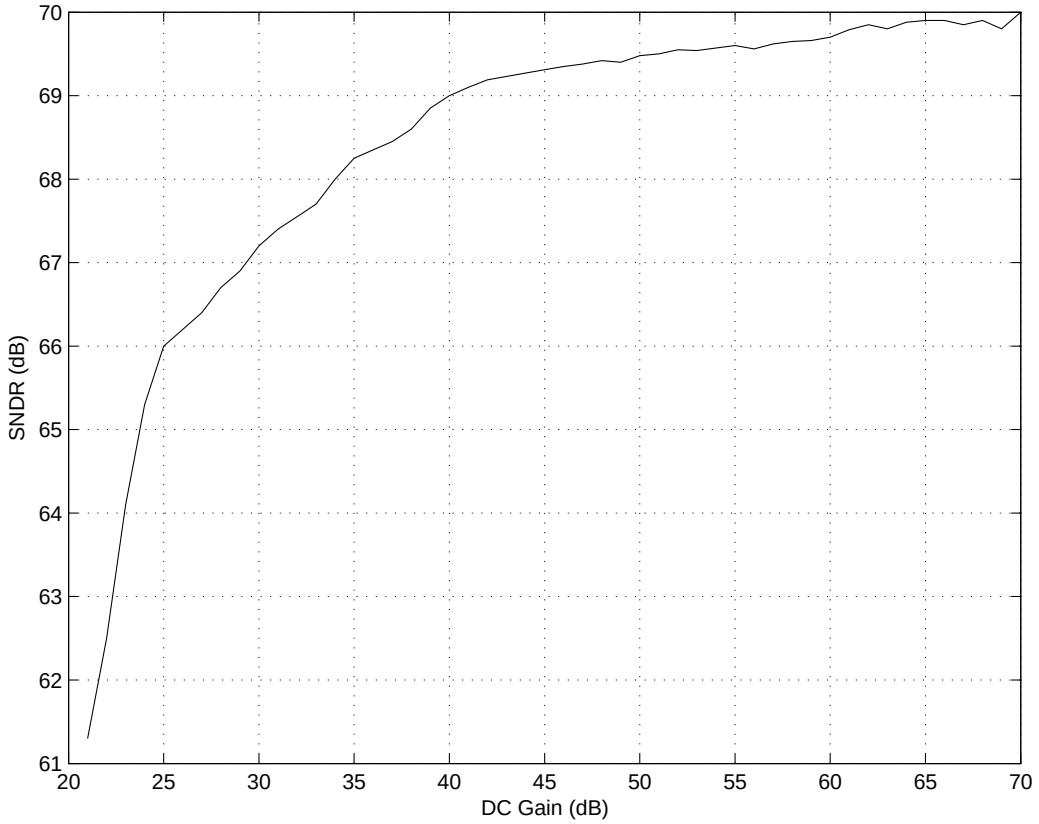

Figure 5.11: SNDR vs. first amplifier DC gain

very large output swing is required from the amplifier, then the topology should be selected such that the output stage of the amplifier does not have cascode structures. Hence, the amplifier will most probably be a two stage amplifier. On the other hand, if we have a reasonable output swing then we may have cascode structures as an output stage and still satisfy other specifications with a single stage amplifier topology.

Fig 5.13 shows the histogram of the outputs of both integrators when a -6dB sine wave with respect to the reference voltage is applied to the input of the modulator. X-axis shows the output swing as a ratio of the reference voltage (Vref=0.75V). According to this, first integrator output is within $\mp 0.6V$ and the second integrator output is within $\mp 0.4V$ in normal operation. The voltage supply is 1.5V in this design. It is therefore possible to have cascode configuration as the output stage and still meet the output swing requirements. Since we have moderate DC gain and GBW

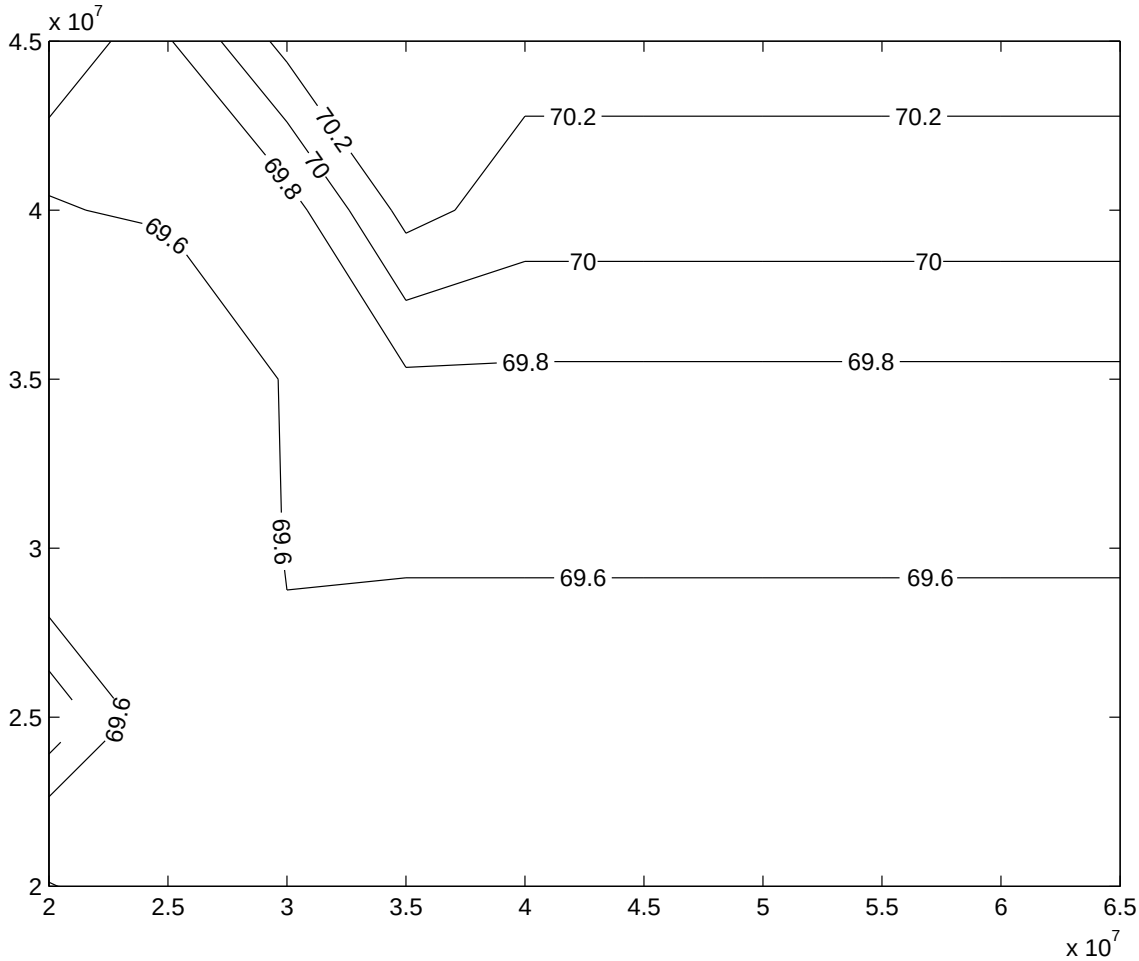

Figure 5.12: SNDR vs. first amplifier DC gain

requirements, a single-stage amplifier like the folded cascode amplifier used in [36] is appropriate for implementation. Unlike two-stage amplifiers, folded cascode will have less number of legs to bias. Hence it will be power efficient as well.

The only way to get an insight about the dynamic behavior of the $\Sigma\Delta$ modulator is through time domain simulations. Observing the evaluation of two state variables (or, in other words integrator outputs) for different input frequencies and at maximum signal level the modulator is designed for, one can obtain the integrator output swings. If integrator output swings are larger than a certain level, the modulator loop coefficients have to be adjusted in order to scale down the integrator output swings. The maximum output swing that we can allow at the output of the integrators is

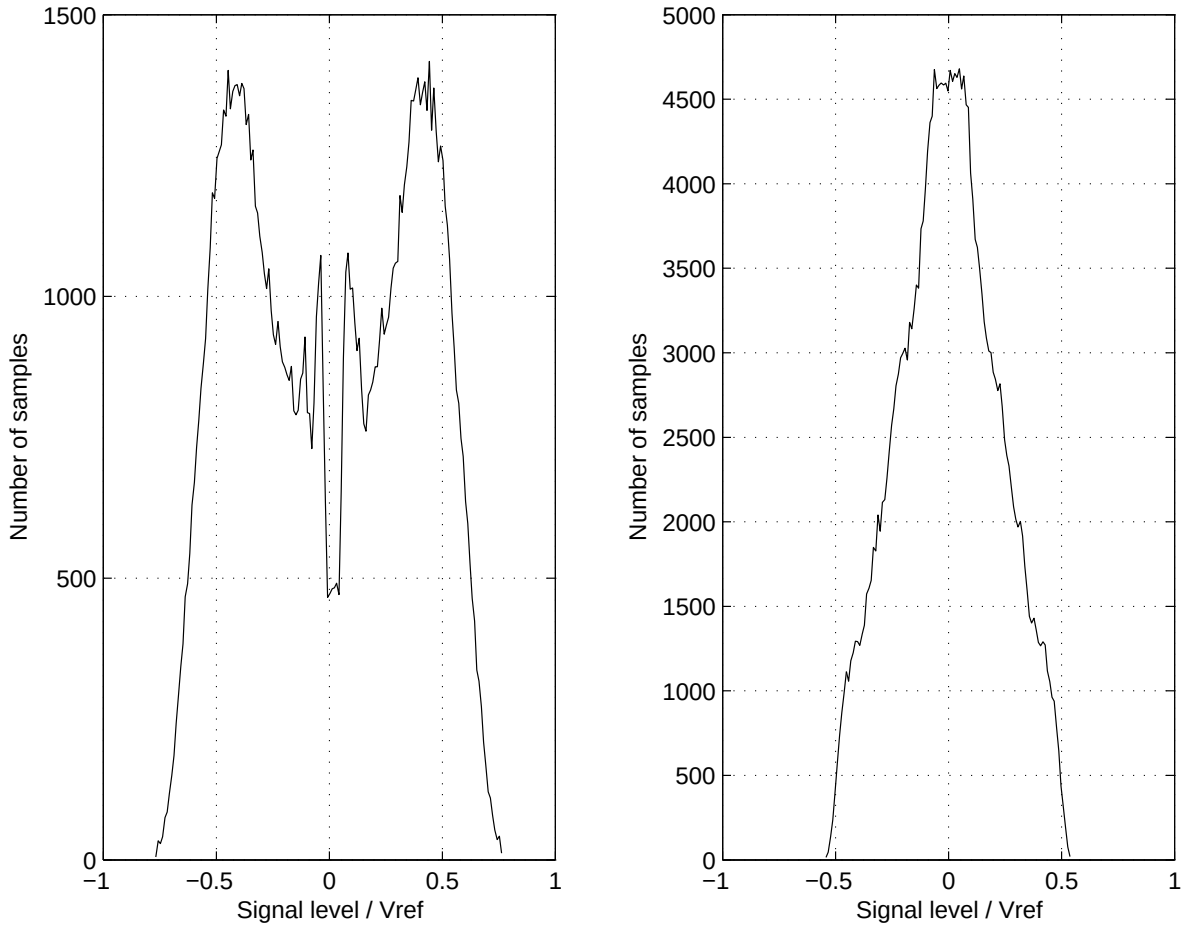

Figure 5.13: Histogram of integrator outputs

dictated by the supply voltage and the amplifier topology that will be chosen for the circuit implementation. When all the loop coefficients are adjusted, capacitor sizes are determined based on the noise specification of the modulator.

One type of the simulation that needs to be done on a $\Sigma\Delta$ modulator is the time domain simulations to verify the stability of the modulator. However, in our case, we have a second order system and from the basic theory of $\Sigma\Delta$ modulators, we know that first and second order modulators are inherently stable. Therefore, we do not need to worry about the stability of the loop based on loop coefficients. However, we need to analyze the usable input range for the modulator at-hand.

Chapter 6

CIRCUIT DESIGN OF THE EXPERIMENTAL PROTOTYPE

6.1 INTRODUCTION

This chapter explores the design of the circuit blocks that are in the $\Sigma\Delta$ modulator. Special attention will be given to design tradeoffs and power-optimization strategies for these circuit blocks. These include switched-capacitor integrators, operational transconductance amplifiers (OTA), bias circuits, comparator, digital FIR filter, dynamic element matching circuit using Individual Level Averaging (ILA) technique, and five-phase clock generation circuitry. An experimental prototype of the Second Order MM-$\Sigma\Delta$ modulator implemented in a 90nm single-poly, five-metal digital CMOS process without analog add-ons will be described.

In this experimental prototype, separate voltage supplies are used for analog and digital domains. Analog voltage supply is 1.5V and the digital voltage supply is 1.3V. There are a number of reasons for using two different voltage supplies: First of all, the noise that will be created by the digital circuits will be isolated from the analog circuits. In this design, some small digital circuits are placed close to analog circuits. Depending on the activity in the digital circuits, significant noise may be generated on the supplies. This may cause degredation on the modulator performance unless the analog circuits are designed for a high Power Supply Rejection Ratio (PSRR). The second reason is the reliability of the MOS transistors. In digital circuits, MOS devices will see the full supply voltage across their gate-to-source terminals. Therefore, unlike analog signals, designers can not use a supply voltage that is higher than the transistor

ratings. On the other side, using a lower supply voltage in the analog circuits generally forces the designer to dissipate more current. Therefore, a higher supply voltage is chosen for the analog part of the design.

In this design, the design target was to minimize the current dissipation of the modulator in order to increase battery life in mobile applications. Therefore, using a higher analog voltage supply enabled the design to use a single-stage Operational Transconductance Amplifier (OTA) rather than a 2-stage OTA. Hence, a significant current savings is achieved through this OTA selection.

6.2 INTEGRATOR DESIGN

In a $\Sigma\Delta$ modulator, integrator performance is specified in terms of nonidealities which limit the overall modulator dynamic range and speed of operation. Parameters such as finite dc gain, linear settling and slew rate can raise the quantization noise floor or introduce distortion depending on the circumstances. The available swing at the output of the integrators sets the modulator overload level (peak input signal handling capability). Thermal noise introduced by the sampling process (kT/C) as well as by the amplifiers adds directly to the quantization noise to set the minimum detectable signal. The effect of each of these nonidealities on the overall modulator will be investigated and procedures will be described to specify integrator performance.

The experimental prototype comprises two switched-capacitor integrators. The architecture of the first and the second integrators were given in Chapter 5 and are repeated here in Fig. 6.1 and 6.2 for the sake of completeness. The integrators are implemented in a fully differential configuration. The first integrator employs a two-phase nonoverlapping clocking scheme and the second integrator employs a three-phase nonoverlapping clocking scheme.

In the first integrator, the input is sampled during phase 1 (N1 and N1D). During phase 2, the charge is transferred from the sampling capacitor (C_{s1}) to the integrating capacitor (C_{i1}). At the same time, depending on the output value, the appropriate

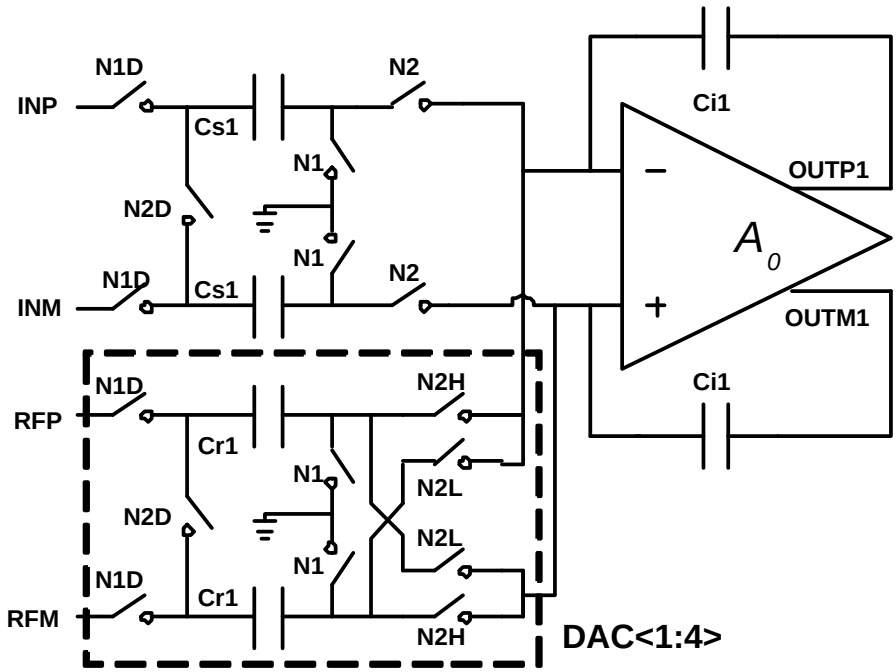

Figure 6.1: Architecture of the first integrator in the proposed MM-ΣΔ modulator

DAC reference level is applied by closing either switches labeled N2H or N2L.

In the second integrator, the input and the reference voltage are sampled onto two sets of capacitors during phase 3 (N3 and N3D). During phase 4, the charge is transferred from the first set of sampling capacitors to the integrating capacitor. At the same time, depending on the output value, the appropriate DAC reference level is applied by closing either switches labeled N4AH or N4AL. At the end of phase 4, the comparator following the second integrator compares the outputs of the integrator and makes a decision. Depending on the outcome of that comparison, the control signals N5AH and N5AL are determined. Then, during phase 5, the charge on the second set of sampling capacitors is also transferred onto the integrating capacitor. At the same time, depending on the comparator output, the appropriate DAC reference level is applied by closing either switches labeled N5AH or N5AL.

Both integrators employ the bottom-plate sampling technique to minimize signal dependent charge-injection [40]. This is achieved through delayed clocks: N1D, N2D, N3D, N4D and N5D. When switches labeled N1 and N3 are first turned off, the

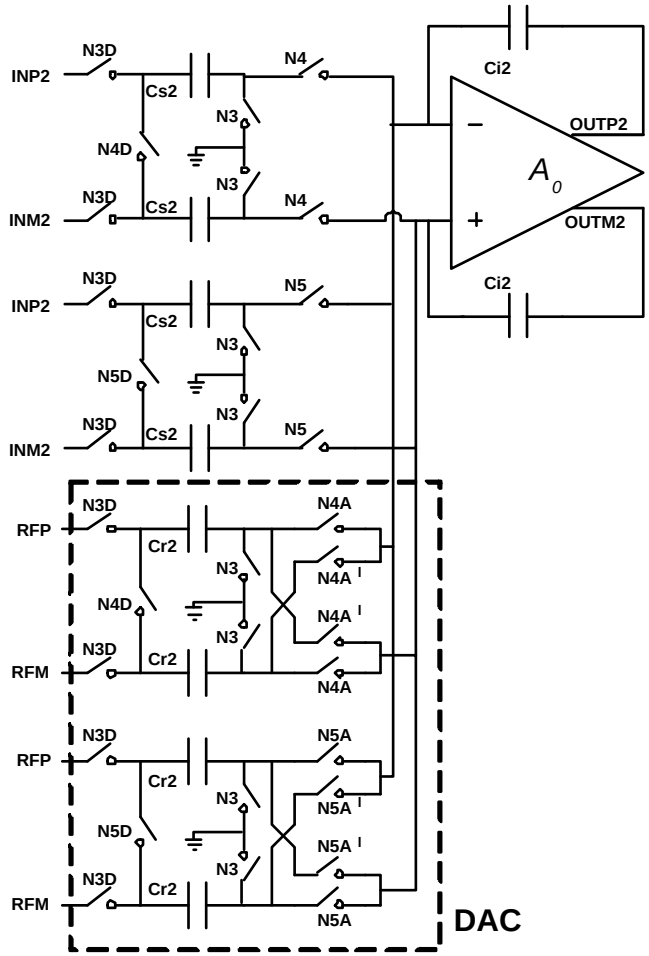

Figure 6.2: Architecture of the 2nd integrator in the Proposed MM-ΣΔ modulator

charge injection from those switches remains, to a first order, independent of the input signal. Because one of plates is now floating, turning off switches labeled N1D and N3D shortly after does not introduce charge-injection errors.

6.2.1 Switch Design

A critical problem in designing switched-capacitor circuits with a low voltage supply is the difficulty of implementing MOS switches. Typically in a switched-capacitor circuit an analog input signal, Vi, is sampled through a MOS switch or transmission gate as shown in Fig. 6.3. Ideally the switch in the on-state acts as a fixed linear resistance Ron. In practice the resistance of the switch varies with the signal voltage

as given by (6.1) and is shown in Fig. 6.4. In this plot, it is first assumed that the voltage supply Vdd is larger than the sum of the two threshold voltages (Vtn and Vtp) by a good margin. On the same plot, we can also see the individual resistances of the NMOS and PMOS devices. By looking at these curves, we observe that when Vin is around Vdd/2, the resistance of the CMOS switch makes a peak. On either side of this peak, Ron is dominated by NMOS or PMOS devices and the resistance drops significantly. In the second case, Vdd is still larger than $Vtn + Vtp$ but this time there is not a big margin. In the third case, Vdd is assumed to be smaller than $Vtn + Vtp$.

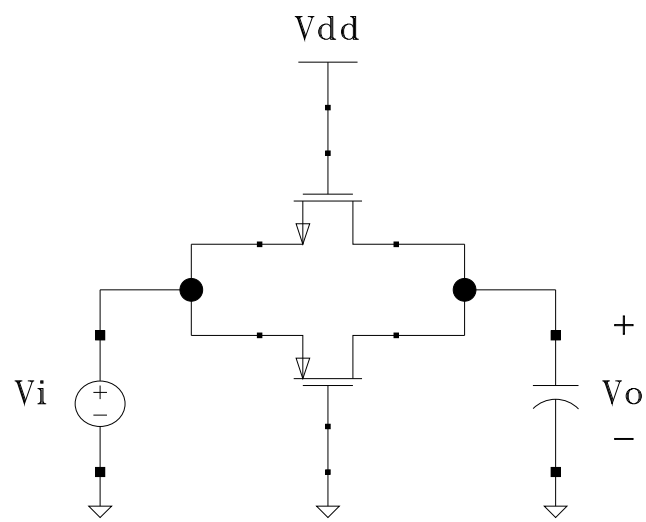

Figure 6.3: CMOS switch used in sampling networks

$$Ron_{CMOS} = [u_n C_{ox} \frac{W_n}{L_n}(V_{GSn} - V_{tn}) + u_p C_{ox} \frac{W_p}{L_p}(V_{GSp} - V_{tp})]^{-1} \tag{6.1}$$

There are three important points in the design of this CMOS switch. The first is the value of the peak resistance. This peak resistance should be such that the bandwidth of the sampling network formed by the switch and the sampling capacitor at any given moment is greater than the sampling rate by a good margin. Usually the rule of thumb is that the minimum bandwidth is about 3-5 times the sampling rate of the switch. The second point is related to the variation of Ron with the input voltage.

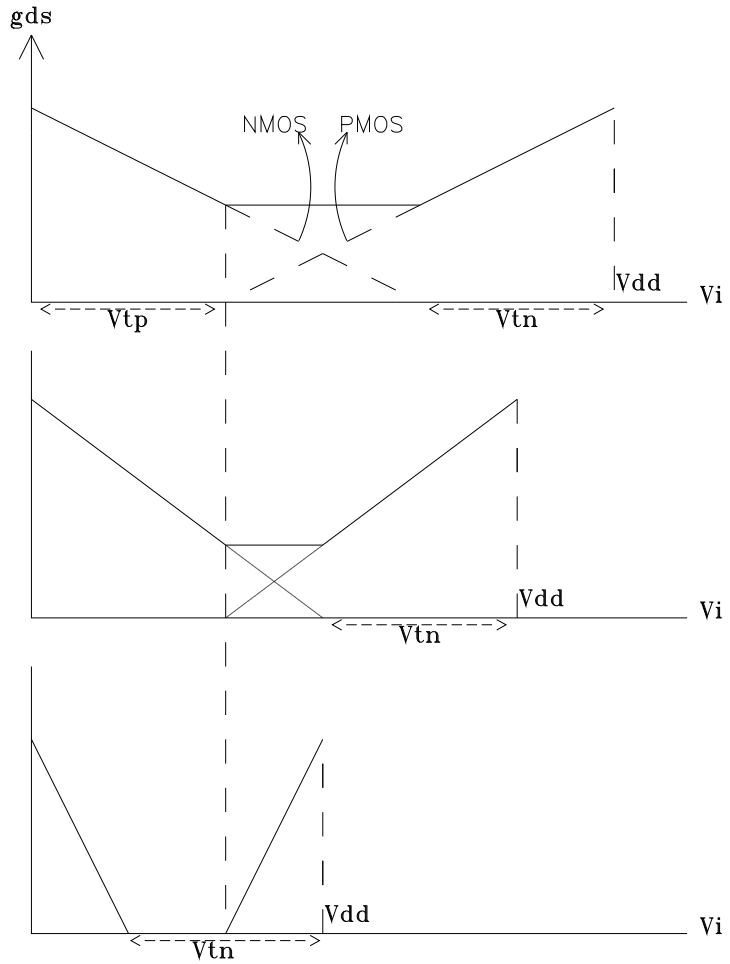

Figure 6.4: On resistance (Ron) versus Input voltage (Vin) in a CMOS switch

If too much variation is allowed, then this will cause distortion which is easily visible at the output of the CMOS switch if we look at the Fourier Transform. How much variation is tolerable depends on design specifications. For example, if our design specification dictates a certain SNDR in a given bandwidth, then we make sure the distortion introduced by the CMOS switch is much smaller than the specification. The third consideration in the design of the sampling switches is the area. We would like to make these switches as small as possible not only because we want to save silicon area but also we want to minimize the parasitic capacitance associated with the switch. The smaller the parasitic capacitances are, the more power efficient the design will be.

Since the nonoverlapping clock generator circuit is a digital block and the value of the digital voltage supply is 1.3V, the clock signals coming out of this block will be 1.3V signals. Spice simulations showed that driving the switches with 1.3V gate voltage would not be practical. The overdrive voltage was not enough and therefore we would be forced to enlarge the switches to reduce the resistance as well as the switch non-linearity. Since this is not desirable, level shifters are inserted in the path of the clock signals to boost them to 1.5V level. This provided sufficient overdrive voltage for the switches and resulted in smaller transistors for the switches. The design of the level shifter will be explained in detail in section 6.2.2

An important factor in designing switches in Ultra-deep Sub-micron(UDSM) processes is the dependence of Vt to the length (L) of the transistor. As the L of the transistor increases starting from the minimum L dictated by the process, the Vt of the transistor will become lower. This means the resistance value of the switch will become smaller even if you keep the W/L ratio of the transistor the same. Moreover the resistance will also become more linear. In this process, the minimum drawn length is 0.13u. However, it is found through Spice simulations that using an L of 0.2u will give us optimum switch sizes both in terms of area and performance. As the length of the transistors composing the switches are increased beyond 0.2u, the benefits of reducing Vt was not justified as compared to the increase in device size. Hence, L=0.2u is extensively used for switches in this design.

6.2.2 Level Shifter

As explained in the previous section, because of different voltage supplies in analog and digital domains and also because of the need to have more overdrive voltage across the gate-source terminals of our switches, level shifters are employed in the path of the clock signals. The sampling and integrating periods in this design may be less than 10ns. Therefore, the rise and fall times of the clock signals must be less than 0.5ns in worst case so that the high-duration of the clock signals can be maximized. It is then obvious that the speed is the most important parameter in the design of

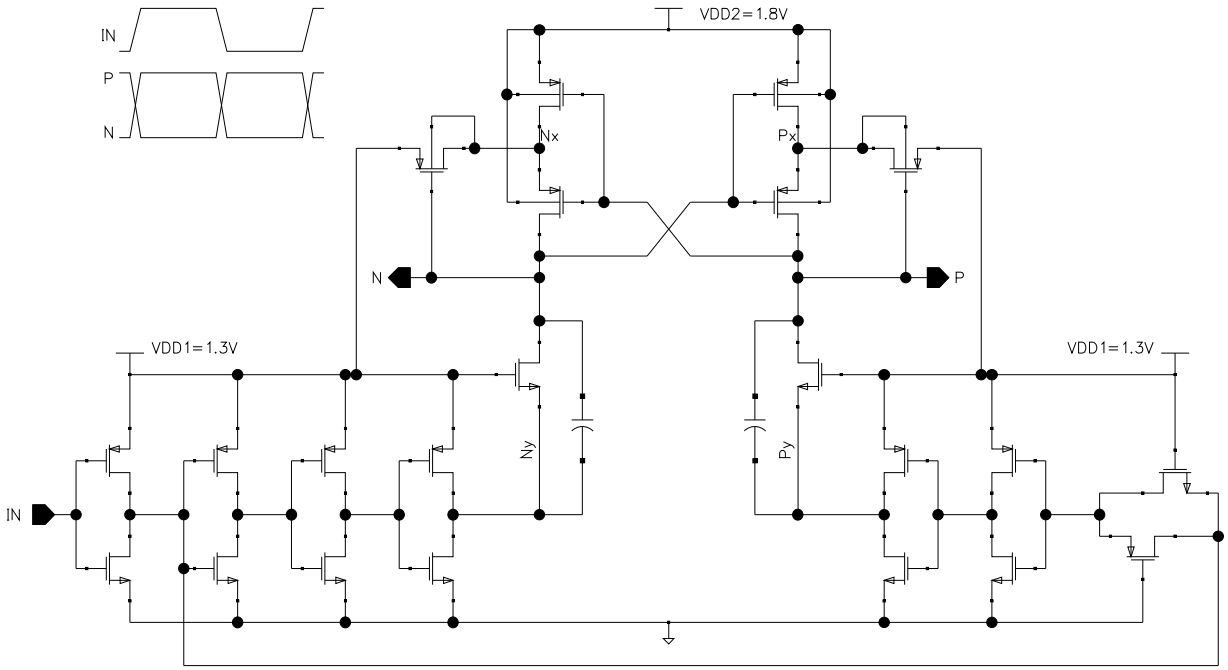

Figure 6.5: A fast cross-coupled level shifter for clock signals

these level shifters.

Fig. 6.5 shows the schematic of the level shifter used in this design. Each one of the clock signals that are coming from the 5-phase non-overlapping clock generator circuit and going to the integrators use one level shifter. As seen from Fig. 6.5, this level shifter produces two outputs that are inverse of each other. These outputs N and P are used to drive the NMOS and PMOS devices that compose a CMOS switch respectively. In this level shifter, depending on the input, one of the output nodes discharges first and because of the cross-coupled PMOS devices at the top, the other output node charges to 1.5V. Therefore, the high-to-low transition will always be smaller than the low-to-high transitions.

Note that the PMOS devices at the top will see a -1.5V gate-to-source voltage difference. This would create a reliability problem for normal devices because they are designed for 1.3V operation. Therefore, devices with thicker gate oxide are used instead of normal devices. These devices are available within the technology and are obtained without any new mask adders to the fabrication process.

Since speed is the main concern in this design, capacitors that are in parallel with the input devices are used. Because the voltage across these capacitors can not change instantly, the moment the input changes and pulls down node Ny (or Py), node N (or P) comes down with it (otherwise we have to wait for the reaction time until the input transistors start conducting). So, first capacitors act to discharge the output node and then transistors take over. These capacitors also serve for the protection of the input devices from reliability issues. Since node N comes down as fast as node Ny (or node P comes down with Py), drain-to-source voltage difference for these input devices are always within certain limits and it does not exceed the proper operation region of the transistor. If the transistors are not protected well, permanent damage may occur over the lifetime of the circuit.

6.2.3 Sampling and Integrating Capacitors

The sizes of the sampling and integrating capacitors are dictated by the noise requirements. The ideal input-referred thermal noise of the integrator is given by 6.2. This equation is valid for when the amplifier noise including the $1/f$ noise is negligible. Since the noise generated by the two sides of the differential path are not correlated, there is a coefficient of 2 in equation 6.2. If they were correlated, the coefficient would be 4 in this equation.

$$\overline{V_{noise}^2} = 2\frac{kT}{C_s} \tag{6.2}$$

If the input voltage to the modulator is fixed, the signal to noise ratio at the output of a differential amplifier is $3dB$ lower than it is at the output of a single ended amplifier. This assumes that the output is taken differentially so that the noise generated by the tail current source is cancelled. As a result, the dB difference between the signal level and noise floor in the differential amplifier case will be $3dB$ less than that of the single-ended amplifier. However, the maximum obtainable differential signal voltage at the output of the differential amplifier is $6dB$ greater than that from

a single-ended amplifier. In $\Sigma\Delta$ modulators, it is often the output signal capability of the amplifier that limits the maximum signal applicable to the input of the modulator. Since the differential structure enables the amplifier to handle $6dB$ larger signal at the output of the amplifier as compared to the single-ended architecture, we now can apply $6dB$ larger signal to the input of the modulator. As a result, in differential architectures with double the input signal amplitude as compared to the single-ended scheme, the signal to noise ratio ratio will be $3dB$ better. Moreover, fully-differential integrators are more immune toward power-supply, common-mode and substrate-coupled noise.

Because of noise shaping, the second integrator will have relaxed noise requirements. This suggests that the capacitors in the second integrator will be selected based on parasitic considerations rather than noise.

The prototype modulator is designed for both GSM (200kHz signal bandwidth) and Wideband CDMA(WCDMA) (2MHz signal bandwidth) applications. At the architecture level, the sampling frequency of the first integrator has been selected to be 19.2MHz and 38.4MHz for GSM and WCDMA, respectively. The required DR is 60dB for GSM and 40dB for WCDMA. Other than the sampling frequency, the difference in the design of the modulator in GSM and WCDMA modes is the bias current that is supplied to the analog circuit blocks. Specifically, the bias current is increased by 50% in WCDMA mode in order to increase the bandwidth of the amplifier and the comparator.

The value of the sampling capacitor in the first integrator has been selected to be 0.4pF for both GSM and WCDMA modes. This is determined by the kT/C noise specification in GSM mode. In WCDMA mode, the output spectrum of the modulator shows that we are limited by the quantization noise and not by the kT/C noise. So, it is possible to reduce this capacitor even more in WCDMA mode. However, since Cs is already small, reducing this cap to less than 0.4pF would cause matching problems and hence is not done in this design.

The desired closed-loop gain is 0.5 in the first integrator. Thus, the integrating

capacitor is 0.8pF.

6.2.4 Operational Transconductance Amplifier

6.2.4.1 DC Gain

Finite amplifier dc gain can degrade both the distortion and noise performance of a $\Sigma\Delta$ modulator. Depending upon modulator architecture, either distortion or quantization noise shaping will set a more severe constraint on amplifier dc gain. Third-order distortion due to nonlinearities in the amplifier dc transfer function over its output range sets one dc gain requirement on the first integrator in a $\Sigma\Delta$ converter. The noise-shaping of the loop relaxes this dc gain requirement for subsequent integrators. Since these nonlinearities are inversely related to the amplifier dc gain, the gain must be increased to the point that the overall modulator performance is not degraded. This dc gain specification is not particularly severe; a moderate dc gain of 60 dB is more than adequate for 16 bit performance [3]. It is also important to note that the distortion specification is relatively independent of architecture for a fixed dynamic range.

A second effect of finite amplifier dc gain is to change the positions of the poles in a switched-capacitor integrator. The block diagram of a switched-capacitor integrator with an amplifier of dc gain A is shown in Fig. 6.6. The diagram is single-ended for convenience but the results apply to fully-differential implementations. Charge conservation analysis in the z domain yields the integrator transfer function H(z) in (6.3). The effect of finite amplifier dc gain is to shift the pole H(z) slightly off of the unit circle. This pole shift known as leak will increase the quantization noise floor at baseband. In a single-loop modulator, this effect is less severe than distortion; a dc gain on the order of the oversampling ratio will make it negligible [13].

$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{(C_s/C_f)z^{-1}}{1-(1-\epsilon)z^{-1}} \tag{6.3}$$

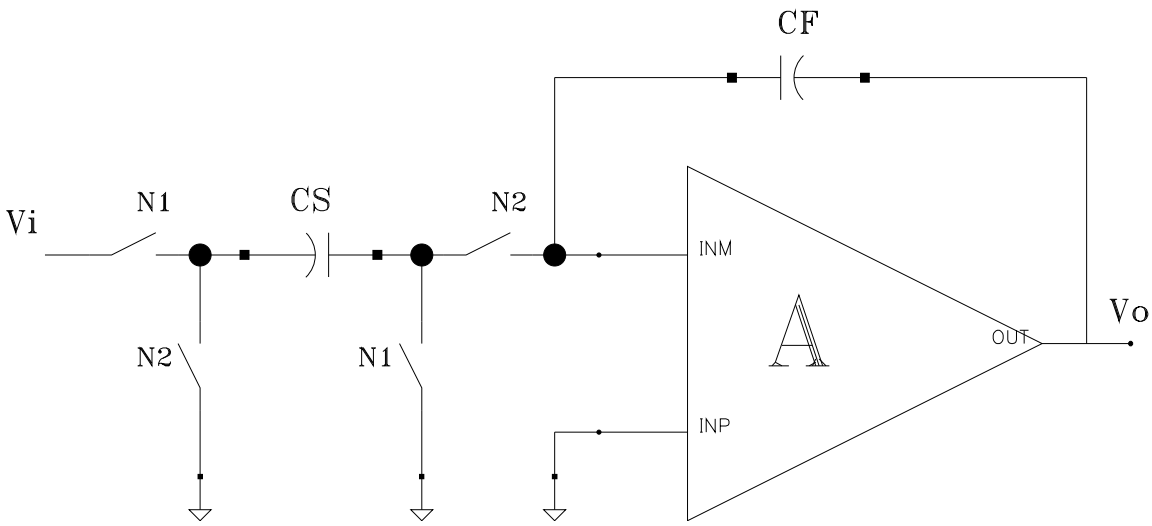

Figure 6.6: Switched-Capacitor integrator with finite amplifier dc gain

$$(1-\epsilon) = \frac{1}{1+\frac{C_s}{AC_f}} \tag{6.4}$$

6.2.4.2 Linear Settling and Slew Rate

Linear settling and slew rate specify the small signal and large signal speed performance of an integrator respectively. In a sigma-delta modulator, a linear settling error results in an integrator gain error while slew rate results in harmonic distortion [51]. In a cascade modulator, this gain error has the same effect as capacitor mismatch but can be made small enough to have negligible effect on the modulator quantization noise. Harmonic distortion due to amplifier slew rate can directly degrade the large signal performance of the modulator. The slew rate in each amplifier must be made large enough that the distortion introduced falls below the noise floor of the modulator. Due to the low g_m/I ratio of short channel CMOS devices and the required high speed operation, this distortion constraint will be satisfied if the amplifier slews for a small fraction of the settling period and spends the majority of its time in a linear settling regime.

To quantify the effect of slew rate and linear settling on a $\Sigma\Delta$ modulator requires

system level simulations like the ones we have done in chapter 5. The simulations assumed a single pole operational amplifier characteristic with slew rate. This amplifier model is a significant oversimplification for a design which employs more complicated two-stage amplifiers. However, in the case of simpler single-stage amplifiers, the results will be quite accurate. Still, it will be a good idea to leave some safety margin on top of what is found from behavioral simulations.

6.2.4.3 Output Swing

Output swing defines the maximum signal handling capability of an operational amplifier and is directly related to the modulator input overload level. Maximizing the output swing will increase the maximum signal handling capability of the modulator. For a kT/C noise limited design, this will minimize the required sampling capacitance and power dissipation.

Output swing is ultimately limited by the power supply voltage, but in practical designs the swing will be lower due to the requirement that the output devices remain in saturation. The circuits in Fig. 6.7 represent the output stages of a typical folded-cascode amplifier and a two-stage amplifier. For an amplifier with cascoded devices at the output as shown in Fig. 6.7(a), the output swing will be given by (6.5) while for the common source configuration shown in Fig. 6.7(b), the output swing will be given by (6.6). Maximizing the output swing favors the common source configuration and therefore a two-stage amplifier. However, a two-stage amplifier will have more branches to bias and the static power dissipation will be higher than a folded-cascode amplifier in general.

$$V_{swing} = V_{DD} - 2V_{dsat,n} - 2V_{dsat,p} \tag{6.5}$$

$$V_{swing} = V_{DD} - V_{dsat,n} - V_{dsat,p} \tag{6.6}$$

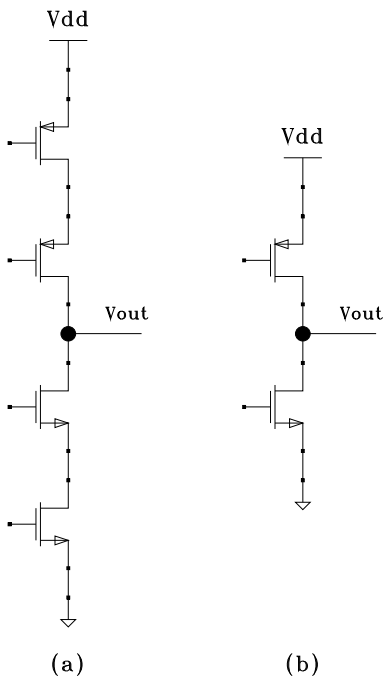

Figure 6.7: Operational amplifier output configurations (a)cascoded and (b)common source

6.2.4.4 OTA Topology selection and design

In chapter 5, all the design requirements of the OTA was found through behavioral simulations using Simulink [54] toolbox of MATLAB [53]. These are summarized in Table 6.1 for our OTA inside the first integrator. In this table, the output swing is the peak-to-peak swing at one of the amplifier outputs. Therefore, the amplifier outputs will be as high as $V_{ocm} + 0.3V$ and as low as $V_{ocm} - 0.3V$, where V_{ocm} is the common mode voltage of the amplifier outputs.

Because the output swing requirements allow us to use cascoding at the output stage of the amplifier, we can obtain a good gain from a single stage amplifier. Therefore, a fully-differential folded cascode OTA with switched-capacitor common mode feedback (SC-CMFB) is the design choice for the prototype $\Sigma\Delta$ modulator.

The schematic for the folded cascode OTA is shown in Fig. 6.8. This is a well known OTA topology in the literature and the design equations are given in equations (6.7), (6.9), (6.10) [45]. Note that in equation (6.9), C_L is the total load capacitance

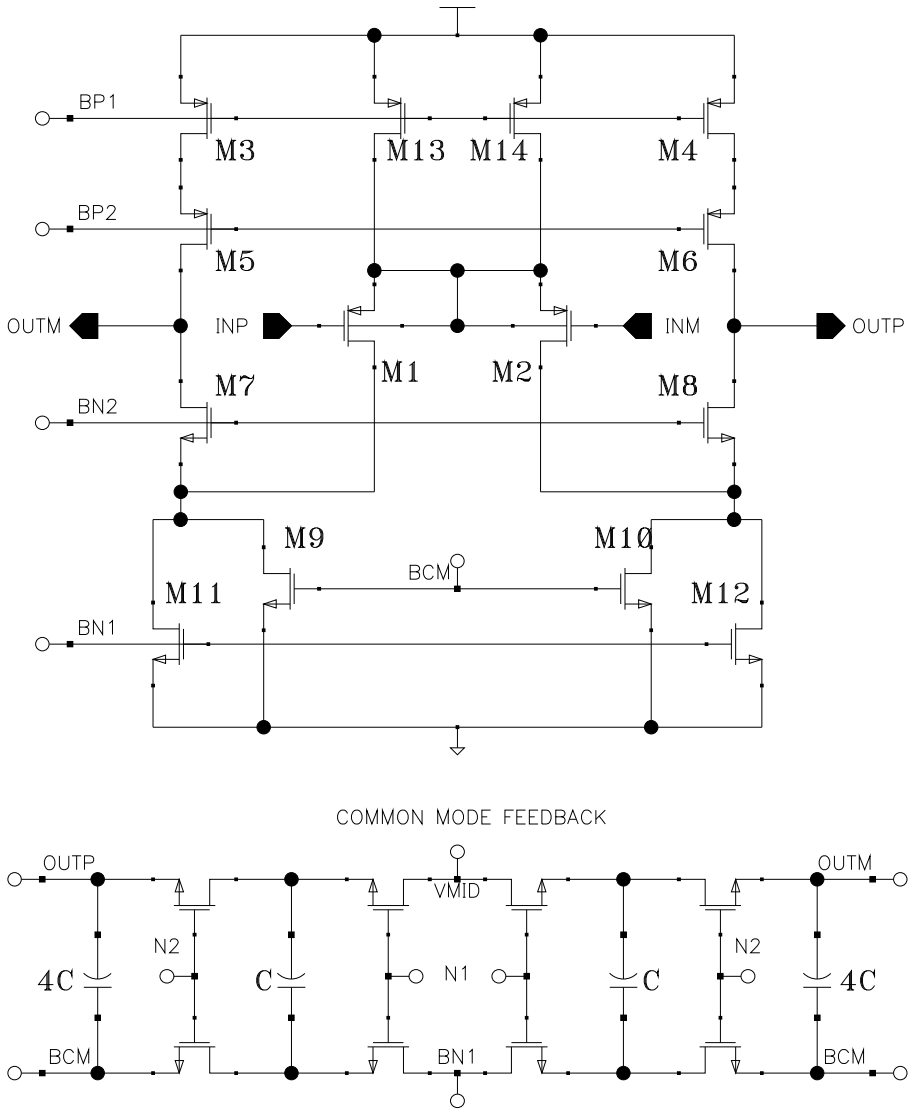

Figure 6.8: Operational amplifier with switched-capacitor common mode feedback

Table 6.1: First integrator OTA specifications determined from behavioral simulations using MATLAB-Simulink.

Item	GSM spec.	WCDMA spec.
Voltage Supply	1.5V	1.5V
DC Gain	45dB	45dB
Bandwidth	40MHz	60MHz
Slew rate	60V/usec	90V/usec
Output swing	0.6V	0.6V
Integrated Noise	20uV in [450Hz,200kHz]	40uV in [450Hz,1.94MHz]
Current consumption	Minimum	Minimum

that accounts for the parasitics associated with the transistors and also the capacitive loading of the second integrator stage. Another important point is the feedback factor (see equation (2.16)) of the integrator stage. Equation (6.9) gives the GBW assuming that the feedback factor is 1. If the feedback factor is not 1, then the GBW should be scaled accordingly. Finally, I_B in equation (6.10) is the total bias current flowing through the transistors M13 and M14 on Fig. 6.8.

$$A_{v0} = g_{m1} R_{out} \tag{6.7}$$

$$R_{out} = g_{m6} r_{ds6} r_{ds4} // g_{m8} r_{ds8} (r_{ds10} // r_{ds12}) \tag{6.8}$$

$$GBW = \frac{g_{m1}}{2\pi C_L} \tag{6.9}$$

$$SR = \frac{I_B}{C_L} \tag{6.10}$$

Because this is a fully-differential amplifier, common-mode feedback is required to define the common-mode voltages at the output nodes in the circuit. This amplifier employs dynamic or switched-capacitor common-mode feedback (SC-CMFB)

as shown in Fig. 6.8. For a detailed explanation of the SC-CMFB architecture, the reader may refer to [40].

Note that with large output swings, the speed of the SC-CMFB loop may in fact influence the settling of the differential output [41]. For this reason, part of the bias current of the differential pair in Fig. 6.8 is provided by a *constant* current source (M11 and M12) so that SC-CMFB loop makes only minor adjustments to the circuit by changing the current flowing through transistors M9 and M10.

6.2.5 Comparator

The quantization is implemented using a single comparator following the second integrator stage. This means significant area and power savings as compared to multibit designs employing flash A/D converters.

In $\Sigma\Delta$ modulators, as we move from the input of the modulator towards the input of the quantizer, the design requirements become less stringent. For example, in this design, the second integrator will be less demanding than the first integrator because there will be a first order noise shaping for the noise produced by the second integrator. Similarly, because there are two integrators before we reach the quantizer, the quantizer noise will be second order shaped. Hence there is no stringent design requirements on the comparator to be used in a $\Sigma\Delta$ modulator. Therefore, a simple comparator structure that does not include an offset cancellation circuit such as the ones reported in [5] [43] [48] [49] can fulfill the design requirements.

A differential, positive feedback comparator is used for this purpose (Fig. 6.9). However, in order to reduce the kickback into the output of the second integrator, a low-gain pre-amp stage is also a part of the comparator. The pre-amp stage consumes a static current of only 20uA from a 1.3V supply.

When the RST signal depicted in Fig. 6.9 becomes low, the latch stage makes the comparison and holds the output even after the RST signal goes high again. Note that, in order to clean all the memory effects, both latch inputs are grounded when the RST signal goes high.

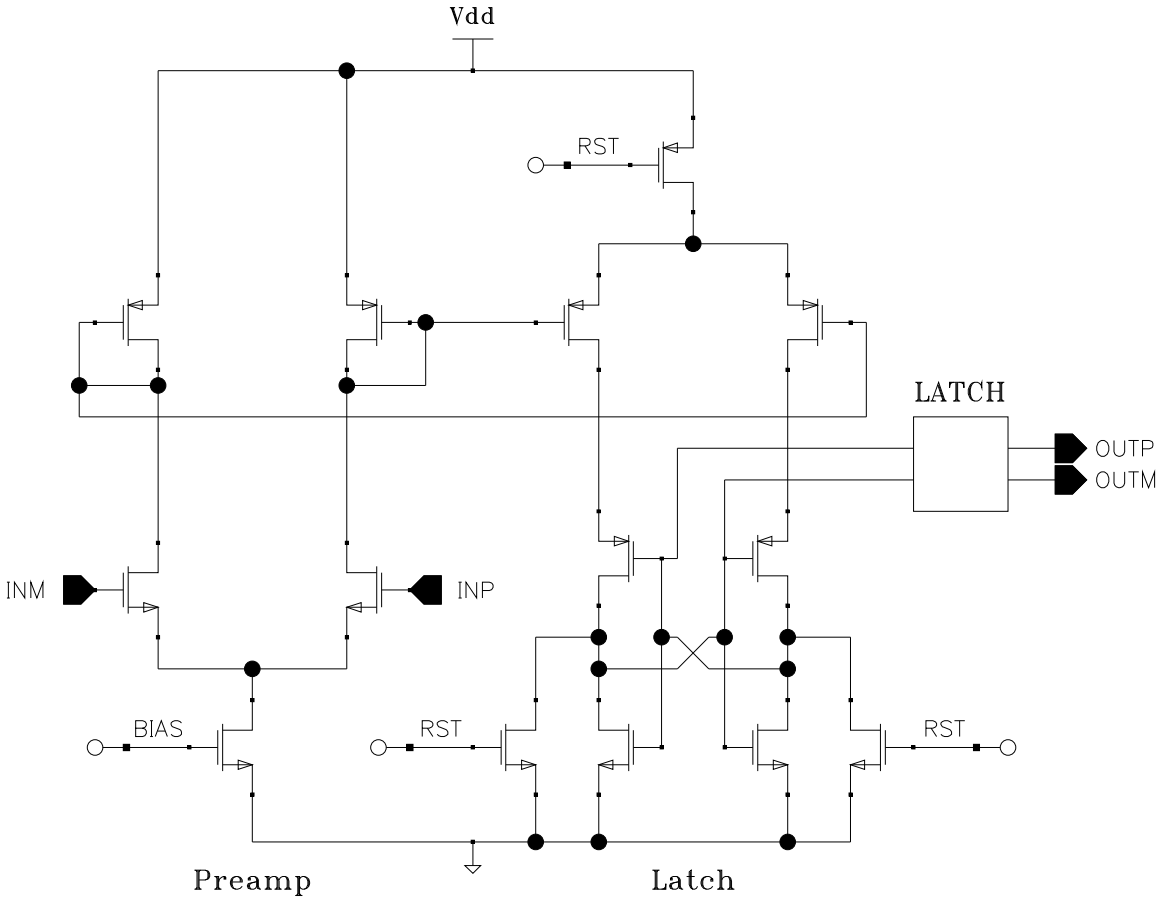

Figure 6.9: Comparator schematic

6.2.6 Clock generator

A five-phase clocking scheme is required for this architecture. The details of the relationship between different clock signals is given in Fig. 5.9. According to this clocking scheme, clocks N1 and N2 need to be non-overlapping. Also, clocks N3, N4 and N5 have to be non-overlapping as well. This non-overlapping clocking scheme is necessary in order to minimize signal dependent charge injection [6]. In Fig. 6.10, the two-phase non-overlapping clock generator circuit is presented. This circuit generates two non-overlapping clock signals N1 and N2 as well as their delayed versions N1D and N2D. Both rising and falling edges of the N1D and N2D are delayed with respect to their undelayed versions. Actually, it is sufficient to delay only the falling edges in order to increase settling time for the integrators [5, 7] but this is not preferred

because the delay between the delayed and undelayed versions of the same clock signal is around relatively small (200-400ps).

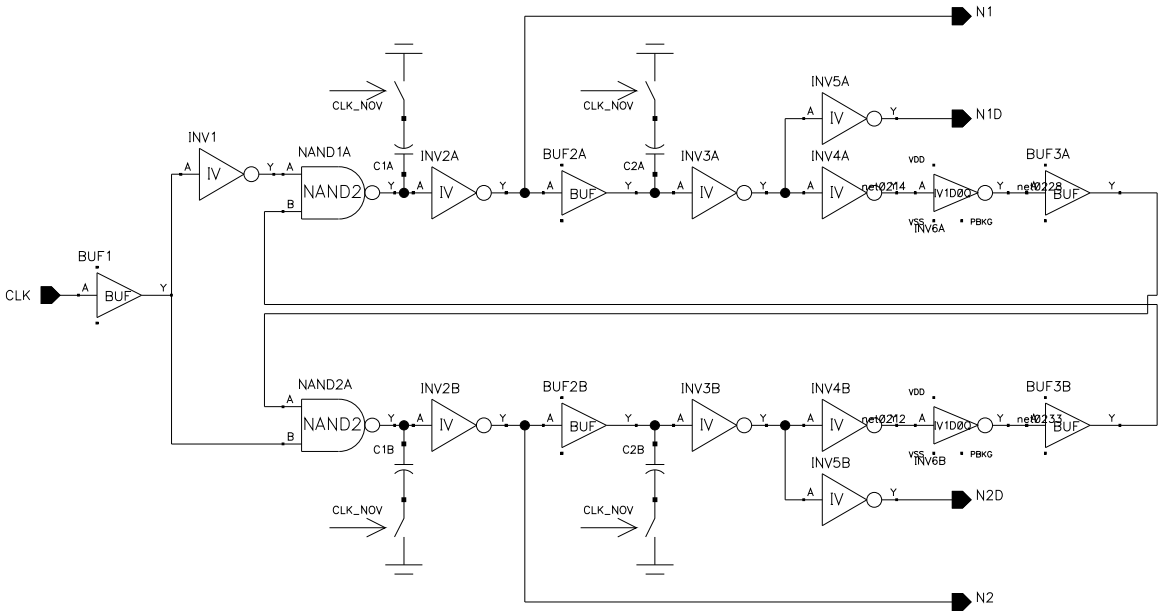

Figure 6.10: Two-phase nonoverlapping clock generator

In order to have some flexibility in adjusting the non-overlapping and delay times between the two clock phases, $100fF$ capacitors that can be switched on/off are added to the design. These capacitors are controlled by a control signal CLK_NOV. If the duty cycle of the input CLK signal is adjusted then the non-overlapping clocks will be automatically adjusted to reflect the same duty cycle with this circuit.

One important reason for the use of this clock circuit to generate the non-overlapping clock signals is the use of feedback. Because of the feedback, it is enough to match the delay of the paths above and below in order to have non-overlapping clocks.

The clock generator circuit operates from a 1.3V supply. Hence all the clock outputs will be 1.3V. This is not high enough to drive the CMOS switches in the sampling stage of the integrators. Therefore, as we have discussed, these clock signals will go through the level shifters and will be shifted upto 1.5V before reaching the switches.

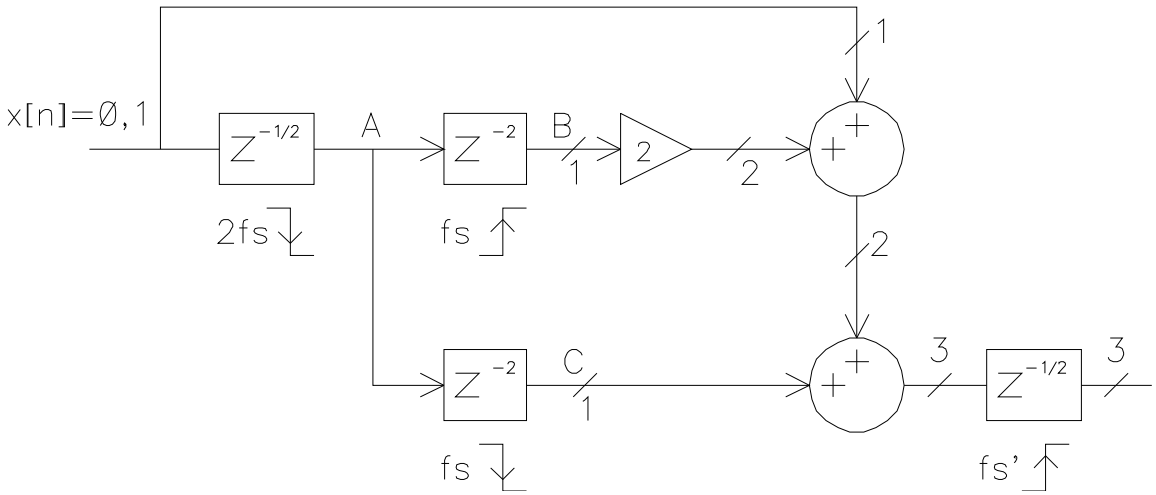

Figure 6.11: Modified diagram of the FIR filter to write RTL level VHDL code

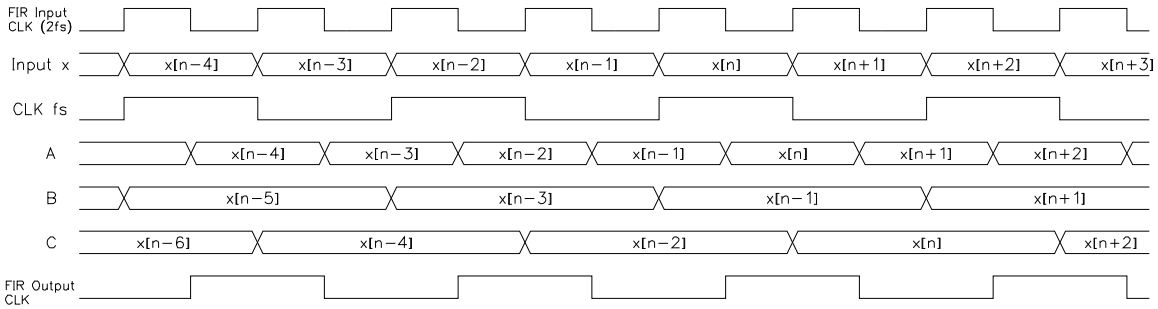

Figure 6.12: The clocking of the FIR filter and other timing information

6.2.7 Design and Implementation of the FIR filter

The block diagram of the FIR filter structure used in the proposed system was given in Fig. 5.10. In order to write the RTL level VHDL code for this filter and then synthesize it with Synopsys tools, this block diagram is modified as seen in Fig. 6.11. On this figure, the maximum number of bits that every register is required to be is also provided.

In Fig. 6.12, the clocking arrangements for this filter and timing information is provided. On this figure, A, B and C show the contents of the registers that was labeled on Fig. 6.11.

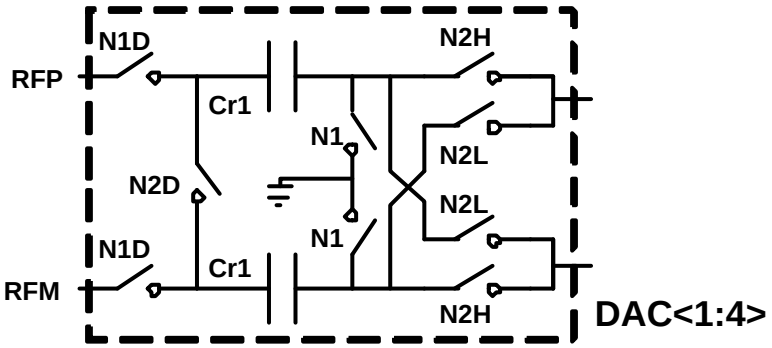

Figure 6.13: DAC element used in the first integrator (Fig 5.7)

6.2.8 Individual Level Averaging for Dynamic Element Matching

The output bits of the $\Sigma\Delta$ modulator are also used as a feedback to the input of the first integrator. In particular, four parallel DAC elements shown in Fig 6.13 are employed within the first integrator architecture. Signal N2H on Fig. 6.13 is obtained by ANDing the thermometer code bit at the output of the modulator with the N2 clock phase. N2L is the inverse of N2H. Since we have four thermometer code bits at the output of the modulator, we need to use four of these DAC elements in parallel to construct the D/A converter in the feedback of the $\Sigma\Delta$ modulator.

In order to alleviate the DAC non-linearity problem that occurs because of the mismatch between C_{r1} in DAC$< i >$ (i=1,2,3,4), a dynamic element matching technique (DEM) should be utilized. In this design, individual level averaging technique (ILA) is selected because of its simplicity and effectiveness in multibit systems with relatively low number of bits generated by the quantizer.

Table 6.2 illustrates how the ILA technique works for our system. In our case, there are 5 possible outcomes at the output of the FIR filter depicted in Fig 5.6. This is shown as thermo-codes in the table. Ideally, in each one of these possible outcomes, one bit of the 5-bit word should be 1 and the remaining bits should be 0. However, sometimes, FIR block may generate glitches at its output and more than one bits may be 1. In order to prevent this, a priority encoder is placed right at the input of

Table 6.2: Truth table for the Individual Level Averaging(ILA) Block.

Thermo-code $TC < 3:0 >$	Priority Enc. $K < 4:0 >$	Number of Patterns	ILA outputs $HL < 7:0 >$
1xxx	10000	1	11110000
01xx	01000	4	11100001
			11010010
			10110100
			01111000
001x	00100	2	11000011
			00111100
0001	00010	4	00011110
			00101101
			01001011
			10000111
0000	00001	1	00001111

the ILA logic. The ILA logic keeps a pattern index for every possible input. This index is the memory of which DAC element will be used in the next clock cycle by the integrator. As we can see from the table, we only need pattern indexes for inputs 01000, 00100 and 00010. The other two inputs have only one pattern and therefore we do not need an index for these cases.

The VHDL code of the ILA logic is written and the schematic and the layout is syntesized from this code by making use of Synopsys [52] design synthesis tools.

6.2.9 Bias generator

There is an input pin from which the chip is supplied an input current. This input current has to be replicated to generate all the bias currents needed by the circuits in the system. Specifically, the circuits that will require a bias current are the amplifiers in the first and second integrators and the comparator.

The circuit shown in Fig 6.14 is designed to serve for this purpose. The NMOS transistors are cascoded to improve matching by equalizing V_{DS} of mirror transistors. The comparator circuit receives the bias current input to an NMOS device. Therefore,

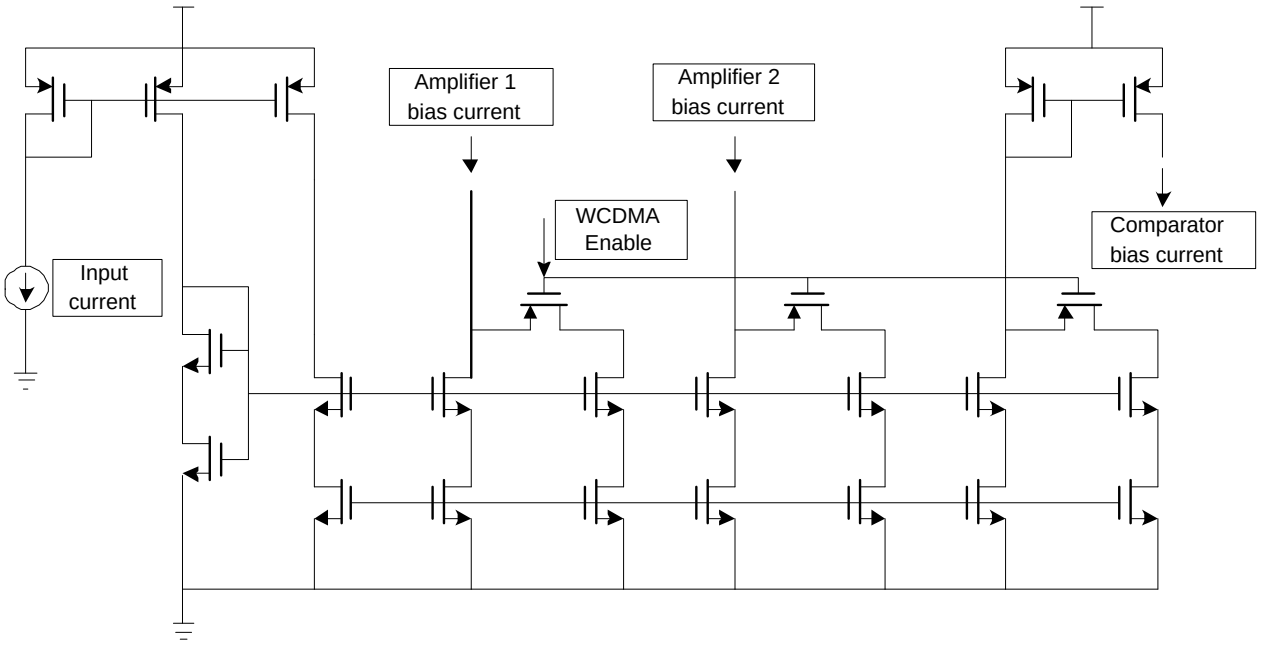

Figure 6.14: The bias generator circuit

it goes through an additional current mirror. The current outputs from this block are carefully shielded when they are routed to individual circuit blocks.

Note that the bias current supplied to the amplifiers and the comparator are controlled by a digital control bit WCDMA Enable. Since this modulator is designed for a dual mode system, this control bits provides an option to increase the bias current by 50% by setting the control bit to 0.

6.2.10 Layout Considerations

Since interference of noise and other signals is a significant concern, care should be taken in the layout to isolate sensitive nodes in the circuit from sources of interference. This was accomplished primarily by shielding and using separate ground and supply voltages. In addition to these, there are some other important layout considerations implemented in this design and those will be briefly mentioned in the following few sections.

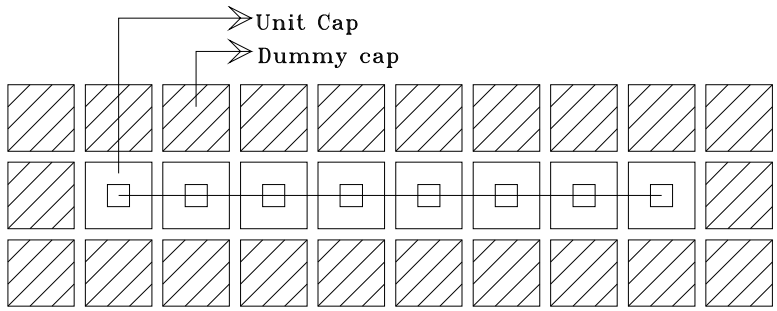

Figure 6.15: Sampling Capacitor Array in the layout

6.2.10.1 Sampling and Integrating Capacitor Layout

The sample and hold amplifier input is the most critical node of the integrated circuit. Therefore, a great deal of care was taken to shield this node from sources of interference. The input to the ADC is also rather sensitive. Therefore, special attention was given to the layout of the sampling and integrating capacitors, which connect both of these nodes. Fig. 6.15 shows how these capacitors are actually laid out in the design. The sampling capacitor, which is 400fF, is composed of 8 unit capacitors of 50fF each. They are surrounded by a ring of grounded dummy capacitors. These dummy capacitors are used to shield the sampling capacitors from interference and to improve matching by making the edge effects similar [37] [42] [47]

6.2.10.2 Interconnect Layout and Shielding

Because the amplifier outputs and inputs are sensitive nodes, the interconnect used to connect the output of one stage to the next stage was also shielded as shown by the cross section in Fig. 6.16. Keeping the signal lines close together prevents other signals from coupling inductively to the signal. Also, the signal lines are surrounded on four sides by grounded conductors to minimize capacitive coupling of sources of interference onto the signal.

Supply noise is a significant problem that often limits the performance of high

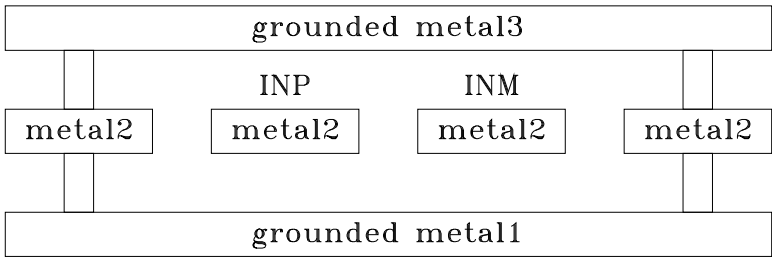

Figure 6.16: Cross sectional view of the shielded interconnect line

resolution high speed analog circuits. Supply noise occurs when variable currents are injected into the supply. For example, in digital circuits where fast switching transients occur, glitches will be added to the supply voltage during the rise and fall of digital data and clock. In the ideal case, when the supply impedance is zero (i.e., the impedance from the supply pin of the chip to the circuit needing that supply is zero), these currents have no effect. However, a real supply voltage source has a finite impedance. As a result, these noise currents cause variations in the supply voltage. These supply voltage variations are then coupled into the signal.

To alleviate this problem, various techniques are used. One technique is to design the circuit in such a way that supply noise is not coupled into the signal. In other words, the circuit is designed such that the power supply rejection ratio (PSRR) is high. One very effective way of accomplishing this is to use fully differential circuit architectures. A fully differential circuit architecture has both positive and negative input and output terminals. Therefore, the signal never has to be referenced to either the positive or negative supply. To first order, the supply noise couples equally onto both the positive and negative signal. When the difference is taken, this supply noise is cancelled out. The fully differential architecture also has the advantage that

variations in current are reduced because increases in current in a positive branch of the circuit tend to be balanced by reductions in a negative branch. This technique is so effective that although it has the disadvantage that extra hardware and complexity is required in comparison to a single ended circuit, it is still very widely used by the designers.

Another way of minimizing degradation due to supply noise is to reduce the noise current on the supply. This can be accomplished by using multiple supplies and isolating the supplies requiring low noise from the digital supplies and other noisy supplies.

A third way is to use local decoupling capacitors inside the design. The decoupling capacitor will be connected to the supply voltage and needs to be placed as close to the circuit as possible. It essentially filters the noise riding on top of the supply line. The more the decoupling capacitor is, the better the filtering is going to be. So, especially after the major layout work is done, it is a good practice to find white spaces in the layout and fill them with decoupling capacitors in order make the supply voltage better.

Finally, supply noise can be reduced by reducing the impedance of the supply. By reducing the impedance, the quantity of supply noise for a given noise current can be reduced. The way to do this is to increase the width of the power supply lines as much as possible. Since metal resistance is usually given in terms of sheet resistance per square in integrated circuit design, increasing the width of the supply lines means that there will be fewer squares from the supply pin to the circuit and hence the resistance will be smaller.

6.3 TOP LEVEL SIMULATION RESULTS AND DISCUSSION

The MM-ΣΔ modulator proposed in chapter 5 is constructed in Cadence and simulated in Spice using a 90nm digital CMOS process.

Fig 6.17 shows the 8192-point FFT of the modulator output spectrum obtained from Spice simulations. The input signal frequency is 30kHz with amplitude of -6dB with respect to the reference voltage (Vref=0.75V).

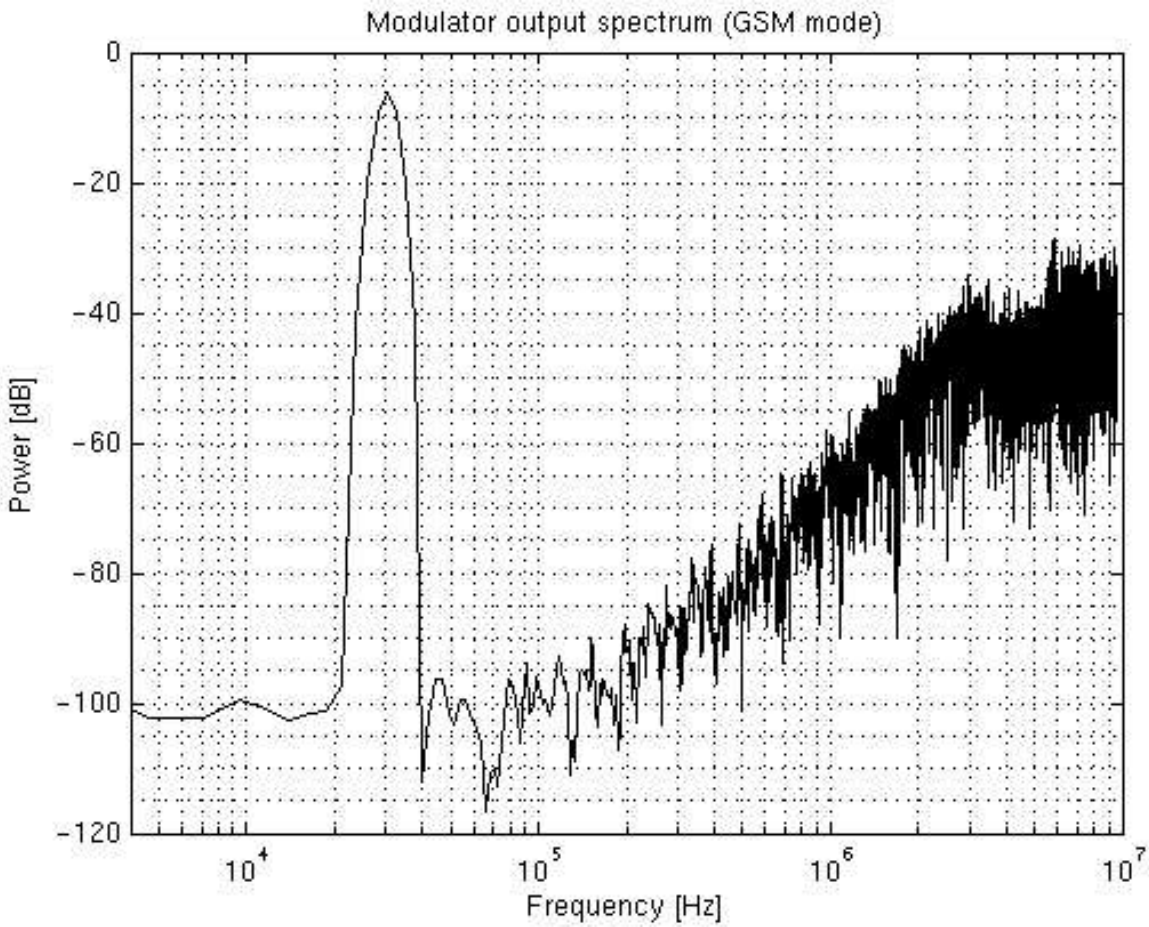

Figure 6.17: Modulator output spectrum in GSM mode

In Fig. 6.18, the simulated SNDR versus input signal amplitude with respect to the reference voltage is given. The x-axis is a voltage quantity. Therefore, -6dB signal with respect to the reference voltage means that the peak amplitude of the

differential input signal is half of the reference voltage, which is 0.75V in this design. The input is a sinusoidal signal with frequencies of 30kHz and 400kHz in GSM and WCDMA, respectively. In this plot, the input power is increased with a step of 10dB from -30dB to -10dB. Then, the step size is reduced to 1dB. Peak SNDR occurs at an input power of -4dB for GSM and -3dB for WCDMA. Any signal higher than this input power causes the modulator to overload. However, normally, once the maximum input signal amplitude that can be applied to the modulator is found, the amplitude of the time varying signal applied to the modulator is chosen a few dB smaller than this maximum signal level in order to have enough safety margin.

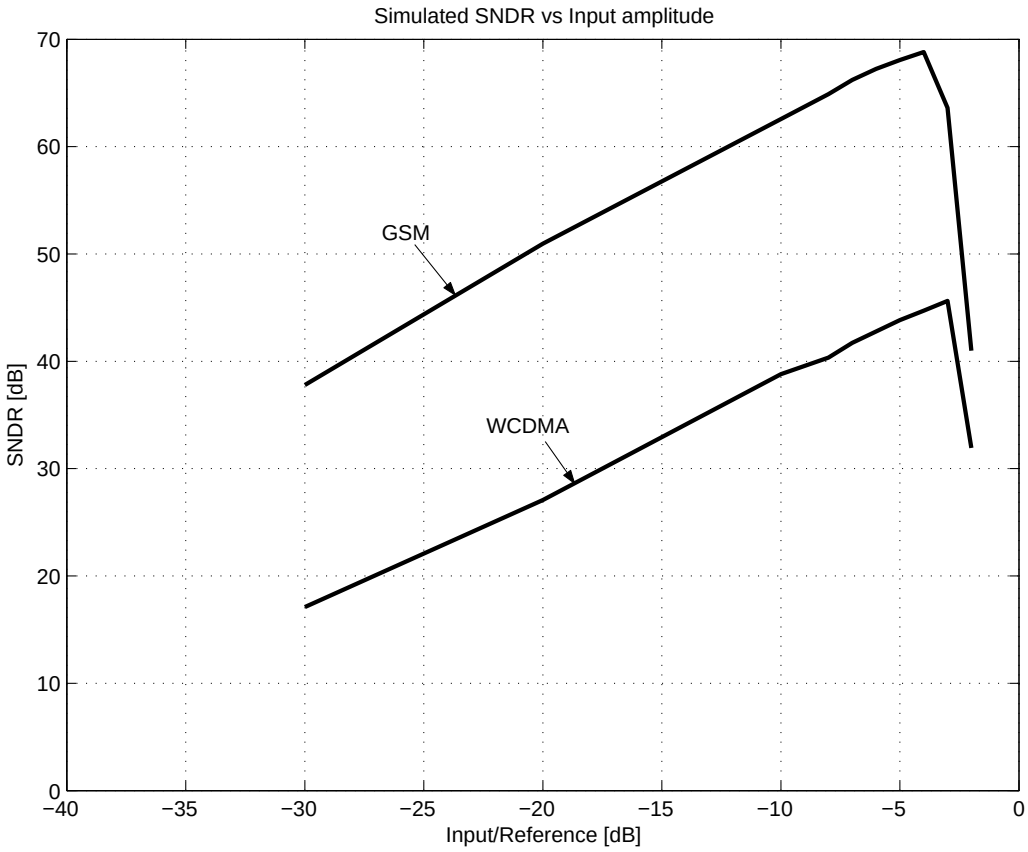

Figure 6.18: Simulated SNDR versus input signal level in GSM and WCDMA modes

6.4 SUMMARY

An experimental prototype that is built by using switched-capacitor circuit design techniques is presented in this chapter. This dual-mode multirate multibit $\Sigma\Delta$ modulator is designed in 90nm digital CMOS process without analog add-ons. It is targeted for mobile communication applications (specifically for GSM and WCDMA) and occupies only $0.165mm^2$ of silicon area.

Chapter 7

EXPERIMENTAL RESULTS

7.1 INTRODUCTION

Measurement results of the fabricated prototype is presented in this chapter. However, because of its importance, the measurement setup will be described prior to the presentation of experimental results.

7.2 MEASUREMENT SETUP

In a $\Sigma\Delta$ modulator, there are analog circuits such as the integrators and digital circuits such as the nonoverlapping clock generator, comparator, level shifters, dynamic element matching block and output drivers. In order to prevent the noise coupling through the supply and ground lines between the noisy digital circuits and sensitive analog circuits, we need to take a few precautions. First of all, seperate supply lines and pads have to be used for the analog and digital parts. In this design, since the values of these supplies are different from each other, this was mandatory. But, even if they were equal in value, they should have been seperated from each other. Inside the chip, as we have already discussed in previous chapters, the noise coupled through the substrate can be significantly reduced by making guard rings around digital and analog parts and connecting them to the proper supply or ground lines.

Another important consideration about the supply lines is to star-connect the supply and ground lines of every important circuit in the system to the pad. By doing so, we isolate each circuit from each other. Although this may bring some area

loss due to extended routing channels for supplies and grounds, it is necessary in the design of high performance systems like the one described in this thesis.

Analog and digital power supplies and the ground have two dedicated pads each to have a robust supply connection to the chip. Moreover, significant amount of decoupling capacitors are added between each one of the supplies and ground.

Fig. 7.1 illustrates the configuration of the instruments used to evaluate the performance of the device under test (DUT). The test circuit is powered by an HP E3616A DC power supply. The differential input of the modulator is generated by a sinewave generator (HP 8664A 0.1-3000MHz Synthesized Signal Generator). The outputs of the signal generator are connected to the test board through coaxial cables and terminated by a 50Ω resistor in order to match the 50Ω output impedance of the signal generator. The modulator output bit stream is captured by a logic analyzer (Tektronix TLA704). Then, it is transferred to a workstation for subsequent processing in Matlab [53]. The clock to the system is provided by a waveform generator (Wavetek 100MHz Synthesized Arbitrary Waveform generator). This same clock is also connected to the logic analyzer to sample the output bit stream coming from the modulator.

The test board is implemented using a printed circuit board (PCB). Following PCB design techniques that are proven and recommended for high-performance mixed-signal ICs are used in this PCB design [55, 56]:

- Partitioning the board with analog components in one area whereas all the digital components are in another area.

- Two seperate ground planes. One of them is for analog with all the analog components, supply and signal traces placed over the analog ground plane. The second one is for digital with all the digital components, supply and signal traces placed over the digital ground plane.

- Orientation of the DUT should be such that all the analog and digital pins reside in analog and digital areas, respectively.

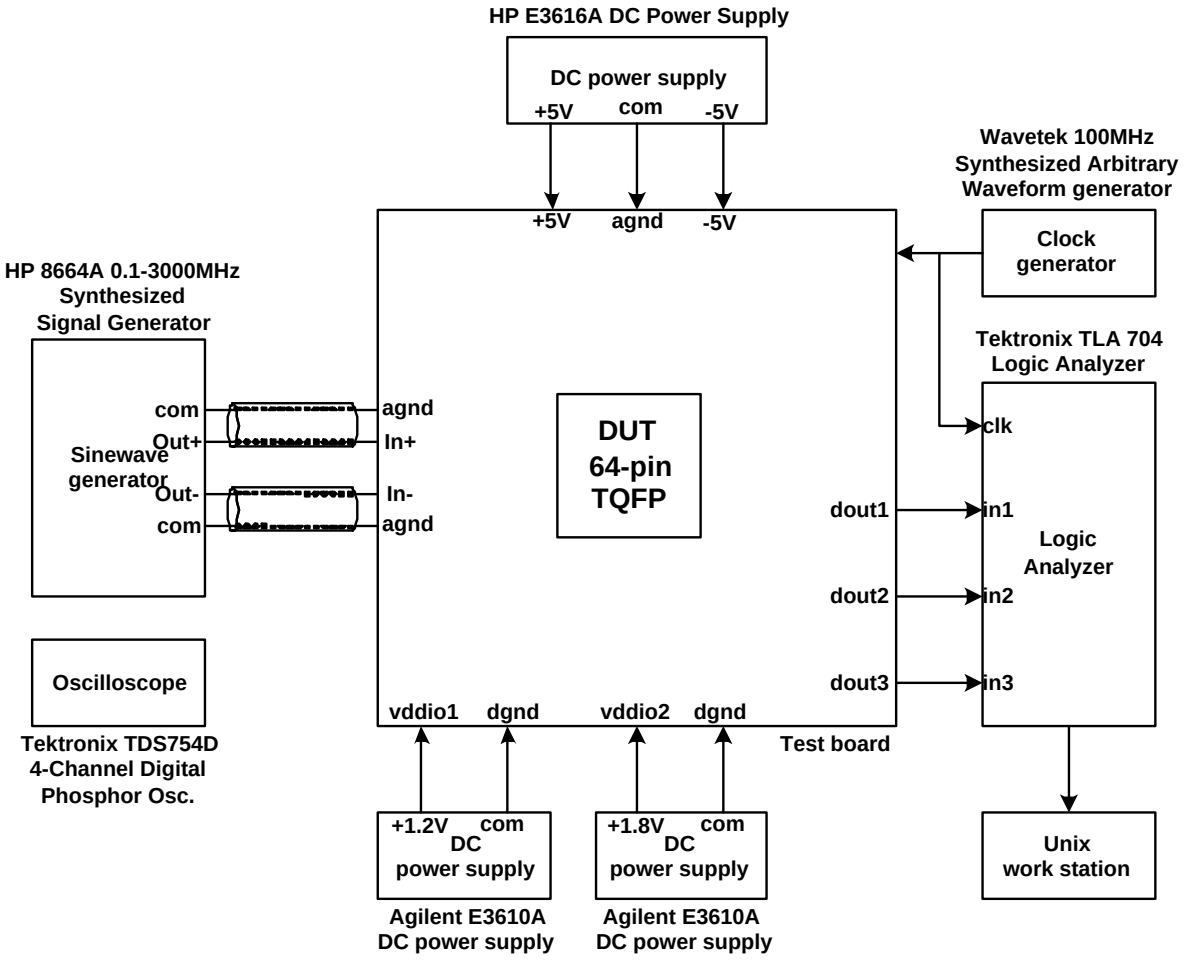

Figure 7.1: Test setup.

- Connecting the analog and digital ground planes at one point only.
- Placing decoupling capacitors very close to the pin.
- Keeping digital traces away from the highly sensitive analog lines.

Fig. 7.2 shows the PCB from the top. The DUT is connected to the board via a socket.

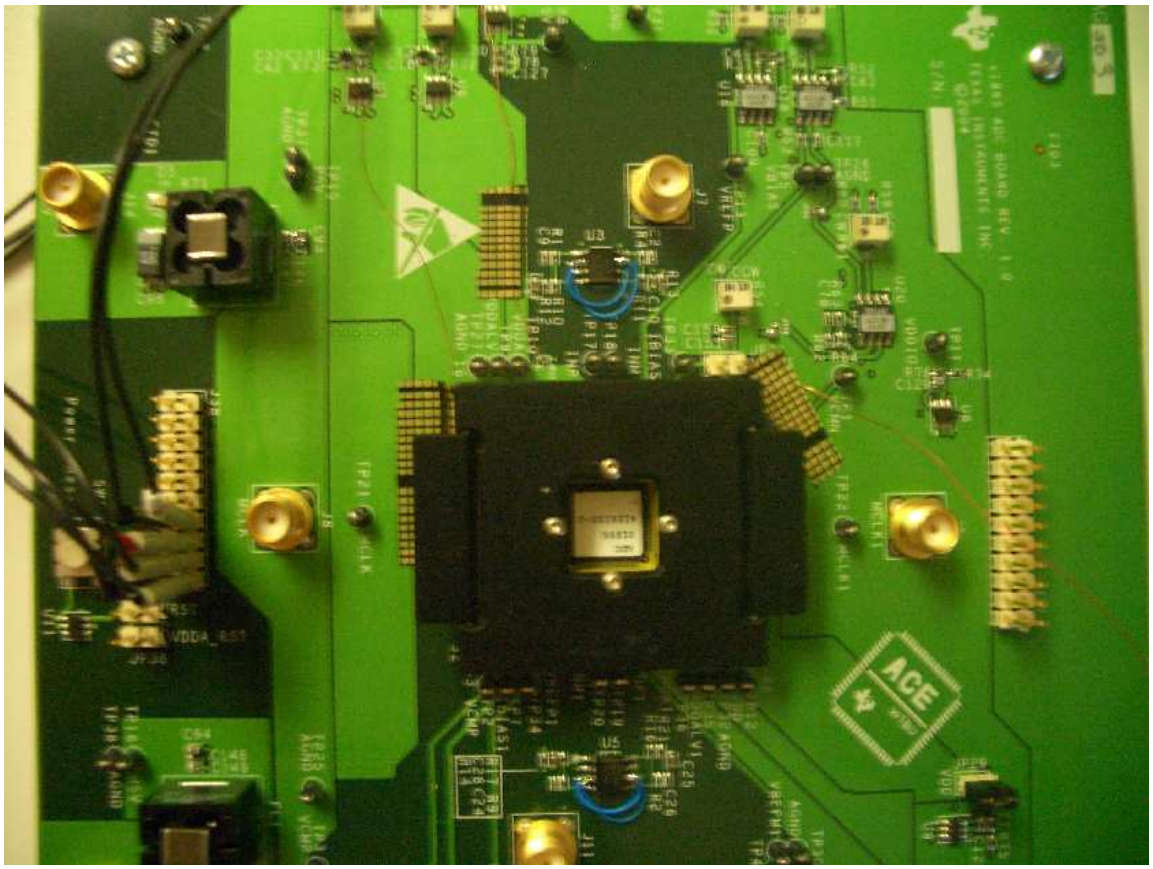

Figure 7.2: Top photo of the PCB.

7.3 RESULTS

A die photo of the prototype modulator implemented in a 90 nm single-poly, five-metal CMOS process is shown in Fig. 7.3. The chip active dimensions are 450μm x 350μm and the area is 0.16 mm^2. The chip is bonded to a 64-pin TQFP package and placed on the Printed Circuit Board (PCB) using an appropriate socket.

Fig. 7.4 shows the simulated and measured SNDR, in GSM mode, as a function of input power for a 30kHz sinusoidal input across a 200kHz signal band with an oversampling ratio of approximately 36. The modulator achieves 68.6 dB peak SNDR at -4dB input level. In GSM mode of operation, the modulator requires a total current of 1.1 mA. 1mA of this current is supplied from a 1.5 V analog supply and the remaining $100uA$ is supplied from a 1.3V digital supply.

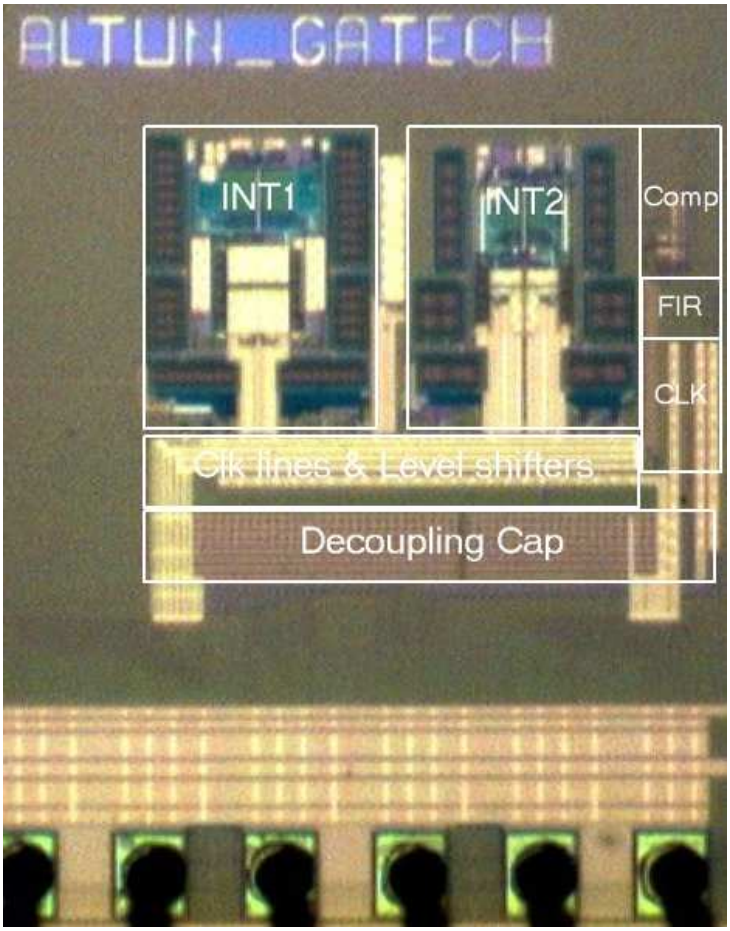

Figure 7.3: Die photo of the experimental prototype.

In Fig. 7.5, the simulated and measured SNDR in WCDMA mode of operation is presented. In this mode, the signal band of interest is 2MHz and the oversampling ratio is approximately 10. The modulator achieves 42.8 dB peak SNDR at -4dB input level. In WCDMA mode of operation, the modulator requires a total current of 1.9 mA. 1.7mA of this current is supplied from a 1.5 V analog supply and the remaining $200uA$ is supplied from a 1.3V digital supply.

In order to see what is limiting the peak performance, we look at the FFT of the output bit stream when the chip was operated in GSM mode. This is shown in Fig. 7.6. The input signal in obtaining this FFT plot was ≈15kHz and the amplitude of the input signal was -6dB with respect to the full scale reference voltage, which is near the maximum signal level that the modulator is designed to handle. Recall that

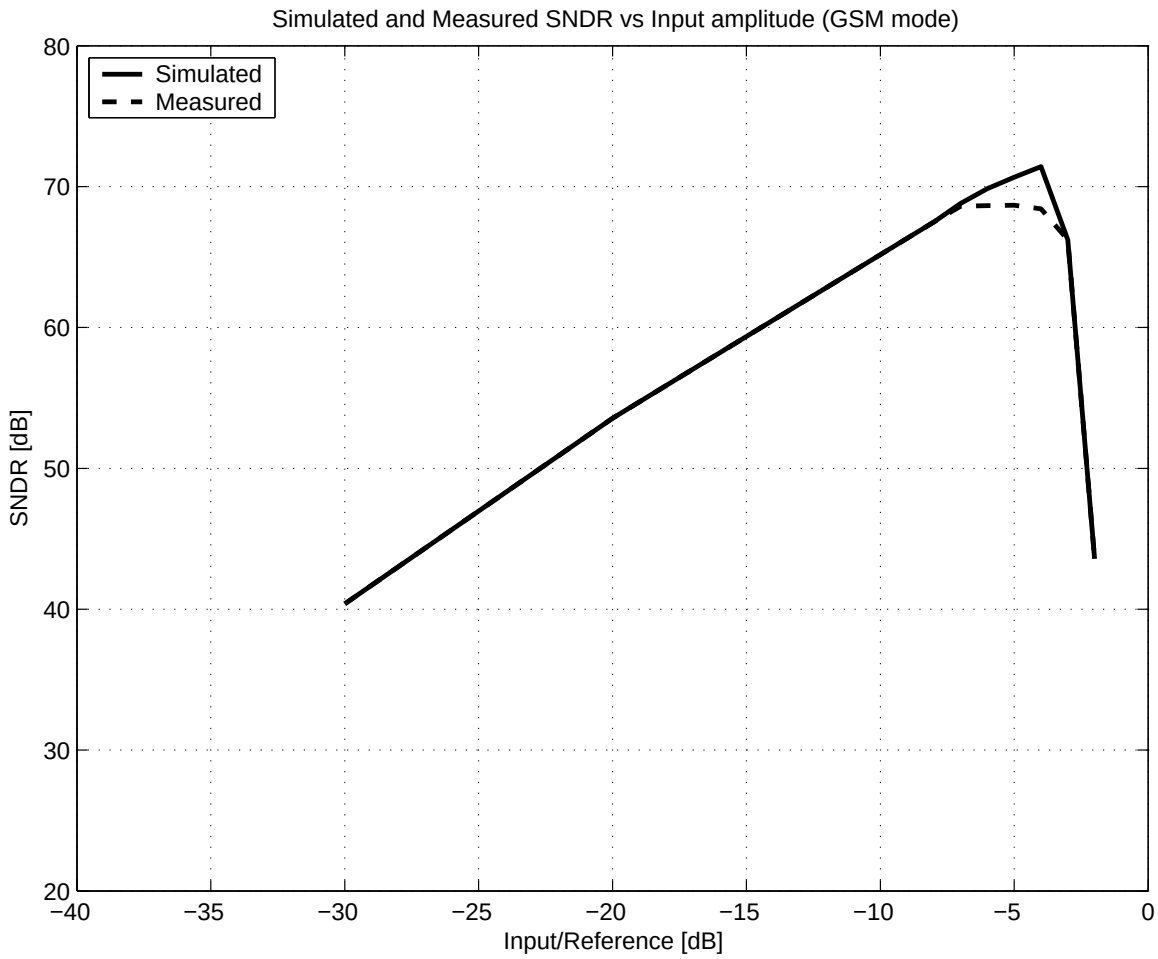

Figure 7.4: Simulated and measured SNDR versus input power across 200kHz signal band (GSM mode).

reference voltage is 0.75V in this particular design.

The number of points in this FFT plot is $2^{17}/3 = 43691$. The reason for this is as follows: The input clock that the modulator is receiving from outside of the chip is three times the sampling rate of the first integrator. Furthermore, the modulator output rate is equal to the first integrator sampling rate. The test equipment that is used for capturing the output bit stream needs an input clock to sample the incoming bit stream. The only clock signal that was available for this purpose was the input clock of the modulator. Therefore, all the digital data that were captured by this equipment was repeated 3 times as the sampling clock is three times as fast as the

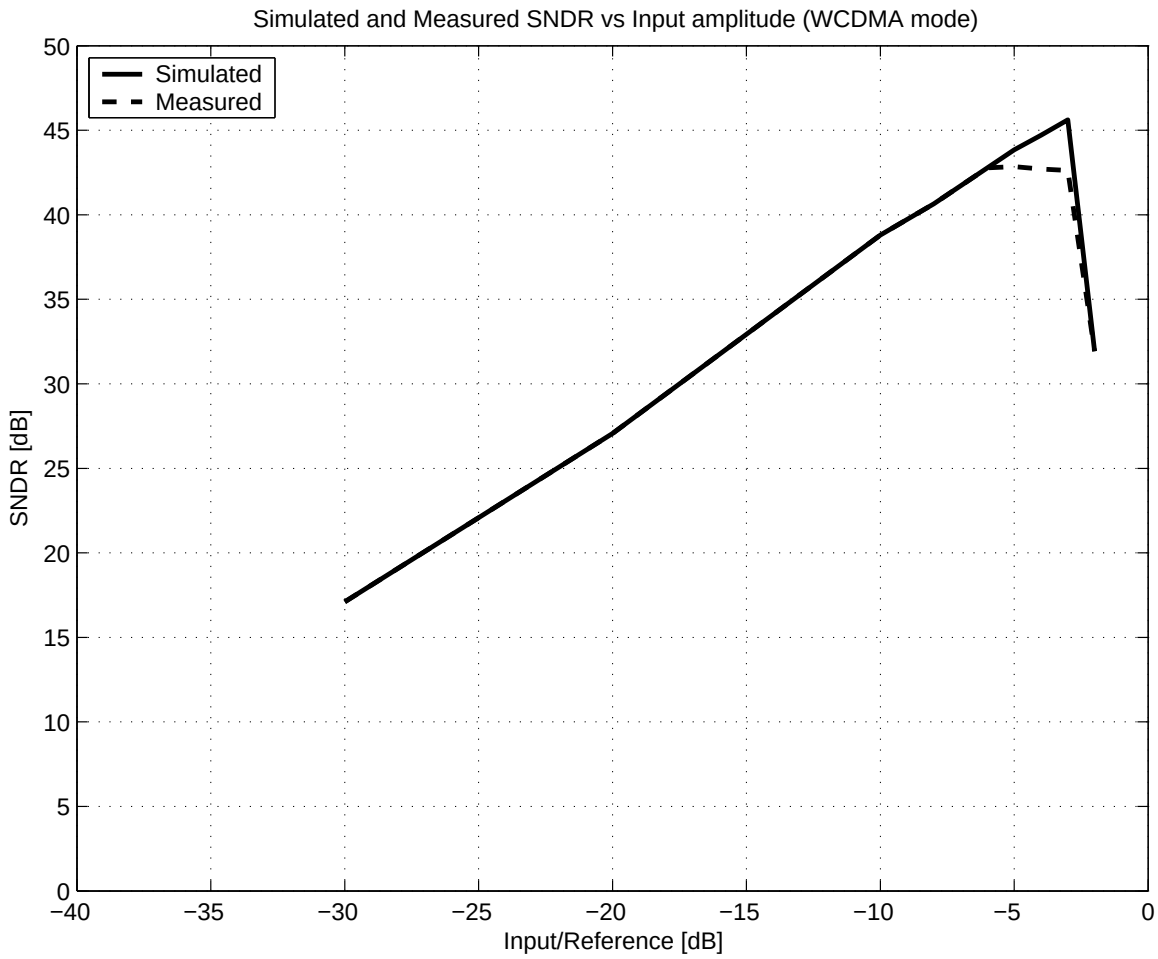

Figure 7.5: Measured SNR/SNDR versus input power across 2MHz signal band (WCDMA mode).

output data rate. That means that the first of these 3 consecutive data samples were useful whereas the next 2 samples were redundant. So, in order to take the FFT with the useful data samples, the output bit stream is downsampled by 3. As a result, when we were trying to capture 2^{17} number of FFT points, we were only getting one third of this.

Looking at this FFT plot, the first important observation is the third and fifth order harmonic components in the spectrum. One potential reason for these harmonic components is the lower than required DC gain provided by the operational transconductance amplifiers in the system. Note that the DC gain of the OTA without large

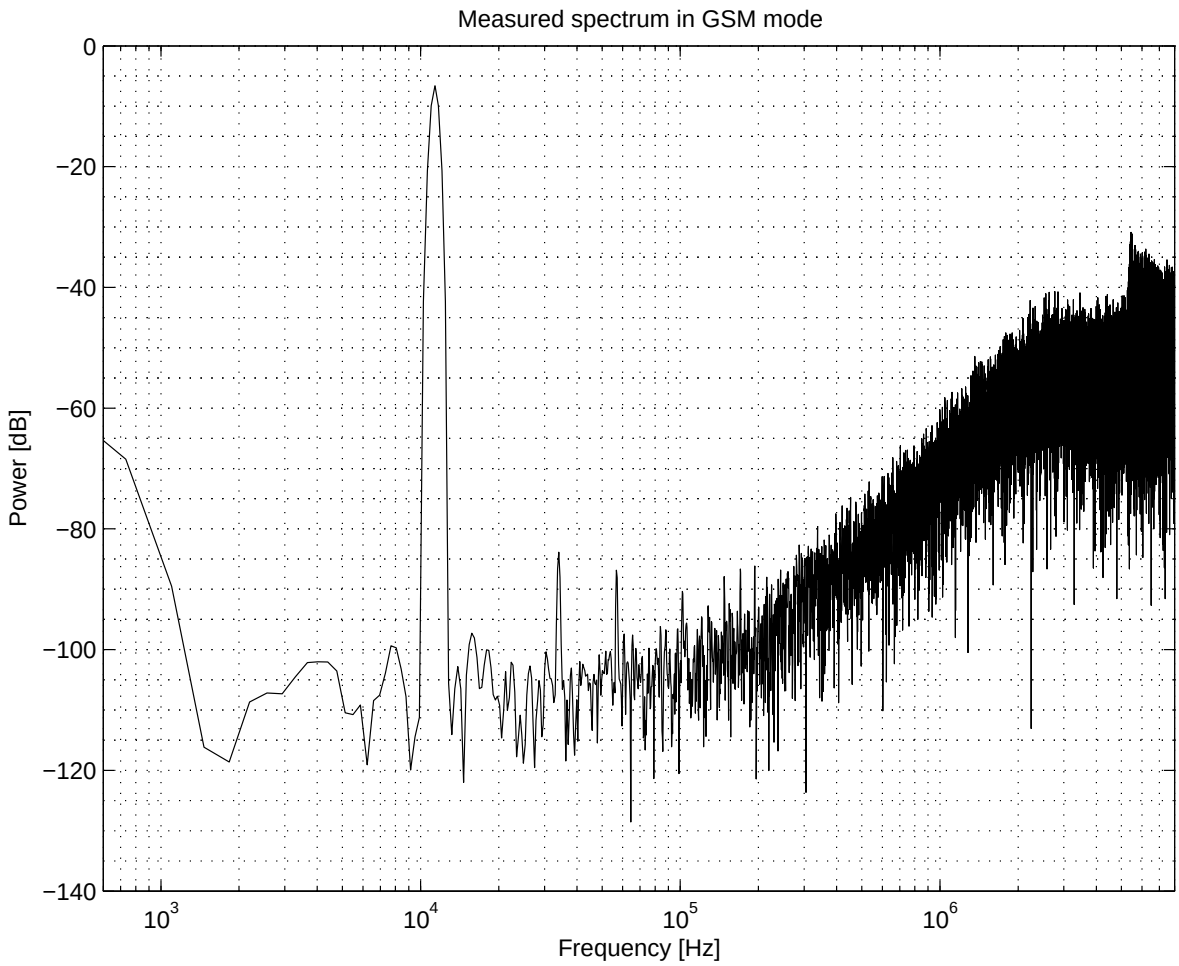

Figure 7.6: FFT for -6dB signal in GSM mode.

signal swings at its output will be generally high. However, as it is the case with many $\Sigma\Delta$ modulators reported in the literature, the signal swing at the output of the first integrator in this design is large as compared to the voltage supply. Consequently, the output cascode devices will be pushed towards the linear region of operation when the output signal swing is large and this will degrade the DC gain of the OTA. Although this case was simulated in Spice before the chip was taped out, we have not observed lower than 45dB of DC gain in different process and temperature corners at peak output swing conditions. However, note that the process did not have fully mature Spice models at the time of the tape out and this may be one of the reasons why we have not seen this in simulations.

The second observation in the output spectrum is the existence of a DC component. There could be a number of reasons for this component. First of all, the design is aggressively scaled down to reduce parasitics as much as possible in order to save power. One potential problem with this approach is that the input differential pair transistors inside the amplifier of the first integrator may be smaller than they need to be. When these devices becomes smaller, their matching properties tend to become worse. Any mismatch between these devices will show itself as input offset. Since this happens at the input of the modulator, it will be added to the input signal and show itself at the output of the modulator as a DC component. Furthermore, when the input signal that is coming from the signal generator is investigated, it is found to have some very small offset as well. So, some part of the DC component we see in the output spectrum comes from the imperfections of the signal generator. It should be noted that as we take more number of samples at the output and increase the number of FFT to decrease the frequency bin width(finer resolution), we will see that the offset will have a smaller spread in the frequency axis. For example, if N is increased by 3, then offset will be seen spread from 0Hz to 500Hz rather than to 1500Hz.

Final observation on the output spectrum plot given in Fig. 7.6 is the shape of the spectrum at very high frequencies (close to $f_s/2$). This behaviour is not investigated in full detail because in real implementation high frequency part of the spectrum will be filtered out by the decimation filter that is following the modulator. However, because there is an abrupt rise in the quantization noise spectrum close to $f_s/2$, there can be some kind of folding effect taking place inside the system. Remember that the sampling clock frequency of the second integrator is twice as much as the sampling clock frequency of the first integrator. Furthermore, we are down-sampling the data rate by 2 right after the second integrator.

Table 7.1: Comparison of three different $\Sigma\Delta$ architectures including the work reported in this thesis.

	W1 (This work)	W2	W3
First amplifier current consumption	650uA	1144uA	650uA
Second amplifier current consumption	325uA	572uA	325uA
Quantizer static current consumption	30uA	30uA	120uA
Quantizer area	$0.0075mm^2$	$0.0075mm^2$	$0.07mm^2$
Total $\Sigma\Delta area$	$0.16mm^2$	$0.16mm^2$	$0.23mm^2$

7.4 COMPARISON OF $\Sigma\Delta$ ARCHITECTURES

At this point, we can compare different $\Sigma\Delta$ architectures mentioned in this thesis. Table 7.1 summarizes the comparison result of the three architectures with respect to a number of important criteria: current consumed by the first and second integrators as well as the quantizer, the area occupied by the quantizer and the total area occupied by each of the $\Sigma\Delta$ architectures provided that each of these architectures were implemented in the same process technology (in this case, it is the 90nm digital CMOS process).

In Table 7.1, the column named as W1 is the work explained in detail in this thesis. The second column W2 is the Multirate Multibit $\Sigma\Delta$ modulator without the idea presented in this thesis. Instead, it uses the brute force approach depicted in Fig. 5.4. Finally, the third column W3 is the conventional second order $\Sigma\Delta$ modulator which was mentioned in Fig. 5.1.

As we can see from Table 7.1, the work presented in this thesis requires significantly less power than W2. On the power consumption front, it yields the same performance with W3. On the other hand, in terms of area occupied by the chip, this work and W2 are almost the same whereas this work occupies approximately 30% less area than W3 on Silicon. So, among these three architectures, the proposed idea achieves the best of power requirement and area consumption.

Chapter 8

CONCLUSIONS

8.1 INTRODUCTION

This chapter summarizes key research contributions and results. There were a couple of motivations at the onset of this work: 1) Addressing the issue of integration in RF receivers with an emphasis on the baseband A/D converter. 2) Addressing the issue of programmability in these converters. 3) Devising new techniques along with the use of existing techniques for minimizing the power dissipation of high-speed $\Sigma\Delta$ modulator. Integration is an important issue in reducing the cost, power dissipation and form factor of RF transceivers. Programmability will allow future RF transceivers to adapt to multiple communications standards with varying bandwidth and dynamic range requirements. While the RF application was emphasized, techniques for minimizing power dissipation in $\Sigma\Delta$ modulators are important to extend battery life in any portable application.

8.2 KEY RESEARCH CONTRIBUTIONS AND RESULTS

Key research contributions and results are summarized below:

- The issues with the ideal MM-$\Sigma\Delta$ modulators are addressed with a new integrator architecture and a novel clocking scheme. This made the practical implementation of such systems possible.

- Demonstrated that a MM-$\Sigma\Delta$ modulator can meet the baseband processing requirements for RF receivers at a reasonable power dissipation. An experimental prototype implemented in a 90nm single-poly, 5 metal CMOS process achieved 68.6dB of Signal-to-Noise and Distortion ratio (SNDR) and dissipated 1.1mA of current across 200kHz signal band. This dual mode modulator also achieved 42.8dB of SNDR across 2MHz signal band and dissipated 1.9mA.

- Showed that scaling integrator sampling capacitors to the minimum value required by kT/C noise at each stage is an effective technique for reducing power dissipation.

- The optimization of circuit specifications in behavioral simulations for minimizing power consumption is shown to be an effective way of designing power efficient $\Sigma\Delta$ modulators.

8.3 RECOMMENDED FUTURE WORK

This work served primarily as a proof of concept that MM-$\Sigma\Delta$ modulators are good alternatives to modulators designed with conventional approaches. They can meet the specifications of a wideband RF system without excessive power dissipation or a large silicon area. In fact, as it is shown in this thesis, they provide power and area savings as compared to conventional methods. The next step would be to integrate the modulator with the other blocks in the receive path to demonstrate an overall system. Issues such as substrate noise and other coupling mechanisms will need to be addressed carefully as part of this integration effort.

An area that requires further attention is the use of double-sampling techniques in the second integrator to effectively create an upsampling in the second integrator without increasing the sampling clock itself. This will simplify the design of the non-overlapping clock generator circuit. It also helps reduce the potential folding effects inside the system that may be the direct result of multiple clock signals in the system.

Although this may require a novel structure for the second integrator, it can simplify the whole system significantly.

The power optimization of the baseband processing block as a whole is another area where further research is required. Power trade-offs when the requirements on the continuous-time antialiasing filter are considered along with those of the $\Sigma\Delta$ modulator should be explored. This work could lead to a more power efficient baseband block as compared to optimizing the modulator alone.

8.4 RELATED PUBLICATIONS

Oguz Altun, Jinseok Koh and Phillip E. Allen, "A 1.5V Multirate Multibit $\Sigma\Delta$ Modulator for GSM/WCDMA in a 90nm digital CMOS process," *International Symposium on Circuits and Systems (ISCAS)*, Kobe, Japan, May 2005.

Oguz Altun, Jinseok Koh and Phillip E. Allen, "Multirate Multibit $\Sigma\Delta$ Modulators for Wireless Applications," *Texas Instruments High Performance Symposium*, Tucson, Arizona, April 2005.

Appendix A

EXTENDING THE PROPOSED IDEA TO IMPLEMENT HIGHER PERFORMANCE $\Sigma\Delta$ MODULATORS

A.1 INTRODUCTION

One of the most exciting aspects of the proposed MM-$\Sigma\Delta$ design technique is that it allows us to improve the performance of our $\Sigma\Delta$ modulator by making relatively simple changes to the system we use to replace the flash ADC. In the following, a few options are discussed to enable the designer build a very high DR modulator. Note that these options will be given for a second order $\Sigma\Delta$ modulator. However, the technique explained in this report is easily applicable to higher order single loop modulators and cascade $\Sigma\Delta$ modulators as well.

A.1.1 Option 1

This is the option that is used in the current design. In the 2nd integrator, we employ an upsampling by 2 (i.e., M=2) and we use 2 sets of capacitors in the 2nd integrator architecture to sample the output of the 1st integrator. The order of the comb filter is 2 and hence its transfer function can be written as:

$$H(z) = 1 + 2z^{-1} + z^{-2} \tag{A.1}$$

We only use a single bit comparator to quantize the output of the 2nd integrator. Therefore, the comb filter generates 5 different levels of output. Consequently, as

it was shown in 5, this system is equivalent to a 2nd order $\Sigma\Delta$ modulator with a quantizer resolution of c=2bits and a sampling frequency of fs in both integrators.

A.1.2 Option 2

This option is very similar to option 1 except the following. Instead of using a single comparator to quantize the output of the 2nd integrator, we use 2 comparators and generate 3 levels of signal (-1,0,1). Therefore, the comb filter now generates 9 different levels of output.

A.1.3 Option 3

If we use 4 comparators and generate 5 levels of signal (-2,-1,0,1,2), then the comb filter will now generate 17 different levels of output. Note that, in this case we would use a 5-level Flash ADC along with the digital block proposed in this report. This way, we end up with a high performance $\Sigma\Delta$ modulator.

In all the three options explained so far, we kept the 2nd integrator same and expanded our single bit comparator to a Flash ADC. Also note that the clocking scheme, which is a crucial part of the proposed design strategy, remained the same.

A.1.4 Option 4

In the 2nd integrator, we employ an upsampling by 4 (i.e., M=4) and we use 4 sets of capacitors in the 2nd integrator architecture to sample the output of the 1st integrator. The order of the comb filter is 3 and hence its transfer function can be written as:

$$H(z) = 1 + 3z^{-1} + 3z^{-2} + z^{-3} \tag{A.2}$$

We only use a single bit comparator to quantize the output of the 2nd integrator. Therefore, the comb filter generates 9 different levels of output.

A.1.5 Option 5

This option is very similar to option 4 except the following. Instead of using a single comparator to quantize the output of the 2nd integrator, we use 2 comparators and generate 3 levels of signal (-1,0,1). Therefore, the comb filter now generates 17 different levels of output.

A.1.6 Option 6

If we use 4 comparators and generate 5 levels of signal (-2,-1,0,1,2), then the comb filter will now generate 33 different levels of output. Note that in this option, once again we would use a 5-level Flash ADC along with the digital block proposed in this report.

One has to note that options 4,5 and 6 are limited with the speed requirement of the 2nd integrator. Because 4 integration periods and some additional time to account for the non-overlapping time between clock signals are required to fit in a half clock period. As an example, if fs=10MHz then T/2=1/(2fs)=50nsec. This much of time would be quite enough for all the integration and the additional time required. However, as we increase fs beyond this frequency, we need to increase the power budget of the second integrator and push the limits of our amplifier. Therefore, options 4, 5 and 6 are more appropriate for narrow signal band applications like voice and audio.

As it is obvious by now, one can extand the number of options even further. The parameters that we can play are the order of the comb filter H(z) and the number of comparators that we use to quantize the output of the 2nd integrator.

A.1.7 Summary

To have a better perspective among all these options mentioned above, we resort to the theoretical equation of the DR of a $\Sigma\Delta$ modulator (Equation 2.7). In this equation, B is the number of bits of the Flash ADC. For a B-bit Flash ADC, we have

$K = 2^B$ number of levels. If we replace 2^B with K, then we obtain the following equation, which is more appropriate for our discussion.

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}}M^{2L+1}(K-1)^2 \tag{A.3}$$

Furthermore, if we call;

$$DR_0 = \frac{3}{2}\frac{2L+1}{\pi^{2L}}M^{2L+1} \tag{A.4}$$

then equation A.3 becomes

$$DR = DR_0 x(K-1)^2 \tag{A.5}$$

By increasing the upsampling ratio and the order of the FIR filter, we are effectively creating more bits to feed back. This means we are increasing B in equation A.5 and increasing the dynamic range. This benefit comes without increasing the quantizer area. However, as the number of feedback bits increase, the DAC in the feedback will now grow in size. Also, the DAC non-linearity problem inherent to multibit $\Sigma\Delta$ modulators will become worse.

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Vita

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