THIN-FILM TRENCH CAPACITORS FOR SILICON AND ORGANIC PACKAGES

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THIN-FILM TRENCH CAPACITORS FOR SILICON AND ORGANIC PACKAGES

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Dedicated to my family

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SUMMARY

The continuous trend towards mega-functional, high-performance and ultra-miniaturized system has been driving the need for advances in novel materials with superior properties leading to thin components, high-density interconnect substrates and interconnections. Power supply and management is becoming a critical bottleneck for the advances in such mega-functional systems because power components do not scale down with the rest of the system resulting in bulky and stand-alone power modules. Amongst the power components, thin film capacitors are considered the most challenging to integrate because of several manufacturability concerns. The challenges are related to process compatibility of high permittivity dielectrics with substrates and high surface area electrodes, yield, leakage and losses. This thesis focuses on novel thin film capacitor technologies that address some of these critical challenges.

Three classes of high-density capacitor technologies are most prevalent in today's power supply modules - Multi-layered Ceramic Capacitor (MLCC), tantalum capacitors and silicon trench capacitors. For emerging thin capacitor needs, even though MLCCs can be thinned down to below 100 μm, they do not provide adequate surface enhancement. Furthermore, achieving higher volumetric efficiency requires thinner dielectrics that usually lead to several challenges related to voids, delamination, firing cracks and thermal cracks. Tantalum capacitors, on the other hand, suffer from high Equivalent Series Resistance (ESR). They are manufactured as sintered particle compacts, which are bulky and cannot be embedded due to their form factor. The emerging silicon trench Integrated Passive Devices (IPDs) are finding limited acceptance because of the high-cost tools for forming conformal dielectrics and mechanical reliability concerns for very high aspect ratio silicon structure. Existing tools and processes are confined to lower permittivity materials which also limits the capacitance density of trench capacitors. Integrated thin film capacitors in

silicon and organic packages are facing several fundamental challenges because of limited capacitance density, substrate process compatibility and yield. Ceramic thin films do not provide more than 3 - 4μF/cm^2 while typical power supply applications require capacitance densities of 10 - 100μF/cm^2.

In this research, two strategies were explored to address the current limitations of package-integrated thin film capacitors and silicon-based IPDs. In the first part of the thesis, high permittivity ceramic thin films were conformally coated on TSV structures using low-cost vacuum infiltration of sol-gel precursor solutions. This novel approach can overcome the cost and through-put limitations of CVD and ALD-deposited dielectrics. An all-solution based capacitor technology consisting of sol-gel conducting oxide electrode and sol-gel high permittivity dielectric was demonstrated to realize the solution-coated trench capacitors. The approach enables high capacitance density by a combination of high permittivity of anti-ferroelectric thin films and high aspect ratio TSV electrode structures for surface enhancement. A planar capacitance of around 2μF/cm^2 at 7V was demonstrated with anti-ferroelectric thin films. A conformal coating of Lanthanum Nickel Oxide was demonstrated on TSV structure with an aspect ratio of 5 as a proof-of-concept for sol-gel vacuum infiltration technique.

The second part of this thesis focuses on organic package-integrated thin film capacitors using etched aluminum foils. The foils provide an estimated 100X enhancement in surface area resulting in dramatic enhancements in capacitance densities compared to thin film capacitors. Solid state aluminum electrolytic capacitors are made up of conducting polymer top electrodes to provide conformality and self-healing. Two alternate top electrode approaches were studied in this work. Using ALD TiN, capacitance densities of 9 - 10μF/cm^2 were demonstrated at 100 kHz frequencies, corresponding to an area enhancement of 20X. Electroless palladium metallization was pursued as an alternate low-cost approach for conformal metallization. Patterning of the palladium electrodes was developed using a lift-off

process with electroless process compatible dry film photoresists. A significant improvement in frequency stability was observed for this low ESR top electrode compared to the conducting polymer electrodes. However, the conformality of this technique requires further improvements.

CHAPTER 1

INTRODUCTION

This chapter lays the background for emerging high-performance, multifunctional and miniaturized systems where thin film system components play an important role. A brief history of system evolution is given, followed by a description of the system integration and miniaturization trend enabled by the second law of electronic system, a.k.a. system-on-package concept. Key technologies of SOP are discussed in detail. High-density thin film capacitors are then introduced as a grand challenge for emerging high-performance systems, and current solutions to address this are briefly described. The proposed research for addressing this challenge and its broad impact are then presented to conclude the chapter.

1.1 Future trends on electronic and bio-electronic systems

"Today, your phone has more computing power than all of NASA back in 1969 and they launched a man to the moon. Now, we launch birds into pigs." This is popularly quoted on Tweeter and Facebook. No verification is needed for people to understand that today's portable devices have no problem outdoing personal computers from 10 years ago. Portable devices today have much more functions and computing power than they used to be. For example, iPhone 4, a big hit in the smart-phone market, is used to take pictures, record lectures, make schedules, run programs, watch movies and TV series, play games, video chat with family and friends, etc. Electronic systems are not only providing more functions, they are becoming smaller in size. Radios used to be larger than fax machines, now they can be made as small as an ear bud. Without performance advances in system components, integration and miniaturization, none of this would be possible.

Decades of advances in systems packaging have shrunk the size as well as improved

the performance of systems down from huge workstations that take up rooms to smart-phones in our pockets, and even smart watches on our wrists. As shown in Figure 1. 1 **Transformation of electronic systems** [1] [1], bulky systems of discrete components gradually transformed into small integrated micro-systems over the last few decades, which are now moving towards nano-systems. Miniaturization allows multifunctional integration while lowering the power requirements and also enhances the system performance. Miniaturization also helps to improve the through-put, reduce cost and also enhance system reliability. Future trends for electronics and bio-electronics require even more functionality, portability, higher performance and lower cost. This can be realized with novel nano-materials having enhanced properties and processability, resulting in improved system performance and miniaturization.

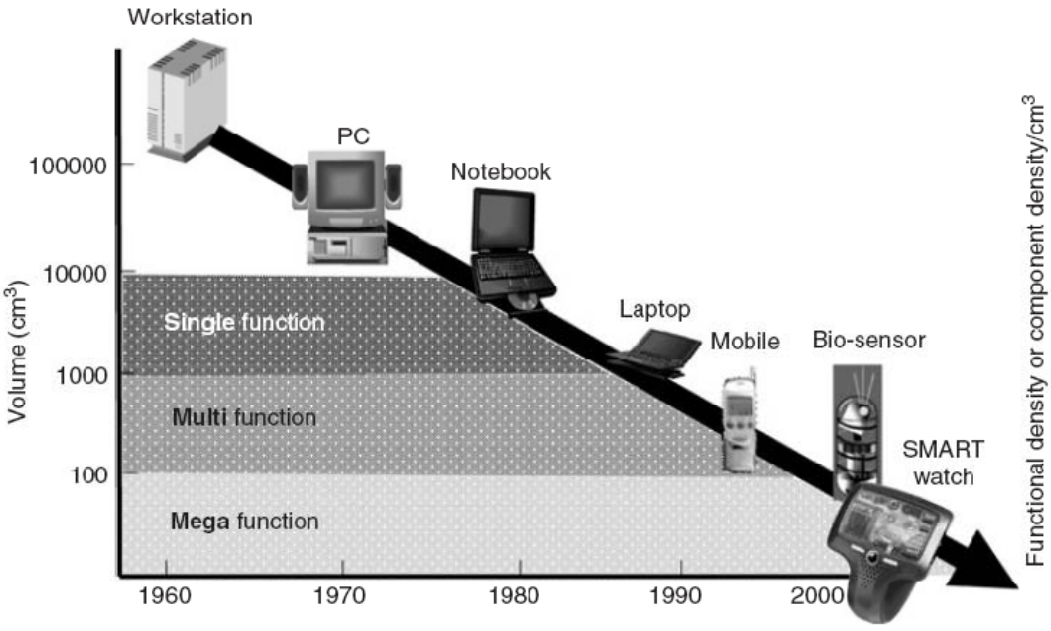


Figure 1. 1 Transformation of electronic systems [1]

1.2 Key technologies for system miniaturization

The evolution of system technologies and its impact on system performance and miniaturization can be broadly described in terms of four technologies, System-on-Board, System-on-Chip, System-in-Package and System-on-Package.

System-on-Board (SOB) technology is based on discrete bulky system components such as Integrated Circuit (IC) packages, discrete components, connectors, cables, batteries etc. that are manufactured separately and assembled onto a system board. Though the progress at IC level has been phenomenal from 2500 nm technology in 1970s to 32 nm and beyond, resulting in a billion-transistor IC, the packages and system boards that package these and other devices and components, however, are almost a billion times bigger in lithographic round rules than the ICs they package. The next wave in miniaturization included IC packages, from DIP to QFP to BGA and to CSP as well as the chip assembly from wire-bond to flip-chip. Miniaturization of such system components as discrete components, SMT interconnections, package and board wiring dimensions has also been pursued. However, most, if not all, of these technologies are incremental. Therefore, the miniaturization achieved with SOB is very limited. Several key technologies emerged along the history of system miniaturization, such as System-on-Chip (SOC), Multichip Module (MCM), Stacked ICs and Packages (SIP) and System on Package (SOP).

SOC technology involves integration of multiple system functions onto a single chip. By integrating active circuits that serves different functions into a single IC chip, system miniaturization with much enhanced performance and lower power requirements can be achieved. However, this kind of miniaturization can only go to a certain extent. Integration of more active functions on an IC implies increased cost, design complexity and decreased yield and reliability. Moreover, SOC addresses integration at device level rather than system level, which is only a small part of the problem [2].

Multichip Modules (MCM) emerged to solve the problem of yield for SOC technology. Since larger chips cannot produce a satisfying yield, chips are fabricated and then integrated onto a module. However, MCM technologies allow only two-dimensional integration, still doesn’t provide enough miniaturization and

performance enhancement because of the large interconnect lengths.

3D enables a more effective and cost-efficient system integration. As a result of increasing need for miniaturization, researchers began to explore the possibility of miniaturization in 3D where ICs and packages are stacked together. Stacked ICs and packages (SIP) technology involve the stacking of ICs and packages using wire bond, flip chip or TSV. They are either stacked packages using wire-bond, tape automated bond or flip-chip process, or stacked ICs enabled by TSVs [1]. For wire-bond SIP, dies are stacked and interconnected by a common interposer or package. Wire-bond SIP suffers from parasitic coming from the long wires. Flip-chip SIP consists of bare dies connected to one another with flip-chip bonds. A significant jump in 3D miniaturization is now realized by thin active components, through-silicon-vias (TSV) and thin film assembly bonding technologies, replacing flip-chip and wire-bond

Moore's law very well predicted the advances in IC industry that the number of transistors in an integrated circuit doubles approximately every couple of years [3]. However, a system consists of much more than just active components, such as batteries, passive components, interconnects, interposers, thermal structures, sensors, MEMS, etc. True system integration and miniaturization happens not just at IC level, but at the system level by miniaturizing all the system components with novel nano-materials and nanostructures with enhanced properties, and interconnecting them. This forms the basis for the concept of System on Package (SOP) technology introduced by Professor Rao R. Tummala at Packaging Research Center of Georgia Institute of Technology in 1994. As shown in Figure 1. 2 [1], if the system components were to be miniaturized to micrometer-scale and eventually nanometer-scale, SOP technology should lead to the second law of electronics [4]. Thus, with the inclusion of all other system components instead of just IC chip or active components, SOP is a complement of Moore's Law on system level.

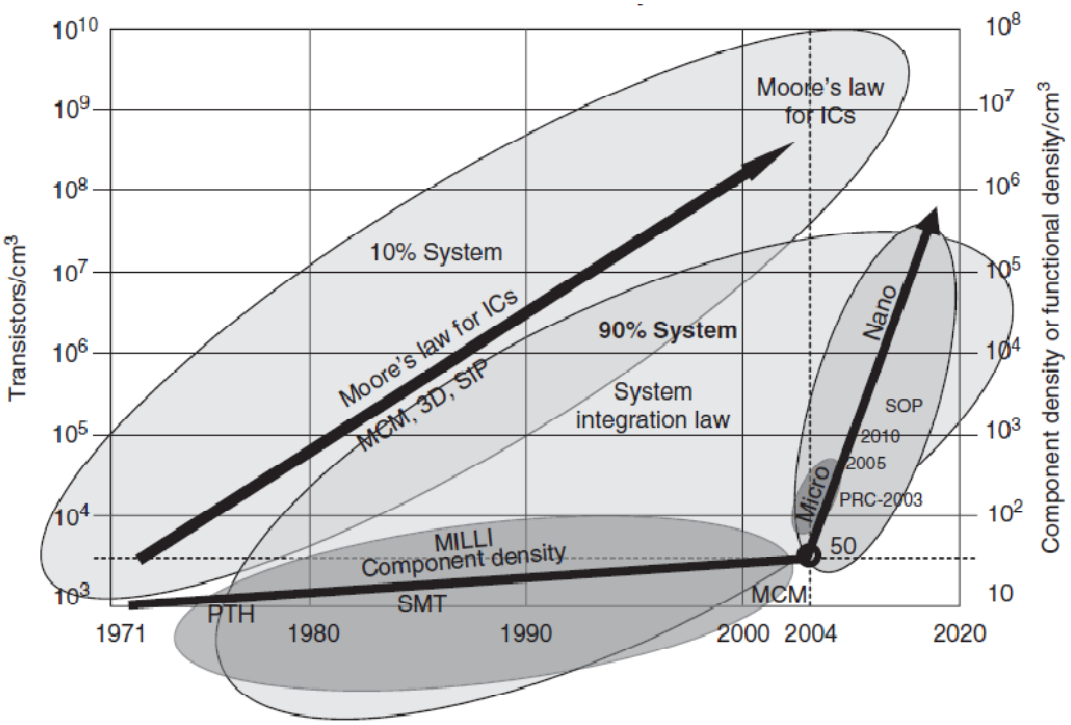


Figure 1. 2 Second law of electronics introduced by SOP [1]

1.3 SOP Paradigm

In the SOP technology, a system package is the combination of IC, package and system [1]. It addresses the integration and miniaturization of the entire system, rather than just at IC level. Unlike SIP technology, which is merely the stacking of ICs and packages, SOP integrates all the system components including active and passive components, interconnections, thermal structures, power sources, etc. One single module provides all the system functions. A well-developed SOP system is shown in cross-section view in Figure 1. 3.

SOP technology combines SOC, SIP technologies and miniaturization of different components to bring the integration to a system level. With high-degree miniaturization of components and ultra-fine pitch and high-density interconnects, one package can act as an entire system with the integration of different modules [[1], [2], [5]] such as RF, optical, thermal, bio, MEMS, etc. The SOP system consists of three inseparable parts, which are substrates, interconnects and functional modules. These are described below.

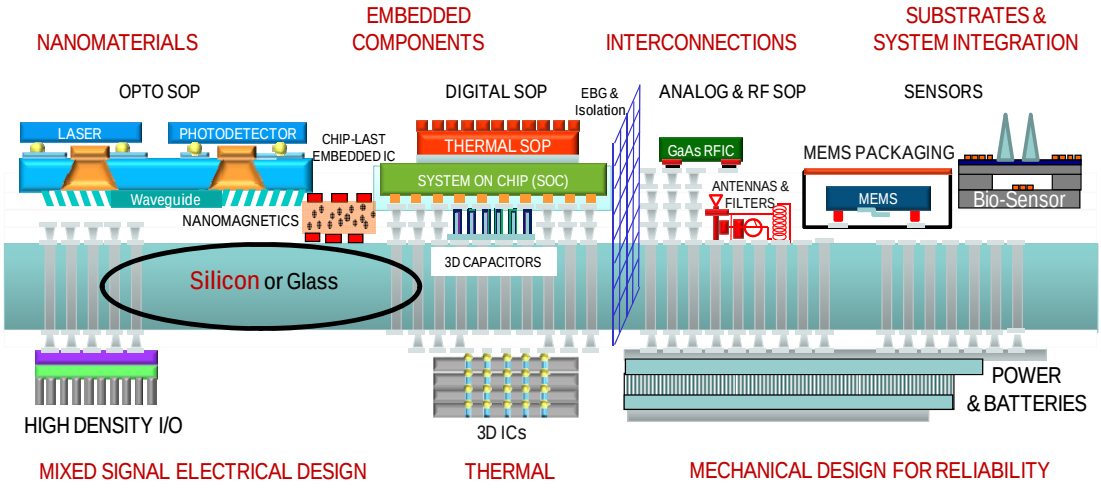


Figure 1. 3 A cross-section view of an SOP system (Courtesy: Packaging Research Center in Georgia Tech)

Substrate:

An ideal substrate material should have good electrical insulation, high thermal conductivity, Young's modulus, low coefficient of thermal expansion (CTE) and good processability. Good electrical insulation in the substrate promises signal integrity with thin and fine line wiring. On the other hand, semiconducting substrates need to be separated from the transmission lines using thick dielectric liners. For highly miniaturized system, thermal dissipation could be a big challenge. Combination of high thermal conductivity for the substrate core material, thin and high-conductivity thermal interface materials (TIMs) and new thermal dissipation structures will mitigate the thermal dissipation issues. High stiffness and Young's modulus ensure low warpage. Low CTE results in little CTE mismatch with silicon, hence improved reliability. Easy and low cost processing for interconnections, TPVs, and embedded component are also required. Currently three types of substrate core materials are prevalent. They are:

Organic Substrates:

The advantages of using organic substrate are: (1) Large area and relatively easy processability. (2) Low cost. (3) Potential application in system that require flexible

substrates. However, they face challenges such as poor heat dissipation, large CTE mismatch with silicon and difficulties in fine-pitch processing.

Silicon substrates:

Silicon substrates are much better for fine pitch processing and in dimensional stability compared to traditional organic substrates, they provides virtually no CTE mismatch, good heat dissipation and compatibility with existing processing technologies. However, silicon being a semiconductor requires thick package liner. Further, silicon processing is limited to 300 mm fabrication. A large-area polysilicon interposer approach was recently explored in Packaging Research Center of Georgia Institute of Technology [6]. The panel-based polysilicon approach guarantees lower cost and high throughput, and thinner processing even without chemical-mechanical polishing.

Glass:

Glass is an excellent insulator, thus no package liner or related process is needed. It has low CTE mismatch with silicon, good compatibility with fine-pitch processing and large panel availability. Its good performance as substrate core material has attracted much attention. The only two problems with glass as a substrate core material are its low thermal conductivity and difficulty in forming through-glass-vias (TGVs). V. Sukumaran et al. [7] demonstrated high throughput TGVs with fine I/O pitches of 30 μm formed using a parallel laser process. Combining with new copper via thermal structures, glass substrates show great potential in future applications.

Interconnections:

Components need to be arranged and interconnected before a device can function as a whole system. Interconnections in SOP system should have low resistance and inductance, high current carrying capability, small size and good reliability. There are mainly three types of interconnections: TSV, flip-chip and wire bond. Wire bond has high reliability, yield and flexibility of process, yet it introduces long interconnection

lengths degrading electrical performance and requires larger real estate. Flip-chip has much better electrical, thermal performance, higher volumetric efficiency and lower cost in high-volume manufacturing.

Tin-based solders are most commonly used for device, package and board-level interconnections. Tin-lead alloys provide low melting point, good electrical conductivity and reasonable shear strengths. As a result of environmental protection trend, lead-free solders were developed to replace Sn-Pb alloys. However, with the trend towards fine pitch, lead-free alloys pose several challenges with respect to interconnect electromigration and thermo-mechanical reliability. Alternative interconnection schemes based on direct Cu-Cu bonding are emerging to address these challenges.

Active and Passive Components:

Various components serve as a part of the system. Each one of them has its own particular function. Majority of the system components are classified into active and passive components. Components that consume external energy to perform are classified as active components. Passive components do not require external energy. They perform functions such as filtering, coupling, decoupling, bypassing, resonating, etc. The embedding of both active and passive components not only leads to small form factors, but also reduces parasitic by bring actives and passives closer together, which results in a miniaturized system with better electrical performance.

Embedded active components:

Active ICs are embedded in the package using three different processes:

(1) Chip-first approach: In a chip-first process, the embedding usually starts with IC. Buildup of wiring begins on top of the IC. This process has small form factor and good electrical performance; it faces challenges such as relatively low yield due to continual build-up process, known-good-die issue, fatigue due to thermal stress,

and thermal management since the chip stays within the substrate.

(2) Chip-middle approach: In this approach, the chip faces down onto a build-up layer and is completely embedded in the subsequent build-up materials, thus stays in the middle of the buildup layers. This process has better yield and fatigue properties. However, thermal management and known-good-die issues still exist.

(3) Chip-last approach: As is given by the name, the chip is embedded into the build-up material after all processes for the substrate are finished. In this approach, there is no known-good die issue, yield is relatively high, and thermal management is no longer a problem since the chip can be attached to a heat sink from the exposed back-side.

Passive components:

Passive components include resistors, capacitors, inductors, most sorts of diodes, etc. They dominate the system volume because they outnumber active components 10 to 1. Furthermore, many of the passive components are manufactured separately and then surface mounted on board as bulky discrete components. Thin film passive components with advanced nano-materials can improve the components properties, reduce the size and lead to better electrical performance due to shorter interconnection. These thin film components can be integrated on chip, mounted as thin Integrated Passive Devices (IPDs) or embedded into the package. Thin film components for power supply, with capacitor as a specific example, will be further discussed in the next section.

Thermal structures:

The most critical bottleneck for ultra-miniaturized and mega-functional systems is the thermal dissipation. Existing cooling techniques are not sufficient to meet the requirements for heat dissipation of these systems. Novel methods for solving thermal problems are being developed and proposed.

The most effective way of heat removal in 3D ICs is by incorporating fluidic micro-channels [8] in silicon. This method avoids thermal contact resistance by introducing built-in structures to remove heat from heat-generating substrates directly. Micro-channel cooling using integrated heat sink is a promising approach to meet the thermal management requirements of future high performance MPU since water has a much higher heat capacity than air [9]. In addition, integrating heat sink into the processors allows to cool each chip individually and also to help reduce the form factor.

Another emerging thermal management solution is active cooling, which is usually in the form of solid state thermoelectric coolers (TECs). The principle of thermoelectric cooling is to use the Peltier effect to create a heat flux between the junction of a metal and a semiconductor. The advantage of this approach is that the cooling rate is controlled at will. The reversion of this principle, which is called Seebeck effect, converts heat flux to electrical power. This approach not only solves the heat dissipation issue, but also proves to be a viable option as an alternative power source. A considerable amount of research is carried out to improve the efficiency of such construction [10].

Apart from heat sink, the thermal interface material (TIM) is also an important part of the thermal structure. TIMs are used to improve thermal contact on the interfaces, replacing what was originally 99% air gap. Typical TIMs include solders and composite materials with polymer or silicone as the matrix and ceramic and metal as fillers. With the emergence of nano-technology, CNTs prove to be a strong candidate for future TIMs, once the issue with reported high interfacial thermal resistance [11] gets resolved.

Sensors and transducers:

Sensors and actuators are probably the most important way for electronic devices to

interact with the environment. By sensing the ambience, information and data are gathered and processed by ICs so further functioning could be carried on. Sensors are widely used in electronic devices, from sensing Bluetooth signal to health monitoring in bio applications. Transducers transform a certain kind of energy to another; each kind of transducer has its own way to interact with the environment. A simple and clear example for sensors and transducers could be found in the iPhone. When touched on one of the buttons on the screen, sensors integrated under the screen detect the pressure change and send an electrical signal out to the IC. After processed by the IC, a click sound (which would be a form of mechanical vibration) is created in the speaker, along with a change in display and execution of application. Microelectromechanical system (MEMS) technology (or maybe in the future nano-scale MEMS or NEMS) has opened the gate for miniaturized and low-cost sensors and transducers in electronic devices. By using existing semiconductor fabrication technology, highly miniaturized devices can be fabricated with high through-put and yield. These devices may function as motion detectors, sensors, transducers and even RF components.

1.4 Need for high density capacitors

As different devices work at different voltages to serve various functions, power convertor modules are needed for stepping up or down voltages and currents supplied by a single power source such as a battery. In a typical power-supply module, capacitors and inductors together with the active network form a voltage convertor. In these applications, capacitors serve important roles such as charge storage for providing output power to active devices, energy storage for voltage conversion, decoupling or more broadly, noise filtering, etc.

Decoupling is perhaps the most important application of power supply capacitors in high-speed digital systems. The switching of active devices creates a big change in current supplied by the power source. This change induces noise in the power rail because of electrical parasitics. As the noise is distributed along the power supply

lines, decoupling capacitors of various capacitance are required along the power network to provide localized noise-free source of DC power for active devices, thus reduce the propagation of the noise [12] induced from the package and board. It is desired that these decoupling capacitors be placed as close to active devices as possible for suppressing noise at high frequencies.

High capacitance density is required to meet the power supply and noise suppression needs as well as accommodating for the ever-shrinking size of the package. Long term strategic needs for this kind of capacitors are: capacitance densities of over 40μF/cm^2, operation voltage of above 10 volts, 60 - 100 microns in thickness and leakage current of less than 0.1μA/μF, with an emphasis on low cost.

The sizes of active devices are quickly moving towards nano-scale, thanks to the rapid advances in IC technology. Decoupling capacitors, however, are still at the edge of micro-scale. As they are preferred to be placed close to active devices, passive components remain to be a bottleneck for system miniaturization.

Multi-layered Ceramic Capacitor (MLCC), tantalum capacitors and silicon trench capacitors are the three most prevalent technologies for today's power supply modules. MLCCs do not provide adequate surface enhancement, hence not high enough capacitance density. Tantalum capacitors are manufactured as sintered particle compacts, which exceed the thickness requirement for thin film capacitors. The emerging silicon trench Integrated Passive Devices (IPDs) involve high-cost tools for forming conformal dielectrics. Existing integrated thin film capacitors in silicon and organic packages are facing several fundamental challenges because of limited capacitance density, substrate process compatibility and yield.

Thin film capacitor components can be addressed with two approaches: 1) Integrated Passive Devices (IPDs) and 2) Thin film capacitors built and integrated as a part of the package. IPDs provide several advantages such as high yield, pre-testability and

reparability coupled with ultrahigh densities because of minimal integration constraints. Thin film capacitors in the organic packages, on the other hand, provide the best performance but are usually plagued with yield, reparability and manufacturability issues. This thesis focuses on addressing the fundamental barriers in two approaches - silicon IPDs and embedded thin film capacitors. IPD capacitor and thin film embedded capacitor are shown in Figure 1. 4, in comparison with traditional capacitor technologies.

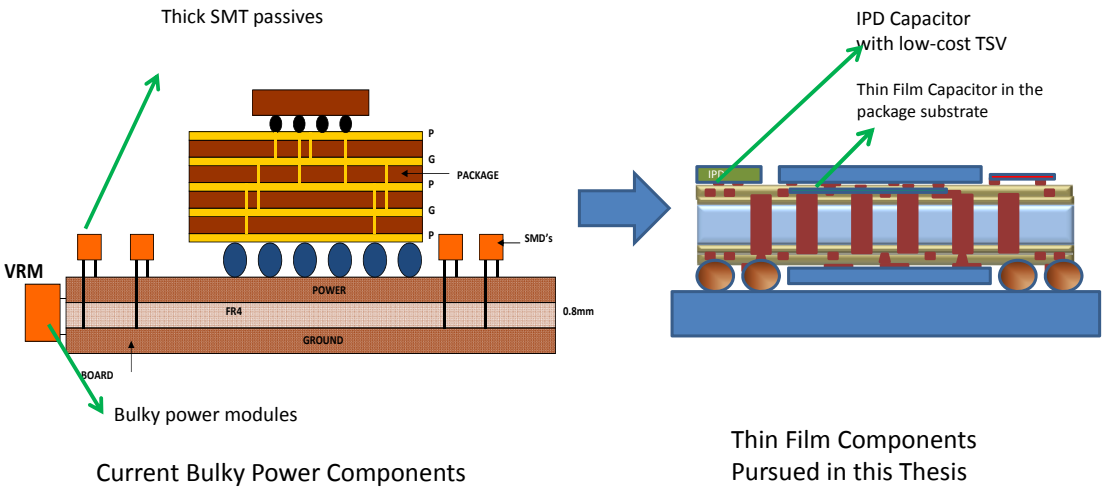


Figure 1. 4 Two thin-film capacitor technologies explored in this thesis

The main challenges with silicon trench capacitors are: 1) inability to form conformal high k dielectrics at low cost and 2) limitations of ferroelectrics in achieving high capacitance densities at operating voltages. This thesis addressed these two challenges with two approaches. A novel anti-ferroelectric dielectric is pursued to demonstrate higher capacitance density under DC bias conditions. A low-cost sol-gel derived conformal coating technique by vacuum infiltration is pursued to overcome the cost and through-put challenges with existing technologies. From these two innovations, an all-solution based thin film capacitor with sol-gel derived conducting oxide electrode and anti-ferroelectric dielectric is demonstrated.

For embedded passive components, current approaches based on thin film capacitors

provide insufficient capacitance. High-density capacitors that are manufactured as discrete components and buried in the package pose many challenges such as thickness, pick-and-place costs amongst others. A novel high-surface-area etched-aluminum-foil approach is demonstrated for thin film capacitor integration in substrate core or build-up layers. Etched foils are anodized and filled with a conformal counter electrode to form a thin capacitor (<100 micron). The capacitance density, leakage and frequency dependence with the new approach are discussed in chapter 4 of the thesis.

The two approaches pursued in this research represent significant breakthroughs in both thin IPDs and thin film capacitors by addressing the cost, thickness and capacitance density limitations of today's approaches.

CHAPTER 2

BACKGROUND

This chapter describes the basics of a capacitor and its properties. Various classes of capacitor technologies are then described followed by details of ferroelectric and anti-ferroelectric thin film materials and processes. Details of aluminum electrolytic capacitor technologies and its critical challenges are presented. Various challenges in the key silicon trench and aluminum electrolytic capacitor technologies are identified.

2.1 Capacitors

Capacitors are made of two electrodes separated by a layer of dielectric. The dielectric material is an insulator that limits the leakage current. When an electric field is applied to the dielectric, dipoles will be generated in the dielectric, resulting in charge accumulation and pile-up at the interfaces.

2.1.1 Properties of capacitors

Capacitance:

When two electrodes of a capacitor possess charge in the amount of q and –q respectively, the ratio between the charge q and potential difference across the capacitor is defined as the capacitance of the capacitor:

$$C = \frac{q}{U_+ - U_-}$$

Tolerance:

Capacitors cannot be repeatedly fabricated with exactly the same amount of capacitance because of material and process limitations. The deviation from the designed value arises because of non-uniformity in thickness, material composition, electrode geometries, instability in properties with temperature and frequency. The statistical deviation in the capacitance is referred to as tolerance.

Leakage:

Dielectric materials are not perfect insulators. A small current passes through dielectric whenever an electric field is applied. This current is referred to as leakage current. Temperature dramatically affects the amount of leakage current.

Dielectric loss:

Due to the leakage current, dielectric absorption, equivalent series resistance (ESR) and so forth, capacitors cannot work as ideal energy storage units, but dissipate a certain amount of power when in service. The dielectric loss refers to the percentage of all the power dissipated and is an indicator of the power efficiency in the capacitor.

Breakdown Voltage (BDV):

In a strong electric field, instead of being an insulator, the dielectric material will breakdown to become a conductor. The breakdown process damages the dielectric permanently. There are three causes for breakdown: temperature, chemical reaction and electric field. The voltage at which the dielectric breaks down is referred to as breakdown voltage. It is desired that the breakdown voltage is much higher than working voltage. As the distance between the two electrodes gets smaller, the electric field increases. Thus, thinner films are prone to electrical breakdown and this is a serious concern for thin film capacitors.

Temperature Coefficient of Capacitance (TCC):

TCC refers to the capacitance change with respect to temperature. Different applications have different requirements for this parameter. TCC can be either positive or negative for both polymer and ceramic capacitors. It is ideal for TCC to be around zero, but some materials such as ferroelectrics have high TCC and therefore suitable for applications where temperature stability is not stringent.

2.1.2 Types of capacitors

Capacitors can be categorized into several subgroups judging by the fabrication processes and material used. Electrolytic capacitors, ceramic capacitors, polymer film capacitors, silver mica capacitors, and supercapacitors are the most common types of capacitor in application.

Electrolytic capacitors:

Electrolytic capacitors are made from high-surface-area valve metals. They are anodized to form a conformal dielectric, which is in contact with an electrolyte that also acts as part of the cathode. They provide the largest capacitance amongst all high-voltage capacitors. Electrolytic capacitors used today mainly constitute of aluminum and tantalum capacitors. High surface area is achieved through etched foil, porous electrodes or sintered powder. This type of capacitor has a wide tolerance; they are mostly used for filtering rectified current and noise suppression in power supply.

Ceramic Capacitors:

Ceramic capacitors are made of metal electrodes separated by ferroelectric dielectrics. These are probably the largest family in capacitors. Their capacitance ranges from picofarads to microfarads. Ferroelectrics-based ceramic capacitors are being widely used for power supply noise decoupling in digital processors because of their extremely high permittivity and thin film processability at low cost. The development of multi-layer ceramic capacitors (MLCC) further increased the capacitance of ceramic capacitors and extended the applications of ceramic capacitors. On the other hand, glass and glass composites showed stable properties with temperature and frequency, and are hence widely used for RF components where tolerance is very critical. It is important to note that ceramic capacitors are graded into various classes, and choosing capacitor with right capacitance, tolerance, loss and TCC is crucial for the application.

Polymer film capacitors:

Polymer film capacitors have polymer dielectrics. Depending on the properties of dielectric material, they have different attributes. Polycarbonate capacitors have good stability over time or a wide temperature range, and a small dissipation factor. Polypropylene capacitors have stable capacitance with time and applied voltage. Polystyrene capacitors have good insulation and low loss. Yet, they are bulky and working temperature is up to only 70°C. They are used for filtering, high-frequency tuning, and equalizing. PTFE capacitors have low loss, frequency stability up to 200°C. PTFE capacitors are mostly used in high frequency applications. Sometimes polymer composite film combining properties of two polymer dielectric are used to suit specific requirements. Conducting fillers are added to the dielectric materials to improve dielectric constant [13].

Silver mica capacitors:

In silver mica capacitors, silver electrodes are plated directly on to mica dielectric. This type of capacitor is not used as widely as it used to be. However, it is still used in applications where high accuracy, low loss and great temperature stability is needed. Mica is very inert and chemically stable, resulting in very good stability as the dielectric. The capacitances of silver mica capacitors are in picofarads, and because of their high accuracy, and high quality factor, they are perfect for high frequency bypassing and decoupling. However, they are large in volume and thus substituted by other modern technologies.

Supercapacitors:

Supercapacitors consist of high surface area electrodes (usually carbon or conducting oxides), that are filled with electrolyte. Capacitances arise from the electric double layer formed on the interfaces of electrode and electrolyte. In recent years, supercapacitors received much attention because of their potential as an alternative power source. They are called super capacitors because of their extremely high capacitance on the scale of hundreds of farads for a single capacitor. Their advantages compared to batteries are much higher power density, longer term cycling stability,

and are environmentally friendly. Unlike most capacitors whose polarization comes from within the dielectric material, the polarization of supercapacitors comes from electrochemical double-layers at the interfaces of electrode and electrolyte. The main limitations of supercapacitors are their low energy density and drop in voltage when discharging. Currently, most of the supercapacitors work as complementary components to batteries.

2.2 Background and literature review of sol-gel TSV capacitors

The capacitance of a parallel-plate capacitor is expressed as:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

where ε_0 is the permittivity of vacuum, ε_r is the permittivity of the dielectric, A is the effective surface area of the dielectric and d is distance between two electrodes. To increase the capacitance density, one can either improve the permittivity of the material, or reduce the dielectric thickness. The critical properties for any capacitor dielectric are its dielectric constant and breakdown electric field strength, which determines the dielectric thickness so that the voltage requirements could be met. For thin film technologies, resistance to leakage current also becomes critical because of the high field strengths applied to the film. High permittivity materials have capacitance density but suffer from high leakage currents and low breakdown voltages. High permittivity also results in unstable properties with respect to frequency and temperature. Hence, selection of the dielectric material depends on process compatibility, target capacitance density, thermal and frequency stability as well as cost. The following section describes various dielectric materials and their important characteristics. Dielectrics are classified as lower k, moderate k and high k dielectrics.

2. 2. 1 Classification of dielectric materials

Lower k materials: Oxides, nitrides and oxy-nitrides with permittivity of 4 to 7 can be thinned to 30nm and still retain breakdown voltage of 20V (Figure 2. 1 [14]). The permittivity arises from a combination of electronic and ionic polarization. This kind

of material has the highest BDV of all materials, ranging from 800 to 1000 V/micron. With their intrinsic properties and state-of-the-art technology applications, such as plasma enhanced chemical vapor deposition (PECVD) and liquid phase chemical vapor deposition (LPCVD), reliability is rarely an issue. They also have good adhesion and compatible CTE with silicon. However, they display insufficient capacitance density (about 0.2 - 0.3 μF/cm^2 on planar devices) for many applications.

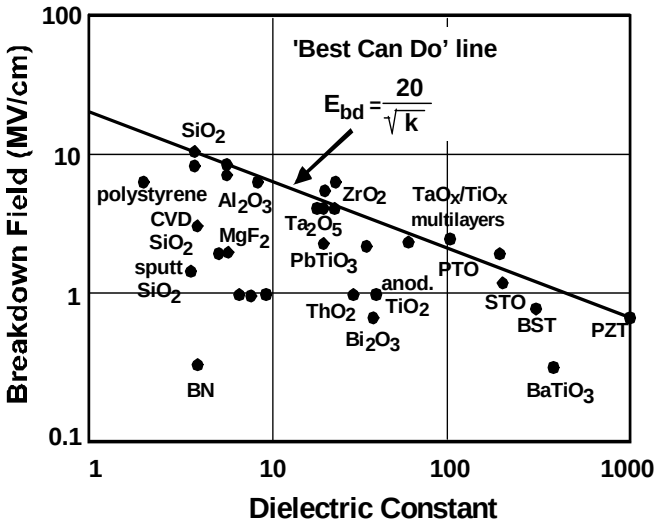


Figure 2. 1 Dielectric Constant vs. BDV of different materials [14]

Moderate k materials: Oxides with permittivity of 9 to 80 such as alumina, hafnia, zirconia and titania are classified as moderate k dielectrics. They have breakdown strength of 300 - 800 V/micron. For a 50nm thick film, capacitance density of close to 1 μF/cm^2 can be achieved. Moderate k materials show a 5 to 10 times increase in capacitance density and are mainly developed as gate dielectric for CMOS transistors in substitution of silicon dioxide. Large amount of R&D resources were invested in this area leading to relatively mature tools and processes. Most important criteria for choosing dielectrics are its k-value and band gap. Higher band gap usually leads to lower leakage currents, but compromises the permittivity of the material (Figure 2. 2 [15]). Researchers thus create compound mixtures of two or more chemicals, which not only gives high-k values, but also good electrical characteristics. Atomic layer deposition is the most common technology for depositing this kind of materials.

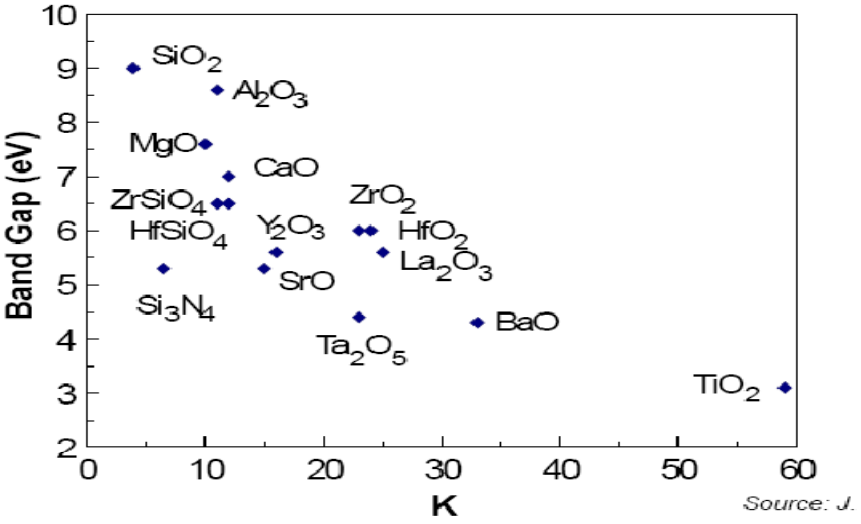


Figure 2. 2 Band gap vs. k values of different dielectrics [15]

High k materials: Ferroelectric materials show dielectric constants on the order of 1000 - 20000 in bulk form. The dielectric constant of ferroelectrics is dependent on the grain size. Most of the nano and submicron ferroelectric thin-films may not show such high dielectric constants. The dielectric constant of $BaTiO_3$ is found to be highest when the grain size is about 1 micron. For grain or crystal sizes below 100 nm, the dielectric constant is not expected to be more than a few hundred, but still it's about 20 - 100 times more than traditional paraelectric oxides. Two reasons attribute to this:

1) Decrease of tetragonality: finer grained films suppress the tetragonality of crystals, hence little or no ferroelectric polarization.
2) Depolarization arises from strain and surface interactions: The suppression of polarization leads to a permittivity of only 600-800.

The breakdown voltage of typical ferroelectric ceramics is about 50-500 V/micron. Higher dielectric constant materials show lower BDVs because of their lower band gaps. Furthermore, introduction of defects lowers the BDV to even lower values. The low BDV is a serious problem for thin high k ceramic films.

2. 2. 2 High k ferroelectric materials

Discovered in 1945 [16], barium titanate is a very important ferroelectric material because it was the first ferroelectric structure without hydrogen bonds and has more than one ferroelectric phase. It has an ABO_3 structure of perovskite $CaTiO_3$. Above the Curie temperature, it transforms to cubic phase with a loss of ferroelectricity and a drop in dielectric constant. The Curie temperature decreases with grain size and can be below room temperature for nano barium titanate [17].

Lead Zirconate Titanate is another widely investigated ferroelectric for both piezoelectric and capacitor applications. It has a Curie temperature of 490°C, at which a first-order transition from cubic paraelectric phase to tetragonal ferroelectric phase takes place upon cooling [18]. $PbZrO_3$ on the other hand, is an anti-ferroelectric material at room temperature with a Curie temperature of 230°C, where a transition from cubic paraelectric phase to orthorhombic anti-ferroelectric phase occurs [19]. PZT suffers from electromechanical fatigue with noble metal electrodes. Two alternatives for PZT, $SrBi_2Ta_2O_9$ and$Bi_4Ti_3O_{12}$, are briefly discussed.

$SrBi_2Ta_2O_9$ has many desirable properties such as fatigue-free, good retention characteristics, low switching fields and low leakage current. At room temperature it has a dielectric constant of 180 and the Curie temperature is reported to be 335°C [20].

$Bi_4Ti_3O_{12}$ is a solid lead-free candidate for FRAM application due to its small coercive field [21] and fatigue-free behavior [22]. With a Curie temperature of 675°C [23], it is a candidate for high-temperature piezoelectric devices.

Anti-ferroelectric PZT

In 1951, Kittel predicted the existence of anti-ferroelectrics [24]. In the 60s, the prediction was proved by Berlincourt et al., reporting anti-ferroelectric behavior of doped PZT [25], [26]. Anti-ferroelectric material show ferroelectricity-like properties

under certain temperature, pressure, external electric field, etc. In an anti-ferroelectric, the material consists of crystalline arrays of electric dipoles, similar to a ferroelectric, but adjacent dipoles oriented in opposite directions, resulting in no macroscopic spontaneous polarization.

For materials with unique anti-ferroelectric properties, researchers have been working on the doping of PZT. P. Gonnard [27] et al. studied doping $Pb(Zr_{0.95}Ti_{0.05})O_3$ with Fe, Cr, Cu and Sb. Pressure-temperature phase diagrams of Nb, Sr, La, Ba doped PZT were acquired by I. J. Fritz et al. Increased amount of La dopant was reported [28] to suppress the long-range order of PLZT and enlarge the anti-ferroelectric phase region. A series of research on Sn dopant by B. Jaffe and D. Berlincourt et al., showed that stable region of tetragonal anti-ferroelectric phase and acceptable range of Zr/Ti ratio are enlarged with the introduction of Sn dopant, which provide convenience for the study and alteration of anti-ferroelectric phases. Similar to La and Sn, Sr also broadens the transition phase boundary from anti-ferroelectric to ferroelectric [29].

2. 2. 3 Ferroelectric thin films

Crystallization of PZT occurs at temperatures of around 600-700°C. Noble metals are commonly used as bottom electrodes for PZT films. In addition, a proper buffer layer is needed to enable good deposition on silicon, silicon oxide or silicon nitride surfaces due to the diffusion and reactions between Pb and these materials. There is increasing evidence that certain materials with perovskite structure can grow with specific orientation on platinum-coated silicon substrates, which leads to better properties. Oriented PZT on Pt/Ti/Si substrates was previously demonstrated by Kalpat et al. [30] and others [31]. A study by Ya Shur et al. demonstrated the role of pyrolysis temperature and ramp rate with respect to textured PZT [32]. However, high k films on platinum typically results in fatigue and reliability issues because of the accumulation of oxygen vacancies at interfaces. Two strategies are used to enhance the permittivity with thickness while improving the reliability at the same time:

Replacing Pt with oxide electrodes such as Barium strontium ruthenate (BSR) is shown to result in higher k with thinner films and better reliability than Pt for BST dielectrics (Figure 2. 3) [33]. Conducting $(LaSr)CoO_3$ is reported to be a better electrode than RuO_2 [34] for BST, the inherent advantage is that lattices of LSCO and BST almost match with each other, and that LSCO enhances the phase stability of BST.

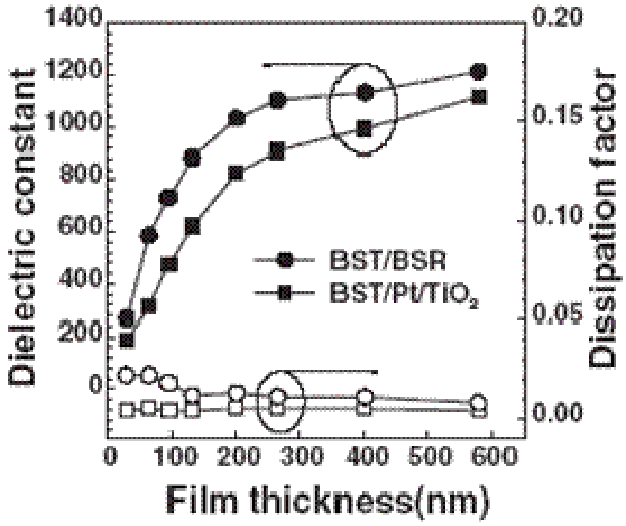


Figure 2. 3 Change in k with thickness for different electrodes [33]

Interface modification: Deposition of dielectrics on silicon usually results in interfacial traps that can degrade the leakage current reliability. Surface pre-nitridation and use of TiN as the electrode is shown to improve reliability [35].

As stated earlier, high k films show very high leakage because of their lower band gap. This problem is aggravated because of the easy formation of defects that provide extra conduction mechanism. High leakage currents in high k films are associated with oxygen or cation vacancies in the film and at the film-electrode interfaces [36], [37], [38], [39] which introduce electrons or holes in the conduction band. The oxygen vacancies are created during crystallization of the film while annealing at high

temperatures. If the high temperature sintering atmosphere is reducing or low-oxygen environment, the chances of creating oxygen vacancies increases. These oxygen vacancies are positively charged and migrate towards cathode under electrical bias and create long-term reliability issue. This contributes to increase in leakage current and degradation of electrical performance and reliability of the devices.

Limitations of traditional high k thin films are listed below:

- Lower BDV requiring thicker films that in turn lowers the capacitance density
- Thickness dependent permittivity which results in diminishing returns of capacitance density with thickness reduction
- Susceptibility to defects leading to conduction
- Intrinsic reliability issues from interfaces

These limitations need to be addressed or avoided before they are put to application.

2.3 Electrolytic capacitors

Increasing the surface area with valve metal electrodes such as Al, Ta and Nb, followed by conformal dielectric formation using anodization process, is probably the easiest way to a low-cost capacitor with volumetric efficiency. In capacitor industry, high surface area with valve metals is usually achieved by using etched aluminum foil or sintered tantalum particles. The other electrode needs to be conformal and in good contact with all the surfaces. This is readily feasible with liquid and gas electrodes. As liquid exhibits much better conductivity, they are used as the counter electrode. Dielectric for electrolytic capacitors cannot be externally deposited because accessing the high surface area through the complex electrode path makes it extremely difficult to achieve conformality. They are derived by anodization of metals such as aluminum, tantalum, niobium and titanium. Aluminum and tantalum are preferred because the corresponding oxides have good insulating property and they are easily available in high surface area architectures. Thus, electrolytic capacitors provide much higher capacitance than other kinds of thin film capacitors. It is important to note that most electrolytic capacitors in service need to operate in specific polarity. If the polarity is

reversed, cathodes tend to react with the electrolyte and cause device failure.

2.3.1 Aluminum electrolytic capacitors

Aluminum electrolytic capacitors are made up of anodized etched aluminum foils. The anode is the aluminum itself. The cathode is formed with paper soaked with electrolyte as well as another aluminum foil. These are rolled together so that an aluminum electrolytic capacitor with large capacitance is formed, as shown in Figure 2. 4.

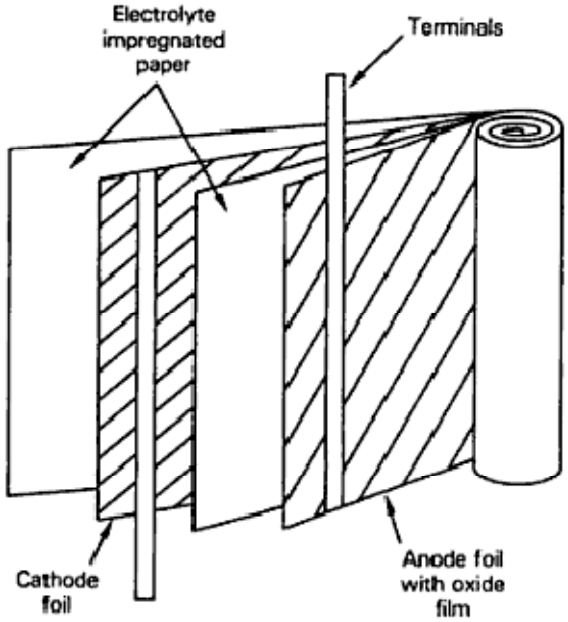


Figure 2. 4 Construction of aluminum electrolytic capacitor [40]

These traditional aluminum electrolytic capacitors served the market for many years. However, there several issues associated with this kind of capacitors. The problems mainly come from the liquid electrolyte.

The liquid electrolyte involves ion conduction, thus electrolytic capacitors with liquid electrolyte are almost impossible for higher frequency applications. Secondly, liquid electrolyte tends to remove oxide layer from the anode. Therefore, if an electrolytic capacitor has not been used for a certain period of time, it is necessary to perform a

so-called re-formation. Finally, liquid electrolyte involves evaporation and chemical reactions that produce gas, which is why these capacitors also face reliability and even safety issues. Solid electrolytes were developed to address these problems.

2.3.2 Tantalum electrolytic capacitors

Tantalum electrolytic capacitors have two kinds of structures that are very different. They can be similar to aluminum electrolytic capacitors as etched metal foils, or anodized sintered particles as porous electrode compacts. Because tantalum is less ductile than aluminum, they are more often seen in the form of sintered particles.

Tantalum particles are mixed with organic solvent, along with tantalum lead, and pressed to a desired shape. The mixture is then sintered under 2000 ℃ to form a sponge-like porous structure [41]. The resulting pellet has an extremely high surface area, and it is subjected to anodization process in phosphoric acid solution. Ta_2O_5 is formed during the anodization process. It has a permittivity of around 27, which is nearly 3 times more than aluminum oxide. After the anodization process, the cathode is introduced. A schematic of tantalum capacitor with MnO_2 top electrode is shown in Figure 2. 5. Figure 2. 6 shows the microstructure of tantalum capacitors.

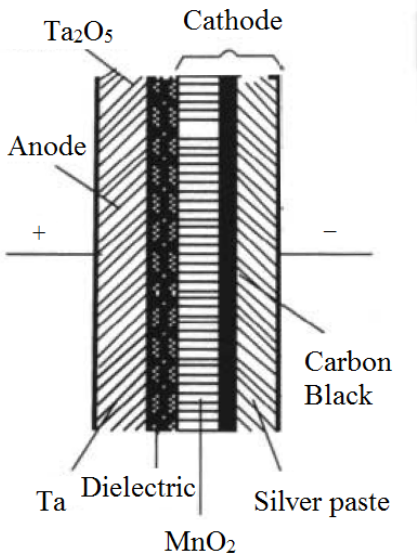


Figure 2. 5 Schematic of tantalum capacitor with MnO2 top electrode [41]

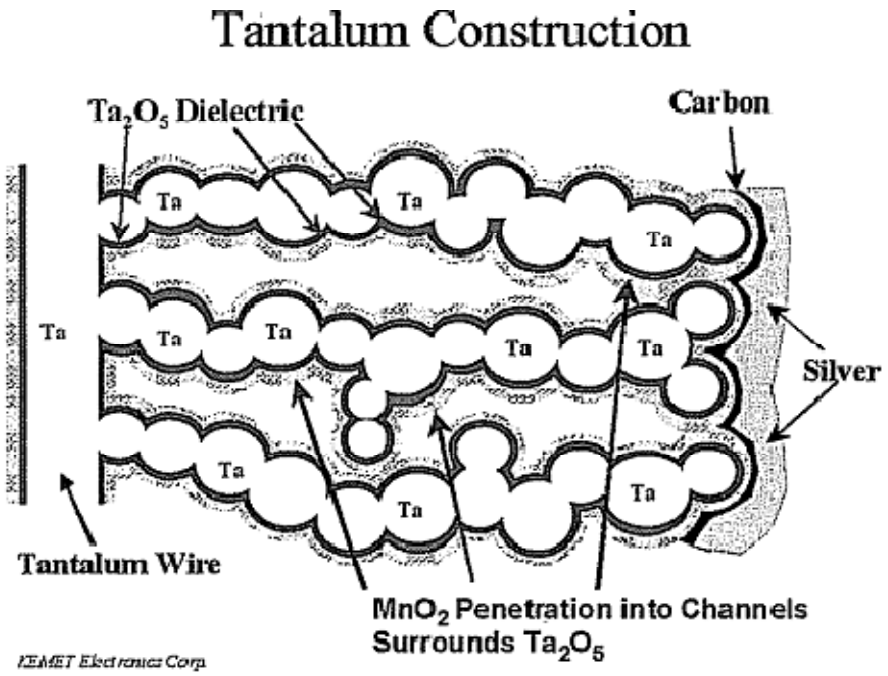


Figure 2. 6 Microstructure of tantalum capacitors [40]

2.3.3 Solid electrolytic capacitors

To resolve issues with liquid electrolyte, several kinds of solid electrolytes were developed for electrolytic capacitors. Two kinds of conducting materials are used as top electrodes for most electrolytic capacitors, conducting oxides and conducting polymers (CP).

An important concept associated with electrolytic capacitors is self-healing. An electrolytic capacitor in service or in storage usually has defects in the oxide film that increase leakage current and degrade the device reliability. Self-healing cathodes can isolate the electrode from these cracks and defects to lower the leakage current. Different electrode materials have different mechanisms. For oxide conductors such as MnO_2, increase of leakage current causes overheating, which results in decomposition of MnO_2 to form a highly insulating Mn_2O_3 and "blocks" the defect. Schematic of the self-healing mechanism for MnO_2 in tantalum capacitors is shown in Figure 2. 7.

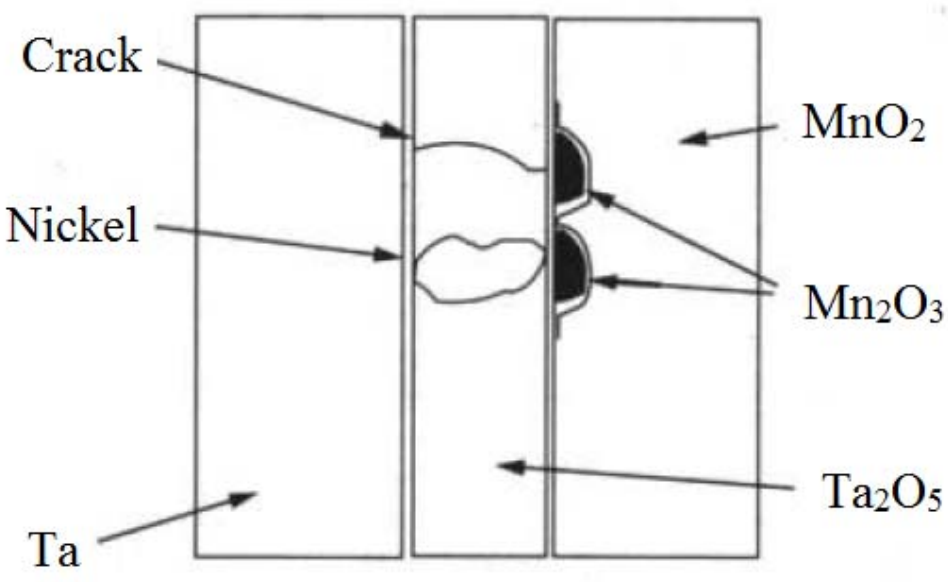


Figure 2. 7 Self-healing mechanism of MnO2 in tantalum capacitors [41]

Self-healing of conducting polymers either results from the evaporation of conducting polymers or the re-oxidation of oxide film [41]. In aluminum electrolytic capacitors, when leakage increases, liquid electrolyte generates oxygen and re-oxidizes the damaged oxide film. Aluminum solid electrolytic capacitors have similar self-healing mechanism, as shown in Figure 2. 8. In tantalum capacitors, as shown in Figure 2. 9, self-healing is rather achieved through evaporation of conducting polymers. The leakage increase result in local heating, evaporating the conductor adjacent to the corresponding spot, thus cutting off the leakage conduction.

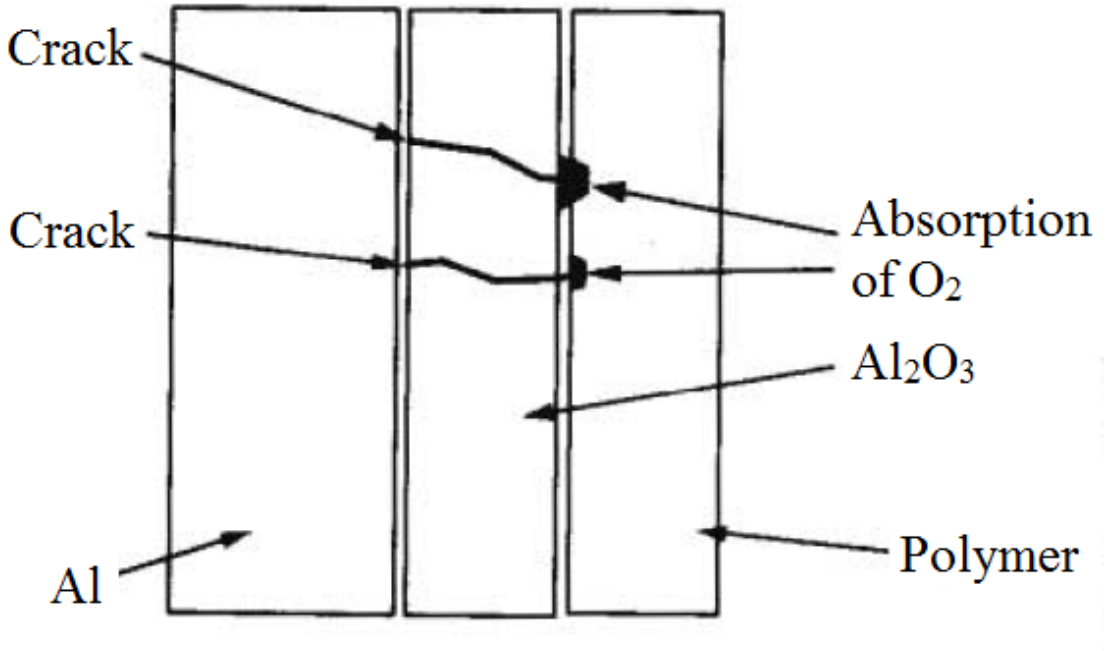


Figure 2. 8 Self-healing mechanism of CP in aluminum electrolytic capacitors [41]

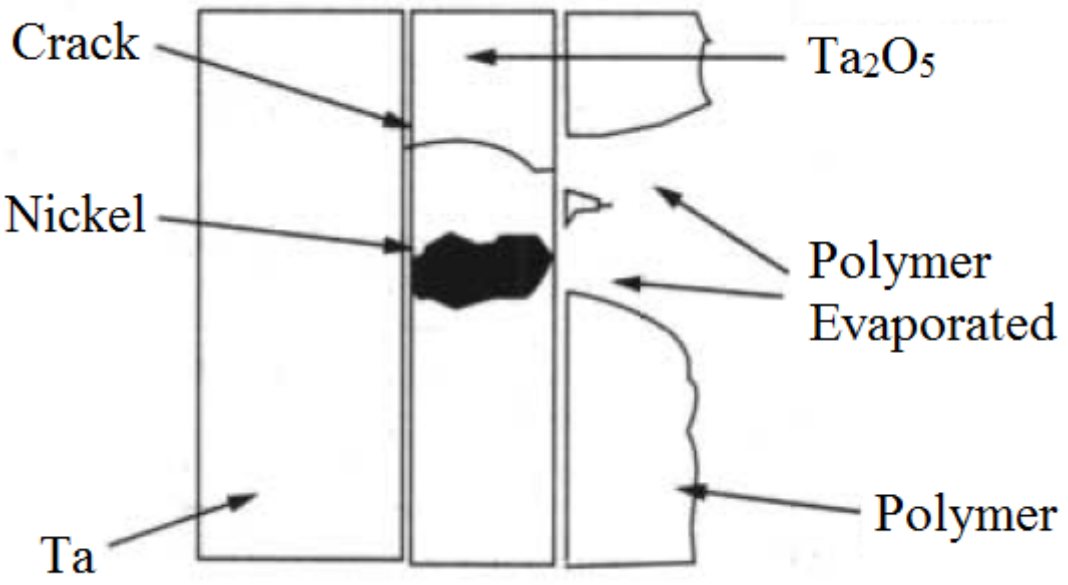


Figure 2. 9 Self-healing mechanism of CP in tantalum capacitors [41]

Electrodes in solid-state electrolytic capacitors:

a) Conducting oxide

Manganese oxide is the most commonly used conducting oxide for cathode. Liquid

manganese nitrate is added to the anodized tantalum pellet, and then subjected to high temperature in the existence of water vapor as a catalyst. The manganese nitrate then decomposes into manganese oxide and nitrogen dioxide. Liquid manganese nitrate is used instead of manganese oxide because it has very low melting point and good adsorption properties. The manganese oxide will then adsorb on all porous surfaces of the tantalum pellet and work as a part of the electrode. Carbon black and silver paste are then applied to lower ESR of manganese oxide and improve conductivity.

Problem with MnO_2 are high Equivalent Series Resistance (ESR) and possible failure of the device due to so-called "ignition failure". Higher ESR degrades the performance at higher frequencies by increasing the RC time constant. Ignition failure happens at the self-healing temperature of MnO_2, which is very close to the transition temperature of amorphous Ta_2O_5 to a conducting crystalline Ta_2O_5 [42]. Once the transition happens, it progresses from the fault site thus enlarging the defective area, and finally causes failure of devices.

b) Conducting Polymers

The top electrode should ideally have good electrical conductivity, easy processability in solution form for the effective conformal coating, and chemical inertia. Chemical inertia ensures a stable dielectric-top electrode interface and also sustains the processing temperature for subsequent integration of the capacitor. Solid-state top electrodes with conducting polymer provide a suitable combination of these properties and are developed as an alternative to oxide electrodes in order to complete the capacitor structure.

These conducting polymers bear long and repetitive carbon chains where the electrical conduction is due to the delocalization of pi-electrons over the long carbon chain. Such conduction is usually enhanced by adding dopants, usually protons (H^+) from acids. PEDT, polyaniline, polypyrrole, are examples of conducting polymers with the conduction mechanism involving delocalized electrons, favored by a proton.

Conducting polymers may be obtained as pre-polymerized dispersion (polyaniline and polypyrrol) in various solvents or as separate monomer and oxidizer components, EDT (monomer) and iron(III) tosylate (oxidizer). It is noted that the pre-polymerized dispersions are usually free of any acidic impurity or residue and therefore chemically more inert towards the dielectric. However, since pre-polymerized polymers constitute large-size particles, infiltration of these particles through deep Al channels with narrow pore size become inefficient.

On the other hand, PEDT particle size can be controlled when formed by mixing the monomer and oxidizer components in specified ratios. These polymers usually have corrosive residue and therefore show higher leakage current as compared to pre-polymerized polymer. The corrosive entities are generally removed by multiple washing and various filtration processes.

CHAPER 3

SOLUTION-DERIVED TSV CAPACITORS

3.1 Introduction

Silicon-based thin film and trench capacitors face two primary barriers towards achieve high capacitance densities:

1) Ferroelectric films do not retain high permittivity at high electric fields and are prone to high leakage.

2) Conformal dielectric formation on silicon trench is usually limited to low permittivity films and expensive tools and processes.

This chapter addresses both of these barriers by exploring anti-ferroelectric thin films with high permittivity and low leakage at high voltages, and a low-cost solution-derived conformal trench coatings to deposit them. A brief introduction of the two research barriers and the strategy to address them is described first. The experimental details, results and discussion are then provided.

Silicon-compatible thin film capacitors frequently utilize high dielectric constant (k) ferroelectrics for achieving higher capacitance densities. However, there are several factors that limit the capacitance density with high k thin films and are listed below:

- Lower BDV of 50-200 V/μm that requires thicker films for adequate reliability.
- Dependence of permittivity on particle or grain size as well as thickness.
- Susceptibility to defects that leads to conduction and hence lossy films.
- Interfacial defects or interfacial reactions that lead to a lower effective dielectric constant of the film.

From the above constraints, the maximum capacitance density obtainable from thin

films is limited to around 2 - 3 μF/cm^2 for high-voltage and low leakage current applications. As discussed in chapter 2, anti-ferroelectrics, on the other hand, show higher permittivity under DC bias conditions. Combined with high surface area from silicon trenches or trench-like structures, these anti-ferroelectric thin films dielectrics can result in high capacitance densities.

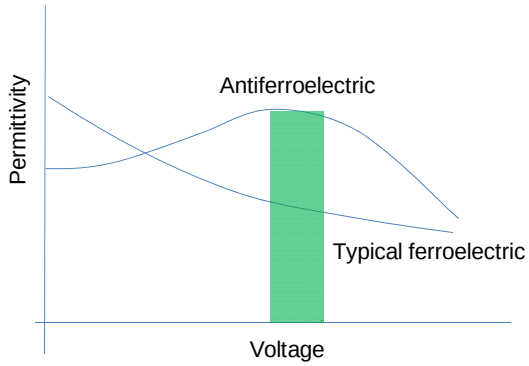


Figure 3. 1 Response of capacitance density to DC bias

Doped anti-ferroelectric thin film capacitors were explored in this chapter to demonstrate its benefits compared to traditional ferroelectric thin film capacitors. By adjusting the composition of lanthanum doped PZT, the permittivity can be enhanced at high voltages with an anti-ferroelectric transition (Figure 3. 1). Unlike traditional ferroelectric capacitors for which high permittivity is achieved at zero voltage bias and lowers with higher voltage, anti-ferroelectric films show maximum capacitance at higher voltages. The leakage currents are lowered by the incorporation of lanthanum dopants to suppress conduction caused by defects.

Conformal dielectrics on deep silicon trenches from thermal oxidation or oxy-nitridation result in lower permittivity. Film deposition from vapor deposition techniques requires expensive tools such as Atomic Layer Deposition (ALD) or Chemical Vapor Deposition (CVD) which lead to low through-put and high cost. High permittivity films cannot be conformally deposited in deep trenches using these techniques.

The second part of this chapter explores and demonstrates a novel technique to conformally coat solution-derived electrodes and dielectric films over Through-Silicon-Via (TSV) structures. In this technique, precursor solution for electrode or dielectric coatings is dispensed on the top of a TSV wafer and infiltrated through vias by creating a pressure gradient.

All experimental procedures of film synthesis as well as TSV structure fabrication are described in the next section.

3.2 Experimental procedures

This section describes the synthesis of sol-gel derived thin films, characterization of thin film capacitor, and fabrication of TSV capacitor structures.

3.2.1 Sol-gel film formation

The choice of technique for film deposition is based on a number of factors: processing temperature, cost, electrical property target, BDV, etc. A number of techniques (Figure 3. 2) may be applied for film fabrication, including high-vacuum processes such as sputtering and chemical vapor deposition (CVD). However, sol-gel process offers a much lower-cost route, as well as better control over chemical composition than sputtering and CVD techniques. Sol-gel process also has the ease of introducing dopants to adjust the dielectric properties such as loss and leakage current. It should, however, be noted that although alkoxide-based sol-gel method is a popular and widespread technique for preparing ceramic coating films in university laboratories, industry is not yet optimistic to employ this technique for mass production. Sol-gel deposition depends on reactive solutions that have shorter shelf life and also can lead to process instabilities that can cause defects. Furthermore, this technology is more labor intensive as multiple coatings are needed. However, with advances in solution stabilization techniques such as chelating agents, and Rapid Thermal Process (RTP) for fast heat processing, this thin film route has potential for

viable and cost-effective manufacturing.

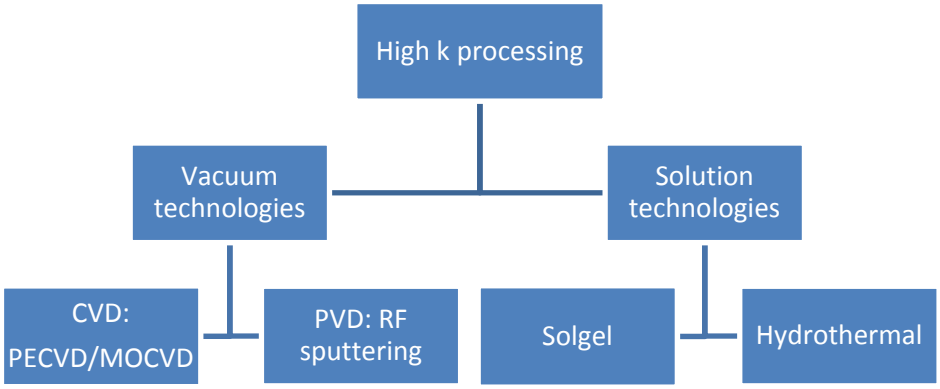


Figure 3. 2 Process technologies for high k thin film

Sol-gel based thin film formation starts with coating of a precursor solution, followed by drying of the sol forming a xerogel. The film is subsequently heat-treated to densify and crystallize, so that a ceramic thin film with required set of properties is formed. This is schematically represented in Figure 3. 3. The densification of xerogel depends on the gel structure described in terms of its pore size and pore distribution.

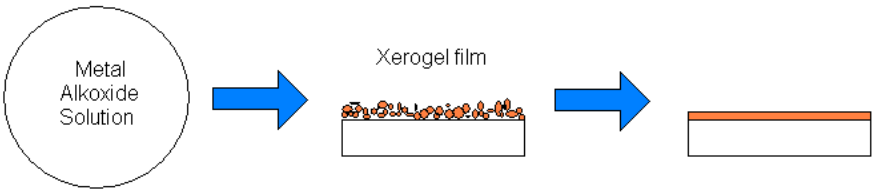


Figure 3. 3 Schematic of sol-gel film formation

Sol-gel technique was used for the synthesis of LNO and PZT because of its advantages such as lower processing cost, flexibility in controlling stoichiometry and, most importantly, its ability to form conformal coating over 3D topographies. LNO was synthesized starting with Lanthanum Nitrate Hexahydrate and Nickel Acetate

Tetrahydrate with molar ratio of one. Methoxyethanol was used as solvent for spin-coating because it wets silicon surfaces very well. The derived precursor solution was spin coated on a Si substrate and then baked on a hot plate at 400˚ C for 5 minutes. The steps were repeated three times to achieve adequate thickness, then heat treated in a tube furnace at 700˚ C for 30 minutes at a ramp of 5˚ C/min. For PZT, the starting materials were Lead Acetate Trihydrate, 70wt% Zirconium (IV) n-Propoxide in 1-propanol, and Titanium (IV) Isopropoxide. Precursor solution was made with Zr to Ti molar ratio of 13:12, and 10% lead excess, to get $Pb_{1.1}(Zr_{0.52}Ti_{0.48})O_3$. The precursors were sequentially dissolved in 2-methoxyethanol to form a 0.2 mol/L solution and refluxed at 120˚C for 2 hours. Derived precursor solution was spin coated onto the LNO film, and then heat treated at 700˚C for 1 minute using Rapid Thermal Processing (RTP). Flow chart for a representative sol-gel process is shown in Figure 3. 4. Platinum bottom electrode was used as the control sample.

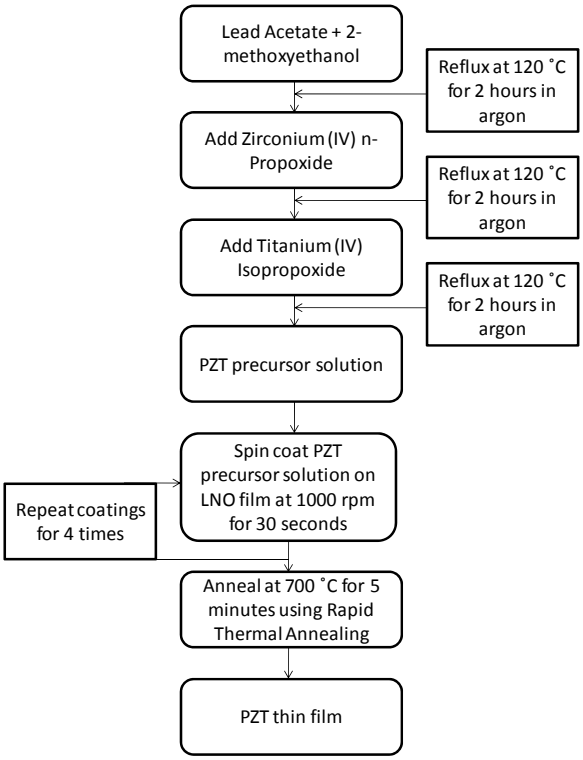


Figure 3. 4 Flow chart for the PZT sol-gel process

3.2.2 Deposition of bottom electrode by sputtering

The bottom electrode of planar capacitors is deposited with DC magnetron sputtering (CVC DC sputterer). In this technique, metal ions are bombarded off the metal target with high speed Argon ion beams, and then accelerated under an electric field to deposit onto the sample. To ensure a good deposition of bottom electrode, adhesion layer is applied. Titanium is a common adhesion layer for Platinum. It has been reported that when PZT film is deposited on Pt/Ti/SiO_2/Si, high degree diffusion of titanium through platinum and into the dielectric layer was found during heat treatment at temperatures between 300 - 700°C [40]. Thus, tantalum was used as adhesion layer and deposited directly on wafers. Platinum was then deposited on tantalum layer. The operating conditions are given as follows:

Table 3. 1 Operating conditions for sputtering of bottom electrode

Metal Target	Power	Deposition time (s)
Ta (3-inch target)	350W (7%)	50
Pt (3-inch target)	350W (7%)	500

3.2.3 Top electrode deposition by e-beam evaporation

Gold is a noble metal that has chemical stability and good electrical conductivity. It also has good wetting properties as a finish for solders. It is widely used in electronic industry. For testing the properties of thin film capacitors, gold was used as the top electrode to make stable, ohmic contact with the testing probes. In e-beam evaporation, metal crucible is heated with an e-beam source, and then evaporated onto the substrate. It requires a high vacuum to ensure a large enough mean free path of the evaporated material. Unlike sputtering, materials evaporated have smaller velocity. As a result sputtering is widely used in electronic industry instead of e-beam evaporation because it has a better step coverage. However, for direct patterning through a shadow mask, e-beam evaporation creates better edge-definition than sputtering and is preferred. A deposition rate of 2.5 Å/s is used for a layer of 200nm gold. It should be

noted that, after each process, chamber should be left idle for at least 10 minutes before venting, to ensure target metal cools down so that it will not be oxidized in air under high temperature. Devices with a diameter of 0.6 mm were formed using a shadow-mask during the e-beam evaporation.

3.2.4 Fabrication of TSV structures

Through-Silicon Vias were obtained by Deep Reactive Ion Etching (DRIE) using thick photoresist layer as the etch mask. Shipley Megadeposit SPR 200 was used as the photoresist for lithography. The photoresist is spin-coated on the wafer with a spinning speed of 3000 rpm for 10 seconds. A glass mask with chromium patterns which have holes around 100 microns in diameter was used. For a 16.5 μm photoresist layer, the energy density of the lamp was set to 50 W/cm^2. Exposure wave length was 405 nm, exposure time was set for 25 seconds.

Plasma-Therm ICP was used as the DRIE tool for the fabrication TSV structure. Bosch recipe was used for DRIE as discussed in chapter 2. Anisotropic etching of silicon is achieved by a combination of high energy on bombardment, chemical etching and polymer sidewall deposition.

Recipe for Bosch process used in this project is listed in the table below:

Table 3. 2 Recipe of Bosch process used for TSV fabrication

Step	Purpose	Pressure	Time	C_4F_8	SF_6	Ar	RF1	RF2
1	Start	0.1mTorr	2min	0 sccm	0 sccm	0 sccm	0W	0W
2	Gas Stabilization	15mTorr	30s	20 sccm	0.5 sccm	40 sccm	0W	0W
3	HDP ignition	15mTorr	10s	20 sccm	0.5 sccm	40 sccm	30W	825W
4	Deposition	15mTorr	4s	70 sccm	40 sccm	40 sccm	1W	800W

Table 3. 2 continued Recipe of Bosch process used for TSV fabrication

5	Etch A	15mTorr	2s	0.5 sccm	50 sccm	40 sccm	9W	800W
6	Etch B	15mTorr	6s	0.5 sccm	100 sccm	40 sccm	9W	800W
7	End	0.1mTorr	2min	0 sccm	0 sccm	0 sccm	0W	0W

The recipe consists of 7 steps. First step is introduced to evacuate and purge chamber and gas lines. Step 2 is for gas stabilization, which sets the stage for step 3. Step 3 is for the ignition of plasma. Plasma is a partially ionized gas which often contains dissociated molecular fragments that are extremely reactive, in this case, used for deposition and etching. Step 4 deposits a thin film of fluoro-carbon polymer on all surfaces, which is mainly used for the protection of sidewalls from being over-etched. Step 5 is the etching of polymer film deposited at the bottom of the trench, so that etching of silicon can be carried on. Step 6 is the etch step for silicon. Steps 4 to 6 are carried out in cycles, so that an anisotropic etching of silicon is achieved. The end step evacuates and purges all the harmful gas away. An anisotropic dry etching can be thus realized with an upright side wall and high aspect ratio. Schematic for the Bosch process is shown in Figure 3. 5, the result from Bosch process is shown in Figure 3. 6. It is worth noting that little structures referred to as “scallops” are formed on sidewall of the trenches. Due to the nature of the Bosch process, each cycle of etching produces a scallop structure. Attempts to smoothen the surface were made by many groups [44],[45],[46],[47].

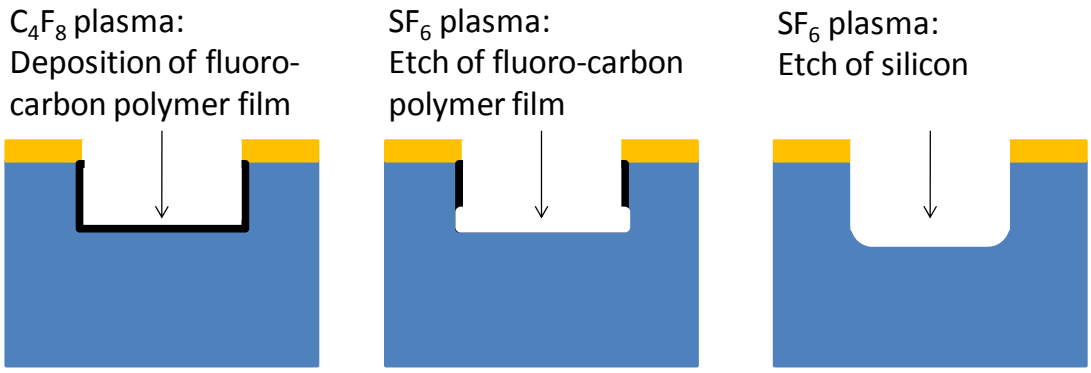


Figure 3. 5 Schematic for the Bosch process flow

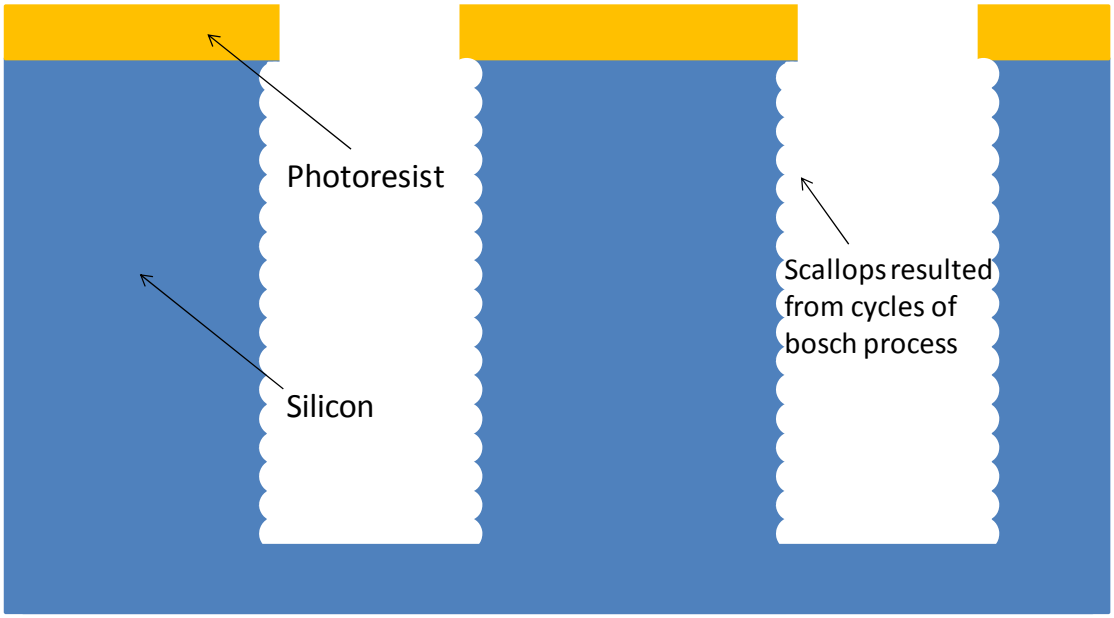


Figure 3. 6 Schematic of trench etched with Bosch process

3.2.5 Vacuum Infiltration Process

In vacuum-infiltration process, the sol-gel precursor solution was dispensed on the TSV wafers while applying a pressure gradient over the wafer, as shown in Figure 3. 7. The sample was then heat treated on a hot-plate at 400˚ C for 5 minutes. Multiple coatings were applied to increase the thickness. The sample was then annealed in air at 700˚ C for 30 minutes. The 3D structure shown in Figure 3. 8 was thus formed, enabled by vacuum-infiltration of sol-gel derived solutions. The vacuum infiltration set-up is shown in Figure 3. 9.

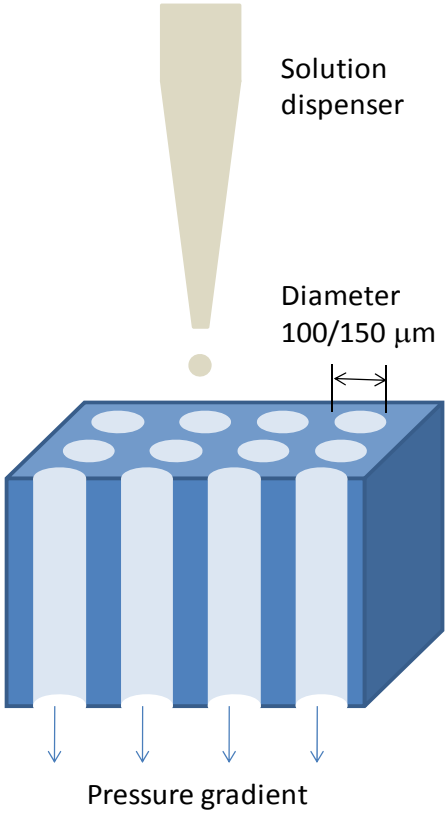


Figure 3. 7 Schematic for sol-gel infiltration process

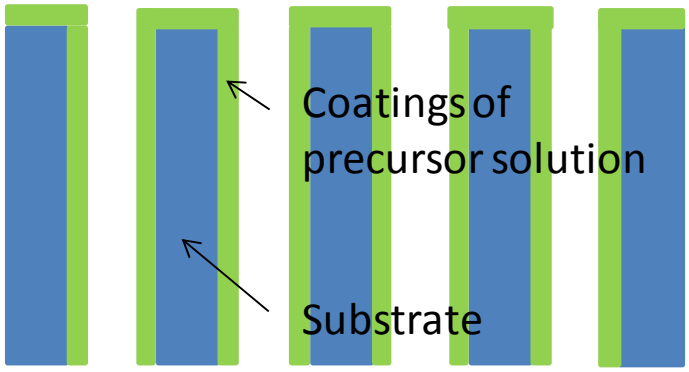


Figure 3. 8 Cross section of TSV structure after sol-gel vacuum-infiltration

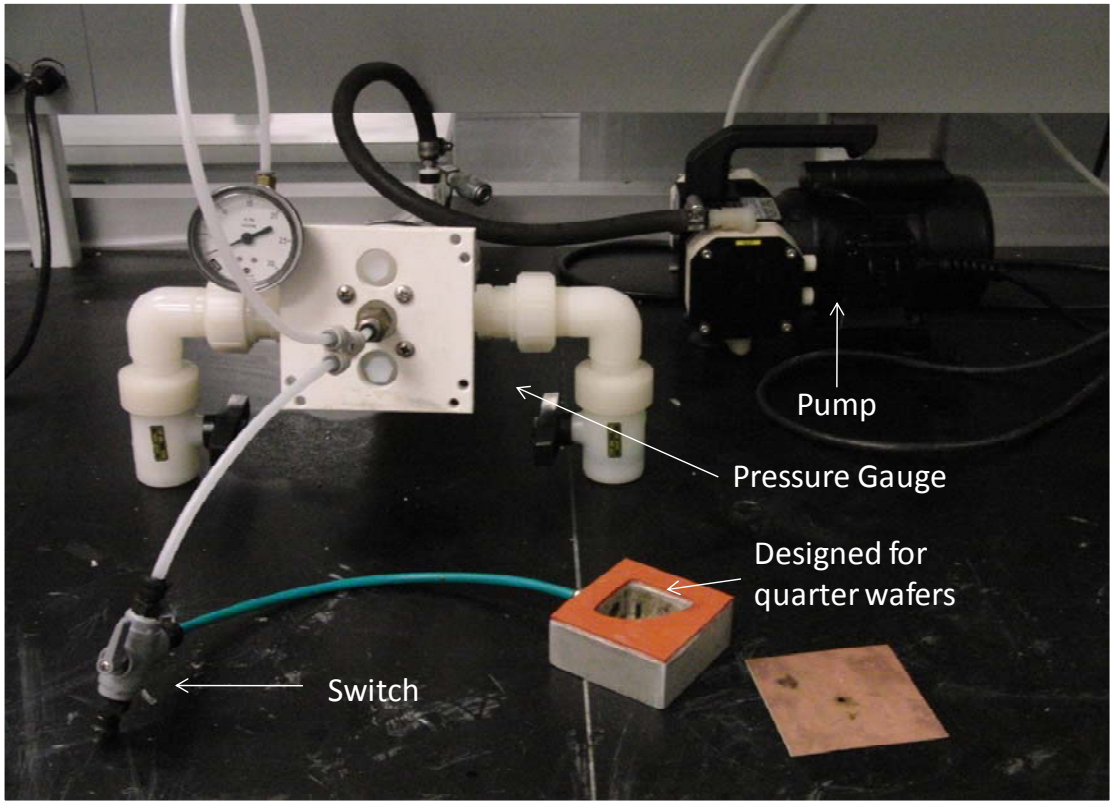


Figure 3. 9 Set-up for vacuum infiltration process

3.2.6 SEM characterization

Due to diffraction caused by large wavelengths of visible light, optical microscopes have limitations observing objects smaller than around 0.2 micrometer. SEM was thus developed for observation of much finer features. A beam is produced in the electron gun, and the electrons are subsequently accelerated towards the specimen. Detectors monitor the interaction between the electrons and surface atoms of specimen by catching signals such as secondary electrons, back-scattered electrons, X-rays, etc. Images are created as electron beams scan across a small area of the specimen. An SEM may go to magnifications as high as 100,000 times or more. PZT films were observed under the SEM for both front view and cross-section view.

SEM was also used to characterize the surface of the TSV side walls after vacuum infiltration was performed, confirming the deposition of a relatively conformal coating.

3.2.7 Capacitance Measurement

Capacitance measurement was done under room temperature using HP 4285 A Precision LCR meter at 100 kHz. DC bias was applied using Keithley 236 Source Measure Unit. For frequency dependence of capacitance, Solartron impedance spectroscopy was used. The frequency ranged from 0.01 Hz to 10 MHz.

3.2.8 X-ray Photoelectron Spectroscopy (XPS) Depth Profile

To study diffusion between layers, XPS depth profile was used. In photoelectric effect, as a result of the absorption of high energy electromagnetic radiation, electrons are emitted from the surface atoms of the material. The binding energy of the electron is decided by the energy of the X-ray and the kinetic energy of electrons emitted. Each state of a material has its own characteristic spectrum. By examining the spectrum, surface composition of a material and its chemical state can be determined. XPS is a widely used surface analysis tool with the ability for precise composition analysis. XPS combined with a sputter gun enables compositional depth profile analysis.

For depth profile, because ion beam of the sputter gun is not perpendicular to the sample surface, a rotating stage was used instead of a fixed stage, so that the crater created by ion bombardment is symmetric therefore eliminating XPS analysis errors. Diameter of the crater was set to be 3 times as large as that of the X-ray gun spot size for similar reason. A low current and 1000V voltage was used for ion gun, sputter time set to 30 seconds to ensure the speed of the compu-centric rotation did not exceed the rotation speed limit. The depth profiling was stopped after the ion gun sputtered past the PZT/LNO interface.

3.2.9 Leakage Current Measurement

Leakage current is measured using Keithley 236 Source Measure Unit. A maximum of 110 volts can be applied by this source, and a current range 100fA to 100mA can be

measured.

3.3 Results and Discussions

3.3.1 Thin film structural and interfacial characterization:

Platinum has been traditionally used as a bottom electrode for perovskite ferroelectric materials because it provides good interfacial stability and conductivity. However, sol-gel derived conducting oxides are preferred as the bottom electrode over platinum for various reasons such as:

(1) Ability to conformally coat TSV structures using solution infiltration processes.

(2) Better fatigue properties than platinum bottom electrode.

(3)Elimination of “hillocks” that are usually seen with platinum bottom electrode [44].

LNO was chosen from amongst all the conducting oxides because its lattice constant is very close to that of ferroelectric thin films and therefore provides good interfacial compatibility.

PZT films were derived by spin coating of sol-gel solution and rapid thermal processing (RTP) on sol-gel derived LNO electrodes. The details are provided in the previous section. The structural information was obtained by X-ray diffraction shown in Figure 3. 10.

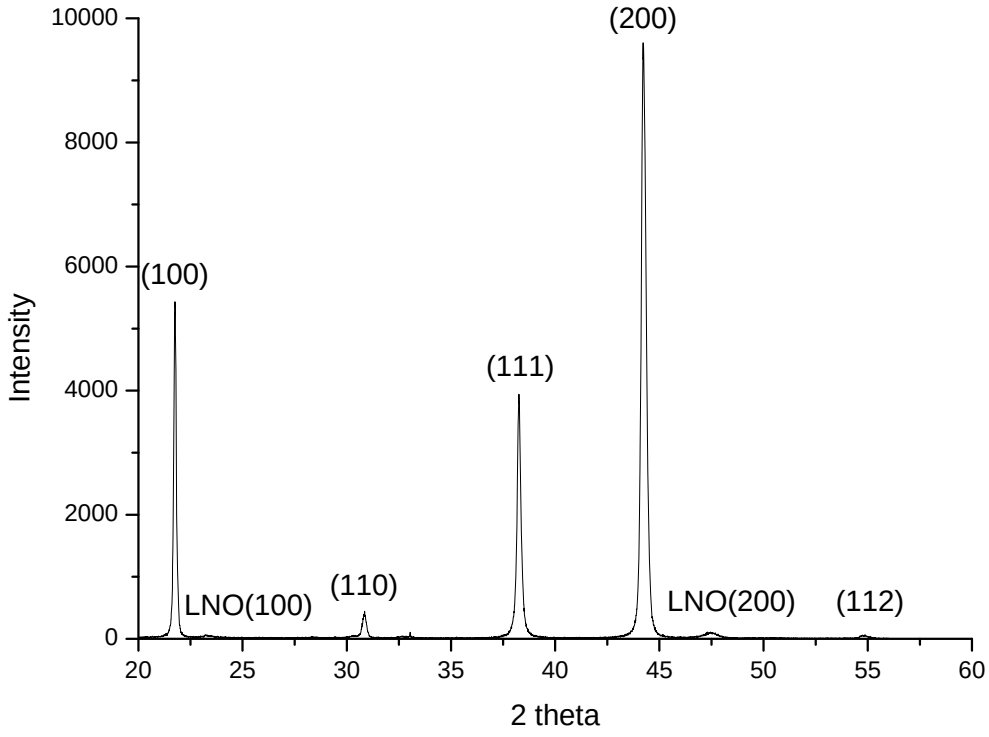


Figure 3. 10 XRD result of PZT/LNO film

As can be observed in Figure 3. 10, the peak intensities for various crystallographic planes indicated a polycrystalline film with random grain orientation. On the other hand, LNO grains showed a single orientation of (100). This is attributed to the lattice match between LNO and Si, as LNO film is directly prepared on silicon wafer. The lattice constant of silicon is 5.428Å, very close to the length of diagonal for (100) LNO, which is $\sqrt{2} \times 3.84 \approx 5.431$Å. Therefore, each square face of the LNO lattice sits in the middle of silicon lattice, schematically shown in Figure 3. 11 .

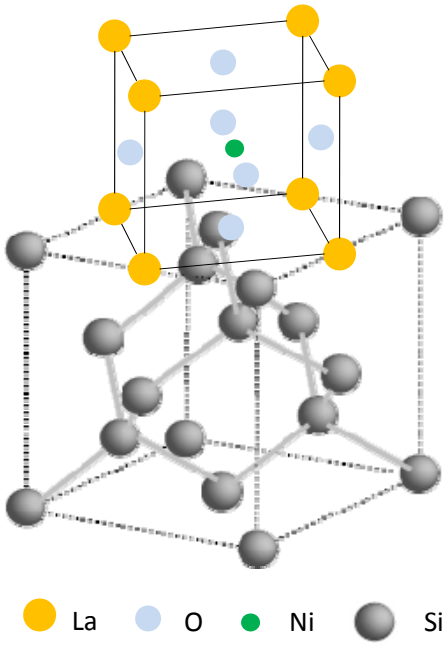
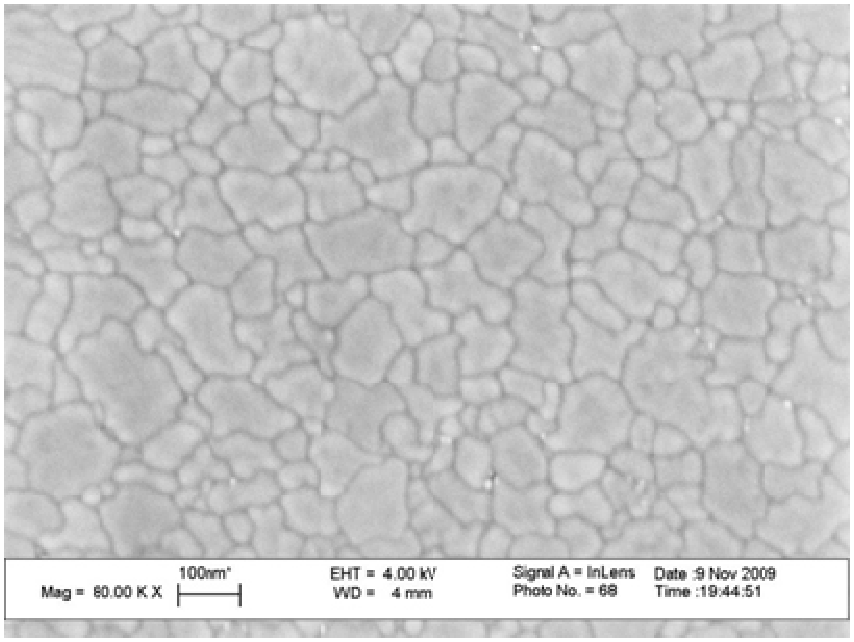
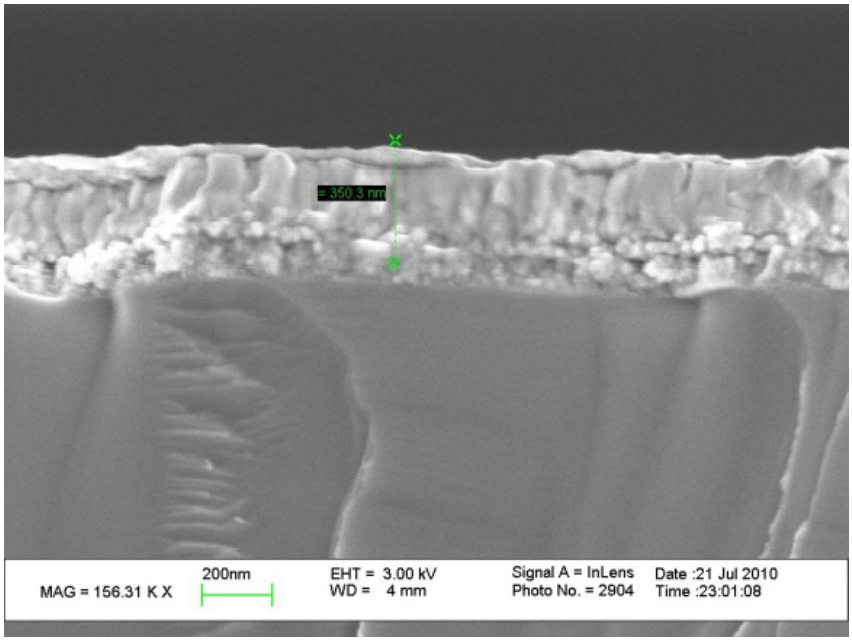


Figure 3. 11 Lattice match between silicon and LNO



(a) Top view of the sol-gel PZT thin film



(b) Cross section of the sol-gel PZT/LNO thin film.

Figure 3. 12 SEM pictures of planar PZT/LNO /Si devices

3.3.2 Electrical property characterization

PZT-based thin film capacitors with LNO electrodes were compared with that of platinum electrodes. Capacitance density of 3.2 - 4.3 μF/cm^2 was achieved with Pt electrode for planar devices. With LNO layer as the electrode, capacitance density was found to be 2.2 - 3.2 μF/cm^2 for planar devices, as shown in Table 3. 3.

Table 3. 3 Dielectric properties of planar devices

	PZT/LNO	PZT/Pt
Capacitance Density (μF/cm^2), 0V/100kHz	2.2 ~ 3.2	3.2 ~ 4.3
Leakage Current at 10V (μA/cm^2)	~7.8	~6.3

The degradation in capacitance density with LNO electrodes is attributed to the roughness of the electrode, defects in sol-gel derived films and inter-diffusion between the LNO and PZT oxides. As shown in Figure 3. 13, inter-diffusion between

sol-gel derived layers were confirmed by XPS depth profile. Surface roughness of LNO layer originates from the sol-gel process itself. Sol-gel derived films from spin-coating and subsequent heat treatment step is not as smooth as films deposited by sputtering. With a relatively rough surface, the spin coating of PZT could be affected, resulting in thickness variations across the surface, which is detrimental to the dielectric properties of the PZT film. Defects could result from hydrolysis of the sol, inhomogeneity in the solution or contamination picked up during any step of the process. Loss tangent of PZT film is found to be much higher with LNO electrode due to the higher electrical series resistance of LNO film compared to platinum.

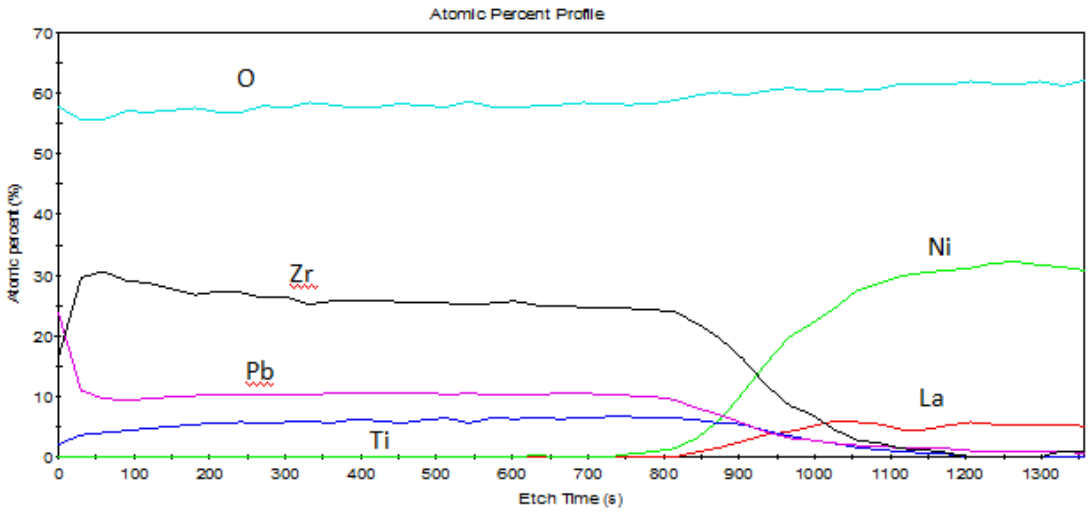


Figure 3. 13 XPS compositional depth profile of planar films

Analysis of electrical characterizations shows two problems with all-solution derived LNO electrode. The first one is inability to scale up. Comparing the capacitance of circular device (diameter of 0.6 mm) with that of a 1 mm×2.5 mm rectangular device, the capacitance of the bigger device is less than two times of the smaller device. This is due to existing defects in the dielectric layer, and can be avoided with clean and moisture-free environment. The second problem is the high loss tangent of devices. This is attributed to high series resistance associated with the LNO, which is many times more resistive than most metals [49]. The high ESR of LNO also compromises high frequency applications of these sol-gel derived thin films.

It is reported that deposition of dielectrics on silicon usually results in interfacial traps that can degrade the leakage current reliability. Surface pre-nitridation and use of TiN as the electrode is shown to improve reliability [35]. To improved leakage property for LNO electrode, an insulating ZrO_2 barrier was deposited between the LNO and silicon wafer.

3.3.3 Capacitors with anti-ferroelectric thin films

To demonstrate anti-ferroelectric thin film capacitors for achieving higher capacitance densities at the operating voltage, PZT was doped with lanthanum, to form antiferroelectric $Pb_{0.92}La_{0.08}(Zr_{0.95}Ti_{0.05})O_3$. The antiferroelectricity behavior of this composition, $Pb_{0.92}La_{0.08}(Zr_{0.95}Ti_{0.05})O_3$, was tested with ferroelectric tester by B. Ma et al. [50] It is shown in Figure 3. 14 that the peak dielectric constant shows under a bias field of around 240kV/cm. For a dielectric film thickness of 200nm, the peak capacitance should be at 4.8V.

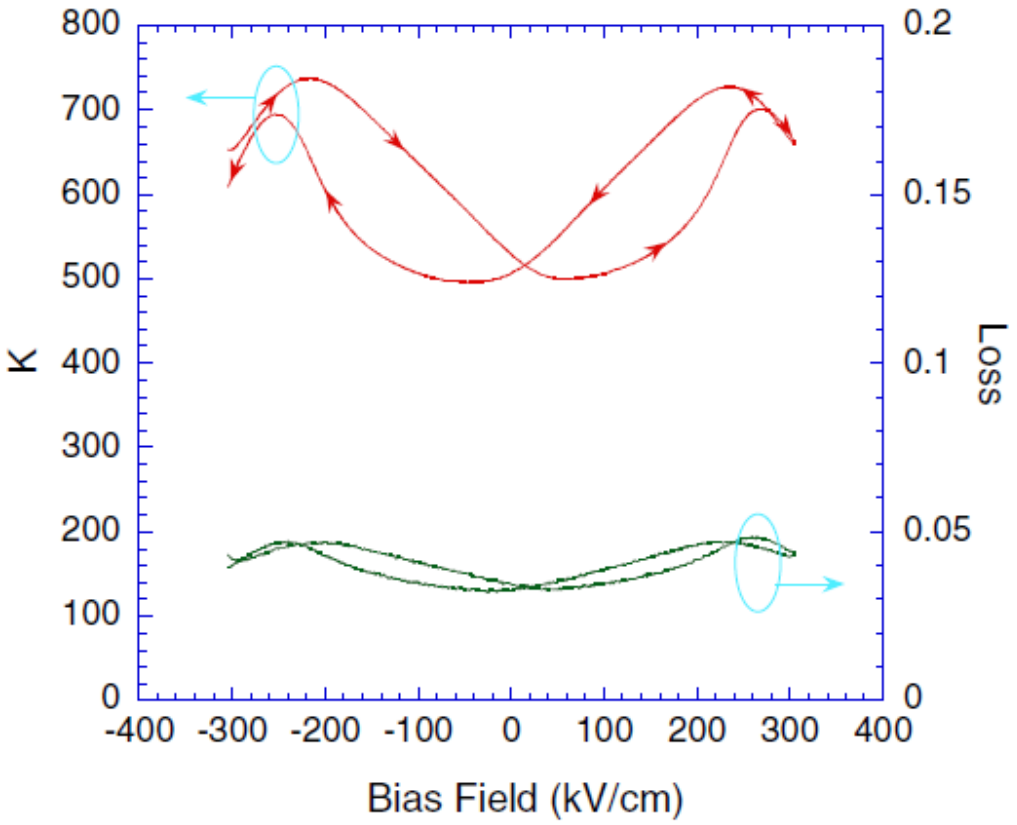


Figure 3. 14 Dielectric properties measured at room temperature as a function of bias field for PLZT/LNO/Ni sample [50]

Results of capacitance density vs. DC bias are shown in Figure 3. 15. The peak capacitance occurred at 7 volts, which is inconsistent with literature [50]. The change in peak capacitance voltage from 4.8V shown by Ma et al., to 7V in this study is probably due to the existence of ZrO_2 layer in current study, as well as varying extent of interfacial diffusion of sol-gel derived thin films, caused by the differences in heat treatment. Capacitors with ZrO_2 barriers showed very different behavior in capacitances vs. voltage plot compared to those with no barrier.

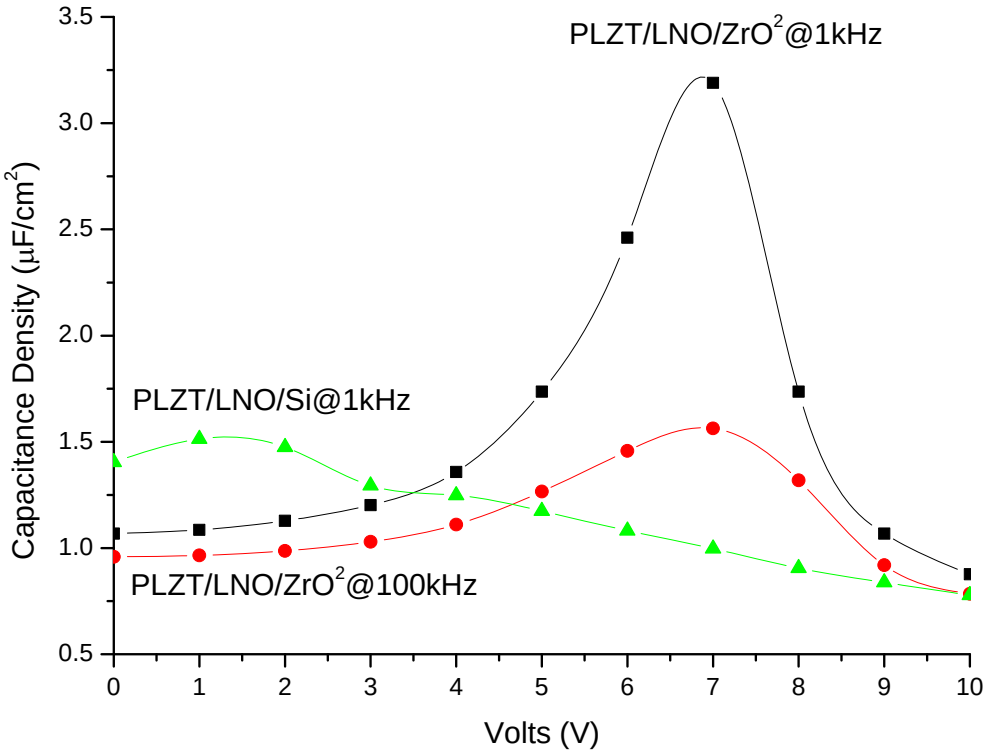


Figure 3. 15 Capacitance density vs. voltage plot for anti-ferroelectric devices

According to Figure 3. 15, the capacitance density for PLZT/LNO/ZrO_2 device increased when testing frequency dropped from 100 kHz to 1 kHz. This is due to the relatively high ESR of the LNO electrode, which degrades performance of the device at higher frequencies. However, the trend for capacitance density over DC bias did not change. Compared with PZT/LNO/Si devices, PZT/LNO/ZrO_2/Si devices show peak capacitance density at 7 volts instead of 1 - 2 volts. This phenomenon and the underlying mechanisms require further investigations.

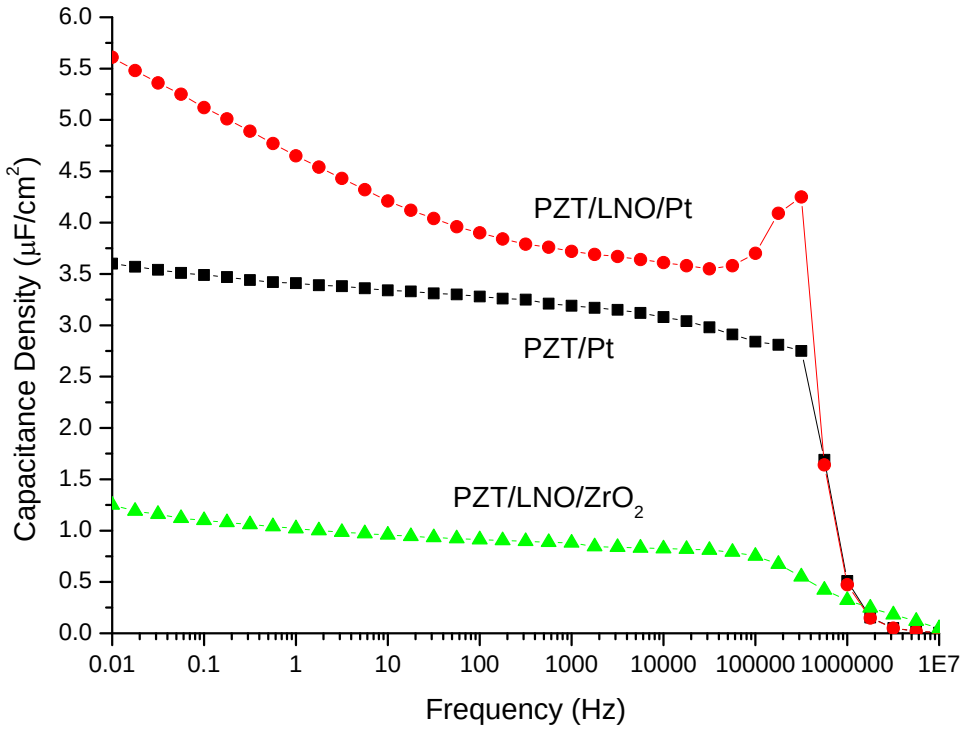


Figure 3. 16 Frequency response of capacitors with different configurations (obtained at 0V bias)

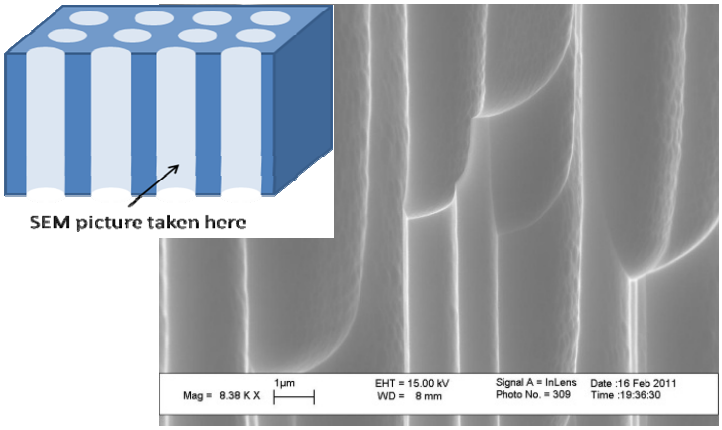
Impedance spectroscopy was used to study the frequency dependence of thin film capacitors. The dielectric film thickness was around 200 nm for all three devices. The results are shown in Figure 3. 16. It can be observed that devices without platinum electrode did not retain their high capacitance density even at 100 kHz while the devices with platinum electrodes retain the capacitance density beyond 400 kHz. This can be attributed to the higher ESR caused by LNO electrode. The capacitances of devices with platinum electrodes were found to drop drastically around 1MHz. Ferroelectric films with noble metal electrodes usually show stable properties till hundred megahertz. The drastic drop in capacitance should be attributed to the parasitic inductance introduced by the cables. To have a more precise characterization at higher frequencies, special connectors and calibration corrections for parasitics are required.

3.3.4 Conformal solution-derived trench coatings

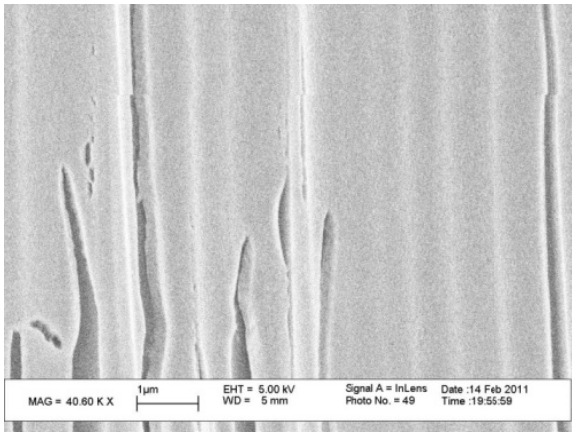
The first part of this research focused on fabricating 50 micron vias with an aspect ratio of 10. However, instead of etching through the 500µm thick wafer, the DRIE stops after around 150µm. The photoresist debris from RIE falls into the small blind vias and block the etching. The tool and photoresist limited the aspect ratio to around 5. By increasing the diameter to100µm, TSVs with an aspect ratio of 5 were successfully fabricated. To obtain TSV structures with higher aspect ratio, oxide masks are preferred, modified processes and more advanced etching tools (such as STS PEGASUS instead of PLASMA-THERM ICP) are needed.

LNO was used to demonstrate the conformal electrode on these TSV structures. The coatings from vacuum infiltration were heat-treated at 700˚ C, for 15 minutes in air, with a heat ramp of 5˚ C n/min. The samples were then cross-sectioned and examined in SEM to study the conformality. The location from where the SEM image was obtained is shown in the schematic in Figure 3. 17 (a). As indicated in Figure 3. 17 (c), there was a conformal coating of LNO layer over the walls of the TSVs. Pressure gradient acted as a driving force to form the conformal coating of the precursor solution. However, too high a pressure can result in a non-uniform thickness of the solution coating, or shattering of the wafer. Furthermore, when concentration of the LNO precursor solution is too high (0.2mol/L), cracks are seen in the film, as shown in Figure 3. 17 (b).

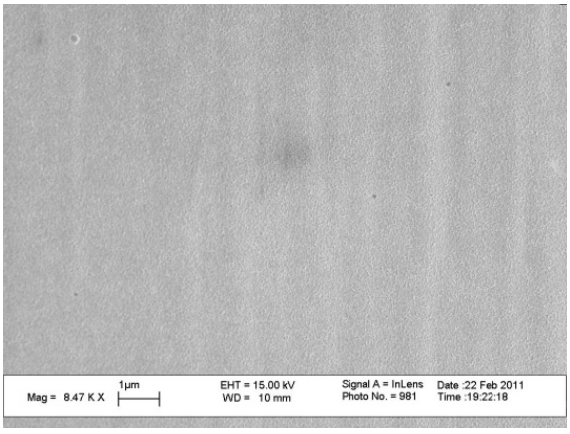
To improve film quality, the concentration of precursor solution was decreased from 0.2mol/L to 0.02mol/L. Multiple coatings were made with reduced pressure gradient. With the above mentioned process optimization, conformal coatings without pores or cracks, as shown in Figure 3. 17 (c), were obtained.



(a) SEM of bare silicon TSV.



(b) TSV Coatings with cracks due to high concentration of precursor solution



(c) Conformal coating without cracks or pores with appropriate concentration and infiltration conditions.

Figure 3. 17 SEM pictures LNO coatings over TSV by sol-gel vacuum-infiltration

In conjunction with the planar capacitors discussed earlier, the feasibility of conformal solution coatings in trenches with aspect ratio of 5 - 10 can potentially lead to a capacitance density 10 - 30μF/cm^2, which can meet the emerging needs for thin power supply capacitors in a silicon interposer.

CHAPTER 4

NOVEL ELECTRODES FOR ALUMINUM ELECTROLYTIC CAPACITORS

4.1 Motivation and impact

Thin film capacitors that are compatible with large-area organic package integration at lost cost are critical for miniaturization and performance enhancement of electronics packages, modules and systems. Three main approaches are currently being pursued for embedding high density capacitors: (1) embedding discrete MLCC or tantalum capacitors, (2) silicon trench capacitors, and (3) embedding planar thin film with high K dielectrics on metal foils. Discrete tantalum or ceramic capacitors, although capable of meeting the capacitance density targets, are limited in form factor reduction required for embedding into thin organic packages. Further, placement costs dominate when discrete components are embedded into a package. Silicon trench capacitors can be thinned down to below 100 microns, but they involve high-cost processes due to the usage of exotic process tools such as Atomic Layer Deposition (ALD). Planar thin film capacitor embedding pursued by GT PRC, DuPont and others can address most of the needs except for scalability to higher capacitance densities and are limited to 1-2 $\mu F/cm^2$. A low cost and scalable platform technology for high volumetric efficiency capacitors based on high surface area structures with conformal dielectrics is thus proposed. Anodization yields a dielectric layer with permittivity of around 8, which is combined with the high surface area from etching deep channels in aluminum foils to yield high-density capacitors.

The primary benefits of this approach are:

1) Aluminum etched foils are available in large-area for low-cost processing and easy integration in organic panels.

2) Aluminum electrolytic and solid-state capacitors are widely studied and hence the

fundamental material system is well-understood.

The main objectives of this research are to:

- Study the role of anodization conditions on the capacitance and leakage for etched aluminum foils.
- Explore various top electrodes for such etched foil capacitors.
- DC and high-frequency characterization of the etched foil capacitors.

4.2 Experiment procedures

Anodization process:

Electrolyte formulations and anodization process was optimized to form the conformal dielectric on etched aluminum foils. The inherent characteristics of anodization such as its self-limited and surface-reactive nature are expected to make the oxide film conformal even in deep channels with aspect ratio of around 40. The uniformity and thickness of the dielectric over a large-area substrate is controlled with the anodizing voltage, chemistry of electrolyte and agitation from stirring.

Anodization is an electrochemical process in which aluminum acts as an anode in the electrolyte to form a thin oxide film on the surface. Stable metals such as platinum form the cathode. The chemical reaction in the anodization process mainly constitutes electrolysis of water. When current passes through the circuit, hydrogen is generated at the cathode, and oxygen at the anode. Along with oxygen gas evolution, atomic oxygen and oxygen ions are also formed. These latter components are much more chemically reactive than oxygen. They diffuse and react with the aluminum to form an oxide on the surface of the anode. The set-up of the experiment is shown in Figure 4. 1. Anode (aluminum) and cathode (platinum) are clamped with alligator clips and dipped in the electrolytic bath. AGILENT U8002A DC current power supply is used.

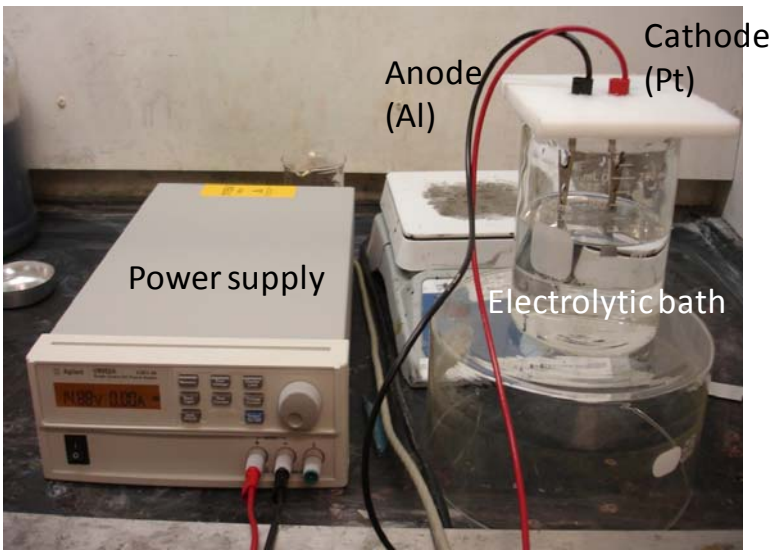


Figure 4. 1 Set-up for anodization process

Chemical reactions in the anodization process:

Anode reaction: $2Al+3H_2O=Al_2O_3+6H^+$

Cathode reaction: $2H^++2e=H_2\uparrow$

Overall reaction: $2Al+3H_2O+6e=Al_2O_3+3H_2\uparrow$

Conducting polymer top electrode process:

PEDT monomer (Ethylene dioxythiophene, EDT, Clevios MV2^{TM}) was mixed with oxidizer iron(III) tosylate (Clevios CB-40^{TM}) in the weight ratio of 1:25 and then quickly dispensed on to the surface of the dielectric film using a syringe, just when the polymerization reaction begins. It was then allowed to polymerize and dried at 50 ^oC on a hot plate in air for about 60 minutes. In-situ polymerization of the monomer and oxidizer was carried out after quickly dispensing the monomer-oxidizer mixture on the etched foils. A layer of conductive graphite was directly deposited onto the PEDT as a current collector. External contact to the polymer electrode was established by applying a layer of silver paste over the graphite.

ALD TiN top electrode process

ALD process is an advanced thin film deposition technology based on surface

chemical reactions. It is widely used in research and industry for deposition of oxides, nitrides, sulfides, metals, carbides and borides. The advantages of this technology are the low temperature process, low stress, excellent adhesion, great step coverage, good film quality and thickness control. Disadvantages of this approach include low deposition rate, high cost and limited material availability. TiN top electrode was only used for a comparative study here.

The ALD process starts with a functionalized surface. The surface is exposed to the first precursor. As the surface is functionalized, the first precursor will cover the surface with a monolayer and bond with the function groups on the surface. The bonding stops as soon as a complete monolayer is formed. A purge and evacuation is performed to remove excessive precursor as well as by-product, leaving only the monolayer formed with the first precursor. The sample is then exposed to a second precursor. This time, a surface chemical reaction happens between the monolayer formed by the first precursor and the second precursor. Again, the surface chemical reaction is self-saturating. Another purge and evacuation is performed to remove the excessive precursor. The process runs in cycles, each cycle constituting the above steps with the first and second precursors. The substrate needs to be heated to an appropriate temperature for the surface reactions to happen in a short interval of time. Plasma ALD is frequently used to lower the deposition temperatures of nitrides. A film of desired product is thus formed layer by layer.

Because of the self-saturating nature of the process, good film quality, thickness control and great step coverage can be obtained. The schematic of the ALD process is shown in Figure 4. 2.

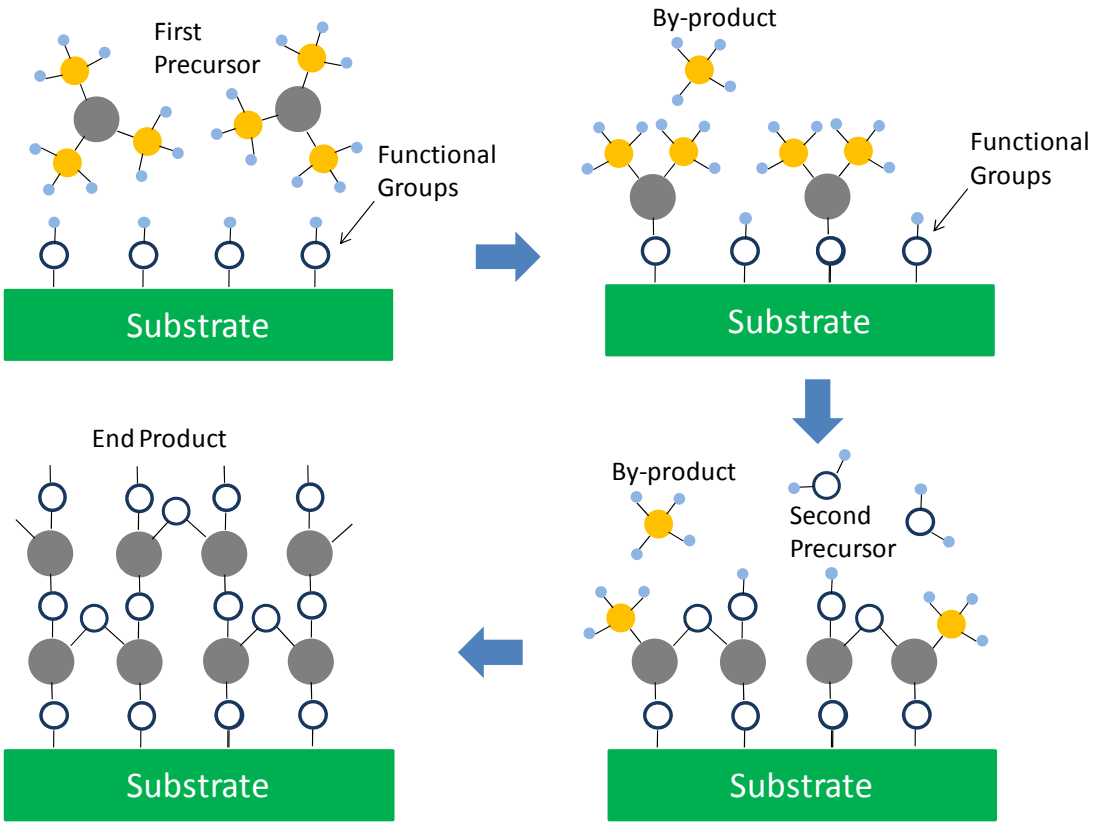


Figure 4. 2 Schematic of ALD process

Titanium nitride has excellent properties such as high melting temperature, thermodynamic stability, and hardness; good thermal and electrical conductivity. TiN is widely used as a seed-layer coating and diffusion barrier between aluminum metallization and silicon in industries. TiN film is normally deposited by Chemical Vapor Deposition (CVD) or reactive sputtering of Ti metal and Ar/N_2 gas mixture.

In this study, TiN was deposited with ALD (Ti precursor and N_2 plasma) to achieve conformality over deep trenches. The TiN film of ~20nm thickness were patterned using carbon black and Ag paste as an etch mask in order to isolate smaller devices. Reactive ion etcher (RIE) was used for the nitride etching process (with following parameters: SF_6 – 45 sccm, O_2 – 5 sccm, RF power – 350W).

Electroless metal process

Though conducting polymers are widely used in aluminum and tantalum capacitors

because of their excellent conformality, self-healing and low cost, they present other challenges such as poor thermal stability and higher Equivalent Series Resistance (ESR). Metal electrodes can address these limitations.

Electroless plating of metals are widely used in packaging industry for the deposition of seed layer for plating on planar as well as 3D surfaces. Advantages of employing electroless metal as top electrode are:

- Easy access of all surfaces by liquid chemicals
- Low-temperature and scalable solution-deposition process
- Inexpensive compared to vacuum deposition technologies
- High throughput
- Well-established industrial process

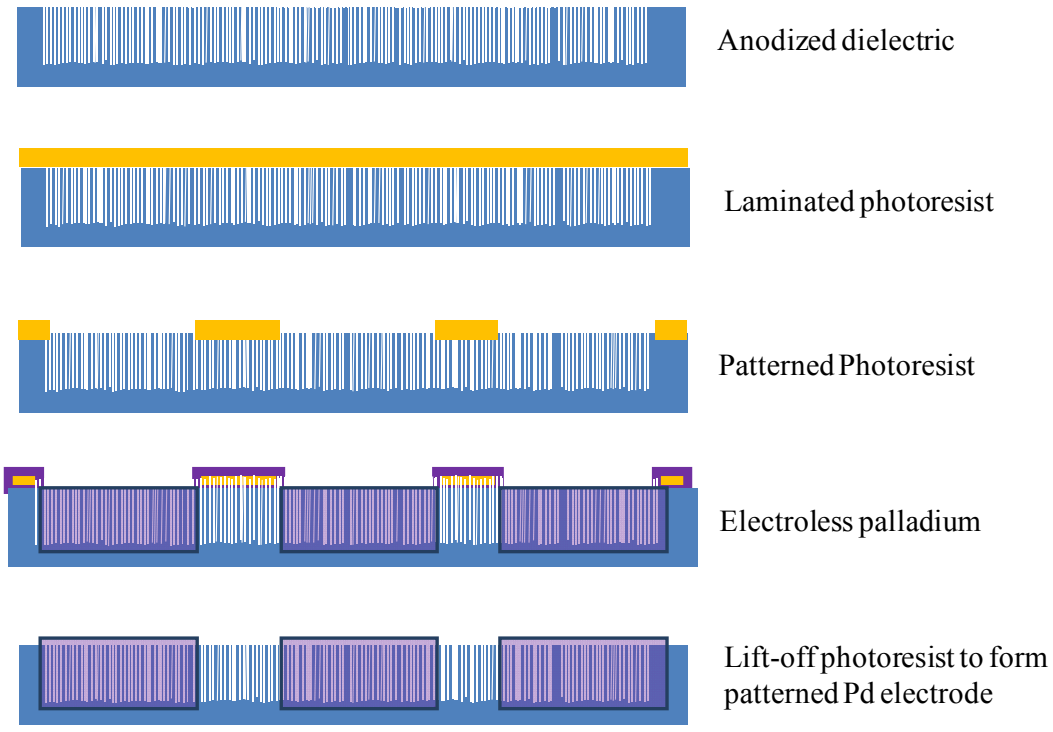


Figure 4. 3 Steps involved in the lift-off process

Palladium deposition and patterning on etched aluminum foils was carried out using a

dry-film photoresist lift-off process (Figure 4. 3). The anodized etched aluminum foils were laminated with dry film photoresist and patterned for selectively depositing palladium as the top electrode.

Electroless Plating of Palladium:

The process is designed to chemically plate palladium on insulating surfaces such as FR4 and was used as obtained. The steps involved for electroless plating of Pd are as follows:

1. Lithography
2. Pre-dip Bath (Room Temperature, 1min)
    - Surface preparation, pH = 1.9
3. Conditioner Bath (50˚C, 5min)
    - Functional polymers, pH=11.5
4. Conductor Bath (55˚C, 5min)
    - Colloidal Pd solution stabilized with an organic compound, pH=1.9
5. Pd Deposition Bath (55˚C, 1min)
    - Auto-catalytic deposition, pH=5.5
6. Lift-off (Removal of Photoresist)
7. Further Deposition of Pd (55˚C, 30min)

Characterizations:

LEO 1530 SEM was used for characterization of the structure of etched aluminum foils. Capacitance measurement was done under room temperature using HP 4285 A Precision LCR meter. Solartron impedance spectroscopy was used to characterize the frequency dependence of capacitance. The frequency ranged from 100 Hz to 10 MHz.

Signatone four-point probe was used for the characterization of top electrode material.

A comparison was made between conducting polymer and TiN. The reason for the use of four-point probe instead of two-terminal probe was that in the four-point probe measurement, current source and voltage meter are separated. This way, the errors from wiring impedance and contact resistance can be avoided and a precise measurement of the sheet resistance can be made. Film thickness is needed for the calculation of the resistance of each material. Film thickness of deposited ALD TiN was calculated from the cycles run, as deposition rate was already characterized by Woollam Ellipsometer. Thickness of PEDT was measured with a Dektak 150 Profilometer.

4.3 Results and Discussions

Ta_2O_5 has much higher permittivity than Al_2O_3, less surface enhancement is needed for tantalum capacitor, this results in smaller ESR per unit capacitance. However, etched aluminum foils are used in this project because of their compatibility with organic panel processing. Tantalum capacitors in the form of sintered particles are not available in large area that is suitable for embedding into an organic substrate. Aluminum foils, compared to tantalum foils, have much lower cost. The first part of this research task focuses on characterization of etched aluminum foils.

4.3.1 Morphology of the etched aluminum foils

Commercial etched Al foils obtained from Hitachi Chemical were used as the high surface-area electrodes. SEM observation of the samples shows the potential to achieve the target channel width and aspect ratio as shown in Figure 4. 4.

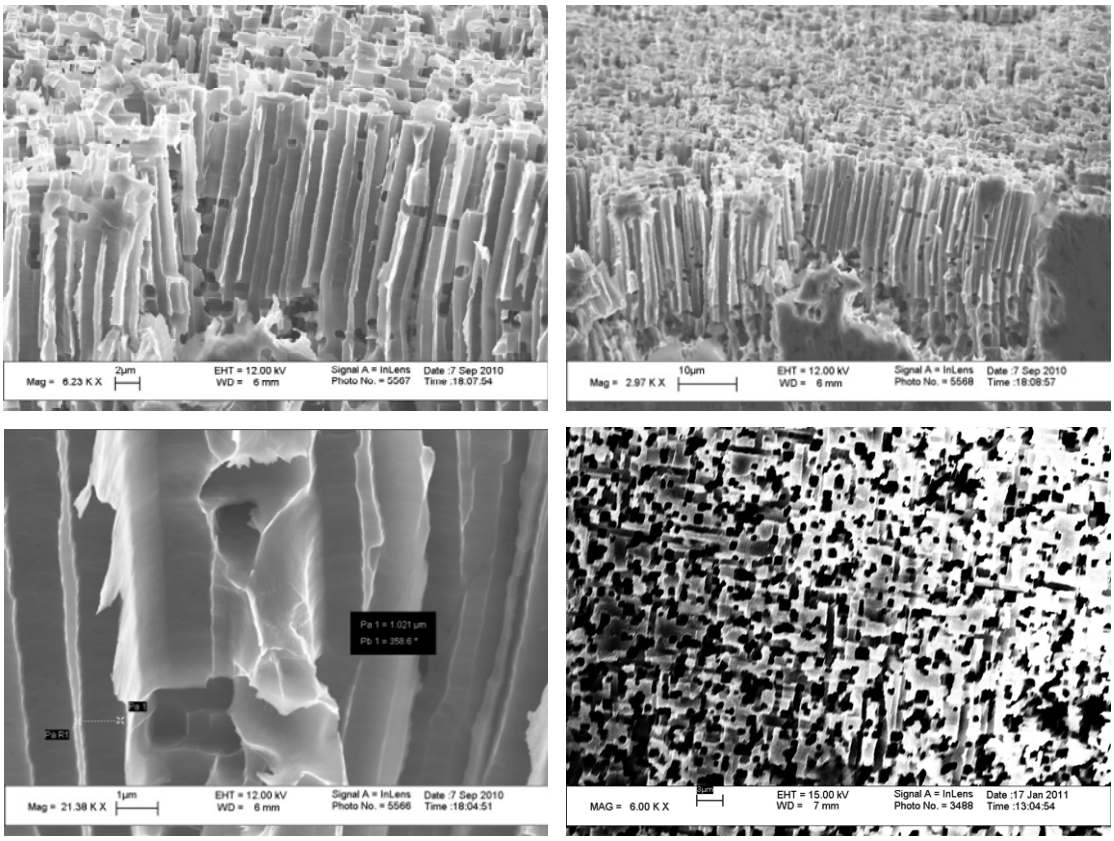


Figure 4. 4 Surface and cross-section morphology of specimen

4.3.2 Anodization conditions

Anodization yield different products with different electrolyte conditions [51]. In the process, the rate of two different reactions determines the formation of the oxide film. The reactions are:

(1) Dissolution of aluminum oxide

$$Al_2O_3 + nH_2O \rightarrow Al^{3+} + O^{2-} + OH^- + H^+$$

(2) Formation of oxide

$$Al + O^{2-} \rightarrow Al_2O_3 + e.$$

In a near-neutral solution, the dissolution of aluminum is very slow. A conformal oxide is thus formed. In an acidic solution, however, the dissolution rate is always uneven at nano-scale, resulting in the formation of a pit shown in Figure 4. 5 (B). It is worth noting that E=U/d (U: voltage difference across the oxide film, d: thickness of

the oxide film) drives oxygen anion through the oxide film into the Al/Al_2O_3 interface, to balance the dissolution of oxide. As the oxide become thinner, the driving force, E, for oxide formation becomes larger, thus resulting in the formation of cylindrical pores.

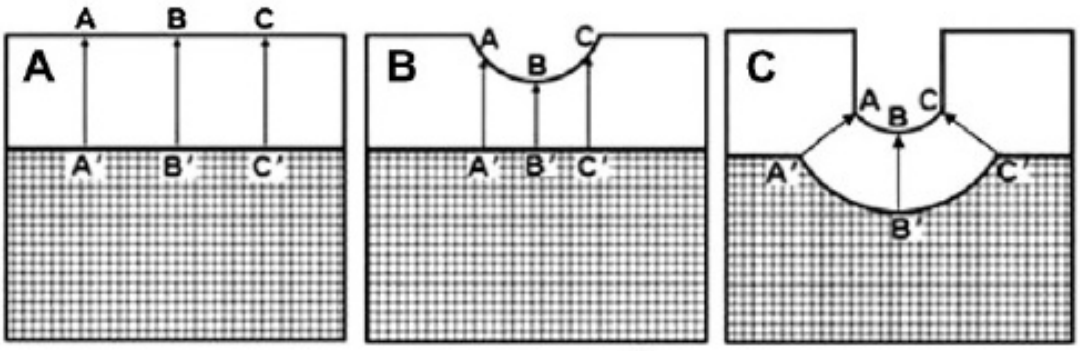


Figure 4. 5 The beginning of formation of nano-porous AAO [51]

As the pores grow deeper, they can also grow wider. When two pores grow together, they will merge as shown in Figure 4. 6 E -> F -> G (oxide dissolution from both sides). When two pores are too close, they will separate with a thickness increase in the shared wall because of the increase in driving force E from both sides.

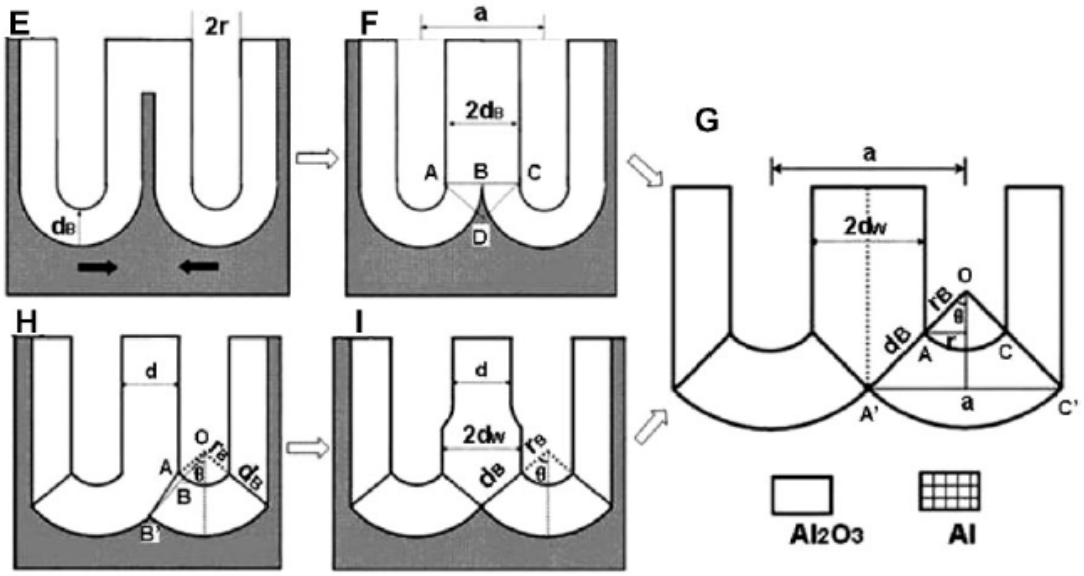


Figure 4. 6 Formation of nano-porous AAO [51]

If the electrolyte is too acidic, the oxide immediately dissolves after formation, which results in anodic etching of aluminum.

To achieve 5μF/cm^2 for Al foils, a planar capacitance of above 0.2μF/cm^2 with an area enhancement of 25 times is desired, which corresponds to an oxide film thickness of around 50 nm. Citric acid with a low concentration of 1g/L was used as the electrolyte, to obtain a conformal layer of oxide film with the required thickness. A constant voltage of 30 V was applied during the 30 min anodization process. The current continuously drops as the anodization proceeds. The anodization process was performed for 30, 60 and 120 min. The capacitance density did not vary much with respect to time of the process, indicating that the film growth stopped after 30 min and did not continue after that. The capacitance density was 0.26, 0.25 and 0.23μF/cm^2 for those respective times. The BDV was 16 to 19 volts in all the three cases.

To further enhance the capacitance density, the anodization process was performed with lower voltages and time. The capacitance density enhanced significantly by lowering the anodization times and also by reducing the anodization voltages. The highest capacitance density was 0.44μF/cm^2. However, shortening process time and lowering anodization voltages also compromise the BDV of the dielectric. The results are compiled in Table 4. 1.

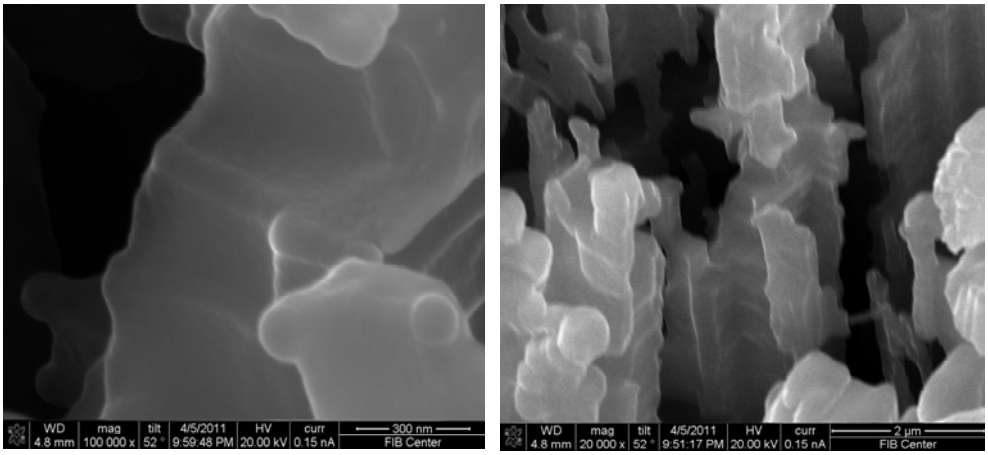
Table 4. 1 Capacitance density and breakdown voltage for planar devices with different anodization voltages and time

Anodization Voltage	Anodization Time	Capacitance Density	BDV
20V	30min	~0.26μF/cm^2	19V
20V	1.5min	~0.31μF/cm^2	14-15V
20V	1min	~0.45μF/cm^2	9-12V
15V	30min	~0.30μF/cm^2	12-14V
10V	30min	~0.44μF/cm^2	12V

Results were obtained at 100 kHz, for planar devices with gold top electrode, impedance spectroscopy showed a flat frequency response. It can be observed from Table 4. 1 that the thickness of oxide film increases rapidly in the beginning stage of the anodization process. As thickness increases, the growth rate decreases. Given the anodization time, the voltage, which determines the driving force for film growth E, is positively related to film thickness. Increase in oxide film thickness results in increase in breakdown voltage, as well as a decrease in capacitance density.

4.3.3 Morphology of the anodized aluminum foils

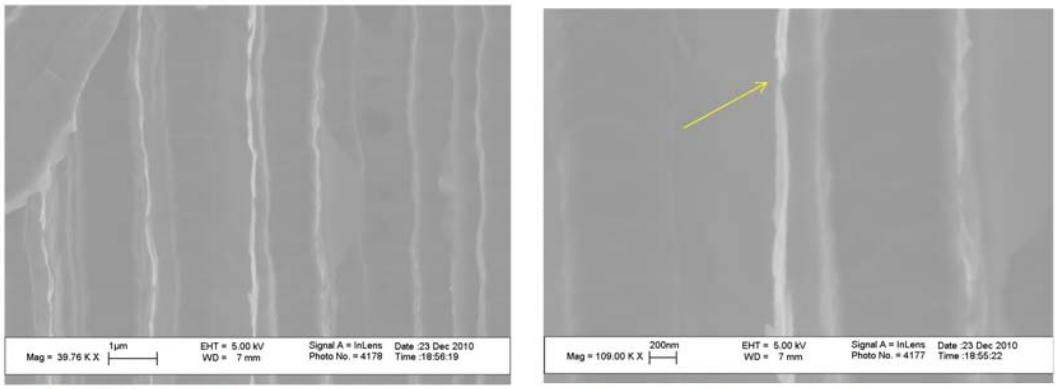
The anodization conditions were then applied for etched foils. Mechanical stirring was used for agitation. FIB-SEM was initially used to characterize the cross-sections. No clear demarcation of Al/Alumina interface was seen even with the FIB cuts (Figure 4. 7). Foils cut with scissors and examined in high-resolution SEM, however, showed some indication of conformal alumina dielectric as shown in Figure 4. 8.



FIB with 0.5 nA ion gun

FIB with 0.5 nA ion gun

Figure 4. 7 Cross-section of anodized aluminum foil by FIB cut



Bright lines: Alumina

Thinner alumina spots in some areas

Figure 4. 8 Cross-section of anodized aluminum foil by cutting

4.3.4 Conducting polymer as a top electrode

For the etched aluminum foil structure, poly(3,4-ethylenedioxythiophene) (PEDT) was chosen as the candidate for top electrode because of its wide use in tantalum capacitors. PEDT infiltration in anodized foils was characterized by SEM and EDS, as shown in 0.

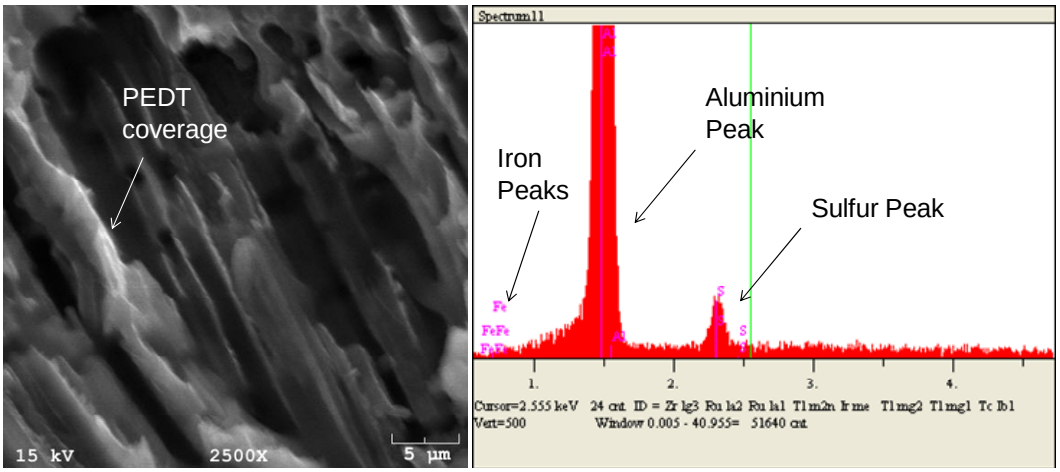


Figure 4. 9 XRD & EDS characterization of PEDT infiltration

In the SEM image, the rugged surface corresponded to the polymer, confirming PEDT coverage at the bottom of the trench. EDS characterization at various depths confirmed the existence of the conducting polymer. The iron and sulfur peaks originate from the oxidizer, iron(III) tosylate.

Planar and etched foils with PEDT/ carbon black (CB)/ silver paste as top electrode were measured with LCR meter. Capacitance densities were measured at various frequencies and the results are plotted in Figure 4. 10.

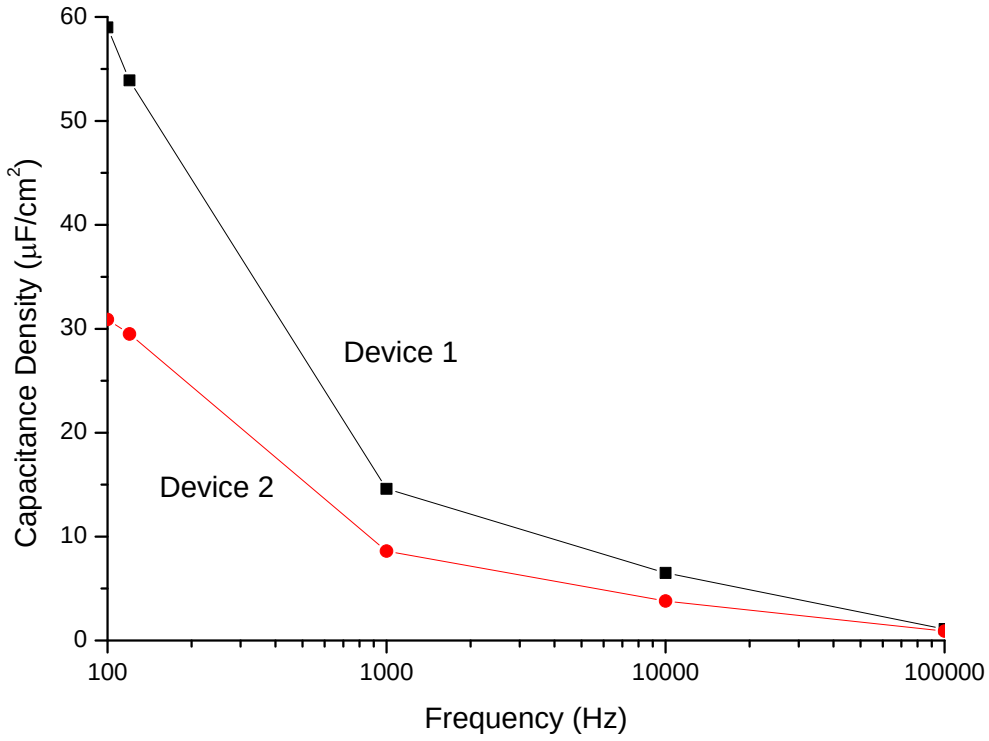


Figure 4. 10 Capacitance density variation with frequency for etched Al foil test devices with PEDT/carbon black and Ag paste as top electrode

As is evident from Figure 4. 10 (obtained at 0V bias), capacitance densities of above 10μF/cm^2 were measured at ~1 kHz for etched foils devices. Most of the etched foil devices showed degradation to 1 - 3 μF/cm^2 at 100 kHz.

Impedance measurements were carried out to compare with the results obtained from the LCR meter. The results also showed similar frequency dependence as etched-foil test structures, while the planar test structures showed more stable capacitance over a large frequency range. Figure 4. 11 shows the frequency sweep result of a planar Al/Anodized Al_2O_3/PEDT/CB/Ag device at 0V bias.

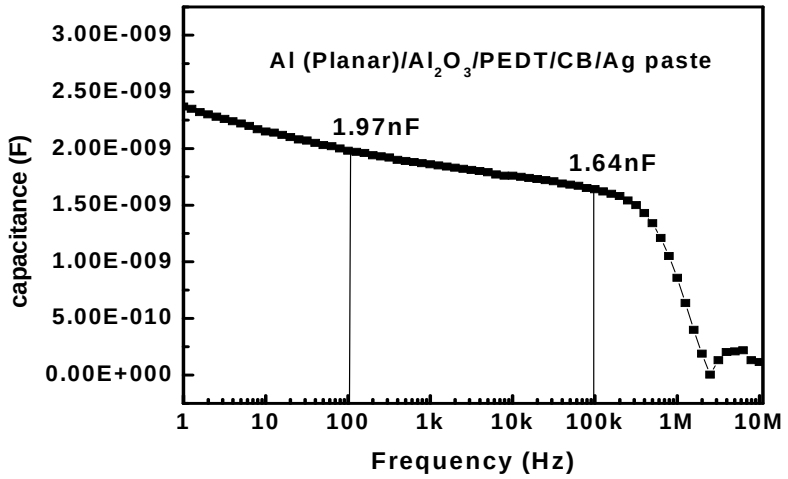


Figure 4. 11 Frequency vs. capacitance density of planar $Al/Al_2O_3/PEDT/CB/Ag$ test structure

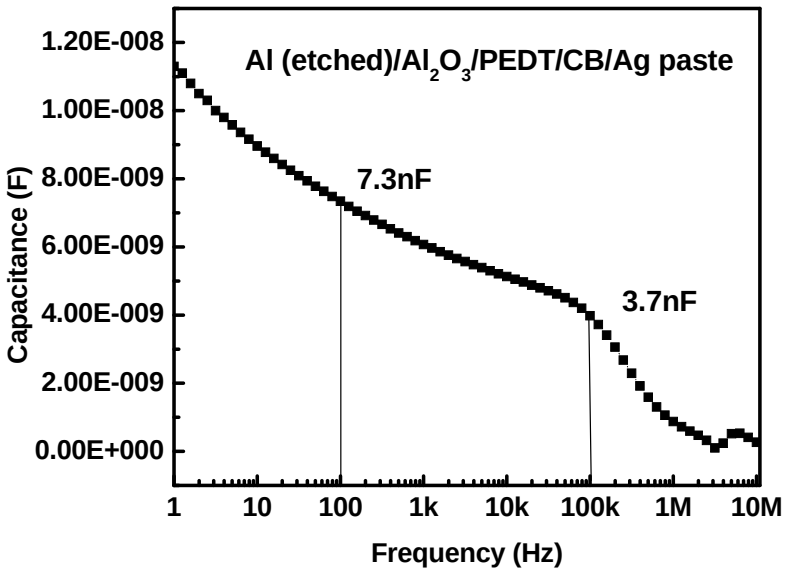


Figure 4. 12 Frequency vs. capacitance density of etched $Al/Al_2O_3/PEDT/CB/Ag$ test structure

Figure 4. 12 is the capacitance vs. frequency plot for an etched foil capacitor structure (results obtained at 0V bias). It can be observed that etched foil devices had a more evidential drop in capacitance than planar devices.

To understand the frequency response, an equivalent circuit of the electrolytic capacitor needs to be studied.

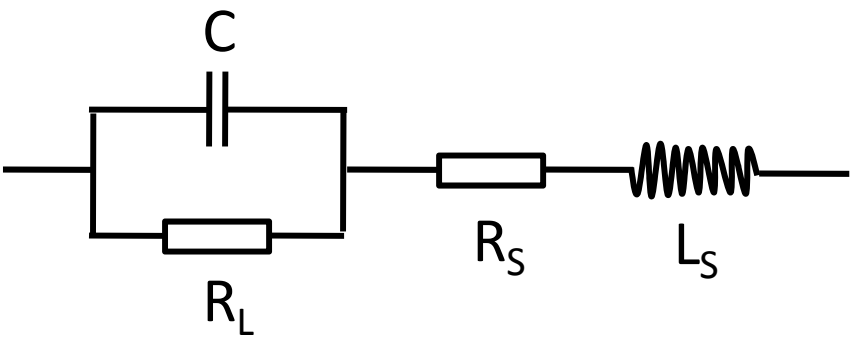


Figure 4. 13 Equivalent circuit of an aluminum electrolytic capacitor

The equivalent circuit of an aluminum electrolytic capacitor is given in Figure 4. 13. C is the capacitance of the ideal capacitor. R_L is the resistance of the dielectric layer. R_S and L_S are the equivalent series resistance and equivalent series inductance contributed by the top electrode material, current collector as well as the connection (including cables of characterization tools), respectively. In low frequency range, the effect of R_S and L_S can be neglected, leaving C and R_L. The impedance for a capacitor and resistor in parallel is given by:

$$Z^* = \frac{1}{\frac{1}{R} + j\omega C}$$

So,

$$C_{test} = \frac{1}{j\omega Z^*} = \frac{\frac{1}{R} + j\omega C}{j\omega}$$

If R is large enough, the term 1/R can be neglected, C_{test} equals to C. However, due to impurities in the foil as well as contamination in the electrolyte in the anodization process, defects are formed. The defects lead to leakage, which makes R much smaller than that of an ideal dielectric film. The 1/R thus contributes to a false capacitance value under low frequency range. The contribution of 1/R term decreases as frequency term ω increases.

This explains the difference between the planar devices and etched foil devices. Etched aluminum foils provided large area enhancement, and thus resulted in more defects than planar devices. As R was compromised, the false capacitance value contributed by the 1/R term is larger than planar devices, which is why a more evidential drop in capacitance density for etched foil devices.

4.3.5 TiN as a top electrode

The conductivity of deposited TiN with thickness of 30 nm is around 6.5×10^4 S/m, much higher than the conductivity of PEDT used, which is around 1.4×10^3 S/m. Aluminum electrolytic capacitors with TiN cathode are thus expected to have much lower ESR and better properties.

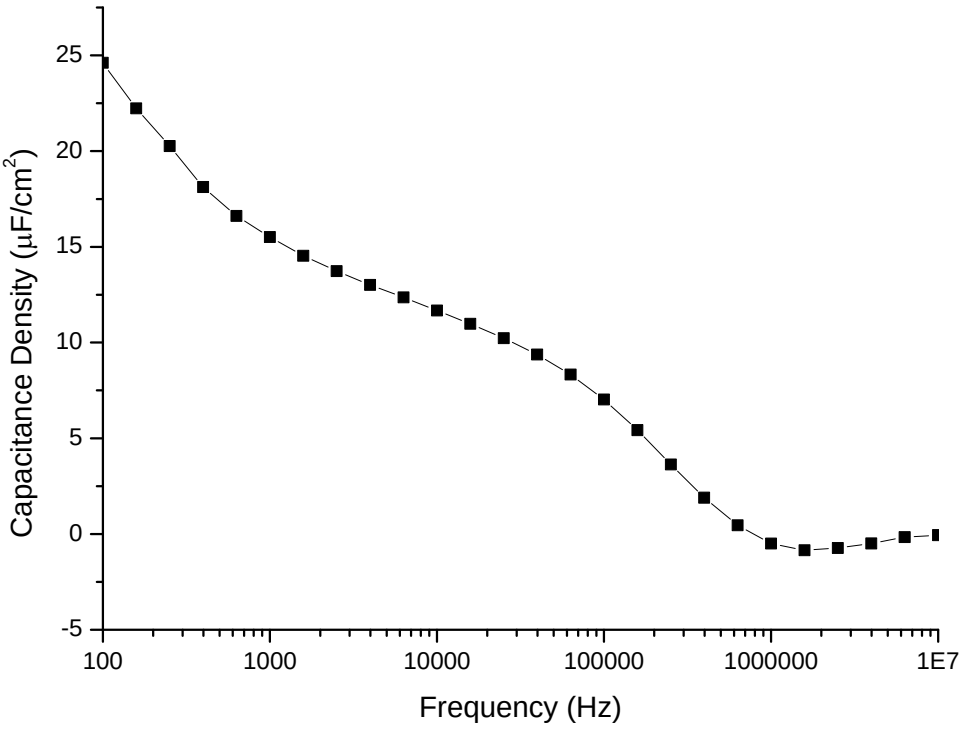


Figure 4. 14 Frequency dependence of devices with TiN top electrode

Samples with TiN top electrode were also characterized using an impedance analyzer at 0V bias. Figure 4. 14 shows the frequency dependence of a device. The capacitance

density is continuously decreasing over frequency range starting from 100 Hz, and drops to zero at around 800 kHz. Impedance spectroscopy showed strong frequency dependence in 100 – 1000 Hz as well as 0.1 – 1 MHz range.

As discussed in the last section, frequency dependence in 100 – 1000 Hz range is due to defective dielectrics. The fact that TiN top electrode does not have a self-healing mechanism adds to this effect.

For high frequency range 0.1 – 1 MHz, the effect of defective dielectric can be neglected. In high frequency range, impedance of the structure is given as:

$$Z^* = R + j\omega L + \frac{1}{j\omega C}$$

The absolute value of the impedance:

$$|Z| = \sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}$$

At low frequencies, as R and L are small values due to the nature of the capacitor, 1/ωC term dominates. As frequency approaches the resonance frequency, ωL gets larger and the contribution of the inductance and capacitance approaches zero. At the resonance frequency, the only contribution to impedance is the R term, and the impedance reaches a minimum.

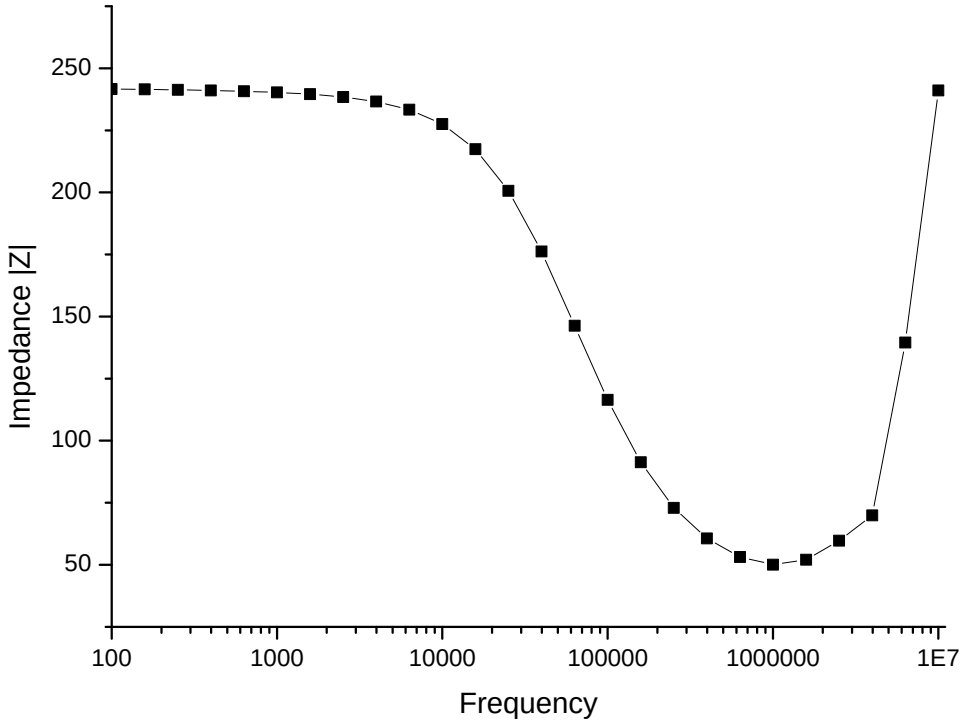


Figure 4. 15 Impedance magnitude vs. frequency for etched foil device with ALD TiN top electrode

The impedance magnitude vs. frequency for the same device shown in Figure 4. 14 is given in Figure 4. 15. The minimum at 1 MHz indicates resonance. Thus the strong frequency dependence for frequency range 0.1 – 1 MHz should be attributed to ESR as well as ESL of the device and testing structures combined.

4.3.6 Electroless metal as the top electrode

Electroless plating of palladium was studied as an alternative to conducting polymer and TiN top electrodes. A lift-off process was added during palladium electroless plating, yielding well defined features, as can be observed in the optical image (Figure 4. 16). Similar patterning step was employed for etched foils, as described in the experimental procedures.

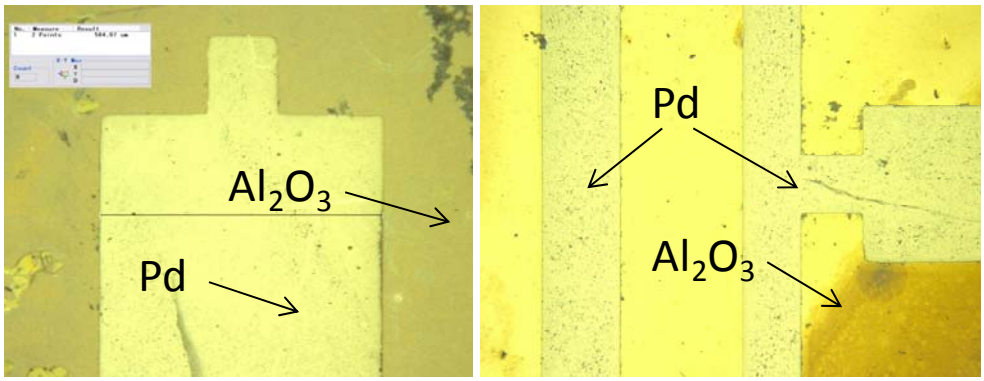


Figure 4. 16 Optical images of patterned Pd on planar alumina film using lift-off process

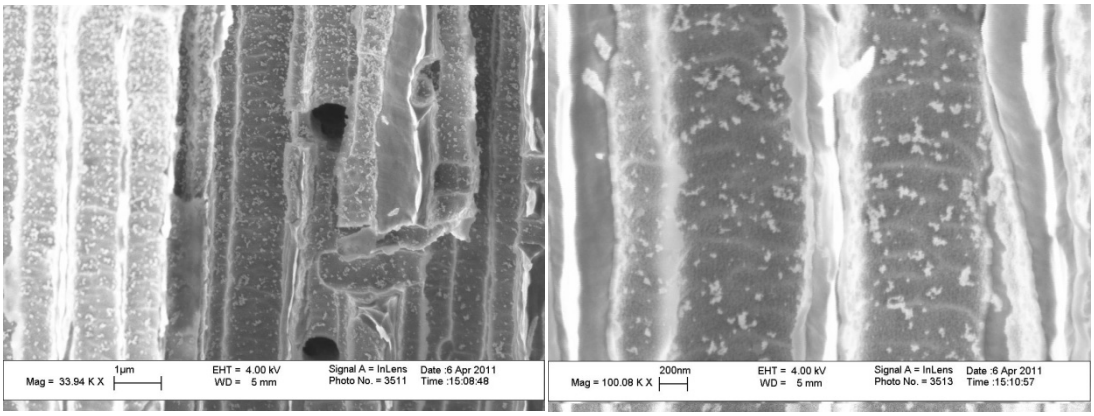


Figure 4. 17 SEM cross sections of electroless palladium plated foils

SEM cross-section images did not show a complete coverage of palladium in the trenches (Figure 4. 17). Spots of Pd deposition on the walls of trenches can be observed. The spots refer to the deposition of palladium before excessive deposition at the opening of the trench closed the gap and prevented further deposition, also known as the pinch-off effect. EDS results in Figure 4. 18 also confirm palladium signal in the middle of the trench but the signal intensity was smaller inside the trench than that on the surface. This suggests that the conditioner and conductor bath were able to access the sidewalls of the trench, but the slower kinetics and pinch-off prevents a full coverage of Pd in the trenches. Attempts to lower the deposition temperature and concentration of the deposition bath did not show any evidential improvement.

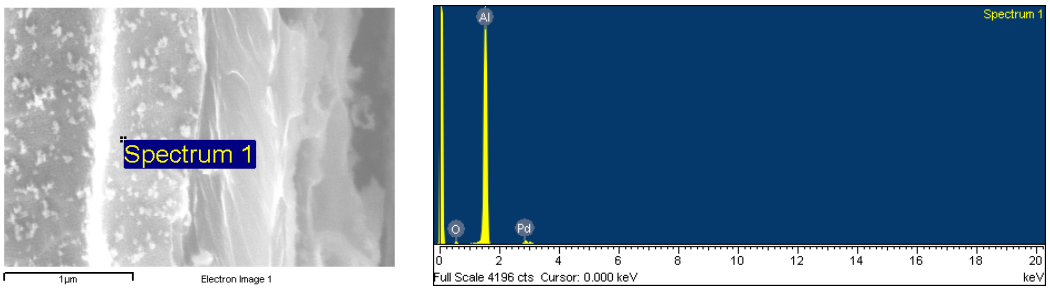


Figure 4. 18 EDS results in the middle of the trench

Accessing more surface areas using inhibitors

It is reported [52] that electroless nickel can access the bottom of channels with aspect ratio of more than 40 using a bottom-up trench filling process by electroless plating with an inhibitor. With a thick dielectric layer before the Ni trench filling, Su-Jeong Suh et al. [52] obtained a low capacitance density of 0.22µF/cm^2. The inhibitor (e.g. Polyethylene Glycol, also known as PEG) passivates the top part of the trench and prevents excessive plating. The additional bath of PEG thus acts as an inhibitor for electroless Pd seed layer (Figure 4. 19).

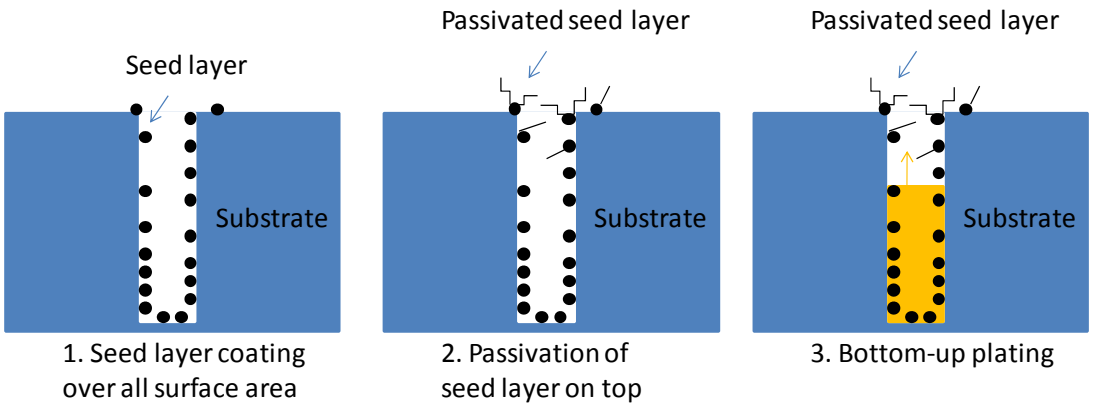
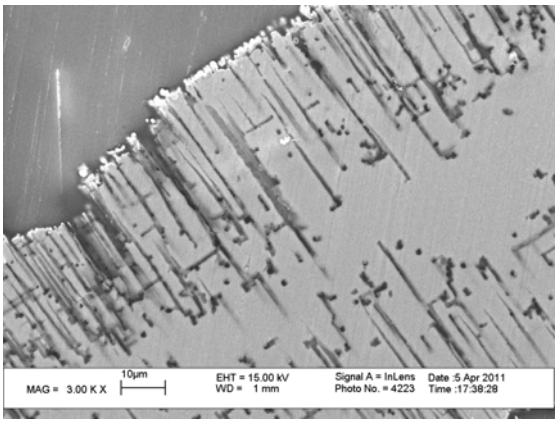
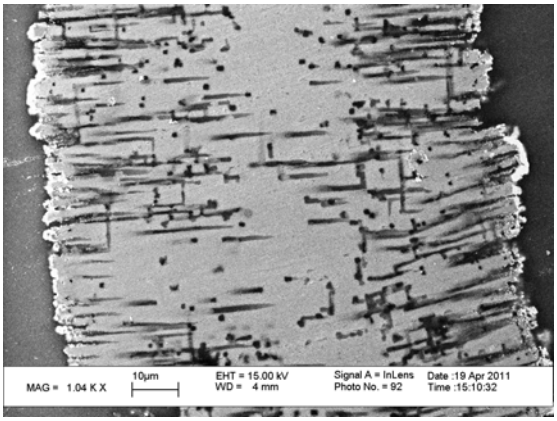


Figure 4. 19 Schematic of bottom-up trench filling using PEG as seed layer inhibitor

As shown in Figure 4. 20, after the conductor bath, a seed layer of palladium covers the surface throughout the trench. The PEG bath enables passivation of the seed layer particles on the surfaces and top part of the trenches by linking to the palladium particles. In the palladium deposition bath, plating will then start from the bottom part of the trench, resulting in a bottom-up trench filling, breaking bonds between PEG and the seed layer as the plating front proceeds.



(a) Electroless Pd with lower concentration



(b) Electroless Pd with PEG 12000 as an inhibitor

Figure 4. 20 SEM cross-sections of electroless palladium

When PEG 12000 (molecular weight) was used as an inhibitor, no evidential improvement in the depth accessed by electroless palladium was observed, as shown

in 0. According to literature [52], the most effective inhibitor was PEG 4000 for full-filling of trenches with electroless Ni. PEG 4000 was therefore used in the subsequent experiment, which did not help the improvement of coverage either. This could be due to the very narrow channels in the current etched foils, or because palladium seed layers require a different inhibitor.

Test measurements on the planar test structure with Pd as top electrode showed capacitance density of around 0.13μF/cm^2 with leakage current of around 4.4μA/cm^2 for a few good devices, although the yield was not high. This suggests that electroless baths may have caused possible damage of oxide layer in the process. It is believed that by using dilute solutions during various dipping steps for Pd plating, coupled with shorter deposition time would help the yield.

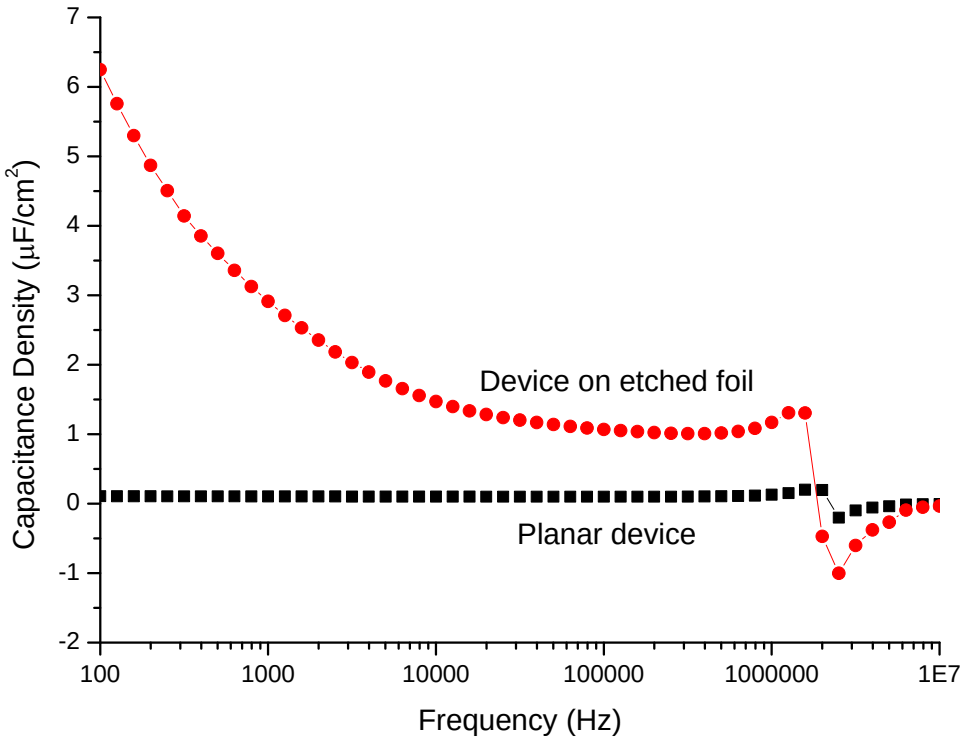


Figure 4. 21 Frequency dependence of capacitance densities for devices with Pd top electrode

Impedance analyzer measurement of electroless palladium samples were also carried out at 0V. As can be seen from Figure 4. 21, capacitance of planar devices with Pd top electrode was very stable around 0.1μF/cm^2 till the resonant frequency of 2 MHz. For device on foil, on the other hand, that was not the case. The reason for the dependence in etched-foil capacitors from 100 Hz to 10,000 Hz was again attributed to defective dielectric as a result of area enhancement. The capacitance density between 10 kHz - 100 kHz is around 1.25μF/cm^2. The spike at 1.5 MHz represents the resonance frequency from the cable and probe parasitic and device capacitance.

More process optimization is expected to enhance the electrode coverage and achieve higher capacitance densities, while maintaining lower ESR with improved frequency response compared to conducting polymers which suffer from high ESR. For electroless metal top electrodes, no self-healing mechanism exists. Combined with possible damage of electroless bath solutions to the oxide film, electroless plated top electrodes present major challenges. Novel counter electrode materials and architectures are needed to address this problem.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

Long-term strategic needs for thin and small power modules require capacitance densities of over 40μF/cm^2, operating voltages above 10 volts, 60 - 100 microns in thickness and leakage current of less than 0.1μA/μF. Existing capacitor technologies such as MLCCs have limited volumetric efficiency, while tantalum capacitors cannot easily be thinned down to less than 100 microns. On the other hand, silicon-based trench capacitors are fabricated with expensive tools and processes, and do not provide enough capacitance density. Two routes were pursued to address these challenges for high-capacitance-density and low-cost thin film capacitors.

5.1 Solution derived TSV capacitors

A novel conformal solution-coating process on silicon trenches was explored as an alternative to CVD and ALD technologies. Solution-derived Lanthanum Nickel Oxide electrodes and PZT dielectrics were demonstrated to enable such an all-solution trench capacitor technology. Anti-ferroelectric PLZT was used to address the limitations of PZT in attaining high capacitance density at high voltages and leakage currents. The properties of all-solution capacitors were comparable to those with platinum electrodes. By modifying the PZT composition to PLZT, anti-ferroelectric characteristics with peak capacitance at 6 - 7 V was demonstrated. In order to demonstrate the feasibility of conformal sol-gel coatings, TSV structures were fabricated using photolithography and DRIE. The conformality of vacuum infiltrated coatings was verified with SEM cross section. A proof-of-concept of solution-derived TSV capacitor was thus provided.

Recommendations

1) **Characterization of precursor solutions.** For sol-gel synthesis, the short

shelf-life of precursor solutions is a major challenge for low-cost manufacturing. Degraded precursor solutions cause defects that can degrade the yield and scalability of devices to larger areas. The exposure to air could hydrolyze the precursors because of its reaction with moisture. Particle size measurement using laser diffraction analyzers can confirm premature gel formation which can result in degraded thin films. FT-IR is an effective technique to provide proof of evidence for the alteration in the solution chemistry due to the hydrolysis.

2) **Conformal deposition of insulating layer between LNO and silicon.** Silicon is known to degrade electrical performance, which is why dielectric liners are deposited in vias of silicon interposers. A vacuum-infiltrated sol-gel ZrO_2 layer between LNO and silicon is expected to address this problem.

5.2 Novel electrodes for aluminum electrolytic capacitors

In the second part of the thesis, etched aluminum foils were explored for package-compatible thin film embedded capacitors. After anodization, conducting polymers are usually applied as the top electrodes to provide the essential attributes such as conformality and self-healing. However, the key challenges with these electrodes are their relatively high ESR and thermal instability which limits the application of aluminum electrolytic capacitors to a frequency range of up to 10 MHz and temperatures of less than 250˚C.

Electroless metal approach was pursued as an alternative to address the ESR challenge with conducting polymer electrodes. However, the conformality with electroless plating is not adequate. When combined with a plating inhibitor such as PEG (polyethylene glycol), electroless plating could result in conformal side-wall coating and trench filling [52]. Preliminary experiments with plating inhibitor showed marginal improvements in conformality. With further adjustment of inhibitor molecular size and the process flow, superior conformality can be achieved. For

palladium electrodes, alternate inhibitors may be required and needs to be further explored.

Recommendation

1) Leakage control. Higher leakage is found in devices with metal electrodes than those with conducting polymer electrodes. To control leakage current, aluminum foils with higher purity may be needed so as to avoid degradation of leakage properties from the contamination in the foil. A balance between implementing impurities for the etching of foils and purer film for anodization needs to be found. Alternative electrolytes for anodization need to be explored for the formation of oxide films with better quality. Use of top electrode with self-healing mechanism could be an alternative to solve this problem.

2) Hybrid top electrode formation. To address the high ESR problem as well as maintain a self-healing top electrode, a hybrid top electrode is proposed. In the proposed approach, a thin layer of conducting polymer is deposited directly on the oxide to enable self-healing mechanism and protect the oxide layer from possible damage caused by the electroless metal baths. Electroless trench filling is carried out subsequently, for the formation of an extremely low ESR electrode. All issues regarding the electroless metal process are addressed in this approach, yielding a low-ESR, self-healing electrode for aluminum electrolytic capacitors.

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