# ASSESSING THE PERFORMANCE AND RELIABILITY OF GALLIUM NITRIDE BASED ELECTRONICS VIA OPTICAL AND ELECTRICAL METHODS

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Georges Pavlidis

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# ASSESSING THE PERFORMANCE AND RELIABILITY OF GALLIUM NITRIDE BASED ELECTRONICS VIA OPTICAL AND ELECTRICAL METHODS

Approved by:

Dr. Samuel Graham, Advisor
School of Mechanical Engineering
*Georgia Institute of Technology*

Dr. Satish Kumar
School of Mechanical Engineering
*Georgia Institute of Technology*

Dr. Eric Heller
Materials and Manufacturing Directorate
*Airforce Research Laboratory*

Dr. Shyh-Chiang Shen
School of Electrical and Computer Engineering
*Georgia Institute of Technology*

Dr. Peter Hesketh
School of Mechanical Engineering
*Georgia Institute of Technology*

Dr. John D. Cressler
School of Electrical and Computer Engineering
*Georgia Institute of Technology*

Date Approved: April 5th, 2018

[To the graduate students of the Georgia Institute of Technology]

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# NOMENCLATURE

| | |
|---|---|
| AL | AlGaN Buffer Transition Layer |
| CCD | Charge-coupled Device |
| G | Gate |
| D | Drain |
| EL | Electroluminescence |
| FEM | Finite Element Method |
| GaN | Gallium Nitride |
| GRT | Gate Resistance Thermometry |
| HEMT | High Electron Mobility Transistor |
| IPA | Isopropyl Alcohol |
| LED | Light-emitting Diode |
| MTTF | Mean Time To Failure |
| NA | Numerical Aperture |
| $P_{diss}$ | Power Dissipated |
| RF | Radio Frequency |
| S | Source |
| SL | Superlattice Transition Layer |
| TLM | Transmission Line Measurement |

| | |
|---|---|
| TSEP | Temperature Sensitive Electric Parameters |
| TTI | Transient Thermoreflectance Imaging |
| $T_{base}$ | Baseplate Temperature |
| $V_{ds}$ | Drain Source Voltage |
| $V_{gs}$ | Gate Source Voltage |
| $\Delta T$ | Temperature Rise |

# SUMMARY

Gallium nitride (GaN) based electronics have shown great potential for RF devices and power electronics. Its superior material properties have enabled the fabrication of high frequency and high voltage devices. Under high power operational conditions, significant localized Joule heating occurs near the drain side edge of the gate which can have detrimental effects on the device. The quantification of performance parameters such as the gate junction temperature is thus necessary to accurately assess the device's quality and lifetime. Until now Raman thermometry has shown to be the most accurate method to estimate the junction temperature. This method, however, is limited to a point measurement and sometimes may be limited by its optical access. Furthermore, the ability to monitor the transient temperature rise under pulsed conditions has not been yet fully developed. This thesis presents advanced methods for *in-situ* transient temperature measurements, using gate resistance thermometry, and temperature mappings across GaN based electronics via transient thermoreflectance imaging (TTI). A combination of experimental and numerical analysis is used to achieve this. The methods are applied to lateral HEMTs, vertical PIN diodes and cross sectional HEMTs. The limitations of the current techniques are discussed and contrasted.

# CHAPTER 1. INTRODUCTION

## 1.1 Background and Motivation

Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) have proven to have great potential for RF devices and power electronics [1]. Compared to GaAs based devices, GaN has a higher break down voltage (10 times greater than silicon [2]), higher power densities [3] and lower on-resistance [4]. These attractive features have pushed GaN based electronics to the forefront of developing high power RF electronics for communications such as base stations, satellites, and for radar applications [5]. In the area of power electronics, currently lateral GaN HEMTs are being developed on Si substrates in order to lower the cost for inverters and converters for battery chargers in electronics, industrial motor controllers, and automotive or aircraft applications [6]. For the case of RF and power HEMTs, a similar geometry as shown in Figure 1 is utilized where different parameters such as the electrode spacing, GaN thickness, and buffer layers are varied to maximize performance. However, in both cases, temperature related concerns arise when biasing the device. In normally on HEMTs, at high drain bias and negative gate bias conditions, electrons are accelerated locally between the gate and the drain and dissipate thermal energy in the region of high electric field at the edge of the gate [7]. The thermal energy from electrons is primarily dissipated through the emission of longitudinal optical (LO) phonons [8] which remain in the active region until they convert into other vibrations to be able to transport the Joule heating [9]. This results in significant localized Joule heating near the drain side edge of the gate (Figure 1) which can have detrimental effects on the device such as metal contact degradation [10] and hot electron induced trap

generation [11]. The generated heat is often dissipated by spreading through the GaN layer and diffusing across the interfacial layers required for heteroepitaxial growth and then into the growth substrate [12]. This makes the dissipation of heat very complicated due to the impact of dislocations near the GaN interface on thermal transport [13], the impact of interfacial layers [14], and the device substrate as well as the stresses induced in the device which can also lead to degradation [15].

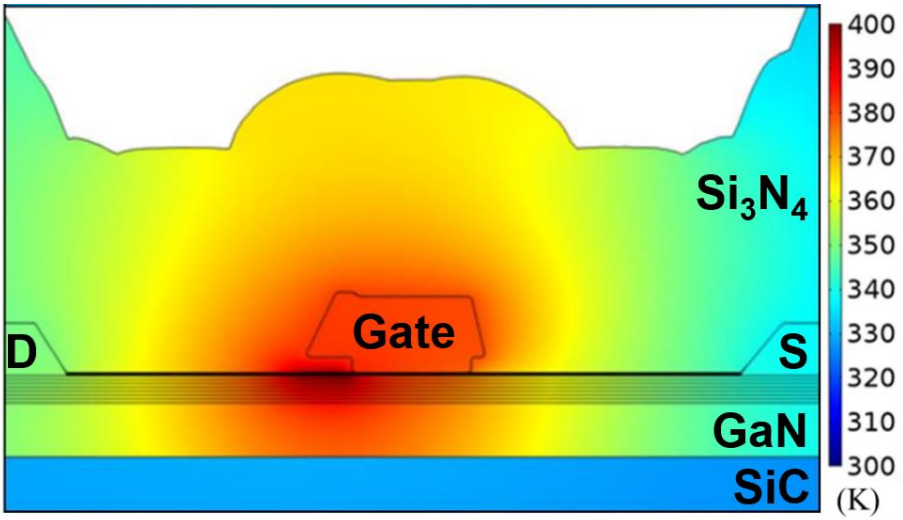



**Figure 1: Hotspot formation in GaN HEMT (adapted from [7]).**

In more recent technology developments, the creation of vertical GaN devices are especially appealing for power electronics [16]. The use of vertical devices will allow the creation of efficient high voltage and high power switches which are needed to advance the state of power electronics [17]. While the development of these devices is in their infancy, the understanding of thermal effects in vertical GaN devices is a relatively unexplored topics and necessary due to its potential impact on device reliability. Overall, several methods have been developed to monitor and characterize the lateral temperature distribution across a device. These established methods are suitable for lateral devices such

as GaN HEMTs where the path of heat travels horizontally through the device (Figure 2a). The transition to fabricating devices on GaN substrates removes the necessity for buffer layers enabling vertical devices where the path of current flow and heat will travel predominantly in the vertical direction (Figure 2b). New characterization techniques must therefore be established to understand the temperature distribution across vertical devices such as PIN diodes.

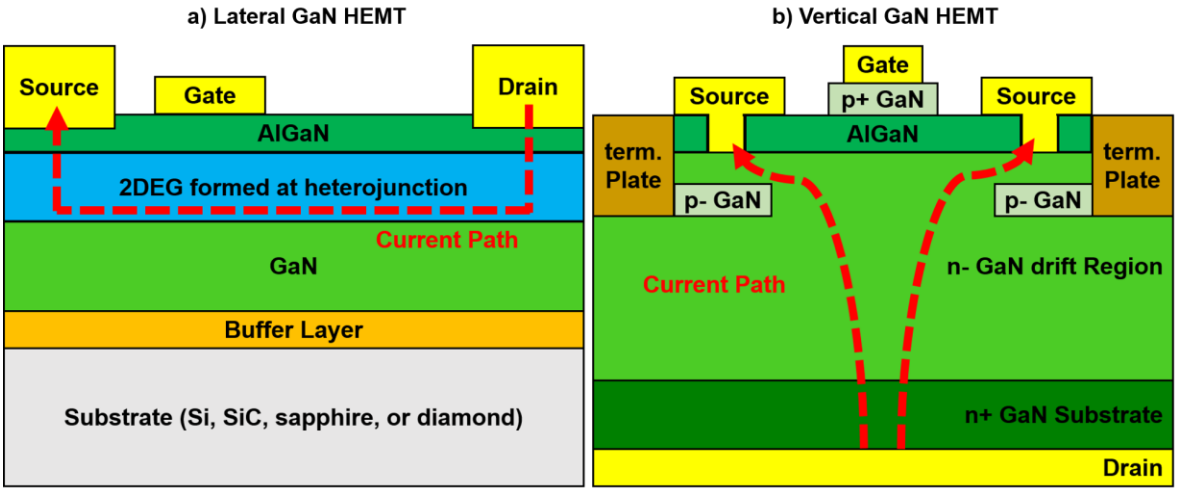



**Figure 2: Current path in a) Lateral GaN HEMT and b) Vertical GaN HEMTs.**

Upon review of previous technology such as Si and GaAs, the thermal time constants associated with the materials were estimated to be on the order of tens of microseconds or longer [18]. In contrast, the thermal time constants associated with GaN have been measured to be on the order of microseconds [19]. Additionally, GaN is typically grown on a Si or SiC substrate with very different thermal diffusivity, unlike Si and GaAs for discrete power FETs. To obtain the full potential out of these devices, understanding and controlling the device's transient thermal dynamics is important to characterizing the nanoscale thermal transport [20, 21]. Accurately predicting the device temperature during biasing is thus necessary for predicting the device's lifetime and reliability [22, 23].

Currently, several thermometry techniques have been developed to estimate the peak temperature (Figure 3) which include IR Thermography [24], Raman Spectroscopy [25], and Gate Resistance Thermometry [26]. However, there are several issues that are seen in the application of accurate thermometry methods to GaN devices, especially lateral and vertical structures in combination with transient operation, which must still be addressed. There is also a desire to understand the vertical temperature gradients in these devices which is often not measured by current techniques [27]. Some of these techniques are reviewed in the next sections and their specific challenges for application to temporal measurements of temperature in GaN devices are explained.

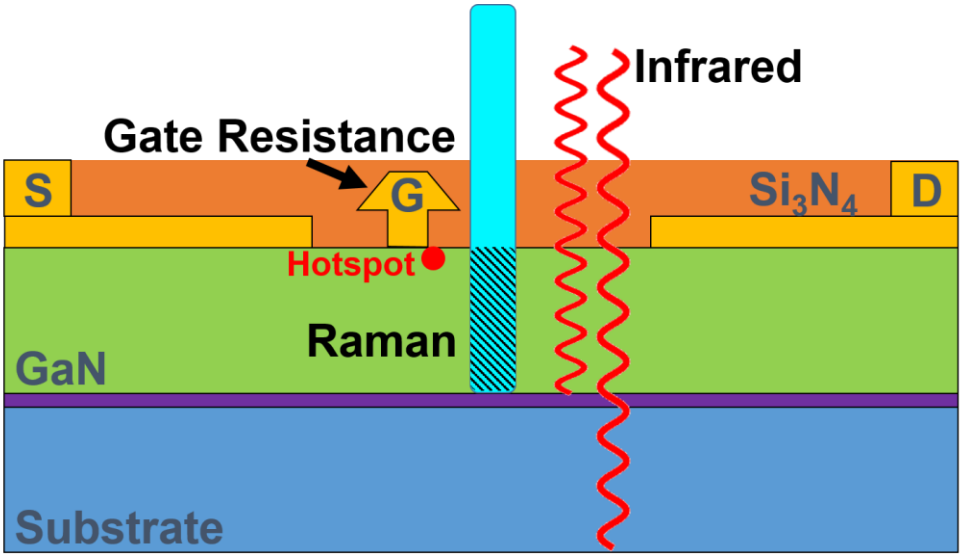



**Figure 3: Schematic of different thermometry techniques for lateral GaN devices.**

## 1.2 Review of Thermometry Techniques

### *1.2.1 IR Thermography*

One of the most commonly utilized methods for measuring the temperature in electronics is Infrared (IR) thermography [28-30]. A CCD is used to detect the change in

emitted radiation in the infrared range from a surface. Since IR wavelengths are transparent to most wideband gap materials, the radiation detected will originate from the multiple layers present and thus be a convolution of the temperature rise across all layers and possibly the layers underneath the device (Figure 3). Consequently for GaN electronics, the inability to monitor the change in radiation in the GaN layer has shown to greatly under predict the junction temperature [31, 32]. Performing calibrations to measure the change in radiation of metal is possible in spite of its low emissivity, but due to the technique's low lateral resolution (~10 μm), it is very difficult to capture the temperature rise across the gate metal which is closest to the localized Joule heating. In addition to its limited spatial resolution, transient IR thermal imaging has only been achieved on the millisecond restricting itself from being able to monitor the temperature of devices under normal pulsed biasing conditions [33, 34].

### *1.2.2 Thermo-Sensitive Electrical Parameters*

Another method that can be used in the measurement of electrical devices are characteristics of the electrical response that are temperature sensitive. By monitoring the temperature dependence of electrical characteristics in semiconductor devices such as voltage [35] or current [36], thermo-sensitive electrical parameters (TSEP) can be extracted to estimate the device temperature rise. A common example is the use of the forward voltage temperature measurement in LEDs for junction temperature assessment [37]. In general, the advantage of using TSEPs is the minimal addition of equipment required to conduct the measurement, the operation of the electronic device and its response itself is used as a temperature sensor [38]. Requiring no optical access or material deposition, TSEPs provide a low-cost option for estimating the device temperature rise. Specifically,

for HEMTs, several different DC I-V characteristics have been employed to measure temperature. Using Schottky diode forward characteristics, the gate-diode forward resistance and threshold voltage have been found to have a linear temperature dependence [39]. Similarly, monitoring the change in saturated drain current has also shown to be used to estimate the channel temperature (McAlister's method in Figure 4 [40]). While these techniques have been found to give a quick approximation of the channel temperature, significant error has been found to be associated with the degradation of the Schottky barrier during operation and current collapse. Furthermore, when performing DC measurements, the device must be switched briefly off to perform the IV sweeps. This method limits these DC characterization techniques from performing *in-situ* measurements. Further studies, using Pulsed-IV, have shown to shorten these acquisition times to sub-microseconds when attempting to monitor the change in ON-resistance and drain current [41]. These methods, however, still incur and error associated with fast switching and leakage currents.

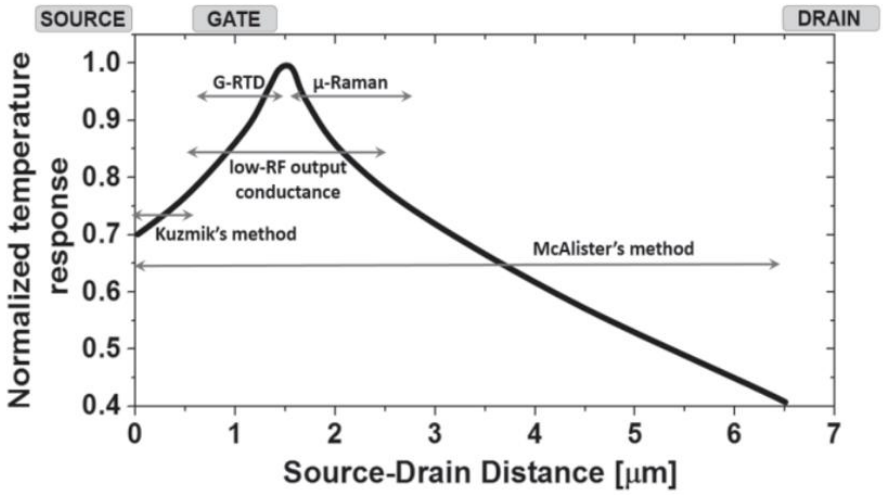



**Figure 4: Comparison of location of TSEPs across GaN HEMT [42].**

An electrical method that has shown the potential to estimate the channel temperature rise in HEMTs is the monitoring of the gate end-to-end resistance [43]. Using a 4-point setup, the resistance of the gate metal has shown to be strongly linearly dependent with temperature [44]. Previous work using Gate Resistance Thermometry (GRT) under DC biasing has been applied to single finger AlGaN/GaN-on-Si HEMTs [45] as well as GaAs pHEMTs [46, 47]. It has been suggested that GRT tends to under predict the junction temperature when a large temperature gradient exists across the channel [48]. The effects of bias conditions and device geometry on the accuracy of estimating the channel peak temperature have not yet been fully investigated. Altering the drain bias can impact the electric field distribution and consequently change the area of localized Joule heating. Elongating the gate width may develop larger temperature gradient along the device [49, 50]. Overall, there is a need to verify the accuracy of GRT and understand exactly the origin of the temperature rise it captures. In addition to being able to conduct this technique without having to switch off the device, the technique also has the potential to transiently monitor the channel temperature [51] which could then be used to characterize the device's transient thermal dynamics.

### *1.2.3 Raman Thermometry*

Of the thermal techniques most widely applied to GaN HEMTs is the use of Raman thermography [25, 52, 53]. Raman thermography can be used to estimate the temperature rise in HEMTs by tracking the temperature dependent peak position of Raman active phonon modes [54]. This technique requires specialized equipment including a monochromatic laser, sensitive CCD and most of all it requires optical access to probe crystalline Raman active materials. Due to the fact, the hotspot is predicted to be in the

GaN, Raman Spectroscopy has proven to estimate accurately the temperature change in the GaN. Either the GaN $E_2$(high) or $A_1$(LO) phonon modes can be used [55]. The phonon frequency, however, is also dependent on stress and thus, errors in temperature measurements can arise due to thermoelastic stresses that occur during operation when using a single phonon mode [56]. To address this problem, it is possible to measure both the shift in the $E_2$ (high) and A1 (LO) mode peak positions to decouple stress and temperature effects [56]. To avoid self-heating sub band gap lasers are typically used to measure the Raman shift in GaN. The Raman temperature shift therefore measures a volumetric average across the depth (tens of microns) of the GaN layer (Figure 3) with approximately a 1 μm diameter in the lateral direction. If thick GaN layers are present in the device, the Raman volumetric averaged temperature will not capture the temperature gradient across the GaN and will result in under predicting the hotspot temperature. Few studies have shown the applicability of UV Raman to capture the surface temperature rise in the GaN [57, 58] but this method may result in exciting electrons into the channel which can affect the electrical performance of the device. Another drawback to using Raman Spectroscopy is its limitation due to optical access. The 'hot spot' is typically formed underneath and near the edge of the gate. Raman Spectroscopy is not able to directly probe the desired area unless probed from the back side of the device. Employing a back-side measurement, however, removes the possibility of any heat-sinking effect which would be present during normal operation.

While Raman thermometry has proven to have high spatial resolution compared to TSEPs the technique requires long acquisition periods (several minutes) which makes it unfavorable for temperature mappings [59]. Furthermore, regarding its temporal

resolution, Raman thermometry has shown to capability to capture temperature rises on the order of microseconds during continuous pulsed biasing [60]. This fine time resolution permits thermal time constants to be extracted for a device to understand and better model the device's transient thermal dynamics [61]. The ability to capture both a mapping and transient temperature rise across the device however is not possible with Raman. Developing a technique to achieve this will allow for better thermal characterization of devices providing validation when attempting to build accurate numerical models.

Overall, current Raman thermometry studies have shown its suitability for lateral devices where the path of heat follows the current and travels horizontally through the device (Figure 2a). The transition to fabricating devices on GaN substrates removes the necessity for buffer layers enabling vertical devices where the path of heat will travel predominantly in the vertical direction (Figure 2b) [16].

New methods of using Raman thermometry must therefore be established to understand the temperature distribution across vertical devices such as PIN diodes. Recent developments in Raman surface thermometry using nanoparticles such as diamond [62] or $TiO_2$ [63] permit temperature measurements of non-crystalline surfaces such as the top metal plates of vertical devices to be conducted. While a depth mapping is not possible unless the laser wavelength used is transparent to all the different layers [64], further research is necessary to fully characterize the heat dissipation through vertical devices.

### *1.2.4 Thermoreflectance*

While Raman thermometry and TSEPs have been used frequently over the past decade, no single acquisition temperature mapping technique has yet been fully developed

apart from IR thermometry which the drawbacks have been already discussed. In a manner similar to temperature dependent electrical parameters, temperature dependent optical properties can also be used to quantify temperature in electronics. Recent studies have shown the feasibility of measuring the change in the optical reflectance (thermoreflectance) of the gate metal in HEMTs to monitor the temperature rise in devices [65]. Thermoreflectance is typically used in a pump probe setup known as Time Domain Thermoreflectance (TDTR) in which thermal properties of different materials are extracted [66]. Replacing the photodiode detector with a CCD, thermoreflectance can be used as a thermal imaging tool to monitor the change in thermoreflectance of every pixel in the CCD. To estimate the surface temperature rise, ΔT, via Thermoreflectance Transient Imaging (TTI) the correct thermoreflectance coefficient, $C_{th}$, must be applied to the thermally induced optical reflectivity variation detected, ΔR, as shown in the equation:

$$\Delta T = C_{th} \times \frac{\Delta R}{R} \tag{1}$$

The $C_{th}$ is both material and excitation source wavelength dependent [67]. With the addition of passivation layers, the $C_{th}$ of GaN and the gate metal can change significantly [68, 69] leading to significant errors in the estimated temperature rise via TTI.

The accuracy of this technique is thus based on how well the thermoreflectance coefficient, $C_{th}$, of the surface studied can be estimated. Due to thermal expansion effects, using a thermal stage and a thermocouple to determine the thermoreflectance coefficient can introduce error in the measurement of reflectivity. Previous studies have used a combination of electro-thermal modelling and Raman thermometry to adjust the

thermoreflectance coefficient of the metal to match the expected results [65, 70, 71]. While this methodology for validating transient thermoreflectance is accurate, the procedure requires additional complex equipment and long acquisition times. With recent advancements in the development of transient thermoreflectance imaging (TTI) technology, a piezoelectric stage can be used to account for thermal expansion during the extraction the thermoreflectance coefficient [72].

## 1.3 Research Objectives

The thermography methods discussed in the previous sections show that several techniques have been employed to thermally characterize GaN HEMTs and vertical GaN electronics. Although some techniques have been extensively studied, there are clear shortcomings in trying to provide both high resolution temporal measurements as well as temperature gradient information that can exist in these structures. Often time, such information is obtained through electro-thermal numerical modeling of the devices with limited validation from experiments [73]. Regarding the monitoring of the gate resistance, until now this technique has not been proven to be used as a true in-situ measurement. The device typically must be briefly switched off to avoid any impact of leakage current on the temperature estimation. Furthermore, the technique has shown the potential to transiently monitor the channel temperature under pulsed biasing but has so far only been proven to obtain a time resolution on the order of milliseconds.

In contrast Raman thermometry, has been shown to be an ideal candidate for DC measurements when there are no optical barriers restricting access to the region next to the hot spot such as a field plate. Some extensions to high temporal resolution transient analysis

have been pioneered [60, 61] but this has not been widely adopted. In addition to optical restriction, Raman thermometry is also limited to a spectral point measurement and requires multiple acquisitions to plot a temperature mapping of a device. Comparing its time-resolved capabilities, it can detect temperature changes in the microsecond regime but requires several accumulations making it a time averaged technique instead of *in-situ* and does not provide a full field analysis of temperature.

To address need for high spatial and temporal resolution thermal measurements, thermoreflectance imaging is a potential solution where a pixel by pixel map is acquired during every measurement. Until now, this technique has only been applied to monitoring the surface temperature rise of unpassivated metal. To find a solution to monitor both the temperature rise in the GaN channel region as well as passivated metal requires a better understanding of the effects of thin film interference on the thermoreflectance coefficient. For vertical temperature gradients, the use of nanoparticles on the surface of GaN devices may allow measurement of the GaN surface temperature along with the average temperature in GaN. Vertical gradients in AlGaN LEDs have shown the potential of doing this [74] but this was done based on tracking the Raman signatures of different materials in the LED. By using Raman active nanoparticles added to the device, it may be possible to perform a similar characterization in both vertical and lateral GaN devices.

The primary research objectives of this work are:

• To develop experimental thermal metrology methods that can accurately measure the in-situ transient temperature rise in GaN based electronics under high frequency pulsed biasing and map the temperature distribution across the device both laterally and vertically.

• To develop an electrical characterization method to determine the channel temperature in GaN HEMTs by continuous monitoring the gate metal resistance (Gate Resistance Thermometry).

• To implement gate resistance thermometry under RF operating conditions and determine any differences in the device thermal performance when compared to DC operation.

• To determine the applicability of transient thermoreflectance imaging for transient thermal measurements in GaN HEMTs, exploring both the gate metal and GaN channel regions.

• To investigate the use of Raman active nanoparticles for the characterization of vertical temperature gradients in GaN devices such GaN Si HEMTs with thick buffer layers.

• To establish a method to thermally map the Joule heating profile across GaN HEMTs using transient thermoreflectance imaging and show the bias dependence on the Joule heating profile.

• To investigate the effects of thin film interference on thermoreflectance imaging and determine the suitability of this technique for fully passivated devices and devices multiple thin film layers such as superlattices.

### 1.4 Dissertation Outline

The present work aims to address the mentioned problems in the following chapters. Chapter 2 discusses the development and verification of gate resistance thermometry (GRT) for both steady state and transient analysis. The errors associated with

the technique are investigated. Chapter 3 highlights the applicability of GRT to GaN/Si HEMTs showing for the first-time gate temperature measurements under RF operating conditions. A direct comparison between the junction temperature achieved via DC and RF operation is presented. Chapter 4 explains the development of advanced optical techniques used for thermometry of GaN based electronics. First the development of Raman active nanoparticles for surface temperature measurements is discussed and its accuracy is verified. Subsequently, a detailed analysis of transient thermoreflectance imaging (TTI) is conducted and its accuracy is verified via GRT. Chapter 5 demonstrates the first ever thermoreflectance imaging of a cross sectional GaN/SiC HEMTs showing the effect of bias conditions on Joule heating. The challenges with measuring the vertical temperature gradient in GaN PIN diodes is also presented. Chapter 6 focuses on quantifying the effects of thin film interference on TTI's accuracy and demonstrates the applicability of TTI to benchmark the thermal performance of GaN/Si HEMTs with strain engineered layers. Chapter 7 discusses the applicability of Raman active nanoparticles and TTI to assess the vertical temperature gradient in GaN/Si HEMTs with thick buffer layers and compare their thermal performance to HEMTs with locally removed Si substrate. The techniques are used to quantify the thermal penalty when removing the substrate and assess the viability of additional thin film layers to improve the thermal performance.

# CHAPTER 2. GATE RESISTANCE THERMOMETRY FOR ALGAN/GAN HEMTS

Content in this chapter (figures and text) adapted from:

1. Pavlidis, G., *et al.*, "Characterization of AlGaN/GaN HEMTs Using Gate Resistance Thermometry," IEEE Transactions on Electron Devices, vol. 64, pp. 78-83, Jan 2017. [26]

## 2.1 Overview and Approach

This chapter introduces the gate resistance thermometry (GRT) technique developed for GaN HEMTs. This method provides a fast and low-cost technique to determine the average temperature of the gate metal. Previous attempts to use electrical methods for thermometry show significant differences in temperature rises measured with different techniques [48]. However, GRT is the most desirable of the electrical methods, if it can be shown to be accurate. The initial feasibility of this technique has been applied to single finger AlGaN/GaN HEMTs. Particular focus is given on verifying the technique's accuracy technique via other experimental methods (Raman) and numerical simulations. The viability is of this technique under different modes of operation (DC and pulsed biasing) is presented and the errors associated with the measurements are quantified.

### *2.1.1 Experimental Setup and Calibration*

Six finger AlGaN/GaN-on-SiC HEMTs were tested and modelled with two different gate widths, 370 μm and 1000 μm. As shown in Figure 5, ground-signal-ground probes connected to bias tees with the RF signal routed to 50 Ohm terminations were used to make

electrical contact with the devices. All power sourcing and electrical measurements were conducted with a Keithley 2410 SMU for biasing the gate and a 2425 SMU for biasing the drain where high current and high voltage are needed. Four terminal sensing was used to measure the gate resistance over a single finger (see Figure 6a). A probe current, $i_p$, was supplied through a metal pad to one end of the finger and was returned directly to the SMU. The voltage drop, $\Delta V$, was then measured across the finger by the additional two pads. All measurements were conducted using a Keithley SMU controlled digitally by the software Test Script Builder.

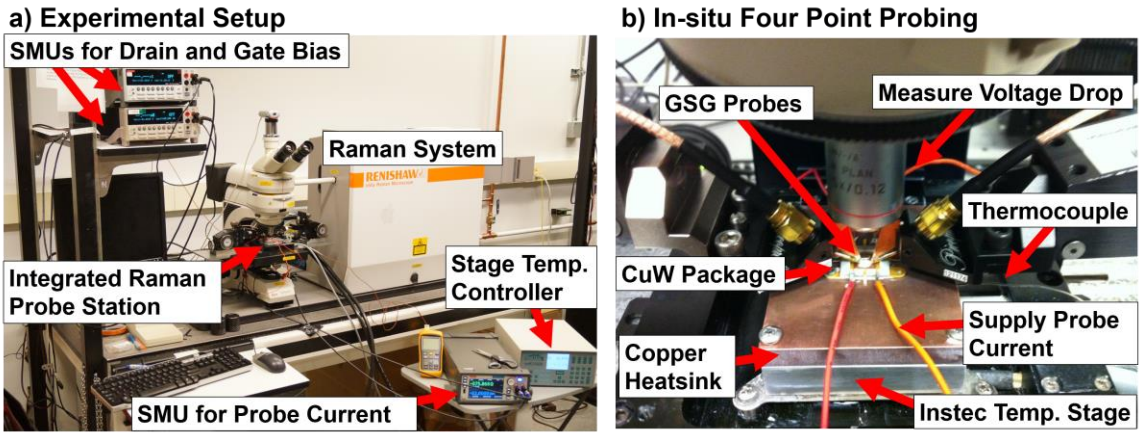



**Figure 5: a) Overview of experimental setup designed for the verification of Gate Resistance Thermometry (GRT) b) Detailed description of different parts used to perform GRT simultaneously to biasing the device.**

To estimate the uncertainty of the measurement, an average of 50 measurements over a time period of 3.4 seconds was conducted at each powering condition. A calibration was performed prior to measuring the Gate Resistance to ensure a consistent relationship between gate resistance and temperature for each device. Resistance was measured at fixed temperatures between 30 - 120 °C which was controlled by a thermal stage (Instec HCP302 shown in Figure 5b). Calibrations were performed on four different devices for both gate

widths. The TCR was estimated to be in between 0.28-0.31 %/K for both devices. To obtain a more accurate representation of the device temperature, a thermocouple was placed below the Stratedge LPA580274 CuW package where the device was attached using Ag-epoxy (H20E). Linear regression was applied to determine the slope between resistance and temperature that was then used to estimate the gate temperature (see Figure 6b). Uncertainty analysis was performed to estimate the error of the slope.

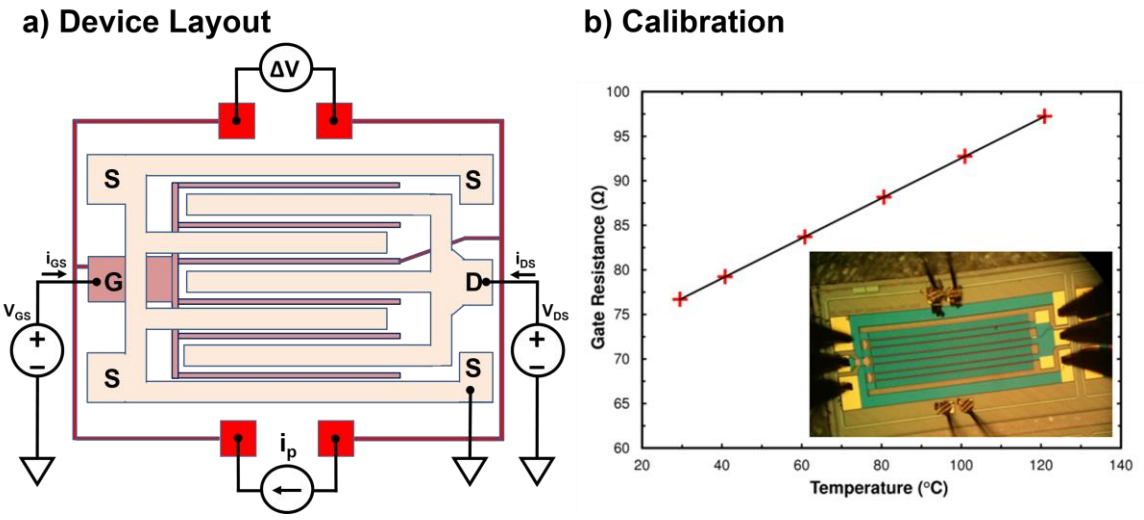



**Figure 6: a) Device layout and configuration of four terminal sensing to measure the gate resistance over a single finger for 6 finger devices with gate widths of 370 µm and 1000 µm. b) Linear calibration fit used to measure the thermal response of the gate metal resistance of a 6 x 1000 µm device for a temperature range of 30 to 120 °C.**

### *2.1.2 Experimental Validation*

Micro-Raman spectroscopy was performed using a Renishaw InVia Raman microscope with a 0.25 m focal length spectrometer and a 488 nm laser as the excitation source. The laser beam diameter was approximated to be 1 µm. The use of sub-band gap laser wavelengths prevented localized heating of the GaN and $TiO_2$ by laser light absorption. A charge coupled device (CCD) camera was integrated into the system to

image the collected Raman signals. Experiments were carried out with the laser light perpendicular to the basal plane of GaN in a 180° backscattering configuration and unpolarized detection with a 100X objective. A 3000 l/mm grating was used with a slit width of 65 μm for all measurements. To estimate the uncertainty in the temperature measurements with 95% confidence intervals, an average of at least 20 measurements was made at all power conditions.

The measurement steps for the Raman thermometry measurements were done with the temperature controlled stage set at 303 K. Silicone thermal grease was used between the backside of the package and the thermal stage to reduce the interface thermal resistance. The resulting Raman spectrum was analyzed with a Gaussian-Lorentzian (Voigt) fit to find peak parameters of the Stokes peaks of GaN and $TiO_2$. For GaN, the temperature of the devices was estimated using the two-peak fit method [56]. For $TiO_2$, the $E_g$ phonon frequency was measured at fixed temperatures between 303 and 393 K. Raman measurements were taken at the middle of the center finger with the center of the Raman laser 1 μm away from the gate edge as shown in Figure 7 (edge of the beam 0.5 μm away from gate). For a direct comparison between the two experimental techniques, the gate resistance was recorded simultaneously with the Raman measurements at various power densities.

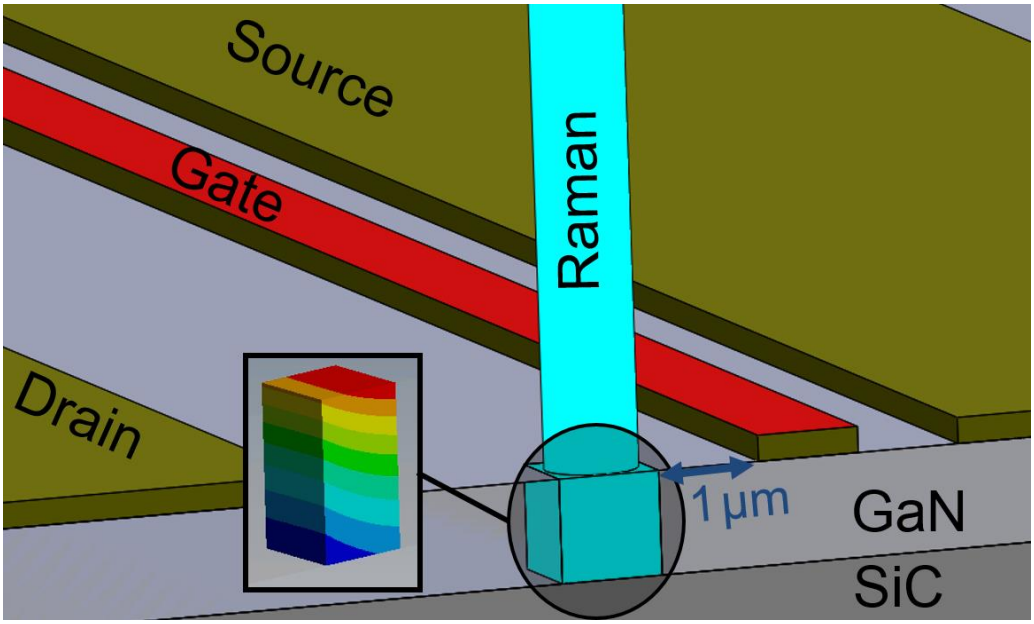



**Figure 7: Schematic of layer configuration implemented in the 3D FEM thermal model including the SiC substrate. The gate resistance probed area is highlighted in red while the GaN probed volume is circled in black.**

### *2.1.3 Numerical Validation*

A 3D finite element model was developed using ANSYS to model the heat dissipation throughout the devices. A schematic of the different material layers included in the model is shown in Figure 7. Applying quarter symmetry, the material properties of the different layers including temperature dependent thermal conductivities were taken from [75] and shown in Table. To ensure close approximation of the device structure, channel dimensions were determined from optical microscope images. The gate-to-drain spacing was measured to be 4.5 µm while the gate-to-source spacing was set to 1 µm. The gate was modelled as a rectangle with nominal length of 1 µm.

**Table 1 Temperature dependent thermal conductivities applied to initial model. Taken from [75].**

| Material | Thermal Conductivity (W/m-K) |
|---|---|
| GaN | $150 * \left(\frac{T}{300}\right)^{-1.4}$ |
| SiC | $387 * \left(\frac{T}{293}\right)^{-1.49}$ |
| Cu | 387 |
| CuW | $204 - 0.0251 * T - 0.0000762 * T^2$ |
| AuSn Solder | 57 |
| Thermal Paste | 0.757 |

Under high drain bias operation conditions with a negative gate bias such that the device is nearly pinched off, the temperature distribution across the channel from source to drain is known to be asymmetric due to localized Joule heating mostly occurring in the depletion region and requiring the need for electro-thermal simulations [9]. In contrast, if the gate is opened fully so that the channel is not significantly modulated by the additional gate bias, Joule heating will then be much more uniform over the entire channel from source to drain without a significant depletion region [76]. Even though the devices had a T-gate configuration, the gate metal layers were modelled as a rectangle with nominal length of 1 μm. Since the model was created to simulate fully open channel conditions, the temperature distribution across the gate length will be parabolic and therefore the effect of the gate structure will be minimal. Based on the channel length, constant heat fluxes were applied to an area of 6.5 μm by the gate width. The bottom face of the CuW package was

constrained to 303 K to simulate a constant thermal stage temperature applied during the experiments. All other boundaries were assumed adiabatic.

Since GRT provides a surface average temperature while Raman provides a volume average temperature, different analysis regions were defined in the model in order to extract temperatures that could be compared to the experimental results obtained from Raman and GRT (Figure 7). When performing Raman Spectroscopy, a volumetric average across the depth of the GaN layer (1.8 μm) is probed with an approximated laser diameter of 1 μm. A cube of 1 x 1 x 1.8 μm was therefore created to model the Raman probed temperature. The gate resistance represented an average over the full cross section of the gate metallization and was thus modelled as a 1 μm long rectangle across the gate width.

The packaging of the devices required the addition of multiple layers other than the GaN and SiC layer. This includes the silver epoxy material, thermal paste, CuW package and mounting plate. To avoid rough approximations of these layers, an effective thermal resistance was applied below the SiC layer to represent the effect of combining these layers. This value was determined by varying the effective thermal resistance and matching the measured and calculated gate resistance and Raman temperatures for a single operating condition. This value was then held constant for all other predictions of temperature versus power response of the device. The passivation layer was not included in the model. The minimum difference between the average temperatures measured by the $TiO_2$ particles to the gate resistance temperatures, showed an insignificant temperature gradient across the passivation layer.

## 2.2 Steady State Analysis

### *2.2.1 Fully Open Channel*

The devices were operated under fully open channel conditions by applying a positive gate bias between 1 and 2 volts. To ensure a fully open channel, the gate current, $I_{gs}$, was maintained at approximately 0.12 mA for each power density. The experimental results obtained for the 370 µm gate width device are shown in Figure 8 and are compared to the numerical model.

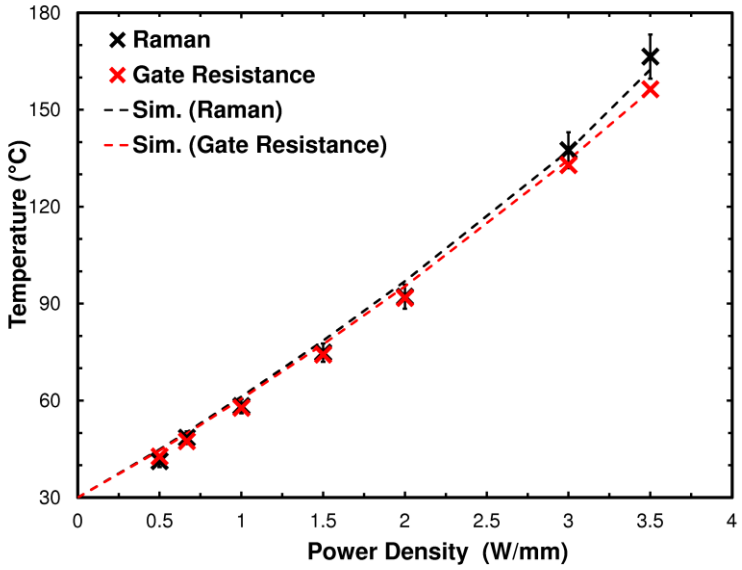



**Figure 8: Comparison of Raman (Black) and GRT (Red) measured temperatures to respective FEM probed temperatures for 6 x 370 µm devices at power densities up to 3.5 W/mm.**

Good agreement was shown between the GRT and Raman data for power densities from 0.5 – 3.5 W/mm. The close agreement of the numerical and experimental data at different power densities validates the implementation of the effective resistance. The data also shows that for the majority of the power densities studied, the GRT and Raman values are very similar, in spite of one being a volume average and one being a surface average

temperature. At higher power densities (e.g., greater than 3 W/mm), the Raman temperature is shown to be higher than the GRT measured temperature. A maximum difference of 10 °C (6 %) is shown for the power densities tested, and this is expected to increase as the power density increases.

The numerical solutions exhibit a similar trend with the Raman numerical temperature shown to be 2 °C higher than the GRT numerical solution. As shown in Figure 7, the location of the probed Raman temperature and the GRT temperature can explain the higher temperatures obtained by Raman. A constant heat flux applied across the channel creates a parabolic temperature profile between the source and the drain and between the ends of the device channel (Figure 9).

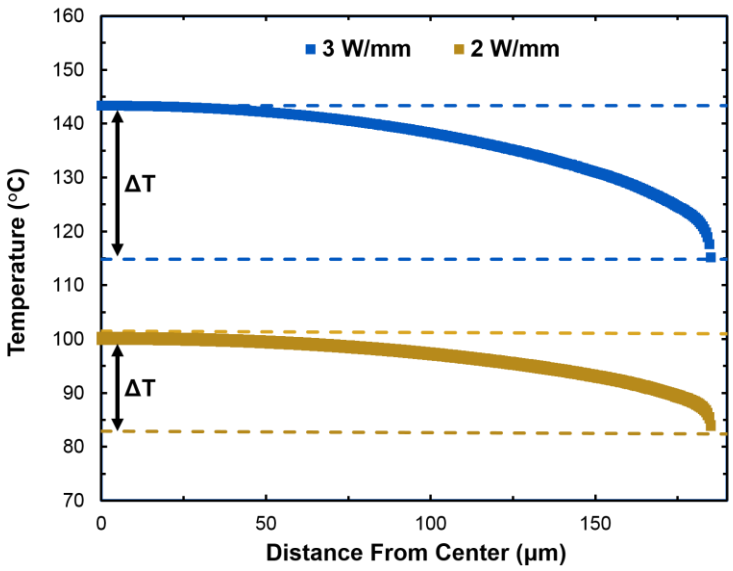



**Figure 9: FEM temperature distribution from the center of the gate finger to the edge of the 6 x 370 µm device. The temperature difference at 3 W/mm (blue) results in a larger temperature difference, ΔT, when compared to the 2 W/mm (gold) powering condition.**

Due to the Raman probed temperature being located closer to the center of the parabolic profile; a higher temperature is measured during operation as opposed to the

average across the surface of the parabolic profile. When increasing the power density as shown in Figure 9, the difference between these two temperatures is magnified and more distinguishable. To further validate this comparison, measurements and simulations were performed on devices with a gate width of 1000 μm. The elongation of the gate width limited the possibility of operating the device to power densities greater than 1 W/mm which was previously possible with the 370 μm wide gate. Similar to the results shown in Figure 8 the temperatures measured using GRT and Raman were again in excellent agreement. The difference between the two metrics is however expected to increase at higher powering conditions where the temperature difference between the center and edge of the channel becomes more significant.

### *2.2.2 High Drain Bias Operation*

To further investigate the applicability of GRT for estimating the gate channel temperature at more representative operational bias conditions, the devices were operated at drain biases of 28 V and 48 V with the gate not fully opened. The results for both the 370 μm and 1000 μm wide devices at 28 V drain bias are shown in Figure 10. At low power densities, the two techniques appear to estimate similar temperatures. For the 370 μm wide devices, a maximum difference of 4.7 °C (6 %)at 1.33 W/mm was observed. For the 1000 μm wide devices at the same power density, this difference increased to 9.5 °C (11 %). Thus, we achieve similar temperatures, but as noted, the difference between the two methods increases as the power density increases. For both types of devices, a quadratic relationship between the power density and temperature is observed with the Raman fitted trend lines having slightly greater gradients than the GRT trend lines for each device respectively.

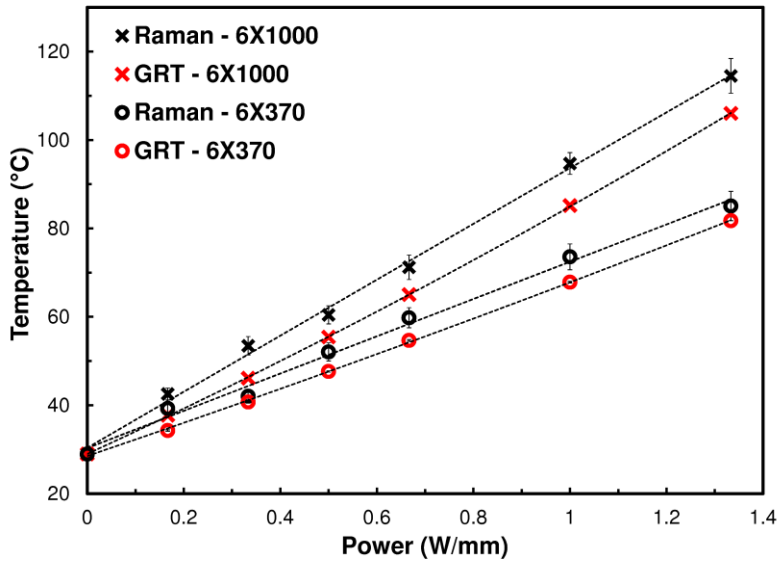
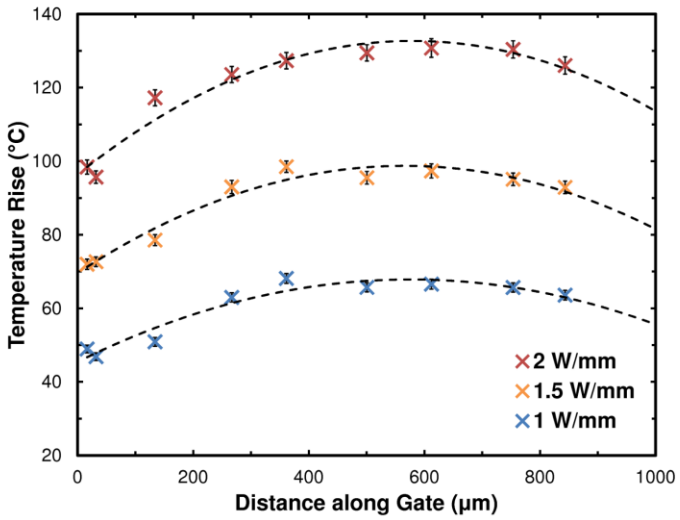



**Figure 10: Comparison of Raman (Black) and GRT (Red) measured temperatures at 28 V drain bias for bot 6 x 370 µm and 1000 µm devices at power densities up to 1.33 W/mm.**

Due to the complex Joule heating profile developed across the channel at high bias conditions, $TiO_2$ nanoparticles were used to measure the surface temperature rise of the gate metal along its width (Figure 11). The applicability of this method will be discussed in Chapter 4. This enabled both a more direct comparison of the GRT estimated temperature with Raman. To directly compare the $TiO_2$ surface temperatures to GRT at 48 V drain bias, second order polynomials were fit to the measured values as shown in Figure 9. An average was then taken across the fitted line to obtain a value that can be compared to the GRT measurements. A maximum difference of 1 °C was found for all three power densities (see Figure 11). The asymmetry of the temperature profile along the gate width shown can be explained by the position of the device on the die. A higher temperature rise is shown on the edge of the device that is closer to the edge of the die whereas the edge which is closer to the center die can dissipate heat more efficiently and thus result in lower temperatures. The possibility that the distribution of the electric field along the gate width

is uneven due to the magnitude of the probe current was neglected but is discussed later on in this Chapter.




| Power Density (W/mm) | Averaged $TiO_2$ (°C) | ± | Gate Resistance (°C) |
|---|---|---|---|
| 1 | 62.6 | 1.2 | 60.2 |
| 1.5 | 92.3 | 1.6 | 94.3 |
| 2 | 130.9 | 2.2 | 130.5 |

**Figure 11: Temperature distributions along the gate width of the 6 x1000 µm device at different power densities using $TiO_2$ nanoparticles to directly measure the gate metal surface temperature. Second order polynomials were fitted to each set of measurements and then averaged to directly compare to GRT values.**

The direct comparison of Raman surface temperature rise to GRT confirms that the technique truly averages across the gate metal surface temperature. In order to estimate the maximum junction temperature however, the accuracy of GRT is thus dependent on the shape of the parabolic temperature profile along the gate width. As power density increases and the peak in the parabolic profile increases, the average temperature across the gate width takes on a value that is lower and deviates from the volume average peak temperature in the center. Since this effect is seen to be more pronounced in the 1000 µm devices as opposed to the 370 µm devices, the impact of device geometry and heat spreading must be accounted for when using the GRT method to estimate the peak temperature in AlGaN/GaN HEMTs. For long gate widths, GRT can therefore be used as a complement

to Raman thermometry, where Raman is used to obtain initial maximum junction temperatures and then a calibration is performed for the GRT measured values. In contrast to Raman thermometry, the GRT method is easier to employ, requiring acquisition times of a few seconds instead of minutes and can be used to monitor the temperature of devices without the need for optical access. Thus, the method has the potential for great utility in monitoring device temperature, as long as the impact of averaging across the channel width is understood and put into proper context.

## 2.3 Transient Thermal Analysis under Pulsed Bias

To obtain the full potential out of these devices, understanding and controlling the device's transient thermal dynamics is necessary for predicting the device's lifetime and reliability. Measuring the device's thermal transient response via the GRT method was investigated by implementing a pulsing method using a Maury AMCAD Pulsed IV system. To measure the voltage drop across the gate finger for the GRT method, a Tektronix DPO3012 Oscilloscope was used. To ensure high accuracy of this technique, the different sources of uncertainty associated with GRT are discussed and quantified in the following section.

### *2.3.1 Effect of Gate Leakage*

An initial attempt to monitor the gate resistance by pulsing both the gate and drain was initially done. As seen in Figure 12, a 500 μs pulse was applied to the drain from 0 to 28 V for a 50% duty cycle. Synchronously, the gate was pulsed from 0 to -2.5 V. Monitoring the transient change in resistance, it was difficult to obtain a consistent gate resistance measurement. When no bias is applied to the gate, the resistance suddenly

dropped and then slowly increased until the gate bias was applied again. This trend would suggest a drop in the gate temperature at the end of the drain pulse and subsequently a slow temperature rise would occur when no power is being dissipated. Since this is not physically possible, this phenomenon highlights that the gate leakage does have a significant effect on the gate resistance measurement during pulsed conditions. When the gate bias is turned on and off, significant gate leakage is injected into the 4 point measurement cause the potential difference measured by the oscilloscope to either over estimate or under predict the resistance for a given probe current.

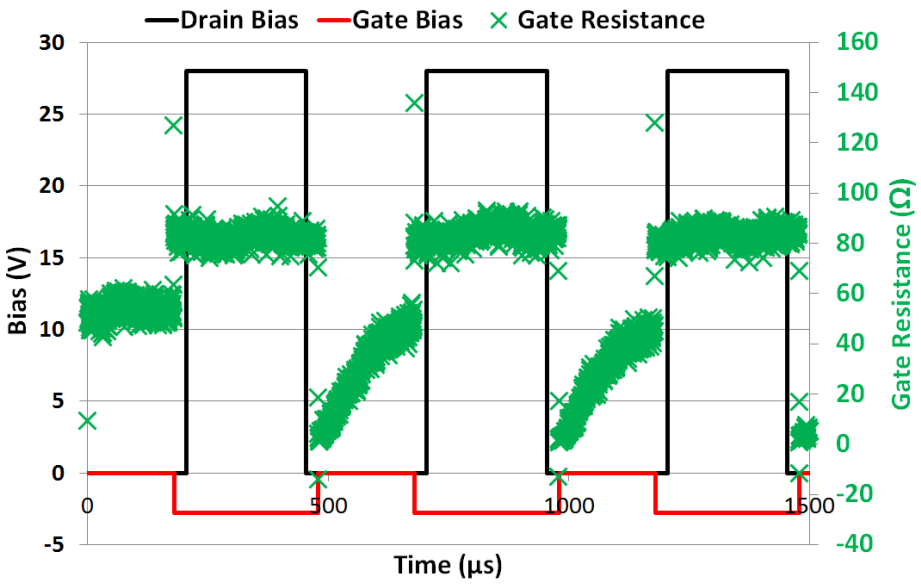



**Figure 12: Attempt to pulse both drain and gate while monitoring the gate resistance.**

For the remainder of this chapter, transient measurements were performed with a constant applied gate bias to enable the accurate measurement of the gate resistance. In the following chapter, the issue of gate leakage current is addressed and a solution is proposed using a peak to peak method.

### *2.3.2 Effect of Probe Current*

The effect of the probe current on the gate resistance was investigated in order to prevent discrepancies between the resistance measured with no bias conditions and during pinch- off ($V_{GS}$ = -6 V & $V_{DS}$ = 20 V) where leakage currents may affect the resistance measured. For steady state measurements, a probe current of 2 mA was found necessary to minimize the impact of biasing the device. This resulted in a probe current to gate leakage ratio of 200:1. Larger probe currents minimize the impact of this source of error, but makes another error source more significant; operating at a significant probe current will result in a large potential difference across the GRT finger (Figure 13). During operation, this additional voltage drop across the gate can affect the electric field distribution across the channel, causing one end of the gate to be more negative than the other and thus altering the path of heat dissipation.

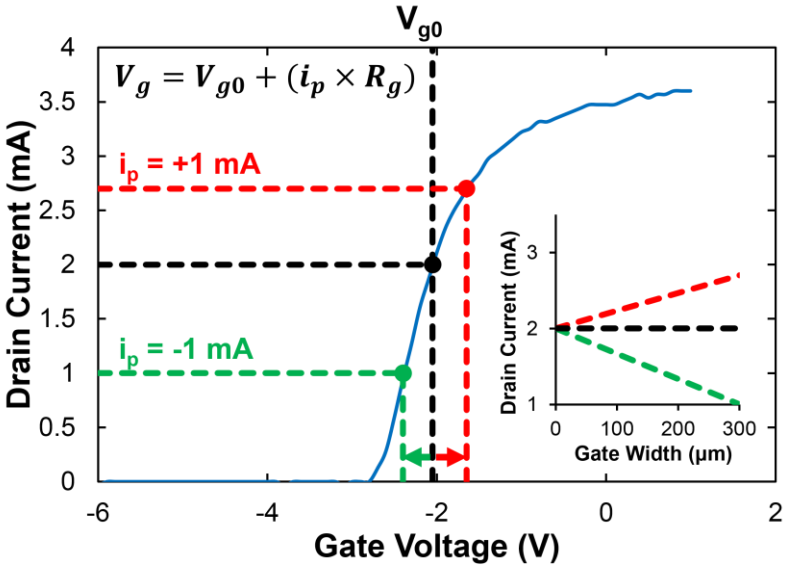



**Figure 13: Effect of probe current's magnitude and direction on drain current, $I_{ds}$. Inset shows $I_{ds}$ distribution along gate when probe current is applied.**

As previously mentioned, the magnitude of the gate leakage significantly impacted the transient gate resistance measurement. The probe current was initially set to 10 mA to temporarily overcome this issue. To determine the effect of the 10 mA probe current on the device operation, IR thermal imaging was used to monitor the temperature distribution across the device. As shown in Figure 14, the temperature profile does indeed alter when increasing the probe current for the gate resistance measurement. The hot spot shifts to the left suggesting the channel is more opened on one end in comparison to the other end. This results in an uneven temperature distribution.

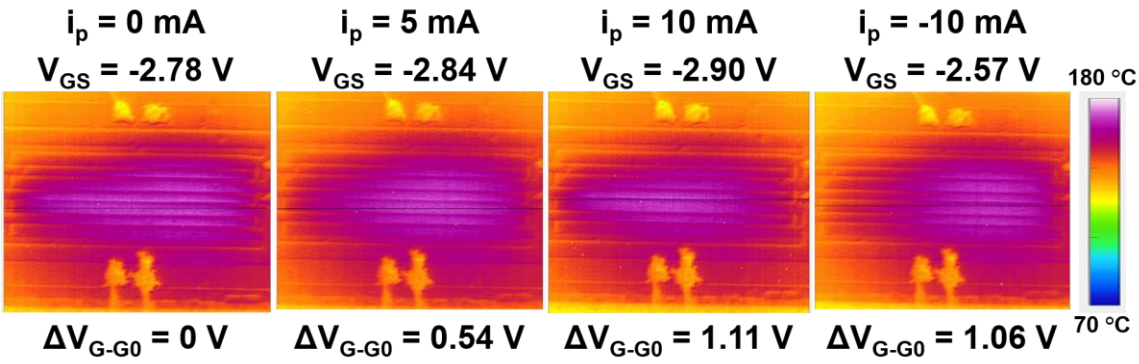



**Figure 14: Effect of probe current on overall thermal distribution. 6x1000 µm GRT devices were biased at 0.8 W/mm.**

It was concluded, for the GRT devices, that a maximum probe current of 2 mA should be supplied when measuring the gate resistance as the temperature profile was minimally different with that obtained with no probe current (Figure 15).

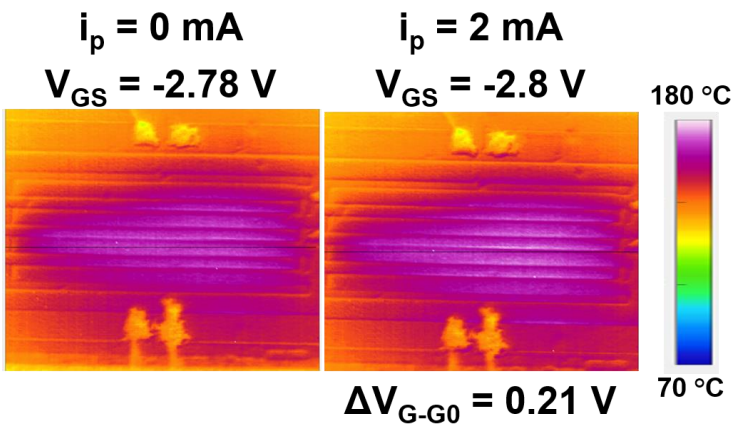



**Figure 15 Effect of 2 mA probe current on thermal distribution was determined minimal and was thus used for the remainder of measurements.**

Having completed IR measurements on the Gate Resistance devices, a comparison of the two techniques was performed. A line probe was taken across the gate finger and 2nd order polynomial was fitted to the temperature profile. Similarly, to Figure 11, an average across the fitted line was taken and compared to the GRT temperature. The results are shown in Table 1. The IR averaged temperatures appear always lower than the GRT temperatures confirming the inaccuracy of IR temperature to estimate the 'hot spot'.

**Table 2 Comparison of GRT to IR thermometry.**

| $I_p$ (mA) | Vgs (V) | GRT (°C) | IR (°C) |
|---|---|---|---|
| 0 | -2.785 | - | 152.7 |
| 2 | -2.8 | 162 | 151.36 |
| 5 | -2.836 | 167 | 154.9 |
| 10 | -2.903 | 174 | 152.96 |

### *2.3.3 Effect of Duty Cycle*

Having quantified the errors associated with the GRT technique, the effect of duty cycle on the device's thermal performance could now be evaluated. Using the pulsed IV system in synchronization with the oscilloscope, the drain duty cycle was varied for a 100 µs period from 10 to 40% (Figure 16a). Initially, 10 V was applied to the drain bias while negative 2.78 V was applied to the gate to result in a peak power density of 3 W/mm. It was immediately observed that the starting absolute resistance value measured by GRT varied with duty cycle. When applying a constant gate voltage of 0 V (Figure 16b), however, this phenomenon was not observed and additionally less noise associated with the measurement. These results show that even with a constant gate bias, a significant gate leakage is injected into the 4-point setup and can significantly alter the potential difference measured by the oscilloscope which translates to an error in the GRT measurement. Holding the gate voltage to 0 V, the effect of the duty can be evaluated.

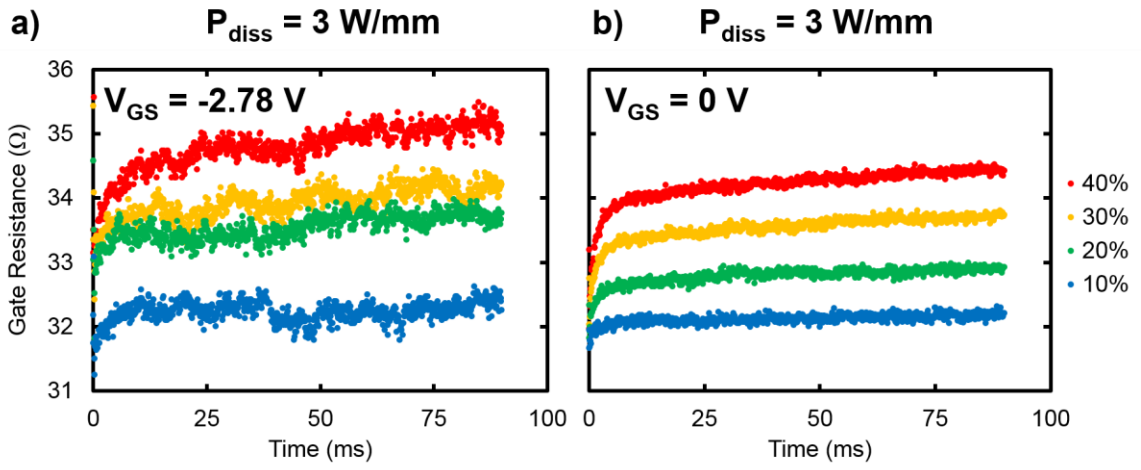



**Figure 16: Transient response of gate resistance for 6x370 µm device under pulsed biasing when a constant gate voltage of a) -2.78 V and b) 0 V is applied. Drain bias was adjusted to match power densities of 3 W/mm.**

Using the device's CTR, the long transient temperature rise of the device can be monitored and is plotted for various duty cycles in Figure 17. Measurements of this type are useful when assessing the average dynamic response of a GaN HEMT under pulsed biasing. A recent study by Bagnall, showed the significance of the device's pseudo step response and how it is possible to extract the multiple time constants associated with a device [61]. This study, however, was performed using transient Raman thermometry where, until now, only an average measurement over multiple pulses can be monitored in contrast to GRT's *in-situ* capabilities. In order to obtain the pseudo step response via Raman, the pulse width is varied for a constant duty cycle <10% and the peak temperature rise is evaluated. Assuming no heat is accumulated at a low duty cycle, the temperature rise is assumed to be equivalent to the pseudo step temperature rise. Lowering the duty cycle down to 1%, a duty cycle lower than 5% is necessary to ensure no significant accumulated heating. Overall, a linear relationship between duty and temperature rise was observed verifying the accuracy of the transient GRT measurement.

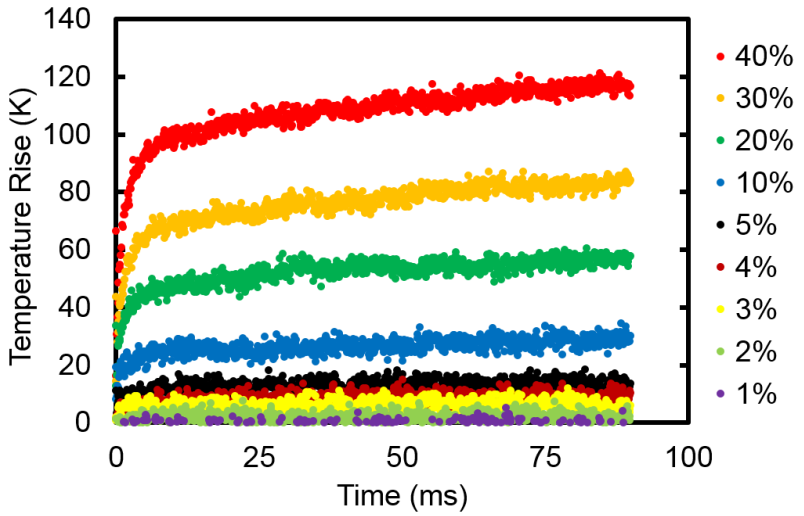



**Figure 17: Transient device temperature response for varying duty cycle at a power density of 3 W/mm.**

After monitoring the temperature rise in the device over a long period of time, an attempt to monitor the effect of a single pulse on the gate resistance was made. It was proven very difficult to capture the initial few pulses when biasing the devices due to the dramatic increase in the average temperature rise. The temperature swing at the steady-state dynamic equilibrium however, could be monitored (see Figure 18). To complete these measurements, the device was pulsed according to the duty cycle and a measurement was taken after the device had reached steady-state. The time of the measurement was determined via the previous analysis of monitoring the transient thermal response over three minutes. During steady state, an average of 256 measurements was taken to accurately capture the temperature swing in the device as shown in Figure 18.

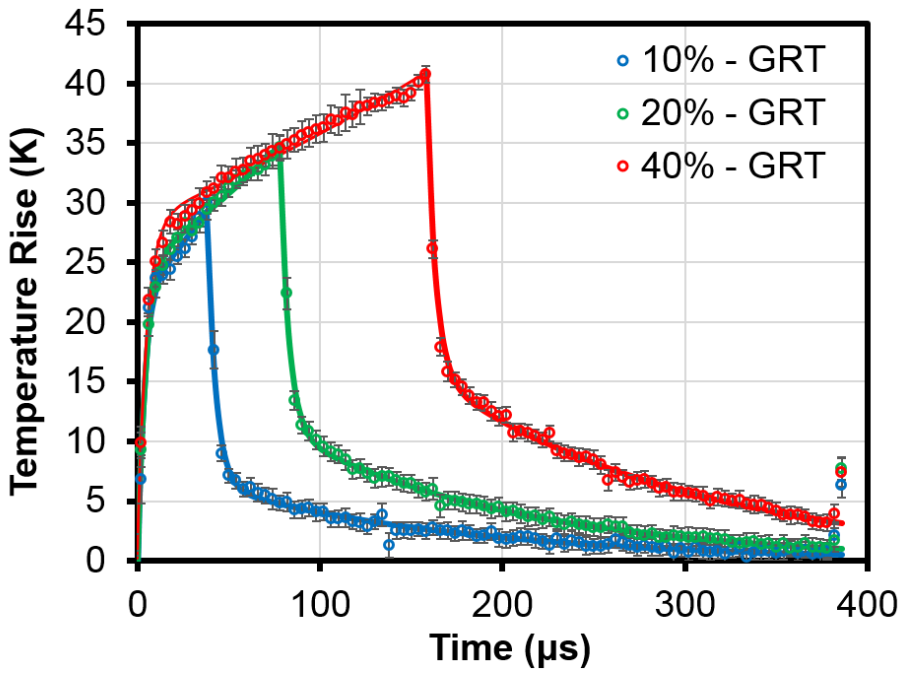



**Figure 18: Transient thermal response of GaN HEMT under various duty cycles.**

Comparing the device's transient response at varying duty cycles in Figure 18, the temperature decay with a 40% duty cycle is shown not to return to its initial temperature at

zero seconds. As previously mentioned, this can be attributed to the significant amount of heat that is not fully removed during the 'off state' period. Converting the GRT temperature rises to absolute values as shown in Figure 19, the base temperature and the peak junction temperature are plotted at different duty cycles. The base temperature represents the temperature at the beginning of the drain pulse while the peak junction temperature represents the temperature at the end of the drain pulse. To directly compare these temperatures to the device's DC thermal performance, the data points were plotted against the average power dissipated. Overall, the base temperature is shown to rise by 26 °C when increasing the duty cycle from 10% to 40%. Comparing this temperature rise to the package temperature rise of 2 °C measured by the thermocouple, indicates that the heating caused under pulsed biasing conditions is primarily dissipated in the die.

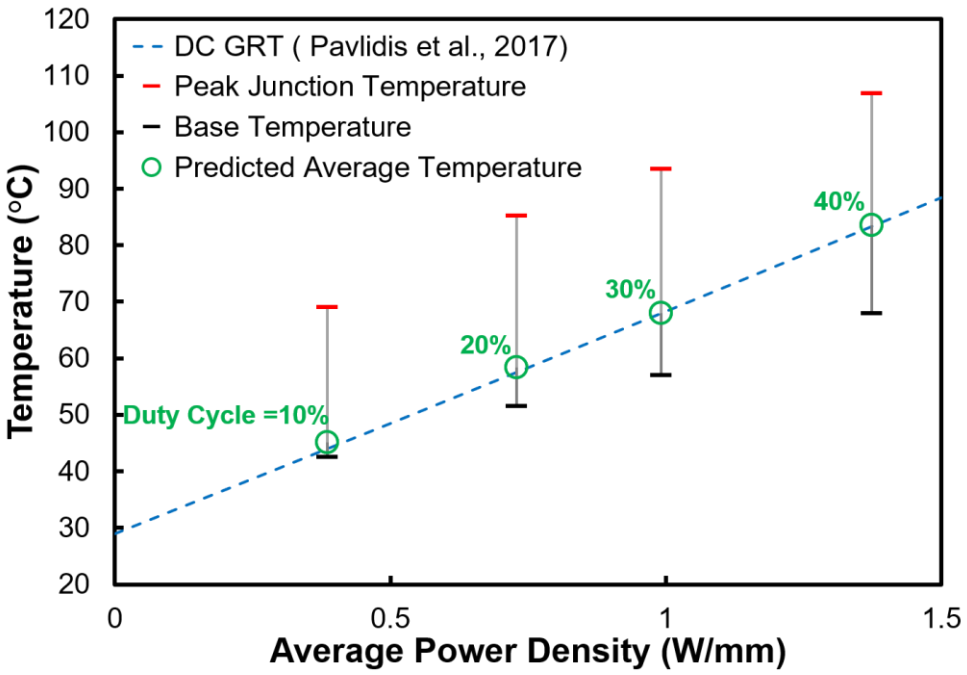



**Figure 19: Absolute base and peak temperature measured by GRT for varying duty cycle from 10% to 40% with a time period of 400 us. A calculated average gate temperature is compared to DC GRT results measured for the same device.**

Using linear interpolation, the average temperature of the gate metal over a pulse can be calculated using the duty cycle applied and the base and peak temperature measured. The results of these averaged temperatures are directly compared in Figure 6 to the GRT measurements previously conducted under DC biasing [26]. The close agreement between these two values for all duty cycles show the potential of using DC GRT, a simpler technique, to estimate the peak temperature under pulsed biasing. Although this DC approach will limit extracting thermal time constants and understanding the device's transient thermal dynamics, it could give a rough estimate of the device's maximum temperature under pulsed biasing.

## 2.4 Summary and Conclusions

Gate Resistance Thermometry (GRT) was used to determine the channel temperature of AlGaN/GaN high electron mobility transistors (HEMTs). Raman thermometry has been used to verify GRT by comparing the channel temperatures measured by both techniques under various bias conditions. To further validate this technique, a thermal finite element model has been developed to model the heat dissipation throughout the devices. Overall this method provides a fast and low-cost technique to determine the average temperature under both steady state and pulsed bias conditions. The errors associated with this technique ae discussed and quantified. When estimating the gate channel temperature, it was found that GRT agreed well with Raman probed temperatures for fully open channel conditions and normal bias conditions at low power densities. It has also been observed that at higher power densities Raman thermometry predicts a higher temperature than GRT. This is due to the large peak temperature in the center of the device versus the surface average across the width of the device, following the shape of the parabolic temperature

profile along the gate width. In comparing the application of the two methods, GRT can be applied to a device with several measurements made within a few seconds while Raman thermometry can take several minutes. Thus, GRT provides very quick probing of the temperature in AlGaN/GaN HEMTs. The results obtained show that GRT is a viable technique for quickly measuring the channel temperature, but with some loss in terms of the ability to sense the true peak temperature at the center of the device. The applicability of using GRT measurements for Pulsed operation has been verified showing promise for monitoring the junction temperature during RF operation.

# CHAPTER 3. COMPARISON OF RF TO DC THERMAL PERFORMANCE IN GAN HEMTS USING GATE RESISTANCE THERMOMETRY

Reliability of gallium nitride (GaN) based electronics is essential for its further commercialization into the high frequency microwave industry. Accelerated lifetime testing is thus performed to predict the device's mean time to failure (MTTF) [22]. The key parameter required for this qualification is the accurate characterization of the peak junction temperature. Under DC biasing, a wide range of thermometry techniques have been conducted to estimate the junction temperature. Primarily due to cost, DC accelerated lifetime testing has also been used to determine MTTF for GaN HEMTs under RF operation. Previous studies have shown, however, that the Joule heating profile is complex and has a high bias dependence [9, 45, 55, 76]. The rapid bias switching under RF operation may consequently result in both different magnitude and position of the peak temperature in comparison to DC operation [22]. Accurate novel thermometry techniques are thus needed to estimate the junction temperature under RF and determine whether the active degradation mechanisms are similar to those under DC operation.

To this date, the thermal performance of GaN HEMTs under RF operation has only been once quantified using Raman thermometry [65]. Without the use of Raman active nanoparticles, however, the technique is optically restricted to measuring the GaN approximately 1 μm away from the gate. Furthermore, the addition of field plates will further elongate the distance of the evaluated temperature from the localized Joule heating near the gate. To obtain a closer temperature to the area of interest, the gate metal

temperature can be directly measured via GRT. This Chapter proves the viability of performing GRT under RF operation and presents the thermal performance of GaN/Si HEMTs in continuous wave (CW) mode. Different effects on the RF thermal performance are investigated such as the gate to gate spacing and the power added efficiency.

## 3.1 Overview and Approach

Using MACOM's manufacturing and processing facilities, AlGaN/GaN HEMTs were grown and fabricated on a silicon substrate. As shown in Figure 20, the GRT design was implemented on a two-finger device with 300 μm gate widths. The gate to gate spacing was varied between 50 and 80 μm. Some devices were packaged on a CuW die using a AuSn die attach. As shown in Figure 20, two different sets of dies were prepared for the different gate pitch devices. The experimental setup necessary for performing GRT measurements consisted of using a four point measurement to monitor the change in resistance of one of the two gates. This required the addition of four extra pads that were extended from both of ends of a single gate. To perform the Kelvin measurement, a probe current, $i_p$, was supplied across the gate finger using a Keysight B2902. The voltage drop across the gate finger was then measured using a differential probe connected to a Keysight oscilloscope.

The replacement of passive probes with a differential probe to monitor the gate end-to-end potential difference was found to improve the accuracy of the resistance measurement by enabling the detection of smaller potentials and remove the effect of gate leakage. In comparison to the passive probe, the active probe tip contains an amplifier that

amplifies the detected signal. The active probe significantly reduces the capacitive loading to achieve higher frequency signal measurements with much better signal fidelity.

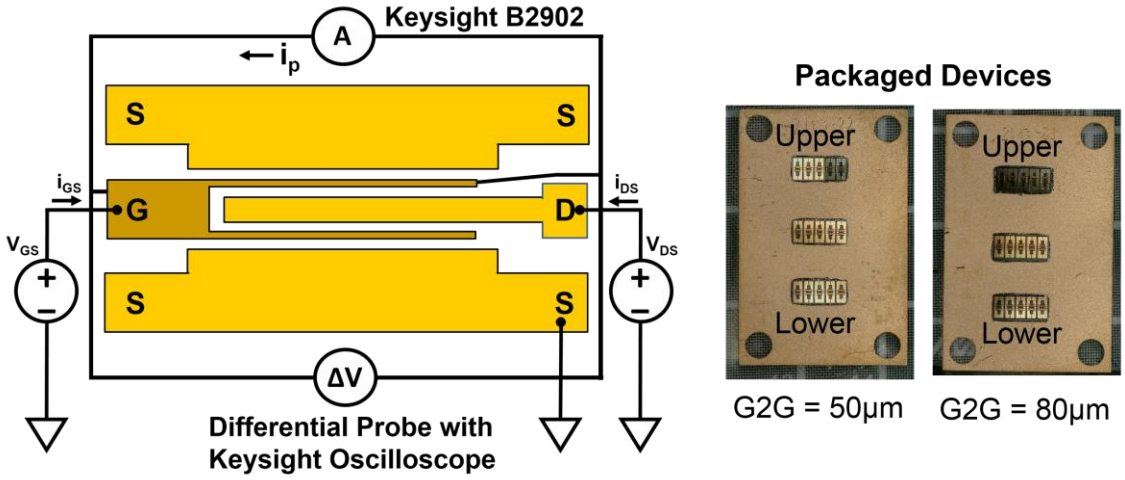



**Figure 20: Experimental setup for gate resistance thermometry (GRT). A four-point measurement across a single finger of a 2x300 µm GaN/Si HEMTs was performed. Both on wafer and packaged measurements were. The devices were packaged on a CuW die.**

### *3.1.1 Removing the Uncertainty due to Gate Leakage*

As discussed in the previous chapter, the accuracy of the GRT can also be influenced by the direction of the probe current in relation to the gate leakage current [47] resulting in an over prediction or underestimation of the junction temperature. Initially, the differential probe was calibrated to read approximately 0 V and then the potential difference was measured once the probe current was supplied. Resetting the differential probe after the gate leakage is injected, removed any effects of the gate leakage and greatly improved the accuracy of the GRT measurements at a constant bias condition. As previously shown in literature, however, the gate leakage was found to vary with bias conditions [43] and the differential probe had to thus be recalibrated for every measurement to avoid any error. If

it was not recalibrated, the errors associated with GRT increased up to 5-7 °C (see Figure 21).

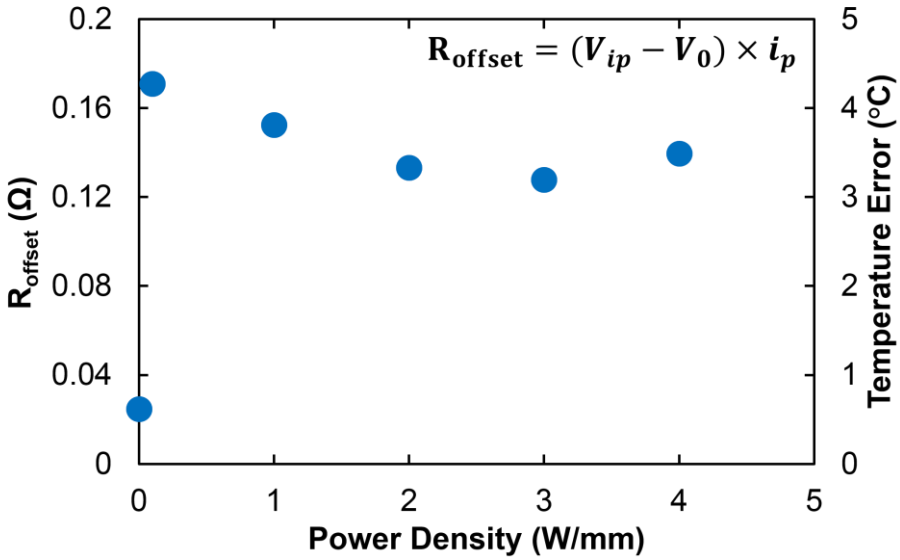



**Figure 21: Effect of power density on the uncertainty of gate resistance thermometry. During operation, significant gate leakage causes an offset in the probe current, $i_p$, which results in a change in the measured gate resistance that is not due temperature.**

To overcome this issue, a peak to peak method with alternating probe currents was implemented. The method is depicted in Figure 22 where the voltage across the gate finger was measured at three different states: a) no probe current, $V_0$ b) forward probe current, $V_{ip}$ c) reverse probe current $V_{-ip}$. The difference between the voltages measured during the forward and reverse probe current state were then used to evaluate the gate resistance. It should be noted that the magnitude of current in the forward and reverse state must be identical to ensure the accuracy of this approach. Initially, the Source Meter Unit (SMU) was programmed to supply a positive and negative current. To determine whether identical magnitudes of current are supplied in both directions, the differential probe was recalibrated to 0 V and the potential difference for the two states was measured. It was concluded that when the potential difference varied within ±10%, errors in the GRT

measurement were measured to be on the order of 10 °C. Beyond the measurement's accuracy, the device's Joule heating profile is also dependent on the probe current's magnitude and direction (discussed in chapter 2). The probe current was thus reduced to 1 mA to prevent any significant voltage drops along the gate width. Note that despite the lower magnitude probe current implemented in comparison to the initial GRT measurements (3 mA), high resolution of the change in gate potential was maintained due to the use of a differential probe.

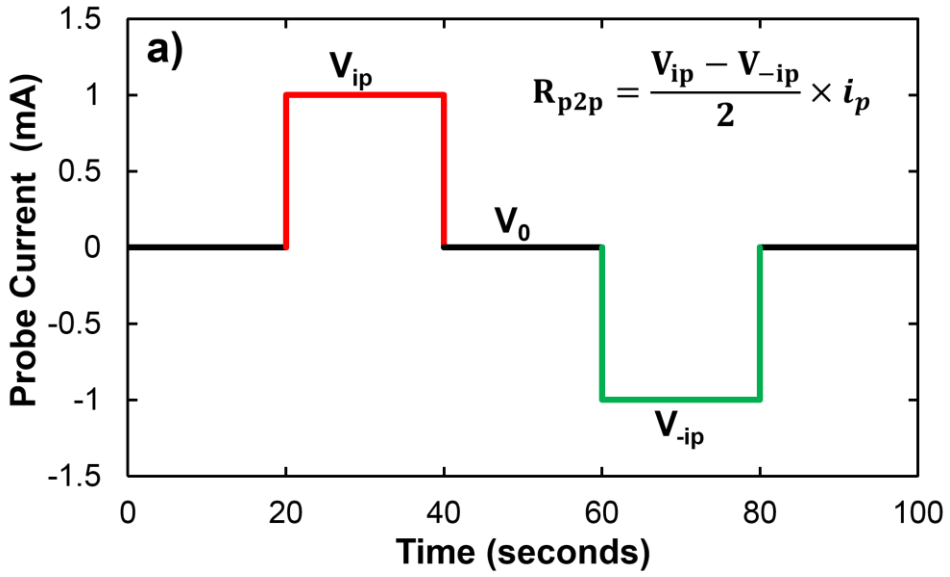



**Figure 22: Peak to peak timing diagram of the probe current direction applied to the GRT device.**

### *3.1.2 Temperature Coefficient of Resistance (TCR)*

Prior to performing thermal measurements, the devices were calibrated using a thermal stage to extract the Temperature Coefficient of Resistance (TCR). Resistance values were recorded from 25 °C to 125 °C in 25 °C increments and are plotted in Figure 23. Using linear regression, the TCR appeared be consistent between devices on wafers for both gate pitches. Measuring 9 devices on wafer (four devices with a 50 µm gate pitch and

five devices with a 80 µm gate pitch), the TCR on average was estimated to be 0.0446 ±0.0008 Ω/K. The packaged devices, however, did not result in the same TCR and even differed in between the same devices on the same die.

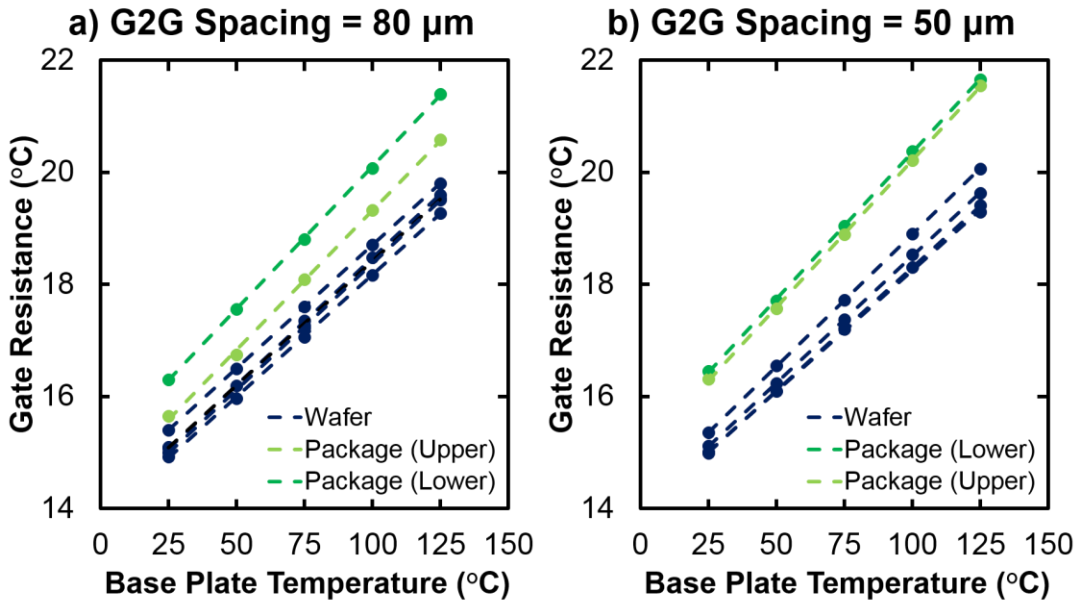



**Figure 23: Linear calibration fit used to extract the temperature coefficient of resistance (TCR) for both on wafer and packaged devices with a gate pitch of a) 80 µm and b) 50 µm.**

The discrepancy between the TCRs extracted from the package devices and the devices on wafer resulted in a maximum of 15% difference. Two devices on each dies were calibrated. For the 50 µm gate pitch, the TCR for both the upper and lower devices was calculated to be 0.0523 Ω/K whereas the 80 µm gate pitch devices resulted in a TCR of 0.0496 Ω/K and 0.0511 Ω/K. Initially it was proposed that large thermal contact resistance created between the package and the thermal stage resulted in a lower temperature the gate metal when measuring the resistance of the packaged devices. Comparing the resistances at room temperature, however, it can be clearly seen that the resistance of the gate metal is different on the packaged devices. The electrical contact resistance associated with probe

could be a potential source of error but the contribution of this resistance was estimated to be on the order of 1% of the total resistance and should be corrected for when performing a 4-point measurement. After reviewing the steps taken to package the devices, it was decided that the solvent was applied to protect the devices during dicing and substrate thinning may have chemically reacted with the gate metal thus causing a change in the overall resistance.

Overall, for the devices on wafer, the same TCR was applied to each device irrespective of the gate pitch. In contrast, a specific TCR associated with each packaged device was used to estimate the temperature rise via GRT. The change in TCR highlights the necessity of remeasuring the TCR after devices have been packaged to avoid any errors in the junction temperature estimation.

### *3.1.3 Steady State Thermal Analysis*

The devices were first biased under DC and the steady state thermal performance of the two different gate to gate spacings was assessed (Figure 24). A 50 V drain bias was applied and the gate voltage was varied to modulate the power density between 1-5 W/mm. As shown previously in literature [73], increasing the gate pitch assists heat spreading and reduces the peak temperature. This trend is confirmed with the GRT devices on wafer (Figure 24a) where a gate to gate spacing of 50 μm results in a 14% higher junction temperature. In contrast, Figure 24b shows the opposite trend for the device's thermal performance mounted on CuW packages (optical images shown in Figure 20). The cause of the higher temperatures achieved by the packaged 80 μm gate pitch devices was attributed to the discrepancy in die attach thickness between the two devices (see Figure

20). The thickness of the die attach was measured to be 40% greater for the 80 µm gate pitch device which translated to a 50% increase in thermal resistance. The difference in thermal performance measured by GRT between on wafer and packaged devices highlights the technique's accuracy and ability to measure changes in the stack configuration.

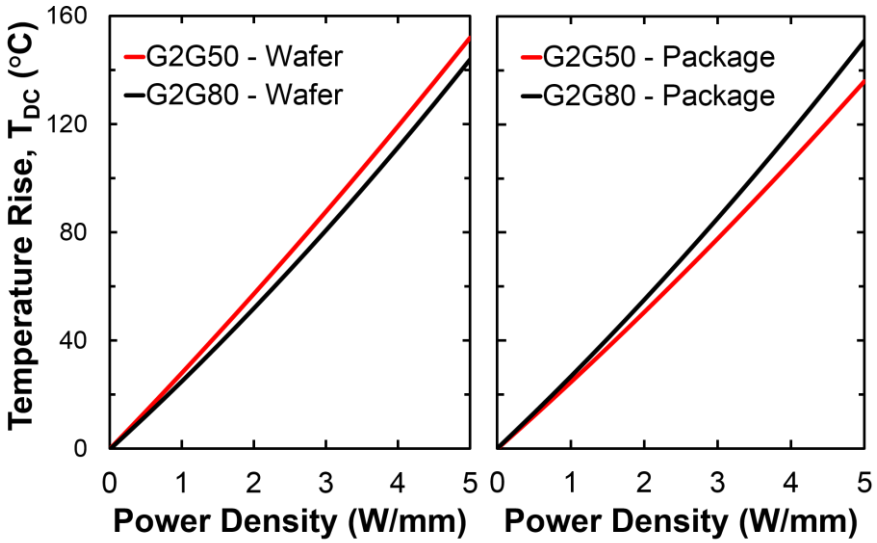



**Figure 24: Steady state thermal response of GaN/Si HEMTs at 125 °C base plate temperature a) on wafer b) mounted on CuW package.**

## 3.2 Effect of Baseplate Temperature

### *3.2.1 DC Biasing*

The effect of the base plate temperature on the steady state thermal performance was assessed to ensure an accurate comparison between DC and RF operation. The baseplate was increased from 25 °C to 125 °C in 25 °C increments. The temperature rise was recorded for both devices on wafer and was plotted in Figure 25. Extracting the slope of the curves, the thermal resistance associated with the devices can be calculated. The thermal resistance was estimated to increase by 7% every 25 °C increment reaching a maximum increase of

28% at 125 °C base plate temperature. This trend agrees well with literature [77] and is to be expected since the thermal conductivity of both silicon [78] and GaN [79, 80] decrease with temperature between 25-125 °C

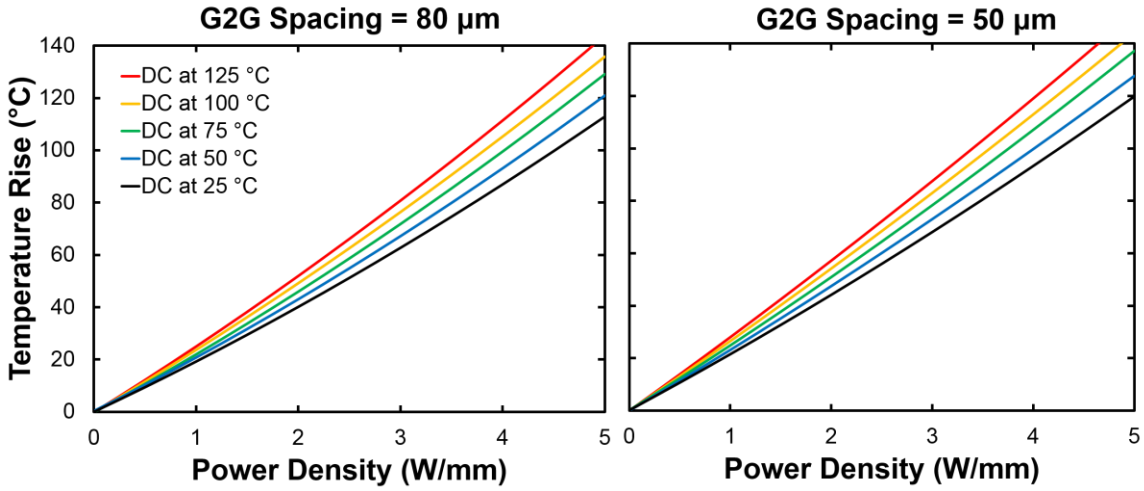



**Figure 25: Effect of base plate temperature on DC thermal performance for a gate to gate spacing (G2G) of a) 80 µm and b) 50 µm.**

A comparison of the thermal resistance between the packaged and wafer devices was performed. Benchmarking the absolute values, the thermal resistance measured at 25 °C showed an increase in thermal resistance for the package device (10%) in comparison the devices on wafer. Despite the silicon substrate being thinned from 625 µm to 50 µm for packaging, the addition of the die attach and the thermal contact resistances at every interface contribute significantly to increasing the thermal resistance. Monitoring the change in thermal resistance relative to the resistance measured at 25 °C, a smaller increase in thermal resistance is observed in the packaged devices reaching a maximum of 15% at 125 °C (Figure 26). The smaller change in the thermal resistance may be attributed to the relatively high thermal conductivity of the CuW package which efficiently removes the heat further away from the device [81].

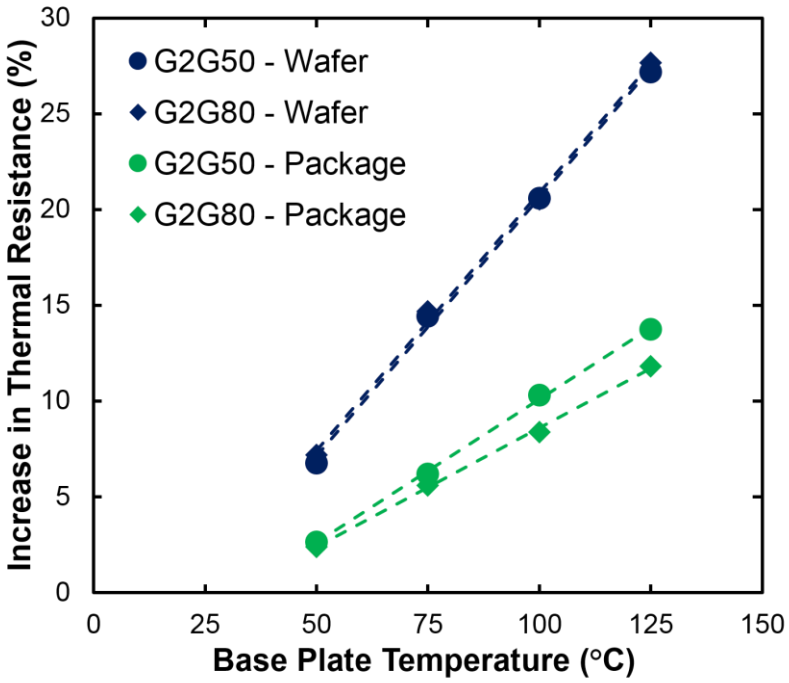



**Figure 26: Effect of base plate temperature on thermal resistance of effective stack. Percentage change is relative to thermal resistance calculate at 25 °C.**

### *3.2.2 RF Operation*

For RF operation Both on wafer measurements and packaged devices were biased and measured on a FOCUS VNA-based load pull stand. The devices were roughly tuned to their peak power added efficiency. For the packaged devices, a CW small signal Gain of 18 dBm was applied at 2.5 GHz where as a 15 dBm was applied to the devices on wafer. The devices were operated under Class AB. Devices were biased at 50 V and 20 mA/mm. Power meters were used to record the input and the output Power. Carrier losses were quantified using a vector network analyzer.

The effect of the baseplate temperature on the RF performance and junction temperature is shown in Figure 27. For all devices, the Power Added Efficiency (P.A.E.) decreased with increasing baseplate temperature. Inherently, the average power dissipated

across the device increased and thus resulted in larger temperature rises measured via GRT. A linear relationship was observed between the temperature rise and P.A.E (which is linearly related to the power dissipated). Based on the results, the viability of using GRT to evaluate the junction temperature under RF operation is highlighted.

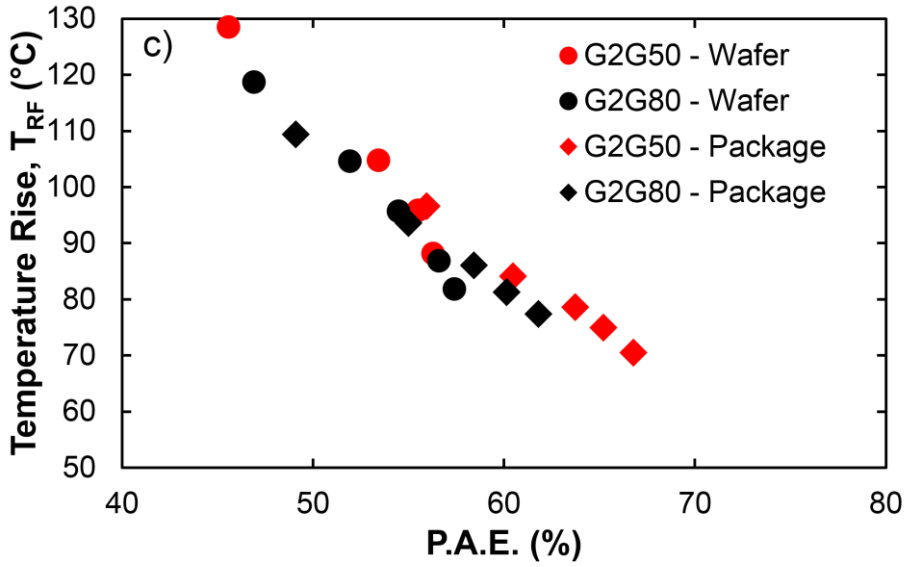



**Figure 27: RF Thermal performance of GaN/Si HEMTs at different Power Added Efficiencies (P.A.E.) evaluated using GRT at different base plate temperatures from 25 to 125 °C.**

Furthermore, the effect of gate to gate spacing on the RF thermal performance can be observed where, on average, a 5% decrease in temperature for the 80 µm gate pitch is achieved. Comparing the packaged to wafer measurements, higher efficiencies are obtained in the packaged devices demonstrating an improvement in the thermal performance. The substrate thinning of the wafer may contribute to this phenomenon by the significant reduction in the substrate thermal resistance.

### 3.3 RF vs DC Operation

To directly compare the junction temperature measured under DC to RF, an accurate estimation of the average power dissipated is necessary. The RF average power was calculated by subtracting the net gain RF power from the DC dissipated power [65]:

$$P_{DISS} = V_{DS} \times I_{DS} - (P_{RFOUT} - P_{RFIN}) \quad (2)$$

Using the average power density calculated at a given baseplate temperature, the device can be biased under DC at the same conditions to obtain the DC temperature rise. The comparison of the temperature responses is shown in Figure 28. For both DC and RF operation, the temperature rise increased linearly with power density. Comparing the junction temperature under RF to DC, however, shows a reduction in temperature under RF. A maximum decrease of 15% is achieved at the highest power density for a packaged device with an 80 μm gate pitch.

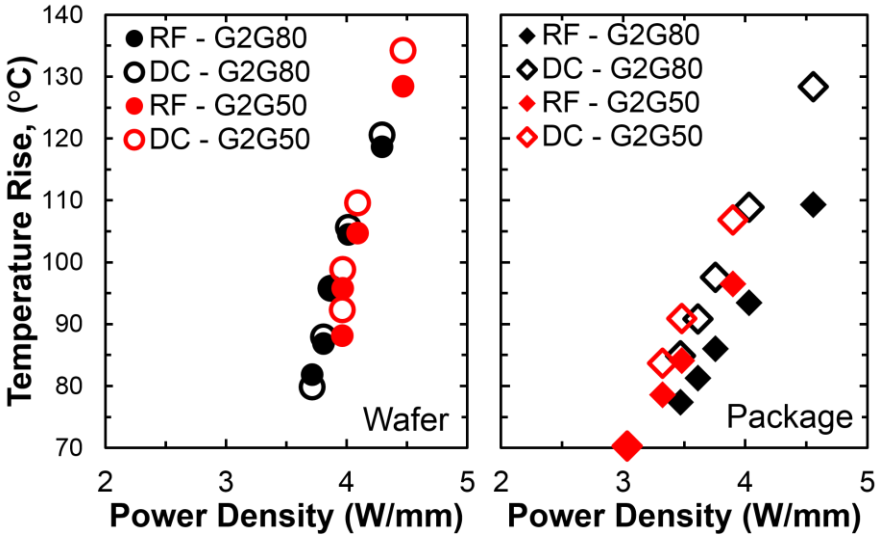



**Figure 28: Comparison of junction temperature measured under RF operation to DC steady state biasing. Temperatures were compared for identical base plate temperatures and power dissipated.**

This comparison suggests a difference in temperature profiles across the device channel between RF and DC operating conditions and the effect of bias dependent Joule heating. Overall, the change in distribution of Joule heating during RF operation causes the average gate metal temperature to decrease in comparison to the equivalent DC power dissipated. Figure 28 also demonstrates a difference in thermal performance between the packaged and on wafer devices. For the same power densities, the devices on wafer exhibit RF temperatures closer to the resulting temperature rises under DC. This discrepancy was attributed to two factors: substrate thinning of the packaged devices and the presence of die attach. Despite the low thermal conductivity of the die attach, the thermal boundary resistance is estimated to be lower than that compared to interface between the wafer and the ceramic vacuum plate. Overall, to gain deeper insight into the thermal performance of GaN HEMTs under RF operation, transient thermal characterization is necessary to monitor the temperature swing in the device. Electrothermal simulations have already been performed to predict the temperature profile across the channel under Class B operation [22].

### 3.4 Transient Analysis

To gain deeper insight into the thermal performance of GaN HEMTs under RF operation, transient thermal characterization is thus necessary to monitor the temperature swing in the device. The results of such measurements could then be compared to electrothermal simulations such as those performed in [22]. Limited by the experimental setup for this study, the transient thermal dynamics of the device could only be investigated under pulsed biasing. The devices were biased using an AMCAD Pulsed IV system. A 50 V 360-μs pulse was applied to the drain with a 10% duty cycle. A constant pulsed gate bias

was applied to prevent errors in the gate resistance measurements due to change in the leakage currents. A 10 µs delay was applied to ensure that the gate bias was applied before the drain bias. While the experimental setup did not allow for pulsed RF testing, the device's transient thermal profile could be used to assess its performance under high frequency periodic heating. Figure 29 compares the transient rise and decay for both devices. The 50 µm gate pitch device exhibits a higher temperature rise showing a peak temperature increase of 15%.

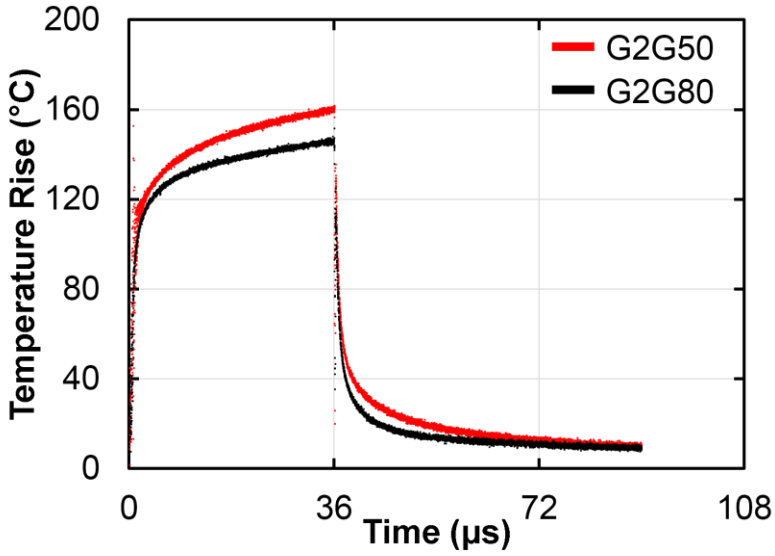



**Figure 29: Transient thermal response of packaged GaN/Si HEMTs with different gate to gate spacings. A 50 V drain bias was applied for a 10% duty cycle.**

It should be noted that the difference in temperature response between the different gate pitches, measured in Figure 29, showed the opposite trend under DC biasing (Figure 24). As previously mentioned, the higher temperatures achieved under DC by the 80 µm gate pitch was caused by the increase in die attach thickness. Pulsing the devices at a higher frequency the thermal penetration depth is shallower and thus does not reach the die attach interface. The results demonstrate that the transient GRT analysis of the device is

insensitive to the device packaging and evaluates the effect of the gate to gate pitch on only the device level. Overall, the use of the differential probe enables a higher temporal resolution than that previously achieved when using an oscilloscope. Despite the temporal resolution not being yet sufficient to monitor the temperature change in devices under GHz operation, the advancements in the GRT technique developed in this study provide a step closer to achieving this.

## 3.5 Summary and Conclusions

The results from this study show the feasibility of using GRT under RF to estimate the junction temperature. In contrast to optical thermal characterization methods, RF GRT provides a quick reliable method to benchmark the device's thermal performance under RF. The results confirm the improvement in thermal performance when using a larger gate to gate spacing and highlight a linear relationship between the device's power added efficiency and temperature rise. The direct comparison of RF to DC temperature rises shows a decrease in junction temperature when operating the device under RF. The lower temperatures observed under RF confirm that the Joule heating profiles is bias dependent. Developing a transient GRT method under RF could provide further insight into the device's transient thermal dynamics. The ability to directly compare these Joule heating profiles, however, is not possible via GRT and thus requires electrothermal simulations and optical mapping techniques to further investigate the differences between these the two modes of operation.

# CHAPTER 4. DEVELOPMENT OF OPTICAL THERMAL METROLOGY TECHNIQUES FOR GAN HEMT RELIABILITY

Content in the chapter (figures and text) adapted from:

1. G. Pavlidis, *et al.,* "Monitoring the Transient Thermal Response of AlGaN/GaN HEMTs using Transient Thermoreflectance Imaging," in CS Mantech, Indian Wells, CA, 2017, pp. 173-176. [82]

## 4.1 Raman Active Nanoparticles for Surface Temperature Measurements

Optical barriers, mainly metal pads, have limited the majority of Raman thermometry studies to estimate the temperature rise in the GaN layer in between the metal contacts. Although this technique has been developed to show high accuracy, the evaluation of the region below the gate metal temperature has only been possible via backside confocal measurements. This setup requires expensive optics and the removal of any heat sink attached to the bottom of the device [31]. Another limitation identified in literature has been the inherent volumetric averaged temperature measured when using visible wavelengths below the bandgap of GaN [24]. This has led to the underestimation of the peak temperature requiring simulations to be conducted to predict this parameter [27]. Furthermore, the stress dependence of the GaN $E_2$ (HI) phonon mode has also required the use of two peak analysis to decouple the temperature and stress effects associated with the phonon modes. The need for a strain free surface temperature measurement using Raman is apparent and would assist in directly monitoring the peak temperature of the device. The

use of Raman active nanoparticles has preliminarily shown to be a good candidate to solve this challenge [62, 63]. By combining the independent Raman sensors on top of the device, both a strain free surface temperature measurement and average GaN signal can be obtained to sense the vertical gradients that may exist in the device. In this chapter, the development and application of Raman active nanoparticles for thermometry is discussed and its suitability for GaN HEMTs is investigated.

### *4.1.1 Sample Preparation and Calibration*

Several nanoparticle powders have been developed from bulk materials that have shown to exhibit strong Raman scattering. A benchmark of different nanoparticles was thus conducted to determine the material with the highest temperature dependence.

**Table 3 Material properties of nanoparticles under investigation.**

| Nanoparticle | Manufacturer | Diameter (nm) | Purity (%) | Raman Shift ($cm^{-1}$) |
|---|---|---|---|---|
| Diamond | Kay Diamond Products | 0-100 | 99.9 | 1330.7 |
| ZnO | Sigma Aldrich | <50 | 97 | 437.5 |
| $TiO_2$ (anatase) | Alfa Aesar | 32 | 99.9 | 143.23 |
| Si | American Elements | 80-100 | 99.9 | 518.87 |

Unfortunately, long acquisitions time were necessary to detect the Raman peak for some of the nanoparticles (SiC, ITO, AlGaN) and were thus not further examined. This led to studying in detail the application of four different nanoparticles (see Table 3).

Initially, three different criteria were defined to ensure the possibility of these particles being applied to GaN HEMTs:

1. Strong phonon temperature dependence.
2. Minimal overlap with Raman peaks associated with GaN.
3. Uniform deposition of particles on device.

The phonon frequency with the highest peak intensity for each nanoparticle is shown in Figure 30. At first glance, no peaks interfere with the two GaN vibrational modes monitored for thermometry ($E_{2high}$: 568 $cm^{-1}$ and $A_1$(LO): 732 $cm^{-1}$). Further testing, however, showed that $TiO_2$ $E_{2high}$ peak near 143 $cm^{-1}$ can interfere with the $E_2$ (LO): 150 $cm^{-1}$ peak associated with GaN [83]. The near proximity of these two peaks requires the multi peak fitting algorithms and, in some cases, the direct overlap of these peaks can result in errors when being used for temperature evaluation. To ensure a strong Raman scattering rate from $TiO_2$, a highly pure single phase form of the material is necessary [84]. Experimenting with different purity levels of $TiO_2$ anatase, it was found that an increase from 99.7% to 99.9% purity had a significant impact in preventing the GaN $E_2$(LO) peak from interfering with the $TiO_2$ peak. Apart from $TiO_2$, the Si nanoparticles may also interfere when evaluating devices on a Si substrate.

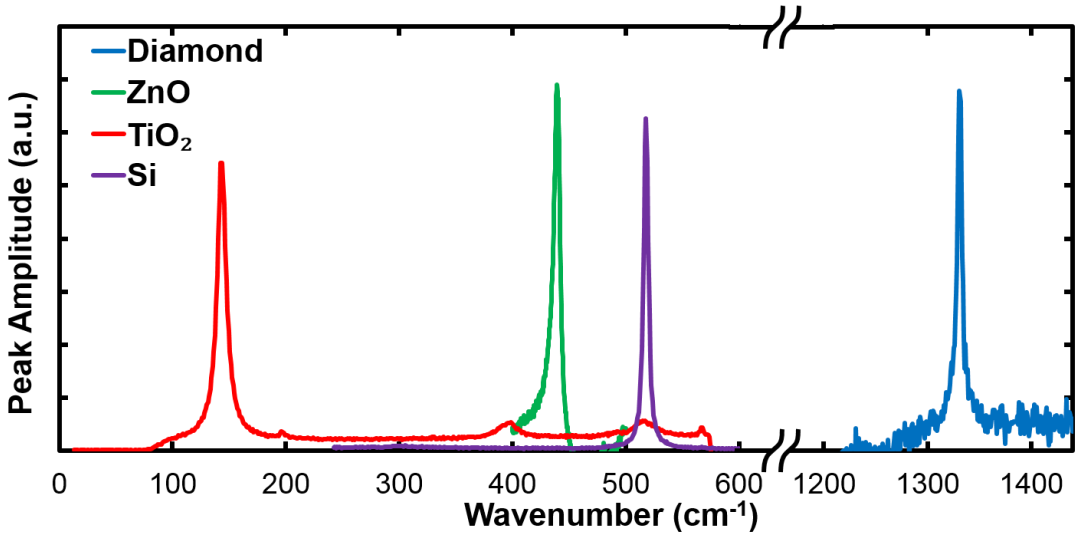
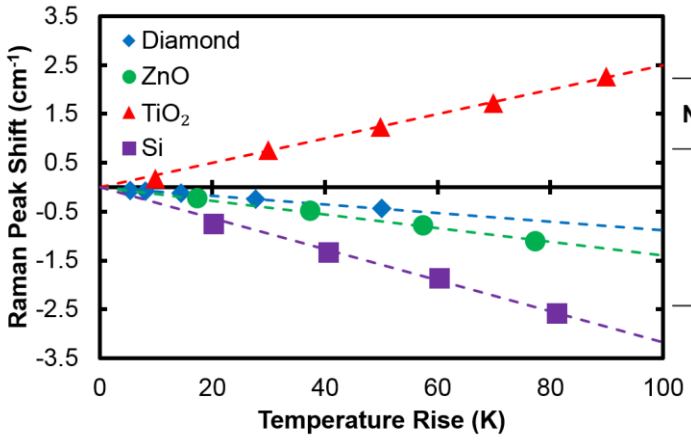



**Figure 30: Raman spectra of nanoparticles under investigation using a 488 nm laser.**

Using a thermal stage, the temperature coefficient of each phonon frequency was extracted to determine the sensitivity of each material. The particles were initially deposited on a glass substrate to avoid any interference from external Raman signatures. A thermocouple was placed on the top side of the glass to ensure close approximation of the substrate temperature. The Raman spectra were fitted at different stage temperatures and the results are plotted in Figure 31. The temperature coefficients were compared to the coefficients previous published in literature for bulk material [85-89]. For all cases, the coefficients aligned well with literature for the temperature range studied and the use of linear fitting was justified. The highest phonon temperature dependence was found in the Si and $TiO_2$ nanoparticles exhibiting coefficients greater than 0.02 $cm^{-1}/K$.




| Nanoparticle | Temperature Coefficient ($cm^{-1}/K$) |
|---|---|
| Diamond | -0.00886 |
| ZnO | -0.01395 |
| $TiO_2$ | 0.02494 |
| Si | -0.03178 |

**Figure 31: Temperature dependence of different nanoparticle phonon frequencies. Linear regression was applied to extract the temperature coefficients.**

In addition to benchmarking the temperature dependence of the Raman signatures, the effect of laser heating must also be taken into consideration. Despite the silicon nanoparticles resulting in the highest temperature dependency, the visible wavelength lasers used for Raman (488 nm and 532 nm) are both absorbed in the material and may cause significant heating. Varying the 488 nm laser power with filters, the effects of laser self-heating are plotted in Figure 32. For the Si nanoparticles, Figure 32 demonstrates that the laser power must be reduced to nearly 1% of the nominal output power (25 mW) to avoid any self-heating effects. This translates to a significant increase in acquisition time to obtain a sufficient amplitude for the Raman peak. Likewise, Diamond also experienced the effects of laser self-heating and it could also be seen optically that the morphology of the particles changed. Overall, $TiO_2$ and ZnO appeared to have no effects of laser self-heating and were chosen as the two nanoparticles to further study.

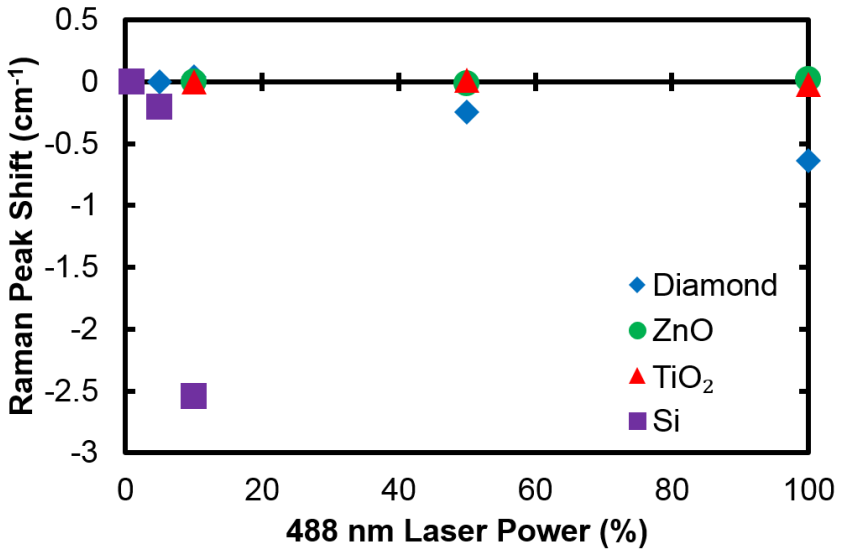



**Figure 32 Effects of laser self-heating on Raman nanoparticles phonon frequency.**

After having deposited the nanoparticles on a glass substrate, the next step was to assess the uniformity of the particle deposition on more similar surface roughness as compared those encountered on commercial device surfaces. In general, the governing processes for the dispersion of particles on a surface depends heavily on the deposition speed and particle volume fraction [90]. All particles were diluted in a solvent (mainly IPA) with varying concentration and then sonicated prior to deposition. Different deposition methods were investigated on a plain silicon substrate. This included a spin coater, an air brush, and a pipette. For spin coating, the spin speed was varied and it was observed that at higher speeds (1500 rpm for 30 seconds), thin layers with low Raman signature peaks were achieved, while at lower speeds, highly concentrated particles in localized areas were deposited. The air brush method resulted in a sparse distribution of the particles which was difficult to obtain a Raman signal. The pipette method included controlling the ambient temperature of the substrate, with a baseplate, to enable the precise localized deposition of the particles. Overall, it was difficult to control the particle

distribution noting that the roughness and topography of the surface played a significant role in the final distribution.

When applying these deposition methods to GaN HEMTs, the pipette method was found most suitable as it enabled the localized deposition of particles and thus prevented the particles from being deposited on areas of electrical contact such as the ground-signal-ground pads (Figure 33). Different concentrations of the particles were tested to determine the best concentration that would result in a sufficient Raman peak intensity and still maintain visibility of the device geometry below. For ZnO, 0.01 g of particles were diluted in 20 mL of IPA, and the baseplate temperature was held at 170 °C for less than one minute after deposition. For $TiO_2$, 0.01 g of particles were diluted in 100 mL of IPA and the baseplate temperature was held at 50 °C.

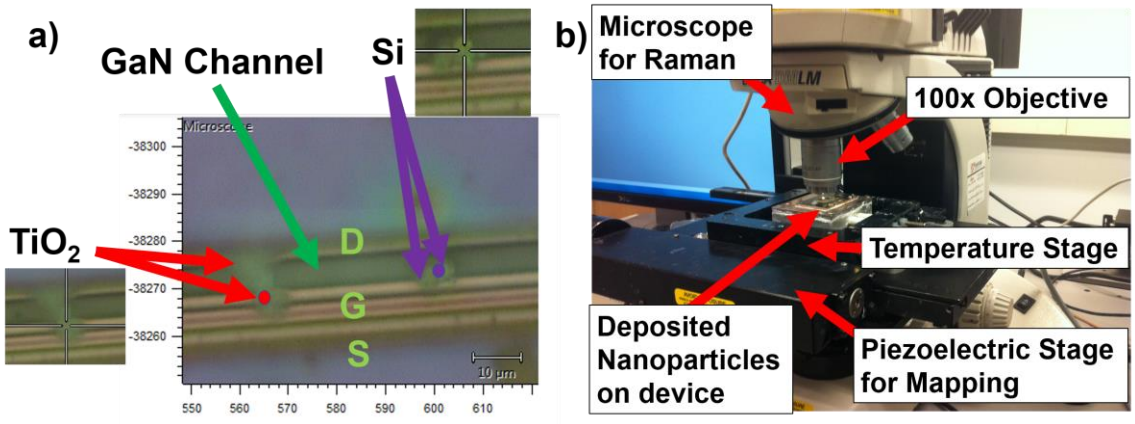



**Figure 33: a) Location of nanoparticles when deposited on GaN HEMT b) Description of setup used to measure nanoparticles and perform calibrations.**

After establishing a robust method of deposition, the uniformity of the temperature coefficient was investigated to determine the necessity of performing calibrations for every particle measured. For $TiO_2$, over 15 different locations across the channel, the source, drain and gate pads were measured (results are plotted in Figure 34 ). An averaged slope

of 0.02455 $cm^{-1}/K$ was determined. Comparing this slope to the specific slope extracted for each location, a maximum error of 7% was estimated. The results of this study confirm the uniformity of the $TiO_2$ temperature coefficient validating the application of a single temperature coefficient to all particles deposited in a single batch.

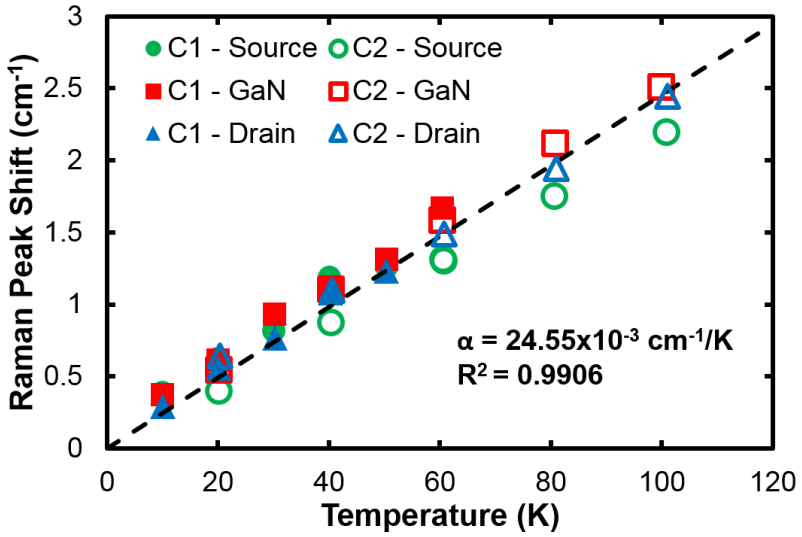



**Figure 34: Uniformity of temperature calibration coefficient of $TiO_2$ nanoparticles across GaN/SiC HEMT.**

Comparing the applicability of ZnO to $TiO_2$ for Raman thermometry, the main advantage identified for using ZnO is the possibility to remove the particles after characterization. The removal of the ZnO particles was attempted using slightly acidic DI water on four different GaN/SiC HEMTs. Water was mixed with a HCL at ratio of 2000:1. Devices were left in the solution for series of hours before being tested again. To determine if any damage was done by the acidic solution, IV characterization was performed prior to and after particle removal. Slight changes in the IV curves led to believe that the metal contacts may have reacted with the acidic solution. It was concluded that in order to apply a particle removal process to the GaN HEMTs, a less reactive acid needed to be investigated.

### *4.1.2 Effect of Nanoparticles on Electrical Performance*

To determine whether the $TiO_2$ nanoparticles have any significant impact on device operation, I-V characterization of the devices were performed before and after the nanoparticle deposition. An example of a device characterized is shown in Figure 35. The 'kink effect' shown near the elbow of the I-V curves was attributed to electron trapping [91]. Since the investigation of nanoparticles was conducted on previously used devices, most devices did not show ideal I-V characteristics. The I-V curves, however, obtained before and after deposition were found to be very similar highlighting that there was no change in the electrical characteristics of the device.

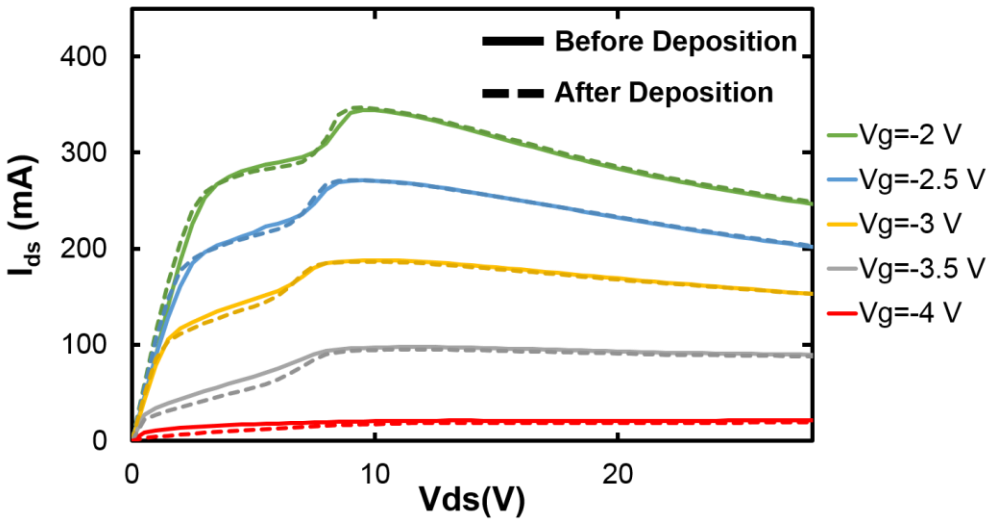



**Figure 35: Effect of $TiO_2$ nanoparticle deposition on GaN HEMT IV characteristics.**

Investigating the effect of the particles on the device's electrical characteristics also led to studying the effect of the electric field on the $TiO_2$ $E_g$ phonon frequency. As previously mentioned, the phonon modes associated with GaN are highly stress dependent and the thermal stresses developed during operation in addition to the piezoelectric stress can lead to an errors in the temperature measurement [92]. Raman measurements were

taken before and during applying a bias to the device in the pinch off conditions (high negative on the gate) to determine any shift in the Raman peak position. Insignificant changes in the peak position were found supporting the claim that the nanoparticles were considered a strain free measurement.

### *4.1.3 Channel Temperature Mapping*

Upon review, the $TiO_2$ anatase nanoparticles were regarded as the most suitable material to be used for surface temperature measurements of GaN HEMTs. The particles were thus deposited on a GaN/SiC HEMT to perform a full lateral temperature mapping of the device. The device was biased at different power densities with a constant drain bias of 28 V. The distributions are plotted in Figure 36.

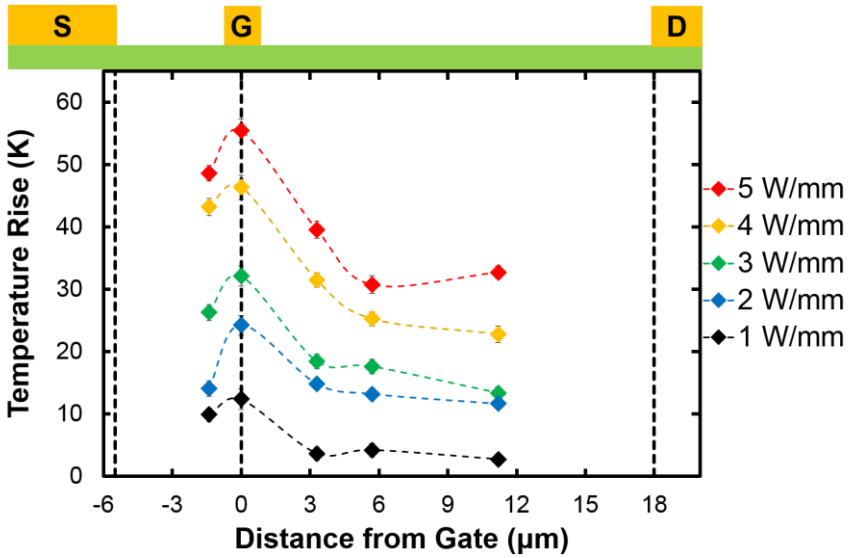



**Figure 36: Lateral surface channel temperature mappings of GaN/SiC HEMT using $TiO_2$ nanoparticles.**

As expected, the results show that the peak temperature rise in the device is located near the gate confirming the accuracy of the technique. The application of implementing a single temperature coefficient for all particles is also verified as no irregularities in the

temperature distributed are observed. Overall, results prove the viability of using $TiO_2$ nanoparticles for surface temperature mappings of GaN providing a method that can measure any point on the device irrespective of the material found below it.

## 4.2 Transient Thermoreflectance Imaging

### *4.2.1 Theory and Experimental Setup*

Developing highly accurate and versatile point measurement techniques such as Raman are useful, however, long acquisition times are necessary to perform full thermal mappings and the acquisition time is exponentially increased when attempting to perform transient thermal analysis. One technique that has the ability to measure simultaneously the transient surface temperature rise of both the channel and the gate metal is transient thermoreflectance [93]. The accuracy of this technique is based on how well the thermoreflectance coefficient, $C_{th}$, of the surface of interest can be estimated [67, 94]. This is based on the change in reflectivity of a surface, ($\Delta R/R$), for a given temperature rise, $\Delta T$.

$$C_{th} = \Delta T \times \left(\frac{\Delta R}{R}\right)^{-1} \tag{3}$$

Due to thermal expansion effects, heating a material without maintaining a constant plane of focus to determine the $C_{th}$ can introduce error in the measurement of reflectivity [21]. Recent advancements in transient thermoreflectance imaging (TTI) technology has enabled the use of a piezoelectric stage to account for thermal expansion during the extraction the $C_{th}$ [72]. Implementing this technology, a Microsanj NT220B was used in this study to perform calibrations and conduct TTI measurements. The experimental setup is shown and explained in Figure 37. Taking advantage of advance timing controls, the device, CCD, and LED are all biased at short time pulses on the nano to microsecond scale. Controlling the delay of the LED excitation source, the temperature of the targeted area can be probed at different time throughout the pulse. To extract the correct $C_{th}$, a

wavelength sweep was performed to determine the optimal wavelength that results in the highest thermoreflectance signal for the region of interest.

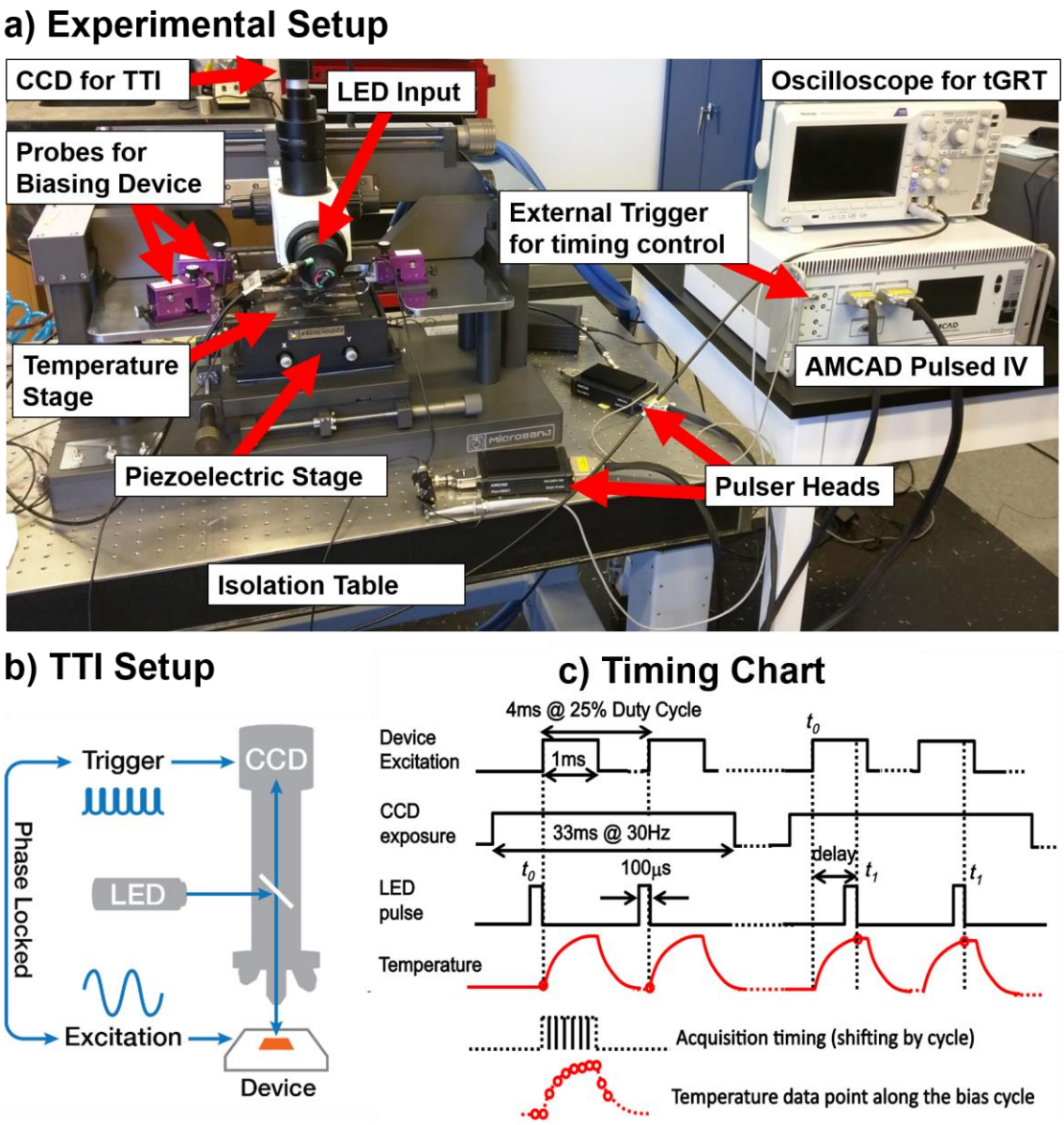



**Figure 37: a) Experimental setup of Microsanj thermoreflectance system b) Schematic describing the different components used in thermoreflectance imaging c) Schematic explaining timing control of different components of Microsanj.**

### *4.2.2 Design Specifications and Considerations*

Due to the difference in feature sizes between the different areas of interest, appropriate selection of the objective's magnification and numerical aperture (NA) is necessary. Increasing the magnification can increase the resolution (108 nm/pixel to 53.5 nm/pixel when switching from a 50x objective to a 100x objective). Choosing a higher NA reduces the objective's working distance which is disadvantageous when attempting to probe devices. A large NA, however, is beneficial for reducing the noise in measurements as the path from the reflected surface to the CCD is decreased. Overall, the calibration measurements were taken at 50x for the drain and source pads while a 100x magnification was used for the GaN channel and gate metal.

To improve the temporal resolution of TTI, the LED pulse width can be reduced to the minimum Full Width Half Max (FWHM) of approximately 50 ns (measured with a photodiode). This also defines the theoretical maximum time resolution possible with the current configuration. This significant reduction in LED pulse width, however, would reduce the thermoreflectance signal and consequently decrease the signal to noise ratio. To maintain a high intensity of light being reflected from the surface, different techniques may be applied.

First, the LED duty cycle relative to the overall time period can be held constant. In the current experimental setup, an LED duty cycle of 1.38% was applied which would require the overall time period to be reduced to 3.6 μs to apply an LED pulse width of 50 ns. When it is not practical to decrease the time period, the LED duty cycle can be reduced and other factors can be varied. The CCD frame rate can be reduced from 30 frames per

second (fps) to 20 or 10 fps. The reduction in frame rate will increase the number of cycles captured in a single frame correlating to an increase in the thermoreflectance signal detected by the CCD. The drawback to this approach is that longer overall acquisition times are required to reduce any noise in the thermoreflectance signal. Lastly, a gain can be applied to the CCD to enhance the detected thermoreflectance signal. When applying this technique, the CCD is more sensitive to the noise attributed to the ambient light and thus requires the setup to be placed in a dark box to reduce any background noise.

### *4.2.3 Understanding the Thermoreflectance Coefficient*

Since the $C_{th}$ is both material and excitation source wavelength dependent (Figure 38a), there exist several difficulties when attempting to use the same wavelength source for thermoreflectance measurements of different GaN devices. For example, the thermoreflectance signals detected from the gate metal with different passivation thicknesses can result in different $C_{th}$'s for the same wavelength source due to thin film interference (see Figure 38b).

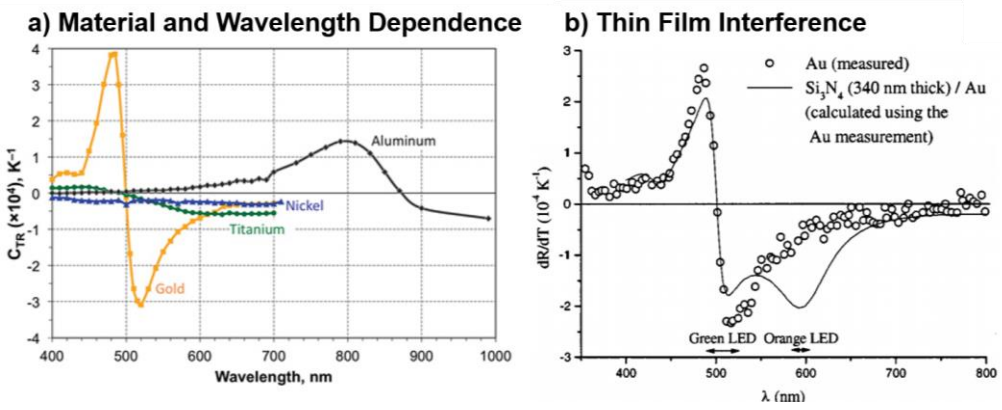



**Figure 38: a) Thermoreflectance coefficient ($C_{TR}$) vs. illumination wavelength for various materials [95] b) Spectrum of dR/dT measured in the case of bare gold (circles), and calculated in the case of $Si_3N_4$-coated gold (line). The arrows indicate the FWHM spectral width of two of the LEDs [69].**

To ensure a high signal to noise ratio, a wavelength source that results in the strongest thermoreflectance coefficient should be selected. This can be assessed by accurately quantifying the $C_{th}$ for different wavelengths using the Microsanj. The piezoelectric stage allows the surface to be autofocused and corrects for thermal expansion on the nanometer scale (typically within ~1 nm at 100x magnification in the X-Y direction and ~10 nm in the Z direction). It employs a combination of commercial and proprietary metrics as feedback for the autofocus control. Furthermore, estimating the true temperature of the surface when measuring the reflectivity can also lead to error in the coefficient. To detect any large temperature rises within the die, a thermocouple was placed directly on the die of the device instead of using the thermocouple in the Peltier stage.

### *4.2.4 Experimental Validation*

In this study, transient thermoreflectance imaging (TTI) is used to perform surface temperature mappings of AlGaN/GaN HEMTs on a SiC substrate. SiN was used as the surface passivation. As shown in Figure 39, the devices tested were six fingered devices with a 370 μm gate width and were identical to the devices measured via gate resistance thermometry (GRT) in Chapter 2.

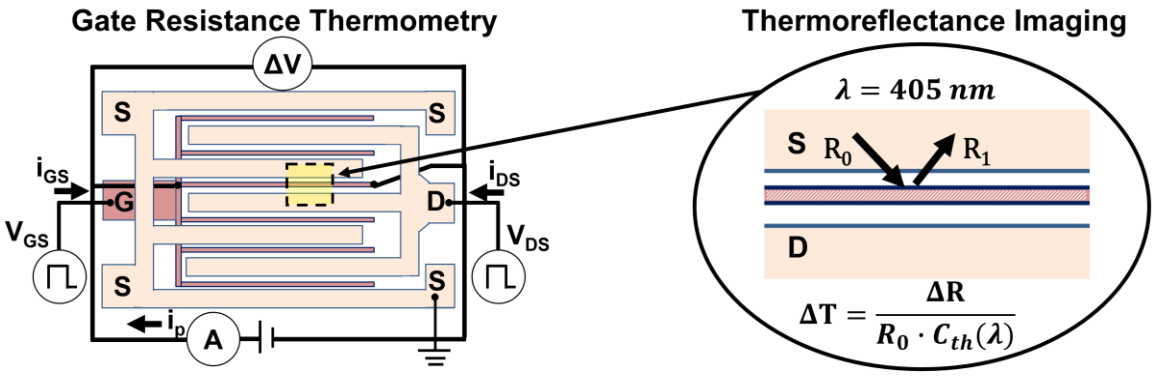



**Figure 39: Four terminal sensing gate resistance thermometry device in pulsed bias configuration. For direct comparison to transient thermoreflectance imaging, simultaneous thermoreflectance mapping of the device gate width was performed. A 405 nm LED excitation was pulsed to measure the transient thermoreflectance response.**

To verify the accuracy of this technique, the GRT technique utilized in Chapter 2 was performed simultaneously to TTI. The voltage drop across the gate finger was measured using a Tektronix DPO3012 Oscilloscope and a probe current of 3 mA was applied. GRT measurements were performed every 2 minutes capturing 4 random periods each time. An average of all the waveforms captured was taken to directly compare to the TTI temperatures estimated above the gate region. The standard error of the GRT uncertainty was calculated using 95% confidence intervals.

A wavelength sweep was performed to determine the optimal wavelength that results in the highest thermoreflectance signal for the regions around the GaN channel. Initially performing the calibration at approximately a 100 °C temperature rise, all regions resulted in a strong $C_{th}$ for a 405 nm LED source. To confirm the linearity of the thermoreflectance coefficient, the change in reflectivity, (ΔR/R), was measured at different temperature rises and linear regression was used to extract the coefficient (Figure 40). A

$C_{th}$ of -2.38 x $10^{-4}$ $°C^{-1}$ and -2.14 x $10^{-4}$ $°C^{-1}$ were extracted for the Gate Metal and GaN region respectively.

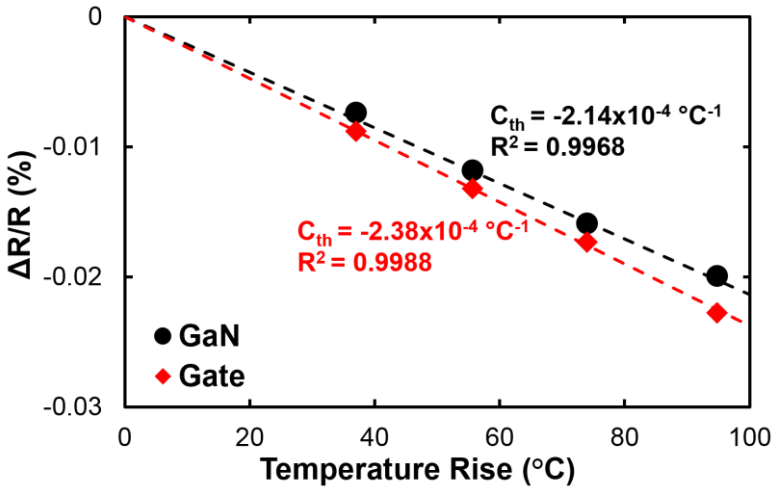



**Figure 40: Linear temperature dependence of the thermoreflectance signal detected from the gate and GaN channel region using a 405 nm LED source. Linear thermoreflectance coefficients, $C_{th}$, were extracted from plotted data.**

Similar to the setup described in Chapter 2, the devices were biased under pulsed conditions using an AMCAD Pulsed IV system. A 20 V 400-µs period pulse was applied to the drain with varying duty cycle from 10-40%. A constant pulsed gate bias was applied to prevent errors in the gate resistance measurements. A 10 µs delay was applied to ensure that the gate bias was applied before the drain bias (Figure 41b). The maximum power dissipated was estimated to be 3.9 W/mm. For TTI, an LED pulse width of 5.5 µs (Figure 41) was used to obtain a strong consistent thermoreflectance signal on the regions of interest. To capture the device's temperature rise and decay, thermoreflectance measurements were recorded every 8 µs from 10 to 270 µs.

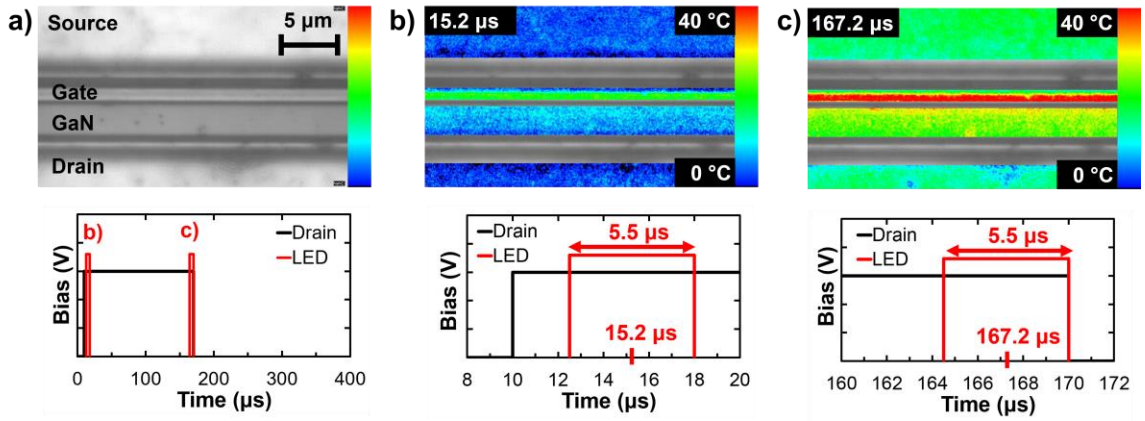



**Figure 41: a) CCD image of 6x370 µm GaN HEMT including timing synchronization between device bias and LED pulse. LED pulse widths of 5.5 µs were applied at time delays of b) 15.2 µs and c) 167.2 µs. The corresponding CCD based thermoreflectance image highlights the area of localized Joule heating along the gate width during pulsing.**

To directly compare the temperature measured by TTI to GRT, thermoreflectance images using a 100x lens were taken of the central measured GRT finger. An example of the temperature rise monitored across the gate via TTI is shown in Figure 41. The images shown were accumulated over 80 seconds at LED time delays of 15.2 µs and 167.2 µs respectively. Noting the applied 10 µs delay to the drain bias, Figure 41b captures the temperature rise at the very beginning of the pulse, between 2.5 µs and 8 µs after the drain bias is applied. The image shows that the highest temperature is found to be along the gate width confirming the localized Joule heating profile present in GaN HEMTs. Figure 41c represents closely the peak temperature rise in the device at the end of the pulse when a 40% duty cycle is applied. The peak surface temperature in the device remains over the gate metal region as expected. The heat is shown to spread along the channel where a temperature gradient can be seen along the GaN channel. The drain and source pads appear to have the lowest temperature rise as they are furthest away from the source of localized Joule heating. Temperature data from pixels located over the edges of the ohmic and

Schottky contacts were filtered due to low intensity of light reflected from these areas which translated into large uncertainties.

Acquiring images every 8 μs, the gate temperature rise and decay of the device under 10%, 20% and 40% duty cycle was monitored. To directly compare the temperature rise using TTI with transient GRT, an averaged probed region across the gate width was used and plotted in Figure 42. The averaged region would represent approximately the same temperature the GRT method is measuring when averaging over the gate metal resistance. The close agreement between the TTI and GRT measurements (maximum 5% difference) indicates that the gate metal $C_{th}$ extracted from the calibration is accurate.

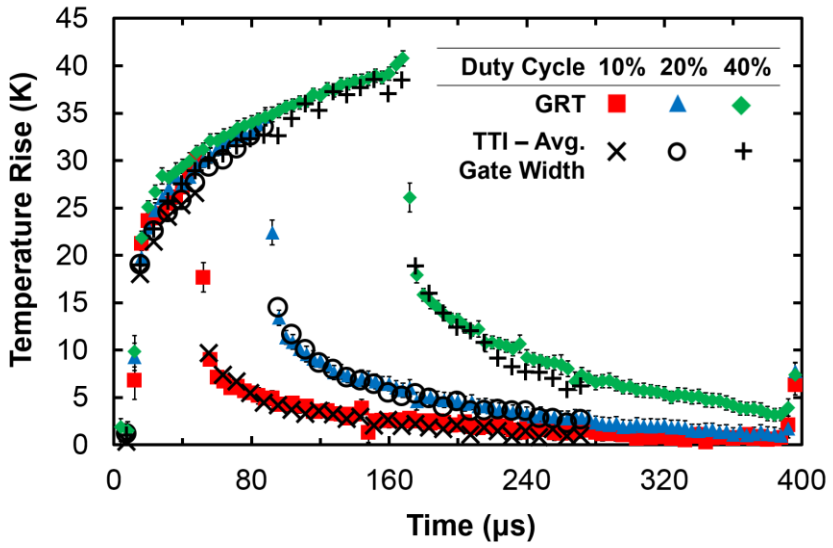



**Figure 42: Comparison of transient thermal response of a GaN HEMT under various duty cycles measured by transient thermoreflectance imaging, TTI (markers) and gate resistance thermometry, GRT (shapes).**

The thermoreflectance coefficients can now be used to monitor the temperature rise across the whole device including the GaN, drain and source regions (Gate $C_{th}$: -2.38 x $10^{-4}$ °$C^{-1}$, drain and source $C_{th}$: -3 x $10^{-4}$ °$C^{-1}$ and GaN $C_{th}$: -2.14 x $10^{-4}$ °$C^{-1}$). Using these

values with a 20x magnification lens, a device thermal mapping is shown in Figure 43. The temperature profile along the gate width for the middle gate finger and bottom gate finger are plotted and second order polynomials were fitted to the raw temperature data. The temperature profile along the middle gate finger shows a significant temperature rise from 23.2 °C at the edge of the mesa to 42.6 °C in the center. As shown in Chapter 2, the averaged GRT temperature (40 °C) does not capture this gradient showing the necessity of a mapping technique such as TTI to capture the peak temperature and gradient. Furthermore, the uneven temperature distribution between fingers is shown in Figure 43. In contrast to the middle gate finder, an 8.8 °C temperature gradient along the bottom gate finger is observed.

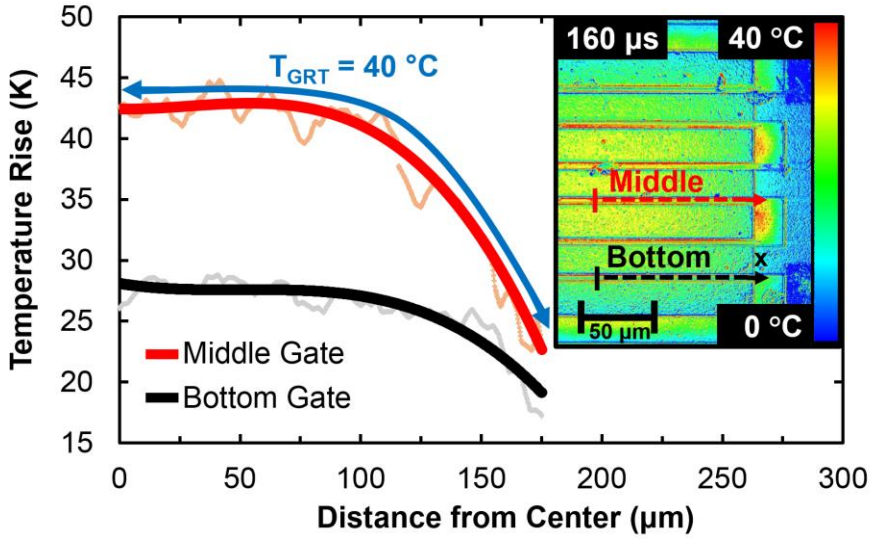



**Figure 43: Temperature profile along gate width of middle gate finger and bottom gate finger. Temperature profiles were extracted from thermal image measured by Transient Thermoreflectance Imaging using a 20x lens. The blue line represents the averaged area that device was biased for a 400 μs period with a 40% duty cycle.**

The noise associated with the raw temperature data in Figure 43 highlights the drawback of using a lower magnification objective. Noting the gate length is approximately

1 μm and the CCD resolution is 274 nm/pixel (for a 20x objective), it is difficult to resolve for the change in thermoreflectance in these areas of low signal to noise ratio. For this reason, a second order polynomial is fitted to the acquired data to characterize the temperature distribution along the gate width. To improve the signal to noise ratio, a higher magnification lens is necessary as shown in Figure 41.

To further investigate the device's thermal dynamics, the temperature profiles of the different regions (using a 100x magnification) are monitored by TTI and plotted against each other in Figure 44.

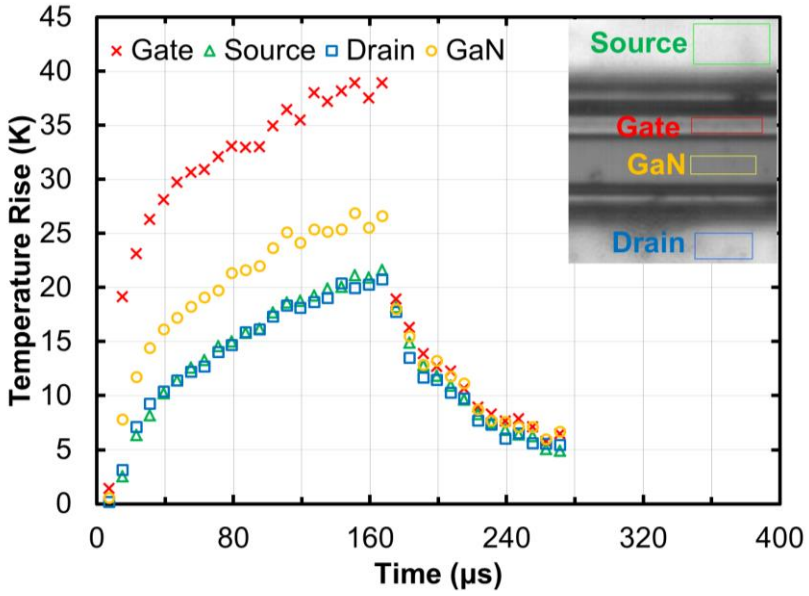



**Figure 44: Temperature profile monitored by transient thermoreflectance imaging, TTI, of different regions across device for a duty cycle of 40%.**

Comparing the temperature rise of the gate metal (40 K) to the GaN channel (25 K), a large temperature gradient is observed. Since the hotspot typically occurs right under the gate in the GaN layer, the temperature of the GaN would be expected to be similar to the gate metal as shown in Chapter 2 under steady state conditions. The discrepancy

between the two values measured by TTI questions the accuracy of applying TTI to non-metal regions such as the GaN channel. It is important to remember that the energy of the 405 nm LED is below the bandgap of GaN which signifies that the excitation source wavelength is not fully absorbed in the GaN. Furthermore, the addition of a SiN passivation layer can contribute to the uncertainty in the thermoreflectance measurement due to thin film interference. Overall, these results highlight the need for the verification of the temperatures extracted from GaN region when using TTI.

### *4.2.5 Development of UV Thermoreflectance Imaging*

To enable the accurate characterization of the GaN channel using TTI, it was determined that UV wavelength LEDs, comparable to the bandgap of GaN, were necessary to obtain a strong GaN thermoreflectance signal. A study on unpassivated AlGaN/GaN HEMTs on a Si substrate was conducted to verify the accuracy of using such wavelengths (340/365 nm). Without the passivation, the uncertainty of thin film interference could be neglected and the temperature rise obtained from the Gate metal via visible wavelengths (470/530 nm) could be directly compared to the UV TTI results. The devices tested were two fingered devices with a 42 μm gate width and have a similar stack configuration as the GaN on Superlattice (SL) structure described in [96]. To ensure linearity of the thermoreflectance coefficient, the change in reflectivity, ($\Delta R/R$) was measured at different temperature rises. Using a 530 nm LED source and measuring the thermoreflectance on the gate metal (spatially averaged along the gate width), a $C_{th}$ of $-1.74 \times 10^{-4}$ $°C^{-1}$ was measured. For the GaN channel, a $C_{th}$ of $-9.6 \times 10^{-4}$ $°C^{-1}$ was measured using a 365 nm LED. The fittings for these two coefficients are plotted in Figure 45.

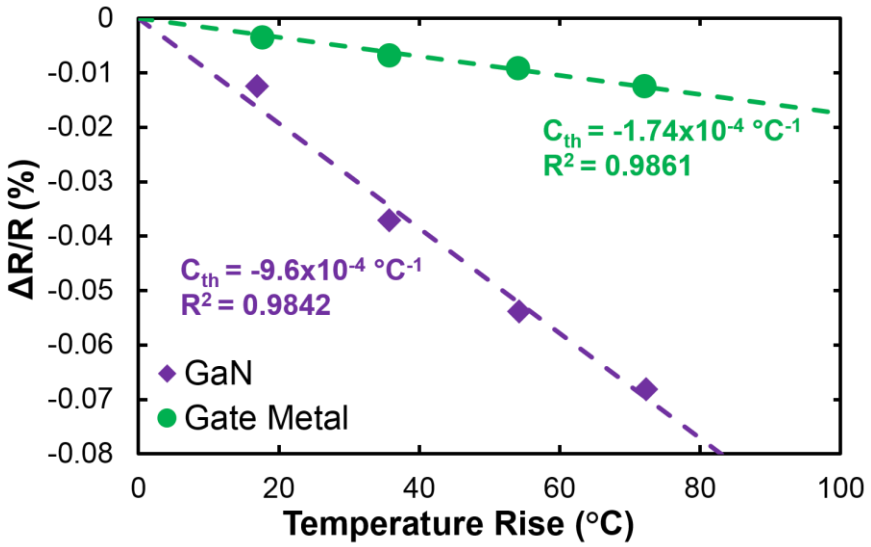



**Figure 45: Linear temperature dependence of the gate metal thermoreflectance signal using a 530 nm LED source and the GaN channel region using a 365 nm LED source.**

Applying the respective $C_{th}$ measured, the temperature mappings between the four wavelengths (340/365/470/530 nm) were compared and are shown in Figure 46. A 20 V pulse was applied to the drain with a 10% duty cycle (100-µs period) while a constant bias was applied to the gate. To account for drain current variation due to electron excitation by UV illumination, the gate bias was adjusted to ensure identical power dissipation across the device for every LED used. The effect of UV illumination on the drain current is possible to detect in contrast to quantifying this variation when using UV Raman. This is because the UV illumination is uniformly distributed across the device whereas UV Raman is locally exciting the channel at the point where the laser is focused. A peak power density of 3.6 W/mm (during the ON state when 20 V is applied to the drain bias) was dissipated across the device for all measurements. A 10 µs delay was applied to ensure that the gate bias was applied before the drain bias.

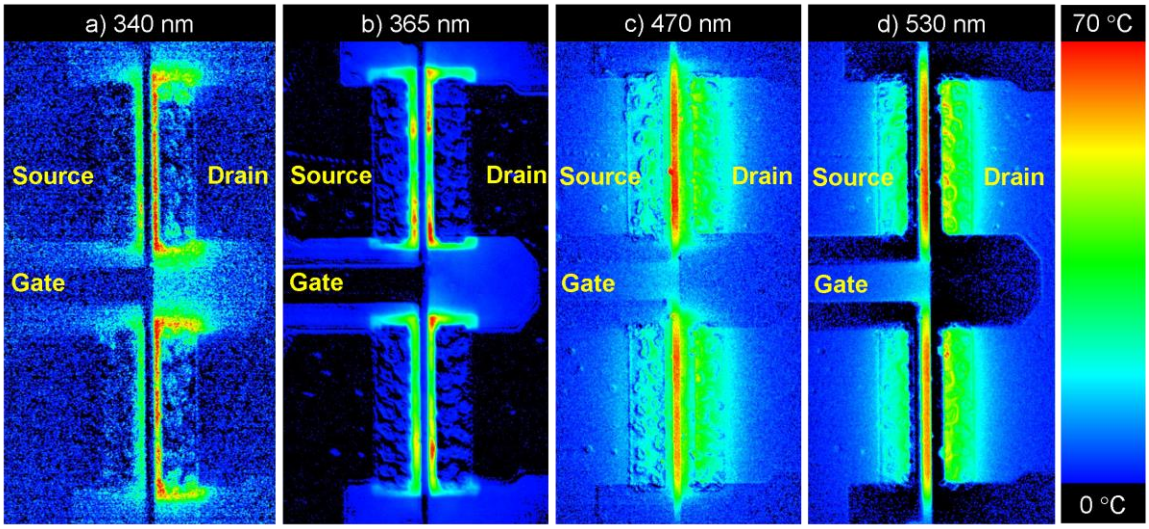



**Figure 46: Transient thermoreflectance imaging of 2x42 µm GaN/Si HEMT using different wavelength LED excitation sources. Near UV wavelengths: a) 340nm and b) 365 nm resulted in strong temperature mappings of the GaN Channel region while longer wavelengths: c) 470 nm and d) 530 nm showed a clear temperature mapping of the gate metal.**

For the initial comparison between all wavelengths, a 50x/0.5NA objective was used. As shown in Figure 46, images were taken near the end of the drain pulse when the device exhibits its maximum temperature. Overall, there is close agreement between the mapping of the gate metal measured by the 470 nm and 530 nm LED resulting in a temperature rise near 70 °C. Symmetric temperature distributions along the gate width are observed for both wavelengths. Using the single $C_{th}$ suitable for the gate metal, no significant thermoreflectance change is observed across the GaN channel for the 530 nm LED source (Figure 46d). In contrast, a temperature rise is observed across the channel for the 470 nm LED source (Figure 46c) despite it being a wavelength significantly below the bandgap of GaN. The signal is thus attributed to the silicon substrate in which the 470 nm wavelength is being absorbed. While the 530 nm wavelength is also absorbed in the Si, it does not result in a large thermoreflectance signal. Overall for the 470 nm excitation source, the thermoreflectance signal originating from the silicon decreases the signal to

noise ratio of the Gate metal thermoreflectance making it a less suitable wavelength for evaluating the gate metal temperature.

The comparison of the GaN channel mapping between the 340 nm and 365 nm highlights significant differences between the measurements. The averaged $C_{th}$ obtained for the 340 nm was measured to be $1.5x10^{-4}$ $°C^{-1}$, an order of magnitude lower than the coefficient extracted for the 365 nm (Figure 45). Due to this weak temperature dependence, a low signal to noise ratio is observed in contrast to the 365 nm temperature mapping. The temperature profile along the gate width, however, appears to be less uniform for the 365 nm image resulting in temperature spikes across the channel. Similar non uniformities were observed in [97] when using a 467 nm excitation source and were attributed to defects in the GaN. The absence of the spikes in the 340 nm LED image, however suggest a wavelength dependence to this phenomenon and can be potentially explained by the near zero residual stress found in the GaN channel [14].The bandgap of strain free GaN has been estimated to be 3.418 eV [98] corresponding to a wavelength of 362.7 nm. Due to the broad spectrum of the 365 nm LED used (Full Width Half Max of 7.5 nm), the thermoreflectance signal detected by the CCD will thus be a combination of absorbed light in the GaN in addition to reflection from lower layers such as silicon. While the GaN channel residual stress for this particular device has, on average, been measured to be near zero, defects formed during growth and processing will cause slight changes in the residual stress and consequently non-uniformities across the channel. This non-uniformity will translate into a small shift in the bandgap and ultimately a non-uniform $C_{th}$ across the GaN channel (shown in Figure 47a). The $C_{th}$ measured by the 340 nm, however, will not be affected by this phenomenon due to having an energy level far above the bandgap of GaN.

Despite the 340 nm LED showing a more uniform temperature distribution, special UV optics are necessary to transmit sufficient light through the Microsanj and consequently limits the objective magnification to 39x. Furthermore, the maximum power of the 340 nm LED was limited to 33% of the power capacity of the 365 nm LED, making the 365 nm LED suitable for higher magnification measurements. A 100x.0.8NA objective was subsequently used for TTI measurements with both the 365 nm and 530 nm LED. To reduce the bandwidth of the 365 nm LED and effectively the variation in $C_{th}$, a 365 nm bandpass filter was placed in front of the LED.

### *4.2.6 Improvement of Transient Thermoreflectance Imaging*

To overcome the non-uniformity of the $C_{th}$ in the GaN channel, a pixel by pixel calibration was used to apply the appropriate coefficient to each pixel. The $C_{th}$ map of the device using an 100x magnification is shown in Figure 47a and confirms the non-uniformity of the coefficient across the GaN channel. As previously discussed, the application of a single $C_{th}$ to all pixels will cause errors in the temperature distribution with large spikes in areas where the $C_{th}$ significantly varies. Figure 47b highlights this phenomenon showing a direct correlation between the temperature spikes and change in the $C_{th}$. Using the piezoelectric stage and adjusting the light intensity to match the pixel intensity of the thermal measurement, a point by point calibration is applied to the TTI image in Figure 47c. A significant improvement of the thermal image is obtained removing most areas of non-uniformities and showing uniform heating along the gate on the drain edge. A few small areas of non-uniformities still exist in the image but are attributed to either small particles laying on the surface of the channel or low intensity pixels near the edge of the ohmic and Schottky contacts.

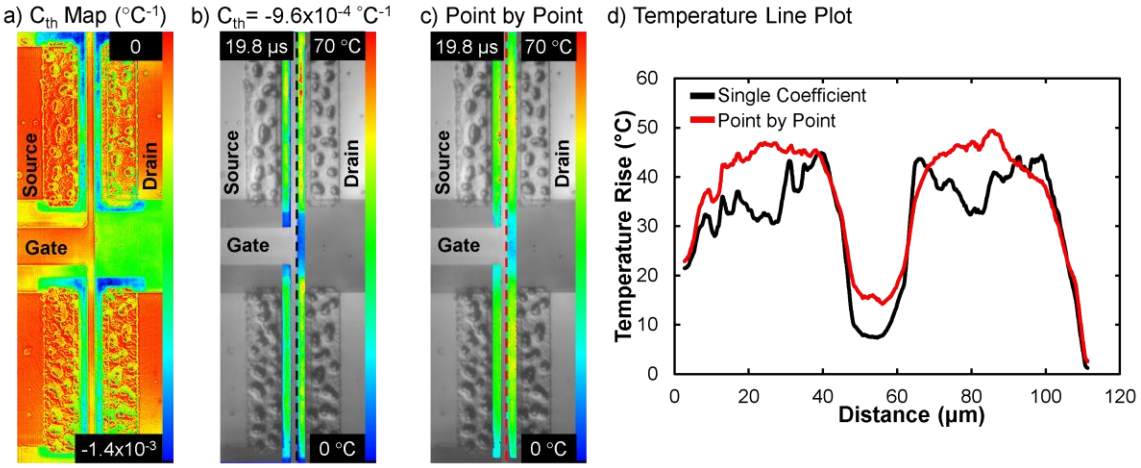



**Figure 47: a) Thermoreflectance coefficient mapping ($C_{th}$) of GaN/Si HEMT using a 365 nm LED source. Resulting GaN channel temperature profile when applying b) a single $C_{th}$ to all pixels c) point by point $C_{th}$ calibration d) Temperature line plot of GaN channel near the drain edge along the gate width.**

A line plot in the GaN channel on the drain edge was taken from the top of the device to the bottom to monitor the temperature profile along the gate width (Figure 47d). The improvement of the temperature profile measured when using the point by point calibration is shown and captures the parabolic thermal profile across the device. The significance of these results demonstrates the necessity of a point by point calibration when measuring the thermoreflectance of semiconductors with excitation wavelengths near the bandgap of the material.

Now having the ability to accurately measure the thermoreflectance change in the GaN channel region, a direct comparison to the gate metal temperature can be made. A full transient analysis of the GaN HEMT was performed and plotted in Figure 48. Averaged regions near the center, of dimensions 0.8 x 0.8 µm, were extracted from the thermal map for the gate metal as well the GaN channel region on both the drain and source edge. Noting

a 10 μs delay before the drain bias is applied, the temperature of all regions increases rapidly within the first two microseconds before reaching a steady state temperature.

Using a single-term exponential model to fit to the temperature rise and decay, thermal times constants associated with the gate metal and GaN can be extracted. The thermal time constant associated with GaN temperature rise was found to be 0.72 μs in contrast to 0.92 μs time constant extracted from the gate metal temperature rise. The shorter time scale associated with the GaN is to be expected as the origin of localized Joule heating occurs in the GaN. A similar trend is found in the temperature decay where a longer thermal time constant is extracted for the gate metal. Further analysis of the device's transient thermal dynamics can be conducted using multiple time constants to fully capture the temperature rise and decay [61].

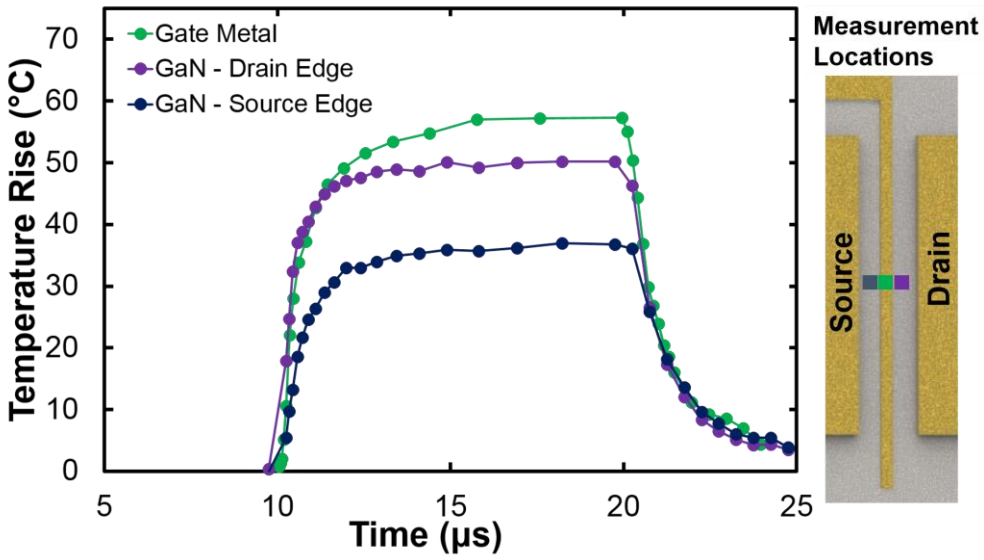



**Figure 48: Transient thermal response of GaN/Si measured by thermoreflectance imaging. Gate metal temperature was monitored using a 530 nm LED and GaN channel temperatures were measured using 365 nm LED. Temperatures represent averaged temperature over 0.8 x 0.8 μm square in the center of the device.**

Comparing the overall temperature rise, the gate metal temperature reaches a maximum temperature of 57 °C whereas the GaN reaches a maximum temperature of 50 °C. The higher gate metal temperature rise indicates that the hotspot is indeed located under the gate metal and is unable to be captured by the UV TTI measurement of the GaN channel mapping. Comparing the peak temperature rise in the GaN on the drain edge to the source edge, the source edge reaches a temperature rise of 36 °C which corresponds to a 36% decrease in temperature. To fully characterize the temperature distribution across the channel, line plots were extracted at different time intervals and plotted in Figure 49. Second order polynomials were fitted to the raw temperature data in all three regions: the gate to drain side; the gate metal; and the gate to source channel. Due to edge effects, the data near the gate edge in the GaN channel were not included in the fittings.

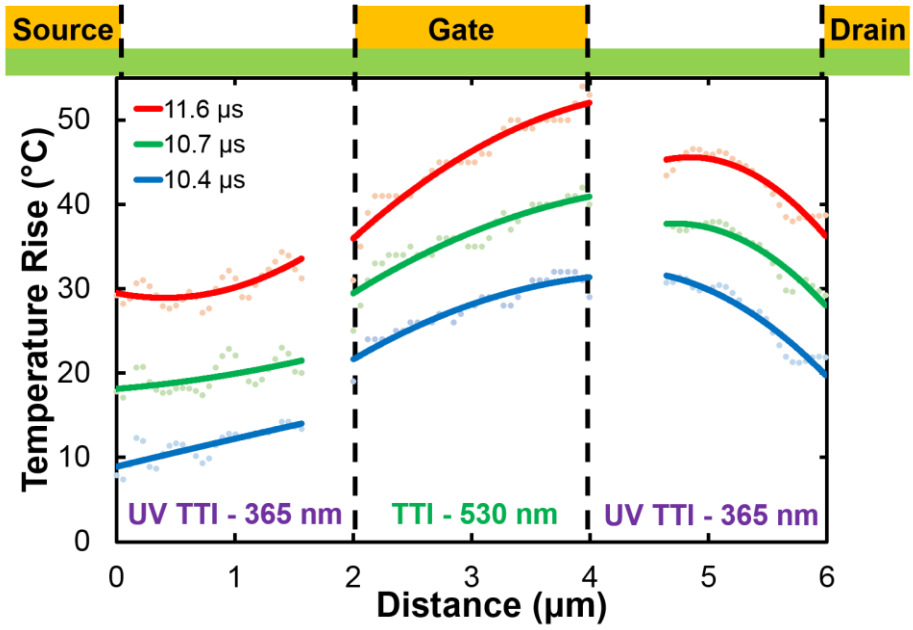



**Figure 49: GaN HEMT channel temperature mapping between source and drain using UV thermoreflectance (365 nm) for the GaN region and visible thermoreflectance (530 nm) for the gate metal. The development of the temperature profile over time is shown. Joule heating is begins at 10 µs when the drain bias is applied. Second order polynomials were fitted and plotted to highlight the temperature gradient across the channel.**

A clear contrast between the temperature gradients across the different regions is presented. The temperature gradient between the gate and source results in a 2 °C rise while a maximum 10 °C rise is measured between the gate and drain. An even larger gradient is observed across the gate metal (15 °C). The large gradient between the gate and drain indicates that the hotspot is located near the gate metal on the drain side edge. This distribution is confirmed in literature where the Joule heating profile has been found to be a function of the electrical field [9]. Overall, further investigation is necessary to verify the accuracy of the channel temperature mapping and identify the position of the hotspot. Electrothermal numerical models can be implemented to obtain a full temperature mapping. To compare the model to multiple experimental data sets, the devices can be operated at different gate and drain voltages which will alter the temperature profile due to the bias dependent Joule heating distribution.

### *4.2.7 Thin Film Interference*

The TTI results highlight the need for gaining a deeper understanding of the thermoreflectance signal originating from an area where multiple thin film layers are present. The passivation layers can strongly influence thermoreflectance signals due to interference among multiply reflected beams (thin film interference). Most films have relatively smooth surfaces with roughness smaller than the typical wavelength of the probe. To fully understand the GaN thermoreflectance signal, a developed technique should be used to verify the temperature estimated in the region. An initial study was carried out using Raman to measure the temperature rise of a passivated versus un passivated device for the same power dissipations. Raman temperature mappings were conducted by taking measurements along channel from 0 to 28 μm in 2 μm steps and moving from 0 to 80 μm

in 5 μm steps along the vertical direction. To estimate the temperature rise, a map was performed prior to and after biasing the device to determine the initial reference peak position. Since the Raman capabilities in the lab are limited to just DC measurements, steady state thermoreflectance images were taken for comparison and are shown in Figure 50. The passivated and unpassivated devices were biased and 17.5V and 21.5 V respectively. This amounted to a power dissipation of approximately 1.1 W. Using a pixel by pixel calibration, good agreement is found between the two measurements for the passivated TLM. The temperature distribution across the TLM appears to be mostly uniform with a slight bias towards the positive terminal of the TLM. This gradient may be due to the age of the TLMs and operating in the saturated region of the IV curve.

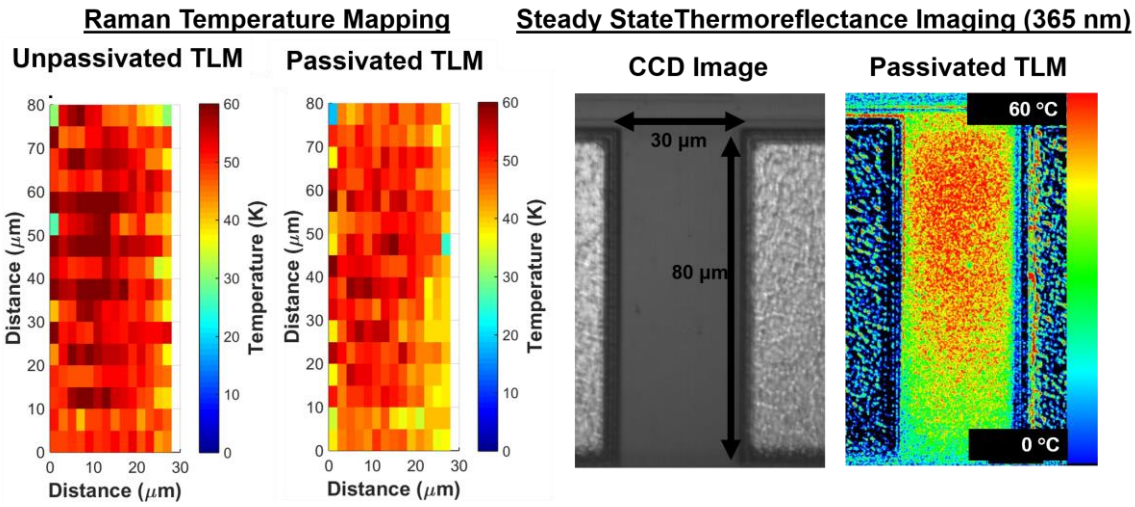



**Figure 50: Comparison of steady state temperature mapping of GaN/SiC TLM performed by Raman thermometry and thermoreflectance imaging. Unpassivated device was fabricated by etching the passivation. Both devices were bias at approximately 1.1 W. No steady state thermoreflectance imaging of the unpassivated device could be measured.**

A steady thermoreflectance image of the unpassivated device was unable to be achieved. This phenomenon may be attributed to the low thermoreflectance signal attributed to the surface and highlights the need of the lock in technique used in TTI to

detect the small signal. To further investigate the difference between the two devices, thermoreflectance coefficient mappings of the two devices were performed. The coefficients for the passivated and passivated device were found to be -1.8x10$^{-4}$ °C$^{-1}$ and -1x10$^{-4}$ °C$^{-1}$ respectively. This confirms the stronger thermoreflectance signal detected under steady state imaging for the passivated device. The change in the thermoreflectance signal of the unpassivated device could be detected under pulsed biasing using TTI. A comparison of the transient thermal profiles is shown in Figure 51. The devices were biased for 250 µs period with a 20% duty cycle. The average power dissipated was approximately 460 mW. Overall, both devices reached the same temperature rise and the temperature profiles are similar to the Raman temperature profiles shown in Figure 50.

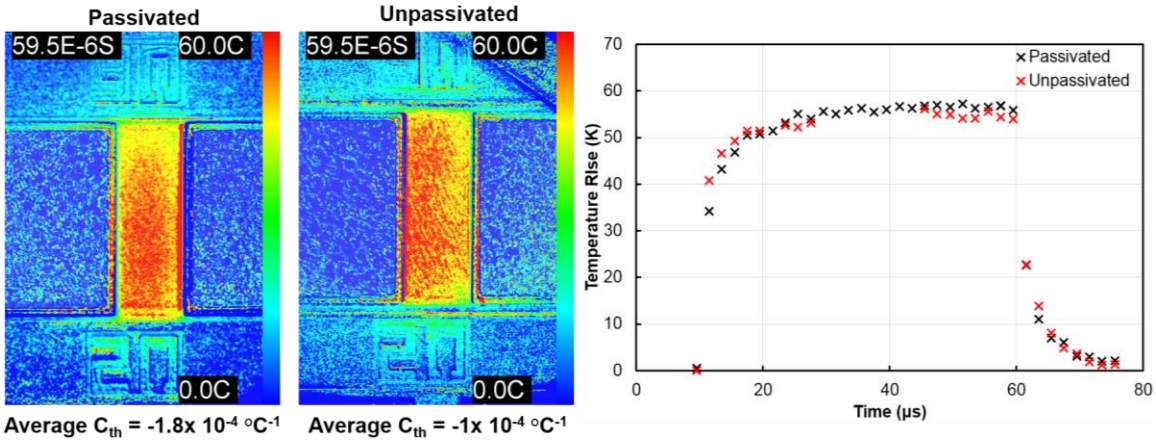



**Figure 51: Comparison of transient thermal profiles of GaN/SiC TLMs. Devices were biased for a 250 µs period with a 20% duty cycle. An approximated averaged power of 460 mW was dissipated across both devices. Thermal images are shown at 60 µs (end of the ON pulse).**

The increase in the thermoreflectance coefficient when a passivation layer is added suggests that thin film interference has a significant effect on the thermoreflectance signal detected. Previous research has been conducted on measuring the reflection and transmission spectra of multiple thin films [99, 100]. A sample of a reflection spectra

measured for an AlGaN/GaN bilayer grown on Sapphire is shown in Figure 52a. It can be observed, that even with the absence of a passivation layer, the reflection from the surface exhibits thin film interference. The thermoreflectance coefficient of the structured studied must therefore be highly sensitive to changes in wavelength of the excitation. To confirm this, a wavelength sweep was performed using a monochromator on both of the TLMs (Figure 52b). Both surfaces are shown to have high wavelength dependence and drastic changes in the coefficient are observed even with the change of a few nanometers.

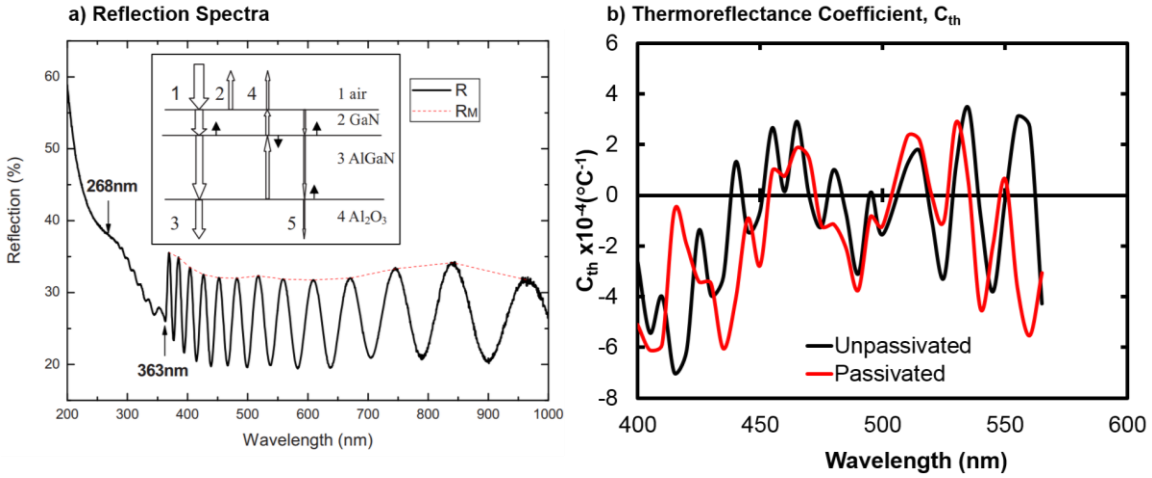



**Figure 52: a) Reflection spectrum and envelope of maxima wavelengths of GaN/AlGaN bilayer on Sapphire (adapted from [99]) b) Thermoreflectance coefficient, $C_{th}$, measured at different wavelengths for both GaN/SiC TLMs with and with and without passivation.**

The full width half max (FWHM) of the LED (±12 nm) consequently contributes the signal noise ratio associated with the thermoreflectance signal. Reducing this deviation will reduce the number of different wavelengths being reflected within the devices and will reduce the amount of destructive interference. A bandpass filter was thus placed immediately after the LED to reduce the full width half max (FWHM) of the LED emission. The results of this study showed a dramatic increase in the thermoreflectance coefficient.

## 4.3 Summary and Conclusions

Overall, TTI shows close agreement with the transient GRT results. For a constant drain and gate bias, the gate metal temperature rise and decay under pulsed biasing is monitored with varying duty cycles from 10 to 40%. The results demonstrate the need of using an advanced autofocusing function to extract the correct thermoreflectance coefficient of the passivated gate metal. Providing an accurate method to employ TTI enables the possibility of extracting thermal time constants to better understand the thermal properties of GaN HEMTs. In contrast to transient GRT, TTI has proven to be advantageous for temperature mappings of the device providing submicron spatial resolution. These mapping techniques will enable direct evaluation of adjusting device geometries such as gate to gate spacing and gate width to improve thermal spreading throughout the device.

The accuracy of UV thermoreflectance imaging to monitor the temperature rise in the channel region of a GaN HEMT has been verified for the first time via the comparison of visible thermoreflectance of the gate metal. A pixel by pixel calibration method is proposed to account for the variability of the thermoreflectance coefficient across different regions of the GaN. This point by point procedure is essential for UV thermoreflectance imaging when using a LED excitation sources near the bandgap of the semiconductor. For sub-micron spatial resolution, magnification objectives up to 100x are shown to accurately map the temperature distribution of the GaN channel. In comparison to Raman thermometry, CCD based transient thermoreflectance imaging is proven to be an accurate and effective method to measure the temperature distribution of both the gate metal and GaN. Further application of this technique can be used to verify numerical models predicting the effect of bias conditions and material selection on the peak temperature.

# CHAPTER 5. UNDERSTANDING THE VERTICAL TEMPERATURE GRADIENT IN GAN BASED ELECTRONICS

Content in the chapter (figures and text) adapted from:

1. G. Pavlidis, *et al.*, "Steady State and Transient Thermal Characterization of Vertical GaN PIN Diodes," in ASME 2017 InterPACK, pp. V001T05A011 [101]

## 5.1 Overview and Approach

For lateral devices, channel temperature mappings are usually performed from either the top or bottom side of the device and then matched to an electro-thermal simulation. No direct measurement of the temperature distribution along its depth has been shown. Using transient thermoreflectance imaging, a cross sectional thermal mapping technique for GaN HEMTs is proposed. The vertical temperature gradient in vertical GaN PIN diodes is also assess using a combination of Raman thermometry and TTI. The feasibility of creating cross sectional samples has been shown by AFRL [102, 103]. Direct mapping of temperature gradients across interfaces will give deeper insight into how to improve the thermal boundary resistance between epitaxial layers. Until now, theoretical and atomistic level models have been developed to characterize the heat transport across interfaces. Having the ability to directly compare these models to experimental data, new models can be developed to help understand the effect of defects, roughness, anharmonicity and interdiffusion on these interfaces. This technique will also help me evaluate new patterned interfaces that could improve thermal interfaces.

## 5.2 Cross Sectioned GaN/SiC HEMTs

AlGaN/GaN HEMTs on a SiC substrate were cross sectioned by AFRL using a combination of a wafer saw and focused ion beam polishing techniques [104]. Three two fingered devices were cross sectioned consisting of two source connected field plated devices and one non field plated device. The devices were packaged and wirebonded to a CuW StratEdge package as shown in Figure 53. Due to the cross sectioning, the gate width varied slightly between the devices. For the device studied in this Chapter (Figure 53), a gate width of 335 ± 1 μm was measured. To reduce the amount of noise in the thermoreflectance signal associated with multiple layers with different thickness in the region of interest, the device without a field plate was initially assessed.

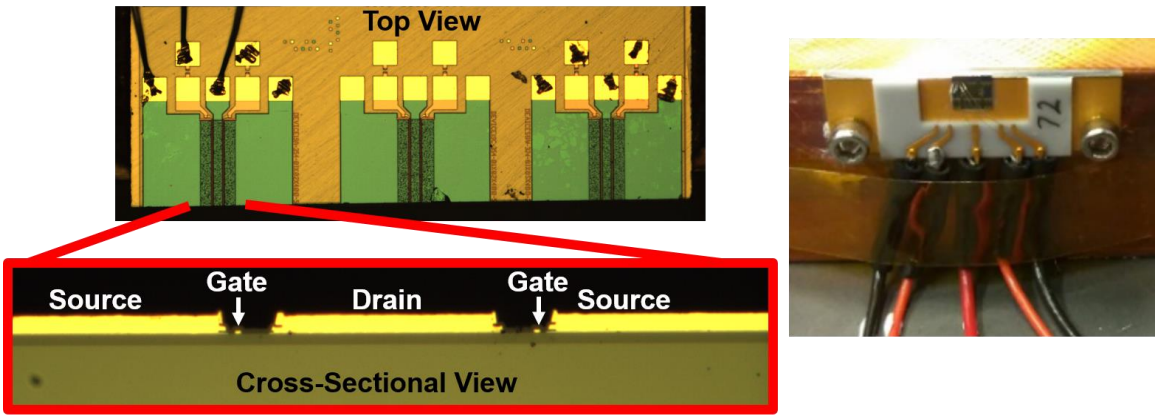



**Figure 53: Optical image of GaN/SiC HEMTs measured for transient thermal analysis. Devices were wire bonded and mounted to a CuW package which was subsequently mound on a copper plate to ensure adequate thermal dissipation.**

### *5.2.1 Plan View TTI*

Prior to performing cross sectional TTI measurements of the HEMTs, the devices were measured from the top side to monitor the temperature distribution along the gate width. Since the devices were cross sectioned, the path of heat conduction that normally

existed surrounding the whole HEMT was now removed. It was hypothesized that significant more heating will occur at the edge of the die where localized Joule heating now occurs. This may result in an alteration of the Joule heating profile and excessively high temperatures at the edge of the device which would not represent normal HEMT operation. 20x magnification TTI measurements were conducted using a 470 nm LED to monitor the temperature rise of the gate metal. A calibration was performed and the $C_{th}$ of the gate metal was found to be $-1x10^{-4}$ °$C^{-1}$. The devices were pulsed biased at a varying drain bias for a constant gate bias of 0 V. The duty cycle was 10% for a 100 µs period. Using an LED pulse width of 140 ns, images were taken at a 2 and 10 µs delay and are shown in Figure 54.

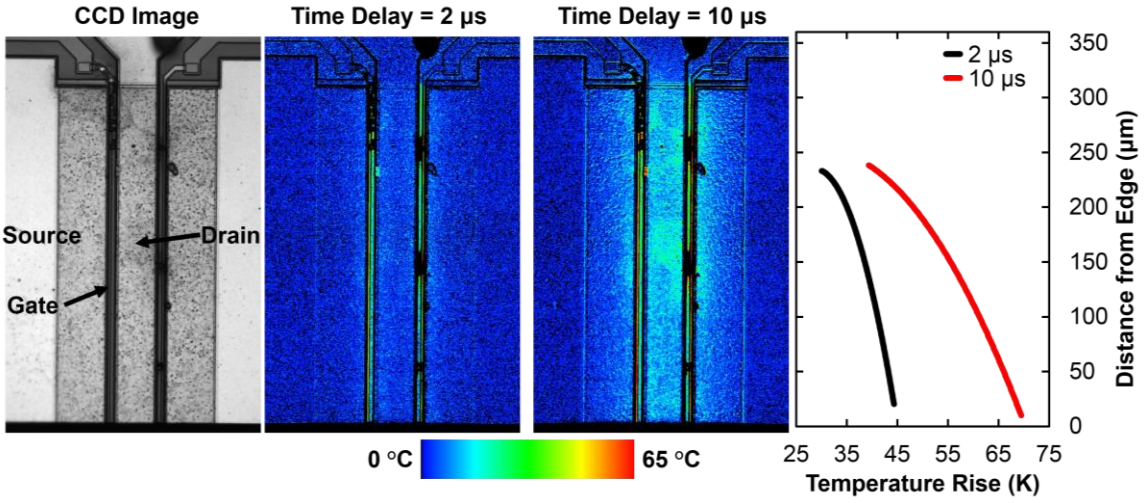



**Figure 54: Top view TTI of cross sectioned GaN/SiC using a 20x magnification. A 470 nm LED excitation was used to obtain the temperature of the gate metal. Device was biased at $V_{ds}$ = 7.5 V & $V_{gs}$ = 0 V.**

At 2 µs, the heating is still localized in the GaN near the gate metal and can be used to determine if there is any change in thermal profile due to cross sectioning. Mapping the temperature distribution across the gate metal, a 15 K temperature gradient is observed from the edge of the cross sectioned device to the opposite end of the device. This gradient

appears to be parabolic and is similar to the temperature distribution observed in the GRT GaN/SiC device (Figure 11). It should be noted that the gradient increased to 40 K at the end of the drain pulse (10 µs). Upon review, no irregularities are observed in the temperature distribution along the gate width and the concern of the cross sectioning altering the thermal distribution was dismissed.

The magnification was increased to 100x to obtain a better temperature estimation of the gate metal and to enable a direct comparison of 100x TTI measurement in the cross-sectional view. The TTI maps taken at 2 and 10 µs delays are shown in Figure 55.

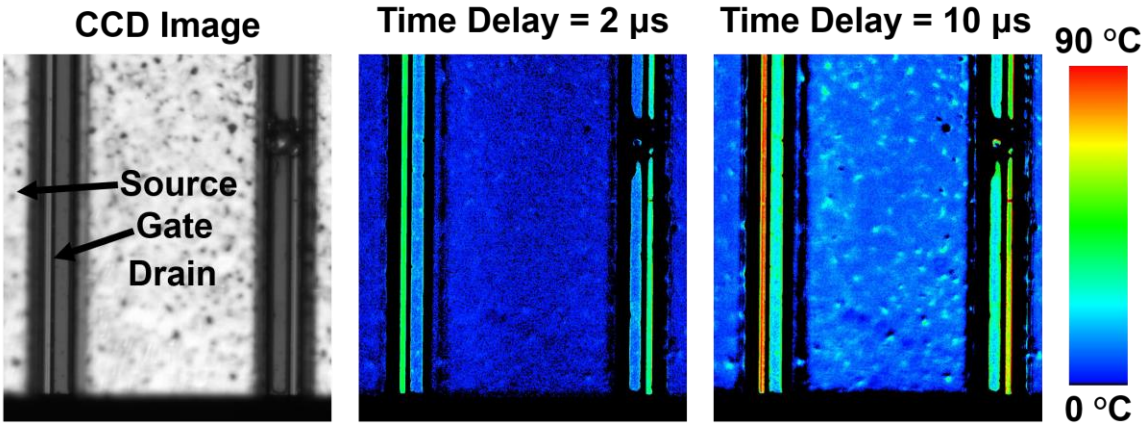



**Figure 55: Top view TTI of cross sectioned GaN/SiC using a 100x magnification. A 470 nm LED excitation was used to obtain the temperature of the gate metal.**

To confirm there was no asymmetry between the two gate fingers, the gate metal temperature rise of both gates was measured to approximately be 80 K at the edge of the device. Comparing this to the 20x TTI measurements, the temperature rise of the gate metal is shown to increase by 10 K. The discrepancy between the values can be explained by the low signal to noise ratio obtained via 20x TTI measurements (discussed in Chapter 4). For direct comparison to the cross-sectional view TTI measurements, the temperature rise

measured by the 100x objective was thus taken. Temperature rises were measured at different power densities to ensure a directly proportional temperature power dependence was observed.

### *5.2.2 Cross Sectional TTI*

The overall objective of performing TTI on the cross-sectional devices was to develop a method to accurately measure the temperature of the GaN channel and determine the bias dependence of the Joule heating profile in GaN HEMTs. To achieve this, the temperature associated with the GaN must be verified by probing a region where the thermoreflectance coefficient is well known. The gate metal resulted in a strong thermoreflectance coefficient and was thus used to compare to the UV TTI measurements performed on the GaN channel. Due to the gate length being less than 1 μm, a 250x objective was used to detect the temperature rise of the gate metal. Despite using a high magnification objective that results in going beyond the diffraction limit, it was still possible to optically differentiate the gate region to the rest of the device.

Large variations were observed, however, when attempting to measure the thermoreflectance coefficient of the gate metal region using a 250x objective due to the small feature size of the gate. For this reason, it was decided not to perform pixel by pixel calibrations. It should be noted that the coefficient did result in a positive value ranging between 0.5-1 x $10^{-4}$ $°C^{-1}$. The sign of the coefficient is opposite to the coefficient measured from the top view. The difference in the sign of the coefficient demonstrates the effect of thin film interference due to the presence of the passivation layer. In the cross-sectional case, the illumination source is reflected directly off the metal without having to transmit

through the passivation. Considering the gate metal is mainly composed of gold, literature reports the thermoreflectance coefficient associated with unpassivated gold is typically around 1-2 x $10^{-4}$ $°C^{-1}$ for a 470 nm excitation source [67]. This confirms the validity of using a positive coefficient for the gate metal when estimating the temperature rise using a 470 nm LED. A value of 1 x $10^{-4}$ $°C^{-1}$ was thus used when performing TTI measurements.

### *5.2.3 Power Dependence*

The temperature power dependence of the GaN HEMT was first evaluated to determine whether the signal obtained from the gate metal region via TTI was accurate. As previously done from the top view, the device was biased for a 100 µs period with a 10% duty cycle and the drain bias was varied from 3.7 to 7.5 V. The cross sectional TTI maps taken at 2 and 10 µs delays for the right side gate are shown in Figure 56.

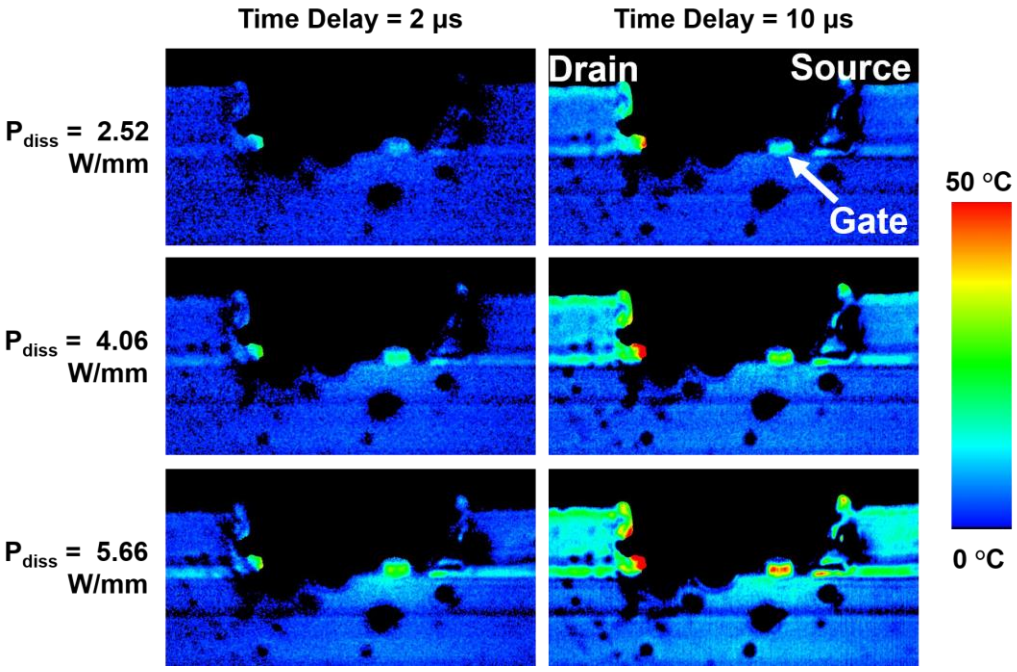



**Figure 56: Cross Sectional TTI of the gate metal temperature rise using a 250x objective. Device was biased at different power densities by varying the drain voltage from 3.7 to 7.5 V.**

TTI measurements with a 250x objective were taken for both gates. The left gate, however, contained particles on the surface and made the image of the full gate difficult. In contrast, the UV TTI measurements are presented for the left gate region as there are significantly less particles present in that region. The results of the gate metal showed an increase in temperature rise with increasing power density and even highlighted the temperature distribution across the t-gate structure. Viewing the thermal image at 10 µs and 5.66 W/mm, the peak spots of the temperature are shown to be located at the ends of the t-gate on the upper side of the whole gate structure. This distribution demonstrates that the heat generated next to the gate is primarily conducted downwards into the substrate via the GaN layer. This outcome is to be expected as the thermal conductivity of the SiN passivation above the gate metal exhibits a much lower thermal conductivity.

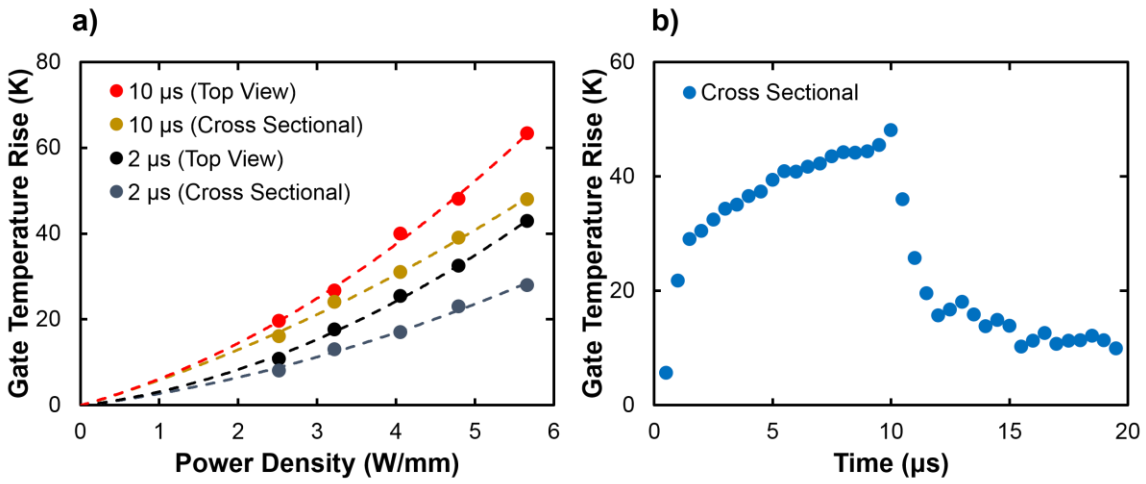



**Figure 57: a) Comparison of temperature response with varying power density of gate metal temperature in HEMT measured by TTI from two different orientations: top side and cross sectional side b) Transient temperature profile measured from cross sectional view.**

Extracting the temperatures of the gate metal for a given power density. The temperature-power plots can be compared for both the top view and cross-sectional view

measurements. The results are contrasted in Figure 57a and show a difference in temperature measured when performing TTI from the different orientations. It should be noted that for all curves, a parabolic temperature power relationship was observed. To analyse the discrepancy between these temperature values, the effect of the LED pulse width should be considered. The LED pulse width used for the cross-sectional measurements was 480 ns. This value was longer than the pulse width applied during the top view measurements (140 ns) and may create discrepancies between the temperatures estimated from different orientations. Comparing the exact averaging time periods between the two measurements at a 10 μs delay: the top view measurement is averaged between 9.86 to 10 μs while the cross-sectional measurement is between 9.52 to 10 μs. The difference in average time lengths should have a more significant effect during the first few microseconds after the drain bias is applied but at longer time lengths, such as 10 μs, the device will have reached a closer value to its steady state, and the difference between the two values should be minimized. This phenomenon is highlighted at higher power densities where the temperature difference between the two orientations measured at 10 μs becomes smaller than those measured at 2 μs. The temperature difference at 10 μs is still, however, significant (11 K). Performing a full transient sweep from the cross-sectional side (Figure 57b), the gate temperature is shown to not have reached a steady state value within the 10 μs pulse implying that a longer LED pulse width will still average over a larger temperature rise.

Another contributing factor to the discrepancy which was deemed more significant was the uncertainty in the thermoreflectance coefficient. Having already mentioned the difficulties associated with obtaining the thermoreflectance coefficient using a 250x

objective, an approximate value was selected similar to the value associated with unpassivated gold. The error associated with this coefficient was estimated to be on the order of 40% which can account for the temperature difference currently observed between the temperatures plotted in Figure 57a. It was concluded that a more accurate method to estimate the thermoreflectance coefficient for this device was necessary to validate the accuracy of the temperature values obtained.

Cross-sectional UV TTI measurements using a 100x objective and a 365 nm LED were still performed to determine the viability of measuring the GaN channel temperature in a cross-sectional configuration. Operating the device at the same biasing conditions, the TTI maps of the GaN channel are plotted in Figure 58 for the two time delays. Since the optics of the system are not optimized for UV wavelengths, a longer LED pulse width was necessary in order to obtain a significant thermoreflectance signal from the GaN channel. An LED pulse width of 720 ns was thus applied in combination with a 365 nm bandpass filter to reduce the broad spectrum of the LED (the effect of the bandpass is discussed further in detail in the following chapter).

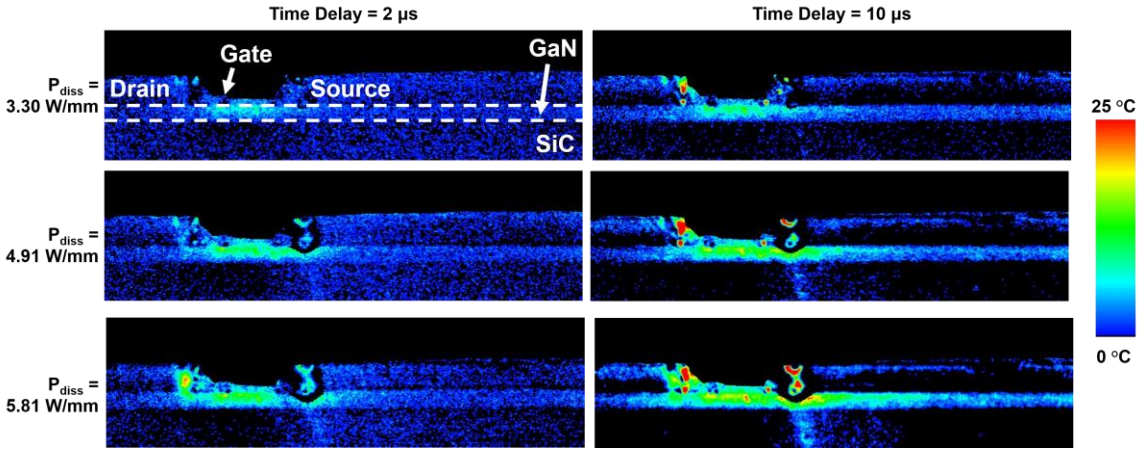



**Figure 58: Cross sectional UV TTI images of a GaN/SiC at varying power densities and time delay. A 365 nm LED was used as an the excitation source.**

The cross sectional temperature distributions achieved via TTI show clearly the highly localized Joule heating that occurs in the GaN HEMT. While this has been shown previously from the top view via numerical simulations, these measurements signify the first ever cross-sectional temperature measurement of a GaN HEMT enabling a full temperature map of the GaN channel. Optical restrictions, such as the gate metal for Raman thermometry, are not faced using this technique. Comparing the temperature distribution at the end of the drain pulse, the heat is shown to dissipate strongly in the lateral direction through the GaN layer. This does not imply, however, that the heat conduction via the substrate is less significant. No change in thermoreflectance was observed in the SiC region and a near zero coefficient was measured during the calibration. Consequently, the temperature of the SiC could not be assessed.

The thermoreflectance coefficient for the GaN was measured to be approximately $-1 \times 10^{-4}$ $°C^{-1}$. Despite it being a larger area than the gate length, the thermoreflectance coefficient was still difficult to measure and large uncertainty was associated with it. Comparing the temperatures achieved by the visible TTI of the gate metal (Figure 59a), the temperatures measured in the GaN layer right below the gate appear to be significantly lower. The temperature of the GaN below the gate can physically not be lower than the gate metal temperature as the Joule heating is generated within the GaN layer. It was concluded that the UV TTI underpredicted the GaN temperature and similar to the 250x gate metal case, a more accurate measurement of the thermoreflectance coefficient associated with the device is necessary. Irrespective of the coefficient, the transient thermal profile of the two regions can be compared (Figure 59b) to differentiate any time constants associated with the temperature rise and decay of the two different regions. The

temperatures have been normalized to the maximum temperature achieved in both region to remove any effects from the absolute value of temperature measured. Upon reviewing Figure 59b, the GaN clearly experienced a faster heating and cooling rate than the gate metal. This is to be expected as the heating occurs in the GaN layer itself. The verification of this confirms that thermoreflectance signal detected is truly associated with the GaN even if the absolute temperature is not correct.

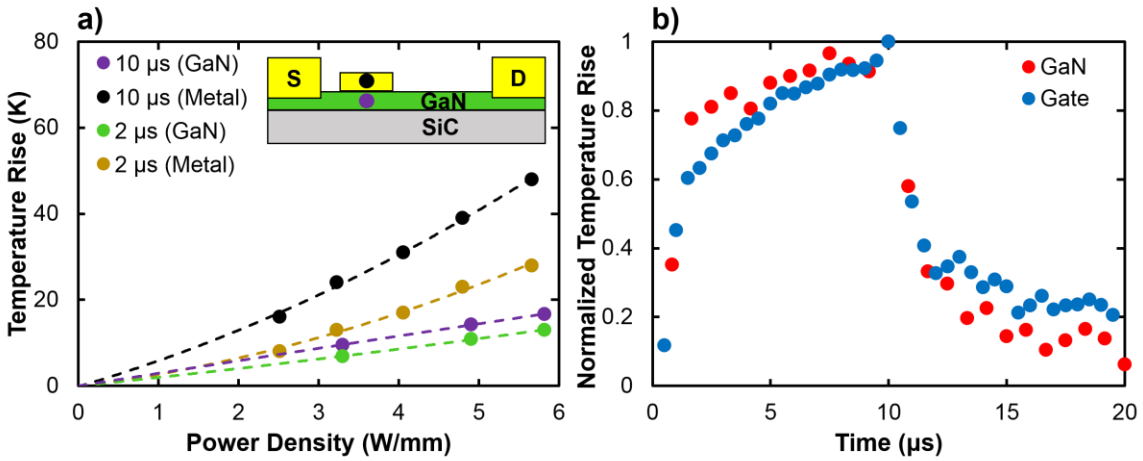



**Figure 59: a) Comparison of temperature response with varying power density of gate metal temperature to GaN channel side b) Transient temperature profile measured from cross sectional view.**

### *5.2.4 Bias Dependence*

The Joule heating profile has been shown via simulations and steady state measurements to be heavily dependent on the electric field [55, 76]. Changing the gate and drain bias, the electric field can be altered and the Joule heating profile will consequently change. Since the thermoreflectance signal obtained via the 365 nm LED excitation source has been shown in the previous section to be attributed to GaN, a bias dependence study was conducted to determine if any changes in the temperature profile could be detected.

To ensure the same power dissipation was applied across all measurements, the gate and drain bias were both adjusted to achieve a peak power density of 3.3 W/mm. The results for three different bias conditions are shown in Figure 60.

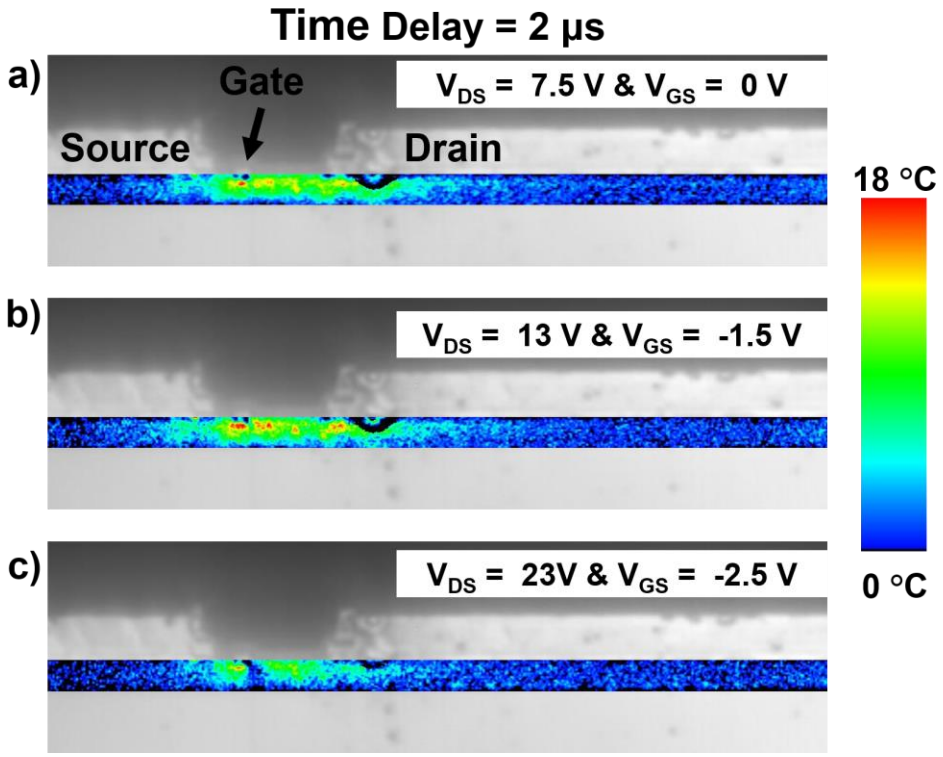



**Figure 60: Bias dependence of temperature distribution across GaN layer in GaN/SiC HEMT.**

The effects of the bias conditions are clearly seen from Figure 60. After 2 µs of the device being turned on, the temperature distribution across the channel is shown to differ. A general trend is observed where the profile is shown to become more localized with increasing drain bias and more negative gate bias. Applying a gate voltage of 0 V, the device is operating in similar conditions to fully open channel conditions (previously explained in Chapter 2) where the heating profile is more spread out across the channel. Applying a more negative voltage such as -2 V, the device transitions to a state closer to pinch-off conditions where a depletion region is formed under the gate. The effect of the

depletion region is clearly seen in Figure 60c where drop in the temperature near the gate on the drain edge is shown.

### *5.2.5 Cross Sectional Raman Thermometry*

Due to the uncertainty in estimating the thermoreflectance coefficient, steady state analysis was performed via Raman thermometry to evaluate the temperature of the GaN. Using a 532 nm laser as an excitation source, strong signals were obtained for the phonon frequencies associated with the A1 (TO) and q-E1 (LO) vibrational modes. The peaks at room temperature agreed well with literature [83, 105] and were measured to be 531.8 $cm^{-1}$ and 741.03 $cm^{-1}$. Typically, the GaN layer is probed along the (0001) crystal growth axis and as previously shown the $E_{2High}$ and $A_1$(LO) phonon frequency are usually detected. The temperature dependence of these frequencies has been well studied and methods to account for the stress using a two peak analysis has been established. Now being unable to detect these peaks, new calibrations were necessary to establish the temperature dependence of the two peak's position as well the peak's Full Width Half Max (FWHM). The device was mounted onto a thermal stage and the peaks were measured at temperatures from 30 °C to 110 °C in 20 °C increments. As shown in Figure 61, linear regression was applied to extract temperature coefficients. The temperature coefficients for the $A_1$ (TO) and q-$E_1$ (LO) peak positions were found to be $K_{A1}$ = -0.01801 ± 0.00046 $cm^{-1}/K$ and $K_{E1}$ = -0.02489 ± 0.00071 $cm^{-1}/K$ respectively. The coefficients for the FWHM were estimated to be $B_{A1}$ = 0.0448 ± 0.00198 $cm^{-1}/K$ and $B_{E1}$ = 0.01102 ± 0.00089 $cm^{-1}/K$. In both cases, the temperature dependence appears mostly linear with a slight parabolic dependence. Comparing to literature, the values appear on the same order of magnitude with the largest discrepancies

found with peak position temperature coefficient of the $A_1$ (TO) mode, $K_{A1}$, which was calculated to be 40% larger [106].

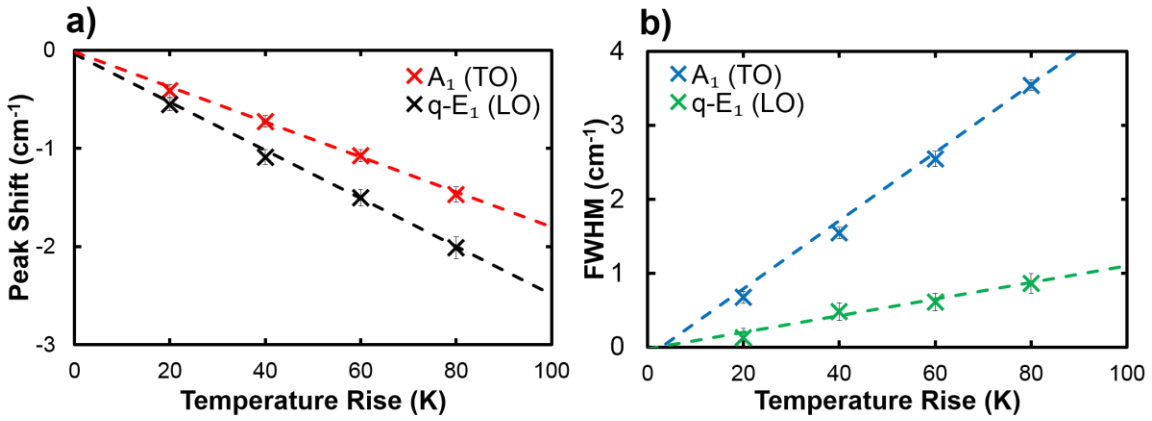



**Figure 61: Temperature dependence of GaN's vibrational modes $A_1$ (TO) and q-$E_1$ (LO) a) peak position and b) full width half max (FWHM). Thermal stage temperature was varied from 30 °C to 110 °C.**

Using the extracted coefficients, the devices was biased a constant $V_{gs}$ = 0 V and the drain bias was varied from 2.4 V to 5.1 V to achieve DC power densities up to 3 W/mm. Measurements were taken from both the top view and cross-sectional view as shown in Figure 62. The top view measurement enabled the estimation of the temperature rise in the GaN (using the two peak method) probing only the edge of the device and average across the depth of the GaN layer. In contrast, the cross sectional measurements were expected to average across the depth of the gate width and potentially results in a lower measured temperature. Comparing the results obtained, the q-$E_1$ (LO) results achieved similar temperature rises to those obtained from the two-peak method. Monitoring the shift in the peak position of the $A_1$ (TO) vibrational mode, the temperature rise appears significantly lower. While it has not been fully investigated, the underestimation of the temperature rise when using this peak position, may be associated with the peak being sensitive to stress changes as previously shown in literature for the $E2_{High}$ peak.

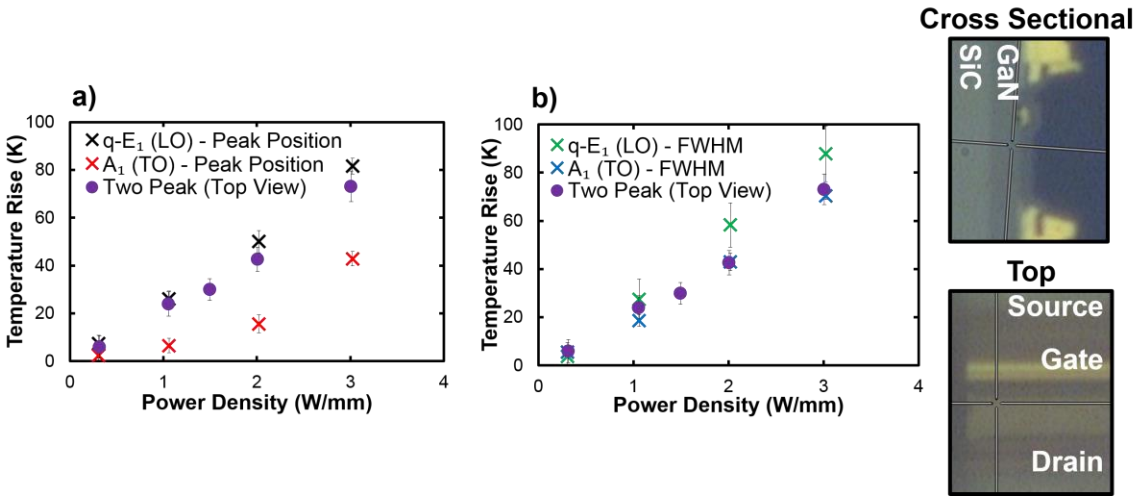



**Figure 62: Comparison of plan view Raman thermometry to cross sectional view thermometry using a) Shift in peak position and b) Shift in FWHM.**

To ensure symmetry in the power dissipation across the device, the temperature in the second channel was also measured at the highest power density measured. The close agreement between the temperatures measured in the cross sectional view to the top view measurements suggests that the peak temperature in the device can be approximated using the different Raman peaks rather than the traditional ones. Further Raman temperature mappings can be conducted to evaluate the thermal distribution across the channel and enable a more accurate comparison to the TTI results previously shown. It should be noted that despite performing Raman using visible wavelengths, a large fraction of the laser is absorbed in the first few microns of the materials confirming the weighted averaged of the temperature rise near the surface. To adjust the coefficient applied to the TTI measurements, transient Raman must be performed to enable a direct comparison of temperatures measured via the two techniques.

## 5.3 Vertical GaN PIN Diodes

Vertical bipolar switches will address numerous deficiencies found in GaN HEMT technology such as leakage current and avalanche incapability for applications to high voltage power devices [16]. The vertical technology trend has been proven in Si and SiC, however, the III-N bipolar switch research has only recently increased with investments in GaN PIN rectifiers. These devices indicate that the III-N bipolar switches are an important technology to realize the next-generation medium-to-high voltage electronics beyond SiC technology [17]. With the design optimization made to fully benefit from the superior electrical properties of GaN, device performance has often been limited due to self-heating effects. The transition to fabricating devices on GaN substrates removes the necessity for buffer layers enabling vertical devices where the path of heat will travel predominantly in the vertical direction. New characterization techniques must therefore be established to understand the temperature distribution across vertical devices such as PIN diodes.

Since vertical devices fabricated on a die can only be probed optically in a cross sectional view, Raman depth mapping or a combination of simulations and lateral surface temperature distributions mappings can be used to gain insight into the heat distribution of vertical devices. In this study, $TiO_2$ nanoparticles are used for Raman surface temperature mapping. To further validate the accuracy of these measurements, TTI is used to monitor the surface temperature rise of vertical GaN PIN diodes. Two sets of GaN PIN diodes were epitaxially grown on sapphire and free standing (FS) GaN substrates. The doping concentrations and layer thickness are described in [107] and [108] respectively. Figure 63 shows the layouts of the two different devices. Even though the n-type contact is located on the top side, a bias can be applied vertically across the diode via a side-contact scheme

started with a mesa etching. For the GaN substrate, the n-type ohmic contact is formed on the backside of the wafer.

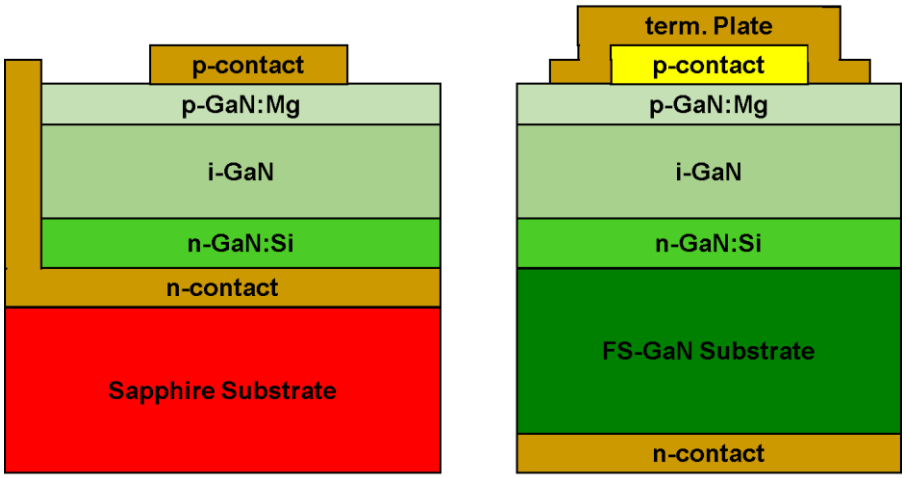



**Figure 63: Schematic of layer of a) GaN/Sapphire PIN Diodes b) Free-Standing (FS) GaN PIN diode.**

In addition to understanding the temperature distribution across a GaN PIN diode, the thermal resistance added by using a thick buffer layer can also significantly affect the device thermal performance. For lateral devices, the thermal resistances imposed by buffer layers depended on low thermal spreading resistance to dissipate heat efficiently. In contrast, significant self-heating may occur in vertical devices if a larger thermal resistance is present between GaN and a non-native substrate. The overall temperature rise between the sapphire GaN buffer (4 μm) and FS GaN buffer (1 μm) is thus compared at varying power conditions to quantify the additional thermal resistance added by buffer layer thickness.

### *5.3.1 Assessing the thermal distribution via Raman Thermometry*

Micro-Raman spectroscopy was performed using a Renishaw InVia Raman microscope with a 488 nm laser as the excitation source. To estimate the uncertainty in the

temperature measurements with 95% confidence intervals, an average of at least 20 measurements was made at all power conditions. Both the calibration and measurement steps for the Raman thermometry measurements were done with the temperature controlled stage set at 303 K. The temperature of the devices was estimated using the two-peak fit method [56]. The devices were biased electrically using needle probes. Applying a forward DC bias, the voltage was increased and the current was monitored to estimate the total power dissipated by the device. Prior to depositing $TiO_2$ nanoparticles for measuring the surface temperature of the GaN and metal contacts, Raman measurements were performed at the edge of the p-contact to estimate the volumetric averaged temperature rise across the GaN. Four locations were chosen to be spaced equally around the p-contact as shown in Figure 64. Temperature rises were estimated at varying power conditions to determine the effect of temperature on thermal spreading throughout the device.

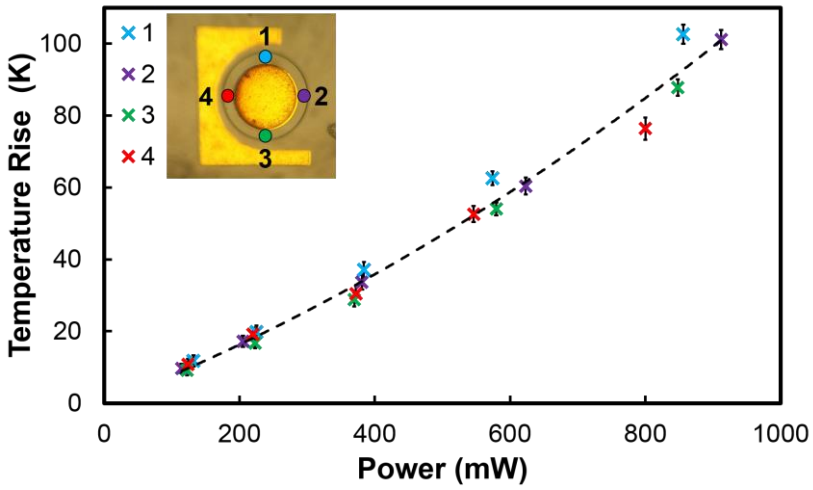



**Figure 64: Temperature rises measured by Raman thermometry of GaN on Sapphire PIN diodes at varying power dissipations. Locations were probed at the edge of the p-type contacts to estimate the temperature rise in the GaN as close as possible to the heat generation. Locations of the four different probed areas are shown in the top left image.**

The temperature rise of each location agreed well with each other suggesting a uniform heating profile occurs when biasing the diode. A second order polynomial was fitted to all the data points to show device's average thermal response with power. The significant improvement in goodness of fit when using linear regression from a first to second order polynomial shows the temperature dependent thermal conductivity of GaN [109]. Furthermore, the symmetric heat dissipation across the PIN diode begins to deviate at higher power densities as shown around 800 mW in Figure 64. At elevated temperature rises, above 80 K, the effects of the surrounding metal layers, specifically the mesa contact, may begin contributing to effective thermal resistance. For example, comparing location 1 and 3 in Figure 64, location 3 is surrounded by a larger area of the mesa n contact which may reduce thermal resistance in the localized area due to Gold's superior thermal conductivity to GaN.

To understand the significance of heat spreading surrounding the PIN diodes, a lateral temperature mapping was performed along the GaN. Figure 65 shows the volumetric averaged temperature rises across the GaN when moving further away from the active region of the PIN diode. At power dissipations lower than 250 mW, the temperature along the GaN is shown to be similar indicating the heat is efficiently dissipated. At higher power dissipations, the temperature rises measured at the three different locations begin to deviate and a temperature gradient as large as 30 K is estimated across the GaN at 750 mW. This significant temperature gradient indicated the effects of thermal spreading resistances and localized Joule heating under the p metal contact in the active region.

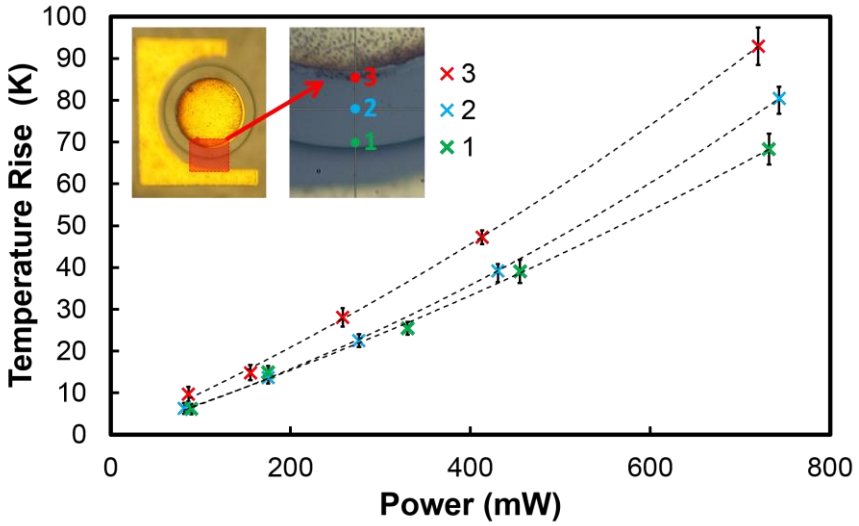



**Figure 65: Lateral temperature distribution across GaN on Sapphire PIN diodes at varying power dissipations measured by Raman thermometry. Locations of the three different probed areas are shown in the top left image.**

While the temperature of the surrounding GaN can be monitored via Raman thermometry, the active region of the vertical PIN diode is covered by the p-metal contact restricting optical access to probe the GaN below the metal. $TiO_2$ nanoparticles are thus deposited on top of the device to be able to measure the surface temperature of metal. The surface temperature of the metal will give a closer estimation of the peak temperature in the device. Furthermore, the characterization of the lateral temperature distribution shows the effect of thermal spreading resistance but does not give any information on the temperature gradient across the different layers of GaN throughout the PIN diode. The overall thickness of the combined GaN layers amounts to approximately 11 µm. Assuming that the Raman signature is a volumetric averaged across the 11 µm, the temperature gradient across these layers will not be captured and the peak temperature will be underestimated. Another characteristic that must be accounted for is the presence of different doping concentrations which may vary the thermal conductivity of the GaN regions and thus alter the vertical temperature distribution across the PIN diode [110]. The

surface temperature rises estimated via the nanoparticles was measured to be always greater than the GaN temperatures confirming the vertical temperature gradient across the device. A maximum of 15 K temperature difference was observed between the surface and the volumetric averaged temperature highlighting the necessity of using $TiO_2$ particles to estimate a more accurate peak temperature.

### *5.3.2 Transient Comparison via Transient Thermoreflectance Imaging*

In this study, TTI is used to perform full surface temperature mappings of the PIN diode's p-contacts. Multiple wavelengths were used to determine the optimal wavelength that results in the highest thermoreflectance signal for p-contact metal. Performing the calibration at approximately a 100 K temperature rise, a 530 nm LED source resulted in a strong $C_{th}$ of $-2.5 \times 10^{-4}$ °$C^{-1}$. Compared to Raman thermometry, the acquisition periods necessary to perform TTI are significantly shorter and also result in a temperature mapping instead of point measurement. Taking advantage of these benefits, both the PIN diodes on the FS-GaN substrate and Sapphire substrate were measured via TTI. The devices were both biased at 8 V with a time period of 400 μs and a duty cycle of 25%. The average power dissipated for the GaN and Sapphire substrate was measured to be 288 mW and 144 mW respectively. An LED pulse width of 2 μs was applied at 10 μs intervals from 0 to 170 μs. A comparison of the results obtained over a quarter of each p-contact metal is shown in Figure 66a. The results show the superior performance of the FS-GaN diode in contrast to the GaN on Sapphire PIN diode. For the same biasing conditions, double the amount of power is obtained across the FS-GaN diode at half of the temperature rise. This comparison highlights the significant contribution of the buffer layer on the overall thermal resistance

of the device. The GaN on Sapphire diode has a buffer layer of approximately 4 µm whereas the FS-GaN diode has a transition layer of only 1 µm.

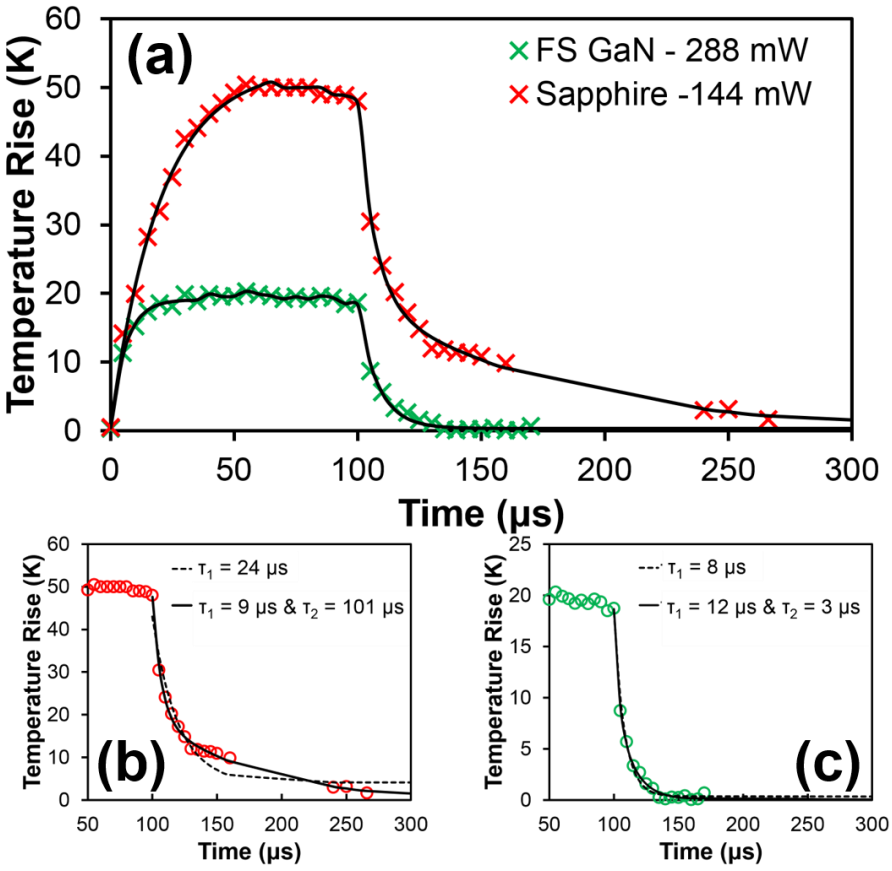



**Figure 66: a) Comparison of transient temperature profiles of p-contact metal of FS-GaN diode (green) and GaN on sapphire diode (red). Devices were biased with 8 V for a period of 400 µs and a duty cycle of 25%. Exponential rise and decay fittings were performed and plotted in solid black lines. Exponential decay fittings to TTI results (circles) using a single time constant (dashed line) and multiple time constants (solid) for b) GaN on Sapphire diode c) FS-GaN diode.**

Further analysis of the transient characteristics of the PIN diodes can be conducted by estimating the thermal time constants associated with the devices. Exponential fittings were performed in Origin to extract both the exponential rise and decay time constant associated with each device. Exponentials with both one and two constants were fitted to determine the best fit and are shown in Figure 66b and c. Using a single time constant for

both devices, the Sapphire substrate device shows to have a longer rise and fall time constant than the FS-GaN device. The poor heat dissipation can be attributed the relative low thermal conductivity of Sapphire to GaN.For the GaN on Sapphire diode in Figure Figure 66b, the need for using two time constants to accurately model the temperature decay is highlighted whereas the FS-GaN can be accurately modelled using just one time constant. This phenomenon can be explained by the amount of different materials present in the stack configuration. Due to the fact that heat is dissipated across GaN and also the sapphire substrate which have different thermal properties, the heat conduction across the layers will travel at different rates resulting in multiple time constants. Similar findings have already been reported in literature when attempting to model the transient temperature behavior of GaN HEMTs using analytical solutions [61]. Based on these results, thermoelectric simulations were implemented to accurately model the heat dissipation throughout the vertical PIN diodes [111].

### *5.3.3 Cross Sectional Temperature Mappings of Vertical GaN PN Diodes*

To directly evaluate the temperature gradient across the vertical GaN diodes, a similar approach was taken as previously shown in the current chapter for the cross sectional HEMTs. PN diodes were fabricated and processed in Nagoya University with the stack configuration shown in Figure 67a. The devices were cross sectioned with a wafer saw and then mounted to a customized package as described in Figure 67b. To obtain full temperature mappings of the device, initial attempts were conducted using TTI. Several difficulties were encountered when attempting to monitor the thermoreflectance change in these devices. Due to the luminescence of the device, a bandpass filter was required to remove the signal attributed to this effect. Using a bandpass filter, a wavelength must be

selected in which the luminescence does not occur. Using a 365 nm LED with a Bandpass filter, the luminescence was successfully removed. The next issue that arose, however, was the high surface roughness created during cross sectioning which consequently caused significant deflection of the reflected light. Further polishing, as previously done for the HEMTs, was not possible due to the limitation of available tools. The thermal analysis was thus focused on using Raman thermometry and probing the cross sectional plane of GaN as shown in the previous section. The luminescence still created difficulties by creating a large background fluorescence near the saturation of the CCD (shown in Figure 67d/e).

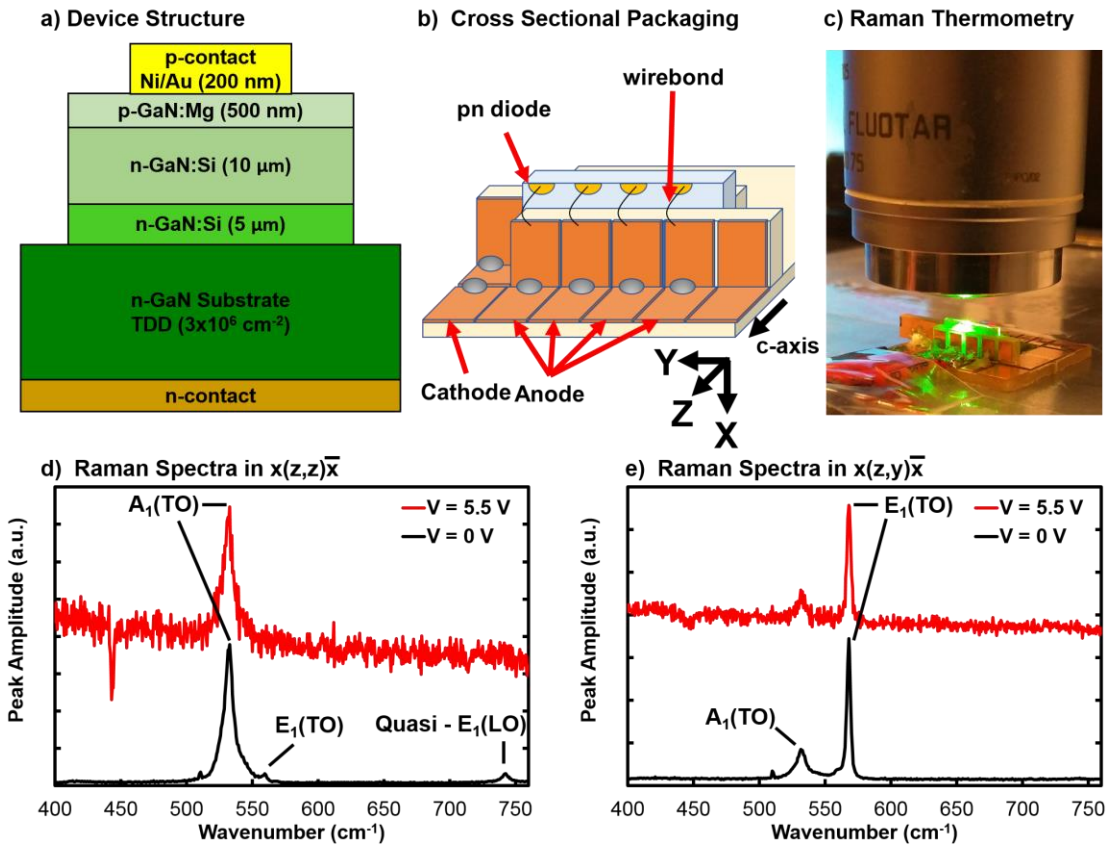



**Figure 67: a) Stack configuration of cross sectional PN diode studied b) Schematic of packaging method for cross section PN diode (figure and package designed by Shiyegoshi Usami) c) Package mounted on Raman thermometry system.**

During biasing, the peak position of quasi $E_1$ (LO) peak could not be monitored for use in Raman thermometry. The peak position and line width of the $A_1$ (TO) vibrational was thus measured as temperature coefficients were previously extracted for this phonon frequency when measuring the cross sectional HEMTs. Despite the $E_1$ (TO) vibrational mode yielding a high intensity during luminescence, the coefficient for this the peak has not yet been investigated and requires further calibration to verify its accuracy.

The diodes were biased in the forward voltage mode enabling large currents to travel vertically through the device. Initial measurements were taken at the center of the diode (the diode diameter was 500 μm) near the p-contact. An average of 10 measurements for each position was taken and the errors associated to the measurements were calculated using a 95% confidence intervals. The results of the temperature rise estimated via the shift in the $A_1$ (TO) peak position and line width are shown in Figure 68. For both cases the temperatures agreed well with each other showing a quasi-linear temperature power dependence. This result contrasted the previous results obtained via the cross sectional HEMTs where the peak position shift was shown to underestimate the temperature rise.

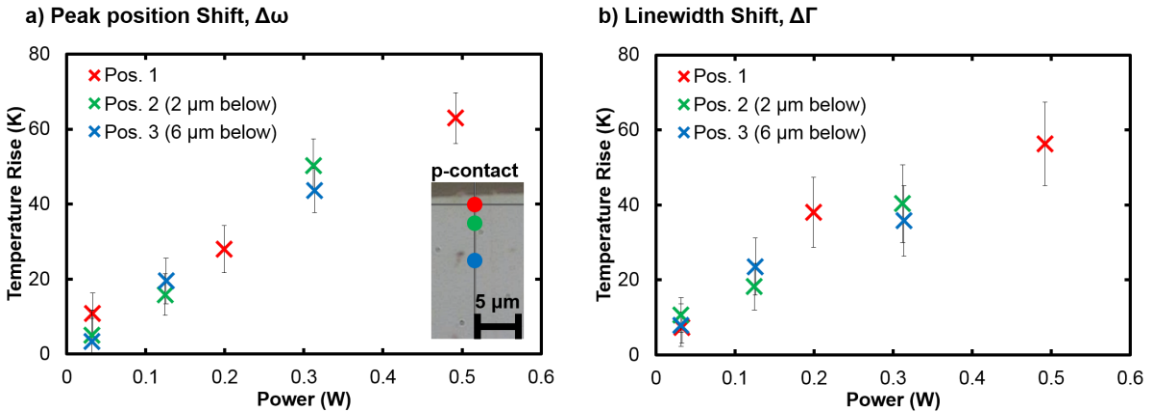



**Figure 68: Temperature distribution in a cross sectional GaN PN diode monitored via a) $A_1$ (TO) peak shift and b) $A_1$ (TO) line width shift.**

Small differences in the temperature rise of the drift layer were observed over the first 6 μm suggesting a uniform temperature distribution across the 10 μm drift layer depth. Comparing the errors bars associated with the peak position and the line width, it can be noted that a larger error (10%) is associated with monitoring the line width. This phenomenon can be attributed to the low signal to noise ratio encountered when biasing the device and causing fluorescence to the Raman signal.

To fully characterize the temperature distribution along the vertical direction, a full Raman line mapping was performed from the p-contact into the substrate in 1 μm steps. To avoid any permanent degradation due to long stress periods, the device was biased at a constant power dissipation of 0.156 W. Using the coefficients previously extracted, the temperature rise along the depth of the device is shown in Figure 69.

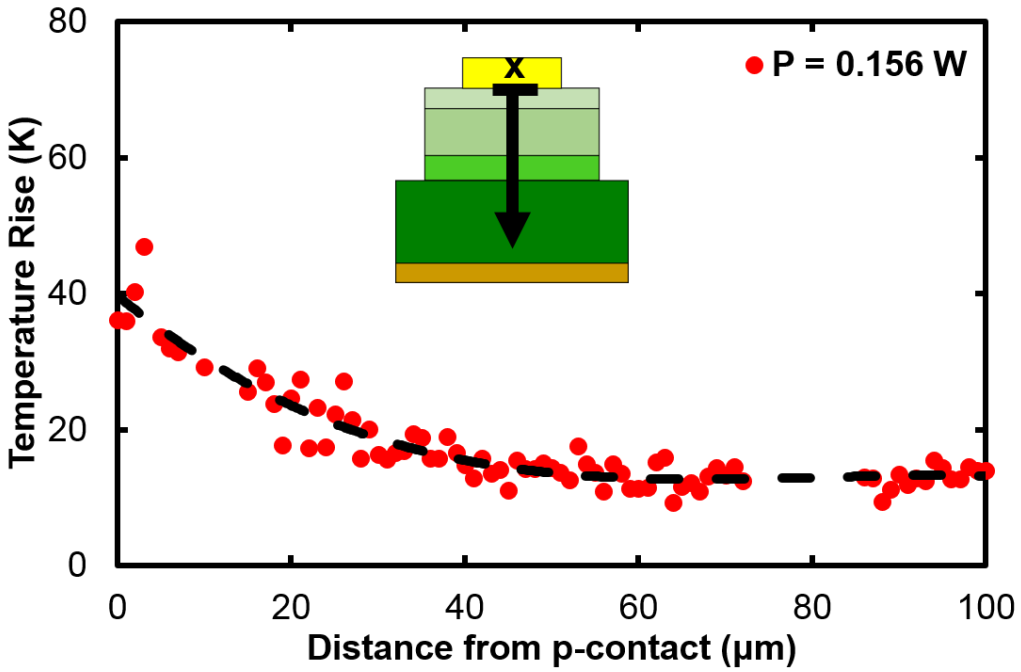



**Figure 69: Temperature depth mapping across the GaN PN Diode at a constant power dissipation.**

The vertical temperature distribution shows that the heat is conducted vertically creating a gradient across the drift layer and dissipating into the substrate. Going beyond the initial 6 μm previously measured, the temperature rise is shown to drop from 40 K to 28 K in the first 10 μm. Despite the PN diode being fabricated on a native substrate and the thermal boundary resistance between the different GaN layers is minimal, a slight decrease has been measured in the thermal conductivity of the Mg doped GaN layers resulting in an increase in thermal of the GaN near the area of heating. Having shown the feasibility of performing temperature depth mappings of PN diodes, numerical models can be developed to understand better the temperature distribution in PN diodes and the thermal conductivity associated with each layer.

## 5.4 Summary and Conclusions

The first ever thermoreflectance images of a cross sectional GaN/SiC HEMTs showing the effect of bias conditions on Joule heating are demonstrated in this chapter. The accuracy of the thermoreflectance coefficient used for these measurements is shown to be associated with a large uncertainty. Comparison of top view and cross-sectional view TTI measurements highlight differences in the thermoreflectance region for the same targeted region such as the Gate Metal. The presence of a passivation layer and the effects of thin film interference are shown to be the most significant factor contributing to the error measured with the thermoreflectance coefficient. A direct comparison of the temperature rises measured using Raman thermometry via the top view and cross-sectional view is reported. Due to the change orientation, alternative vibrational modes are detected. The temperature dependence of the newly detected peaks in the cross-sectional view are investigated and their coefficients are extracted. The close agreement between the

temperature rise measured via the top view and cross sectional highlight the viability of using Raman thermometry to estimate the peak temperature of the device in the cross sectional view.

To assess the thermal distribution in vertical GaN PIN diodes, the use of $TiO_2$ nanoparticles is shown to accurately capture the surface temperature of both the GaN and metal regions. Since the active region is located under the p-contact metal, a quicker temperature measurement is proposed based on the change in thermoreflectance of the gold metal. TTI was used to compare the transient thermal dynamics of both the GaN on Sapphire diode and the FS-GaN diode. A higher temperature rise for a smaller power dissipation is observed for the sapphire substrate diode highlighting the significance of the buffer layer on the thermal resistance. Applying exponential fittings to the temperature rise and decay curves of the devices, two time constants are required to model the GaN on sapphire diodes. This can be attributed to presence of two different materials in the stack configuration whereas for the full GaN diode only one time constant is necessary for fitting. Cross sectioning the PIN diodes, vertical temperature mappings via Raman thermometry were conducted for PN diodes to assess the temperature distribution along the depth of the device. The temperature was found to be localized towards the top of the device near the drift layer. Showing the feasibility of vertical temperature mappings of PN diodes will enable a deeper understanding of the thermal resistance associated with each layer and determine whether there is bias dependence to the Joule heating profile.

# CHAPTER 6. THE IMPACT OF STRAIN RELIEF LAYERS ON POWER ELECTRONICS

## 6.1 Overview and Approach

While silicon carbide (SiC) and diamond substrates have been used to improve the thermal performance of GaN HEMT devices, significant research has been conducted on fabricating GaN on silicon (Si) substrates to ensure low power devices that can take advantage of current CMOS processing lines and foundries. One drawback of using Si substrates, however, is its inherent weak electrical field strength (0.3 MV/cm) which has shown to be at least ten times lower than wide band gap materials like GaN [112]. This limitation has been identified as the main cause for breakdown in GaN on Si HEMTs when the high electric field reaches the silicon underneath the gate and drain [113]. Thus, GaN on Si power HEMTs are industrially being targeted for applications up to 600 V with the limitations only coming from the Si, and not the active GaN layer itself. Applications at medium voltages up to 2000 V would allow GaN on Si to be used in electric motor drives in electric vehicles as well as industrial applications.

Currently, several techniques have been developed to redistribute the electric field and thus increase the device's breakdown voltage. For high off-state biases, field plates have been frequently used to reduce the peak electric field at the gate edge. Attempts to create a back-barrier above the Si substrate by using a p-doped buffer layer or double heterostructure have also proven to reduce the leakage current and enable high voltage operation [114]. Furthermore, the thickness of the buffer layer (AlGaN) can be increased

up to 5 μm to improve the breakdown voltage [115]. The lattice mismatch between AlGaN and Si, however, leads to large tensile strains in the GaN which produces an increase in the number of defects. This effect directly decreases the device's performance and lifetime [116]. To avoid thick single AlGaN buffer layers, the addition of superlattices can be implemented to reduce the residual stress in the GaN. The superlattices, typically composed of alternating layers of thin AlN/GaN or AlN/AlGaN, are grown onto Si enabling the epitaxial GaN to be grown on a layer with a closer lattice constant. The drawback to this approach is the increase in the thickness of the devices which leads to an overall increase in thermal resistance [117]. Exploring the possibility of simultaneously engineering these interfaces to simultaneously reduce the stress in the GaN and minimize the thermal resistance [118], requires the accurate assessment of the device's thermal performance. In this chapter, a comparison of superlattice devices (SL) to AlGaN transition layer devices (AL) is conducted. TTI is used to assess benchmark the thermal performance and further detail into the applicability of UV TTI on GaN HEMTs is explored. To complement the thermal analysis of these structures, Electroluminescence (an optical technique used to identify electron trapping) is also performed to compare the quality of the GaN channel in the devices.

## 6.2 Thermal Analysis

### *6.2.1 Comparison of Gate Metal Temperatures*

Three different device structures, with varying superlattice (SL) thickness and GaN:C buffer layer thickness were investigated (the layout of the structures are described in Figure 70). An initial comparison of the gate metal using TTI with a 530 nm LED

excitation source was performed. A calibration was performed and the $C_{th}$ of the gate metal was measured to be -1.74 x $10^{-4}$ $°C^{-1}$ for all devices (previously shown in Chapter 3). The devices were pulsed biased with a drain bias of 20V. The gate bias was varied (always negative) to match a peak power density of 3.6 W/mm.

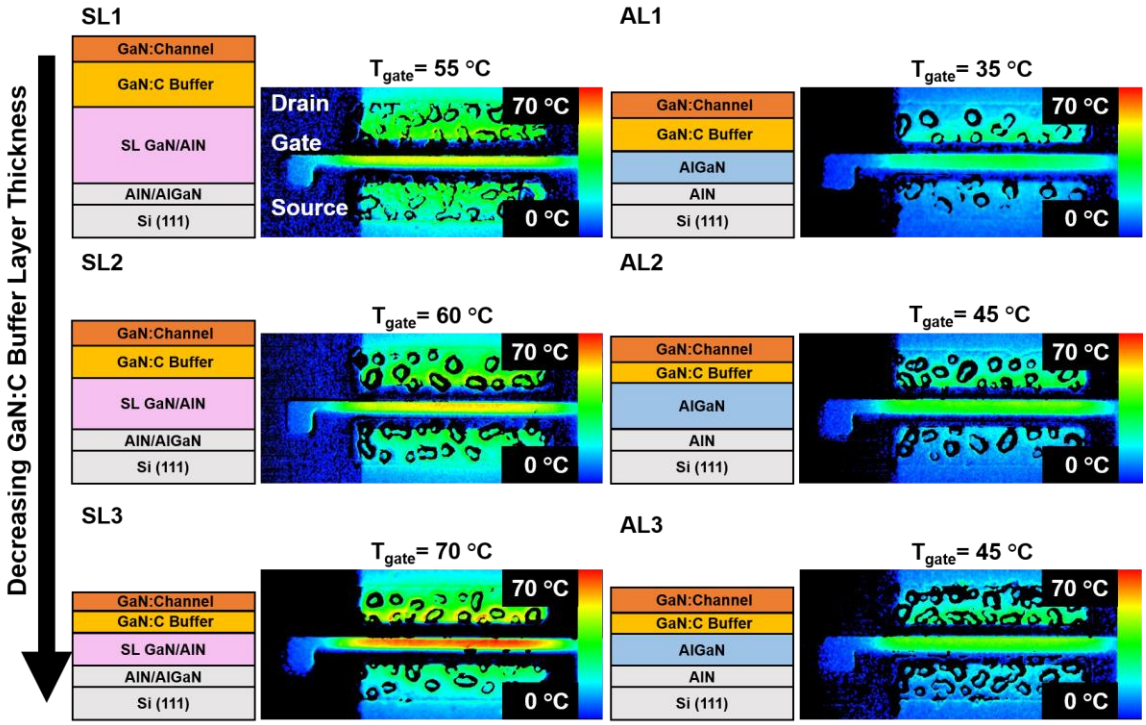



**Figure 70: Comparison of gate metal temperature for three different GaN HEMTs on Superlattice (SL) structures and three additional GaN HEMTs on AlGaN buffer layers (AL). TTI was performed with a 530 nm LED excitation source. Devices were biased at the same power conditions.**

Despite the implementation of a thicker SL layers, the gate metal temperature appears to decrease with increasing SL thickness. This phenomenon can be explained by the change in thickness of the GaN:C buffer layer just below the GaN channel. Literature has shown that the spreading resistance in the GaN:C buffer layer decreases with increasing thickness [96, 119]. Since the devices in this study contain GaN:C buffer layers with

thicknesses proportional to the SL thicknesses, the effect of carbon doped layer dominates the thermal performance when benchmarking the device temperature.

Comparing the gate metal temperature to the three additional devices with AlGaN buffer layers (AL), the temperature rise appears higher in the SL structures (50-100% increase in temperature rise). One should note that the thickness of the GaN:C layer in the AL devices is comparable to the thinnest GaN:C layer in the SL devices (SL3). The overall increase in temperature of the gate metal, when comparing the SL devices to the AL devices, can thus be attributed to the addition of the SL structures and not an increase in the GaN:C layer.

### *6.2.2 Bandgap Dependence UV Thermoreflectance Imaging*

The results from Figure 70 show, in some cases, a significant temperature gradient across the gate metal. To further investigate this gradient, the temperature in the GaN channel must be examined and consequently requires the need of higher energy wavelengths that are not transparent to the GaN layer (UV TTI). A comparison of UV TTI to TTI for SL3 was already presented and discussed in Chapter 3, but the application of using a 365 nm LED to all devices has not been completed. The importance of study will help understand the effects of near bandgap wavelengths on the thermoreflectance signal from a given material and determine the origin of the thermoreflectance signal.

Prior to performing TTI measurements, calibrations were performed to estimate the thermoreflectance coefficient, $C_{th}$, in the GaN channel region. The results of the coefficient maps for the three SL structures is shown in Figure 71. The devices with the thicker SL structures, SL1 and SL2, are shown to have a smaller coefficient ($-0.6 \times 10^{-3}$ °$C^{-1}$), while

SL3 results in a coefficient of -0.9 x $10^{-3}$ $°C^{-1}$. The bandgap of each device was also measured using a 325 nm Laser with JY Horiba system. The bandgap for all three SL devices was found to be range of 3.42 eV. This is correlated to a small compressive residual stress in the GaN which is to be expected with the implementation of the SL structures.

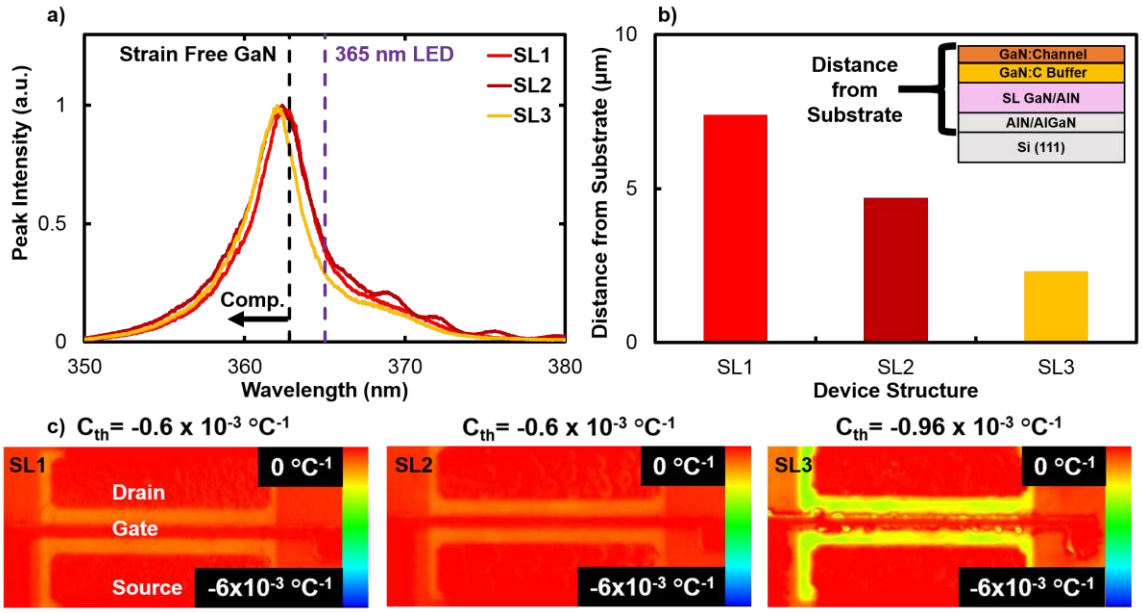



**Figure 71: a) Photoluminescence (PL) spectra of the Superlattice (SL) structured GaN HEMTs b) The distance from the top of the device to the substrate is plotted and the c) thermoreflectance coefficient, $C_{th}$, for all three devices is mapped.**

Converting the PL spectra to nm (as shown in Figure 71a), the bandgap of the GaN is shown to be within 3 nm of 365 nm. Due to the broad spectrum of the LED (±12 nm), the wavelengths below 362 nm, will be absorbed in the GaN layer and will contribute to the thermoreflectance signal measured from the GaN channel. Following this logic, it was hypothesized that for same range of wavelength excitation, a device with a bandgap closer to 365 nm will result in a larger thermoreflectance coefficient. Comparing the band gap values of the SL structures measured, the opposite trend was discovered. This led to the consideration of thin film interference effects on the thermoreflectance signal measured.

Since a portion of the wavelengths emitted from the LED are below the bandgap of the structure, these wavelengths will transmit all the way to the silicon substrate. The reflection of these wavelengths through multiple different layers, including the GaN:C buffer layer and the SL structure, will contribute significantly to the thin film interference effect previously described in Chapter 3. Comparing the overall thickness between the top surface and the substrate in Figure 71c, the structure with the shortest distance, SL3, results in the strongest coefficient. These results highlight the effect of both thin film interference and the bandgap of the material on UV TTI.

Measuring the bandgap of the AlGaN buffer layer devices (AL), more tensile stresses were found in the GaN Channel (Figure 72a). This resulted in a shift of the band gap towards the 365 nm LED. At first glance (Figure 72c), the thermoreflectance coefficient measured for each AL structure was found to be significantly higher than the SL structures corresponding to thermoreflectance coefficients on the order of $10^{-3}$ $°C^{-1}$. The increase in thermoreflectance signal detected from the AL structures cannot be attributed solely to the shift in the bandgap. Comparing the overall thickness of layers above the silicon substrate (Figure 72b), a significant reduction in the total layer thickness is achieved and it is expected that the effects of thin film interference will be significantly reduced.

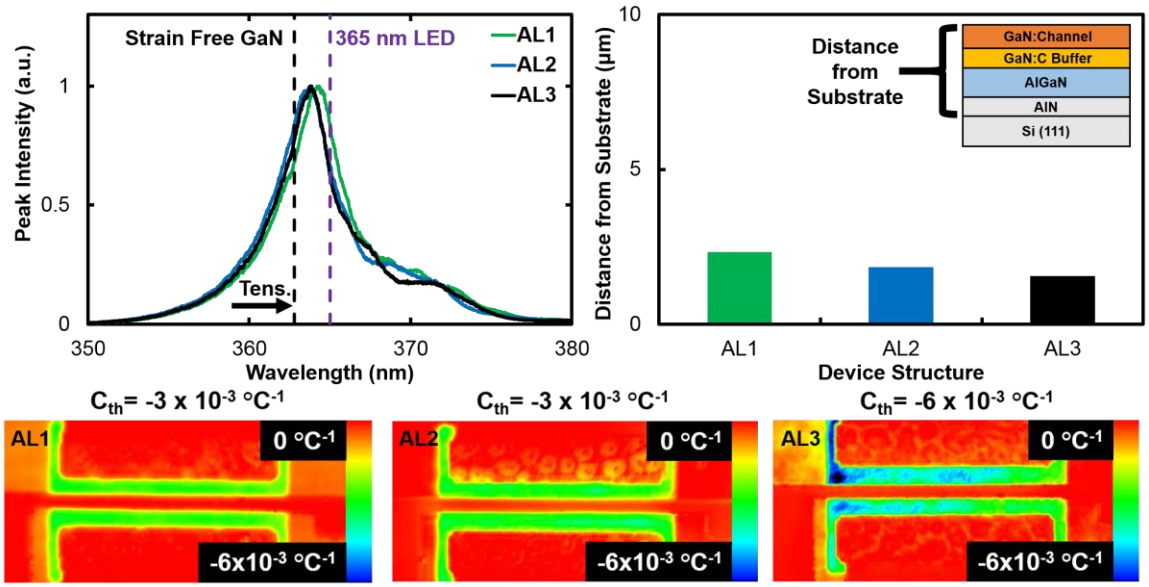



**Figure 72: a) Photoluminescence (PL) spectra of the AlGaN buffer layer (AL) GaN HEMTs b) The distance from the top of the device to the substrate is plotted and the c) thermoreflectance coefficient, $C_{th}$, for all three devices is mapped.**

### *6.2.3 Above Bandgap UV Thermoreflectance Imaging*

To temporarily overcome the issue of using LED excitation sources partially over the bandgap of the material, an LED with a much a higher energy was applied (340 nm). Point by point calibrations were used for these images and the results are shown in Figure 73. The devices appear to reach similar temperature rises as those measured by the gate metal in Figure 70. This close agreement shows the validity of using above bandgap excitation to measure the thermoreflectance in the GaN region. It should be noted that only one of the SL structures (SL3) was possible to measured using the 340 nm LED excitation. The other two devices were found to have a very weak thermoreflectance coefficient and temperature rise was detected via the CCD. Overall a clear temperature difference is observed between the GaN region on the drain edge and the GaN region on source edge.

A maximum temperature difference of 15 K is observed. This distribution confirms the gradient also observed across the gate metal.

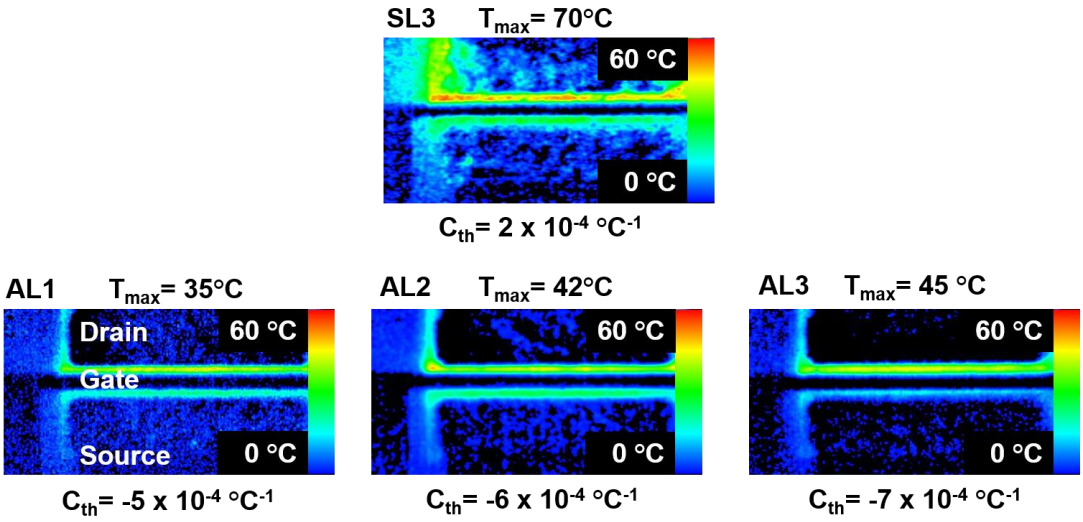



**Figure 73: UV TTI Results using 340 nm LED excitation source. No thermoreflectance imaged of the SL1 and SL2 device structures could be obtained. Devices were biased at the same power conditions.**

Comparing the thermoreflectance coefficients measured for each device, the coefficients all appear to be on the same order of magnitude. It is observed that there is a slight increase in thermoreflectance coefficient with decreasing device layer thickness but not as significant as results obtained via the 365 nm LED. The results suggest that there still exist some interence.

### 6.3 Electroluminescence

Beyond thermal analysis, several electrical methods have been use for accelerated lifetime testing to understand the failure modes in GaN HEMTs and quantify the device's reliability. Due to the piezoelectric nature of GaN, large stresses are developed throughout the device in addition to thermal stresses. These stresses cause pits to be formed on the

surface at the gate edge and have been found to be directly correlated to electrical degradation in the device [11]. Previous literature has applied large negative gate biases to accelerate degradation [120, 121]. These bias conditions are however, not typical of device operating conditions and thus may activate different degradation mechanisms [122, 123]. Biasing at normal operating conditions, the exact amount of degradation has been quantified using expensive material characterization equipment such as SEM, AFM, TEM [10, 124]. A strong correlation has been found between these methods and a non-destructive method known as Electroluminescence (EL) [125, 126]. This method is able to detect the photon emission of 'hot electrons' that are trapped in the GaN layer due to the presence of material defects. Since the device degradation can lead to increase in material defects, this will correspond to an increase in electron trapping which will then be detected as an increase in EL intensity. EL is used in the following study to assess the effect of the strain relief layers on GaN/Si HEMTs.

### *6.3.1 Experimental Setup and Methods*

Devices were probed in a dark box on a Cascade Probe Station with the detector mounted via the camera port on the top side as shown in Figure 74. Two different detectors were used to perform EL measurements. For steady state and slow transient analysis (> milliseconds), a Princeton Instruments PIXIS BR Excelon was used. This detector has a 90% Quantum Efficiency in near IR range and shutter speed of 10 ms. The emission of wavelength of hot electrons has been estimated to be in the mid IR range [127, 128]. For transient analysis in the microseconds, a Princeton Instruments PI-MAX 4L 1024i RB was used. In contrast to the PIXIS, the detector was limited to a 6% Quantum Efficiency in near IR range. The main advantage of using this detector was the SuperSynchro Timing

Generator enabling external trigger capabilities with an insertion delay of 27 ns. The transient EL analysis technique was based on the technique employed for TTI and is explained in Figure 74. The device is continuously pulsed biased at a certain duty cycle and time period while an external control board is used to control the read out time of the CCD. It is impossible to control the CCD shutter on the order of microseconds so the timing of the CCD is modulated using a picosecond gating technology via the use of a microchannel plate intensifier.

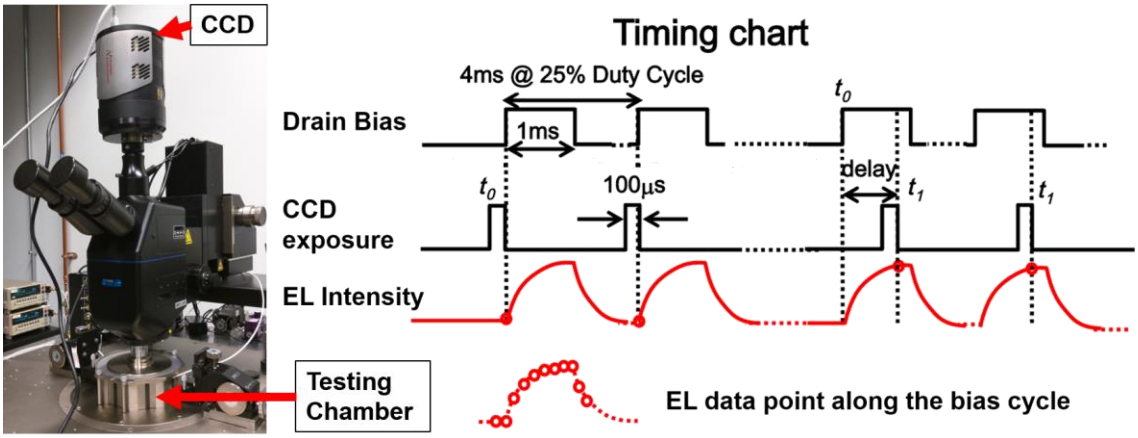



**Figure 74: Experimental setup for electroluminescence (EL). Timing diagram explained for transient EL analysis.**

To decouple the hot electrons produced during self-heating from the defect analysis, the current dissipated across the device must be kept at a minimum. Typically, gate biases used for pinching off the devices are applied to ensure small power dissipations. Furthermore, a certain activation energy is required to initiate defects in high quality GaN devices. This is performed by step stressing the drain voltage until degradation is detected. After several of tests, it was found that, at a gate bias of -6 V, 5 out of 6 devices required the drain bias to be pulsed at a minimum of 30 V to detect EL. One device was required to be pulsed at a minimum of Vds = 38 V (SL2). Once the degradation in the device has been

initiated, a lower drain bias can be applied to continue to detect EL and at the same time prevent further degradation.

To compare the degradation measured by EL to an electrical technique, IV sweeps were performed to detect any changes in the drain current. Initially, EL measurements were taken after a short period of time after stressing (1-5 minutes) and significant difference were detected between the superlattice structures and the AlGaN buffer layer devices. With the aim to detect the permanent degradation in the device, however, measuring the EL intensity at such a short time interval after biasing is inaccurate due to the temporary surface traps that are formed during biasing [129, 130]. To enable an accurate comparison, the devices were allowed to recover for 48 hours to remove any effects of surface trapping. The surface trapping was found to be monitoring the IV characteristics throughout the recovery period (see Figure 75). To summarize, the following procedure was used to conduct EL analysis:

1. Stress device for 90 seconds ($V_{ds}$ = 30 V and $V_{gs}$ = -6 V.
2. Perform $V_{ds}$ sweep
3. Allow 48 hours for full recovery (determined by subsequent $V_{ds}$ sweeps)
4. Perform EL at $V_{ds}$ = 20 V and $V_{gs}$ = -6 V

Due to the variation in layer thicknesses for each device, the degradation can be attributed to different factors (GaN:C buffer layer thickness, active GaN layer) and not just due to the reduction of the GaN residual stress using a super lattice. To perform a more accurate comparison, devices with similar GaN:C buffer layer and active GaN layer thicknesses were compared.

### *6.3.2 Transient Electroluminescence*

When performing transient EL measurements, the devices were pulsed for a period of 4 ms with a 30% duty cycle. Examples of the EL mappings for both devices are shown in Figure 63. Comparing the number of locations where the device has degraded, more EL spots are observed with the AlGaN buffer layer (AL) device than the Superlattice devices (SL). Furthermore, the EL intensity is found to be significantly higher for the SL devices (40%) signifying an increase in the number of electrons being trapped. The trends confirm the presence of a higher quality epitaxial GaN layer in the SL devices which contains a lower residual stress.

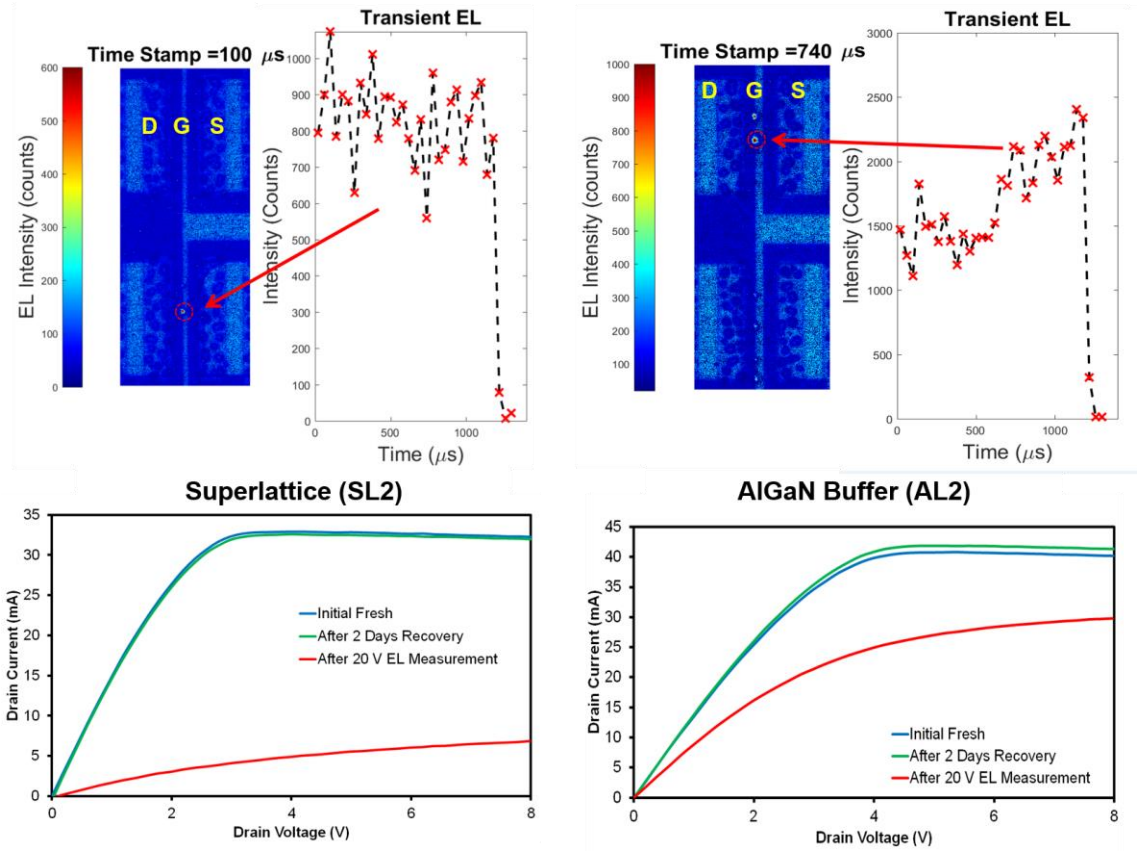



**Figure 75: Transient electroluminescence analysis of superlattice (SL) structured GaN HEMT on Si and AlGaN buffer layer (AL) devices. The change in IV characteristics are compared to the number of EL spots and EL intensity.**

Regarding the change in IV characteristics for both devices. The SL device shows full recovery of its IV trace while the AL device is shown to reach 95% of the original drain current. This comparison follows the same trend as shown in the EL where more degradation is observed in the AL structure. Measuring the drain current immediately after the stress period, however, the effect of current collapse is more severe in the SL device. This suggests that surface trapping has a more significant effect on SL devices than AlGaN devices. Assessing the applicability of this technique, transient EL demonstrates more degradation in the AL device (high tensile residual stress) than SL device (low residual stress). EL analysis also enables the detection of degradation despite full Ids recovery highlighting its sensitivity compared to classical electrical detection methods.

### *6.3.3 Design Considerations*

In order to detect any changes in the EL signal and position on the order of microseconds, several design factors must be considered. The primary issue with applying an accumulation based technique is small movements of the device relative to the CCD due to stage drift. Without the implementation of an autofocusing feature as used in TTI via a piezoelectric stage, stage drift will inevitably occur. The effects of stage drift were immediately apparent when attempting to estimate the intensity of the EL spot over time. Placing a probe at a fixed location, large oscillations in the EL intensity were measured (±10,000 counts) even though when the intensity of the overall image was not changing. Assuming there is minimal change in the location of the EL spot, a tracking algorithm must be developed to monitor more accurately the intensity of the EL spot. Using MATLAB, a code was developed to perform this and record the intensity value transiently. Depending

on the EL spot size, the code enables the user to define how big of an area he/she would like to probe. The steps involved in the code are outlined below:

1. Scan area to locate pixel with highest intensity
2. Extract intensity data for surrounding pixels
3. Average intensity values
4. Repeat for next frame

Also associated with stage drift, is the temporal resolution of the system. The intensity of EL is dependent on the CCD exposure time. A minimum of 200 ns was found to detect any EL signal. Using this exposure time, however, requires a significant increase in accumulations (10,000 to 70,000). The longer accumulations resulted in more stage drift and was thus not found practical. To solve this issue the 20x objective used was replaced with a 100x near IR lens, it was possible to achieve higher time resolution (2 μs) of EL spots for a minimum intensity of 10,000 counts and 20,000. Two factors are thought to have contributed to improvement of the time resolution. First, since the emission of the hot electrons are predicted to be in the near IR range, the use of an objective with a high transmissivity in this range will enable a fine detection of EL signal. Second, using a higher magnification, the working distance between the sample and the detector is decreased which also assists in transmitting more electrons to the detector. Using this time resolution, the rise of EL intensity could be clearly observed whereas the decay was still not possible

to detect. The potential of this technique could enable the direct comparison of the time rise associated with the EL intensity to the time constants associated with the Joule heating.

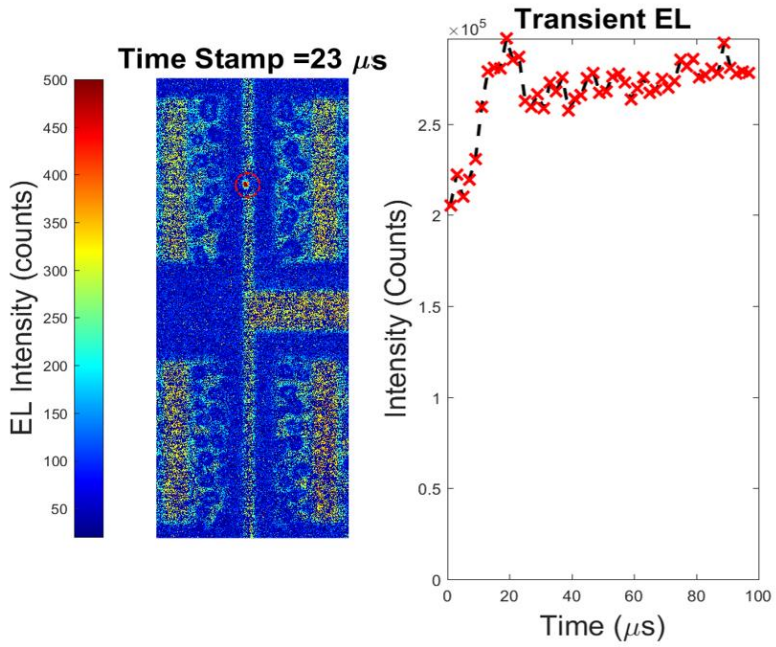



**Figure 76: Improvement of temporal resolution in transient EL analysis when using a near IR 100x objective.**

## 6.4 Summary and Conclusions

The results of this chapter highlight the advantages of using superlattice structures to reduce the residual stress in the epitaxial GaN layer and improve the breakdown voltage of the device. Small compressive stresses in the GaN layer improve the device performance and is shown via the analysis of electroluminescence. The smaller percentage of electrical degradation correlates to increase in EL intensity. Based on EL, more defects are found in tensile stressed GaN layer. Regarding the state of the EL technique, the ability to achieve microsecond resolution during EL is demonstrated. The development of real time EL

measurements may show further degradation mechanisms and could be potentially achieve by using a CCD with a higher quantum efficiency CCD.

Comparing the thermal performance of the devices, via TTI, a clear increase in thermal resistance is observed when implementing a SL layer in comparison to an AlGaN buffer layer. The applicability of UV TTI to measure the temperature in the GaN channel is demonstrated to have a high dependence on the overall thickness of the stack configuration which causes thin film interferences effects. The use of a near bandgap wavelength excitation is thus found not be sufficient enough to accurately measure the temperature rise of the GaN channel. The advantages of using a wavelength excitation source well above the bandgap (340 nm) are highlighted and shown to accurately measure the temperature rise in the GaN.

# CHAPTER 7. THE IMPACT OF SUBSTRATE REMOVAL ON POWER ELECTRONICS

Content in the chapter (figures and text) adapted from:

1. G. Pavlidis, *et al.*, "The thermal effects of substrate removal on GaN HEMTs using Raman Thermometry," in 2016 IEEE ITherm, pp. 1255-1260.[64]

## 7.1 Overview and Approach

In order to avoid the development of large stress gradients across thick buffer layers and complex strain engineered layers, the removal of the Si substrate between the gate and drain region has shown to increase the device's breakdown voltage well-above 2000 V (Figure 79a) [131]. While removing the Si substrate extends the capabilities of GaN HEMTs for high power conversion applications, the effects of the Si removal on the thermal performance during operation has not yet been investigated. The removal of the Si substrate prevents the possibility of the localized heat to be directly conducted through the substrate. To accurately estimate the temperature rise, Micro-Raman spectroscopy and TTI is used in this study to measure the impact of substrate removal on channel temperature in these GaN power HEMTs.

A comparison of the channel temperature rise between a local substrate removed (LSR) device and a non-LSR device is completed. Both volumetric averaged Raman measurements of the GaN as well as nanoparticles surface temperature measurements are conducted on the devices ($TiO_2$ and ZnO). Based on these results, an objective comparison on tradeoffs between the thermal performance and high breakdown voltage of LSR and

non-LSR GaN on Si power devices will be discussed. Improvements of thermal performance via insertion of an AlN and copper layer on the back [132] will also be studied and the reduction in temperature will be quantified.

## 7.2 Device Description and Electrical Characterization

Two fingers AlN/GaN on Si HEMTs were tested with gate widths of 50 µm and gate lengths of 1 µm. The thicknesses of the different layers are indicated in Figure 77. The first device measured (Figure 77a) contained a large GaN buffer layer of approximately 5.5 µm on top of a 200 nm AlN nucleation layer which enabled relatively large breakdown voltages using a large Gate-to-Drain spacing of 20 µm. The second device (Figure 77b) utilized a thinner buffer layer of approximately 2 µm AlGaN with a 200 nm AlN nucleation layer. However, the Si substrate was removed from the region between the gate and drain (5 µm spacing). The process for the removal of Si is explained in [113]. It should be noted that no source field plates or gate dielectrics have been implemented in these devices.

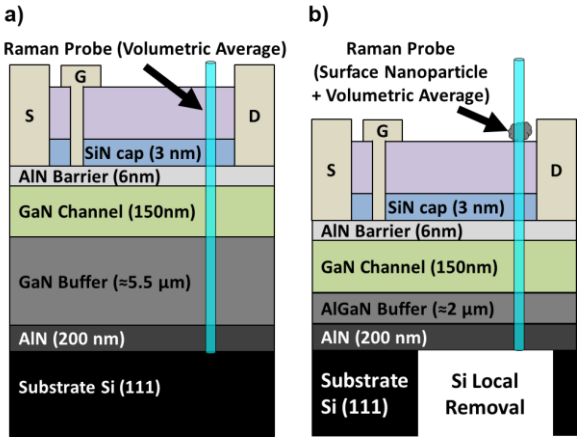



**Figure 77: Cross section of layers of AlGaN/GaN HEMTs with a) 5.5 µm thick GaN buffer layer and b) 2 µm thin AlGaN buffer layer with silicon locally removed region. A 488 nm laser was used to probe a volumetric average temperature across the device (left) as well as a surface temperature using ZnO/$TiO_2$ nanoparticles (right).**

The devices have a common layout which is shown in Figure 78. Regarding the thinner buffer layer device from Figure 77b, the device was etched so that only one out of the two channels would have the substrate material removed below itself. This enabled the direct comparison of a single finger device with locally removed Si (LSR) and another single finger device with no Si removed (non-LSR). Due to the fact that both fingers were fabricated under the same process there would be no uncertainty about the variation in the growth processes.

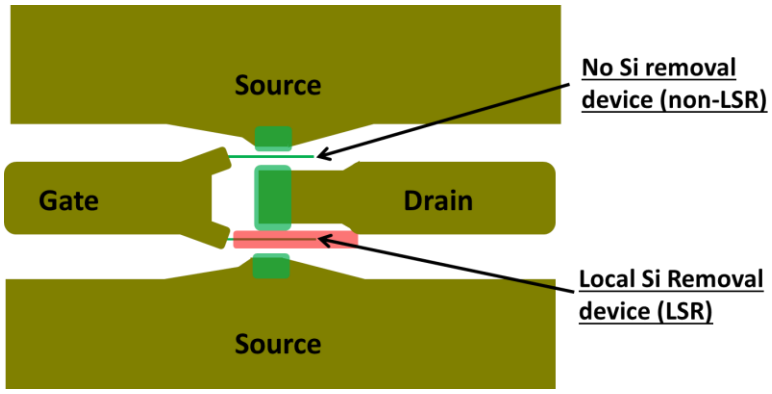



**Figure 78: Position of locally removed silicon on Device. Upper device has no silicon removed between the gate and drain (non-LSR) while the silicon is removed lower device.**

When biasing both fingers, ground-signal-ground probes connected to bias tees with 50 Ohm terminations were used to make electrical contact with the devices. All power sourcing and electrical measurements such as I-V characterization were conducted using a dual-channel Keithley 2602a source meter. DC needle probes were used to locally probe single channels as shown in Figure 78 in order to enable direct comparison of temperature rises of LSR and non-LSR regions.

Prior to conducting thermal measurements, the I-V characteristics between the LSR and non-LSR devices were compared (see Figure 79b). The drain bias ($V_{ds}$) was swept

from 0 to 10 V while the gate bias ($V_{gs}$) was increased from -1.5 to +1 V. As expected, the LSR devices reached lower saturation currents than the non-LSR devices. Due to their higher temperature rise, the LSR devices electron mobility and thus decrease the drain current.

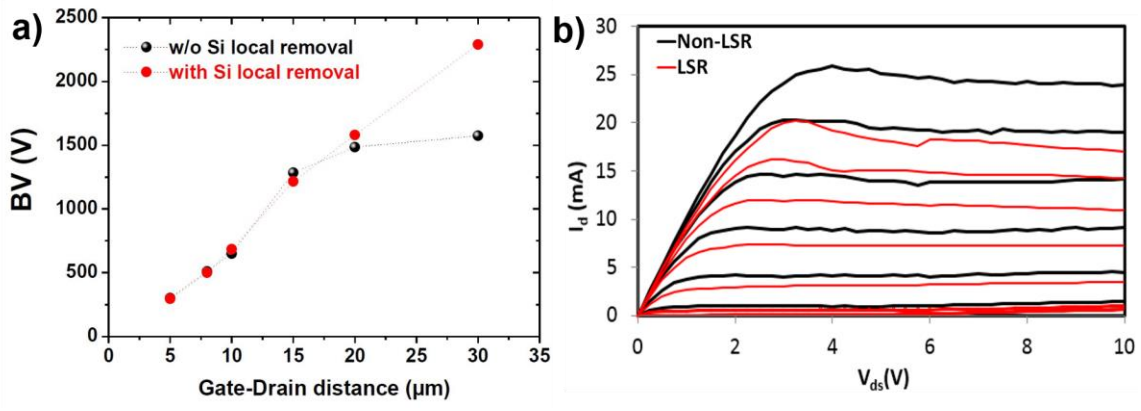



**Figure 79: a) Improvement of breakdown voltage when locally removing the substrate [131] b) Comparison of IV Characteristics of local silicon removed device (red line) and no silicon removed (black line). Drain bias ($V_{ds}$) was swept from 0 to 10 V while the gate bias ($V_{gs}$) was held constant at biases from -1.5 to 1 V in 0.5 V increments.**

For all measurements, electrical parameters were set as follows. The source-drain voltage (Vds) was set to 10 V and the drain current (Id) was varied by sweeping the gate-source voltage (Vgs) from -3 to 1 V in order to measure a range of power dissipation densities up to 6 W/mm (Power densities calculated using the 50 μm gate width). The gate current, Igs, was generally measured to be in the range of 0.1 mA indicating low leakage current. For both types of measurements, pinch-off mode was measured first for a minimal current baseline.

## 7.3 Application of Raman Active Nanoparticles

All temperature measurements were conducted using a Renishaw InVia Raman microscope with a 0.25 m focal length spectrometer and a 488 nm laser as the excitation source. To estimate the uncertainty in the temperature measurements with 95% confidence intervals, an average of 10 measurements was made at all power conditions. Both the calibration and measurement steps for the Raman thermometry measurements were done with the temperature controlled stage. A constant base temperature of 303 K was applied when biasing the device. It was found that all phonon frequencies including GaN, AlGaN and AlN showed a linear temperature dependence. The channel temperature of the devices was then either estimated using the two-peak fit method to correct for thermoelastic stresses or directly from the calibration curve for each peak.

The use of the GaN and AlGaN phonon frequencies to measure the temperature rise of the device represents a volumetric average (1 μm diameter multiplied by the depth of the GaN layer). As both devices possess thick buffer layers, the temperature gradient across the depth will be significant enough to cause the volumetric averaged temperatures measured by Raman to appear lower than the maximum temperature rise. To allow stress-free measurements at the top of the device channel, $TiO_2$ and ZnO nanoparticles were deposited on top of the device to provide a unique Raman surface temperature measurement (further detail discussed in Chapter 4). A sample of the Raman spectra of the LSR and non-LSR device is shown in Figure 80. A calibration was performed prior to measuring the particles to ensure a consistent relationship between the Raman shift and temperature. To determine whether the nanoparticles have any significant impact on the HEMT operation, I-V characterization of the devices were performed before and after the

nanoparticle deposition. For both $TiO_2$ and ZnO, the I-V curves obtained after deposition were found to be very similar to the initial curves.

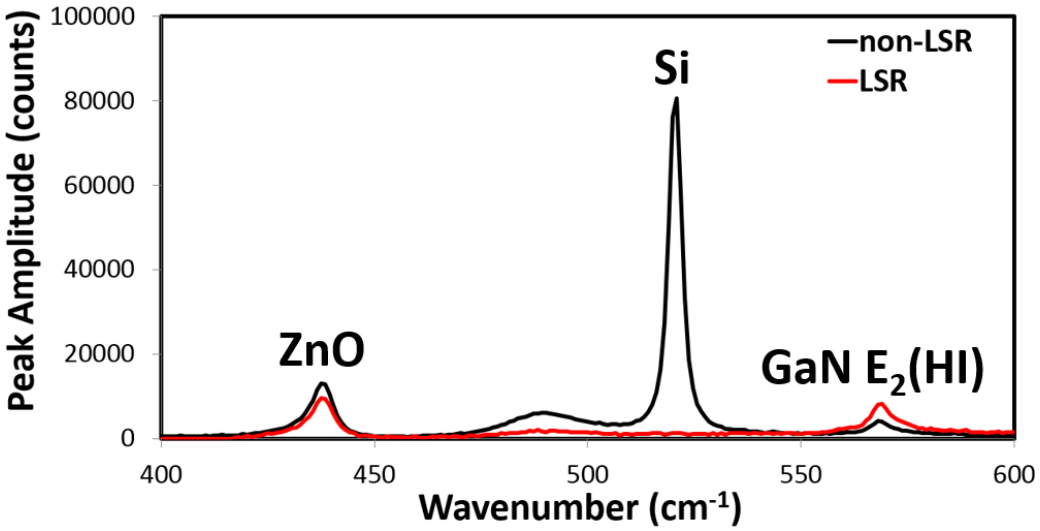



**Figure 80: Example of Raman spectra obtained when probing locally silicon removed channel (LSR) and no silicon removed channel (non-LSR). The Raman peak of ZnO shows the potential of simultaneously probing the surface temperature as well as the average volumetric averaged temperature.**

### 7.4 Thickness Dependent Vertical Temperature Gradient

Initial measurements were conducted on the device with the 5.5 μm buffer layer from Figure 77a to compare the surface temperatures measured via the $TiO_2$ nanoparticles with the volumetric averaged GaN temperatures by Micro-Raman (see Figure 81). For direct comparison of the two techniques, measurements were taken at the middle of the finger with the center of the Raman laser 1 μm away from the gate edge. For power densities up to 6 W/mm at a 10 V drain bias, the temperatures obtained by the $TiO_2$ nanoparticles resulted in temperature rises up to 40 degrees higher (66%) than the volumetric averaged GaN temperatures.

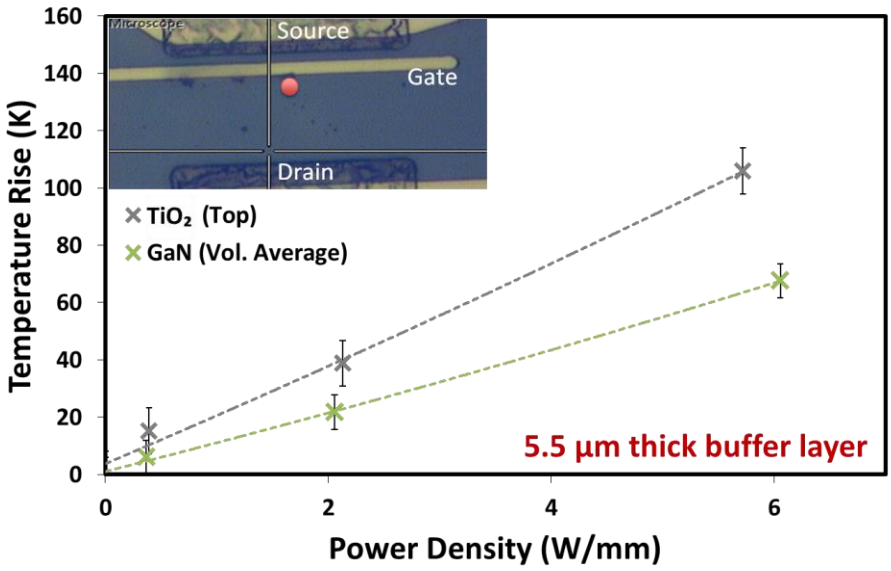



**Figure 81: Thermal response of 5.5 µm GaN buffer layer HEMT. Comparison of $TiO_2$ surface temperatures (grey) and volumetric averaged GaN temperature (green). Image of location where Raman measurements were taken (top-left).**

To determine whether there are significant temperature gradients across the thinner 2 µm buffer layer, ZnO particles were used to measure the channel surface temperature of the non-LSR device. As seen in Figure 82, the surface temperature results in differences up to 20 degrees higher than the volumetric averaged GaN temperatures. The increased temperature confirms that a large temperature gradient exists even across thinner buffer layer and therefore nanoparticles should be used to estimate the maximum temperature rise across buffer layers. Furthermore, the larger temperature gradients shown across the thicker buffer layers confirms the need for avoiding growing large buffer layers when attempting to increase the breakdown voltage GaN-on-Si HEMTs.

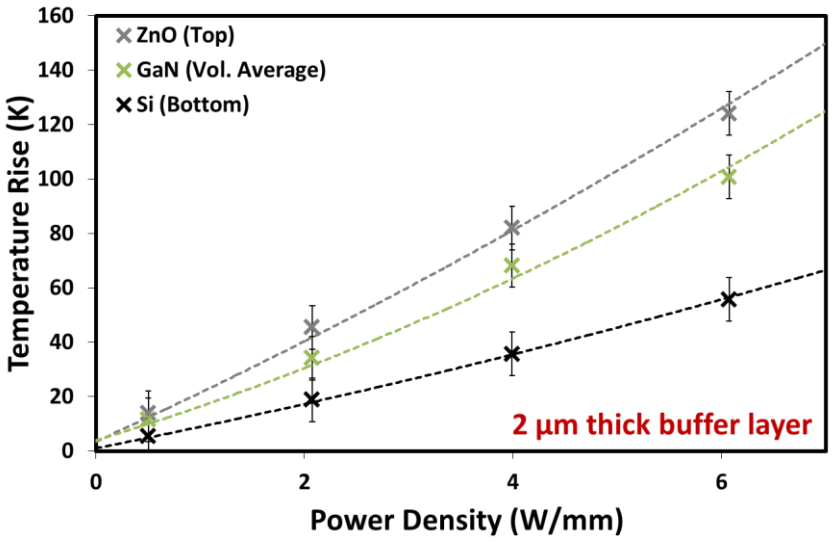



**Figure 82: Thermal response of 2 µm AlGaN buffer layer HEMT. Comparison of ZnO surface temperatures (grey), volumetric averaged GaN temperature (green) and silicon base temperatures (black).**

## 7.5 Effect of Substrate of Removal

After having fully characterized the thick buffer layer device with nanoparticles, the thermal performance of the LSR device was measured and compared to its non-LSR counterpart (see Figure 83). As predicted, the thermal dissipation for the LSR device was proven to be much lower than the non-LSR device. The gate voltage was increased for both devices until a channel temperature rise of 200 °C was obtained. Due to poor thermal dissipation, the LSR was only able to reach a power density of 3 W/mm while the non-LSR could operate until 10 W/mm (approximately 2.8 times greater).

The significant increase in temperature between the LSR and non-LSR device (150 K difference at 3 W/mm) suggests that the device lifetime and reliability will dramatically decrease when removing the Si substrate. Although the etched substrate devices have been shown to increase the breakdown voltage up to 2000 V, the device current carrying capability would be limited in order to manage the junction temperature rise. Assuming a

device will operate at 95% efficiency (dissipating 3 W/mm as heat to ensure maximum temperature rise of 200 K), the maximum current at 2000 V would be 1.5 mA.

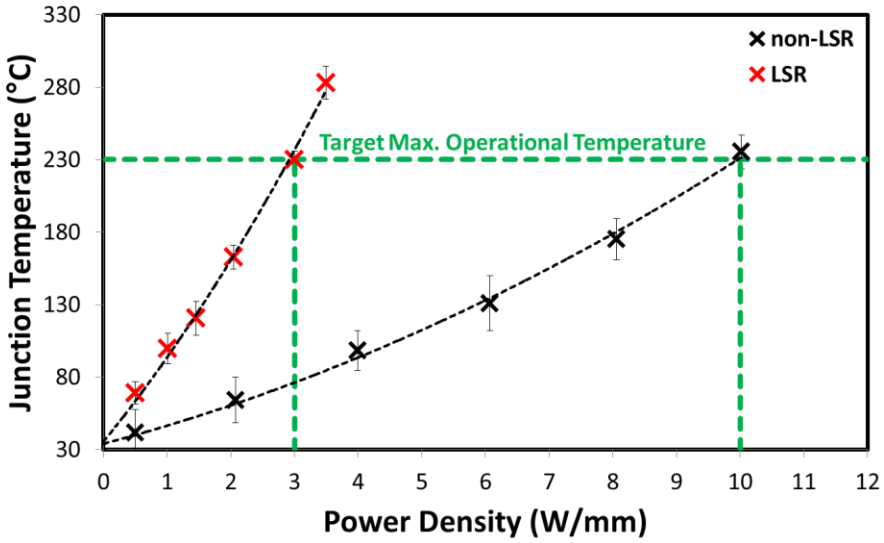



**Figure 83: Comparison of thermal performance between local silicon removed device (red) and non-LSR device (black). Temperature rises were computed using ZnO particles. The non-LSR device shows to achieve a maximum power density of 10 W/mm while LSR device can only perform up to 3 W/mm.**

## 7.6 Improvement of Thermal Performance by AlN/Cu Layer Insertion

To be able to support a high electric field with higher current carrying capability, an improvement to the thermal performance of the LSR devices would be necessary. This can be done by depositing a material with a high breakdown field (>4 MV/cm) and a relatively good thermal conductivity into the trench of the LSR devices such as AlN. Developments in the fabrication processes at IEMN enabled to accomplish this by depositing PVD AlN below the etched membrane (see Figure 84c). To improve the thermal dissipation, an additional 2 μm of Cu is deposited below the AlN (see Figure 84d).

The thermal performance of these novel structures was initially assessed using Raman thermometry. As discussed in the previous section, measurements were taken 1 μm

from the gate on the drain edge at the center of the gate width. Since the GaN layer thicknesses did not change between the device structures, the two-peak method was used to assess the volumetric averaged temperature rise across the GaN layer. The device geometry was similar to the devices studied in the previous section (shown in Figure 78) except that the whole device was either etched or non-etched instead of selectively etching of each finger. The gate to drain spacing for the devices was 40 μm. The temperature of the device was assessed when both fingers were biased. Figure 84 shows the steady state thermal response of the devices under DC biasing for two different drain biases: 10 V and 28 V.

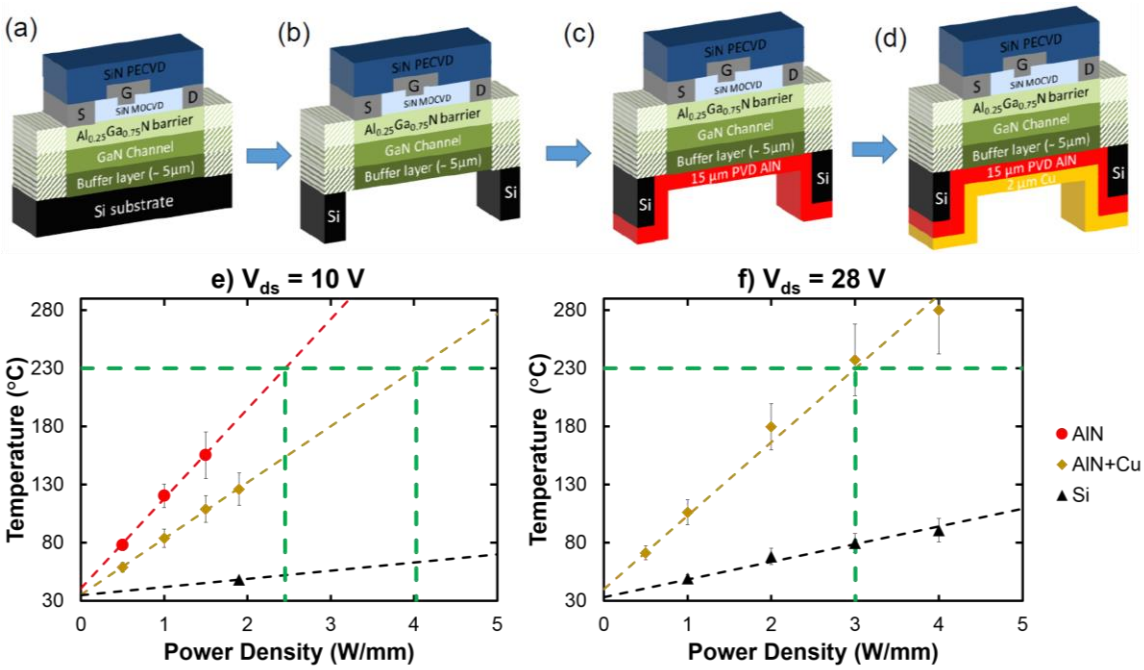



**Figure 84 Device stack configuration of GaN HEMTs studied with a) silicon substrate b) Etched substrate c) AlN filled trench d) AlN/Cu filled trench [132]. Comparison of thermal performance, measure by Raman, between different stack configuration at a constant gate bias of e) 10 V and f) 28 V**

Temperature measurements were taken at different power densities and linear fittings were used to extrapolate the maximum power density achieved at a temperature rise of 200

K. For both drain bias conditions, the temperature rise is seen to decrease when transitioning from solely the AlN layer to an additional copper layer being deposited below it. As expected the Si device achieves a much lower junction temperature in comparison to the etched devices even after the addition of the AlN and the Copper layer. For a drain bias of 10 V, a 11.6x and 7x reduction in maximum power density is observed for the AlN and AlN+Cu device respectively. Increasing the drain voltage to 28 V, the heating profile becomes more localized and the temperature measured become significantly higher. A 4.3x reduction in power is achieve by the AlN+Cu device in comparison to the silicon one. The magnitude in reduction of power is shown to be significantly greater than the power reduction reported in the previous section for the LSR vs non-LSR comparison. The increase in thermal resistance observed in these newly fabricated devices can be attributed to the full etching of the substrate below the device. In the previous scenario, the substrate was locally removed below the channel and thus resulted in a smaller increase in thermal resistance. Fully etching the substrate removes the possibility of the localized heating to be conducted via the substrate.

To benchmark the thermal performance of these novel structures under conditions similar to those applied in real life, the temperature rise under puled biasing was estimated using TTI. The gate to drain spacing for the devices tested was 20 μm. The presence of a thick SiN passivation layer made it difficult to assess the temperature distribution of the GaN channel. Despite several LED excitation sources resulting in strong thermoreflectance signal from the GaN region (340 nm, 365 nm, 405 nm and 470 nm), thin film interference effects caused non-uniformities in the signal and resulted in large uncertainties due to low signal to noise ratios. The most consistent signal was found to be achieved from the gate

metal when using a 365 nm LED source. The $C_{th}$ was estimated to be 1 x $10^{-4}$ °$C^{-1}$. The TTI maps measured for each device is shown in Figure 85. To directly compare the transient thermal performance to the steady state Raman results, the devices were pulsed biased with a drain bias of 28 V for 100 µs time period with a 10% duty cycle. Similar to the steady state analysis, the AlN device resulted in the highest temperature rise (approximately double the temperature rise detected in the Si device).

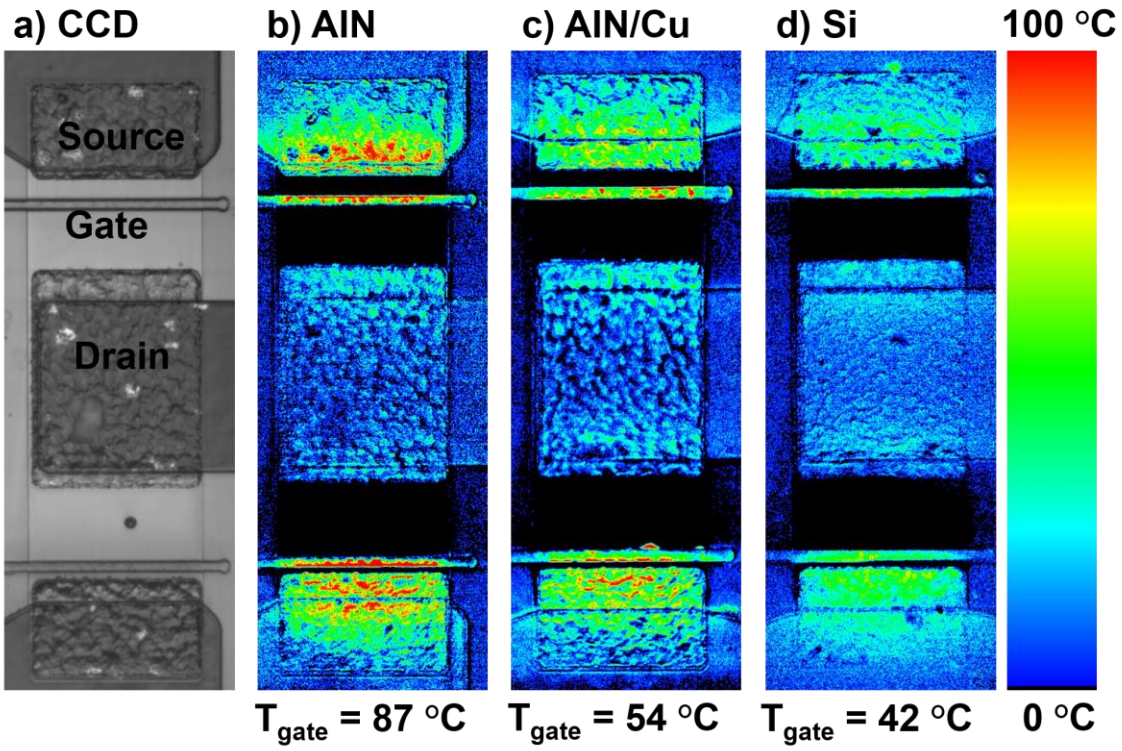



**Figure 85: Comparison of TTI maps representing the temperature rise of the metal contacts. A 365 nm LED excitation was used. Devices were pulsed biased for a 100 µs period with a 10% duty cycle. A drain bias of 28 V was applied corresponding to a peak power density of 5.6 W/mm.**

Performing a transient sweep of the three devices, the temperature rise and decay of each device can be plotted against each other (Figure 86). Both the AlN and AlN+Cu device are shown not to reach a steady state temperature within the 10 µs pulse signifying

the time constants associated with these devices are longer than 10 μs. In contrast, a first order exponential fitting was applied to the Si transient temperature rise and a time constant of 8.5 μs was extracted. Similar trends were found when assessing the transient temperature profiles of the devices studied in the previous section where thermal time constants of 5 μs and 17 μs were extracted for the nonLSR and LSR device.

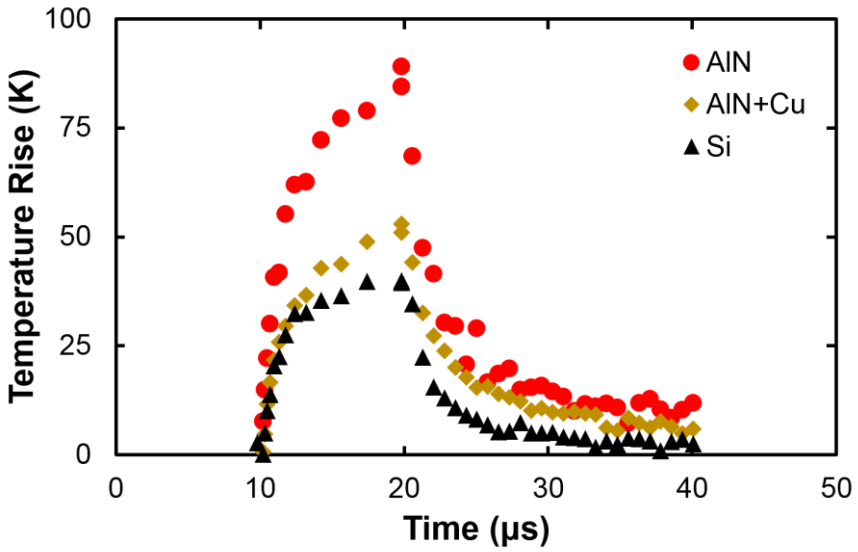



**Figure 86: Transient thermal profiles of gate metal temperature rise using UV TTI.**

## 7.7 Residual Stress Analysis

Apart from the thermal performance of etched silicon devices, the residual stress of the GaN layer was also measured to determine whether the etching process or the addition of new materials would cause any relaxation in the buffer layer. Stress mappings were conducted across the channel between the gate and drain in 10 μm steps along the gate width and 5 μm steps across the channel. Residual stress measurements were measured using a Horiba Jobin Yvon LabRAM HR800 with a 325-nm laser as the excitation source. Similarly to the temperature measurements, the incident laser power was adjusted to

prevent self-heating of silicon (0.33 mW). A liquid nitrogen cooled CCD camera was integrated into the system to image the collected PL spectra. Experiments were carried out with a 39x NUV objective. The reference for the band gap strain-free GaN which was used to predict the residual stress of the GaN layer was taken from [98].

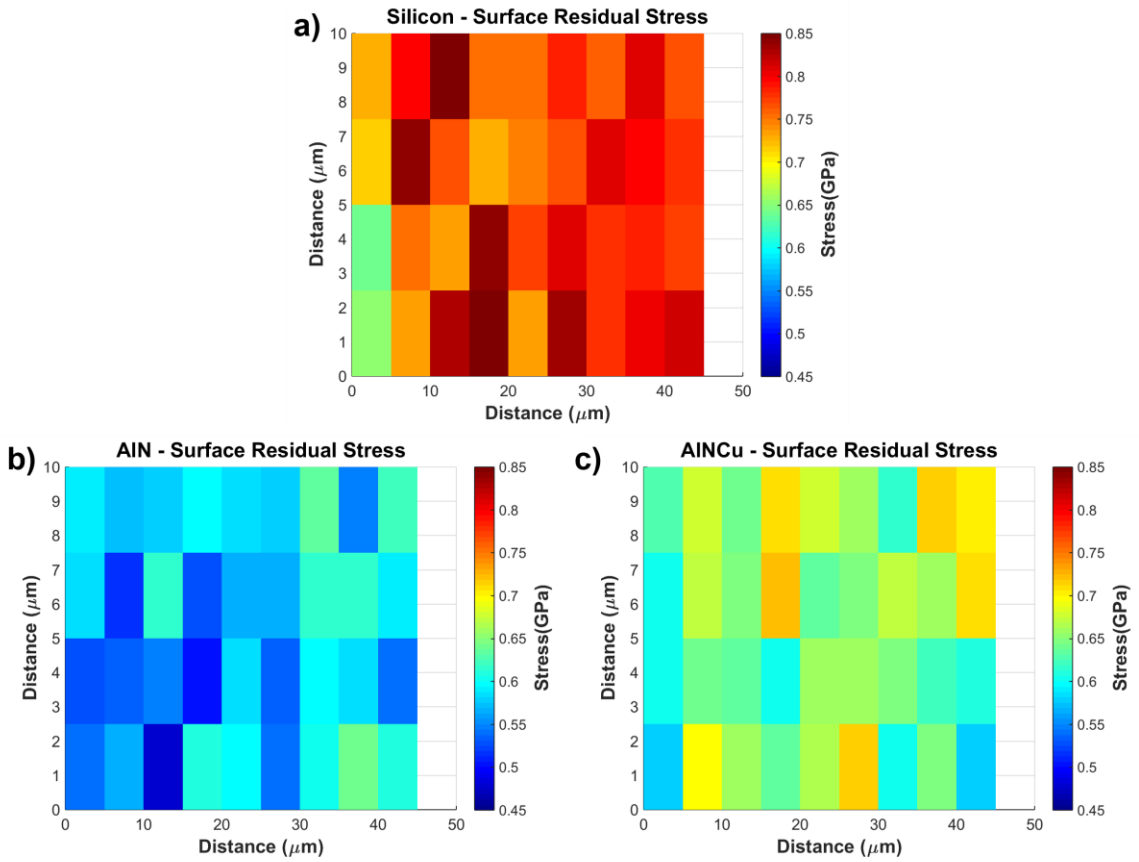



**Figure 87: PL residual stress mappings of the three different devices structures studies. Stress mappings were performed between the gate and drain in in 10 µm steps along the gate width and 2.5 µm steps across the channel.**

The residual stress mappings for the three different devices is plotted in Figure 87. As previously shown in literature [98], the residual stress in GaN grown on Si is found to be tensile (approximately 800 MPa). The removal of the substrate and the addition of the PVD AlN layer demonstrates a reduction in tensile stress. The average residual stress was found to be approximately 600 MPa. This reduction in stress is beneficial for the device

reliability to reduce the peak stress exhibited by the device during operation. Measuring the stress distribution after the copper layer has been deposited, a slight increase in the overall average stress is observed (700 MPa).

## 7.8 Summary and Conclusions

The removal of substrate below the electric field of GaN-on-Si HEMTs has proven to significantly decrease its thermal performance. Using Raman Spectroscopy, temperature increases up to 150 K between a non-etched and etched substrate device are observed. Consequently, this limits the device's maximum power density by reaching critical temperatures for degradation at much lower powers. The successful use of ZnO and $TiO_2$ nanoparticles to measure the device surface temperatures has shown that large temperature gradient exist across the thick buffer layers and therefore the average temperature measured across the buffer layer tends to under predict the gate junction temperature. Overall, the removal of Si below the channel allows for higher break down voltages in the off state but prevents the excessive Joule heating during operation from being conducted through the substrate. In order to maintain a high electric field strength, the thermal performance of the etched Si can be improved by depositing a combination of materials such as AlN and copper inside the trench. The transient thermal profiles of these devices were assessed and the addition of these layers were found to indeed improve the thermal performance.

Apart from the thermal effects of the substrate removal, residual stress mapping via Photoluminescence shows that the GaN layer becomes less tensile in regions where the Si is removed and AlN is deposited. A slight increase in the residual stress is observed with

the addition of the copper layer. The relaxation of the GaN layer may potentially increase the device performance.

# CHAPTER 8. CONCLUSIONS

Gallium nitride (GaN) based electronics have shown great potential for radio frequency (RF) devices and power electronics. The developments of transistor technology in these two markets has been designed differently to meets the needs of the customer. More specifically, epitaxial GaN is grown on different substrates for these two industries. RF electronics require high frequency and high power density operation resulting in the need of a thermally conductive substrate such as SiC. To ensure high electron mobility, high quality GaN must also be grown requiring a substrate material with a small lattice mismatch. Prioritizing a low cost of manufacturing for power electronics, an effort towards using a silicon substrate has emerged over the last decade. Taking advantage of unused silicon foundries, GaN can be grown on silicon wafers that have double the diameter of SiC yielding higher output. To ensure a low number of defects in the GaN, strain engineered layers using superlattices have been implemented. Furthermore, silicon's inherent weak electric field strength has motivated the fabrication of GaN/Si HEMTs where the substrate is subsequently etched. In both cases, GaN is grown on a foreign substrate and the devices are operated in the lateral direction in relation to the substrate.

In both cases, the quantification of performance parameters such as the gate junction temperature is necessary to accurately assess the device's quality and lifetime. For lateral devices, Raman thermometry has shown to be the most accurate method to estimate the junction temperature. This method, however, is limited to a point measurement and sometimes may be limited by its optical access. Furthermore, the ability to monitor the transient temperature rise under pulsed conditions has not yet been fully developed.

Advanced techniques were developed in this study to provide an in-situ transient temperature measurements and temperature mappings across GaN based electronics. The results presented show the necessity of using different techniques to address these two issues. For in-situ transient temperature monitoring, electrical methods are preferred due to their simplicity and easy implementation. Gate Resistance Thermometry (GRT) was proven to be the most accurate electrical thermometry method. For mapping the transient thermal distribution of devices, the advantages of using Transient Thermoreflectance Imaging (TTI) are presented and applied to different technologies. Throughout the study, the limitations of each technique are discussed and contrasted with each other.

## 8.1 Summary of Contributions

### *8.1.1 Electrical Methods*

An in-situ transient GRT method for pulsed biasing measurements with a sub-microsecond resolution is developed (Chapter 2). The technique is shown to yield high accuracy and be easily integrated into device structures. The sources of error associated with GRT are quantified and the solutions to account for them are presented. This includes the effect of the drain bias, the length of the gate width, the accuracy of the calibration coefficient, and the magnitude of the leakage current.

The first ever GRT measurements are performed under RF operation (Chapter 3) enabling the characterization of the junction temperature under real life operating conditions. A direct comparison between the Joule heating profile under DC operation and RF operation is conducted to help understand the difference in degradation mechanisms

between the two modes. The average temperatures achieved show an improvement in thermal performance when the device is operated under RF operation.

### *8.1.2 Optical Methods*

The application of using $TiO_2$ nanoparticles for surface temperature mappings of GaN HEMTs is presented and it is proven to provide an accurate strain free surface temperature measurement (Chapter 4). This enables the temperature mappings on any point of the device irrespective of the material found below it. The implementation of nanoparticles transparent to the lasers used for Raman is also shown to offer opportunities for vertical thermal characterization of electronics. The temperature gradients in GaN/Si HEMTs and Vertical PIN diodes are demonstrated and are shown to accurately estimate the device peak temperature.

Major developments in Transient Thermoreflectance Imaging (TTI) are presented (Chapter 4) to enable the direct probing of the GaN layer. Until now, the technique has required adjusting the calibration coefficients to match simulations in order to accurately measure the transient temperature rise. Introducing the use of UV TTI, a mapping technique to measure the temperature rise across all areas of the device including the GaN channel is demonstrated. The novel technique is applied to cross sectioned GaN/SiC to show the first ever cross-sectional temperature profiles within these devices. Previous literature has been limited to numerical simulations and indirect experimental methods to show the bias dependence of the Joule heating profile. The effect of bias conditions has now been directly quantified via the use of UV thermoreflectance imaging (Chapter 5).

Improvements to the errors associated with TTI are developed and applied to different GaN transistor structures. The need for a point by point calibration to accurately map the temperature distribution in GaN HEMTs is proven (Chapter 6). Furthermore, the effects of thin film interference and its relation to both the thickness and the number of layers present in the stack configuration are highlighted.

The tradeoff between electrical and thermal performance of GaN/Si HEMTs is assessed and quantified. The insertion of strain relief layers to improve the breakdown voltage of GaN HEMTs is shown to significantly increase the overall thermal resistance of the device (Chapter 6). The thermal penalty of removing the silicon substrate to contain the electric field within the GaN is also quantified (Chapter 7). Improvements to the thermal performance of these devices is shown via a backside deposition of an AlN dielectric layer and a copper thin film. The difficulty in applying the TTI technique to thin film membrane structures such as these, highlights the need for Raman active nanoparticles to accurately assess the devices thermal distribution.

## 8.2 Future Work

For gate resistance thermometry, the temporal resolution must be improved to the GHz range in order to accurately assess the temperature swing in RF devices. Development of an experimental setup using pulsed RF equipment can enable the transient monitoring of the device temperature under RF operation. To enable a deeper understanding into the transient thermal dynamics of GaN devices and the thermal time constants associated with the different materials and interfaces, analytical or numerical models can be developed to extract the time constants associated with the device.

While addressing the thermal challenges, it is equally important to characterize the defects formed in devices as quantification of degradation. Applying high voltages across AlGaN/GaN HEMTs can induce large stress gradients in the channel in addition to the stress created by the thermal expansion mismatch between the gate metal and GaN. These large stresses create additional defects in the material which can enhance failure mechanisms such as electron trapping and percolation. Typical defect characterization methods of these materials include Atomic Force Microscopy (AFM), Scanning Electron Microscopy (SEM) which require the removal of metal contacts thus making the device non-functional. The primary non-invasive electrical technique used for identifying the activation energy associated with traps is Deep-level transient spectroscopy (DLTS). Based on the sensitivity of GRT, a new electrical defect characterization technique could be developed using the gate metal as a defect sensor. Converting the gate metal into a pulsed heater and sensor, the gate heater could be swept at different frequencies and obtain a thermal response. Using defect characterization techniques, the effect of defects on the thermal response could be correlated and would provide quicker characterization techniques of electronic devices without having to modify the device structure. For example, this will allow to explore the effects of biasing conditions and growth processes on the defect formation in HEMTs.

More accurate evaluation of the thermoreflectance coefficient in GaN when using UV illumination wavelengths is needed. The development of an optical model to quantify the percentage of light reflected from each interface and its contribution to the thermoreflectance signal detected would greatly assist in understanding the errors associated with measurement.

Similar to the Raman active nanoparticles, the resolution and accuracy of thermoreflectance imaging can be improved by the addition of a new thermoreflective material. The material must yield a high thermoreflectance coefficient, be electrically insulating and partially transparent and must also be easily deposited on samples. The implementation of such material would minimize the effects of the thin film interference and the error associated with the uncertainty in measuring the thermoreflectance coefficient.

Currently thermoreflectance imaging is performed using an excitation source with a broad wavelength emission. When measuring devices with multiple thin layers, thin film interference can alter the thermoreflectance expected from a single material causing error in the thermal measurement. It has been preliminary shown that using a hyperspectral illumination (repetitive measurements performed with different wavelengths) rather than a single wavelength can improve accuracy and result in a clearer thermal image of all regions of an electronics system. Improvements in thermoreflectance imaging can be made by implementing a high intensity white light with different bandpass filters to emit different wavelengths of light when desired (hyperspectral emission) and transmit specific wavelengths to the CCD. Not only will this remove the necessity of multiple excitation sources but it will permit a full thermal mapping of every electronic system irrespective of the material. The thermal properties of extreme bandgap devices based on materials such as AlGaN, Gallium Oxide and Diamond could be investigated.

For a cross sectional thermal mapping, direct mapping of temperature gradients across interfaces will give deeper insight into how to improve the thermal boundary resistance between epitaxial layers. Until now, theoretical and atomistic level models have

been developed to characterize the heat transport across interfaces. Having the ability to directly compare these models to experimental data, new models can be developed to help understand the effect of defects, roughness, anharmonicity and interdiffusion on these interfaces. This technique can also be used to evaluate new patterned interfaces that could improve thermal interfaces. For improving the performance of GaN/SiC HEMT, combining 2D electrothermal simulations with cross sectional thermal imaging to study the effect of bias conditions and substrate selection on the Joule heating distribution will lead to the comparison of DC to RF operation. This study will answer key questions surrounding their reliability, where it is still unknown if it is accurate to perform DC reliability testing in lieu of expensive RF testing. To ensure the cross sectioned HEMT electrically functions in a similar manner to a non-cross sectioned device, further electrical characteristics must be monitored (including the logarithmic IV curves at μW/mW power dissipation. This will ensure that the temperature profile monitored across the cross-sectioned HEMT will be identical to the Joule heating profile distributed across a non-cross sectioned device. Exploring the possibility of cross sectioning the device outside the active region may also assist in achieving this goal.

The addition of a deep depletion CCD for Electroluminescence (EL) to thermoreflectance system will enable the direct correlation of electron trapping to thermal properties under RF operation. Ultimately, the path of the electrons flowing through the channel will also influence the Joule heating profile. Using EL under steady state conditions, areas where hotspots will form can be potentially predicted without having to bias the device with high drain currents. Intensified CCDs with a microchannel plate to perform transient EL measurements can also enable time constant extraction which can be

directly compared to the ones achieved by transient thermal characterization. Not only will this be significant for modelling device physics and the electron-phonon coupling mechanisms but it will also assist in optimizing the electrical and thermal performance of novel materials devices.

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