FINAL REPORT
For the project

CMUTs with integrated electronics for forward looking IVUS imaging

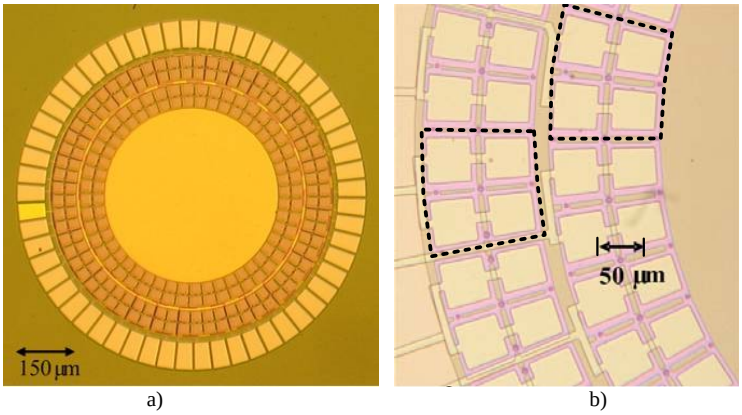
Original Project Summary

Capacitive micromachined ultrasonic transducers (cMUTs) have a great potential for implementing miniature arrays for intravascular ultrasound (IVUS) imaging. The Degertekin laboratory has recently developed cMUT manufacturing processes which enable post-CMOS fabrication of cMUT arrays for electronics integration. The purpose of this research proposal is to develop forward looking cMUT IVUS arrays and associated electronics for operation in the 10-50MHz range, and investigate the feasibility of integration of high performance cMUTs with CMOS electronics on a single silicon chip for the first time. If successful, this project will lead to low-cost forward looking IVUS imaging devices with high imaging performance and enable numerous diagnosis and therapeutic applications of IVUS.

With the stated goals above, during the past several years, our efforts in this project have resulted in significant advances in CMUT structures, front-end integrated electronics, IVUS array designs, and finally monolithic CMUT-CMOS integration. These results have been reported in several journal papers in addition to numerous conference proceedings including four best student paper award winners. Some of the results relevant to this project are summarized here.

Dual-Ring Annular CMUT Arrays

In a ring-shaped FL annular array, the need for small element size both in radial and lateral dimensions to avoid grating lobes leaves an unused area around the center guide wire opening. The difficulties in piezoelectric transducer fabrication technology limit the array structure to have a single ring array. *By taking advantage of the flexibility offered by CMUT technology, we proposed and implemented multiple-ring arrays for FL-IVUS imaging to utilize this area efficiently*. A particular example of this array configuration is a dual-ring array, where separate transmit (Tx) and receive (Rx) arrays are employed. **Figure 1** shows a 10MHz dual-ring annular CMUT array with 32 Rx and 24 Tx elements we fabricated for testing purposes. The detailed parameters are given in Table 1. T*his dual-ring array configuration enables the Tx and Rx arrays to be independently optimized for transmit or receive operation. For example, each ring can have a different DC bias, gap thickness, membrane or electrode size, or different number of membranes for CMUT element to control the receive sensitivity and transmit pressure generation independently.* Similarly,



a) b)

Figure 1. Pictures of a) a fabricated dual-ring array, b) close-up view of a few Tx and Rx elements each consisting of 4 parallel CMUT cells. Note that a significant outer area of the chip is reserved for electrical connection bondpads.

the size and operation mode of the CMUT membranes in the Tx and Rx arrays can be adjusted to have different frequency responses, which may be useful for harmonic imaging or broadband operation. *In addition, the area underneath the CMUT array element may be utilized more efficiently for monolithic CMUT-on-CMOS electronics integration as the demand for Tx/Rx switch is either relaxed or eliminated. An important point to note is that, in terms of image resolution, this configuration provides the nearly the same performance as compared to single-ring without losing active area as the Tx and Rx ring arrays are close to each other, separated about half a wavelength at the center frequency.* Our project uses some of these features to build the single chip imaging arrays and investigates some novel array architectures.

TABLE I
DUAL-RING ARRAY PARAMETERS

Number of array elements	24-Tx and 32-Rx
Overall array size	1 mm
Array size (excluding bond pads)	800 µm
Elements size	70 µm x 70 µm
Cell size	35 µm x 35 µm
CMUT cells per element	4
Top electrode thickness/coverage	0.12 µm / 70%
Gap thickness	0.1 µm

Array Characterization

To test the performance of the dual-ring CMUT arrays we designed and built a custom IC in a standard 0.5-µm CMOS process of TMSC available at MOSIS. Each 1.5-mm^2 receiver IC chip has 8 channels with 20-k gain common source transimpedance amplifier (TIA). The TIA has a 50-MHz bandwidth for 5-pF input capacitance. In addition, the chip has 8×1 MUX and buffer amplifier to drive the output cable. A picture of the chip is shown in **Figure 2-a**. We placed the CMUT dual-ring array on a 64-pin chip carrier. The CMUT array and 4 IC chips for 32 Rx channels were placed on a glass substrate with patterned metal layer for interfacing the chips. The electrical connections between array elements and IC chips were provided by wire bonding. A picture of the integrated array chip is shown in **Figure 2-b**. We used a test setup consisting of three aluminum wire targets immersed in oil; each with a diameter of 600 µm to characterize the pulse echo response of the array element as shown in **Figure 2-c**. As seen in **Figure 2-b**, more than 120 wire bonds were made to connect the electronics to the CMUT array through the glass routing substrate. *This approach is cumbersome and reduces overall reliability. As will be shown in the next sections, we resolve this issue with direct fabrication of CMUT array on CMOS electronics..*

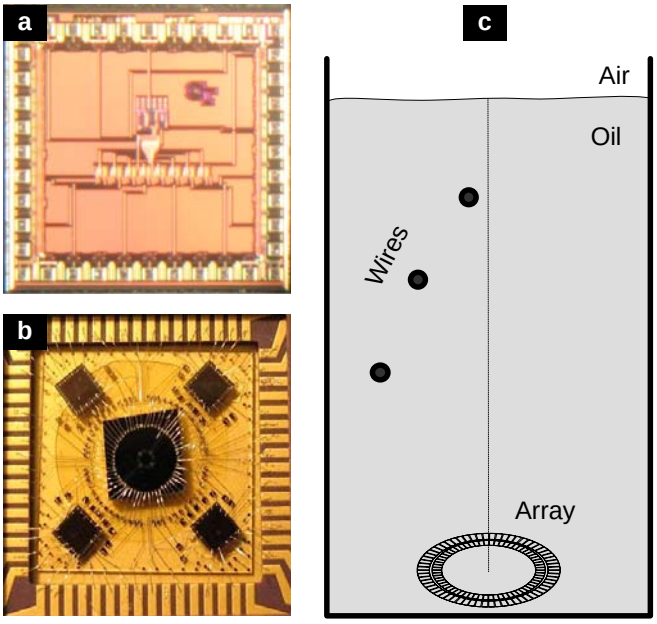


Figure 2. a) Picture of the IC chip. b) Picture of the integrated CMUT array. C) Schematics of the test setup consisting of three wire targets, each with a diameter of about 600 µm.

Both the transmit and receive arrays were operated in conventional mode at 90% of the collapse voltage and 50V peak signal is applied to the transmit elements. We collected 768 RF A-scans from 24×32 Tx-Rx element combinations and generated

beamformed temporal and frequency responses of the array using the experimental 2-D PSF of the third target as shown in **Figure 3**. This frequency response represents the overall array response and shows a 6-dB FBW of 80% at 10.3-MHz center frequency. The measurement also shows the effect of substrate ringing around 7.6MHz and some cross talk effects. The first issue is addressed by thinning the silicon wafer and applying a backing. The cross talk will be investigated further especially after the array chip is shaped as a donut as this would change the cross talk behavior.

We computed SNR of each A-scan as the ratio of RMS amplitude in ta time window including the echo signal of the third target which is at 1cm distance from the array (f/12.5) to the RMS amplitude in time window including no target echo. The SNR values for non-averaged single Tx single Rx element reaches 22 dB with some channel to channel variation mostly due to the non-ideal placement and lack of symmetry of the target. *This is significant because this data shows that dual-ring CMUT array elements can provide 22dB SNR from a target at 1cm despite ~6dB higher attenuation in oil around 10MHz as compared to blood. As determined earlier, this SNR level from each firing, along with properly determined set of 210 firings is adequate for real time clinical quality images.* Furthermore, we have determined through experiments and detailed models that the SNR is limited by the TIA noise. As discussed below the TIA noise can be significantly improved by our latest designs in connection with the CMUT-CMOS integration process development.

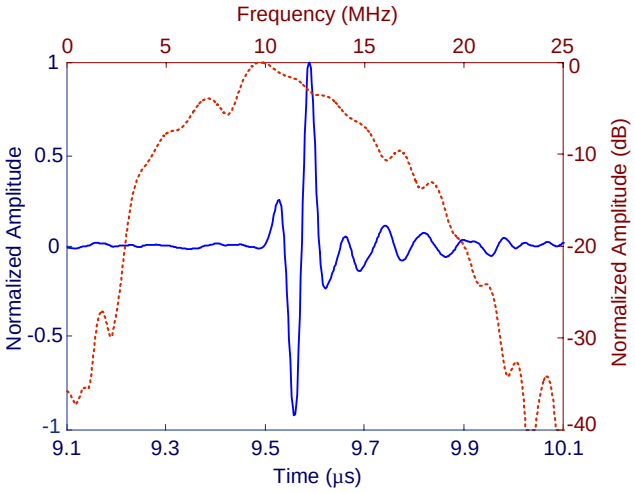


Figure 3. Temporal and frequency responses of the beamformed A-scan.

Demonstration of Volumetric Imaging

To evaluate the imaging performance and verify our models, we reconstructed B-scan images obtained using synthetic phased array beamforming. **Figure 4** shows the B-scan images for orthogonal *xz*- and *yz*-cross-sections with 25-dB dynamic range. We reconstructed three different planes of *yz*-cross-section, where each plane has the maximum intensity corresponding to one of the wire targets. Each B-scan image is normalized to its own maximum. The cross-sectional image of a wire target represents the 2-D PSF if the wire's diameter is smaller than the wavelength. Here the wire's diameter (600 μm) is larger than the wavelength by about four times. The wire's cylindrical surface acts as a specular reflector, and hence the array can only detect a very small portion of the wire's front-surface around the surface normal towards the array. As a result, each reconstructed image in **Figure 4** approximates the 2-D PSF at the target location. The three wire targets are clearly observable in the *xz*-cross-section: the first strong echo is the reflection from the front-surface of the wire, whereas the relatively weak second echo is the echo after the reflection from the back-surface of the 600-μm thick wire. We also observed the multiple reflections on B-scan images with larger dynamic display range, such as 35 dB or higher. We used a 25-dB display range in **Figure 4**

intentionally for the visual illustration of the main- and near side-lobe performances of the PSFs in particular.

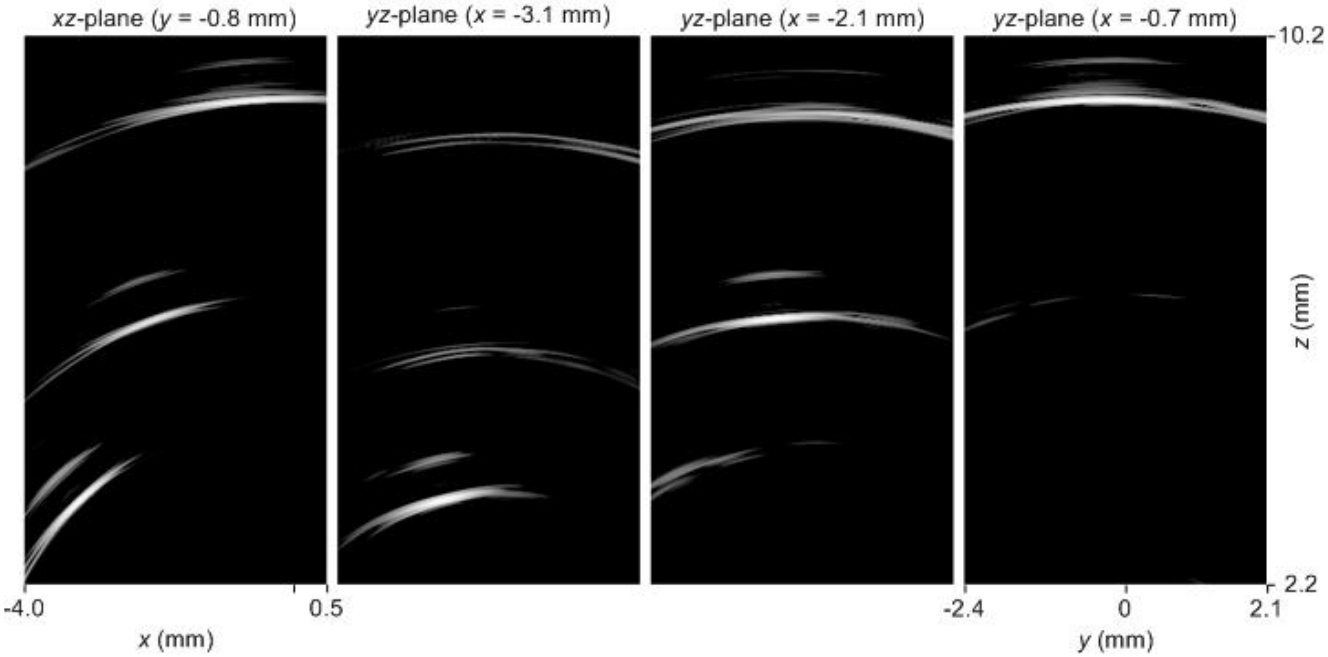


Figure 4. Cross-sectional 2-D B-scan images reconstructed using the experimental data acquired from the test phantom consisting of 3-wires in oil bath. The image depth (*z*-axis) extends from f/3.1 to f/14.2. Each image is normalized to its own maximum, displayed with 25-dB dynamic range.

We used the MicroView software of the GE Healthcare to display a volume rendered image of the same targets as shown in **Figure 5**. The front-surface of each wire target is seen as a patch on this display, while the back-surface of the first target is also observable. Note that this 800µm diemeter array can detect only a small portion of the front-surface of each wire target because most of the specular reflections were not received by the small aperture. Each image should approach to a cylindrical surface as the aperture size gets larger. Nevertheless the results show that the CMUT array is capable of true volumetric imaging. *In the proposed effort, we plan to fabricate 2mm diameter arrays for operation at 10MHz to improve the image resolution for FL-ICE application and increase the operating frequency to 20MHz or FL-IVUS application.*

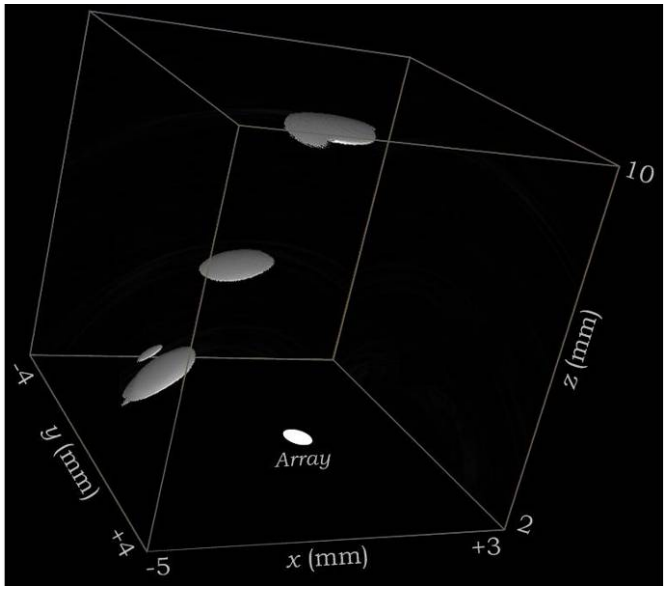


Figure 5. Volumetric display of the image of the phantom with three wire targets. The size of the array relative to the volume is also shown.

<u>Modeling and Verification of Imaging Performance</u>

To verify our imaging models we also constructed both the simulated and experimental 2-D PSFs of the third target on $r\theta$- plane for comparison. For the simulated PSF, we used a point target placed at the coordinates of the 3rd

wire target, a Gaussian pulse and the parameters of the experimental setup. We then produced lateral 1-D PSFs by taking the axial average over a window covering the axial spreads. The two PSFs in **Figure 6** show close agreement around the main lobe. The noticeable differences between the side-lobes of the two PSFs are due to the differences in experimental and simulated pulse-shapes and target types (thick wire vs. point).

TABLE II
MEASUREMENT ON B-SCAN IMAGE
(SYNTHETIC PHASED ARRAY IMAGING WITH 560 TX-RX COMBINATIONS)

		Wire Target		
		1 (f/6)	2 (f/8.5)	3 (f/12.5)
Lateral Resolution	Experimental	0.88 mm	1.1 mm	1.68 mm
	Theoretical	0.9 mm	1.25 mm	1.88 mm
Axial Resolution	Experimental		65 µm	
	Theoretical		93 µm	

The theoretical 6-dB lateral resolution of the dual-ring array can be approximated as

$$6\text{-}dB\ Lateral\ Resolution \cong 1.02 \cdot \lambda \frac{R}{0.5\left(D_T + D_R\right)}$$

where λ is the ultrasound wavelength, R is the target distance from the array, D_T and D_R are the diameters of the transmit and receive rings, respectively [37, 38]. The theoretical lateral resolution of our experimental dual-ring array with D_T = 640 µm and D_R = 800 µm, is equivalent to that of a single-ring array with a diameter of $0.5(D_T+D_R)$ =720 µm. Table II summarizes the experimental axial and lateral resolution figures of the particular dual-ring array along with simulations. The results in Table II indicate that the experimental lateral resolution for the first target is almost identical to the theoretical one, while for the second and third targets it is better than prediction by about 10%. The enlarged aperture size due to the cross coupling surface waves on the transducer array-oil boundary can be the main reason for this discrepancy.

The theoretical 6-dB axial resolution of the dual-ring array can be calculated by using the following expression:

$$6\text{-}dB\ Axial\ Resolution = \frac{0.5 \times v_0}{f_0 \times FBW},$$

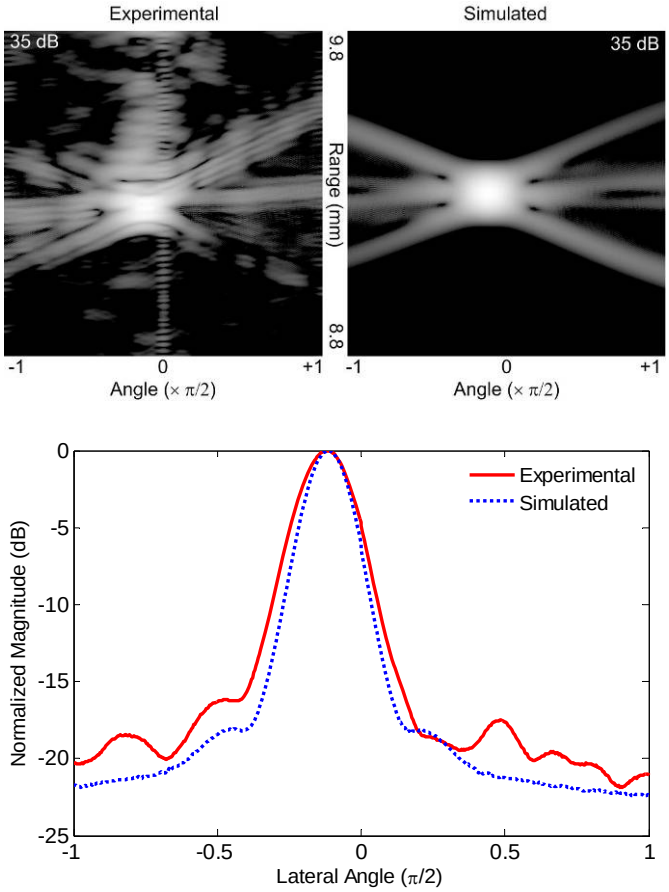


Figure 6. Experimental and simulated 2-D cross-sectional images of the 3rd wire target.

where v_o, f_0 and FBW are sound speed, the center frequency and 6-dB FBW, respectively. We measured an axial resolution of 65 µm, almost identical on all the three wire targets. The theoretical axial resolution calculated by using (3) is 93 µm. This discrepancy between the measured and

expected results is caused by non-uniform pass-band, e.g., the pass-band gain above the center frequency is relatively higher than that below the center frequency (see **Figure 3**). *These results show that we developed the necessary models to predict and analyze imaging performance of the dual-ring CMUT arrays and verified them through experiments. The CMUT arrays provide the bandwidth and overall sensitivity for real time FL volumetric imaging even when a single transmitter receiver pair is used for each firing and wire bonded IC electronics is used. As discussed later in the report, we also developed more efficient and broadband CMUT structures, as well as monolithically integrated electronics which should further improve the array performance.*

Monolithic integration of CMUTs with CMOS Electronics

Single chip MEMS-CMOS integration has lead to the most successful commercial MEMS devices, such as air bag accelerometers from Analog Devices, digital mirror displays from Texas Instruments. We believe that this is also the case for CMUT based miniature arrays for ultrasound imaging like IVUS and ICE. This approach a) eliminates the parasitic capacitance due to interconnect between the electronics and CMUT array element, critical for achieving high SNR from small CMUT elements, b) reduces the chip-to-chip electrical interconnect problem which requires either delicate flex circuits or flip-chip bonding and through wafer vias, complex manufacturing steps reducing the yield and signal quality due to considerable wire bond pad capacitance. W*e had developed well characterized low temperature CMUT processes to enable fabrication of CMUTs on CMOS wafers. Furthermore, these CMUTs have either equal or better performance as compared to their counterparts fabricated using higher temperature processing prohibiting single chip electronics integration.*

More recently, in this project, we demonstrated monolithic integration of CMUT and CMOS electronics. This was based on a wafer scale CMOS electronics fabrication run with a commercial entity using 0.35u, 3.3V TSMC process. We essentially re-designed the electronics used for wire bonded testing for this technology. In addition, the transmitters, logic circuitry and cable drivers were designed with layout compatible with the CMUT imaging arrays, since the electrodes of the capacitive array elements need to be connected directly to the inputs of the array of matching amplifiers. This was a total team effort including Prof. Hasler, Prof. Karaman and having the ME and ECE graduate students working together. A picture of a whole wafer is shown in **Figure 7**. As seen in the leftmost picture of the wafer, a 2.2cm square reticle is repeated to fill the wafer. Each reticle (second from left) is divided in to subsections and half of each reticle is dedicated to CMUT related electronics whereas the other half is used for other projects to share the cost of the wafer run. The last part of the figure shows the details of the layout for one set of CMUT-on-CMOS electronics designed for 8 element high frequency (20-60MHz) annular array for SL- IVUS. This chip is approximately 1mmx2mm in size, has 8 receive amplifiers as well as transmitters. As seen from the drawing, the overlaid CMUT array elements are aligned with the interconnect structure for the amplifiers. The last picture shows the photograph of the fabricated electronics chip. The CMUT arrays on the wafer run include annular arrays, linear arrays of dual-electrode CMUTs, dual-ring annular arrays and other blocks of electronics for testing purposes. The completion of this wafer run was a significant milestone for our CMUT-on-CMOS research.

After the wafers are received, they were cut into 2x3 reticle pieces for post-CMOS CMUT fabrication since the microfabrication facility at Georgia Tech used for CMUT fabrication is a 4" wafer fab. The wafers were coated with a 6µm thick oxide layer which was then polished down to about 2µm to remove the topography of the CMOS electronics and have a smooth surface for CMUT fabrication. CMUT arrays are then implemented on the CMOS electronics and initial tests were performed to see if there were be any thermal budget or electrostatic discharge issues while

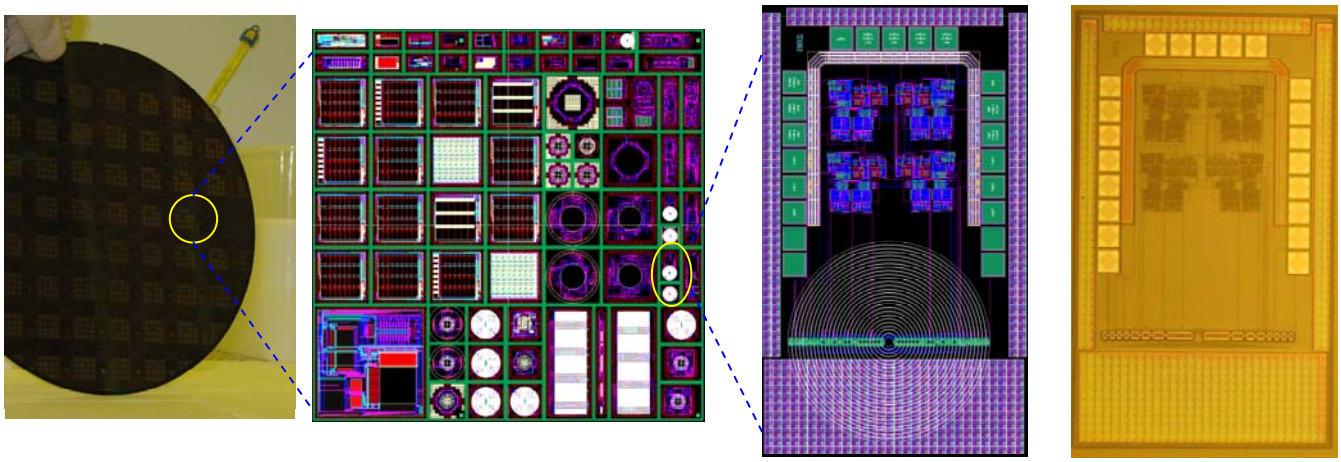


Figure 7. Left to right: The 8" CMOS wafer processed in commercial foundry. Detail of one reticle. The particular 1mmx2mm die for an 8 element annular array with integrated electronics. Picture of the same die on the processed wafer.

CMUT-on-CMOS fabrication. **Figure 8** shows micrographs of one set of CMOS electronics for dual-ring arrays before CMUT fabrication on the left. The figure also shows the same circuit after a 10MHz dual-ring array was fabricated on top of the same electronics. As seen in the picture, the top electrodes of the CMUTs are directly connected to the inputs of the underlying electronics, reducing the parasitic capacitance and achieving the single chip CMUT array with electronics structure. For the ultimate testing, the chips were immersed in oil where the CMUT-on-CMOS array elements with integrated electronics were used to transmit and receive ultrasonic waves. **Figure 9** shows the pulse echo signal from oil-air interface ~4mm away from a simple CMUT-on-CMOS chip amplified and multiplexed by the on chip electronics. The echo signal has adequate SNR without averaging with 100V DC bias on the CMUTs and 10V peak pulse input. The center frequency of the signal is around 17MHz with a fractional bandwith of

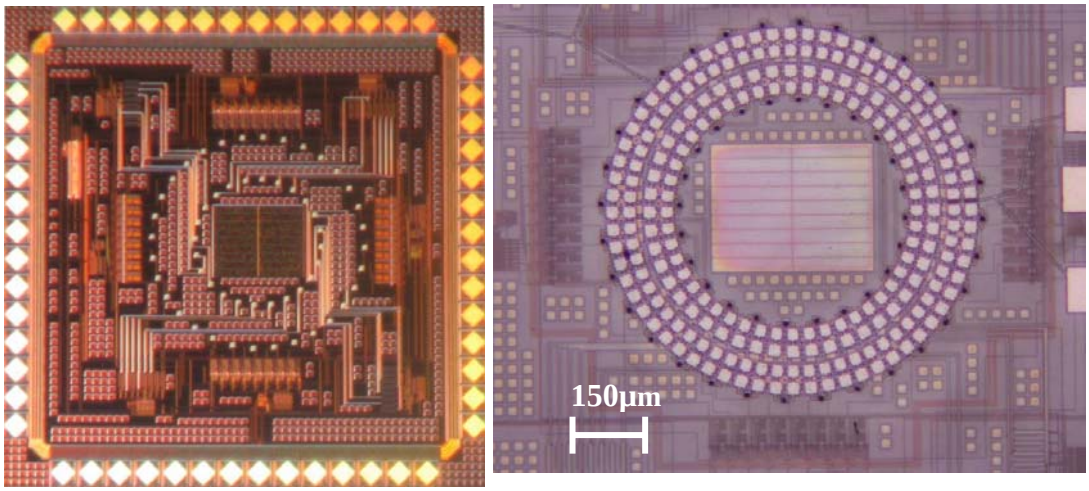


Figure 8. Left: CMOS electronics chip with electronics for 32Rx-24Tx dual-ring CMUT array. Right: The same chip after CMUT-on-CMOS fabrication.

~100%. **This is a clear demonstration of CMUT-on-CMOS technology, which was the main aim of the current project and puts us in a unique position as the first university group demonstrating the monolithic CMUT-on-CMOS transducer technology for these demanding applications. With the proper interconnect technology and real-time imaging electronics, this project can lead to a highly forward-looking IVUS probe for CTO and ICE applications.**

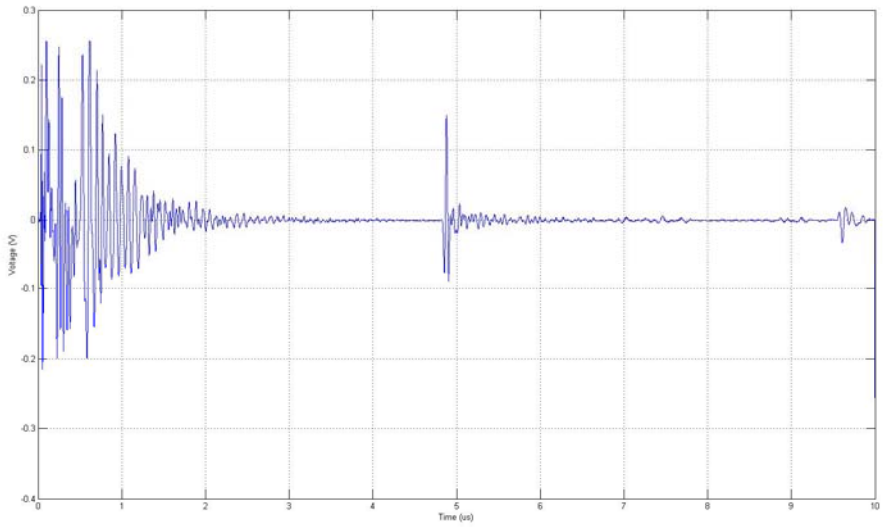


Figure 9. Pulse-echo signal obtained from a single transmit-receive element pair of a CMUT-on-CMOS array for forward-looking IVUS.