QUALITY INSPECTION AND RELIABILITY STUDY OF SOLDER BUMPS IN PACKAGED ELECTRONIC DEVICES: USING LASER ULTRASOUND AND FINITE ELEMENT METHODS

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LIST OF ABBREVIATIONS

ANOVA	Analysis of Variance
ATC	Accelerated Thermal Cycling
BGA	Ball Gird Array
BLM	Bump Limiting Metallurgy
CC	Correlation Coefficient
CCD	Central Composite Design
CCD	Charge-Coupled Device
CSAM	C-Mode Scanning Acoustic Microscopy
CSP	Chip Scale Package
CT	Computed Tomography
CTE	Coefficient of Thermal Expansion
CWT	Continuous Wavelet Transform
C4	Controlled Collapse Chip Connection
DI	De-ionized
DNP	Distance from Neutral Point
DOE	Design of Experiments
DUT	Device under Test

DWT	Discrete Wavelet Transform
ER	Error Ratio
FCLGA	Flip Chip Land Grid Array
FCP	Flip Chip Package
FE	Finite Element
FEA	Finite Element Analysis
FFT	Fast Fourier Transform
FR-4	Flame Resistant-4
GCLAD	Gas-Couples Laser Acoustic Detection
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
IREM	Infrared Emission Microscopy
LDV	Laser Doppler Vibrometer
LGA	Land Grid Array
LTC	Local Temporal Coherence
MCC	Modified Correlation Coefficient
MEMS	Micro-Electro-Mechanical Systems
MLCC	Multi-Layer Ceramic Chip
MLTC	Modified Local Temporal Coherence

NDT	Non-destructive Testing
MSD	Multi-Resolution Signal Decomposition
Nd:YAG	Neodymium-Doped Yttrium Aluminum Garnet
NSMD	Non-Solder Mask Defined
OCT	Oblique Computed Tomography
ppm	Parts per Million
PCB	Printed Circuit Board
PCT	Planer Computed Tomography
PDS	Probability Design System
PGA	Pin Grid Array
PSB	Persistent Slip Band
PWB	Printed Wiring Board
QFP	Quad Flat Pack
RF	Radio Frequency
RMS	Root Mean Square
RSM	Response Surface Methodology
SAM	Scanning Acoustic Microscopy
SAW	Surface Acoustic Wave
SED	Strain Energy Density

SLAM	Scanning Laser Acoustic Microscopy
SMD	Surface Mount Device
SMT	Surface Mount Technology
SNR	Signal to Noise Ratio
STFT	Short-Time Fourier Transform
SOIC	Small Outline Integrated Circuit
SPD	Spectral Power Distribution
SQUID	Superconductive Quantum Interference Device
SSM	Scanning SQUID Microscopy
TSAM	Transmission Scanning Acoustic Microscopy
UBM	Under Bump Metallization
WLP	Wafer Level Package

SUMMARY

Consumer demands are driving the current trend in the microelectronics industry to make electronic products that are miniature, fast, compact, high-density, reliable and low-cost. The transition from traditional through-hole assembly to surface mount assembly is a significant step in the evolution of electronic packaging. The use of surface mount devices (SMDs), such as flip chip packages (FCPs), chip scale packages (CSPs), ball grid arrays (BGAs), and land grid arrays (LGAs) has helped to decrease the size of electronic packages through the use of solder bump interconnections between the devices and the substrates/printed wiring boards (PWBs). Solder bumps act as not only mechanical, but also electrical interconnections between the device and the substrate/PWB.

Common manufacturing defects – such as open, cracked, missing, and misaligned solder bumps – are difficult to detect because solder bumps are hidden between the device and the substrate/PWB after assembly. The packaged electronic devices may be in use for months or years and may experience extensive power and thermal cycling, vibration and other mechanical loading, as well as exposure to hostile environments. The reliability of packaged electronic devices in storage and usage is a major concern in the microelectronics industry. Package constituents can reach critical stress levels during mechanical and thermal processing, testing and usage, causing various failures. This is expected to become more critical in the future devices due to further miniaturization and function integration. Therefore, quality inspection of solder bumps has become a critical process in the microelectronics industry to help reduce cost and ensure product quality and reliability.

Most current techniques available for inspecting solder bumps fall into one of the four categories: 1) electrical testing, 2) X-ray inspection, 3) thermal inspection, and 4) acoustic inspection. While many of these techniques and systems are suitable for specific inspection tasks, they do not necessarily fulfill all the requirements for evaluating the quality of solder bump interconnections in electronic packages. New inspection techniques are urgently needed to fill the gap between available inspection capabilities and industry requirements of noncontact, nondestructive, high-speed, high-resolution, and low-cost inspection systems.

The laser ultrasound-interferometric inspection system under development aims to provide a solution that can overcome some of the limitations of current inspection techniques. The fully developed system will be automated and capable of inspecting solder bumps with multiple defect types – including, but not limited to open, cracked, missing, and misaligned – to meet the inspection requirements from microelectronics manufacturing industry. This research work is based on laser ultrasound and interferometer techniques. A pulsed laser acts as an excitation source to induce ultrasound in the electronic packages in the thermoelastic regime, and the transient out-of-plane displacement response with an ultrasonic arrival is measured by a laser Doppler vibrometer. Solder bump defects can be detected and/or classified by analyzing the transient out-of-plane displacement responses since solder bumps with different qualities cause different responses.

Previous work in this area has shown the potential of using this laser ultrasound-interferometric inspection system to detect solder joint/bump defects in FCPs, CSPs, multilayer ceramic chip (MLCCs) capacitors and other surface mount packages. However, some research issues still need to be addressed before this system can be broadly used to evaluate solder bump quality of different types of electronic packages. The following are the research objectives for

this thesis: 1) develop new signal-processing methods for analyzing the transient out-of-plane displacement signals to improve the measurement accuracy and sensitivity of the inspection system. These include wavelet analysis and local temporal coherence analysis (LTC) methods, which are suitable for processing nonstationary laser ultrasound signals; 2) Develop an integrated analytical, numerical, and experimental modal analyses approach to predict and explain the structural characteristics and the defect effect on the structural characteristics of packaged electronic devices under pulsed laser loading. This integrated approach includes: a) an analytical model based on the Power Balance Law to quickly predict the natural frequencies of a given package structure and to examine how they are influenced by the package geometries and solder bump defects; b) a finite element (FE) model to extract modes and mode shapes of a given package structure with complex and nonlinear geometry/material properties; and c) mode extraction technique from experimental data obtained by using the laser ultrasound-interferometric inspection system. This developed integrated modal analysis approach can also predict mode frequencies and corresponding mode shapes most sensitive to specific defects for further signal processing with wavelet analysis; 3) develop a finite element model to study thermomechanical reliability of packaged electronic devices under thermal loading; investigate fatigue-induced crack initiation and propagation in solder bumps using laser ultrasound-interferometric technique and FE method; and study the correlation between experimental data and FE simulation results; 4) carry out statistical analysis to study package parameter sensitivity and tolerance on solder bump thermomechanical reliability using design of experiments (DOE) and analysis of variance (ANOVA) methods; 5) conduct experiments on a variety of test vehicles with different package formats and defect types to expand the application scope of the laser ultrasound-interferometric inspection system under development. These include flip chip

packages with open solder bumps; flip chip packages with cracked solder bumps due to thermal fatigue, high-density and fine-pitch electronic packages with cracked solder bumps at end-of-line, and over-molded land grid array packages, where board-level solder bump reliability is a concern. Apart from these defects, a batch of flip chip packages ("SiMAF", Siemens AG) with manufacturing defect(s) has been evaluated as well.

Because of the successful completion of the research objectives, the system has been used to evaluate a broad range of solder bump defects in a variety of packaged electronic devices. The development of this system will help tremendously to improve the quality and reliability of electronic packages, and this will save microelectronic and electronic packaging industry millions of dollars per year.

CHAPTER 1

INTRODUCTION

Profound changes in the microelectronics industry driven by Moore's Law, the doubling of transistor density every eighteen or twenty-four months, have led to increasing transistor counts (from 2 thousand to 1 billion), increasing die size, and increasing power density (W/cm^2) by 30 times [Blish R. et al., (2003); Intel®, (2007)]. Consumer demands are driving current trend in the microelectronics industry to make electronic products that are fast, compact, high-density, reliable and low-cost. These trends have driven packaging interconnection density more than six-fold in the last five years [Goyal D., 2007]. The transition from traditional through-hole assembly to surface mount assembly is a significant step in the evolution of electronic packaging. By the late 1990s, surface mount assembly accounted for more than 80 percent of electronics manufacturing [Tummala R., 2001]. Surface mount packages have advantages of size reduction with smaller footprint and cost reduction due to reduced assembly time. Among surface mount packages, FCPs, CSPs, wafer level packages (WLPs), BGAs, and LGAs are widely used in the microelectronics industry.

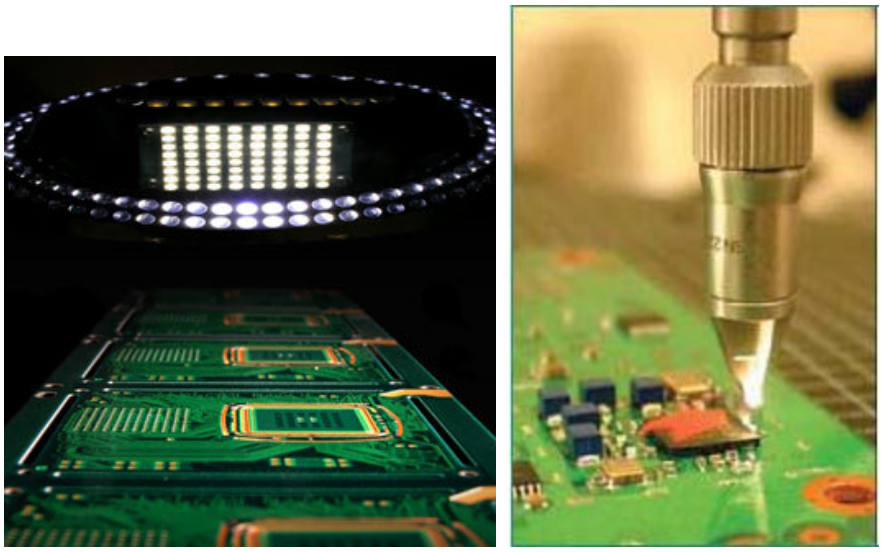
Packaged electronic devices may be in use for months or years and may experience extensive power and thermal cycling, vibration and other mechanical loading, and exposure to hostile environments. The failure of solder joint/bump interconnections is not only dependent on the environmental conditions, but also inherently associated with the manufacturing history [Zhang L., 2005].

Common manufacturing defects, such as open, cracked, missing, and misaligned solder bumps, are difficult to detect because solder bumps are hidden between the devices and the substrates/PWBs after assembly. Therefore, solder bump inspection has been a crucial process in the electronics manufacturing industry to help reduce cost and ensure product quality and reliability. Some techniques have been developed and are commercially available for inspecting solder bumps. Most of them fall into one of the four categories: 1) electrical testing, 2) X-ray inspection, 3) thermal inspection, and 4) acoustic inspection. While many of these techniques and systems are suitable for specific inspection tasks, they do not necessarily encompass all the capabilities required for evaluating the quality of the overall assembly. At the same time, the transition to lead-free packaging due to the environmental requirements has brought a new challenge for microelectronics industry. New inspection techniques are urgently needed to fill the gap between available inspection capabilities and industry requirements for nondestructive, noncontact, low-cost, and fast inspection systems.

1.1 Survey of Nondestructive Solder Joint/Bump Inspection Methods

There have been intensive efforts in automated visual inspection of solder joints/bumps in surface mount packages and several 2-D or 3-D vision systems have been developed by different researchers. The techniques reported in the literature include: (a) a technique for automated inspection of solder bumps by analyzing spatial features and intensity characteristics of image highlights based on high contrast imaging of specular soldered surfaces against a reflective background using dark-field illumination for selective enhancement of surface topography [Ray R., 1989]; (b) an automated

windowing function based on Hough curve detection for solder joint detection and classification in automatic printed wiring board solder joint inspection [Driels M., 1990]; (c) a developed surface shape estimation technique in computer vision technology using structured light with an efficient solution for solder joint inspection [Loh H., 1996]; (d) an application of endoscopy, which has been used to examine internal structure of an organ in medical area, for inspecting solder joint integrity in chip scale packages, including cold joint, misaligned solder joints, and standoff height measurement [Chan Y.C., 2000]; (e) an automatic inspection method for diagnosis of solder joints in integrated circuits mounted with surface mounting technology using a classification algorithm based on a neural network approach [Acciani G., 2007]. Figure 1-1 shows two typical commercialized automated vision inspection systems. However, all vision inspection techniques can only be used for inspecting traditional visible solder joints, or solder bumps still being visible before assembly or a very limited part of solder bumps lying at the edge of the packages after assembly. Therefore, they are not suitable for on-line inspection of solder bumps in current electronic packages through assembly process or failure analysis of solder bumps after assembly process.



(a) (b)

Figure 1-1 3-D solder bump vision inspection systems: (a) wafer inspection system with structured laser-light illumination system [Source: Vision Systems Design] (b) flip chip optical system for critical solder bump inspection at the edge of package [Source: Electronic Manufacturing]

The following sections are a brief survey of the four major categories of nondestructive techniques suitable for on-line inspection of solder bumps in current electronic packages through assembly process and failure analysis of solder bumps after assembly process. Both commercially available inspection systems and inspection methods still at the research stage are reviewed. All these techniques belong to nondestructive testing (NDT), which utilizes various non-invasive measurement techniques, including X-ray and acoustics to determine the integrity of a component, structure, or material without destroying the usefulness of the item.

1.1.1 Electrical Testing

Traditionally, solder joint inspection has been performed via electrical testing. Electrical testing is the process by which an electronic, photonic, MEMS device, or the

complete system in which they are used, is tested to be electrically functional before it is put to end-product use. This is done by applying controlled electrical stimuli to a circuit and comparing its response with an allowed range of expected response [Tummala R., 2001]. Electrical testing consists of two primary methods: functional and in-circuit testing. Functional testing is characterized by exercising the circuit to drive all possible functions performed under all possible environmental conditions, which can verify that the circuit performs the intended functions [Tummala R., 2001]. A functional testing normally can not trace the defect(s) down to a specific component. In-circuit testing (structural testing) is to analyze the circuit from a structural perspective. It is more efficient than functional testing because the circuit can be portioned into simpler sub-circuits that are checked independently from the other sub-circuits [Tummala R., 2001]. One drawback of the electrical testing is that testing pads are required which take up a lot of valuable board space. Electrical testing is also incapable of detecting intermittent defects and the equipment cost is high.

1.1.2 X-ray Inspection

Commercial X-ray solder joint/bump inspection systems have been used for inspecting solder void, solder bridge, insufficient solder volume and various geometrical deviations from the ideal solder bump. There are three types of X-ray inspection methods, including *radiography*, *laminography,* and *tomography* [O'Conchuir D., (1991), Moore T., (2002), Goyal D., (2000, 2003)]. X-ray emission is caused by the sudden deceleration of the electrons as they collide with the target. X-rays have a wavelength of about 100 angstroms. This short wavelength allows them to penetrate most materials. A typical system will have an X-ray source to produce a focused spot of

radiation with a 0.1-0.4 mm diameter beam, an X-ray conversion screen to collect the penetrated radiation, and a video camera to convert the photons on the screen to a digital form and imaging interpretation software [O'Conchuir D., 1991].

Most commercially available 2-D X-ray inspection systems use radiography (shown in Figure 1-2) since it can see through the whole solder joint/bump. This technique has been used for years in both medicine and technology for looking through opaque materials to find the underlying material's structure. The smaller the grain size of X-ray converting screen, the better is the resolution, but the shorter is its life [O'Conchuir D., 1991]. One problem with radiography is that it's very difficult to interpret the images of multilayered or double-sided boards. Another disadvantage is that it is difficult to detect cracks. The cracks must be properly positioned within the joint relative to the radiation to promote sufficient contrast [Martin P., 1999].

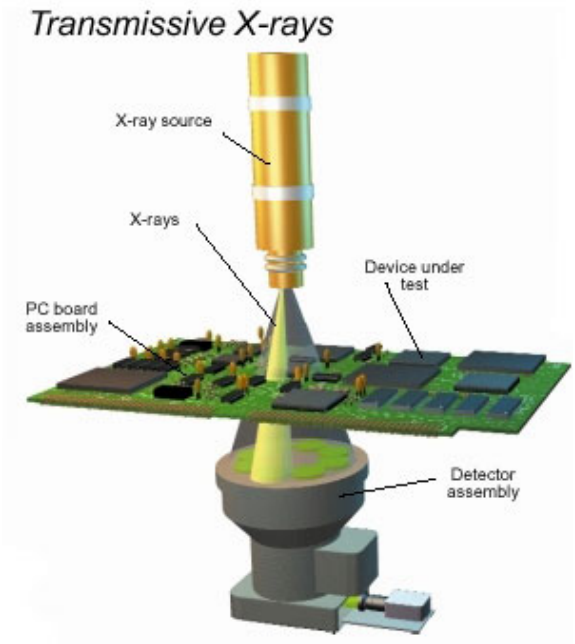


Figure 1-2 X-ray radiography (Source: Machinedesign®)

X-ray laminography circumvents the problem of X-ray radiography by focusing the X-ray beam on one plane at a time and slicing the board horizontally, as shown in Figure 1-3. This is achieved by continuously rotating the source and detector relative to the observation point. X-ray laminography is a natural extension of radiography that can give depth as well as the X-Y position of defects. However, its spatial resolution is limited because it requires high X-ray flux for rapid pass/fail solder bump inspection and the equipment and operation cost of these systems is high [O'Conchuir D., (1991), Teramoto A., (2007)]. It is also considered unsuitable for online application because of its slow inspection speed [Neubauer C., 1994].

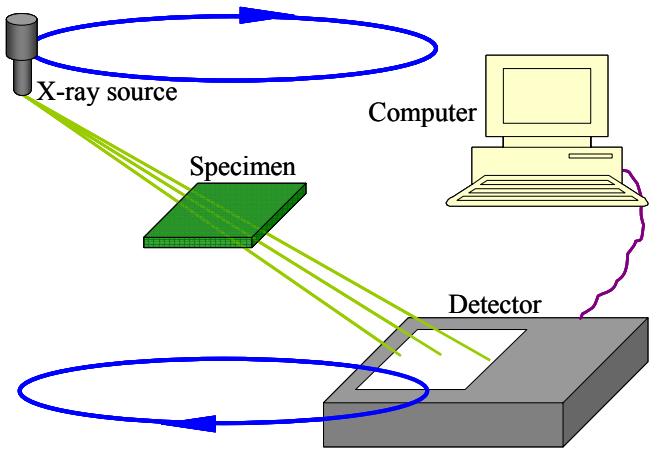


Figure 1-3 X-ray laminography (Source: Zhang L., 2006)

X-ray tomography, as shown in Figure 1-4, reconstructs the 3-D image of the device from a sequence of images taken while the device under test (DUT) rotates between the X-ray source and detector and the detector collects X-ray images of DUT at different tilt angles. By doing this, the analysis is able to perform virtual cross sectioning of the DUT. This inspection technique is effective and can detect almost all solder

joint/bump defects [Goyal D., 2000, 2003]. However, X-ray tomography has the following disadvantages: its data acquisition time is long, it requires post-processing and data interpretation, and its equipment and operation cost is prohibitive.

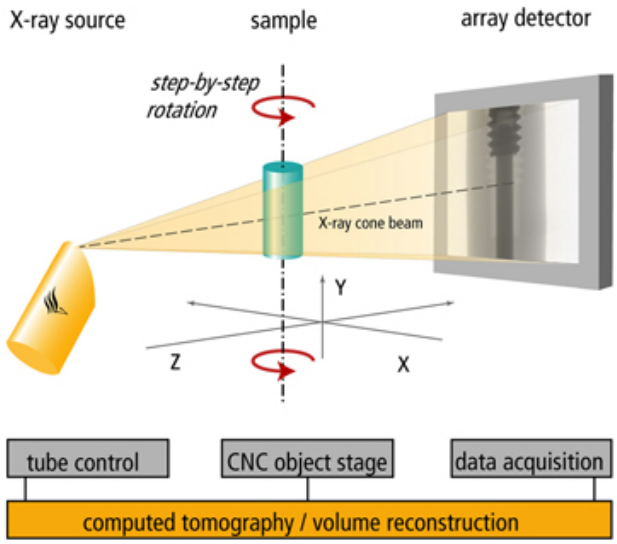


Figure 1-4 X-ray tomography (Source: Phoenix X-ray®)

A new and faster 3D reconstruction technique, called Planer Computed Tomography (PCT), was proposed by researchers at Fraunhofer Institute, German [Neubauer C., 1994]. Compared to conventional axial computer tomography, the lateral planer movements in two dimensions are applied to acquire several views of solder joint and PCT is better suited than the total rotation necessary for classical computed tomography (CT). They concluded that using simulation results to reconstruct solder joint shapes with this technique can be used for online inspection of solder joints.

An imaging method for improving solder bump inspection process by combining the X-ray laminography with a neural network classification method has been proposed

by researchers at Rensselaer Polytechnic Institute [Kalukin A., 1996]. This method has been used to identify different classes of defects in BGA solder bumps.

An automated inspection technique for BGA-mounted substrates and solder bumps by means of oblique computed tomography (OCT) has been proposed by researchers at Nagoya Electronic Works Corporation, Nagoya University and Gifu University [Teramoto A., 2007]. Oblique computed tomography, as shown in Figure 1-5 is a novel imaging technique and the proposed technique consists of position adjustment, bump extraction, character extraction and judgment. OCT obtains the projection images of an object from an oblique direction by rotating the X-ray detector first, and then a 3-D OCT image is obtained with 3-D image reconstruction. Linear discriminated analysis and artificial neural network techniques have been used as determination methods for inspecting solder bumps automatically. The application of this technique for online inspection of BGA solder bumps has been demonstrated by the developers.

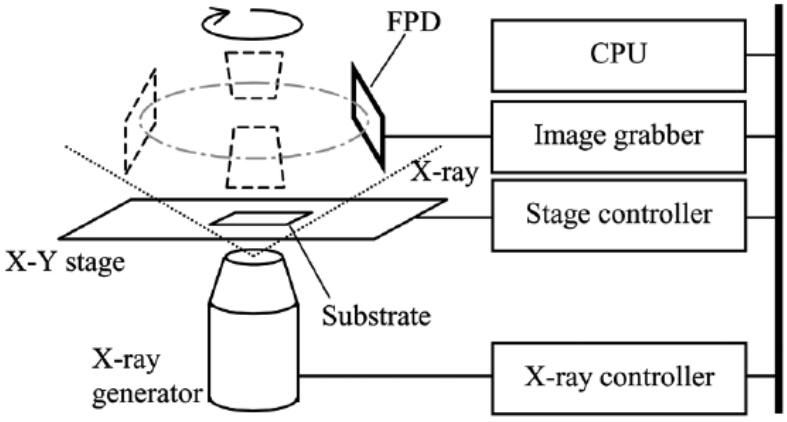


Figure 1-5 Schematic layout of OCT inspection system (Source: Teramoto A., 2007)

1.1.3 Thermal Inspection

Thermal inspection operates on the premise that different materials exhibit unique thermal properties and as a result, absorb and release heat energy differently. Therefore, the heat capacity of a defective solder joint will differ from that of a good joint. Measurement of heat capacity can be done in two ways: thermal imaging and thermal profile inspection [O'Conchuir D., 1991].

In thermal imaging inspection, the entire PCB assembly is exposed to an IR heat source, and then the thermal energy released during cooling is monitored using an IR camera. The recorded video image represents the thermal energy as variations in grayscale data. The images are compared to previously stored images to assess variations, which then can be related to specific defects.

The thermal profile inspection technology is different from thermal imaging in that it takes values for the solder joint's temperature over time instead of an instantaneous thermal map of the whole assembly. The temperature of a solder joint will rise then cool down when exposed to a short laser pulse. This system follows the principle that solder joints will rise in temperature when exposed to short laser pulse and then cool down. The thermal signature of the joint will contain information on the joint's structure [Traub C., 1988]. The typical operation starts with positioning a solder joint under the confocal lens. A continuous-wave Nd:YAG laser then emits a pulse of laser energy at about 12W. The pulse duration ranges from 20 to 100 microseconds. The solder joint's temperature is monitored by a photo-detector sensitive to IR radiation. The thermal signatures are then compared with ideal signatures from previously stored data, and any differences in thermal mass or surface absorption can be related to specific defects. This system can

distinguish bad joints from good ones, but cannot identify the cause of defective solder joints.

Infrared emission microscopy (IREM), which has been used to locate carrier emission and thermal emission sites in integrated circuits (ICs), has been applied by the researchers to wafer and flip chip package inspection [Hsiung S., 2002]. It works on the principle that IREM monitors near-infrared photon emission from the locations on ICs, when they are powered up, and then locates and characterizes defects. It is reported that the anomalies in flip chip solder bumps have been localized with this system.

1.1.4 Acoustic Inspection

Acoustic techniques are widely used in the microelectronics industry for inspecting defects, such as voids, cracks and interfacial delaminations in electronic packages in a non-invasive, fast, and reliable way. The acoustic imaging is generated based on ultrasound waves. The ultrasonic waves are sound waves whose frequencies are above 400 KHz and are used for nondestructive evaluation in many areas. When an ultrasonic wave travels through a medium, its attenuation and propagation speed are dependent on the structure and material properties of the media. Ultrasonic waves are refracted and reflected during propagation. Scanning acoustic microscopy (SAM) uses an ultrasound point source to scan across the sample surface and capture reflections or transmissions of ultrasonic waves. Its working frequencies range from 10 MHz to 2 GHz. C-mode scanning acoustic microscopy (CSAM) is commonly used and it forms images by capturing acoustic reflections from a specific depth region in the packages. Figure 1-6 (a) shows a typical schematic of a CSAM system, in which water acts as a couplant and propagates the acoustic energy from the transducer to the specimen to be tested. When

there is a flaw, it reflects a different echo whose amplitude is proportional to the difference in acoustic impedances between the flaws and surrounding medium. The typical received reflection waveform in time domain is shown in Figure 1-6 (b). Through transmission acoustic microscopy (TSAM) images are absorption of ultrasound as it passes through the package. TSAM is relatively easy to set up, however it provides less spatial resolution than CSAM and it does not provide depth information of the defect. [O'Conchuir D., (1991), Goyal D. et al., (2003)]. TSAM is normally used to verify CSAM results. The two SAM inspection modes discussed above are shown in Figure 1-7 (a) and (b) separately.

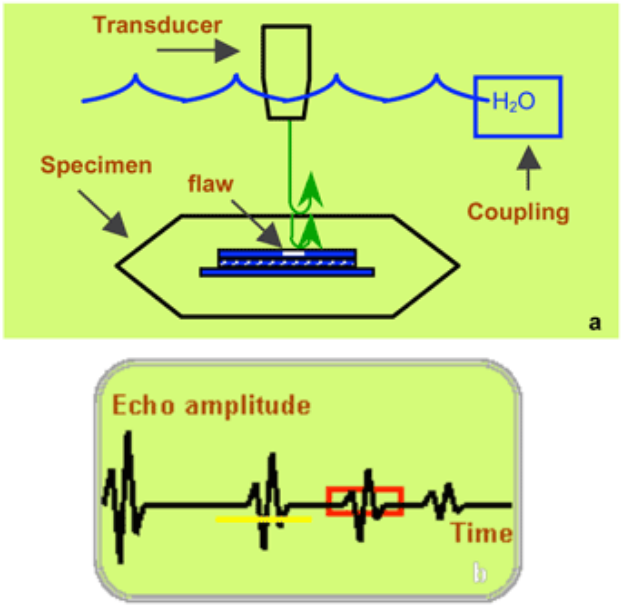


Figure 1-6 Schematic of acoustic microscopy operation principle (Source: Intel® Corporation)

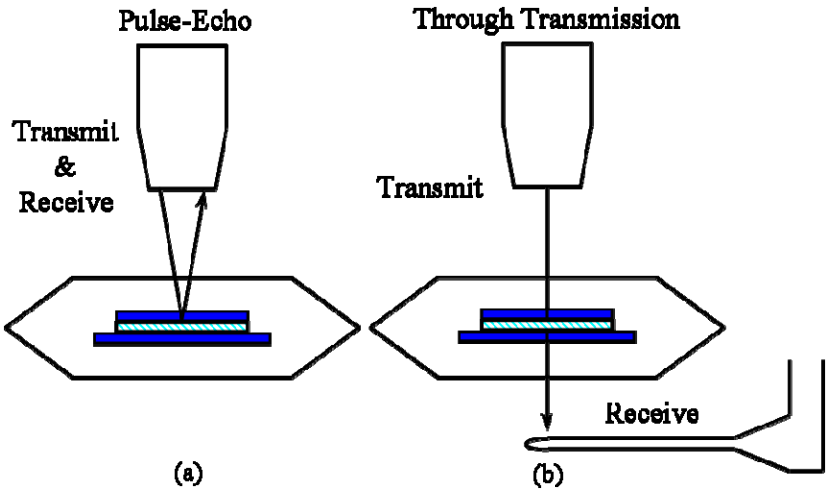


Figure 1-7 Acoustic inspection modes: (a) pulse-echo (reflection) mode (b) through transmission mode (Source: Intel® Corporation)

The limitations of SAM technique are that the length of the pulse prevents focusing the beam on thin layers, and a coupling medium (usually deionized water) is always required to propagate acoustic energy from a piezoelectric transducer to the specimen. SAM has poor resolution when used on thick specimens since the attenuation of high frequency ultrasound which has a high resolution is directly proportional to specimen thickness. This can cause poor resolution due to the decreasing of signal to noise ratio as ultrasound propagates deeper into the specimen, and defects that are located deep beneath the specimen may not be detected. Also the diagonal/vertical defects will not be detected.

Another acoustic technique is scanning laser acoustic microscopy (SLAM) [Embree P.M., 1983], which is an extension of SAM. Comparing to the SAM technique, SLAM detects transmitted ultrasound and measures the disturbances induced by the ultrasound on a polished surface. Laser interferometry is used to capture the output responses in the scanning mode and it decreases processing time. One key drawback of

SLAM is that ultrasound scatters through the multilayer materials like FR-4; therefore SLAM can only be used for inspecting ceramic PCBs.

Besides the four categories of nondestructive inspection techniques introduced previously, advanced magnetic current imaging is another choice for inspecting bump-to-bump shorts. It has been known that it is suited for inspecting circuit defects in buried layers of packages and flip chip mounted dies from both the front and backside of the unit [Pacheco M., 2005]. One sensitive sensor, called superconductive quantum interference device (SQUID) is used in the magnetic imaging technique. For scanning SQUID microscopy (SSM), the sensor is moved in the scanning mode. In the SSM configuration, as shown in Figure 1-8, the SQUID sensor measures the weak magnetic fields produced by energized conductive structure of ICs. A map of the magnetic field, which is correlated with internal circuit structure, is generated when the specimen moves under the SQUID sensor and the complete internal current image is obtained through Biot-Savart law [Pacheco M., 2005]. The advantage of the SSM is that it has high sensitivity and bandwidth, and the disadvantage of relatively modest spatial resolution [Kirtley J. R., 1999].

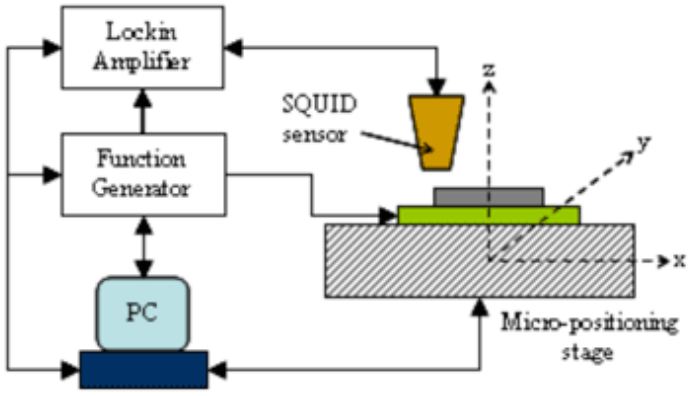


Figure 1-8 Configuration of scanning SQUID microscope (Source: Intel® Corporation)

In summary, although there are several techniques available for inspecting solder joints/bumps of electronic packages, they have their respective disadvantages. With new package formats emerging, it brings up more stringent requirements for a noncontact, nondestructive, high-speed, and low-cost technique for internal solder bump inspection. Therefore, research continues aiming to develop new techniques to satisfy the requirements of microelectronic packaging.

1.2 Laser Ultrasound-Interferometric Inspection System

The overall objective of this research is to develop a noncontact, nondestructive, automated, accurate and low-cost system for evaluating the quality of solder joints/bumps in packaged electronic devices, including flip chip packages, chip scale packages, wafer level packages, ball grid arrays and land grid array packages, etc. This system is expected to be used in-line during assembly process or off-line during process development and failure analysis.

This research is based on laser ultrasound and interferometric techniques (Monchalin J. P., 1989). A pulsed laser acts as an excitation source to induce ultrasound in the thermoelastic regime, and the induced transient out-of-plane displacement with an ultrasonic arrival in nanometer scale on the package surface is measured by a laser Doppler vibrometer. The solder joints/bumps with different qualities cause different responses (Lau J. et al., 1989). Solder bump defects may be detected and/or classified by analyzing the transient out-of-plane displacement responses. Figure 1-9 shows the operating principle of laser ultrasound inspection system from laser-induced ultrasound generation in the packaged electronic devices, to signal acquisition of transient out-of-

plane displacement responses on the package surface with a laser Doppler vibrometer. A typical captured time-domain signal is also shown in Figure 1-9.

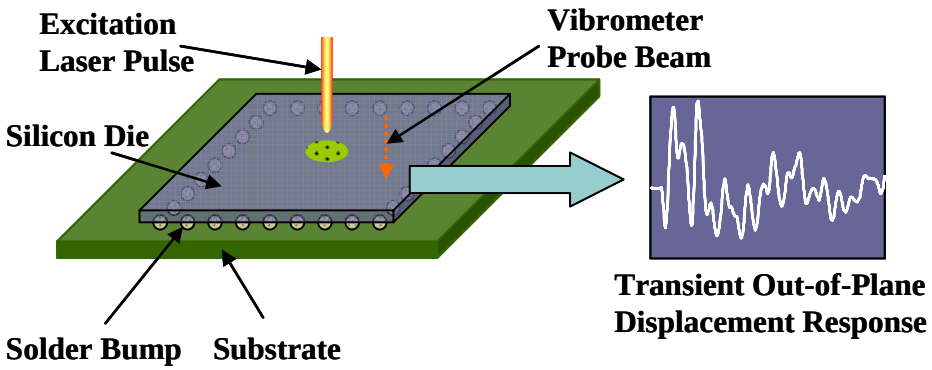


Figure 1-9 Operating principle of laser ultrasound-interferometric inspection system

Previous work in this area has shown the potentials of using this laser ultrasound-interferometric inspection system for detecting solder bump/joint defects in the flip chip packages, chip scale packages, multilayer ceramic capacitors and other surface mount packages. However, there are still some research issues that need to be addressed before the system is ready for industrial use. The work in this thesis includes: 1) new signal-processing methods for analyzing the transient out-of-plane displacement responses to improve inspection accuracy and sensitivity. These include wavelet analysis and local temporal coherence analysis (LTC) methods, which are suitable for processing non-stationary laser ultrasound signals; 2) an integrated analytical, numerical, and experimental modal analyses approach to predict and explain modal behavior and the effect of defects on the structural characteristics of packaged electronic devices under pulsed laser loading. This integrated approach includes: a) an analytical model based on the Power Balance Law to quickly predict natural frequencies of a given package

structure and to examine how they are influenced by the package structure and solder bump defects; b) a finite element model to extract modes and mode shapes of a given package structure; and c) mode extraction technique from experimental data obtained by using the laser ultrasound-interferometric inspection system. This developed integrated modal analyses approach can also predict frequency modes and corresponding mode shapes most sensitive to specific defects for further signal processing with wavelet analysis; 3) a finite element model to study the thermomechanical reliability of packaged electronic devices under thermal loading; investigate fatigue-induced crack initiation and propagation in solder bumps using the laser ultrasound-interferometric technique and FE method; and study the correlation between experimental data and FE simulation results; 4) statistical analysis to study the parameter sensitivity on solder bump thermomechanical reliability using design of experiment and analysis of variance methods, and 5) experiments on a variety of test vehicles with different package formats and defect types to expand the application scope of the laser ultrasound-interferometric inspection system under development.

This dissertation is organized as follows. Chapter 2 provides a review to literature and background for this work, including electronic package technologies, solder bump quality and reliability challenges in the microelectronic packaging, laser ultrasound generation and detection, advanced signal processing, modal analysis technique, design of experiment and analysis of variance methods and solid mechanics for thermomechanical reliability study. Chapter 3 introduces the development of laser ultrasound-interferometric inspection system. Chapter 4 presents signal processing methods, including wavelet analysis and local temporal coherence analysis for

interpreting measurement data and analyzing the relationship between measurement data and solder bump defects to improve measurement accuracy and sensitivity. Chapter 5 presents an integrated analytical, finite element and experimental modal analyses approach. Analytical and finite element models have been developed to study the structural characteristics of electronic packages analytically and numerically. Chapter 6 presents fatigue-induced crack propagation inspection and thermomechanical reliability study of solder bumps in electronic packages including land grid arrays and flip chip packages using laser ultrasound technique and finite element method. A finite element model has been developed to study the thermomechanical reliability of solder bumps in flip chip packages and the correlation between experimental results and finite element simulation has been studied. The parametric sensitivity study and tolerance analysis of package geometric parameters on solder bump lifetime using DOE and ANOVA methods have shown the different effects of package parameter variations on the thermomechanical reliability of electronic packages. Chapter 7 demonstrates the application of laser ultrasound-interferometric inspection system to other advanced electronic packages and thus expands the application scope of the system. Chapter 8 concludes the contribution, impact of this research work, and recommendations for future work.

CHAPTER 2

LITERATURE AND BACKGROUND

A review of the research background and literature survey is presented in this chapter. This review includes electronic packaging technologies, solder bump quality and reliability challenges in microelectronic packaging, laser ultrasound generation and detection, advanced signal processing, modal analysis technique, design of experiments and analysis of variance methods and solid mechanics for thermomechanical reliability study.

2.1 Electronic Packaging

Packages which are mounted and soldered to the surface of the boards rather than inserted into holes are called surface mount packages. The transition from through-hole assembly to surface mount assembly has been a significant step in the evolution of electronic packaging. By the late 1990s, surface mount assembly accounted for more than 80% of electronic manufacturing [Tummala R., 2001]. Surface mount packages have advantages of size reduction with smaller footprints and cost reduction due to reduced assembly time. Among surface mount packages, FCPs, CSPs, WLPs, BGAs, and LGAs are widely used in microelectronics industry. The flip chip (as shown Figure 2-1) is an advanced form of surface mount technology inaugurated by IBM in early 1960s, in which the bare die is flipped over and the active side of the die is then placed down on the substrate or leadframe using small conductive bump made of solder or conductive adhesive. So far, the most common packaging interconnect is solder. Solder bumps act

not only as mechanical connection, but also as electrical interconnection between the die and substrate. In contrast, traditional wire bonding uses face-up chips with a wire connection to each pad.

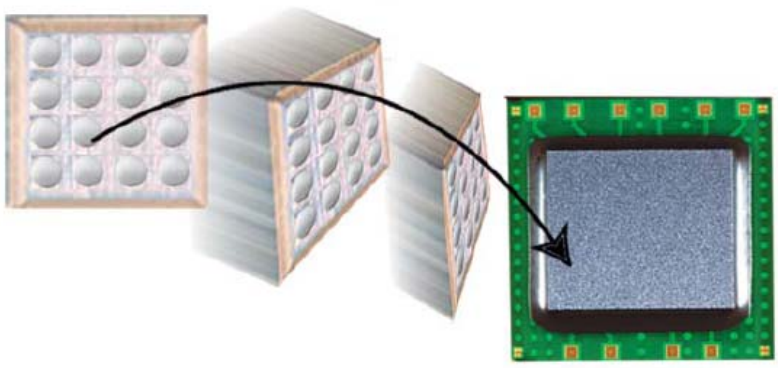
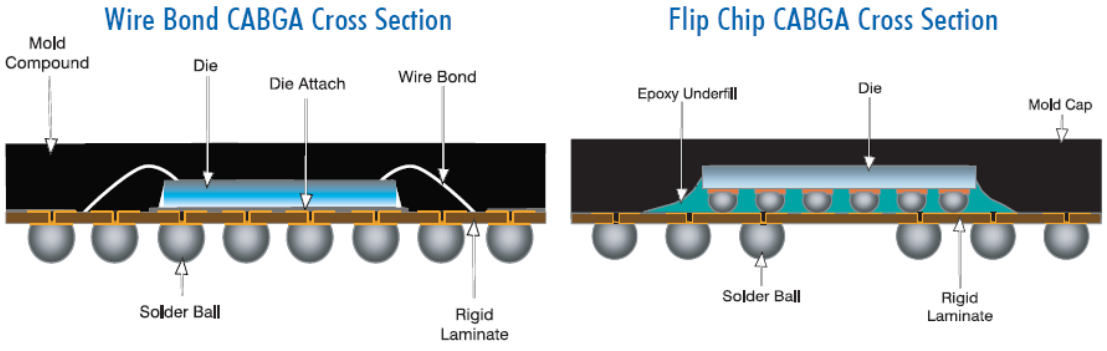


Figure 2-1 Flip chip package (Source: Amkor®)

A solder bump is typically 70-100 μm high, and 100-125 μm in diameter [Amkor, 2005]. Flip chips are also called C4 or controlled collapse chip connection. The flip chip interconnection can be divided into four functional layers: under bump metallization (UBM), chip bump, underfill encapsulant and substrate metallization. The UBM serves as a compatible layer between the bump metallization and final chip metallization. Underfill is a specially engineered epoxy that fills the area between the die and carrier, surrounding the solder bumps. It is designed to counteract the stress in the solder bumps caused by a coefficient of thermal expansion (CTE) mismatch between the die (~2.6 ppm/°C) and carrier (~18 ppm/°C). Once cured, the underfill absorbs the stress, reducing the strain on the solder bumps, and increasing the life of the finished package [Amkor, 2005]. The underfill also resists moisture absorption and provides physical protection for the active face of the chip [Tummala R., 2001]. The substrate metallization connects the solder

bump and pads or traces on the substrate. In 2006-2007, a new solder bumping technology, called Controlled Collapse Chip Connection New Process (C4NP), was developed and implemented by IBM®. C4NP is a new solder transfer technology where molten solder is injected into pre-fabricated and reusable glass templates (molds). A filled mold and wafer are brought into close proximity and solder bumps are transferred onto the entire 300 mm wafer in a single process step without the complexities associated with liquid flux. C4NP addressed the limitation of existing bumping technologies, including solder paste printing, solder sphere attachment, and electroplating by enabling low-cost, fine pitch bumping using a variety of lead-free solder alloys [Laine E., 2006, 2007].

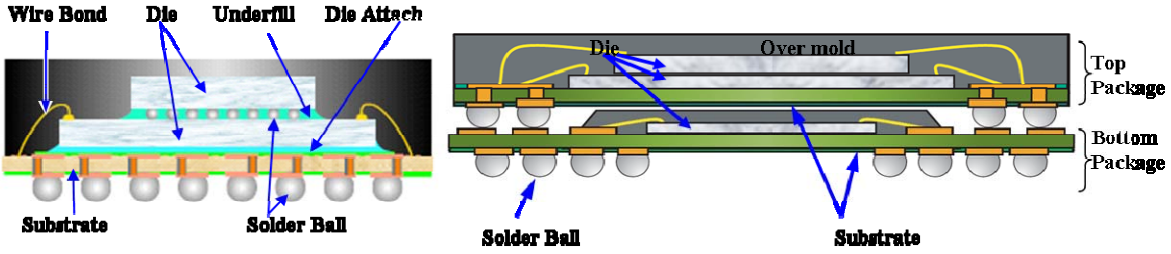
Flip chip technology is also a building block for other electronic packages including but not limited to: ball grid arrays, stacked die package and stacked packages. Many of these packages are based on flip chip technology. For example, Figure 2-2 shows cross-sections of two types of BGA packages. One of them uses the wire-bonding technology; while the other uses flip chip interconnection.



(a) (b)

Figure 2-2 Cross sections of BGAs: (a) wire bond BGA (b) flip chip BGA (Source: Amkor®)

3-D packaging is becoming more popular since 3-D packaging can reduce package size, remove interconnect bottleneck and realize hetero integration at the wafer level. Figure 2-3 (a) and (b) show two typical formats of 3-D packages: stacked die package and stacked package.



(a) (b)

Figure 2-3 3-D packaging: (a) stacked die package (b) stacked package (Source: Amkor®)

Flip chip packages reduce the package size, increase the I/O density, improve the package reliability and reduce the cost of assembly. However, there are also drawbacks for flip chip packages. Flip chip solder bumps are difficult to inspect with many existing inspection systems, and the rework becomes impossible after underfill. Meanwhile, many advanced electronic packages, including BGAs, 3-D packages also use solder bumps to realize the interconnection with the boards. These solder bump interconnections are hidden between the device and substrate/PWB as well. Similarly, they are difficult to inspect with commercially available inspection techniques.

2.2 Solder Bump Quality and Reliability Challenges in Microelectronics Industry

Quality and reliability are key considerations that cannot be overlooked in the development of new packages. Quality is defined to be conformance to set standard of a product on arrival to the customer, and reliability is the probability that a product can perform its intended function for a given time under specified operating conditions [Tummala R., 2001].

The interconnection in electronic packages is normally divided into different levels. The first level connects the silicon die to the package and is widely implemented with C4 type bumps. The second level is the connection between the package and system board, for example board-level solder bump interconnection in ball grid arrays. The current trend in the microelectronics industry is to make products that are compact, miniature, high density, light, and small. Scaling demands are driving the bump size and pitch of electronic packages to the limits of current technologies. As the bump size decreases, the bump becomes less compliant, making it more susceptible to thermal and mechanical failures. Consequently there will always be a great need for quality and reliability assurance of the solder bump interconnections in electronic packages.

Table 2-1 Development trend of chip interconnection pitch [Fjelstad J., 2005]

Year	2001	2002	2003	2004	2005	2006	2007
IC Technology Node (nm)	130	115	100	90	80	70	65
Chip Interconnect Pitch (μm)							
Wire bond- ball	45	35	30	25	20	20	20
Wire bond- wedge	40	35	30	25	20	20	20
TAB	40	40	40	40	30	30	30
Flip chip (area array)							
Cost-performance & High- performance	160	160	150	150	130	130	120
Handheld Low-cost & Harsh environment	150	130	120	110	100	90	80

In a recent study, nearly 253,018 printed circuit board assemblies with 843,171,778 solder joints/bumps were inspected from 566 different board types and different manufacturers [Oresjo S., 2002]. Different component types including BGAs, quad flat packs (QPFs), connectors, chip resistors, and chip capacitors with different sizes and pitches were examined. The study revealed that the average defect level in industry was 1083 ppm (parts per million). The most common defects are opens (48 percent), shorts (23 percent), insufficient solder (15 percent), and missing components (4 percent), as listed in Table 2-2.

Table 2-2 Defect type and percentage of solder joint/bumps [Oresjo S., 2002]

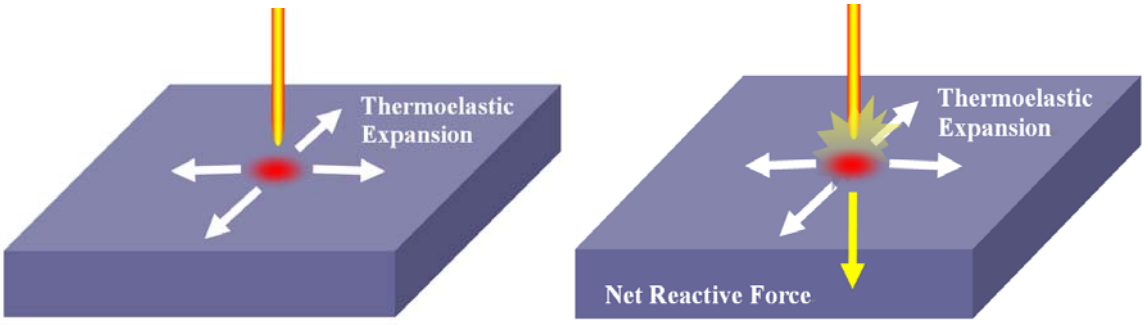
Defect type	Percent of defects
Open joint	48%
Short joint	23%
Insufficient solder	15%
Misaligned joint	4%
Missing joint	4%
Void in joint	2%
Excess solder	2%
Other	2%

For the first-level interconnection, the shift toward reduced k material for the inter-layer dielectric (ILD) in the silicon die brings reliability concerns. These low-k materials challenge the mechanical reliability of first-level solder bump interconnections since they are substantially weaker than previous materials. Meanwhile, the transition from tin-lead to lead-free packaging raises new quality and reliability issues to first-level solder bump interconnections. Higher processing temperatures required for lead-free materials increase thermal stresses, which may cause solder bumps to fail during manufacturing or in service. For the second-level solder bump interconnections, the first reliability challenge arises from greater number of interconnections required to meet the long-term industry trends for greater integration of functions and features in devices. Meanwhile, second-level interconnections have the same reliability challenge as the first-level with the requirement of switch to lead-free solders [Intel®, 2005].

In summary, the reliability of electronic packages in storage and usage is one of the major concerns in microelectronic industry. Critical stress levels can be reached in package constituents during mechanical and thermal processing, testing and usage, causing various forms of failures. It is expected to become more critical in future products due to further miniaturization and function integration, which causes increased power dissipation, higher interconnection density, and higher reliability demands [van Driel, W., 2003].

2.3 Laser Ultrasound Technique

Research at Hull University and Harwell in England during the early 1980s indicated that ultrasound generation by a pulsed laser usually lies between two extreme regimes. The two regimes are: a) thermoelastic regime (damage free but relatively inefficient source for normal incidence waves), and b) ablation regime (intense longitudinal waves generated at the expense of surface damage) [Scruby et al., (1990), Davies et al., (1993)].



(a) (b)

Figure 2-4 Laser ultrasound generation in: (a) thermoelastic regime (b) ablation regime

Laser pulses consist of a train of electromagnetic waves, at the wavelength of the laser cavity, which reaches the surface of the structure to be excited. The high energy and very short duration of each pulse induces a quick increase of the local temperature due to partial absorption of the radiation. If the local temperature rises very rapidly and higher than melting point of the surface materials, local vaporization and ejection of small particles (plasma) will occur, as shown in Figure 2-4 (b). This phenomenon is called ablation and can be used for cutting and cleaning in industrial process. On the other hand, if the laser power is set below the ablation threshold, a thermomechanical effect is produced. As the laser radiation is absorbed in a thin layer near the surface, the internal energy of the layer increases. The heated layer will rapidly expand due to the thermal expansion and a pressure wave can be generated, which can exert a pressure on the adjacent material, as shown in Figure 2-4 (a). The accumulated results can be a compressive wave which travels through the material.

In order to avoid surface damage to the electronic packages in the testing using the laser ultrasound inspection system, the laser power is controlled below the ablation threshold. The strain and stress caused by the local thermal expansion propagate and an ultrasonic wave is generated if the thermal energy is deposited very rapidly.

The optical detection techniques for ultrasound can be classified into non-interferometric and interferometric techniques. Since the amplitude of ultrasound generated in thermoelastic regime lies in micro or even nanometer scale, interferometric techniques are preferred with the ability of providing a high-resolution measurement. These techniques can be classified into three types: 1) optical heterodyning, 2) differential interferometry, and 3) velocity or time-delay interferometry. As far as

sensitivity is concerned, these techniques have almost the same theoretical sensitivity. The choice of a particular technique for a given application is therefore not a matter of sensitivity, but rather its light collection efficiency, immunity to background noise, and the sample surface conditions [Zhang L., 2006].

In this research, a heterodyne Michelson optic fiber interferometer is used for ultrasound detection. The heterodyne interferometer is a two-beam interferometer with a reference beam and an object beam reflected from the object. The two beams to be mixed are of slightly different optical frequencies. Typically, this is obtained by passing a laser beam through an acoustic-optical modulator (Bragg cell) as shown in Figure 2-5. The frequency shifted beam (of frequency Ω + ωB) will be refracted at a different angle and serve as the reference arm. The unaltered beam (of frequency Ω) will be the object beam. Both beams pass through a beam-splitter and are collected by the optical detector. The heterodyne interferometer has a broad detection bandwidth and a good immunity to ambient vibrations. The optic fiber interferometer also adds flexibility to configuring the system [Zhang L., 2006].

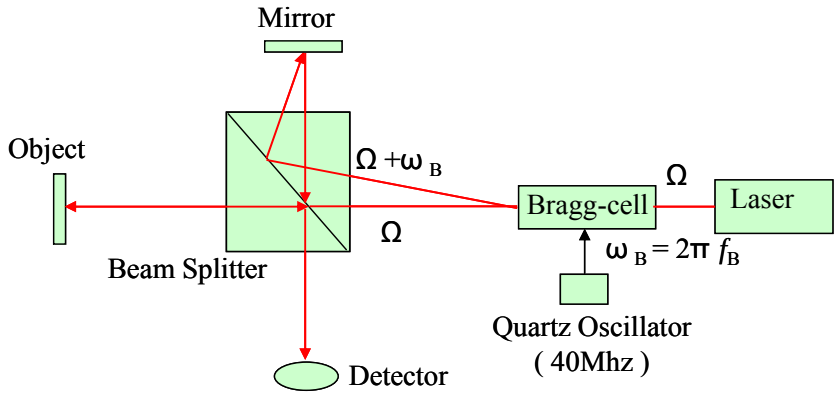


Figure 2-5 Diagram of heterodyne interferometer (Source: Zhang L., 2006)

Laser ultrasound NDE offers some advantages over conventional techniques. First, laser ultrasound is a noncontact technique and can be applied to inspecting samples in inaccessible or hostile environments, or samples with complex geometries. Second, no couplant is required in laser ultrasound inspection so that signal variation due to bonding quality of couplant with the sensor and samples is eliminated. The disadvantage of laser ultrasound is the relatively poor signal to noise ratio mainly due to relative inefficiency of optical detection compared to traditional contact detection methods. Laser ultrasound technique has been widely used in scientific and engineering areas, including characterization of a variety of engineering materials and tissues used in biology or biomedical area, integrity inspection of structures, from large-scale aerospace components to small-scale thin films. A laser ultrasound detection system has been developed for noninvasive imaging of internal structures of soft tissues. The developed detection system (as show in Figure 2-6) has a high sensitivity and is used for detecting small tumors located deeply in human tissues, such as the breast [Hejazi M., 2005]. A scanning laser source and a microcantilever ultrasound receiver have been developed for detecting surface flaws in microdevices using surface acoustic waves (SAWs) [Sohn Y., 2005]. In Sohn's work, the laser ultrasound source was in the near-field of a scatter and the changes in amplitude and frequency content were observed for ultrasound generated by the laser over uniform and defective areas. In order to eliminate signal variation measured in the far-field, the authors developed a contact ultrasound detector to measure near-field ultrasound. Figure 2-7 shows the setup of both near-field scanning laser ultrasound generation and detection for surface crack identification. Caron reports the development progress of a portable laser based ultrasound sensor for interrogating flight-

critical aircraft wings [Caron J., 2005]. In his work, a gas-coupled laser acoustic detection (GCLAD), which works as an alternative to interferometric detection, has been developed to intercept ultrasound signals after they have been transmitted to air and works independently of the optical properties of the sample surface. The arrangement of this inspection system with GCLAD is shown in Figure 2-8.

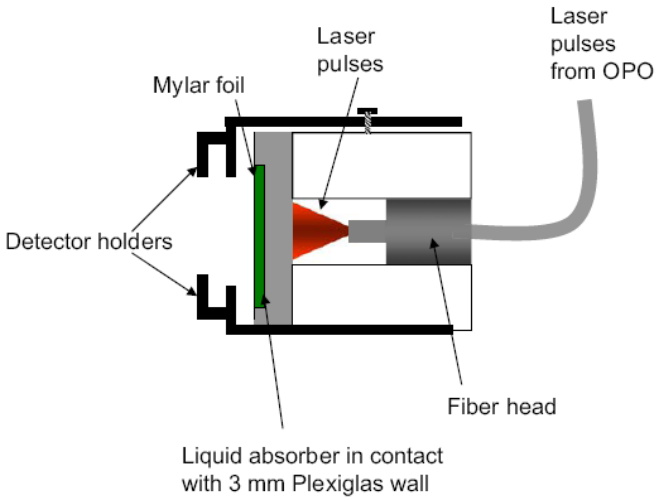


Figure 2-6 Schematic of experimental sensor head in laser ultrasound inspection system

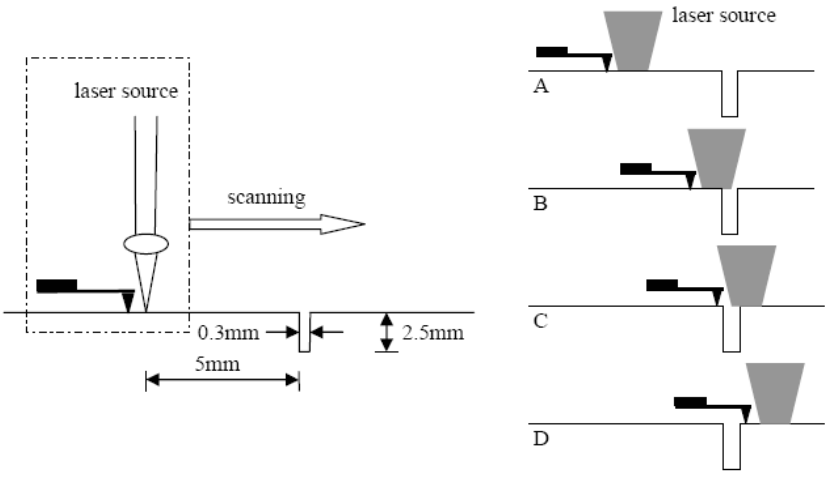


Figure 2-7 Setup of both near-field scanning laser ultrasound generation and detection

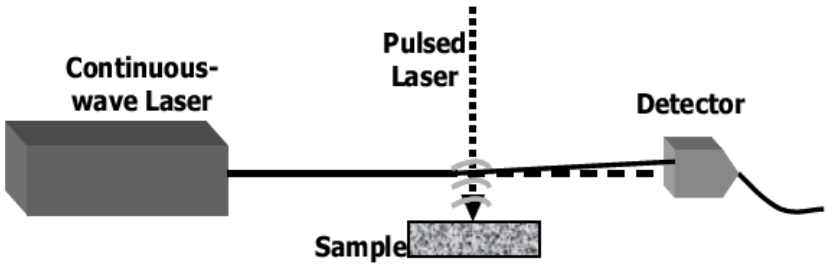


Figure 2-8 Arrangement of inspection system with GCLAD

2.4 Digital Signal Processing

Digital signal processing plays an important role in the development of the laser ultrasound-interferometric inspection system. The principle underlying how this system evaluates the package quality is quantification of the differences in transient out-of-plane displacement responses between the packages to be tested and a known-good-package. However, the transient out-of-plane displacement responses captured by the interferometer have a relatively small magnitude in nanometer scale and are buried in white noise from the testing environment. In order to precondition, de-noise, and extract useful information from the raw signals, a number of signal-processing methods, both in the time and frequency domains, have been implemented by Liu or Zhang. Liu used error ratio (ER) to compare signals directly in the time domain [Liu et al., 2003]. This method integrates the squared error between the measured and reference signals and then normalizes this integrated value by the total energy of the reference signal, as represented by Equation 2-1,

$$ER = \frac{\int [f(t) - r(t)]^2 dt}{\int [r(t)]^2 dt} \tag{2-1}$$

Where, $f(t)$ is the measured signal and $r(t)$ is the reference signal.

The ER value appeared to be a relatively sensitive indicator of the existence of solder joint/bump defects in certain cases [Liu et al., 2003]. Liu also used periodogram averaging to analyze the signal power density distribution in the frequency domain. A frequency shift between the signals measured from a defective package and a good package was observed as well. However there are some limitations to ER method. The scale of ER method depends on the device being tested and should only be used for the relative comparison between similar product types. ER is also largely dependent on the laser power. Alternatively, Zhang proposed correlation coefficient (CC) method to analyze the time domain signals in a statistical way, shown in Equation 2-2 [Zhang L., 2004]. The r is a normalized measure of the strength of the linear relationship between signals, with the scalar value lying between -1 and 1. The CC method appeared to show some successes in detecting missing, misaligned, and cracked solder bumps in FCPs and CSPs [Zhang L. et al., 2005].

$$r = \frac{\sum_n (R_n - \overline{R})(A_n - \overline{A})}{\sqrt{(\sum_n (R_n - \overline{R})^2)(\sum_n (A_n - \overline{A})^2)}} \tag{2-2}$$

Where,

R_n: the reference signal,

$\overline{R}$: the mean of R_n,

A_n : the measured signal,

$\overline{A}$: the mean of A_n.

In order to make the CC method compatible with the ER method, a modified correlation coefficient (MCC) was used, defined as $1 - r$.

In another work, several signal processing techniques have been developed to detect surface-breaking cracks by analyzing surface acoustic waves [Park et al., 2007]. Facing the variation of the peak-to-peak value in the time domain and the spectrum distribution in the frequency domain according to the crack depth, a normalized peak frequency variation and the attenuation of high-frequency part of a normalized transfer function spectrum with a half-period window is used for processing laser ultrasound signals. The experimental results showed that the attenuation of the high-frequency part of the spectral signals in the frequency domain provide better information about the crack depth than the amplitude variation of the ultrasonic signals in the time domain.

2.5 Modal Analysis of Electronic Packages

There are certain frequency modes and corresponding mode shapes for any given structure, including electronic packages. Each electronic package and its solder bump interconnections can be modeled as a plate with spring supports and a damping element. The short duration of the laser pulse induces a rapid increase in the local temperature on the package surface. This is followed by a consecutive temperature decrease caused by heat transfer in the material. A local thermomechanical expansion is induced, with

consequent out-of-plane displacement on the package surface when the energy level of laser pulses is controlled below the ablation threshold in order to avoid surface damage. The overall displacement response will be close to the impulse response of the system. In this research work, modal analysis is important to correlate the defects with the dynamic responses of electronic packages under pulsed laser loading.

Intense efforts in numerical analysis and experimental studies of vibration-induced solder joint/bump failures have been reported in the literature. However, the literature available on how defects affect the dynamic responses and structural characteristics of electronic packages is very limited. Early work on solder joint inspection using modal analysis technique dates back to 1989 by Lau [Lau J., 1989]. In his work, modal analysis technique has been shown as a potential for inspecting solder joint defects in surface mount devices though the reported detectable defect was only unsoldered leads in early simple surface mount devices. Vibration frequencies and corresponding mode shapes of soldered and unsoldered leads of surface mount devices, including the small outline integrated circuit (SOIC), plastic leaded chip carrier, and plastic quad flat pack were derived from both analytical and finite element methods. A laser Doppler vibrometer (LDV) method was developed by the authors to measure frequencies of leads and solder joints for spectral analysis. Experimental results showed difference in the vibration spectra between bad and good joints (unmounted leads) and it was concluded by the authors that this spectra technique can be used as an inspection criteria to detect unsoldered leads.

This research requires understanding the structural characteristics of electronic packages in correlating the defects with dynamic responses of electronic packages under

pulsed laser loading. This involves experimentally measuring the transient out-of-plane displacement responses and correlating experimental results with the analytical and numerical models. The analytical model can help to quickly identify the structural characteristics and it is computationally less expensive than the numerical model using FE method. Suhir has developed analytical models to predict dynamic responses of portable electronic products [Suhir E., 1994]. However, a simplified two degree-of-freedom model developed in his work can not capture the full structural characteristics of a complicated system with multi degree-of-freedom. Bake and Perkins developed analytical models of vibration-induced failures in surface mount components and applied them to the drop reliability analyses of CSPs or ceramic column grid array packages separately [Bake D.B., (1993), Perkins A., (2004)]. Lee has developed an analytical model for system identification of partially restrained composite plates [Lee C.R., 2006].

The numerical model using FE method is capable of representing the complex geometry, material properties, and boundary conditions of electronic packages more accurately than analytical models. In the present context, FE modal analysis of electronic packages has several uses, one of which is to explain the results obtained from experimental modal analysis. For example, the structural characteristics of electronic packages can help to predict the modes and mode shapes most sensitive to certain defects. This would enable one to be reasonably certain that the modes most sensitive to defects are strongly excited, and therefore give high signal-to-noise ratios, which can enhance measurement accuracy and sensitivity. Therefore, FE modal analysis can provide a valuable direction for further signal processing of laser ultrasound signals for defect detection. Another use of FE modal analysis is to enable one to carry out a parametric

study on a wide variety of package formats without fabricating actual products. Zhu, Luan and Pitarresi have done numerical modeling and experiments to characterize the natural frequencies, mode shapes and system responses at both board and product levels [Zhu L., (2005), Luan J., (2005), Pitarresi J., (2002)]. Meanwhile, the laser excitation technique is also used for experimental modal analysis of other structures with various sizes by Castellini [Castellini P., 2004].

This research uses a pulsed laser for the experimental modal analysis of electronic packages. The power spectrum of laser ultrasound signals can be extracted from a Fast Fourier Transform (FFT) of measured responses. The transient out-of-plane displacement responses measured by the interferometer come mainly from the transverse motion (surface acoustic waves), and only the modes and corresponding mode shapes in the direction perpendicular to the package surface are extracted.

2.6 Design of Experiments and Analysis of Variance

2.6.1 Analysis of Variance

Design of experiments (DOE) is defined as a structured, organized method for determining the relationship between factors affecting a process and the output of the process or refers to experimental methods used to quantify indeterminate measurements of factors and interactions between factors statistically through observance of forced changes made methodically as directed by mathematically systematic tables [sixsigma, 2008]. In the experiment, a factor is a variable that is studied. In order to study the effect of a factor on the response, two or more values of the factor are used. These values are referred to as levels or settings of a factor. A treatment is a combination of factor levels in

the experiment. Analysis of variance (ANOVA) is defined as a collection of statistical models, and their associated procedures, in which the observed variance is partitioned into components due to different explanatory variables [wikipedia, 2008]. In simple problems, ANOVA computations can be performed using linear regression model as shown in Equation 2-3.

The general linear model between the response y and the input variables x_i is expressed as,

$$y = \beta_0 + \sum_{i=1}^{k} \beta_i x_i + \varepsilon \tag{2-3}$$

Where, ε is assumed to have mean zero and variance σ^2, i.e., $\varepsilon \sim N(0, \sigma^2)$.

The matrix form of general linear model is expressed as,

$$y = X\beta + \varepsilon \tag{2-4}$$

If n observations are collected in an experiment, then $y = (y_1, y_2, ..., y_n)^T$ is the $n \times 1$ vector of responses, $\beta = (\beta_0, \beta_1 ..., \beta_k)^T$ is the $(k+1) \times 1$ vector of regression coefficients, and X is the $n \times (k+1)$ model matrix.

The least square estimate of β when $(y - X\beta)^T (y - X\beta)$ is minimized is given as,

$$\hat{\beta} = (X^T X)^{-1} X^T y \tag{2-5}$$

None of the input variables (factors) has explanatory power if the null hypothesis H_0 holds, i.e., $H_0: \beta_1 = \beta_2 = \cdots \beta_k = 0$. Table 2-3 gives the ANOVA table for the above general linear model.

Table 2-3 ANOVA table for general linear model [Wu J., 2000]

Source	Degrees of freedom	Sum of squares	Mean squares
Regression	k	$\hat{\beta}^T X^T X \hat{\beta} - N\overline{y}^2$	$(\hat{\beta}^T X^T X \hat{\beta} - N\overline{y}^2)/k$
Residual	$n-k-1$	$(y - X\hat{\beta})^T (y - X\hat{\beta})$	$(y - X\hat{\beta})^T (y - X\hat{\beta})/(N-p-1)$
Total	$n-1$	$y^T y - N\overline{y}^2$	

In order to test the above null hypothesis $H_0: \beta_1 = \beta_2 = \cdots \beta_k = 0$ against the alternative hypothesis $H_1: \beta_i \neq 0$, t-test is used to calculate the test statistic t. The higher the value of t, the more significant is the corresponding coefficient β_i. Alternatively, P-value approach has been adopted in practice. The P-value is the probability that the test statistic will take on a value that is at least as extreme as the observed value of the statistic when the null hypothesis H_0 is true. The smaller the P-value, the stronger is the evidence that the null hypothesis does not hold.

2.6.2 Monte Carlo Simulation and Response Surface Methodology

The Monte Carlo Simulation, whose term was coined in the 1940s, is a class of computational algorithms that rely on repeated random sampling to compute their results. Monte Carlo Simulation provides a way to simulate how virtual components behave the

way they are built in reality. It is a common, traditional method for probability analysis of a system.

Response surface methodology, which was proposed by Box and Wilson, is a collection of statistical and mathematical techniques useful for developing, improving, and optimizing processes, in which a response of interest is influenced by several variables [Myers R., 2000]. Comparing to traditional Monte Carlo Simulation, RSM often needs fewer simulation loops and has the advantage of reducing processing time.

In RSM, the relationship between the output response *y* and the input factors $X_1, X_2, ..., X_k$ is modeled by,

$$y = f(X_1, X_2, ..., X_k) + \varepsilon \tag{2-6}$$

Where, the form of the true response function f is unknown and ε is an error term that represents the sources of variability not captured by f. ε is assumed to have mean zero and variance σ^2.

The input variables are normally converted to coded variables $x_1, x_2, ...x_k$, which are dimensionless and have mean zero and the same standard deviation,

$$x_i = \frac{X_i - \overline{X}}{S} \tag{2-7}$$

Where, $\overline{X}$ is the mean, and S is the standard deviation.

Then the response y is expressed as input factors that are in the coded form as $y = f(x_1, x_2, ..., x_k) + \varepsilon$ and is called response surface.

If the response is modeled by a linear function of the independent input variables, then the approximating function is a first-order model,

$$y = \beta_0 + \sum_{i=1}^{k} \beta_i x_i + \varepsilon \tag{2-8}$$

Where, β_i represents the slope or linear effect of the coded variable x_i.

A design or experiment that allows the coefficients to be estimated in the linear model is called a first-order design or first-order experiment.

If there is a curvature in the system, the response surface should be approximated by a second-order model,

$$y = \beta_0 + \sum_{i=1}^{k} \beta_i x_i + \sum_{i<j}^{k} \beta_{ij} x_i x_j + \sum_{i=1}^{k} \beta_{ii} x_i^{\,2} + \varepsilon \tag{2-9}$$

Where,

β_i : linear effect of x_i,

β_{ij} : bilinear interaction coefficient between x_i and x_j,

β_{ii} : quadratic effect of x_i.

Central composite design (CCD) is the most commonly used second-order design in response surface study. Suppose k coded input variables denoted by $x = (x_1, x_2, ..., x_k)$,

a central composite design consists of the following parts [Box and Wilson, 1951], as shown in Figure 2-9,

(1) n_f corner points with $x_i = -1, 1$ for $i = 1,...,k$,

(2) n_c center points with $x_i = 0$ for $i = 1,...,k$,

(3) $2k$ axial points of the for $(0,...x_i,...,0)$ with $x_i = -\alpha, \alpha$ for $i = 1,...,k$.

Where, α is the distance of axial points from the center point and it depends on the number of experimental runs in the factorial portion of CCD.

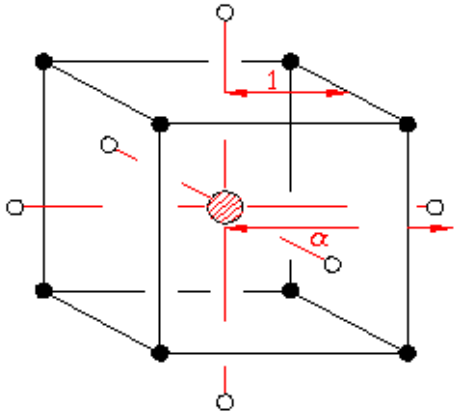


Figure 2-9 Schematic of a central composite design for three factors (black circles: corner points, white circles: axial points, shaded large circle: center point) [Source: U.S. DOT]

2.7 Mechanics Based Reliability Study of Solder Bumps in Electronic Packages

Under cyclic thermal loading, solder bumps are subjected to stresses due to a coefficient of thermal expansion mismatch between package constitutions. Because of the constraints of thermal expansion, excessive strains/stresses might be induced and might eventually initiate and propagate fatigue cracks in solder bumps [Darveaux R., (2002),

Lau J., (1997)]. There have been intensive efforts in the prediction of solder bump reliability under low cycle fatigue loading and several types of thermal fatigue models for predicting solder bump reliability in electronic packages have been proposed.

In strain based failure criteria, thermal fatigue failure is associated with the cyclic inelastic strains of solder bumps. Among strain based models, the most popular is Coffin-Manson empirical model (the fatigue-life relationship is shown in Equation 2-10) [Yan W., 2006], which is based on the calculation of cyclic shear strain range,

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon'_f}\right)^{1/c} \tag{2-10}$$

Where,

N_f : mean cycles to failure,

ε'_f : fatigue ductility coefficient, $\varepsilon'_f = 0.325$ for eutectic solder,

c : fatigue ductility exponent, $c = -0.7 \sim -0.5$,

$\Delta\gamma$: cyclic shear strain range.

From the Coffin-Manson model, it is easy to derive the simplified relationship between solder bump life and solder bump standoff, CTE mismatch between silicon die and substrate in flip chip packages before underfilling (assuming $\varepsilon'_f = 0.325$ and $c = -0.5$),

$$N_f = \frac{1}{2}\left(\frac{0.65h}{L_{DNP}(CTE_{sub} - CTE_{die})\cdot\Delta T}\right)^2 \tag{2-11}$$

Where,

h : solder bump standoff,

L_{DNP} : distance of solder bump from neutral point,

ΔT : temperature change the packages experience.

It is clearly seen that solder bump life will be increased by increasing solder bump standoff. It is an important conclusion and a more accurate relationship between lifetime and standoff of solder bumps will be shown in thermomechanical reliability study of solder bumps with finite element method in Chapter 6.

Another important strain based fatigue model of solder bumps was proposed by Solomon [Solomon H., 1986]. This model, which is shown in Equation 2-12, is based on plastic strain range instead of shear strain range used in Coffin-Manson model,

$$N_f = \theta(\Delta\gamma_p)^{\varphi} \tag{2-12}$$

Where,

N_f : mean cycles to failure,

$\Delta\gamma_p$: cyclic plastic strain range,

$\theta = 1.292$: for eutectic solder,

$\varphi = -1.96$: for eutectic solder.

The inherent drawback of strain based life prediction models is that they fail to account for loading path or loading time effect on solder bump reliability [Sarihan V., 1993]. Damage accumulation based models have been proposed and they are classified

into two classes: fracture mechanics based approach and energy based approach. In the fracture mechanics based approach, a finite crack is always assumed to exist initially and the damage is related with crack growth [Sarihan V., 1993]. In the energy based approach, no crack is assumed and the energy is accumulated to cause failures in the course of cyclic loading.

In the energy based approaches, Zahn's and Darveaux's models are two popular ones.

In Zahn's model, the life prediction uses a power law fit as shown in Equation 2-13,

$$N = C_1(\Delta W_{avg})^{C_2} \tag{2-13}$$

Where,

N : cycles to failure,

ΔW_{avg} : plastic strain energy density accumulated per cycle,

C_1, C_2 : coefficients.

In Darveaux's model, the crack growth data are fit to relations with calculated strain energy density in the following form,

Crack initiation: $N_0 = K_1 \Delta W_{avg}^{K_2}$

Crack growth rate: $\frac{d\alpha}{dN} = K_3 \Delta W_{avg}^{K_4}$

Characteristic life: $N = N_0 + \frac{\alpha}{d\alpha / dN}$ (2-14)

Where,

α : smallest characteristic dimension of the cross-section of solder bump,

ΔW_{avg} : plastic strain energy density accumulated per cycle,

K_1, K_2, K_3, K_4 : crack correlation constants.

The intensive studies, including inelastic strain based, fracture damage based, or energy based approaches discussed previously are empirical in nature and have not addressed the size effect and microstructure difference between bulk specimens and actual solder bumps used in miniature electronic packages. Solder is a polycrystalline material, and a solder structure is an aggregation of crystallites. These crystallites have different crystallographic orientations. Meanwhile, solder materials such as SnPb (tin-lead materials), SnAgCu or SnAg (lead-free materials) and others have a high homologous temperature and operate at a high temperature range. Micromechanics research has shown that the representative volume, which the empirical fatigue formula can apply to, is larger than that of current solder joints. Bulk solder specimens can be viewed as statistically homogeneous and isotropic; however, solder bump may have to be viewed as anisotropic. Therefore, micromechanics based fatigue theory might be desired to study microstructure characteristics of solders without size limitation [Wen S., 2002, 2005].

A dislocation model was proposed by Huang to study shear fatigue damage of solder bumps under thermal cycling [Huang J. et al., 1992]. In his work, the fatigue damage of metals results from plastic deformation, while the plastic deformation in turn

is caused by the slip of dislocations in the metal crystal. Accordingly, the crack initiation and propagation in the course of fatigue can be treated as continuous course in which the dislocation continuously gathers to a certain place to make the crack form and grow [Huang J. et al., 1992].

The failure of solder bumps under thermal cycling results from cyclic plastic shear strain caused by the CTE mismatch in the thermal cycle (D_s), and the damage from the creep in the dwell time of thermal cycle (D_c). Since the plastic deformation of metals is supposed to be caused by the slip of dislocation in the metal crystal, it is understood that the plastic shear strain of solder bumps under thermal cycling results from the slip of the dislocations in Sn-Pb alloys. The creep in Sn-Pb alloys at a high temperature involves intercrystalline sliding, grain or phase boundary sliding and localized grain coursing. However, the creep strain is mainly caused by intercrystalline sliding and grain or phase boundary sliding. In addition, the grain or phase boundary sliding could also be considered to be caused by the slip of dislocations [Huang J. et al., 1992]. Therefore, the damage from the cyclic plastic strain and creep in the dwell time can be expressed as,

$$(D_s + D_c)_i - (D_s + D_c)_{i-1} = K_w \Delta W_p \tag{2-15}$$

Where, i is the cycle index of the thermal cycling, and ΔW_p is the plastic strain work, i.e., the plastic work absorbed by unit volume of Sn-Pb solder in one cycle.

It is clearly seen that the failure damage is correlated with the plastic strain work accumulated per cycle, which constructs the basis of FE based reliability analysis of solder in Chapter 6.

Suppose the plastic stress-strain relation of a material is $\sigma = K\varepsilon_p$, and there is no creep damage, the final relationship between lifetime and plastic strain range of solders is derived after simplification [Huang J. et al., 1992],

$$N_f^{\alpha} \cdot \Delta\varepsilon_p = C \text{ with } \alpha = \frac{1}{n+1} \text{ and } C = \left(\frac{n+1}{2KK_w} \right)^{\frac{1}{n+1}} \tag{2-16}$$

It is seen that Equation 2-16 falls into the format of famous Manson-Coffin equation as shown in Equation 2-10.

In the work done by Wen, a fatigue theory based on dislocation and percolation damage mechanics has been developed to predict fatigue behavior of solder materials used in the electronic packages [Wen S., 2002, 2005]. The theory begins with fatigue behavior of an individual grain, which is caused by microcracking within its persistent slip bands (PSB). The PSBs are formed by motion of slip planes, and the motions can occur only in particular directions, where such motion is related to the magnitude of local resolved shear stress on the slip plane. Therefore, the resolved shear stress is the key parameter to characterize the fatigue behavior of an individual grain. When ductile materials are subjected to cyclic loading, dislocations appear and are followed by PSB formation within grains. Extrusions and intrusions appear in the form of striation as the PSB strike the free surface. In Mura's model [Mura T., 1990, 1994, 1996], PSB formation results from dislocation density increment in two adjacent but reversely gliding

layers during the cyclic loading. At the same time, change of Gibb's free energy increases as the dislocation energy increases because of dislocation increment. At a certain point, the Gibb's free energy change reaches a maximum and microcracking occurs within the PSB. This cycle number is defined as the fatigue point. The Mura's model is able to produce the fatigue S-N curve and capture the grain size effect and to incorporate material properties such as surface energy density, and critical friction stresses.

The number of cycles at which a microcrack initiates within PSB or on the grain facets is calculated by the simplified equation,

$$n_{cr}\left(\frac{\Delta\tau}{\tau}\right)^3 \approx \frac{(2-\nu)\pi(\gamma-\gamma_d)E^2}{32(1-\nu^2)^2\bar{d}\,\tau_y{}^3} \tag{2-17}$$

Where,

n_{cr}: number of cycles at which a microcrack initiates,

γ: free surface energy,

γ_d: dislocation energy density,

$\bar{d}$: grain size,

$\Delta\tau$: local resolved shear stress,

τ_f: critical friction stress,

τ_y: shear strength,

E: Young's modulus of solder,

ν: Poisson ratio of solder.

It is clearly shown in Equation 2-17 that the dislocation density γ_d, gain size $\bar{d}$, and the local resolved shear stress $\Delta\tau$ within the cracking plane strongly influence number of cycles at which a microcrack initiates n_{cr}.

CHAPTER 3

LASER ULTRASOUND AND INTERFEROMETRIC INSPECTION SYSTEM

3.1 Laser Ultrasound and Interferometric Inspection System

The laser ultrasound-interferometric inspection system, whose setup is shown in Figure 3-1, has been developed for this work. The system consists of (a) a pulsed neodymium-doped yttrium aluminum garnet (Nd:YAG) laser to generate the laser pulses, (b) a fiber optic beam delivery system to transmit laser pulses onto the package surface, (c) a laser Doppler vibrometer which captures the transient out-of-plane displacement responses with an ultrasonic arrival on the package surface, (d) an automated X-Y positioning table to position the packages to be tested, (e) a manual stage sitting on the automated positioning stage to adjust the position of the laser excitation spot on the package surface, (f) a vision system to position the packages by capturing the fiducials on the PWBs, and (g) a PC to coordinate the operations of these components and to acquire and process the transient displacement responses. Figure 3-2 shows a chip scale package (CSP) sample being inspected with the laser ultrasound-interferometric system.

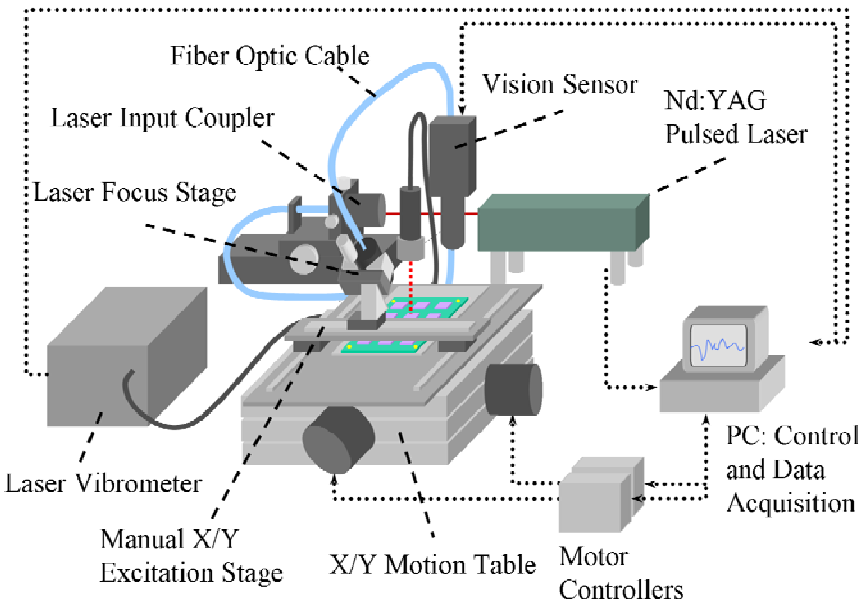


Figure 3-1 Setup of laser ultrasound-interferometric inspection system

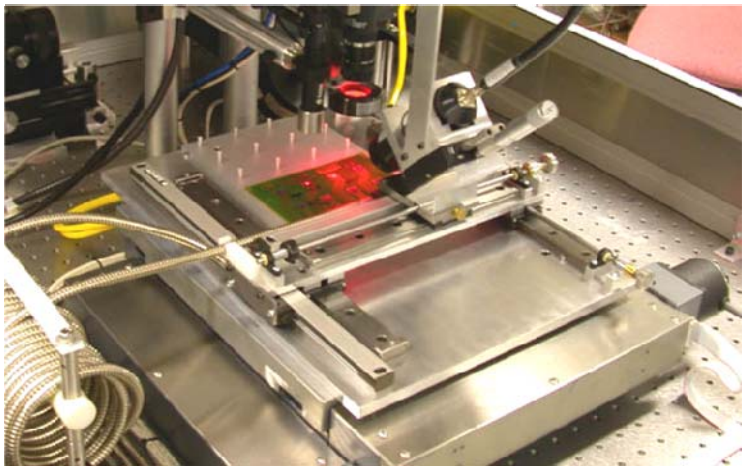


Figure 3-2 CSP being inspected with laser ultrasound-interferometric system

The pulsed Nd:YAG laser generates short laser pulses with a duration of 4~5 ns at the wavelength of 1064 nm. The laser has a variable repetition rate from 1 to 20 Hz and the pulse energy is adjustable through an optical attenuator. The maximum energy per

pulse is 45 mJ. A fiber optic beam delivery system is used to launch laser pulses onto the package surface with an incident angle of 45° to the sample surface. This angle is necessary to avoid conflicts with the interferometer, which is perpendicular to the package surface [Howard T., 2002]. The laser energy is measured using a laser power meter. The fiber-optic laser Doppler vibrometer is used to capture the transient out-of-plane displacement response at selected inspection positions. Its sensor head is positioned perpendicular to and 55 mm away from the sample surface. The sensor head has a spot size of 3 μm. The vibrometer has a displacement measurement resolution of 0.3 nm and a bandwidth from 50 kHz to 25 MHz. For a single inspection point, multiple measurements are taken at consecutive laser pulses and averaged to increase signal-to-noise ratio (SNR). The analog output signal of the vibrometer is internally low-pass filtered with a cutoff frequency of 2 MHz and is sampled at 25 MHz. The transient out-of-plane displacement responses normally die out completely before the end of each acquisition period. The vision system is used to capture the board fiducials to calculate the coordinates of laser excitation and inspection points on the sample surface. The automated X-Y positioning table positions the test device under the interferometer for measurement. The positioning repeatability of the table is approximately ±6 μm and ±4 μm in the X and Y directions, respectively. The laser excitation spot is positioned by a manual stage affixed to the top of the automated positioning table. The manual stage uses preloaded linear motion components and linear encoders for precise positioning, and the overall stage precision is estimated to be better than ±10 μm in each axis. The test device is held by a vacuum fixture underneath the X-Y positioning table during the experiments. The data

acquisition, stage positioning and machine vision subsystems are controlled and coordinated by a PC.

3.1.1 Pulsed Nd:YAG Laser System

A Polaris II Q-switched Nd:YAG laser system from New Wave Research, shown in Figure 3-3, was used as the pulsed laser source. The pulsed Nd:YAG laser generates short laser pulses with a duration of 4~5 ns at the wavelength of 1064 nm. The laser has an adjustable repetition rate from 1 to 20 Hz. The pulse energy is adjustable through a motorized optical attenuator and can be up to 45 mJ/pulse. The diameter of laser beam in this system is 3 mm. After a 30-minute of warm up, the energy stability pulse by pulse is over 98% for 10000 shots.

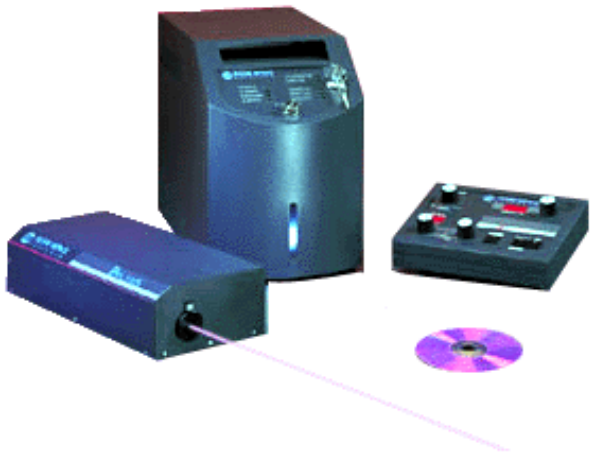


Figure 3-3 Pulsed Nd:YAG laser system (Source: New Wave Research®)

3.1.2 Laser Doppler Vibrometer

In this research, laser Doppler vibrometer is used to capture the transient out-of-plane displacement responses in nanometer scale induced by laser ultrasound. This laser Doppler vibrometer consists of a heterodyne fiber optic interferometer with the model OFV-511 (shown in Figure 3-4) and an ultrasonic vibrometer controller with the model OFV-2700 both from Polytec®. The operating principle of heterodyne interferometer is shown in Figure 2-5. The vibrometer is used to directly measure the transient out-of-plane displacement responses on the package surface. Its sensor head is positioned perpendicular to and 55 mm away from the sample surface. The sensor head has a spot size of 3 μm to facilitate a high spatial resolution. The maximum range of displacement measurements is 150 nm peak-to-peak and it provides 50 nm/V analog output. The vibrometer has a high displacement measurement resolution of 0.3 nm and a bandwidth from 50 KHz to 25 MHz. Multiple measurements are taken at a series of laser pulses and averaged to suppress noises. The output bandwidth of the vibrometer can be configured as to measure transient displacement responses either up to 2 MHz or up to 20 MHz, depending on the application. The configuration with the output bandwidth limit of 2 MHz has a smaller bandwidth but a better resolution. Current experiments are done with the 2 MHz bandwidth limit since the signals of interest are normally below 2 MHz.

Figure 3-4 Fiber-optic heterodyne interferometer (Source: Polytec®)

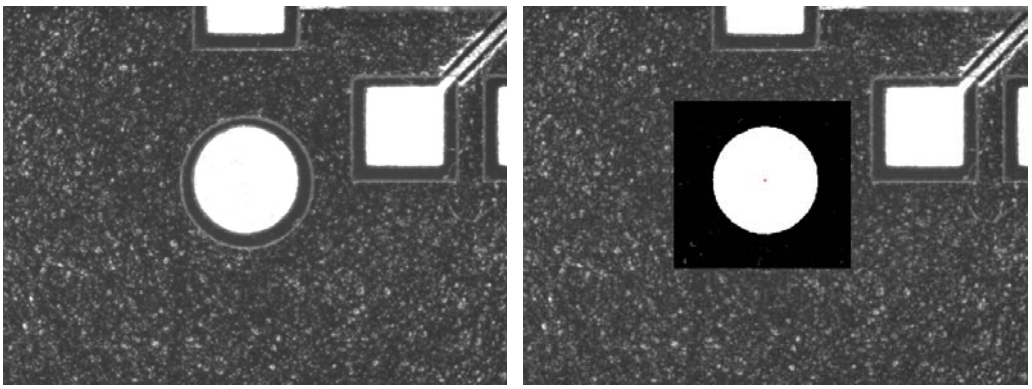
3.1.3 Vision System for System Calibration

Fiducial marks are a feature of the printed wiring board artwork, usually circular, square or cross-shaped solid pads on the printed wiring boards. The fiducial marks provide common measurable features to allow automated assembly equipments, which use vision systems, to accurately place components on their corresponding bond pads. In this research work, these fiducial marks are used in a similar way to precisely align a specimen to be inspected with the laser vibrometer. The smart sensor - DVT Series 600 (shown in Figure 3-5) selected for this research uses a 3.6 x 4.8 mm CCD with 480 x 640 pixel resolution and is combined with network communications (Ethernet). This sensor produces 8-bit grayscale images and incorporates a number of useful software tools for easy image processing.

Figure 3-5 DVT series 600 smart sensor for fiducial mark locating

The software, called FrameWork, was provided with the sensor to manage and operate DVT smart sensor. For fiducial mark locating, the "blob" software tool was most effective because it grouped light or dark pixels together and then calculated the centroid position of the resulting blob of pixels. This tool was ideal for fiducial measurement because fiducial marks are often gold plated pads against the high contrast background of the substrate material, forming a bright spot in an image. The vision system comes with an alignment and calibration procedure to find the actual scale factor between units of pixels and real distance units, as well as to eliminate the image distortion [Howard T., 2002].

The fiducial marks are measured with sub-micron resolution and ±1.0 μm repeatability in the view area of the vision system. Figure 3-6 shows the measurement of an actual fiducial mark on a test substrate [Howard T., 2002].



(a) (b)

Figure 3-6 Blob measurement of fiducial marks: (a) raw image (b) fiducial blob

3.1.4 X-Y Positioning Table

An X-Y positioning table from Nutec Inc., as shown in Figure 3-7, features excellent accuracy, orthogonality and bidirectional repeatability. The manufacturer's specifications claimed an accuracy of 7.5 μm per 100 mm of travel, orthogonality error of less than 7.5 arc-seconds and bidirectional repeatability of ±1.0 μm. The precise, preloaded, crossed-roller bearings in the stage eliminated the problems with play. The precision-grade lead screw drive also provides positioning accuracy and repeatability. The motion stage has a travel of 200 mm x 200 mm and a large mounting surface.

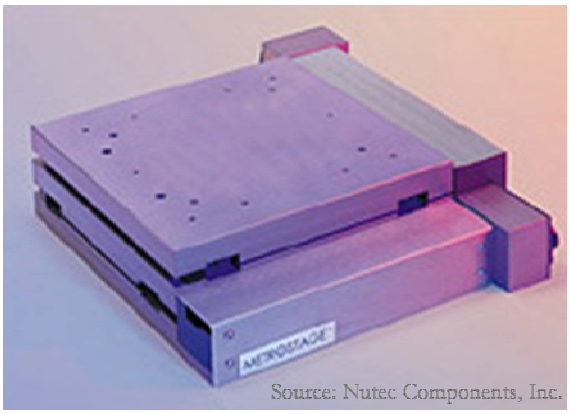


Figure 3-7 X-Y positioning table (Source: Nutec®)

The positioning table positions the test boards under the vibrometer light beam for measurement. The positioning repeatability of the stage has been verified to be approximately ±6 μm and ±4 μm in the X and Y axis, separately [Howard T., 2002].

3.1.5 Manual Laser Positioning Stage

A manual X-Y stage, as shown in Figure 3-8, is used in this work to provide repeatable laser excitation positioning. It uses preloaded linear motion components and linear encoders for precise positioning. The stage was designed with a locking mechanism that allowed fine positioning through an adjustor screw when locked and rapid manual repositioning when unlocked. The linear encoders have 1.0 μm resolution, and the overall stage precision is estimated at better than ±10 μm in each axis.

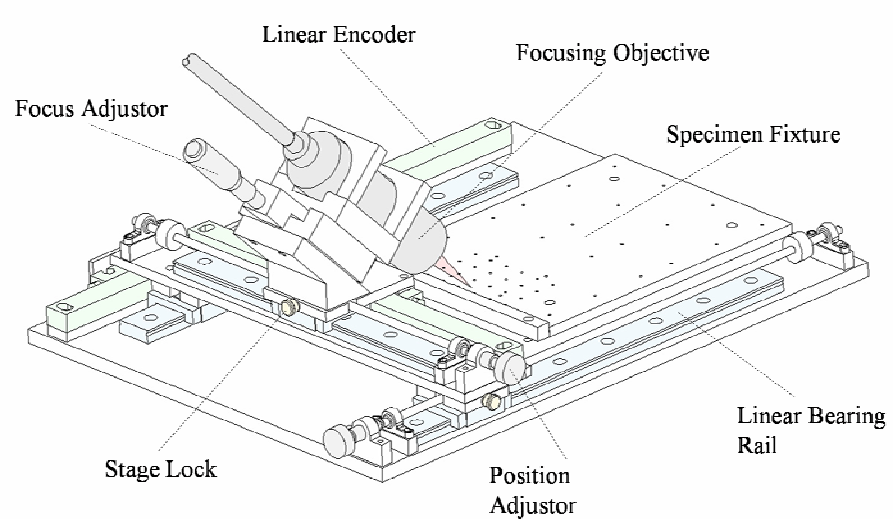


Figure 3-8 Manual X-Y laser excitation positioning stage

The manual focus stage for the output objective of the fiber optic beam delivery system is mounted on the X-Y stage with a 45° angle, as shown in Figure 3-8 [Howard T., 2002]. This focus stage had 25.0 mm of total travel, allowing the laser spot size to be adjusted over a wide range to control laser energy density excited on the package surface.

The laser spot excited on a specimen is elliptical rather than circular, as shown in Figure 3-9, because the output objective is mounted at a 45° angle to allow the measurement of out-of-plane displacement with the laser vibrometer from above. The range of possible excitation areas varies from 1.48 mm^2 to approximately 3.81 mm^2, providing much more flexibility in adjusting excitation spot size and then controlling laser pulse energy density.

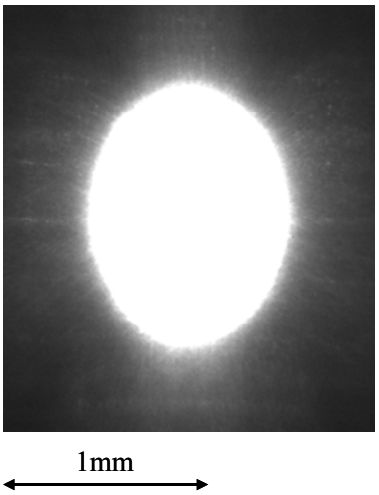


Figure 3-9 Elliptical shape of laser spot

3.1.6 Fiber Optic Beam Delivery System

The delivery of nanosecond scale laser pulses in the mJ energy range through optical fibers was a challenging task. These operating conditions pushed the limits of high damage threshold, fused silica fiber [Howard T., 2002]. The goal of the fiber delivery system is to deliver the required pulsed laser through one fiber with a standoff distance between the delivery system and test specimen. This delivery system from US Laser Corporation, whose schematic is shown in Figure 3-10 [Howard T., 2002], consists of an input coupling assembly, a rugged fiber optic cable with a 600 μm core diameter and an output focusing objective.

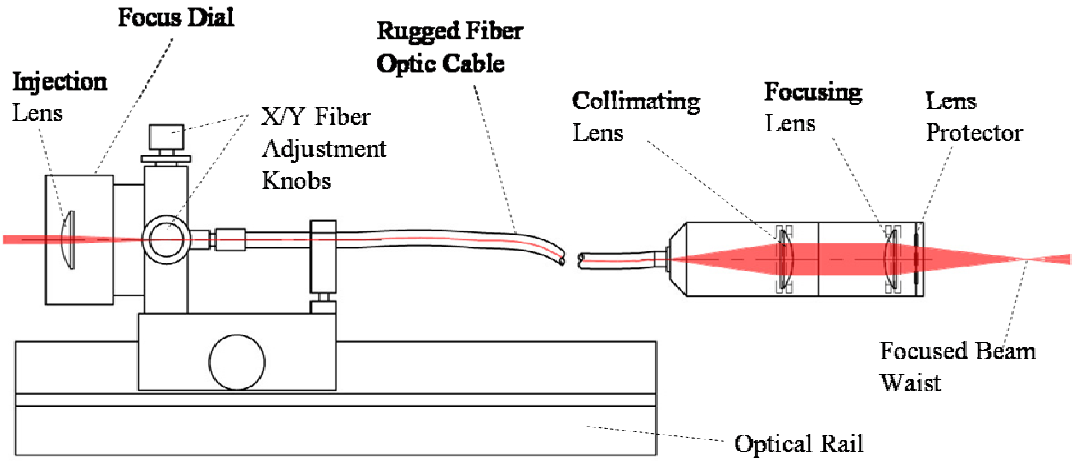


Figure 3-10 Fiber optic laser beam delivery system

3.1.7 Vacuum Fixture

A vacuum fixture, as shown in Figure 3-11, is used to constrain test boards on the X-Y positioning table in experiments. This fixture consists of a vacuum plate to hold test boards as large as 152.4 mm x 203.2 mm. The vacuum plate has channels on its back surface to connect two vacuum ports in the fixture base plate to 48 individual ports in the vacuum plate. Two separate vacuum port arrangements were built into this fixture for holding various sizes of test boards.

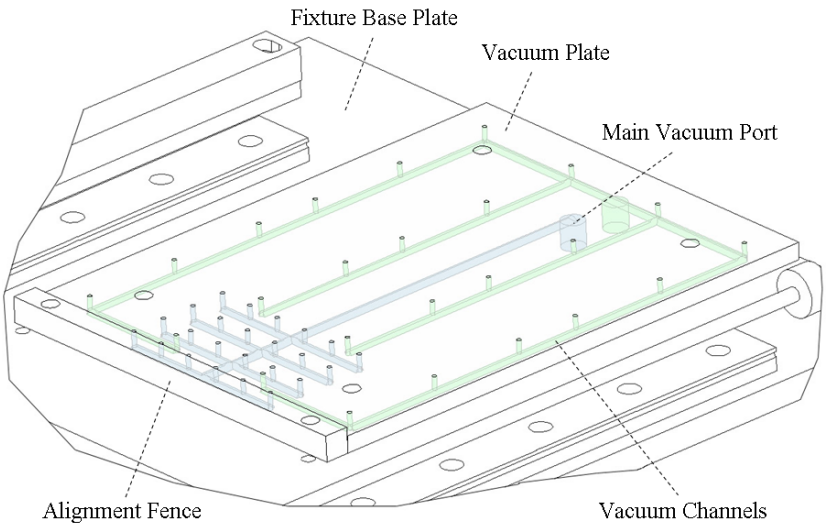


Figure 3-11 Vacuum fixture

3.2 System Integration and Calibration

Different components of this system have to be integrated to function as a whole to enable and facilitate inspection process. The calibration should be first carried out to build appropriate 'recipes' for measurement of test boards. During a typical inspection process, two fiducial marks on the test board were first captured and located by the vision sensor, then the translation and rotation of CAD frame coordinate system in the design file (Gerber file in this case) relative to the vision sensor (CCD camera) coordinate system were calculated by using a coordinate transformation program. Once the translation distance and rotation angle were obtained, the coordinates of samples and inspection points on the samples in the CAD frame coordinate system can be transformed to the vision sensor coordinate system. One appropriate inspection 'recipe' is then created for one type of test boards. When this step is done, the inspection process starts by following the created 'recipe'. The X-Y positioning table and pulsed laser head are then

driven automatically or manually to the desired positions separately following the 'recipe' and complete the whole inspection process, whose duration depends on the number of inspection points.

3.2.1 Calibration of Pulsed Laser Excitation Energy Density

It is reported by Dixon that a strong normal force component was present in single-crystal silicon <100> and the ablation had occurred when the pulsed Nd:YAG laser was above an energy density of 0.2-0.24 J/cm^2 [Dixon S., 1996]. In current electronic packages, a thin passivation layer (approximately 1.0 μm in thickness) is applied to the backside of the wafer to protect the underlying silicon from corrosion and to prevent excessive damage to the die edges during the dicing process. Though the existence of this thin passivation layer could alter reflectivity of laser on the package surface, pulsed Nd:YAG laser can still induce strong ultrasound in the silicon die since it was reported by Dixon that there was enough penetration of Nd:YAG laser pulses into single-crystal silicon [Dixon S., 1996]. A calibration of pulsed laser excitation energy density with manual stage standoff was done to investigate the conditions under which the ultrasound was generated in the thermoelastic regime. First, the relationship between laser excitation spot size and manual laser stage standoff was calibrated, as shown in Figure 3-12. Second, the power of laser pulses excited at corresponding stage standoff was measured with the power meter and the package surface was checked for ablation with naked eyes after each test. In the phase I of calibration, the standoff of manual laser stage was fixed at 22.5 mm achieving the minimum spot area of 1.484 mm^2 and the laser power was adjusted from 38.0 mW to 61.2 mW. In the phase II, both the stage standoff and laser power were adjusted to study the evolution of laser energy density by increasing

spot area size. From the calibration results summarized in Table 3-1, it is known that when the laser power reached 61.2 mW with the minimum spot area of 1.484 mm^2, the laser energy density was 0.21 J/cm^2, which exceeded the safety threshold of avoiding laser ablation in silicon as discussed previously. Correspondingly, ablation mark was observed on the silicon die surface after test. In other cases when the laser power was below 61.2 mW with the minimum spot area of 1.484 mm^2, no clear mark was observed visually. In the phase II study, though the laser power was increased, laser energy density decreased with the increasing of laser excitation spot area and laser energy density was below the calculated safety threshold. There was no obvious ablation mark observed after the test for these cases. It is concluded that the laser energy density can be controlled below the threshold of laser ablation by increasing laser excitation spot area if high laser power is required for complex and dense package formats, including emerging 3-D packages. It should be stated that tiny marks were observed on the die surface under microscopy for the cases with energy density being below but close to the threshold. It was considered that the tiny marks came from initial marks on the silicon die surface, including die chipping induced in assembly process. Meanwhile, the calibration results can be improved when the effect of thin passivation layer on the silicon surface is included into the analytical calculation of safety threshold to avoid laser ablation in the silicon die.

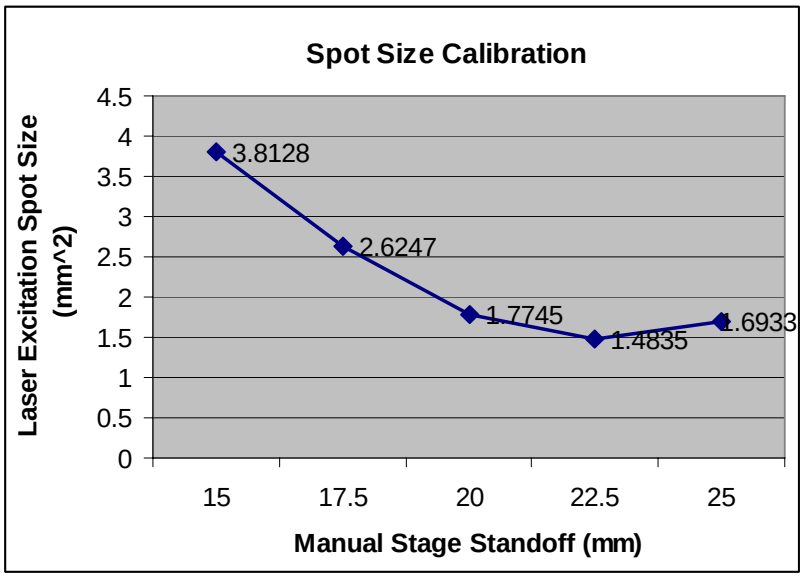


Figure 3-12 Laser excitation spot size calibration

Table 3-1 Laser energy density calibration

Calibration Phase	Laser power (mW)	Laser energy (mJ/Pulse)	Spot area (mm^2)	Laser energy density (J/cm^2)
1	38.0	1.9000	1.484	0.13
1	39.6	1.9800	1.484	0.13
1	42.0	2.1000	1.484	0.14
1	44.4	2.2200	1.484	0.15
1	61.2	3.0600	1.484	0.21
2	39.6	1.9800	1.775	0.11
2	48.5	2.4250	1.775	0.14
2	73.4	3.6700	3.813	0.10

3.2.2 Coordinate Transformation

Previous work thoroughly examined all the coordinate frames necessary for system calibration [Howard T., (2002), Zhang L., (2006)]. Figure 3-13 shows the components of the system with their respective coordinate frames [Howard T., 2002]. Four coordinate systems were chosen to describe the inspection system from the base frame of the vision system to the local frame of a specimen on the test board.

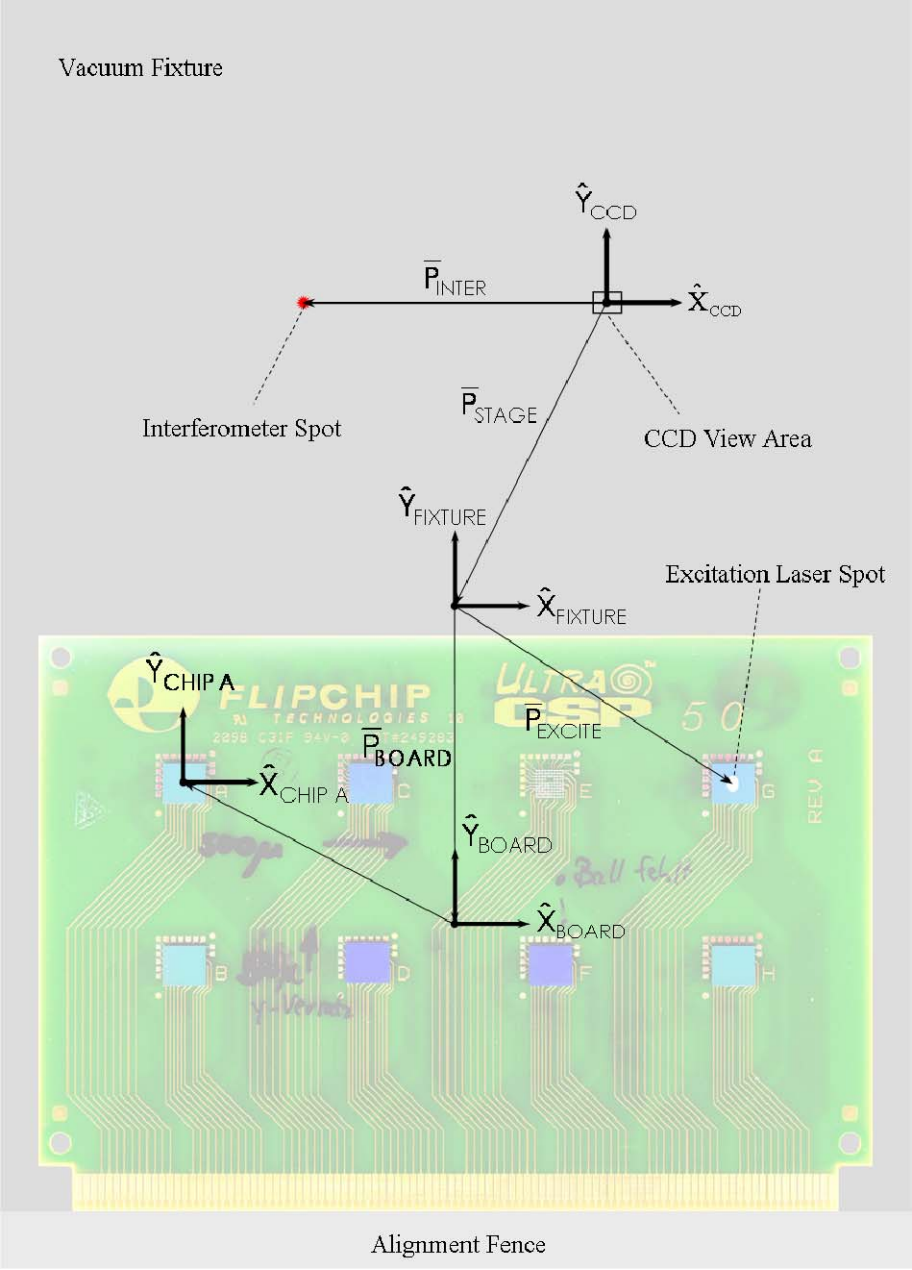


Figure 3-13 Coordinate frames for inspection: chain of coordinate frames from the base frame (CCD) to the local specimen frame (Source: Howard T., 2002)

Two coordinate frames, as shown in Figure 3-13, namely the PCB design coordinate system (the CAD frame) and the vision sensor coordinate system (the measurement frame) were used to calculate the rigid body transformations by assuming there was no non-linear transformation between different parts. Two fiducial points on

the test vehicle were measured to calculate both translation and rotation of the CAD frame relative to the measurement frame. Once the rigid body transformations, i.e. the translation and rotation between the two frames are obtained, all the inspection and excitation locations can be transformed from the CAD frame to the measurement frame. The rotation transformation provides a skew correction allowing the sample to be arbitrarily positioned on the fixture as opposed to having to be aligned against an alignment fence.

The coordinates of a fiducial point in the CAD frame can be denoted as (x', y'), the coordinates of the same point in the measurement frame as (x, y), the translation between the two frames as X and Y, and the rotation between the frames as θ. The translation matrix $T(X,Y)$ in a 2-D homogeneous form can be written [Zhang L., 2006] as,

$$\begin{bmatrix} x \\ y \\ 1 \end{bmatrix} = T(X,Y)\begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & X \\ 0 & 1 & Y \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} \tag{3-1}$$

The rotation matrix $R(z,\theta)$ can be written as,

$$\begin{bmatrix} x \\ y \\ 1 \end{bmatrix} = R(z,\theta)\begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} \tag{3-2}$$

The composition of XY translation and z-axis rotation is,

$$\begin{bmatrix} x \\ y \\ 1 \end{bmatrix} = T(X,Y)R(z,\theta)\begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & X \\ \sin\theta & \cos\theta & Y \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} \tag{3-3}$$

Given two measured fiducial points (x_1', y_1') , (x_2', y_2') and their coordinates (x_1, y_1) , (x_2, y_2) in the CAD frame, the simultaneous equations are solved to calculate $\sin\theta, \cos\theta$, X and Y as,

$$\sin\theta = \frac{(x_1' - x_2')(y_1 - y_2) - (x_1 - x_2)(y_1' - y_2')}{(x_1' - x_2')^2 + (y_1' - y_2')^2} \tag{3-4}$$

$$\cos\theta = \frac{(x_1 - x_2)(x_1' - x_2') + (y_1 - y_2)(y_1' - y_2')}{(x_1' - x_2')^2 + (y_1' - y_2')^2} \tag{3-5}$$

$$X = x_1 - x_1' \cos\theta + y_1' \sin\theta \tag{3-6}$$

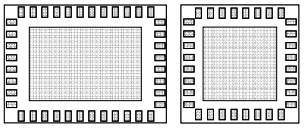
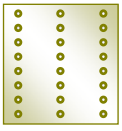
$$Y = y_1 - x_1' \sin\theta - y_1' \cos\theta \tag{3-7}$$

3.3 Test Vehicles

A variety of electronic packages with defects have been used to evaluate the laser ultrasound-interferometric inspection system under development. These include flip chip packages on the organic FR-4 substrates ("PB18") with open bumps or cracked bumps

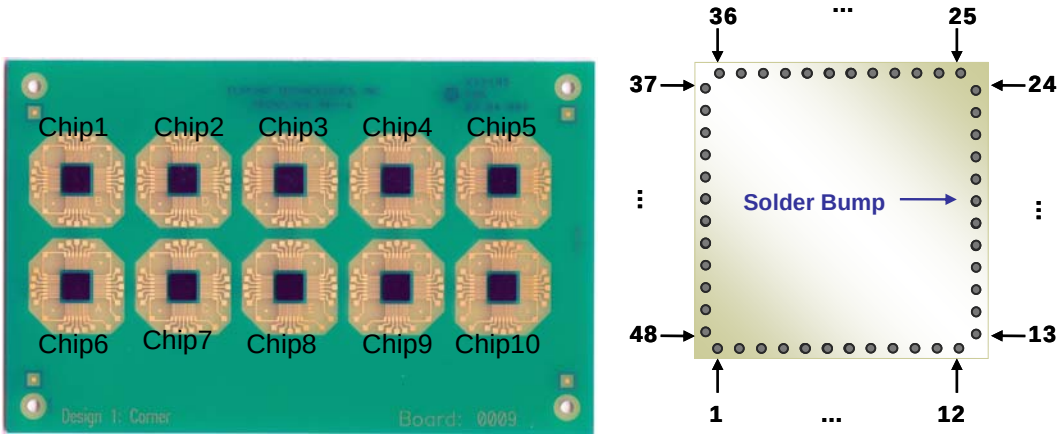
due to thermal fatigue, flip chip packages on the ceramic substrates ("SiMAF") with manufacturing defects, land grid arrays on the FR-4 board with concerns on solder bump thermal reliability. The specifications and associated defect types are tabulated in Table 3-2. Good samples were prepared to use as the reference. In PB18 flip chip packages, open bumps were created by removing individual copper pads before reflow soldering; thermal fatigue cracks were created through accelerated temperature cycling (ATC) following JEDEC standards in both flip chips and land grid arrays.

Table 3-2 Test vehicle specifications

Device Name	PB18	Kedron	SiMAF
Device Type	Flip Chip	Land Grid Array	Flip Chip
I/O count	48	32/40	12/24
Package size	6.35 mm x 6.35 mm	8 mm x 8 mm, 8 mm x 11 mm	4.36 mm x 4.16 mm
Array pattern			
Package thickness	600 µm	1400 µm	400 µm
Bump diameter	190 µm	400 µm x 700 µm	200 µm
Bump height	140 µm	100 µm	160 µm
Bump pitch	457 µm	500 µm	500 µm
Solder Material	Sn-Pb eutectic solder	Sn-Ag-Cu solder	Sn-Pb eutectic solder, or lead-free solder
Substrate	FR-4	FR-4	Ceramic
Defect Type(s)	open bumps, thermal fatigue cracks	Thermal fatigue defects	Various manufacturing bump defects
Underfill	No	No	No

3.3.1 Tin-Lead PB18 Flip Chip Test Vehicle

One set of flip chip test vehicle is PB18 without underfill, which is a daisy chain flip chip with 48 eutectic tin-lead solder bumps (63Sn37Pb) around the peripheral of the chip. The die size is 6.35 mm × 6.35 mm × 0.6 mm and the typical bumps are 190 μm in diameter and spaced with a pitch of 457 μm, with twelve located on each edge of the chip. This test vehicle has 10 flip chips on each board numbered from chip 1 to chip 10, as shown in Figure 3-14 (a). The schematic of flip chip is shown in Figure 3-14 (b).



(a) (b)

Figure 3-14 (a) Board layout of PB18 flip chip test vehicle (b) schematic of flip chip

The flip chips on the tin-lead test vehicle were created with one to four adjacent open bumps starting from the left top corner of each flip chip, as shown in Figure 3-15. The white circles indicate the locations of open bumps in Figure 3-15. To create these specimens, individual solder pads were removed from the PWB design. The boards were placed in a reflow oven and run through a standard eutectic solder reflow profile to attach the chips to the board. Without any metal to bond with, the solder bumps were not

attached to the board [Erdahl D. et al., 2005]. As listed in Table 3-3, chips 4 and 5 are good; while chips 1, 2, 3 and 6 have one to four open bumps separately beginning from the left top corner of the die. Chips 7 to 10 are omitted in this work.

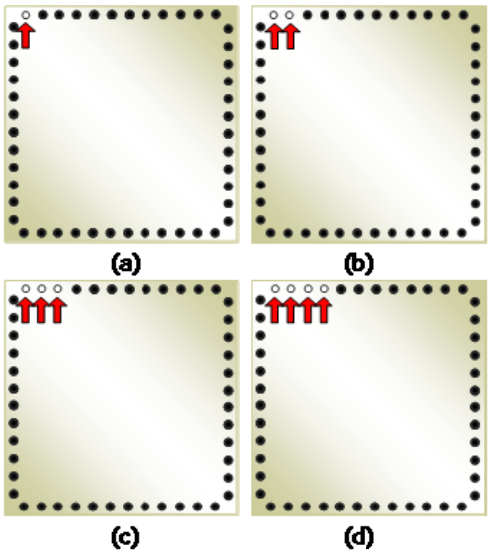


Figure 3-15 Schematic of open bump pattern in PB18 flip chips

Table 3-3 Open bump distribution in PB18 flip chips

Chip number	Status
Chips 4&5	Good
Chip 1	1 open bump
Chip 2	2 open bumps
Chip 3	3 open bumps
Chip 6	4 open bumps

For PB18 tin-lead test vehicles, the measurement locations are selected on the chip surface directly on top of solder bumps. The laser excitation and inspection pattern of the tin-lead flip chip test vehicle is shown in Figure 3-16. In Figure 3-16, solder bumps are marked as large round circles and the stars represent the inspection positions, with the excitation laser spot indicated by an elliptical shape.

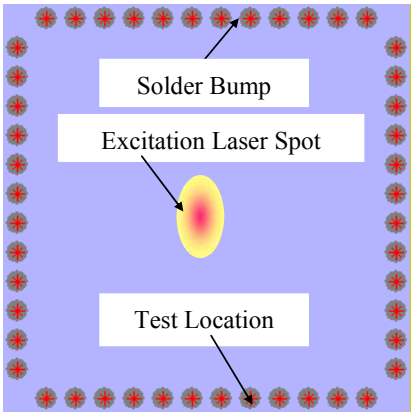


Figure 3-16 Excitation and inspection pattern of tin-lead flip chip test vehicle

3.3.2 Lead-Free "SiMAF" Flip Chip Test Vehicle

The other set of flip chip test vehicle contains at most 30 flip chip specimens ("SiMAF", Siemens AG) on each board, with board layout shown in Figure 3-17. This flip chip specimen has 24 lead-free solder bumps distributed evenly on three parallel columns and is surface mounted onto ceramic-based PWB without underfill. The die size is 4.36 mm × 4.16 mm with a thickness of 400 μm. The bump diameter and height are 200 μm and 160 μm separately with a bump pitch of 500 μm.

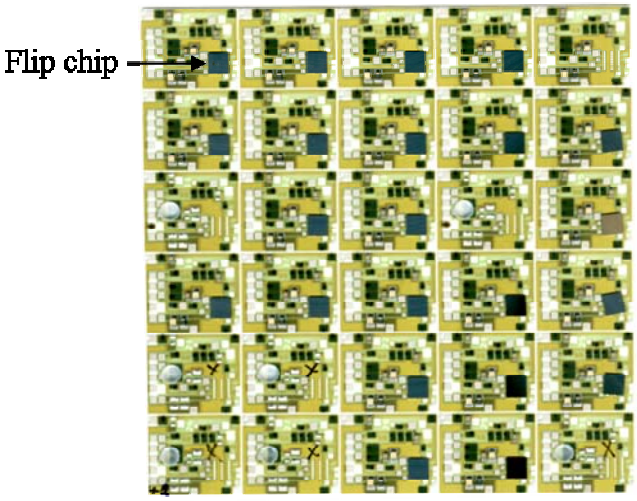


Figure 3-17 Board layout of lead-free flip chip test vehicle

For the lead-free test vehicle, the inspection points are selected on the chip surface directly on the top of solder bumps. The laser excitation and inspection pattern of lead-free flip chip test vehicles is shown in Figure 3-18. In Figure 3-18, solder bumps are marked as large round circles and the stars represent the inspection points, with the excitation laser spot indicated by an elliptical shape.

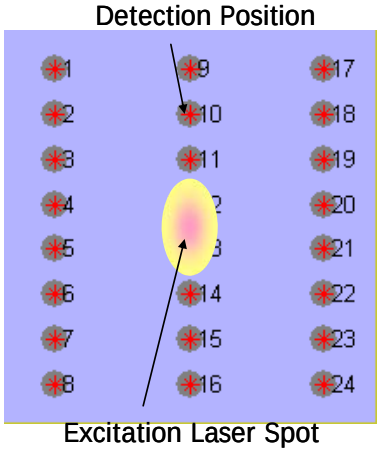


Figure 3-18 Excitation and inspection pattern of lead-free flip chip test vehicle

3.3.3 Land Grid Array Test Vehicle

Land grid array package (LGA) has been increasingly used in portable electronics and wireless products in terms of its low profile on the printed wiring boards, and direct lead-free assembly process compatibility. In 2004, the flip chip land grid array (FCLGA) package was introduced by Intel® in its microprocessors to eliminate the fragile package pins in the pin grid array (PGA) packages and enable the second-level interconnect pitch to shrink for socketed components [Intel®, 2005].

The two devices with LGA packages are RF modules built on a substrate containing several laminated layers of organic materials. The modules are encapsulated through over-molding. They are mounted on a typical 4-layer 1 mm-thick FR-4 board.

Figure 3-19 illustrates the overall top view of the board, on which two devices U5 and U6 are placed. The overall dimension of device U5 is 8 mm × 8 mm × 1.4 mm and that of device U6 is 8 mm × 11 mm × 1.4 mm. The package of U5 has 32 peripheral pads with the size of 0.4 mm × 0.7 mm and one 5 mm × 5 mm central pad. The package of U6 has 40 peripheral pads with the size of 0.4 mm × 0.7 mm and a larger central pad (5 mm × 7.6 mm). The pad surface finish is gold. The components are mounted on the supporting boards through LGA terminations. The bottom layer schematics of LGA packages are shown in Figure 3-20 (a) and (b) for devices U5 and U6 separately, with the gray rectangles representing peripheral and central pads. All the pads are non-solder mask defined (NSMD) to enhance thermal reliability of the LGA packages. Figure 3-21 shows the normal cross-section of LGA packages.

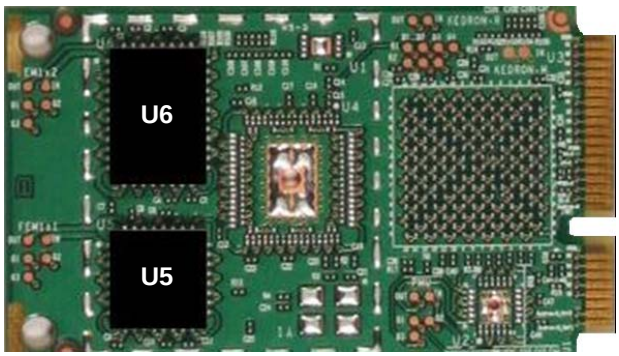
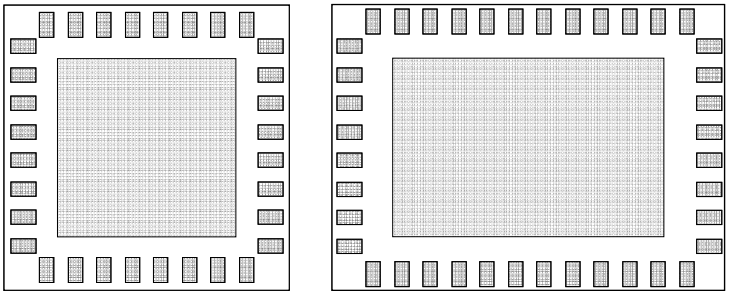


Figure 3-19 LGA test vehicle



(a) (b)

Figure 3-20 Bottom layer schematic of LGA packages: (a) U5 (b) U6 (rotated)

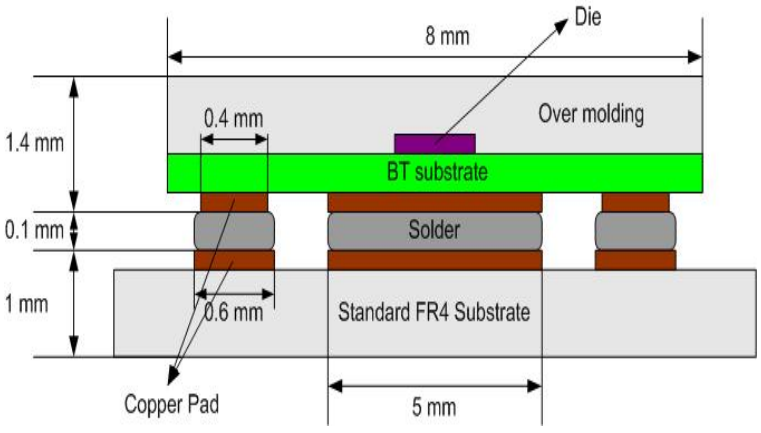


Figure 3-21 Cross-section of LGA package (not to scale)

CHAPTER 4

INTERPRETATION AND PROCESSING OF LASER ULTRASOUND SIGNALS

The principle for the laser ultrasound-interferometric inspection system to detect and identify solder joint/bump defects is to extract and quantify the difference in the transient out-of-plane displacement responses between the package to be inspected and the known-good-package under pulsed laser loading. While a minor difference may come from the geometry or material variation of electronic packages during manufacturing process, or variation of measurement instruments and environment, a major difference between the responses indicates abnormal solder joint/bump interconnections. In order to extract and quantify the response differences, Liu and Zhang proposed error ratio, power spectrum analysis and correlation coefficient methods separately [Liu et al., (2002), Zhang et al., (2004)]. These methods have been employed and have been successful in detecting missing, misaligned, or cracked solder bumps in FCPs and CSPs.

However, there are two problems for laser ultrasound signal processing with these methods. First, the transient out-of-plane displacement response induced by the laser pulse is intrinsically non-stationary and broadband, with frequencies ranging from kilohertz to megahertz. The spectral power distribution (SPD) of laser ultrasound signals changes with time during the sampling period. FFT-based power spectrum analysis, ER and CC methods all use raw transient responses from the entire frequency range to extract and quantify the difference between responses. However, defect features are more prominent in specific frequency ranges (and corresponding time-domain components)

rather than being evenly spread across the whole frequency range. The data analysis in the whole frequency range might obscure the extraction of features most sensitive to the defects.

Having in mind that small defects have a minor effect on the transient out-of-plane displacement response, more sensitive methods capable of detecting small changes of transient displacement responses become important. In recent times, methods based on wavelet analysis are increasingly being used as promising tools for defect detection and identification. They have been widely used in the areas of fault diagnosis of electronic machines [Goumas K., 2002], crack identification in beam and plate structures [Douka E., 2004], internal delamination detection in multi-layer composite materials [Chan Y., 2000], and transient signal analysis for electronic circuits and power switching [Wilkinson W., 2004]. Wavelet analysis has also been used for ultrasound signal processing. In the work done by Aydin, wavelet analysis was used to detect embolic Doppler ultrasound signals by optimizing time-frequency resolution [Aydin N., 2004].

The advantage of wavelet analysis is that it can decompose a signal into a series of wavelet components, each of which is a time-domain signal that covers a specific frequency band, and allows identification of local features from the scale of wavelets. In this research, a method for inspecting solder bumps in electronic packages based on wavelet analysis has been developed and applied to overcome the previous problems with ER, CC and FFT. The power spectrum variation with time can be reflected by joint time-frequency spectrum analysis using a continuous wavelet transform (CWT) method. Although short-time Fourier transform (STFT) has also been introduced in the time-frequency spectrum analysis of transient signals, it does not provide multi-resolution in

both time and frequency domains. In contrast to STFT, wavelet analysis provides a good resolution in the frequency domain at low frequencies and a good resolution in the time domain at high frequencies [Douka E., 2004]. The signal components most sensitive to the defects can be extracted and quantified using discrete wavelet transform (DWT) based on multi-resolution signal decomposition (MSD). The hidden details of signals, that maybe otherwise go unnoticed, can then be detected. This is valuable in laser ultrasound signal analysis, where it is important to detect small changes in the signals. The measurement sensitivity can be increased by analyzing the characteristic signal components sensitive to the defects. In this research, the wavelet analysis method has been implemented for processing the transient signals.

There is another problem for processing laser ultrasound signals with correlation coefficient method. Correlation coefficient method is suitable for processing stationary signals; however the transient out-of-plane displacement response induced by the laser pulse is intrinsically non-stationary. Local or short-time temporal coherence (LTC) analysis has been proposed in this work to overcome this limitation. LTC is a measure of time-dependent shape difference between two signals and it emphasizes the short-time coherence between signals [Michaels J. et al., 2005]. A windowing function, which is normally a rectangular function, is used to estimate the short-time coherence between signals within a window length at a particular time. It provides a quantitative measure of the relative change in waveform shapes as a function of time [Michaels J. et al., 2005].

In the literature, local temporal coherence analysis has been applied to structural detection and identification by researchers. Michaels applied the LTC to diffuse ultrasonic signals for inspecting the structural damage and demonstrated its effectiveness

by comparing LTC analysis to other signal-processing methods, including time domain differencing and spectral differencing [Michaels J. et al., 2005]. Bennacer and Dather used short-time correlation analysis to find the water-ice spatial interface in porous media with an acoustic system [Dather K., (1997), Bennacae R., (1998)]. Lubinski used short-time correlation to estimate high-resolution, high signal-to-error ratio strain in ultrasound elasticity imaging [Lubinski M., 1999]. LTC is a measure of time-dependent shape differences between signals, and it emphasizes the short-time coherence between signals. The laser ultrasound signal is intrinsically nonstationary and broadband, with frequencies ranging from kilohertz to megahertz, and therefore LTC is suitable for processing laser ultrasound signals.

4.1 Wavelet Analysis of Laser Ultrasound Signals

4.1.1 Introduction to Wavelet Analysis

A function $\psi(t)$ is a mother wavelet only and only if its Fourier transform $\Psi(\omega)$ satisfies the admissibility condition [Goswani J., 1999],

$$C_{\psi} = \int_{-\infty}^{\infty} \frac{|\Psi(\omega)|^2}{|\omega|} d\omega < \infty \tag{4-1}$$

This condition implies that,

$$\Psi(0) = \int_{-\infty}^{\infty} \psi(t) dt = 0 \tag{4-2}$$

Equation 4-2 shows that a mother wavelet is an oscillating function with zero mean value. The CWT of a function $f(t)$ is defined as,

$$W(b,a) = \int_{-\infty}^{\infty} f(t) \frac{1}{\sqrt{a}} \psi^* \left(\frac{t-b}{a} \right) \tag{4-3}$$

Where, $\psi^*(t)$: complex conjugate of wavelet function,

b and a : translation and dilation parameters.

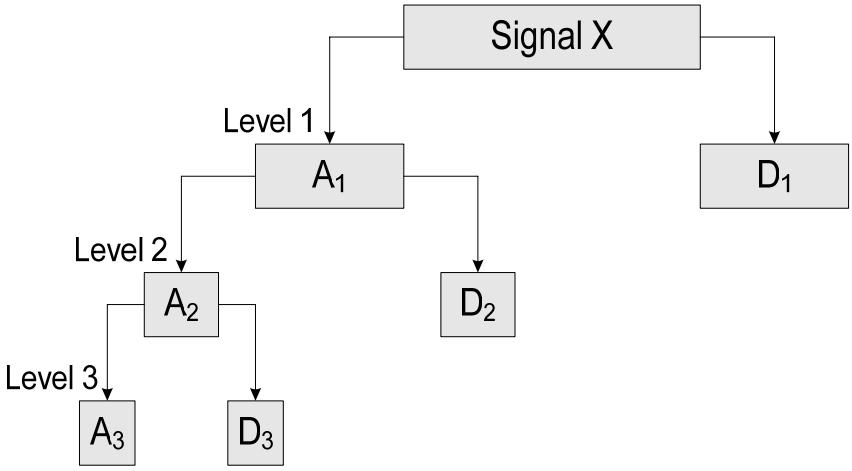
Equation 4-3 is in fact the inner product of $f(t)$ with scaled and translated mother wavelet $\psi(t)$. A smaller value of dilation parameter a corresponds to a smaller time interval and a larger frequency range, and vice versa. The translation parameter b, on the other hand, indicates the location of the wavelet window along the time axis. Thus, by changing (b,a), the time-frequency spectrum of a function $f(t)$ is obtained through CWT. Wavelet transform retains both time and frequency resolution compared to traditional Fourier Transform, which loses the time resolution of non-stationary signals.

The DWT of a function $f(t)$ is defined in Equation 4-4, which is suitable for applications with the requirement of high-speed processing.

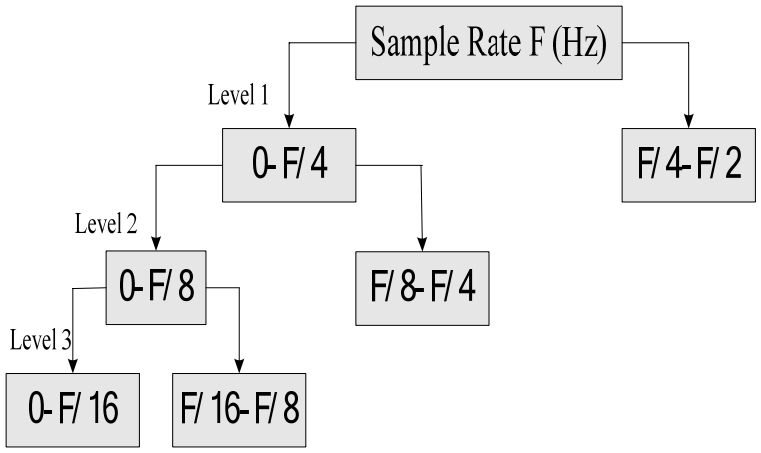
$$W(k,s) = \int_{-\infty}^{\infty} f(t) \frac{1}{2^{s/2}} \psi^* \left(\frac{t}{2^s} - k \right) dt \tag{4-4}$$

The DWT can be implemented efficiently with parallel filter bank algorithm proposed by Mallat [Mallat S., 1989]. With parallel filter bank algorithm, the DWT is a decomposition of a function following hierarchical levels with different resolutions,

shown in Figure 4-1 (a). The decomposition algorithm starts with the original signal X, and computes the values of the approximate signal A_1 and detailed signal D_1 at decomposing level 1, then those of A_2 and D_2 at level 2, and so on. At each step, the function is decomposed into two sets of wavelet coefficients: low-frequency components (low-pass filtering) and high-frequency components (high-pass filtering) of the function. The frequency bands corresponding to the decomposed approximate and detailed signals during the decomposition process are shown in Figure 4-1 (b). The signal is thus decomposed into exclusively separate frequency bands and the filtering outputs are then downsampled. The number of wavelet coefficients for each branch is then reduced by a factor of two. The general steps of one decomposition are shown in Figure 4-2. Furthering the decomposition means increasing the scale that corresponds to zooming into low-frequency portion of the spectrum. The DWT proceeds in $\log_2 n$ steps at most, if a signal of length n is given. This operation is termed multi-resolution signal decomposition (MSD) [Goswani J., 1999].



(a)



(b)

Figure 4-1 (a) Schematic of Mallat decomposition (b) frequency bands of Mallat decomposition

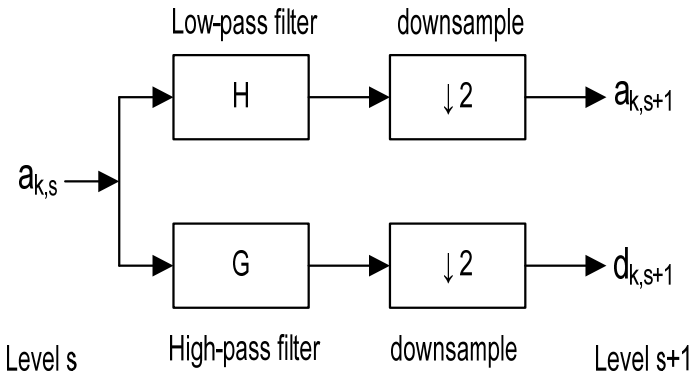


Figure 4-2 General steps of DWT decomposition

MSD uses low and high pass filters to obtain the approximate and detailed components of a signal. The decomposition relation in filter bank algorithm is expressed as,

$$\phi(2^s t - l) = \sum_k \{h_0[2k-l]\phi(2^{s+1}t - k) + h_1[2k-l]\psi(2^{s+1}t - k)\} \tag{4-5}$$

Where,

$\phi(t)$ and $\psi(t)$: scaling function and wavelet function separately,

$h_0(k)$ and $h_1(k)$: decomposition coefficients of low-pass and high-pass filter banks.

Equation (4-6) relates the coefficient $a_{k,s+1}$ of the scaling function and coefficients $d_{k,s+1}$ of the wavelet function at any scale to scaling function at the next lower scale $a_{k,s}$.

$$a_{k,s+1} = \sum_l h_0[2k-l]a_{l,s}$$
$$d_{k,s+1} = \sum_l h_1[2k-l]a_{l,s} \quad (4\text{-}6)$$

After decomposing the original signal into approximate and detailed components corresponding to different frequency ranges by Mallat's filter banks algorithm, the signal components which are sensitive to defects can be obtained and defect features can be extracted.

There are many families of wavelets, such as Harr, Mexican hat, Biorthogonal, Daubechies wavelets. Daubechies wavelet is a family of orthogonal wavelets and is referred to as D_n, where n is the order of wavelet. This family of wavelets has been extensively used, since its wavelet coefficients capture the maximum amount of signal energy [Goumas S., 2002]. D_4 wavelet has been chosen and used as the mother wavelet throughout the present work.

4.1.2 Application of Wavelet Analysis to Tin-Lead Flip Chip Test Vehicle

4.1.2.1 Time and frequency domain analyses of laser ultrasound signals

Figure 4-3 shows the time-domain responses of tin-lead flip chips 1 to 6 (as shown in Figure 3-14) measured at the same detection position. Even though the total measurement period is 164 μs, we choose to show the signals in the time interval from 0 to 20 μs. It shows the transient out-of-plane displacement responses of the chips with one to four open solder bumps compared to those of two good chips. It is observed that the waveforms from two good chips match very well, and one of them is selected as the reference. However, the signals from the chips with open solder bumps differ from the

reference one. The more open bumps a chip has, the larger difference is shown in the responses between the chip and the reference. The power spectrums of time-domain signals are shown in Figure 4-4. Figure 4-4 (a) shows the original power spectrum and Figure 4-4 (b) shows power spectrum segment with the frequency ranging from 160 to 320 KHz.

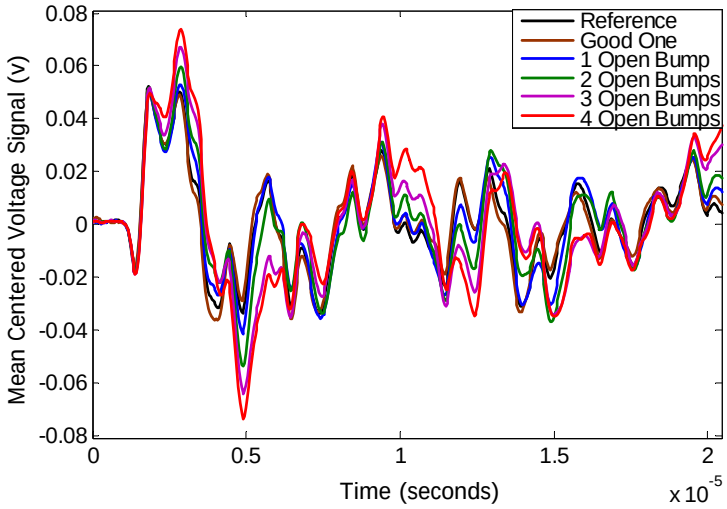


Figure 4-3 Time-domain responses of tin-lead flip chips with open bumps

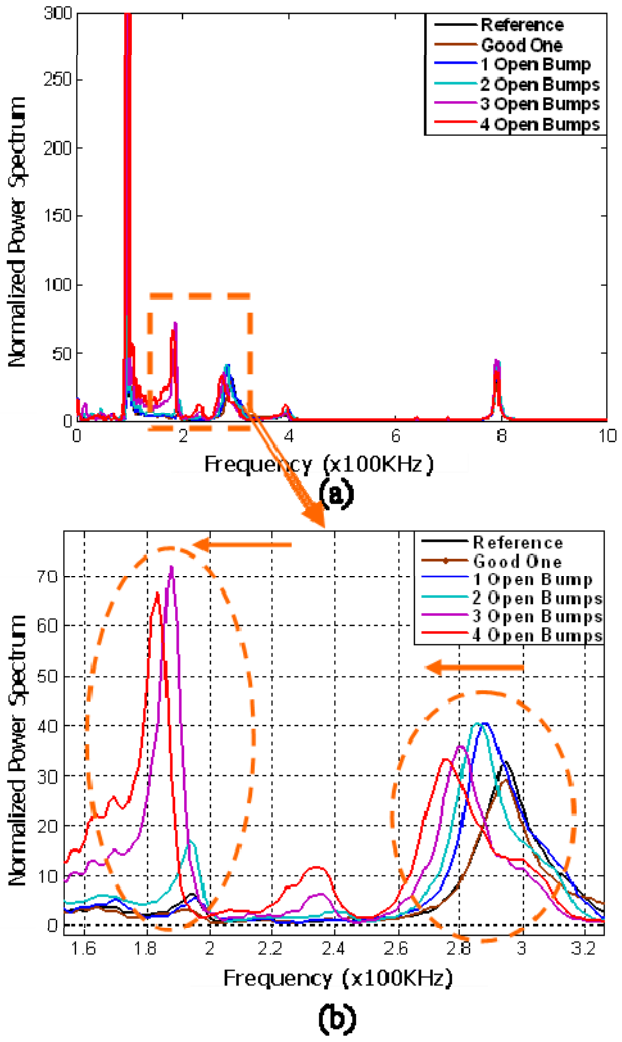


Figure 4-4 Power spectrums of time-domain responses of tin-lead flip chips: (a) original power spectrum (b) segment in range of [160-320] KHz

The electronic package with solder bump interconnections is modeled as a mass-spring structure. When there is a defect in the spring(s), the stiffness of the system decreases. In the same way, when there is a defect in the solder bump(s), the stiffness of the whole electronic package decreases. Therefore the natural frequencies of PB18 flip chip shift backward when it has open detects, and the natural frequencies can be extracted from the power spectrum. Frequency shifts are clearly observed from Figure 4-4 in the

two frequency ranges of [180-200] KHz and [270-300] KHz with the increasing number of open bumps. It is shown that there are obvious defect features, which are caused by open bumps, in the signal components corresponding to these two frequency ranges. The analysis of signal components in these frequency ranges can produce the features corresponding to open bump defects.

4.1.2.2 Comparison of CWT, ER and Correlation Coefficient methods for data analysis

In order to quantify the differences in the transient out-of-plane displacement responses between the chips to be tested and the reference, Liu and Zhang previously used error ratio or correlation coefficient methods separately to process laser ultrasound signals as discussed in Section 2.4.

Correlation coefficient method removed or eliminated some limitations of ER method. However, the CC method, as well as the ER method, use time-domain signals in the whole frequency range to quantify the difference between signals and are not easy to tell the minor difference caused by defects in the time or frequency domain. With continuous wavelet transform, the time-frequency spectrum of signals can be obtained and the variance of spectral power distribution over time can be observed. This variation of the spectral power distribution with time shows that laser ultrasound signal is non-stationary. The signal components sensitive to solder bump defects can be obtained with discrete wavelet transform and quantified. The goal is to increase the measurement sensitivity by using discrete wavelet transform implemented with a filter banks method.

Figure 4-5 (a) to (e) show the time-frequency spectrums of good flip chip and chips with 1 to 4 open bumps from tin-lead test vehicle using CWT. By comparing the time-frequency spectrums of the chips with open bump defects to that of a good chip, it is

observed that the laser ultrasound signal is broadband and non-stationary. Its power spectrum varies with time, which can not be demonstrated in the power spectrums as shown in Figure 4-4. With the increasing number of open bumps, there are larger differences in the time-frequency spectrums between defective chips and the good chip.

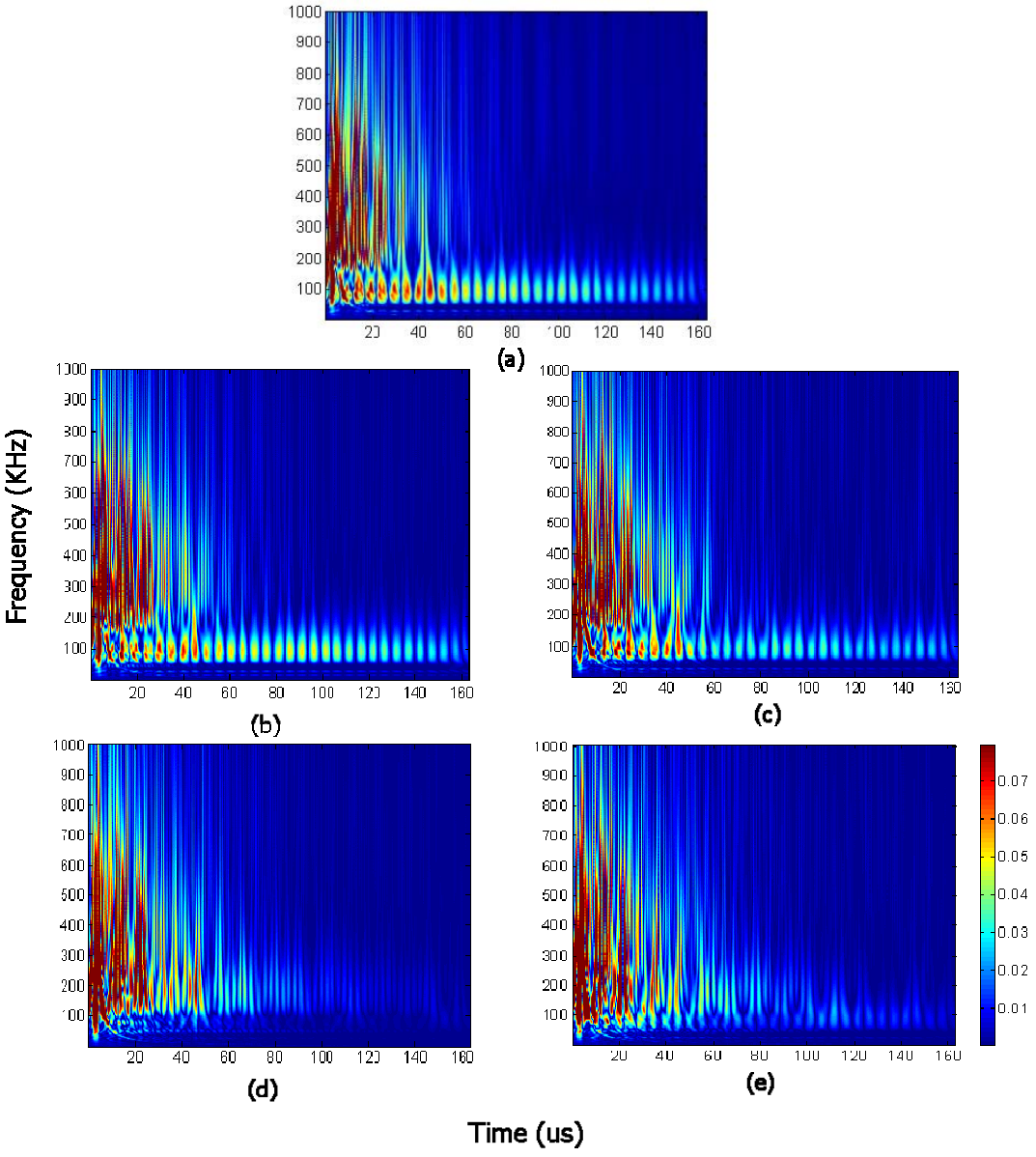


Figure 4-5 Time-frequency spectrums of tin-lead flip chips with CWT: (a) good chip (b) chip with 1 open bump (c) chip with 2 opens (d) chip with 3 opens (e) chip with 4 opens

4.1.2.3 Comparison of DWT, correlation coefficient methods for data analysis

The approximate and detailed signal components of transient responses through decomposing to level 6 from the good tin-lead flip chip using DWT are shown in Figure 4-6. It is observed by estimating the period of signal components that different levels of signal components lie in different frequency ranges as expected.

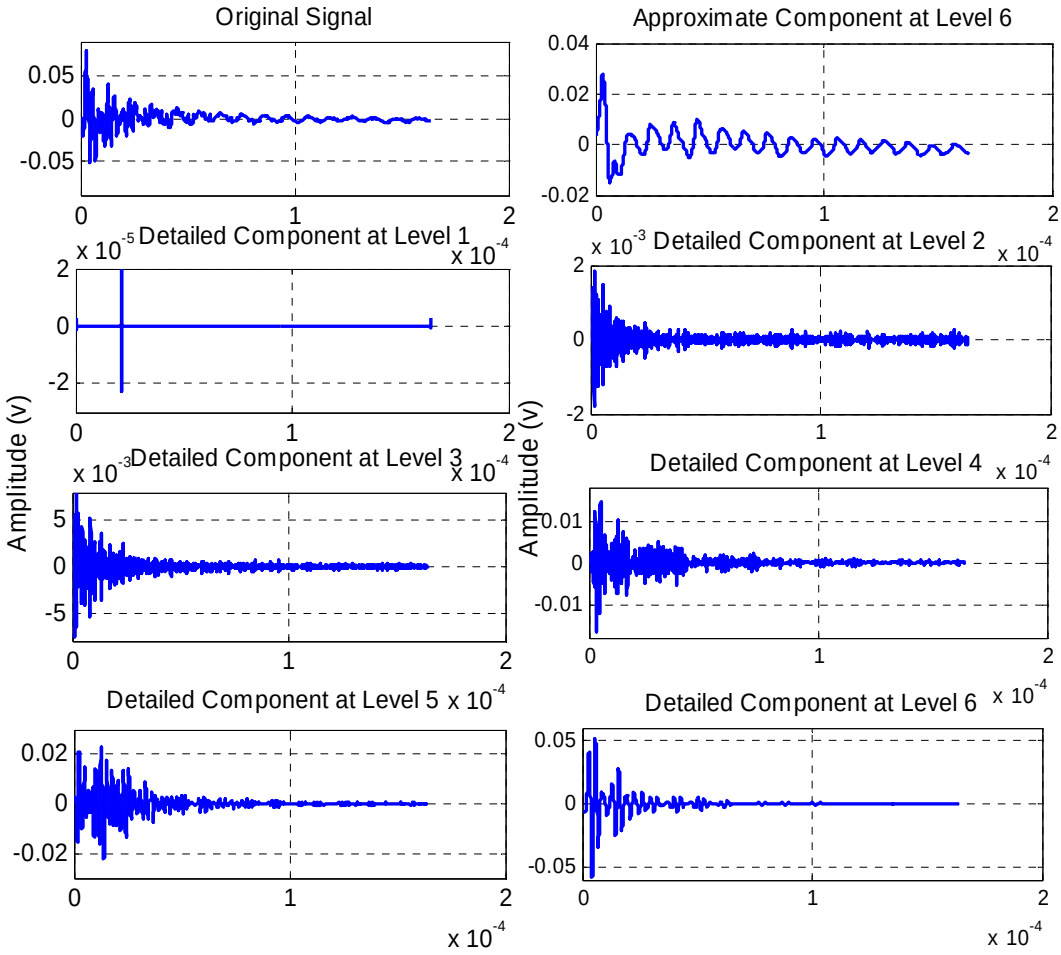
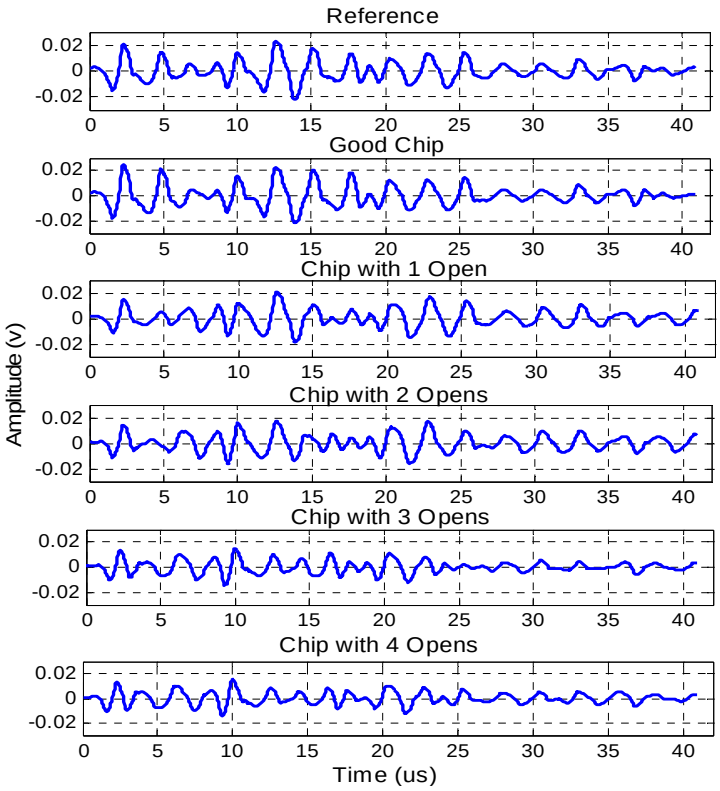


Figure 4-6 Approximate and detailed signal components after DWT

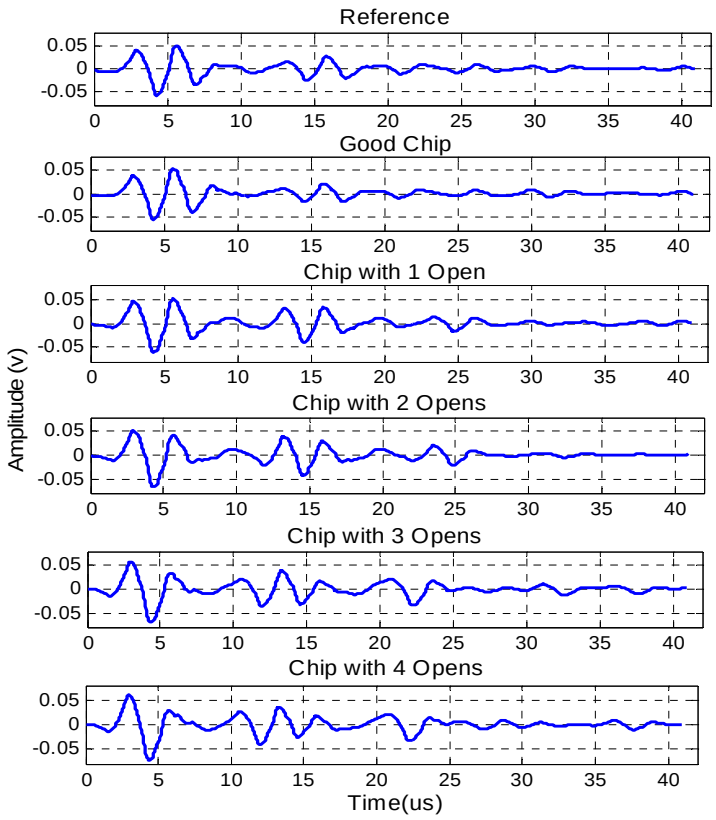
From Figure 4-1, it is known that the detailed signal components at levels 5 and 6 lie in the frequency ranges of [F/64-F/32] and [F/128-F/64] separately if *F* is assumed to

be the sampling rate, which is set to be 25 MHz in this work. Therefore, the frequency ranges corresponding to decomposed detailed signals at levels 5 and 6 are [390.6 781.2] KHz and [195.3 390.6] KHz. From the power spectrums shown in Figure 4-4, certain signal components lie in these two frequency ranges respectively. The detailed signal component at levels 5 and 6 are selected for further processing. These signal components at levels 5 and 6 from good and defective chips are extracted and shown in Figure 4-7 (a) and (b) separately in the time interval from 0 to 40 μs.



(a)

Figure 4-7 Decomposed detailed signal components: (a) level 5 (b) level 6



(b)

Figure 4-7 continued

Differences in detailed components between the measured signals and the reference are quantified with root mean square (RMS). On the tin-lead test vehicle, flip chips 4 and 5 are good chips, and chip 4 is selected as the reference. Chips 1 to 3 and chip 6 have 1 to 4 open bump(s) separately. The results from MCC and wavelet analysis methods are listed in Table 4-1. In Table 4-1, the MCC and wavelet values between the good chip and the reference are defined as X_0. Correspondingly, the values between chips 1 to 3, 6 and the reference are defined as X_1, X_2, X_3 and X_4, respectively. From Table 4-1, it is shown that the differences in the responses between chips with open

bumps and the reference have been amplified using wavelet analysis when compared to MCC values.

Table 4-1 Comparison of MCC and wavelet analysis for tin-lead test vehicle

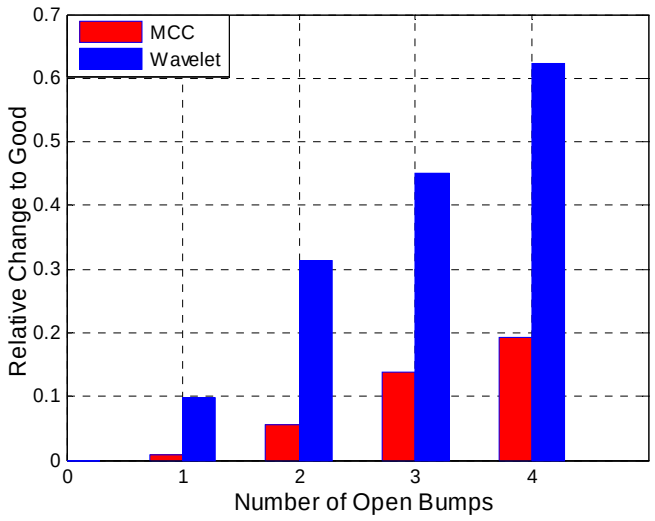
	X_0	X_1	X_2	X_3	X_4
	Chip 5 (good) vs. chip 4 (Ref)	Chip 1 (1 open) vs. chip 4 (Ref)	Chip 2 (2 opens) vs. chip 4 (Ref)	Chip 3 (3 opens) vs. chip 4 (Ref)	Chip 6 (4 opens) vs. chip 4 (Ref)
MCC	0.0109	0.0198	0.0662	0.1482	0.2036
Wavelet (level 5)	0.0344	0.1331	0.3478	0.4860	0.6578
Wavelet (level 6)	0.0120	0.0297	0.0834	0.1831	0.2622

The relative changes in calculated values X_i of defective chips compared to a known-good-chip for both MCC and wavelet analysis methods can be obtained with the following equation,

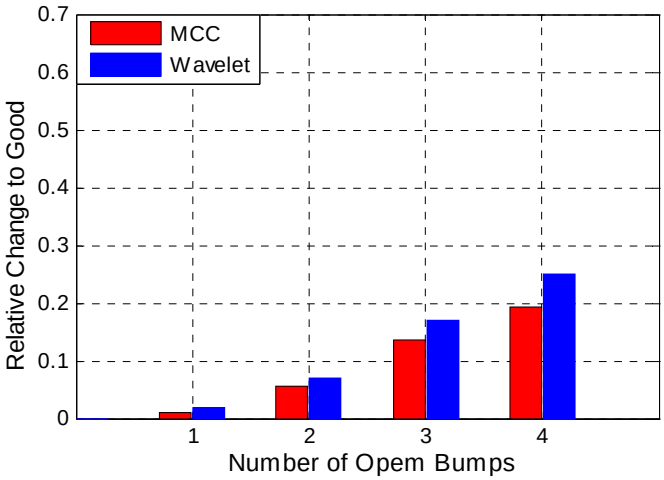
$$RC_i = X_i - X_0 \tag{4-7}$$

The comparisons of relative changes between wavelet methods and MCC at decomposing levels 5 and 6 are shown in Figure 4-8 (a) and (b) separately. When there is no open bump, the change relative to the good chip will be zero. With the increasing number of open bumps, the relative changes become larger. It is clearly shown that the

effect of open bumps on the transient out-of-plane responses has been amplified with wavelet analysis method compared to MCC, and therefore its measurement sensitivity is higher.



(a)

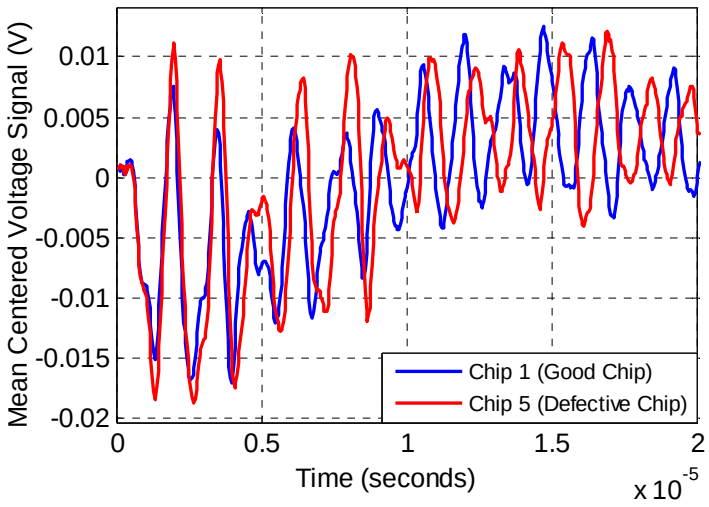


(b)

Figure 4-8 Comparison of relative change between MCC and wavelet methods for tin-lead test vehicle: (a) level 5 (b) level 6

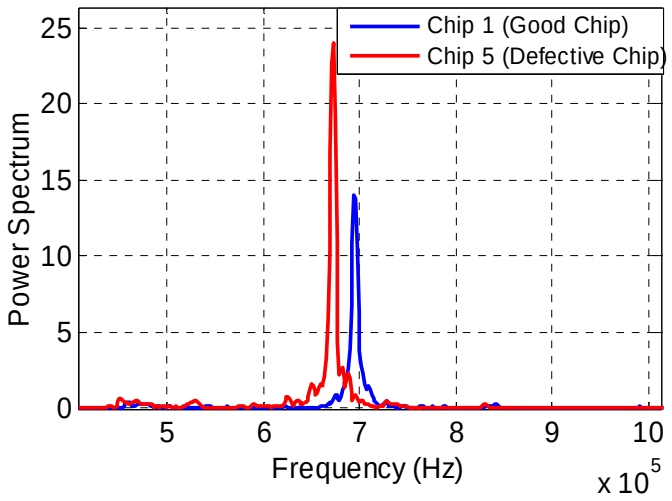
4.1.3 Application of Wavelet Analysis to Lead-Free Flip Chip Test Vehicle

The above analyses are based on the tin-lead flip chip test vehicle with traditional tin-lead eutectic solder bumps (63Sn37Pb). For the lead-free flip chip test vehicle, the test samples are made with lead-free solder bumps (Sn/Ag/Cu). On the lead-free test vehicle, chips 1, 3, 4 are good chips and chips 5 to 10 are defective ones with various manufacturing defects. Chip 1 is selected as the reference. The time-domain signals and corresponding power spectrums of chip1 (good chip) and chip 5 (defective chip) are shown in Figure 4-9 (a) and (b). It is observed from Figure 4-9 (b) that there is an obvious frequency shift backward for the defective chip compared to the good chip and the dominant signal component lies in the frequency range from 600 KHz to 750 KHz. This frequency range corresponds to the detailed signal component with discrete wavelet transform at level 5 lying in the range of [390.6 781.2] KHz.



(a)

Figure 4-9 (a) Time domain signals and (b) power spectrums of lead-free flip chip 1 (good chip) and chip 5 (defective chip)



(b)

Figure 4-9 continued

The detailed signal components of good and defective chips at level 5 were extracted and shown in Figure 4-10 in the interval from 0 to 40 μs. The results from MCC and wavelet analysis methods are shown in Figure 4-11 and summarized in Table 4-2. The results show that the flip chips with defective solder bumps can be distinguished from good chips with both MCC and wavelet analysis methods. It is also observed from the Figure 4-11 and Table 4-2 that the wavelet analysis amplifies the difference of the transient out-of-plane responses between defective and good chips by 20%, which means that the measurement sensitivity has been increased.

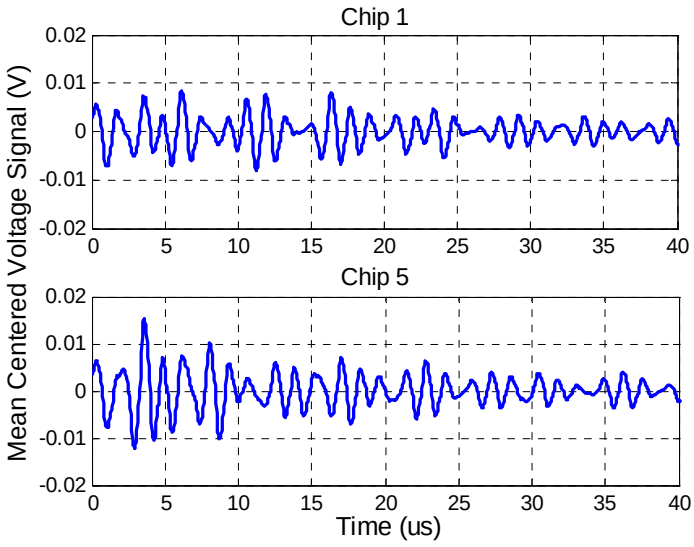


Figure 4-10 Detailed signal components of good and defective flip chips with DWT at decomposing level 5

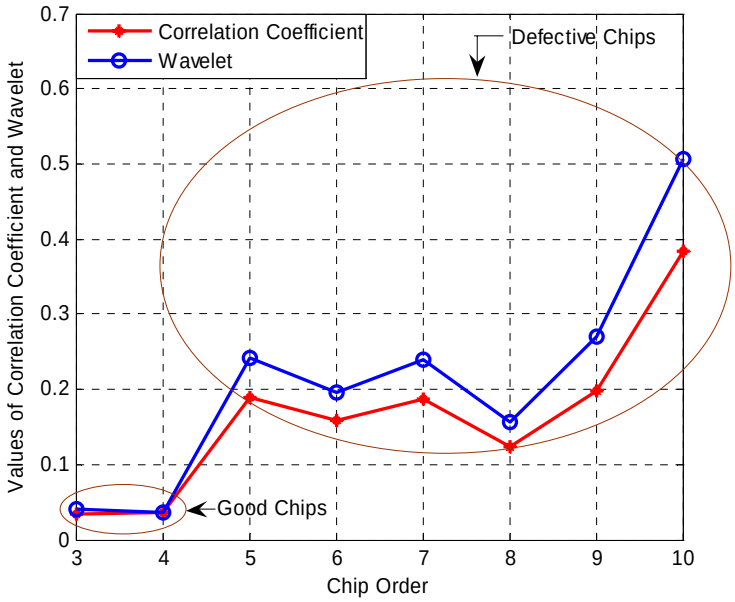


Figure 4-11 Comparison of MCC and wavelet analysis at level 5 for lead-free flip chip test vehicle

Table 4-2 Comparison of MCC and wavelet analysis methods for lead-free test vehicles

	Chip 3 (good) vs. chip 1 (Ref)	Chip 4 (good) vs. chip 1 (Ref)	Chip 5 (bad) vs. chip 1 (Ref)	Chip 6 (bad) vs. chip 1 (Ref)
MCC	0.0349	0.0358	0.1885	0.1589
Wavelet	0.0397	0.0355	0.2427	0.1962
	Chip 7 (bad) vs. chip 1 (Ref)	Chip 8 (bad) vs. chip 1 (Ref)	Chip 9 (bad) vs. chip 1 (Ref)	Chip 10 (bad) vs. chip 1 (Ref)
MCC	0.1869	0.1245	0.1990	0.3848
Wavelet (level 5)	0.2387	0.1570	0.2694	0.5068

From Table 4-2 and Figure 4-11, it is observed that the wavelet analysis amplifies the difference between the transient out-of-plane responses between the defective chip and the reference. It means that the measurement sensitivity of wavelet analysis method is much higher than correlation coefficient method. It is also shown that this system is capable of inspecting flip chip solder bumps made with lead-free materials.

4.1.4 Summary of Wavelet Analysis of Laser Ultrasound Signals

The results show that wavelet analysis increases the measurement sensitivity of flip chip solder bump inspection using laser ultrasound and interferometric techniques. Wavelet analysis has the capability for real-time processing, and can improve the efficiency of on-line evaluation of solder bump interconnections. It can be concluded that the laser ultrasound-interferometric system under development is capable of inspecting solder bumps made from tin-lead or lead-free materials.

4.2 Local Temporal Coherence Analysis

4.2.1 Introduction to Local Temporal Coherence

For stationary signals, the cross-correlation between two signals $x_1(t)$ and $x_2(t)$ is defined [Stark H., 2001] as,

$$R_{12}(\tau) = E[x_1(t)x_2(t+\tau)] \tag{4-8}$$

Where, E denotes the mathematical expectation and τ is the correlation lag.

The temporal coherence, which provides an amplitude-independent measure of shape similarity between signals, is defined [Stark H., (2001), Michaels J. et al., (2005)] as,

$$r_{12}(\tau) = \frac{R_{12}(\tau)}{\sqrt{R_{11}(0)R_{22}(0)}} \tag{4-9}$$

For signals defined in the interval of $[-T/2, T/2]$, the cross-correlation and coherence are estimated [Lubinski M., 1999] by Equations 4-10 and 4-9 separately,

$$R_{12}(\tau) = \frac{1}{T}\int_{-T/2}^{T/2} x_1^{*}(s)x_2(s+\tau)ds \tag{4-10}$$

Where, * denotes the complex conjugate for complex signals.

For the nonstationary signals, a short-time cross-correlation within a window of length T_0 (also called the kernel length) at a particular time t is estimated [Michaels J. et al., 2005] by,

$$R_{12}(\tau,t)=\frac{1}{T_0}\int_{-\infty}^{\infty} x_1{}^{*}(s)w^{*}(s-t)x_2(s+\tau)w(s+\tau-t)ds \qquad (4\text{-}11)$$

Where,

$x_1(t)$ and $x_2(t)$: nonstationary signals,

$w(t)$: windowing function and typically rectangular, as shown in Figure 4-12,

* denotes the complex conjugate for complex signals.

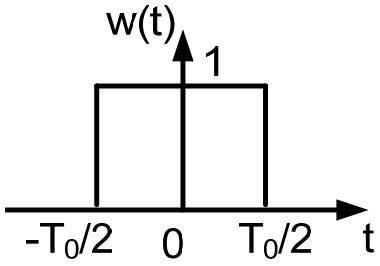


Figure 4-12 Rectangular windowing function

$$w(t)=\begin{cases}1 & -T_0/2\le t\le T_0/2\\ 0 & Otherwise\end{cases} \qquad (4\text{-}12)$$

The local temporal coherence between two signals at time t is estimated [Michaels J. et al., 2005] by,

$$r_{12}(\tau,t)=\frac{R_{12}(\tau,t)}{\sqrt{R_{11}(0,t)R_{22}(0,t)}} \tag{4-13}$$

Two simple examples were given below to illustrate how LTC is applied to signal analysis. In the first example, as shown Figure 4-13, $x_1(t)$ is a sinusoidal signal in the interval of [0 164] μs with peak-to-peak amplitude of 2, and $x_2(t)$ is constructed by attenuating signal $x_1(t)$ by one half in the first interval of [0 82] μs and attenuating signal $x_1(t)$ linearly from ½ to 0 in the second interval of [82 164] μs. The LTC contour and peak coherence values with time between these two signals $x_1(t)$ and $x_2(t)$ are plotted in Figure 4-14 (a) and (b) separately. It is shown from Figure 4-14 that the coherence between signals $x_1(t)$ and $x_2(t)$ in the first interval is 1 and modifying signal amplitude coincidently does not change the coherence between signals. Therefore, there is a perfect coherence between these two signals in the first interval. It is also shown that the coherence between signals $x_1(t)$ and $x_2(t)$ in the second interval has a little drop around 0.1 from 1 and decreasing signal amplitude linearly does change the local coherence between signals; however, the coherence decrease between signals is small by decreasing the ratio of signal amplitude between signals only.

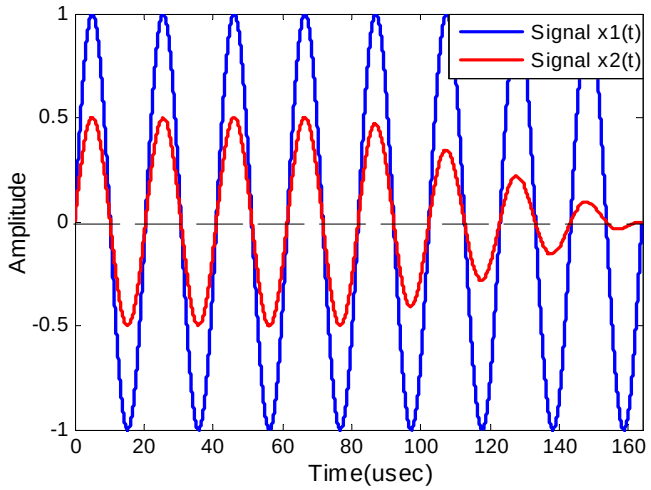
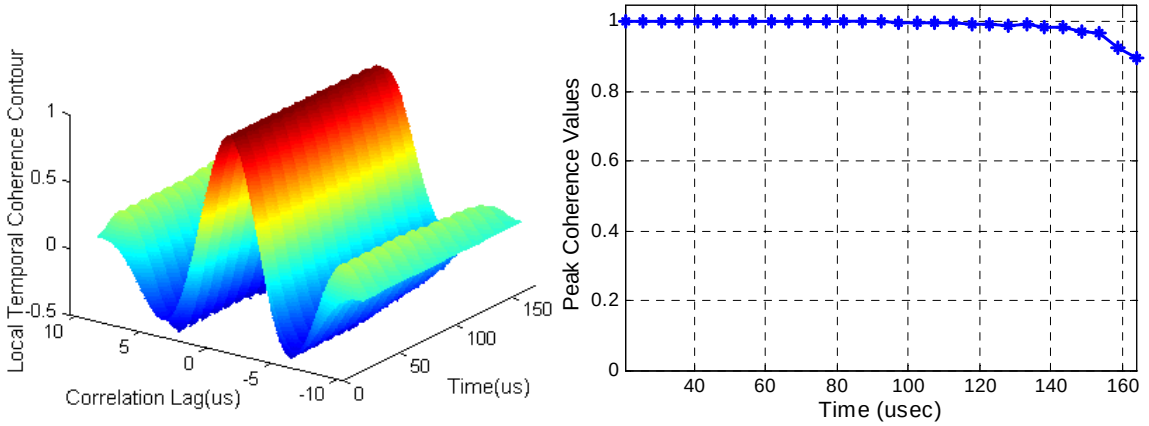


Figure 4-13 Time domain signals in first illustrative example



(a) (b)

Figure 4-14 (a) LTC contour (b) peak coherence values in first illustrative example

In the second example, as shown in Figure 4-15, $x_1(t)$ is a sinusoidal signal in the interval of [0 164] μs with peak-to-peak amplitude of 2, and $x_2(t)$ is constructed by attenuating signal $x_1(t)$ by one half in the interval of [0 82] μs and decreasing the period

of signal $x_1(t)$ by two in the second interval of [82 164] μs. The LTC contour and peak coherence values with time between these two signals $x_1(t)$ and $x_2(t)$ are plotted in Figure 4-16 (a) and (b) separately. It is shown from Figure 4-16 that the coherence between signals $x_1(t)$ and $x_2(t)$ in the first interval is 1 and modifying signal amplitude coincidently does not change the local coherence between signals, which has been shown in the first illustrative example too. However, it is shown that there is a large drop of coherence between these two signals in the second interval. The phase change between signals causes low coherence between signals since these two signals are out of phase in the second interval. Therefore, the effect of phase change on signal coherence has been demonstrated with the local temporal coherence analysis.

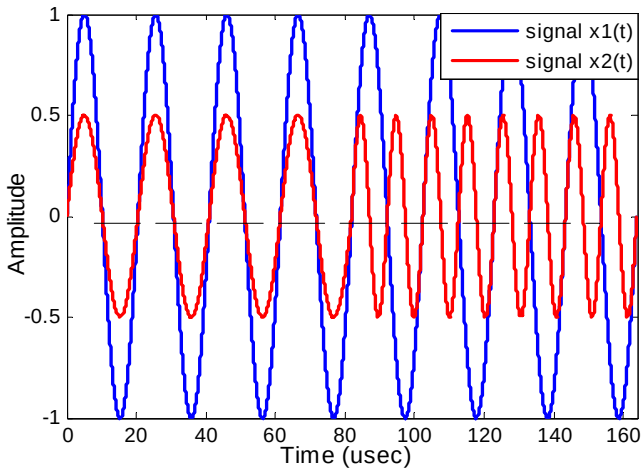
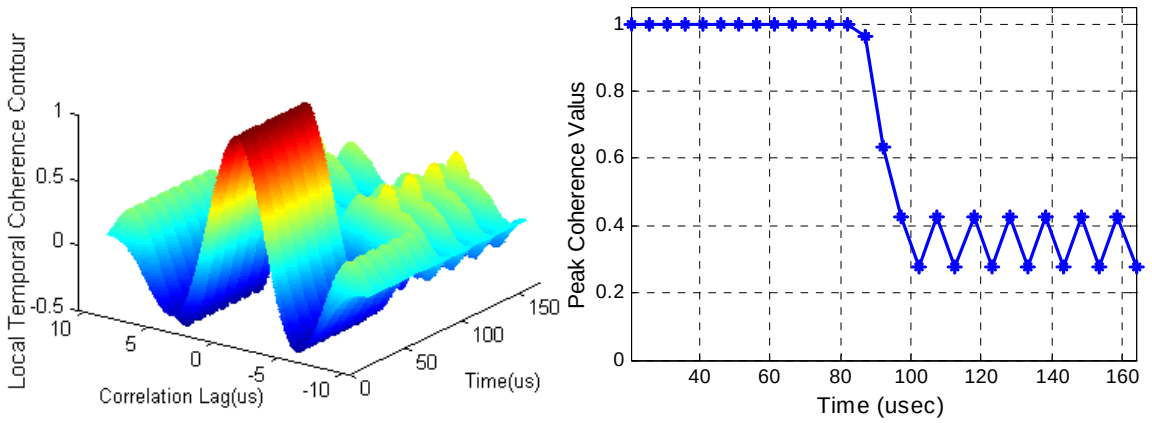


Figure 4-15 Time domain signals in second illustrative example



(a) (b)

Figure 4-16 (a) LTC contour (b) peak coherence values in second illustrative example

In calculating LTC, a fixed-length windowing function, which is typically rectangular, is used to estimate short-time coherence between signals at a particular time. The similarity between signal shapes is estimated with LTC analysis. In order to analyze the trend of coherence evolution with time, we propose a modified LTC (MLTC) that redefines the windowing function $w(t)$ to have an unfixed length. In the definition of MLTC, window length increases linearly with the time increment. Assuming that the time increment is Δt, then the window length T_0 is defined as,

$$T_0 = i\Delta t \tag{4-14}$$

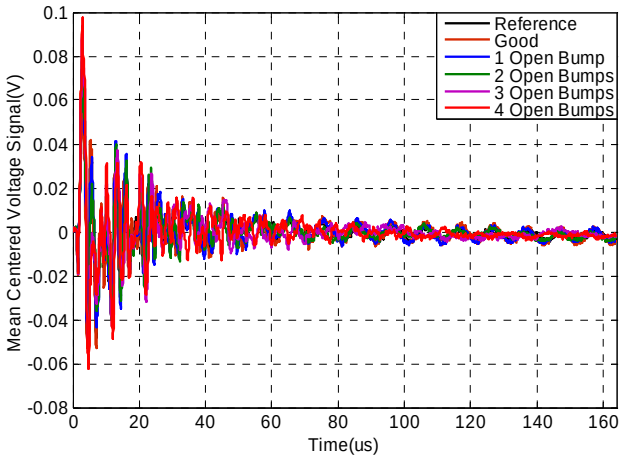
Where, i is the order of the time segment.

Meanwhile, the cross-correlation and modified LTC at time t are still defined in the same format as Equations 4-11 and 4-13.

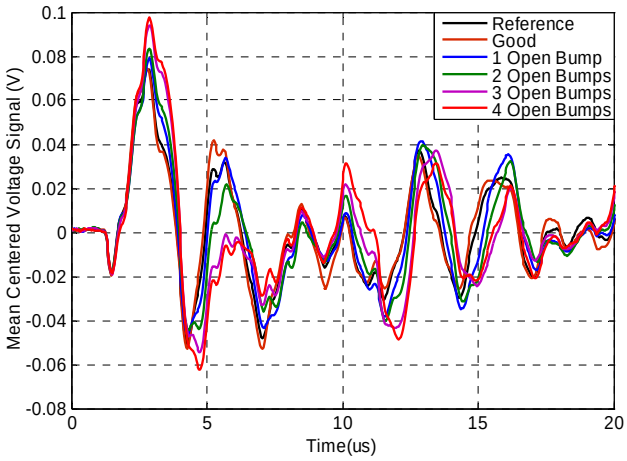
4.2.2 Application of Local Temporal Coherence Analysis to Tin-Lead Flip Chip Test Vehicle

4.2.2.1 Time and frequency domain analyses of laser ultrasound signals

Figure 4-17 (a) shows the time-domain responses of tin-lead flip chips #1 to 6 at the same inspection point #36, with the whole measurement interval being 164 μs. Figure 4-17 (b) and (c) show the response segments in the intervals of [0-20] μs and [100-164] μs, separately. These figures show the transient out-of-plane displacement responses of flip chips with one to four open solder bumps in comparison with those of two good chips. It is observed that the waveforms from two good chips matched very well, one of which was selected as the reference. However, the transient signals of chips with open solder bumps differed from the transient signal of the known-good-chip. The more open bumps a chip has, the larger difference is shown in the responses between this chip and the reference. Figure 4-17 (c) shows a large time shift in time-domain responses of chips with three or four open bumps compared to that of the known-good-chip.

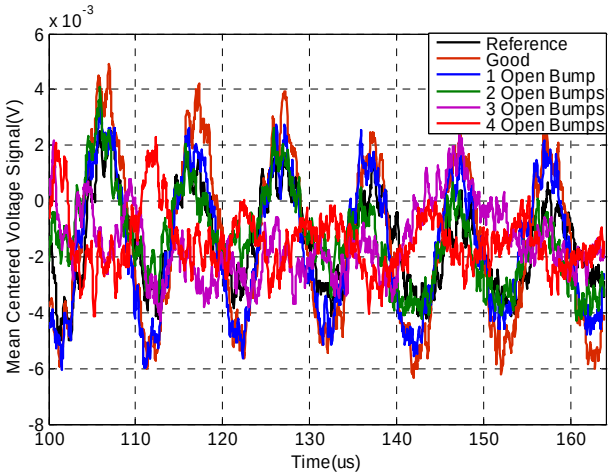


(a)



(b)

Figure 4-17 Time-domain responses of tin-lead flip chips at different intervals: (a) 0-164 μs (b) 0-20 μs (c) 100-164 μs



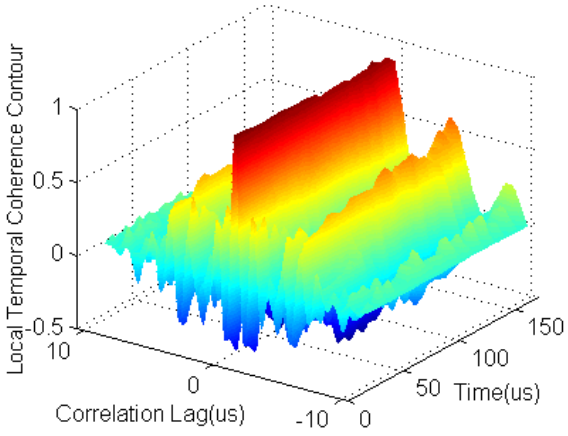
(c)

Figure 4-17 continued

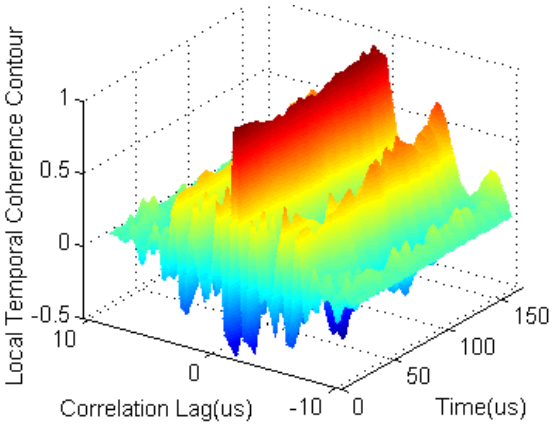
4.2.2.2 LTC results of tin-lead flip chip test vehicle

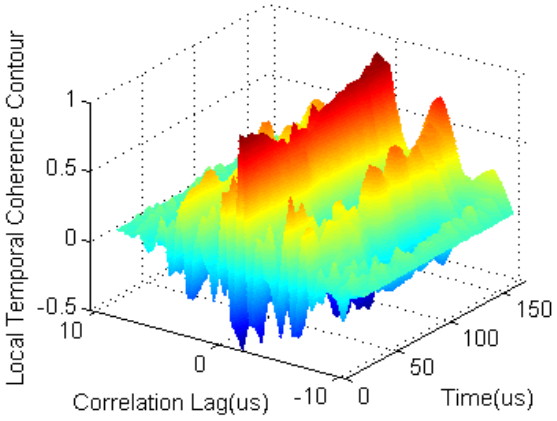
The transient out-of-plane displacement response of electronic packages under pulsed laser loading is intrinsically nonstationary. In order to emphasize the short-time coherence between the nonstationary response signals, local temporal coherence is calculated between measured signals and the reference. The response from good chip #4 is selected as the reference. The window width T_0 is 20.48 μs and the time increment Δt is 5.12 μs, which correspond to 512 and 128 sampling points at the sampling rate of 25 MHz. The LTC contours with parameters of time t and correlation lag τ are shown in Figure 4-18 for the good chip and chips with open bumps, compared to the reference. The effect of open bumps on signal coherence is clearly shown in Figure 4-18. For a good chip, a clear ridge with a value being close to 1 is observed in Figure 4-18 (a) when the correlation lag τ is equal or close to 0, which demonstrates a high coherence in the responses between the known-good-chip and the reference. As the number of open

bumps increases, Figure 4-18 (b)-(e) show that the ridges become blurry and the coherences in the responses between the defective chips and the reference become lower and lower.



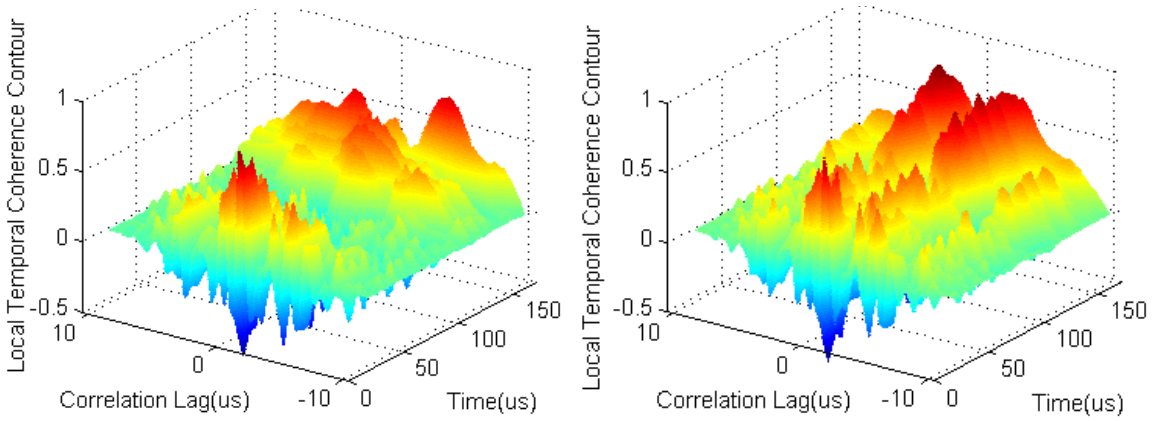
(a)





(b) (c)

Figure 4-18 Local temporal coherence contours: (a) good flip chip (b) chip with 1 open bump (c) chip with 2 open bumps (d) chip with 3 open bumps (e) chip with 4 open bumps



(d) (e)

Figure 4-18 continued

In the following analysis, the correlation lag τ is set to be 0 in Equation 4-12 and only the instantaneous comparison between the measured signal and the reference is considered. The window width T_0 is 20.48 μs, and the time increment Δt is 5.12 μs, which correspond to 512 and 128 sampling points separately at the sampling rate of 25 MHz. The LTC values are calculated between the responses of good chip, chips with open bumps, and the reference for 48 inspection points on the tin-lead test vehicle. The mean of LTC values at different time t is shown in Figure 4-19. It is observed that the LTC changes with time, and Figure 4-19 demonstrates clearly the nonstationary characteristics of the transient out-of-plane displacement responses. There is a high coherence in the signals between the good chip and the reference with time, while the coherence in signals between the chips with open bumps and the reference decreases much faster with time. The more open bumps one chip has, the less coherence is there in the signals between this chip and the reference. Therefore, Figure 4-19 demonstrates the effect of open bump defects on LTC. It is also observed that the SNR ratio of the

transient out-of-plane displacement responses decreases with time, since the LTC in signals between the good chip and the reference decreases slowly with time. By modifying the parameters of window length T_0 and the time increment Δt, the mean values of LTC are recalculated and shown in Figure 4-20. A window length of 10.24 μs and a time increment of 5.12 μs are used to calculate LTC between signals and shown in Figure 4-20 (a), while a window length of 20.48 μs and a time increment of 10.24 μs are used to calculate LTC and shown in Figure 4-20 (b). It reveals that LTC values show more variation with time in Figure 4-20 (a) compared to Figure 4-19, since the window length is reduced in the former. A similar trend of LTC with time is revealed in Figure 4-20 (b) compared to Figure 4-19, although some local information is lost by reducing calculation points. However, Figure 4-19 and Figure 4-20 both show the same trend of LTC values with time. Without losing accuracy, a window width T_0 of 20.48 μs and a time increment Δt of 5.12 μs are selected and used in the following LTC and MLTC analyses.

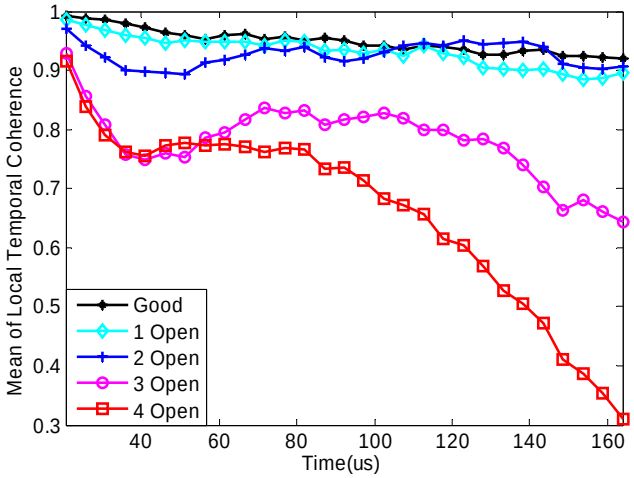


Figure 4-19 Mean of local temporal coherence of tin-lead flip chips with open bumps (window width = 20.48 μs and time increment = 5.12 μs)

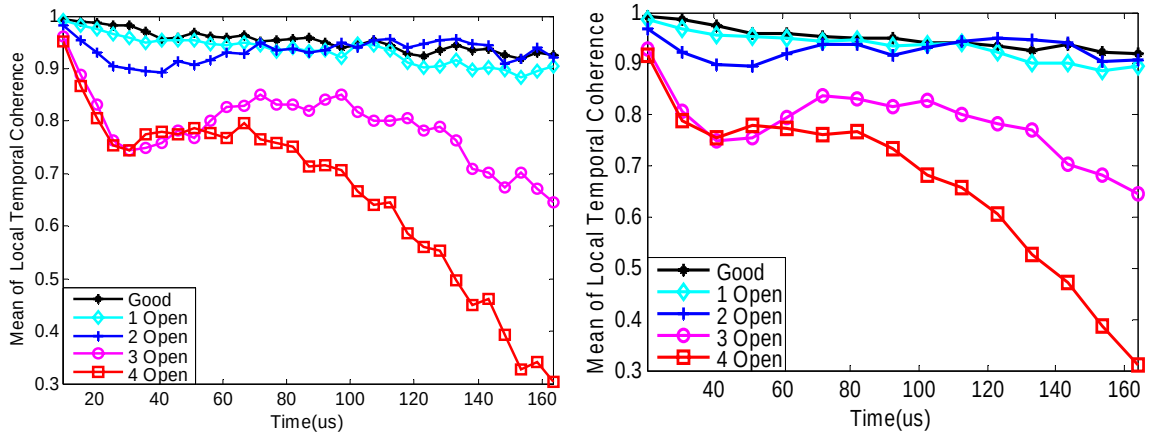


Figure 4-20 Mean of local temporal coherence of tin-lead flip chips with open bumps: (a) (window width = 10.24 μs and time increment = 5.12 μs) (b) (window width = 20.48 μs and time increment = 10.24 μs)

The local temporal coherences in the responses between the good chip, defective chips and the reference at inspection point #36 are shown in Figure 4-21 and it is shown that there is less coherence in the responses between the defective chips and the reference. Point #36 is just where the open bump starts for all defective chips (as shown in Figure 3-15), and the effect of open bump defects on displacement response is shown clearly in Figure 4-21 with LTC analysis. It is observed in Figure 4-21 that LTC values between the chips with three or four open bumps and the reference are negative in some time intervals, indicating that the time-domain signals of chips with three or four open bumps and that of the reference are out of phase by over 90 degrees. It corresponds to the large shift in time-domain signals of the chips with three or four open bumps compared to the reference, as shown in Figure 4-17.

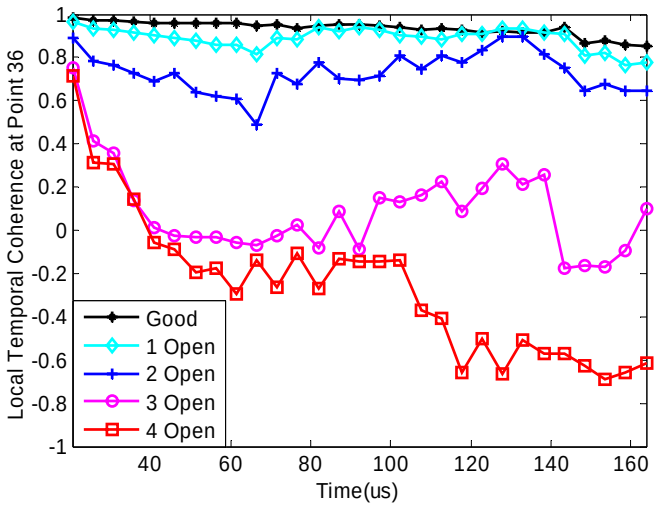
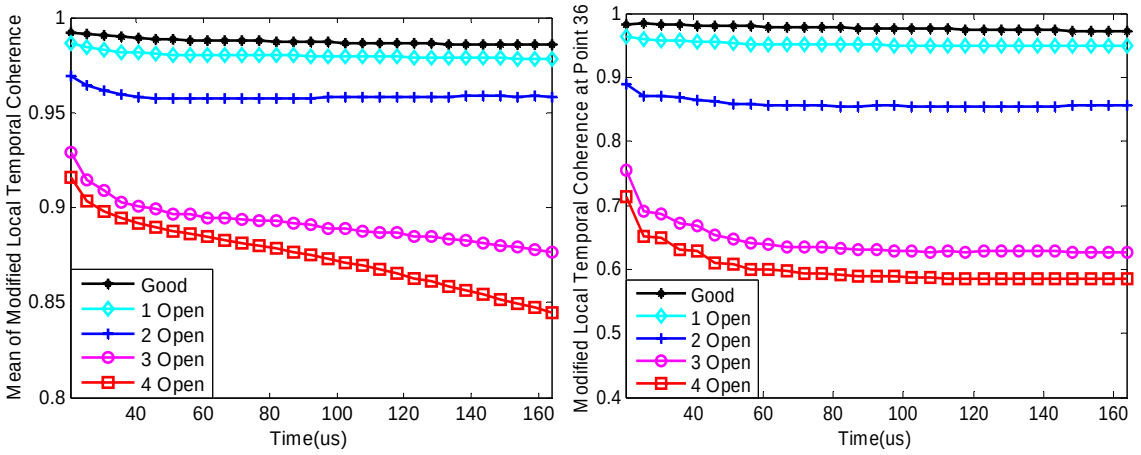


Figure 4-21 LTC values of tin-lead flip chips with open bumps at inspection point #36

4.2.2.3 MLTC results of tin-lead flip chip test vehicle

The similarity in laser ultrasound signals of tin-lead flip chip samples has been estimated with LTC analysis, which uses a fixed-length windowing function in previous section. From Figure 4-19 to Figure 4-21, the LTC demonstrates large variation with time and the difference in LTC between flip chips with one or two open bumps and the reference is small, making it difficult to distinguish the chips with one or two open bumps from the good chip with LTC analysis. In order to analyze the trend of coherence evolution between signals over time, the MLTC is estimated whose windowing size increases linearly with the time increment Δt. Since the rectangular windowing function works as a smoothing filter, the MLTC acts as even more of a smoothing filter with the increase of window length. In MLTC analysis, the time increment T_0 is 5.12 μs, which corresponds to 128 sampling points at the sampling rate of 25 MHz, and the window size increases linearly with the time increment Δt. The MLTC values are calculated between the responses of the good chip, defective chips, and that of the reference for 48 inspection

points. The mean of MLTC values at different time t is shown in Figure 4-22 (a). Figure 4-22 (b) shows the MLTC in the responses between the good chip, defective chips, and the reference at inspection point #36. The difference in MLTC values between the chips with one or two open bumps and the reference can be clearly distinguished, as shown in Figure 4-22.



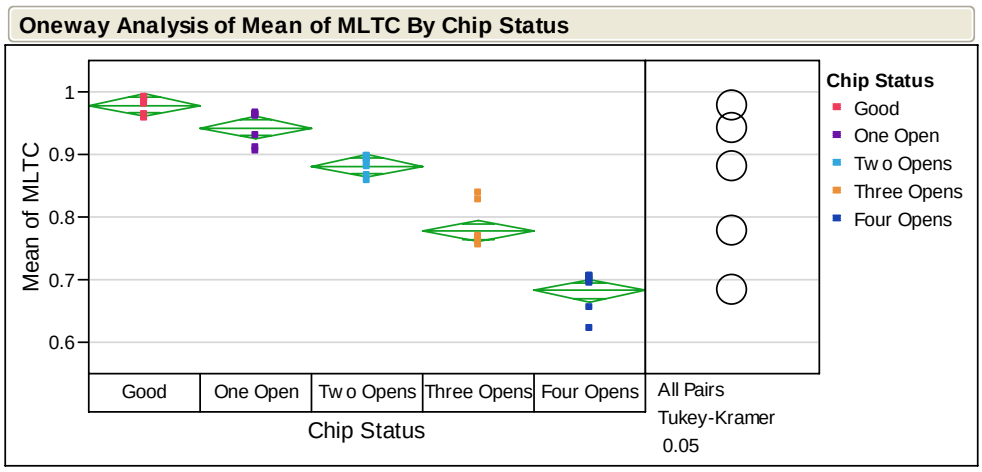
(a) (b)

Figure 4-22 (a) Mean values of MLTC (b) MLTC at inspection point #36 for tin-lead flip chips with open bumps

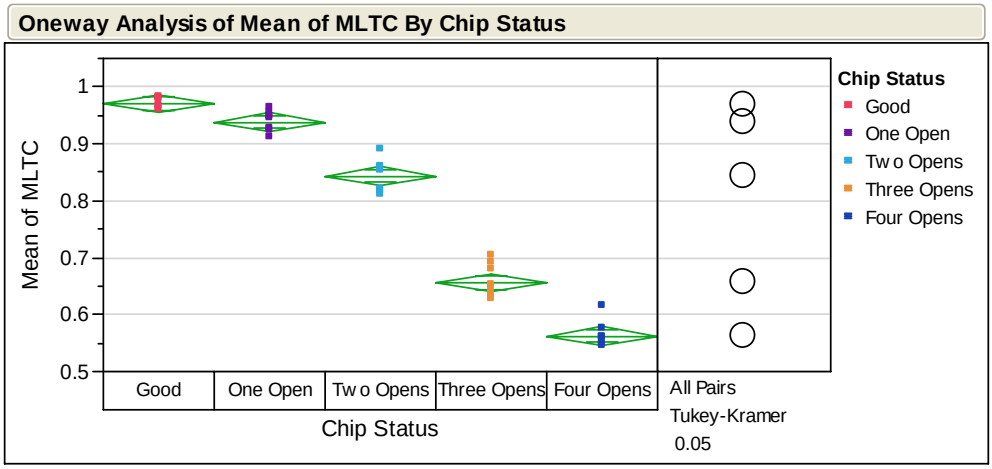
4.2.2.4 Statistical analysis of MLTC results of tin-lead flip chip test vehicle

Since open bumps start from the left top corner (specifically from bump #36) as shown in Figure 3-15, the largest difference in captured laser ultrasound signals between the defective chips and known-good-chip (reference) is observed at point #36. Therefore, inspection point #36 is most sensitive among the forty-eight inspection points selected directly on solder bumps. In order to study the system capability statistically, eight test vehicles with flip chips having the same defect pattern (open bump defects as shown in

Figure 3-15) were tested using laser ultrasound-interferometric inspection system. The laser ultrasound signals from these samples were analyzed with the MLTC method. The MLTC values of inspection point #36 at two typical sampling times - sampling start time (time = 0 μs) and sampling end time (time = 164 μs), are shown in Figure 4-23 (a) and (b) separately. The decreasing trend of coherence between the defective chips and good chip can be clearly observed with increasing number of open bumps for all the test vehicles. The Tukey (or Tukey-Kramer) multiple comparison test was applied to the MLTC values to determine whether the mean values are statistically distinct among the chips with different number of open bumps. The Tukey test is a single-step multiple comparison procedure which is applied simultaneously to the set of all pairwise comparisons. It is a statistical test generally used in conjunction with an ANOVA to find which mean values are significantly different from the other ones. It compares all possible pairs of mean values, and is based on a studentized distribution. [wikipedia, June 2008]. The one-way ANOVA analysis of MLTC values is shown in right columns of Figure 4-23 (a) and (b). In this analysis, the Tukey multiple comparison test at the statistical significance level α of 0.05 is used. The circles in the columns stand for clusters of testing values of flip chip samples with different number of open bumps (from good chip to a chip with four open bumps). By following Tukey multiple comparison hypothesis judgment, the hypothesis that the mean values are distinct is verified. Therefore, chips with one to four open bumps can be statistically distinguished from good chip and among themselves at the confidence level 95%.



(a)



(b)

Figure 4-23 One-way ANOVA analysis of MLTC values of eight tin-lead test vehicles at two different times: (a) analysis of MLTC values at sampling start time (time = 0 μs) (b) analysis of MLTC values at sampling end time (time = 164 μs)

In the Tukey multiple comparison test, levels are used to stand for different conditions of samples (from good chip to chip with four open bumps). The mean comparisons between these levels with Tukey multiple comparison test at two different sampling times (sampling start time and end time) are summarized in Table 4-3 and Table 4-4 separately. From Table 4-3 and Table 4-4, it is also shown that the flip chip

samples with one to four open bumps can be statistically distinguished from good chip and among themselves at the confidence level 95%.

Table 4-3 Mean comparisons between different levels at sampling start time

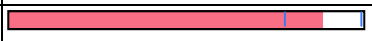
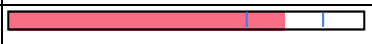
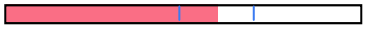
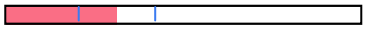
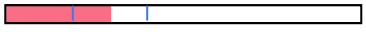
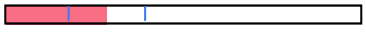
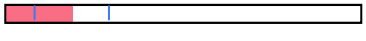
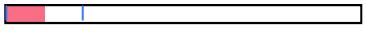
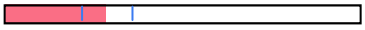
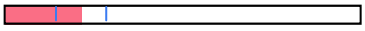
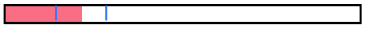
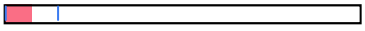
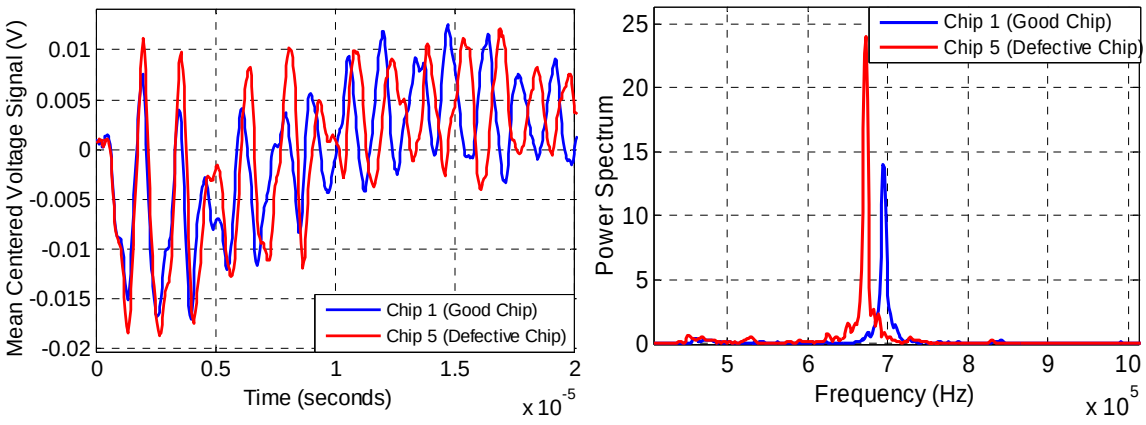
Level	- Level	Difference	Lower CL	Upper CL	Difference
Good	Four Opens	0.2956763	0.2601249	0.3312276	
One Open	Four Opens	0.2598538	0.2243024	0.2954051	
Good	Three Opens	0.2011350	0.1655837	0.2366863	
Two Opens	Four Opens	0.1982263	0.1626749	0.2337776	
One Open	Three Opens	0.1653125	0.1297612	0.2008638	
Two Opens	Three Opens	0.1036850	0.0681337	0.1392363	
Good	Two Opens	0.0974500	0.0618987	0.1330013	
Three Opens	Four Opens	0.0945413	0.0589899	0.1300926	
One Open	Two Opens	0.0616275	0.0260762	0.0971788	
Good	One Open	0.0358225	0.0002712	0.0713738	

Table 4-4 Mean comparisons between different levels at sampling end time

Level	- Level	Difference	Lower CL	Upper CL	Difference
Good	Four Opens	0.4078775	0.3758220	0.4399330	
One Open	Four Opens	0.3755862	0.3435307	0.4076418	
Good	Three Opens	0.3138187	0.2817632	0.3458743	
One Open	Three Opens	0.2815275	0.2494720	0.3135830	
Two Opens	Four Opens	0.2812875	0.2492320	0.3133430	
Two Opens	Three Opens	0.1872287	0.1551732	0.2192843	
Good	Two Opens	0.1265900	0.0945345	0.1586455	
One Open	Two Opens	0.0942988	0.0622432	0.1263543	
Three Opens	Four Opens	0.0940587	0.0620032	0.1261143	
Good	One Open	0.0322913	0.0002357	0.0643468	

4.2.3 MLTC Results of Lead-Free Flip Chip Test Vehicle

The above analyses considered tin-lead test vehicles, on which the flip chip packages were made from eutectic tin-lead solder bumps. On lead-free test vehicles (“SiMAF” flip chips, Siemens AG), solder bumps were made with lead-free materials (Sn/Ag/Cu). On one lead-free test vehicle, chips 1, 3, and 4 are good chips and chips 5 to 10 are defective ones that have various manufacturing defects. Chip 1 is selected as the reference. The time-domain signals and corresponding power spectrums of chip 1 (good chip) and chip 5 (defective chip) are shown in Figure 4-24 (a) and (b). It is observed from Figure 4-24 (b) that there is an obvious frequency shift backward for the defective chip compared to the good one and the dominant signal component lies in the frequency range from 600 KHz to 750 KHz.



(a) (b)

Figure 4-24 (a) Time-domain signals and (b) power spectrums of lead-free flip chip #1 (good chip) and chip #5 (defective chip)

Following the same analysis procedure as applied to tin-lead test vehicles, the mean values of MLTC analysis are calculated and shown in Figure 4-25. It is clearly shown that the difference in MLTC between the defective chips and the good ones can be clearly distinguished. A small difference in MLTC values between two good lead-free flip chips is observed in Figure 4-25 and it is thought that this difference comes from the variation during the manufacturing process of flip chip samples. Since there is a large threshold between defective flip chips and good chips, the effect of this difference on inspection capability could be omitted.

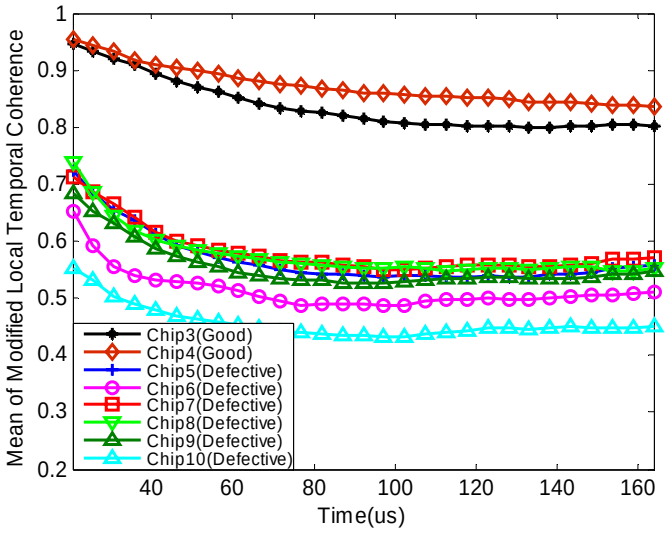
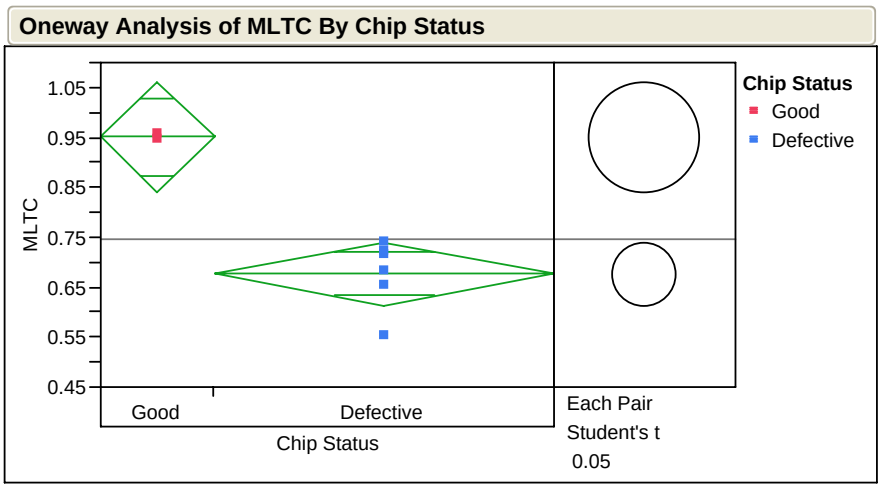
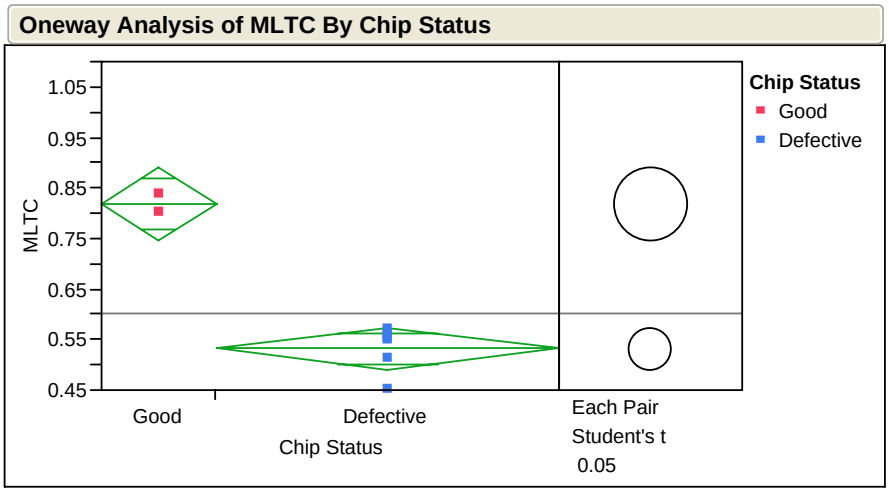


Figure 4-25 Mean values of MLTC of lead-free flip chips

Since there is only one individual comparison required, the Student's t-test was applied to the MLTC values of lead-free flip chips to determine whether the mean values are statistically distinct between defective flip chips and good chips. The mean comparisons between the defective and good flip chips at sampling start time (time = 0 μs) and sampling end time (time = 164 μs) are shown in Figure 4-26. The one-way ANOVA analysis of MLTC values using t-test at the statistical significance level α of 0.05 is shown in right columns of Figure 4-26 (a) and (b). The circles in the columns stand for clusters of testing values from the defective and good flip chips. By following t-test hypothesis judgment, the hypothesis that the mean values are distinct is verified since there are no intersections between the circles. Therefore, defective lead-free flip chips can be statistically distinguished from good chips with MLTC analysis at the confidence level 95%.



(a)



(b)

Figure 4-26 One-way ANOVA analysis of MLTC values of lead-free test vehicles at two different times: (a) analysis of MLTC values at sampling start time (time = 0 μs) (b) analysis of MLTC values at sampling end time (time = 164 μs)

4.2.4 Summary of Local Temporal Coherence Analysis of Laser Ultrasound Signals

These results demonstrate the application of local temporal coherence and modified LTC analyses for detecting solder bump defects in flip chip packages using the laser ultrasound-interferometric technique. The local temporal coherence analysis

provides a quantitative measure of the relative change in waveform shapes as a function of time when comparing samples. The LTC and MLTC analyses increase the measurement accuracy and sensitivity compared to the correlation coefficient method because they have the ability to process nonstationary laser ultrasound signals, while correlation coefficient does not.

4.3 Cross-Examination and Validation of Laser Ultrasound Inspection Results of Flip Chip Test Vehicles with X-ray, CSAM, Dye/Peel and Cross-Section Techniques

Laser ultrasound inspection results of flip chip test vehicles, including tin-lead flip chip test vehicles with open bump defects and lead-free flip chip test vehicles with various manufacturing defects, were cross examined with X-ray and CSAM techniques and validated through destructive dye/peel and cross-section observations. X-ray and SAM, which are two known nondestructive techniques, are used to assess solder bump failures as cross-examination and compared to laser ultrasound-interferometric technique.

4.3.1 X-ray Results of Flip Chip Test Vehicles

4.3.1.1 2-D X-ray results of tin-lead flip chip test vehicle

One method for assessing potential incipient failures of solder bumps in electronic packages is X-ray technique. In the 2-D X-ray technique, top-down images are captured using a Fein Focus® X-Ray system, which offers detection capability in the micrometer scale. Figure 4-27 (a) through (e) show X-ray images of good flip chip and chips with one to four open bumps separately. In Figure 4-27, the black circles are top-down images of solder bumps obtained with X-ray. Almost no difference is revealed in Figure 4-27 (b)

through (e) compared to Figure 4-27 (a); therefore, no open defects are observed using 2-D X-ray imaging. The reason why 2-D X-ray imaging cannot reveal open defects lies in the fact that X-ray operates in a through-transmission mode and its operation is based on the differences in materials' density. Two-dimensional X-ray provides a composite image of the entire sample thickness. Therefore, it cannot easily provide information about a specific layer in electronic packages. For this case, the open layer between the solder bump and substrate is too small compared to the standoff of the solder bump, and the small open layer can hardly cause material density differences in X-ray testing. Therefore, no open defect has been identified with 2-D X-ray imaging.

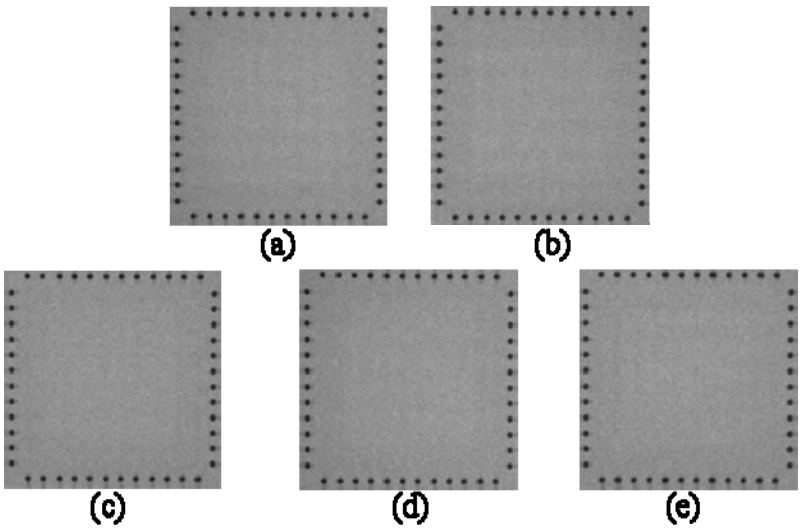
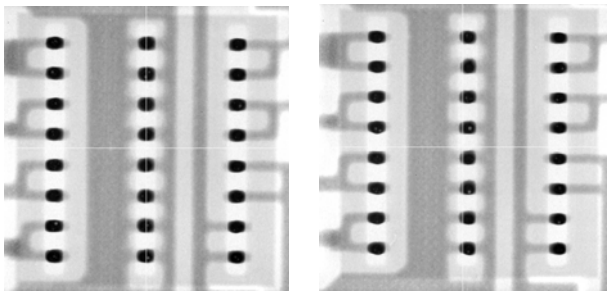


Figure 4-27 Top-down X-ray images of tin-lead flip chips: (a) good chip (b) chip with 1 open bump (c) chip with 2 open bumps (d) chip with 3 open bumps (e) (d) chip with 4 open bumps

4.3.1.2 2-D X-ray results of lead-free flip chip test vehicle

Two-dimensional X-ray images of "SiMAF" flip chips were captured using a Phoenix PCBA Analyzer® X-ray imaging system, which offers detection capability in the

micrometer scale. This X-ray imaging system has a beam diameter of 0.9 um and its overall resolution is 8 um. Figure 4-28 (a) and (b) are X-ray images of good chip 1 and defective chip 5 separately, and the black circles are top-down images of solder bumps in Figure 4-28. Almost no difference can be observed in Figure 4-28 (b) compared to Figure 4-28 (a); therefore, no open defect has been detectable using 2-D X-ray imaging.



(a) (b)

Figure 4-28 Top-down X-ray images of lead-free flip chips: (a) good chip (b) chip with manufacturing defects

4.3.2 CSAM Results of Flip Chip Test Vehicles

Scanning acoustic microscopy utilizes a piezoelectric crystal oscillator to produce a high-frequency sound wave to interact with the devices to detect internal defects, such as cracks, voids and interfacial delaminations. The widely used C-mode SAM (CSAM) acquires the pulse echo signals reflected from a specified interface or layer over the entire scanning area and converts their amplitude into an image. The raw time-domain ultrasonic signal and CSAM image of a good flip chip at the die-bump layer are shown in Figure 4-29 using the Sonix® UHR-2001 SAM system with a 110-MHz

ultrasonic transducer. The 48 solder bumps are shown in black on the periphery of the package in Figure 4-29.

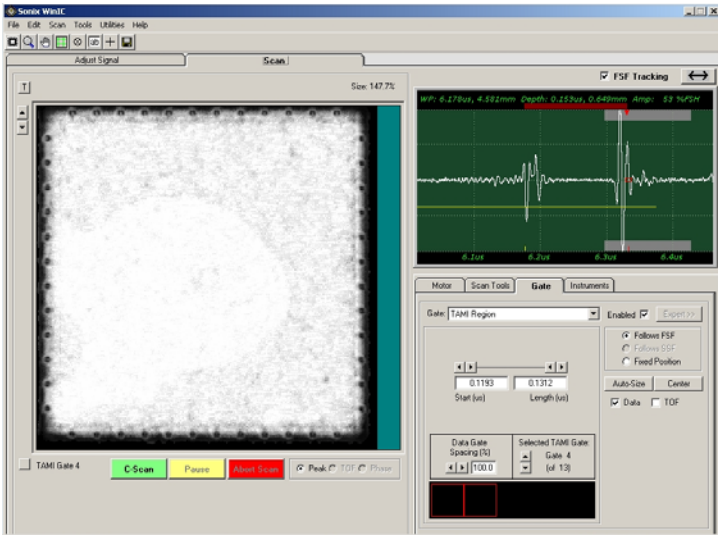


Figure 4-29 Ultrasonic signal and CSAM image of tin-lead flip chip at die-bump interface

The CSAM pictures shown in Figure 4-30 (a) through (e') were taken at two adjacent scanning layers of the good flip chip and chips with one to four open bumps. The white circles represent solder bumps in these pictures. Figure 4-30 (a) and (a') show CSAM images of the good chip at two adjacent scanning layers (Figure 4-30 (a) is the image obtained when the SAM is focused at the solder/copper pad interface, while Figure 4-30 (a') is obtained when the SAM system is focused on solder/FR-4 substrate interface), and no difference is observed between them. In Figure 4-30 (b), one white circle is observed to be missing at the top left corner compared to Figure 4-30 (b'), which indicates that the copper pad layer is missing at this position, where one open bump exists. The rest of the figures can be analyzed by analogy to see the effect of removing copper pads. Solder bumps are not completely distinguishable in CSAM images because

of the edge effect of CSAM technique since solder bumps lie at the four edges of tin-lead flip chip packages. When part of the acoustic wave is scattered at the edge of the specimen and only part of the signal is reflected, a small portion of the specimen near the edge cannot be clearly inspected. This phenomenon is called edge effect and it is one of the limitations of SAM. The solder bumps lying at the right top corner of flip chip package seem to have open defects in CSAM pictures shown in Figure 4-30 (e) and (e'), however no open bumps could be detected using laser ultrasound technique or validated through cross-section observation. This might be induced by large package warpage at the die corner. Another drawback of SAM is that deionized (DI) water is required to act as a couplant between the ultrasound transducer and the specimens. Moisture introduced by such couplants as DI water increases warpage of the packages, which is not desirable in microelectronic packaging.

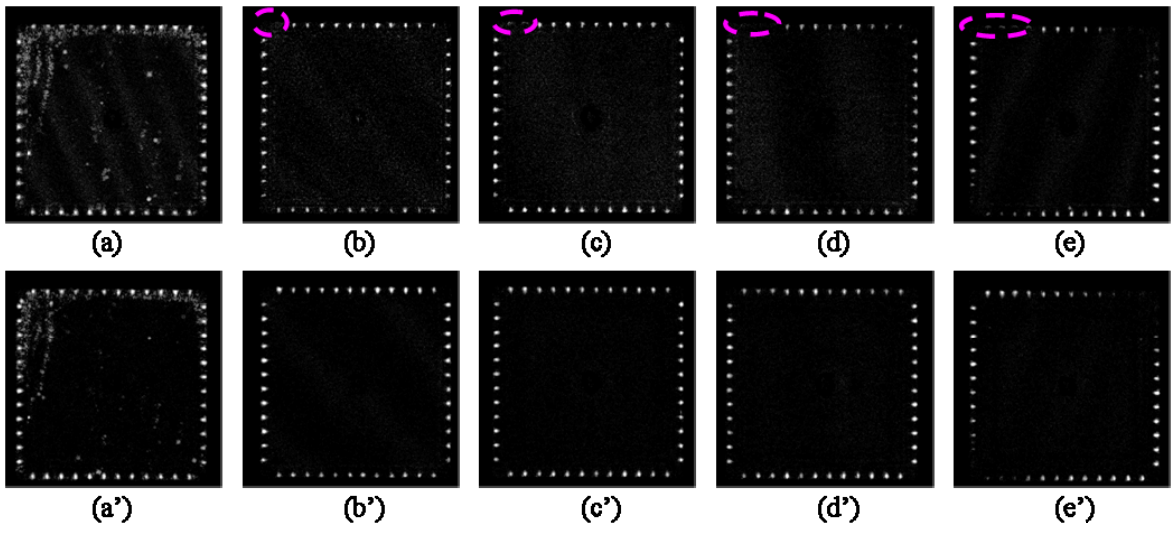


Figure 4-30 CSAM images of tin-lead flip chips at two adjacent layers: (a) and (a') good chip (b) and (b') chip with 1 open bump (c) and (c') chip with 2 open bumps (d) and (d') chip with 3 open bumps (e) and (e') chip with 4 open bumps

The CSAM results of lead-free test vehicle are not included due to the poor quality of CSAM images. We suspect that the poor quality of CSAM images comes from the low reflection of ultrasound signals at the interface of lead-free solder material and ceramic substrate. Note that the tin-lead flip chip test vehicle is made of FR-4 substrates.

4.3.3 Dye/Pull and Cross-Section Results of Flip Chip Test Vehicles

Figure 4-31 shows the destructive dye/pull results of tin-lead flip chip packages with open bumps. Red dye was applied to the chips and it penetrated into the tiny open space between the solder bump and substrate. The die broke away from the substrate when it was pulled using the die pull tool. In Figure 4-31 (a), the shining circles shown in the purple frame are solder bumps left on the substrate after die pull, while the three blurry circles in the green frame were positions where open bumps lay before the die pull. The die broke away from the substrate with the solder bumps being connected to the die at the positions where open bumps lay. Other solder bumps were still connected to the substrate instead of the die after the die pull. Since the rupture always occurs at the weakest interface connecting two different parts, Figure 4-31 verifies the existence of open interconnections between solder bumps and the substrate. Figure 4-31 (b) shows red dye penetration into the open space between the solder bump and the substrate.

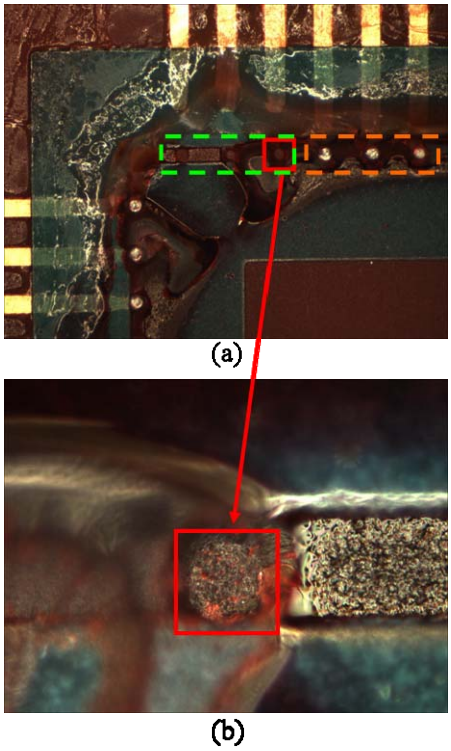


Figure 4-31 Dye/pull images of tin-lead flip chips with open bumps: (a) die pull result (b) red dye penetration into open bump

The cross-section of tin-lead flip chip is shown in Figure 4-32. The removal of copper pad from two solder bumps on the right was clearly observed. These two solder bumps were not firmly connected to the FR-4 substrate by the small spacing (1-2 μms) being left between the solder bump and substrate.

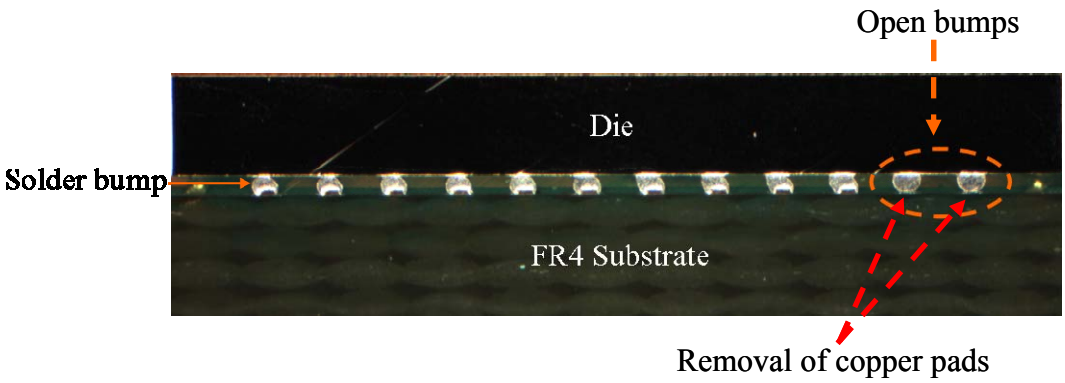


Figure 4-32 Cross-section observation of tin-lead flip chip with microscopy

4.4 Chapter Summary

In summary, new advanced signal processing methods, including wavelet analysis and local temporal coherence analysis have been developed and implemented to analyze the transient out-of-plane displacement responses on the package surface captured by laser ultrasound-interferometric inspection system. These methods are suitable for processing nonstationary laser ultrasound signals and the experimental results demonstrate that they have improved measurement accuracy and sensitivity of inspection system when compared to ER and CC methods. With electronic packages becoming more complex and dense, these advanced signal processing methods make it easier to apply laser ultrasound-interferometric inspection to detecting small defects in high-density and complex packages.

The comparisons between laser ultrasound, X-ray and CSAM results show that the laser ultrasound-interferometric inspection system has advantages in detecting open bump defects in flip chip packages. The 2-D X-ray system was unable to show the presence of open bump(s) or manufacturing defects in both test vehicles. The CSAM

system was able to show the presence of open bump(s) in tin-lead test vehicles, flip chip packages with organic substrate, but failed to show the presence of manufacturing defects in lead-free test vehicles, flip chip packages with ceramic substrates and lead-free solder bumps.

CHAPTER 5

MODAL ANALYSIS OF ELECTRONIC PACKAGES

There are certain mode frequencies and corresponding mode shapes for any given structure, including electronic packages. The electronic package and its solder bump interconnections can be modeled as a plate with spring supports and damping. When defect(s) appear in the solder bump interconnections, the structural characteristics of electronic packages changes and it correspondingly alters the dynamic responses of electronic packages under pulsed laser loading. In this research work, modal analysis is important to correlate solder bump defects with the dynamic response of electronic packages under pulsed laser loading. Intense efforts in analytical and numerical analyses and experimental studies of vibration-induced solder joint/bump failure have been reported in the literature [Bake D.B., (1993), Perkins A., (2004)]. The application of modal analysis for integrity analysis of other types of structure or media, including layered media and thin clamped metallic plates has also been reported [Hirao M. et al., (2004), Servagent N. et al., (1997)]. However, the literature available on how defects affect the dynamic responses and structural characteristics of electronic packages is very limited.

In this work, an integrated analytical, numerical, and experimental modal analyses approach has been developed to predict and explain structural characteristics and the defect effect on the structural characteristics of electronic packages under pulsed laser loading. This integrated method includes: a) an analytical model based on the Power Balance Law to quickly predict the natural frequencies of a given package structure and

examine how they are influenced by the package geometries and solder bump defects; b) a finite element model to extract modes and mode shapes of a given electronic package structure and correlate mode shift and mode shape evolution with solder bump defects; and c) a modal extraction technique from experimental data obtained by using the laser ultrasound-interferometric inspection system. This integrated modal analysis approach has also shown benefits for further signal processing of laser ultrasound signals with wavelet analysis by providing predicted mode frequencies and corresponding mode shapes most sensitive to specific defects.

5.1 Analytical Modal Analysis

5.1.1 Analytical Model Based on Power Balance Law

An analytical model based on the Power Balance Law [Ginsberg J., 2001] is used to predict natural frequencies of flip chip packages and examine how they are affected by solder bump defects. In this work, the following assumptions are made [Zhang et al., 2006].

1. Silicon die is a plate with homogenous material properties.

2. The under bump metallurgy (UBM) is inconsequential to the model and the solder bump is directly attached to the chip.

3. The natural frequencies of the flip chip are sufficiently higher than those of the substrate to prevent coupling since the size of silicon die is much smaller than that of substrate board.

4. All material properties are assumed to be linear elastic.

The silicon die is modeled to be a thin continuous rectangular plate of length a, width b and thickness h. The solder bump is modeled as a massless tension spring. The plate is then partially restrained by these springs and only the flexural motion in the direction perpendicular to the chip surface is considered in this model. Each spring has one end fixed to the plate; while the other end of each spring is fixed to the substrate. A three-dimensional representation is shown in Figure 5-1.

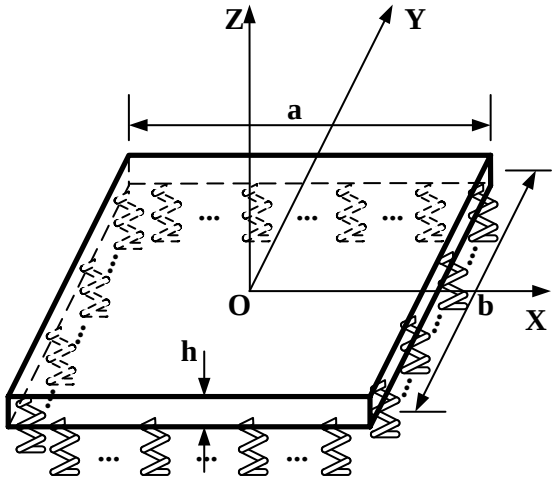


Figure 5-1 3-D model of plate and spring system

As Power Balance Law [Ginsberg J., 2001] states, the rate of change of kinetic energy (T) plus the rate of change of potential energy (U) is equal to zero for a conservative system without external work,

$$\dot{T} + \dot{U} = 0 \tag{5-1}$$

The displacement of the plate $w(x, y, t)$ in the vertical direction is assumed as [Pitarresi J., (2002), Weaver W., (1990), Barber J., (2002)],

$$w(x, y, t) = W(x, y)\sin \omega t \tag{5-2}$$

Where, $W(x, y)$ is the deflection function and ω is natural frequency.

The strains in the thin plate are represented [Weaver W., 1990] by,

$$\varepsilon_x = -z\frac{\partial^2 w}{\partial x^2},\ \varepsilon_y = -z\frac{\partial^2 w}{\partial y^2},\ \gamma_{xy} = -2z\frac{\partial^2 w}{\partial x \partial y} \tag{5-3}$$

Where,

$\varepsilon_x, \varepsilon_y, \gamma_{xy}$: normal and shear strains for a thin plate.

The stresses corresponding to the strain are determined by the following relationships [Weaver W., 1990],

$$\sigma_x = \frac{E}{1-\nu^2}(\varepsilon_x + \nu\varepsilon_y) = -\frac{Ez}{1-\nu^2}(\frac{\partial^2 w}{\partial x^2} + \nu\frac{\partial^2 w}{\partial y^2})$$

$$\sigma_y = \frac{E}{1-\nu^2}(\varepsilon_y + \nu\varepsilon_x) = -\frac{Ez}{1-\nu^2}(\frac{\partial^2 w}{\partial y^2} + \nu\frac{\partial^2 w}{\partial x^2})$$

$$\tau_{xy} = G\gamma_{xy} = -\frac{Ez}{1-\nu^2}\frac{\partial^2 w}{\partial x \partial y} \tag{5-4}$$

Where,

ν: Poisson ratio of silicon,

G : shear modulus of silicon.

The strain potential energy U_p and kinetic energy T of the plate are expressed separately [Pitarresi J., (2002), Weaver W., (1990)] as,

$$U_p = \frac{D}{2}\iint\{(\frac{\partial^2 w}{\partial x^2})^2 + (\frac{\partial^2 w}{\partial y^2})^2 + 2v\frac{\partial^2 w}{\partial x^2}\frac{\partial^2 w}{\partial y^2} + 2(1-v)(\frac{\partial^2 w}{\partial x \partial y})^2\}dxdy \tag{5-5}$$

Where,

D : Flexural rigidity of the plate and $D = Eh^3/[12(1-v^2)]$,

E : Young's modulus of silicon,

h : Thickness of silicon die.

$$T = \frac{\rho h}{2}\omega^2\iint(\frac{\partial^2 w}{\partial x \partial y})^2 dxdy \tag{5-6}$$

Where,

ρ : density of silicon.

The potential energy U_s stored in the boundary springs is written as,

$$U_s = \frac{1}{2}\sum_{i=1}^{N} K_i w(x_i, y_i, t)^2 \tag{5-7}$$

Where,

K_i : stiffness of the i^{th} spring at location (x_i, y_i),

(x_i, y_i) : position of i^{th} spring relative to the center of the plate,

$w(x_i, y_i, t)$: plate displacement at the location of i^{th} spring at time t,

N : number of springs.

The total potential energy of this system is,

$$U = U_p + U_s \tag{5-8}$$

Substituting the equations from Equation 5-2 to 5-8 into Equation 5-1 and after simplification, Equation 5-1 is expressed as,

$$D\int_{-a/2}^{a/2}\int_{-b/2}^{b/2}\left\{\left[\frac{\partial^2 W(x,y)}{\partial x^2}\right]^2 + \left[\frac{\partial^2 W(x,y)}{\partial y^2}\right]^2 + 2\nu\frac{\partial^2 W(x,y)}{\partial x^2}\frac{\partial^2 W(x,y)}{\partial y^2} + 2(1-\nu)\left[\frac{\partial^2 W(x,y)}{\partial x \partial y}\right]^2\right\}dxdy$$
$$+\sum_{i=1}^{N} K_i W^2(x_i, y_i) - \omega^2 \rho h\int_{-a/2}^{a/2}\int_{-b/2}^{b/2} W^2(x,y)dxdy = 0 \tag{5-9}$$

The deflection function can be expressed in the following non-dimensional form using the Rayleigh-Ritz method [Ginsberg J., (2001), Lee C. et al., (2006)],

$$W(\xi,\eta) = \sum_{i=1}^{I}\sum_{j=1}^{J} C_{ij}\phi_i(\xi)\varphi_j(\eta) \tag{5-10}$$

Where,

C_{ij} : undetermined displacement coefficient,

$\phi_i(\xi), \varphi_j(\eta)$: orthogonal functions,

ξ, η : normalized coordinates,

I, J : order of Rayleigh-Ritz series for $\phi_i(\xi)$ and $\varphi_j(\eta)$ separately.

The $\phi_i(\xi)$ and $\varphi_j(\eta)$ can be constructed using the Legendre's orthogonal polynomials [Hoffman J., (2002), Lee C. et al., (2006)],

$$\phi_1(\xi) = \frac{1}{\sqrt{2}},\ \phi_2(\xi) = \frac{\sqrt{6}}{2}\xi$$

For $n \geq 3$,

$$\phi_n(\xi) = \frac{\sqrt{2(2n-1)}}{2}[(2n-3)\times\phi_{n-1}(\xi) - (n-2)\times\phi_{n-2}(\xi)]/(n-1) \tag{5-11}$$

Where,

$\xi = 2x/a, -1 \leq \xi \leq 1$ and $\eta = 2y/b, -1 \leq \eta \leq 1$.

The orthogonal polynomials $\phi_i(\xi)$ ($\varphi_j(\eta)$) satisfies the orthogonal conditions as,

$$\int_{-1}^{1} \phi_n(\xi)\phi_m(\xi)d\xi = \begin{cases} 0 & if\ n \neq m \\ 1 & if\ n = m \end{cases} \tag{5-12}$$

Equation (5-9) is then rewritten as,

$$D\int_{-1}^{1}\int_{-1}^{1}\{(\frac{2}{a})^3(\frac{b}{2})(\frac{\partial^2 W}{\partial\xi^2})^2+(\frac{2}{b})^3(\frac{a}{2})(\frac{\partial^2 W}{\partial\eta^2})^2+2\nu(\frac{4}{ab})(\frac{\partial^2 W}{\partial\xi^2})(\frac{\partial^2 W}{\partial\eta^2})+2(1-\nu)(\frac{4}{ab})(\frac{\partial^2 W}{\partial\xi\partial\eta})\}d\xi d\eta$$
$$+\sum_{i=1}^{N}K_i W^2(\xi_i,\eta_i)-\omega^2\rho h\int_{-1}^{1}\int_{-1}^{1}(\frac{ab}{4})W^2(\xi,\eta)d\xi d\eta=0 \qquad (5\text{-}13)$$

The matrix equations of motion can be derived by substituting Rayleigh-Ritz series into Equation 5-13 and the following eigenvalue problem with respect to the displacement coefficient C_{ij} is derived [Ginsberg J., (2001), Lee C. et al., (2006), Weaver W., (1990)],

$$\left|[K]-\omega^2[M]\right|\{C\}=0 \qquad (5\text{-}14)$$

With $K=K_p+K_s$,

Where,

$\{C\}=$ Displacement coefficient vector,

$[K]=$ Structural stiffness matrix,

$[K_p]=$ Plate stiffness matrix,

$[K_s]=$ Spring stiffness matrix,

$[M]=$ Plate mass matrix.

The elements of plate stiffness matrix are expressed as,

$$[K_p]_{ijmn} = D\{\int_{-1}^{1}(\frac{2}{a})^3 \frac{d^2\phi_i}{d\xi^2}\frac{d^2\phi_m}{d\xi^2}d\xi\int_{-1}^{1}(\frac{b}{2})\varphi_j\varphi_n d\eta + \int_{-1}^{1}(\frac{a}{2})\phi_i\phi_m d\xi\int_{-1}^{1}(\frac{2}{b})^3 \frac{d^2\varphi_j}{d\eta^2}\frac{d^2\varphi_n}{d\eta^2}d\eta$$
$$+\nu\int_{-1}^{1}(\frac{2}{a})\frac{d^2\phi_i}{d\xi^2}\phi_m d\xi\int_{-1}^{1}(\frac{2}{b})\varphi_j\frac{d^2\varphi_n}{d\eta^2}d\eta + \nu\int_{-1}^{1}(\frac{2}{a})\varphi_i\frac{d^2\varphi_m}{d\eta^2}d\eta\int_{-1}^{1}(\frac{2}{b})\frac{d^2\phi_j}{d\xi^2}\phi_n d\xi + 2(1-\nu)$$
$$\int_{-1}^{1}(\frac{2}{a})\frac{d\phi_i}{d\xi}\frac{d\phi_m}{d\xi}d\xi\int_{-1}^{1}(\frac{2}{b})\frac{d\varphi_j}{d\eta}\frac{d\varphi_n}{d\eta}d\eta\} \tag{5-15}$$

The elements of spring stiffness matrix are expressed as,

$$[K_s]_{ijmn} = \sum_{k=1}^{N} K_k\phi_i(\xi_k)\phi_m(\xi_k)\varphi_j(\eta_k)\varphi_n(\eta_k) \tag{5-16}$$

The elements of mass matrix are expressed as,

$$[M]_{ijmn} = \rho h\int_{-1}^{1}\phi_i(\xi)\phi_m(\xi)d\xi\int_{-1}^{1}\varphi_j(\eta)\varphi_n(\eta)d\eta \tag{5-17}$$

Where, $i, m = 1,2,3,...,I;$ and $j, n = 1,2,3,...,J$.

The theoretical model derived above can be used to predict natural frequencies of flip chip packages. With the order of Rayleigh-Ritz series increasing, more modes can be extracted and the calculation accuracy can be improved. In this work, good accuracy is obtained using a 10^{th} Rayleigh-Ritz series.

PB18 is a daisy-chain flip chip with 48 eutectic solder bumps around the perimeter of the packages with twelve bumps located on each edge of the package, as shown in Figure 5-2, where each small circle indicates a solder bump. In a counter-

clockwise direction, all 48 solder bumps are numbered from 1 to 48. The geometric specifications of PB18 flip chip are listed in Table 5-1. The material properties of silicon and eutectic solder (63Sn/37Pb) are listed in Table 5-2. The largest and smallest diameters of solder bump are 190 μm and 112.5 μm reading from the cross-section observations, and the standoff of solder bumps is read as $Std = 116$ μm. Therefore the effective cylindrical radius of solder bump is defined as $R = (190 + 112.5)/4 = 75.625$ μm and the stiffness of solder bump is calculated as $K_i = E_s * \pi * R^2 / Std = 5.2558e^6$ N/m (E_s stands for Young's modulus of solder).

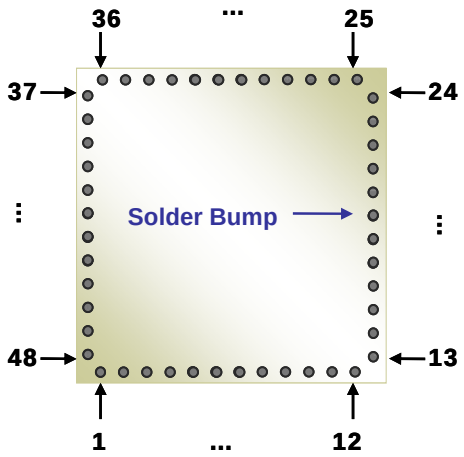


Figure 5-2 Schematic of PB18 flip chip

Table 5-1 Geometric specifications of PB18 flip chip

Die size (a×b)	6.35 mm×6.35 mm
Die thickness (h)	600 μm
Number of bumps (N)	48
Bump diameter	190 μm
Bump height	140 μm
Bump pitch	457 μm

Table 5-2 Material properties of PB18 flip chip

Materials	Young's modulus (GPa)	Density (Kg/m^3)	Poisson ratio
Silicon	112.4	2.33×10^3	0.25
UBM (Al/Cu/Si (98/1/1))	70	2.7×10^3	0.35
Copper pad	110	8.96×10^3	0.34
Solder (63Sn37Pb)	32	8.4×10^3	0.40

The natural frequencies of a good flip chip are calculated from the analytical model and listed in Table 5-3.

Table 5-3 Mode frequencies of good PB18 flip chip from analytical model

Mode	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
Frequency (KHz)	102.54	243.88	358.01	430.73	646.55	737.27	758.24

5.1.2 Effect of Open Bump Defects on Structural Characteristics of Electronic Packages

5.1.2.1 Effect of corner open bump(s) on mode frequency

In order to study the effect of defects on mode frequencies, the flip chip package with open bump defects is also modeled. Four cases are considered here, with one through four adjacent open bumps on the left top corner of flip chip packages.

The natural frequencies of the good chip and these four defective cases are calculated from the analytical modal analysis and listed in Table 5-4. It is seen from Table 5-4 that all natural frequencies shift downward with increasing number of open bumps because the total stiffness decreases when some spring supports are disconnected. In order to compare the relative mode shifts among these modes with increasing number of open bumps, mode shift relative to the good chip for each mode is calculated and shown in Figure 5-3. The frequency shifts of modes 3 and 4 in defective flip chips compared to the good chip are observed to be large. It is shown that mode 4 is more sensitive to one open bump defect; meanwhile, mode 3 is more sensitive to two and more open bump defects. Mode 2 does show large changes for three and four open bumps. The changes are small for the other four modes, which demonstrate that these modes are less sensitive to open bump defects.

Table 5-4 Mode shift of FCPs with open bump defects from analytical model

	Good chip	Chip with one open bump	Chip with two open bumps	Chip with three open bumps	Chip with four open bumps
Mode 1 (KHz)	102.54	102.35	102.34	102.28	101.92
Mode 2 (KHz)	243.88	243.88	243.03	238.38	224.93
Mode 3 (KHz)	358.01	356.09	342.53	311.25	287.79
Mode 4 (KHz)	430.73	423.57	389.60	378.21	376.09
Mode 5 (KHz)	646.55	645.45	642.05	634.86	626.40
Mode 6 (KHz)	737.27	735.94	735.75	734.82	730.64
Mode 7 (KHz)	758.24	757.02	752.16	744.41	742.19

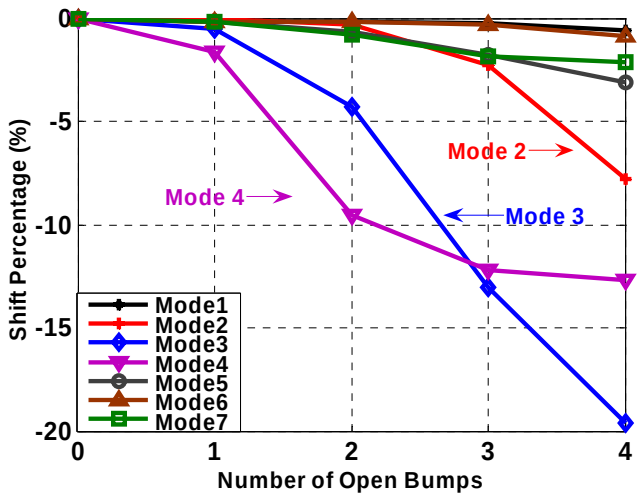


Figure 5-3 Mode shift percentage of defective flip chips relative to good chip from analytical model

5.1.2.2 Effect of open bump locations on mode frequency

It is easy and quickly to examine how open bump locations affect the structural characteristics of electronic packages using the analytical model.

When open bumps appear at the center of top edge instead of top left corner with other parameters being unchanged, natural frequencies of the good chip and chips with one to four open bumps are calculated and listed in Table 5-5. The mode shift relative to the good chip for each mode is shown in Figure 5-4. It is observed that open bump defects at the edge center have a different effect on the mode frequencies, compared to the previous case with open bumps starting from top left corner of the silicon die. In particular, the frequency shift of chips with one to four open bumps for mode 3 is small. This can be roughly explained using the mode shape obtained from the FE modeling, which will be discussed in the next section. The mode shape corresponding to mode 3 has a higher axisymmetry than mode shapes of modes 2 and 4; therefore, open bump defects at or close to the center location have a smaller effect on mode 3 than modes 2 and 4.

Table 5-5 Mode shift of FCPs with open bumps at the center of die edge from analytical model

	Good chip	Chip with one open bump	Chip with two open bumps	Chip with three open bumps	Chip with four open bumps
Mode 1 (KHz)	102.54	102.16	101.51	100.47	98.77
Mode 2 (KHz)	243.88	241.57	237.59	230.57	220.06
Mode 3 (KHz)	358.01	357.82	357.75	354.96	352.59
Mode 4 (KHz)	430.73	421.65	403.83	380.39	355.09
Mode 5 (KHz)	646.55	645.73	645.28	639.19	634.36
Mode 6 (KHz)	737.27	726.89	717.63	714.43	712.08
Mode 7 (KHz)	758.24	756.71	755.96	754.72	753.99

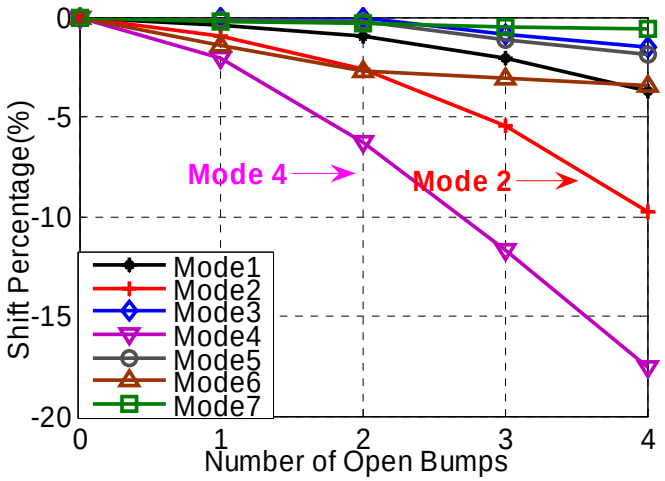


Figure 5-4 Mode shift percentage in analytical model with open bumps at the center of die edge

Another particular case is studied as follows. When four open bumps are lying at each corner of the silicon die, it is estimated that the effect of open bumps on modes is smaller than the previous case with four opens in a row from the die corner since the effect of open defects has been distributed in the previous case. The comparison of natural frequencies between these two cases is listed in Table 5-6 and the results validate the estimation. For the area array packages with more solder bumps, it is estimated that defect effects on mode shift would be decreasing since the system stiffness has increased with more solder bump supports between the silicon die and substrate. In summary, this kind of analytical modeling can provide a direction for experimental data analysis and an quick idea of the defect effect on the system responses of electronic packages under loading.

Table 5-6 Comparison of mode shift for two cases of FCPs with four open bumps

	Good chip	Chip with four corner open bumps in a row	Chip with four open bumps at four corners
Mode 1 (KHz)	102.54	101.92	101.98
Mode 2 (KHz)	243.88	224.93	243.87
Mode 3 (KHz)	358.01	287.79	351.36
Mode 4 (KHz)	430.73	376.09	410.34
Mode 5 (KHz)	646.55	626.40	643.67
Mode 6 (KHz)	737.27	730.64	731.42
Mode 7 (KHz)	758.24	742.19	754.12

5.2 Finite Element Modal Analysis

5.2.1 Finite Element Model

The finite element model chosen here is a 3-D model which can capture the full-field vibration modes and mode shapes of electronic packages. A quarter model can not be used here since the imposed boundary conditions prevent some of the real modes from occurring. In addition, when there are defects in solder bumps, for instance open bump defects, the structure loses its symmetry. All modeling and simulation in this work are done with ANSYS® 11. SOLID45 (as shown in Figure 5-5), which is a 3-D element with 8 nodes, is used in this work to mesh the silicon die, UBM, copper pad and all solder bumps. SOLID45 element has large deflection and strain capabilities [ANSYS® User Manual, 2007]. The element density is higher in the area which contains all solder bumps

and the parts of the plate adjacent to solder bumps, where stress varies much more rapidly.

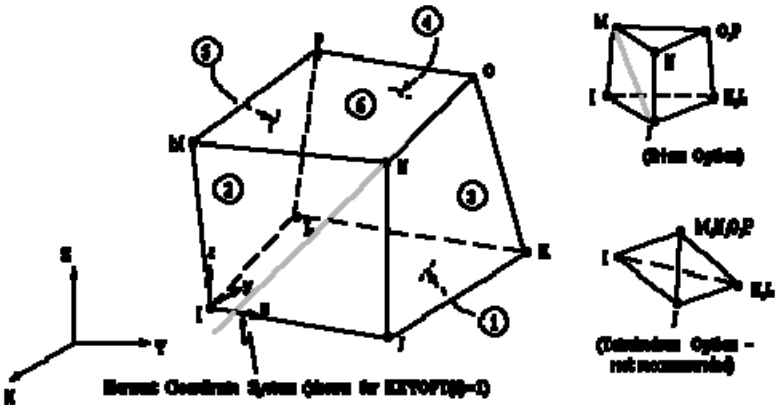


Figure 5-5 3-D structure solid of SOLID45 element [Source: ANSYS® User Manual]

Figure 5-6 shows the meshing of PB18 flip chip with SOLID45 elements. As to the boundary conditions, it is assumed that all solder bumps are fixed at the bottom during the simulation for good FCPs. For FCPs with open bumps, there are no constraints for open bumps as shown in Figure 5-7. The Block Lanczos modal analysis solver is used to calculate the modal parameters. This solver provides a mathematical solution and calculates modes in all six degrees, however only modes and mode shapes moving primarily in the vertical direction are extracted in this work.

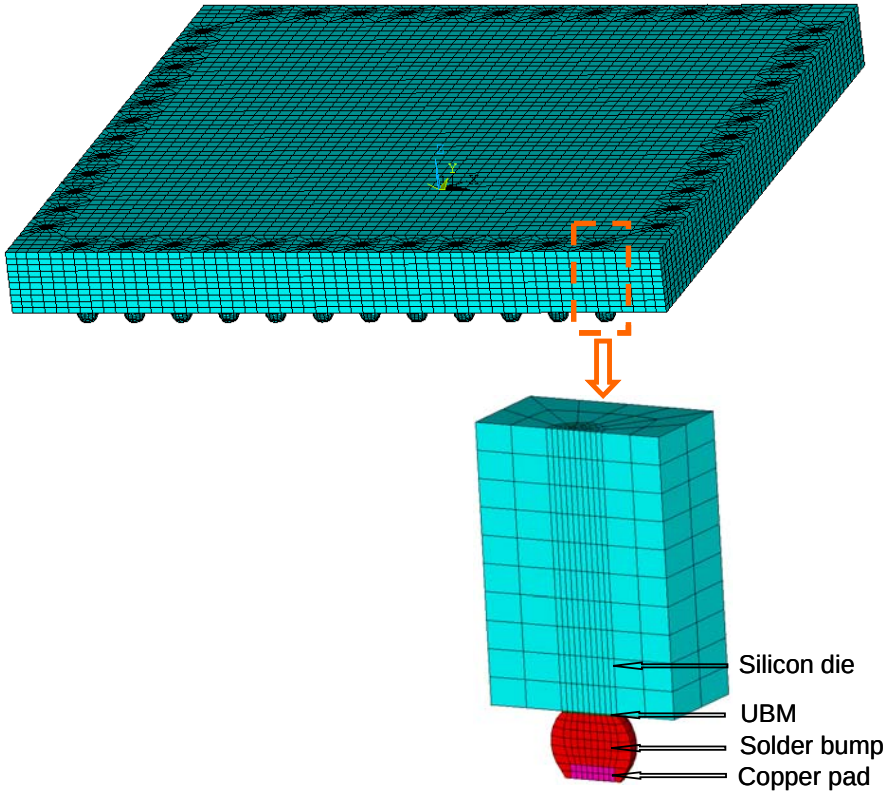


Figure 5-6 3-D finite element model of PB18 flip chip

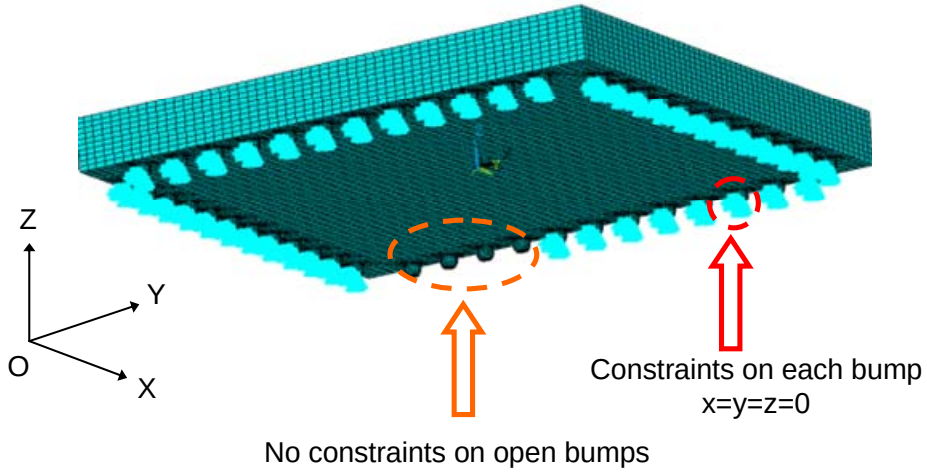


Figure 5-7 Boundary conditions of flip chip with 4 open bumps in FE model

5.2.2 Convergence Study of Finite Element Model

The mode frequencies of an initial coarse model and a refined model are used to determine the convergence of finite element model. The refined model is obtained by increasing division numbers of line elements in the coarse model, thus controlling the number of meshed elements.

The refined meshing has 97408 elements and 109515 nodes in the whole assembly, while there are 80384 elements and 91833 nodes in the coarse model.

The mode frequencies from both the initial model and the refined model are listed in Table 5-7. The percent differences between the refined model and the initial coarse model are listed in the last column of Table 5-7. The frequency difference between the initial coarse model and the refined model ranges from 0.7% to 1.4% for all the modes, which meets the 5%-10% difference requirement and indicates a converged solution.

Table 5-7 Mode frequencies of initial model and refined model

Mode number	Coarse model (KHz)	Refined model (KHz)	Difference (%)
Mode 1	102.91	102.82	-0.9
Mode 2	227.65	227.46	-0.8
Mode 3	319.33	319.01	-1.0
Mode 4	422.63	422.00	-1.4
Mode 5	642.00	641.56	-0.7
Mode 6	723.93	723.33	-0.9
Mode 7	796.10	795.30	-1.0

5.2.3 Mode Analysis

Table 5-8 lists the seven most predominant natural frequencies of a good PB18 flip chip from the analytical and FE models. It is shown that there is a small difference in natural frequencies between the analytical model and FE model. The difference comes from the simplifications made in the analytical model, including simplifications of the package structure. In-plane motion is also omitted in the analytical model.

Table 5-8 Comparison in mode frequencies of good chip from analytical and FE models

Mode	Analytical model	FE model	Difference (%)
Mode 1 (KHz)	102.54	102.82	0.27
Mode 2 (KHz)	243.88	227.46	-6.73
Mode 3 (KHz)	358.01	319.01	-10.89
Mode 4 (KHz)	430.73	422.00	-2.03
Mode 5 (KHz)	646.55	641.56	-0.77
Mode 6 (KHZ)	737.27	723.33	-1.89
Mode 7 (KHz)	758.24	795.30	4.89

In order to study the effect of defects on the natural frequencies, PB18 flip chips with open bump defects are also modeled in FE model. Four identical cases as used in the analytical modal analysis are studied. Similar to the results from the analytical model, all natural frequencies from the FE model decrease with the increasing number of open bumps, which indicates weaker solder bump interconnections caused by open defects. The natural frequencies of a good chip and defective chips are listed in Table 5-9. Figure 5-8 shows a similar shift trend as that from the analytical model. It is observed that open

bump defects play a different role on the frequency shift for each mode. For example, the first dominant mode is not sensitive to open bump defects since there is only a very small frequency shift for this mode with increasing number of corner open bumps, modes 3 and 4 are more sensitive to open bump defects because they exhibit reasonable frequency shifts relative to the natural frequencies of good chip. The mode 4 is particularly sensitive to one open bump defect as shown in Figure 5-8.

Table 5-9 Mode shift with open bump defects from FE model

	Good chip	Chip with one open bump	Chip with two open bumps	Chip with three open bumps	Chip with four open bumps
Mode 1 (KHz)	102.82	102.67	102.58	102.35	101.73
Mode 2 (KHz)	227.46	227.13	225.48	219.27	204.24
Mode 3 (KHz)	319.01	316.00	299.87	273.29	257.61
Mode 4 (KHz)	422.00	394.80	389.20	388.80	388.36
Mode 5 (KHz)	641.56	640.19	638.83	638.14	637.80
Mode 6 (KHz)	723.33	721.39	720.27	716.82	713.60
Mode 7 (KHz)	795.30	792.61	788.15	786.03	785.04

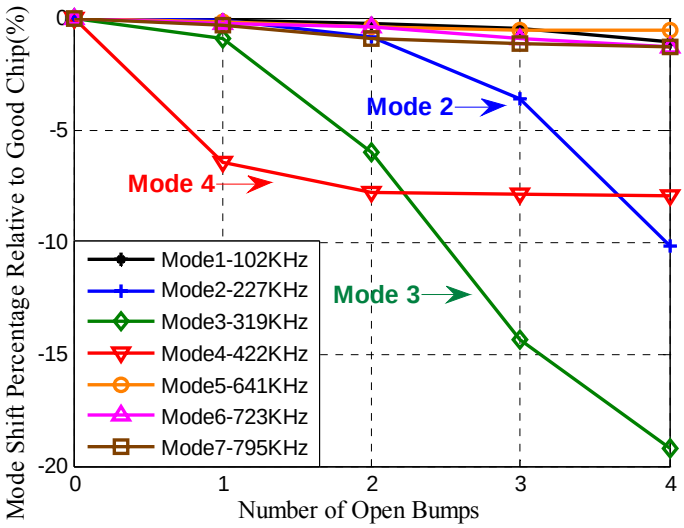


Figure 5-8 Mode shift percentage of defective flip chips relative to good chip from FE model

5.2.4 Mode Shape Analysis

Mode shapes may disclose the differences between good flip chips and defective ones more intuitively than mode shift. Figure 5-9 shows mode shapes corresponding to the seven predominant modes of a good flip chip.

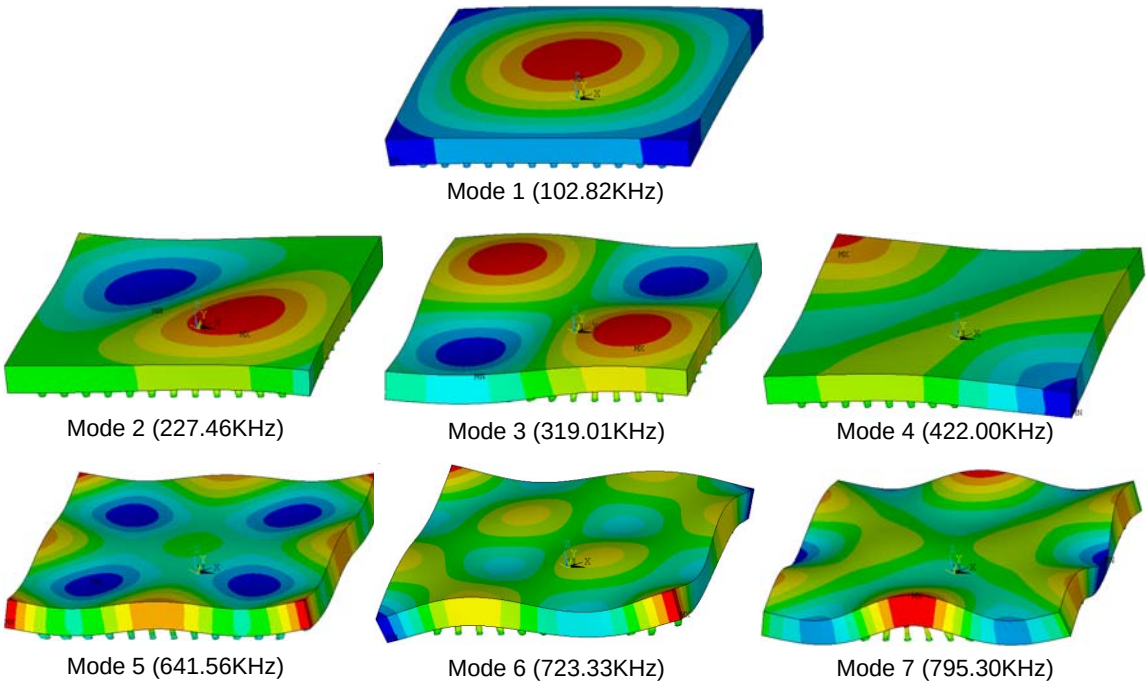
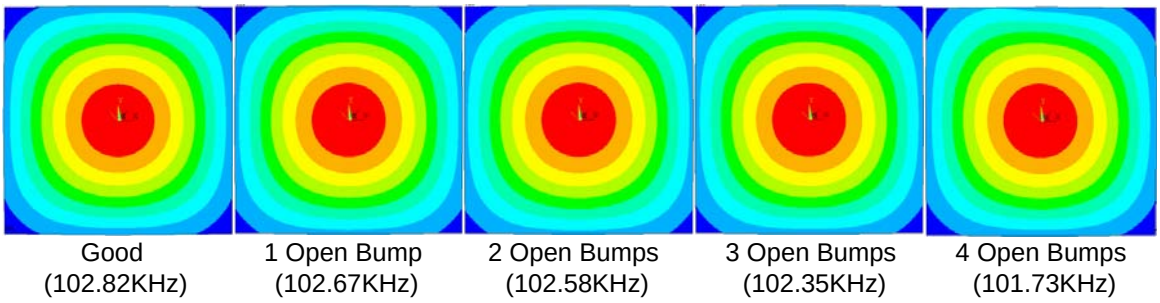
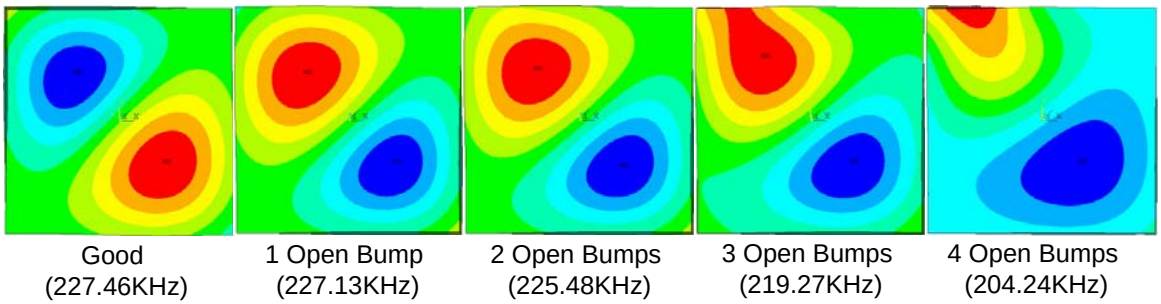


Figure 5-9 Mode shapes of seven predominant modes of good PB18 flip chip

Figure 5-10 shows mode shape evolution from a good chip to a chip with four open bumps for modes 1 to 7. The different effects of open bump defects on the structural characteristics are observed in terms of mode shape evolution with increasing number of open bumps. It is observed that the change of mode shape for mode 1 is small and it demonstrates again that mode 1 is not sensitive to open bump defects at the die corner. For modes 2 to 4, the maximum deformation locations keep moving, approaching the open bump defects as the number of open bumps increases. It indicates that a larger deformation can be detected in the region where open bump defects lie. It is also shown that both mode shift and mode shape evolution are correlated with the severity of open bump defects. The finite element based modal analysis not only indicates the presence of defects, but also helps to locate the defects.



(a)



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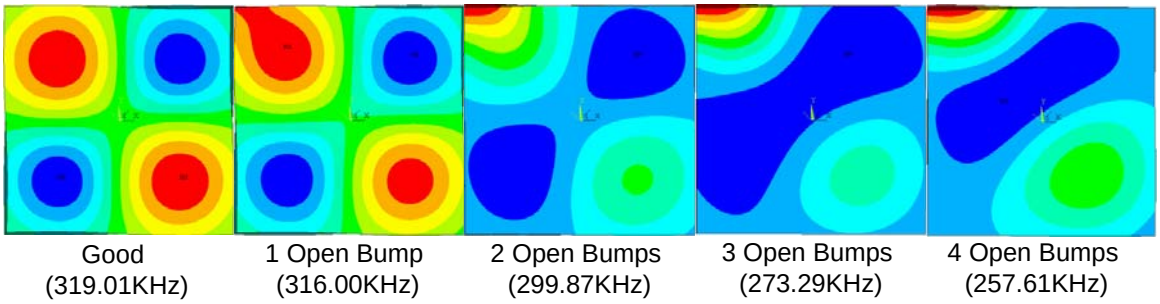

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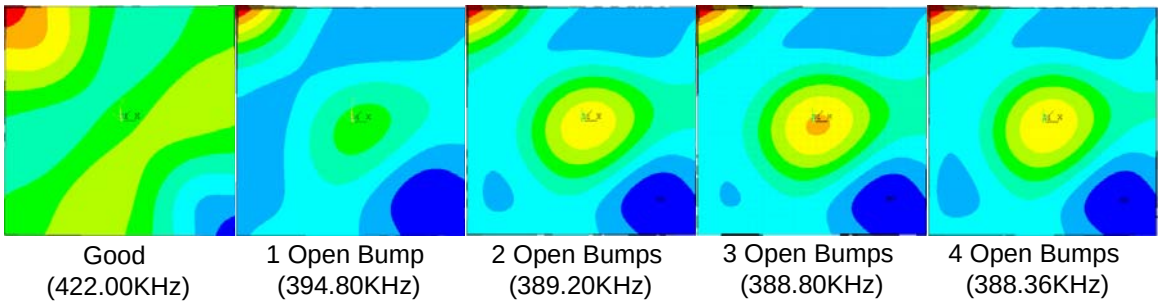
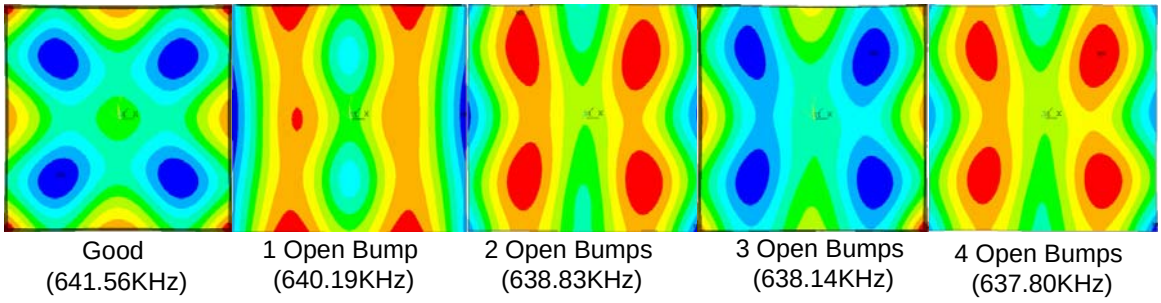
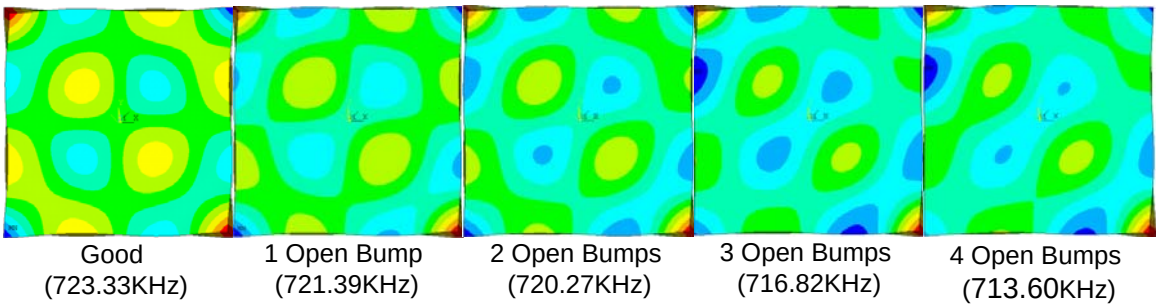


(d)

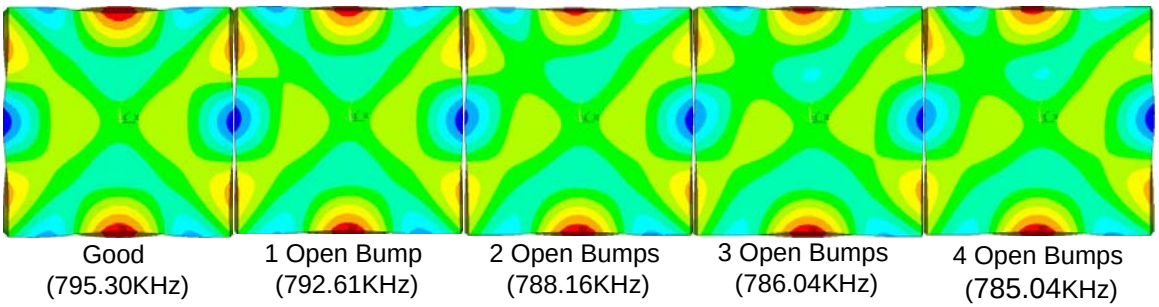
Figure 5-10 Mode shape evolution with increasing number of open bumps: (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7



(e)



(f)



(g)

Figure 5-10 continued

In order to quantify the differences in transient time-domain signals between the electronic packages to be tested and a known-good-package and evaluate the quality of solder bumps, wavelet analysis method was proposed in Chapter 4 for processing the transient out-of-plane displacement responses, which are intrinsically non-stationary. In the discrete wavelet transform, decomposed signal components sensitive to specific

defects can be obtained, and defect features can be extracted to improve measurement sensitivity. These decomposed signal components take up distinct frequency ranges in DWT. With the help of numerical modal analysis with finite element method, the modes sensitive to specific defects and corresponding frequency ranges obtained from experimental data can be estimated before taking any experiments. It can provide a valuable direction for further signal processing of experimental data for defect detection. With the help of this prediction from FE simulation, the decomposed signal components sensitive to defects have been extracted and utilized for wavelet analysis in Chapter 4.1. This demonstrates the value of modal analysis to the signal processing of experimental data.

5.3 Experimental Modal Analysis

Experimental modal analysis of the PB18 tin-lead flip chip test vehicle was performed to validate the analytical and finite element models. The laser ultrasound-interferometric inspection system was used to generate laser pulses to excite the package and collect the transient out-of-plane displacement responses on the package surface. Since the duration of the laser pulse is very short (4-5 nanoseconds) compared to the measurement interval (819.2 microseconds), the laser excitation can be approximated as an impulse load. The power spectrum of transient displacement signals can be directly used to extract the mode frequencies of flip chip packages.

5.3.1 Power Spectrum Analysis of Experimental Data

Figure 5-11 shows the transient time domain responses of flip chips 1 to 6 on the same tin-lead flip chip test vehicle at inspection point #36 during the time interval of [0

20.48] μs. Differences are observed to increase in the time domain responses between the defective chips and the good chip with increasing number of open bumps.

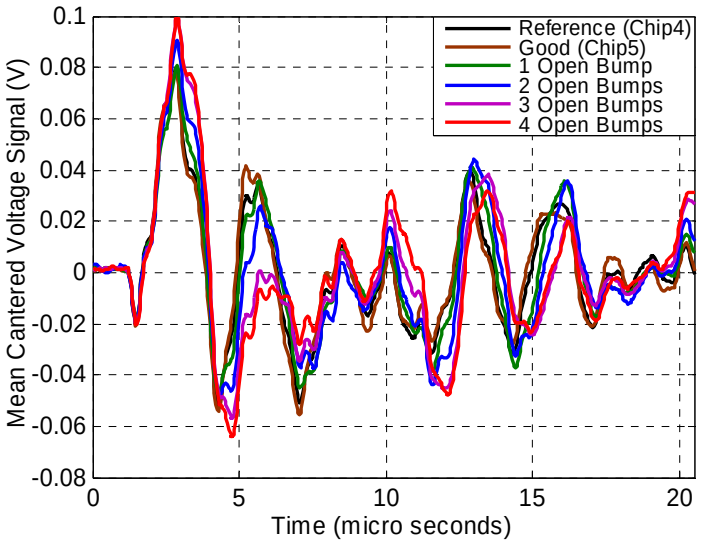


Figure 5-11 Time domain responses of flip chips 1-6 on tin-lead flip chip test vehicle

The corresponding power spectrums of transient time domain signals are shown in Figure 5-12. Figure 5-12 (a) shows the original power spectrum and Figure 5-12 (b) shows the power spectrum ranging from 150 KHz to 350 KHz. The peak natural frequencies are extracted from the power spectrum.

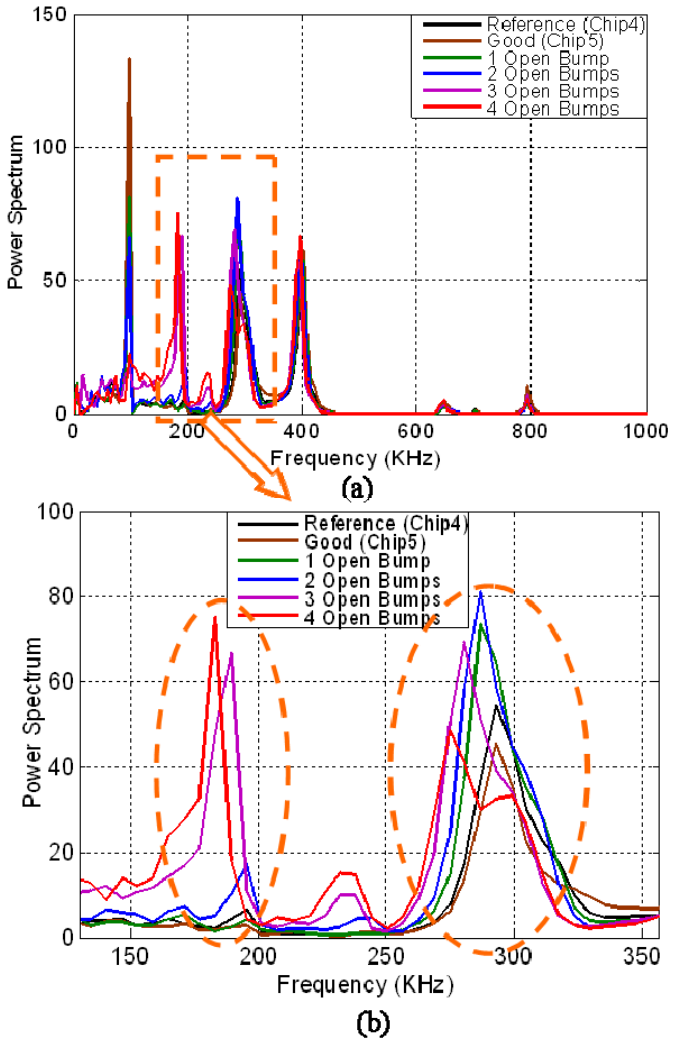


Figure 5-12 Power spectrums of flip chips 1-6: (a) original power spectrum (b) power spectrum ranging from 150 KHz to 350 KHz

The frequency shifts are observed in Figure 5-12 (b) clearly, and they correspond to frequency shifts of modes 2 and 3 extracted from the FE modal analysis. Although there is a small difference in the strength of frequency peaks around 300 KHz between the good chips 4 and 5, there is almost no difference between peak locations, or frequency values. This difference between signal strengths from different but both good chips may be caused by the difference in reflection conditions on package surfaces and

their effect on the interferometer sensitivity. However, it will not affect internal structural characteristics or cause mode shift, on which the attention of this analysis is focused on. The measurement interval T_0 is 819.2 μs and the theoretical resolution in frequency domain is calculated to be $S = 1/T_0 = 1.2$ KHz.

5.3.2 Comparison between Finite Element and Experimental Modal Analyses

The comparison of natural frequencies of a good flip chip between the FE model and experimental results is listed in Table 5-10. Table 5-11 compares the natural frequencies of a flip chip with one open bump between the FE model and experimental results. It is observed both from Table 5-10 and Table 5-11 that the differences in frequency between the FE model and experimental results are small, mostly ranging from 1% to 10%. It is shown that there is a good correlation between the FE and experimental modal analyses and the experimental results validate the FE model.

Table 5-10 Comparison in natural frequencies of good flip chip between FE model and experimental results

Mode	FE model	Experimental results	Difference (%)
Mode 1 (KHz)	102.82	98.5	-4.20
Mode 2 (KHz)	227.46	197.0	-13.39
Mode 3 (KHz)	319.01	295.0	-7.53
Mode 4 (KHz)	422.00	402.0	-4.74
Mode 5 (KHz)	641.56	649.0	1.16
Mode 6 (KHZ)	723.33	704.0	-2.67
Mode 7 (KHz)	795.30	795.0	-0.04

Table 5-11 Comparison in natural frequencies of flip chip with one open bump between FE model and experimental results

Mode	FE model	Experimental results	Difference (%)
Mode 1 (KHz)	102.67	97.6	-4.94
Mode 2 (KHz)	227.13	196.0	-13.71
Mode 3 (KHz)	316.00	289.0	-8.54
Mode 4 (KHz)	394.80	400.0	1.32
Mode 5 (KHz)	640.19	648.0	1.22
Mode 6 (KHZ)	721.39	703.7	-2.45
Mode 7 (KHz)	792.61	794.0	0.18

The reason for larger difference in the frequency for mode 2 between the FE model and experimental results may come from two aspects. The frequency from experimental data corresponding to mode 2 has a quite small strength and wide sideband when the chip has two or less corner open bumps and it is hard to extract an exact peak value from the experimental results as the frequency. Meanwhile, damping is not included into the FE model and it might have a larger effect on mode 2.

From the FE and experimental modal analyses discussed above, mode 2 is sensitive to open bump defects. The power spectra ranging from 150 KHz to 210 KHz at inspection points #36 and 48, which contains mode 2, are shown in Figure 5-13 (a) and (b). At the inspection point #36, peaks corresponding to mode 2 are observed clearly from the power spectrum, especially for chips with two to four open bumps; while there are no obvious peaks observed in the power spectrum of responses measured at the inspection point #48. Correspondingly, this phenomenon is observed from the mode

shape evolution of mode 2 in the FE analysis, as shown in Figure 5-14, in which the scale of deformation is shown. It is observed that with the evolution of mode shapes, the location of maximum deformation approaches the position of open bump defects, resulting in a large deformation at inspection point #36. However, for inspection point #48, there is almost no change in the amplitude of mode shape. Therefore, mode shape analysis explains why frequency peaks are observed at inspection point #36 instead of point #48 in the power spectrum shown in Figure 5-13.

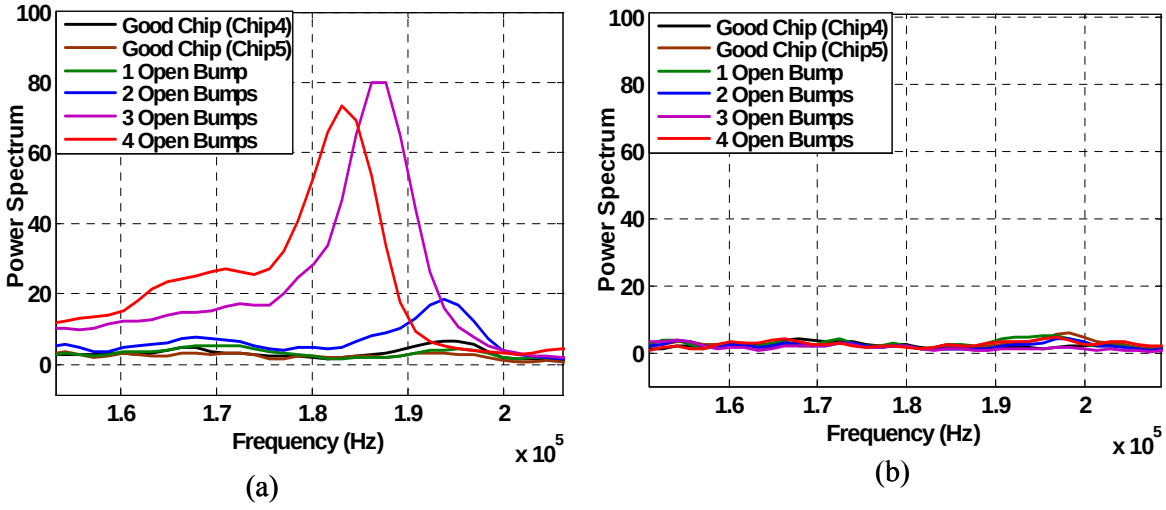


Figure 5-13 Power spectrums ranging from 150 KHz to 210 KHz: (a) inspection point #36 (b) inspection point #48

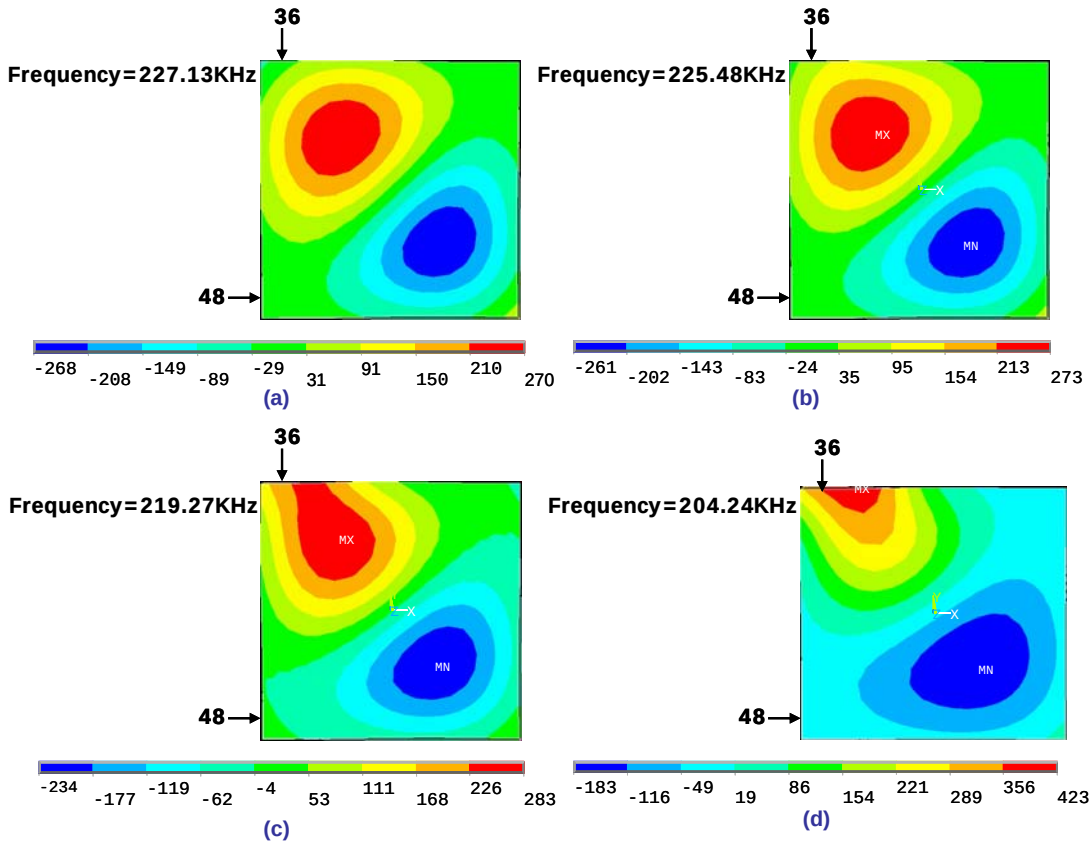


Figure 5-14 Mode shape evolution of mode 2 from FE model: (a) 1 open bump (b) 2 open bumps (c) 3 open bumps (d) 4 open bumps

In general, there is a good correlation between the FE modal analysis and experimental results. The mode shift and mode shape evolution from FE analysis explains the effect of open bump defects on the structural characteristics of flip chip packages, and correlates to the experimental observation.

5.3.3 Effect of Simplifications in Analytical Model on Mode Calculations

The difference between the analytical model and experimental results is not very small because more simplifications were made in the analytical model. The most likely reasons for this difference include: first, the solder bump is simplified to be in cylindrical

shape in the analytical model and the stiffness of solder bump (spring) is calculated based on this simplified spring model; second, the UBM and copper pads are not included into the analytical model; third, the in-plane motions and damping effect are not included into the analytical model.

If there is a variation for the nominal stiffness of solder bump (spring) by $\pm 5\%$, the largest corresponding mode change relative to the nominal value from the analytical model is calculated to be 1.73% and at mode 4. It is shown that the mode variation is small if the stiffness variation of solder bump caused by the package materials is small.

The damping ratio of the package structure can be roughly estimated from the power spectrum of transient out-of-plane displacement responses of flip chip packages under pulsed laser loading. The damping ratio is estimated by using the known half-power bandwidth method [Franklin J. et al., 2002]. It is shown in the power spectrum that different modes have different damping ratios. The possible largest damping ratio is estimated to be 4% with the half-power bandwidth method and it happens at mode 2. When the effect of damping ratio is included into the analytical model, all the modes are decreased by 4% at maximum. It can be concluded that the difference between the analytical model and experimental results would decrease with the consideration of the damping ratio in the analytical model.

5.4 Chapter Summary

Analytical, numerical and experimental modal analyses are successfully integrated to investigate the structural characteristics of flip chip packages and the effect of defects on modes and mode shapes of package structures. The mode shift and mode

shape evolution indicate quality degradation of flip chip solder bumps, and they are correlated with the severity of open bump defects. The results show that modal analysis is a useful tool for quality evaluation of flip chip packages. The application of modal analysis to flip chip packages can be expanded to other electronic packages, including chip scale packages, land grid array packages, ball grid array packages, and etc.

The integrated analytical, numerical and experimental modal analysis is a useful tool to understand the dynamic characteristics of flip chip packages and other package formats. The finite element modal analysis can indicate the modes and mode shapes most sensitive to particular defect(s) at specific positions, which can help to narrow down the frequency range to be investigated in power spectrum analysis and provide a valuable direction for further signal processing of experimental data.

CHAPTER 6

THERMOMECHANICAL RELIABILITY STUDY OF SOLDER BUMPS IN ELECTRONIC PACKAGES USING LASER ULTRASOUND TECHNIQUE AND FINITE ELEMENT METHOD

Solder bumps with cracks often have intermittent interconnections and can pass functional test or in-circuit test, but will cause problems in the usage. It is a challenging task to inspect solder bump cracks in electronic packages without cross-sectioning or utilizing other destructive methods. From the survey of nondestructive solder bump inspection methods in Chapter 1.1, X-ray tomography and CSAM are nondestructive techniques for inspecting cracked bumps, however they have disadvantages [O'Conchuir D., 1991]. For example, X-ray tomography normally takes a very long time for image interpretation and its price is prohibitive. CSAM always requires a coupling medium (usually deionized water) to propagate acoustic energy from a piezoelectric transducer to the specimen.

Under the cyclic thermal loads, solder bumps are subjected to strain and stress due to a coefficient of thermal expansion (CTE) mismatch between the package constitutions. Due to the constraints of thermal expansion, excessive strains/stresses might be induced and eventually initiate and propagate fatigue cracks in solder bumps [Darveaux R., (2002), Lau J., (1997)]. The thermomechanical reliability of solder bumps in electronic packages, including tin-lead and lead-free materials, has been intensively studied with analytical, simulation and experimental methods [Michaelides S., (1998), Lau J. (2000), Xiao G., (2001), Darveaux R., (2002), Balkan H., (2002), Guven I., (2004), Yang D.

(2004), Noritake C., (2006), Biswas K., (2007)]. However, the study on crack propagation in solder bumps with the combination of finite element simulation, nondestructive inspection and destructive validation is still limited.

The FE model has been intensively used to characterize the thermomechanical reliability of solder bumps in electronic packages. The models for assessing fatigue lifetime of solder bumps in electronic packages can be grouped into models based on plastic strain [Yan W. et al., 2006] and models based on energy (inelastic strain energy density dissipation per cycle) [Shi X., (2000), Soloman H., (1986), Vandervelde B., (2002)]. The solder bump reliability study under cyclic thermal loading normally requires two steps [Yeo A., 2006]. First, an FE model integrating a suitable solder constitutive law to extract stress-strain results as failure parameters. Second, a solder failure model to predict the lifetime of solder bumps using the failure parameter extracted from the FE model. A viscoplastic constitutive law has been intensively studied for the inelastic deformation and reliability analysis of electronic solders [Shi X., (2000), Pang H. et al., (1999)].

This chapter shows the application of laser ultrasound-interferometric technique to thermomechanical reliability study of board-level (second-level) solder bumps in the land grid arrays and first-level solder bumps in the flip chip packages. In Chapter 6.1, the reliability of board-level solder bump in the LGA packages on organic substrates is studied and the inspection results show that they can withstand 1000 thermal cycles and therefore have a high reliability satisfying design requirements under the cyclic thermal loading. The solder bump defects induced by further thermal fatigue have been detected in the land grid arrays after 2000 thermal cycles using laser ultrasound-interferometric

technique. In Chapter 6.2, the thermomechanical reliability of flip chip solder bumps has been systematically investigated using laser ultrasound technique and finite element method. The quality degradation (crack propagation) of solder bumps in the flip chip packages with increasing number of thermal cycles has been tracked with the laser ultrasound-interferometric inspection system. The correlation between the finite element simulation and experimental results on the thermomechanical reliability of solder bumps is also studied. The effect of package parameter sensitivity and tolerance on the thermomechanical reliability of solder bumps has been studied with statistical methods in Chapter 6.2.

6.1 Thermomechanical Reliability Study of Solder Bumps in Land Grid Array Packages

Since a land grid array package has lower standoff height and different material properties compared with a conventional ball grid array (BGA) package, LGA package gains attention on its reliability characteristics. A major concern is board-level solder bump reliability of the LGA packages under thermal loading. Tee has studied board-level solder joint reliability of the thermally enhanced BGAs and LGAs with finite element modeling, and especially focused on the effect of package dimensions and material properties on solder joint reliability of the BGA packages [Tee T., 2004]. Lee has analyzed thermal performance and solder joint reliability of the modified lead-frame land grid array packages using FE modeling integrated with the design of experiment concept [Lee C., 2005]. Kujala compared the reliability performance of LGA and BGA packages numerically and experimentally [Kujala A., 2002]. Through both board-level drop and

temperature cycling tests, good performance of LGA packages for portable electronic application was demonstrated by Kujala.

6.1.1 Experimental Procedures

In order to assess solder bump reliability of the LGA packages under the temperature extremes of a non-operating or storage environment, thermal cycling tests were performed on several boards. Temperature cycling also constitutes an accelerated stress test. In this work, an air-cooled, fast temperature changing ESPEC environmental chamber was used to perform the tests. The boards with the samples were subjected to a specially derived temperature profile, as shown in Figure 6-1. The temperature profile was from -40°C (minimum) to 85°C (maximum), with a ramp rate of 7°C /minute and a 30-minute dwell time at the two temperature extremes. The samples were pulled out after each 250 cycles, visually observed and tested with 2-D X-ray. Laser ultrasound test was performed on the boards after 250, 1000 and 2000 cycles. This study is the first application of laser ultrasound-interferometric technique to the over-molded packages, such as LGA packages.

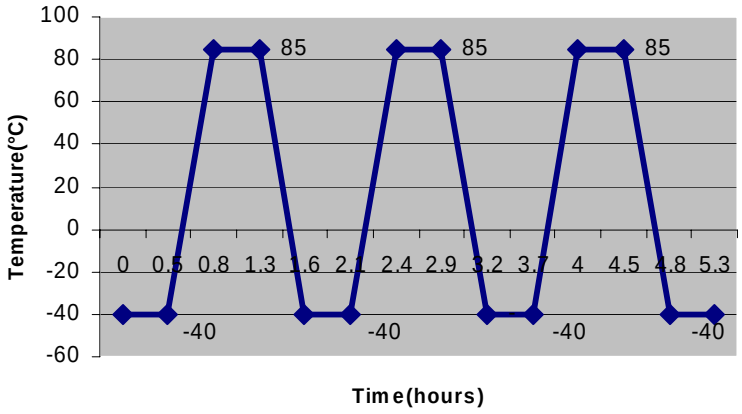
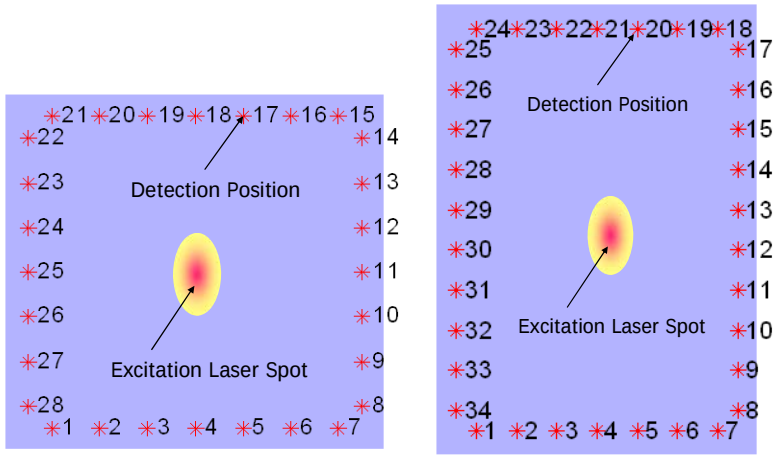


Figure 6-1 Temperature profile of ATC test for LGA package

In the laser ultrasound testing, the laser is excited at the center of devices U5 and U6. The inspection points are selected on the periphery of both device surfaces. For U5 and U6, 28 and 34 inspection points are sampled separately. The inspection patterns of both devices are shown in Figure 6-2 (a) and (b) respectively, in which the stars represent the inspection positions, with the excitation laser spot indicated by an elliptical shape. In a counterclockwise direction, inspection points on U5 and U6 are numbered from 1 to either 28 or 34.



(a) (b)

Figure 6-2 Inspection patterns of LGA packages: (a) U5 (b) U6

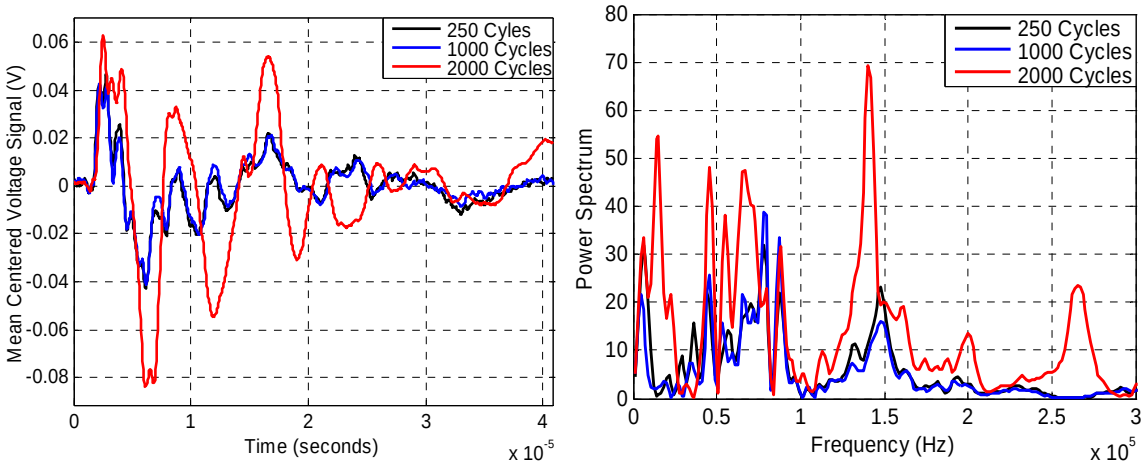
6.1.2 Experimental Results and Discussions

The electronic packages with solder bump interconnections can be modeled as a mass-spring structure. The device is modeled to be a thin continuous rectangular plate and the solder bump is modeled as a spring. The defects within solder bumps, such as cracks, induce changes to the constraint conditions of the package structure and it leads to

changes in the transient out-of-plane displacement responses of electronic packages under pulsed laser loading. The principle of the laser ultrasound inspection system is to compare the transient out-of-plane displacement responses from a temperature cycled package to that before thermal cycling. The difference between the responses comes mainly from abnormal solder bump interconnections. Normally, the transient out-of-plane displacement response from a good electronic package before thermal cycling is used as a reference when evaluating the quality of electronic packages after thermal cycling. In this particular case, the LGA packages used in this study went through 250 thermal cycles. Typically, 250 thermal cycles are too low to induce any defect in LGA packages; therefore, we can safely use the responses after 250 thermal cycles as references for both U5 and U6 packages.

Figure 6-3 (a) shows the time-domain responses of package U5 on board 2 after 250, 1000 and 2000 thermal cycles. Even though the total measurement period is 164 μs, we choose to show the signals in the time interval from 0 to 40 μs. There is only a small difference between the transient time domain responses obtained after 1000 and 250 thermal cycles, while there is a large difference between transient signals obtained after 2000 and 250 cycles. The corresponding power spectrums of the time domain responses after 250, 1000 and 2000 cycles are shown in Figure 6-3 (b). The electronic package with solder bump interconnections is modeled as a mass-spring structure. When there is a defect in the spring(s), the stiffness of the system decreases. In the same way, when there is a defect in the solder bump(s), the stiffness of the whole package decreases. Therefore, natural frequencies of the defective package shift downway on the frequency scale relative to the good package and can be extracted from the power spectrum of laser

ultrasound signals. It is observed from Figure 6-3 (b) that there is no obvious frequency shift for package U5 after 1000 thermal cycles compared to 250 cycles. It indicates that there is no measurable quality degradation of solder bumps in the LGA package after 1000 thermal cycles. However, a frequency shift is observed for package U5 after 2000 cycles relative to 250 and 1000 cycles, and the quality degradation of solder bumps was readily detected. Meanwhile, new frequency peaks were observed between 250 KHz and 300 KHz and it indicated that new modes corresponding to these frequency peaks were induced on the LGA specimen after 2000 thermal cycles. This is a clear indication of solder bump quality degradation in the LGA package after 2000 thermal cycles, which caused a change to the structural characteristics of the LGA package.

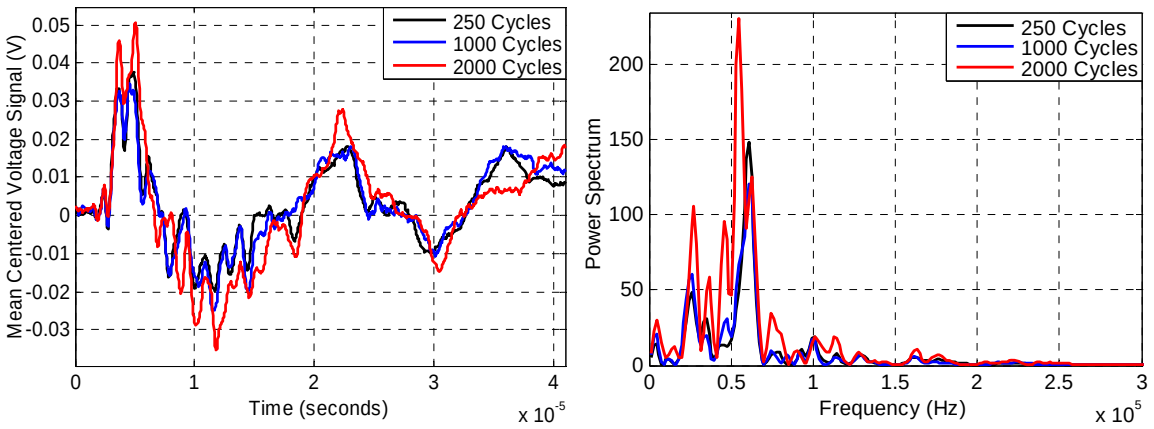


(a) (b)

Figure 6-3 (a) Time domain responses and (b) power spectrum of U5 on board 2

The same thermal cycling and measurement were done on U6. Figure 6-4 shows the time-domain responses of device U6 on board 2 after 250, 1000 and 2000 thermal cycles during the time interval from 0 to 40 μs. The corresponding power spectrums are

shown in Figure 6-4 (b). The difference between time-domain signals is small and no obvious frequency shift is observed after 1000 thermal cycles compared to that after 250 cycles, which are similar to the results of device U5. A large difference in time domain responses is observed of package U6 after 2000 cycles compared to that after 250 cycles and a frequency shift is also observed for package U6 after 2000 cycles relative to that after 250 cycles.

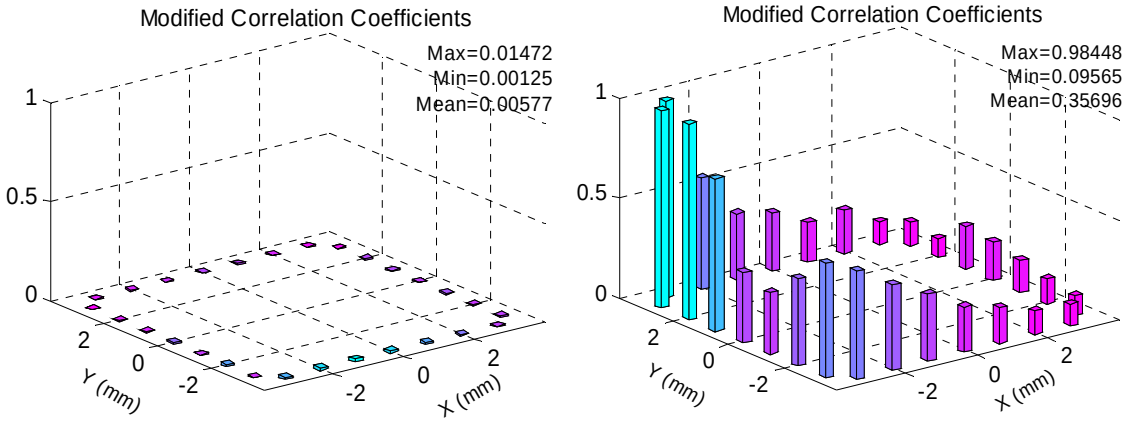


(a) (b)

Figure 6-4 (a) Time domain responses and (b) power spectrum of U6 on board 2

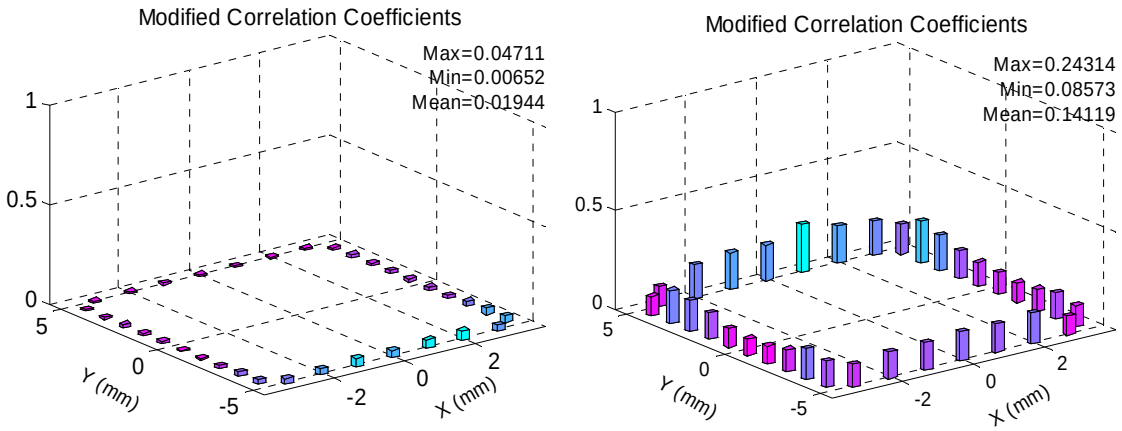
The responses after 250 thermal cycles are used as references to calculate MCCs for both packages U5 and U6. The responses after 1000 and 2000 thermal cycles are compared to the reference using the MCC method. This gives 28 and 34 comparisons for U5 and U6 respectively. The MCC values of U5 on board 2 are shown in Figure 6-5 (a) and (b) after 1000 and 2000 cycles separately. The MCC values are very small in Figure 6-5 (a), with the mean value being 0.00577. It is shown that the difference in the out-of-plane displacement responses between 1000 and 250 thermal cycles is small and it

indicates that there is almost no quality degradation for solder bump interconnections after 1000 thermal cycles when 250 thermal cycles is used as a reference. However, the MCC values shown in Figure 6-5 (b) are large, especially at the corners. It is shown that the difference in the out-of-plane displacement responses of package U5 between 2000 and 250 thermal cycles is large and it indicates existence of solder bump failures in the package U5 induced by thermal fatigue. Similarly, the MCC values of U6 are shown in Figure 6-6 (a) and (b) after 1000 and 2000 cycles separately. The similar results are observed in Figure 6-6 (a) and (b) for package U6 after 1000 and 2000 cycles. The quality degradation of solder bumps in package U6 after thermal cycling is also demonstrated using MCC analysis of laser ultrasound signals, as shown in Figure 6-6.



(a) (b)

Figure 6-5 Experimental results of U5 on board 2 with laser ultrasound-interferometric technique after: (a) 1000 cycles (b) 2000 cycles

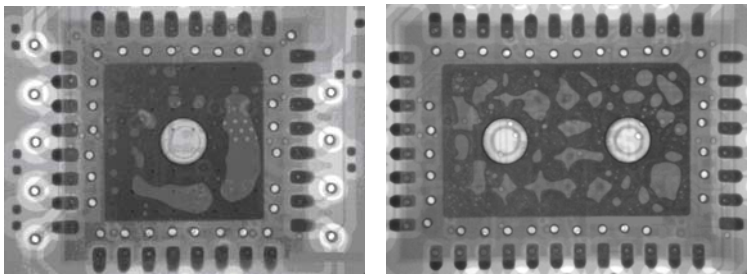


(a) (b)

Figure 6-6 Experimental results of U6 on board 2 with laser ultrasound-interferometric technique after: (a) 1000 cycles (b) 2000 cycles

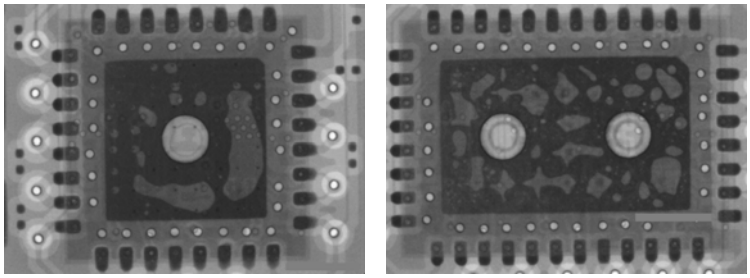
6.1.3 X-ray Results of LGA Test Vehicle

One nondestructive method for assessing potential incipient failures in solder bumps is X-ray technique. 2-D X-ray Images of LGA packages were obtained using a Fein Focus® system in order to observe potential problems in solder bumps. The images shown in Figure 6-7 and Figure 6-8 were taken after 250 thermal cycles and 1000 cycles. The images were taken from the top of the board 2. The results show that no solder bump quality degradation was observed after 250 and 1000 thermal cycles. The visual observation with an optical microscope also revealed that no solder bump failure could be observed after 250 and 1000 thermal cycles. Therefore, it demonstrates that laser ultrasound inspection results matched the visual observation and X-ray results.



(a) (b)

Figure 6-7 2-D X-ray images of LGA samples: (a) U5 and (b) U6 on board 2 after 250 thermal cycles



(a) (b)

Figure 6-8 2-D X-ray images of LGA samples: (a) U5 and (b) U6 on board 2 after 1000 thermal cycles

6.1.4 Summary of Thermomechanical Reliability Study of Solder Bumps in LGA Packages

In this study, it is found that board-level solder bumps in the LGA packages on organic substrates can withstand 1000 thermal cycles and therefore have a high reliability under cyclic thermal loading. Even though only results from two LGA packages on one board are shown, the LGA packages on other boards show similar results. This feasibility study has demonstrated the use of laser ultrasound-interferometric technique for evaluating solder bump quality in over-molded packages. It can also be concluded that

this method has a broad application prospect for quality assessment of lead-free solder bumps in the electronic packages.

6.2 Thermomechanical Reliability Study of Solder Bumps in Flip Chip Packages

The previous section has shown the reliability study of second-level (board-level) solder bumps in LGA packages using laser ultrasound-interferometric inspection technique. This section presents a systematic study on the thermomechanical reliability of flip chip solder bumps (first-level solder bumps) using laser ultrasound-interferometric technique and finite element simulation. The experimental results have shown that laser ultrasound technique could track solder bump crack propagation induced by thermal loading.

The purpose of the presented three-dimensional thermomechanical FE analysis is to understand strain energy density responses in flip chip solder bumps with 63Sn37Pb solder alloy, use them as failure parameters to study solder bump failures induced by cyclic thermal loading and correlate the failure parameters extracted from FE modeling with laser ultrasound testing results of FCPs through ATC tests. The FEA results are also used to help explain the effect of dwell time or ramp rate on solder bump reliability. This study has shown a good correlation between the failure parameter extracted from FE simulation and experimental results using laser ultrasound-interferometric technique.

6.2.1 Flip Chip Test Vehicle

The test vehicle used in this study is tin-lead flip chip package without underfill (as introduced in Chapter 3.3), which is a daisy-chain flip chip with 48 eutectic 63Sn37Pb solder bumps around the periphery of the package. The die size is 6.35 mm × 6.35 mm ×

0.6 mm and the typical bumps are 190 μm in diameter and spaced with a pitch of 457 μm, with twelve located on each edge along the perimeter of the package. The schematic of flip chip cross-section with dimension is shown in Figure 6-9. (The schematic of flip chip is shown in Figure 3-14 (b)).The laser excitation and inspection pattern are the same as those shown in Figure 3-16.

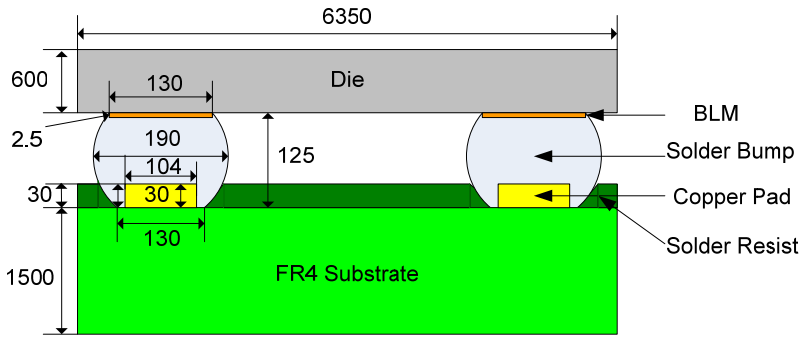


Figure 6-9 Cross section of tin-lead flip chip package (not to scale, unit in microns)

6.2.2 Experimental Procedures

ATC tests were performed in two phases on the FCP test vehicles following JEDEC standard JESD22-A104-C under condition G. As shown in Figure 6-10, the temperature profile is from -40°C (minimum) to 125°C (maximum), with a 25-minute dwell time at each of the two temperature extremes. In phase I of experiments, four boards were thermal cycled up to 70 cycles. The boards were taken out after every ten cycles and the FCPs on each board were tested for presence of cracks by measuring electronic resistance and using laser ultrasound method. These measurements were repeated every 10 cycles and stopped after 70 cycles. After 70 cycles, FCPs on the boards

were cross-sectioned to check for presence of cracks using a microscope. The resistance measurements show that the resistance values were essentially constant until 50 cycles when the resistance values went to infinity. Laser ultrasound testing showed that the MCC values began to increase gradually from 10 cycles to 50 cycles when there was a sharp jump. The cross-section was done only after 70 cycles, and the results show that all solder bumps at the corner had through cracks, while solder bumps at the center had partial cracks.

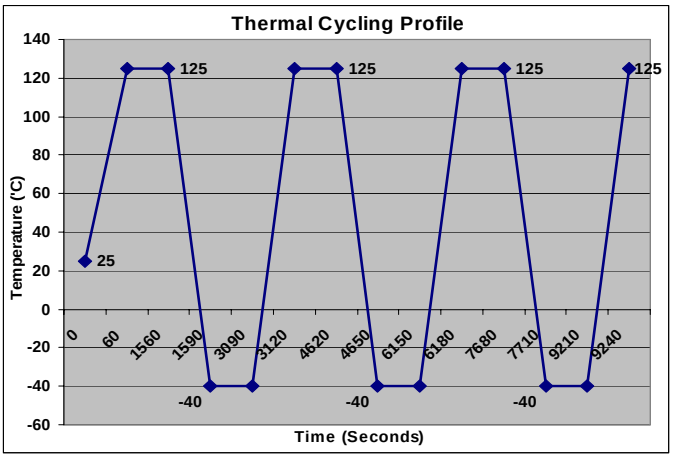


Figure 6-10 Temperature profile of ATC test for flip chip package

The phase II study is refinement of phase I study. In phase II study, seven boards were thermal cycled starting from 27 cycles to 56 cycles at an increment of approximately five cycles. After each five cycles, only one board was pulled out and tested to track crack initialization and propagation in solder bumps. Smaller thermal cycle increments were used to help determine exactly when cracks were initiated and how they propagated. In this phase, resistance, laser ultrasound and scanning acoustic microscopy (SAM) measurements were carried out for each board. In addition to these measurements,

cross-sections of these FCPs were done to validate previous measurement results. For each 5-cycle interval, a board was cross-sectioned.

6.2.3 Experimental Results and Discussions

6.2.3.1 Results from phase I of experiments

Figure 6-11 (a) shows the time domain laser ultrasound signals of tin-lead FCPs, which went through different number of thermal cycles at an increment of ten cycles, in the interval of 0 to 20.48 μs. Figure 6-11 (b) shows the corresponding power spectrums of time domain signals. It is observed that there is a larger difference in time-domain signals and there are larger backwards frequency shifts between thermal cycled samples and the reference one with increasing number of thermal cycles. Figure 6-12 (a) and (b) show the frequency shift around the frequency peaks of 100 KHz and 300 KHz. The decreasing trend of frequency peaks indicates quality degradation of solder bumps through thermal cycling. Comparing to the experimental modal analysis of flip chip samples with open bumps discussed in Chapter 5.3 (shown in Figure 5-12), it is clearly observed that there was a large shift for the dominant mode around 100 KHz in ATC test while there was almost no shift for the same mode with open bump defects. It comes from the fact that all the solder bumps went through quality degradation in ATC test; however, there are only tiny gaps between few bumps and the substrate in the flip chip samples with open bumps.

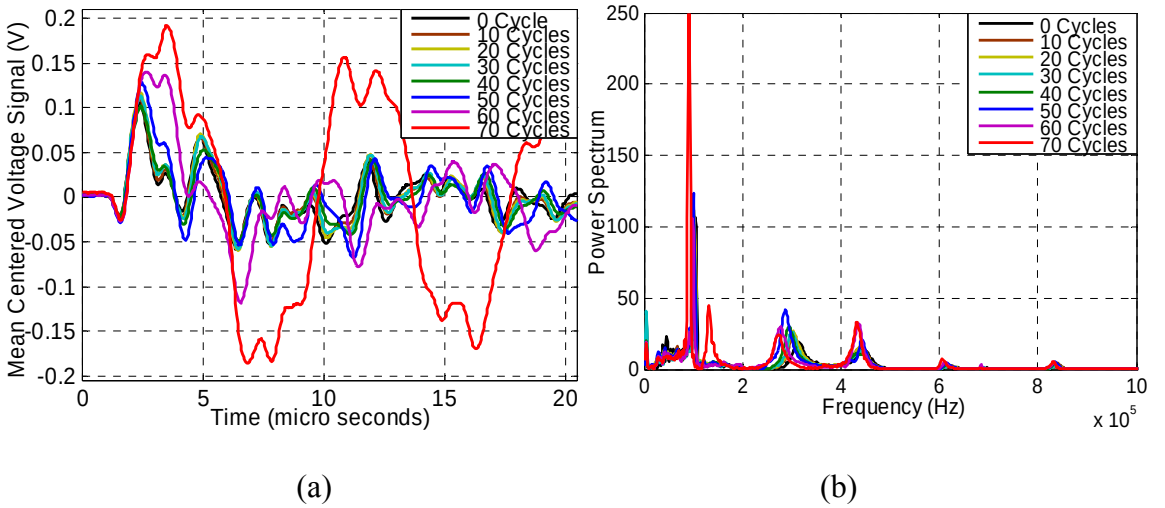


Figure 6-11 (a) Time domain signals and (b) power spectrum of time domain signals from flip chip samples in ATC test

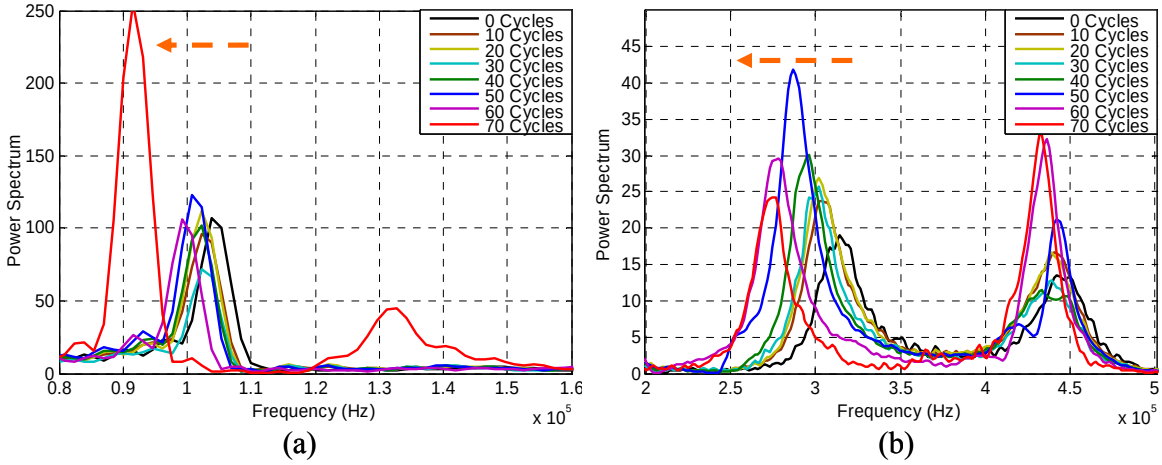


Figure 6-12 Frequency shifts around frequency peaks: (a) 100 KHz and (b) 300 KHz from flip chip samples in ATC test

In phase I study, resistance measurement of the daisy-chain FCPs through thermal cycling is shown in Figure 6-13. It is observed that the electronic resistance remained at a constant value near 2.5 Ohms before 50 thermal cycles and there was a sharp jump from 2.5 Ohms to infinity at 50 cycles, indicating the appearance of a through crack in the

solder bumps of the FCPs. It is shown from Figure 6-13 that the resistance value is not a good indicator of quality degradation or crack propagation in solder bumps since it did not show significant changes with increasing number of thermal cycles before the through crack appeared. The corresponding mean and maximum MCC values with thermal cycles are shown in Figure 6-14. It is observed that the maximum MCC value was obtained from the corner solder bump of flip chip sample. There was a steady increase for both mean and maximum MCC values before 50 cycles and it indicated quality degradation of solder bumps with increasing number of thermal cycles. There was a sharp jump of MCC values at 50 cycles and it indicated a severe quality degradation of solder bumps (which corresponds to a through crack observed in cross-section of FCP). Therefore, the quality degradation or crack propagation of solder bumps has been tracked using laser ultrasound-interferometric technique.

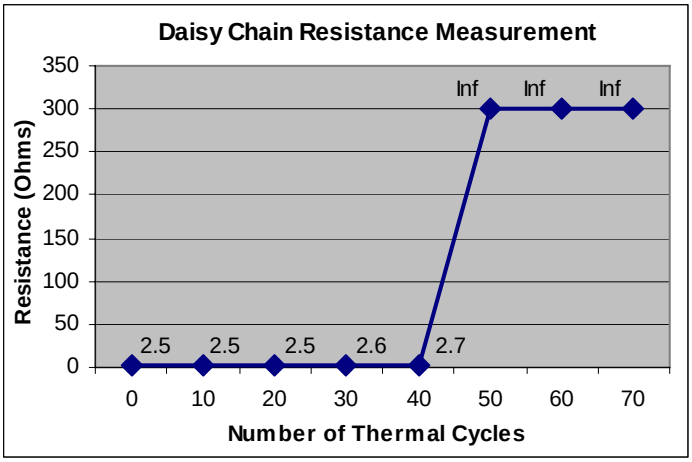


Figure 6-13 Resistance measurement of FCPs with increasing number of thermal cycles

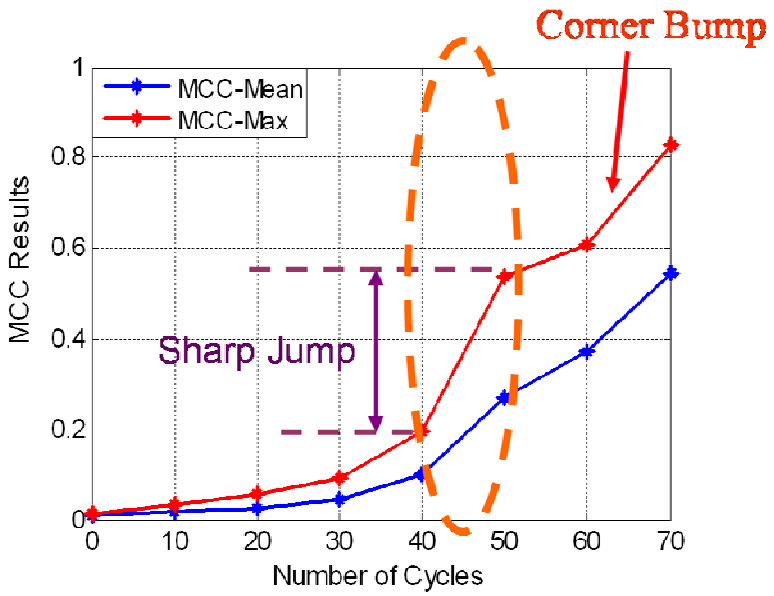


Figure 6-14 MCC values with thermal cycles in phase I study

The distribution of MCC values at all 48 inspection points with increasing of thermal cycles is shown in Figure 6-15. The largest MCC values always happened to corner bumps of FCPs and it showed the corner bumps were the critical ones in ATC tests. These results agreed well with FE simulation and were validated by cross-section observation of the solder bumps after ATC tests.

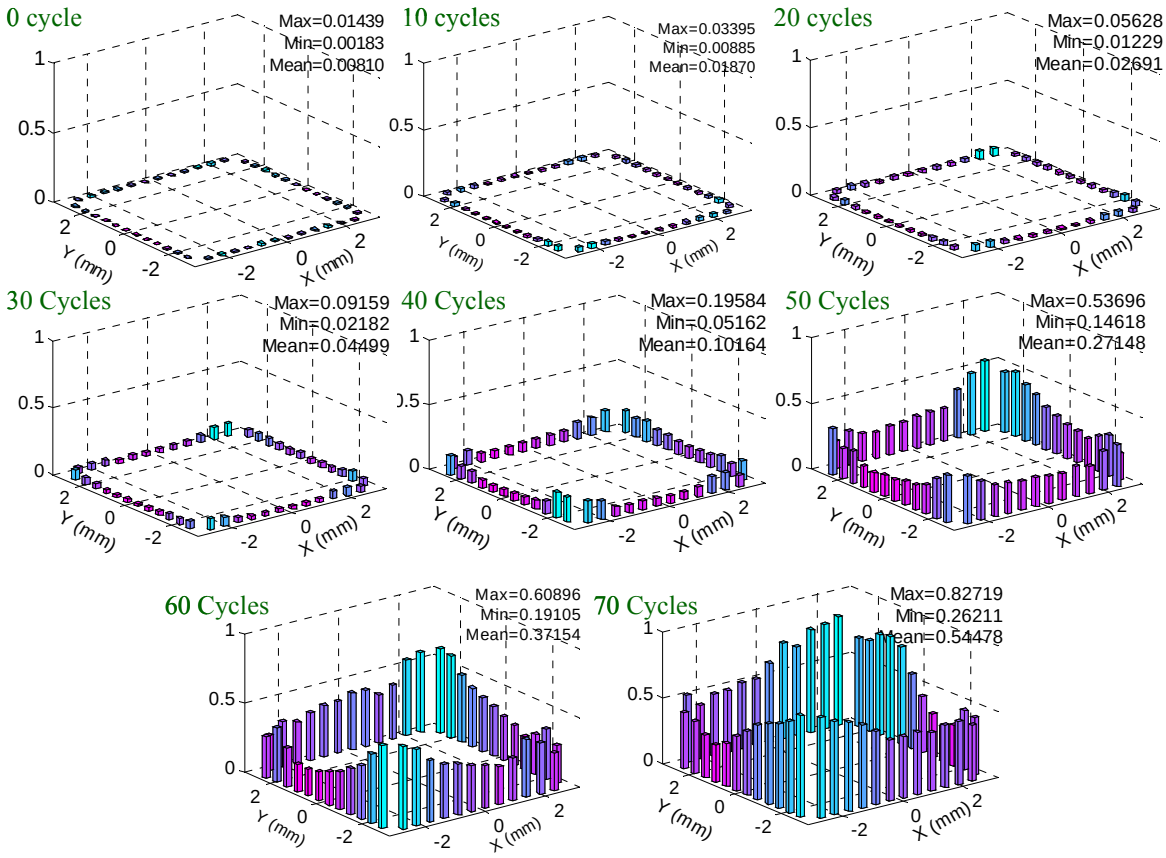


Figure 6-15 MCC values of 48 inspection points with thermal cycles

The cross-section pictures of solder bumps from #25 to #36 at one die edge after 70 thermal cycles are shown in Figure 6-16. Through cracks were clearly observed for corner bumps or bumps close to the chip corner and all the cracks lay close to the UBM layer. For the solder bumps lying at the center of the die edge, the cracks propagated into the solder bumps from bump corner, however through cracks did not form in these bumps at 70 thermal cycles.

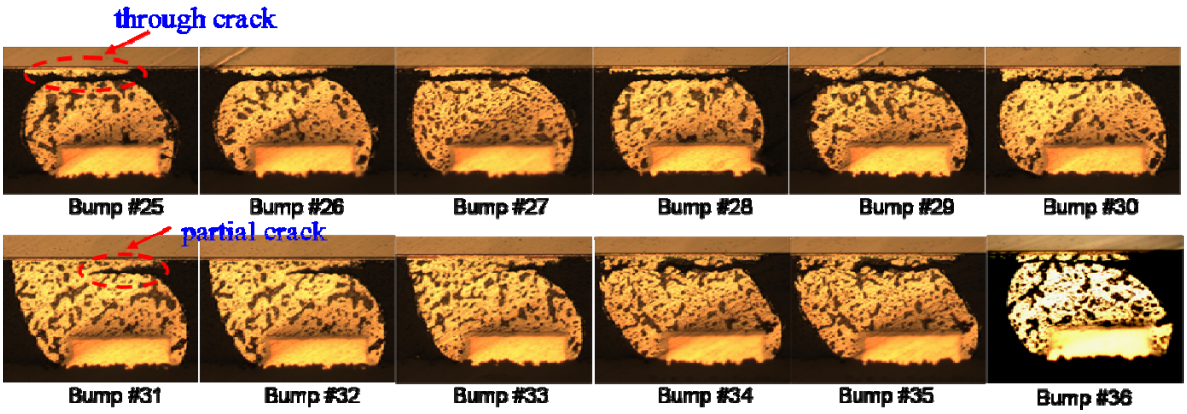


Figure 6-16 Cross-sections of bumps #25-36 in tin-lead FCP after 70 cycles

6.2.3.2 Results from phase II of experiments

In phase II study, a refined thermal cycling step was used to study solder bump quality degradation under cyclic thermal loading. Figure 6-17 and Figure 6-18 show the results from resistance measurement and laser ultrasound testing. Similar to the results from phase I study, the resistance value remained near 2.5 Ohms and jumped to infinity at 50 cycles indicating the appearance of through crack in solder bumps. However, MCC values increased steadily with thermal cycles from 27 to 56 cycles, indicating crack propagation (quality degradation) of solder bumps with increasing number of thermal cycles in ATC tests. A sharp jump of MCC value was observed at 50 cycles indicating a severe quality degradation of solder bumps, and this corresponds to through crack observed in cross-sectioned samples.

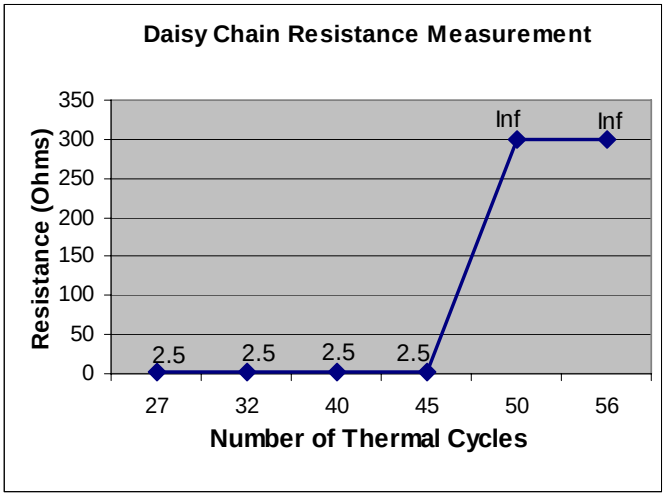


Figure 6-17 Resistance measurement with increasing number of thermal cycles in phase II study

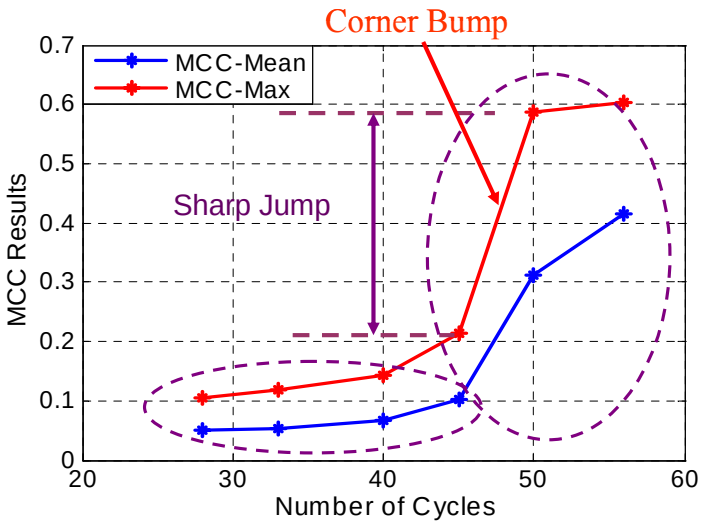
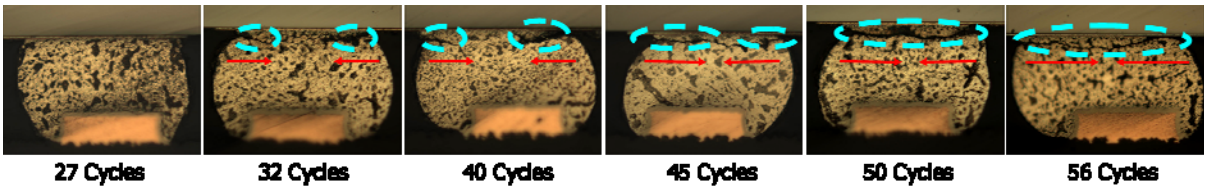


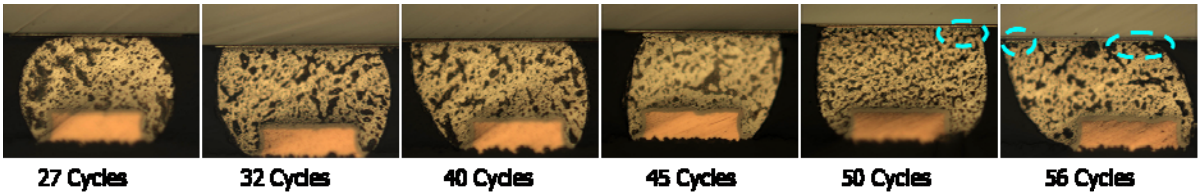
Figure 6-18 MCC values of FCPs with thermal cycles in phase II study

The cross-section pictures of critical solder bump #25 at the corner and the least-critical solder bump # 30 at the center are shown in Figure 6-19 (a) and (b). It is clearly shown that the crack appeared in the critical solder bump #25 at around 32 thermal cycles, much earlier than solder bump #30. The cracks started from bump corners near

the UBM layer and propagated into inside of the solder bump with increasing number of thermal cycles. Through crack was observed around 50 cycles for the critical solder bump #25. Therefore, the cross-section pictures validated the laser ultrasound testing results, and crack propagation observed from cross-sections agreed well with inspection results.



(a)

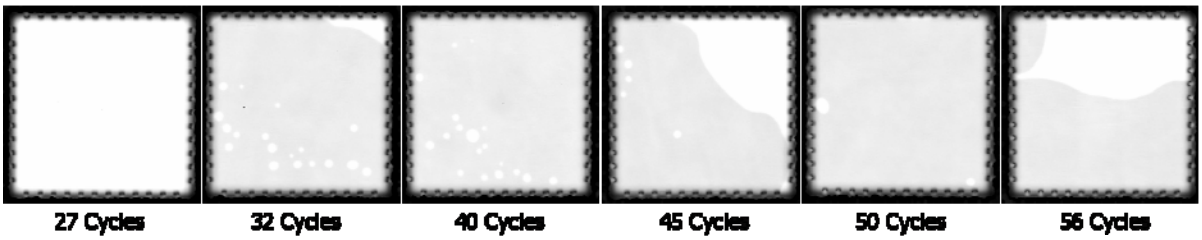


(b)

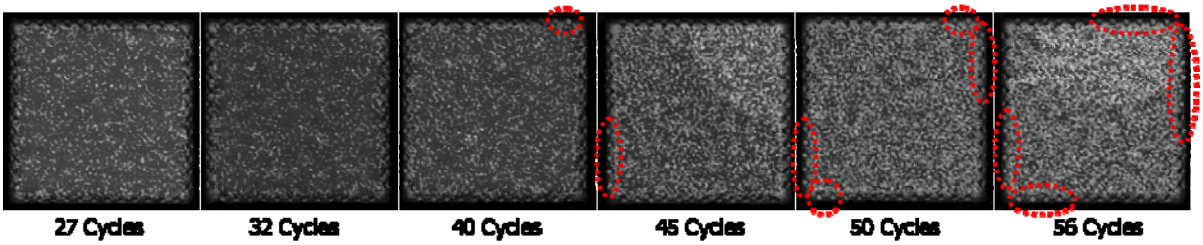
Figure 6-19 (a) Cross-sections of solder bump #25 with thermal cycles (b) cross-sections of solder bump #30 with thermal cycles in flip chip packages

The CSAM pictures, shown in Figure 6-20, were taken of FCPs in phase II study at two adjacent scanning layers using the Sonix® UHR-2001 SAM system with a 110-MHz ultrasonic transducer. The dark circles in Figure 6-20 represent solder bumps at the edges of FCPs. When thermal cycles increased, light areas (highlighted with red circles as shown in Figure 6-20) were observed in solder bumps starting from the corner bump, and these light areas indicated the appearance of cracks in solder bumps. However, it is still hard to clearly identify the cracks in solder bumps from CSAM images. Meanwhile,

solder bumps were not quite clear themselves in CSAM images because of the edge effect of the CSAM technique since solder bumps lay on the four edges of the FCPs.



(a)



(b)

Figure 6-20 CSAM pictures of FCPs through different thermal cycles captured at two adjacent layers: (a) layer 1 (b) layer 2

6.2.4 Finite Element Modeling of Solder Bump Thermal Reliability

6.2.4.1 Finite element model

In this section, a three-dimensional (3-D) quarter FE model for non-underfilled FCPs was developed with ANSYS® 11.0 [ANSYS Inc., 2007], with the dimensions being taken to be the average values of measurements made on several test vehicles (as shown in Figure 6-9). VISCO107 (shown in Figure 6-21), which is a 3-D element with 8 nodes, is used in this work to mesh solder bumps and represent the viscoplastic behavior of Sn-Pb solder during the cyclic thermal loading. Element VISCO107 can be used to represent

high nonlinear behavior of materials, therefore is suited to represent large and non-linear plastic strain of Sn-Pb solder under the cyclic thermal loading. The other materials, including silicon die, FR-4 substrate, copper pad, BLM and solder mask are meshed with element SOLID185, which is 3-D 8-node structural solid element and has the same structure as element VISCO107 (shown in Figure 6-21).

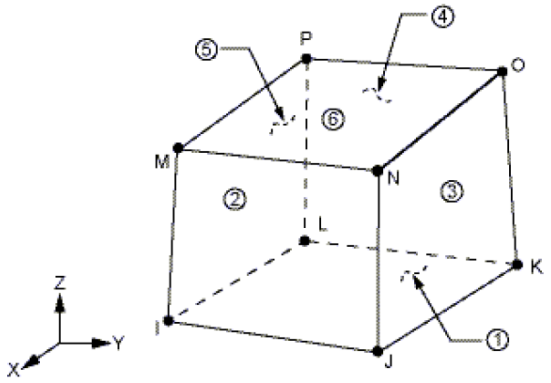


Figure 6-21 3-D viscoplastic solid of VISCO107 element [Source: ANSYS® User Manual]

Three boundary conditions, including zero displacements on two symmetric surfaces normal to X and Y directions, and zero displacement at the center point of bottom surface in all X, Y and Z directions, were applied to the 3D-quarter model (as shown in Figure 6-22). The meshing of representative solder bump column including silicon die, BLM, solder bump, solder mask, and FR-4 substrate is also shown in Figure 6-22 in detail. The quarter model was subjected to a uniform cyclic thermal loading from -40°C to 125°C, the same as the condition used in the ATC test. The stress-free reference temperature was taken to be at ambient temperature (25°C).

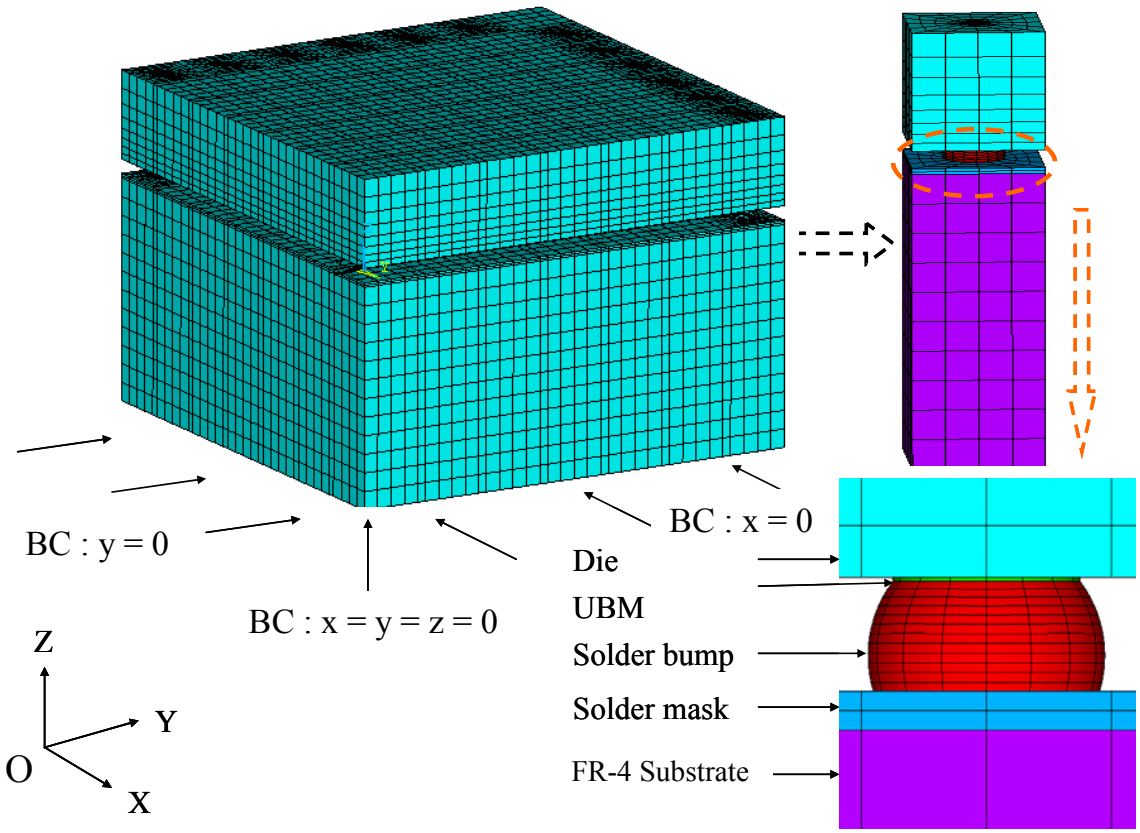


Figure 6-22 Three-dimensional quarter FE model of flip chip package and boundary conditions

The material models and properties of FCP used in FE analysis are summarized in Table 6-1 [Yeo A. et al., (2006), Zahn B., (2006)].

Table 6-1 Material models and properties of tin-lead FCPs in FE model

	Constitutive Model	E (N/mm^2)	CTE (ppm/K)	Poisson Ratio
Silicon Die	Elastic isotropic	131000	2.6	0.28
Al/Cu/Ni (98/1/1) UBM	Elastic isotropic	70000	23.1	0.35
Cu Pad	Elastic isotropic	120000	17	0.35
Solder Mask	Temp-dependent elastic, isotropic	4700@298K, 3914@323K, 2342@373K, 1556@398K	60	0.47
FR4 Substrate	Temp-dependent elastic, orthotropic	in plane: 27924-37T out of plane: 12204-16T	in plane: 16.0 out of plane: 84.0	in plane: 0.11 out of plane: 0.39
63Sn37Pb	Viscoplastic	30000@278K, 27143@323K	24.5	0.35

The Anand's viscoplastic constitutive law was employed to represent the inelastic behavior of eutectic 63Sn37Pb solder. The fatigue lifetime of solder bump has been found to correlate with the inelastic strain energy density W [Darveaux R., (2002), Vandervelde B., (2003)], which is integral of the stress σ_{ij} with respect to the inelastic strain ε_{ij}^{in}, and is defined in tensor format in Equation 6-1. The element volume averaging method (as shown in Equation 6-2) [Yeo A. et al., (2006), Zahn B., (2006)] was employed to calculate the inelastic strain energy density (SED) ΔW_{avg} accumulated or dissipated per cycle from the interface elements of critical solder bump, as shown in Figure 6-23.

$$W = \int_0^{\varepsilon_{ij}^{in}} \sigma_{ij} d\varepsilon_{ij}^{in} \tag{6-1}$$

$$\Delta W_{avg} = \frac{\sum_{i=1}^{n} \Delta W_i * \Delta V_i}{\sum_{i=1}^{n} \Delta V_i} \tag{6-2}$$

Where,

ΔW_i: inelastic SED accumulated per cycle in interface element i,

ΔV_i: volume of interface element i.

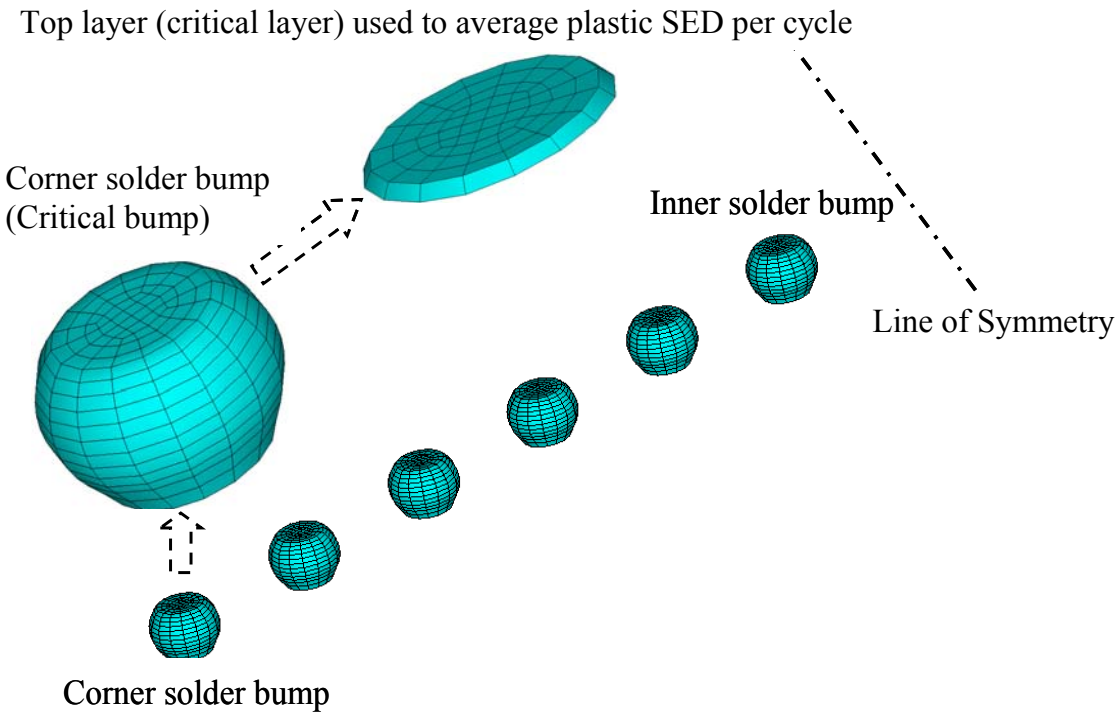


Figure 6-23 Meshing of solder bump and plastic SED extraction with volumetric averaging method

The element volume averaging method can minimize the effect of mesh sensitivity and stress-strain singularity in calculating inelastic SED for corner elements [Yeo A. et al., (2006), Zahn B., (2006)]. The simulated thermal cycling continues until the change in element averaged inelastic SED per cycle being $\leq 1\%$ between two consecutive cycles.

The plastic SED at each load step of an initial coarse model and a refined model is used to study the convergence of finite element model. The refined model is obtained by increasing mapped mesh density.

The refined mode has 55384 SOLID185 elements and 8064 VISCO107 elements in the whole assembly, while there are 50384 SOLID185 elements and 7296 VISCO107 elements in the coarse model.

The plastic SED results from both the initial model and the refined model are listed in Table 6-2. The percent differences between the refined model and the initial coarse model are listed in the last column. The difference between the initial coarse model and the refined model ranges from 5% to 6% in all the load steps, which meets the 5%-10% difference requirement and indicates a converged solution.

Table 6-2 Plastic SED of initial model and refined model at each load step

Load step	Coarse model (MPa)	Refined model (MPa)	Difference (%)
1	2.195	2.327	5.6
2	2.310	2.451	5.7
3	9.675	10.274	5.8
4	11.837	12.621	6.2
5	18.275	19.340	5.5
6	18.464	19.544	5.5
7	25.832	27.373	5.6
8	27.992	29.717	5.8
9	34.425	36.433	5.5

6.2.4.2 Viscoplastic constitutive model of solder

Viscoplasticity is defined as unifying plasticity and creep via a set of flow and evolutionary equations where a constraint equation is used to reserve volume in the plastic region [ANSYS®, 2007]. The Anand's viscoplastic model is available in ANSYS® library and the VISCO107 element is used as the large strain element in FE model to represent viscoplastic/creep behavior of the solder [ANSYS®, 2007]. The substrate, silicon die, UBM, copper pad and solder mask, which are assumed to exhibit elastic behavior, are modeled by using SOLID185 elements. In Anand's model, a deformation resistance variable "s" is used to represent averaged isotropic resistance to inelastic flow of the materials [ANSYS®, 2007]. One flow and three evolution equations are used to express Anand's model and given in Equation 6-3 to Equation 6-6. Therefore, Anand's model characterized the inelastic strains with an Arrhenius term for the temperature

dependency and the stress and strain rate dependency of the Garafalo form [Lee Y., 2006].

Flow equation:

$$\frac{ds}{dt} = \{h_0 \mid B \mid^{\alpha} \frac{B}{\mid B \mid}\} \cdot \frac{d\varepsilon_p}{dt} \tag{6-3}$$

Evolution equations:

$$\frac{d\varepsilon_p}{dt} = A[\sinh(\xi \frac{\sigma}{s})]^{1/m} \exp(-\frac{Q}{\kappa T}) \tag{6-4}$$

$$B = 1 - \frac{s}{s^*} \tag{6-5}$$

$$s^* = \hat{s} \cdot [\frac{d\varepsilon_p / dt}{A} \exp(\frac{Q}{\kappa T})]^n \tag{6-6}$$

Where,

$\dot{\varepsilon}_p$: inelastic strain rate,

A : pre-exponential factor,

Q : activation energy,

κ : universal gas constant,

T : current absolute temperature.

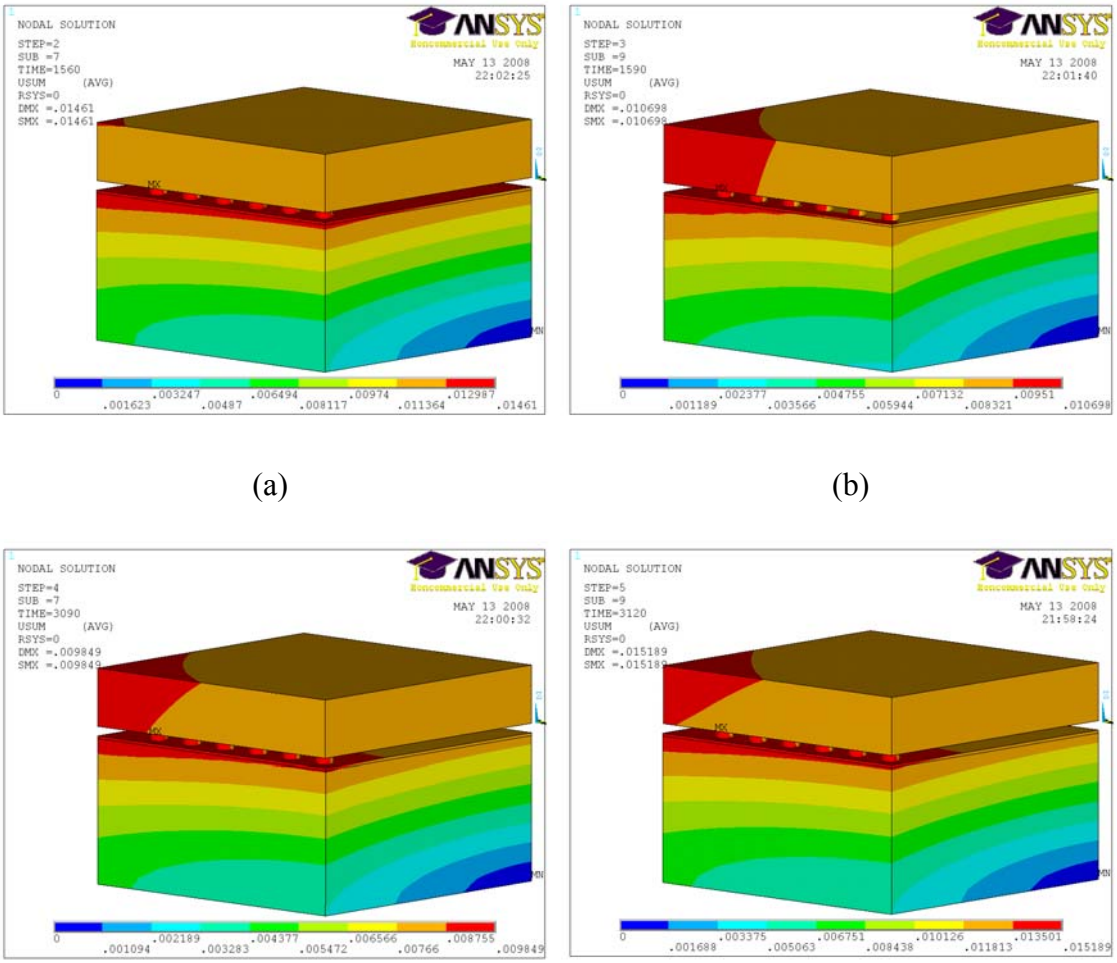
The Anand's model constants proposed by Shi [Shi X. et al., 2000] and Yeo [Yeo A. et al., 2006] were used in this study, as shown in Table 6-3 [ANSYS®, 2007].

Table 6-3 Anand's model constants for 63Sn37Pb solder

Parameter	Parameter/Unit	Description
C1	S_0 (N/mm^2)	Initial value of deformation resistance
C2	Q/k (1/K)	Activation energy/Boltzmann's constant
C3	A (1/sec)	Pre-exponential factor
C4	ξ	Multiplier of stress
C5	m	Strain rate sensitivity of stress
C6	H_0 (N/mm^2)	Hardening constant
C7	$\hat{S}$ (N/mm^2)	Coefficient for deformation resistance saturation value
C8	N	Deformation resistance value
C9	a	Strain rate sensitivity of hardening

6.2.4.3 FE simulation results

Two thermal cycles were simulated to achieve the change in accumulated inelastic SED $\Delta W_{avg} \leq 1\%$ between consecutive cycles in the viscoplastic model. Figure 6-24 (a)-(d) show the deformation contours of the flip chip package in one complete cycle, from heating, dwell at the maximum temperature, cooling, to dwell at the minimum temperature.



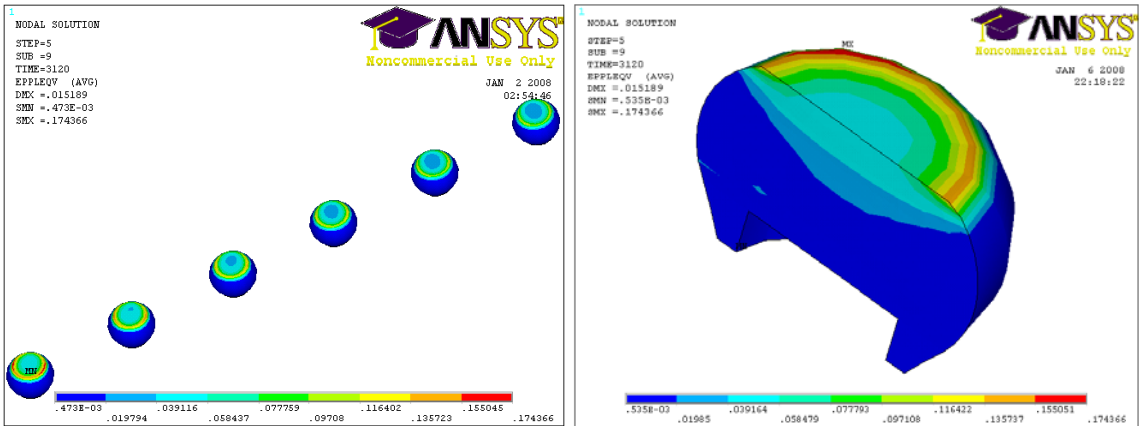
(a) (b)

(c) (d)

Figure 6-24 Deformation contours of flip chip package in one cycle: (a) thermal heating (b) dwell at the maximum temperature (c) thermal cooling (d) dwell at the minimum temperature

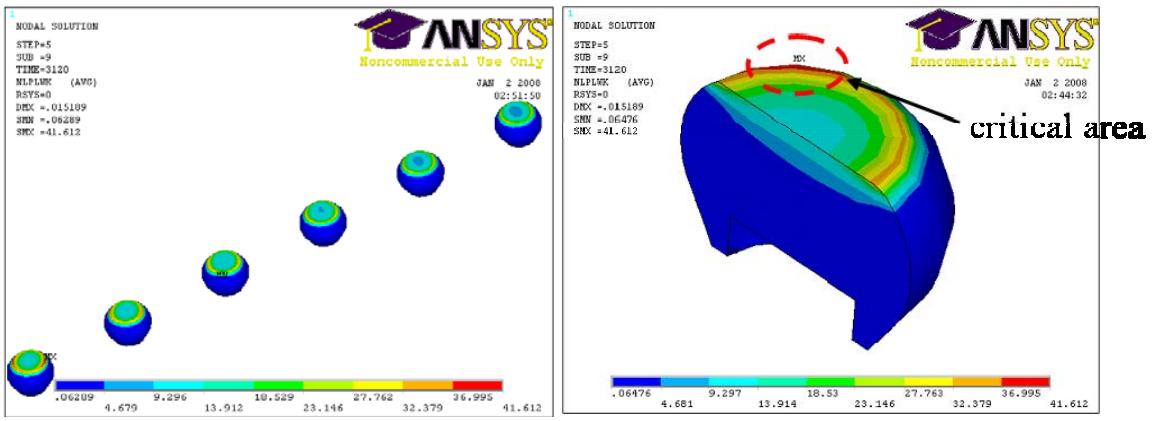
Figure 6-25 (a) shows plastic strain contours of six solder bumps in a row from corner to center solder bump at the end of one complete cycle from the viscoplastic model. It is observed that the plastic strain decreases consecutively from the corner to the center bump, numbered from bump #1 to bump #6, respectively. The corner solder bump is the critical one with maximum plastic strain. Figure 6-25 (b) shows the plastic strain contour of critical solder bump. Figure 6-26 (a) shows plastic SED contours of six solder

bumps from corner to center solder bump from the viscoplastic model. It is observed that the plastic SED decreases consecutively from the corner to the center bump. The corner bump is the critical one with maximum plastic SED, and observed to show appearance of crack and fail first validated by cross-section observations as shown in Figure 6-16 and Figure 6-20. Figure 6-26 (b) shows the plastic SED contour of the critical solder bump, in which the critical area with maximum plastic SED is clearly observed to lie at the elements close to the BLM layer. All these simulation results have a good agreement with cross-section observations of solder bump cracks.



(a) (b)

Figure 6-25 (a) Plastic strain contour of solder bumps extracted from viscoplastic model (b) Plastic strain contour of critical solder bump from viscoplastic model



(a) (b)

Figure 6-26 (a) Plastic SED of solder bumps from viscoplastic model (b) Plastic SED of critical solder bump from viscoplastic model

It is known from Equation 2-11 that there is a quadratic relationship between the fatigue lifetime and the distance of solder bump from the neutral point. It can be derived that the plastic SED that a solder bumps experiences will increase with the increase of distance from the neutral point (DNP) since the plastic SED is used as the failure parameter for predicting the fatigue lifetime of solder bumps. The relationship between the plastic SED and DNP of six solder bumps from the corner bump to center bump is shown in Figure 6-27. It is observed from Figure 6-27 that there is an approximate quadratic relationship between plastic SED and DNP of solder bump and it approximately matches the simplified theoretical model.

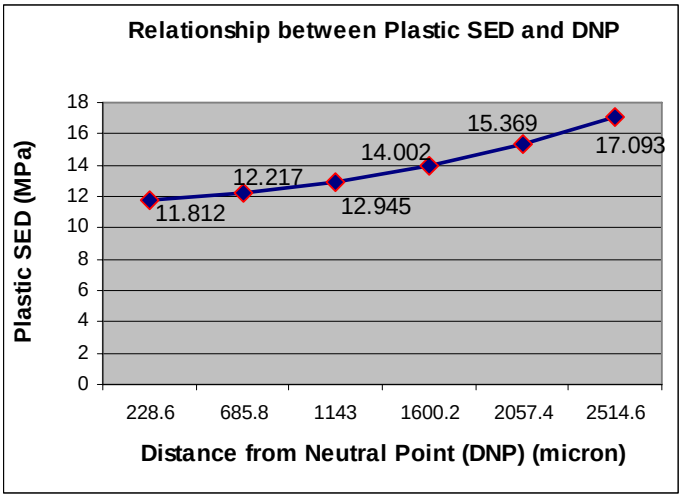


Figure 6-27 Relationship between plastic SED and DNP of solder bumps

6.2.4.4 Correlation study between experimental results and FE model

The plastic SED ΔW_{avg} accumulated per cycle is selected as the failure parameter to predict solder bump fatigue lifetime in FE analysis since it is correlated with the thermal fatigue of solder bumps from the previous analysis in sections 2.7 and 6.2.4.1. The laser ultrasound results measured directly on top of each solder bump tracked the quality degradation of solder bumps through ATC; therefore the testing results are correlated with thermal fatigue of solder bumps. The MCC value at 50 thermal cycles, which corresponds to the critical number of cycles when through crack appeared, is selected as experimental failure parameter. In terms of the structural symmetry of FCP used in this study and in order to minimize the variation in measurements, forty-eight solder bumps were grouped into six groups in calculating experimental failure parameters. The eight solder bumps (bumps #1, 12, 13, 24, 25, 36, 37 and 48 as shown in Figure 3-14 (b)) with the same location characteristics in FCP as solder bump #1 were

grouped into group #1. The eight solder bumps with the same location characteristics as solder bumps #2 to #6 were grouped into group #2 to #6 respectively by analogy. The sum of eight MCC values from eight solder bumps in each group was calculated and six sums were obtained from these six groups. The plastic SED ΔW_{avg} accumulated per cycle of solder bumps #1 to #6 from viscoplastic model and corresponding normalized MCC values at 50 cycles are listed in Table 6-4. In FE analysis, the corner solder bump has a viscoplastic SED accumulated per cycle approximately 1.5 times higher than the center solder bump. In laser ultrasound testing, the corner solder bump has a normalized MCC value approximately 1.6 times higher than the center solder bump. The correlation between ΔW_{avg} from viscoplastic model and normalized MCC values is plotted in Figure 6-28. The R-squared value of 0.9549 shows a strong linear correlation between them, as shown in Figure 6-28.

Table 6-4 Averaged plastic strain energy densities and normalized laser ultrasound testing values for six solder bumps from corner to center bump

Bump group #	ΔW_{avg} (MPa)	Normalized MCC value
1	17.093	1.00E+00
2	15.369	8.77E-01
3	14.002	8.43E-01
4	12.945	6.69E-01
5	12.217	6.36E-01
6	11.812	6.27E-01

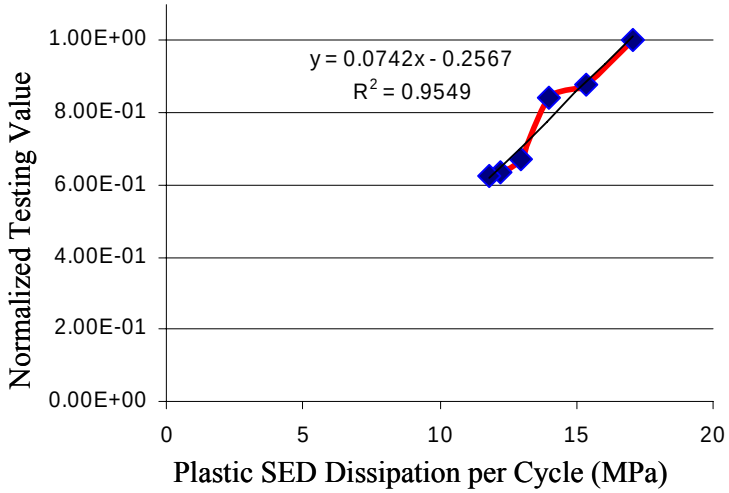


Figure 6-28 Correlation between plastic SED dissipated per cycle from viscoplastic model and MCC values from laser ultrasound testing

6.2.4.5 Solder fatigue life prediction

Two prediction models were selected from the literature to predict solder bump fatigue life. Solomon's method is strain-based approach and Zahn's method is energy-based approach [Soloman H., (1986), Zahn B., (2006)]. Solomon's strain-based approach is used here as a cross-examination of energy-based approach to predict fatigue life of flip chip solder bumps under cyclic thermal loading. The governing equations and coefficients of these two models are listed in Table 6-5 [Soloman H., (1986), Zahn B., (2006)].

Table 6-5 Solder bump fatigue life prediction models and coefficients

	Failure parameter	Governing equations
Strain-based	$\Delta\varepsilon_{plastic}$ Plastic strain range at two extreme temperatures	$N_f = \theta(\Delta\varepsilon_{plastic})^{\phi}$ θ = 1.292 for eutectic solder ϕ = -1.96 for eutectic solder
Energy-based	ΔW_{avg} (MPa) Inelastic strain energy density	$N = C_1(\Delta W_{avg})^{C_2}$ $C_1 = 781.99,\ C_2 = -0.9065$

The plastic strain range at the two extreme temperatures and the plastic SED are 0.1371 and 17.093 MPa from the viscoplastic model. Therefore, the characteristic lives calculated from Solomon's and Zahn's methods are 64 cycles and 60 cycles respectively. A characteristic life is calculated to be 54 cycles from Weibull distribution analysis (shown in Figure 6-29) of ATC testing results. Therefore, the FE analysis provided a good match with the experimental data.

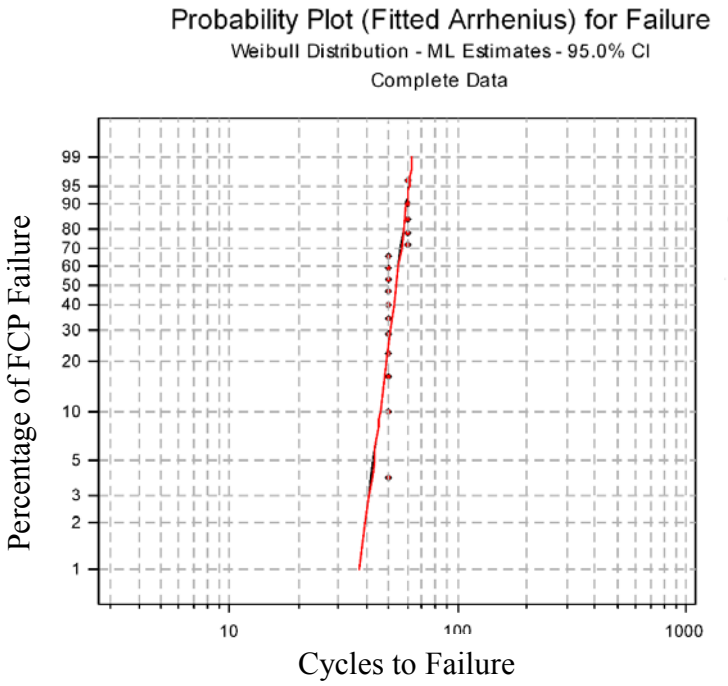


Figure 6-29 Weibulll distribution of ATC testing results

6.2.4.6 Summary

In this work, the thermomechanical reliability of flip chip solder bumps was systematically investigated using laser ultrasound-interferometric techniques and finite element analysis. The following are the key findings of this research work.

1) The results demonstrate the application of laser ultrasound-interferometric techniques to detecting solder bump fatigue cracks in flip chip packages. The quality degradation (crack propagation) of solder bumps with the increasing number of thermal cycles has been tracked with this system. The comparisons between laser ultrasound, resistance measurement and CSAM show that the laser ultrasound inspection system has advantages for inspecting solder bump fatigue cracks in flip chip packages as well as tracking interconnect quality degradation.

2) There is a good correlation between the inelastic strain energy density accumulated per cycle, which is a failure parameter extracted from FE analysis, and laser ultrasound testing results (experimental failure parameter). The FE analysis has been validated by laser ultrasound testing and the cross-section observations.

3) The corner solder bump always experienced the highest inelastic strain energy density from FE analysis and failed first. Therefore, the corner bump is the most critical one under cyclic thermal loading.

6.2.5 Parametric Sensitivity Study on Solder Bump Reliability

Parameter sensitivity studies have been carried out to investigate solder bump reliability with the design of experiments (DOE) method. The objective is to study the influence of package parameters on the thermomechanical reliability of solder bumps using statistical methods. Solder bump standoff, bump diameter, die thickness, and substrate thickness were selected as design factors, and the plastic SED extracted from FE simulation was selected as the response output. The values of these four factors are listed in Table 6-6. For each factor, its low value and high value were converted to the corresponding low and high codes (-1 or 1) used in DOE. Therefore, a four-factor full-factorial DOE at two levels was used in this study and 16 FE simulations were conducted. The observations - plastic SED at different combinations of factor levels obtained from FE simulations are listed in Table 6-7.

Table 6-6 Four-factor DOE at two levels for solder bump thermal reliability study

Parameters	Low value	High value	Low coded	High coded
Bump standoff (A): S_{bump} (μm)	115	135	-1	1
Bump diameter (B): D_{bump} (μm)	180	200	-1	1
Die thickness (C): T_{die} (μm)	550	650	-1	1
Substrate thickness (D): T_{sub} (μm)	1000	1500	-1	1

Table 6-7 Plastic SED obtained from full-factorial DOE

Simulation serial	A	B	C	D	Plastic SED (MPa)
1	-1	-1	-1	-1	17.168
2	1	-1	-1	-1	10.907
3	-1	1	-1	-1	23.223
4	1	1	-1	-1	15.199
5	-1	-1	1	-1	17.057
6	1	-1	1	-1	10.883
7	-1	1	1	-1	23.112
8	1	1	1	-1	15.149
9	-1	-1	-1	1	17.798
10	1	-1	-1	1	11.323
11	-1	1	-1	1	23.886
12	1	1	-1	1	15.719
13	-1	-1	1	1	17.608
14	1	-1	1	1	11.341
15	-1	1	1	1	23.919
16	1	1	1	1	15.727

The plastic SED is expressed as a function of the four factors and their two-factorial interactions (bilinear model),

$$P\_SED = \beta_0 + \beta_1 S_{bump} + \beta_2 D_{bump} + \beta_3 T_{die} + \beta_4 T_{sub} + \beta_5 S_{bump} D_{bump} + \beta_6 S_{bump} T_{die} + \beta_7 S_{bump} T_{sub} + \beta_8 D_{bump} T_{die} + \beta_9 D_{bump} T_{sub} + \beta_{10} T_{die} T_{sub} \quad (6\text{-}7)$$

Where, β_0 through β_{10} are regression coefficients.

The regression coefficients β_0 through β_{10} and corresponding t and P values were calculated using a linear regression given in Table 6-8. The larger the magnitude of the t value and smaller the P-value, the more significant is the corresponding factor. A P-value which is lower than 0.001 indicates that the corresponding factor is statistically significant.

Therefore, the regression equation can be expressed with estimated regression coefficients as,

$$P\_SED = 16.9 - 3.60 S_{bump} + 2.62 D_{bump} - 0.0267 T_{die} + 0.289 T_{sub} - 0.448 S_{bump} D_{bump} + 0.0207 S_{bump} T_{die} - 0.0424 S_{bump} T_{sub} + 0.0117 D_{bump} T_{die} + 0.0321 D_{bump} T_{sub} + 0.0103 T_{die} T_{sub} \quad (6\text{-}8)$$

Table 6-8 Estimated regression coefficients and corresponding t and P values

Predictors	Terms	Coefficients	t	P
Constant	Constant	16.9	1453.73	< 0.001
A	S_{bump}	-3.60	-309.69	< 0.001
B	D_{bump}	2.62	225.31	< 0.001
C	T_{die}	-0.0267	-2.30	0.070
D	T_{sub}	0.289	24.89	0.002
AB	$S_{bump}*D_{bump}$	-0.448	-38.60	< 0.001
AC	$S_{bump}*T_{die}$	0.0207	1.78	0.135
AD	$S_{bump}*T_{sub}$	-0.0424	-3.66	0.015
BC	$D_{bump}*T_{die}$	0.0117	1.01	0.360
BD	$D_{bump}*T_{sub}$	0.0321	2.76	0.040
CD	$T_{die}*T_{sub}$	0.0103	0.89	0.415

In terms of variance analysis of the input variables listed in Table 6-8 and Equation 6-8, it is observed that the solder bump standoff (S_{bump}) and diameter (D_{bump}) are two most important factors that influence solder bump reliability among the four analyzed factors: bump standoff, bump height, die thickness and substrate thickness. The larger the bump standoff, the higher is the solder bump reliability. The larger the bump diameter, the lower is the solder bump reliability. The previous observation of positive effect of bump standoff on solder bump thermal reliability matches with the theoretical analysis discussed in Section 2.7. The reason lies in that the stress concentration in solder bumps can be decreased by increasing solder bump standoff as represented by Equation

2-11 and that will improve solder bump thermal reliability. As to the negative effect of bump diameter on solder bump reliability, the contact angle between solder and silicon die, FR-4 substrate will decrease by decreasing bump diameter; therefore, it will be of help for decreasing stress concentration at the bump corner and improve thermal reliability of solder bumps. Meanwhile, a thinner substrate is desirable for better solder bump lifetime observed from Table 6-8 and the reason is that thinner substrate is of help to decrease the effect of CTE mismatch between silicon die and FR-4 substrate, which is the cause of thermal fatigue of solder bumps under thermal loading. The die thickness has the least important influence on solder bump reliability. Among two-factorial interactions, the interaction between the standoff and diameter of solder bump has a larger influence on solder bump reliability than others.

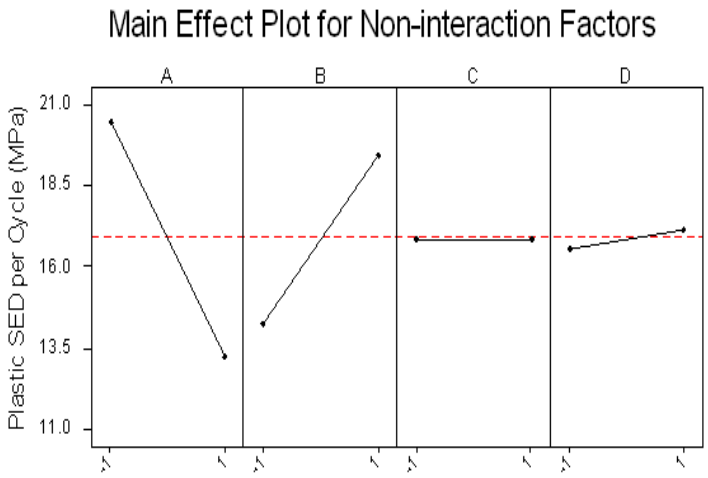
In order to measure the average effect of a factor, the difference between the average value of all observations in the experiment at the high (+) level of A and the average value of all observations in the experiment at the low level (-) of A is computed. The difference is called the main effect of one factor and represented by,

$$ME(A) = \bar{z}(A+) - \bar{z}(A-) \tag{6-9}$$

Where, z denotes one observation, and $A+$ and $A-$ represent the high and low levels of A, respectively.

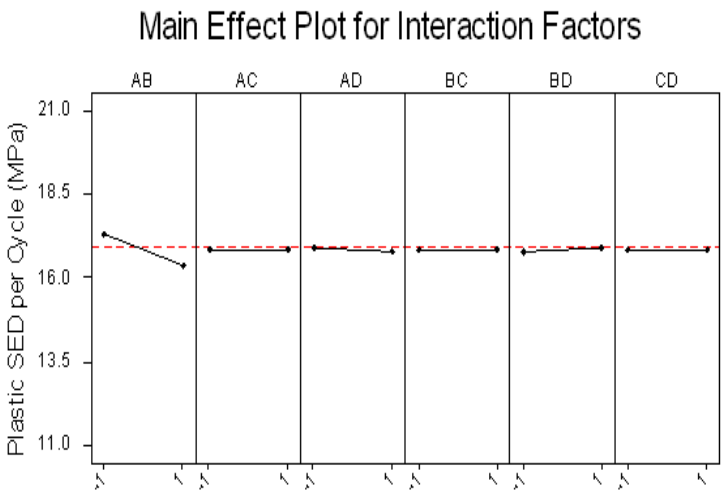
The main effect plot (shown in Figure 6-30) shows that factors A (solder bump standoff) and B (solder bump diameter) are the main effects on solder bump reliability since these two factors cause much larger difference in output observations between the

low and high levels they take. The slopes of main effect lines for factors A (solder bump standoff) and B (solder bump diameter) are opposite and it demonstrates the opposite effect that bump diameter and standoff play on the solder bump reliability. The bump standoff has a positive effect on solder bump reliability since plastic SED decreases with the increase of solder bump standoff, which means solder bump reliability or lifetime increases by increasing solder bump standoff. On the contrary, solder bump diameter has a negative effect on the solder bump reliability since plastic SED increases with the increase of solder bump diameter, which means solder bump reliability or lifetime is decreased by increasing solder bump diameter.



(a)

Figure 6-30 (a) Main effect plot (b) Plot for interaction factors



(b)

Figure 6-30 continued

When the solder bump lifetime was directly selected as regression output instead of plastic SED discussed previously, the regression coefficients were recalculated with linear regression model. The estimated regression coefficients and corresponding t and P values are listed in Table 6-9. The regression equation is expressed with estimated regression coefficients as,

$$Lifetime = 64.2313 + 12.5562S_{bump} - 9.19375D_{bump} - 0.08125T_{die} - 1.04375T_{sub} - 2.16875S_{bump} * D_{bump} - 0.06875S_{bump} * T_{die} - 0.026875S_{bump} * T_{sub} - 0.04375D_{bump} * T_{die} + 0.18125D_{bump} * T_{sub} - 0.04375T_{die} * T_{sub}$$

(6-10)

Table 6-9 Estimated regression coefficients and corresponding t and P values (output is solder bump lifetime)

Predictor	Terms	Regression coefficient	t	P
Constant	Constant	64.2313	1468.14	<0.001
A	S_{bump}	12.5562	287	<0.001
B	D_{bump}	-9.19375	-210.14	<0.001
C	T_{die}	0.08125	1.86	0.122
D	T_{sub}	-1.04375	-23.86	0.003
AB	$S_{bump}*D_{bump}$	-2.16875	-49.57	<0.001
AC	$S_{bump}*T_{die}$	-0.06875	-1.57	0.177
AD	$S_{bump}*T_{sub}$	-0.26875	-6.14	0.002
BC	$D_{bump}*T_{die}$	-0.04375	-1	0.363
BD	$D_{bump}*T_{sub}$	0.18125	4.14	0.009
CD	$T_{die}*T_{sub}$	-0.04375	-1	0.363

6.2.6 Tolerance Analysis on Solder Bump Reliability with Response Surface Methodology (RSM) and Monte Carlo Simulation

In previous finite element simulations, all simulation parameters are deterministic and they are called deterministic simulations. However, there is always variation or uncertainty for structure dimensions, material properties, tolerances, and other parameters of electronic packages from manufacturing process or environment variability. In fact, every input variable in FE simulation should be a variable with a statistical distribution. The package parameters, including geometry parameters always have tolerances. In order to include these practical variations into consideration, the effect of parameter tolerances on solder bump reliability has been studied with the response surface methodology

(RSM) and Monte Carlo Simulation. The tolerance analysis on solder bump reliability based on FE simulation has been implemented in ANSYS® with ANSYS Probability Design System (PDS). In this study, the parameters are defined with a probability distribution in FE simulation instead of deterministic values. Therefore, the finite element simulation and probability design technique have been integrated and it is called FE analysis based probability design. Figure 6-31 shows the flow chart how probability data analysis is implemented in ANSYS®.

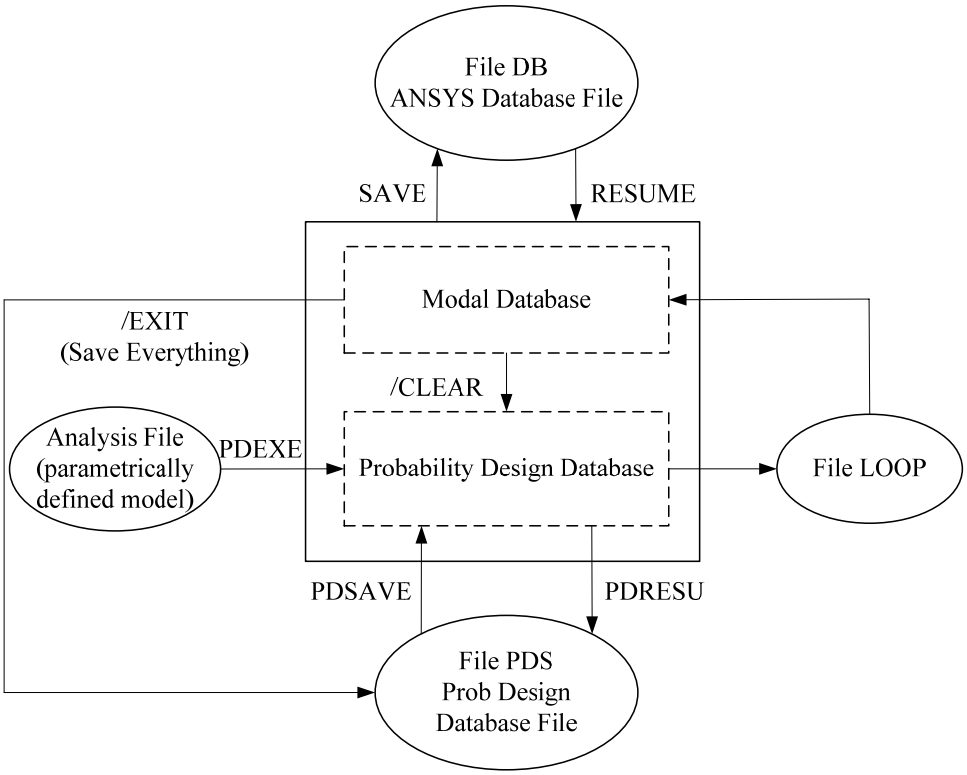


Figure 6-31 Probability Design Data Flow

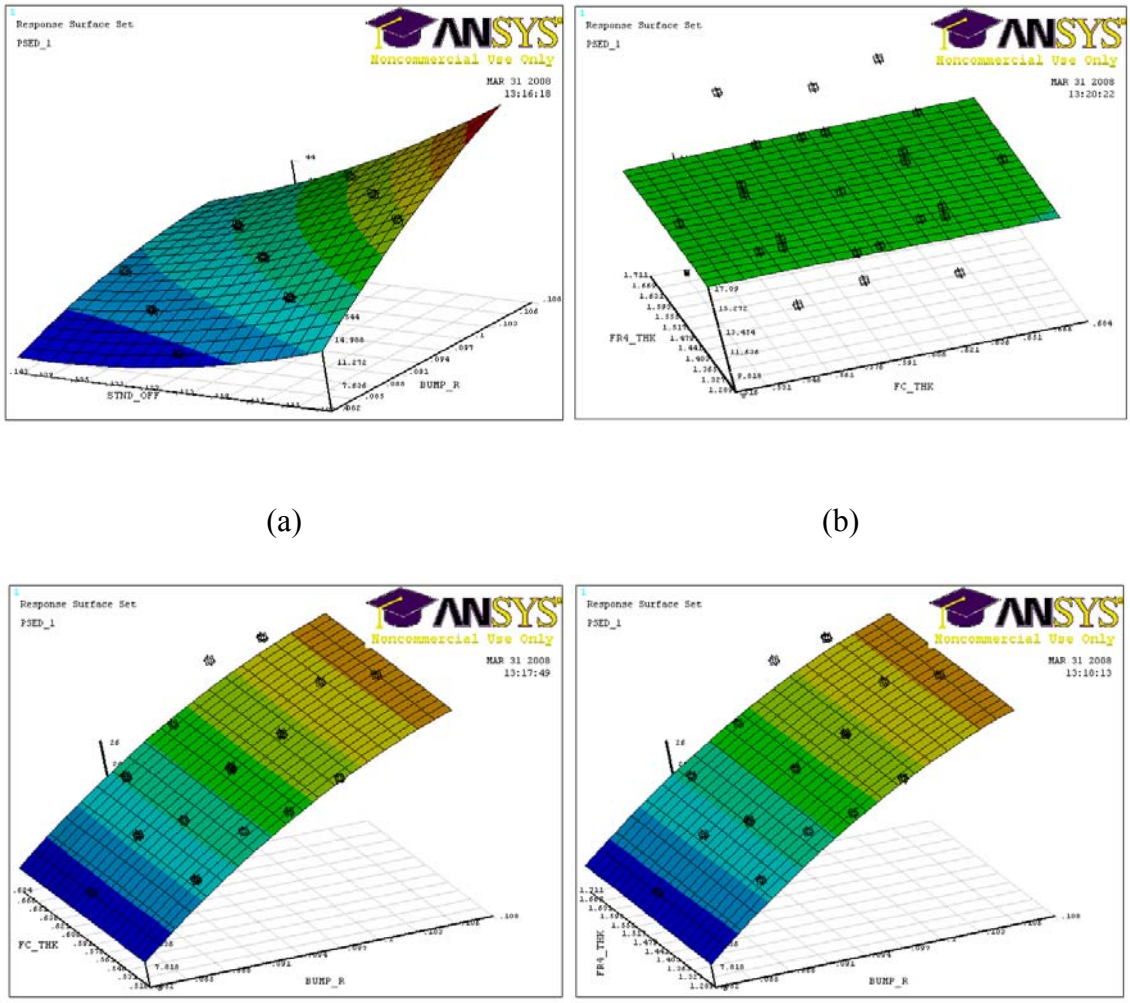
Table 6-10 lists the nominal values and realistic tolerances for the four design parameters, which are assumed to have a Gaussian distribution with a standard deviation

of ± 5% from the nominal value. All other parameters used in FE simulation, including geometry parameters and material properties, are assumed to be deterministic for simplification.

Table 6-10 Realistic tolerance for four package parameters

Parameters	Nominal value (μm)	Tolerance (3σ, μm)
Bump standoff (S_{bump})	125	± 6.3
Bump diameter (D_{bump})	190	± 4.8
Die thickness (T_{die})	600	± 30
Substrate thickness (T_{sub})	1500	± 75

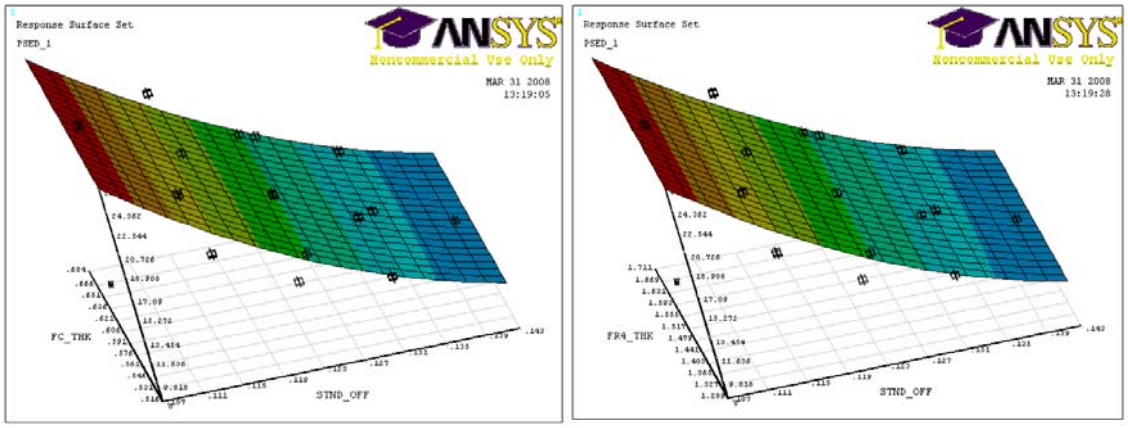
As discussed in Section 2.6, the number of simulation loops required for a response surface analysis depends on the number of random input variables and RMS often needs fewer simulation loops than Monte Carlo Simulation. In this study, CCD based RSM with four random geometric input parameters needs 25 simulation loops. A regression analysis was performed to derive regression coefficients of the approximating function after 25 simulation loops. The response surface contours of response output - plastic SED with two input variables among solder bump standoff, solder bump diameter, die thickness and substrate thickness are plotted in Figure 6-32 (a)-(f) respectively. It is shown again from Figure 6-32 that the bump diameter and standoff are two important factors which has the largest influence on solder bump reliability among the analyzed four factors. The opposite effect of bump diameter and standoff on solder bump reliability is also shown in Figure 6-32.



(a) (b)

(c) (d)

Figure 6-32 Response surface contours of plastic SED with two input parameters: (a) solder bump diameter and standoff (b) die thickness and substrate thickness (c) bump diameter and die thickness (d) bump diameter and substrate thickness (e) bump standoff and die thickness (f) bump standoff and substrate thickness



(e) (f)

Figure 6-32 continued

The approximating function, which was derived from FE simulation based probability design, was used directly in Monte Carlo Simulation. By using an approximating function in the Monte Carlo Simulation, the estimated response parameters can be evaluated thousands of times in a fraction of seconds comparing to hours or days of computation with looping in traditional Monte Carlo Simulation. The histogram of plastic SED from CCD based Monte Carlo Simulation is shown in Figure 6-33. After 10000 times of Monte Carlo Simulation, the predicted mean value of plastic SED is 17.045 MPa and the standard deviation is 3.706 MPa. The contribution plot (shown in Figure 6-34) indicates the parameters for which a small tolerance has a significant change to solder bump reliability. It is shown that the sensitive geometry parameters are solder bump standoff and diameter. The die thickness and substrate thickness are parameters whose small tolerance has a neglectable change to solder bump reliability.

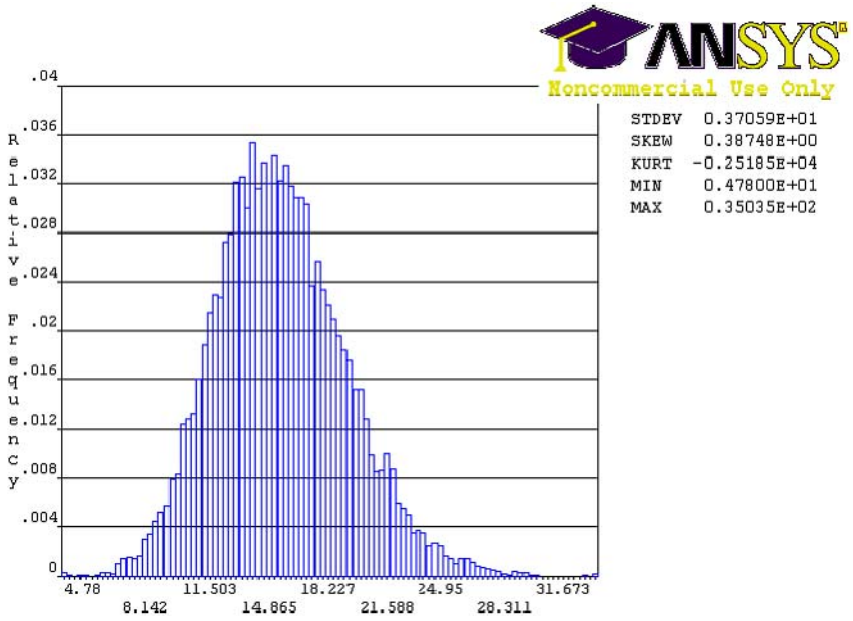


Figure 6-33 Histogram of plastic SED from CCD based Monte Carlo Simulation

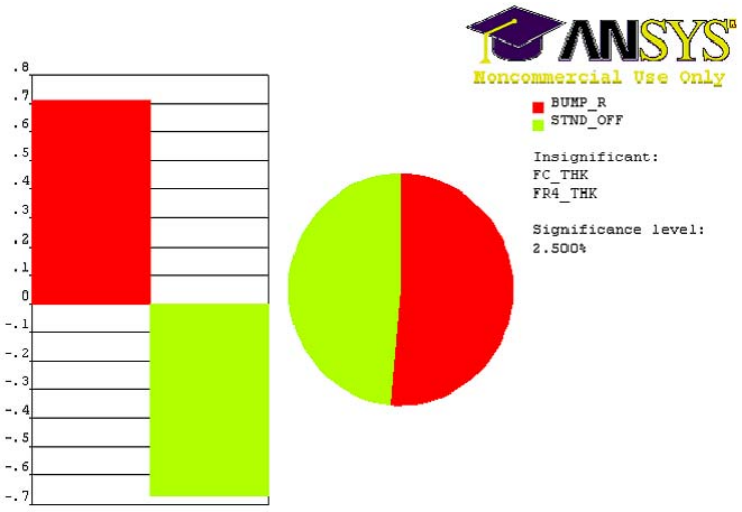


Figure 6-34 Contribution of package parameters to solder bump reliability

6.3 Chapter Summary

In summary, the thermomechanical reliability of board-level (second-level) solder bumps in land grid array packages and first-level solder bumps in flip chip packages has been studied using laser ultrasound-interferometric technique and finite element method. The study shows a strong linear correlation between failure parameter (plastic strain energy density accumulated per cycle) extracted from finite element simulation and nondestructive testing results using laser ultrasound-interferometric inspection system in thermomechanical reliability of solder bumps in flip chip packages. The effect of package parameter sensitivity and tolerance on thermomechanical reliability of solder bumps in flip chip packages has been also studied with statistical methods, including DOE, ANOVA, RSM and Monte Carlo Simulation. The different effects of package parameter variations on the thermomechanical reliability of solder bumps have been investigated.

CHAPTER 7

SOLDER BUMP CRACK INSPECTION IN HIGH-DENSITY ELECTRONIC PACKAGES

Previous chapters see the application of laser ultrasound-interferometric system under development for inspecting open bump(s), cracked solder bump(s) induced by thermal fatigue, and other bump defects induced by the manufacturing process in a variety of flip chip packages and board-level cracked solder bump(s) induced by thermal fatigue in land grid array packages. With the development and implementation of new signal processing methods, the measurement accuracy and sensitivity of inspection system have been improved for detecting small defects in these packages. The structural characteristics of electronic packages under pulsed laser loading and effect of defects on the modes and mode shapes of electronic packages have been studied using integrated analytical, numerical and experimental modal analyses approach.

With electronic packages being becoming more miniature, complex, and dense, it brings new challenges for nondestructive inspection of electronic packages at a high-speed and a low-cost. This chapter shows the preliminary application of laser ultrasound-interferometric technique for inspecting cracked solder bumps in high-density flip chip packages.

7.1 Inspection of Cracked Solder Bumps and Die Chipping in Flip Chip Packages

The flip chip package, as shown in Figure 7-1, has over thousands of lead-free solder bumps hidden between the silicon die and the substrate with bump pitch being

around 100 μm. The silicon die size is 11 mm × 11 mm. Small cracks were created on the solder bumps at one corner of one sample at end-of-line.

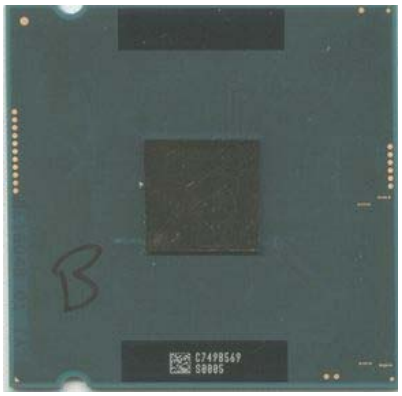
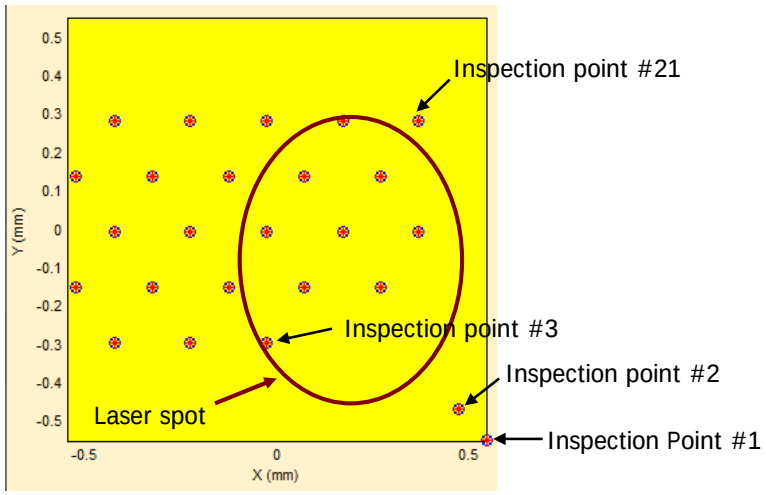
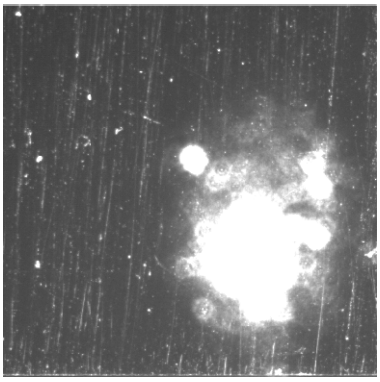


Figure 7-1 High-density flip chip package

The inspection pattern of high-density flip chip packages using laser ultrasound-interferometric inspection system is shown in Figure 7-2 (a), where the small circles indicate 25 inspection points coinciding with solder locations and the ellipse stands for laser spot. The laser spot excited on the silicon surface is shown in Figure 7-2 (b).



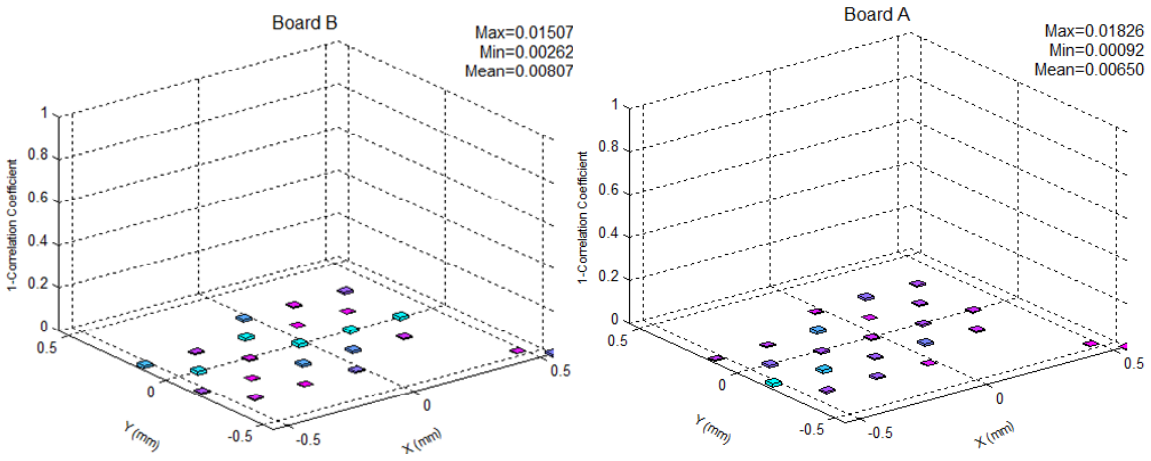
(a)



(b)

Figure 7-2 Inspection pattern of high-density flip chip package: (a) inspection pattern (b) laser spot

The measurement repeatability was studied on these flip chip samples and the results are shown in Figure 7-3 (a)-(b) for the reference chip and chip with cracked bumps respectively. The small mean values during repeatability tests for these samples (mean = 0.0065 for reference chip and mean = 0.0081 for chip with cracked solder bumps) show good repeatability.



(a) (b)

Figure 7-3 Measurement repeatability study of high-density flip chip samples: (a) reference chip (b) chip with corner cracked bumps

The time domain laser ultrasound signals from the chip with cracked solder bumps and the reference chip at inspection points #3 are shown in Figure 7-4. It is clearly obvious from Figure 7-4 that there is a larger difference in time domain responses between the chip with cracked bumps and the reference chip at inspection point #3, which shows the effect of the cracked bump on laser ultrasound responses. It is observed that the laser ultrasound response from board A, on which the flip chip has cracked solder bumps, has a larger time period and therefore a smaller mode frequency comparing to that from board B. The smaller mode frequency shows the effect of cracked solder bumps on laser ultrasound responses. The presence of cracks reduced the stiffness of solder bumps and therefore caused backwards shift of mode frequency.

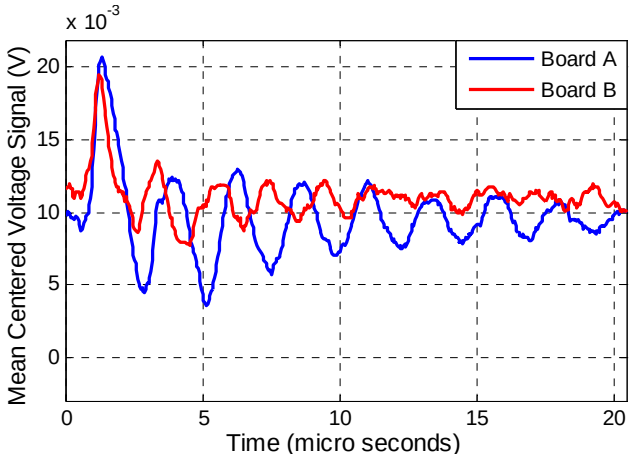


Figure 7-4 Time domain signals of flip chip with cracked solder bumps and reference chip at inspection point #3

The differences between the laser ultrasound responses from the flip chip with cracked bumps, which were repeated twice and those from the reference chip are quantified and compared in Figure 7-5. The large values shown in Figure 7-5 demonstrate that cracked bumps are detectable using laser ultrasound-interferometric technique. Comparing to the 3-D X-ray tomography technique, laser ultrasound-interferometric technique provides a fast and low-cost approach for quantifying the quality of solder bumps.

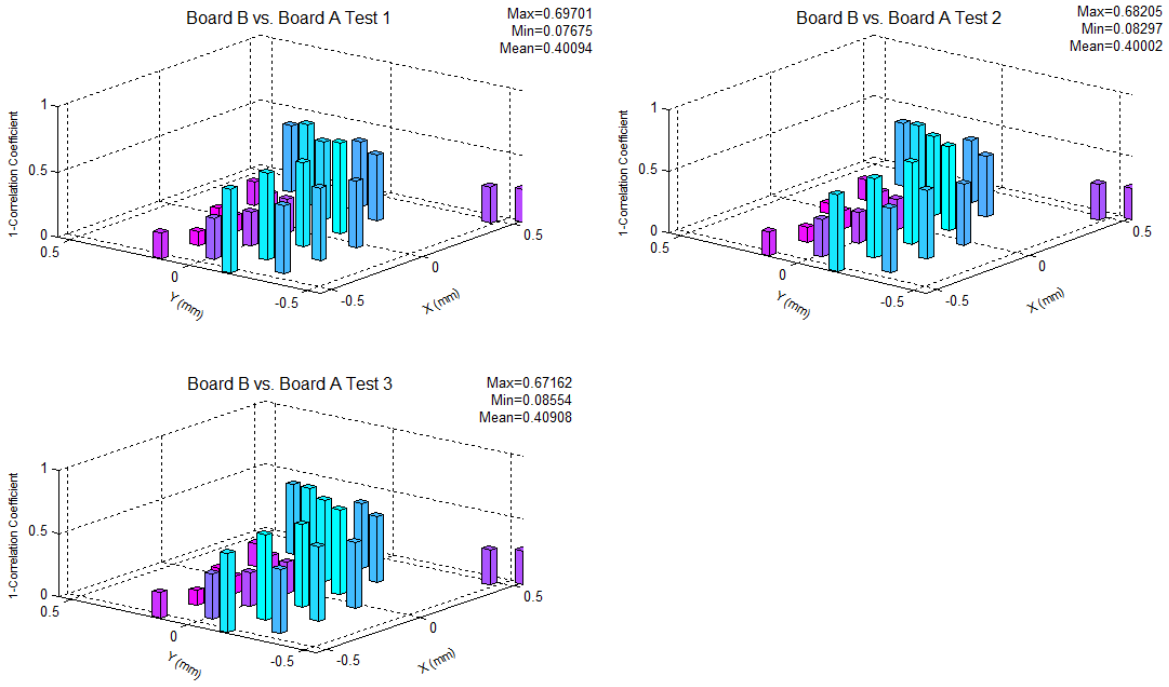


Figure 7-5 Comparison between flip chip with cracked corner bumps and reference chip

CHAPTER 8

SUMMARY, CONTRIBUTIONS AND RECOMMENDATIONS

8.1 Summary

The realization of the research objectives has enabled the laser ultrasound-interferometric inspection system under development to inspect a broad range of solder bump defects in a variety of electronic packages. The performance of this system has been improved through the development of new signal-processing methods and finite element modeling, making it a versatile, automated, and cost-effective tool. The fully developed system will be used on-line as a go/no-go quality evaluation tool, and off-line for failure analysis or process development. Therefore, the quality and reliability of electronic packages will be improved with this research by catching defects early in the manufacturing process.

In this research, quality inspection and reliability study of solder bumps in a variety of electronic packages have been successfully investigated using laser ultrasound-interferometric technique and finite element method. The simulation and experimental results have validated and led to a better understanding of the underlying physics of laser ultrasound-interferometric technique applied to electronic packaging.

8.2 Contributions

My contributions in this research can be summarized as the following:

1. Calibrated and integrated the laser ultrasound-interferometric system for solder bump quality inspection. The calibration study of laser energy density with manual stage

standoff revealed the conditions under which the ultrasound was generated in the thermoelastic regime and it matched well with theoretical analysis. The system throughput and measurement repeatability have been improved as a result of the calibration and integration.

2. Developed and implemented new signal-processing methods, including wavelet analysis and local temporal coherence analysis for processing and analyzing the nonstationary laser ultrasound signals. These methods have improved measurement accuracy and sensitivity of the inspection system. Wavelet analysis has improved inspection sensitivity by extracting and analyzing the characteristic signal components most sensitive to specific defects. Local temporal coherence analysis provides a quantitative measure of the relative change in laser ultrasound signals compared to a reference as a function of time. The local temporal coherence analysis has increased measurement accuracy and sensitivity compared to correlation coefficient method because it incorporates the ability to process nonstationary laser ultrasound signals, while correlation coefficient does not.

3. Developed an integrated analytical, numerical, and experimental modal analyses approach to predict and explain structural characteristics and the effect of defects on structural characteristics of the electronic packages excited with pulsed laser loading. An analytical model based on the Power Balance Law has been developed to quickly predict the natural frequencies of a given package structure and to examine how they are influenced by the package geometries and solder bump defects. A finite element model has been developed to extract modes and mode shapes of a given package structure and study how to correlate solder bump defects with mode shift and mode shape

evolution. The developed integrated modal analyses approach can also predict mode frequencies and corresponding mode shapes most sensitive to specific interconnect defects for further signal processing with wavelet analysis. It also leads to a better understanding of the underlying physics of experimental phenomenon.

4. Conducted experimental modal analysis to extract mode frequencies from experimental data obtained by using the laser ultrasound-interferometric inspection system. The experimental results have validated analytical and finite element modal analyses.

5. Developed a finite element model to study the thermomechanical reliability of solder bumps in flip chip packages with the viscoplastic constitutive law, which was integrated into the model to represent the inelastic stress/strain behavior of eutectic tin-lead solder under cyclic thermal loads. The finite element analysis reveals that corner solder bumps are the most critical ones under cyclic thermal loading and would fail first since they always experience the highest plastic strain energy density. The finite element analysis also shows that the critical area in the critical solder bump with maximum plastic SED lies at the elements close to the BLM layer and cracks initiate from that area. All these simulation results have a good agreement with cross-section observations of solder bump cracks.

6. Carried out systematic study on the thermomechanical reliability of board-level (second-level) solder bumps in land grid array packages and first-level solder bumps in flip chip packages with laser ultrasound-interferometric technique and finite element method. For land grid array packages on the organic substrates, board-level solder bump reliability has been studied and laser ultrasound inspection results verify that they can

withstand 1000 thermal cycles and therefore have a high reliability satisfying design requirements under cyclic thermal loading. Solder bump defects induced by further thermal fatigue have been detected after 2000 thermal cycles using laser ultrasound-interferometric technique. For flip chip packages, the crack propagation (quality degradation) of solder bumps with the increasing number of thermal cycles has been successfully tracked and quantified using laser ultrasound-interferometric inspection system. The comparisons between laser ultrasound, resistance measurement and CSAM show that the laser ultrasound technique has advantages for inspecting solder bump fatigue cracks in flip chip packages. Meanwhile, this study also shows a good correlation between the failure parameter (plastic strain energy density) extracted from finite element simulation and nondestructive testing using the laser ultrasound-interferometric inspection system.

7. Carried out study of package geometric parameters sensitivity and tolerance on the thermomechanical reliability of solder bumps in flip chip packages with statistical methods, including DOE, ANOVA, RSM and Monte Carlo Simulation. This study shows that the variations from package parameters have different effects on solder bump reliability. The solder bump standoff and diameter are two most important factors that influence solder bump thermal reliability among the four factors studied including die thickness and substrate thickness too. The larger the solder bump standoff, the higher is the bump reliability. The larger the solder bump diameter, the lower is the bump reliability. This study is of great help for design optimization of electronic packages for higher reliability.

8. Carried out study on qualification of a variety of electronic packages with various representative solder bump defects, including open bump(s), cracked bumps induced by the thermal fatigue, manufacturing defects in various flip chip packages, cracked board-level solder bumps induced by the thermal fatigue in land grid array packages, and end-of-line cracked solder bumps in high-density and fine-pitch flip chip packages. These studies significantly expand the application scope of laser ultrasound-interferometric inspection system, making it a versatile inspection tool.

In summary, I developed a methodology for quality evaluation and reliability study of solder bumps in electronic packages using the non-destructive and non-contact laser ultrasound-interferometric technique, finite element and statistical methods in this research work. This methodology includes the following aspects: 1) inspection pattern – specific inspection patterns are created according to inspection purpose and package formats, 2) laser pulse energy density calibration – specific laser pulse power and excitation laser spot size are selected in terms of package formats, 3) processing and analysis methods, including integrated analytical, finite element and experimental modal analyses approach, advanced signal processing methods and statistical analysis method, 4) approach combining modal analysis and advanced signal processing to improve measurement sensitivity of laser ultrasound-interferometric inspection technique, and 5) calibration curve using energy based simulation method and laser ultrasound inspection technique to predict thermomechanical reliability of solder bumps in electronic packages.

8.3 Recommendations

8.3.1 Quality Inspection Using Virtual Reference

In the laser ultrasound-interferometric inspection system under development, the principle underlying how this system evaluates the package quality is the quantification of the differences in transient out-of-plane displacement responses between the packages to be tested and a known-good-package. A known-good-package is always required and used as the reference in experiments. Therefore, a known-good-package is critical since the quality evaluation of other packages to be tested is based on this known-good-package. However, it is difficult to construct a purely perfect package in actual manufacturing process and it is difficult to verify whether one package is totally defect-free. Meanwhile, there are always differences among known-good-packages due to manufacturing variation though this kind of difference might be small.

The idea of virtual reference is proposed using finite element simulation to replace actual reference package. With the help of the constructed virtual reference using FE simulation, no actual known-good-package is required and the quality evaluation of the packages is based on the quantification of the difference between measured transient displacement responses from the packages to be tested and constructed virtual reference from FE simulation. The steps to construct the virtual reference with finite element analysis include: 1) build a finite element model to represent the process from pulsed laser radiation to transient temperature distribution in the electronic package under pulsed laser loading, 2) build another finite element model to represent the process from transient temperature distribution to the transient stress/strain field in the electronic package, 3) extract the transient out-of-plane displacement responses on the package

surface from stress/strain field in the electronic package. The virtual reference can be built being defect-free and the extracted responses can be used the reference response for quality evaluation of other packages. This is a multi-physics simulation process integrating transient thermal analysis induced by pulsed laser loading and transient structural analysis under temperature field from previous step. Though this is a complicated analysis process, there is no need to model complex inelastic behavior of solder material since pulsed laser loading with duration in the nanosecond scale only affects the temperature field on the silicon die surface with little penetration into the package from the preliminary study and other literature. At the same time, the effect of manufacturing variation on the responses of a good package under laser loading can also be studied. The idea of virtual reference has been already used in several other areas. In the area of image processing, a generated virtual reference picture was used as a reference instead of an actual sequence picture in the temporal prediction [Zhang G., 2005]. In the area of microelectronics, FEA has also been used to model the response of an assembly to compressive loads and variation in the mechanical load system components [Lopez L., 2007]. This approach allows virtual qualification of socket assemblies without carrying out expensive experiments.

8.3.2 Pulsed Laser Excitation with Fiber Phased Array Technique

In the configuration of current laser ultrasound-interferometric inspection system, a single laser fiber with the diameter of 600 μm is used in the laser fiber optic beam delivery system to deliver pulsed laser to the electronic package. With electronic packages becoming more complex and dense; the laser power transmitted through single fiber is not high enough to excite transient out-of-plane displacement responses on the

package surface with acceptable signal to noise ratio. At the same time, with the laser power increasing, the excitation spot size should be increased to control laser energy density to avoid damage to the electronic packages. A fiber phased array is a tool to steer and amplify the ultrasound field in a particular direction and can be used to enhance the signal propagation in the region of interest. This fiber phased array technique has been implemented in ultrasound generation system and used for quality control of arc welding process [Mi B., 2003]. This technique has also been used in endoscopic imaging by building multicore microstructure fiber phased array.

8.3.3 Study on Effects of Laser Excitation and Interferometer Inspection Positions on Measurement Sensitivity

In current experiments, laser pulses are excited at the center of electronic packages for simple electronic packages, including flip chip packages and chip scale packages. As to the complex or high-density electronic packages, pulsed laser can be excited at the position close to the area of interest. The interferometer inspection positions are normally selected directly on solder bumps. During the recent experimental study on high-density flip chip samples, transient displacement responses with different amplitude and phase were excited and captured when the pulsed laser was excited at different locations. It will be a challenging but important topic to study the effect of laser excitation and interferometer inspection positions on measurement sensitivity with finite element simulation and experimental validation. The measurement sensitivity of the inspection system will be improved by selecting optimal excitation and detection positions on the package surface.

8.3.4 Expansion of Application Scope

The project started with a focus on quality evaluation of solder bumps in flip chip packages after reflow process but before underfill process. A lot of money and time can be saved if defective solder bumps are detected before the underfill process and it makes rework of electronic packages possible. In previous and current research work, various solder bump defect types, including missing, open, misaligned, and cracked solder bumps have been studied in different formats of electronic packages, including flip chip packages, chip scale packages, land grid arrays, and high-density flip chip packages. The application scope of current prototype system can be expanded to 3-D packages, high-density and other complex electronic packages. One possible application is crack detection of silicon wafers and it is a very attractive research and application area. Since silicon wafer (8 or 12 inch) is much larger than current small-size flip chip packages, wave propagation principle can be applied to interpret captured responses and localize cracks within silicon wafers. Preliminary experiments have demonstrated this application. One other possible application is quality evaluation of wafer level packaging, which is currently a hot research area in microelectronic industry. Another possible application of the current system is the characterization and integrity evaluation of MEMS devices.

APPENDIX A

MATLAB CODES FOR WAVELET ANALYSIS ALGORITHM

Matlab Codes for Wavelet Analysis Algorithm:

```
function varargout = pushbutton_wavelet_Callback(h, eventdata, handles, varargin)
current_fig = handles.current_fig;
dirs = handles.dirs;
%get number of detection points
total_dect_pts = str2num(get(handles.text_dect_pts_mod,'String'));
total_samp = str2num(get(handles.text_tot_samp_mod,'String'));
StartN = str2num(get(handles.edit_start,'String'));
EndN = str2num(get(handles.edit_end,'String'));
reference = get(handles.listbox2_scans,'String');
reference_selected = get(handles.listbox2_scans,'Value');
comparisons = get(handles.listbox3_scans,'String');
comparisons_selected = get(handles.listbox3_scans,'Value');
scan_dir_index = handles.scan_dir_index;
samp_rate = str2num(get(handles.text_samp_rate_mod,'String'));
load(handles.mat_file);
wave_analy_point = handles.plots_selected;


if length(comparisons_selected) >= 5,
   subplot_rows = 2;
```

```
    subplot_columns = 3;
elseif length(comparisons_selected) >= 3,
    subplot_rows = 2;
    subplot_columns =2;
else
    subplot_rows = 1;
    subplot_columns =1;
end
%Check for points to Suppress
%check for default and plot_selected for "all"
if isempty(get(handles.edit_suppress,'String')),
    for i = 1:total_dect_pts
        plots_selected(i) = i;
    end
else
    index = 0;
    for i = 1:total_dect_pts
        match = 0;
        index = index+1;
        for j = 1:length(handles.plots_suppressed)
            if i == handles.plots_suppressed(j)
                match = 1;
                index = index-1;
```

```
        end
    end
    if match == 0,
        plots_selected(index) = i;
        ERnew(index,:) = ERxy(i,:);
    end
  end
  total_dect_pts = str2num(get(handles.text_dect_pts_mod,'String'))-
length(handles.plots_suppressed);
  ERxy = ERnew;
end

%Read in Reference Data
for i = 1:total_dect_pts,
  cd(dirs{scan_dir_index(reference_selected)})
  fid = fopen(strcat(reference{reference_selected},int2str(plots_selected(i)),'.txt'));
  file_temp = fscanf(fid,'%f',total_samp);
  fclose(fid);
  ref_data(:,i) = file_temp(StartN:EndN);
  if get(handles.checkbox_ER_normalize,'Value') == 1,
    ref_data(:,i) = (ref_data(:,i) - mean(file_temp));
  end
end
```

```
%Read in Comparison Data
for i = 1:length(comparisons_selected);
   for j = 1:total_dect_pts,
      index = comparisons_selected(i);
      cd(dirs{scan_dir_index(index)})
      fid = fopen(strcat(comparisons{index},int2str(plots_selected(j)),'.txt'));
      file_temp = fscanf(fid,'%f',total_samp);
      fclose(fid);
      comp_data(:,j,i) = file_temp(StartN:EndN)';
      if get(handles.checkbox_ER_normalize,'Value') == 1,
         comp_data(:,j,i) = (comp_data(:,j,i) - mean(file_temp));
      end
   end
end

ref_copy=ref_data(:,wave_analy_point);

decompose_level=6;
% Originally 'bior4.4', trying 'db4' this time % wave_string='bior4.4';
wave_string='db4' %wave_string='db10';
fs=samp_rate;
coef_threshold=1/8;
% Signal Denoising and comparison with original ones
```

```
TPTR='heursure'; %TPTR='rigrsure';

SORH ='s';

SCAL='sln'; %SCAL='mln'; %SCAL='one';

xd=wden(ref_data(:,wave_analy_point),TPTR,SORH,SCAL,decompose_level,wave_stri
ng);


figure_series=100;

figure(figure_series);

figure_series=figure_series+1;

subplot(2,1,1);

plot(StartN/fs:1/fs:EndN/fs,ref_data(:,wave_analy_point));

title('Original Signal');

xlabel('Time(s)');

ylabel('Amplitude');

grid on

subplot(2,1,2);

plot(StartN/fs:1/fs:EndN/fs,xd);

title('Denoised Signal');

xlabel('Time(s)');

ylabel('Amplitude');

grid on

% Defining the denoised signal as raw signal

ref_copy=xd;
```

```
% Wavelet Decomposition
[C,L] = wavedec(ref_copy,decompose_level,wave_string);
cA = appcoef(C,L,wave_string,decompose_level);

dCell = detcoef(C,L,[1:decompose_level]);
[row_num,column_num]=size(dCell);

% Wavelet Decomposition Coefficients
figure(figure_series);
figure_series=figure_series+1;

subplot_num=round((decompose_level+1)/2);
% Original Signal
subplot(subplot_num,2,1);
plot(cA);
title('Approximation Coefficient');
grid on
%cD_Rms=zeros(decompose_level,1);

for i=1:decompose_level
   cD=dCell{1,i};
   subplot(subplot_num,2,i+1);
   plot(cD);
```

```
    grid on
    string=strcat('D',int2str(i),' Coefficients');
    title(string);
end

% Stem for Wavelet Decomposition Coefficients
figure(figure_series);
figure_series=figure_series+1;

subplot_num=round((decompose_level+1)/2);
% Original Signal
subplot(subplot_num,2,1);
stem(cA,'b.');
title('Approximation Coefficient');
grid on

for i=1:decompose_level
    cD=dCell{1,i};
    subplot(subplot_num,2,i+1);
    stem(cD,'b.');
    grid on
    string=strcat('D',int2str(i),' Coefficients');
    title(string);
```

```
end

% Wavelet Approximation and Detailed Components
figure(figure_series)
figure_series=figure_series+1;
subplot_num=round((decompose_level+2)/2);
subplot(subplot_num,2,1);
plot(StartN/fs:1/fs:EndN/fs,ref_copy);
title('Original Signal');
xlabel('Time(s)');
ylabel('Amplitude');
grid on
Aa = wrcoef('a',C,L,wave_string,decompose_level);
subplot(subplot_num,2,2);
plot(StartN/fs:1/fs:EndN/fs,Aa);
title('Approximation A');
xlabel('Time(s)');
ylabel('Amplitude');
grid on

for i=1:decompose_level
   Dd=wrcoef('d',C,L,wave_string,i);
   if (i==5)
```

```
        ref_new=Dd;
    end
    subplot(subplot_num,2,i+2);
    plot(StartN/fs:1/fs:EndN/fs,Dd);
    string=strcat('Detail D ',int2str(i));
    title(string);
    xlabel('Time(s)');
    ylabel('Amplitude');
    grid on
end

% Signal Reconstruction after assuming the approximation Coefficients zero
non_appro=0;
if (non_appro==1)
   for i=1:1:L(1)
    C(i,1)=0;
   end
end
    ref_copy=waverec(C,L,wave_string);

% Power Spectrum of Original and Approximation Signals
        num_sample=4*length(ref_copy);
        Y1 = fft(ref_data(:,wave_analy_point),(EndN-StartN+1)*4);
```

```
        N = length(Y1);
        Y1(1) = [];
        Pyy1 = abs(Y1(1:N/2)).^2;
        Y2 = fft(xd,(EndN-StartN+1)*4);
        N = length(Y2);
        Y2(1) = [];
        Pyy2 = abs(Y2(1:N/2)).^2;
        Pyy_max=max(Pyy1);


f = fs*[0:1/num_sample:(1/2-1/num_sample)];
figure(figure_series)
figure_series=figure_series+1;
subplot(2,1,1);
plot(f,Pyy1(1:length(f)));
grid on
title('Power Spectrum of Original Signal');
xlabel('frequency(Hz)');
ylabel('Signal Power');
axis([0 1e6 0 Pyy_max]);
subplot(2,1,2);
plot(f,Pyy2(1:length(f)));
grid on
xlabel('frequency(Hz)');
```

```
ylabel('Signal Power');
title('Power Spetrum after Removing Approximation Signal');
axis([0 1e6 0 Pyy_max]);

% Short Time Fourier Transform
clow=0.00; chigh=1.0;
clim = [clow chigh];
figure(figure_series);
figure_series=figure_series+1;
window_size=256;
over_lap=128;
subplot(2,1,1);
[Bb,Ff,Tt]=specgram(ref_copy,window_size,fs,gausswin(window_size),over_lap);
imagesc(Tt,Ff,abs(Bb),clim);
axis xy
title('Short Time Fourier Transform');
xlabel('time(s)');
ylabel('frequency(Hz)');

axis([StartN/fs (EndN-over_lap)/fs 0 1e6]);
colorbar

subplot(2,1,2);
```

```
contour(Tt,Ff,abs(Bb));
title('Short Time Fourier Transform(Contour)');
xlabel('time(s)');
ylabel('frequency(Hz)');
axis([StartN/fs (EndN-over_lap)/fs 0 1e6]);
colorbar

% Time-Frequency Spectrum Analysis with Wavelet
clow=0.00; chigh=0.08;
clim = [clow chigh];
figure(figure_series);
figure_series=figure_series+1;
delta=1/fs;
wave_f=1000:1e3:1e6;

% Originally 'bior4.4', Trying 'db4'
wave_string='bior4.4';
center_frq=centfrq(wave_string);
scales=center_frq/delta./wave_f;
coefs=cwt(ref_copy,scales,wave_string);
imagesc(StartN/fs*10^6:1/fs*10^6:EndN/fs*10^6,wave_f/10^3,abs(coefs),clim);
title('Time-Frequency Spectrum with Wavelet');
xlabel('Time(us)');
```

```
ylabel('Frequency(KHz)');
axis xy
colorbar
%axis([StartN/fs EndN/fs 0 2e6]);

% Comparison time-domain signal and wavelet time-frequency spectrum
figure(figure_series);
figure_series=figure_series+1;
subplot(2,1,1)
plot(StartN/fs:1/fs:EndN/fs,ref_copy);
title('Denoised Signal');
xlabel('Time(s)');
ylabel('Amplitude');
grid on

subplot(2,1,2);
clow=0.00; chigh=0.08;
clim = [clow chigh];
imagesc(StartN/fs:1/fs:EndN/fs,wave_f,abs(coefs),clim);
title('Time-Frequency Spectrum with Wavelet');
axis xy
xlabel('Time(s)');
ylabel('Frequency(Hz)');
```

```
%colormap('HSV');

colormap('default');

colorbar;

% New Part1: Time-Domain Filtring and Removing Approximation Component,

% Follow the previous steps to calculate time-domian signal Error Ratio

% & Correlation to check whether these two steps can improve the resolution


% Wavelet Decompose Level

decompose_level=8;

wave_string='db4';

fs=samp_rate;


% Signal Denoising and comparison with original ones

TPTR='heursure';

SORH ='s';

SCAL='sln';


% Reference Signal Denoising and Decomposition

[ref_xd(:,i),ref_cxd(:,i),ref_lxd(:,i)]=wden(ref_data(:,i),TPTR,SORH,SCAL,decompose_l
evel,wave_string);

[comp_xd(:,i,j),comp_cxd(:,i,j),comp_lxd(:,i,j)]=wden(comp_data(:,i,j),TPTR,SORH,SC
AL,decompose_level,wave_string);


for i=1:1:total_dect_pts
```

```
    [ref_cxd(:,i),ref_lxd(:,i)]=wavedec(ref_data(:,i),decompose_level,wave_string);
end

% Comparison Signal Denoising and Decomposition
for j=1:1:length(comparisons_selected)
 for i=1:1:total_dect_pts

[comp_cxd(:,i,j),comp_lxd(:,i,j)]=wavedec(comp_data(:,i,j),decompose_level,wave_strin
g);
end
end

for i=1:1:total_dect_pts
  ref_dCell(:,i) = detcoef(ref_cxd(:,i),ref_lxd(:,i),[1:decompose_level]);
end

for j=1:1:length(comparisons_selected)
 for i=1:1:total_dect_pts
  comp_dCell(:,i,j) = detcoef(comp_cxd(:,i,j),comp_lxd(:,i,j),[1:decompose_level]);
 end
end

% Reference and Comparison Signals Reconstruction
recons_level=7;
```

```
for i=1:1:total_dect_pts

  ref_data_recons(:,i) = wrcoef('d',ref_cxd(:,i),ref_lxd(:,i),wave_string,recons_level);

end


for j=1:1:length(comparisons_selected)

 for i=1:1:total_dect_pts

  comp_data_recons(:,i,j) =
wrcoef('d',comp_cxd(:,i,j),comp_lxd(:,i,j),wave_string,recons_level);

 end

end


num_sample=4*length(ref_data_recons(:,wave_analy_point));

       Y1 = fft(ref_data_recons(:,wave_analy_point),(EndN-StartN+1)*4);

       N = length(Y1);

       Y1(1) = [];

       Pyy1 = abs(Y1(1:N/2)).^2;

       Y2 = fft(comp_data_recons(:,wave_analy_point,1),(EndN-StartN+1)*4);

       N = length(Y2);

       Y2(1) = [];

       Pyy2 = abs(Y2(1:N/2)).^2;

       Pyy_max=max(Pyy1);

f = fs*[0:1/num_sample:(1/2-1/num_sample)];

figure(figure_series)

figure_series=figure_series+1;
```

```
subplot(2,1,1);

plot(f,Pyy1(1:length(f)));

grid on

title('Power Spectrum');

xlabel('frequency(Hz)');

ylabel('Signal Power');

axis([0 2e6 0 Pyy_max]);

subplot(2,1,2);

plot(f,Pyy2(1:length(f)));

grid on

xlabel('frequency(Hz)');

ylabel('Signal Power');

title('Power Spetrum');

axis([0 2e6 0 Pyy_max]);


% % % %######## facilitate AutoComp######Start here#########

if get(handles.checkbox_AutoComp,'Value')

       for j = 1:36,

          ER(j)=ERcalc(ref_data(1:(EndN-StartN+1),j),(ref_data(1:(EndN-
StartN+1),j+12)));

       end

   for i = 1:length(comparisons_selected),

       for j = 1:24
```

```
            ER(j,i)=ERcalc(comp_data(1:(EndN-StartN+1),j,i),(comp_data(1:(EndN-
StartN+1),j+24,i)));

        end

    end

    meanER=mean(ER)'

    figure

    subplot(1,2,1)



    plot(ER)

    ylabel('ER')

    legend(comparisons{comparisons_selected(:)});

     if(get(handles.checkbox_ER_normalize,'Value')==1) MeanCtrtag='Yes';

     else MeanCtrtag='No';

     end

     title({['Autocomparison: point i(i=1:24) compares to points i+24'];...['Data Range:'
num2str(StartN) '~' num2str(EndN) '    MeanCtr:',MeanCtrtag]},'FontSize',8)

    subplot(1,2,2)

    for i = 1:length(comparisons_selected),

        bar(i,meanER(i))

        hold on

    end

    legend(comparisons{comparisons_selected(:)});



    ylabel('meanER')
```

```
    title('36 comparisons\phi average','FontSize',8)
else
    for i = 1:length(comparisons_selected)
        for j = 1:total_dect_pts,
            Comp_Num=256;
  ER(j,i)=1-
corr2(ref_data_recons(1:Comp_Num,j),comp_data_recons(1:Comp_Num,j,i));
        end
    end


    total_fig = ceil(length(comparisons_selected)/(subplot_rows*subplot_columns));
    for j = 1:total_fig,
        total_plot = j*subplot_rows*subplot_columns;
        if total_plot <= length(comparisons_selected),
            k = subplot_rows*subplot_columns;
        else
            k = (subplot_rows*subplot_columns) - (total_plot -
length(comparisons_selected));
        end
        figure(current_fig+j)
        for i = 1:k,
            subplot(subplot_rows, subplot_columns , i)
            current_plot = (j-1)*subplot_rows*subplot_columns + i;
            ER_current = ERxy;
```

```
            ER_current(:, 3) = ER(:,current_plot);
            if get(handles.checkbox_zaxis,'Value')
               z_scale = str2num(get(handles.edit_zaxis,'String'));
            else
               z_scale = 1.25*max(ER_current(:,3));
            end
            SuperAnalysis('ERvis_Callback',gcbo,[],guidata(gcbo),...
               ER_current, handles.bar_width, device_size,z_scale)
            xlabel('X (mm)','FontSize',8,'rotation',30)
            ylabel('Y (mm)','FontSize',8,'rotation',-30)
            zlabel('','FontSize',8)
            if(get(handles.checkbox_ER_normalize,'Value')==1) MeanCtrtag='Yes';
            else MeanCtrtag='No';
            end


title({[reference{reference_selected(1)} ' (Ref) vs. '
comparisons{comparisons_selected(current_plot)}];...['Data Range:' num2str(StartN) '~'
num2str(EndN) '   MeanCtr:',MeanCtrtag]},'FontSize',8)

        end
    end
    handles.current_fig = current_fig+total_fig;
    guidata(h, handles);
    ER
End
```

APPENDIX B

MATLAB CODES FOR LOCAL TEMPORAL COHERENCE ANALYSIS ALGORITHM

Matlab Codes for Local Temporal Coherence Algorithm:

```
function varargout = pushbutton_LTC_Callback(h, eventdata, handles, varargin)
current_fig = handles.current_fig;
dirs = handles.dirs;
total_dect_pts = str2num(get(handles.text_dect_pts_mod,'String'));
total_samp = str2num(get(handles.text_tot_samp_mod,'String'));
StartN = str2num(get(handles.edit_start,'String'));
EndN = str2num(get(handles.edit_end,'String'));
reference = get(handles.listbox2_scans,'String');
reference_selected = get(handles.listbox2_scans,'Value');
comparisons = get(handles.listbox3_scans,'String');
comparisons_selected = get(handles.listbox3_scans,'Value');
scan_dir_index = handles.scan_dir_index;
samp_rate = str2num(get(handles.text_samp_rate_mod,'String'));
load(handles.mat_file)

if length(comparisons_selected) >= 5,
   subplot_rows = 2;
   subplot_columns = 3;
```

```
elseif length(comparisons_selected) >= 3,
    subplot_rows = 2;
    subplot_columns =2;
else
    subplot_rows = 1;
    subplot_columns =1;
end
%Check for points to Suppress
if isempty(get(handles.edit_suppress,'String')),
    for i = 1:total_dect_pts
        plots_selected(i) = i;
    end
else
    index = 0;
    for i = 1:total_dect_pts
        match = 0;
        index = index+1;
        for j = 1:length(handles.plots_suppressed)
            if i == handles.plots_suppressed(j)
                match = 1;
                index = index-1;
            end
        end
```

```
        if match == 0,
            plots_selected(index) = i;
            ERnew(index,:) = ERxy(i,:);
        end
    end
    total_dect_pts = str2num(get(handles.text_dect_pts_mod,'String'))-
length(handles.plots_suppressed)
    ERxy = ERnew;
end


%Read in Reference Data
for i = 1:total_dect_pts,
    cd(dirs{scan_dir_index(reference_selected)})
    fid = fopen(strcat(reference{reference_selected},int2str(plots_selected(i)),'.txt'));
    file_temp = fscanf(fid,'%f',total_samp);
    fclose(fid);
    ref_data(:,i) = file_temp(StartN:EndN);
    if get(handles.checkbox_ER_normalize,'Value') == 1,
        ref_data(:,i) = (ref_data(:,i) - mean(file_temp));
    end
end
%Read in Comparison Data
for i = 1:length(comparisons_selected);
    for j = 1:total_dect_pts,
```

```
        index = comparisons_selected(i);
        cd(dirs{scan_dir_index(index)})
        fid = fopen(strcat(comparisons{index},int2str(plots_selected(j)),'.txt'));
        file_temp = fscanf(fid,'%f',total_samp);
        fclose(fid);
        comp_data(:,j,i) = file_temp(StartN:EndN)';
        if get(handles.checkbox_ER_normalize,'Value') == 1,
           comp_data(:,j,i) = (comp_data(:,j,i) - mean(file_temp));
        end
    end
end

point_length=EndN-StartN+1;

for i=1:length(comparisons_selected)
    DSC_cor_sum=0;
    DSC_ref_sum=0;
    DSC_com_sum=0;
    for j=1:total_dect_pts
        ref_mean(j)=mean(ref_data(:,j));
        com_mean(j)=mean(comp_data(:,j,i));
        for k=1:point_length
           DSC_cor_sum=DSC_cor_sum+(ref_data(k,j)-ref_mean(j))*(comp_data(k,j,i)-
com_mean(j));
```

```
        DSC_ref_sum=DSC_ref_sum+(ref_data(k,j)-ref_mean(j))^2;
        DSC_com_sum=DSC_com_sum+(comp_data(k,j,i)-com_mean(j))^2;
      end
   end
   DSC_correlation(i)=1-DSC_cor_sum/sqrt(DSC_com_sum*DSC_ref_sum);
end
DSC_correlation


%Calculation
if get(handles.checkbox_AutoComp,'Value')
   for i = 1:length(comparisons_selected),
      for j = 1:12
            ER(j,i)=1-corr2(comp_data(1:(EndN-StartN+1),j,i),(comp_data(1:(EndN-
StartN+1),37-j,i)));
        end
   end


   ER=[ER(:,2:10), ER(:,1)]
   comparisons_selected=[comparisons_selected(2:10),comparisons_selected(1)];
   cmap=jet;
   sizecmap=size(cmap);
   Ncycles=[25 35 45 50 55 60 65 75 90 110];
   meanER=mean(ER)*2
   sizeER=size(ER)
```

```
    figure
    subplot(2,1,1)
    for i=1:sizeER(2)
    plot(ER(:,i),'color',cmap(i*floor(sizecmap(1)/sizeER(2)),:))
    hold on
    end
    ylabel('1-corr')
    legend(comparisons{comparisons_selected(:)});
     if(get(handles.checkbox_ER_normalize,'Value')==1) MeanCtrtag='Yes';
     else MeanCtrtag='No';
     end
     title({['Autocomparison: point i(i=1:12) compares to points 37-i'];...['Data Range:' num2str(StartN) '~' num2str(EndN) '    MeanCtr:',MeanCtrtag]},'FontSize',8)
    subplot(2,1,2)
    for i = 1:length(comparisons_selected),
       bar(i,meanER(i))
       hold on
    end
    legend(comparisons{comparisons_selected(:)});
    ylabel('mean of 1-corr')
    title('12 comparisons average','FontSize',8)
else
    for i = 1:length(comparisons_selected),
       for j = 1:total_dect_pts,
```

```
          ER(j,i)=1-(corr2(ref_data(1:(EndN-StartN+1),j),(comp_data(1:(EndN-
StartN+1),j,i))));

       end

   end


% Latest Version ---Jin's Modification combined with step April 25, 2007 ******

 win_size=512;

 win_step=128;

 lag_width=2*win_size-1;


 for k=1:1:(4096-win_size)/win_step+1;

   for i = 1:length(comparisons_selected),

      for j = 1:total_dect_pts,

% ER(j,i)=corr2(ref_data((win_step*(k-1)+1):(win_step*(k-
1)+win_size),j),(comp_data((win_step*(k-1)+1):(win_step*(k-1)+win_size),j,i)));

 ER(j,i)=corr2(ref_data(1:(win_step*(k-1)+win_size),j),(comp_data(1:(win_step*(k-
1)+win_size),j,i)));

% ER(j,i)=corr2(ref_data(1:(EndN-StartN+1),j),(comp_data(1:(EndN-StartN+1),j,i));


% X_c=xcorr(ref_data((win_step*(k-1)+1):(win_step*(k-
1)+win_size),j),comp_data((win_step*(k-1)+1):(win_step*(k-1)+win_size),j,i));

% Ref_c=xcorr(ref_data((win_step*(k-1)+1):(win_step*(k-
1)+win_size),j),ref_data((win_step*(k-1)+1):(win_step*(k-1)+win_size),j),0);

% Comp_c=xcorr(comp_data((win_step*(k-1)+1):(win_step*(k-
1)+win_size),j,i),comp_data((win_step*(k-1)+1):(win_step*(k-1)+win_size),j,i),0);

%  ER(j,i,:)=X_c/sqrt(Ref_c*Comp_c);
```

```
%  cor_value(k,i,j,:)=ER(j,i,:);
            cor(j,i,k)=ER(j,i);
        end
%     cor_max(k,i,:)=cor_value(k,i,36,:);
%     cor_mean(k,i,1:lag_width)=mean(ER(:,i,1:lag_width));
    end
  end

% Added by Jin to Plot the Contour of Local Temporal Coherence
   fs=samp_rate;
   for k=1:1:length(comparisons_selected)
    cor_cal_value(:,1:lag_width)=cor_max(:,k,:);
    for i=1:((4096-win_size)/win_step+1)
          LTC_time(i,1:lag_width)=(win_size+(i-1)*win_step)/fs*10^6;
    end
    for i=1:lag_width
          lag_time(1:(4096-win_size)/win_step+1,i)=(i-(lag_width+1)/2)/fs/2*10^6;
    end
    % Calcualting Correlation Lag
       for i=1:((4096-win_size)/win_step+1)
          temp_value1=cor_cal_value(i,1);
          temp_value2=(1-(lag_width+1)/2)/fs*10^6;
          for j=1:lag_width
```

```
            if (cor_cal_value(i,j)>temp_value1)
               temp_value1=cor_cal_value(i,j);
               temp_value2=(j-(lag_width+1)/2)/fs*10^6;
            end
         end
         Super_value(i,k)=temp_value1;
         lag_value(i,k)=temp_value2;
      end

%    Ploting Local Temporal Coherence in 3D
   figure(k)
   contour3(LTC_time,lag_time,cor_cal_value,30);
   axis([0 170 -10.5 10.5 -0.5 1]);
   surface(LTC_time,lag_time,cor_cal_value);
   xlabel('Time(us)');
   ylabel('Correlation Lag(us)');
   zlabel('Local Temporal Coherence');
   grid off
   view(-55,30);
   shading interp
   colormap gray
   colormap cool
  end
```

```
figure(length(comparisons_selected)+1)


for k=1:1:length(comparisons_selected)
    plot(LTC_time(:,1),Super_value(:,k),'-b*','LineWidth',2);
    axis([LTC_time(1,1) LTC_time((4096-win_size)/win_step+1,1) 0 1]);
    hold on
end
figure(length(comparisons_selected)+2)
for k=1:1:length(comparisons_selected)
    plot(LTC_time(:,1),lag_value(:,k),'-b*','LineWidth',2);
    axis([LTC_time(1,1) LTC_time((4096-win_size)/win_step+1,1) -6 8]);
    hold on
end
```

********** End of JIN's Modification April 25, 2007 **********

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