# APPLICATION OF CELLULOSIC MATERIALS AS FLEXIBLE SUBSTRATES FOR TWO-DIMENSIONAL ELECTRONIC HETEROSTRUCTURE DEVICES

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APPLICATION OF CELLULOSIC MATERIALS AS FLEXIBLE SUBSTRATES FOR TWO-DIMENSIONAL ELECTRONIC HETEROSTRUCTURE DEVICES

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# SUMMARY

With the goal of creating a set of materials to enable flexible electronics, two-dimensional (2D) materials are incredibly capable. This family of nanomaterials comprises a suite of strong and flexible conducting, semiconducting, and dielectric materials. These materials, all compatible with one another can be combined to enable an incredibly wide variety of behaviors and device structures.[1]–[4] Designs for structures using 2D materials have been proposed or developed that allow for photovoltaic (PV) energy production,[5] logic and general computing capabilities,[6],[7] and memory or data storage.[8]

In this work, I show that paper can be considered as a promising substrate material for these flexible electronics, as it provides a variety of interesting benefits including environmentally friendliness, flexibility, and low-cost. By mating pervasive flexible cellulose products with the new and exciting capabilities of 2D materials, we seek to help build a complete package of technologies for low-power electronics and computing applications.

There are several challenges when it comes to meshing these two materials systems. The surface properties of most papers have a great deal of roughness and texture, which can degrade performance of the 2D materials. Additionally, paper tends to be incompatible with most standard lithographic processes, requiring further processing to produce devices.

This work has helped to improve understanding of the effects of surface and interface properties on the paper and 2D nanolayer system, characterized the surface qualities of select paper substrates, determined preliminary methods to enable fabrication of structures directly on the final paper material, and performed initial electronic

characterization of graphene-based transistors on cellulose, and improved synthesis procedures for $MoS_2$.

As the world becomes more interconnected, everyday products and items are becoming smarter which is driving demand for low power and inexpensive computing technologies. A paper-based product would fit this need; inexpensive, environmentally conscious, and having a wide and tunable range of properties and possibilities.

# CHAPTER 1: INTRODUCTION

## 1.1 History of Flexible Materials for Electronics

### *1.1.1 Development of Flexible Electronics*

Flexible electronics have been a goal for the electronics industry nearly since its inception, yet it got its first developments in the late 1960s when the space industry needed lightweight photovoltaic (PV) power supplies. When the technology was developed to thin the crystalline silicon substrate, which minimized its weight, it also became flexible and compliant.[9]–[12]

Shortly after the development of the first flexible PV cells, the first flexible thin film transistors (TFTs) were demonstrated. Early devices were formed from tellurium deposited upon a strip of paper, first shown by Brody, et. al. in 1968, which had improved performance over the same samples on rigid glass slides and were capable of being bent to a radius of 1/16" without failure. A series of example devices were assembled into flexible audio amplifiers, logic circuitry, and oscillators.[10],[11] These same structures were shortly thereafter shown on polymeric films and thin metal foils.[9]–[11][12]

The next major advancement in the industry occurred in the 1980s, when active-matrix liquid-crystal displays (AMLCD) began to become the dominant display technology. These first displays had low pixel densities and were only capable of black and white, but they were revolutionary as they posed an opportunity to migrate away from the cathode-ray tube displays which were heavy, bulky, and consumed a great deal of power.[12]

The next breakthrough was the development of organic electronic materials, mostly comprised of highly-conjugated polymers. These opened a new class of semiconductors, however they were plagued with low performance for a long time but their flexibility and solution-processability were valuable attributes for these applications.[12]

### *1.1.2 Current Technology*

As techniques and technologies improved, flexible electronics transitioned into many products used commonly to this day. Flexible electronics are now commonly fabricated on polymers or thin glass sheets. The most common example of flexible electronics is the TFT which is an integral component of modern LCD displays, such as shown in Figure 1.1. These are fabricated as large sheets (greater than 2m wide) on a flexible backing, which are subsequently bonded to the glass plate of the display.

Another technique that is gaining traction is printable electronics. With the advent of improvements in organic electronic materials, printing is a valuable method for batch preparation of devices and novel structures.[13]–[19] The same technique is capable of printing devices, such as transistors, using inks based on a suspension of carbon nanotubes (CNT).[20]–[23] This technique is also commonplace for printable devices on paper substrates.[24]

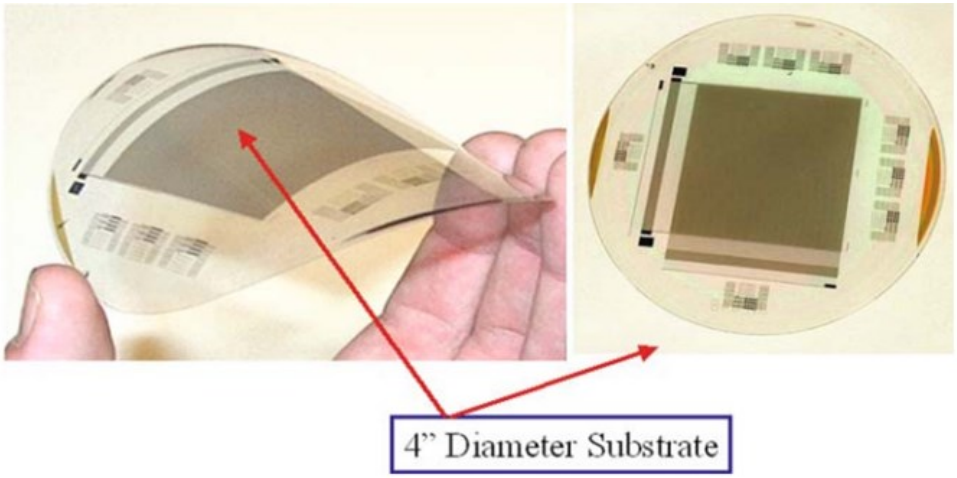



Figure 1.1: Modern flexible TFT-based displays have high pixel densities, and are capable of producing high-quality greyscale (as shown in this picture) or color images at a wide range of sizes and shapes.[12]

Another major advantage of flexible electronics is that it allows the use of hugely scalable manufacturing methods such as roll-to-roll processing. By transitioning from a batch to a continuous process, it becomes simple to fabricate huge quantities of product rapidly and compactly.[25],[26] Roll-to-roll has also been shown to be possible using novel two-dimensional materials, particularly graphene, to fabricate devices and even a complete display package.[27][31]

## 1.2 Two Dimensional Materials

### *1.2.1 Introduction to relevant materials*

Two dimensional materials are a relatively novel class of materials. Their existence was first predicted in the late 1940s with a two-dimensional allotrope of pure carbon, as its common form graphite was then known to have a novel layered structure.[32],[33] Experiments succeeded in making extremely thin graphite as early as 1966,[34] but it was not until 2004 that true graphene — a single atomic layer of hexagonal carbon — was isolated in the laboratory. This was achieved

using what is known as the “scotch tape method” allowing exfoliation of a highly crystalline sample of graphite.[35],[36]

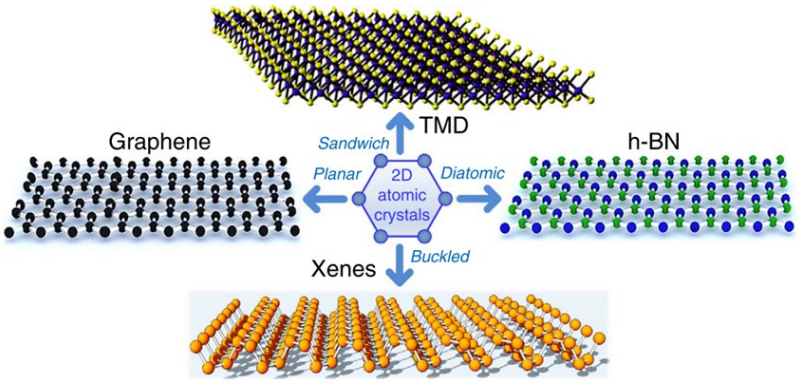



Figure 1.2: The family of 2D materials is diverse and growing.[37]

Once the existence of this class of materials was known to truly exist in nature, a menagerie of different materials has since been discovered to exist. Most exciting about this variety is that there exist examples of each of the three primary classes of electronically active materials: conductors, with graphene being the primary example; semiconductors, the most prominent of which are the family of transition metal dichalcogenides (TMDs); and dielectrics, with hexagonal boron nitride (h-BN) being the principal example, a summary of the different structural variations that comprise the family of layered crystals is shown in Figure 1.2.

*Graphene*

Graphene as a material exhibits a variety of impressive properties. It has incredible strength (130 GPa under tension), unsurpassed by any currently known material; it has a unique electronic

structure that gives rise to electron mobilities exceeding 100,000 $cm^2/Vs$; and is nearly completely transparent to visible light.

Structurally, graphene is a two-dimensional hexagonal lattice of $sp^2$ hybridized carbon atoms with an atomic spacing of 1.42Å (see Figure 1.3). The in-plane bonding of the carbon lattice forms from the hybridization of the $2s_2$, $2p_x$, and $2p_y$ orbitals; the $2p_z$ orbital remains unhybridized and forms π bonds, which coalesce into a π band that traverses the entire crystal. The electrons from this π band are the sole contributors to conduction, the σ bonded electrons remain localized and bound.[38]

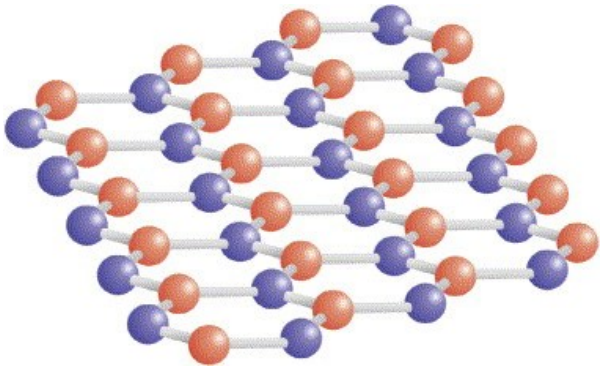


Figure 1.3: Graphene's crystal structure, highlighting the difference between A and B sites in the lattice.[36]

Due to the nature of this bonding, graphene exhibits a unique electronic structure not found in any other material. At specific points in its Brillouin zone, specifically the K and K' points, the conduction and valence band structure, which can be seen in Figure 1.4, form tight cones and come to a sharp point. This phenomenon is known as a Dirac cone, and the point at which the bands meet is the Dirac point. As the cones of the valence and conduction band have maxima and minima at the same energy, graphene is effectively a 'zero-gap semiconductor' or

'semimetal.' This allows electrons in the valence band to not experience any energy barrier to entering the conduction band, which helps lead to graphene's high conductivities. Additionally, by virtue of the dispersion being linear near the K points, carriers exhibit behavior reminiscent of massless relativistic fermions under the influence of ballistic transport mechanisms;[32],[33],[39] while there is an upper limit on the mobility due to the presence of phonons which can scatter the carriers, experiments have shown mobilities surpassing 200,000 cm2/Vs for graphene suspended in vacuum.[2]

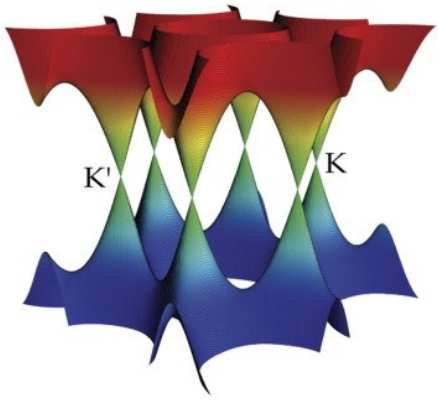



Figure 1.4: Graphene's band structure is unique amongst materials. Of particular interest are the regions near the K and K' points, where the conduction and valence bands form 'Dirac' cones that meet at their tips.[36]

However, for use as an active material in a field effect transistor (FET) used in digital logic, graphene has some drawbacks. In an ideal case, the band structure of graphene would lead it inherently having a Fermi energy of zero along with a density of states (DOS) at zero as well. This would be fine as there would not be any free carriers in the conduction or valence bands that would conduct given a bias.[2] However, real graphene does not behave in this manner. Via the effects of dopants imparted during synthesis, induced charge carriers from the substrate or the

ambient atmosphere, or even thermally generated carriers at any temperature there will never be a filled valence band or empty conduction band. This causes graphene to constantly have mobile carriers, and subsequently have a large current even under its ideal 'off' state. With typical on/off current ratios around 10:1, this precludes graphene from being used in traditional FET architectures.[39]

*Transition Metal Dichalcogenides (TMDs)*

Where graphene is considered the quintessential two-dimensional material, it is not perfect for all applications. In particular, its lack of an intrinsic band-gap limits its applications somewhat. The group of TMDs help to fill the role of true semiconductors in the family of two-dimensional materials.

As the name implies, TMDs are compounds of the form $MX_2$, where M is a transition metal (most commonly molybdenum or tungsten) and X is a member of the group of chalcogens (sulfur, selenium, tellurium, etc.). The formation of the compound leads to the metal atoms being encapsulated between two monolayers of sulfur atoms; the adjoining chalcogen layers do not have any strong bonding and only interact via Van-der-Waals forces. An image of the crystal structure of a few layers of $MoS_2$ can be found in Figure 1.5.

One of the most interesting aspects of the set of TMD materials involves their thickness-dependent electronic structure. As the crystal is thinned by removing layers, the band gap of the material changes dramatically. As an example, in its bulk form $MoS_2$ exhibits an indirect bandgap of 1.2eV. As the number of layers decreases, this bandgap begins to widen, eventually reaching the end case of an isolated layer of $MoS_2$ which has a bandgap of 1.9 eV.[40] Additionally, as

layers are removed, the valence band maximum shifts away from its bulk location at the Γ-point and eventually lining up with the conduction band minimum at the K-point; meaning the material transitions from an indirect to a direct-gap semiconductor, which has implications in the optical properties of the $MoS_2$. This shift can be seen in Figure 1.6, which shows the results of DFT calculations of the band structure of $MoS_2$ crystals with a variety of thicknesses.[40],[41]

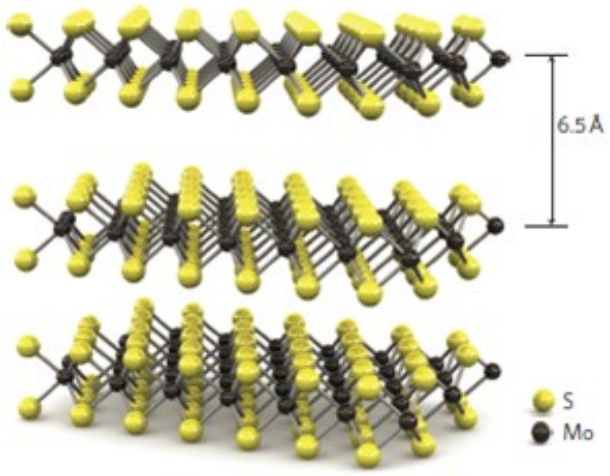



Figure 1.5: The crystal lattice of MoS2 shows the unique layered structure of the material. Whilst there is strong bonding between atoms in a single layer, interlayer bonds are weak van der Waals interactions.[3]

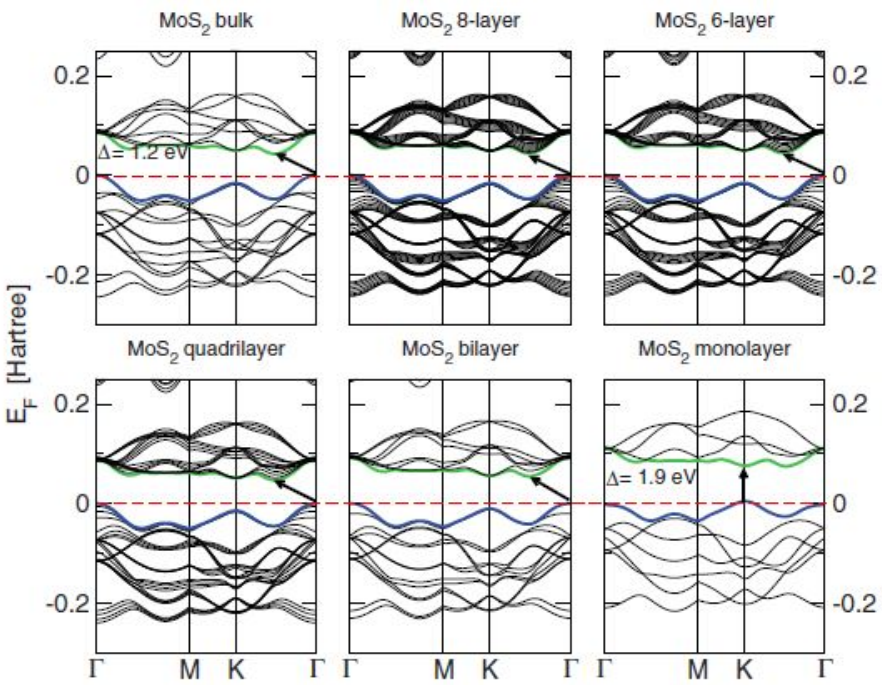



Figure 1.6: Variable band structure of $MoS_2$ crystals of varying thickness.[40]

*Hexagonal Boron Nitride*

Hexagonal boron nitride (h-BN) is incredibly similar to graphene in many ways, and is often colloquially referred to as 'white graphene.' It takes on the same layered hexagonal crystal structure as graphene, but each triangular sublattice contains either boron or nitrogen.[42],[43] However unlike graphene, h-BN features a favorable dielectric quality, matching or exceeding the properties of $SiO_2$. It has a large band gap of 5.97 eV, is superior at screening electric charges, and its two-dimensional nature precludes the existence of undesirable dangling bonds; all of which allow for improved mobilities and general performance in the other materials that it supports.[44],[45]

*1.2.2 Why are 2D materials unique and valuable to improving flexible electronics?*

2D materials bring a variety of unique and high-performance capabilities which can dramatically improve the functionality of flexible electronics. Logic devices such as FETs can be formed using a variety of materials,[46]–[52] such as one design based on graphene and $WS_2$ heterostructures.[46] This structure is formed by sandwiching a layer of $WS_2$ between two graphene layers (see Figure 1.7), by controlling the voltage bias across the structure and the Fermi level using the gate electrode the tunneling current can be modulated (see Figure 1.8).

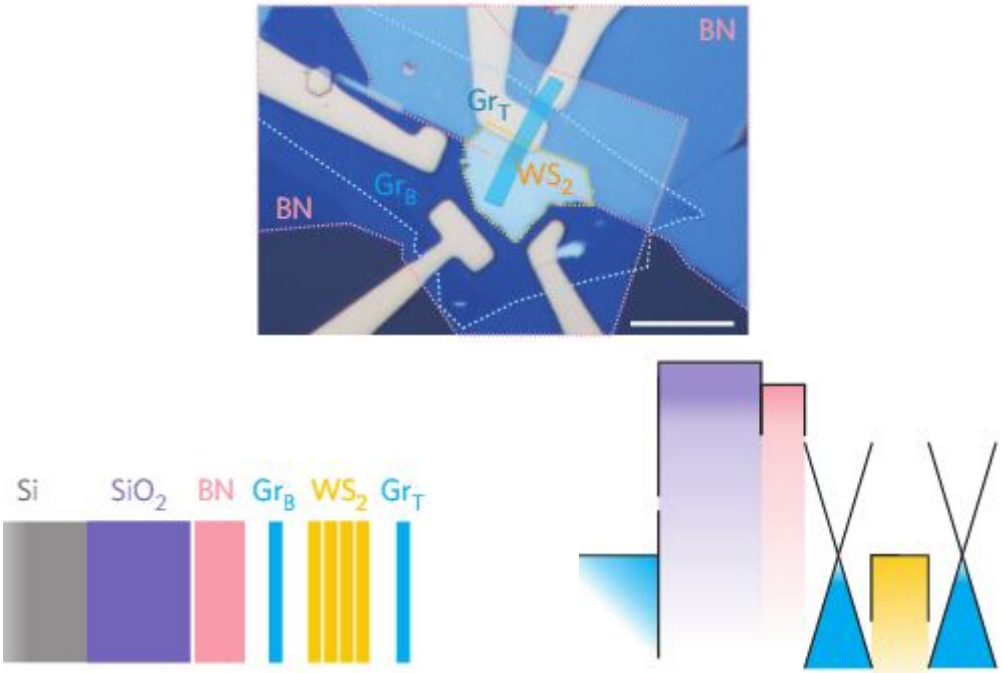



Figure 1.7: Optical image of a graphene-$WS_2$-graphene heterostructure (top). Ordering of the layers in the device (bot. left) and the associated band schematic (bot. right).[46]

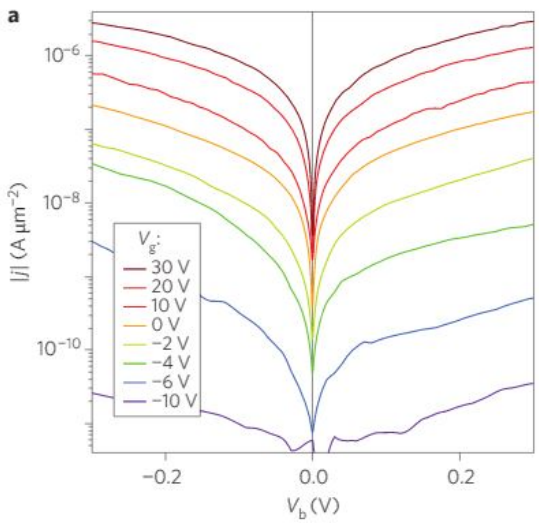



Figure 1.8: Tunnel current through graphene-$WS_2$-graphene heterostructure at various gate bias levels.[46]

Tunnel diodes can be fashioned using two types of TMDs that can be together form a p-n junction, see Figure 1.9 for a graphic describing the structure of such a device made from an interface between $MoS_2$ (n-type) and $WSe_2$ (p-type).[53] Sensors for biologicals[54] or mechanical strain,[55],[56] have also been reported using two-dimensional materials.

By leveraging the capabilities and large library of potential device structures, a diverse variety of applications can be envisioned. Flexible or foldable cell phones, electro-active tattoos, wearable computing devices, and many more possibilities become feasible.[37]

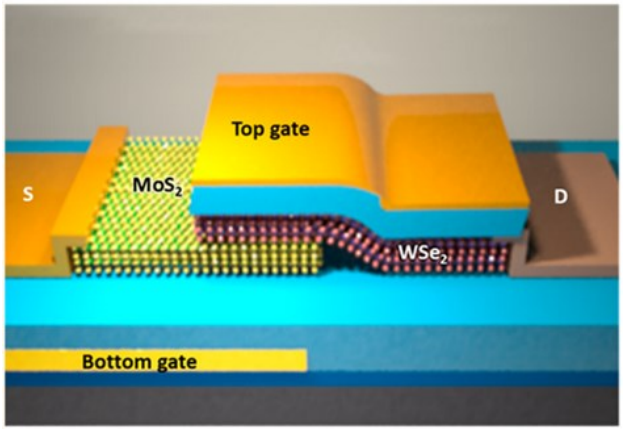



Figure 1.9: 2D materials can be utilized to make a wide variety of devices and structures. Here a graphical representation of a tunnel diode made from a junction between few-layer $MoS_2$ and $WSe_2$ is shown.[53]

## 1.3 Cellulosic Materials as Substrate for Electronics

### *1.3.1 Structure and Properties of Cellulose Fibers*

Cellulose, the primary material from which paper is made, is an interesting and attractive platform for electronic materials. It is inexpensive, highly flexible, environmentally preferable, and disposable option. While conventional paper materials have been around for millenia, some more modern and advanced products are making paper a possible option for hosting electronics.

Cellulosic materials as substrates generally fall into one of two categories: conventional large-fiber products such as newsprint, photo paper, and other specialty papers or a new class of bioproducts made from cellulosic nanomaterials (CNs), which offers unique properties not generally seen with paper materials.

As can be seen in Figure 1.10, natural structures based on cellulosic materials can have a rich hierarchal structure. Traditionally, paper is made by chopping wood or plant biomass into small chips, and then subsequently breaking the chips down into individual fibers; this is done by

chemically attacking and dissolving two of the primary components of the wood: lignin and hemicellulose. These two materials act together to hold the individual fibers in their proper location and orientation. When seeking to make paper, the biomass is broken down into individual microfibril bundles; further processing can achieve nanoscale fibers or break the material down into crystalline particles for forming smart materials.

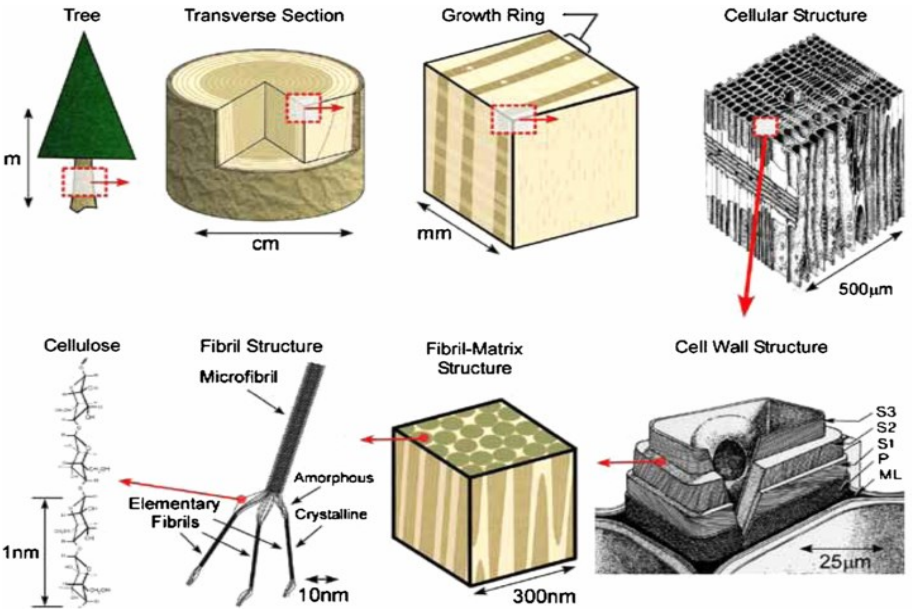



Figure 1.10: Wood biomass (the primary source of cellulose material) shows an incredible hierarchy from the macroscale, to mesoscale, and even down to nanoscale components.[57]

Cellulose products have a number of desirable properties as a substrate. One major advantage is that it is an environmentally friendly material. The material itself is easily recycled into new products, or it will rapidly biodegrade when exposed to the environment. Additionally, as the paper industry is extremely mature, paper as a product is very inexpensive when compared

to nearly any other potential substrate material for electronics, and its production tends to be much gentler on the environment.

*Conventional Fibrous Paper Materials*

After the wood chips are digested to remove the lignin and liberate the individual cellulose fibers, they undergo chemical washing and bleaching processes. The final cleaned slurry is then used to form the mat of fibers that becomes paper. The slurry is sprayed over a filtration mesh and allowed to drain, where enough water leaves to form a hydrated but solid web of fibers. Further processing presses and then heats the web to eliminate the remaining water from the newly-formed paper.

One of the primary challenges with matching 2D electronics with traditional papers is their generally high surface roughness, which can be seen in AFM micrographs in Figure 1.11. Even the smoothest options (e.g. multi-layer coated inkjet photo paper or calendered laser printer paper) can be an order of magnitude rougher than conventional electronic substrates, for example a polished silicon wafer. When the active materials are transferred to the target substrate, this topography causes the material to distort as it attempts to conform to the substrate. This can cause poor adhesion to the substrate, damage to the device structure, and drastically degrades material performance. Because of the performance issues associated with rough surfaces,[58] it is preferable to utilize the smoothest possible papers when considering substrates for electronic applications.

Additionally, many paper products are coated with various materials to provide improvements to a variety of properties. These can include surface treatments to improve the paper's brightness

(how white the sheet looks), have different adsorptive or absorptive properties for printing pigments and inks, amongst other options.[58],[59] Many of these coatings are made of inorganic materials — such as kaolin clays or calcium carbonate particles — polymers, or elastomers (latex is a common binder for inorganics on paper). See Figure 1.12 for an example SEM micrograph of a paper surface coated with kaolin-based pigment to improve brightness.[25],[60],[61]

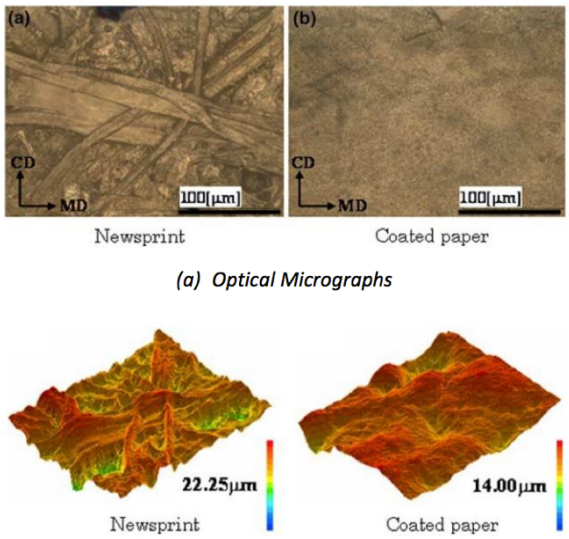
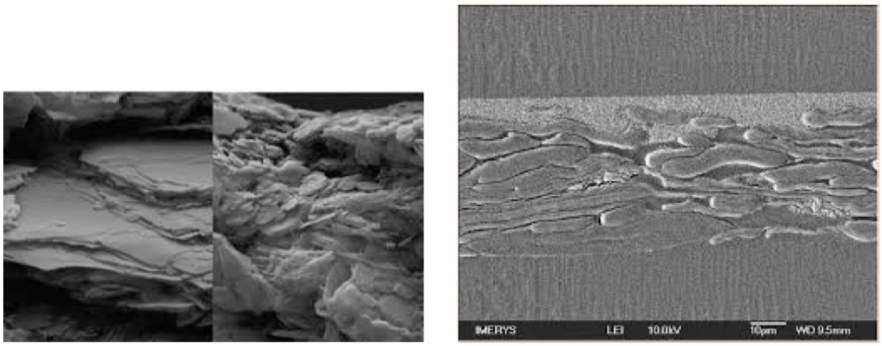



Figure 1.11: Here we show the rough paper surface that is formed by the interlocking fibers of a traditional paper material. (a) Optical micrographs of a newsprint (left) and coated paper (right) surface. (b) AFM showing the surface topography of the two paper types.[62]




(a) (b)

Figure 1.12: Paper is often coated with clays and pigments to affect its surface properties or brightness. (a) Kaolin, a clay material with a distinctive platelike structure, is a common choice among manufacturers. (b) A cross section of a thin paper sample coated with kaolin and a polymeric top layer.

*Cellulosic Nanomaterials*

Once the cellulosic biomass has been broken down into the microfiber bundles traditionally used for manufacturing paper materials, it can continue to be processed in order to obtain structures with dimensions on the order of nanometers and are referred to as cellulosic nanomaterials (CNs). This process is generally done via extensive mechanical refinement processes, which yield cellulose nanofibrils (CNF) as a product, or chemical digestion which yields cellulose nanocrystals (CNCs).

CNF material is produced via mechanical methods using high-pressure homogenizers or griders which delaminate the cell walls of the fibers and expose the individual fibrils. This process can be assisted via a variety of pre-treatments of the pulp; these can be an enzymatic digestion,[63] surface decoration with charged species (e.g. via carboxymethylation[64]), or an oxidative process

(often using the TEMPO-mediated process[65]). Once the CNF stock material is prepared, it can be processed into films or coatings. Cast sheets made from CNF solutions act similarly to polymer films. They are optically transparent, and can be created with extremely smooth surfaces. Studies have shown that the average surface roughness of these films can achieve values of less than 2 nm.[66],[67]

Cellulose nanocrystals (CNCs) are a form of cellulose in which the original large wood fiber has been digested to eliminate all but its nanoscale crystalline portions; examples of these are shown in Figure 1.10 and Figure 1.13. This is done by using traditional methods to break the wood biomass into fiber pulp; this pulp is then subjected to dissolution in a strong acid environment – high concentrations of sulfuric or hydrochloric acid are generally utilized – or an active enzyme is used to digest the undesirable regions. The acid or enzyme preferentially attacks the bonds between cellulose monomers that are located in the amorphous regions, while the crystalline portions of the fiber are relatively unaffected. Given sufficient time, all that remains of the wood pulp is a slurry of CNC crystallites suspended in solution. These are washed and neutralized prior to use.[68],[69]

This produces a material that can combine high strength along with flexibility, and low thermal expansion.[68]–[72] Additionally, it is readily recyclable or biodegradable and simple to adapt to roll-to-roll processes.[73] It may require some modifications to optimize properties such as its hydrophobicity and water permeability.[74],[75] CNs can be directly formed into sheets or can be used as a filler for polymers and other composites. When the material has reached the end of its life, it is readily recyclable or biodegradable.

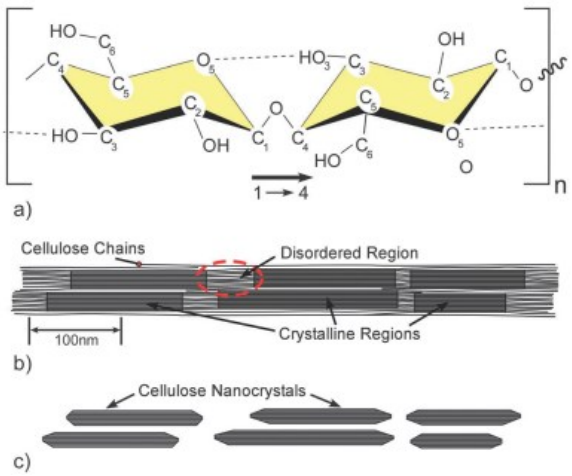



Figure 1.13: The nanoscale structure of cellulose. (a) The chemical structure of a cellulose monomer. (b) An elementary fibril is formed of regions of ordered and disordered cellulose chains. (c) Dissolving the disordered regions in a strong acid yields CNC particles.[68]

### *1.3.2 Cellulose as a Substrate for Electronics*

#### *Traditional Paper Materials*

Cellulosic materials have shown significant promise as substrates for electronic devices. Example devices such as a-Si TFT structures[76] and PV solar cells[77] have been successfully fabricated and tested on paper-based substrates. One common method for fabricating these structures utilizes inkjet printing techniques to deposit organic semiconductors and metallic contacts,[13]–[19] or dispersed carbon nanotube inks[20]–[23] in order to make transistors or solar cells.[24]–[26],[78]

#### *Cellulose Nanomaterials*

Cellulose nanomaterials are also an effective substrate material, and have been used in some examples of flexible electronics. The nanocellulose can be used as a surface coating, such as in

the bilayer substrate devices presented by Bao, *et.al.*,[54] where a thin layer of CNF material was used in order to create a smooth 2-4 μm top surface suitable for nanoelectronics.

Neat films of CN also function well as substrates, and with their useful optical and mechanical properties are being used to fabricate many of the same types of structures previously shown on traditional papers. Examples include light-emitting diodes[73] and foldable electrode carriers[79] on films of NFC, and PV solar cells fabricated on a cast film of CNC.[66]

# CHAPTER 2: METHODOLOGY

## 2.1 Synthesis of $MoS_2$ Nanolayers

Figure 2.1 illustrates a process and apparatus for synthesizing centimeter-scale samples of uniform-thickness $MoS_2$ thin films.[80] The method begins with a thermal $SiO_2$ substrate which is coated with a thin layer of molybdenum, between 0.3-1 nm, via e-beam evaporation; the final thickness of the $MoS_2$ film is directly correlated with the original thickness of the evaporated metal, allowing for the synthesis of mono-, bi-, or trilayer samples in a controllable manner. Upon removal from the evaporation tool, the evaporated film partially oxidizes in the ambient atmosphere, forming a mixture of Mo and $MoO_x$ species.

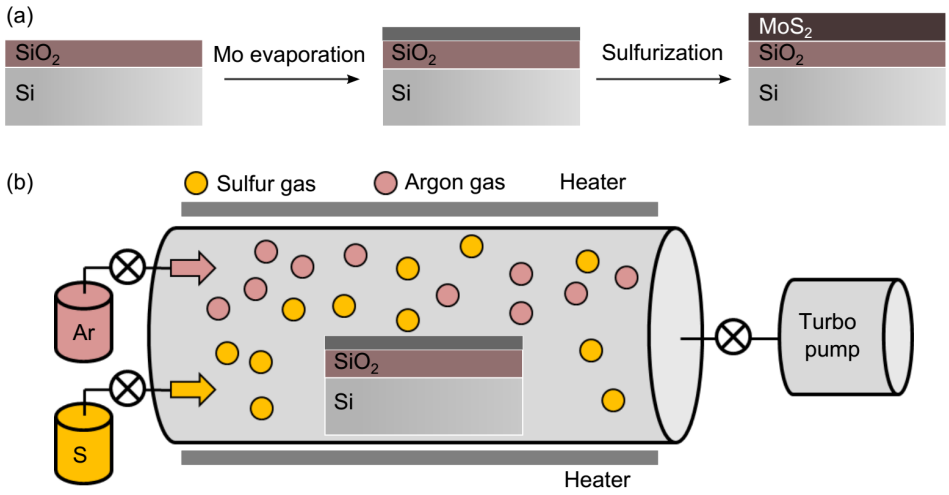



Figure 2.1: Schematic of $MoS_2$ growth process. (a) A thin film of Mo is evaporated onto a substrate of 300 nm thermal $SiO_2$ on Si. This film is then reacted at high temperature in a sulfur-containing environment to produce $MoS_2$. (b) Schematic of the sulfurization furnace.[80]

To sulfurize the $MoO_x$ film, a measured amount of high-purity powdered sulfur is first loaded into a graphite crucible, to serve as the source of sulfur for the reaction. The Mo-coated substrates and the sulfur-containing crucible are subsequently placed into a tube furnace and evacuated under a turbo pump to sub-mTorr pressures. Once evacuated, the furnace increases the chamber pressure to approximately 5 Torr using a mixture of Ar and $H_2$, and subsequently seals the chamber from both the inject and vacuum lines. This gas mixture is used to both help to strip atmospheric contaminants from the chamber and film surfaces as well as to help reduce the oxidation state of the $MoO_x$ species. These reduced compounds are more readily reacted with sulfur to form the desired $MoS_2$ product. The isolated chamber is then rapidly heated to the sulfurization temperature of 1050°C. At this temperature, all the powdered sulfur has evaporated and is available to react with the $Mo/MoO_x$ film. After holding at process temperature for 60 minutes, the sulfurization reactions are completed.

Following the sulfurization step, the chamber continues to be held at 1050°C while any residual reactants and contaminants are purged from the system using a 30 min flow of Ar at 200 sccm. Once the purge is complete, the chamber is cooled to room temperature while remaining under Ar flow. Once the chamber has reached ambient temperature, the sample is then removed from the system and is ready for further characterization or fabrication steps.

## 2.2 Transfer Procedures for 2D Materials

### *2.2.1 Traditional Etch Transfer*

2D materials often need to be synthesized on specific substrates, for example common CVD growth methods for graphene and h-BN require a transition metal substrate to catalyze the

reaction. However, these materials tend not to be ideal for use in the final devices, which necessitates the use of a method to transfer the nanolayers from one substrate to another.

Generally, this transfer is effected by using wet-etching techniques to dissolve the growth substrate while not harming the 2D crystal. First, approximately 2 μm of polymethyl methacrylate (PMMA) is deposited by spin-coating onto the 2D material; this acts as a carrier layer and prevents it from undertaking significant damage during the rest of the transfer protocol.

In the case of graphene, or monolayer h-BN also grown on copper, ammonium persulfate (APS; $(NH_4)_2S_2O_8$; 0.5 M) is used to etch the thin copper foil substrate. It may be necessary to first ensure that any graphene that was grown on the back-side of the substrate is eliminated, as it dramatically slows the etching progress. This can be done using a 50 W $Ar/O_2$ plasma for 30 sec, or by immersing in nitric acid (3:1 $HNO_3$:DI $H_2O$) for 60 seconds. The Cu etch process takes approximately 6 hours to fully consume the Cu, but APS does not adversely affect graphene and thus the nanolayer can be left in solution for extended periods of time without incurring damage.

For $MoS_2$ and h-BN, the etch process uses buffered oxide etch (BOE; 6:1 40% $NH_4F$:49% HF) to release the nanolayer from its substrate. The acid attacks the $SiO_2$ on the growth wafer for $MoS_2$. h-BN is commonly grown on nickel foils, which readily oxidize in the presence of water and then this oxide is dissolved by the BOE.

After the substrate has been etched completely, only the carrier polymer and nanolayer remain floating on the surface of the solution. This stack then can be carefully lifted out of the etch solution and placed into DI $H_2O$ to rinse. The last step is to transfer the samples into a bath

of isopropyl alcohol to flush any remaining water from the surface of the material. Finally, the layer can be introduced to its final substrate and lifted out of the solvent.

After being gently but thoroughly blow-dried to expel and evaporate as much of the residual solvent as possible, the material should then be placed upon a cold hot-plate and slowly heated to 220°C at a rate of 20°C/min and allowed to bake for 5 min. This helps to remove any remaining liquid as well as serves to soften the carrier polymer and allow the nanolayer to make better contact with the underlying substrate. After allowing the sample to cool, immersion in acetone serves to dissolve the carrier polymer leaving the 2D material upon its new substrate.

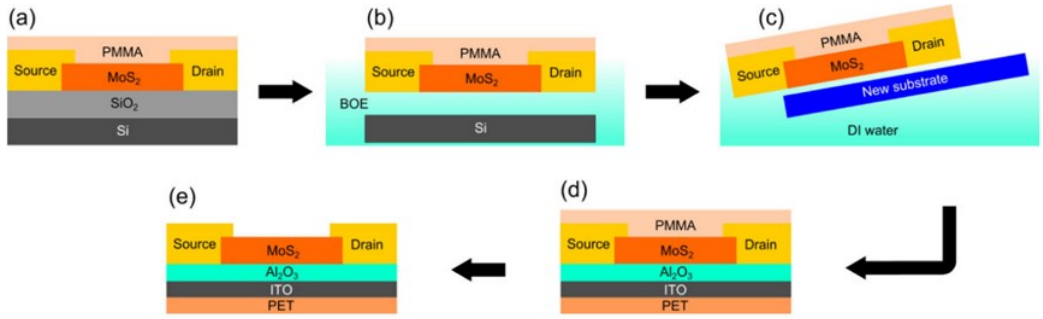



Figure 2.2: Diagram for the transfer of prefabricated devices to arbitrary final substrates.[56] The same general procedure is used to transfer the 2D layers themselves. Due to being grown on copper foil, graphene uses APS as the etchant in step (b) as opposed to BOE.

This method can be extended to allow for the transfer of fabricated device structures from a fabrication substrate to any arbitrary material. This procedure has been demonstrated for transfer to polymers,[56] and has also been used to transfer $MoS_2$-based devices to paper-based substrates (for these substrates the baking temperature was lowered to 105°C and the time extended to 30 min). A schematic diagram of this process is given in Figure 2.2, which specifically

illustrates a method for transfer of completed device structures, but can be generalized to any of the transfer procedures.

*2.2.2 Etchless Transfer of TMDs*

Surface energy affects hydrophilicity or hydrophobicity of the materials, in particular $MoS_2$ is highly hydrophobic while its silica growth substrate is comparatively hydrophilic. By leveraging this difference, it becomes possible to separate the nanomaterial from its growth substrate by simply mechanically delaminating a small region of the nanolayer and allowing water to intercalate and eventually release the material completely.[81]

The process also begins by affixing a carrier layer to the surface of the TMD that is to be transferred. This can be the commonly utilized PMMA, but if the carrier polymer is more hydrophobic the surface energy effect is heightened. To this end, polystyrene (PS) is used in place of PMMA for these transfers, and is spin-coated in a similar fashion as PMMA. After the polymer has dried sufficiently, one edge of the TMD/PS stack is exposed by removing material with a razor blade. This allows for easy access to a large interface between the hydrophilic $SiO_2$ surface and the TMD/PS. Then, a small amount of deionized water is applied to this interface and the water is allowed to intercalate between the TMD and $SiO_2$. This completely removes the TMD from its growth surface. Following the intercalation step, the whole sample can be gently immersed in water and allow the TMD/PS stack to float on the surface.

Once the material has released fully, it can then be transferred to the target substrate in the standard fashion. The material is transferred to a bath of IPA to expel residual water, then transferred to its final substrate and subsequently dried and baked. If the bake must be done at

a lower temperature (e.g. using paper substrates), it should be done for a longer time to compensate. Finally, the PS layer is removed by gently rinsing or soaking in an appropriate solvent, e.g. toluene or acetone.

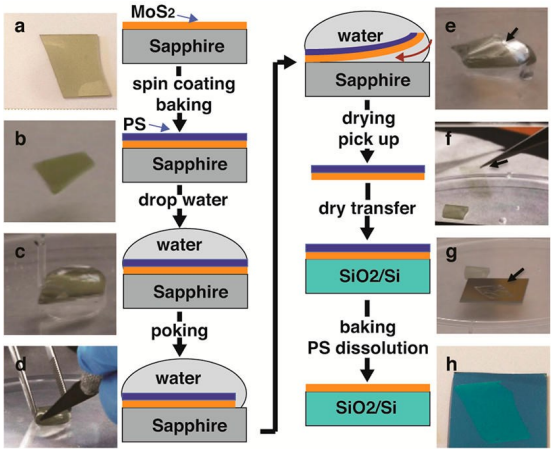



Figure 2.3: Schematic for the surface-energy-assisted method for transfer of TMD material.[81]

Another method is to apply a thicker, more mechanically robust layer of carrier polymer which can be directly handled without failing. In this case, the water droplet can be wicked away using absorbent material, and the TMD/PS film can be gently removed with forceps and dried with $N_2$. Then the dried film can be placed onto the target substrate, baked to adhere, and finally the PS layer is removed. A schematic diagram for the process is shown in Figure 2.3.

## 2.3 Device Fabrication

Two types of devices were used over the course of this project: field effect transistors (FETs) and metal-oxide-semiconductor capacitors (MOSCAPS). The device structure used for the FETs can be found in Figure 2.4, while that of the MOSCAPs is shown in Figure 2.5.

### *2.3.1 Field Effect Transistor Fabrication*

To fabricate the FETs, the substrate is first cleaned thoroughly using washings of acetone, methanol, and isopropanol. Then, the back gate is defined using a standard photolithographic procedure. The contact metal is then evaporated using an e-beam evaporation system, and the contacts are finished during a lift-off step.

The back-gate dielectric is deposited by first creating a seeding layer of alumina by evaporating a 3nm layer of aluminum and allowing it to oxidize in ambient atmosphere. ALD was then used to deposit the chosen oxide, either hafnia ($HfO_2$) or alumina ($Al_2O_3$). The active 2D material was then transferred to the substrate, the precise procedure for which is described in the next section.

Once the 2D material has been transferred, the FET channels must be defined. A protective layer of photoresist is created using standard techniques, and then the excess 2D material is etched using a dry etching process. For graphene, 2 min of 50w $Ar/O_2$ plasma is used; for TMDs the oxygen is replaced with sulfur hexafluoride ($SF_6$).

The source and drain contacts are then defined, evaporated, and lifted-off in the same fashion as the back-gate contact. Then another dielectric layer is deposited on the top of the device stack, with a final metallization step to create the top-gate contact.

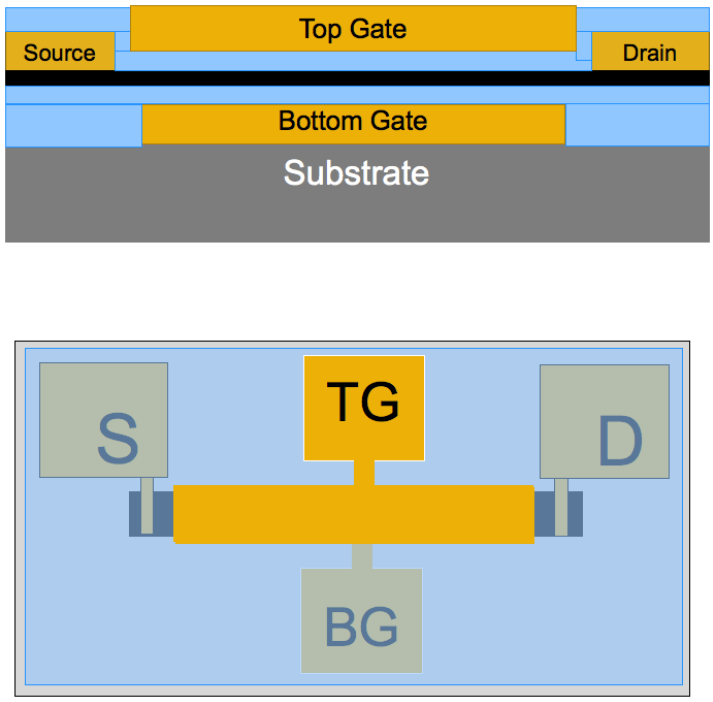



Figure 2.4: Layer structure of the FET test structures in cross-section (above) and top-down views (below). The gold sections are metallized regions, light blue represents dielectric material, and black is the active 2D material.

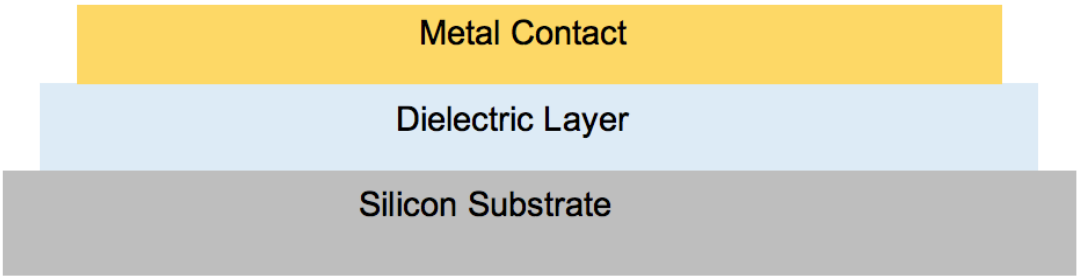



Figure 2.5: Cross section of the MOSCAP test structure.

*2.3.2 Metal-Oxide-Semiconductor Capacitor Fabrication*

The MOSCAPs are fabricated by first etching the oxide layer from a thermally oxidized silicon wafer using a standard 6:1 buffered oxide etchant (BOE) solution. Once it is etched, a dielectric layer is deposited onto the bare silicon surface. Finally, the metal contacts can be defined either using lithography/lift-off or via a shadow mask (physical masking) technique. The shadow masks used in this project were Cu TEM grids with square 100x100 um apertures.

## 2.4 Deposition of Planarization and Barrier Layers

Traditional paper products are unable to withstand the procedures involved in the fabrication of electronic devices. In order to overcome this obstacle, parylene, a xylylene-based polymer with the structure shown in Figure 2.6, is used to provide a barrier layer against the various solvents used during processing. Parylene is a common choice as it is easy to work with and provides a high-quality, water-resistant, and transparent barrier layer to nearly all commonly encountered solvents (such as acetone or alcohols) and is also unaffected by most acidic or basic solutions.[82]

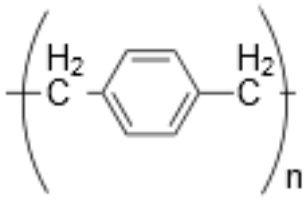



Figure 2.6: The chemical structure of polymeric Parylene is based upon the repeating unit shown here.[83]

Parylene can be deposited using a variety of techniques, such as spin-coating[84] or vapor-phase deposition.[82],[85]–[88] The latter is more commonly utilized and commercial coating systems

are readily available. The source material for the reaction is solid pellets of a xylylene dimer. This dimer is first volatilized at a moderate temperature (70-140°C), and then cracked into reactive monomers in a furnace held at 690°C. The monomer polymerizes once it encounters a solid surface. Any unreacted monomer is captured using a cryogenic cold trap to prevent damage to the vacuum system.

To perform the deposition, first the sample to be coated is placed within the reaction chamber which is then evacuated to pressures in the mTorr range. Once a suitable pressure is reached, the furnace chamber is heated to operating temperature. Once the system has stabilized, the vaporization chamber is heated. The partial pressure of the monomer vapor within the reaction chamber, on which the deposition rate of the film is highly dependent, is controlled by modulating the temperature of the vaporization stage.

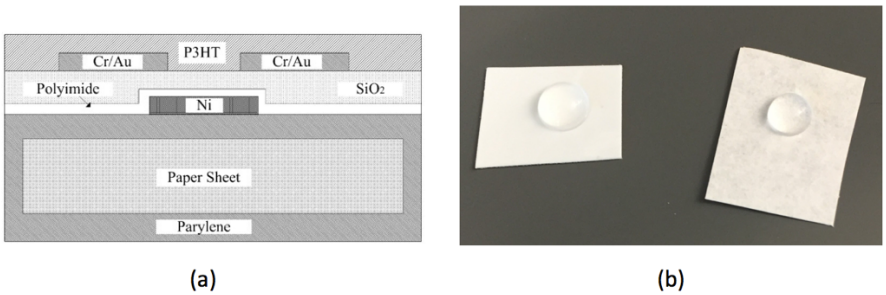



Figure 2.7: Parylene can act as a high-quality barrier and planarizing layer for a variety of paper types. (a) Parylene in use as a coating for an organic TFT.[89] (b) Parylene creating a hydrophobic surface on photo (left) and copy paper (right).

This work utilized parylene to prepare samples of Kodak Ultra-Premium Glossy Inkjet Photo Paper (referred to subsequently as 'photo paper') which can withstand the conditions required for photolithographic processing, discussed in the previous section. Figure 2.7 shows a schematic

of how the parylene is used to isolate the substrate from the electronic materials as well as an image showing the hydrophobicity of the coated samples.

## 2.5 Characterization Methods

### *2.5.1 Surface Roughness and Topography*

Atomic force microscopy was used to investigate the topography of the sample surfaces. This study utilized a Veeco Dimension 3100 Scanning Probe Microscope (SPM) operating in tapping AFM mode. Images with dimensions of 10x10 um were collected from several locations on each of the samples, and the surface roughness parameter ($R_s$) was extracted from them using a commercial software package.

### *2.5.2 Adhesion Testing*

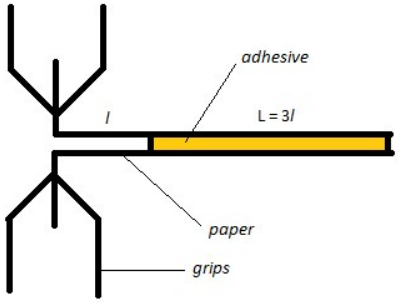



Figure 2.8: A diagram for creating a sample for peel-test analysis.

Samples for adhesion testing were created by transferring a sample of 2D material onto a strip of paper substrate. A double-sided pressure sensitive adhesive (PSA) was then affixed atop the region where the 2D material was present. A second sample of paper substrate was placed

on the opposite face of the PSA. The sample structure and geometry used is illustrated in Figure 2.8.

These samples were then destructively tested using a peel-testing apparatus operating in constant velocity mode. The force required to separate the two layers was recorded as a function of distance down the sample length, and was normalized to the linear width of the sample.

*1.1.1 Raman and Photoluminescence Spectroscopy*

Raman and photoluminescence spectroscopy was performed using a Renishaw InVia microRaman system configured with two excitation sources – a 532 nm diode laser and 488 nm $Ar^+$ laser – and a 0.25 m focal length spectrometer. The measurement system was also equipped with an automatic stage controller, providing the ability to collect spectra from selected areas of samples to create maps of the Raman response.

*2.5.3 X-Ray Photoelectron Spectroscopy*

X-Ray Photoelectron Spectroscopy (XPS) was utilized to characterize the composition of the layered materials. For this study a Thermo Scientific K-Alpha XPS system was used. This system is equipped with a monochromated Al $K_\alpha$ X-ray source, a 400 μm spot size, and a neutralizing ion flood gun to prevent sample charging.

# CHAPTER 3: RESULTS

This work is focused on answering two primary questions central to the successful integration of 2D electronic materials and flexible paper substrates. First, how does the physical structure of the underlying paper affect the properties of the 2D adlayer, and how can this substrate and the interface between the two materials be tuned and engineered to improve performance?

The second aspect of this thesis focused on the intricacies of obtaining functional devices on the target substrates. I investigated two methods for obtaining the desired structures; these involve either fabrication of the devices directly upon the paper substrates or prior fabrication of test structures on traditional silicon wafers and subsequent transfer of the entire device stack to a target paper.

## 3.1 Physical Characterization of the Materials System

The physical structure of paper substrates vastly differs from that of traditional materials upon which electronics have been manufactured previously. The traditional substrates offer surfaces that are smooth and homogeneous, such as the polished surface of a silicon wafer or a film of flexible polymer. Paper, with its complex web of interlocking fibers, in general tends to have a rougher surface that is not necessarily homogeneous in all directions.

In this section I discuss the implications of the physical properties of the substrate's surface as well as the interface with the active materials.

### *3.1.1 Surface Roughness*

Two-dimensional materials are extremely susceptible to the effects of surface roughness. It impacts their performance, can cause variation in the properties of the material, or in extreme cases can cause delamination or failure of devices entirely. It is therefore of the utmost importance to understand the physical characteristics of the surfaces that are to be used to host 2D materials and heterostructure devices.

*Paper Substrates*

Two paper types have been investigated for use as target substrates for test devices: the photo paper mentioned previously as well as an unbranded supercalendered glassine paper. The photo paper is an example of a coated paper product, with absorptive pigments bonded to the surface with a barrier layer to isolate fluids (traditionally inks) to the top coating for optimal printing properties; glassine paper has no additional coatings or fillers and is a web of cellulose fibers that has been subjected to additional high-intensity pressing operations to form a smooth, slick textured surface.

Tapping-mode AFM was the primary method for surface analysis of these two paper types. Shown in Figure 3.1 are two representative micrographs highlighting the major structural differences between the two materials. The photo paper sample seen in Figure 3.1(a) exhibits a platy particulate structure, which is expected from a pigment coated paper. This substrate intrinsically has an average surface roughness of 11.25 nm. In comparison, AFM micrographs of the uncoated glassine paper, shown in Figure 3.1(b), reveal distinct fibers which cause large

surface features to be present. In smooth regions without protruding fibers, its RMS roughness averages to 25.6 nm. Figure 3.4 compares this to that of a bare oxidized silicon wafer at 0.87 nm.

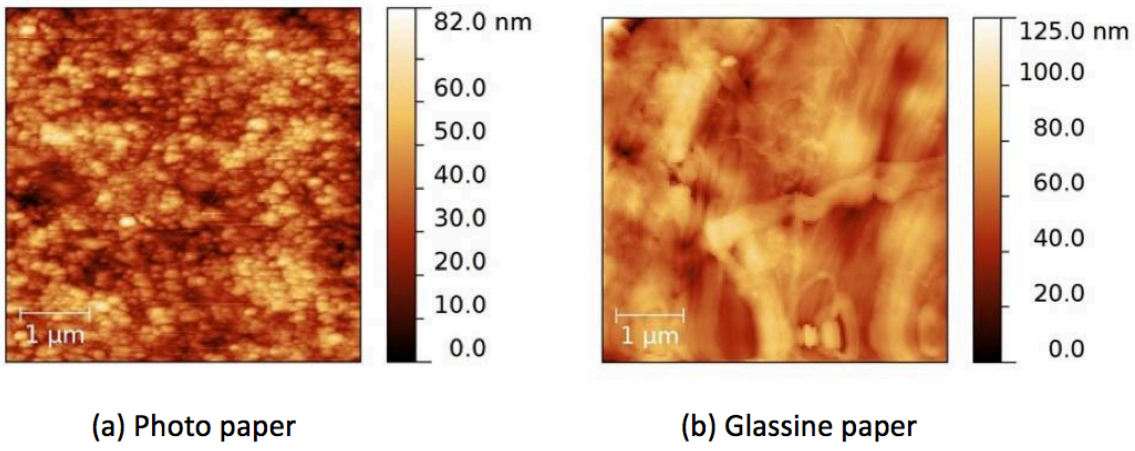



Figure 3.1: AFM micrographs of the (a) photo paper and (b) glassine paper substrates prior to transferring any 2D layers. The photo paper exhibits a uniformly textured surface due to its platy particulate surface coating while the glassine sample shows very visible fibrous features.

*2D Materials*

When 2D materials are transferred to a smooth surface, such as the polished surface of a $SiO_2$ wafer, it can be seen that the layers are nearly atomically smooth. The main source of increased roughness of the surface following transfer is the presence of residues from the transfer process; these generally are particulates of the carrier polymer or photoresist that do not dissolve when removing using a solvent.

Examples of this can be seen in the AFM micrographs shown in Figure 3.2 and Figure 3.3. The former illustrates the transfer of an $MoS_2$ trilayer to the polished wafer. Prior to the transfer,

the surface exhibited a surface roughness of 1.01 nm; with the layer of $MoS_2$ transferred and cleaned, this value increased to only 1.33 nm. Clearly visible in the micrograph are particulates on the surfaces, 20-30 nm above the surface of the material, and these are likely the source of much of the surface roughness.

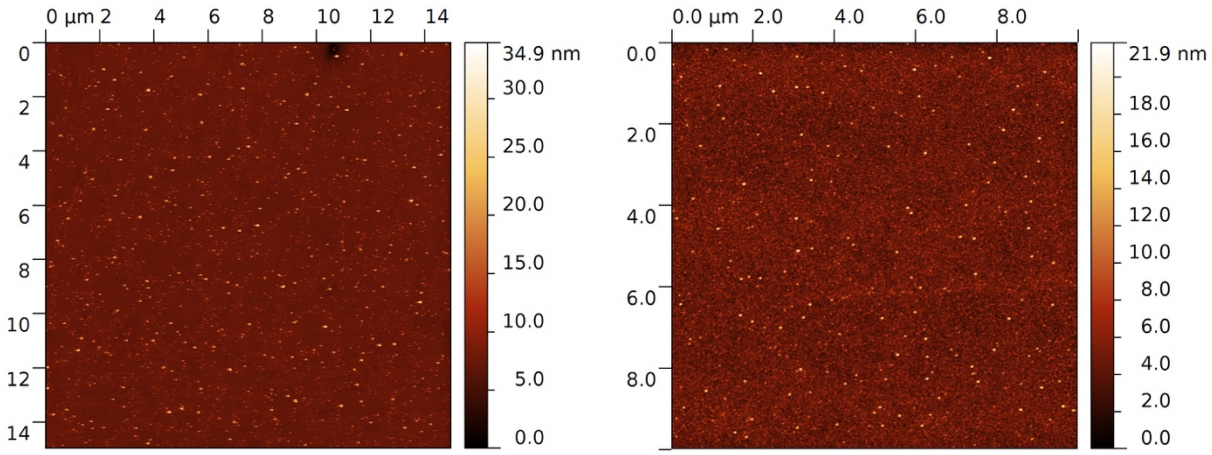



Figure 3.2: AFM micrographs of an $SiO_2$ substrate (top) and the same sample after transferring a layer of $MoS_2$ (bottom). The RMS roughness increased by 0.32nm during the process.

The transfer of h-BN onto $SiO_2$ (Figure 3.3) shows a similar result. In this image can be seen the border of the transferred region (lower-right) and the smooth $SiO_2$ surface (top-left). When the surface roughnesses of these two regions are calculated, the result is 0.70 nm and 0.94 nm, respectively.

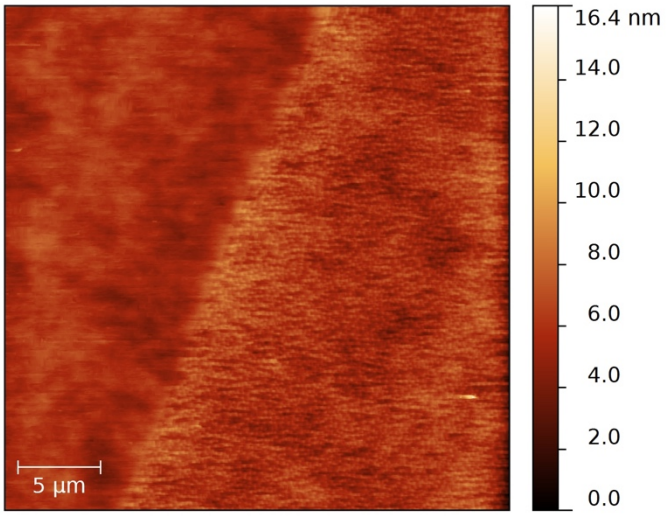



Figure 3.3: AFM micrograph showing border of h-BN transfer (bottom-right) onto $SiO_2$ (top-left). RMS roughness of the transferred area increased by 0.24 nm over that of the substrate region.

*2D Nanolayers on Paper*

Adding 2D materials to the papers affects the roughness of the laminated sample. As can be seen in Figure 3.4, adding $MoS_2$ onto a photo paper substrate reduced the RMS roughness slightly on photo paper (11.25 to 10.52 nm) and more strongly on glassine paper (25.6 to 18.31 nm). This indicates that while the surface of the substrate has a strong effect on the roughness of the stack, the 2D layer conforms well but imperfectly (as perfect conformation would exhibit no change to the roughness). In comparison to the results of the transfers to $SIO_2$, the roughness associated with the nanolayers themselves is negligible in comparison to the contribution from the substrate.

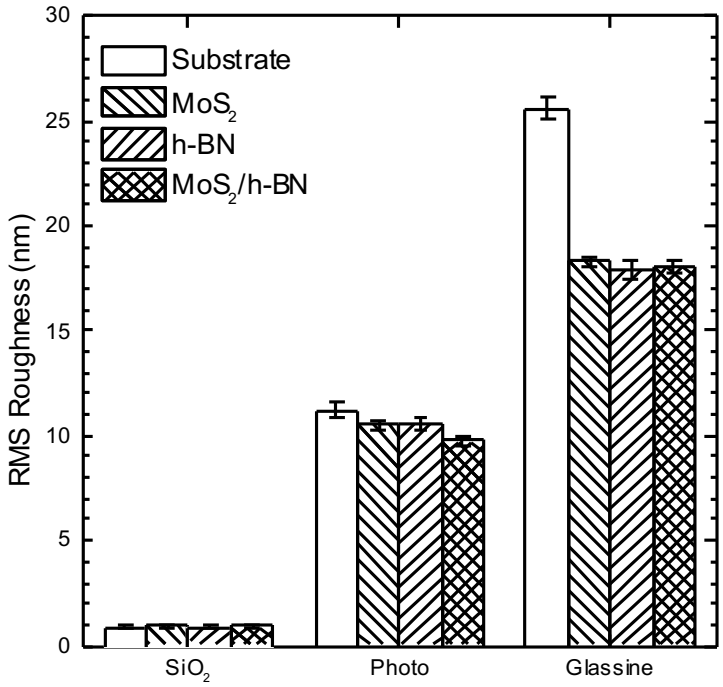



Figure 3.4: RMS roughness analysis of $SiO_2$ and paper substrates, as well as nanolayers transferred to these substrates

h-BN was investigated as an interlayer to isolate the $MoS_2$ from the substrate. It had a similar effect as $MoS_2$, in that it decreased the roughness by approximately the same amount (refer to Figure 3.4). When the layers were stacked upon one another, there was no significant improvement in roughness. It follows that a single 2D layer conforms as well as it can to the surface, and then any additional layers tend to conform to the interlayers below rather than directly to the surface.

### *3.1.2 Interfacial Adhesion of 2D Layers to Paper*

The adhesion strength of the nanolayers once transferred to the surface is an important property of the substrate-layer interactions. When graphene was tested on a series of samples

on photo paper, the material adhered very strongly to the surface. These data are shown in Figure 3.5. Each sample exhibited an onset where the adhesive would begin to fail, then the force required to continue to peel the surface would drop and level to a steady state plateau before finally reaching the end of the testing sample. The increase in force required at the end was due to the alignment and eventual rupture of the adhesive polymer as the two halves of the sample separated.

In each test, failure occurred not at the interface between the graphene and the paper substrate, but instead the adhesive material failed to adhere strongly to the graphene layer. This was evident in optical microscopy, as the graphene is easily visible on the paper surface. This allows for the determination of a lower bound for the adhesion strength of graphene to photo paper, at an average of 3.5 N/cm.

A second set of samples had been prepared, but the paper substrates had been coated with 100 nm of ALD deposited alumina ($Al_2O_3$) prior to the application of the graphene layer. When the samples were tested, it was instead the interface between the alumina coating and the graphene that failed, with the graphene remaining firmly adhered to the adhesive layer. These samples also showed a much lower adhesion strength at this interface, with the peeling strength averaging 1.75 N/cm instead of the previous 3.5 N/cm. The results from this set of samples is shown in Figure 3.6.

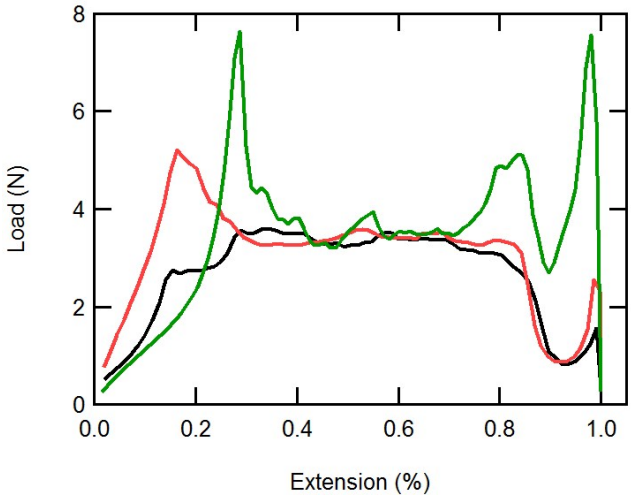



Figure 3.5: Results of peel tests of graphene on photo paper.

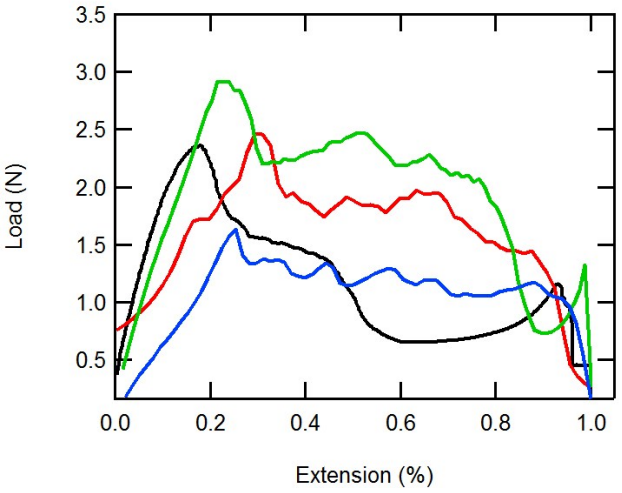



Figure 3.6: Results of peel tests of graphene on alumina coated photo paper.

*3.1.3 Raman Analysis of Nanolayers on Paper*

Raman analysis of 2D materials is a valuable method of identifying if the material is present following transfer, and can also provide additional insight into the properties of the layer. For example, graphene has a characteristic Raman spectrum that is formed primarily of three peaks: *G*, *D*, and 2*D*; two example spectra comparing graphene to bulk graphite can be found in Figure 3.7. The 2*D* and *G* peaks are indicative of graphitic carbon, and the ratio of their intensities and lineshapes are related to the number of layers of graphene present. The *D* peak is forbidden in pristine graphene samples, however it can be reactivated by disorder in the layer due to grain boundaries or other defects.[74]

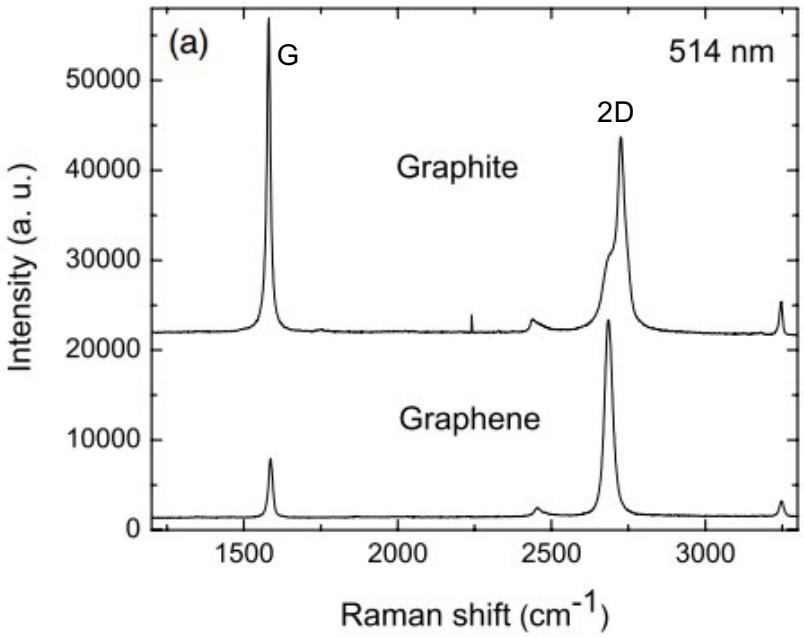



Figure 3.7: Raman spectrum of the 2D and G modes of graphene and graphite. The forbidden D mode is not shown in this figure, but would appear at 1350 $cm^{-1}$.[80]

$MoS_2$ also has characteristic behaviors that manifest changes to its Raman spectrum. Raman can be used to determine the number of layers of $MoS_2$ in a sample, as that is very closely tied to the peak separation between its $E_{2g}$ and $A_{1g}$.[90],[91] And increasing the temperature of the layer, by using a higher power excitation laser, causes redshifting of the $A_{1g}$ peak.[92]

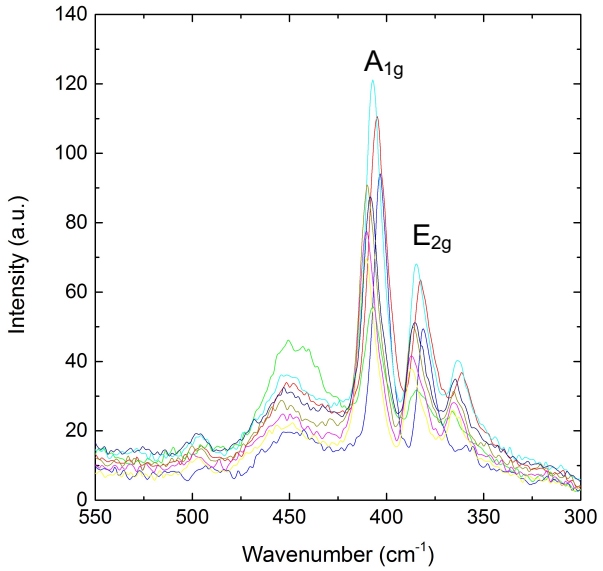



Figure 3.8: A selection of Raman spectra from analysis of $MoS_2$ on photo paper.

However, the two stimuli that are of primary importance for this study are strain and doping. Strain impacts the Raman spectrum by affecting the phonon frequency of both peaks. As the $E_{2g}$ mode is along the in-plane surface, strain applied to the surface in this direction has a stronger impact on this mode in comparison to the $A_{1g}$ (out-of-plane) mode. For small strains (less than $\varepsilon = 1\%$) it has been shown that biaxial stress, which can be caused by material being suspended above a surface, redshift the $E_{2g}$ mode by -5.2 $cm^{-1}$ and the $A_{1g}$ mode by -2.2 $cm^{-1}$ per percentage point of strain in the lattice.[93]–[95]

Doping of the material has a strong effect on the position and width of the $A_{1g}$ peak, but little on the $E_{2g}$. Redshift can be generated by the presence of n-type dopants at the surfaces of the interface between the substrate and MoS2. Working from the model proposed by Chakraborty, et.al.,[96] where extra electron concentration was directly correlated to the change in the $A_{1g}$ mode with the relationship having a slope of $2.6 \times 10^{12}$ $cm^{-2}/cm^{-1}$.[55][96]

In this case, the $E_{2g}$ is a better fingerprint for strain as it is nearly completely insensitive to doping effects. Once the strain for a sample is known, the doping level can be calculated. The total amount of $A_{1g}$ shift is a combination of the contribution from the strain effect – which can be determined using the strain value found from the $E_{2g}$ mode – and the presence of additional dopants or charge carriers. By compensating for the strain, the effective charge carrier concentration can be determined from the magnitude of the remaining $A_{1g}$ shift.

In investigating the effects of the paper substrate on the behavior of transferred $MoS_2$ layers, it was found that the samples on paper consistently had redshifted peaks for both modes when compared to samples transferred to or grown on $SiO_2$ substrates. It is also noteworthy that the samples had significant variability in the peak positions on paper. A representative set of spectra on photo paper is shown in Figure 3.8, while

Figure 3.9 gives a summary of the average values of peak position and Full-Width at Half-Maximum (FWHM) for the $A_{1g}$ and $E_{2g}$ peaks on both paper types.

In analyzing the results from the Raman study, it was found that the two paper surfaces did not affect the material in a predictable manner. In the case of the $E_{2g}$ mode, which is expected to be more sensitive to lattice strain than the $A_{1g}$, it was found that the rougher glassine sample

exhibited a lower degree of redshift than that of the photo paper. Adding the h-BN as an interlayer was intended to help mitigate some of the effects arising from the complex interface at the surface. In some cases, it helped improve the variability in the sample data, such as the $A_{1g}$ peak position and FWHM for the Photo paper samples. However, this effect was not seen for the $E_{2g}$ peak or any result on glassine paper. Additionally, when h-BN was used on Photo paper it was found that the actual peak position of the $A_{1g}$ peak shifted back toward that of the $SiO_2$ sample, but the $E_{2g}$ peak shifted further away from the reference location. The $A_{1g}$ position was similarly improved by applying h-BN between $MoS_2$ and the glassine substrate, but in this case the $E_{2g}$ was found to be relatively unaffected by the presence of this layer; for both peaks, the h-BN worsened their FWHM in the case of the glassine samples.

Ultimately, this result indicated that there is some combination of interfacial effects occurring at the surface which is not homogeneous across the surface of the samples. However, efforts to quantify exactly which mechanisms are effecting this behavior have not been fruitful.

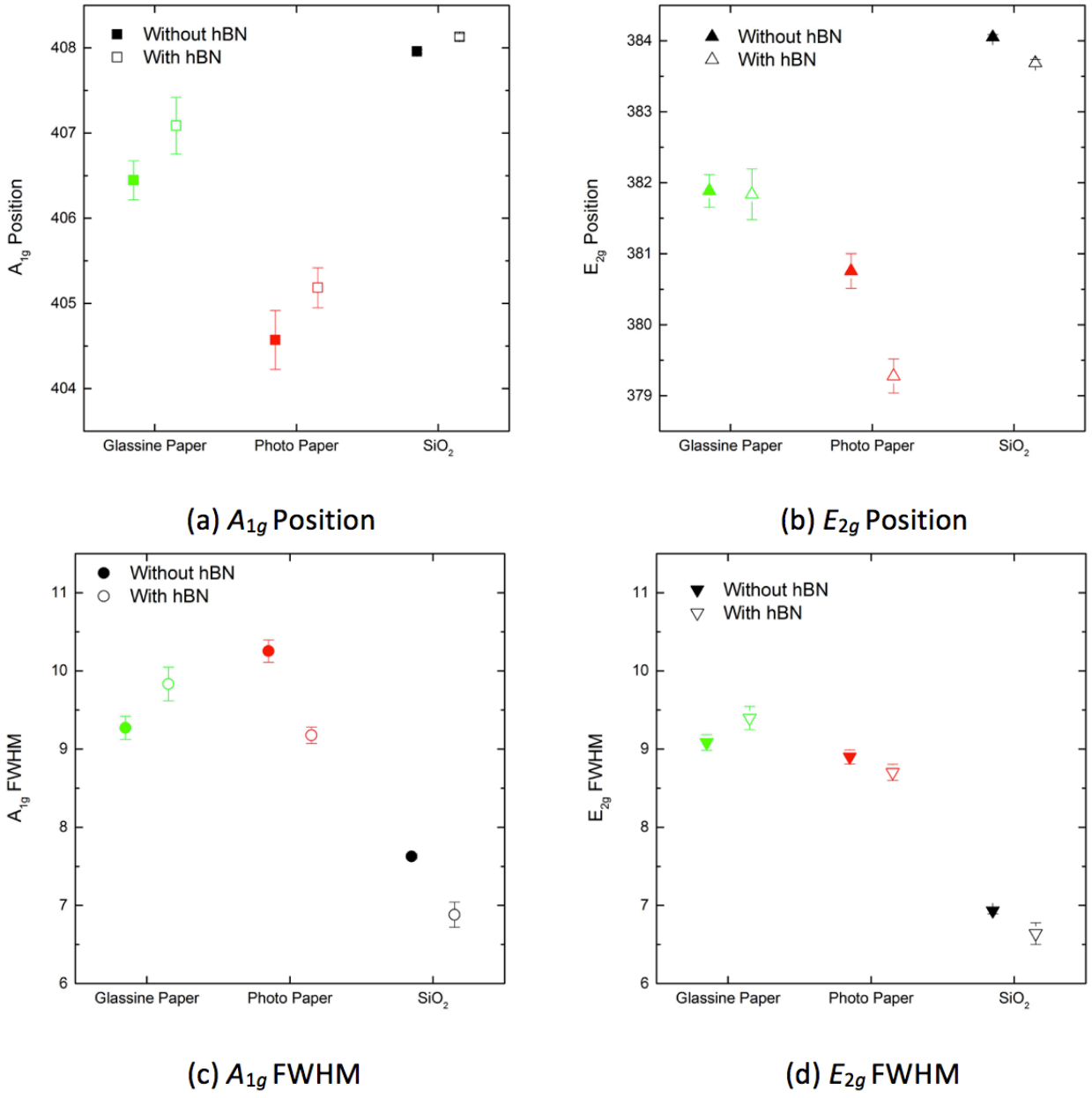



Figure 3.9: Raman peak position and widths of $A_{1g}$ and $E_{2g}$ modes of $MoS_2$ when transferred to paper substrates. Open symbols indicate that there is an interfacial layer of h-BN between the paper surface and the $MoS_2$.

## 3.2 Fabrication and Transfer of Devices to Paper Substrates

In order to understand how devices will ultimately perform on these cellulosic substrates, it is necessary to obtain real and functional device structures on these materials. The fabrication process for these devices is complex, requiring a number of processing steps. I will discuss three aspects of this fabrication process: the current methodologies for transferring 2D materials to arbitrary substrates, the process of transferring devices that were fabricated on silicon wafers to a final paper-based substrate, and how devices can be fabricated directly upon the paper itself.

The methodologies involved in either pre-fabricated transfer or *in situ* fabrication have both advantages and disadvantages. These have impacts on the design of the structures, the final yield of functioning units, and the properties of the devices. Solving the materials challenges associated with both of these two avenues is central to this work, and enables greater investigation to the properties of the substrate-nanolayer interface itself.

### *3.2.1 Improvement of Transfer Methodologies for Graphene, h-BN, and MoS2*

Investigation into what causes failure during the transfer of pre-fabricated devices to paper substrates allows for the improvement of the protocols, improving yields. Some considerations include exposure of the paper surface to liquids, which can impact the surface qualities in an adverse manner for good adhesion. This may necessitate a dry transfer, or a protective surface coating. Additionally, if the issue involves poor adhesion between the layers, this may be improved by using such techniques as plasma activation.

*3.2.2 Pre-fabricated Device Transfer*

Sets of test devices, comprised of $MoS_2$ FET and four-point-probe structures, were transferred to a prefabricated back-gate structure on photo paper. This substrate was fabricated by first evaporating 120 nm of Al onto a sheet of photo paper using e-beam evaporation to form a large-area planar back-gate electrode. Following this deposition, the substrate had an additional 80 nm of alumina ($Al_2O_3$) deposited at 100$^{o}$C using low temperature atomic layer deposition (ALD) to act as the gate dielectric.

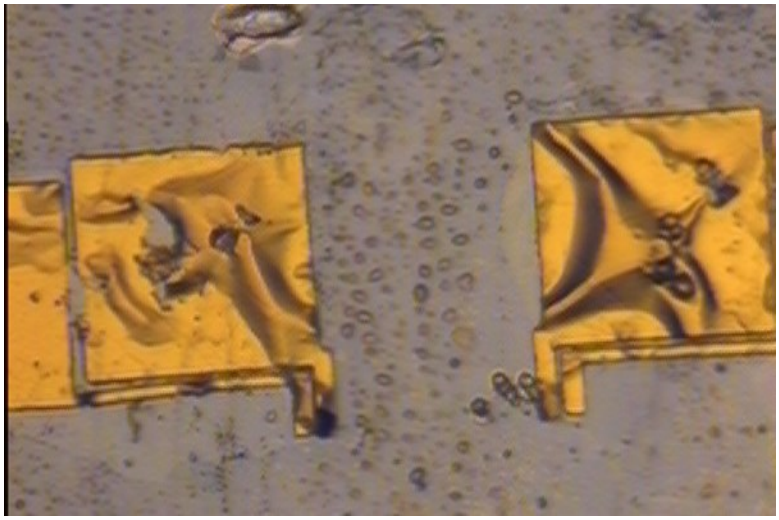


Figure 3.10: Poor adhesion between the contact pads on transferred $MoS_2$ devices and the target paper substrate.

These transfers to the back-gate structure have not succeeded in producing functional devices. One major issue appears to involve the adhesion between the $MoS_2$ layer and the underlying oxide/electrode/paper substrate. This manifests as a large migration of contact electrodes and channels out of place and alignment, which renders the device useless.

Additionally, when this occurs it is much more likely to trap fluid under the contact. This liquid or gas causes the contact to bulge away from the surface, and can distort its shape, such as can be seen in Figure 3.10.

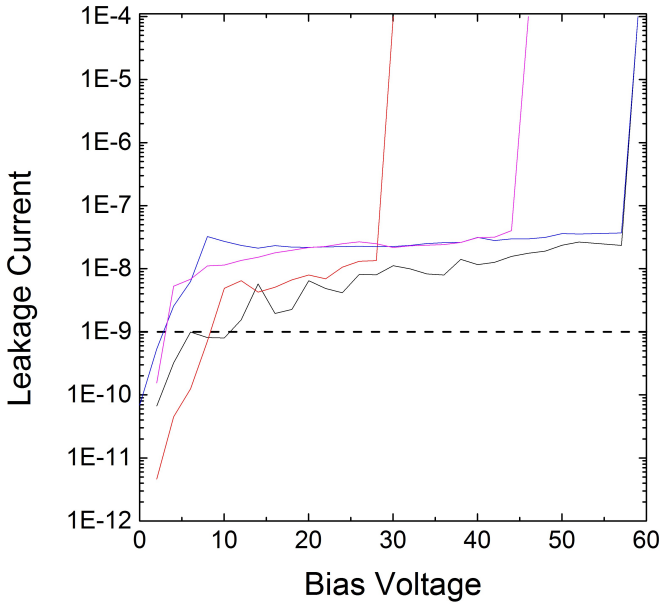



Figure 3.11: Plot of leakage current vs. gate voltage for 80 nm $Al_2O_3$/120 nm Al/Photo Paper.

Another significant factor impacting the measurement of these devices is the quality of the underlying gate oxide material. There are two primary concerns at this time: high magnitudes of leakage current through the gate and low limits on the breakdown voltage of the material. As can be seen in Figure 3.11, the current material being used does not perform as is expected for alumina. Generally, alumina gate oxide layers experience breakdown at voltages approaching 5–10 MV/cm,[97] which is far greater than the 250 kV/cm of the alumina gate oxide on paper. In addition, typical leakage currents for high-quality $Al_2O_3$ films are as low as $10^{-10}$A/cm$^2$.[97] The

leakage currents seen for these devices on paper is a significantly higher $10^{-5}$A/cm$^2$. This type of behavior serves to indicate an issue with the ALD growth process when using a paper-based substrate.

The issue with the ALD growth process likely stems from the low temperature stability of the paper substrates. Because the paper incurs damage when exposed to temperatures exceeding 115$^o$C, the deposition was performed at a low 100$^o$C. The low deposition temperature can lead to poor film stoichiometry and increased concentrations of defects; in comparison, most ALD reactions are performed between 250-300$^o$C, and are frequently annealed at even higher temperatures to further improve film properties.

### *3.2.3 in situ Device Fabrication*

*in situ* fabrication methods, as compared to the transfer-based method discussed above, offer great benefits to the development of test devices on paper substrates. While transfer methodologies are expected to improve, they are always going to involve some degree of damage or component drift that will impact the final yield of functioning structures. *in situ* fabrication allows for the devices to be directly fabricated on the paper substrate, providing higher yields and better performing devices (see Figure 3.12). In particular, utilizing the *in situ* process allows for the improvement of the adhesion of the source, drain, and gate contacts could be improved using interfacial metal layers to improve the adhesion between the evaporated gold metal and the underlying substrate, improvement to the properties of the gate oxide due to eliminating exposure to etchants (a required step when transferring prefabricated structures), and allows for the use of top-gated structures for additional channel modulation effects.

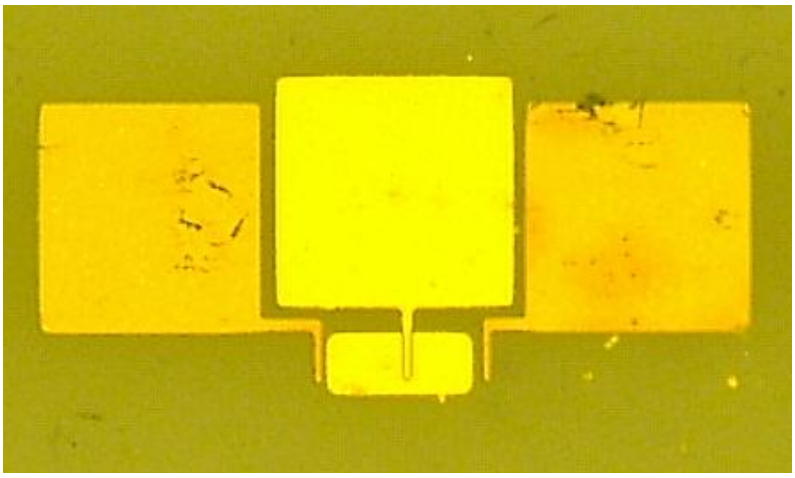


Figure 3.12: Optical image of in situ fabricated FET structure on photo paper

In order to accomplish this, the paper needs to be capable of sustaining exposure to photoresist, development, and lift-off solutions for short periods with minimal absorption into the paper's surface layers or bulk. As papers typically are highly absorptive of fluids, it is important to determine how this intercalation can be prevented. As discussed previously, I have shown that by utilizing a thin surface coating of parylene, samples of photo paper and copy paper can be modified to have quality barrier properties; parylene coated samples resist absorption of water-based solutions, solvents (e.g. acetone and IPA), and photoresists (both positive and negative).

The paper surface also needs to be sufficiently smooth for high-fidelity exposure of the mask pattern into the resist; too much surface waviness could impact this patterning step by causing image blurring, under-, or overexposure. To this end, vacuum is utilized to assist in holding the paper flat against the alignment chuck during lithography steps. Photo paper has sufficient mechanical robustness to support itself and remain flat during the application of vacuum. In contrast, the thin glassine paper was not sufficiently rigid to span the grooves in the chuck without

severe deformation; this deformation precluded the ability to successfully transfer the mask pattern to the sample.

### 3.3 Electronic Characterization of Devices on Cellulose

Graphene-based single layer field effect transistor structures were fabricated onto a substrate of photo paper coated with 1μm of parylene-C. While yields of operational devices were low, a number exhibited some channel modulation under top-gate bias conditions as shown in the transfer curve in Figure 3.13. The behavior of these devices is not what is typically expected; while they show the presence of the graphene's Dirac point on the forward sweep, when reversing the bias the previously seen modulation is not observed. Similar behavior is seen in each of the functioning devices from the sample.

It is believed that this response is due to issues with the high-k oxide used in the gate, and are likely to be caused by the ALD deposition parameters used. Due to the limitations of the paper substrate, the deposition temperature for the oxide layer is limited to 100$^{o}$C. While this temperature is sufficient for the deposition reactions to proceed, the material that is formed is non-ideal; higher levels of carbon from unreacted ligands are often present, and the films are generally non-stoichiometric. These impurities and defects create opportunities for the formation of trap states in the material as well as mobile charges.

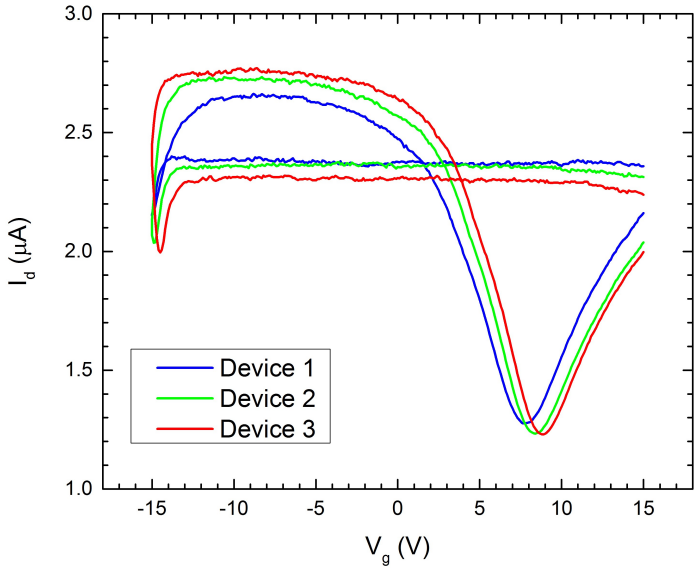



Figure 3.13: Transfer curve ($I_d$-$V_g$ plot) for a single layer graphene FET. Notable features are the variations in gate bias dependence between forward (negative to positive) and reverse bias sweeps, and the occurrence of two minima in the curve.

To investigate this further, MOSCAP structures using both alumina and hafnia ($HfO_2$) were fabricated on silicon wafers using identical deposition parameters to the process used during the deposition of the alumina gate oxide from the previous devices. Capacitance-Voltage (C-V) measurements, shown in Figure 3.14, show the characteristic hysteresis of the presence of trapped and mobile charges, as predicted from the previous results. The hafnium oxide samples were the focus, due to the higher dielectric constant of hafnia over alumina.

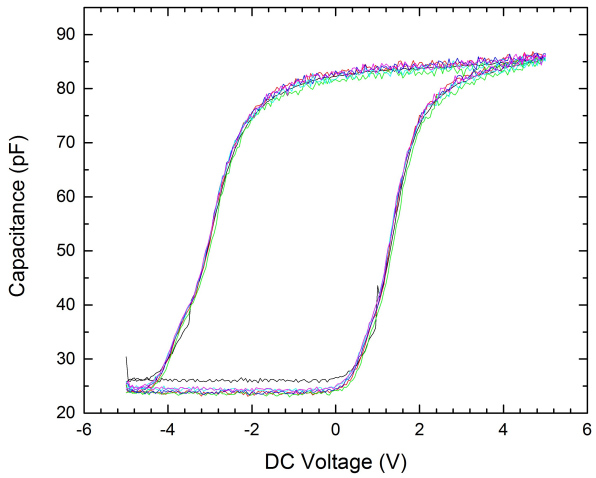



Figure 3.14: C-V measurements of the ALD deposited hafnium oxide exhibit large hysteresis between forward and reverse sweeps, indicative of charge trap states and mobile charges.

Methods to improve the quality of the oxide-based dielectrics which are compatible with the paper substrate materials are limited, as they generally require an elevated temperature annealing treatment. To avoid this, there are a number of possible replacement candidates for this gate dielectric. Hexagonal boron nitride, a 2D material discussed previously, is a promising candidate for this application. h-BN has a similar dielectric constant to silica while simultaneously possessing flexibility and strength, and is capable of withstanding aggressive oxide etch processes. As it is transferred, much the same as graphene or $MoS_2$, it is not subject to the same limitations as the oxide growth processes and can have much higher performance than the oxides.

### 3.4 Characterization of $MoS_2$ Synthesis Method

The $MoS_2$ films were characterized using Raman spectroscopy. This technique allowed for the identification of the number of layers of $MoS_2$ synthesized during the growth as well as the spatial uniformity across the sample. Figure 3.15(a) illustrates an example Raman spectrum of an $MoS_2$ film using the 488 nm laser. The sample can be confirmed as trilayer, as it has a separation between the $E^1_{2g}$ and $A_{1g}$ peaks of 23.5 $cm^{-1}$. The mapping function of the system was utilized to highlight the uniform nature of the synthesized film, and Figure 3.15(b) shows the peak separation for Raman measurements at 15 different points spread over an area of several $cm^2$ on the $MoS_2$ film. The average peak separation of 23.53 ± 0.06 $cm^{-1}$ corresponds to a thickness variation of less than a monolayer across the sample, which indicates the excellent uniformity of these synthetic $MoS_2$ films.

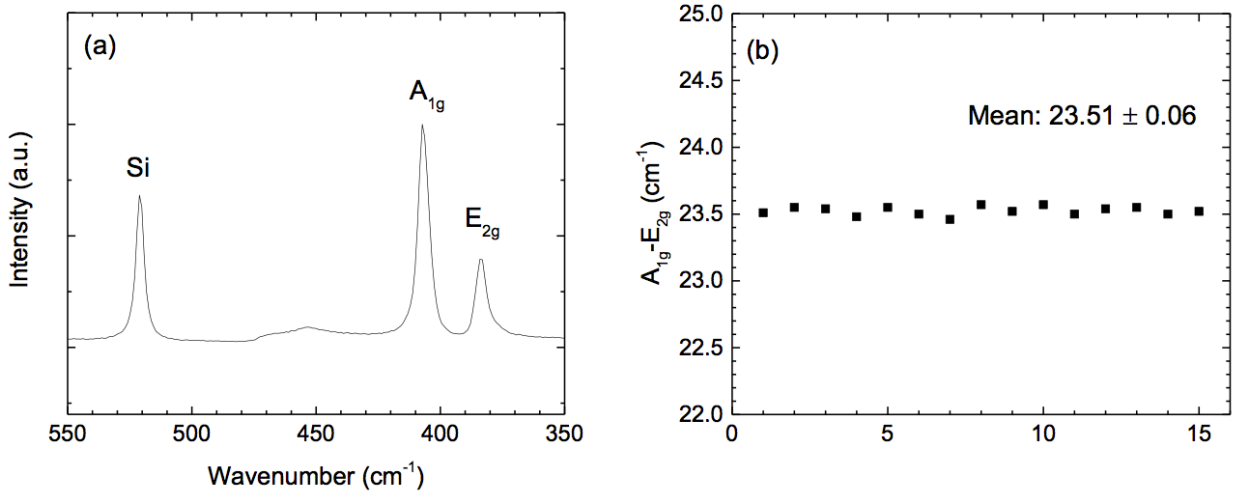



Figure 3.15: (a) Example Raman spectrum of a $MoS_2$ sample showing a peak separation of approximately 23.5 $cm^{-1}$, indicating that the sample is trilayer. (b) Peak separation results for 15 individual Raman spectra taken from across a 4" sulfurized wafer. The average peak separation is 23.51 ± 0.06 $cm^{-1}$, which represents a thickness error of less than one layer.

The PL response of the $MoS_2$ film is another valuable metric for analyzing the quality of the synthesized layers. $MoS_2$ exhibits two characteristic peaks in PL; the first represents the $A^-$ and $A^0$ excitons, whose response overlaps one another, the second arises solely from the B exciton. Both peaks are expected to be present in the semiconducting 2H form of the $MoS_2$ crystals. Suppression or quenching of the B mode can indicate a transition toward 3R stacking, which breaks the hexagonal crystal symmetry and does not exhibit semiconducting behavior.[98]

Using the PL response, we have investigated the impact of utilizing the reducing $Ar/H_2$ gas mixture during the film synthesis step. The inclusion of hydrogen is used to improve the reaction kinetics inside the chamber, but has the potential to trap hydrogen interstitials in the lattice and between the layers during the growth. The hydrogen content of the mixture was varied from 0 to 33%, and the resultant samples were characterized. The results of the PL on these samples are shown in Figure 3.16.

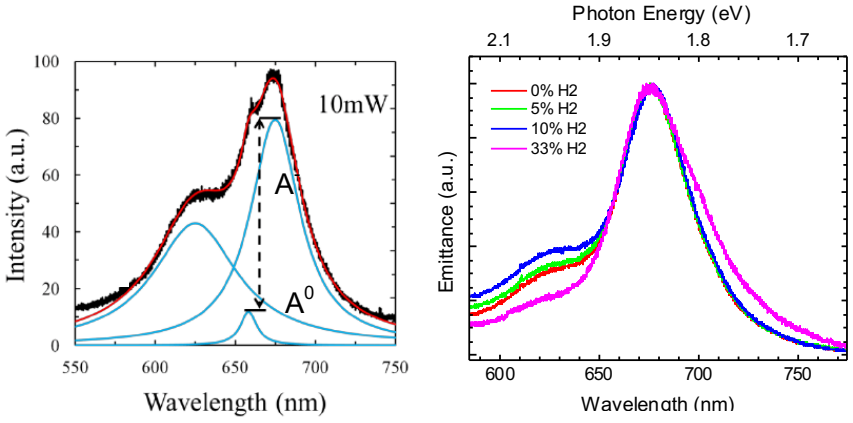



Figure 3.16: (Left) PL spectrum of exfoliated $MoS_2$ monolayer.[99]
(Right) PL spectra (532 nm illumination) of trilayer $MoS_2$ samples synthesized in atmospheres containing various concentrations of $H_2$.

As can be seen, there is some improvement to be gained by utilizing hydrogen during the growth, due to the slight improvement in the response of the B exciton at around 625 nm. However, with a heavy excess of hydrogen present in the chamber, the reducing atmosphere appears to degrade the resulting material. Relative to the samples with lower $H_2$ exposure, the peak from the B exciton is heavily diminished in intensity, as well as the large peak from the activity of the A excitons broadens significantly.

# CHAPTER 4: CONCLUSIONS

Cellulosic materials are promising candidates as substrates for flexible electronics technology. By being environmentally friendly, compatible with scalable manufacturing techniques, and having a low cost to fabricate, they are ideal to help bring about the vision of pervasive computing to daily life.

2D nanomaterials, such as graphene, $MoS_2$, and h-BN, are also poised to be a possible post-silicon set of technologies. These high-performance materials are compatible with the requirements of paper-based electronics, and are strong, flexible, and have a variety of useful electronic properties that can be leveraged to create a wide variety of devices for many applications.

This project has shown the importance of understanding the details involved in the synthesis stage can have a direct impact on the quality and performance of the resulting 2D materials. Additionally, this project has succeeded in investigating the properties of the interfaces between paper substrates and 2D materials.

The procedures involved in transferring prefabricated devices from silicon to paper have been tested, but current methods are insufficient to produce functional structures. A number of functioning FET devices exhibiting field effect modulation have been fabricated directly on paper using graphene as the active material, however their performance was found to be poor due to a highly defect gate dielectric layer.

# CHAPTER 5: RECOMMENDATIONS

## 5.1 Dry Transfer Methodologies

One method for improving the transfer methods described above is to implement a “dry transfer” of the 2D layer or the fabricated devices. The primary advantage of this method is to avoid the necessity of exposing the substrate and device to any solutions or solvents. This is particularly useful when considering absorbent paper materials, which are often affected negatively by exposure to such environments.

A number of methods have been reported for dry transfer of 2D materials. These mostly utilize the low adhesion coefficients of low-surface energy materials. Polytetrafluoroethylene (PTFE, Teflon) is the quintessential example of a material with this property, but it is rigid and generally difficult to work with. Instead, polydimethylsiloxane (PDMS) is very commonly used. PDMS is a transparent elastomer with extremely low surface energy. It is an integral component of many microfluidic designs, and as such methods for patterning and fabricating “stamps” of this material are well known.[100]

PDMS stamp techniques have been shown for graphene transfer, and rely on the higher adhesion energy between the target substrate and the nanolayer than that between the nanolayer and the PDMS carrier. This allows for the material to be transferred simply by affixing it firmly to the target, and then gently peeling off the PDMS.[101]–[106] A diagram of this method can be found in Figure 5.1.

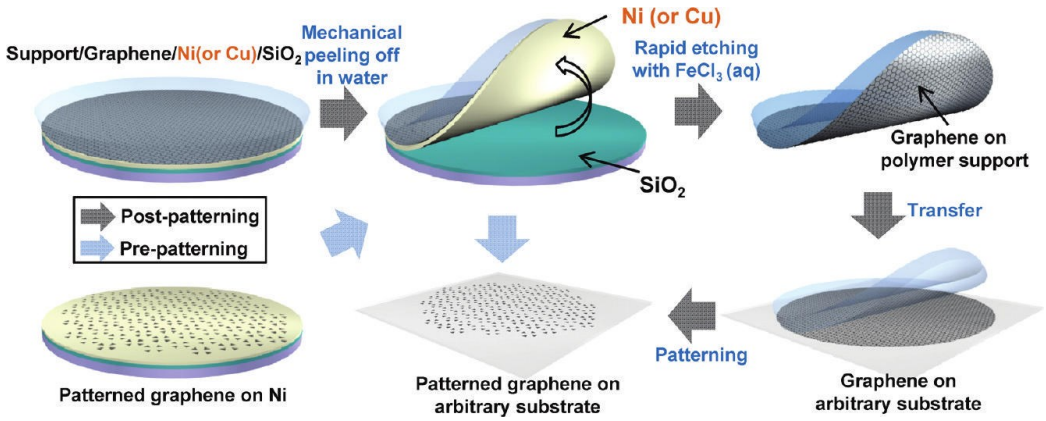



Figure 5.1: A dry transfer method for graphene-based devices and layers.[101]

When considering this method, two main concerns arise. First involves the reliable dissociation of nanolayers or device stacks from the carrier polymer. This may be understood by carefully testing each stage of the transfer, beginning from the creation of the stamp and testing each subsequent stage to ensure desirable behavior. An additional question is if any properties of the stamp will affect the devices following transfer; transfer residues are a major concern when using any carrier polymer-assisted technique, and understanding of the performance impact of any residues on the device behavior will drive development of improved cleaning procedures, if necessary.

Future development of dry-transfer techniques should help to improve the performance of devices. The paper surface would not come into contact with any liquids or heat prior to application of the transfer material, and as such it will have the least impact on the properties of the paper. Additionally, this should help avoid damage and corrosion of any back-gate/gate oxide layers by minimizing exposure to water (which instigates corrosion of aluminum gate into alumina) and any contaminants (e.g. oxide etchant).

## 5.2 Gate Dielectric Improvement

### *5.2.1 Plasma-Enhanced ALD*

Plasma-Enhanced or Plasma-Assisted ALD (PE-ALD or Plasma ALD), is a method of improving the quality of films by activating the reactant species using a inductively-coupled plasma (ICP) system. The reaction kinetics are improved by the increased reactivity of the ionized radicals created within the plasma.[107]

An example schematic of what the design of a PE-ALD system would look like is presented in Figure 5.2. In this scenario, a plasma gas is passed through an ICP generator and ignites into a plasma. The activated plasma streams toward the substrate chamber, where it joins a flow of precursor reactant. The plasma ionizes a portion of the precursor molecules, and the gas mixture streams toward the substrate surface. In this particular example, the substrate chuck is biased in order to accelerate ions toward the sample surface, improving the reaction kinetics by increasing the kinetic energy of the arriving species as well as limiting precursor waste via sidewall deposition. During the purge step, the plasma may or may not be extinguished in order to minimize surface erosion due to sputtering processes. Once the chamber has been purged, the second half-reaction takes place in a similar manner. One or both of the reactions may utilize the plasma step. Additionally, some systems mix the plasma and reactant gases prior to entering the plasma generator, which would increase the efficiency of the reaction but may make plasma ignition more challenging.

For future progress on this study, the use of PE-ALD would be beneficial in order to help improve the quality of the deposited gate dielectric film when using paper substrates. This may

allow for sufficient improvement to overcome the challenges faced when growing the dielectric at the low temperatures required by the paper.

However, care must be taken as the 2D materials are highly sensitive to plasma bombardment; due to the fact that they are only a few atoms thick, it is very easy for sputtering reactions to heavily damage or destroy a transferred layer. To this end, some ALD systems are equipped with a “remote” plasma system, where the bulk of the ionized plasma is contained in a separate zone from the substrate, and reactant species are passed through this zone prior to entering the deposition chamber. This configuration would likely be ideal for the successful application of a PE-ALD technique to these 2D devices.

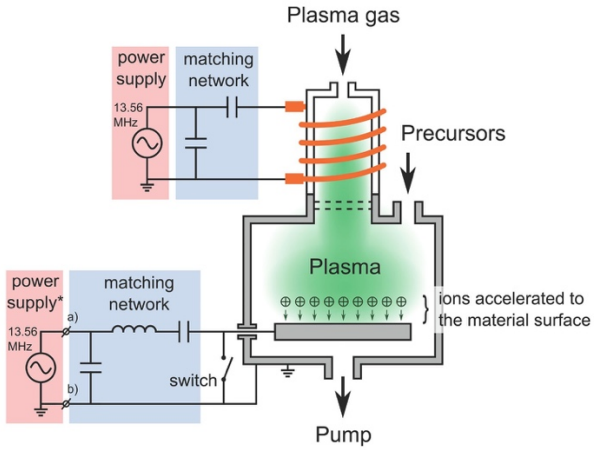



Figure 5.2: Schematic for the design of a PE-ALD deposition tool.[107]

*5.2.2 h-BN as a Gate Dielectric*

Another alternative for the FET gate dielectric is to use a layer of h-BN in place of the oxide materials. This would provide the opportunity to avoid a deposition step altogether, as the h-BN

is synthesized and then transferred onto the target just as with graphene or the TMDs, forming a structure much like that in Figure 5.3. Because there is no deposition step, the quality of the h-BN is not limited by the properties of the paper substrate. To this end, one could use either mechanically exfoliated h-BN crystals or CVD grown samples to supply the material.

Additionally, the native flexibility of the h-BN layers affords additional mechanical robustness against damage incurred by flexing the heterostructure; crystalline oxides are still prone to some mechanical damage when strained repeatedly.

One challenge would be performing a high quality transfer of the material without trapping material on the surface or at the interface between the active layer and the h-BN. Once the layer is transferred to the paper substrate, options for cleaning the surfaces and interfaces are limited.

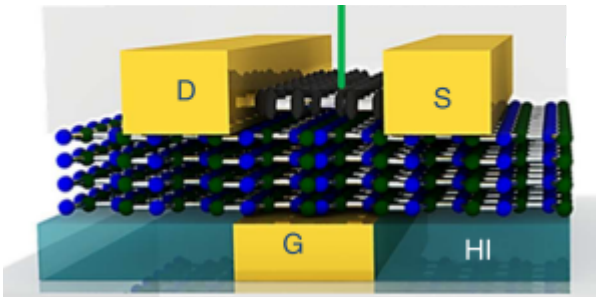



Figure 5.3: Example structure of a graphene FET using four layers of h-BN as a gate dielectric.[37]

### 5.3 Nanocellulose Surface Coatings

One way to assist in improving the surface quality of the paper substrates is to apply a planarization layer. Examples of nanocellulosic layered composites, such as NFC on traditional papers (see Figure 5.4),[54] have been shown to exhibit highly smooth surfaces.

These samples can be fabricated using a variety of methods (e.g. spin coating or vacuum filtration) from commercially available stock materials. This would allow for the creation of a high-quality 100% cellulosic substrate for the application of 2D materials.

However, it would be important to evaluate the reliability of these substrates. CN materials are often soluble in aqueous solutions,[66] which would limit their compatibility with fabrication processes without the application of additional barrier layers (e.g. thin Parylene). As such, it would be a good candidate as a high-quality substrate if the transfer of pre-fabricated devices or dry transfer techniques are improved.

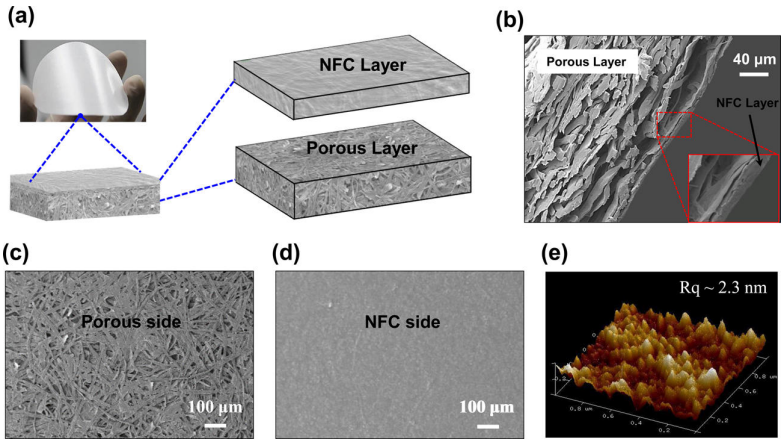



Figure 5.4: SEM and AFM images of a layer of NFC atop a porous traditional paper substrate[54]

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