

**AN ASSESSMENT OF SILICON-GERMANIUM BICMOS
TECHNOLOGIES FOR EXTREME ENVIRONMENT
APPLICATIONS**

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AN ASSESSMENT OF SILICON-GERMANIUM BICMOS TECHNOLOGIES FOR EXTREME ENVIRONMENT APPLICATIONS

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To José, and Maria Lourenco

whose sacrifice and unwavering support

have allowed me to be where I am today.

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SUMMARY

The research presented in this thesis serves as an evaluation of silicon-germanium (SiGe) technology for electronic systems intended for wide-temperature and radiation intense environments.

Chapter 1 presents the motivation for this research, focusing on the need for extreme environment capable semiconductor processes. The limitations of bulk silicon processes are discussed and SiGe technology is introduced as a possible platform to extend the usable temperature range of silicon into cryogenic and high temperature environments. The device theory governing the performance improvements in SiGe heterojunction bipolar transistors (SiGe HBTs) is discussed and cryogenic measurement results validate SiGe technology's potential for electronics in low temperature environments.

Chapter 2 serves as a broad introduction to the world of radiation effects, covering the important issues of ionizing radiation on semiconductor materials and electronics. The natural radiation environment is characterized and the effects of these radiation sources on orbital and deep-space electronics are reviewed. The concepts of total ionizing dose (TID) and single event effects (SEE) are introduced, providing a background for the studies presented in future chapters.

Chapter 3 highlights a study of radiation effects in a state-of-the-art fourth generation SiGe BiCMOS process. The total dose and transient response of this highly-scaled SiGe technology are compared to data for earlier SiGe BiCMOS generations in order to assess the impact of device scaling on radiation response.

Chapter 4 covers two studies investigating the suitability of SiGe BiCMOS for

high temperature (up to 300 °C) applications. SiGe devices and circuits show increased leakages, but otherwise acceptable operation at elevated ambient temperatures. A radiation hardening by design (RHBD) technique, originally intended for SEE mitigation is shown to reduce device leakage currents, thereby extending the upper temperature limit for SiGe-based electronics.

Chapter 5 provides concluding remarks, recaps key contributions and discusses future research work. The research in this thesis has led to three separate publications that are listed below (in chronological order).

- D. B. Thomas, N. E. Lourenco, J. D. Cressler, and S. Finn, “SiGe Amplifier and Buffer Circuits for High Temperature Applications,” *Proceedings of the 2010 IMAPS International High-Temperature Electronics Conference*, pp. 379-385, 2010.
- D. B. Thomas, L. Najafizadeh, J. D. Cressler, K. A. Moen, and N. E. Lourenco, “Optimization of SiGe Bandgap-Based Circuits for up to 300C Operation,” *Solid-State Electronics*, vol. 56, pp. 47-55, 2011.
- N. E. Lourenco, R. L. Schmid, K. A. Moen, S. D. Phillips, T. D. England, and J. D. Cressler, “Total Dose and Transient Response of SiGe HBTs from a New 4th-Generation, 90 nm SiGe BiCMOS Technology,” in *2012 IEEE Radiation Effects Data Workshop*, 2012

CHAPTER I

INTRODUCTION

This chapter provides the motivation for this thesis and serves as an introduction to silicon-germanium technology.

1.1 Motivation

Electronic systems intended for orbital, lunar, interplanetary, and deep-space applications face a host of design challenges. Ambient temperature is a major design constraint for spacecraft electronics. The lunar surface, for example, has an average surface temperature between -180 °C and 125 °C. The surface temperature of Mars is relatively cold, ranging between -143 °C to 35 °C due to its fairly elliptical orbit (eccentricity: $\epsilon \approx 0.093$, second only to Mercury) and thin atmosphere. The mean surface temperature of Venus, on the other hand, is a scorching 462 °C. In addition to these extremely wide temperature ranges, these systems must endure heavy bombardment of ionizing radiation from solar, planetary, and galactic sources.

Extreme environments are defined as environments with ambient temperatures outside of military specification (mil-spec, -55 °C to 125 °C) range and intense exposures to ionizing radiation. Clearly it is no easy task to design devices and circuits capable of handling such extreme conditions. A traditional approach to ensure long-term operation in extreme environments is the use of a warm electronics box (WEB). A WEB is a shielded (metallic), insulated enclosure that provides protection from radiative heat loss and ionizing radiation. Light-weight materials, such as silica aerogels and titanium are commonly used to reduce unnecessary weight, but since present-day launch costs can be prohibitively high, \$10,000 to \$25,000 per kilogram to low-Earth orbit (LEO) [3], there is a substantial interest in new semiconductor technologies that

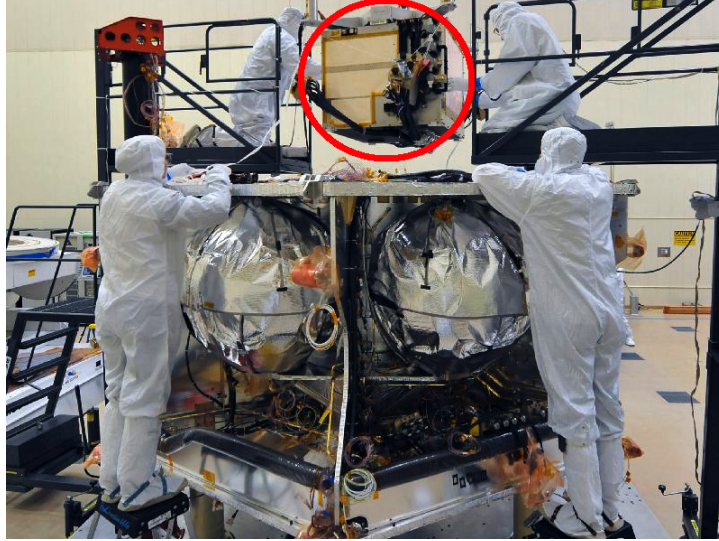


Figure 1: The Juno spacecraft being assembled at JPL. The radiation vault has been highlighted.

can tolerate unshielded exposure to these extreme conditions. The encircled module in Figure 1 is the radiation vault used in NASA’s Juno spacecraft. This protective enclosure weighed approximately 200 kilograms and shielded the Juno spacecraft’s central electronics from Jupiter’s harsh trapped radiation environment.

For over forty years, silicon has been the semiconductor of choice for most general-purpose electronics. During this time, bulk silicon platforms have followed the exponential growth pattern predicted by Intel co-founder Gordon Moore in 1965 [48], driving remarkable feats in digital storage and communication. However, lateral shrinking of silicon technologies is approaching a physical limit and many “vanilla” silicon processes are unable to provide the performance necessary for high-speed digital and RF communications. In addition to these application-induced design constraints, bulk silicon bipolar junction transistors (Si BJTs) experience performance degradation at low and high temperatures due to low emitter-base injection efficiency and thermal runaway respectively. III-V semiconductors, such as gallium arsenide (GaAs) provide superior RF, noise, and radiation performance, but lack a native oxide and the

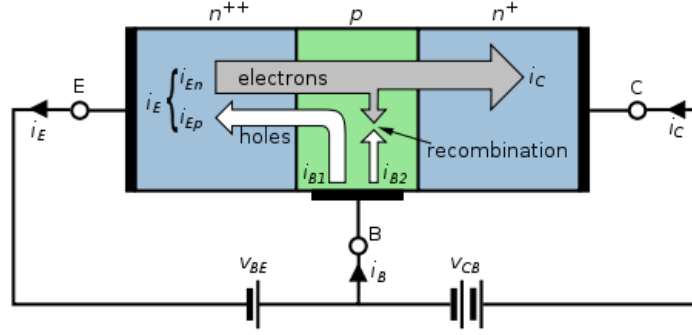


Figure 2: A simplified diagram of a bipolar junction transistor.

economies of scale available to the silicon industry. Luckily, silicon bandgap engineering can provide a way to combine III-V performance with the yield and cost advantages of bulk silicon into an ideal platform for wide-temperature, radiation intense environments.

1.2 *Silicon-Germanium Technology*

The silicon-germanium heterojunction bipolar transistor (SiGe HBT) can overcome the limitations of Si BJTs. The idea of incorporating germanium into the active area of a Si BJT is not a new one, dating back to William Shockley and his original 1951 patent of the npn bipolar transistor [69]. Herbert Kroemer generalized the concept of the HBT and provided the theoretical understanding of bandgap engineering in 1957 [35]. While the theoretical framework of bandgap engineering and the HBT were in place, process engineers were unable to epitaxially grow defect-free SiGe films until the mid-1980s [59], [47]. IBM demonstrated its first generation SiGe BiCMOS process in 1992 [27] and very recently revealed its state-of-the-art fourth generation SiGe BiCMOS process [56].

As shown in Fig. 2, a Si BJT can be simplified as two p-n junctions placed side-by-side to create a three terminal device. From basic p-n junction physics, majority carriers diffuse from one doped region into an adjacent region of opposite doping type and vice versa. As electrons and holes diffuse across these junctions, they leave behind

ionized donor or acceptor atoms (fixed positive charge in n-type silicon, fixed negative charge in p-type silicon), giving rise to depletion or space charge regions (SCRs). The fixed charge at either side of the SCR generates a built-in electric field and potential barrier that maintains charge neutrality once the system reaches equilibrium. Applying an external voltage across these junctions reduces this potential barrier, resulting in an exponential increase in carrier diffusion across the SCR. If one side (the emitter) of the p-n junction is more heavily doped, then most of this current across the SCR is due to the majority carrier diffusion from the highly doped side. Furthermore, if the lowly doped side (the base) is made extremely thin or narrow, then only a small fraction of these injected carriers will recombine in the base leaving the majority of carriers to diffuse across the base, sweep across the second SCR, and be collected at the third terminal (the collector). Therefore for a small input current into the base terminal of the transistor, a large current is driven between the emitter and collector terminals. Improving the current gain in a Si BJT is accomplished by manipulating the base doping profile. Since current gain is defined as the ratio between the output collector current and input base current, current gain can be improved by reducing the base doping level. However, there are practical performance level limitations that restrict the minimum base doping concentration because the reduction in base doping also increases the intrinsic base resistance, resulting in poor high-speed performance and higher device noise. Therefore there is a fundamental tradeoff between current gain and speed/noise performance for a Si BJT.

The SiGe HBT utilizes bandgap engineering to overcome this fundamental limitation in homojunction BJTs. The introduction of germanium into the silicon lattice lowers the effective bandgap of the material (now a SiGe alloy) and causes a reduction in the energy level of the conduction band, which reduces the potential barrier seen by electrons in the emitter and boosts carrier injection into the base. This effectively decouples the base doping concentration from current gain, so the base can be doped

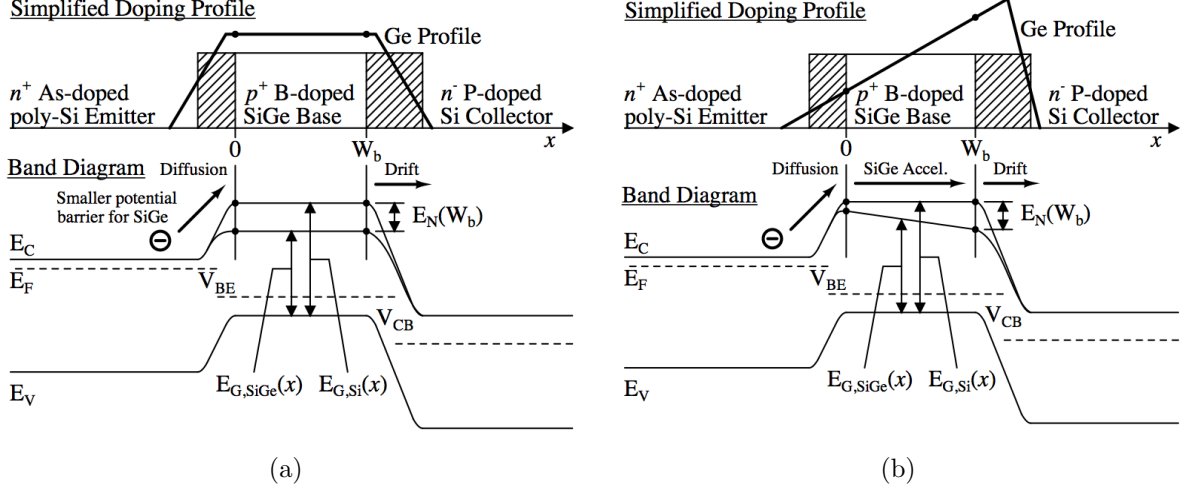


Figure 4: Simplified HBT schematics and energy band diagrams for a) constant (box) Ge profile and b) linearly graded (triangular or ramp) Ge profile (after [14]).

area of the box or triangular profile. By defining the Ge-induced bandgap grading factor as

$$\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0) \quad (1.1)$$

where $\Delta E_{g,Ge}(0)$ and $\Delta E_{g,Ge}(W_b)$ are the Ge-induced reductions in the base energy bandgap at the emitter-base and collector-base edges of the quasi-neutral base, Eqs 1.2 - 1.4 describe the improvement in current gain (β), Early voltage (V_A) and base transit time (τ_B), three important parameters that describe the *dc* and *ac* performance of a bipolar transistor between a comparatively built (similar doping profiles, identical emitter contact topology, etc.) SiGe HBT and Si BJT.

$$\left. \frac{\beta_{SiGe}}{\beta_{Si}} \right|_{V_{BE}} = \frac{\tilde{\gamma} \tilde{\eta} \Delta E_{g,Ge}(grade) / kT}{1 - e^{-\Delta E_{g,Ge}(grade) / kT}} e^{\Delta E_{g,Ge}(0) / kT} \quad (1.2)$$

$$\left. \frac{V_{A,SiGe}}{V_{A,Si}} \right|_{V_{BE}} \simeq e^{\Delta E_{g,Ge}(grade) / kT} \left[\frac{1 - e^{-\Delta E_{g,Ge}(grade) / kT}}{\Delta E_{g,Ge}(grade) / kT} \right] \quad (1.3)$$

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \left[1 - e^{-\Delta E_{g,Ge}(grade) / kT} \right] \right\} \quad (1.4)$$

Eq. 1.2 shows that the improvement in β is linearly proportional to the Ge-induced bandgap grading factor, $\Delta E_{g,Ge}(grade)$ and exponentially dependent to the Ge-induced band offset at the emitter-base boundary, $\Delta E_{g,Ge}(0)$. From Eqs. 1.3 and 1.4, the improvements in V_A and τ_b are dependent only upon $\Delta E_{g,Ge}(grade)$. Therefore, a box profile achieves maximum β improvement but no improvement in V_A or τ_b as there is no Ge grading across the neutral base. However, the Ge grading factor is greatest for a ramp or triangular profile so devices incorporating these types of profiles will benefit from improved V_A and τ_b , but due to the lower Ge content at the emitter-base boundary β will be reduced. Hybrid profiles such as Ge trapezoids provide improved gain while maintaining good dynamic response [14]. Both Ge profiles in Fig. 4 exhibit a steady decrease in Ge content near the collector-base junction, called a Ge retrograde. This Ge retrograde helps mitigate high-injection effects that may degrade device performance, most notably Kirk effect and heterojunction barrier effects (HBE). Fig. 5 shows the theoretical calculations for the current gain, early

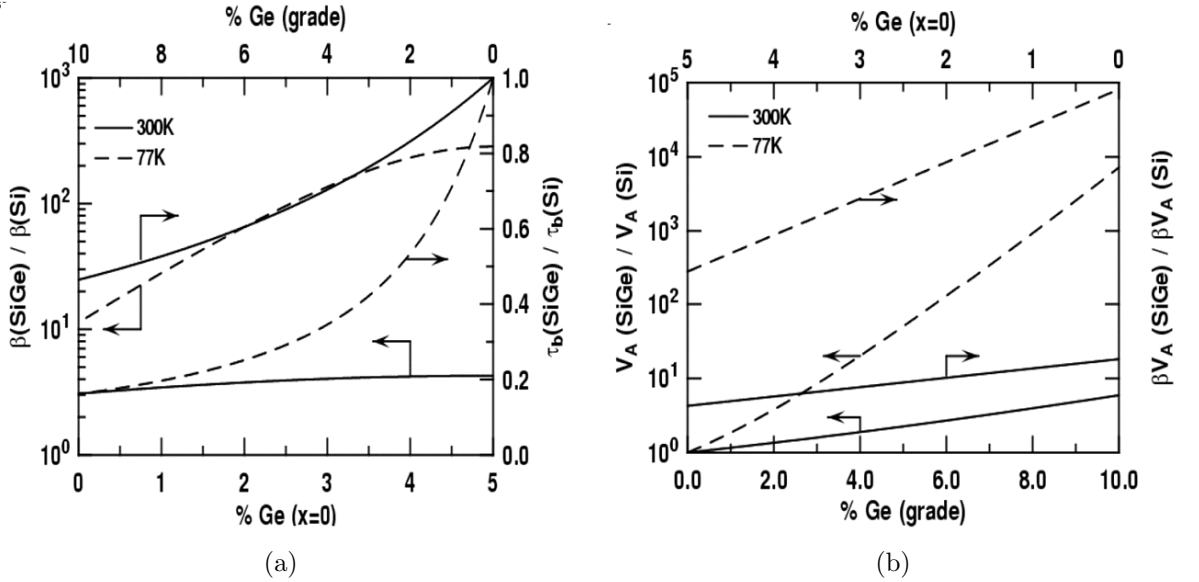


Figure 5: Theoretical calculations of a) the current gain ratio and transit time ratio; b) the Early voltage and current gain - Early voltage product ratio as a function of Ge profile shape (after [14]).

voltage, and base transit time ratios as a function of Ge profile shape and confirms that a box Ge profile ($\%Ge(x = 0) = 5$ and $\%Ge(grade) = 0$) exhibits maximum β while a triangular Ge profile ($\%Ge(x = 0) = 0$ and $\%Ge(grade) = 10$) exhibits maximum V_A and minimum τ_b .

Eqs 1.2 - 1.4 suggest a very strong dependence between transistor performance and ambient temperature—this effect is also seen in Fig. 1.2. These cryogenic effects will be covered in the next section.

1.3 Cryogenic Operation of Silicon-Germanium HBTs

In the previous section, the shape of the Ge profile was shown as a potential tool to control the performance parameters of a SiGe HBT. By revisiting Eqs 1.2 - 1.4 and paying close attention to the kT terms, we see that these performance metrics are also inversely proportional to temperature. Therefore, the performance of a SiGe HBT should improve at lower ambient temperatures. By comparing the 300 K and 77 K performance curves in Fig. 1.2, a dramatic increase in β and V_A and a decrease in τ_b , i.e. higher unity-gain cutoff frequency (f_T) are observed.

Empirical measurements are needed to corroborate these theoretical observations, so second generation (IBM 7WL) SiGe HBTs were *dc* and *ac* characterized at cryogenic temperatures. For *dc* characterization, a semiconductor die containing npn HBT test structures was packaged onto a 28 pin ceramic DIP, wirebonded, and placed inside a closed-cycle cryostat measurement station where *dc* characteristics were measured at regular temperature steps down to 77 K. Fig. 6 shows the forward Gummel characteristics for $0.24 \times 1 \mu m^2$ npn SiGe HBT at 300 K and 90 K. The large V_{BE} shift (approximately 500 mV) is attributed to the increase in the emitter-base built-in voltage with decreasing temperature. A larger V_{BE} is required before the electrons in the conduction band can overcome this increased potential barrier. The transconductance, $g_m = \partial I_C / \partial V_{BE}$, is improved at low temperatures, resulting in an

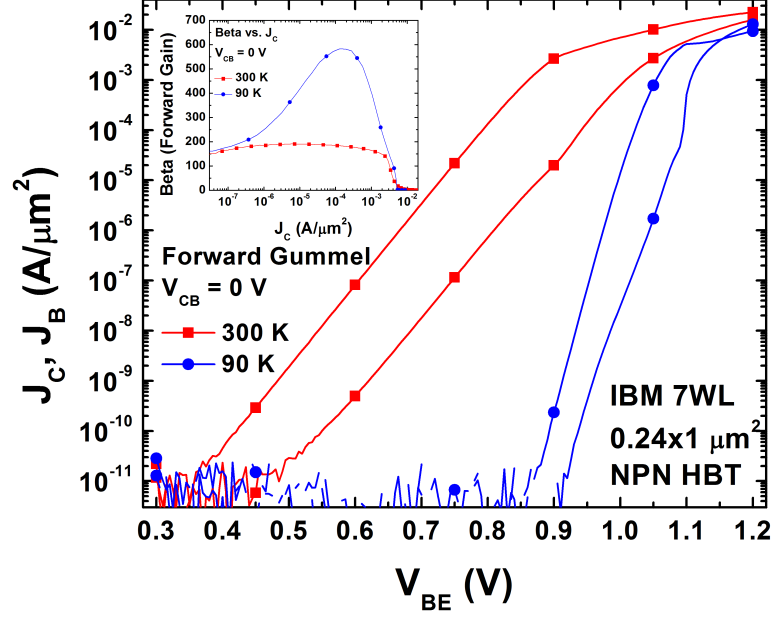


Figure 6: Forward Gummel characteristics for a $0.24 \times 1 \mu m^2$ IBM 7WL SiGe HBT at 300 K and 90 K.

increase in slope for the collector (output) current. The inset figure is current gain (β) vs. collector current density (J_C). At room temperature, β remains relatively flat until high-injection effects (Kirk effect and HBE) quickly degrade β . However at cryogenic temperatures, increased base leakages at low J_C and high-injection effects limit the current range of improved β , resulting in the blue bell-shaped curve. β vs. J_C curves at other temperatures are shown on the inset plot in Fig. 7. From 150 K to 100 K, there is a sharp increase in low-injection base leakage resulting in a sharp drop in β at low J_C . Peak β follows the exponential inverse temperature dependency from Eq. 1.2, showing that the theoretical calculations from the previous section are valid.

Cryogenic *ac* measurements were made using an on-wafer open-cycle liquid-helium cryogenic probe system capable of dc to 40 GHz operation from 350 K to 5 K [34]. An Agilent 4156 Semiconductor Parameter Analyzer (for device biasing) and Agilent E8361C Vector Network Analyzer were used for *ac* measurements. Standard calibration and de-embedding techniques were used at each measurement temperature.

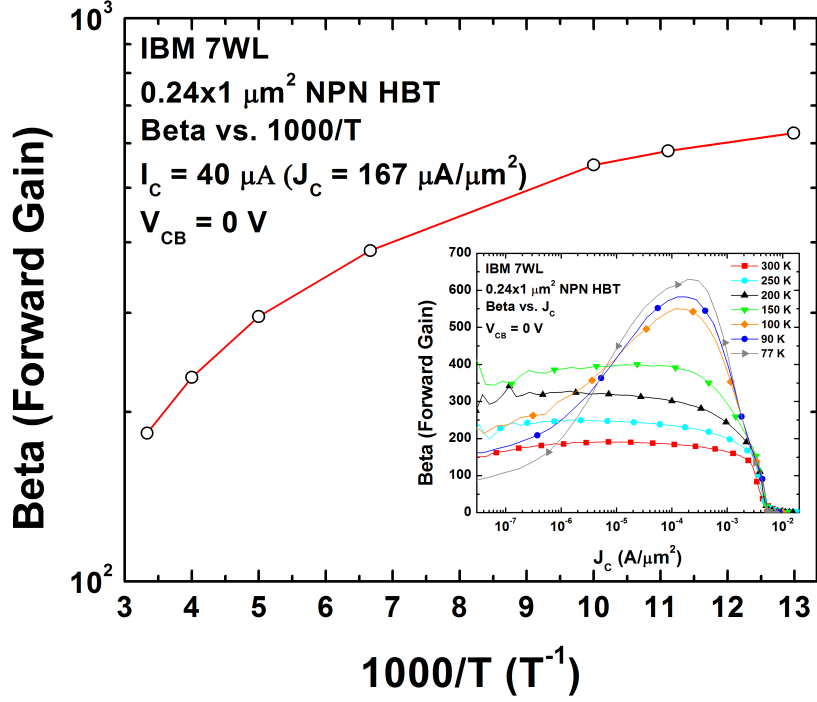


Figure 7: Forward current gain vs $1000/T$ for a $0.24 \times 1 \mu\text{m}^2$ IBM 7WL SiGe HBT from 300 K to 77 K.

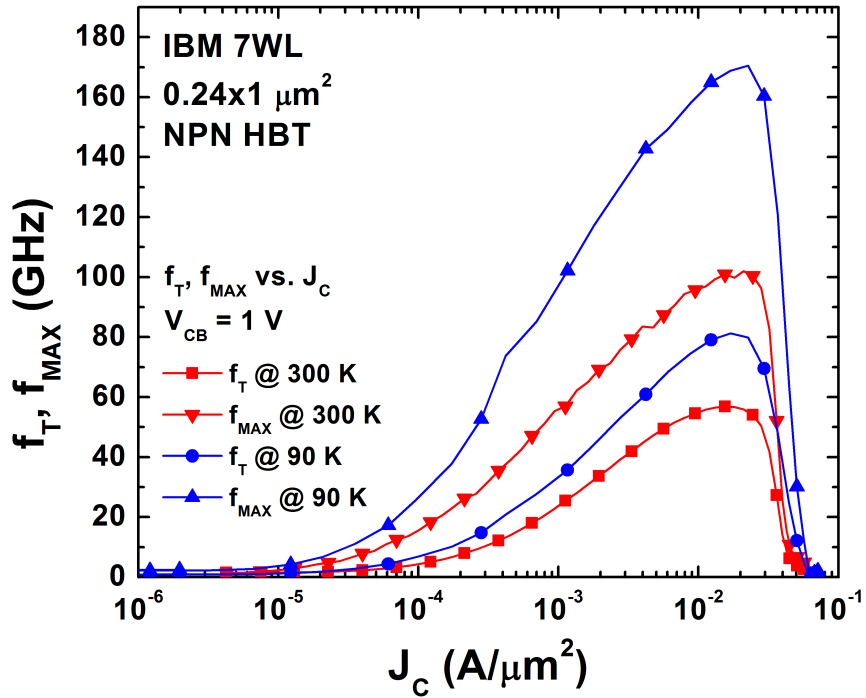


Figure 8: Unity current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) for a $0.24 \times 1 \mu\text{m}^2$ IBM 7WL SiGe HBT at 300 K to 90 K.

Fig. 8 shows the unity current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) at 300 K and 90 K. Knowing that $f_{MAX} \propto f_T \propto 1/\tau_b$ and τ_b diminishes at reduced temperatures, f_T and f_{MAX} should improve at cryogenic temperatures. The measured *ac* results in Fig. 8 confirms these assumptions; f_T and f_{MAX} increased by 43% and 67% respectively.

1.4 Summary

There is a growing need in the space electronics industry for semiconductor technologies that can operate within wide-temperature and radiation intense environments. Current bulk silicon technologies require WEBs to provide protection from thermal losses and radiation, but the increased payload incurred from these enclosures can be prohibitively expensive. SiGe BiCMOS technology combines the performance of a III-V technology with the yield and cost savings of bulk silicon. SiGe HBTs are an excellent transistor technology for cryogenic applications due to their excellent low temperature behavior, but in order for SiGe to qualify as a wide-temperature, radiation-tolerant platform, its high temperature performance and radiation response must be characterized.

CHAPTER II

INTRODUCTION TO RADIATION EFFECTS

This chapter serves an overview on the radiation threat faced by satellite and spacecraft electronics. The major sources of ionizing radiation and their effects in semiconductor materials and devices are covered, providing the background for technical discussion for future chapters.

2.1 Natural Space Radiation Environment

2.1.1 Particle Sources

Planetary satellites and deep-space spacecrafts encounter a myriad of high-energy particles, the origin of which can fall into three general categories: 1) the background flux of ions originating from outside our solar system, known as Galactic Cosmic Rays (GCRs); 2) particles emitted from the Sun during solar events; and 3) particles that are trapped by the Earth's magnetic field into discrete bands known as the Van Allen Belts. This radiation environment can be very dynamic, with solar activity

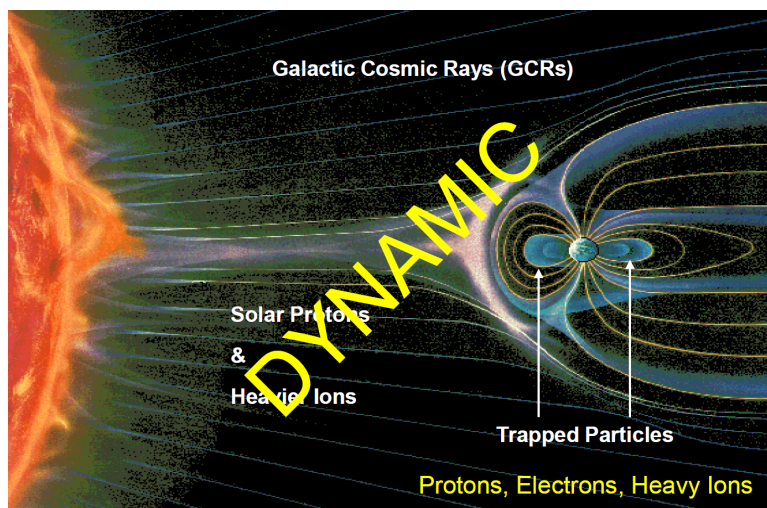


Figure 9: Artist's depiction of the natural space environment local to earth (after [7]).

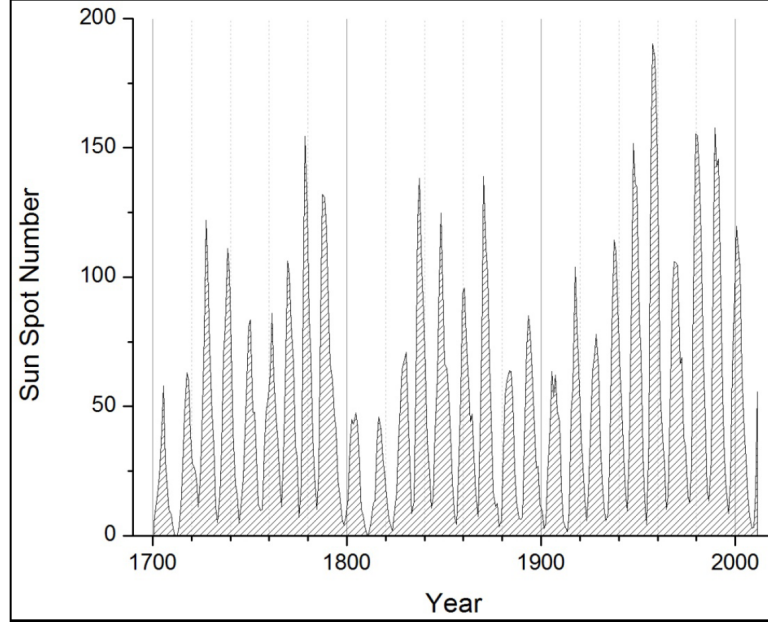


Figure 10: Solar activity (sun spot count) vs. time, highlighting the cyclical (11-year period) pattern (after [57]).

modulating GCR fluxes and the frequency of solar events. An artist’s depiction of the natural space environment local to the Earth is shown in Fig. 9.

Since the Sun is both a producer and modulator of high-energy particles, it would seem pertinent to observe and model solar activity. The earliest record of sunspot observation dates back to 4th century BCE by Chinese astronomers Shi Shen and Gan De [51]. As shown in Fig. 10, solar activity follows a cyclical pattern with a period of approximately 11 years. During each cycle, there is approximately seven years of elevated solar activity, called solar maximum, and four years where the solar activity levels are low, called solar minimum. The magnetic polarity of the Sun reverses every 11-year period, so there is a larger 22-year cycle as well. Solar activity levels are generally unaffected by the magnetic field reversal, but GCR flux models do show a correlation between the Sun’s magnetic field polarity and GCR flux [4].

Table 1: Characteristics of Galactic Cosmic Rays [7]).

Hadron Composition	Energies	Flux	Radiation Effects	Metric
87% protons 12% alphas 1% heavier ions	Up to 10^{11} GeV	1 to $10 \text{ cm}^{-2}\text{s}^{-1}$	SEE	LET

2.1.2 Galactic Cosmic Rays

GCRs originate from outside our solar system, most likely accelerated in the blast waves of supernova remnants. The particles that make up GCRs, i.e. protons, electrons, and ionized atomic nuclei, are accelerated up to a certain maximum energy from the magnetic fields within these stellar remnants. Astronomers have observed cosmic rays with energies above this maximum value and have surmised their origination to sources outside of our galaxy, e.g. active galactic nuclei [1]. These ultra-high-energy cosmic rays (UHECRs) or extreme-energy cosmic rays (EECRs) are very rare and are not considered a part of the galactic background flux. It can be seen from Fig. 11 that the abundance of GCR drops off rapidly for ions heavier than iron. One can logically infer this observation from the fusion processes within dying stars. As a massive star ($M_{STAR} > 10$ solar masses) begins to deplete itself of its hydrogen fuel source, it will continue to fuse heavier elements up until a core of iron is formed. The fusion of iron is an endothermic process, causing the star to gravitationally collapse and go supernova. Elements that are heavier than iron are fused in the high energy densities within these supernovae. Approximately one percent of stars have the mass necessary to generate supernovae, so it not a surprise that these elements constitute a small fraction of GCRs. Some general characteristics of GCRs are shown in Table 1.

GCRs with energies less than 10 GeV/amu of kinetic energy are modulated by the Sun's magnetic field and solar wind. As shown in Fig. 12, most constituents of GCRs have energies below this threshold. The greatest suppression of GCRs occurs

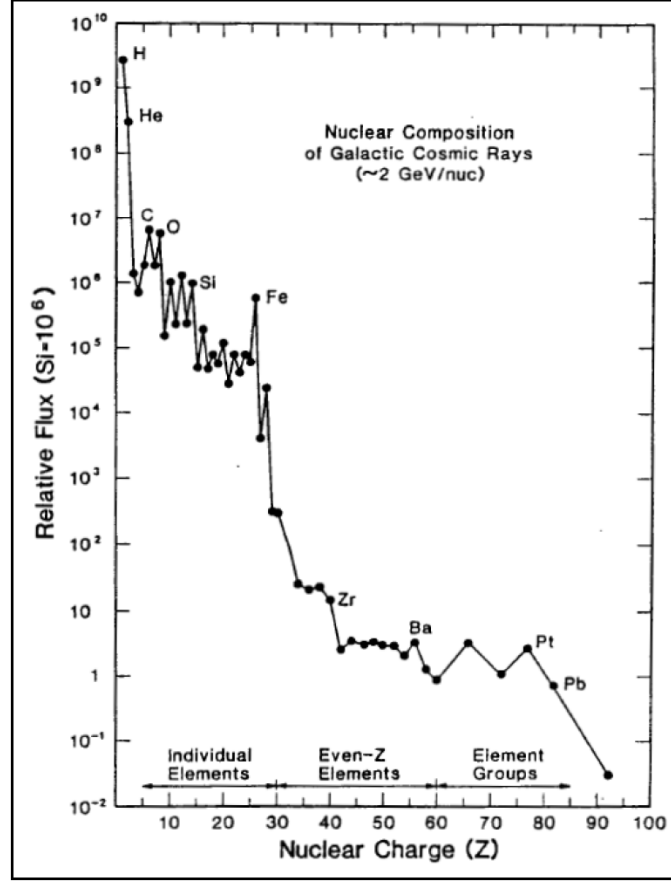


Figure 11: GCR relative abundances by nuclear charge (Z), normalized to $\text{Si} = 1000$ for $Z < 28$ and $\text{Si} = 10^6$ for $Z > 29$ (after [7], [46]).

during solar maximum, when solar wind fluxes are at their maximum. The Sun's modulative effects are graphically shown in Fig. 13. Because GCRs can travel at extremely high energies, they can produce Single Event Effects (SEE) in orbital and deep-space electronics. It should be noted that several GCR models are publically available. GCR flux models have been published by Moscow State University [52], [53] and NASA [4], [5], and an ISO standard exists (ISO 15390:2004) based on the MSU models.

2.1.3 Solar Energetic Particles

Solar energetic particles (SEP) are produced by two types of solar events: solar flares and coronal mass ejections (CMEs). Solar flares and CMEs accelerate particles in

a distinct manner. As described in [Xapsos2006short], solar flares result when the localized energy storage in the coronal magnetic field becomes too great and causes a burst of energy to be released. They tend to be electron rich, last for hours, and have an unusually high helium-3 (^3He) content relative to helium-4 (^4He). A CME, on the other hand, is a large eruption of plasma (a gas of free ions and electrons) that drives a shock wave outward and accelerates particles. CMEs tend to be proton rich, last for days, and have small ^3He content relative to ^4He . The total mass of ejected plasma in a CME is generally 10^{15} to 10^{17} grams. Ejected plasma from CMEs travel at relatively slow speeds, with an average speed of around 400 km/s. Particles ejected from CMEs can take anywhere from 12 hours to a few days to reach the Earth. It should be noted that CMEs are responsible for major disturbances in interplanetary space as well as major geomagnetic disturbances on Earth. Some general characteristics of CMEs are shown in Table 2.

While CMEs are composed of a cocktail of different particles, protons account for about 96% of the total composition. These low and high-energy protons can cause permanent damage in the form of Displacement Damage Dose (DDD) and

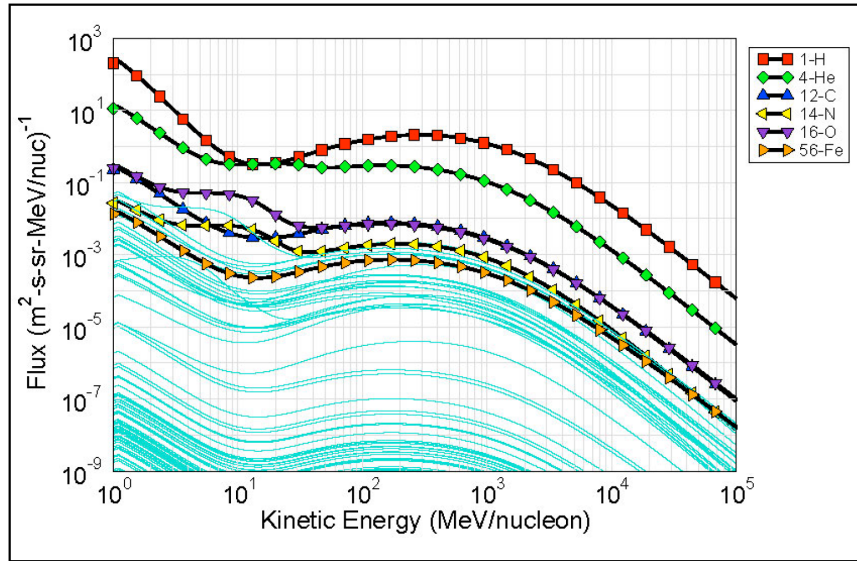


Figure 12: Differential flux of GCR as predicted by the Moscow State University model implemented in the CREME96 tools [52], [82] (after [7]).

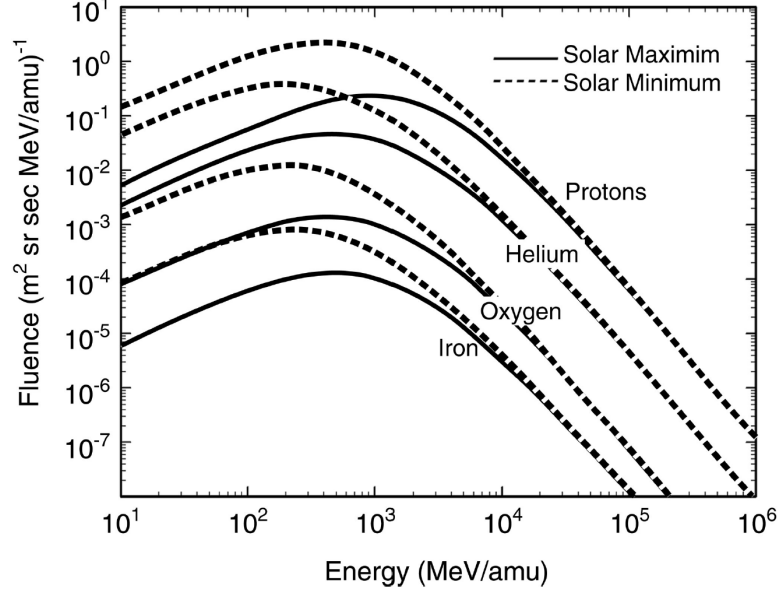


Figure 13: GCR energy spectra for protons, helium, oxygen and iron during solar maximum and solar minimum (after [4]).

Table 2: Characteristics of CMEs (after [7]).

Hadron Composition	Energies	Integral Fluence (>10 MeV/nuc)	Peak Flux (>10 MeV/nuc)	Radiation Effects
96.4% protons 3.5% alphas ~0.1% heavier ions	Up to ~GeV/nuc	$>10^9 \text{ cm}^{-2}$	$>10^5 \text{ cm}^{-2}\text{s}^{-1}$	TID DDD SEE

Total Ionizing Dose (TID). While heavy ions make up a small percentage of ejected solar particles, their effect on spacecraft cannot be overlooked. Heavy ions, as well as protons and alpha particles from solar particle events, can cause transient and permanent SEE. Fig. 14 and Fig. 15 illustrate the periodic dependence of low energy (>0.88 MeV) and high energy (>92.5 MeV) protons respectively. Attention should be focused on the statistical nature of solar particle events. Due to their stochastic nature, modeling solar particle events can be a difficult process. Luckily several models have been created, including the JPL91 [23] and ESP [86], [87] models. An additional model, known as the PSYCHIC model has been developed as an extension

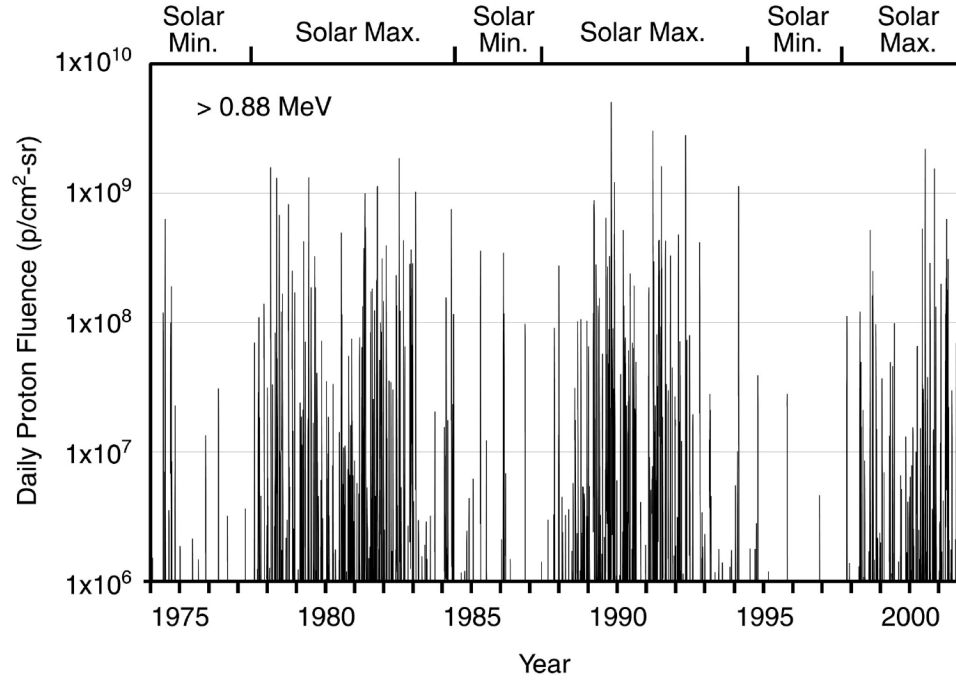


Figure 14: Daily fluences of > 0.88 MeV protons due to solar particle events between approximately 1974 and 2002 (after [7]).

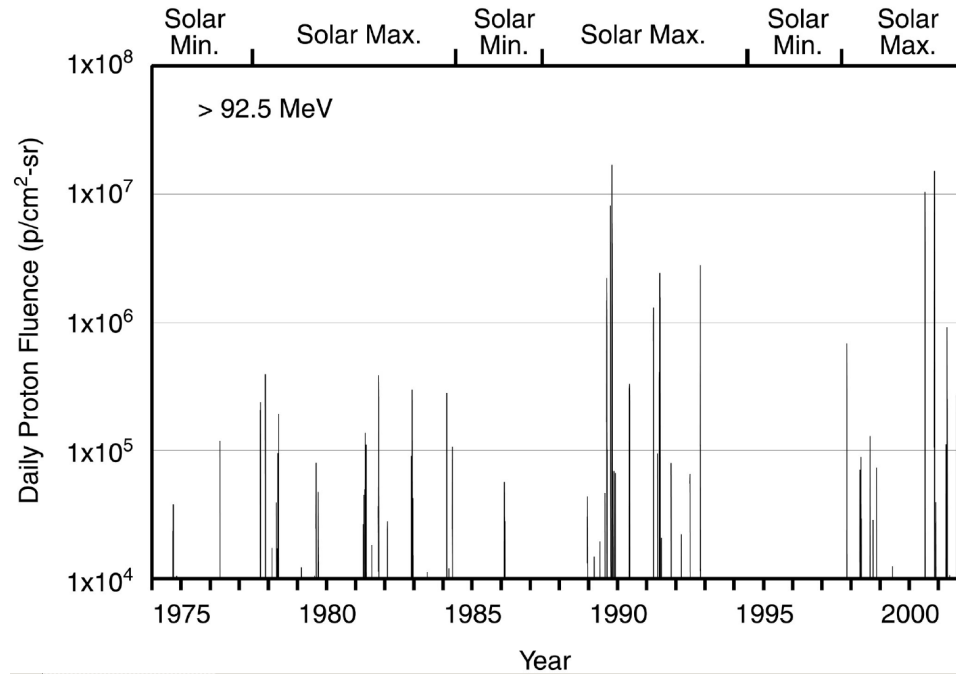


Figure 15: Daily fluences of > 92.5 MeV protons due to solar particle events between approximately 1974 and 2002 (after [7]).

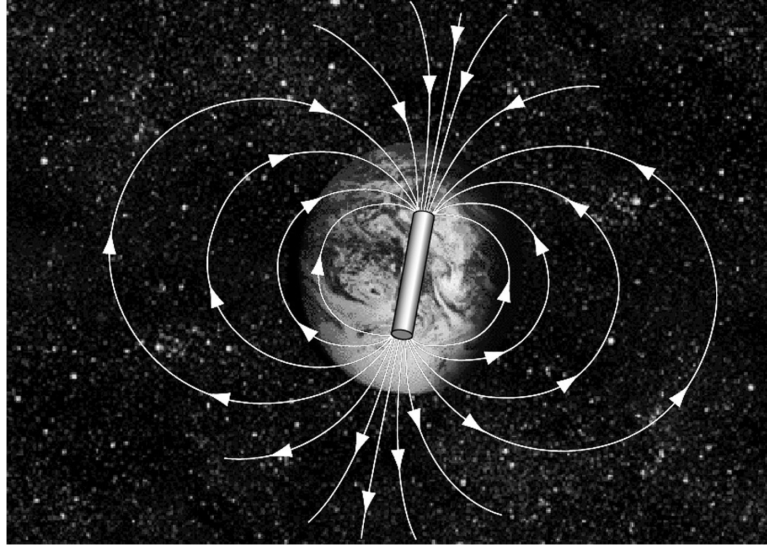


Figure 16: The internal magnetic field of the Earth is approximately a dipole field (after [84]).

of the ESP model [85].

2.1.4 The Earth's Trapped Radiation Environment

The Earth's magnetosphere consists of both an external and internal magnetic field. The external field is the result of the ionized gas particles that comprise the solar wind. Earth's geomagnetic field originates from electrical currents present in the liquid outer core. The geomagnetic field can be approximated as a dipole magnet up to altitudes of about 5 Earth radii. This dipole approximation is visualized in Fig. 16. This dipole field is tilted about 11° from the Earth's north-south axis and displaced by more than 500 km from the Earth's geocenter [15]. The standard method to describe the Earth's dipole field uses McIlwain's (B, L) coordinates, where L represents the distance from the origin in the direction of the magnetic equator in Earth radii, and B is the magnetic field strength [40]. For reference, the International Union of Geodesy and Geophysics (IUGG) defines the mean Earth radius as 6371 km [49]. The magnetic field strength is at a minimum at the magnetic equator and at a maximum at the magnetic poles. Protons and electrons can become trapped along these magnetic

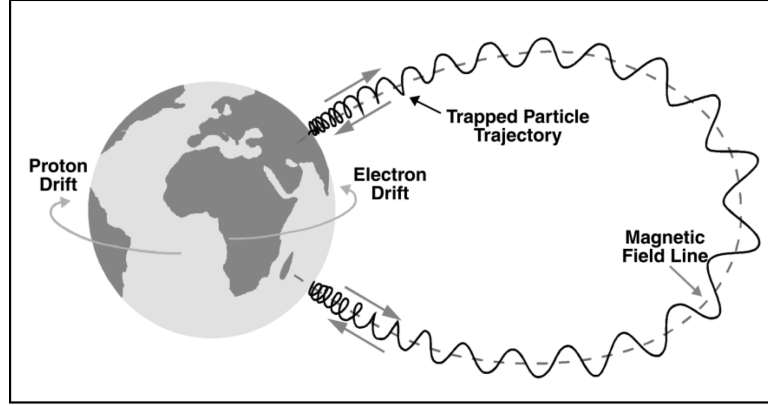


Figure 17: Motion of a charged trapped particle in the Earth’s magnetic field (after [84], [72], [74]).

field lines called the Van Allen Belts. These charged particles drift around the Earth while being dragged in the longitudinal direction. The resulting toroidal surfaces traced out by these particles are called drift shells. Charged particle motion along the Van Allen Belts is shown in Fig. 17. Trapped particles spiral around and move along the magnetic field line. When the particle approaches the polar regions, the magnetic field strength increases, causing the spiral to tighten. The magnetic field continues to increase until there is sufficient force to send the particle in the reverse direction. The points where particles reflect to and from are called “mirror points” or “conjugate mirror points.” As shown in Fig. 17, protons and electrons longitudinally drift in opposite directions.

Fig. 18 shows the distribution of charged particles in the Earth’s magnetosphere. As described in [84] and [57], trapped protons have energies up to 100s of MeV, fluxes up to $10^5 \text{ cm}^{-2}\text{s}^{-1}$ for energies $>10 \text{ MeV}$, and exist in L -shells between 1.15 and 10, though high-energy protons ($>10 \text{ MeV}$) only exist below altitudes of about 20,000 km. Close to the inner edge, proton fluxes are modulated by the atmospheric density. At solar maximum, these proton fluxes can decrease by a factor of 2 to 3 due to atmospheric expansion and various scattering processes. Various trapped proton models have been developed and are available to the general public, including

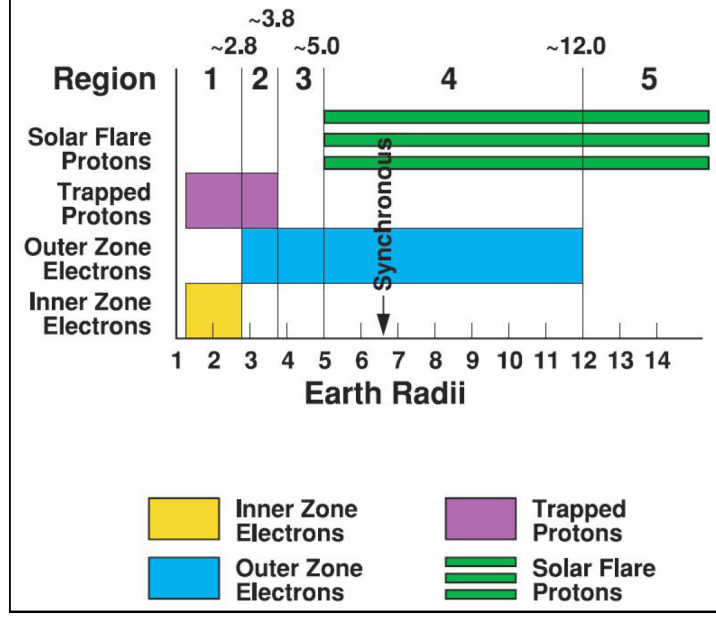


Figure 18: The distribution of charged particles (protons and electrons) in the Earth’s magnetosphere (after [74]).

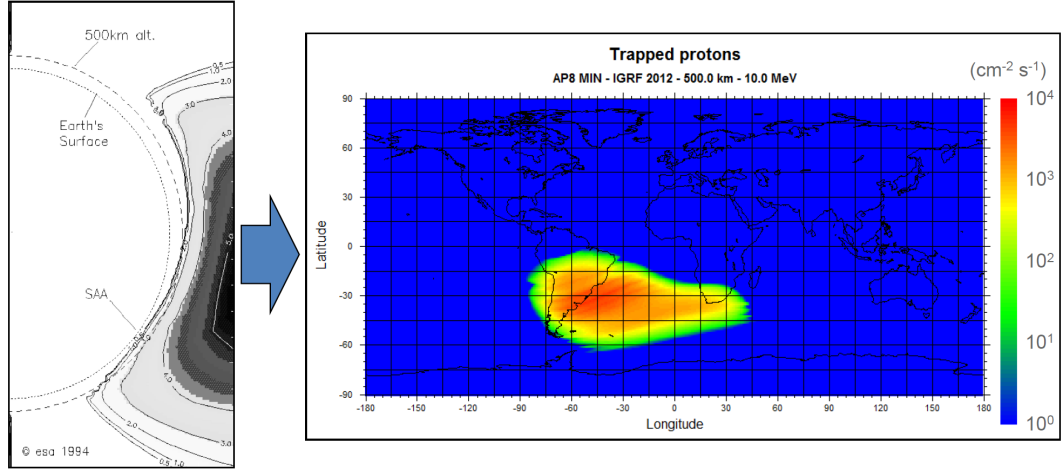


Figure 19: Cross-sectional view and OMERE trapped proton (10 MeV AP-8 protons at 500 km altitude) plot highlighting the ”South Atlantic Anomaly” (after [15], [57]).

the AP-8 [67], CRRESPRO [44], and a more recent model based on SAMPEX/PET data [28].

A unique feature of the trapped proton environment is a region known as the “South Atlantic Anomaly” (SAA). Fig. 19 shows a cross-sectional view (cut through the Earth at meridian 325°) and flux plot highlighting the SAA. Located off the coast

of Brazil, the SAA is a distinct area on the Earth where part of the inner trapped proton belt is at a lower altitude than normal. This phenomenon is caused by the tilt and displacement of the geomagnetic field with respect to Earth’s axis of rotation. The SAA primarily affects satellites and spacecraft with orbits below 1000 km.

The trapped electron environment is unique due to the existence of two distinct zones: an inner belt with L values between 1 and 2.8 and an outer shell with L values between 2.8 and 10. Electrons in the inner zone have energies up to 4.5 MeV and fluxes that peak around $10^6 \text{ cm}^{-2}\text{s}^{-1}$ (for >1 MeV electrons) near $L = 1.5$. Inner zone electron fluxes are generally stable but can gradually increase by a factor of 2 or 3 at solar maximum. Outer zone electrons have energies that peak at about 10 MeV with peak fluxes between $L = 4.0$ and $L = 4.5$. The outer zone is very dynamic with day-to-day fluxes varying by several orders of magnitude. A long-term average value of flux for >1 MeV electrons is approximately $3 \times 10^6 \text{ cm}^{-2}\text{s}^{-1}$. Trapped electrons are distributed across the inner zone and outer zones, but there is a region between the high intensity zones where electron flux is at a minimum called the slot region. Due to the dynamic nature of the outer zone, the location of the slot region is dynamic but its location is usually between $L = 2$ and $L = 3$. There are several available trapped electron models, including AE-8 [83], CRRESELE [9], and IGE-2006/POLE [8], [63], [70]. It should be noted that all trapped proton and electron models introduced are specific to the Earth trapped particle environment. References and models for other trapped environments, including the Jovian system [25] are also available.

Standalone radiation effects software and online toolsets are available for characterizing Earth’s trapped particle environment. OMERE, developed by TRAD, Tests and Radiations, is a freeware dedicated to space environment and radiation effects on electronic devices [80]. OMERE combines GCR, SEP, and trapped particle models and radiation effects analyses (DDD, TID, SEE) to provide an all-in-one interface for

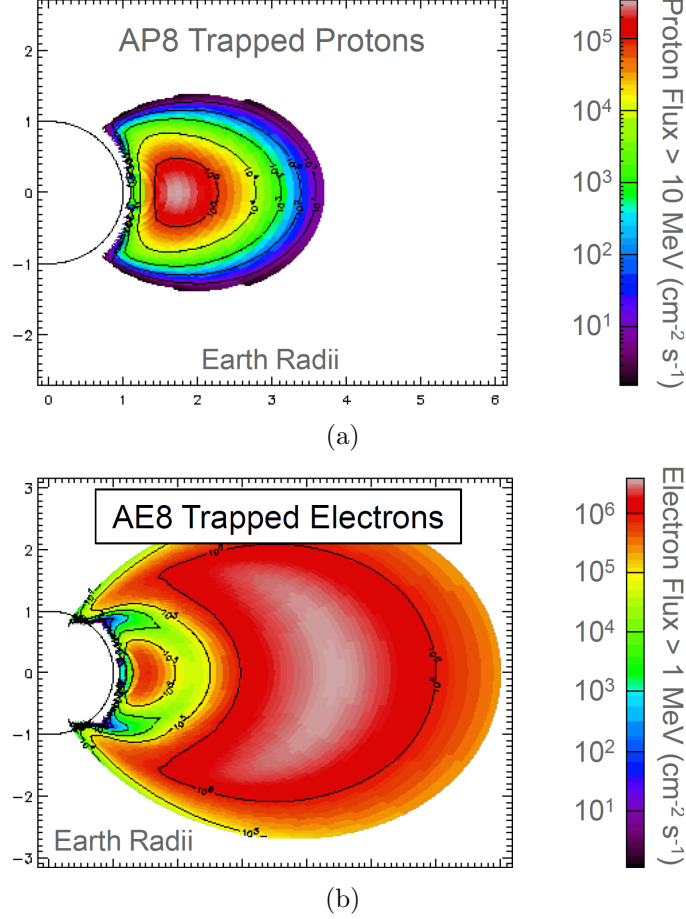


Figure 20: Trapped particle flux populations for (a) protons with energies >10 MeV and (b) electrons with energies >1 MeV (after [57]).

investigating potential reliability issues for Earth orbiting spacecraft. The topographical map highlighting the SAA in Fig. 19 was generated using OMERE. The Space Environment Information System (SPENVIS) provides similar functionality but uses an online interface for analyzing radiation effects [28], [21]. Fig. 20 shows the trapped proton and trapped electron flux populations which were generated using the SPENVIS toolsets. The inner and outer trapped electrons zones as well as the slot region ($L \approx 2$) are visible.

2.1.5 Radiation Environment Threats

Table 3 lists the major constituents of the ambient radiation environment for several classes of orbital trajectories. The difference between equatorial and polar low Earth

Table 3: Radiation Threat Summary (after [57], K.A. LaBel, NASA/GSFC).

Name	Trapped Electrons	Trapped Protons	Solar Particles	Cosmic Rays
LEO Low-Inclination	Moderate	Yes	No	Moderate
LEO Polar	Moderate	Yes	Yes	Yes
MEO	Severe	Severe	Yes	Yes
HEO	Yes	Yes	Yes	Yes
GEO	Severe	No	Yes	Yes
Interplanetary	During phasing; other planets	During phasing; other planets	Yes	Yes

orbits (LEO) is attributed to the enhanced displacement of the Van Allen Belts at the Earth’s equator. Medium Earth orbits (MEO) encompass the maximum flux regions of the proton and inner electron belts, so spacecraft at these orbits are very susceptible to proton and electron damage. Geosynchronous orbits (GEO) and high Earth orbits (HEO) exist within the outer electron belt, but due to the dynamic nature of this region, it can be hard to predict TID/SEE at these orbits. LEO polar, MEO, GEO, and HEO are susceptible to SEPs and GCRs, while LEO with low inclination benefit from the protection of the Earth’s magnetic field. Interplanetary orbits are susceptible to other planets’ trapped radiation environments in addition to SEPs and GCRs.

2.2 Energy Deposition in Materials and its Effects

The mechanisms by which different types of radiation interact with matter vary, but at the basic level, high-energy particles and photons deposit energy while passing through matter. For semiconductor materials, this deposited energy manifests itself as electron-hole pairs and atomic (lattice) dislocations. The radiation type, energy, and length of exposure can have profound impact on the measured results. The following subsections will focus on electron-hole pair generation as they are the source of TID and SEE. While certainly relevant to radiation effects, DDD will not be covered in the

subsequent sections. There are excellent background references covering the subject of DDD, including [29], [62], [73]. The following sections will consist of broad overviews of the mechanisms of energy deposition in matter and their effects in electronic devices (TID, SEE). [66] and [64] contain more in-depth investigations as well as references for additional reading.

Electrons, protons, and heavy-ions deposit energy into materials through two processes: direct and indirect ionization. As a charged particle passes through matter, it interacts with the field of electrons through Coulombic forces. Most interactions involve relatively small amounts of energy loss (usually a few eV) by the moving charged particle, but enough energy is imparted to generate electron-hole pairs. There are many thousands of these “direct” ionization events along the path of a charged particle. Occasionally, a larger energy transfer may occur between the charged particle and an electron, producing an energetic secondary electron often referred to as a delta ray (δ -ray). These δ -rays will then go on to produce multiple ionization events. This two-step ionization process is called indirect ionization.

A popular way to quantify direct ionization effects in matter is the linear energy transfer, or LET. LET describes the amount of energy an ionizing particle has lost per unit path length through a specified material. LET has units of Energy-Length²/Mass, commonly expressed as MeV-cm²/mg. LET is derived by normalizing electronic stopping power, denoted as S , by the specified material density (see Eq. 2.1).

$$LET = \frac{S}{\rho} = \frac{-dE/dx}{\rho} = \frac{MeV/cm}{mg/cm^3} = \frac{MeVcm^2}{mg} \quad (2.1)$$

Active regions of devices, e.g. the depleted channel between source and drain in a FET or the vertical bipolar region of a HBT, are often modeled as a rectangular parallelepiped (RPP). These RPP models are commonly used in SEE predictions for electronics in radiation-intensive environments. A modified LET term, called effective LET, takes into account the incidence angle of an ionized particle [60]. Effective LET

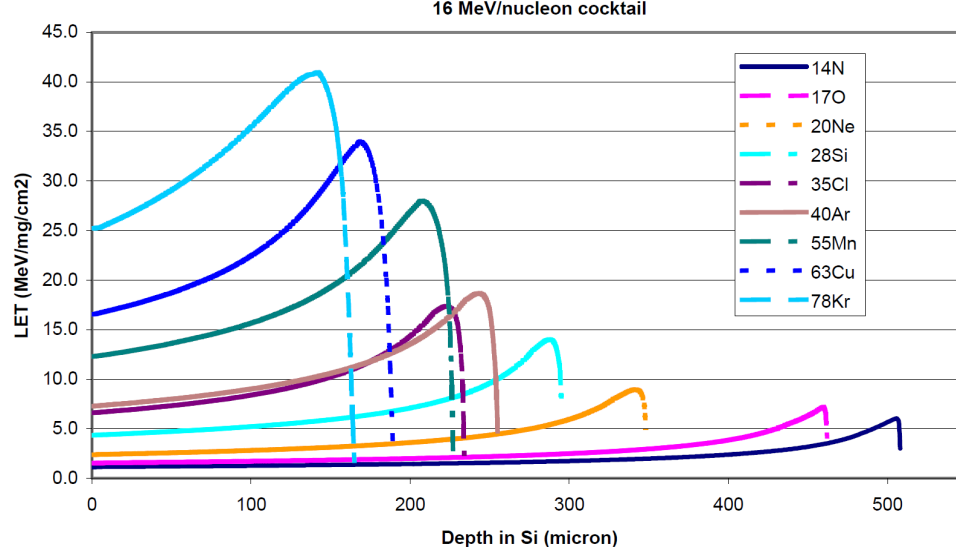


Figure 21: Depth in silicon (μm) vs. LET ($\text{MeV}\cdot\text{cm}^2/\text{mg}$) for various heavy-ions (after [42]).

is the exact same as LET except that it is scaled by $1/\cos(\theta)$, where θ is the incident angle of the ion. As the incidence angle is increased toward 90° , the effective LET increases because the path length through the assumed sensitive volume (RPP) gets longer.

Fig. 21 shows the depth in silicon (μm) versus LET for a variety of heavy-ion particles. High-energy particles are slowed down as they traverse through matter and deposit energy. The rate of energy deposition increases as the particle slows down until it reaches a maximum known as the Bragg peak. The particle comes to a halt shortly after the Bragg peak, resulting in a sharp drop in LET. If the energy per nucleon for all ions is fixed, heavier ions will traverse less material before halting due to greater interactions with the surrounding material. This can cause problems for technologies with large back end of the lines (BEOLs) because the particles will exhaust most of their energy before striking the sensitive volume. Luckily, tools have been developed to help predict the energy losses for high-energy particles as they propagate through matter. SRIM/TIRM, short for Stopping and Range of Ions in Matter/Transport of Ions in Matter, are a group of free programs which calculate

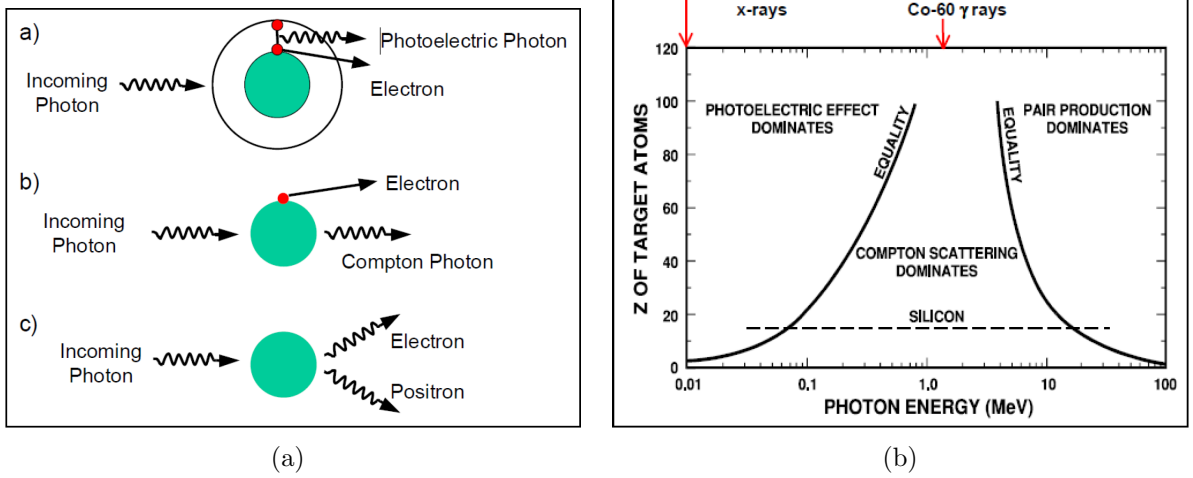


Figure 22: a) The three photon interaction mechanisms [22]; after J. R. Schwank, *et al.* b) Dominant photon interaction mechanism as a function of photon energy and the target atom's nuclear charge [41]; after J. R. Schwank, *et al.*

the transport properties of ions through matter [89]. SRIM/TRIM can generate semiconductor/insulator/metal stacks and predict LET energies at a specified depth.

Photons deposit energy much like electrons, protons, and heavy-ions, but the photons themselves cause little damage. There are three photon interaction mechanisms: the photoelectric effect, Compton scattering, and pair production which are illustrated in Fig. 22a. All three interaction mechanisms result in the generation of an energetic secondary electron (δ -ray) that in turn creates electron-hole pairs through ionization events. In the photoelectric effect, a photon is completely absorbed by an atom, exciting an inner shell atomic electron to a high enough energy state that it is emitted from the atom. An outer shell electron then falls in to take the place of the ejected electron (photoelectron), releasing its excess energy in the form of a photoelectric photon. Compton scattering is a type of inelastic scattering that X-rays and γ -rays undergo in matter. Compton scattering is named after Arthur Holly Compton who won the 1927 Nobel Prize in Physics for its discovery. An unexplainable phenomenon occurred when high-energy photons (X-rays) interacted with atoms. These photons were scattered through an angle θ and emerged at a different wavelength

related to θ . Classical electromagnetism predicted the wavelength of scattered X-rays to remain unchanged, but experimental results revealed the scattered rays had longer wavelengths (lower energies). In Compton scattering, part of the energy of the incoming photon is transferred to a scattering electron, which recoils and is ejected from the atom. The rest of the energy is taken by the scattered photon, resulting in a wavelength shift. Pair production occurs when a high-energy photon interacts with the nucleus of an atom. The result is the creation of an electron and its anti-particle, a positron. The energy of the incoming photon is converted to mass through Einstein's equation, $E = mc^2$, where E is the photon energy, m is the sum of the electron and positron rest masses (2x electron rest mass), and c is the speed of light. For pair production to occur the photon must have enough energy to create the rest masses of the electron and positron. The rest mass of an electron (or positron) is about 9.11×10^{-31} kg, which translates to approximately 0.511 MeV/ c^2 . Fig.22b indicates which interaction process dominates with respect to the nuclear charge of the target atom and photon energy. The dashed line at $Z = 14$ represents silicon and shows that lower energy photons, e.g. 10-keV X-rays from an ARACOR X-ray irradiator, usually produce electrons via the photoelectric effect but γ -rays from ^{60}Co (1.25 MeV) will produce electrons via Compton scattering.

The use of X-rays and γ -rays for accelerated TID testing has several advantages over particle beam experiments. Photon-based testing facilities do not require the particle accelerators needed to accelerate particles with mass to high energies. Particle accelerators are complex systems that are expensive to install and costly to upkeep. Fig. 23 shows the fractional hole yield versus electric field for a variety of particles spanning a wide variety of LETs in SiO_2 . From Fig. 23, ^{60}Co (γ -ray) and 10-keV X-rays have high fractional hole yields, reducing exposure times and experiment costs for the end user. A key advantage between photon and proton/neutron beam facilities is the unwanted activation of devices under test (DUTs) and other

testing equipment. Proton or neutron activation is a process where atoms pick up free protons or neutrons and enter excited states. These excited atoms are unstable and undergo radioactive decay, which can take several days to weeks before dropping below background radiation levels. Metals, such as aluminum or copper, are very susceptible to proton activation. Therefore, test packages, e.g. dual in-line packages (DIPs) and testing boards, e.g. printed circuit boards (PCBs), may become unsafe to handle if exposed to multi-Mrad proton doses. X-ray and γ -ray testing is not without its own disadvantages. TID experienced by spacecraft is primarily a result of long-term exposure to trapped and solar protons and/or electrons, so photon-based TID testing may not accurately predict how electronics degrade over time in the natural space environment (photons do not cause DDD).

2.2.1 Total Ionizing Dose

TID is a measure of the absorbed energy from ionizing radiation in a given material. It should not be confused with the concept of equivalent, effective, or committed dose, which represent the stochastic biological effects of ionizing radiation and are

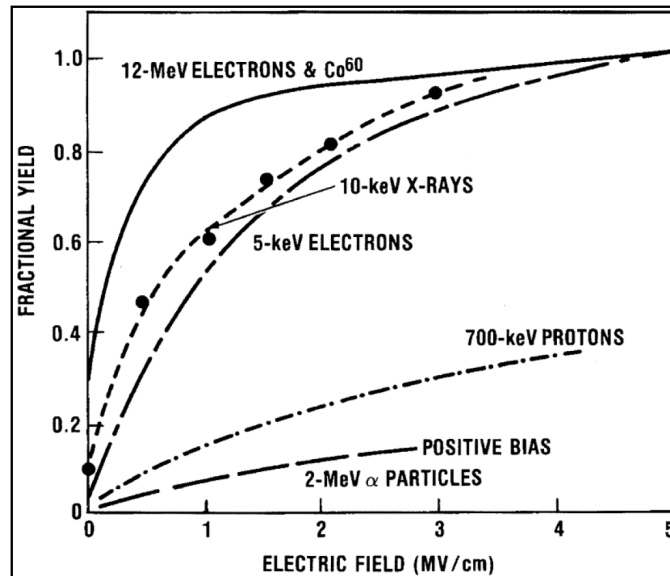


Figure 23: Fractional hole yield vs. electric field for various types of ionizing radiation (after [41]).

Table 4: Electron-Hole Pair Generation Energies and Pair Densities Generated by 1 rad (after [41], [57]).

Material	E_p (eV)	Density (g/cm ³)	Pair Density Generated per rad, g_0 (g/cm ³)
GaAs	4.8 (approx)	5.32	7×10^{13} (approx)
Silicon	3.6	2.328	4×10^{13}
Silicon Dioxide	17	2.2	8.1×10^{12}

reported in sieverts or roentgen equivalent man (rem). The units of TID are equal to the energy deposited per unit mass of medium and can either be represented by the SI unit, gray (1 Gy = 1 J/kg) or the CGS unit, rad (1 rad = 100 erg/g), where 1 Gy = 100 rad. It should be noted that the rad is more commonplace in the radiation effects community and will be the unit of choice for subsequent chapters.

For advanced electronics, TID effects manifest as damage-induced parametric shifts, including threshold voltage shifts, increased off-state leakage, parasitic leakage paths, mobility degradation, and changes in recombination behavior. These shifts are primarily caused by charge trapping in bulk and interface oxides or by traps generated at oxide interfaces. Holes are responsible for TID charge trapping and the resulting trap states because hole mobility < electron mobility in SiO₂ [30]. For MOS devices, charge trapping in the gate oxide generates threshold voltage shifts, while charge trapping at the shallow trench isolation (STI) oxide interface creates parasitic leakage paths that increase off-state leakage. For SiGe HBTs, TID results in interface trap states at either the EB spacer oxide or STI oxide interfaces depending on whether the device is operated in forward-mode or inverse-mode. This increased trap density generates a perimeter-dependent space-charge generation/recombination (G/R) base-current leakage component, resulting in a degradation in current gain [13]. These oxide interface traps can also degrade carrier mobility and transit times, which may affect SiGe HBT performance (f_T).

In space radiation environments, TID is primarily the result of long-term exposure to trapped and/or solar protons and electrons. The amount of damage due to ionization from electrons, ions, or photons is directly proportional to the charge yield per unit dose, which is the number of electron-hole pairs generated per rad. Table. 4 lists several important TID parameters for various materials. E_p is the average ionization energy needed to generate an electron-hole pair and g_0 is calculated by multiplying 1 rad ($100 \text{ erg/g} = 6.24 \times 10^{13} \text{ eV/g}$) by the material density and dividing by E_p . The actual charge yield in a given material is a function of the electric field and density of the electron-hole pairs. The large variance between particles in Fig. 23 indicates a strong dependence of charge recombination on TID.

A schematic energy band diagram for a MOS structure is shown in Fig. 24, highlighting the major physical processes underlying TID response. Incident radiation generates electron-hole pairs via direct and indirect ionization processes. Holes that did not recombine remain relatively immobile and stay near their point of generation. Holes gradually move towards the Si/SiO₂ interface over many decades in time

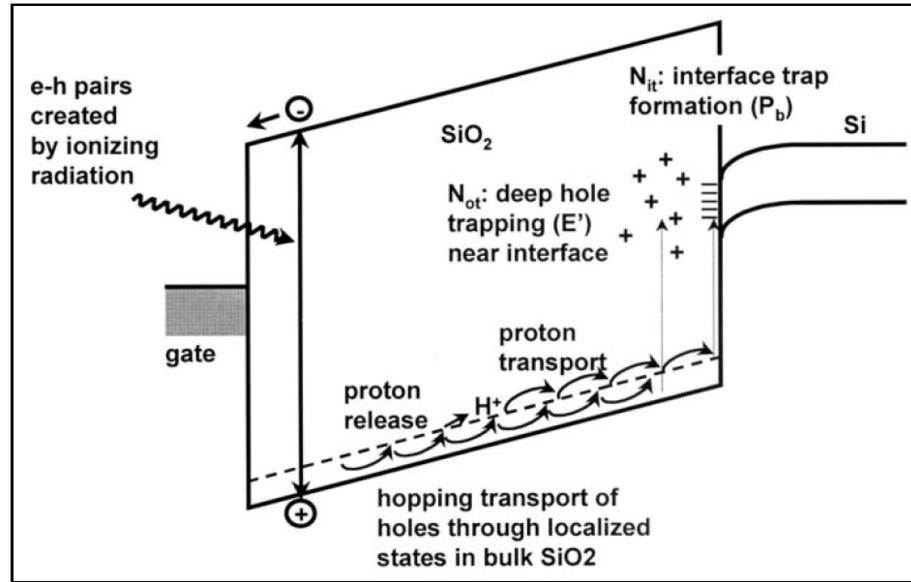


Figure 24: The major physical processes underlying total ionizing dose (TID) degradation (after [41], [55]).

(with respect to electron/hole generation times). This hopping transport process is very sensitive to temperature, oxide thickness, oxide quality, and applied field. At room temperature, this transport process is normally over in much less than one second. As the holes reach the SiO_2 interface, a fraction of them fall into deep, long-lived trap states. These states undergo gradual annealing that can be accelerated at high temperatures. In response to the fixed charge at the SiO_2 boundary of the oxide/semiconductor interface, interface traps (localized states with energy levels in the Si bandgap) buildup on the silicon side, degrading device performance.

Dose rate sensitivities and enhanced low dose rate sensitivity (ELDRS) is a subject of immediate interest within the radiation effects community. ELDRS, a radiation effect unique to bipolar technologies, is a dramatic increase in total dose degradation for DUTs exposed in low dose rate environments [20]. The effects of ELDRS on LM111 voltage comparators is shown in Fig. 25. Traditionally, TID characterization utilizes high dose rates to minimize experimental complexity and test time (cost) at irradiation facilities. The natural space environment, on the other hand, is a low dose rate environment where total dose degradation occurs due to long-term exposures to ionizing radiation. Therefore ELDRS represents a serious concern for orbital and deep-space missions.

2.2.2 Single Event Effects

A SEE is a disturbance to the normal operation of a circuit caused by the passage of a single ion through or near a sensitive node in the circuit. There are two major categories of SEE: destructive and non-destructive. Destructive SEE include single event latchup (SEL), single event burnout (SEB) and single event gate rupture (SEGR). Non-destructive SEE include single event upsets (SEUs), multiple bit upsets (MBUs), single event transients (SETs) and single event functional interrupts (SEFIs). There are other types of SEE, but this list comprises the major types of SEE.

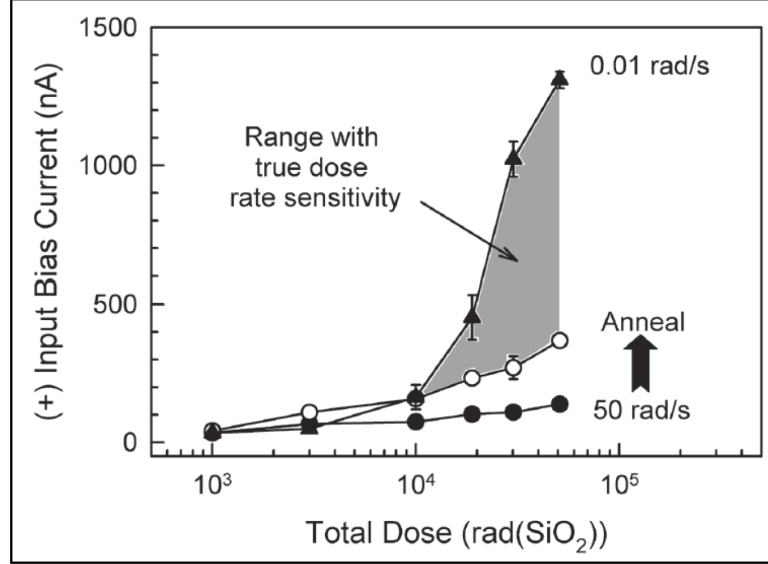


Figure 25: IB+ vs. total dose for LM111 voltage comparators, highlighting ELDRS effects (after [68]).

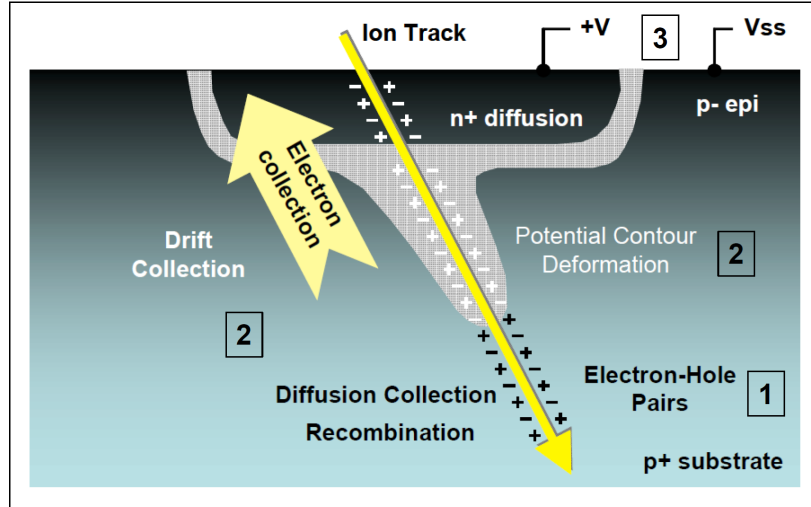


Figure 26: Illustration of a heavy ion strike and the subsequent charge collection processes (after [6]).

An illustration of an ion strike is shown in Fig. 26. As the ion passes through the silicon (or another semiconductor) it generates electron/hole pairs through direct and indirect ionization processes. Both drift and diffusion processes collect these excess carriers, but there is a temporal dependence as to whether drift or diffusion collection dominates. In short timescales post strike, drift collection dominates until

enough charge has been removed for the pn junction's space charge region (SCR) to reform. For longer time scales, diffusion processes dominate and electrons and holes diffuse across the SCR into the n-well and p-substrate respectively. Similar processes occur for ion strikes in vertical SiGe HBTs, except there are two pn junctions in the active device volume (emitter-base and base-collector junctions) that collapse and reform during an ion strike. The charge collected at the device terminals result in voltage and current transients (SETs), which may cause errors or failure in the parent circuit/system.

SEU and MBU occur in a digital circuit or system when an ion strike results in an unwanted bit flip (or multiple flips for MBU), corrupting a digital data stream. The digital system recovers once the radiation-induced transients subside. A SEFI is a soft error that causes a digital component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require a power cycle to restore operation. SEFIs usually occur when an ion strike corrupts a control bit or register. SEL, on the other hand, is an abnormal high-current state that causes a digital component to malfunction. If the device is not permanently damaged from SEL, power cycling is necessary to restore normal operation. SEL events that result in overcurrenting and catastrophic failure are called SEB. An example of SEL for a CMOS device occurs when the passage of an energetic particle creates a parasitic bipolar (p-n-p-n) structure that shorts the power rail to ground. SEGR occurs when an ion strike on a MOSFET results in the breakdown of the gate dielectric, which creates a conducting path through the gate oxide. SEGR causes an increase in gate leakage current and can result in device degradation or complete failure.

2.3 Summary

Ionizing radiation poses several threats to electronic systems in deep-space, interplanetary, and orbital spacecraft. The two most important radiation effects for electronics

are total ionizing dose (TID) and single event effects (SEE). TID occurs when ionizing radiation generates electron-hole pairs that migrate and become trapped at oxide interfaces. The generation/recombination (G/R) traps created by these carriers can cause shifts in device performance, e.g. parasitic leakage paths, threshold voltage shifts, etc., that can degrade the performance of the larger circuit or system. SEE, on the other hand, are operational disturbances within an electronic system caused by the passage of high-energy particles through a sensitive node. The system response to the aforementioned effects is highly dependent on the device topology, therefore a semiconductor technology must be thoroughly characterized before it can be deemed suitable for radiation intense environments.

CHAPTER III

TID AND TRANSIENT RESPONSE OF STATE-OF-THE-ART 4TH GENERATION SiGe HBTs

This chapter details the total dose and transient testing of a fourth generation SiGe BiCMOS process. SiGe HBTs were subjected to proton and TPA backside laser for TID and device transient testing respectively. Comparisons are made with earlier SiGe BiCMOS generation to evaluate the impacts of device scaling on radiation response.

3.1 Introduction

Silicon-Germanium heterojunction bipolar transistor (SiGe HBT) technology has emerged as a serious contender for a diverse set of extreme environment applications. SiGe HBTs possess performance characteristics comparable with III-V technologies while leveraging seamless integration with traditional low-cost, high-yield, Si-based CMOS fabrication [12]. The need for highly integrated millimeter wave/sub-millimeter wave (mm-wave) applications, such as Gb/sec wireless communications, radars, medical imaging, and ultra-high-speed digital electronics (e.g., for 100 Gb Ethernet), requires faster devices than current 130 nm third-generation SiGe BiCMOS technology can provide. Careful vertical and lateral scaling ensures that unity-gain cutoff (f_T) and maximum oscillation (f_{MAX}) frequencies increase at the same rate [65], [88]. The measured f_{MAX} and f_T across SiGe HBT technology generations are shown in Fig. 27. The technology described in the present paper is the new state-of-the-art, fourth-generation, SiGe BiCMOS (9HP) process fabricated at IBM, featuring 90 nm CMOS and 90 nm SiGe HBTs. The process has a target f_T/f_{MAX}

of 300/350 GHz and an advanced BEOL, which includes a full suite of mm-wave passive elements. In order to accomplish this formidable feat, the SiGe HBT structure has fundamentally changed from its predecessors, necessitating a re-evaluation of its radiation response. Careful changes to the lateral and vertical profile were made in order to improve performance, including larger Ge mole fraction, thinner base and collector profiles, and a new device structure that minimizes parasitics associated with the collector-base junction. In order to maintain low emitter resistance with scaling, innovative processes were employed to ensure clean interfaces in the emitter/base and poly emitter/tungsten stud region [56]. IBM 9HP will combine this new SiGe HBT with “off-axis” CMOS, providing a versatile, high-performance platform for ultra-high-speed analog, digital, and mm-wave applications. The 9HP devices characterized in this paper represent preliminary hardware ($f_T \approx 260 \text{ GHz}$) using the new device structure.

The effects of lateral and vertical scaling on the observed proton tolerance for earlier IBM SiGe technology generations (IBM 5AM/5HP, 7HP, and 8HP) have been

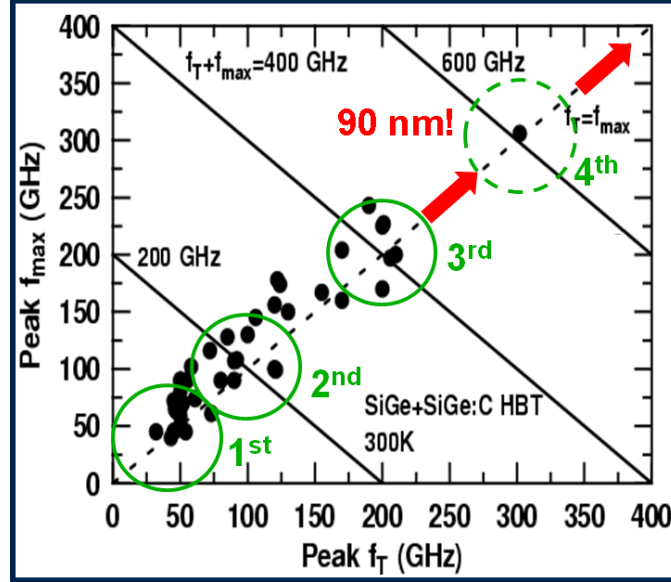


Figure 27: Measured maximum oscillation frequency versus unity-gain cutoff frequency for a variety of SiGe HBT technology generations (after [88]).

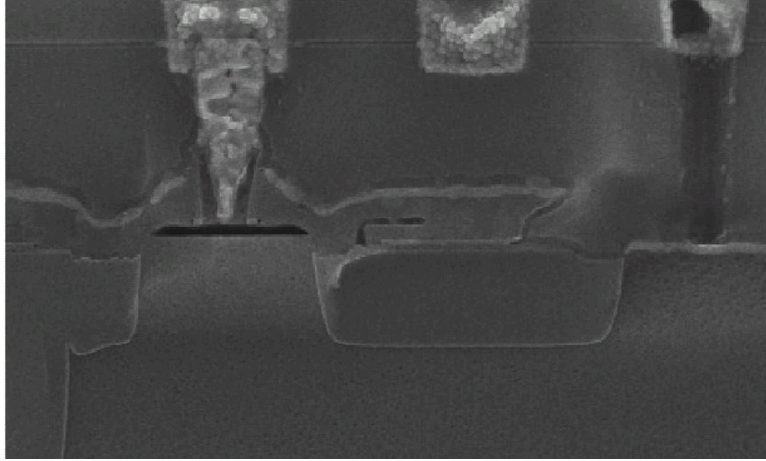


Figure 28: SEM cross-section of IBM 9HP SiGe HBT.

previously reported [32, 13, 37]. An earlier experimental direct-shrink of IBM 8HP (labeled 9T) have also been reported [76], but these devices lacked the scaling modifications present in 9HP and, for clarity, are not included here. This novel 9HP device structure, shown in Fig. 28, raises several questions regarding the potential susceptibility to radiation-induced G/R trap centers along the EB spacer oxide and shallow trench isolation (STI) interfaces. In this paper are both, the first report of the total ionizing dose (TID) tolerance of 9HP and the first data on its laser-induced transient response.

3.2 Experimental Details

3.2.1 Total Ionizing Dose Testing

For the total ionizing dose analysis, the samples were irradiated with 63.3 MeV protons at the Crocker Nuclear Laboratory at the University of California at Davis. The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup. The radiation source (Ta scattering foils) located several meters upstream of the target establishes beam spatial uniformity of about 15% over a 2.0 cm radius circular area. Beam currents ranging from about 20 to 100 nA allowed testing with proton fluxes from 1×10^9 to 1×10^{12} protons/cm²s. The dosimetry system

has been previously described [50] and is accurate to about 10%. At proton fluences of 7.5×10^{11} p/cm² and 2.3×10^{13} p/cm², the measured equivalent total ionizing dose was approximately 100 krad(SiO₂) and 3.0 Mrad(SiO₂), respectively, the upper bound covering virtually all orbital environments.

3.2.2 Pulsed-Laser Testing

Laser-induced transients were measured at the Naval Research Laboratory using a two-photon absorption (TPA) backside pulsed laser system capable of supplying a $1.0 \mu\text{m}$ diameter charge distribution profile [43]. This system was employed because it enables 3-D, position-dependent, time-resolved measurements of single event transients (SET). In this TPA system, device-level current transients are induced by injecting carriers using TPA from a sub-bandgap pulsed laser. These carriers are then recorded using high-bandwidth measurement equipment, including a Tektronix DPO71254, 12.5 GHz, 50 GS/sec, real-time oscilloscope. The system is configured to produce optical pulses at 800 nm at a repetition rate of 1 kHz and a pulsewidth of approximately 120 fs. The x-y-z translation platform has a position resolution of $0.1 \mu\text{m}$, and all data was collected in a rectangular x-y grid at a fixed “z”, with a step size of $0.25 \mu\text{m}$. Upon inserting each DUT, the “z” position was optimized to place the sensitive volume at the peak focus of the laser beam. Transient currents in first-generation SiGe HBTs have been measured using a similar experimental setup [58]. For this paper, minimum-sized IBM SiGe 5AM ($0.5 \times 1.0 \mu\text{m}^2$) and 9HP ($0.1 \times 1.0 \mu\text{m}^2$) SiGe HBTs were measured at worst-case bias conditions to discern whether new transient mechanisms might result from device scaling.

3.3 Results and Discussion

3.3.1 Total Ionizing Dose Response

The forward-mode Gummel characteristics as a function of total ionizing dose for the $0.1 \times 1.0 \mu\text{m}^2$ IBM 9HP SiGe HBTs are shown in Fig. 29. The 9HP HBT exhibits

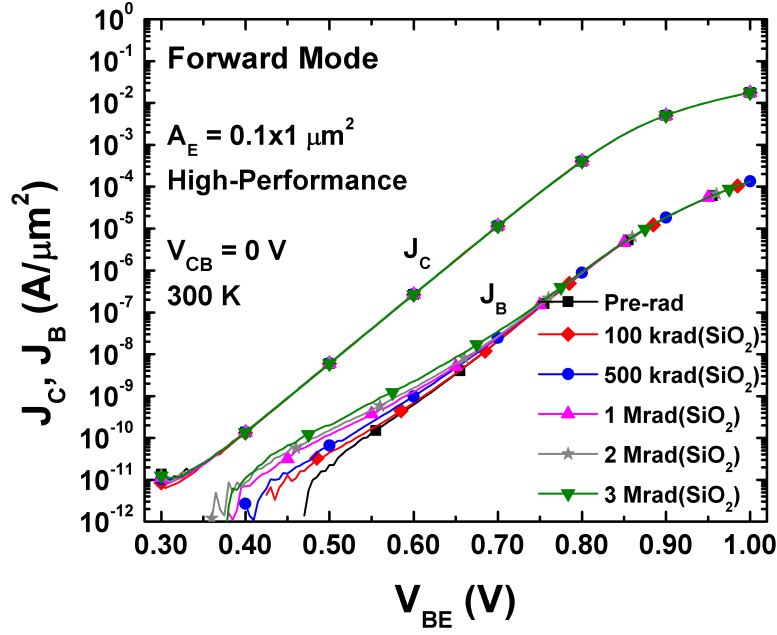


Figure 29: Forward-mode Gummel characteristics of a $0.1 \times 1.0 \mu\text{m}^2$ IBM 9HP SiGe HBT (after [36]).

minimal base leakage across V_{BE} at 100 krad(SiO_2). As the HBT was subjected to larger ionizing dosages, base leakage (at lower V_{BE}) increased by more than one order of magnitude. However for many high-speed digital and RF applications, HBTs are commonly biased close to peak f_T , in order to benefit from increased circuit speed and performance. From Fig. 29, the minimum-sized ($0.1 \times 1.0 \mu\text{m}^2$) device exhibits minimal base leakage at these functional circuit biases ($V_{BE} > 0.6 \text{ V}$). The forward-mode current gain (β) shown in Fig. 30 reveals that for collector current densities close to peak f_T , the current gain remains relatively unaffected by TID. As can be seen in Fig. 31, the 9HP HBT also exhibits negligible shifts in output current (I_C vs. V_{CE} and output conductance (g_{CE})). These results confirm that IBM 9HP maintains the TID tolerance observed in previous SiGe BiCMOS generations and suggests that the new 9HP structure does not incur any added TID risk.

The increase in base leakage current density, a classical signature for TID damage in bipolar transistors, is attributed to radiation-induced G/R traps located at the EB

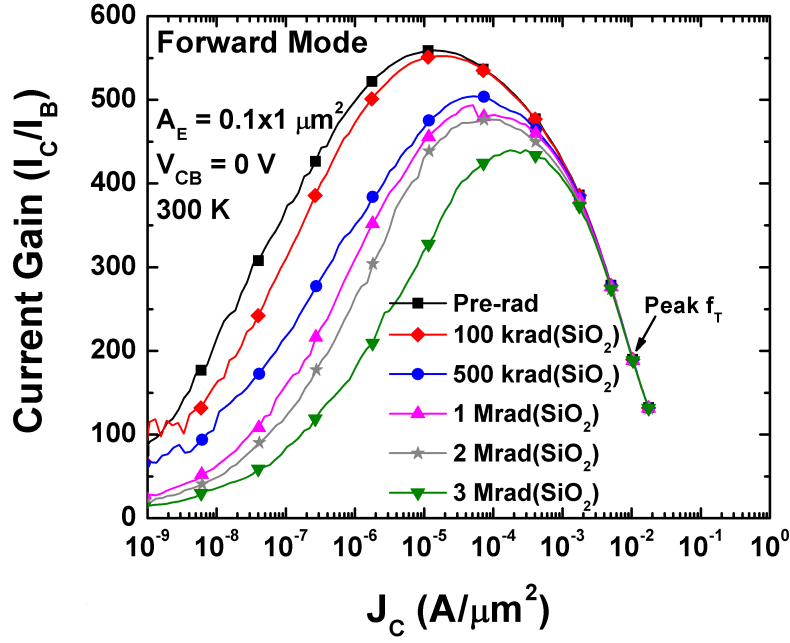


Figure 30: Forward-mode current gain vs. collector current density for various values of TID (after [36]).

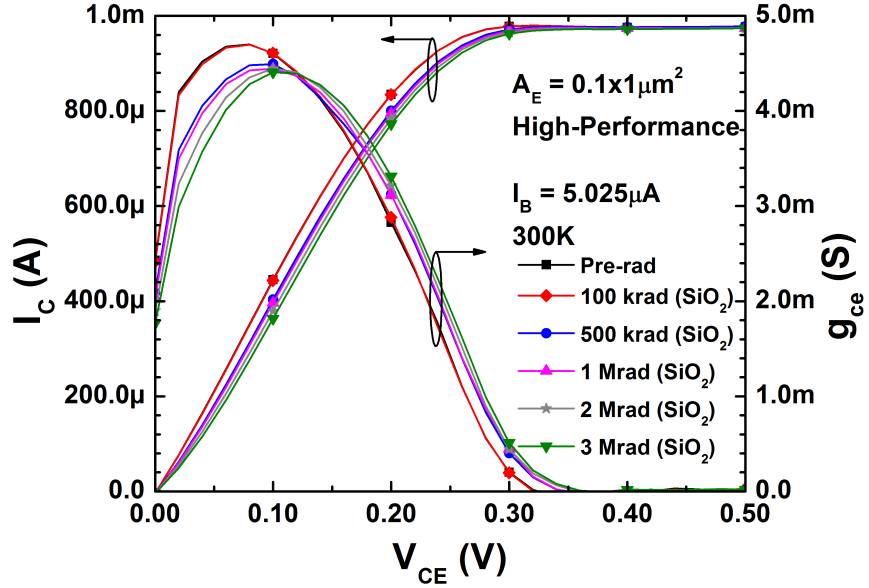


Figure 31: Output characteristics of a $0.1 \times 1.0 \mu\text{m}^2$ IBM 9HP SiGe HBT (after [36]).

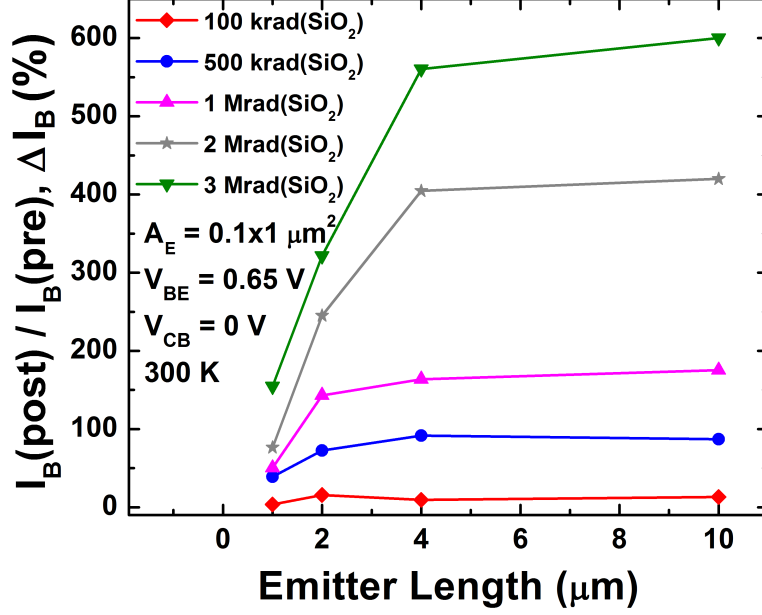


Figure 32: Normalized base current leakage across HBT emitter length (after [36]).

spacer oxide [4]. The normalized base leakage current across emitter length at various TID is shown in Fig. 32. Since the damage incurred at this interface increases with the perimeter of the active emitter (PE), greater TID sensitivity is expected at longer emitter lengths, and a tradeoff between current drive and TID tolerance should exist for highly-scaled technology nodes. Fig. 32 can be split into two regions of interest: a linear damage region (Region 1) and a saturated damage region (Region 2). All four devices exhibit similar base leakages at 100 krad(SiO₂). As the ionizing dose is increased to 500 krad(SiO₂) and 1 Mrad(SiO₂), Region 1 extends to an emitter length of 2 μm before entering Region 2. Continuing irradiation to multi-Mrad TID marks an extension of Region 1 up to an emitter length of 4 μm. While greater TID sensitivity was seen at longer emitter lengths, these preliminary results show a potentially new damage mechanism for highly-scaled SiGe BiCMOS technology nodes. Repeated measurements on new, commercial hardware and 3-D TCAD simulations are required before these mechanisms can be described in detail.

Two *DC* figures-of-merit, excess base leakage current (Fig. 33) and peak current

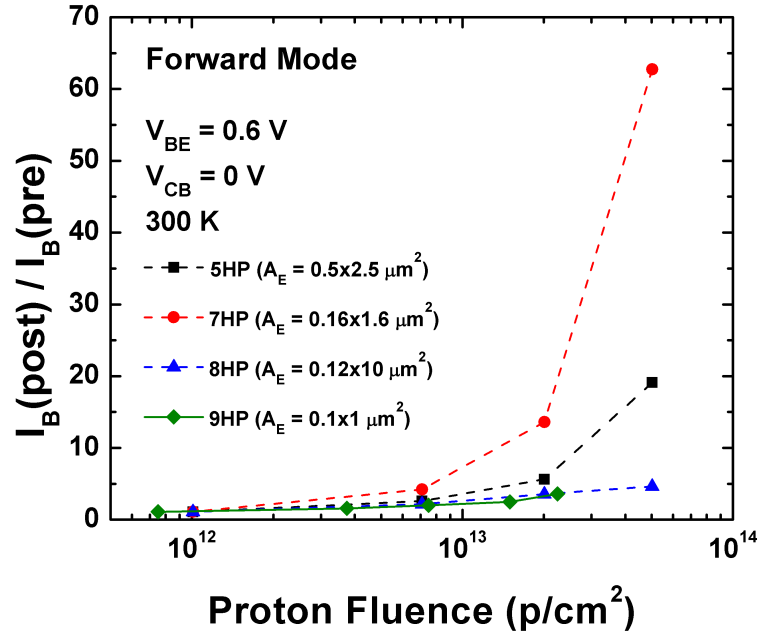


Figure 33: Forward-mode base current degradation vs. proton fluence across IBM SiGe technologies (after [36]).

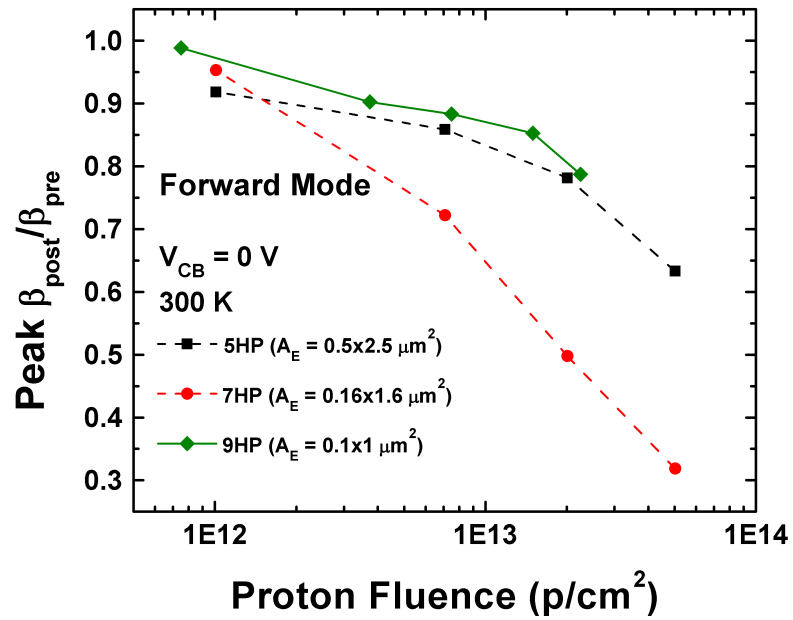


Figure 34: Peak current gain degradation vs. proton fluence across IBM SiGe technologies (after [36]).

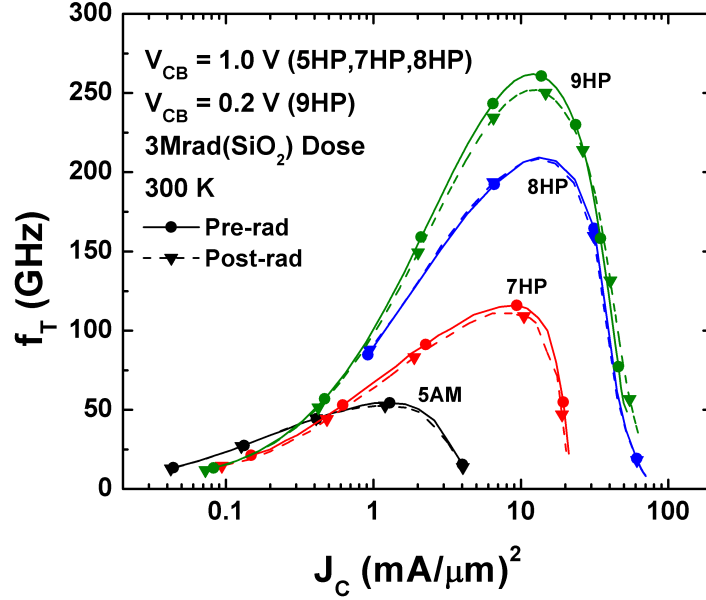


Figure 35: Pre-rad and post-rad unity gain cutoff frequencies across IBM SiGe technologies (after [36]).

gain degradation (Fig. 34), were used to make preliminary proton tolerance comparisons across several SiGe technology generations. IBM 9HP exhibits lower base leakage currents at higher proton fluences (3 Mrad(SiO₂)), resulting in an on-par or superior current gain response in comparison with previous SiGe generations. In addition to the above figures-of-merit, pre- and post-irradiation unity gain cutoff frequencies (f_T) were compared and are shown in Fig. 35. IBM 9HP exhibits a minor (4%) reduction in peak f_T (effectively within the error bars of measurement repeatability), similar to other SiGe generations. IBM 9HP maintains the TID robustness of earlier SiGe HBT generations, while providing superior current gain and cutoff frequency.

3.3.2 Pulsed-Laser Transient Response

While the previous section demonstrated that 9HP SiGe HBTs are inherently robust to ionizing radiation in terms of TID, single event effects (SEE) are a critical issue for high-speed digital and analog applications. Beam testing on digital shift registers are

a proven method for probing single event sensitivities within a technology [61]. While these measurements have not yet been performed (the hardware is in fabrication), the laser-induced transient response of 9HP and 5AM devices were measured and compared at various biases to help understand the underlying transient mechanisms. The experimental hardware (same hardware run as proton TID), had an unpolished backside substrate surface. This poor substrate surface resulted in some scattering at the backside interface and an uncertainty in the exact energy deposition within the SiGe HBT. The goal of this work is to determine whether the same transient mechanisms are present in 9HP as are found in other IBM SiGe platforms and if the 9HP SiGe HBTs investigated possess an improved SEE response with scaling. Due to the aforementioned substrate quality issues, this discussion focuses on a qualitative rather than quantitative understanding of 9HP device transients.

Transistor node transients were captured along a raster scan, resulting in the 2-D collected charge plots as shown in Fig. 36 and Fig. 37. These raster scans were captured while the collector-substrate junction of the HBT was reverse-biased. Similar to previous SiGe generations, there is a collector-substrate diffusion funnel resulting in collected charge of equal magnitude but opposite polarity as electrons/holes diffuse into the sub-collector/substrate respectively. Preliminary transient plots at a different worst-case off-state transient scenario (high V_{CE}) are shown in Fig. 38. Observe that the transient magnitude is reduced substantially in 9HP compared to 5AM devices due to the smaller active device area. These reduced transient magnitudes suggest a possible strong reduction in error cross-section across LET for shift-registers fabricated in IBM 9HP. To first order, 9HP appears to follow the same transient mechanisms as earlier SiGe generations. In order to verify these preliminary device-level transient measurements, TPA testing on second-round, commercial 9HP hardware is required. Broadbeam testing on master-slave shift registers designed in 9HP will determine if there is any single event upset (SEU) improvement.

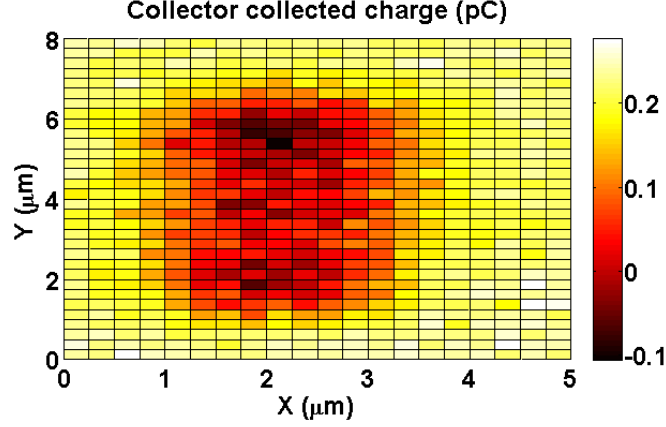


Figure 36: 2-D collected charge at collector terminal for a $0.1 \times 1.0 \mu\text{m}^2$ 9HP SiGe HBT with reverse-biased collector-substrate junction (after [36]).

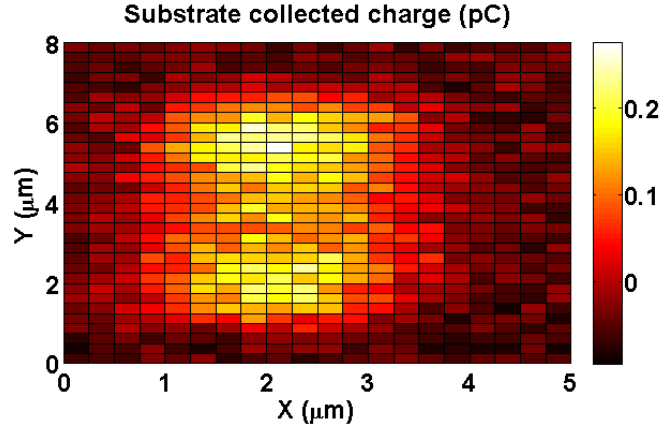
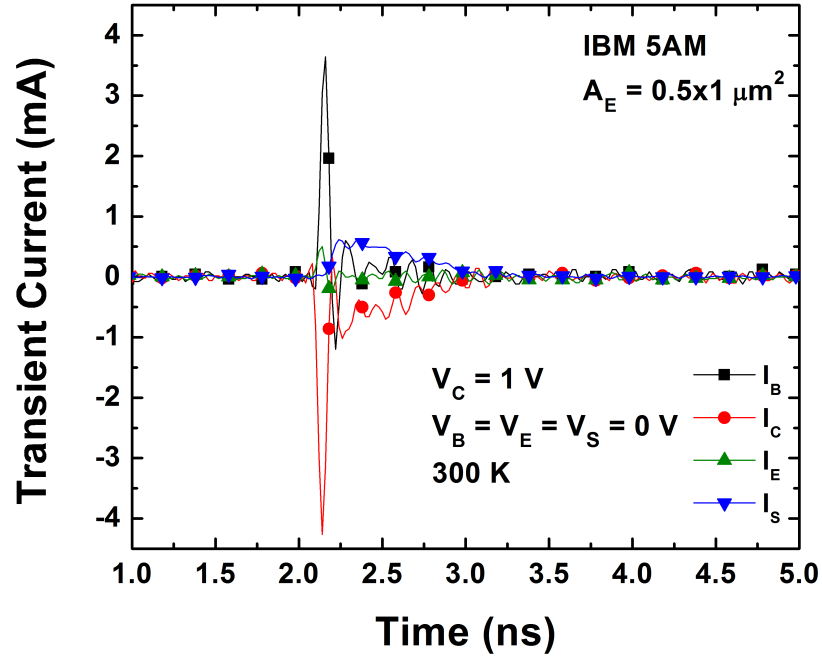


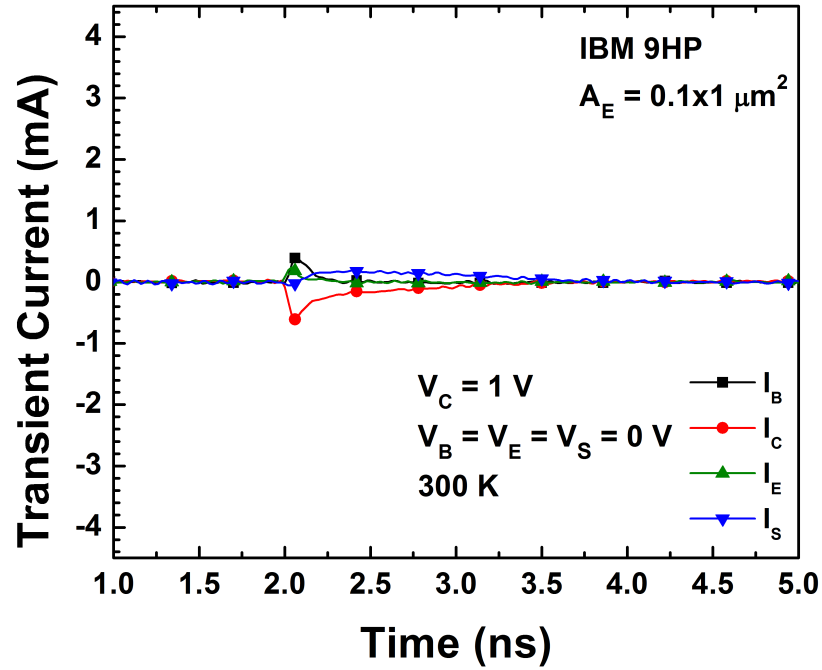
Figure 37: 2-D collected charge at substrate terminal for a $0.1 \times 1.0 \mu\text{m}^2$ 9HP SiGe HBT with reverse-biased collector-substrate junction (after [36]).

3.4 Conclusion

The proton tolerance and laser-induced transient response of SiGe HBTs from the new 90 nm, SiGe BiCMOS platform were investigated. IBM 9HP SiGe HBTs exhibited minor base leakage, gain degradation, and f_T degradation at ionizing doses up to 3 Mrad(SiO₂). TID damage was negligible at functional biases near peak f_T . Laser-induced transient analysis revealed a favorable reduction in device node transients with scaling, suggesting a possible SEE improvement for analog and high-speed digital circuits.



(a)



(b)

Figure 38: Transient waveforms for (a) IBM 5AM ($0.5 \times 1.0 \mu\text{m}^2$) and (b) IBM 9HP ($0.1 \times 1.0 \mu\text{m}^2$) SiGe HBTs at high V_{CE} (after [36]).

CHAPTER IV

EVALUATION OF SIGE BICMOS FOR USE IN HIGH TEMPERATURE APPLICATIONS

This chapter serves as a general assessment of SiGe's applicability in high temperature environments. Devices and circuits are characterized up to 300 °C and a RHBD technique is introduced to help mitigate thermally increased leakage currents.

4.1 *Applications of High Temperature Electronics*

Interest in high temperature electronics has increased steadily over the past decade as technology improvements have begun to open up new application opportunities. An illustration detailing emerging high temperature markets, semiconductor technologies and their suitable temperature ranges is shown in Fig. 39. Of the emerging markets, the automotive industry represents one of the largest, especially with the recent move toward hybrid electric and fully electric vehicles. Under-the-hood electronics must

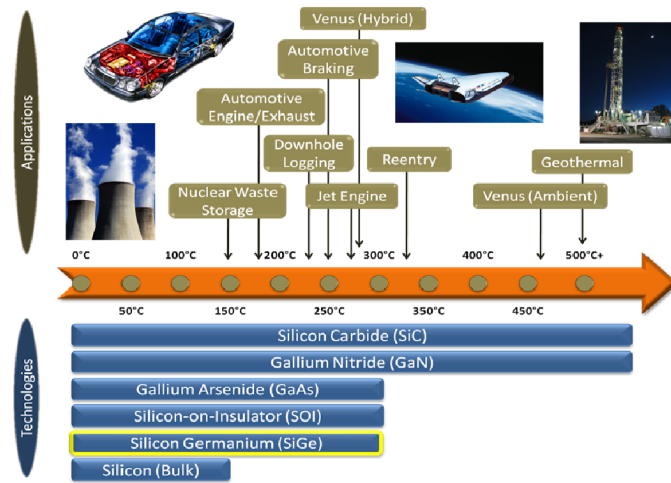


Figure 39: Emerging high temperature applications and safe operating ranges of popular high-T technologies.

withstand temperatures up to 200 °C, with even higher temperatures needed for brake systems, cylinder pressure sensors, or exhaust sensing [31]. Related to the push for electric vehicles, the need for more effective downhole well logging requires electronics able to function at temperatures up to 300 °C and beyond [81]. In addition, next generation commercial aircraft hope to reduce complexity and weight by moving electronics closer to their controlled systems, many of which need are at elevated ambient temperatures [45]. Not to be overlooked, high temperature electronics are key requirements for potential NASA missions to Venus and Jupiter, where temperatures can exceed 400 °C [17]. NASAs proposed missions to the surface of Venus will likely use a dual-temperature zone or hybrid system of high temperature electronics (250 °C and 460 °C) with dramatically longer survival times [33]. In order to satisfy these emerging applications, we must carefully re-evaluate existing device, circuit, manufacturing, and packaging design options.

4.2 Experimental Details

The development of reliable high temperature packaging is an on-going area of research and a non-trivial concern for experimental characterization. FR-4, lead-tin solders, and other conventional packaging processes used for commercial electronics begin to fail around 150 °C [38]. Special attention must be paid to the printed wiring board or substrate material, wire bonding method, interconnect metallization, ceramic package, adhesive, and wiring/cabling for reliable operation up to and beyond 200 °C [26]. Based on lessons learned from previous attempts at packaging, a custom, reusable high temperature test system was designed for use with these measurements.

Using an ultra-high temperature glass-mica ceramic called Macor, a test fixture was designed to accept a 44-pin ceramic quad-flatpack, which was self-aligned by carefully sized grooves for each lead on the package. Macor was chosen for its low

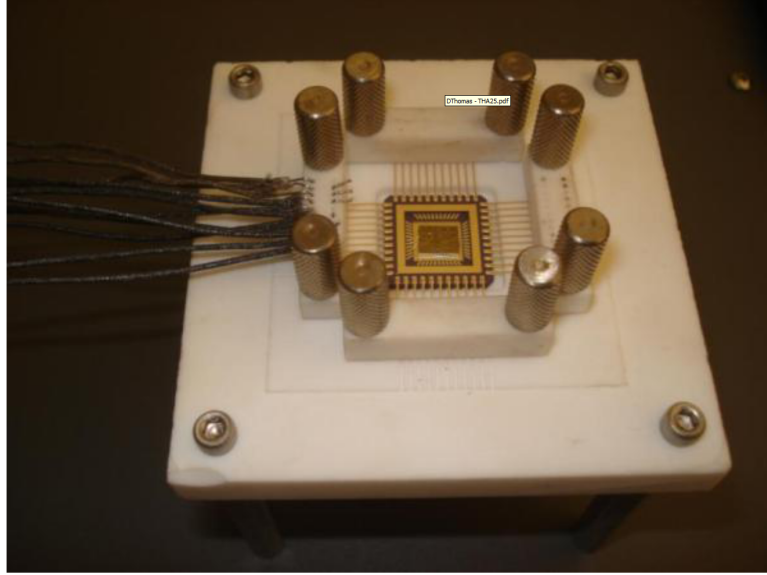


Figure 40: PCB-based packaging used for 300°C testing (after [78]).

coefficient of thermal expansion (CTE), high maximum continuous operating temperature (800 °C), excellent electrical insulation, and relative ease of manufacturing [11]. Four bar clamps, one on each side, were then screwed down over the leads to secure the package in the fixture. Due to previous successes using mechanical force to maintain electrical continuity, two small holes were drilled in each bar, and a high temperature wire was passed through one hole, along a groove acting as a guide, and back up through the second hole. Each bar clamp included eleven such wire slots to match the number of package leads, which allowed for a simple, reusable wire interface. Finally, stainless steel offsets were added to the fixture to align the platform height with the ports on the oven in order to keep the wire length to less than 6 inches, minimizing losses and parasitics. Fig. 40 shows a packaged SiGe circuit ready for characterization.

All testing was performed inside a Delta Design 9023 test oven capable of 315 °C operation, and measurements were obtained using Agilent 4155/6C semiconductor parameter analyzers, Tektronix TDS 7054 digital oscilloscope and AFG 3252 function generator and HP 89410A VSA .

4.3 SiGe BiCMOS Device Test Structures at High Temperatures

The potential for using SiGe platforms in high temperature applications can be first established by examining the devices that comprise the fundamental building blocks of simple circuits. Previous work has shown that SiGe HBTs are fully functional up to temperatures as high as 300 °C; furthermore, the SiGe HBTs show acceptable performance in key specifications such as gain, breakdown voltage, cutoff frequency, and low-frequency noise [10]. Additionally, the inverse temperature dependency of the current gain in SiGe HBTs also serves to limit thermal runaway, which is a concern in Si BJTs at high temperatures. The typical family of output characteristics is shown in Fig. 41. Although the leakage currents were substantially higher, on the order of 1 μA , as expected in a bulk-SiGe technology, these transistors still maintained a very usable active range up to 300 °C. If elevated substrate leakages become a limiting factor, a traditional solution is to utilize an SOI process with lateral transistors. The

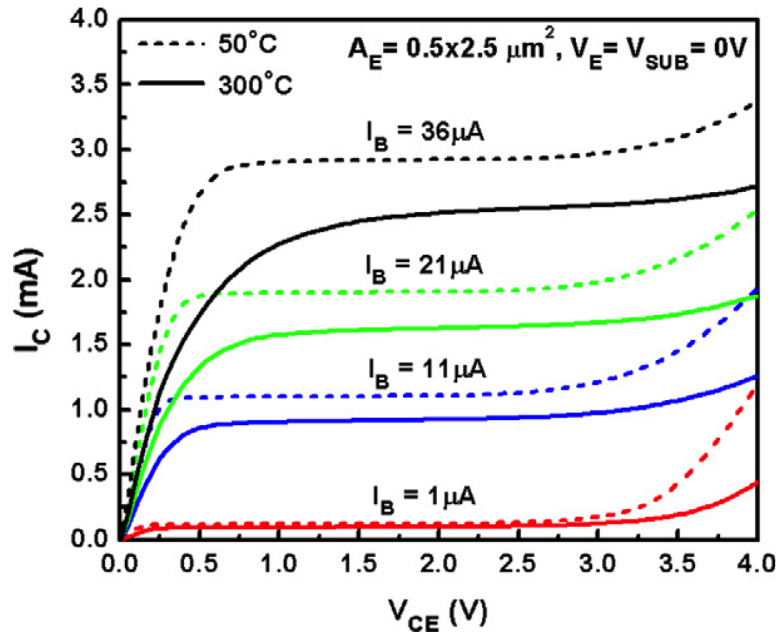


Figure 41: Comparison of the output characteristics for a SiGe HBT at 50 °C and 300 °C, showing ideal, useable performance at high temperatures (after [79]).

availability of SiGe-on-insulator (SGOI) technology in recent years offers a possible path forward if needed.

MOSFETs are another class of important devices in the BiCMOS platform to characterize under high ambient temperatures. The output characteristics of both nFETs and pFETs exhibited a 20% to 40% decrease in drain current magnitude at 300 °C when compared to room temperature operation; however, the subthreshold characteristics of the MOSFETs were of greater concern due to the potential influence of leakage currents [16]. Fortunately, the magnitude of these currents was only 0.1 μA at 300 °C. Threshold voltage decreased with rising temperature, as expected, and the presence of a zero-temperature coefficient (ZTC) bias point was confirmed, as shown in Fig. 42 [39].

A wide variety of resistors are available in the SiGe BiCMOS platform under investigation, and these resistors could be grouped into three general families based upon their temperature dependency: strongly proportional, weakly proportional, and

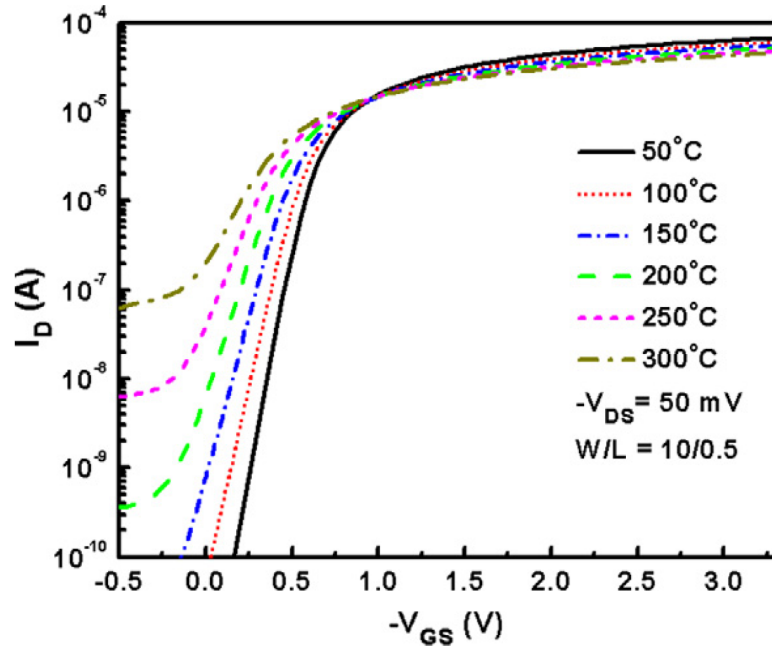


Figure 42: Sub-threshold curves for pFET across temperature, demonstrating zero-temperature coefficient bias point and acceptable performance up to 300 °C (after [79]).

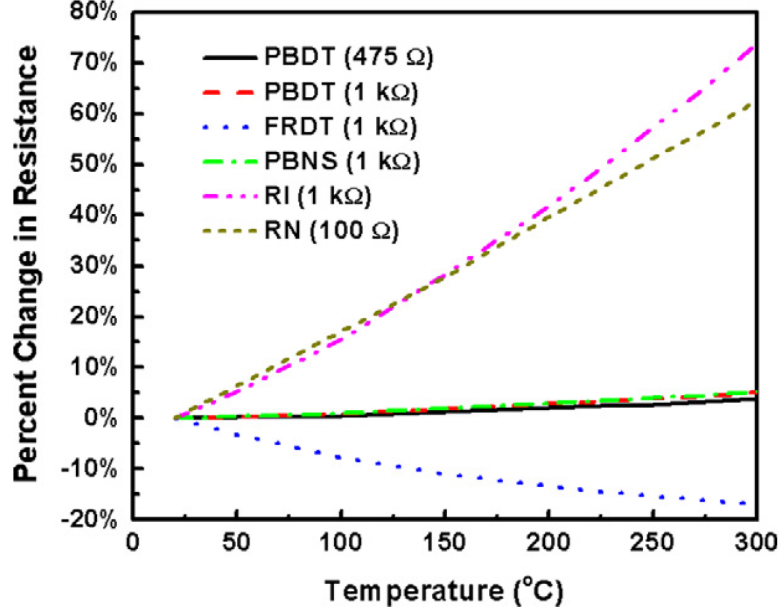


Figure 43: Measured resistance change of 1st generation SiGe BiCMOS resistors over temperature indicating good linearity for each resistor type (after [79]).

inversely proportional. As shown in Fig. 43, all resistors maintained a linear relationship across the entire temperature range. The PBDT (p+ poly over oxide) resistors are particularly important because they are used extensively in the bandgap reference (BGR) and temperature sensor circuits described in the following sections. The PBDT resistor, with its relative temperature-independence, experienced only a 5% increase in resistance between room temperature and 300 °C.

One promising device-level RHBD approach is the inclusion of an n-type implant surrounding the deep trench isolation of a SiGe HBT, known as an external n-ring and illustrated in Fig. 44 [75]. With a positive bias applied to the n-ring, the charge deposited during heavy ion strikes is collected by the n-ring rather than the collector, mitigating any changes in HBT biasing due to the strike. In high temperature environments, the presence of n-rings was expected to alter the electric field near the collector-substrate junction, thereby reducing collector-substrate leakage currents in bulk-SiGe HBTs.

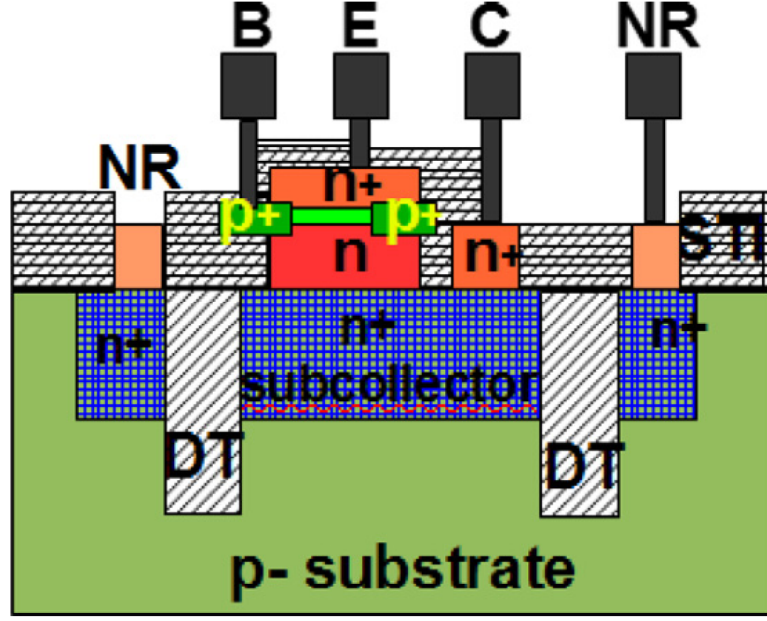


Figure 44: Cross-section of RHBD SiGe HBT in 1st generation platform with external n-ring, deep trench isolation, and vertical stack (after [75]).

Because the collector-substrate junction is always reverse-biased, the leakage current is determined by the diffusion of minority carriers across the collector-substrate SCR. As temperature increases, the intrinsic carrier concentration in the silicon substrate increases, approaching the doping concentration and causing the number of free electrons to increase dramatically. The external n-ring should counteract this increase of carriers in the substrate by acting as a vacuum and pulling excess free electrons in the vicinity away from the collector, which in turn should suppress leakage currents at higher temperatures. As shown in Fig. 45, measurements confirmed that leakage currents were reduced by a factor of two in ambient conditions above 175 °C. The SiGe HBT with external n-ring was modeled in Sentaurus TCAD simulator, and the same general behavior was observed a drop in leakage current with a bias applied to the n-ring. However, these simulations reported a decrease in leakage current by two orders of magnitude, considerably higher than empirical observations. Despite the discrepancy, this RHBD technique could potentially allow bulk-Si platforms to function in higher temperature environments than previously thought possible.

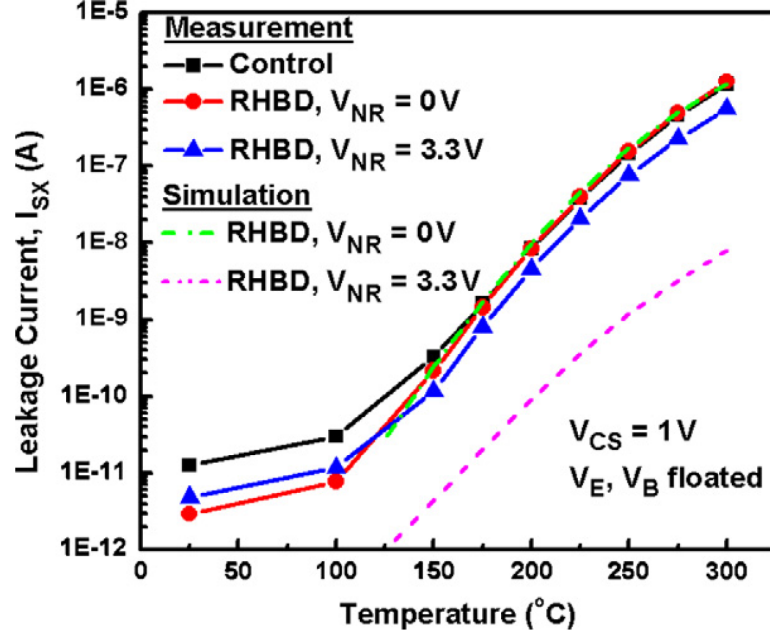


Figure 45: Substrate leakage currents for a SiGe HBT collectorsubstrate junction across temperature, both with and without external n-ring. Both simulation and measurement show improvement with biased ring (after [79]).

4.4 High Temperature Operation SiGe BiCMOS Circuits

4.4.1 Operational Amplifier for Large Capacitive Loads

Piezoelectric sensors are a widely used class of sensors that measure pressure, acceleration, strain, or force by converting the desired input into an electrical current. In order to process the signal from the piezoelectric sensor, a data acquisition system must contain a charge amplifier to convert the incoming charge into a voltage, which is traditionally accomplished through the use of an operational amplifier with a capacitive feedback loop. Charge amplifiers are also useful with other charge-based devices such as photodiodes.

To build a charge amplifier, an operational amplifier (opamp) that is capable of handling the large capacitances in the system must be designed first. The opamp shown in Fig. 46 is a suitable circuit using an operational transconductance amplifier (OTA) topology [24]. This circuit utilizes a pFET differential pair to minimize input currents, which could compromise its sensitivity to small charge variations from the

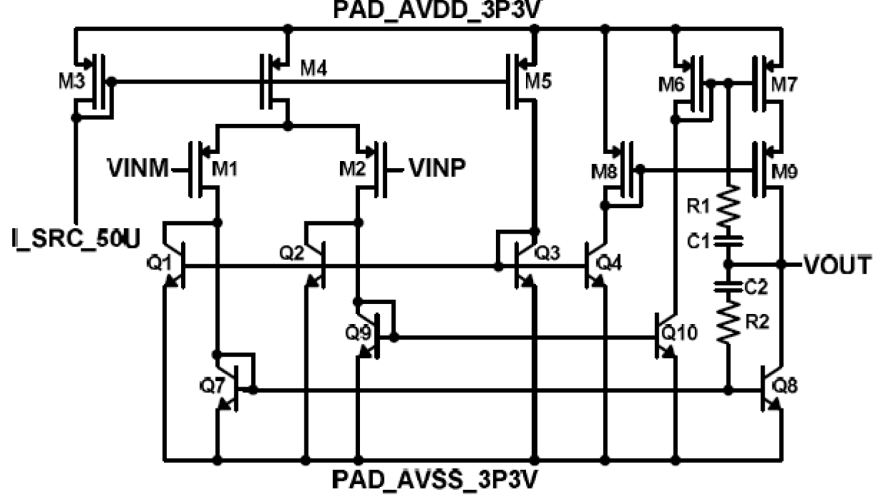


Figure 46: Circuit topology of a SiGe opamp for large capacitive loads (after [78]).

sensor. The circuit was designed using only SiGe HBTs and pFETs due to their superior radiation tolerance. Unfortunately, mismatch (systematic or random) between the positive and negative input stages of the amplifier could lead to offset problems that would be exaggerated at high temperatures. All DC and AC measurements were performed with a 33 nF capacitive load on the amplifier output.

Typical piezoelectric sensors operate at very low frequencies, so the associated charge amplifier did not require the superior RF performance offered by SiGe HBTs but instead benefited from their low $1/f$ noise. Although the opamp under investigation was required to have a bandwidth of 5 kHz according to the specification, it was designed with higher frequency applications in mind for versatility and reusability. As with previously tested SiGe BGR and temperature sensor circuits, the sponsoring program had targeted this circuit for lunar operating conditions of $-180\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, with elevated radiation fluxes and possible low temperatures of $-230\text{ }^{\circ}\text{C}$ in the shadowed craters. Fig. 47 shows the measured frequency response of the opamp from room temperature to $300\text{ }^{\circ}\text{C}$, with passives located outside the test chamber in room temperature conditions. From room temperature up to $250\text{ }^{\circ}\text{C}$, the opamp was fully functional, experiencing minor drops in open loop (DC) gain, -3dB bandwidth

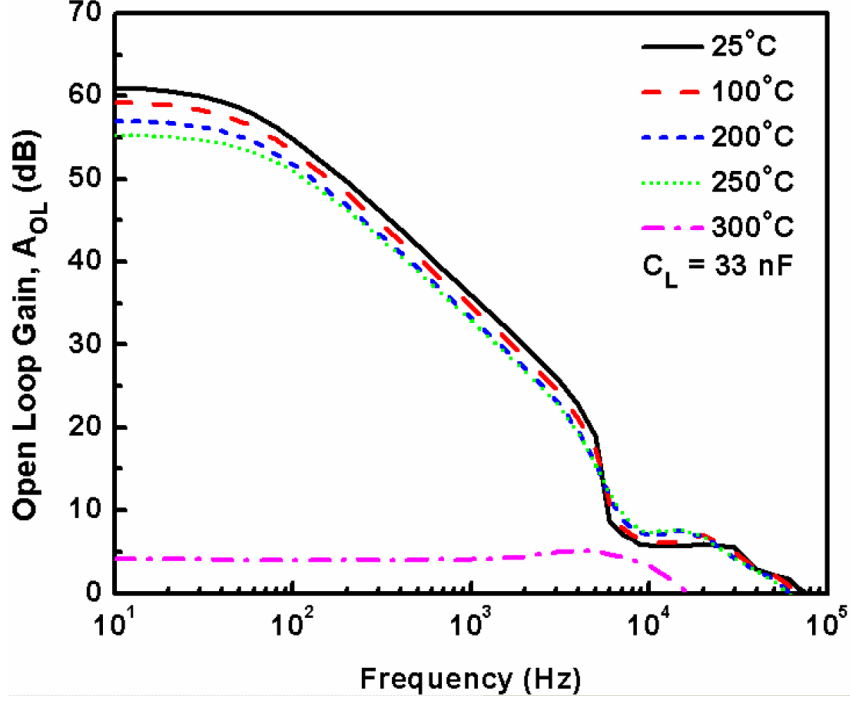


Figure 47: Frequency response of the SiGe opamp with 33nF load across temperature (after [78]).

(f_{3dB}), and unity gain bandwidth. The DC gain remained above 55 dB across the temperature range, while -3dB and unity-gain bandwidth were above 55 Hz and 60 kHz, respectively. Above 250 °C, the open loop gain dropped rapidly due to clipping and rising DC offset, and by 300 °C, the amplifier was no longer usable in a practical system.

Surprisingly, these results show good agreement with compact model (Cadence) simulations. In Fig. 48, the experimental results match simulation except for a slightly lower DC gain, which is notoriously difficult to measure. In fact, the measured bandwidth was slightly higher when compared to simulation. Lastly, the non-linearity observed near 10 kHz is most likely caused by harmonics and reflections arising from a combination of the packaging approach and parasitic effects between the amplifier and externally located passives, especially in the feedback network.

In addition to the bandwidth of the amplifier, several other important parameters were characterized up to 300 °C, although the results from room temperature to 250

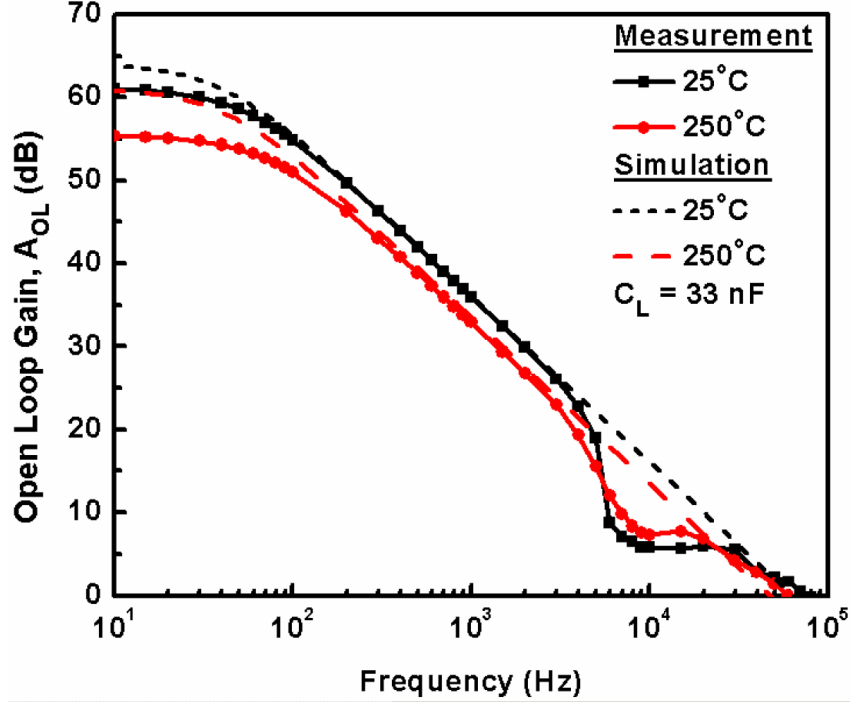


Figure 48: Comparison of simulated and measured frequency response of the SiGe opamp at 25 °C and 250 °C (after [78]).

°C are presented here due to the previously mentioned degradation at temperatures above 250 °C. The DC offset voltage for the opamp, measured at the output by grounding both input terminals through 100 Ω resistors, adding a 1 k Ω feedback resistor, and dividing out the gain factor (10), was significantly higher than anticipated, with values ranging from 5.93 mV at 25 °C to 8.77 mV at 250 °C. However, by using an alternate simulation approach not feasible for experimental characterization, the simulated DC offset was on the order of 1 mV.

The slew rate of the amplifier, which is the maximum rate of change in the output voltage for all possible input signals, actually improved slightly with increasing temperature a welcome sign. Furthermore, the quiescent current (Q-current) drifted only slightly higher with temperature, and accordingly, the power consumption of the amplifier remained near 5 mW. A comparison between measured and simulated figures of merit (FoM) is shown in Table. 5. In general, measurements were in agreement

Table 5: Measured and simulated FoM for the SiGe operational amplifier with 33 nF load (after [78]).

Parameter	Measurement		Simulation		Unit
	25°C	250°C	25°C	250°C	
3dB Bandwidth, f_{3dB}	58	76	40	42	Hz
Open-loop Unity Gain Bandwidth	77	60	63	48	kHz
Open-loop (DC) Gain	61.0	55.3	64.1	61.1	dB
DC Offset (Gain = 10)	5.93	8.77	5.57	8.41	mV
Positive Slew Rate	42.3	46.5	47.5	45.4	kV/s
Negative Slew Rate	-51.1	-53.0	-51.5	-51.5	kV/s
Quiescent Current ($V_{IN} = 1.65$ V)	1432	1684	940	995	μ A
Power Consumption ($V_{IN} = 1.65$ V)	4.73	5.56	3.10	3.25	mW
Maximum V_{OUT} ($V_{IN} = V_{DD}$)	2.63	2.83	2.62	2.86	V

with simulation results with quiescent current having the greatest deviation.

4.4.2 Low-Impedance Output Buffer

Many amplifiers that are designed for integrated systems lack the ability to drive low-impedance loads, necessitating the addition of an output buffer. In addition to a low output impedance, these buffer circuits offer a high input impedance and an inherent unity gain. An emitter follower is the most basic topology for an output buffer; however, it exhibits undesirable DC gain behavior and signal distortion due to changes in transconductance during large signal swings. The circuit shown in Fig. 49 is a realized output buffer circuit with shunt feedback at the output to reduce the sensitivity inherent in emitter follower topologies [24]. This buffer was designed with a 50 Ω oscilloscope load in mind. In addition to the standard supply voltage, the output buffer also required a 100 μ A bias current, which could be provided from an external supply. Alternatively, an on-chip current source, based on the BGR in [77], was available. The voltage applied to a MOSFET switch determined whether the internal supply was used.

For this relatively simple circuit, the most important indicator of performance is

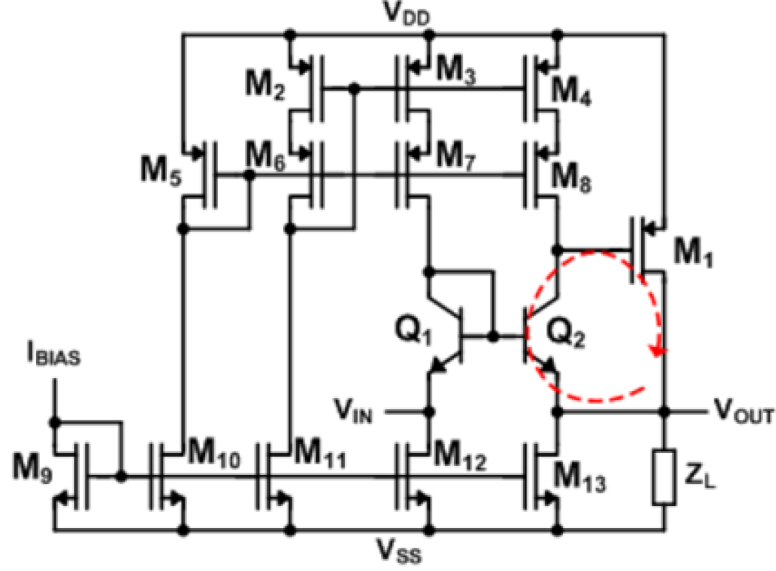


Figure 49: Circuit topology for the low-impedance output buffer with shunt feedback (after [78]).

the ability to generate a one-to-one match between the input and output signals across the widest possible input range. The DC transfer characteristic captures these fundamental performance metrics, and the experimental results across temperature are shown in Fig. 50 using the on-die current source. Impressively, the buffer experienced virtually no change in behavior between room temperature and 300 °C; furthermore, there were no stress-related effects on the circuit after short-term exposure to 300 °C. The continued lack of damage due to short-term exposure in bulk-SiGe circuits is very encouraging. In addition, these results also indicate the internal current source functioned properly, rendering the ability to provide an external source unnecessary.

The minimum and maximum output voltages in Fig. 50 were also largely temperature independent. For a grounded input, V_{OUT} remained well below 100 mV, and the maximum V_{OUT} remained just above 2.1 V across the entire temperature range. Input leakage currents did increase from 1.8 μA to 7.4 μA , but these levels are still acceptable for a high input impedance circuit. From a power consumption standpoint, the buffer required 151 mW to drive a 50 Ω load with the input at mid-rail; however, less than one-third of this power was consumed (45 mW) with no load

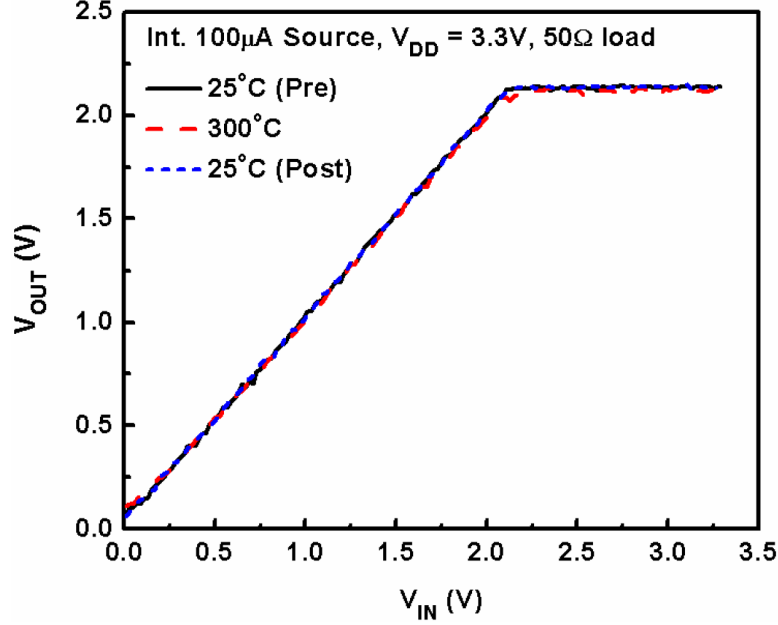


Figure 50: DC transfer characteristic for the SiGe output buffer across temperature with 3.3V VDD, 50 Ω load, 100 μ A internal current source (after [78]).

attached (high-Z output). Both load conditions showed little to no variation in power consumption with respect to temperature. The onboard current source, which drew only 12.1 mW at 25 $^{\circ}$ C, required only 1 mW of additional power at 300 $^{\circ}$ C.

With excellent DC characteristics over temperature established, the next step was to examine the AC performance. Simulations predicted a -3dB bandwidth on the order of several hundred MHz, but unfortunately, the high temperature stations measurement capabilities were limited to approximately 10 MHz. With this limitation in mind, the frequency response of the output buffer is shown in Fig. 51, confirming that the circuit functioned as expected over the system-limited frequency range. The circuit did demonstrate a minor 0.1 dB decrease in gain at 300 $^{\circ}$ C which was not present in the DC characteristics and is likely due to a calibration error during measurement.

An attempt to measure the step response of the output buffer was made; however, the system bandwidth limitations proved to be a problem. According to Cadence simulations, settle times were on the order of several nanoseconds well beyond the

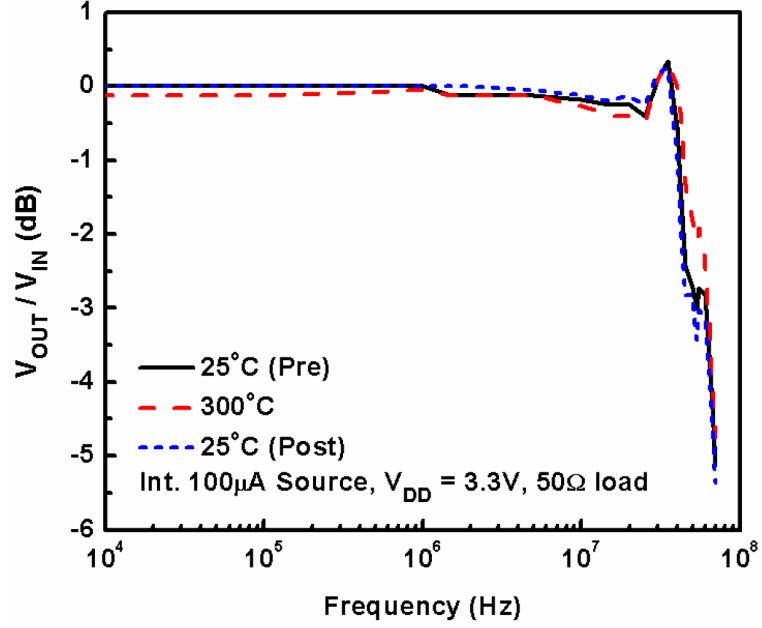


Figure 51: System-limited frequency response of the SiGe output buffer across temperature using on-die 100 μA current source (after [78]).

experimental capabilities of the high temperature system. These results should not be a concern except for circuits that are pushing the upper limits of the buffers frequency range. Both DC and AC FoM are summarized in Table 6 for the output buffer with a 3.3 V power supply (V_{DD}).

In addition to the standard 3.3 V power supply specified for the SiGe BiCMOS technology under investigation, the output buffer circuit could be overdriven to accept a higher range of input signals by applying a 5 V supply. The maximum output voltage was extended beyond 3.3 V across the 300 °C temperature range, and as expected, the power consumed increased proportionally for a mid-rail input. Simulation and measurement results for the primary FoM were in good agreement and are summarized in Table 7. Further work to establish the reliability with a 5 V supply should be undertaken in order to fully qualify the output buffer under these conditions.

Table 6: Measured and simulated FoM for the SiGe output buffer with 3.3 V V_{DD} , internal 100 μ A current source, and 50 Ω load unless otherwise specified (after [78]).

Parameter	Measurement		Simulation		Unit
	25°C	250°C	25°C	250°C	
3dB Bandwidth, f_{3dB}	>40	>40	432	175	MHz
Quiescent Current ($V_{IN} = 1.65$ V)	45.8	48.0	46.7	46.3	mA
Quiescent Current ($V_{IN} = 1.65$ V, No Load)	13.8	16.4	14.0	13.9	mA
Input Current ($V_{IN} = 1.65$ V)	1.8	7.4	0.9	38.6	μ A
Int. 100 μ A Source Power Consumption	12.1	13.1	1.5	1.6	mW
$V_{OUT,MIN}$	44	79	39	63	mV
$V_{OUT,MAX}$	2.14	2.12	2.17	2.13	V
$V_{OUT,MAX}$ (No Load)	2.40	2.74	2.41	2.72	V

Table 7: Measured and simulated FoM for the SiGe output buffer with 5.0 V V_{DD} (after [78]).

Parameter	Measurement		Simulation		Unit
	25°C	250°C	25°C	250°C	
Quiescent Current ($V_{IN} = 2.5$ V)	62.6	64.9	64.0	63.5	mA
Quiescent Current ($V_{IN} = 2.5$ V, No Load)	13.9	16.6	14.4	14.1	mA
Input Current ($V_{IN} = 2.5$ V)	-26.3	-16.6	-53.9	5.9	μ A
$V_{OUT,MIN}$	83	144	48	75	mV
$V_{OUT,MAX}$	3.57	3.45	3.70	3.60	V
$V_{OUT,MAX}$ (No Load)	4.09	4.43	4.11	4.40	V

4.4.3 Bandgap Voltage Reference

Precision voltage references are a key primitive building block for analog and mixed-signal circuit designs, and a temperature independent voltage source is a prerequisite for more complex electronic designs. A number of high temperature voltage reference circuits have been demonstrated over the past several years. Using silicon-on-insulator (SOI) or silicon carbide (SiC) processes, these circuits offer temperature limits ranging from 225 °C to 350 °C and beyond; however, both SOI and SiC are considerably more expensive compared to commercial Si [18], [71], [2], [19], [54]. These SOI voltage references, which a SiGe BGR could replace, demonstrate temperature coefficients

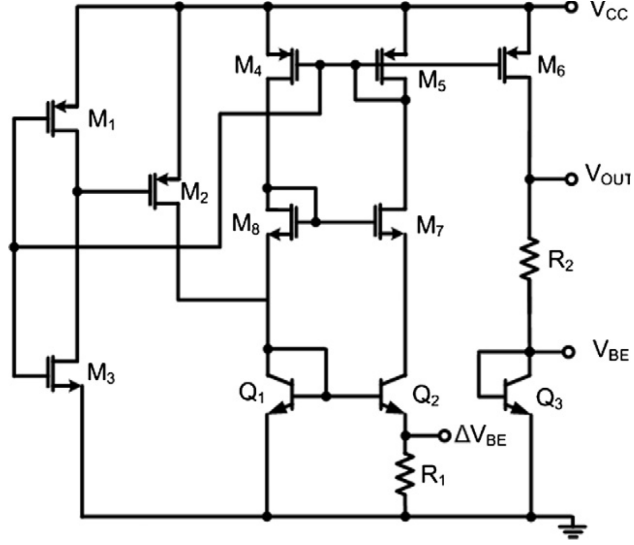


Figure 52: Schematic of a first-order (control) SiGe BGR circuit consisting of startup, PTAT current generation, and summing blocks (after [79]).

ranging from approximately 20 ppm/°C up to 100 ppm/°C.

In order to establish SiGe as a viable option for high temperature voltage references, a first-order BGR circuit, an example of which is shown in Fig. 52, was selected as a control BGR. This BGR is composed of three blocks: a startup circuit, proportional-to-absolute-temperature (PTAT) current generator, and a final summing stage. Transistors M_1M_3 form the startup block, and the PTAT current is generated by M_4M_5 , M_7M_8 , and Q_1Q_2 . The PTAT current is then mirrored into the summation stage by M_6 , which results in a linear, temperature dependent voltage across R_2 . This voltage combines with the inversely temperature dependent baseemitter voltage of Q_3 to produce a constant output voltage. Fig. 53 shows the output voltage across temperature. Even though this circuit was in no way optimized for high temperature operation, the output voltage remains flat to 200 °C, with a ΔV_{OUT} of only 10 mV. Above 200 °C, the output voltage rises rapidly, but the BGR remains operational and stable to 300 °C.

The successful operation of a voltage reference in a bulk-SiGe platform to such high temperatures is very encouraging; however, the rapid rise in output voltage

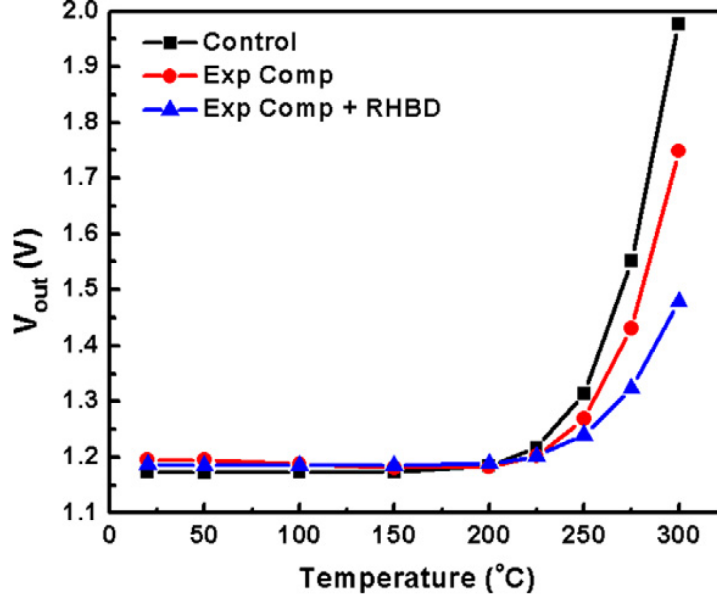


Figure 53: Output voltage of SiGe BGRs versus temperature. Using exponential compensation architecture and/or a device-level RHBD technique improves performance above 200 °C (after [79]).

above 200 °C warrants further investigation. If the underlying mechanisms driving this behavior can be identified, then design techniques at the device and circuit level could be explored to extend the useful operating range of bulk-SiGe technology. By combining the baseemitter voltage of a bipolar transistor with a PTAT current, the output voltage for the first-order BGR circuit is approximated by Eq. 4.1

$$V_{OUT} = V_{BE} + \Delta V_{BE} \frac{R_2}{R_1} \quad (4.1)$$

where V_{BE} , ΔV_{BE} , R_1 , and R_2 are defined in Fig. 52 [16]. As previously established, the PBDT resistors used for this circuit behave linearly across the entire temperature range, ruling them out as the cause of the output voltage rise. In Fig. 54, the measured values for V_{BE} and ΔV_{BE} , which represents the generated PTAT current, are linear across temperature, and they show good agreement with Cadence simulations. Unfortunately, those same simulations do not reproduce the behavior of V_{OUT} above 200 °C, complicating matters considerably; however, the circuits current

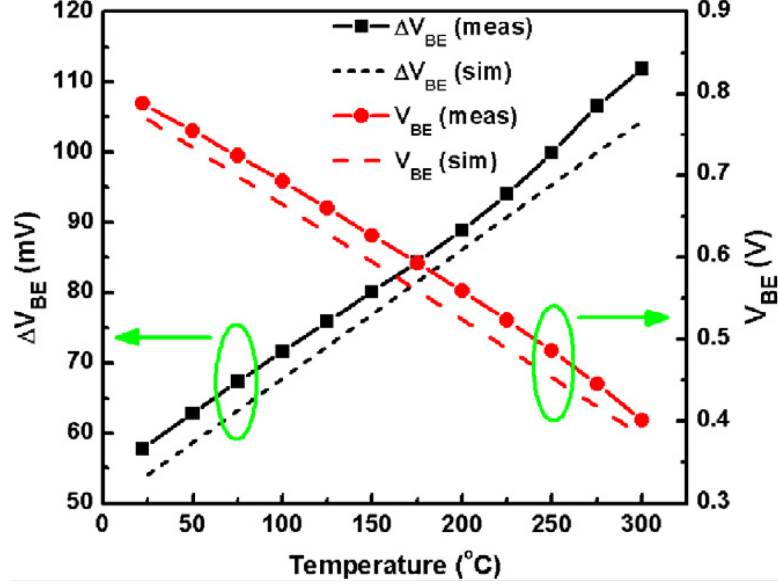


Figure 54: Comparison of key simulated and measured internal BGR voltages over temperature, all of which demonstrate acceptable linearity (after [79]).

draw provides a clue about those underlying causes. A rapid rise in both substrate leakage and ground current occurring simultaneously with the V_{OUT} increase was identified in [77]. These currents indicate the collector current in the output stage of the BGR (i.e., the current flowing through R_2) is no longer changing linearly with temperature, contributing to the increase in output voltage. Although the impact of substrate leakage was expected at high temperatures, the reason for the rise in current through the ground terminal was difficult to determine. One hypothesis is a failure of the pFETs to accurately mirror the current from the PTAT generator to the output stage of the BGR. A second possibility is that ΔV_{BE} does not accurately represent the PTAT current once substrate leakage in Q_2 becomes significant at temperatures above 200 °C.

While the control (first-order) BGR demonstrates functionality up to 300 °C, Fig. 53 also shows the results from two BGR circuits modified for improved performance across a wider temperature range using an exponential compensation architecture [30]. This circuit employs a three-stage design similar to the first-order BGR,

except it utilizes the inverse temperature dependence of the SiGe HBTs current gain to compensate for the higher order terms in V_{BE} . Additional SiGe HBTs are connected to the summing stage to create a feedback loop through the base connections. The result is a reduced temperature variation with comparable layout area and power consumption compared to a first-order BGR.

With exponential compensation, the SiGe BGR has been shown to achieve a 49.8 ppm/°C temperature coefficient over a 200 °C range, from room temperature to 180 °C [31]. Furthermore, the same BGR architecture extends the useful operating temperature up to 225 °C ($\Delta V_{OUT} \approx 13$ mV) and reduces V_{OUT} from 1.977 V to 1.749 V at 300 °C. A third BGR that combined exponential compensation with the transistor level RHBD n-ring technique to suppress leakage was also characterized. This BGR demonstrated the best high temperature performance, with ΔV_{OUT} equal to 2.2 mV at 200 °C and a further reduction in V_{OUT} at 300 °C to 1.479 V. With the simple addition of RHBD n-ring structures, the BGR improves its high temperature performance considerably at a very minor penalty to layout area.

High temperature applications require circuits that perform to acceptable specifications, but the effort is wasted if the circuits fail prematurely during use. With the BGRs performance across temperature characterized, the long-term reliability of the BGR with exponential compensation was investigated next. An initial test of approximately 150 hours at 300 °C showed minimal to no degradation in V_{OUT} ; however, there was concern over the suitability of the packaging technique die bonded directly to PCB for long-term expose to such high temperatures. Several of these packaging materials were not specified for extreme high temperature operation, including the Rogers 4003 laminate and silver epoxy die attach. For the second reliability experiment, a ceramic dual in-line package and Au₈₈Ge₁₂ eutectic die attach were utilized to minimize the likelihood of packaging degradation or failure. After 250 hours of continuous operation at 300 °C, the output of both BGRs had increased by only 0.6%,

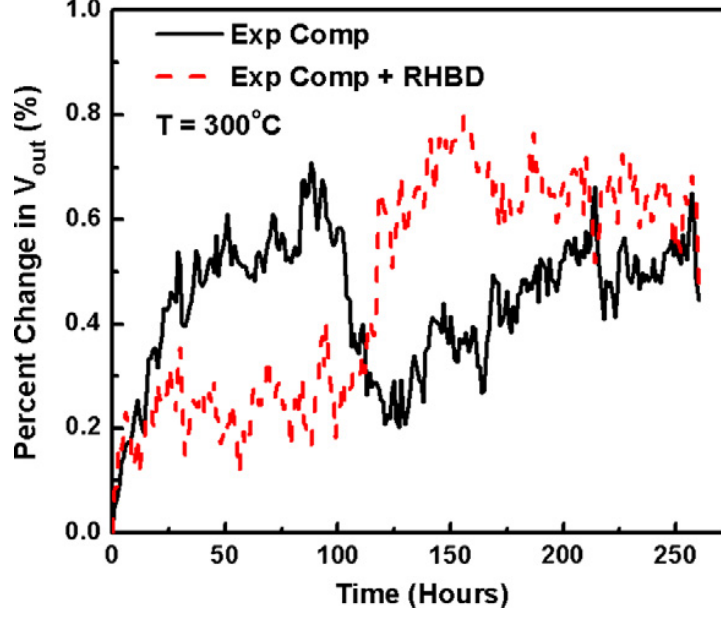


Figure 55: Reliability testing results for the SiGe BGR circuits in continuous operation at 300 °C for over 250 hours indicate very limited drift in V_{OUT} (after [79]).

as shown in Fig. 55. The circuits remained powered on for the duration of the test, with data samples collected every 30 seconds, which were then averaged into 1 hour data points for ease of viewing. Common failure mechanisms in high temperature environments, such as electromigration in interconnects or intermetallic voiding of the wirebonds, were not observed [26].

4.5 Summary

This work has demonstrated the potential of a bulk-SiGe BiCMOS platform for designing circuits that can operate successfully in environments with ambient temperatures up to 300 °C. Two classes of existing SiGe amplifier circuits, an operational amplifier for large capacitive loads and an output buffer, were shown to operate at very usable performance levels in high temperature environments. Using an existing transistor level RHBD technique, leakage currents were suppressed directly, demonstrating a promising device layout for applications requiring wide-temperature and radiation-tolerant behavior. The bandgap reference circuit, a critical building block

in many analog systems showed negligible degradation after 250 hours of continuous operation at 300 °C. These results lend further support to the case for SiGe technology as a suitable platform for ultra-wide temperature range applications.

CHAPTER V

CONCLUSION

This thesis has assessed the potential of silicon-germanium (SiGe) technology for use in extreme environment applications. The research covered in the previous chapters has shown that SiGe BiCMOS is an excellent platform for cryogenic, high temperature (up to 300 °C), and radiation intense environments.

5.1 Contributions

Chapter 3 detailed a study on the total dose and transient response of an uncharacterized, highly-scaled fourth generation SiGe BiCMOS process. HBTs exhibited TID-hardness up to 3 Mrad(SiO₂), improved DC and AC performance, and reduced device-level transients over previous IBM SiGe BiCMOS technologies. Comparisons across several SiGe BiCMOS generations reveal a strong correlation between device scaling and TID response. The results in chapter 4 were published in the Radiation Effects Data Workshop (REDW) at the 2012 IEEE Nuclear and Space Radiation Effects Conference (NSREC) [36].

Chapter 4 focused on high temperature operation and reliability of SiGe BiCMOS. The devices and circuits characterized were in no way optimized for high-temperature performance, but results show that the Ge grading present in SiGe HBTs helps mitigate thermal runaway issues. All SiGe circuits demonstrated reliable operation at elevated ambient temperatures with minimal deviations from room temperature behavior. By incorporating n-ring RHBD techniques, high temperature performance is improved by providing an alternate path for excess charge carriers. The results in chapter 3 have been accepted into two separate publications: the 2010 International

Conference on High Temperature Electronics (HiTEC 2010) [78] and Solid-State Electronics [79].

5.2 *Future Work*

While the results presented in this thesis are a good indicator of SiGe's suitability for applications requiring wide-temperature or radiation-tolerant electronics, there are still unanswered questions that warrant investigation. Chapter 3 suggested a possible improvement in SEE for circuits/systems incorporating these highly-scaled devices, but the experimental hardware raised an uncertainty in the exact energy deposition within the SiGe HBT. TID and TPA measurements on commercial IBM 9HP hardware are needed to confirm these suggestions. Heavy-ion broadbeam bit error rate (BER) testing of IBM 9HP master-slave (M/S) shift registers are also needed to verify the potential SEE benefits from this technology.

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