ON THE EFFECTS OF TOTAL IONIZING DOSE TO THE SINGLE-EVENT TRANSIENT RESPONSE OF A SILICON-GERMANIUM BICMOS PLATFORM

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ON THE EFFECTS OF TOTAL IONIZING DOSE TO THE SINGLE-EVENT TRANSIENT RESPONSE OF A SILICON-GERMANIUM BICMOS PLATFORM

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SUMMARY

The research presented in this thesis focuses on the radiation effects on Silicon-Germanium (SiGe) BiCMOS Technology. This study investigates the effects of total ionizing dose (TID) on the single-event transient response of both Complementary Metal Oxide Semiconductor (CMOS), and SiGe Heterojunction Bipolar Transistor (SiGe HBTs) devices. This document is organized as follows:

Chapter 1 provides an introduction to SiGe BiCMOS technologies, SiGe fabrication techniques, and methods of operation for both HBTs, and CMOS devices. Chapters 2 and 3 provide supplemental background information on the Earth and Jupiter's radiation environment and the radiation effects that SiGe BiCMOS electronics are exposed to for space based applications. Chapter 2 sets the stage with potential radiation environments, and radiation sources for extreme environment electronics. Chapter 3 addresses the effects of TID, displacement damage (DD) and single-event effects (SEE) on a SiGe BiCMOS platform.

Chapters 4, 5, and 6 include a study on the total dose effects on the transient response. TID testing and simulations are presented in chapter 4 and single-event transients (SETs) testing and simulations presented in Chapter 5. Chapter 6 contains a study presented by the author [29] and is pending publication in *IEEE 2016 Radiation Effects on Components and Systems (RADECS) Conference Proceedings* and to be submitted to *IEEE Transactions on Nuclear Science.*

Chapter 7 presents concluding remarks, the author's contributions and future work.

CHAPTER I

INTRODUCTION TO SILICON-GERMANIUM BICMOS PLATFORMS

This chapter provides background on transistor fundamentals and operation to provide the foundation of technical discussions in chapters to follow.

1.1 Motivation

Over the past 10 years, the satellite industry has experienced overall growth by a factor of 2.3 and currently thrives as a 200 billion dollar industry shown in Fig. 1. This growth is not only due to the betterment of aerospace, computing, and communications technologies, but also due to the ever-growing demand that the average person impresses on space technologies. Television, telephone, broadband, aviation, maritime, road, rail, agriculture, meteorology, and more industries depend on the continued operation of satellite telecommunications and observations. As each of these fields grows, the commercial satellite infrastructure will be required to grow as well, maintaining a constant demand for high quality space technologies.

SiGe technology provides performance improvements that, will enable lower design cost, higher performance, and longer life for these satellite systems in space environments.

SiGe has several advantages over Si CMOS relating to high frequency operation that are directly demanded by the telecom industry - f_T and f_{MAX} to be precise. As SiGe technology evolves, scales, and becomes more integrated, the telecom industry will be able to leverage the technology to design higher bandwidth communication systems that not only out-perform existing technologies, but also have a longer mean
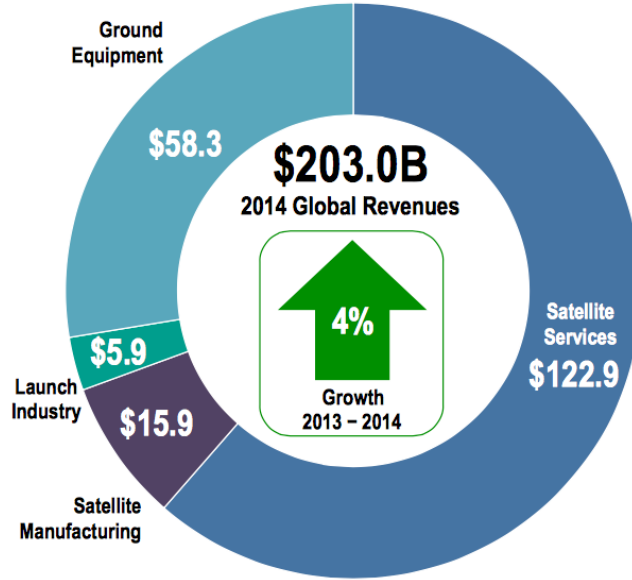
Figure 1: Satellite industry overview by sector (after [27]).

time to TID induced failure when used on space systems compared pure Si CMOS counterparts.

The use of SiGe technology has significant implications for space agencies considering both longer-range missions, where the electronics need to be operational for a relatively long time, and manned missions, where personnel safety is a concern.

Long-range exploration missions are crucially dependent on the behavior of electronics exposed to space radiation over a long period of time. These missions are designed to operate for tens of years. Designing electronics for space environments introduces unique challenges compared to Earth-based (or terrestrial) applications. New Horizons, the space probe that passed Pluto in July of 2015, was launched in 2005 and is expected to continue transmitting to Earth until the 2030s. Such a mission would not be possible without environmental hardening to protect the sensitive integrated circuits from space radiation.

As more ambitious and longer-range missions are conceived, environmental hardening will continue to be a large part of the design. The integration of SiGe technology

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provides as platform that will be a key aspect of designing long-range, long-lifetime space electronics.

What are perhaps the most ambitious and technically challenging space missions are those based around taking mankind into space. In particular, interplanetary manned missions have numerous scientific and technological hurdles that must be overcome before a launch is even considered. To support life in space we must not only focus on shielding the living human from space radiation for an extended period of time, but also all of the supplemental electronics and subsystems on a spacecraft that are equally crucial for the safety of the astronauts. With the current trend of engineers, physicists, and all bright minds working on these difficult space environment problems, it is not unreasonable to expect that one-day mankind will be an interplanetary species.

A deep and thorough investigation of the harsh effects of the radiation environment is crucial to the success of future missions. The following investigation analyzes the complex and synergistic nature of extreme radiation environments. SiGe platform can enable robust systems for space based applications [6]. Radiation hardness assurance in mixed radiation environments can be difficult, but is crucial to the longevity and performance of systems for space exploration.

1.2   SiGe BiCMOS Technology

Si CMOS has been the bedrock of the global electronics market. For the foreseeable future, there is no indication of this trend changing. However, Si CMOS is not the one-size fits all answer to IC design. While cost and simplicity is a main driving factor in Si CMOS IC design, SiGe platforms are still developed by over two-dozen companies in a diverse analog electronics market [4]. In particular, extreme environment electronics have created a market that lies outside of conventional commercial and military electronics. An advantage that the SiGe bandgap-engineered

Heterojunction Bipolar Transistor (HBT) plectronics. An advantage that the SiGe bandgap-engineered Heterojunction Bipolar Transistor (HBT) presents is the ability to operate at low temperatures and TID with minimal to no process modifications. An advantage SiGe holds over Si CMOS is linearity. That being said, voltage headroom for aresents is the ability to operate at low temperatures and TID with minimal to no process modifications. An advantage SiGe holds over Si CMOS is linearity. That being said, voltage headroom for a given supply voltage and breakdown voltage are driving factors to using HBTs in space environments [4]. The performance of the SiGe HBTs over the range of radiation and temperature variances is an advantage at the high performance circuits and systems [4]. Providing designers with devices and circuits that are TID tolerant would greatly influence the extreme environment electronics industry. The status quo in the space industry is to encase electronic components in bulky aluminum shielding. This inhibits the designer's ability to have a modular and distributed system. Having a centralized vault creates issues such as excessive wiring, increased weight, complexity, and the degradation of system reliability. The development of circuits with the capability to operate outside of the electronics vault will unchain the designers from this inhibiting design. Electronics capable of operating without shielding would enable the designers to reimagine the system design, and not be limited by the size, weight, and power consumed by the current electronics vault approach. TID tolerant high performance SiGe BiCMOS are excellent candidate for read out circuitry outside the bulky electronics vault. Researching the radiation effects on SiGe devices and systems is a crucial step to head towards the modular and distributed design in space systems. It is essential to address that SiGe BiCMOS circuits were not first designed for extreme environments. Current space-design engineers simply take advantage of the inherent pre-existing advantages of the bandgap-engineered SiGe devices. These advantages include both the ability to operate over a wide temperature gradient and being radiation tolerant a high total

ionizing dose level.

1.3 SiGe HBT Fabrication and Theory of Operation

A number of fabrication techniques have been developed that demonstrate the capability to introduce the germanium profile in SiGe devices. The most common methods to produce commercial SiGe HBTs are the ultra-high vacuum chemical vapor deposition (UHV/CVD), and atmospheric pressure chemical vapor deposition (APCVD). The film growth process can be broken down into two distinct phases, the first being preparation of the initial growth interface, the second being the film growth itself [5]. The surface being prepared is often unpatterned, bulk grown Si wafer. The absence of any subsurface patterning allows exposure to high temperatures without any damaging effects to the wafer. The UHV/CVD technique eliminates the need for higher temperatures by use of chemical means. The Si surface can be passivated by a wet chemical procedure. A 10-15 second etch in a 10:1 dilute of H_20/HF solution is used in this etching process [5]. The hydrogen adlayer created during the wet etch reduces the reactivity of the growth by approximately 13 orders of magnitude [5]. The wet etching process allows for the growth of the epitaxy at room temperature. The UHV step is used to achieve adequate film purity at low temperatures. The target range for the vacuum is 10^{-1} torr. The germanium profile is essential to the performance of the SiGe HBT devices. The gradient of Ge in the base is fundamental to the bandgap engineering of SiGe HBTs. Controlling the bandgap of the device is centered around the different lattice constant of the two elements, Si and Ge. Ge having a larger lattice constant than Si, is why Ge has a smaller bandgap energy of 0.66 eV as compared to the 1.12 eV of Si. The new SiGe alloy will have a shrinkage of the bandgap, and this is caused by compressive strain. The new offset in the bandgap, illustrated in Fig. 2 is predominately in the valance band, which is why this new alloy is suitable for the use in HBT transistors. The device is constructed in a fashion that the Ge is graded

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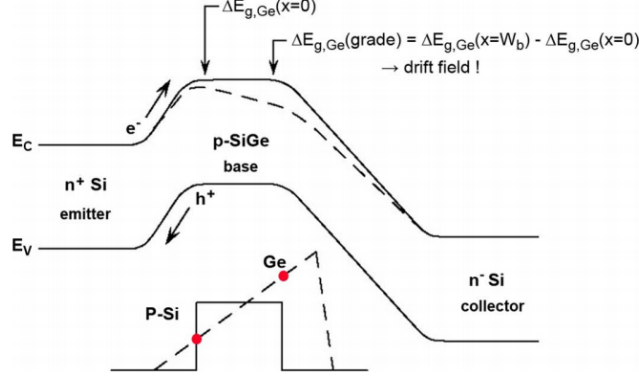
Figure 2: Comparison of the energy band diagram of a SiGe HBT vs Si BJT (after [4]).

linearly from 0 percent at the EB junction to a maximum value as the Ge approaches the CB junction, as seen in Fig. 3. Then, it is rapidly decreased back to 0 percent [4]. The compressive strains also lift the conduction and valence band degeneracies at the extremes of the band. This reduces the density of states and improves the mobility of the carriers by reducing the effect of carrier scattering.

To discuss the effects of Ge in the base region it is best to review the operation of a Si BJT. The forward bias applied is from V_{BE}, this causes the electrons from the emitter to be injected into the base region through the EB potential barrier. The electrons then diffuse through the base until they are swept into electric field of the CB junction. This phenomenon is what is referred to as collector current. Another aspect to take into consideration is the back injection of holes. The forward bias applied to the EB junction back ejects the holes form the base into the emitter region. If the emitter region is heavily doped as compared to the base region then the density of holes that are back injected will be small when compared to the density of electrons that are forward injected. This is why there is a finite amount of current gain [4]. Now to analyze the effect that Ge has in the base region, the resulting change in DC performance is due to the reduction in the potential barrier if the EB region is decreased. With a smaller EB barrier, we can infer that there will be more
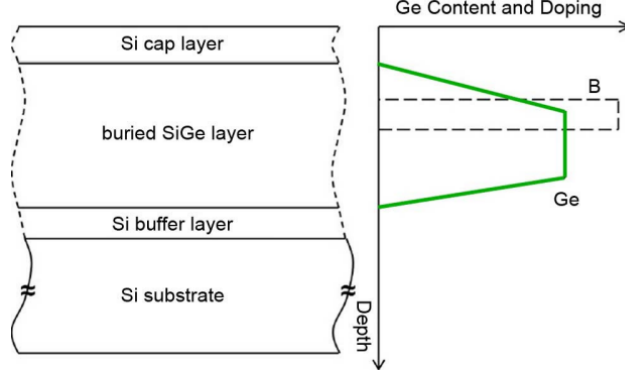
Figure 3: Shape and composition of the Ge profile in SiGe HBT(after [4]).

electrons injected for a given V_{BE}. With more electrons traveling between the EB barrier, there is a higher collector current and higher current gain. In Si BJTs the base doping is a major factor in the current gain. The collector current density is inversely proportional to the integrated base charge. This finite amount of Ge in the base region positively influences the output conductance of the transistor. The AC performance of the device is also improved by the presence of Ge in the base region. The injection of minority electrons across the base are accelerated due to Ge gradient-induced drift field across the base which is aligned from the collector to the emitter. The electron transport now has a larger component due to the larger drift field. This effect speeds up the diffusive transport of the minority carriers which, decreases the amount of time it takes the electrons to diffuse across the base region. The Ge influence on the drift field improves the frequency response of the device. The offset of the EB junction enhances the collector current density and consequentially the β . In addition to TID tolerance, and improved low-T performance, the AC and DC performance characteristics make the SiGe HBT a prime candidate for use in space applications.
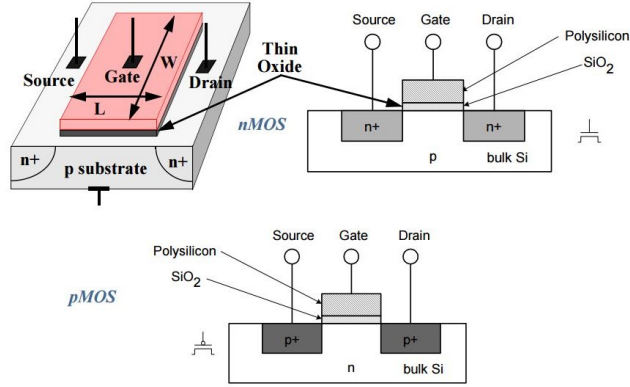
Figure 4: CMOS Cross Section for nMOS and pMOS transistors(after [28]).

1.4 CMOS Theory of Operation

This section provides an overview of the essentials of operation of the Silicon MOS-FET (Metal Oxide Semiconductor Field Effect Transistor). Understanding the modes of operations will provide insight on how radiation damage affects the single-event transient response of the CMOS device. CMOS devices are similar to the Si HBT in the fact that both devices use a third terminal to modulate the current flow of the first two terminals. The difference being the mechanism by which that occurs. Consider the following cross sectional view of the nFET device in Fig. 4. Where the n-channel MOSFET has a positively doped silicon substrate between two pn junctions formed at the interface of the Source-Substrate and Drain-Substrate interface. The source and drain are spaced by length L to form a channel that is referred to as the gate length. On top of this channel is an oxide . The flow of current between the drain and source terminals is controlled by a voltage applied to the gate terminal.

Three main modes of operation are observed with the nFET. the first mode being cut-off. This transistor is biased where $V_{GS} < V_{TH}$ i.e., the gate to source voltage is less than the threshold voltage of the device. The channel region in this bias condition contains an excess of holes or very few electrons [19]. Minimal current flows between the drain and source terminals due to the high resistance. The next operation region is
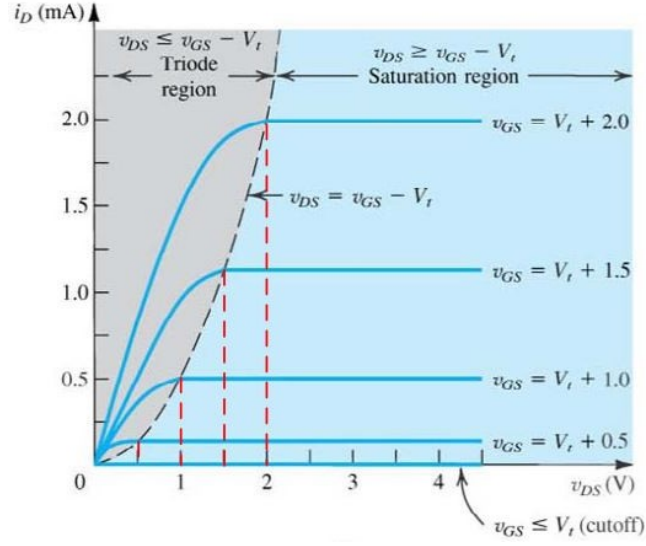
Figure 5: N-type MOSFET output characteristics (after [28]).

$V_{GS} > V_{TH}$ is inversely biased($V_{Gs} > V_{TH}$ and $V_{DS} < V_{GS}$ - V_{TH})the ohmic region, this leads to the creation of an inversion layer containing mobile electrons and is formed directly under the gate. This induced n channel connects the Drain to Source. Now turning our attention to the drain, as we slowly increase the drain voltage, the voltage drop from the drain to the source negates the inverting effect of the gate. The depletion region widens, as well as extends further into the substrate. As the depletion region extends, the number of carriers decreases the channel conductance and the channel Pinches off. As the drain voltage is greater than the pinch off voltage, the pinched off region of the channel absorbs most of the voltage drop in excess of of VD_{SAT}. This operating condition($V_{GS} > V_{TH}$ and $V_{DS} > V_{GS}$ - V_{TH}) is referred to as the saturation region as seen, in Fig. 5.

CHAPTER II

RADIATION ENVIRONMENT

This chapter serves as an introduction to the radiation environment that electronics for space based applications may be exposed to in their lifetime. Radiation sources and environments are discussed to provide background for technical discussions in later chapters.

2.1 Introduction

The development for the testing and design of extreme environment electronics is essential to the proper operation of electronics of electronics that are launched into space. These missions can range from communication satellites, remote sensing satellites, interplanetary space travel, and the exploration of the outer planets. The unfriendly environments of space, shown in Fig. 6, are detrimental to conventional electronic devices used in terrestrial applications. As tempting as it would be to only utilize commercial off-the-shelf components (COTS), these products can fail at an astonishing rate due to the total ionizing dose that occur to in the space environment [6]. At this time, it is not recommended to use COTS components in an exposed capacity in space, so the need for radiation hardened electronics is essential to the success of any space mission.

The ramifications of radiation-induced damage on space hardware are extensive, and the possibility of the loss of satellite functionality is a real risk. For example, an earth-orbiting system with an expected 10 year life span will be exposed to 1 $Mrad(SiO_2)$ of radiation by the end of the mission [6]. In comparison, exposure to a total ionizing dose of 200-300 $krad(SiO_2)$ will kill a human. This highlights the resilience needed in modern electronics design. Furthermore, this highlights the need
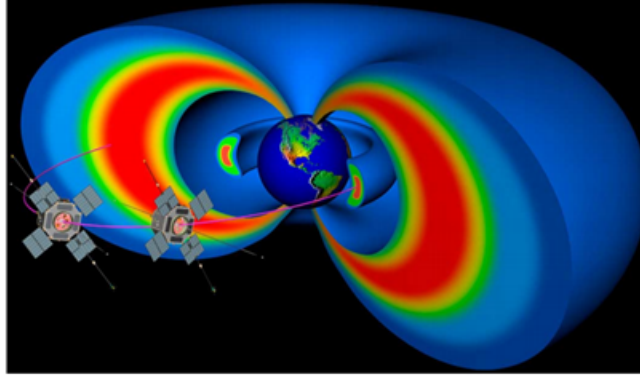
Figure 6: An illustration of the radiation belts encountered by orbital satellite systems(after [6]).

to research, understand, and test for radiation damage in any new technology or design that will be exposed to these harsh environment.

There are multiple forms of radiation that must be accounted for in the design of extreme environments electronics. The three major classes to address are: total ionizing dose (energized particles that ionize materials that they pass through), displacement damage (highly energized particle that displace atoms in the lattice), and single-event effects (can cause burnout of gate oxides, destructive latch-up, digital bit flips, and error propagation) [4].

2.2 Solar

The solar radiation environment is influenced by the 11-year solar cycle, which consist of 7 years of increased solar activity (solar maximum) and 4 years of decreased solar activity (solar minimum). Solar events typically include solar flares and Coronal Mass Ejections (CMEs). The level of solar activity directly influences the flux of Galactic Cosmic Rays (GCRs) that interact with the Earth's radiation environment, both of which will be discussed in following sections. Solar flares are a result of the coronal magnetic field. Once the magnetic field reaches a critical magnitude release the energy over the span of a few hours. CMEs are larger eruption of plasma that occurs over a few days. This eruption produces a wave of accelerated particles [31]. CMEs are also
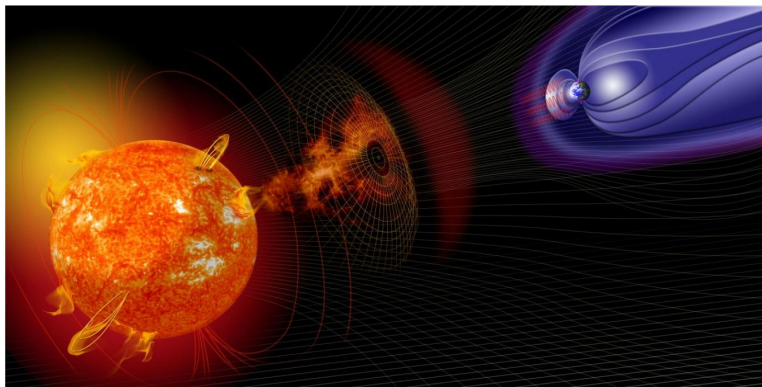
Figure 7: An illustration of a solar coronal mass ejection (after [30]).

responsible for geomagnetic disturbances on Earth.

2.3 Galactic Cosmic Rays

Galactic Cosmic Rays originate from outside of our solar system. These highly energetic particles (GeV and higher) are thought to originate from Supernovas. Protons, electrons, and ionized nuclei are the contributing highly energetic particles. Particles with energy at this level are difficult to stop with typical shielding techniques used in space-based applications. GCRs with less than 10 GeV/amu of kinetic energy are influenced by solar activity. As the solar cycle reaches solar maximum the flux of GCRs decreases. These highly energetic particles are also a concern terrestrially. As the GCRS collide with the Earth's magnetic field and trapped particle environment, the particles generate atmospheric neutrons.

2.4 Earth's Trapped Radiation Environment

The very first American satellite, Explorer 1, was crucial in the discovery of the Earth's trapped radiation environment. Data from this mission was used to confirm the existence of charged particles that were trapped by the Earth's magnetic field. There are two main components of the earths trapped radiation , known as the Van Allen belts. The outermost magnetic field is comprised of charged particles. The magnetic field is a result of current flow in the liquid outer core of the Earth. The

field can be approximated as a magnetic dipole tilted 11° from the north-south axis [16]. The field strength maximum is at the magnetic poles and the minimum is occurring at the magnetic equator. As charged, particles , specifically from CME and solar flares, interact with the magnetic field, the Van Allen belts dynamically react and fluctuate in response to the flux of solar activity. The dynamic Van Allen belts are illustrated above in Fig. 6. The Outer belt resides at approximately 4-5 Earth radii [31].

2.5 Jupiter's Trapped Radiation Environment

Electrical upsets on both the Pioneer and Voyager spacecraft have led to and further research into the Jovian radiation environment [14]. This charged environment has become a driving factor in mission planning, and spacecraft design. The three major factors that shape the Jovian Charging environment are: its magnetic field (with 11° relative to its spin axis), its rapid rotation, and the Jovian moon Io which generates a torus of neutral gas and cold plasma [12]. The first Jovian radiation environment publication dates back to Divine and Garrett, *Charged Particle Distributions in Jupiter's Magnetosphere*, published in the Journal of Geophysical Research in 1983. The Garrett review paper [12] breaks the Jovian charging environment into three categories: background plasma, high-energy electrons, and magnetic field. The Jovian magnetic field is approximately $20\times$ larger than Earth's. Strong magnetic fields provide the capability to retain charged particles at much higher rates than Earth. The Jovian rotation rate is an important factor for plasma dynamics, as this determines the velocity at which the cold plasma impacts the spacecraft surface. Another key aspect of the Jovian charging environment is the additional source of cold plasma, Io at 5.9 Jovian radii. This source alters the magnetic field at the equatorial plane as seen in Fig. 9. The Jovian background environment is characterized by three categories: low-energy plasma (ionospheric plasma 1-100eV), the Io torus, and the plasma disk.

$$A_n = a_n + (b_n - a_n)\,\frac{3(c_n - 1)^2 x + 3c_n(c_n - 1)x^2 + c_n^2 x^3}{3 - 9c_n + 7c_n^2}$$

L	a_0	a_1	a_2	a_3	b_0	b_1	b_2	b_3	c_0	c_1	c_2	c_3	D_2	D_3
1.089	6.06	0.00	0.00	4.70	6.06	0.00	0.00	4.70	0.00	0.00	0.81	0.50	2.0	30.0
1.55	6.90		0.30	4.30										
1.75	7.34		0.57	3.98										
1.90	7.00		0.47	4.38	6.51			5.42			0.83			
2.00	7.36		0.75	3.65	6.26			4.76			0.68			
2.10	7.29		0.69	3.41	6.33			4.79			0.70			
2.40	7.31	0.72	0.67	4.15	5.91			5.21		0.58	0.14	0.18	0.7	26.0
2.60	7.33	0.96	0.69	4.24	5.79			4.85		0.55	0.06	0.00		
2.80	7.39	0.76	0.59	2.65	5.86			6.09		0.56	0.36	0.35	0.2	22.0
2.85	7.44	0.80	0.60	2.65	5.80			6.09		0.56	0.37	0.35		
3.2	7.00	1.32	0.53	2.65	5.89			6.09		0.49	0.40	0.35		
3.6	6.91	1.37	0.51	3.51	5.75			6.70		0.58	0.49	0.35		
5.2	6.21	1.70	0.48	4.93	5.80		0.34	4.28		0.56	0.00	0.50		
6.2	6.37	1.33	0.00	2.27	6.33		1.66	3.07		0.56	0.13	0.40	1.0	10.0
7.2	6.39	1.07	0.02	3.02	6.12		1.82	3.56		0.32	0.06	0.40		
9.0	6.60	0.65	0.54	3.60	5.63	0.65	2.07	2.00		0.00	0.59	0.47		
10.5	7.23	0.59	1.95	2.23	5.73	0.93	2.71		0.55	0.00	0.62	0.56		
11.0	7.07	0.92	2.00	2.00	5.56	0.82	2.82		0.56	0.57	0.47	0.00		
12.0	6.76	0.95	2.13		5.00	1.20	2.99		0.58	0.26	0.37			
14.0	6.67	0.20	2.90		3.34	2.86	1.01		0.62	0.65	0.00			
16.0	4.44	0.89	0.90		5.86	0.76	7.95		0.00	0.26	0.70			

Figure 8: Parameter value for the Jupiter electron model (after [13]).

The low energy electrons are dominated by the torus ejections from Io. The complex aurora environment can also contribute three factors: a narrow aurora zone above $\approx$ 60 ° latitude in the northern and southern polar regions, a broad region of diffuse aurora over the polar caps, and the aurora footprint associated with the **velocity** $\times$ **magnetic field** field [12].

The compact and quantitative model of charge particle distribution between 1 eV and several MeV was first presented by Divine and Garrett in 1983. Data for the model was primarily taken from experimental results of the Pioneer and Voyager spacecraft, and the data were supplemented by earth-based radio frequency observations.

The successful missions to Jupiter up until 1983 were able to begin the development of the model of the magnetic fields, high-energy particle fluxes and the confirm the thin magnetodisk. The time-averaged charged environment modeled by the Divine-Garrett model is able to accurately represent the intensity, number density, connection speed, and temperature for high-energy and thermal plasma populations within a factor of two [7].

The GIRE update is a quantifiable improvement to the Divine-Garrett model.
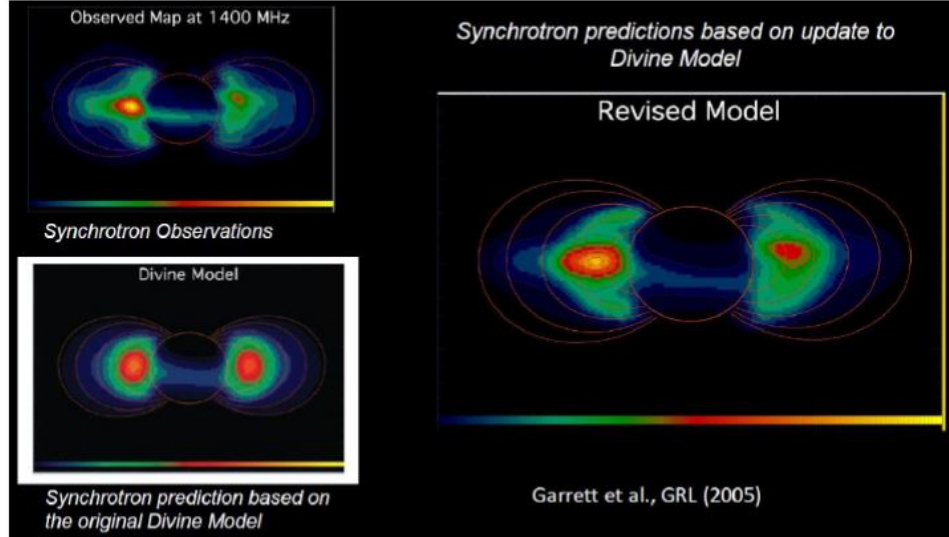
Figure 9: Update to the Divine-Garrett Model in the L < 4 R_J region using Earth-based ultra high frequency (UHF) radio observations (after [13]).

The GIRE update improves the high-energy electron model from the ranges of 8-16 L-shells by incorporating in-situ data from the Energetic Particle Detector (covering energy ranges from 0.1 MeV to 30 MeV) from 35 Galileo orbits. The Synchroton update improved the Divine-Garrett model in the L < 4 region using earth-based radio observations as seen in Fig. 9.

CHAPTER III

RADIATION EFFECTS

3.1 Total Ionizing Dose

Total Ionizing dose (TID) effects are usually associated with the damage to semiconductor-dielectric interfaces when energy deposited by incident photons or high-velocity charged particles produces traps, or induces incomplete bonding at surfaces that generally will lead to excess leakage currents. In SiGe HBT results in degradation in the base current and causes a current gain reduction at low injection. Fig. 10 depicts the sensitive volumes of a SiGe HBT semiconductor-dielectric interfaces that are susceptible to charge build-up.

The study of ionizing radiation on SiGe devices has been popular topic in publications and attracted significant interest, since SiGe devices are inherently TID hardened. This ionizing radiation causes the buildup of charge in oxide-silicon interface of the HBT. Buildup of charge on the oxides is a result of the exposure to high-energy electrons (electrons present in the environment and secondary electrons that are generated from photon interactions), and protons that ionize the atoms generating electron-hole pairs [23]. The space environment places these SiGe devices in a high flux of electrons and protons that greatly reduce the device performance as well as the lifetime of the device. If the energy of the electrons is greater than the energy needed to create electron-hole pairs, then the incident electrons can create additional electron hole pairs.

The accumulation of the acceptor traps will occur in the oxides [8]. The regions that are the most susceptible are the EB spacer, and the shallow trench isolation edge shown in Fig. 10. The trapped holes in the oxide produces excess base leakage
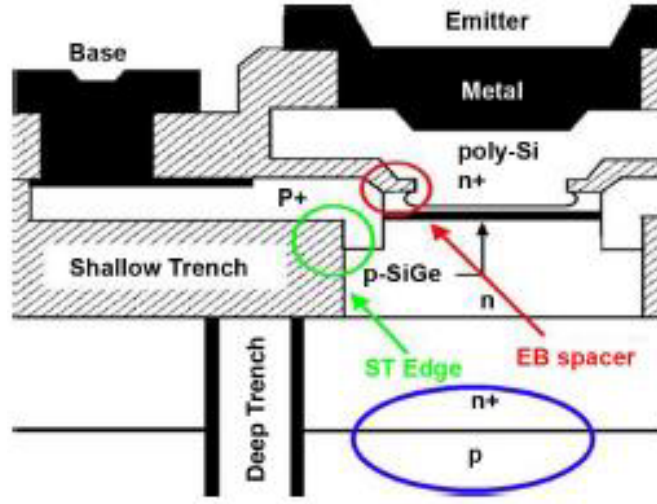
Figure 10: Schematic cross-section of a commercial SiGe HBT, indicating the damage points associated with the emitter-base (EB) spacer and the shallow trench (STI) edge. Also shown the n^+ - p^- (after [6]).

current. Such traps act as recombination centers when located within the EB space-charge region, producing parasitic base current leakage and current gain degradation [5]. The device structure of the SiGe HBT makes the device more tolerant compared to FETs. The SiGe HBT has three features that harden the device by design: (1) The EB spacer is very thin (approximately 100 nm) and is contained within the heavily doped region of the epitaxial base; (2) the base is also very thin (approximately 100 nm) and heavily doped; (3) the shallow trench isolation in the collector base junction is very thin and well away from the core transport path of the transistor [6].

FETs TID response differs from its HBT counterpart. FET TID damage include: shifts in voltage threshold, increased off-state leakage, parasitic leakage paths, mobility degradation and, changes in recombination at the interface.

The dependency on gate thickness plays a crucial role in the ability of the gate oxide to trap charge. Saks investigated this dependency [22] and discovered there was a strong decrease in radiation-induced hole trapping as seen in Fig. 11 at 80 K for thicknesses below approximately 10 nm. Below this thickness, the decrease in hole trapping is more rapid than the established approximately t_{ox} dependence for thicker

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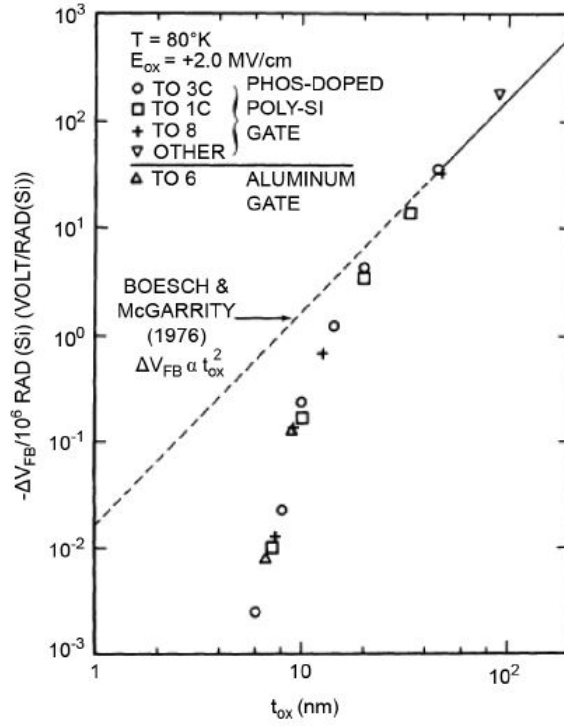**Figure 11:** Voltage shift per $Mrad(SiO_2)$ for MOS capacitors irradiated with Co-60 gamma rays at 80K, as a function of gate oxide thickness. The dashed curve is the extrapolation to thinner oxides assuming that the usual oxide-thickness-squared dependence of oxide thickness from Boesch and McGarrity (after [22]).

oxides. The stark decrease is credited to the trapped holes within approximately 3 nm of either gate-SiO_2 or Si-SiO_2 interface via tunneling [1]. Ultra-thin gate oxides have become less of a factor when considering TID radiation tolerance.

Another important study on MOSFETs is the effects of dose rate and post-irradiation annealing time [15]. Worst case bias conditions were applied to the FETs as the transistors dose-rate was adjusted from 0.165 (SiO_2) with Cs-137 to 6×10^9 rad (SiO_2)/2 using a linear accelerator (LINAC). Fig. 12 illustrates that threshold-voltage shifts due to oxide and interface traps charge were found to be similar for low-dose-rate irradiation and high-dose-rate irradiation, assuming that were both followed by biased annealing for an equivalent time [9]. These finding demonstrate that both low and high dose-rate sources, given the same positive annealing bias and time, demonstrates that MOSFETs do not have the dose-rate effect as seen in BJTs.

With the integration of ultra-thin gate dielectrics, the study of ionizing dose on MOSFETS transitioned to the oxide isolation, Silicon on Insulators (SOI) and advanced technologies including high-k dielectrics. Corner and edge shunt leakage paths have been a focus of TID studies for approximately 20 years. This is where the shunt leakage path caused by radiation induced traps along the STI-Si can lead to trap assisted tunneling current [3].

The defects at the oxide interface are caused by proton transport and reactions. This interaction was investigated and calculated by Rashkeev and Pantelides [18] [20] by calculating the density functions. As a proton approaches the SiO_2 barrier it encounters a 1 eV barrier as it attempts to enter the Si [18] . Fig. 13 illustrates the potential well that is formed. These traps can reach equilibrium by a tunneling electrons or the proton can react with directly with a Si-H or (Si-OH) at or near the interface. To form an interface trap as seen in Fig. 14.

This damaged interface of the Si/SiO_2 is demonstrated in Fig 19. This top view of a nFET illustrates overlap of the gate oxide over the shallow trench isolation
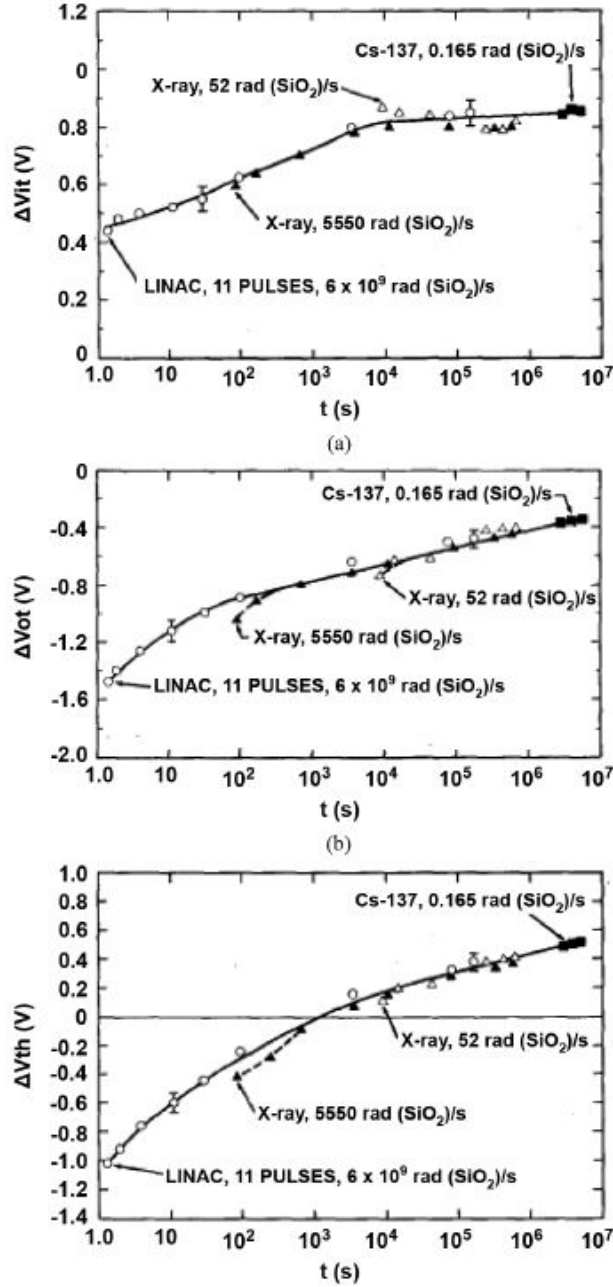
Figure 12: Threshold-voltage shifts to (a) interface-trap and (b) oxide-trap charge, and (c) net threshold voltage shift as a function of irradiation and room temperature annealing time for nMOS transistors with 32-nm oxides irradiated to 500 krad(SiO$_2$) at an electric field of 2 MV/cm with 20-MeV electrons at approximately 6×10(to the 9) rad(SiO$_2$)/s, 10-keV X-rays at approximately 52 to 5550 rad(SiO$_2$)/s and Cs-137 gamma rays at 0.165 rad(SiO$_2$)/s) (after [9]).

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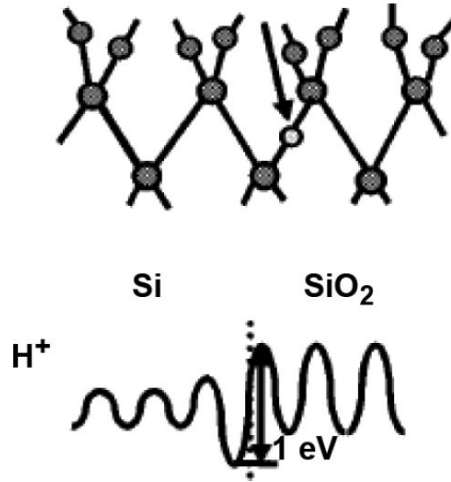
Figure 13: (top) Transporting H+ approaching an abrupt (defect free) Si-SiO$_2$ interface, and (bottom) potential energy well experienced by the H+ in the vicinity of the interface (after [18]).
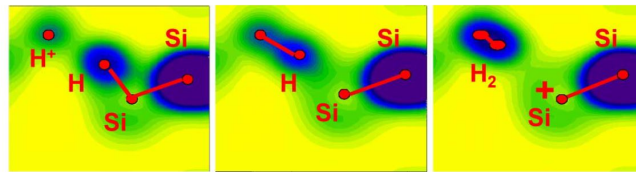
Figure 14: Electron density as a function of the position of a transporting proton as it approaches the Si/SiO$_2$ interface: (left) The proton is positively charged until it is sufficiently close to form (middle) an H+ - H - Si bridge structure, which then resolves (right) into an H$_2$ molecule and dangling Si bond (Pb defect) at the interface (after [20]).

which provides a shunt leakage path. A shunt leakage path between drain and source increases off state leakage as a function of increasing TID (with a positive bias applied to be in worst case conditions).

3.2 Displacement Damage

Atomic displacement can occur through an ionizing and non-ionizing process as energetic particles pass through a given material. The energy lost by the ion produces electron-hole pairs and displaces atoms in the Si lattice structure [25]. The lattice damage is a result of movement of atoms from their normal lattice structure to an interstitial structure. The vacancy left behind and the new interstitial atom are referred to as a Frenkel pair. The energy needed for an incident particle to cause displacement damage to the lattice is approximate 1 MeV for a typical incident electron or neutron.

There are different aspects of the damage causes: 1) incident ion displacing atoms, 2) the defects give rise to new energy levels in the band gap, 3) the altered energy levels alter the material and device electrical and optical properties, 4) recombination of electron-hole pairs in unintended regions, 5) temporarily trapping of carriers, 6) tunneling of carriers through a potential barrier through the defect level, 7) incident ions act as scattering centers and cause the carrier mobility to decrease [25].

3.3 Single-Event Effects

Single-Event effects (SET) are caused by a high-energy particle passing through the material and generating electron-hole pairs. SET is the umbrella term used to describe several destructive and non-destructive effects. Destructive effects include: single-event latch up (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR). The non-destructive effects include: single-event upsets (SEU), multiple-bit upsets (MBUs), single-event transients (SETs), and single-event functional interrupts (SEFIs).

Single-Event Upsets are a large concern for CMOS circuitry. An example being
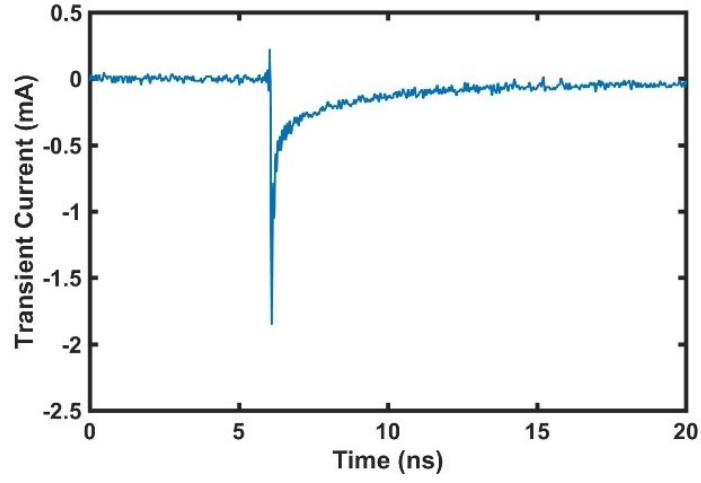
Figure 15: Measured collector output current for the 3rd-generation SiGe npn under forward-active bias (V_{CE}=1 V, V_{BE}=1 V).
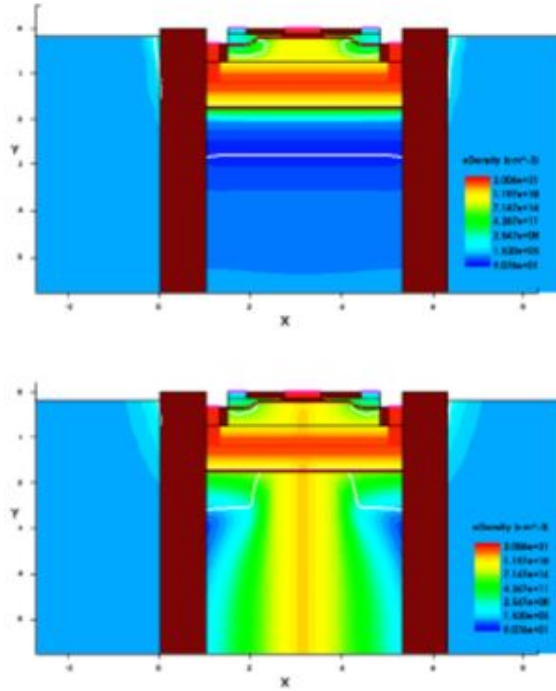

Figure 16: 2D nFET Syntaurus model heavy ion strike simulation.

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a heavy-ion strike causes a bit to flip in a digital circuit. The SEU is characterized by the error cross section, which is the number of measured errors normalized to the effective fluence. This metric is typically measured as a function of LET. LET is defined as charge deposition per unit path length (pC/μm). Just as they are tolerant to TID they are very susceptible to SEEs, that are caused by highly energetic particles strike sensitive regions of the device in the EBC junction of the HBT. This heavy-ion strike can cause a transient disruption of the circuit operation, change of a logic state or cause permanent damage to the device [4]. The vertical device structure of the SiGe HBT exacerbates the effects of a heavy ion strike. If a heavy ion strike occurs at the EB junction of the device, the charge collection at this junction shorts out the terminals of the EB junction and the BC junction. This short produces a large quasi-resistive transient on the emitter, base, and collector terminals [6]. If any ion strike occurs within the deep trench isolation ring, the reversed bias sub collector to substrate junction forms an ideal collection point for the majority of the deposited charge from the heavy-ion strike into the substrate. This fast change in charge will drive a fast transient followed by a diffusion trial. Fig. 16 depicts a heavy ion strike in the EBC junction. The transient charge followed by the diffusion tail as seen in Fig. 15. There are two main features of a SET emitter centered strike, a large and quick transient caused by the shunt drift current, followed by a slower diffusion charge which is smaller in magnitude but larger in duration. The majority of the collected charge occurs during the diffusion portion of the transient.

While charge generation mechanisms are similar for a heavy-ion strike on a CMOS and HBT, the severity and single-event transient response differs between the two different types of transistors. Device geometry and operating principles play a large role in the differences between the single-event transient responses.

The CMOS transient current is a result of the heavy ion particle generating charge as it passes through the reverse biased junctions of the FET. The struck terminals
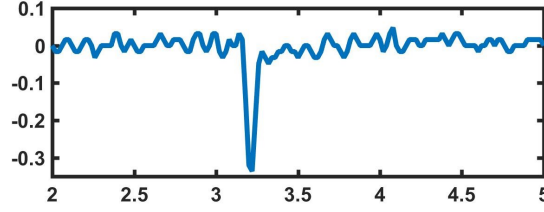
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Figure 17: Measured 2-D collector output current for the 3rd Generation SiGe nFET under bias (V_{DS}=1.5V, V_{GS}=1V).

then collect the transient charge as it passes through the material. The SET may propagate and induce a single-event upset if these four conditions are met: 1) the SET is generated at a sensitive logic node, 2) it propagates down an open logic path and arrives at a latch or other memory element, 3) it arrives with sufficient amplitude and duration to change the memory state and, 4) it arrives while the cell that is on i.e., when the clocking conditions enables the transient to be captured [8]. The transient current response consists of the two main mechanisms similar to the HBT single-event transient response with the fast drift current, that is large in magnitude and small in duration, and a slower diffusion tail, which is small in magnitude and longer. The transient peak of the drain terminal during a single event transient is seen in Fig. 17.

The size and shape of the transient duration differs when comparing a single CMOS transistor and a transistor that is integrate in a chain of logic cells. For transistors in a digital logic cell the transient duration can elongate. This phenomenon is known as propagation-induced-pulse broadening. This is caused by a hysteresis effect induced by charging or discharging of the internal floating body node because of the transistors recent bias history [8]. The previous bias of the transistors induces very small differences in the transistor threshold voltage.

CHAPTER IV

TOTAL IONIZING DOSE TESTING AND SIMULATIONS

4.1 Experimental Setup

The 8HP nFETs and SiGe HBTs were irradiated up to 2 Mrad(SiO_2) using a 10-keV X-ray source, at a dose rate of 60 krad(SiO_2)/s. The nFETs and SiGe HBTs were measured at intermediate doses immediately following irradiation. For all TID experiments, the FETs were biased to maximum rated gate voltage (worst case condition), and all SiGe HBTs were irradiated with all terminals grounded (again, worst case condition). The goal of this experiment is to analyze the effects of ionizing radiation to the DC performance of the SiGe BiCMOS platform.

4.2 Experimental Results

Fig. 5 depicts transfer characteristics for the nFET across multiple dose points. The lack of threshold voltage shift seen in Fig 5 indicates that there is very little net charge trapping in the gate oxide. Previous work indicates that this high leakage current is a result in the parasitic sidewall leakage current path. This is the primary IC failure mechanism for the shallow trench isolation (STI) present in this technology [24]. The observed degradation is therefore primarily caused by radiation-induced charge accumulation in the STI and its interface with the channel region. This illustrates charge trapping along the STI edge as seen in Fig 19 showing the susceptible damage regions as the gate overlaps the STI. A parasitic inversion channel is created which induces a shunt leakage path between the source and drain [24]. The physical structure of the STI dictates the electric-field contours at the upper STI corner which ultimately drives the TID response [21].

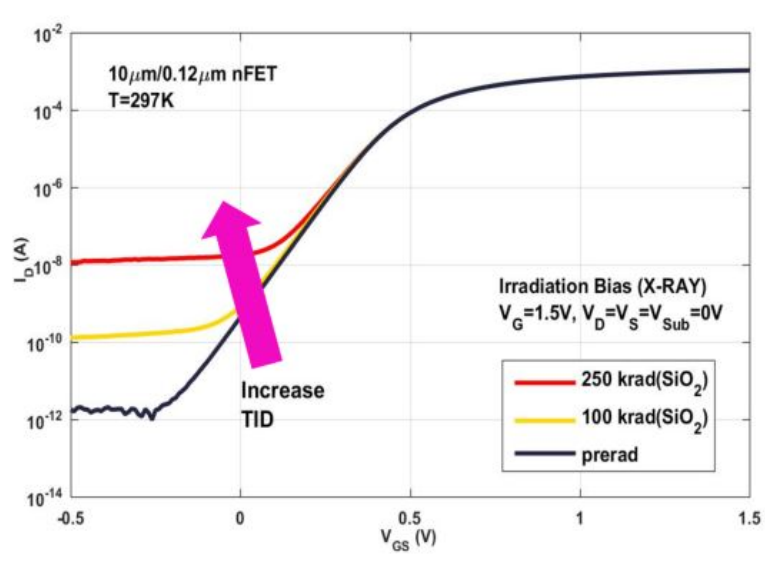**Figure 18:** Transfer characteristics of the device under test for pre-irradiation, 100krad(SiO$_2$), and 250 krad(SiO$_2$) dose conditions.
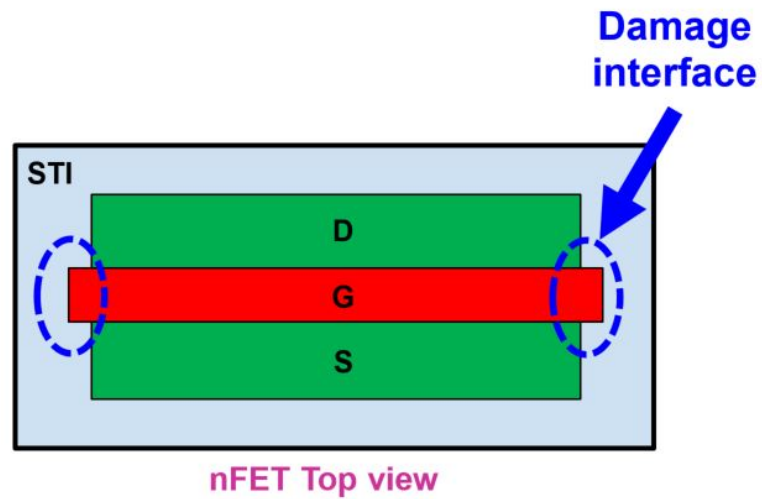

Figure 19: Top view of nFET to illustrate interfaces susceptible to TID damage and charge accumulation.
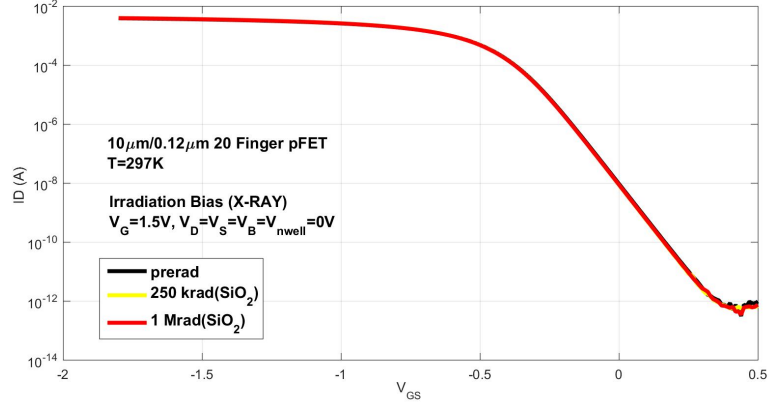
Figure 20: Transfer characteristics of the pFET device under test for pre-irradiation, 250krad(SiO$_2$), and 1 Mrad(SiO$_2$)dose conditions.

pFETs on the other hand, do not produce the same increase in off state leakage results as seen with the nFETs. One leading factor is the introduction of the n-well, which provides a layer of isolation between the current transport and the sensitive ionizing charge build up channel and STI interface regions. Also, different bias conditions for the devices during irradiation. pFETS with a negative bias, sweep radiation-induced holes away from the critical Si/SiO$_2$ interface [17] illustrated in figure 20 as the 8HP pFET 130nm 10/0.12 μm device was irradiated up to 1M rad (SiO$_2$) a much higher dose point than the nFET

The response of an irradiated npn SiGe HBT is shown in Fig. 21. This figure depicts a SiGe HBT forward gummel. There is a shift in the base current at low injection, which is a result in the generation of traps at the emitter-base (EB) spacer oxide and EB space charge region interface. These traps in the EB spacer oxide generated by ionizing radiation results in excess recombination current [11]. Previous work has demonstrated that discrete bipolar junction transistors (BJT) show a decreased degradation on the current gain β due to total dose [21]. The change in current gain is a result of these recombination centers at the EB spacer and STI. It can be noted there is minimal change in collector current as seen in Fig. 21. This is because of the device structure, where the carrier transport is not near sensitive interfaces that
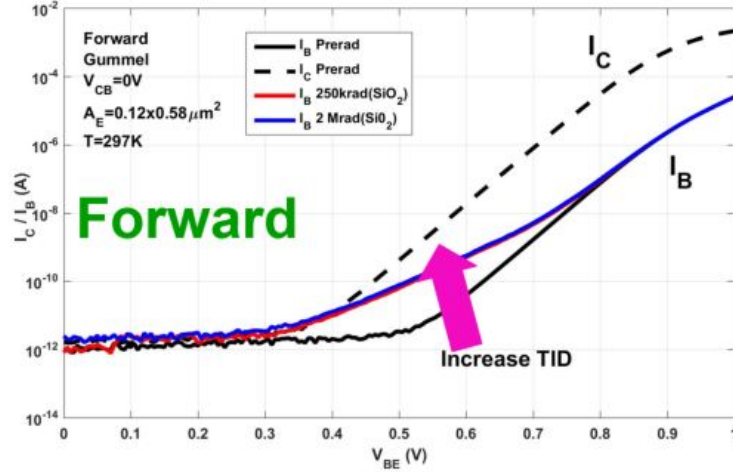
28

Figure 21: Forward Gummel characteristics of the npn, showing radiation-induced degradation.

accumulate traps.

4.3 Simulation and Modeling Results

To further confirm these results, 3-D 130 nm CMOS models were developed by using the Synopsys TCAD suite [26]. This model utilizes electric-field-dependent mobility and hydrodynamic models to provide insight into the nFET increase in off state leakage. The trap concentration in the STI interface and gate oxide were adjusted incrementally to match trends of experimental data. The 3-D nFET model's transfer characteristics as seen in Fig. 23 increase donor traps at the STI-Si interface surrounding the transistor. As the number of traps increase, the off-state leakage also increases, which matches the trend seen in measured data.

A 3-D pFET model was also created in Synopsys TCAD suite. Acceptor traps were incrementally added to STI-Si interfaces. It can be noted in Fig. 24 that the lack of voltage threshold shifts and minimal off state leakage mimics similar trends as seen in measured data.

To provide further insight into the effects of ionizing radiation on SET response observed during pulsed-laser TPA testing of the HBT, a 2-D TCAD model of a SiGe

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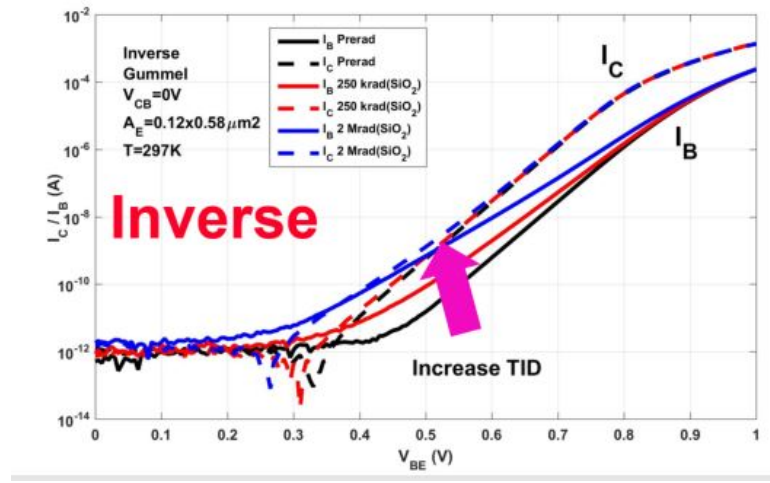
Figure 22: Inverse Gummel characteristics of the npn, showing radiation-induced degradation.
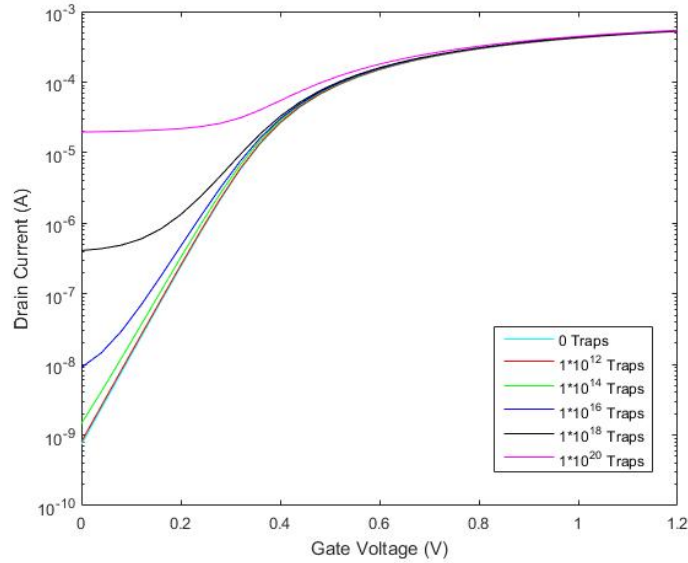
Figure 23: Simulated nFET transfer characteristics.
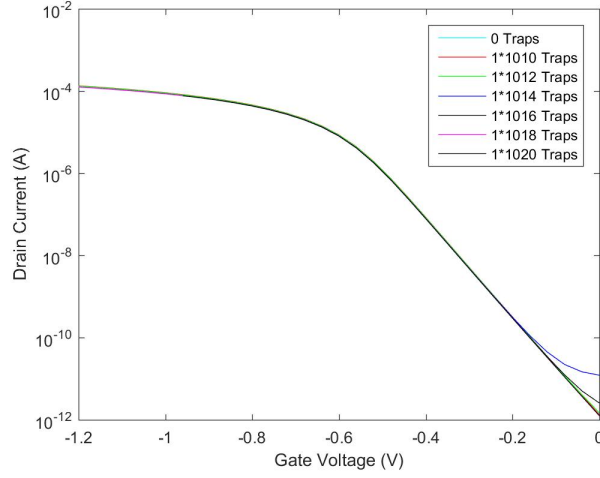
Figure 24: Simulated pFET transfer characteristics.
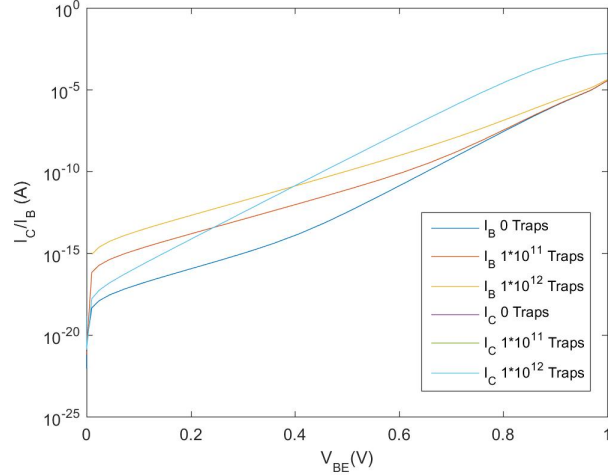
Figure 25: Measured forward gummel NPN characteristics.

HBT was also developed using the Synopsys TCAD suite [26]. TID was simulated by adding oxide traps in the EB spacer and STI regions. Incremental donor traps were increased from 0 to 1×10^{13} C/cm^2 to emulate the accumulation of traps in the oxide induced by TID damage. The amount of traps was adjusted until the inverse gummel characteristics exhibited a similar I$_B$ shift as seen in Fig. 21.

CHAPTER V

SINGLE EVENT TRANSIENT TESTING AND SIMULATIONS

5.1 Experimental Setup

Pulsed-laser experiments were conducted at the U.S. Naval Research Laboratory (NRL) using through-wafer two-photon absorption (TPA). Electron-hole pairs produced by TPA closely resemble those induced by a heavy-ion irradiation. The single photon energy is below the silicon bandgap in TPA, which allows the laser to penetrate through the bulk silicon (allowing for backside irradiation) with minimal energy loss [2]. TPA carrier injection allows for time-resolved, position-dependent three-dimensional measurements of SETs. The system features 150 fs, 1260 nm wavelength optical pulses at a repetition rate of 1 kHz with a 1 μm full-width-at-half-maximum (FWHM) focused spot size. The samples were attached and wire-bonded to a custom designed printed circuit board (PCB). SETs were captured using a high-bandwidth (12.5 GHz, 50 GS/s) real-time oscilloscope with 50 Ω bias tee terminations. It is important to note that the experiments were conducted across multiple days and the TPA laser at the facility must be hand-tuned daily potentially introducing minor beam variations across experimental runs [10]. A SiGe HBT was used daily to calibrate the laser, minimizing beam variation across days.

5.2 Experimental Results

The transient at the collector terminal of an 8HP SiGe npn in Fig. 26 shows the single-event transient response to the electron-hole pairs generated by the emitter stack strike of the TPA laser, demonstrating the SEE sensitivity of the HBT. The
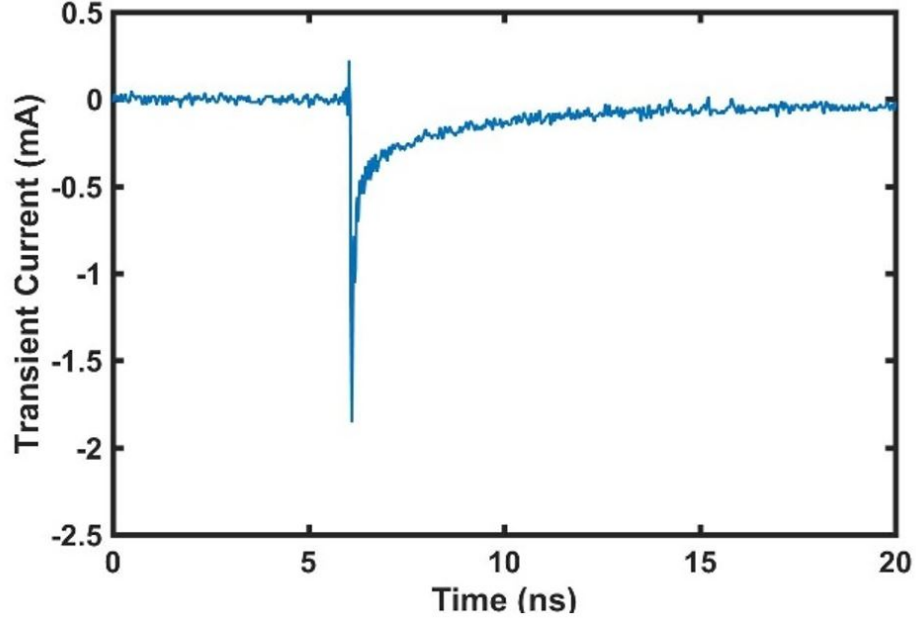
Figure 26: Measured collector output current of the npn SiGe HBT under (V_{CE}=1 V, V_{BE}=1 V) bias conditions.

two prominent mechanisms shown in the figure are the large magnitude fast drift current generated by the ion-shunt effect, and the longer duration, but smaller in magnitude, diffusion transient. The emitter-centered strike demonstrates the vulnerability of the npn to large charge collection. The deep trench of the device traps the charge generated by the electron-hole pairs, which are primarily swept to the terminals instead of charge slowly diffusing to the substrate.

Individual transistors were measured for both the pMOS and nMOS transistors. The nMOS device was biased V_D=1.0 V and 0.25 mA, V_G=1 V, V_S= V_{SUB}= 0 so the device is biased to the saturation region. An example of a nFET transient captured is seen in Fig. 27, and a pFET single-event transient response is seen in figure 28. For both types of devices, electron hole pairs generated by the TPA laser system pass through a reverse-biased junction a transient current is generated and the charge is swept to the electrical nodes of the device. One major factor in the difference between the single-event transient response of the CMOS devices is the difference in
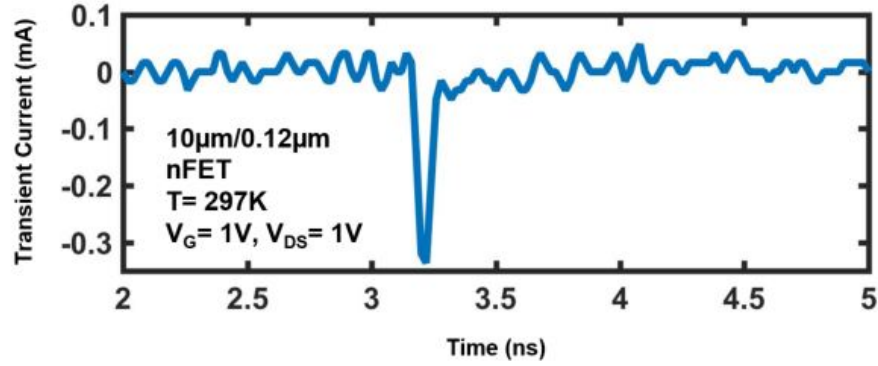
33

Figure 27: Measured drain output current for the nFET transistor under (V_G=1.0 V, V_{DS}=1 V).

the carrier mobility of free charges. In the n-type device the free carriers transport to the terminals with less recombination occurring. With the p-type device, more recombination occurs due to the free carrier mobility .

5.3   SEE Modeling

To further investigate the single-event transient response of the SiGe BiCMOS platform, single-event transient response simulations were performed using the Synopsys TCAD suite and model for all transistors as described in the previous chapter. Ion-strike simulations were emitter-centered strikes for the npn and gate-centered strikes for the CMOS platforms. The depth of the ion strike was set to generate charge through all sensitive volumes of the device. The simulations were performed with an LET =10 MeV-cm^2/mg) while the CMOS devices were biased to saturation and the npn was biased to forward-active mode.

Simulated heavy-ion strike in Fig. 29 generated electron hole pairs and demonstrates the two part transient (drift and diffusion) as seen in the measured data. The simulated transient has generated enough charge to break down the biased junctions. As previously discussed, the two part (drift and current) aspects of the npn single-event transient response are seen in figure 30. While both aspects are apparent in the

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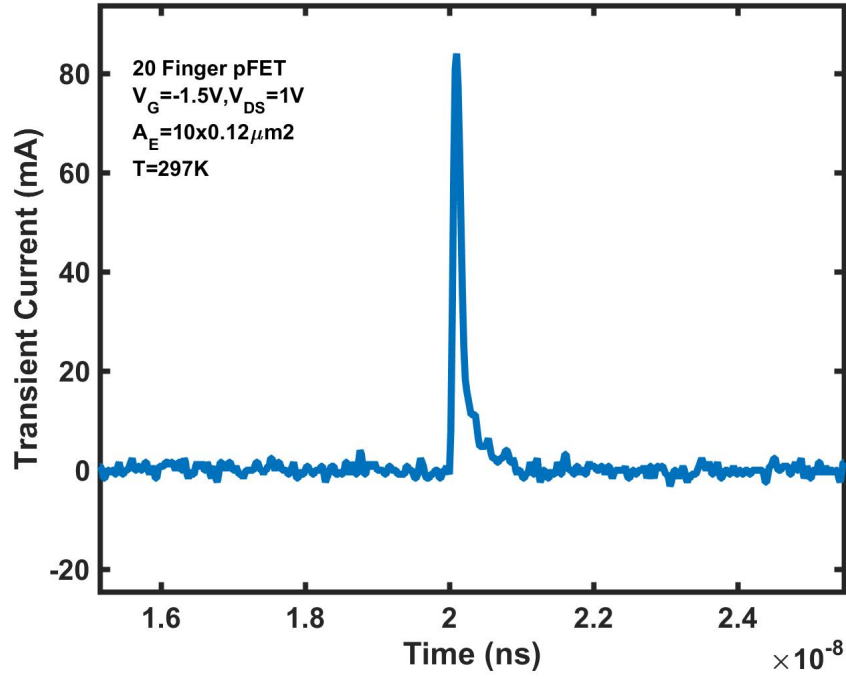
Figure 28: Measured drain output current for the pFET transistor under (V_G=-1.5 V, V_{SD}=1 V).

nFET simulations, the diffusion current in the nFET is less pronounced compared to the npn device. This is due to the differences in device structure and while the npn has the deep trench that isolates the generated charge to the sensitive regions of the device, the nFET only has shallow trench isolation. Another major factor is how current is transporting through the device. The npn has current vertically transporting through the device and it is at this junction (worst case) that the simulation is generating the heavy ion strike. On the other hand, CMOS devices are laterally transport devices. Therefore less of the sensitive charge transport region is effected by the heavy ion charge track when compared to the vertical transport npn device.

Figure 29: Simulated drain output voltage for the nFET device under (V_G=1.0 V, V_{DS}=1 V).

Figure 30: Simulated collector output voltage for the npn device under (V_{CE}=1 V, V_{BE}=1 V) bias conditions.

CHAPTER VI
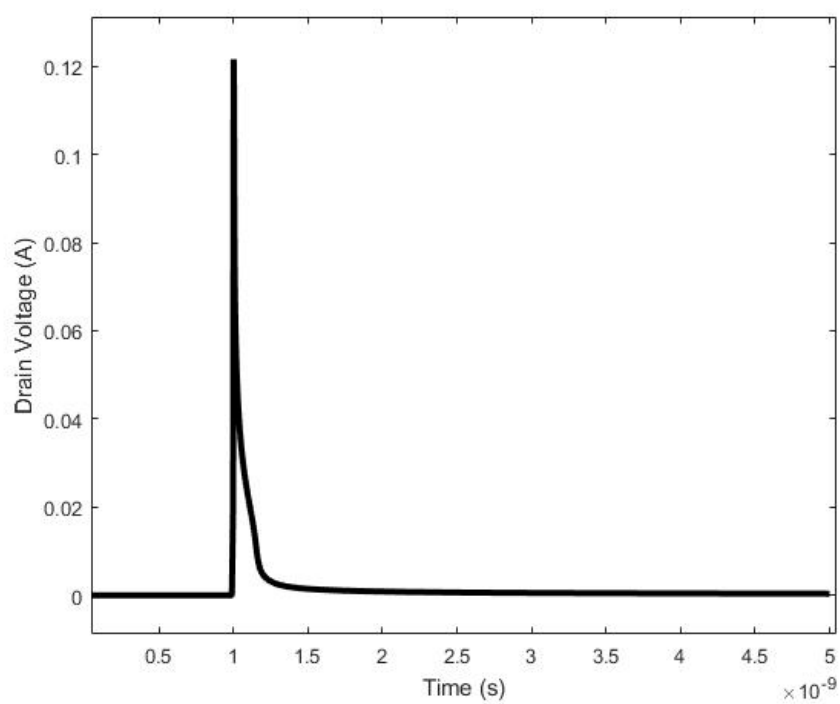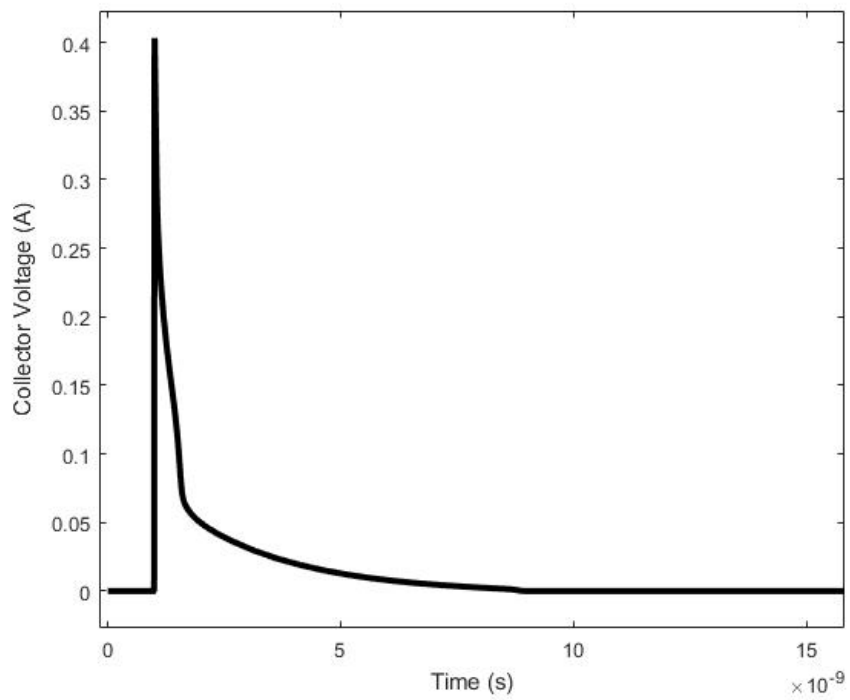
TOTAL DOSE EFFECTS ON THE SINGLE-EVENT
TRANSIENT RESPONSE

6.1 *Experimental Setup*

The experimental setup for the following study follows the same testing procedures
and testing facilities as both the Ionizing Dose and Single Event effects chapters.

6.2 *Experimental Results*

Immediately following X-ray irradiation, the device under test (DUT) was character-
ized and then mounted for pulsed-laser exposure. Two-dimensional rasters scans were
performed before total dose irradiation and at total dose points of 100 krad(SiO_2) and
250 krad(SiO_2), as shown in Fig. 31. These raster scans illustrate the magnitude of
the transient peak decreases as the accumulated dose increases. A single transient
waveform captured through the oscilloscope with the laser focused on the most sen-
sitive area of the device is shown in Fig. 32 for the corresponding dose points.

Fig. 31 further demonstrates that when ionizing radiation is increased from 0-250
krad(SiO_2) the magnitude of the transient peak on the drain decreases. The intro-
duction of trapped charges in the STI interface and STI channel region introduce a
shunt leakage path away from the channel. The laser strike generates charge in the
body of the transistor, producing excess carriers. The carriers either recombine, or
exit through one of the terminals. The introduction of excess charge in the STI region
provides recombination centers for the laser-generated electron-hole pairs. Recombi-
nation centers decrease the amount of carriers that will reach the device terminals.

Previous work has demonstrated that discrete bipolar junction transistors (BJT)
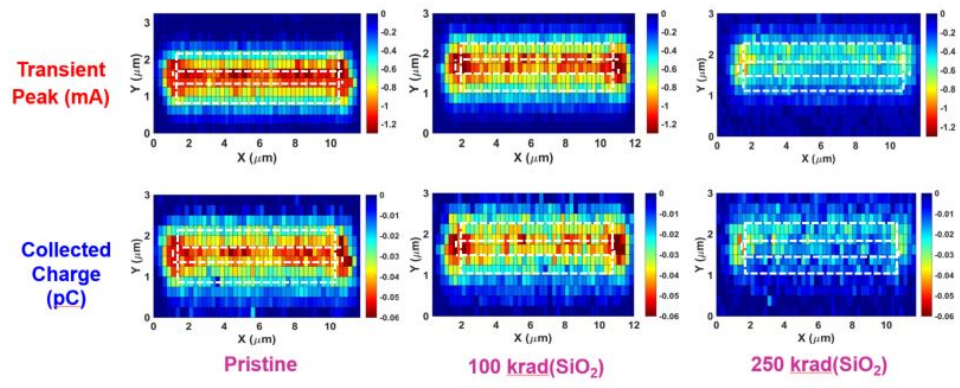
Figure 31: Measured 2-D drain output peaks and collected charge for the nFET devices at a) pristine b) 100 krad(SiO$_2$) c) 250 krad(SiO$_2$) under (V$_G$=1 V, V$_{DS}$=1 V) bias conditions.
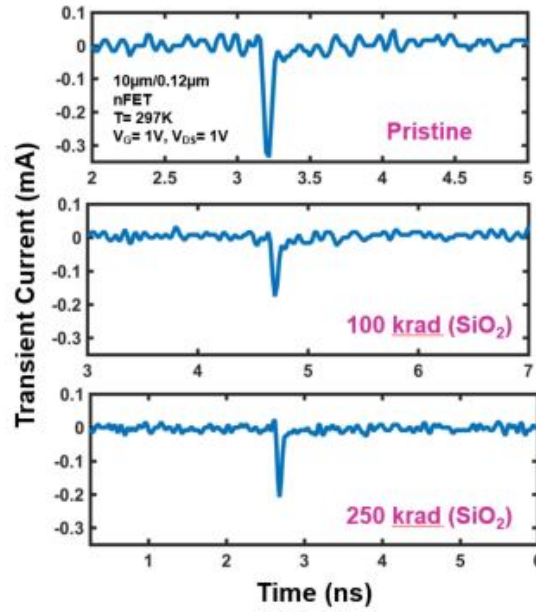

Figure 32: Measured drain output current for nFET devices at a) pristine b) 100 krad(SiO$_2$) c) 250 krad(SiO$_2$) under (V$_G$=1 V, V$_{DS}$=1 V) bias conditions.
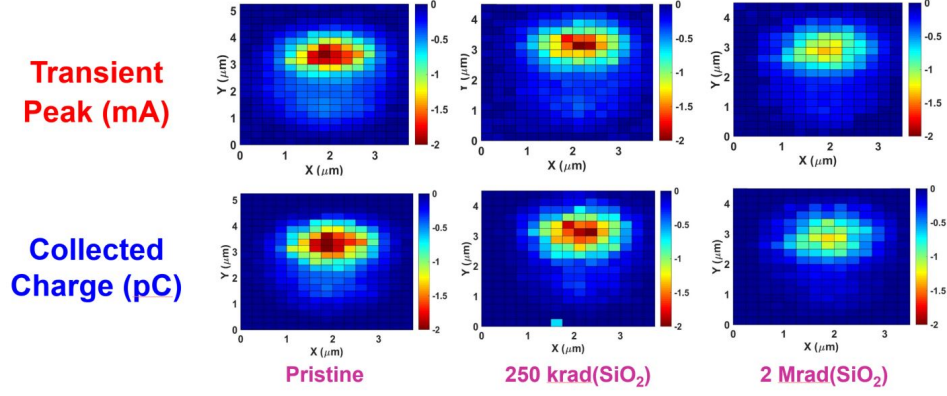
Figure 33: Measured 2-D collector output current and collected charge raster scans for the npn device at a) pristine b) 250 krad(SiO$_2$) c) 2 Mrad(SiO$_2$) under (V$_{BE}$=1 V, V$_{CE}$=1 V) bias conditions.

show degradation of the current gain (β) due to total dose [21]. 2-D raster scans, shown in Fig. 33, show the collector transient peaks of the npn SiGe HBT under forward-active bias (i.e., emitter-base junction forward-biased, collector-base junction reverse-biased). These figures depict the SET response of the SiGe HBT is impacted less due to the same total dose when compared to the nFET device.

When the dose is increased to 2 Mrad(SiO$_2$), the amplitude of the TPA laser-induced transient peak decreases as seen in Fig. 33. The increase in ionizing radiation exposure induces a strong degradation of the current gain (the ratio of collector current to base current I$_C$/I$_B$). The current gain decreases as a function of ionizing exposure, the transient peak likewise decreases as seen in Fig. 33 as compared to previous raster.

As ionizing radiation builds up charge on the EB spacer oxide and EB spacer charge region interface, an accumulation of charge increases. This introduces recombination centers and charge trapping sites in the oxide. As a result, recombination centers increase the base current, which leads to a degradation of the current gain.

The main emphasis on the npn measured results is the difference in dosage points
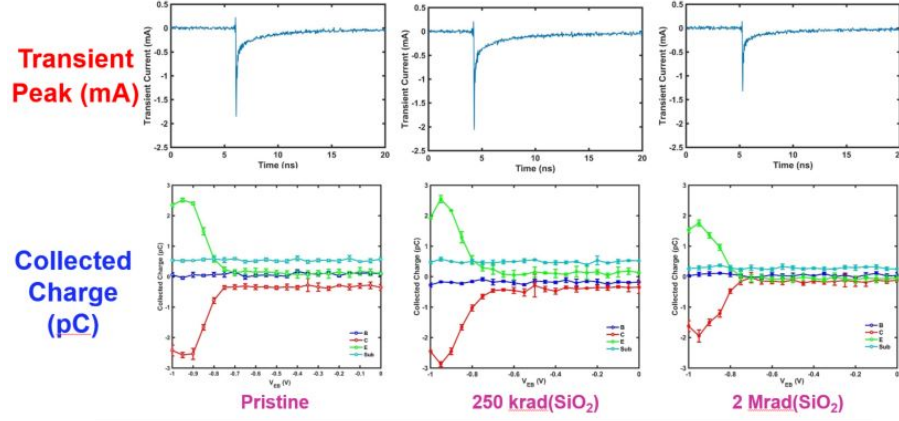
Figure 34: Measured collector output current and collected charge for the npn device at a) pristine b) 250 krad(SiO$_2$) c) 2 Mrad(SiO$_2$)under (V$_{BE}$=1 V, V$_{CE}$=1 V) bias conditions.

at which the single-event transient response degradation occurs. For the nFET devices in Fig. 31 this dosage point is on the order of 250 krad (SiO$_2$), for SiGe HBTs the dosage point we see a decrease in single-event transient response magnitude is significantly higher, on the order of multi Mrad (SiO$_2$). It can be stated that the single-event transient response of the SiGe HBTs exhibits minimal changes for comparable total dose that affects the corresponding CMOS platform.

Just as HBTs are noted to be TID tolerant to multi Mrad(SiO$_2$), pFET devices have shown similar TID tolerant trends at similar total dose levels. Immediately following total dose X-ray exposure a 20 finger 8HP 10/0.12 μm devices were exposed to the same TPA laser source as described in the experimental section. The drain output of the 8HP 130nm pFET is shown in Fig. 41 for total dose levels of 0 rad(SiO$_2$), 250 krad(SiO$_2$) and 1 Mrad(SiO$_2$). The isolation between the STI oxide and the device provided by the n-well the effect of charge build up from the carriers. This is why there is no noticeable shift of the drain output current seen in Fig. 35.
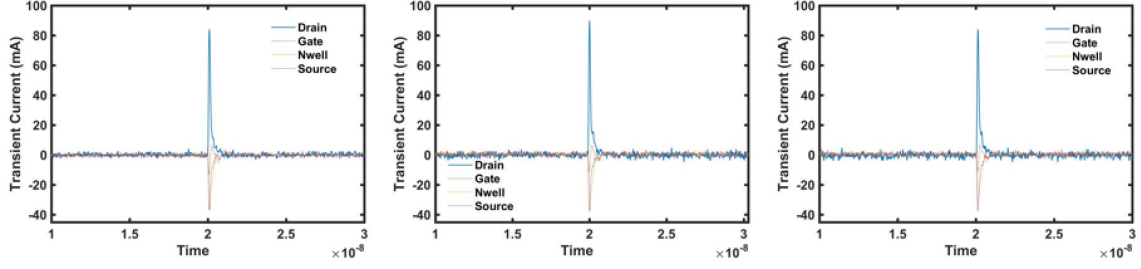
Figure 35: Measured drain output current for the pFET under (V_G=-1.0V, V_{SD}=1 V) bias conditions.

6.3 Simulation, Modeling and Results

To further confirm these results, a 3-D 130 nm nFET model was developed by using the Synopsys TCAD suite [26]. This model utilizes electric-field dependent mobility to provide insight into the nFET single-event transient response as a function of ionizing dose. The trap concentrations in the STI interface and gate oxide were adjusted incrementally from 0 to 1×10^{18} to match experimental data. The traps were added to all Si-SiO$_2$ that surround the transistor illustrated in Fig. 36.

A heavy-ion strike simulation was performed with a model that induces 10 MeV-cm^2/mg^2 and travels 5 μm through the device. The strikes are device-centered shown in Fig. 37, and the simulations assume the ion passes through the device with minimal energy loss. To ensure accuracy of the simulations, the testing conditions were reproduced within the TCAD simulation environment. Each device terminal assumes proper loading of the bias tee and scope terminal. By looking at the device transfer characteristics shown in Fig. 18, one can confirm the increase of recombination centers at the STI interface and gate oxide. The heavy-ion simulation plot of drain node voltage shows a decrease in transient amplitude. This finding verifies that the measured data shows the majority of traps accumulating in the STI interface. Adding hole traps to the STI shows no shift in threshold voltage there we do see a change in transient peak. Simulations verify this claim by the increase in electron density along the STI wall interface. Looking at the effects of this increased charge build up on
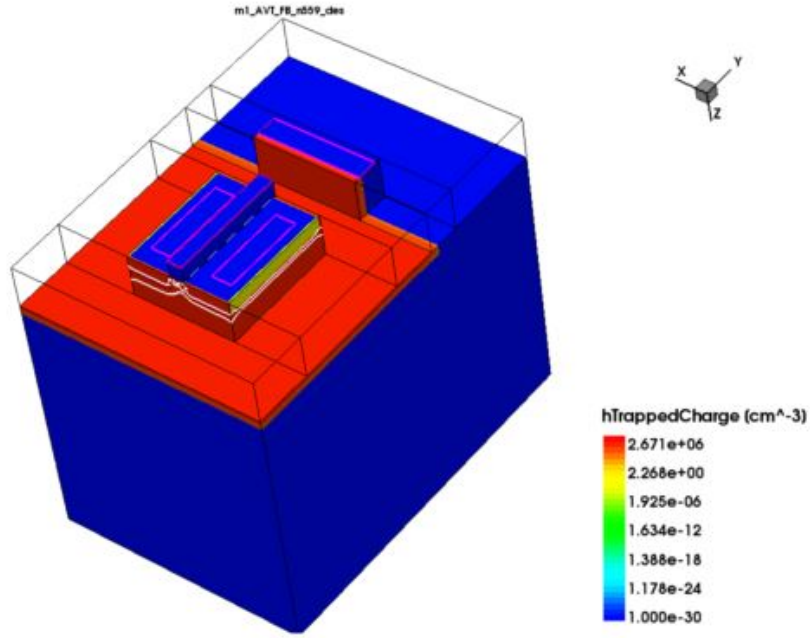
42

Figure 36: 3D nFET Syntaurus TCAD model plot of hole trapped charge density.

the SET is shown in Fig. 29. The heavy ion strike that occurs at 1 ns in this figure exhibits the decrease in transient peak follow similar trends seen in the measured single-event transient response data.

Adding traps to the STI shows no traps in threshold shifts, shown in Fig. 23. We do so a shift in transient peak as the number of acceptor traps is increased. This causes a change in recombination at this interface. Traps were increased from 0 to 1×10^{18}. Therefore, these simulations allow us to conclude that the observed reduction in transient peak as a function of increasing total dose is a direct result of acceptor traps to the STI interface for the nFETS.

To provide further insight into the effects of ionizing radiation on SET npn response observed during pulsed-laser TPA testing, a 2-D TCAD model of a SiGe HBT was also developed using the Synopsys TCAD suite [26]. TID was simulated by adding oxide traps in the EB spacer and STI regions. Incremental donor traps were
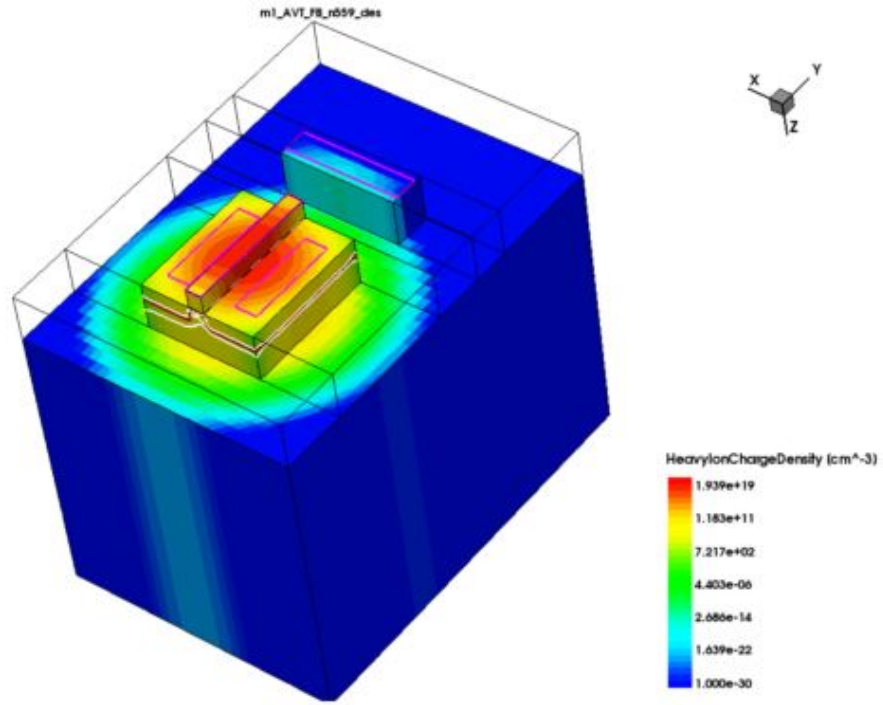
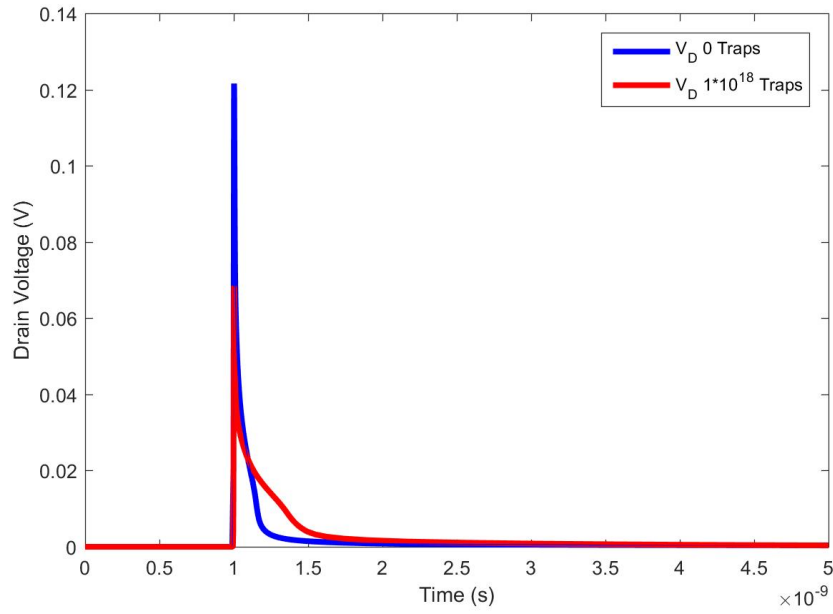**Figure 37:** 3D nFET Syntaurus model heavy ion strike simulation.

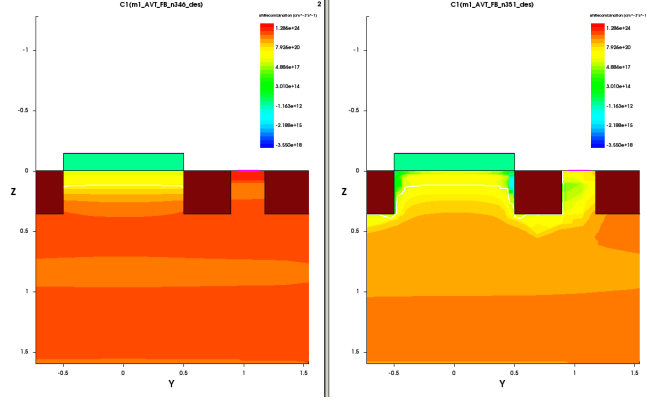**Figure 38:** Simulated drain voltage for the nFET device under the following bias conditions V_G=1 V V_{DS}=1 V.

Figure 39: CMOS Cross Section illustrating surface reed hall recombination a) 0 traps, b) 1×10^{18} traps.

increased from 0 to 1×10^{13} C/cm^2 to emulate the accumulation of traps in the oxide induced by TID damage. The amount of traps was adjusted until the inverse Gummel characteristics exhibited a similar I_B shift as seen in Fig. 22. Heavy-ion simulations were performed with a linear energy transfer (LET) of approximately 10 MeV-cm^2/mg with the device biased in the forward-active region. The increase of electron density due to a heavy-ion strike is depicted in Fig. 16.

These TCAD simulations confirm the trend of maintaining a similar transient peak and collected charge for the comparable dose of 250 krad(SiO$_2$). The drain voltage output in Fig. 40 overlap for both 0 and, 8×10^{11}. Because the charge built up at the interfaces are not as close to the carrier transport, the accumulation of traps has a minimal shift in the single-event transient response, confirming the measured results.

pFET heavy ion strike simulations were also conducted in the Synopsys TCAD suite. Acceptor traps were incrementally increased to 1×10^{11} to all STI-Si interfaces that are flush with the device. Heavy-ion simulations were performed with a LET of approximately 10 MeV-cm^2/mg with the device biased in saturation mode with V_G=-1.5 V and V_{SD}= 1 V. A gate centered strike, as illustrated in Fig. 37, occurs at 1ns and the single-event transient response of the drain output voltage is plotted in Fig. 41. The overlapping single-event transient response confirms pFET is TID
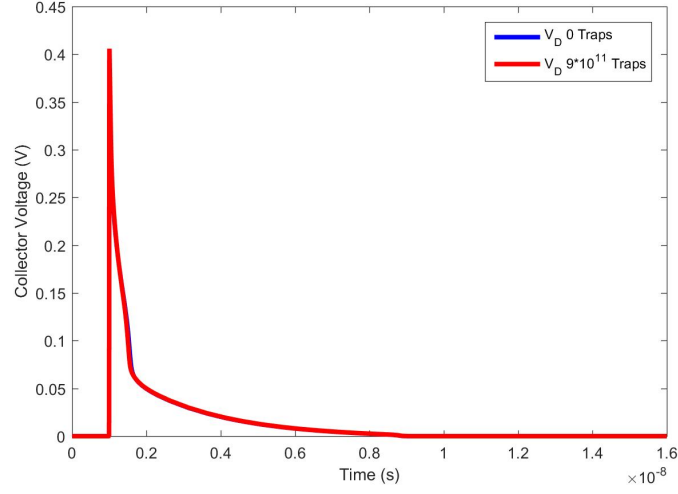
Figure 40: Simulated collector output voltage for the npn under the following bias conditions V_{BE}=1 V $V_{CB=}$=1 V.

tolerant to multi Mrad (SiO_2) plotted in the measured data in Fig. 35.

6.4 Summary

The changes in single-event transient response due to ionizing radiation of a third-generation SiGe BiCMOS platform has been evaluated. Both the npn SiGe HBT and nFET show similar trends of a decrease in the single-event transient response magnitude as ionizing radiation dose increases. The nFET exhibits minimal on-state current degradation and minimal threshold voltage shift; however, a large off-state leakage current results from TID. This response indicates that the ionizing radiation is primarily building up a layer of charge in the STI interface. The accumulation of charge creates recombination centers, a mechanism that is the driving factor for the decrease in transient peak of the SET response. As TID exposure increases from 0-250 krad(SiO_2), the number of recombination centers increases, which in turn, decreases the magnitude of the single-event transient response. TID exposure of the npn SiGe HBT reduces the current gain of the transistor at low injection. Both the nFET and SiGe HBT show a decrease in current as a function of TID exposure. This work further illustrates that testing the combined (coupled) effects of TID and SET is important
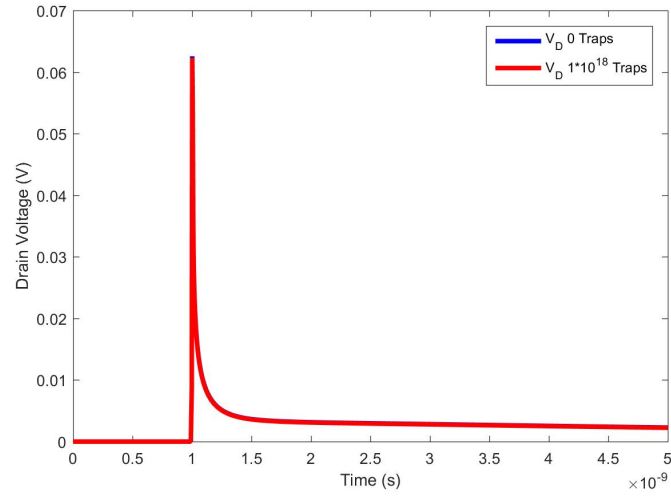
Figure 41: Simulated drain output voltage for the pFET device under the following bias conditions V_G=-1.5 V V_{SD}=1 V.

for accurately assessing device and circuit robustness in space environments.

CHAPTER VII

CONCLUSION

This work has evaluated the effects of ionizing dose on the single-event transient response of the SiGe BiCMOS for the first time. This study furthers the investigation of the SiGe BiCMOS platform for extreme environments applications and space missions with extremely high TID requirements such as missions to Jupiter's moon, Europa. This study of the synergistic effect of ionizing dose on single-event transient response in previous chapters shows that the SiGe BiCMOS is a plausible platform for intense radiation environments.

7.1 Contributions

The results from Chapter 6 evaluate the effects of total dose on the transient response and show that the nFET single-event transient response improves as a function of TID. There is a decrease in transient peak from the output node (drain) and decrease in full transient duration. The SiGe HBT single-event transient response also improves as a function on TID, also showing a decrease in transient peak from the output node (drain) and decrease in full transient duration. However, this decrease occurs at a much higher dosage point. The pFET single-event transient response is unchanged at comparable dose rate, and this is due to the isolation provided by the n-well. The 3D TCAD model investigating the synergistic effect is presented for the first time for a SiGe BiCMOS platform. TCAD modeling confirms STI sidewall shunt leakage path for the nFET and the EB leakage path for the SiGe HBT.

The SiGe HBT and pFET tolerate much higher TID levels than the nFET. There is no change in SET response in the HBT and pFET at the highest HBT total dose level. The results of this work are to be published in the RADECS conference

proceedings and to be submitted to *IEEE Transactions on Nuclear Science.*

7.2   Future Work

To further understand TID effects on the single-event transient response of the SiGe BiCMOS platform, improvements to TCAD models are needed. The present model is adequate in evaluating changes in the transient peak, however further refining and modeling is needed to investigate which types of recombination at the interface is responsible for the recombination occurring. Being able to isolate types of recombination and mobility models will provide further insight into which types of recombination are the dominating factors in the study of TID on the SET response of a SiGe BiCMOS platform. Generational studies would provide further insight to this study. As each generation continues to restructure the device geometry, the response may differ from generation to generation. Each technology may have a slightly different response, so it is necessary to look at multiple generations in order to better understand the underlying physics of charge collection during heavy-ion strikes in these platforms.

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