A FAST QUASI-STATIC TIME SERIES SIMULATION METHOD USING SENSITIVITY ANALYSIS TO EVALUATE DISTRIBUTED PV IMPACTS

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Muhammad Umer Qureshi

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Approved by:

Dr. Santiago Grijalva, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Maryam Saeedifard
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Lukas Graber
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. A. P. Sakis Meliopoulos
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Godfried L. Augenbroe
School of Architecture
Georgia Institute of Technology

Date Approved: April 18, 2019

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LIST OF ABBREVIATIONS

AC: Alternating Current

AMI: Advanced Metering Infrastructure

ANSI: American National Standard Institute

DER: Distributed Energy Resource

EMT: Electro-magnetic Transient

FPF: Fixed Power Factor

HC: Hosting Capacity

IEEE: Institute of Electrical and Electronics Engineers

LDC: Line Drop Compensation

LTC: Load Tap Changer

LVR: Line Voltage Regulator

NREL: National Renewable Energy Laboratory

PCC: Point of Common Coupling

PF: Power Factor

PV: Photovoltaic

QSTS: Quasi-Static Time Series

RMS: Root Mean Square

SbML: Sensitivity-based Midpoint Linearization

SCADA: Supervisory Control and System Acquisition

VR: Voltage Regulation

VReg: Voltage Regulator

VV: Volt-VAR

VW: Volt-WATT

WVM: Wavelet Variability Model

SUMMARY

The desire to reduce carbon footprint coupled with government incentives has led to a massive deployment of renewable energy resources, solar photovoltaics (PV) in particular. Electric utilities in the United States face the challenge of numerous solar PV interconnection requests filed by customers, which seems to increase every day. The approval process for an interconnection request often requires a detailed impact analysis to ensure that the installed resource will not adversely affect the reliability of the distribution grid. Currently, impact analysis for a single PV system using high resolution Quasi-Static Time Series (QSTS) simulation can take anywhere between 10-120 hours to complete, which becomes an infeasible option for utilities, considering the ever increasing number of interconnection requests. To streamline the process, utilities use static scenario-based simulations to determine the maximum hosting capacity of the distribution feeders. However, these hosting capacity estimates don't take into account the voltage regulation (VR) equipment within the feeder. The VR devices, such as tap changing transformers and switched capacitor banks, have the capability to maintain the feeder voltage profile within the ANSI C84.1 limits. Therefore, excluding their impacts while determining the hosting capacity estimates can produce overly conservative results. Consequently, states with aggressive renewable portfolio standards, such as Hawaii and California, are inadvertently limiting their solar PV deployments by relying solely on these conservative estimates.

The goal of this dissertation is to develop a fast, robust, scalable and accurate QSTS analysis tool that can overcome the limitations of existing PV impact evaluation techniques. This work starts by performing a critical analysis of the currently used methods for PV integration studies, and then makes an argument as to why the QSTS analysis is the way forward. The novel algorithm developed in this work leverages the local linearity of the AC power flow manifold to compute the sensitivity coefficients, using a regression-based framework. Furthermore, due to the discontinuities caused by the VR equipment in the

manifold, these coefficients are recomputed for every new observed state of the VR devices. A unique aspect of the proposed algorithm is its ability to decouple the estimation of the states of VR devices and the bus voltage profiles. As a result, the PV impact metrics that are sensitive to the operation of VR devices are estimated at a very high resolution time-step, while a coarser resolution is used for the rest. By using an abstract notion of a VR device, the algorithm can also model the smart inverter dynamic real and reactive power control including Volt-VAR and Volt-WATT operational modes. Apart from the voltage-related impacts of PV systems, the proposed algorithm is capable of accurately estimating the maximum thermal loading, line losses, and overload duration of the distribution system infrastructure.

The novel algorithm developed in this dissertation is evaluated on a variety of 3-phase, unbalanced distribution feeders with multiple VR devices including load tap changing transformers, line voltage regulators, switched capacitor banks and smart inverters. Both the standard IEEE test circuits and utility-scale distribution feeders, with low voltage secondary side modeled, are used for evaluating the robustness of the algorithm. In addition, actual feeder SCADA data and on-field irradiance sensor measurements were used to synthesize the 1-second resolution, yearlong load and PV time series profiles used in this work. The proposed algorithm shows an average speed improvement of around 150 times, when compared to the traditional brute-force QSTS method, and is able to maintain high accuracy levels across a variety of different PV impact metrics. Finally, the scalability of the algorithm is also established in terms of its ability to simulate any number of input time series profiles and VR devices.

CHAPTER 1

INTRODUCTION

1.1 The Electric Grid Revolution

The electric grid is one of the most complex feats of engineering capable of transmitting power reliably over hundreds of miles through a sophisticated network of components including transmission lines, transformers and switching devices. For the past fifty years or so, the electric grid has been evolving at rapid pace in part due to ever changing public policies, push towards better economics and technological innovations. The traditional notion of unidirectional flow of power from bulk generating stations to the end customers via transmission and distribution networks is no longer valid. Today, Distributed Energy Resources (DERs) are being constantly integrated at both transmission and distribution levels. Recent innovations in wind and solar generation coupled with advances in energy storage have resulted in their large scale deployments in the United States, Germany, Spain and Australia. A 2017 study indicates that the Levelized Cost of Electricity (LCOE) of onshore wind and utility-scale solar are both lower than new coal, and are cost-competitive with new combined-cycle natural gas [1].

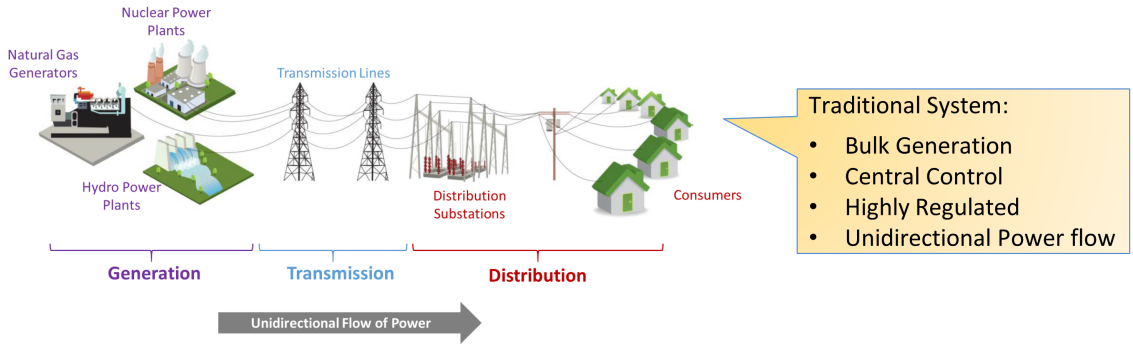


Figure 1.1: Traditional electric grid

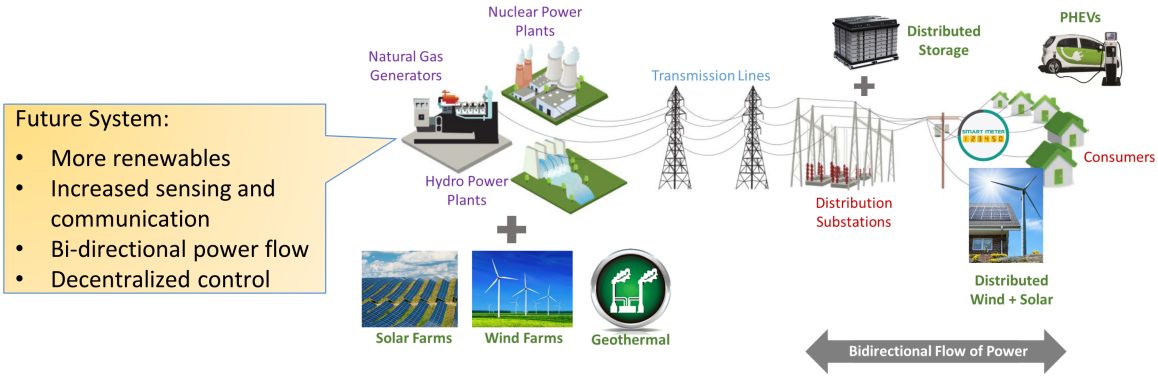


Figure 1.2: Future electric grid with more renewables

The non-dispatchable nature of wind and solar means that the electric grid of today has more temporal and spatial variability than ever before. On the other hand, the digital revolution has caused dramatic improvements in sensing and communication capabilities, allowing more rapid situational awareness to the grid operators. The grid of the future is poised to have significant penetration of renewables along with a more decentralized control architecture that will blur the boundaries between generation, transmission and distribution.

Over the past decade, distribution networks have seen a significant increase in the penetration of DERs. More and more customers are becoming prosumers, deploying DERs to offset their local demand and utilizing grid only as a source of backup power. In addition, during times of low demand, these systems inject excess power back to the grid for which customers expect to be compensated for. Installations of solar PV systems alone have seen an average annual growth rate of 68% per year in the United States over the past 10 years [2]. In 2017, the U.S. market added 10.6 GW_{dc} of solar PV capacity, of which 41% was from distributed solar [2]. This unprecedented growth has been primarily attributed to the decreasing cost of PV systems as well as federal tax incentives [3]. In addition, many states have ambitious Renewable Portfolio Standards (RPS), which mandate local electric utilities to incorporate a specified percentage of renewables in their generation mix. Consequently, to ensure compliance, many electric utilities purchase power from customer-end

DERs through programs such as Net Metering. However, reliable integration of grid-tied DERs pose significant technical challenges to the electric utilities. The focus of this work is to understand these challenges and develop analysis techniques that can quickly quantify the impacts of new solar PV installations in distribution networks.

1.2 Interconnection Study: Why and How?

Solar PV is an intermittent, non-dispatachable resource, the output of which is dependent upon the instantaneous solar irradiance at a particular geographical location. This means that the power produced by a solar panel can be constant or highly variable depending upon the weather conditions. Figure 1.3 shows a typical residential demand curve with and without a rooftop PV system. During the day time when the PV power output is maximum, the net demand goes negative indicating excess generation which is injected back into the grid. In addition, the temporal variability in the demand curve caused by the PV system is significant which often results in power quality issues for both the customers and the electric utilities.

High penetration of solar PV in distribution feeders can result in voltage limit violations [4, 5], flicker [6] and system losses [7] as well as cause thermal overloading of existing distribution infrastructure [8]. In addition, voltage regulation equipment including load tap changing transformers and capacitors banks can suffer from an excessive increase in the

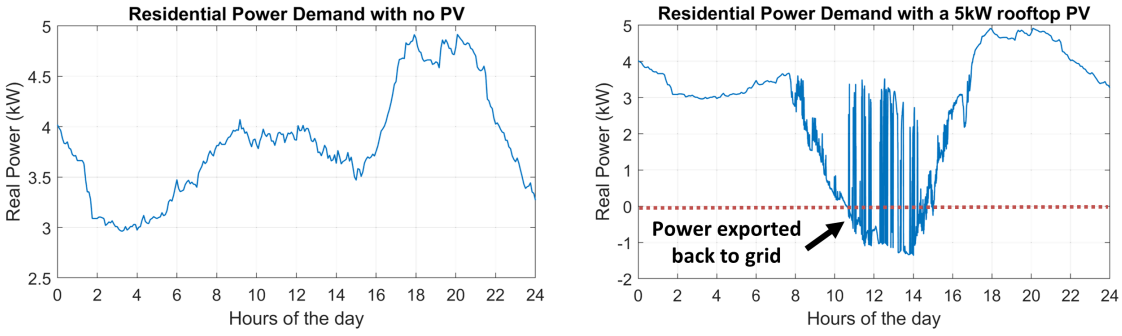


Figure 1.3: Net residential power demand curve (Left: No rooftop PV system installed, Right: A 5kW rooftop PV system installed)

number of operations and exhibit potential oscillatory behavior [9]. This can lead to premature equipment failure resulting in power outages and costly repairs. Therefore installations of customer-end grid-tied PV systems are required to go through an interconnection study process to identify their potential impacts and develop possible mitigation alternatives [3]. Existing methods for PV interconnection studies broadly fall into two categories:

1.2.1 Static Screening Methods

The static screening methods were initially designed to streamline the interconnection study process by allowing PV systems that did not pose any significant impact to the grid to be quickly interconnected without any additional technical studies. Most electric utilities in the U.S. have adopted the standard small generator interconnection procedure (SGIP) which utilizes a set of static screens to quickly evaluate whether an interconnection request will be approved or directed for a supplemental study [10]. One of the most commonly used screens is the 15% threshold which identifies situations where the cumulative DER capacity on a line section exceeds 15% of the annual peak load observed on that specific line section [10]. These static screens work well when the penetration of PV systems is low. However, many states including California and Hawaii are experiencing high penetration scenarios (solar PV contribution is greater than 15% of the in-state generation [11]), where such methods tend to break down [12, 13].

1.2.2 Scenario-based Simulations

Scenario-based simulations are used by electric utilities to determine the feeder PV hosting capacity (HC), which refers to the amount of total PV that a feeder can reliably host without causing power quality and reliability issues. This process essentially involves solving a small set of static power flows designed to simulate extreme scenarios such as light and peak loading, minimum and maximum PV output, etc [14]. The HC estimates are then used to set an upper bound on the total PV that can be installed at various locations within

the feeder. Interconnection requests in areas where the installed PV capacity is close to the predefined HC are directed for supplemental studies. Although much more effective than static screens, the underlying assumptions for scenario-based simulations can produce overly conservative HC estimates. First, due to the complex locational and temporal interdependence of the PV systems, identifying a limited set of scenarios that capture all their potential impacts is statistically impossible. Second, for feeders with voltage regulation equipment (33% of feeder in the U.S. have at least 4 such devices [9]), identifying worse-case scenarios is far more challenging. Finally, the scenario selection process is heuristics-based which can cause significant inconsistencies in the absence of a standardized methodology.

Both of the aforementioned methods provide conservative estimates and fail to accurately quantify all the potential impacts of PV resources. Moreover, these methods to do not take into account any temporal aspects of PV power output, which by its very nature is dependent on the geographic solar irradiance. As a result, time dependent metrics such as duration of voltage and thermal limit violations cannot be estimated using these methods. Furthermore, the impact on expensive voltage regulation equipment cannot be accurately captured using these techniques [15].

1.3 Quasi-Static Time Series Analysis

To fully understand the impacts of PV systems, a time series analysis is required which introduces a temporal dimension to the problem. The IEEE standards association defines Quasi-Static Time Series (QSTS) as a series of steady state power flows solved chronologically with a time step that ranges from 1-second up to an hour [16]. The term "quasi-static" refers to the concept that a static steady-state power flow solution is being used to evaluate an inherently dynamic, i.e. non-steady state, system [17]. The discrete control elements within the circuit are modeled along with their delays and may change their state from one time step to the next. If the variations in the system state from one discrete-time interval

to the next are slow, the low frequency dynamics of the system are well captured in the QSTS simulation. Furthermore, since the solution of the power flow equations at each time step serves as the initial condition for the next interval, the complex interactions amongst the time-dependent controllable elements are also captured. Moreover, by utilizing actual profiles for load and generation, QSTS simulation can accurately determine the locational and temporal impacts of PV systems.

Two types of inputs are required to run a QSTS simulation: circuit model data and time series data[1]. Commercial software packages used by electric utilities to compute the HC estimates already have detailed 3-phase mathematical models of the distribution feeders including overhead/underground transmission lines, transformers, line voltage regulators (LVR), load tap changers (LTC) and capacitor banks. On the other hand, the time series data constitutes historical data for both load and coincident PV output. Load data is typically available at 15-minute or 1-hour resolution, which is too coarse to run an accurate QSTS study. The limiting factor in this case are the time delays of various controllable elements (LTCs, LVRs and capacitor banks), which are usually on the order of a few seconds. Therefore, to accurately capture the time-dependent aspects of these devices, time series data at a very high resolution is required [9, 18]. A common approach to solving this problem is to perform linear interpolation between time steps to obtain a 1-second resolution load data. Similarly, high resolution PV output data is synthesized using wavelet-based variability models that convert irradiance point sensor measurements into time series power injection data [19, 20]. Due to high correlation between solar irradiance at various points along the feeder, the aggregate PV output data has much more variability as compared to aggregate load data [21], as shown in Figure 1.4. Therefore, it is important to have high resolution PV output data as well.

The time horizon of a QSTS simulation is another crucial parameter that needs to be chosen carefully. Seasonal variations are a dominant factor in the load time series data

[1]Time series data is often referred to as power injection profiles, therefore these words are used interchangeably throughout this dissertation.

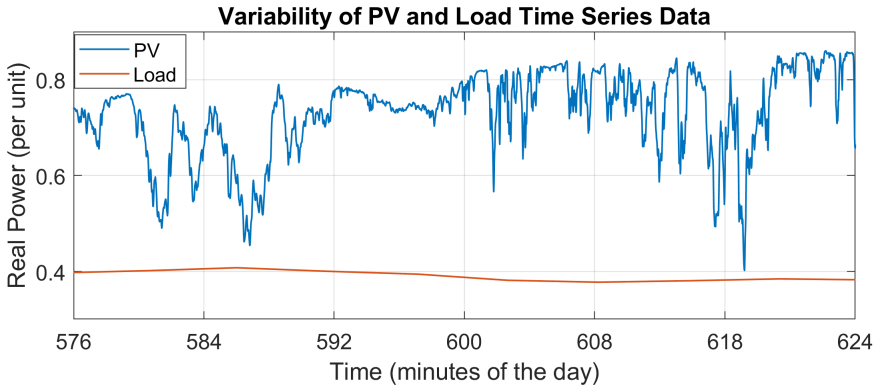


Figure 1.4: Solar PV output changes within a few seconds whereas the aggregate load demand curve stays relatively flat. The data is obtained from [18].

because of varying customer demand during different times of the year. A yearlong QSTS simulation is recommended to fully capture these seasonal impacts [18]. The output of the QSTS simulation is a time series vector of nodal voltages and branch currents for the entire feeder. This data is used to extract the PV impacts across two dimensions:

1. *Locational Impacts:* This includes identifying buses that exhibit extreme voltages and locating circuit elements that are overloaded beyond their thermal ratings. In addition minimum and maximum voltages at each node, maximum thermal loading of various circuit elements, total line losses and feeder highest/lowest voltage points are also analyzed to better understand the location specific impacts of a PV system.

2. *Temporal Impacts:* In contrast to locational impacts, which only provide insight regarding the magnitude of an impact, temporal impacts provide frequency and duration as well. This includes the time duration for specific nodes that violated the voltage and/or thermal limit constraints. Furthermore, insights regarding the change in number of equipment operations by the VR devices and voltage flicker at the customer end can also be obtained using QSTS analysis.

In addition, QSTS is the only effective method to understand and evaluate the impacts of various smart inverter (sometimes referred to as *advanced* inverters) control functions including Volt-VAR and Volt-WATT. It has been shown that negative impacts of grid-tied PV

Table 1.1: Summary of various PV interconnection study methods

	Feeder Model	VR Devices	Locational Impacts	Temporal Impacts	Inverter Impacts
Static Screens	✓	–	–	–	–
Scenario-based	✓	–	✓	–	–
QSTS Analysis	✓	✓	✓	✓	✓

systems can be somewhat mitigated using inverters capable of providing reactive power support and active power curtailment [22, 23]. Metrics such as total reactive power injected/absorbed and the total kW-hour curtailed are important as they directly impact the efficiency and economics of the PV systems. Finally, QSTS can also provide insights regarding optimal strategies for feeder reconfiguration and conservation voltage reduction. Table 1.1 summarizes the capabilities of various PV interconnection study methods. It is important here to mention that only a high resolution QSTS analysis is able to capture the wide range of PV impacts mentioned in Table 1.1.

1.4 Why not QSTS?

The aforementioned discussion begs a very simple question– *If QSTS is the magic bullet, why is it not widely used by electric utilities and system planners?* The answer to this question is two-fold: data requirements and computational time. As discussed earlier, time series data is often not readily available. Only 47% of the U.S. electricity customers have Advanced Metering Infrastructure (AMI) smart meters that can report power consumption at a minimum of hourly intervals [24]. In addition, PV plant data requires a sophisticated deployment of irradiance sensors at various points along a feeder footprint. Various entities including Electric Power Research Institute, Sandia National Laboratories and National Renewable Energy Laboratory are spearheading the efforts to make high resolution data

publicly available for time series analysis [25, 26, 27, 28].

Computational time, on the other hand, acts as a major roadblock to the widespread adoption of QSTS within the industry. A 1-second resolution, yearlong QSTS simulation can take anywhere between 10 to 120 hours to complete, depending upon the size and complexity of the distribution feeder [18]. Often times, multiple simulation runs are required during the interconnection study process to better understand the overall impacts and to develop possible mitigation alternatives. This implies a total computation time that can extend several weeks, for a single interconnection request. According to a recent report, existing leading times for detailed impact studies during interconnection process can reach up to a maximum of 120 days [29]. Adding a high fidelity QSTS study to this process would result in further delays, thereby making the overall process less efficient and more time consuming. Thus, reducing the computational burden associated with running a QSTS simulation is the first step in making it the gold standard for PV interconnection evaluation and impact studies.

1.5 Research Objectives

This research aims is to develop a fast quasi-static time series interconnection analysis tool that can quantify the impacts of installing solar photovoltaic systems in distribution feeders. The goal is to develop a robust, scalable and accurate QSTS algorithm that can perform an impact analysis in a matter of minutes as opposed to days. The tangible objectives of this research are as follows:

1. Perform a review of various PV interconnection study methods used in the industry and elaborate the importance of using QSTS analysis for interconnection evaluation for future high penetration PV scenarios.

2. Develop a QSTS algorithm that can reduce computation time by utilizing a sensitivity model that leverages the physics of the system to create a linear mapping between

QSTS inputs and outputs.

3. Establish the scalability of the algorithm across two dimensions (QSTS inputs):

   (a) Type of feeder model: The algorithm should be universally applicable to any type feeder model (radial/meshed, 3-phase balanced/unbalanced). In addition, it should also work for a variety of voltage regulation devices commonly used in distribution systems (LVRs, LTCs, capacitor banks, smart inverters, switches).

   (b) Number of time series profiles: The algorithm should demonstrate the ability to accurately run a QSTS simulation with any number of time series data inputs regardless of their type (AMI data, SCADA data, PV data).

4. Demonstrate the accuracy of the proposed algorithm in measuring both the locational and temporal impacts of PV systems. The baseline will be against the traditional method for running the QSTS simulation, also referred to as the *brute-force* QSTS.

5. Finally, validate the robustness of the proposed algorithm on a variety of distribution systems including the standard IEEE test cases as well as 3-phase unbalanced utility scale feeders with a low voltage secondary side modeled.

It is important here to note that the scope of work is limited to understanding only the electrical impacts of PV systems in distribution circuits and does not include any socio-economic or environmental impact analysis. The fast QSTS algorithm developed in this thesis can assist system planners, researchers and electric utilities in conducting high fidelity impact studies in a very short period of time.

1.6 Outline of Chapters

Chapter 2 highlights the need for QSTS analysis and presents a detailed literature survey of the existing methods used for performing a time series simulation. Furthermore, it includes an overview of the common challenges faced in speeding up the QSTS simulations.

Finally, a thorough critique of the existing fast QSTS methods is done towards the end of the chapter.

In Chapter 3, a brief overview of sensitivity analysis is presented, which is followed by a mathematical formulation of the power flow manifold and the linear sensitivity model. The impact of VR devices on the nodal voltage magnitude is also discussed and an efficient regression-based framework is proposed to estimate the sensitivity coefficients. A novel algorithm is developed that utilizes these sensitivity coefficients to speed up the QSTS simulation, which is tested on a small IEEE 13-bus circuit.

In Chapter 4, various scalability aspects of the proposed algorithm are discussed and improved. A more accurate method to create linearization of the power flow manifold is proposed which drastically reduces errors in estimating the states of VR devices. In addition, a novel method for estimating the nodal voltage profiles is also presented. Towards the end of the chapter, two utility-scale distribution feeders are used as test cases to evaluate the robustness, accuracy and scalability of the proposed fast QSTS algorithm.

In Chapter 5, the impact of various smart inverter control functions on the power flow manifold is examined. The discontinuities introduced in the manifold due to the dynamic real and reactive power control of the PV inverter are also analyzed and an abstract notion of a controllable element is devised for the linear sensitivity model. Furthermore, the scalability of the algorithm to other types of controllers (such as feeder reconfiguration switches) is also discussed in this chapter. Two test cases, with smart inverters operating in fixed power factor, Volt-VAR and Volt-WATT mode, are used to evaluate the efficacy of the fast QSTS algorithm.

In Chapter 6, current-related impacts, such as thermal loading and over load duration, caused by the PV systems are discussed. It is shown that the current flowing through a power delivery element exhibits a highly nonlinear convex behavior due to the reverse power flow in the circuit. A novel decomposition-based method is proposed that utilizes the linear sensitivity model to estimate the nodal real and reactive power and the corresponding

voltage magnitude to estimate the magnitude of the current. Finally, a summary of the results for all the test cases is presented towards the end of the chapter.

Chapter 7 provides a summary of the work presented in this dissertation and highlights its major accomplishments. The potential areas for future research are also explored. A brief overview of all the test circuits along with the box plots of load and PV power injection profiles are presented in Appendix A and Appendix B, respectively. The student publications are listed in Appendix C.

CHAPTER 2
LITERATURE REVIEW

2.1 Case for Quasi-Static Time Series Analysis

The use of *time series* simulations for impact assessment in distribution systems has gained wide acceptance within the power systems community with the emergence and deployment of various types of DERs. The ever increasing penetration of DERs have highlighted the need for specialized studies with the capability to capture the system dynamics, as opposed to conventional studies which completely ignore it. Two of the most commonly used simulation techniques that capture the dynamic behavior of DERs in distribution systems are electro-magnetic transient (EMT) and quasi-static time series (QSTS). EMT simulation is used to study the instantaneous system behavior in detail and requires the use of continuous-time differential equations for representing the system model. Numerical integration techniques with a short time-step (usually 1-50 μs) are used to solve these differential equations in conjunction with the nodal equations that represent the overall power system. EMT studies are commonly used for islanding detection, protection device design and coordination, and power quality analysis (temporary overvoltages, harmonics, resonance, ferro-resonance) [16]. Due to the impracticality of modeling large networks using EMT tools, reduced circuit models are commonly utilized during an EMT analysis.

QSTS simulation is composed of sequential steady-state power flow solutions where the converged state of one power flow solution is used as an initial state for the next [9]. It does not involve numerical integration of differential equations between the simulation time-steps and assumes a constant fundamental system frequency. Compared to EMT studies, QSTS provides a fair compromise between accuracy and computation complexity, as shown in Figure 2.1. The IEEE 1547.7-2013 standard recommends the use of QSTS simu-

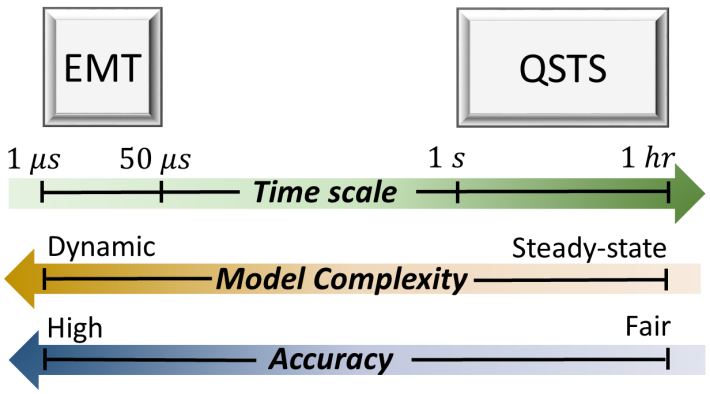


Figure 2.1: Comparison between QSTS and EMT analysis.

lation for impact studies under the following circumstances [16]:

1. Conventional impact studies (e.g. scenario-based simulations) yield marginal results and cannot definitively rule out the adverse impacts of the DER.

2. Control algorithms and coordination strategies of the DERs can interfere with the normal operation of regulation equipment on the feeder.

3. Adverse impact is anticipated for the DER under various loading conditions of the distribution feeder.

Detailed impact analysis using QSTS has been performed in literature, covering all three of the above mentioned aspects. QSTS analysis is performed for solar PV in [9, 30, 17, 31, 32, 33, 34, 35, 36], wind in [37, 38], plug-in electric vehicles in [39, 40, 41, 42] and energy storage in [43]. In [22, 44, 45, 46], authors evaluate various types of dynamic reactive power control strategies of DERs using high resolution QSTS analysis. [23] performs a detailed evaluation of appropriate smart inverter control parameters using multiple QSTS simulations. In addition, several QSTS studies have been conducted to evaluate the impacts of DERs on the voltage regulation equipment within a distribution feeder [9, 30, 17, 31, 32, 36, 47].

A comprehensive discussion regarding the need for QSTS analysis is presented in [18], along with the data and computational requirements. Since QSTS is a chronological solu-

tion of power flows, the resolution at which it is performed directly correlates to the accuracy of the results. For fast intermittent technologies such as solar PV, a high resolution time series simulation is desired, as it can accurately capture variations in PV power output and its corresponding impact on the power quality [9]. On the flip side, a high resolution time series simulation requires significant data and computational effort [9, 18]. There are several practical advantages of running QSTS over scenario-based impact analysis:

1. QSTS captures temporal variations in the load and PV power output, due to which it can accurately estimate the time duration of a particular violation (voltage outside ANSI C84.1, thermal overload etc.). On the other hand, scenario-based simulations cannot provide any insight on how often a particular violation is likely to occur over a given time horizon.

2. Scenario-based simulations, by their very nature, are unable to track the operations of voltage regulation equipment and their corresponding impacts on the voltage profile along the feeder. Such an analysis usually results in extremely conservative hosting capacity estimates that are solely dependent on the particular scenario being evaluated (which is usually extreme feeder loading). In contrast, QSTS analysis seamlessly tracks the states of various voltage regulation devices along with their impact on the voltage profile. This directly translates to an accurate evaluation of distributed PV impacts that is highly methodical rather than heuristic.

3. With increased penetration of smart inverters, the concept of a static hosting capacity estimate will soon become obsolete. QSTS is the only viable method that can accurately quantify the impacts of various smart inverter control functions (including Volt-VAR, Volt-WATT etc.).

In [18], the authors recommend using a year-long, 1-second time-step QSTS simulation to accurately analyze the distributed PV impacts. However, a simulation with such granularity corresponds to solving roughly 31.5 million power flows which can take several days to

run for a realistic feeder using modern computers. Consequently, running multiple QSTS simulations to study locational impacts for various PV sizes becomes an infeasible option. In majority of the aforementioned studies, QSTS analysis is performed for either just a few days [22, 23, 34, 36, 44, 45, 46] or at low resolution time-steps [17, 31, 32, 33]. Therefore, speeding up the QSTS analysis can not only improve the PV interconnection process, it can also play a transformative role in the way DER impact analysis is performed.

2.2 Brute-force QSTS

Brute-force is by far the most common method of running a QSTS simulation. As the name suggests, this method involves solving a power flow for each instant of the given time series data. The time series data can be a vector of the overall feeder load demand (SCADA data), individual customers' power consumption (AMI data), power output of PV systems (synthesized from solar irradiance data) or a combination thereof. Figure 2.2 shows a flow chart of a brute-force QSTS simulation. The simulation starts at time $t = 0$, where the circuit is compiled once and the input time series data is uploaded to the memory. The synthesis and conditioning of the time series data is a separate task which usually is done before hand and is not a part of the simulation. Two important parameters to specify during the initialization process are the simulation time-step and the overall time horizon. The time-step dictates the resolution at which QSTS analysis is performed, and can range anywhere between 1 second up to an hour. The time horizon, on the other hand determines the length of the simulation, which is usually a yearlong for PV impact studies. The next step is to actually solve the 3-phase unbalanced power flow problem corresponding to the feeder load and PV power injections, as specified by the time series data. Once the solver converges, the power flow solution is stored in memory for later retrieval. In addition, the controller logic for various VR devices read their respective control voltages from the power flow solution to determine if a control action is required. The controller logic varies depending upon the type of controller and will be discussed in detail in Chapter 3. If a

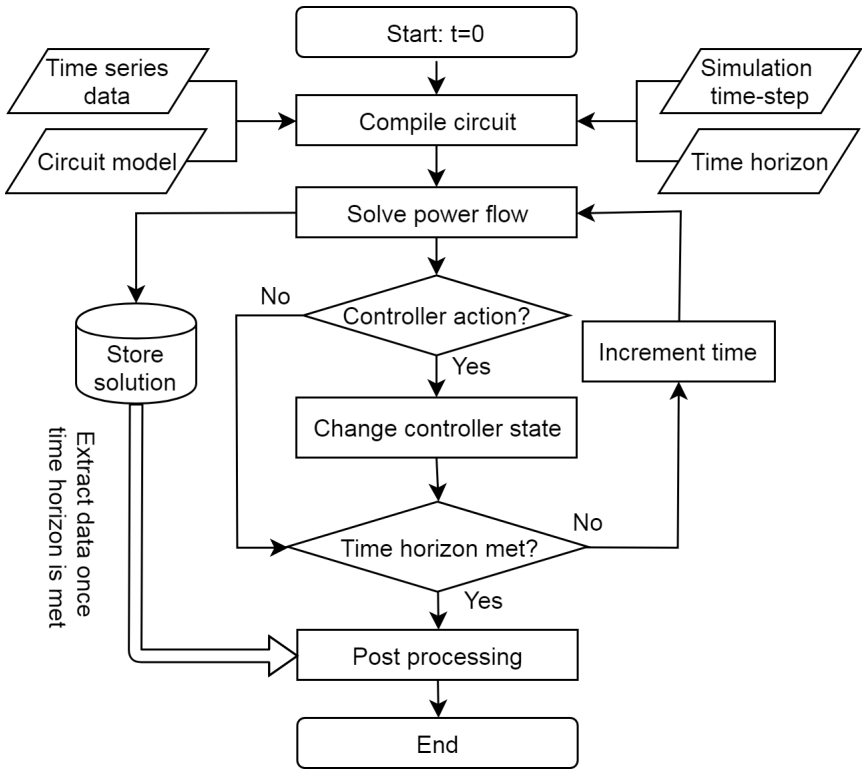


Figure 2.2: Flow chart of the brute-force QSTS algorithm.

control action is required, the state of the VR devices is updated and the simulation steps through time. This process is repeated until the time horizon is met, after which the stored solution space is accessed and post processing is performed on the voltage and current profiles to extract the locational and temporal impacts of PV systems.

Estimating the time taken by a brute-force QSTS is a trivial process. The circuit compilation and post processing are only performed once and utilize less than 1% of the total time taken by the algorithm. Majority of the time is spent solving the 3-phase unbalanced non-linear AC power flow equations. Existing solvers such as OpenDSS and GridLAB-D have been optimized for this purpose and take a fraction of a second to obtain a single power flow solution. However, due to the nature of the brute-force QSTS, a high fidelity 1-second, yearlong simulation would require over 31.5 million power flow solutions. Assuming the time taken by a single power flow solution, t_{PF}, remains constant, the total time

taken by the brute-force QSTS is given by,

$$t_{BF} = t_{PF} \times N_{PF} \tag{2.1}$$

where N_{PF} is the total number of power flows solved, and is dictated by the simulation time-step and the time horizon. Equation (2.1) shows the two factors which dictate the overall time taken by a brute-force QSTS and provides a good starting point for a discussion on some of the challenges for fast QSTS.

2.3 Obstacles in Speeding Up Brute-force QSTS

There are numerous challenges in speeding up a QSTS simulation. The authors in [15] discuss six interesting aspects of QSTS which act as limiting factors for reducing its computational time. The first and the most obvious challenge is the total number of power flow solutions required by a brute-force QSTS analysis. Even though t_{PF} is on the order of milliseconds, a significantly large N_{PF} makes the overall product in equation (2.1) substantial. Therefore, one viable method for reducing computational time of a QSTS simulation is curtailing the total number of power flows solved. This, however, is not a trivial task because of the following reasons:

1. *Time and State Dependency*: The solution of a QSTS simulation at time t is dependent upon the state of the circuit at time $t-1$. For a distribution feeder with LTCs, LVRs and capacitor banks, the state of the circuit is a function of the individual states of these voltage regulating devices. This means that reducing N_{BF} by increasing the time-step will introduce estimation errors that will have a domino effect as the simulation progresses through time. Furthermore, these devices are configured to have delays and hysteresis in their controller logic. The aim is to avoid a phenomena called *hunting* in which the device continuously changes its state to achieve a set point that is physically not possible. This implies that the state of a controller at time $t-1$ is

also a function of some previous history that needs to be accounted for to accurately compute the overall state of the circuit at time t. In [18], the authors present an accuracy comparison for the standard IEEE 13 bus test case for different time-steps. The error in estimating the states of VR devices goes beyond 10% as the simulation time-step approaches 30 seconds. Consequently, just increasing the resolution of a QSTS simulation is not a viable option for reducing t_{BF}.

2. *Multiple Valid Solutions*: Often times, in order to eliminate high frequency components in the control signal, VR devices have a deadband in their controller logic. This prevents oscillations and increases their life expectancy. An important consideration when determining the size of this deadband for LTCs and LVRs is ensuring that at least three valid tap positions exist for any loading condition. However, such configurations tend to produce multiple feasible power flow solutions for a given QSTS input (load and PV power injection at time t). In order to determine the valid power flow solution, the state of voltage regulators at time $t-1$ is required. This means that a one-to-one mapping between the QSTS inputs and outputs cannot be established without tracking their states through time. Both supervised and unsupervised machine learning approaches tend to produce significant estimation errors when used for modeling QSTS simulations because of this lack of direct one-to-one mapping [48].

3. *VR Device Interactions*: VR devices installed in a 3-phased unbalanced circuit have a tendency to interact with each other. These interactions are significant if the devices are placed on the same phase having a close proximity to each other. Consequently, errors in estimating the states of upstream devices can inevitably cause cascading errors in state estimation of the downstream devices. This further highlights the need for accurately estimating the controller states at each time instant, thereby, making the task of reducing N_{BF} even more challenging.

Another possible method to reduce t_{BF} is to further decrease the time it takes to solve a single power flow solution, t_{PF}. Commercially available distribution system simulators, such as OpenDSS and CYMDIST, perform QSTS analysis by solving the 3-phase unbalanced AC power flow equations at each time-step. The nonlinear nature of the power flow equations require iterative gradient-type methods which need multiple iterations to converge to a unique solution. A single snapshot power flow solution with a flat start (all voltage angles set to zero and all voltage magnitudes set to 1.0 p.u.) might require anywhere between 10 to a 100 iterations to converge depending upon the circuit complexity and the error thresholds. In contrast, QSTS utilizes the solution from the previous power flow as the initial condition for the next time-step [9]. Since the variation between time-steps is minimal when performing a 1-second resolution analysis, the power flow solver converges in the least number of iterations. Therefore, directing any effort to further optimizing the existing solvers is futile. In addition, since distribution feeders have significant imbalance (due to single-phase loads and unsymmetrical wires), the commonly used power flow approximation methods at transmission level cannot be used for QSTS studies. Techniques derived from Newton-Raphson load flow, such as fast decoupled power flow or Shamanskii method, suffer from convergence issues and perform poorly for ill-conditioned networks with high R/X line ratios [49]. Furthermore, smart inverters with dynamic reactive power control add an additional layer of complexity due to their nonlinear control curves.

2.4 Existing Fast QSTS Methods

Common techniques widely discussed in literature to reduce the QSTS computation time include reducing the total number of power flows solved, utilizing faster techniques to compute the power flow solution and decreasing the size of the modeled distribution feeder using circuit reduction. Several algorithms have been proposed so far for speeding up the brute-force QSTS, each with its advantages and limitations.

Applying vector quantization (VQ) to the input time series data is perhaps the most

thoroughly researched technique for speeding up QSTS simulations. Initially proposed in [30, 50], VQ groups together scenarios throughout the year that produce similar power flow solutions, thereby limiting the total computations of the non-linear AC power flow equations. Authors in [30] utilize multi-dimensional clustering, whereas [50] uses k-means++ to quantize the input time series data. While an impressive time gain is reported, the test circuits used in both of the aforementioned studies lack VR equipment. In addition, [50] is unable to accurately estimate extreme voltages while [30] uses a very coarse resolution for input time series data (10 minutes). A novel method for applying VQ to circuits with VR devices was developed in [51]. It utilizes the input time series data along with the state of voltage regulators and capacitor banks to uniquely characterize a quantization cluster. Further improvements to this algorithm were proposed in [52], where a sensitivity-based quantization strategy was investigated. It provides a significant reduction in QSTS computation time while maintaining reasonable accuracy levels, however, suffers from inherent scalability issues. Increasing the number of input time series profiles causes a drastic surge in the total number of unique scenarios, which directly translates to an increase in N_{PF}. Although the power flow solutions required by VQ is always less than that of the brute-force, the computational time reduction quickly diminishes as more time series profiles are added.

Variable time-step (VT) is another method that aims to speed up QSTS by reducing N_{PF}. The goal of a VT solver is to focus computational efforts during the periods of the year when the system state is changing rapidly [53]. For example, the variability in the net load demand is significantly lower during the night time because of zero PV output. This means that the system state does not change drastically from one time-step to the next and hence, the QSTS algorithm can be configured to run at a much coarser resolution at night. The VT algorithm proposed in [54] is 50 times faster than the traditional brute-force QSTS and produces an average error of 7% in estimating the states of VR devices. One limitation of this method is the error in detecting nodal voltage extremities, which can potentially

occur in-between the time-steps where the algorithm is making larger jumps.

Intelligent Sampling (IS), developed in [55], uses representative samples from input time series data to perform a QSTS analysis. It decomposes the year into smaller 6-hour time periods, and then characterizes them using the solar variability index and mean load values. The underlying assumption in IS is that similar time periods will have closely correlated QSTS results. Therefore, by only solving the representative samples, the results can be extrapolated for the whole year. The proposed IS method in [55] produces an average error of 10% in estimating the states of VR devices. However, it provides a computational time reduction of only 57% (2.3 times faster), when compared to the brute-force QSTS.

Utilizing machine learning to speed up brute-force QSTS is another approach that has produced promising results (such as in [56, 57, 58]). Instead of solving power flows at each instant of time, the proposed methods in [56, 57] utilize a regression algorithm and a correction method to determine the time-series power flow results during the studied period. However, both of these studies consider circuits without any VR equipment which limits their applicability. An ensemble neural network (NN) based machine learning algorithm for QSTS is presented in [58]. This method utilizes the brute-force QSTS to initially train the NN, which can then be used to accurately model the impacts of high penetrations of distributed PV on VR equipment. However, the training of the NN is feeder specific and requires at least 21% of the yearlong brute-force QSTS to run. Recently, a fast QSTS simulation method based on voltage sensitivities of controllable elements has been presented in [59]. The proposed method creates decision boundaries for various controllable elements in the circuit by estimating nodal voltage sensitivity coefficients. Instead of solving power flows at each time instant, it exploits these decision boundaries to predict the controller states for a year-long QSTS simulation. A significant reduction in computation time is reported however, the proposed iterative approach for estimating decision boundaries suffers from scalability issues as the number of unique load and PV power injection profiles increases. In [59], the decision boundaries become more complicated with additional

dimensions being added for each profile. Consequently computing boundaries for these higher dimensional spaces requires an exponentially increasing number of power flow solutions, which becomes computationally time intensive. Moreover, the proposed algorithm in [59] is unable to estimate extreme feeder voltages as well as lacks the ability to detect any potential thermal overloading of circuit devices.

Another class of methods used to speed up QSTS rely solely on decreasing the average time taken by a single power flow solution, t_{PF}. Circuit reduction [60] creates a simplified equivalent representation of the feeder by reducing the total number of buses in it. This shrinks the dimension of the resulting power flow problem, and hence reduces the total time taken by the solver. This method however, relies on detecting specific buses of interest which can be a challenging task given that the lowest and highest voltage extremes can occur anywhere in the feeder. Similarly, A-diakoptics [61] divides the distribution feeder into smaller geographical subnetworks, which can then be solved in parallel on multi-core machines. Computationally efficient power flow analysis techniques based on neural networks, as well as probabilistic algorithms have been proposed in [62, 63, 64]. The focus of this research is not on speeding up the individual solution of the power flow, since existing solvers have already been optimized for this purpose. The main objective is speeding up QSTS by reducing the total number of power flows solved for a 1-second resolution, year-long QSTS simulation. In addition, the algorithm should be able to address the limitations of the existing methods in terms of scalability, accuracy and robustness.

CHAPTER 3

SENSITIVITY-BASED FAST TIME SERIES ANALYSIS

In this chapter, a linear sensitivity model is developed which creates a linear mapping between QSTS inputs and outputs by using sensitivity analysis. It exploits the correlation between the phase voltage magnitudes and power injections in the circuit by using multiple linear regression. The impact of controllable elements (voltage regulators and capacitor banks) on the bus voltage is also analyzed. Finally, a fast and scalable QSTS algorithm is presented that utilizes the linear sensitivity model to evaluate voltage-related PV impacts. The efficacy of the proposed algorithm is evaluated on a variety of test circuits. This chapter expands the work originally presented in [65].

3.1 Review of Sensitivity Analysis

The nonlinear nature of the AC power flow equations require iterative gradient-type methods, which demand significant computational burden when performing a time series analysis. In contrast, sensitivity analysis projects these complex equations governing the voltage-power relationship into a linear space through sensitivity coefficients. This provides a more intuitive cause-and-effect based correlation between changes in network voltages as a response to changes in load and generation [66, 67, 68, 69, 70, 71]. Sensitivity analysis has been extensively used in voltage management strategies for distribution networks. In [72], the authors use same-bus sensitivity analysis to mitigate voltage fluctuations caused by the variability of the PV power output. On the other hand, [73] uses sensitivity theory to perform voltage regulation by using the reactive power exchanged between the network and the distributed generators. Furthermore, sensitivity analysis has been used for identifying the optimum location of DERs within the distribution networks to minimize the power losses [74]. Various techniques have been proposed in literature to compute sen-

sitivity coefficients including Gauss-Seidel method [75], Jacobian-based method [76] and adjoint-network method [77]. Two of the most widely used methods are discussed next.

3.1.1 Jacobian-based Sensitivity Analysis

The inverse of the Jacobian matrix J in the Newton-Rapshon load flow (NRFL) technique directly yields the network sensitivity coefficient matrix as a by-product [72]:

$$\begin{bmatrix} \Delta\theta \\ \Delta|V| \end{bmatrix} = J^{-1} \begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \begin{bmatrix} \frac{\partial\theta}{\partial P} & \frac{\partial\theta}{\partial Q} \\ \frac{\partial|V|}{\partial P} & \frac{\partial|V|}{\partial Q} \end{bmatrix} \begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} \tag{3.1}$$

where $\Delta|V|$ and $\Delta\theta$ represent vectors of small variations in voltage magnitudes and angles as a result of changes in real and reactive powers, ΔP and ΔQ respectively. The terms $\partial|V|/\partial P$ and $\partial|V|/\partial Q$ represent the sensitivities of $|V|$ with respect to changes in P and Q respectively. This method is particularly useful since it does not require any additional calculations and provides nodal sensitivities as a function of the current system state. However, most common load-flow simulation packages either don't provide access to the formed Jacobian or may use alternative load-flow techniques. This is because the NRFL is not well-suited for solving distribution systems due to their high R/X ratios. Furthermore, NRFL is unable to compute the sensitivities against the transformers tap-changers positions.

3.1.2 Perturb-and-observe Sensitivity Analysis

Another commonly used procedure for obtaining network sensitivities is perturb-and-observe method. In contrast to the analytical techniques, it is more of an more empirical approach that relies on introducing small perturbations in the injected power and then measuring the overall impact. It involves the following steps [78]:

1. An initial load flow calculation is performed at a given operating point to obtain the

voltage at bus Y, denoted by $|V_Y|$.

2. A small variation in the injected power is introduced at bus X, denoted by ΔP_X. A load flow calculation is performed once more around this new operating point to obtain the deviation in the voltage at bus Y, denoted by $\Delta|V_Y|$.

3. The sensitivity of voltage at bus Y with respect to perturbation in bus X is obtained using the following expression,

$$\frac{\partial|V_Y|}{\partial P_X} = \frac{\Delta|V_Y|}{\Delta P_X} \tag{3.2}$$

One major benefit of this approach is the ease with which network sensitivities can be computed—a working power flow solver is all that is needed. In this chapter, we propose a multiple linear regression based perturb-and-observe algorithm to compute voltage sensitivities and consequently utilize them to speed up the QSTS analysis.

3.2 Review of Multiple Linear Regression

This section revisits the basic framework of multiple linear regression. For a given data set of q statistical units $\{y_i, x_{i1}, ..., x_{ip}\}_{i=1}^{q}$, linear regression attempts to model a linear relationship between the scalar dependent variable y_i and p explanatory variables $x_{i1}, ..., x_{ip}$. For $p > 1$ the process is called multiple linear regression and the model takes the form,

$$y_i = \alpha_0 + \beta_1 x_{i1} + ... + \beta_p x_{ip} + \varepsilon \tag{3.3}$$

where α_0 is the intercept, $\beta_1, ..., \beta_p$ are the slopes and ε is the residual error of estimation. For q observations, (3.3) can be written compactly as,

$$\boldsymbol{Y} = \boldsymbol{X}\boldsymbol{\beta} + \boldsymbol{\epsilon} \tag{3.4}$$

where,

$$\boldsymbol{Y} = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_q \end{bmatrix}, \ \boldsymbol{X} = \begin{bmatrix} 1 & x_{11} & x_{12} & \dots & x_{1p} \\ 1 & x_{21} & x_{22} & \dots & x_{2p} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & x_{q1} & x_{q2} & \dots & x_{qp} \end{bmatrix}, \ \boldsymbol{\beta} = \begin{bmatrix} \alpha_0 \\ \beta_1 \\ \vdots \\ \beta_p \end{bmatrix}$$

Here $\boldsymbol{Y} \in \mathbb{R}^q$ is the response vector, $\boldsymbol{X} \in \mathbb{R}^{q \times p+1}$ is the design matrix, $\boldsymbol{\beta} \in \mathbb{R}^{p+1}$ is the parameter vector and $\boldsymbol{\epsilon} = [\varepsilon_1, \varepsilon_2, ..., \varepsilon_q]^\top \in \mathbb{R}^q$ is the residual error vector. We can estimate $\boldsymbol{\beta}$ using ordinary least squares which attempts at minimizing the sum of squared residual error S given by,

$$S = \sum_{i=1}^{q} (\varepsilon_i)^2 \tag{3.5}$$

If $\boldsymbol{X}$ has full rank $p + 1 \leq q$, the ordinary least squares estimator for $\boldsymbol{\beta}$ is,

$$\hat{\boldsymbol{\beta}} = (\boldsymbol{X}^\top \boldsymbol{X})^{-1} \boldsymbol{X}^\top \boldsymbol{Y} \tag{3.6}$$

The predicted value of $\boldsymbol{Y}$ is given by,

$$\hat{\boldsymbol{Y}} = \boldsymbol{X} \hat{\boldsymbol{\beta}} \tag{3.7}$$

For a more detailed discussion on multiple linear regression, see [79].

3.3 Power flow Manifold

To create a mapping between the bus voltage magnitude and power injections in the circuit, it is important to introduce the concept of a power flow manifold. Let $V_k = v_k \angle \theta_k$ represent the complex voltage phasor at bus k, where v_k, θ_k represent the voltage magnitude and angle respectively. The injected complex power through bus k in rectangular coordinates is given by $S_k = p_k + jq_k$, where p_k, q_k denote the active and reactive power injections respectively.

For an n-bus network, we also define the bus admittance $\boldsymbol{Y} \in \mathbb{C}^{n \times n}$ matrix as,

$$\boldsymbol{Y} = \begin{cases} y_i + \sum_{\substack{k=1,2,..,n \\ k \neq i}} y_{ik}, & \text{if} \quad i = j \\ -y_{ij}, & \text{otherwise} \end{cases} \tag{3.8}$$

Let $\boldsymbol{V}, \boldsymbol{S} \in \mathbb{C}^n$ represent the complex voltage and power vectors obtained by stacking the nodal quantities $v, \theta, p, q \in \mathbb{R}^n$ for all the buses. The complex vector of the branch currents $\boldsymbol{I} \in \mathbb{C}^n$ in the system can be obtained using nodal analysis,

$$\boldsymbol{I} = \boldsymbol{Y}\boldsymbol{V} \tag{3.9}$$

Ohm's law allows us to link the nodal power injections with voltages through the expression $\boldsymbol{S} = \boldsymbol{V}\boldsymbol{I}^*$. The AC power flow equations describing the network are thus given by,

$$\text{diag}(\boldsymbol{V})(\boldsymbol{Y}\boldsymbol{V})^* = \boldsymbol{S} \tag{3.10}$$

where $\text{diag}(\boldsymbol{V})$ represents a square matrix with elements of $\boldsymbol{V}$ on its diagonal. We now represent the state of the power network by a vector $\boldsymbol{g} \in \mathbb{R}^{4n}$,

$$\boldsymbol{g} = [v, \theta, p, q]^\top \tag{3.11}$$

A power flow manifold $\mathcal{M}$ is defined as a constraint set which satisfies the non-linear AC power flow equations (3.10). Mathematically it can be expressed as [80],

$$\begin{aligned} \mathcal{M} &:= \{\boldsymbol{g} \mid \mathcal{F}(\boldsymbol{g}) = \boldsymbol{0}\} \\ \mathcal{F}(\boldsymbol{g}) &= \begin{bmatrix} \Re(\text{diag}(\boldsymbol{V})(\boldsymbol{Y}\boldsymbol{V})^* - \boldsymbol{S}) \\ \Im(\text{diag}(\boldsymbol{V})(\boldsymbol{Y}\boldsymbol{V})^* - \boldsymbol{S}) \end{bmatrix} \end{aligned} \tag{3.12}$$

where $\mathbf{0} \in \mathbb{R}^{2n}$ is a vector with all zeros and $\mathcal{F}(\boldsymbol{g}) : \mathbb{R}^{4n} \rightarrow \mathbb{R}^{2n}$ is the power flow constraint obtained by rewriting the equation (3.10) into real and imaginary coordinates. Equation (3.12) represents all the values of the system state $\boldsymbol{g}$ that are physically possible. In a QSTS simulation, the input time series data dictates the power injections of both the load and generation PQ buses at each time instant. These power profiles can be only real power injections, only reactive power injections, or a combination scaling both active and reactive power proportionally for fixed-power-factor loads. We can mathematically express their impact by defining a scalar $x_i \in [0, 1]$ corresponding to some bus i, which can either be a PQ generation bus or a PQ load bus. For fixed power factor loads, x_i acts as a multiplier scaling the complex power from zero to rated the value S_{ri} as follows,

$$\begin{aligned} S_i &= x_i S_{ri} \\ &= x_i(P_i + jQ_i) \end{aligned} \tag{3.13}$$

where P_i and Q_i is the peak active and reactive power (of load or generation) at bus i. In case of a PV operating at unity power factor, the term Q_i in equation (3.13) is set to zero. Similar expressions can be written for other types of loads as well.

3.3.1 Geometric Interpretation

The power flow manifold $\mathcal{M}$ links the exogenous power injections in the circuit to the resulting feasible voltage phasors. A modified IEEE 13-bus test circuit [18] is used to show the geometric interpretation of $\mathcal{M}$. The test case has a centralized 3-phase, 2 MW PV system installed at the end of the feeder, as shown in Figure 3.1. Both single and three phase loads (represented by yellow dots) are connected to various points along the feeder. The modified test case also has line voltage regulators and capacitor banks, however their states are fixed. The impact of these devices on the manifold will be discussed later in this chapter. Furthermore, all the PQ load buses are assigned a scalar x_l and the single PQ generation bus, to which the PV system is connected, is assigned x_{pv}.

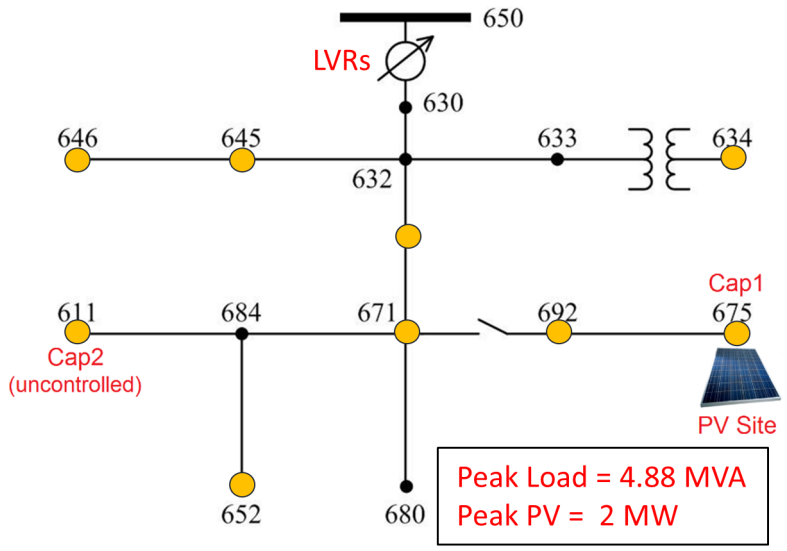


Figure 3.1: Modified IEEE 13-bus test case with a 2 MW, 3-phase PV system along with 3 single phase LVRs at substation and a 600 kVAR, 3-phase capacitor (Cap1) at bus 675.

In a QSTS simulation, (x_l, x_{pv}) act as input time series profiles. Different values of these inputs will result in varying loading conditions causing the phase voltages across the entire feeder to change. For PV impact studies, voltage magnitude v is usually the quantity of interest rather than the phase θ, therefore θ is treated as a state variable rather than an output. Figure 3.2 shows the solution of the power flow manifold (3.12) for the modified IEEE 13-bus test case using OpenDSS. For notational consistency, we call it a *voltage-power* manifold as it links the impact of exogenous power injections (x_l, x_{pv}) on the nodal voltage. The x-y plane represents all the possible combinations of the input time series data whereas the z-axis corresponds to the resulting voltage magnitude at bus 611, phase C. Furthermore, voltage magnitudes at various loading conditions are also highlighted in the figure. The lowest voltage is observed at peak load and zero PV output (i.e. $x_l = 1, x_{pv} = 0$) whereas the highest voltage is seen when the PV output is at its rated value and there is no load in the circuit (i.e. $x_l = 0, x_{pv} = 1$). It is important here to note that although equation (3.12) is highly non-linear, the resulting manifold exhibits a somewhat linear behavior, as shown in Figure 3.3. The plotted surface in Figure 3.3a is a first order polynomial which represents the simulated data with an R^2 of 0.999. The linear sensitivity model exploits this

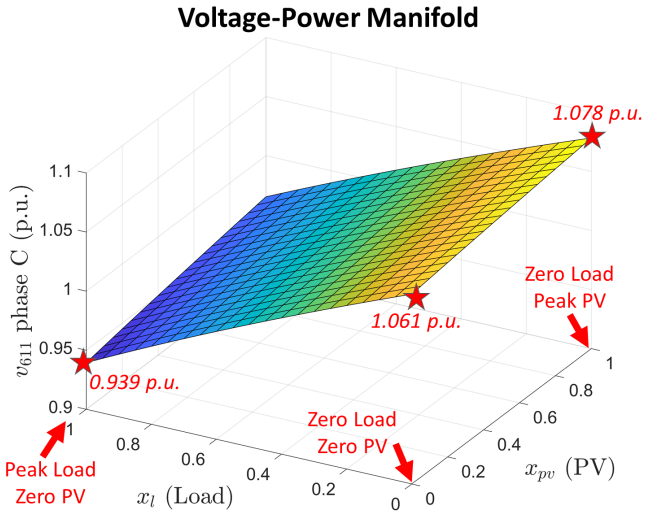
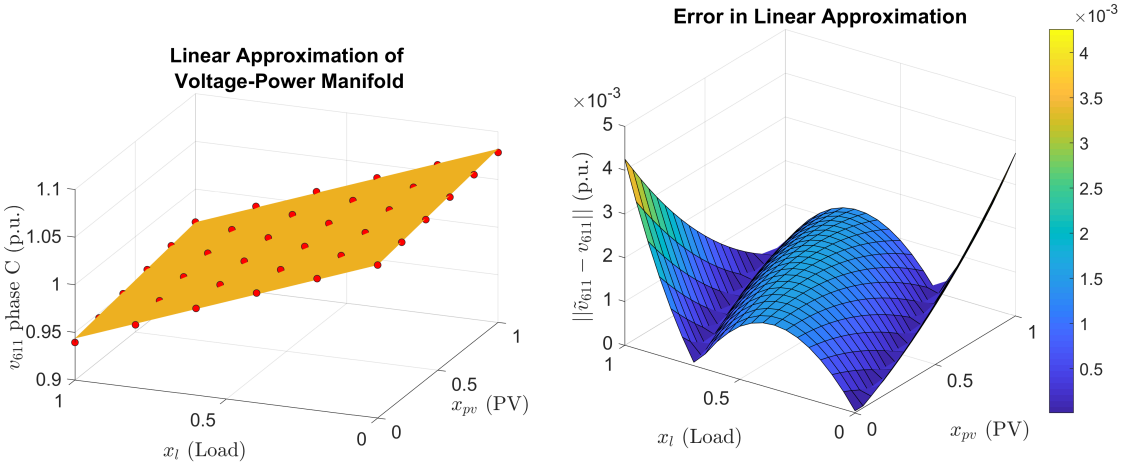


Figure 3.2: Voltage-power manifold for bus 611 phase C obtained by solving 441 discrete power flows. The voltage magnitude at various values of x_l and x_{pv} is represented by red stars.



(a) A first order polynomial approximation of the power flow manifold. The points in red denote the actual solution of Equation (3.12) whereas the yellow surface represents their linear approximation.

(b) Absolute error due to linear approximation.

Figure 3.3: A linear approximation of the voltage-power manifold and the resulting estimation error. As the voltage deviation from the nominal increases in either direction, the non-linearity is more pronounced and therefore, the approximation error tends to increase.

strong correlation between phase voltage magnitude and power injections in the circuit, by creating a linearization of the voltage-power manifold. This allows for a quick estimation of voltage sensitivity coefficients which can then be used to create a mapping between QSTS inputs and outputs. The following section presents a formal mathematical formulation of the linear sensitivity model.

3.4 Linear Sensitivity Model Formulation

3.4.1 Basic Model for Bus Voltage

We start by developing a model for the bus voltage in an unbalanced distribution circuit with no controllable elements. Let $v_{\phi}^{(j)}$ denote the dependent variable which represents the phase-to-ground voltage magnitude of phase $\phi \in \{A, B, C\}$ at bus j. Without loss of generality, we drop the subscript ϕ to keep the formulation concise. Moreover, for an h-bus network, we form the voltage vector $\mathbf{v} = [v^{(1)}, v^{(2)}, ..., v^{(h)}]^{\top}$. Furthermore, let $\mathbf{x} = [1, x_1, ..., x_p]$ be the vector of p independent variables with x_p representing the p^{th} load or PV profile of power injections. We assume that there exists a linear relationship between $v^{(j)}$ and $\mathbf{x}$ given by,

$$v^{(j)} = \alpha_0 + \beta_1 x_1 + ... + \beta_p x_p \tag{3.14}$$

where β_i are the voltage sensitivities defined as,

$$\beta_i = \frac{\partial v^{(j)}}{\partial x_i}, \qquad \forall i \in \{1, 2, ..., p\} \tag{3.15}$$

In context of geometry, equation (3.14) represents a hyperplane with coefficients $\mathcal{H}^{(j)} \triangleq [\alpha_0, \beta_1, ..., \beta_p]$ uniquely characterizing a p dimensional flat in $\mathbb{R}^{p+1}$. The plane slopes $\beta_i \in \mathcal{H}^{(j)}$ capture the impact of each profile on the voltage at bus j. A higher magnitude of β_i indicates that the bus voltage is more sensitive to the variation in the profile x_i. Since the power injections in the distribution circuit impact the voltage at each bus differently, we propose (3.14) for every bus in the circuit.

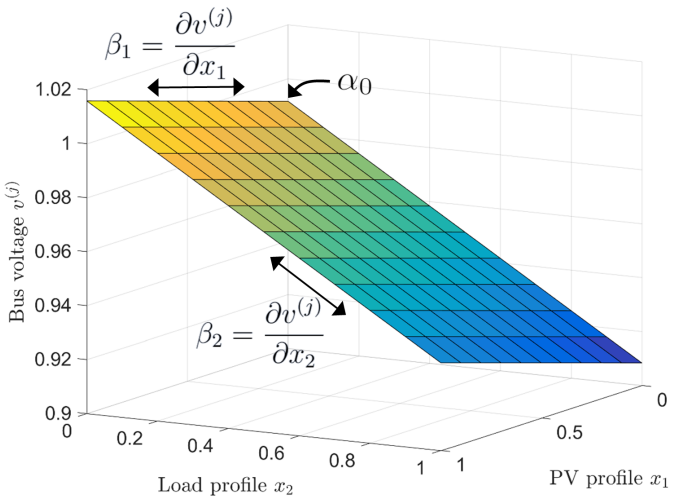
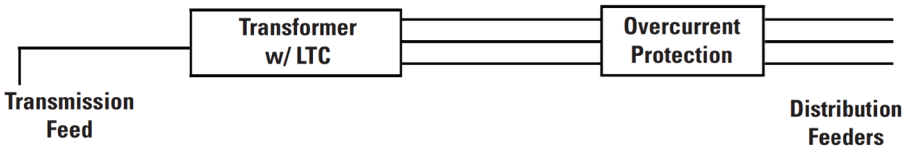


Figure 3.4: Voltage plane (p.u.) for bus j for a load and a PV profile.

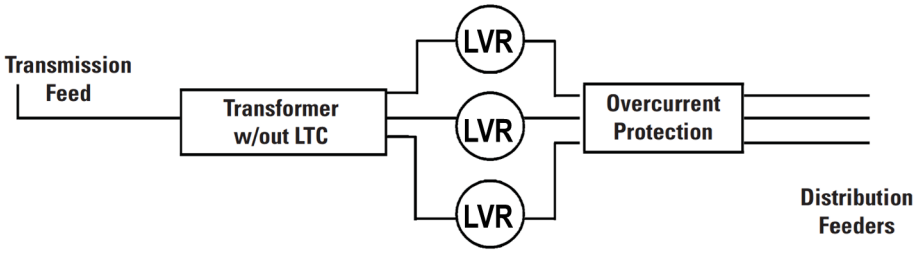
Figure 3.4 shows a voltage plane in $\mathbb{R}^3$ for a single load and a PV profile characterized by $\mathcal{H}^{(j)} = [0.99, 0.024, -0.083]$. Since increasing the load decreases the bus voltage, β_2 has a negative value. Due to the non-linearity of power flow equations, the bus voltages are not strictly linearly correlated to the power injections, as shown earlier. However, for localized variations in power injections, the linearity assumption produces a small error that is bounded (see Figure 3.3b).

3.4.2 Operation of Voltage Regulators and Capacitor Banks

As the distance from the substation increases, the voltage tends to drop due to Kirchhoff's laws. In addition, varying loading conditions also impact the voltage profile. Voltage regulators are therefore used to maintain the feeder voltage within a specified range. They accomplish this by changing their tap positions to vary the turns ratio, thereby increasing or decreasing the downstream bus voltages. To reduce oscillations, deadbands and delays are incorporated in the controller logic for these devices. Oftentimes, substation transformers have an inbuilt on-load tap changer that regulates the voltage of all the three phases combined (i.e. gang-operated). A major disadvantage of this configuration is that whenever one phase of the LTC fails, the entire package is removed from service. To address



(a) Circuit configuration when using an LTC



(b) Circuit configuration when using an LVR

Figure 3.5: Comparison of LTC and LVR circuit configurations.

this issue, electric utilities often use line voltage regulators which control each phase of the system independently (see Figure 3.5). This decoupling significantly reduces down time and allows for a more precise voltage control of each phase. The operating principle of both these devices is essentially the same therefore, we collectively refer to them as voltage regulators.

Let V_r denote the input control voltage to the regulator. Usually, it is the voltage across the secondary winding of the regulator unless line drop compensation is used. Furthermore, let V_{min} and V_{max} denote the lower limit and the upper limit of the regulator deadband respectively. If V_r falls below V_{min}, the regulator tap position increases, which steps up V_r. Similarly, if V_r goes above V_{max}, the regulator tap position decreases causing a drop in V_r. These corrective control actions continue until V_r falls back within the regulator deadband. However, in case the regulator tap is already at an extreme position, no action is taken.

To incorporate the impact of regulators on bus voltage, we create a new voltage plane each time a regulator changes its tap position. Figure 3.6 shows the planes for control voltage V_r for two different tap positions. The horizontal plane formed by $V_{min} = 0.98$ defines the lower limit for the regulator deadband. Plane 1 corresponds to the current position of the regulator tap and as such control voltage is confined to this plane based on

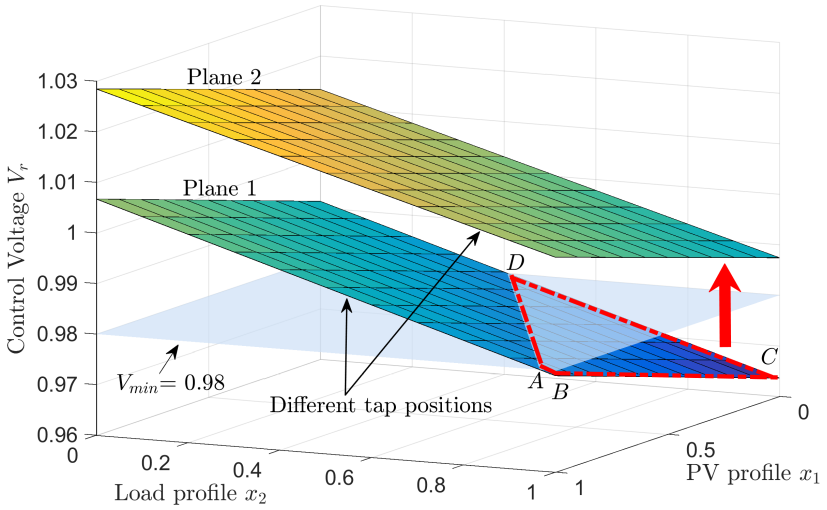


Figure 3.6: Impact of regulator tap position on the control voltage plane. If V_r goes below V_{min}, a tap change is triggered causing V_r to shift from plane 1 to plane 2.

(3.14). The intersection of the two planes forms the line AD. As soon as V_r enters the region defined by the quadrilateral $ABCD$, a tap action is triggered. This is because every point in the region $ABCD$ corresponds to a value of V_r lower than V_{min}. The tap change causes V_r to jump from plane 1 to plane 2 and remain on it as long as it stays within the deadband. Therefore, by using multiple planes, we can predict the regulator tap positions and transitions.

Capacitors can regulate the reactive power in distribution circuits by switching on and off based on a control signal which can either be voltage, current, temperature or power factor. In our model, we consider capacitor banks which rely on a voltage signal for their operation. Unlike the regulators however, capacitors generally have only two states i.e. they are either connected (on) or disconnected (off). Let V_c denote the input control signal to the capacitor. If V_c falls below the minimum voltage threshold V_{on}, the capacitor switches to the on state. Conversely, if V_c goes beyond the maximum voltage threshold V_{off}, the capacitor switches off. Figure 3.7 shows the planes for control voltage V_c corresponding to the two states of the capacitor.

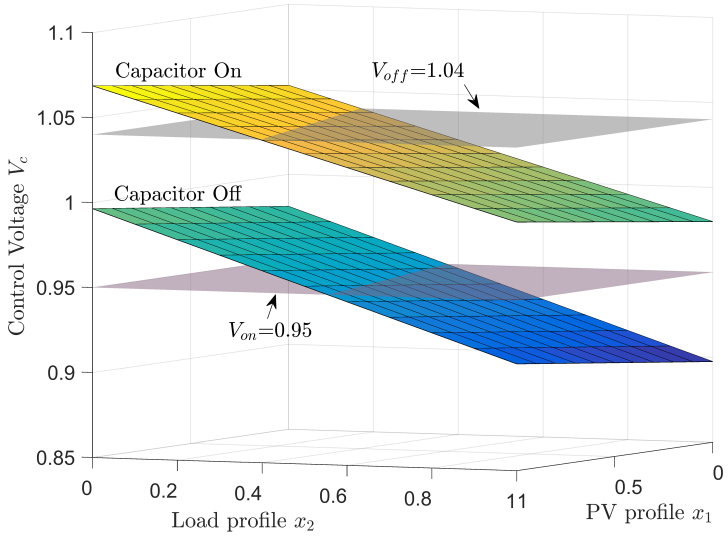
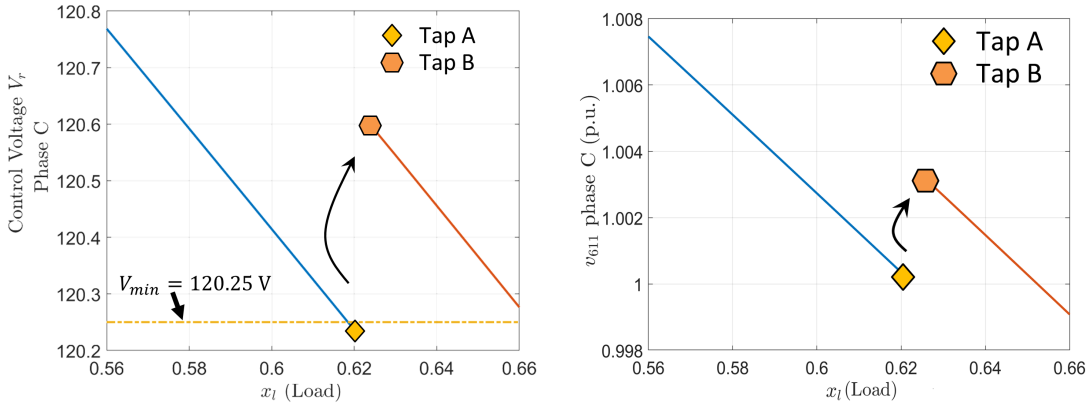


Figure 3.7: Impact of capacitor state on the control voltage plane. If V_c goes below V_{on}, the capacitor turns on causing V_c to jump from one plane to the other and vice versa.

3.4.3 Bus Voltage Model with Controllable Elements

For a distribution feeder with multiple controllable elements, we need to create a new plane for bus voltages each time a regulator tap action occurs or a capacitor changes its state. This is because each change creates a discrete jump in the bus voltages across the entire feeder. Based on the network topology, some buses will experience a small change while others will see a significant discontinuity in the voltage profile. To further illustrate this phenomenon, we utilize the modified IEEE 13-bus test circuit, discussed earlier in this chapter. The voltage regulator at the substation is now enabled and is allowed to change its state depending upon the control signal. Figure 3.8a shows the control voltage of the single-phase regulator monitoring the phase C at the substation. The PV power injection is fixed to a constant value ($x_{pv} = 0.5$) and the circuit loading is varied by changing x_l. The moment control voltage goes outside the lower boundary of the deadband ($V_{min} = 120.5V$), a delay timer is initiated. Once the timer runs out, the regulator changes its tap position, which causes a jump in the voltage-power manifold (see Figure 3.8b). An important observation to note here is that estimation errors in the states of controllable elements can cause significant errors in the resulting estimated voltage magnitude.



(a) Control voltage of the regulator ($120V_{base}$)

(b) Voltage magnitude at bus 611

Figure 3.8: Impact of regulator tap action on the voltage-power manifold. The results are obtained by solving Equation (3.12) in OpenDSS.

For a circuit with m controllable elements, let $u_m(t)$ denote their respective states at time t. For a regulator i with 33 tap positions, $u_i(t) \in \{0, 1, .., 32\}$. Similarly, for a capacitor bank j, $u_j(t) \in \{0, 1\}$. Furthermore, for ease of notation we refer to the set of voltage regulators and capacitor banks as *system controllers* and define the system controller state at time t as,

$$s_t = T(u_1(t), .., u_m(t)) \tag{3.16}$$

where $T : \mathbb{Z}^r_{\geq} \rightarrow \mathbb{Z}_+$ is a hashing function that produces a unique positive index for every different combination of inputs. For example, in a circuit with 2 regulators and 1 capacitor, $s_t = 1$ might correspond to regulator A at tap position 2, regulator B at tap position 6 and a capacitor that is in an off state. The voltage at bus j at time t is then given by,

$$v^{(j)}(t) = \mathcal{H}^{(j)}_{s_t} \mathbf{x}^\top(t) \tag{3.17}$$

where $\mathcal{H}^{(j)}_{s_t} = [\alpha_0, \beta_1, ..., \beta_p]^{(j)}_{s_t}$ is the vector of plane coefficients indexed by s_t. Equation (3.17) essentially states that each time the system controller state changes, a new set of plane coefficients characterize the voltage hyperplanes.

3.5 Estimation using Multiple Linear Regression

The fidelity of the proposed linear sensitivity model (3.17) is greatly influenced by the estimation quality of the plane coefficients corresponding to a particular system controller state. In addition, the total feasible system controller states can be considerably large depending upon the type and number of controllable elements in the feeder. For example, a feeder with 2 regulators (33 taps) and 2 capacitor banks, has a space of $33^2 \times 2^2 = 4356$ feasible system controller states. However, in practice this space of possible system controller states is extremely sparse [81]. This is because of the cyclic nature of the time series data which causes the system controller states to repeat when running a brute-force QSTS simulation. To exploit this sparsity, we propose estimating the plane coefficients for only the unique system controller states that are observed during the time series simulation.

In order to accurately compute the plane coefficients and efficiently determine the controller states, we propose a multiple linear regression based perturb-and-observe estimation methodology. The objective here is two-folds: computing the plane coefficients $\mathcal{H}_{s_t}^{(j)}$ for all the buses and estimating control voltages to determine the controller states.

3.5.1 Computing Plane Coefficients

Using the framework of multiple linear regression, we can determine the plane coefficients for a given system controller state s_t. For n PV and k load profiles of power injections, we only need $n + k + 1$ observation to estimate $\mathcal{H}_{s_t}^{(j)}$. However, since bus voltages and power injections are not exactly linearly correlated, we use $n + 2k + 1$ observations to minimize the linearization error. To accurately capture the sensitivity of the bus voltages to each of

the load/PV profiles, we propose the design matrix $\boldsymbol{X}$ with the following structure,

$$\boldsymbol{X} = \begin{bmatrix} 1 & x_1(t) & \dots & x_k(t) & 0 & 0 & \dots & 0 \\ 1 & \vdots & \dots & \vdots & 1 & 0 & \dots & 0 \\ \vdots & \vdots & \dots & \vdots & 0 & 1 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ \vdots & x_1(t) & \dots & x_k(t) & 0 & 0 & \dots & 1 \\ \vdots & x_1(t) - \delta & & \vdots & 1 & 1 & \dots & 1 \\ \vdots & x_1(t) + \delta & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ \vdots & \vdots & & x_k(t) - \delta & 1 & 1 & \dots & 1 \\ 1 & x_1(t) & \dots & x_k(t) + \delta & 1 & 1 & \dots & 1 \end{bmatrix} \tag{3.18}$$

$$\underbrace{\qquad\qquad}_{k \text{ Load profiles}} \qquad \underbrace{\qquad}_{n \text{ PV profiles}}$$

where $\delta \in [0.05, 0.1]$ and $x_k(t)$ is the value of k^{th} load profile at time t. Following are some important observations regarding $\boldsymbol{X}$,

1. $\boldsymbol{X}$ has a full rank, $n + k + 1 \leq n + 2k + 1$

2. The number of observations required to estimate plane coefficients increase linearly with the number of profiles

3. PV profiles have greater temporal variability than load profiles, therefore the sensitivity of bus voltage to PV power injection is measured over the complete range i.e. from 0 to 1.

4. Sensitivity of bus voltage to load profiles is measured at the present value of load power injection and its δ-neighborhood.

5. The value of PV power injection is kept constant when measuring the sensitivity of bus voltage to the load profiles and vice versa.

It is worthwhile mentioning here that the proposed estimation technique can accommodate other types of time series profiles as well including power output of an energy storage system or the charging of electric vehicles etc. After forming the design matrix $\boldsymbol{X}$, the vector of observed bus voltages $\boldsymbol{Y}^{(j)} \in \mathbb{R}^{n+2k+1}$ is obtained by solving the nonlinear power flow equations corresponding to each observation. Using the ordinary least squares estimator, the plane coefficients corresponding to a given system controller state s_t are then given by,

$$\mathcal{H}_{s_t}^{(j)} = (\boldsymbol{X}^\top \boldsymbol{X})^{-1} \boldsymbol{X}^\top \boldsymbol{Y}^{(j)} \tag{3.19}$$

The matrix $(\boldsymbol{X}^\top \boldsymbol{X})^{-1} \boldsymbol{X}^\top$ is called the Moore–Penrose pseudoinverse. It will always exist since $\boldsymbol{X}$ has a full rank [79].

3.5.2 Estimating Controller States

Accurately estimating the controller states is vital because of the dependency of plane coefficients on the system controller state. As mentioned earlier, the regulator tap position and the capacitor state are determined by the control voltages seen by the respective devices. Once the plane coefficients are computed, the control voltages can be easily estimated by evaluating (3.17) for the specific buses, which are being monitored by the controllers. If the estimated voltages are within the deadband, no controller action occurs. Otherwise the regulator tap position is changed or the capacitor is switch on/off according to the type of controller, control logic, and delays. This causes the system to transition to a new state for which the plane coefficients are again computed.

3.6 Fast QSTS Simulation using Linear Sensitivity Model

In this section, we discuss how to perform fast QSTS simulation using the linear sensitivity model. Let T_f and $\mathcal{N}$ denote the time horizon of the QSTS simulation and the set of all the

buses in the circuit, respectively. Furthermore, let $\mathcal{C} \subset \mathcal{N}$ denote the set of buses whose voltages are monitored by the control elements.

Figure 3.9 shows a detailed flow chart of the proposed algorithm. Upon initialization at $t = 0$, the circuit is compiled once to obtain the present states of voltage regulators and capacitor banks. During the compilation process, the input time series profiles are also loaded into the memory. The next step is to formulate $\mathbf{x}$, which involves reading the value of input time series vectors at t. After updating s_t, based on the present states of controllable elements, the algorithm checks to see if a linear sensitivity model exists. If s_t is unique and has not been observed before, a linear approximation of the voltage-power manifold is generated around present the value of load and PV power injections. The block in red, which is used to compute the plane coefficients for all the buses, is the only part of the algorithm that requires solving the nonlinear AC power flow equations. However, once the plane coefficients corresponding to a system controller state s_t are computed, they are stored in a look up table using matrix indexing. In this manner, the algorithm keeps track of the system controller states encountered through time and reuses the plane coefficients every time a similar state is encountered. After estimating the control voltages, the next step is to establish if they lie within the deadbands of the respective devices. If they do, the controller states remain unchanged and the simulation steps through time, otherwise the controller logic determines the appropriate states of the controllers for the next time interval. The controller logic for regulators and capacitor banks is fairly straightforward and involves the following steps:

1. A delay timer is initiated the moment control voltage of a regulator or a capacitor bank escapes the predefined deadband. The goal of the timer is to ensure that the in-built delay period has passed before any control action is taken. If the control voltage slides back within the deadband before the time delay period has elapsed, the timer is reset and no control action is taken.

2. If the control voltage is outside the deadband after the time delay period has elapsed,

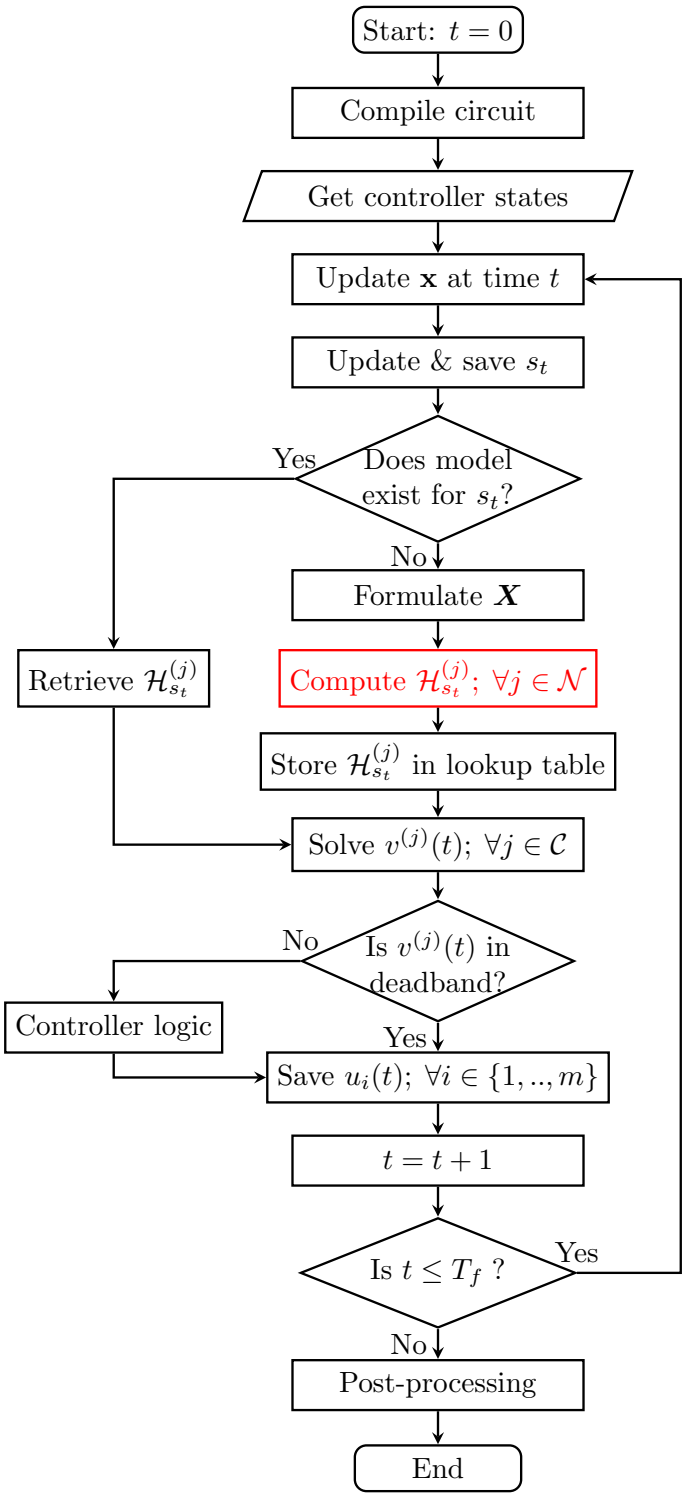


Figure 3.9: Flow chart of the proposed algorithm for fast QSTS simulation at 1-second resolution.

the next step is to check if the it exceeds the upper or the lower boundary of the deadband. This determines what type of action is required to bring the control signal back within the deadband. For example, in case of a voltage regulator, if the control signal exceeds the upper boundary of the deadband, a decrease in tap position would be the desired control action.

3. The last step is to check if the desired control action is physically possible. For example, a voltage regulator that is already at its lowest tap position cannot execute any action to further reduce the control voltage.

4. Sometimes, a deadtime is also added to the controller logic which causes a delay in successive device operations. This can be easily accounted for by initiating a timer after the controller action has occurred.

After the completion of time series simulation, the post-processing block computes the important QSTS metrics that will be discussed in the subsequent section.

3.6.1 QSTS Metrics

The most important aspect of running a QSTS simulation is to accurately produce a set of output metrics that will quantify the impacts of PV on a distribution feeder. The proposed algorithm can be used to study voltage-related impacts which are listed in Table 3.1, along with their acceptable absolute accuracy thresholds. These thresholds have been established

Table 3.1: Voltage-related PV impact metrics measured by QSTS

	QSTS Metrics	**Error Threshold**
1	Total regulator tap actions	10%
2	Total capacitor switching operations	20%
3	Highest/lowest voltage on the feeder	0.005 pu
4	Per phase highest/lowest voltage at each bus	0.005 pu
5	Duration of ANSI voltage violations	24 Hrs

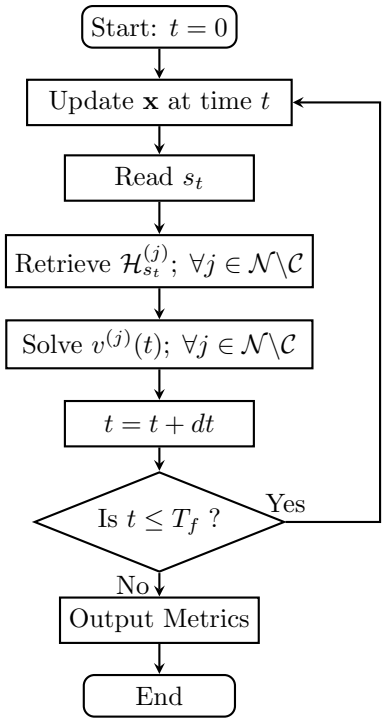


Figure 3.10: Flow chart of the voltage reconstruction process using uniform time-step

in [18]. The motivation for these metrics comes from [8], where the authors present a detailed discussion on voltage issues arising in feeders with significant PV penetration. Metrics 1-2 can be easily computed since the proposed algorithm keeps track of controller states at each time instant. For metrics 3-5, the phase voltage profile at each bus is required, which can be obtained by evaluating equation (3.17), $\forall j \in \mathcal{N} \backslash \mathcal{C}$, at each time-step. Since, the plane coefficients for each bus, at every time instant are already computed, estimating phase voltages only requires a multiplication operation (see equation (3.17)). We refer to this process as *reconstruction* of the voltage profile.

One of the most unique aspects of the proposed fast QSTS algorithm is its ability to decouple the estimation of controller states and the reconstruction of voltage profiles. This is important because metrics 1-2 are much more sensitive to the time-step of the QSTS simulation as compared to metrics 3-5. Authors in [18] suggest using a high resolution QSTS to evaluate the impact of distributed PV on voltage regulating devices to ensure the error thresholds in Table 3.1 are met. On other hand, extreme feeder voltages and ANSI

violations can be estimated using larger time-steps. The fast QSTS algorithm exploits this finding by estimating the controller states at the smallest possible time-step whereas, allowing flexibility in reconstructing the voltage profiles at a much coarser resolution. The flow chart diagram of voltage reconstruction using a uniform time-step, dt, is shown in Figure 3.10. The value of dt can range anywhere from 1-second up to an hour.

3.7 Simulation Case Study: IEEE 13-Bus

To evaluate the performance of the fast QSTS algorithm, a variety of test cases are discussed throughout this dissertation. All of these test cases represent unbalanced, 3-phase distribution systems. The modified IEEE 13-bus test case, introduced earlier in this chapter, is used as a starting point. The single line diagram of the test case is shown in Figure 3.1. There are a total of 4 voltage regulating devices installed in the feeder. The substation has 3 single-phase voltage regulators with line drop compensation (LDC), each with a total of 33 tap positions. In addition, there are two capacitor banks in the circuit, however, only one of them is controllable (at bus 675). All the loads in the circuit are assigned a 1-second resolution, yearlong power injection profile. This data set is obtained by linearly extrapolating the 5-minute SCADA measurements obtained from a utility in California. Furthermore, a 3-phase utility scale 2 MW PV system operating at unity power factor, is

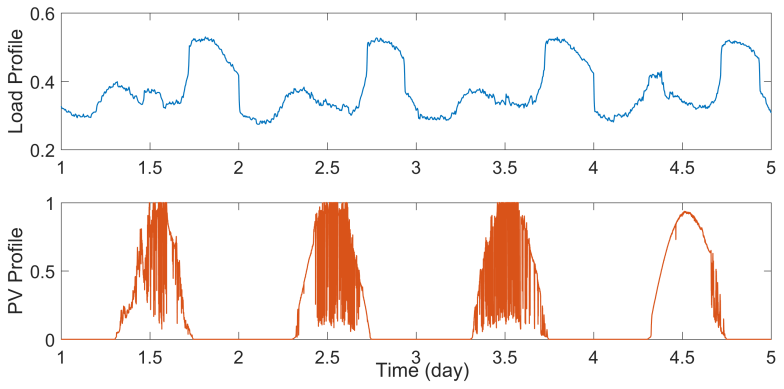


Figure 3.11: Load and PV power injection profiles for the QSTS simulation. Notice the variability in the PV profile which models the impact of a cloud passing over the PV site.

Table 3.2: Characteristics of IEEE 13-Bus test case

Name	Buses, Nodes	Voltage (kV)	Peak Load (MW)	Length of Feeder	Regulating Devices	PV Penetration	Total Profiles
IEEE 13-bus	16, 41	4.16	4.3	1.5 km	3 LVRs with LDC, 1 switching cap bank	40%	2

installed at bus 675. This system is also assigned a unique 1-second resolution, yearlong power injection profile. The PV power output for this profile is synthesized from global horizontal irradiance data at NREL Oahu site [82] by using DIRINT decomposition model, Hay/Davies transposition model, and the Sandia Array performance model [83]. Figure 3.11 shows four days of data for the two input time series profiles used for this test circuit. Other important characteristics of this test circuit are shown in Table 3.2.

3.7.1 Simulation Setup

A MATLAB based software tool is developed to run the proposed fast QSTS algorithm. The test circuits are modeled in OpenDSS, which is linked to the MATLAB tool via COM interface. Figure 3.12 shows the block diagram of the simulation setup. The time series profiles are fed to the software tool which utilizes the linear sensitivity model to speed up the QSTS simulation. The controller logic for all the controllable elements is written in MATLAB, and OpenDSS is only used for solving the nonlinear AC power flow equations. The COM interface allows the software tool to interact with the feeder model (update the

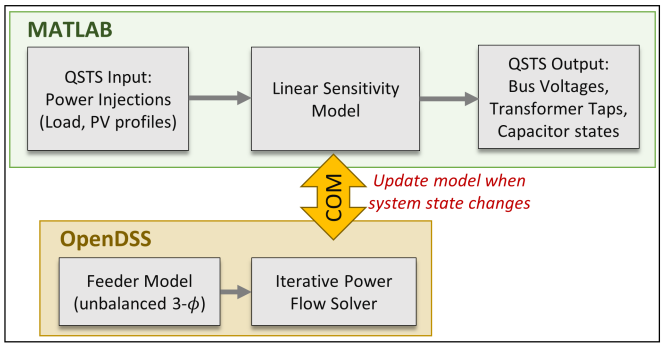


Figure 3.12: Simulation setup for the proposed fast QSTS algorithm.

states of regulators and capacitor banks) and extract power flow solutions. Whenever a new system state is observed, the response vector $\boldsymbol{Y}^{(j)},\ \forall j \in \mathcal{N}$ is updated by solving the power flow problem corresponding to each row in the design matrix $\boldsymbol{X}$. The plane coefficients are then estimated using equation (3.19).

3.7.2 Simulation Results

Table 3.3 shows a comparison of the QSTS simulation results obtained by using brute-force method and the proposed fast QSTS algorithm. The estimation error is calculated by comparing the results of the proposed algorithm with the baseline 1-second resolution, yearlong brute-force QSTS. The ANSI Range A standard for medium voltage systems is used to determine the duration of ANSI voltage limit violations (126/117 V on a 120 V_{base}). The proposed algorithm produces an average error of 3.6% in tracking the states of controllable devices. Figure 3.13 shows a comparison of the states of voltage regulator (Vreg 1), installed at phase A of the substation, through time. The plot in blue corresponds to the actual controller state obtained through the brute-force solution whereas, the overlaid red plot shows the estimated states obtained by running the proposed fast QSTS algorithm. The regulator operation is significantly impacted by the PV system which is evident from the oscillations observed in Figure 3.13.

The voltage reconstruction is performed at a uniform time-step of 60 seconds. A zero-order hold filter is used to estimate the value of voltage in between the time-steps. Figure 3.14 shows the impact of dt on the estimated voltage profile of bus 611, phase C. A smaller value of dt results in a voltage profile that closely resembles the one obtained by the brute-force simulation (see Figure 3.14a). As the value of dt increases, the reconstruction accuracy decreases which can cause significant errors in calculating extreme nodal voltages as well as duration of ANSI violations. For the 13-bus test case, a dt of 60 seconds produces a root mean square (RMS) error of 0.0006 p.u. in estimating the highest voltage at each node. Figure 3.15 plots this absolute error for each node. The error is almost negligible for

Table 3.3: Accuracy comparison of the fast QSTS algorithm (IEEE 13-bus)

QSTS Metric	**Brute-force**	**Fast QSTS (error)**
Regulator tap actions:		
VReg 1 (A-ϕ)	7056	+4.32%
VReg 2 (B-ϕ)	7233	+4.78%
VReg 3 (C-ϕ)	8460	+1.63%
Capacitor switches:		
Cap 1 (3-ϕ)	2506	+3.83%
Feeder phase voltage:		
Highest	1.0607 p.u.	<0.0001 p.u.
Lowest	0.9673 p.u.	<0.0001 p.u.
Duration of ANSI violations:		
Over voltage	22.13 Hrs	+1.40 Hrs
Under voltage	11.46 Hrs	+0.19 Hrs
Per phase voltage (each bus):	total of 41 nodes	
Highest	0.0006 p.u. (mean error)	
Lowest	0.0004 p.u. (mean error)	

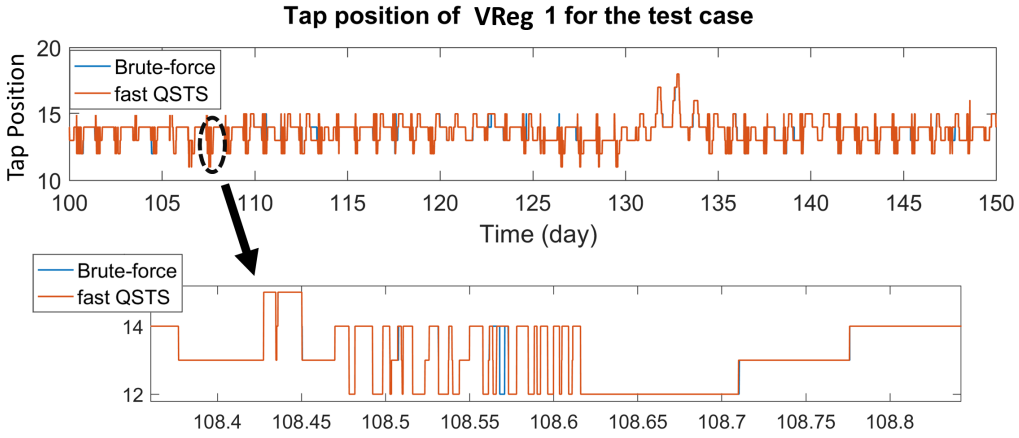
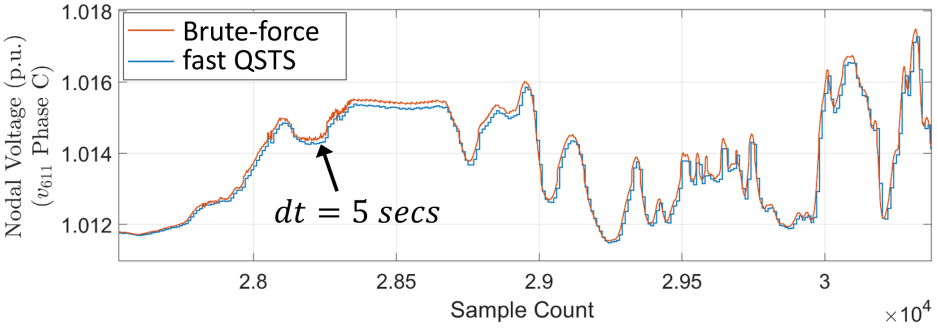
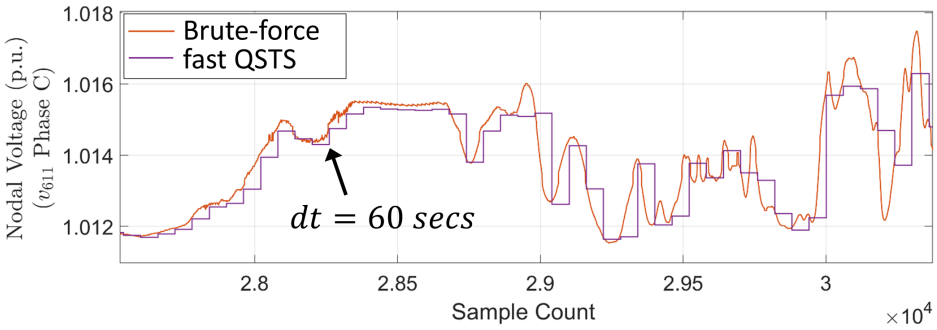


Figure 3.13: Tap position of VReg 1 for 50 days obtained using the brute-force method and the proposed fast QSTS algorithm. Regulator tap varies from 1 (lowest) to 33 (highest).



(a) Voltage reconstruction at $dt = 5$ seconds



(b) Voltage reconstruction at $dt = 60$ seconds

Figure 3.14: A comparison of voltage profiles obtained using brute-force method and the proposed fast QSTS algorithm. As the reconstruction time-step increases, the estimation error also increases due to the zero-order hold filter.

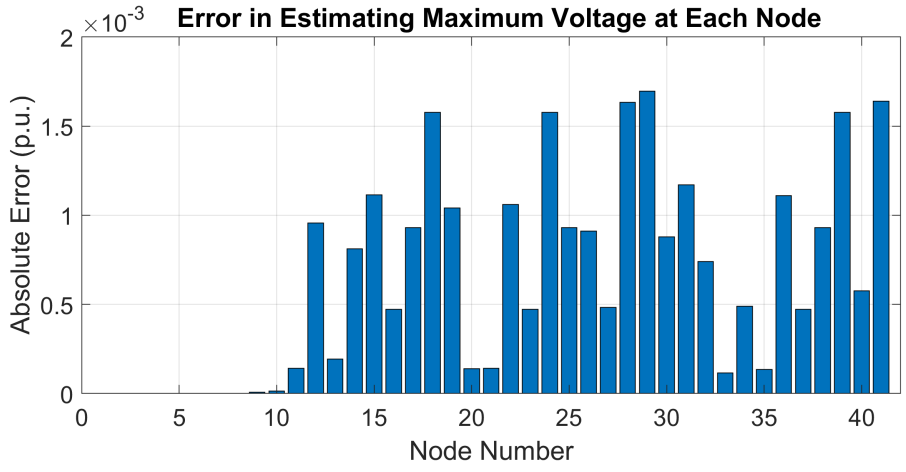


Figure 3.15: Estimation error in calculating the per phase maximum voltage at each bus (or maximum voltage at each node) observed during the yearlong, 1-second resolution QSTS.

nodes 1-9 since they are very close to the substation and hence, observe a minute voltage drop. Depending upon the application specific requirements, the voltage reconstruction can be performed with the desired accuracy level by selecting appropriate dt in the post-processing block. A novel nonuniform voltage reconstruction technique is discussed in section 4.2 that significantly reduces the estimation errors while allowing a larger value of dt.

3.7.3 Analysis of Computation Time

The total time taken by the proposed algorithm, T_{sol}, is given by,

$$T_{sol} = T_p + T_c + T_r \tag{3.20}$$

where T_p, T_c is the time taken to compute the plane coefficients and the controller states, respectively, and T_r is the total time required for reconstructing the voltage profile at each node. The proposed linear sensitivity model requires new plane coefficients every time the system controller state changes. Furthermore, for every new unique state, equation (3.19) has to be evaluated which requires solving $n + 2k + 1$ nonlinear AC power flow equations. Consequently, the total number of power flows solved by the proposed algorithm, N_{PF}, is given by,

$$N_{PF} = (n + 2k + 1)N_s \tag{3.21}$$

where N_s is the total number of unique system controller states observed for the given time horizon. Therefore, T_p is directly proportional to N_{PF}. For the 13-bus test case, a total of 205 unique system controller states are observed by the proposed fast QSTS algorithm. Figure 3.16 shows the monthly distribution of N_s over the yearlong time horizon. As the simulation progresses through time, the number of new unique states decreases drastically. This is because of the cyclic nature of regulator and capacitor states, which tend to repeat themselves. Furthermore, the load profile reaches peak values only during the summer,

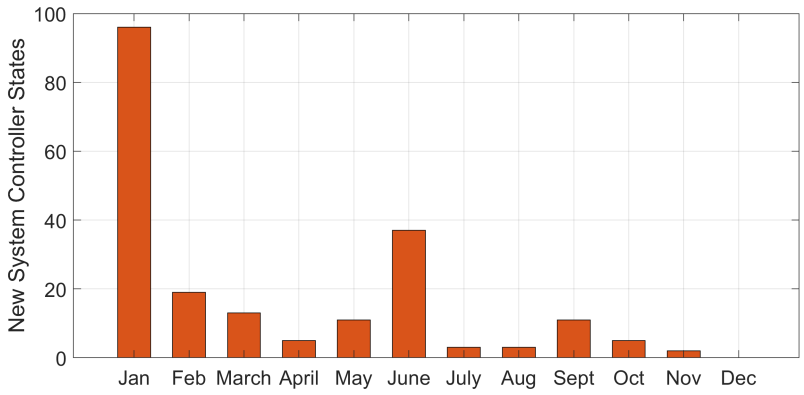


Figure 3.16: New system controller states observed by the proposed fast QSTS algorithm for the yearlong simulation.

which results in voltage regulators observing rather extreme tap positions. This explains the sharp rise in N_s for the month of June. Since we only have two profiles, the total number of power flow solutions required for each unique system controller state is 4. Therefore, from equation (3.21), the total number of AC power flow solutions required by the proposed algorithm is 820. Compared to the brute-force approach, which solves power flows at each time-step, the proposed algorithm drastically reduces the total number of power flows solved which in turn causes a significant reduction in the computation time.

Estimation of controller states and reconstruction of voltage profiles requires evaluating equation (3.17), which is essentially a matrix multiplication operation. The time taken by any matrix operation is linearly correlated to its size. Therefore, T_c is dependent upon the number of input time series profiles (rows) and the total number of controllers in the circuit (columns). Similarly, T_r is dictated by the number of input profiles along with the total number of buses in the circuit. In addition, since reconstruction is performed at uniform time-steps, T_r is also dependent upon dt. A larger value of dt would result in fewer evaluations of equation (3.17), thereby reducing T_r.

Table 3.4 shows the time taken by the proposed fast QSTS algorithm. It is able to compute all the voltage-related impact metrics in 13.2 seconds[1], which represents a computa-

[1]The computation time of the proposed algorithm includes the communication overhead between MATLAB and OpenDSS (due to COM calls), unless otherwise stated.

Table 3.4: Timing comparison of the fast QSTS algorithm (IEEE 13-bus)

	Brute-force	**Fast QSTS**	**% Reduction**
Total time taken	14.25 mins	13.2 secs	98.46%
Power flow solutions	31.5 million	820	99.99%

tional time reduction of 98.46% when compared to the brute-force method[2]. This reduction in computation time is primarily due to the fact that the proposed method only solved 820 AC power flows while running the 1-second, yearlong QSTS simulation.

[2]The brute-force simulations were performed natively in OpenDSS and the computation time is reported based on that. All simulations were performed on a Windows 10 machine with 32 GB of RAM and 3.50 GHz processor.

CHAPTER 4
ACCURACY, SCALABILITY AND ROBUSTNESS OF THE FAST QSTS ALGORITHM

The fast QSTS algorithm, developed in chapter 3, shows promising results on a small test case. However, certain aspects of this algorithm need to be improved to ensure scalability and robustness. In this chapter, we propose a more accurate method to create a local linearization of the voltage-power manifold that drastically reduces the errors in estimating the states of voltage regulators and capacitor banks. In addition, a nonuniform voltage reconstruction technique is also developed that selects the time instances where voltage extremities are more likely to occur, thereby further improving the estimation quality. Towards the end of the chapter, two utility-scale distribution feeders are used as test cases to evaluate the robustness, accuracy and scalability of the proposed algorithm.

4.1 Linearization of the Voltage-Power Manifold

The linear sensitivity model, proposed in the previous chapter, exploits the correlation between phase voltage magnitude and power injections in the circuit. The underlying idea is to introduce a variation around the operating point (perturb), and measure its corresponding impact on the bus voltages (observe). The operating point is just the value of load and PV power injections at a given time t obtained from the input profiles. We use the framework of multiple linear regression to create a linearization of the voltage-power manifold. The rows of the design matrix $\boldsymbol{X}$ are the query points, which represent the perturbed exogenous power injections. Solving the nonlinear AC power flow equations for each of these query points allows us to create a response vector $\boldsymbol{Y}^{(j)},\ \forall j \in \mathcal{N}$, which represents actual points on the voltage-power manifold. Once enough observations are obtained, an ordinary least squares (OLS) estimator is used to calculate the plane coefficients of the linearized

manifold.

The accuracy of the OLS estimator is greatly influenced by the number of observations. Figure 3.3b shows the residual error in estimating bus voltage magnitude using OLS, for the 13-bus test case. It uses a uniform grid of 36 query points (6 for each dimension) to obtain the response vector, corresponding to which the plane coefficients are computed. Such an approach, however, suffers from scalability issues. This is because the number of nonlinear AC power flow solutions required to estimate the plane coefficients increases exponentially as more power injection profiles are added. For the above example, adding another load or PV profile would require 216 power flow solutions (6^3) to obtain the response vector. Furthermore, if the state of a voltage regulator or a capacitor bank changes, new plane coefficients are required to estimate the bus voltages. As a result, the total number of power flow solution required by the fast QSTS algorithm increases drastically causing a proportional increase in the computation time.

The structure of $\boldsymbol{X}$ proposed in equation (3.18) overcomes this limitation by systematically choosing the query points. It ensures that $\boldsymbol{X}$ has a full rank and the number of query points always increase linearly with the number of profiles. However, it does not take into account the value of PV power injection at time t. Instead, it arbitrarily chooses a value of 0 and 1. This creates a linearization of the voltage-power manifold that is not around operating point. Furthermore, it is not clear how much of a variation in load power injection yields the optimal performance of the algorithm. In this section, we develop a sensitivity-based linearization technique that significantly reduces the error in estimating the controller states. The analysis is presented for the IEEE 13-bus test circuit with a single load and a PV profile. For simplicity sake, we assume that there is only one single phase regulator at the substation (VReg 1). However, without the loss of generality, the results presented in this section can be extended to any number of controllable elements and input time series profiles.

4.1.1 Local Linearization

As the name suggests, this method aims at creating a local linearization of the voltage-power manifold by perturbing the system around the operating point. For the IEEE 13-bus test circuit, the operating point of the feeder is given by $x^* = (x_l(t), x_{pv}(t))$. Hence, the most efficient approach is to independently introduce a small variation δ in both x_l and x_{pv} as follows,

$$\boldsymbol{X} = \begin{bmatrix} 1 & f_1(x_l + \delta) & x_{pv} \\ 1 & f_2(x_l - \delta) & x_{pv} \\ 1 & x_l & f_1(x_{pv} + \delta) \\ 1 & x_l & f_2(x_{pv} - \delta) \end{bmatrix} \tag{4.1}$$

where $f_1(.) = \min(., 1)$ and $f_2(.) = \max(., 0)$ ensure that the query points don't leave the valid solution space $(x_l, x_{pv}) \in [0, 1]$. For notational simplicity, we drop the variable t. The reason behind creating a local linearization is simple; the control voltage of VReg 1 will escape the deadband if there is a significant change in x^*. As a result, the regulator tap position would change and new plane coefficients would be required. Hence, we are only truly interested in accurately estimating the control voltages around the operating point, instead of the complete solution space of x_l and x_{pv}. Figure 4.1a shows the estimated and the actual control voltage seen by VReg 1 for every possible combination of input profiles. The estimated control voltages are obtained by creating a local linearization around $x^* = (0.65, 0.65)$ with a $\delta = 0.05$. Figure 4.1b shows a heat map of the corresponding residual error (absolute values) due to the local linearization approach. The lines in red denote the upper and lower boundaries of the regulator deadband. The region enclosed within these boundaries represents the values of load and PV power injections that will not trigger any tap action. We refer to this region as the *feasible* solution space. The maximum residual error within the feasible solution space is 0.06 V, which is 4% of the deadband (1.5 V). The residual error increases as we move away from x^* due to the nonlinear nature of the voltage-power manifold. However, outside the feasible solution space, the regulator tap

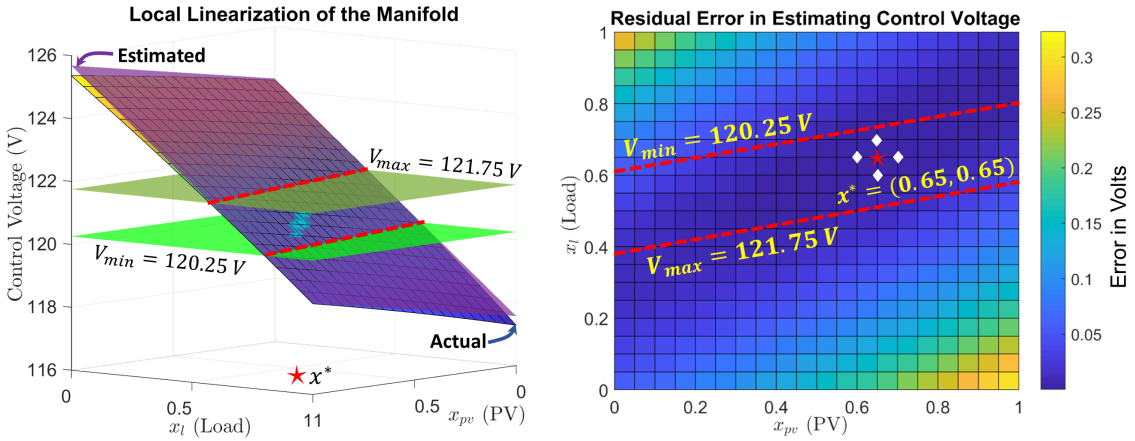


Figure 4.1: Residual error (absolute) in estimating the control voltage of VReg 1 using local linearization. The regulator set point is 121 V with a deadband of 1.5 V. The white diamonds represent the query points, whereas the operating point is depicted by a red star.

action would occur causing s_t to change, and therefore resulting in re-linearization of the manifold around the new x^*.

Although extremely accurate, there are two limitations of this method. First, for controllers that have a larger deadband (usually capacitor banks), the residual error can be significant within the feasible solution space. This can cause error in estimating the control voltages, especially near the boundaries of the deadband, resulting in false controller actions. This is because δ does not take into account the impact each profile has on the control voltages. Second, if the operating point is at the boundary of the valid solution space (e.g. $x^* = (0.65, 1)$), the number of independent rows in $\boldsymbol{X}$ decreases by 1. In case of PV profiles, it is fairly common to observed a value of 1 during the day time. As a result, the number of observations in the response vector decreases and hence, the residual error further increases within the feasible solution space.

4.1.2 Sensitivity-based Midpoint Linearization (SbML)

This method aims at minimizing the error near the boundary of the feasible solution space by perturbing x^* based on sensitivity analysis. Sensitivity analysis provides a good estimate

of the expected change in control voltage for a given change in power injections. Because of the circuit topology and the location of loads and PV systems, each profile has a different impact on each controller. Therefore, we separately define δ_l and δ_{pv}, which represent the variation in x_l and x_{pv}, respectively. Furthermore, to overcome the limitation of local linearization, we propose $\boldsymbol{X}$ with the following structure,

$$\boldsymbol{X} = \begin{bmatrix} 1 & x_l & x_{pv} \\ 1 & f_1(x_l + \delta_l) & x_{pv} \\ 1 & f_2(x_l - \delta_l) & x_{pv} \\ 1 & x_l & g(x_{pv} + 0.5\gamma) \\ 1 & x_l & g(x_{pv} + \gamma) \end{bmatrix} \tag{4.2}$$

where,

$$\gamma = \begin{cases} +\delta_{pv}, & 0 \leq x_{pv} < 0.5 \\ -\delta_{pv}, & 0.5 \leq x_{pv} \leq 1 \end{cases}, \quad g(.) = \begin{cases} f_1(.), & 0 \leq x_{pv} < 0.5 \\ f_2(.), & 0.5 \leq x_{pv} \leq 1 \end{cases}$$

and $f_1(.), f_2(.)$ are the same as before. The load profile is perturbed in the δ_l-neighborhood of x_l. In case of PV profile, the variation is *directional* and is based on the present value of x_{pv}. This is because fluctuations in solar irradiance are dependent upon the motion of clouds. If there is no cloud cover, the PV output remains close to 1 and hence, $\gamma = -\delta_{pv}$. The negative sign ensures that the query points are always lower than the present value of x_{pv}. This causes a bias in the resulting residual error, which is much lower in one direction as compared to the other. As the cloud cover comes in, x_{pv} decreases, thereby improving the estimation quality. Similarly, at night time x_{pv} is 0, which causes γ to take up the value of $+\delta_{pv}$. In this case, estimation error further decreases as the value of x_{pv} starts to increase (such as during sunrise). Moreover, the function $g(.)$ ensures that the query points don't leave the valid solution space.

The value of δ_l and δ_{pv} can be calculated using the following steps:

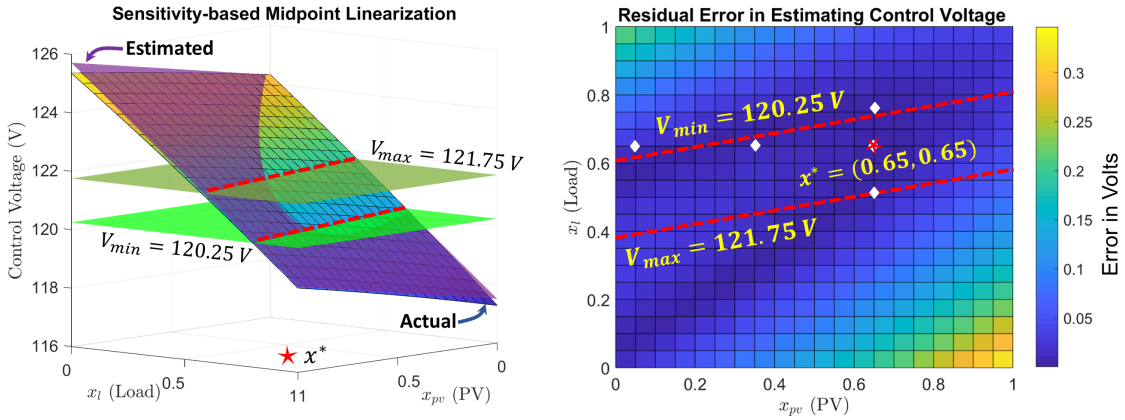
1. Obtain the mean values of the load and PV profiles ($\bar{x}_{pv}, \bar{x}_l$). Solve a static power flow corresponding to these mean values, with all the controllable elements enabled. This will ensure that the control voltages of the regulators and capacitor banks are within their respective deadbands.

2. Formulate the design matrix $\boldsymbol{X}$ as shown in equation (4.1), with a $\delta \leq 0.05$. Disable all the controllers in the circuit and solve the power flow problem to obtain $\boldsymbol{Y}^{(j)}, \forall j \in \mathcal{C}$. Using the OLS estimator (equation (3.17)), obtain the values of the plane coefficients for each controller. The β_i within the plane coefficients measures the impact of profile i on the controller voltage. In other words, β_i represents the change in control voltage caused by a 0 to 1 p.u. change in the profile i. Furthermore, β_i remains nearly constant, regardless of the the state of voltage regulator or capacitor bank [84].

3. Normalize the voltage sensitivity coefficients with respect to the size of the controller deadband. This is because voltage regulators and capacitor banks can have different sized deadbands. The normalized sensitivity coefficients incorporate these variations, thereby providing a uniform measure to establish a comparison. For each profile, compare the normalized coefficients of all the controllers and select the one with the largest absolute value. Let $\hat{\beta}_l, \hat{\beta}_{pv}$ denote this value for the load and the PV profile, respectively.

4. Set $\delta_l = 0.5/\hat{\beta}_l$ and $\delta_{pv} = 0.5/\hat{\beta}_{pv}$. In other words, δ_l, δ_{pv} will perturb the system in a way that would cause the control voltage of the most sensitive controller to observe a change of 50% (of the deadband).

For the 13-bus test circuit, the normalized sensitivity coefficients for VReg 1 are 0.837 (PV) and 4.433 (load). The control voltage of VReg 1 is more sensitive to the variation in load profile as compared to the PV profile. This is because the PV penetration is at 40% of the peak load. Therefore, if the PV output were to change from 0 to 100% of its rated



(a) (b)

Figure 4.2: Residual error (absolute) in estimating the control voltage of VReg 1 using sensitivity-based linearization. The query points are well spread out and lie close to the boundary of the feasible solution space.

value, the control voltage of VReg 1 would shift by 83.7% (of the deadband) or 1.25 V (0.837 $\times$ 1.5 V). To limit this shift to 50% of the deadband, the corresponding change in PV profile would be 0.597 p.u. Therefore, $\delta_{pv} = 0.597$ and similarly, $\delta_l = 0.112$. Figure 4.2 shows the residual error in estimating the control voltage of VReg 1 using the proposed sensitivity-based method. The query points lie very close to the edge of the feasible solution space, resulting in lower residual error at the boundary. The upper bound on the absolute error within the feasible solution space is 0.05 V, which is close to the local linearization approach (0.06 V). Therefore, the proposed method shows a similar error performance while overcoming the limitations of local linearization. In case of multiple power injection profiles, the design matrix in equation (4.2) will have an additional column for each profile. However, the number of query points will always increase linearly with the number of input profiles, thereby ensuring scalability of the method.

4.1.3 Performance of Fast QSTS Algorithm with SbML

To test the accuracy of the proposed SbML method, we run the yearlong 1-second resolution QSTS on the IEEE 13-bus test circuit, discussed in section 3.7. Table 4.1 shows

Table 4.1: Fast QSTS with SbML (IEEE 13-bus)

QSTS Metric	**Brute-force**	**Fast QSTS (Error)**	
		Old Method	SbML
Regulator tap actions:			
VReg 1 (A-ϕ)	7056	+4.32%	-0.42%
VReg 2 (B-ϕ)	7233	+4.78%	-0.15%
VReg 3 (C-ϕ)	8460	+1.63%	-0.52%
Capacitor switches:			
Cap 1 (3-ϕ)	2506	+3.83	-1.03%
Total time taken	14.25 mins	13.2 secs	13.3 secs
Power flow solutions	31.5 million	820	1015

a comparison of the error in estimating the states of regulators and capacitor banks with respect to the 1-second, yearlong brute-force QSTS. The proposed SbML is very accurate, and produces an estimation error with RMS value of 0.53%. The *old method* here refers to the linearization of voltage-power manifold using the design matrix $\boldsymbol{X}$ proposed in equation (3.18). The total number of power flow solutions required by SbML is slightly higher. This is because the number of rows in $\boldsymbol{X}$ for SbML is $2(n+k)+1$, as opposed to $n+2k+1$ (for the old method), where n, k is the total number of PV and load profiles, respectively. In other words, fast QSTS algorithm with SbML has to solve n more power flows for each new unique system controller state, when compared to the old method. This however, has a negligible impact on the total time taken, as shown in Table 4.1.

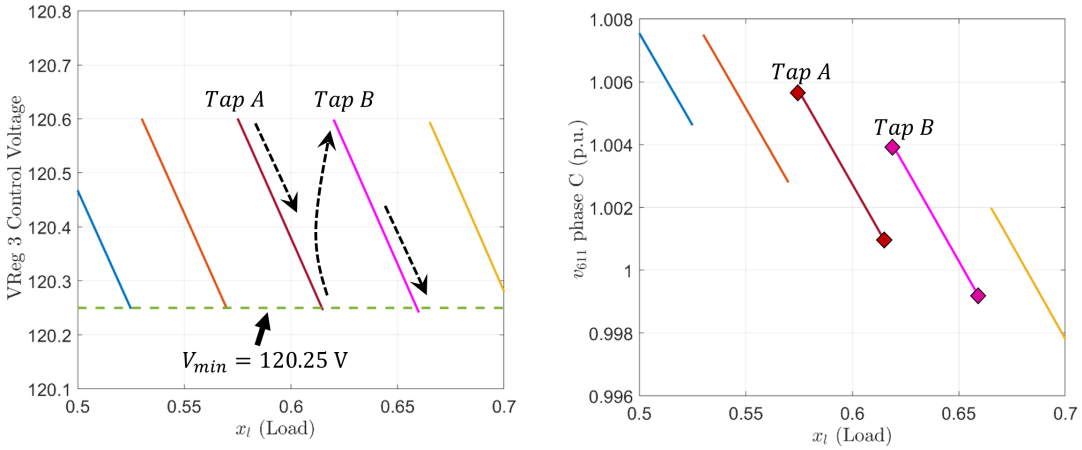
4.2 Nonuniform Voltage Reconstruction

Another important aspect of running a QSTS analysis is to accurately predict the voltage extremities that might occur due to high PV penetrations. To estimate the maximum and minimum voltage at each node, a time series voltage profile is required. The proposed fast QSTS algorithm estimates these voltage profiles using a uniform time-step voltage reconstruction method. The flow chart for this method is shown in Figure 3.10. The reconstruction time-step, dt, directly impacts the accuracy of the results, as shown in Figure 3.14b. For the IEEE-13 bus test case, a time-step of 60 seconds yields fairly accurate re-

sults. However, the proposed method of reconstruction using uniform time-step suffers from scalability issues. This is because the total time required for voltage reconstruction, T_r, is a function of dt as well as the number of buses and input profiles. Typical utility feeders have thousands of buses, which makes the resulting matrix multiplication operation computationally time intensive. A smaller value of dt corresponds to more frequent evaluation of equation (3.17), resulting in a proportional increase in T_r. On the other hand, a larger value of dt (such as 10 minutes) requires a small T_r, however, produces significant errors in estimating voltage extremities. In this section, a novel nonuniform voltage reconstruction method is proposed which overcomes the aforementioned limitations.

The magnitude of maximum and minimum voltage at any node during a QSTS simulation is dependent upon two things. First, it is a function of the present value of input power injection profiles. Figure 3.2 shows the voltage-power manifold for bus 611 (phase C) of the IEEE 13-bus test circuit with all the controllable elements disabled. The minimum and maximum voltages occur at $(x_l, x_{pv}) = (1, 0)$ and $(x_l, x_{pv}) = (0, 1)$, respectively. Second, it is dictated by the states of voltage regulators and capacitor banks. Figure 4.3 shows the impact of changing VReg 3 tap position on the voltage-power manifold at bus 611, phase C. For ease of visualization, x_{pv} is fixed at 0.5, which yields a 2-D plot of the manifold. Increasing the value of x_l causes the regulator control voltage to drop, which triggers a tap action, as shown in Figure 4.3a. For a given regulator tap position, the maximum and minimum voltages occur right before a new tap action is triggered, as shown in Figure 4.3b. Similarly, in a circuit with multiple controllable elements, extreme voltages occur right before the state of system controllers change. We refer to the time instant immediately preceding a controller action as a *critical event*.

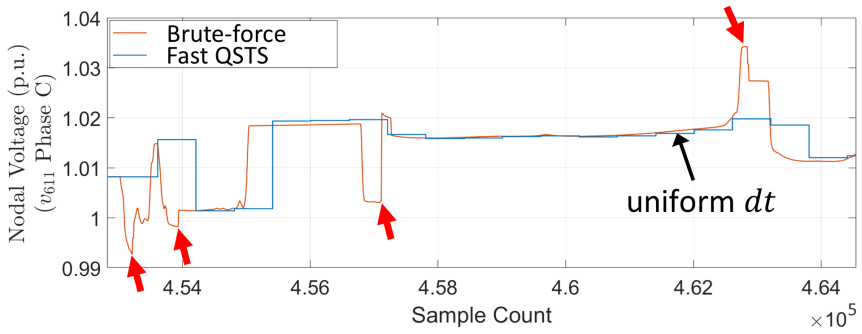
As mentioned earlier in Section 3.6.1, the proposed fast QSTS algorithm decouples the estimation of system controller states and voltage reconstruction. The estimation of system controller states is performed first, at the smallest possible time-step, which is then followed by voltage reconstruction. Therefore, during the reconstruction process, the critical events



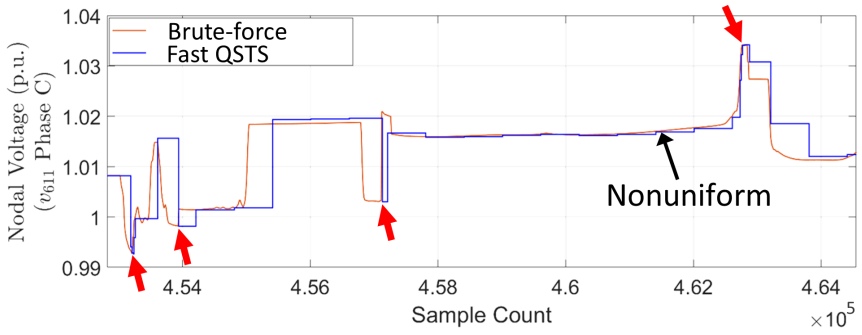
(a) Control Voltage of VReg 3 ($120V_{base}$)

(b) Voltage magnitude at bus 611

Figure 4.3: Impact of regulator tap action on the voltage-power manifold. The voltage magnitude corresponding to each tap position is represented by a different color. The diamonds represent the maximum and minimum voltages for a given tap position.



(a) Uniform reconstruction with dt = 10 mins



(b) Nonuniform reconstruction with the same dt

Figure 4.4: Accuracy comparison of the fast QSTS algorithm using uniform and nonuniform voltage reconstruction. The x-axis represents the sample count or time in seconds. The brute-force results are obtained by running a 1-second resolution QSTS on the IEEE 13-bus test circuit discussed in Section 3.7.

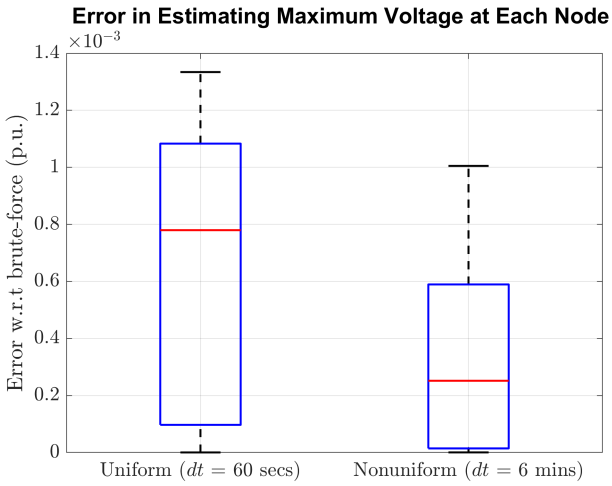


Figure 4.5: Box plot of maximum nodal voltage error for the uniform and nonuniform reconstruction methods. The bottom and top edges of the box indicate the 25th and 75th percentiles, respectively, and the red line inside the box represents the median error values. The black horizontal lines indicate the maximum and minimum error values observed amongst all the nodes.

are a known *priori*. Hence, equation (3.17) needs to be evaluated only at the critical events to estimate voltage extremities. We propose a nonuniform reconstruction method in which equation (3.17) is evaluated at both uniform time-steps and critical events. Consequently, a larger value of dt can be selected without causing any significant estimation errors.

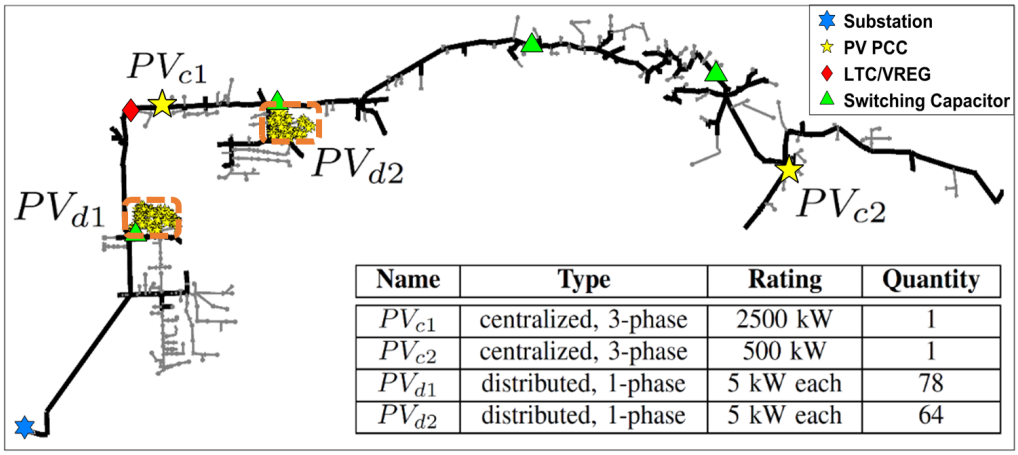
Figure 4.4 shows a comparison of the voltage profiles obtained from uniform and nonuniform reconstruction methods. The baseline profile is the voltage at bus 611, phase C obtained by running a 1-second resolution brute-force QSTS on the IEEE 13-bus circuit. The location of critical events is denoted by red arrows, which is detected using the proposed fast QSTS algorithm. The uniform reconstruction method is unable estimate the voltage magnitude at these instances because of the large value of dt, as shown in Figure 4.4a. However, by using nonuniform reconstruction with the same dt, the magnitude of local voltage extremities can be easily calculated, as shown in Figure 4.4b. A zero-order hold filter is used to estimate the value of voltage magnitude in between the reconstruction time-steps. Figure 4.5 shows a comparison of the error performance in estimating maximum voltage at each node of the IEEE 13-bus test circuit for the two methods. For a

fair comparison, the uniform voltage reconstruction is performed at a 60 second time-step, which takes around 2.8 seconds. It produces a mean error of 0.0006 p.u. when compared to the 1-second resolution, yearlong brute-force QSTS results. In contrast, the nonuniform method with a time-step of 6 minutes produces half the error (mean value of 0.0003 p.u.), while being 3.5 times faster (0.8 seconds). In the following sections, we evaluate the scalability and robustness of the modified fast QSTS algorithm[1] by testing it on two utility-scale feeders.

4.3 Simulation Case Study: Utility Feeder CO1

CO1 is an actual distribution feeder [85], with 2969 buses and 5469 nodes. A single line diagram of the feeder is shown in Figure 4.6, with black and grey lines representing the feeder backbone and laterals, respectively. The length of the feeder is 21.37 km, and has a total of 9 controllable elements: a single three-phase substation LTC transformer (33 taps), 3 single-phase LVRs (33 taps), 3 three-phase and 2 single-phase switching capacitor banks. There are 1,111 single-phase customers and 317 three-phase customers on the feeder, each modeled individually, connected on the low-voltage secondary networks. The feeder includes detailed models of the service transformers for the secondary system, including both wye and delta connected. All three-phase loads are designated as commercial while single-phase loads are assumed to be residential, accounting for 1.69 MW and 4.25 MW of the peak load respectively. Other feeders connected to the substation transformer are modeled as aggregate lumped loads with 12 MW of peak power. The mean phase-to-ground voltage imbalance in the feeder at rated load is 2.71%. Both load types are assigned a unique 1-second power injection profile generated from SCADA measurements of the feeder under consideration. Figure 4.7 shows a boxplot for the yearlong residential and commercial load profiles grouped by the hour.

[1]The modified fast QSTS algorithm incorporates both SbML and nonuniform voltage reconstruction. All the simulations following this section were performed using the modified algorithm with a reconstruction time-step of 1000 seconds.



Name	Type	Rating	Quantity
PV_{c1}	centralized, 3-phase	2500 kW	1
PV_{c2}	centralized, 3-phase	500 kW	1
PV_{d1}	distributed, 1-phase	5 kW each	78
PV_{d2}	distributed, 1-phase	5 kW each	64

Figure 4.6: Circuit diagram of the distribution feeder with various types of PV installations.

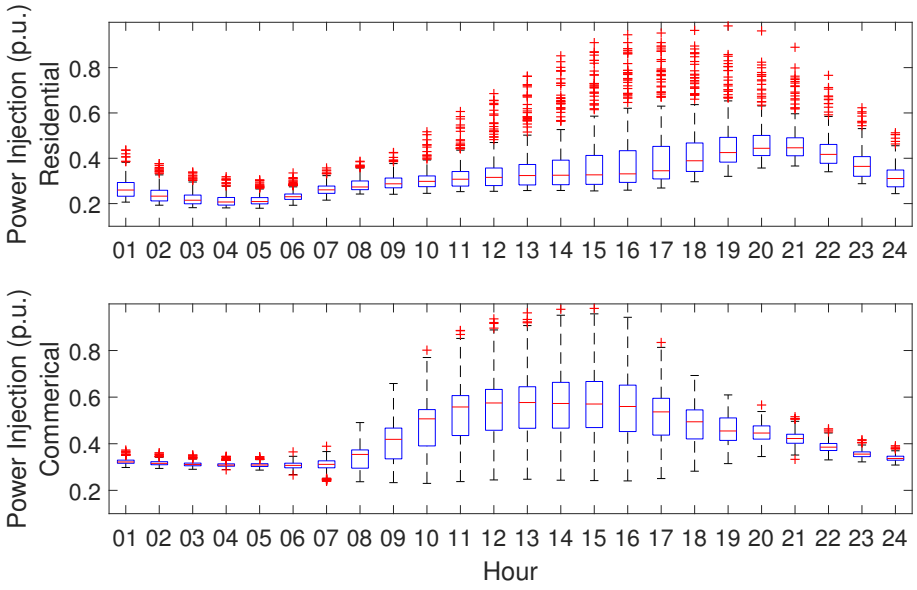


Figure 4.7: Boxplot for the two load profiles. The residential profile peaks during the evening hours, whereas the commercial profile reaches peak values during the day time.

A total of 144 PV systems are installed on the feeder, which are grouped into four categories based on their geographical locations, as shown in Figure 4.6. Distributed PV systems are residential rooftop installations modeled on the low-voltage networks adjacent to the loads. The centralized PV systems are 3-phase utility-scale installations with their own interconnection transformer. Each category of PV system is also assigned a unique 1-second power injection profile based on solar irradiance data. The raw irradiance measurements were obtained from DEMROES network at UC San Diego, which were then converted to yearlong synthetic PV profiles[2] using wavelet-based variability model (WVM) [19]. In addition, all PV systems are configured to operate at unity power factor. We simulate two different scenarios to test the efficacy of the proposed algorithm.

4.3.1 Case A : Two Load Profiles with no PV system

In the first simulation case, the feeder has no PV installations. Moreover, since the total number of profiles in this case is only two, the behavior of bus voltages in a three dimensional space can be easily visualized. The baseline simulation results are obtained by running a 1-second resolution, yearlong brute-force QSTS simulation with a residential and a commercial load profile. Figure 4.8 shows the control voltages seen by the substation LTC as a function of the two load profiles. Each dot represents a power flow solution at a particular time instant in the time series simulation. The substation LTC is configured to regulate the control voltage to 124 V (120 V_{base}) with a deadband of 2 V. The various colors represent power flow solutions corresponding to different tap positions. It is evident from the figure that the control voltages are confined to planes whose coefficients are dependent on the particular state of the controllable elements. These observations are coherent with our proposed linear sensitivity model. Since the substation LTC has a delay timer in the controller logic, a few power flow solutions are out of the deadband.

Table 4.2 shows the error in estimating the states of voltage regulators and capacitor

[2]Refer to Appendix B for box plots of all the profiles.

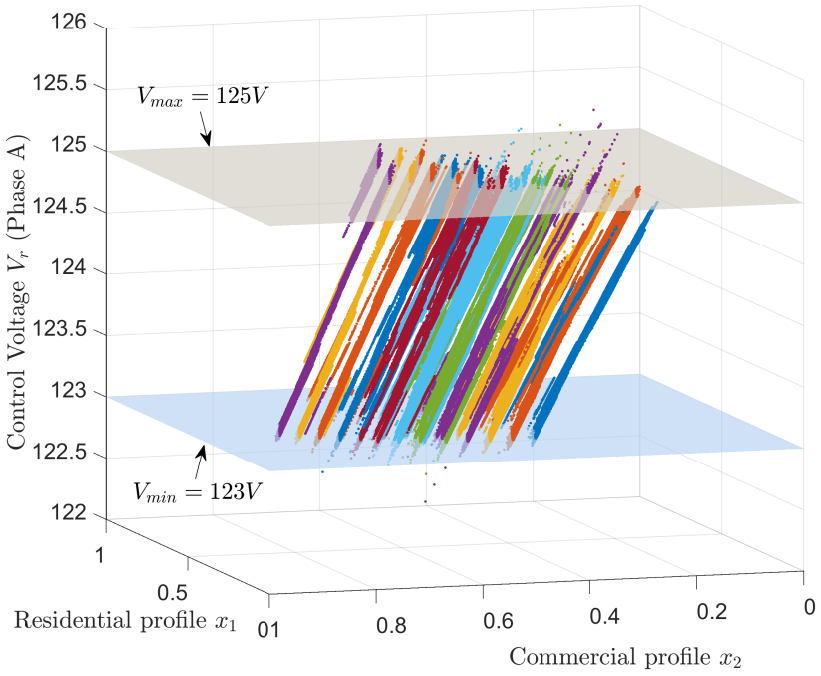
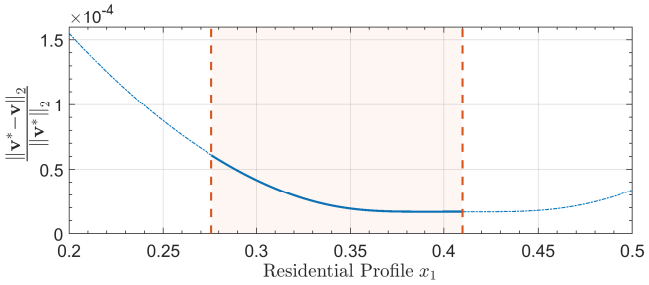


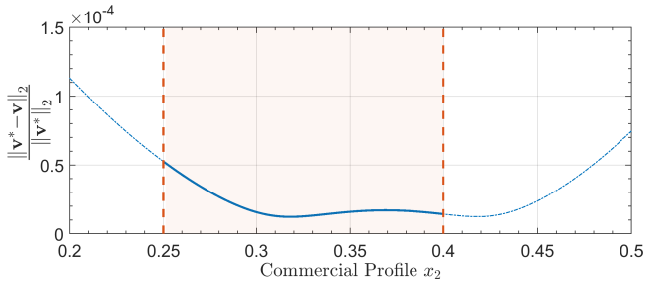
Figure 4.8: Control voltages seen by the substation LTC in a 1-second yearlong brute-force QSTS simulation (31.5 million points), with a different color for each tap position.

Table 4.2: Accuracy and timing comparison (CO1: Case A)

QSTS Metric	**Brute-force**	**Fast QSTS (error)**
Regulator tap actions:		
Sub LTC (3-ϕ)	2742	-0.18%
VReg 1 (A-ϕ)	3125	+0.03%
VReg 2 (B-ϕ)	4177	+0.07%
VReg 3 (C-ϕ)	3872	-0.10%
Capacitor switches:		
Cap 1 (3-ϕ)	628	0%
Cap 2 (3-ϕ)	0	0
Cap 3 (3-ϕ)	44	0%
Cap 4 (A-ϕ)	464	0%
Cap 5 (B-ϕ)	722	0%
Total time taken	29 hours	2 minutes



(a) Relative error for variation in residential profile



(b) Relative error for variation in commercial profile

Figure 4.9: Error introduced due to the linear sensitivity model for a given system controller state. For (a), x_2 is fixed at 0.3676, while for (b) x_1 is fixed at 0.4056.

banks using the proposed fast QSTS algorithm. Since the voltage-power manifold is not exactly linear, the proposed algorithm produces a small estimation error. Let $\mathbf{v}^*$ denote the voltage vector obtained by solving the actual nonlinear power flow equations. A plot of the relative error introduced due to the linear sensitivity model is shown in Figure 4.9. In order to obtain the plane coefficients, the linearization of voltage-power manifold is done around the operating point $(x_1, x_2) = (0.4056, 0.3676)$, which is essentially the value of power injection profiles at $t = 1$. The shaded region represents the permissible values of power injections for which the control voltages of all the controllable elements remain within their respective deadbands before changing states. As shown, the error is well behaved within this feasible solution space with a value of less than 0.0075%. Once the value of power injection profiles leave this region, a new set of plane coefficients are computed, as discussed earlier.

The proposed fast QSTS algorithm computes all voltage-related impact metrics in 2 minutes as compared to the brute-force approach, which takes almost 29 hours to complete.

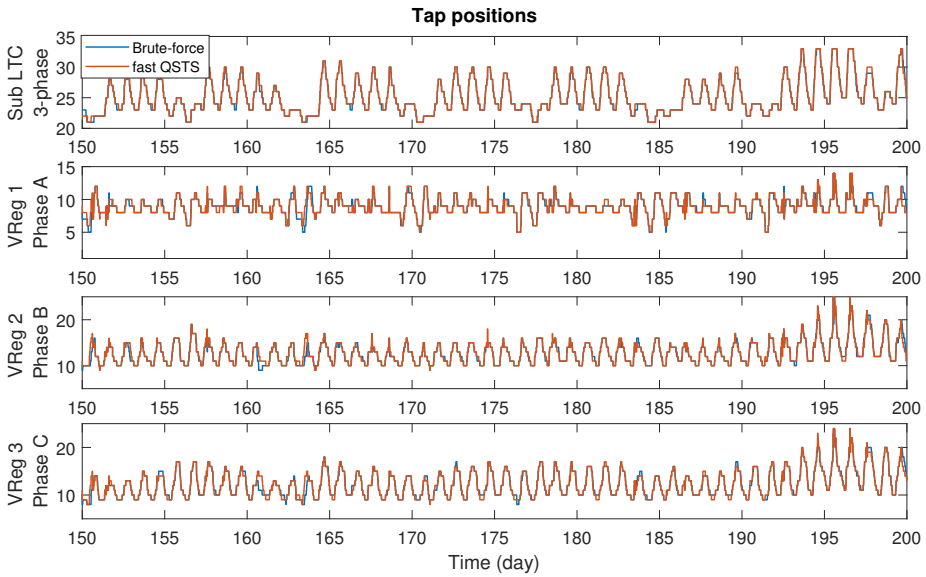


Figure 4.10: Comparison of voltage regulator states through time. All regulators have a total of 33 tap positions.

The 99.89% reduction in computation time is primarily due to the fact that the proposed algorithm only solved 9,490 power flows to estimate the linear sensitivity model for all the nodes in the circuit.

4.3.2 Case B : Two Load Profiles with significant PV

In this case, we run the QSTS simulation with all four categories of PV systems connected to the feeder, each following its own unique power injection profile. Thus, a total of six 1-second resolution, yearlong profiles are used as inputs to the QSTS simulation. The PV penetration is at 62% of the peak load. Figure 4.10 shows a comparison of the states of voltage regulators through time. The plot in blue corresponds to the actual controller states obtained through the brute-force solution whereas, the overlaid red plot shows the estimated states obtained by running the proposed fast QSTS algorithm. It can be seen that the fast QSTS algorithm is extremely accurate at predicting the actual states of the controllers through time.

Table 4.3: Accuracy comparison of the fast QSTS algorithm (CO1: Case B)

QSTS Metric	**Brute-force**	**Fast QSTS (error)**
Regulator tap actions:		
Sub LTC (3-ϕ)	2737	+0.21%
VReg 1 (A-ϕ)	5538	+1.51%
VReg 2 (B-ϕ)	5288	+0.22%
VReg 3 (C-ϕ)	5166	+0.92%
Capacitor switches:		
Cap 1 (3-ϕ)	376	-1.06%
Cap 2 (3-ϕ)	52	-3.84%
Cap 3 (3-ϕ)	30	0%
Cap 4 (A-ϕ)	534	+0.74%
Cap 5 (B-ϕ)	758	-0.79%
Feeder phase voltage:		
Highest	1.0631 p.u.	+0.0005 p.u.
Lowest	0.9019 p.u.	+0.0002 p.u.
Duration of ANSI violations:		
Over voltage	222.97 Hrs	+22 Hrs
Under voltage	125.37 Hrs	+0.17 Hrs
Per phase voltage (each bus):	total of 5469 nodes	
Highest	0.0003 p.u. (mean error)	
Lowest	0.0004 p.u. (mean error)	

Table 4.4: Timing comparison of the fast QSTS algorithm (CO1: Case B)

	Brute-force	**Fast QSTS**	**% Reduction**
Total time taken	29 hours	7.39 minutes	99.58%
Power flow solutions	31.5 million	48,282	99.85%

A comparison of the accuracy for various QSTS metrics is presented in Table 4.3. It can be seen that installing PV in the feeder causes a significant increase in the number of controller actions. This is due to the highly variable PV power output. The fast QSTS algorithm produces an average error of 0.71% and 1.28% in estimating the states of voltage regulators and capacitor banks, respectively. In addition, the proposed algorithm is able to predict the duration of ANSI voltage limit violations (Range A, 126/114 V on a 120 V_{base}) as well as extreme voltages within the specified error thresholds. The voltage profile is estimated using nonuniform reconstruction with a time-step of 1000 seconds. The error

in estimating the over voltage duration decreases with a smaller value of dt (e.g. +13 hours for dt = 600 seconds). Table 4.4 shows that the fast QSTS algorithm takes less than 8 minutes to compute all the voltage-related PV impact metrics which corresponds to a speed increase of more than 230 times. Because of the additional profiles and more unique system controller states, the total number of power flows solved in this simulation case is greater than in case A, but it is still 1000 times less than solving a power flow for every second for a yearlong QSTS simulation.

4.4 Simulation Case Study: Utility Feeder J1

Feeder J1 is a 12 kV distribution feeder, located in the northeastern US [86]. It has a length of 18.1 km with a total of 3433 buses and 4242 nodes. The single line diagram of the feeder is shown in Figure 4.11. There are a total of 1300 commercial, residential and light industrial customers connected to this feeder, which serves a peak load of 6.3 MW. While not a heavily loaded feeder, it does require the use of an LTC as well as multiple LVRs and switching capacitor banks to provide voltage regulation. It has a total of 12 controllable elements: a single three-phase substation LTC transformer (17 taps), 8 single-phase LVRs (33 taps) and 3 three-phase switching capacitor banks. The feeder model includes detailed low-voltage secondary networks, with both wye and delta connected service transformers. Other feeders connected to the substation are modeled as aggregate lumped loads, with a peak rating of 10 MVA. Each load type is assigned a unique 1-second power injection profile. The residential and commercial load profiles are similar to the ones used for feeder CO1, however aggregate lumped loads are assigned their own unique power profile, obtained from the J1 SCADA data [86].

The default J1 feeder has only two PV installations, PV_{c1} and PV_{c2} (both three-phase), shown in the Figure 4.11. To increase the overall PV penetration, five additional single-phase PV systems are installed at various locations in the feeder. Each PV system is assigned a unique 1-second power injection profile, synthesized from high resolution irra-

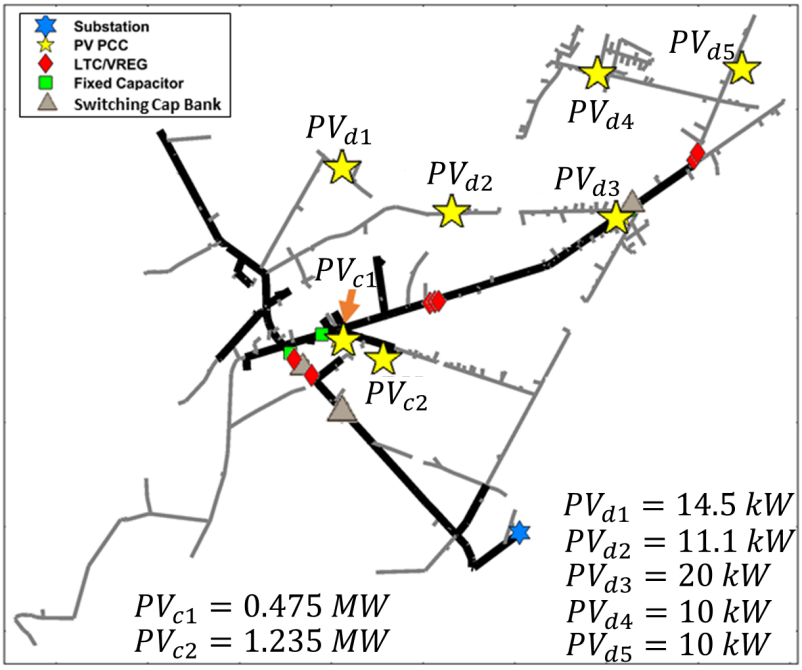


Figure 4.11: Circuit diagram of the distribution feeder with various PV installations.

diance measurements (NREL Oahu site [82]) using WVM [19]. In addition, all the PV systems are configured to operate at unity power factor.

The J1 feeder is a particularly challenging test case because of two reasons. First, the total number of controllable elements in the circuit are 12. Multiple LVRs are in series, which means that the operation of an upstream device directly impacts the downstream devices. Consequently, the circuit experiences significant controller interactions, which makes the task of estimating controller states all the more challenging. In addition, the switching capacitor bank located towards the end of the feeder can change the local bus voltage by almost 7 V (120 V_{base}). Therefore, whenever it changes its state, the LVRs have to update their tap positions as well to ensure that the feeder voltage remains within the ANSI limits. Hence, the duration of ANSI limit violations is closely coupled with the controller states. Second, a total of ten unique 1-second resolution, yearlong power injection profiles are used as inputs to the simulation. Each individual PV system has its own unique profile based on its size and location. Therefore, the J1 feeder provides a unique opportunity to test the robustness, scalability and accuracy of the proposed fast

QSTS algorithm.

4.4.1 Simulation Results

Table 4.5 shows a comparison of the QSTS simulation results obtained by using brute-force method and the proposed fast QSTS algorithm. The estimation error is calculated by comparing the results of the proposed algorithm with the baseline 1-second resolution, yearlong brute-force QSTS. The proposed algorithm is extremely accurate in estimating the states of voltage regulators (0.36% RMS error) and capacitor banks (1.11% RMS error). In addition, the errors in estimating the voltage extremities as well as duration of ANSI limit violations (Range A, 126/114 V on a 120 V_{base}) are well under the specified thresholds. Similar to the previous test case, the nodal voltage profiles are estimated using the nonuniform reconstruction method with a time-step of 1000 seconds.

A timing comparison of the proposed algorithm with the brute-force QSTS is established in Table 4.6. The fast QSTS algorithm takes less than 15 minutes to compute all the voltage-related impact metrics, which corresponds to a computational time reduction of 98.98%. Due to significant controller interactions in J1 feeder, the number of unique system controller states are relatively high i.e. 7,492. In addition, estimating plane coefficients for each state requires 21 power flow solutions ($2(n + k) + 1$). Consequently, a total of 157,332 nonlinear AC power flows are solved for the yearlong time series simulation. The error performance of the fast QSTS algorithm on this test circuit is extremely impressive and speaks for the robustness and accuracy of the method. On the other hand, the significant computational time reduction demonstrates the scalability and applicability of the proposed algorithm.

Table 4.5: Accuracy comparison of the fast QSTS algorithm (J1)

QSTS Metric	**Brute-force**	**Fast QSTS (error)**
Regulator tap actions:		
Sub LTC (3-ϕ)	433	-0.46%
VReg 1 (A-ϕ)	6194	+0.41%
VReg 2 (B-ϕ)	6851	0%
VReg 3 (C-ϕ)	6990	-0.31%
VReg 4 (A-ϕ)	3045	+0.39%
VReg 5 (B-ϕ)	3041	-0.65%
VReg 6 (C-ϕ)	2468	+0.97%
VReg 7 (A-ϕ)	4509	-0.08%
VReg 8 (B-ϕ)	3527	-0.05%
Capacitor switches:		
Cap 1 (3-ϕ)	60	+3.33%
Cap 2 (3-ϕ)	627	0%
Cap 3 (3-ϕ)	11	0%
Feeder phase voltage:		
Highest	1.0883 p.u.	$<$ 0.0001 p.u.
Lowest	0.9365 p.u.	+0.0004 p.u.
Duration of ANSI violations:		
Over voltage	151.34 Hrs	-0.50 Hrs
Under voltage	14.09 Hrs	+1.18 Hrs
Per phase voltage (each bus):	total of 4242 nodes	
Highest	$<$ 0.0001 p.u. (mean error)	
Lowest	0.0001 p.u. (mean error)	

Table 4.6: Timing comparison of the fast QSTS algorithm (J1)

	Brute-force	**Fast QSTS**	**% Reduction**
Total time taken	24.3 hours	14.8 minutes	98.98%
Power flow solutions	31.5 million	157,332	99.50%

CHAPTER 5
FAST QSTS ALGORITHM FOR PV SMART INVERTERS

5.1 Introduction

Decreasing costs, government incentives and global policies have caused a significant growth in the deployment of solar PV systems. However, temporal and spatial variability of the PV power output has introduced numerous technical challenges that directly impact the reliability of the distribution grid. The first version of the IEEE 1547 standard, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems, did not allow DER to actively regulate the voltage at the Point of Common Coupling (PCC) [87]. Consequently, problems arising due to high PV penetration including over/under voltage violations, excessive reverse power flow and thermal overloading created a need to incorporate voltage regulating capability in grid-tied PV inverters [8]. Many countries including Germany and the United States have now modified their grid integration requirements allowing PV systems to actively regulate voltage and frequency through the use of smart inverters [88, 89]. The California Public Utilities Commission recently amended its Rule 21 to mandate the use of inverters that can operate under a wide range of voltage and frequency levels and provide advance grid support functionality including voltage and frequency ride-through, soft-start reconnection, and dynamic power management [90]. In addition, the latest version of the IEEE 1547 standard mandates voltage regulation capabilities of the grid-tied inverters through the use of real and reactive power management functions including Fixed Power Factor (FPF), Volt-VAR (VV) and Volt-WATT (VW) [91]. PCC voltage in distribution systems with high penetration of legacy inverters is usually driven by feeder events. However, vast deployments of smart inverters can potentially introduce significant variations in the overall feeder voltage profile. Therefore, understanding the

impacts of various smart inverter control functions is extremely important.

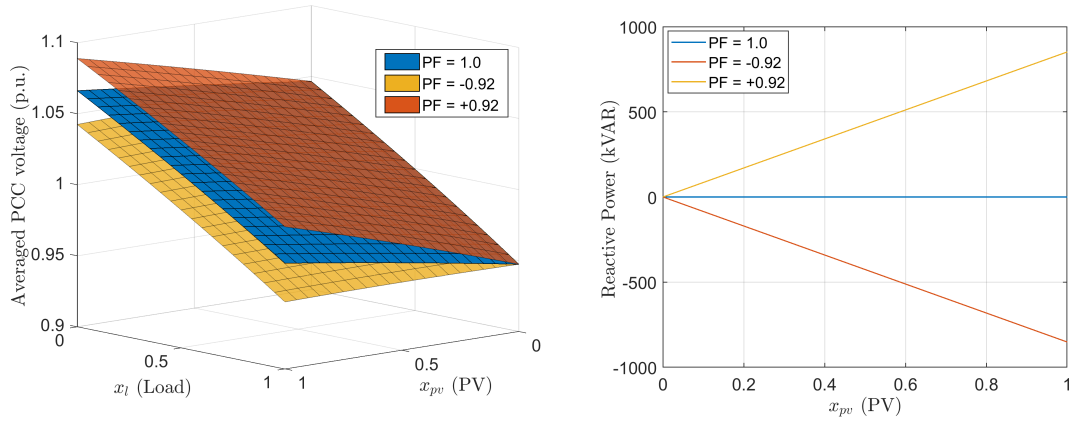
Evaluating the voltage regulation performance of smart inverters using QSTS analysis is an area of growing interest [22, 23, 44, 45, 92]. However, as mentioned in the introduction, these studies either run a very coarse resolution QSTS or reduce the simulation time horizon due to computational constraints. Hence, a fast and accurate QSTS algorithm, capable of analyzing the impacts of grid-tied PV inverters, is critical to maintaining distribution system reliability. In this chapter, we investigate the impact of three smart inverter control functions on the voltage-power manifold i.e. FPF, VV and VW. Furthermore, we create an abstract notion of a controllable element which allows the proposed fast QSTS algorithm to simulate these smart inverter control modes with a high degree of accuracy. Finally, to evaluate the efficacy of the algorithm, a variety of simulation case studies are presented towards the end of this chapter.

5.2 Smart Inverter Control Modes

5.2.1 Fixed Power Factor Mode

In this mode of operation, the inverter is configured to operate at a constant power factor. Hence, an increase in the real power output of the inverter causes a proportional increase in the reactive power as well. Most legacy inverters were designed to operate at unity power factor, meaning they could only supply real power output. However, smart inverters are capable of operating at both leading (+) and lagging (-) power factors. Typical values of power factor settings range from 0.90 lag to 0.95 lead [93]. To mitigate overvoltages caused by PV systems at PCC, the inverters are typically programmed to operate at lagging power factors. This allows them to proportionally absorb reactive power as the real power output increases, thereby reducing voltage variability. One major drawback of FPF mode is that reactive power feed-in is always present, even when the PCC voltage is fairly stable.

To demonstrate the impact of various smart inverter control modes on the voltage-power manifold, we utilize the IEEE 13-bus test circuit, discussed in section 3.7. The 2 MW cen-



(a) Voltage-power manifold.

(b) Reactive power output at various PFs.

Figure 5.1: Impact of changing the inverter power factor (PF) on the voltage-power manifold for the IEEE 13-bus test circuit. Each manifold is obtained by solving 441 discrete power flows in OpenDSS.

tralized PV system at bus 675 is now interfaced via a 2.2 MVA smart inverter. Overrating the inverter by 10% ensures that it is 1547 compliant, and is therefore able to provide reactive power support at peak power output without any curtailment [91]. Figure 5.1a shows the impact of changing the power factor setting on the voltage-power manifold, with all the controllable elements disabled. The z-axis represents the mean voltage magnitude of the phase A, B and C at bus 675 (PCC). Three different power factor (PF) settings are simulated. At unity PF, no reactive power is injected or absorbed by the PV system, and the resulting manifold is shown in blue. At leading PF, the reactive power produced (+ sign) by the PV system increases proportionally with respect to x_{pv}, as shown in Figure 5.1b. Consequently, the PCC voltage rises much more steeply at a leading PF, when compared to unity PF mode. On the other hand, a lagging PF causes the PV system to absorb reactive power (- sign), resulting in a lower PCC voltage. The important thing to note here is that even though the reactive power output is non-zero, the manifold still exhibits an almost linear behavior, similar to what was observed in section 3.3.1. Therefore, the proposed fast QSTS algorithm is easily able to estimate all the voltage related impact metrics, without any modifications. Furthermore, the reactive power output of the inverter is directly pro-

portional to x_{pv} in FPF mode. Hence, the total reactive power injected or absorbed during the time series simulation can be easily estimated using the linear sensitivity model.

5.2.2 Volt-VAR mode

VV mode allows a grid-tied inverter to vary the reactive power injection or absorption based on its PCC voltage. This type of reactive power control follows a utility-defined curve, such as the one shown in Figure 5.2. The underlying principle of VV control is to inject reactive power if the terminal voltage drops below a predefined value (P2), and to absorb reactive power if the voltage increases beyond the set limit (P3). A deadband is often added to the VV curve, which stops the reactive power feed-in as long as the terminal voltage remains inside the deadband. The VV curve has five regions; In R1 and R5, the reactive power feed-in is constant, and is usually based on the apparent power rating of the inverter, S_{rtg}. A commonly used value is 30% of S_{rtg} [94]. In R2 and R4, the reactive power feed-in follows the line formed by points (P1,P2) and (P3,P4), respectively and in R3 the reactive power output is zero. In contrast to FPF mode, VV control allows the inverter to perform voltage stabilizing measures only when the PCC voltage goes out of the deadband. By adjusting the reactive power output based on a feedback signal, the inverter acts as a shock absorber and thus, prevents the grid voltage from oscillating.

We now change the inverter mode in the IEEE 13-bus circuit to VV, and use the curve shown in Figure 5.2 as an input. For single phase PV systems, the terminal phase voltage is used as the reference PCC voltage. However, in case of three-phase systems, an average value of the terminal voltage (of all the phases) is used instead. Each region of the VV curve causes a discontinuity in the resulting voltage-power manifold, as shown in Figure 5.3a. When the PCC voltage lies within the region R3, the reactive power feed-in is zero, as shown in Figure 5.3b. The manifold within this region exhibits the same behavior as that of the FPF mode with unity power factor setting. As the feeder load drops (decrease in x_l), the PCC voltage starts to increase. Once it exceeds P3, the inverter starts operating

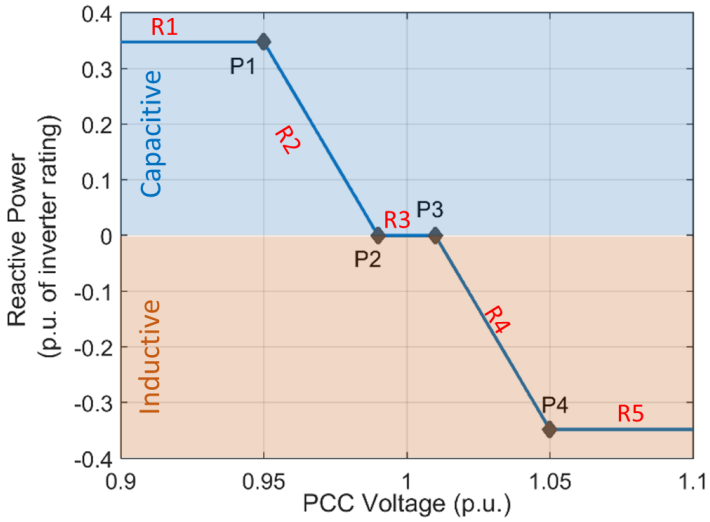
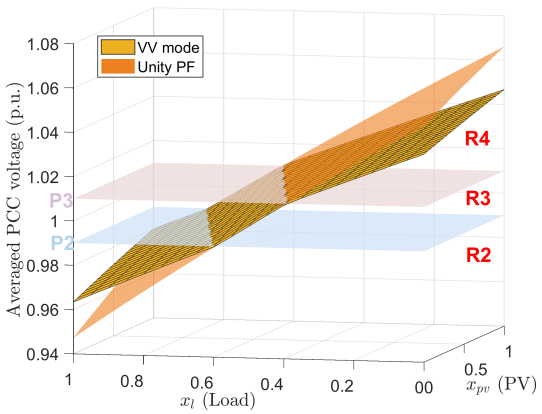
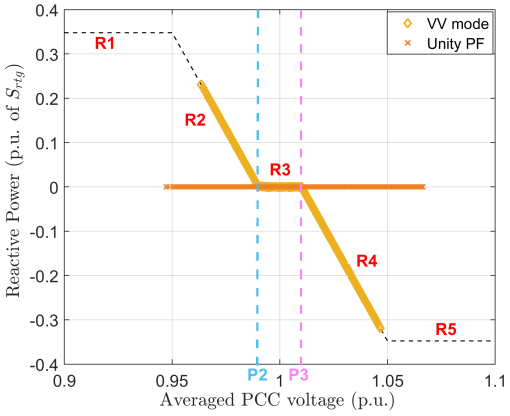


Figure 5.2: Example of an aggressive Volt-VAR curve with a deadband between 0.99 p.u. (P2) and 1.01 p.u. (P3).



(a) Voltage-power manifold.



(b) Reactive power output.

Figure 5.3: Impact of VV control on the bus voltage. The horizontal planes represent the boundaries of the deadband. The curve on the right shows the actual values of reactive power corresponding to the resulting PCC voltages, for both unity PF and VV mode. The dotted line shows the input VV curve.

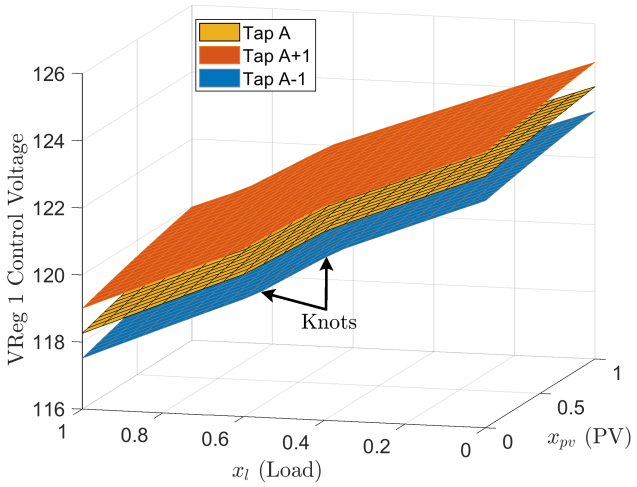


Figure 5.4: Impact of VV mode on VReg 1 control voltage. Each surface corresponds to a different tap position. The plot is obtained by disabling the regulator controller and manually changing the tap positions in OpenDSS.

at a lagging power factor. This causes the PCC voltage to increase at a much slower rate, as compared to unity power factor setting (see Figure 5.3a). Similarly, in region R2, the inverter operates at a leading power factor causing the PCC voltage to decrease at a much slower rate, due to the reactive power support. Furthermore, the reactive power absorbed or injected by the inverter in VV mode is confined to the input curve, as shown in Figure 5.3b.

We refer to the point of discontinuity in the voltage-power manifold as a *knot*[1]. In Figure 5.3b, the inverter never enters R1 or R5, therefore there are only two knots in the corresponding manifold. Furthermore, the VV control introduces knots in the voltage-power manifold of every bus in the circuit. This is because the reactive power injected or absorbed by the inverter changes the power flow across the entire circuit. The magnitude of impact on the voltage magnitude at each bus is dictated by the size of the inverter and the circuit topology. Figure 5.4 shows the impact of VV mode on the control voltage of VReg 1 in the IEEE 13-bus circuit. Changing the tap position causes discrete jumps in the manifold. In addition, for a given tap position and capacitor state, the location of the

[1]The nomenclature is inspired from piece-wise regression theory.

knots in the x-y axis remains constant across the entire circuit. Although the knots in the voltage-power manifold make it highly nonlinear, the behavior can still be approximated using the linear sensitivity model (discussed in section 5.3).

5.2.3 Volt-WATT mode

VW mode allows a grid-tied inverter to vary the PCC voltage by curtailing its real power output, instead of dispatching reactive power. An example of a reference curve for VW control is shown in Figure 5.5. The y-axis is in per unit of the rated real power output capability of the PV system, P_{rtg}. The shaded area in blue is the allowable region of operation in VW mode. The inverter starts to curtail its real power output, P_{out}, once the PCC voltage goes beyond a predefined value (P1). P1 can either be at the nominal voltage or up to +4% from it [23]. Total curtailment occurs if the PCC voltage exceeds the upper limit (P2). We define three operating regions of the VW curve as follows,

1. Region R1: No curtailment i.e. $P_{out} = x_{pv}$, where x_{pv} is the time series profile assigned to the PV system under consideration. In other words, P_{out} will be dictated by the solar irradiance at a particular location.

2. Region R2: Variable curtailment i.e.

$$P_{out} = mV_{pcc} + c \tag{5.1}$$

   where m and c is the slope and intercept of the line joining the points P1 and P2, respectively and V_{pcc} is the magnitude of the PCC voltage (terminal phase voltage in case of single-phase system and averaged phase voltage for three-phase system).

3. Region R3: Total curtailment i.e. $P_{out} = 0$. The inverter output remains zero as long as the PCC voltage exceeds P2.

Region R2 is particularly interesting since the power output of the inverter is confined to

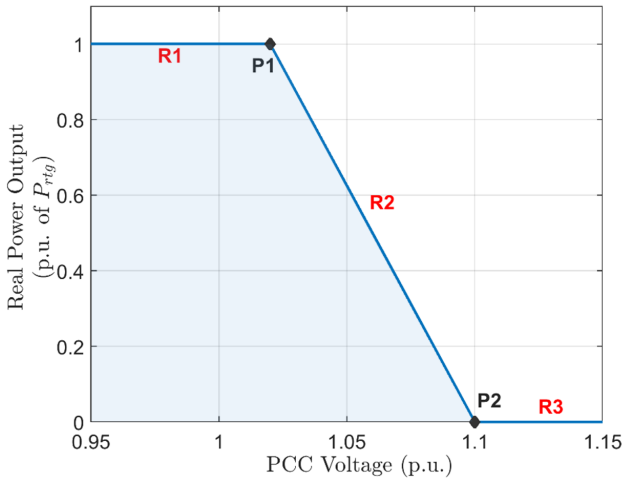
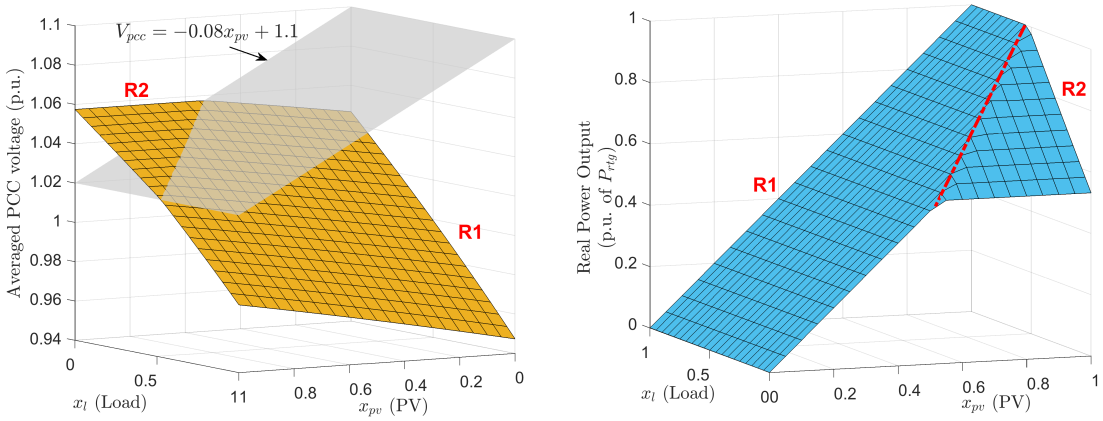


Figure 5.5: Example VW curve with a 2% deadband. The real power curtailment begins once the PCC voltage exceeds 1.02 p.u. (P1).

the line joining points P1 and P2. To understand the physical interpretation of R2, we consider the IEEE 13-bus test circuit with the inverter at bus 675 in VW mode (input curve shown in Figure 5.5). The impact of VW control on the voltage-power manifold is shown in Figure 5.6a. In region R1, P_{out} increases proportionally with respect to x_{pv}, and remains constant along the dimension of x_l, as shown in Figure 5.6b. The behavior of the manifold in R1 is similar to the one obtained in FPF mode with unity power factor setting. The grey plane represents the boundary of R1 and R2, which is obtained by replacing x_{pv} in equation (5.1). In R2, $V_{pcc} > -0.08x_{pv} + 1.1$ and P_{out} satisfies equation (5.1). Moreover, if the feeder loading does not change (x_l is fixed), P_{out} remains constant regardless of the value of x_{pv}. Therefore, due to equation (5.1), the PCC voltage remains constant as well. In R3, $V_{pcc} > 1.1$ and $P_{out} = 0$. In Figure 5.6, the inverter never enters R3 within the valid solution space $(x_l, x_{pv}) \in [0, 1]$, and therefore, P_{out} does not drop to zero. Similar to VV mode, the number and location of the knots in the voltage-power manifold is dictated by the input VW curve.



(a) Voltage-power manifold.

(b) Real power output P_{out}.

Figure 5.6: Impact of VW control on the bus voltage magnitude. The curve on the right shows the real power output of the inverter for all possible values of x_l and x_{pv}. The grey plane and the red dotted line represent the boundaries of the region R1 and R2.

5.3 Linear Sensitivity Model for Smart Inverters

The linear sensitivity model, proposed in section 3.4, relies on creating a linearization of the voltage-power manifold using multiple linear regression. The resulting sensitivity coefficients are used to estimate of the impact of load and PV power injections on the bus voltage magnitude. Controllable elements (such as LTCs, LVRs and capacitor banks) within the feeder try to maintain the voltage profile inside a specified range by changing their states. For a voltage regulator, a change in state corresponds to moving the tap position up or down whereas a capacitor switches on or off based on a control signal. If the state of these devices change, discrete jumps are introduced in the manifold. Consequently, the sensitivity coefficients are recalculated corresponding to the new system controller state, s_t. In general, the control logic for these controllable elements comprises of three key factors:

1. A control signal which is either the voltage across the secondary winding for voltage regulators or the terminal phase voltage for capacitor banks.

2. Unique and well defined states which are the tap positions of the regulators (usually 33 or 17 taps) and connected/disconnected state of the capacitor banks.

3. A predefined transition boundary for the control signal at which the state of the controllable element changes. These are usually defined by the regulator or the capacitor deadbands.

5.3.1 Smart Inverter Abstraction

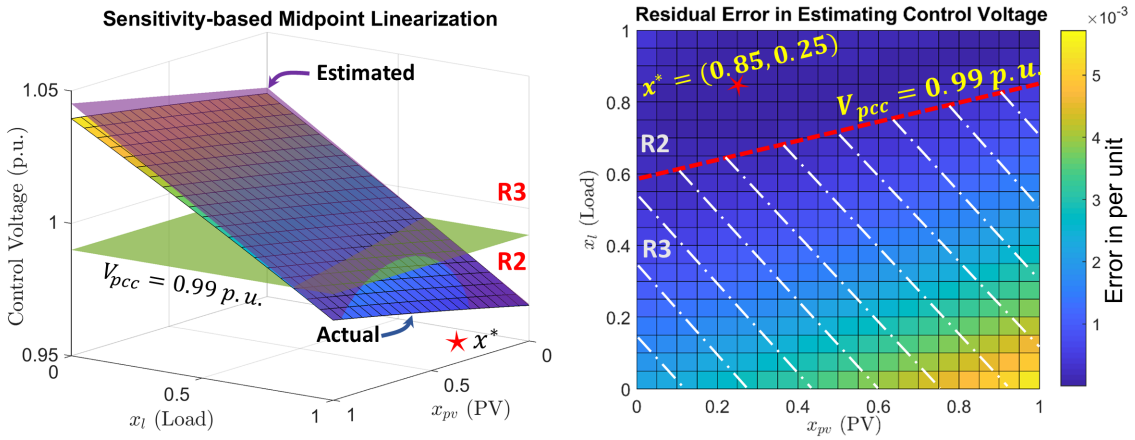
Although not obvious, the inverter control logic can be abstracted in a manner similar to a voltage regulator or a capacitor bank. The control signal for the inverter is the average PCC voltage for a three-phase system or the terminal phase voltage for a single-phase system. Each region of the reference curve (VV or VW) can be regarded as a unique and well defined state of the inverter. For example, in Figure 5.2, the inverter has five possible states from R1 through R5. Furthermore, each state of the inverter has a predefined transition boundary for the control signal. In case of VV mode, the transition boundary for each state is as follows,

$$\text{Inverter state in VV mode} \begin{cases} \text{R1}, & V_{pcc} \leq P1 \\ \text{R2}, & P1 < V_{pcc} \leq P2 \\ \text{R3}, & P2 < V_{pcc} \leq P3 \\ \text{R4}, & P3 < V_{pcc} \leq P4 \\ \text{R5}, & P4 < V_{pcc} \end{cases} \tag{5.2}$$

where V_{pcc} is the inverter control signal. Similarly in case of VW mode, the transition boundaries are defined as,

$$\text{Inverter state in VW mode} \begin{cases} \text{R1}, & V_{pcc} \leq \frac{1}{m} x_{pv} + \frac{1}{c} \\ \text{R2}, & \frac{1}{m} x_{pv} + \frac{1}{c} < V_{pcc} \leq P2 \\ \text{R3}, & P2 < V_{pcc} \end{cases} \tag{5.3}$$

where m and c is the slope and intercept of the line joining P1 and P2 (see Figure 5.5). There are two important distinctions between an inverter (in VV or VW mode) and a volt-



(a) (b)

Figure 5.7: Residual error (absolute) in estimating the control voltage of the inverter (at bus 675) using SbML. The inverter is operating in VV mode with its state fixed in region R2. The horizontal plane and the red dotted line represent the upper boundary of R2. The feasible solution space is denoted by the unshaded region.

age regulator or a capacitor bank. First, instead of causing discrete jumps, the inverter introduces knots in the voltage-power manifold. Second, it does not have delays in the controller logic and acts instantaneously.

By considering the inverter as a part of the set of system controllers, an accurate linearization the manifold can be done using SbML. Let $u_i(t)$ denote the state of a controllable element at time t. For an inverter, $u_i(t) \in \{1, 2, .., 5\}$ in VV mode and $u_i(t) \in \{1, 2, 3\}$ in VW mode. The system controller state at time t is now dependent not only on the state of voltage regulators and capacitor banks, but also upon the state of the inverters in the feeder (see equation (3.16)). Consequently, whenever the state of the inverter changes, a new set of plane coefficients are estimated. And since the manifold exhibits an almost linear behavior for a fixed s_t, the SbML produces very little estimation error. Figure 5.7 shows the estimated and actual control voltage of the inverter at bus 675 (in VV mode) in the IEEE 13-bus circuit. The inverter state is in region R2, the regulators are at their nominal tap positions and the capacitor bank is in a connected state. The linearization is done around an arbitrary point $x^* = (0.85, 0.25)$. The inverter state does not change as long as V_{pcc} remains

within R2. The maximum absolute estimation error within this feasible solution space is 0.04V (120 V_{base}). If the PCC voltage crosses into R3, the system controller state changes resulting in re-linearization of the voltage-power manifold. The plane coefficients corresponding to this new s_t inherently capture the impact of the knot introduced by the inverter. In this manner, a piece-wise linear model of the voltage-power manifold is generated by the fast QSTS algorithm.

Two important metrics of interest linked to VV and VW modes are total reactive energy injected/absorbed and total real energy curtailed by the inverter, respectively. This is because reactive power directly impacts the losses within the distribution feeder. On the other hand, real power curtailment results in reduced the revenue for the owner of the PV system. A high resolution, yearlong QSTS analysis is the only viable method to estimate these metrics. Formally, they can be defined as,

$$\begin{aligned} E^i_+(\text{kVARh}) &= \frac{1}{3600}\int_0^{T_f} Q^i_+(t)\ dt \\ E^i_-(\text{kVARh}) &= \frac{1}{3600}\int_0^{T_f} Q^i_-(t)\ dt \\ E^i(\text{kWh}) &= \frac{1}{3600}\int_0^{T_f} (x_i(t) - P^i_{out}(t))\ dt \end{aligned} \tag{5.4}$$

where $Q^i_+(t), Q^i_-(t), x_i(t), P^i_{out}(t)$ are the profiles of reactive power produced, reactive power consumed, input power injection and real power output of the PV system i over the simulation time horizon T_f, respectively. Estimating these metrics using the fast QSTS algorithm is a trivial task. In FPF mode, the reactive power output is directly proportional to the input PV profile (see Figure 5.1b). In VV mode, the reactive power feed-in is dictated by the state of the inverter, however, the magnitude is directly proportional to the load and the PV profiles. Similarly, in VW mode, the real power output is dependent on the mode of the inverter but still maintains a linear relationship with the input profiles (see Figure 5.6b). Therefore, the proposed linear sensitivity model can easily estimate the real and reactive power output of the PV system, for a given s_t, by using multiple regression.

The proposed algorithm can accommodate other types of devices as well including energy storage (ES), electric vehicles (EV) and switches. The charging and discharging of ES and EV can be modeled as an input profile to the fast QSTS algorithm. The control logic of the switch can be abstracted in a manner similar to the other controllable elements. It has two unique states i.e. on and off. In addition, the state transitions are driven by a predetermined signal rather than voltage or current. Hence by adding switches to the set of system controllers, their behavior can be easily simulated. In the following section, we evaluate the performance of the fast QSTS algorithm on various test circuits with smart inverters and switches.

5.4 Simulation Case Study: IEEE 123-Bus

The IEEE 123-bus is a 4.16 kV test circuit, with 278 nodes [95]. The length of the circuit is 6.2 km and requires the use of an LTC as well as multiple LVRs and shunt capacitor banks to provide voltage regulation. The single line diagram of the feeder is shown in Figure 5.8. There are a total of 84 single phase loads, attached to phase A, B and C of the circuit. In addition, 7 loads are connected to more than one phase. The feeder serves a peak load of 3.6 MW and contains a total of 7 controllable devices: a single three-phase substation LTC transformer (33 taps) and 6 single-phase LVRs (33 taps). Each load is assigned a unique 1-second, yearlong power injection profile depending upon if its connected to phase A, B or C. Furthermore, the loads attached to more than one phase are assigned another unique power injection profile. All load profiles are synthesized from SCADA measurements of the feeder CO1 (discussed earlier in section 4.3).

The default IEEE 123-bus circuit has no PV installation. To simulate 50% PV penetration, a 1.8 MW utility scale three-phase PV system (PV_{c1}) is installed at the end of the feeder using a 1.98 MVA smart inverter. A unique 1-second, yearlong power injection profile, similar to the one used for IEEE 13-bus test circuit, is assigned to this PV system. To simulate feeder reconfiguration, the upper right corner of the circuit is fed from switch

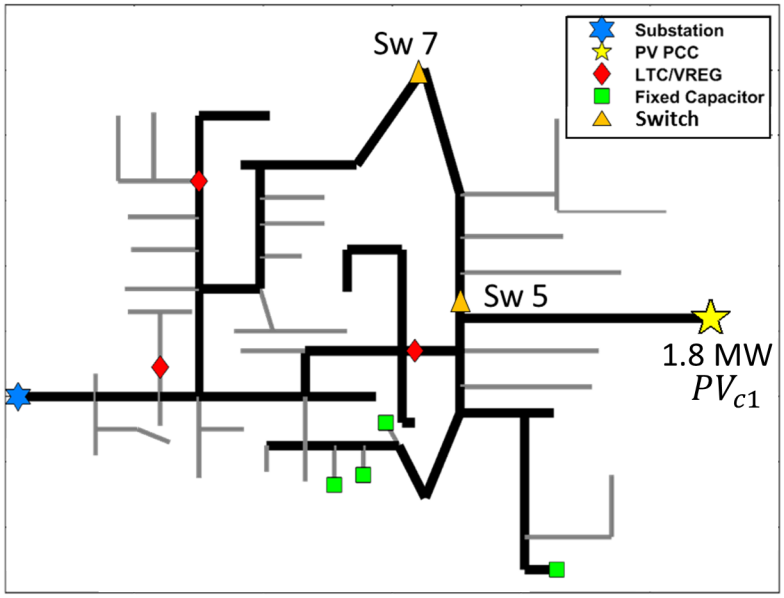


Figure 5.8: Circuit diagram of the IEEE 123-bus test circuit with a centralized PV system installed at the end of the feeder.

7 instead of switch 5 during the summer months (May 15th to September 15th). Lastly, the voltage regulators in the default feeder are modified to include reasonable delays (45-60 secs). We simulate two different scenarios to test the efficacy of the proposed algorithm.

5.4.1 Case A: Inverter in FPF mode

In the first scenario, the PV_{c1} inverter is configured to operate at a 0.98 lagging power factor to compensate for the voltage rise caused by the PV system. Table 5.1 shows a comparison of the QSTS simulation results obtained by using brute-force method and the proposed fast QSTS algorithm. The estimation error is calculated by comparing the results of the proposed algorithm with the baseline 1-second resolution, yearlong brute-force QSTS. The RMS error in estimating the states of voltage regulators is 1.01%. In addition, the errors in estimating the voltage extremities as well as duration of ANSI limit violations (Range A, 126/117 V on a 120 V_{base}) are well under the specified thresholds. Since the PV system is operating at a lagging power factor, it only absorbs reactive power. The error in estimating the total reactive energy absorbed by the inverter is less than 0.2% for the yearlong

Table 5.1: Accuracy comparison of the fast QSTS algorithm (IEEE 123-bus: Case A)

QSTS Metric	**Brute-force**	**Fast QSTS (error)**
Regulator tap actions:		
Sub LTC (3-ϕ)	403	-0.49%
VReg 1 (A-ϕ)	252	0%
VReg 2 (A-ϕ)	1219	0%
VReg 3 (C-ϕ)	536	+1.11%
VReg 4 (A-ϕ)	2286	+0.17%
VReg 5 (B-ϕ)	1653	0%
VReg 6 (C-ϕ)	415	-5.3%
Feeder phase voltage:		
Highest	1.0588 p.u.	-0.0006 p.u.
Lowest	0.9643 p.u.	-0.0006 p.u.
Duration of ANSI violations:		
Over voltage	115.5 Hrs	+1.64 Hrs
Under voltage	101.9 Hrs	+2.52 Hrs
Total kVARh absorbed:		
PV_{c1} (3-ϕ)	7.056×10^5	+0.15%
Per phase voltage (each bus):	total of 278 nodes	
Highest	0.0002 p.u. (mean error)	
Lowest	0.0005 p.u. (mean error)	

Table 5.2: Timing comparison of the fast QSTS algorithm (IEEE 123-bus: Case A)

	Brute-force	**Fast QSTS**	**% Reduction**
Total time taken	1.52 hours	19.9 secs	99.64%
Power flow solutions	31.5 million	5,379	99.98%

simulation.

A timing comparison of the proposed algorithm with the brute-force QSTS is established in Table 5.2. The fast QSTS algorithm takes less than 20 seconds to compute all the voltage-related impact metrics, which corresponds to a speed increase of more than 270 times. Estimating plane coefficients for each state requires 11 power flow solutions (since there are five input profiles). Consequently, a total of 5,379 nonlinear AC power flows are solved for the yearlong time series simulation.

Table 5.3: Accuracy and timing comparison (IEEE 123-bus: Case B)

QSTS Metric	**Brute-force**	**Fast QSTS (error)**
Regulator tap actions:		
Sub LTC (3-ϕ)	397	+1.15%
VReg 1 (A-ϕ)	236	+2.54%
VReg 2 (A-ϕ)	1155	+1.21%
VReg 3 (C-ϕ)	524	+2.29%
VReg 4 (A-ϕ)	1456	+4.53%
VReg 5 (B-ϕ)	563	0%
VReg 6 (C-ϕ)	375	+1.06%
Duration of ANSI violations:		
Over voltage	107.05 Hrs	-4.28 Hrs
Under voltage	112.31 Hrs	-2.52 Hrs
Total kVARh absorbed:		
PV_{c1} (3-ϕ)	6.347×10^5	+0.38%
Total kWh curtailed:		
PV_{c1} (3-ϕ)	3.490×10^5	-0.38%
Total time taken	3.4 hours	32.3 secs
Total power flow solutions	31.5 million	7,392

5.4.2 Case B: Inverter in VW mode

In the second scenario, the inverter is configured to curtail its real power output while operating at a 0.98 lagging power factor. The reference VW curve is shown in Figure 5.5. Table 5.3 shows the accuracy and timing comparison of the fast QSTS algorithm. The RMS error in estimating the states of voltage regulators is 1.82%. Notice the significant drop in the total number of regulator tap actions of Vreg 4 and 5, when compared to case A. This is due to their close proximity to the PV system, which is now curtailing its real power output to reduce the voltage variability. Figure 5.9 shows the real power curtailed (during day 4) by the PV inverter. The error in estimating the total real energy curtailed by the inverter is less than 0.4%. The observed maximum and minimum feeder voltages in this case were similar to case A, and therefore are not shown in the table. The brute-force QSTS takes significantly longer to simulate the smart inverter VW mode of operation due to the complex iterative process required to ensure the convergence of the power flow solution

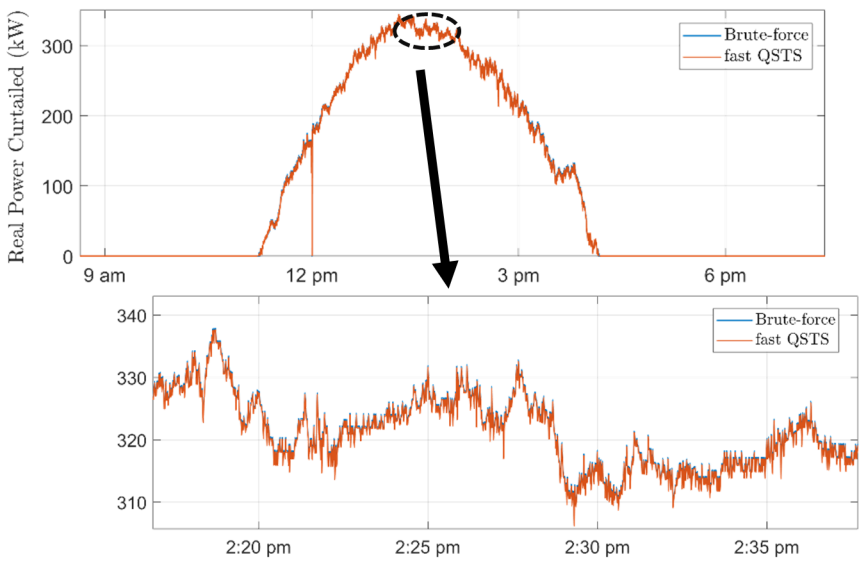


Figure 5.9: Real power curtailed by the PV inverter during the time series simulation (for day 4).

[96]. The proposed algorithm, on the other hand, shows an impressive speed improvement of more than 370 times, when compared to the brute-force approach.

5.5 Simulation Case Study: Utility Feeder CO1_VV

In this case study, we modify the centralized PV systems (PV_{c1} and PV_{c2}) in the feeder CO1 and interface them via 10% overrated smart inverters operating in VV mode. The single line diagram of the feeder is shown in Figure 4.6. Since PV_{c1} is in close proximity to the three single-phase LVRs, the deadband of its VV curve is designed to overlap with the deadband of the LVRs. This prevents the inverter from only absorbing reactive power. Figure 5.10 shows the reference VV curves for both PV_{c1} and PV_{c2}. Inverters operating in VV mode usually turn off at night time. To replicate this behavior, inverters for both PV_{c1} and PV_{c2} are configured to turn off if their real power output drops below 0.001 p.u. This particular test case allows us to evaluate the performance of the proposed algorithm in modeling smart inverter dynamic reactive power control in extended-term time series simulations.

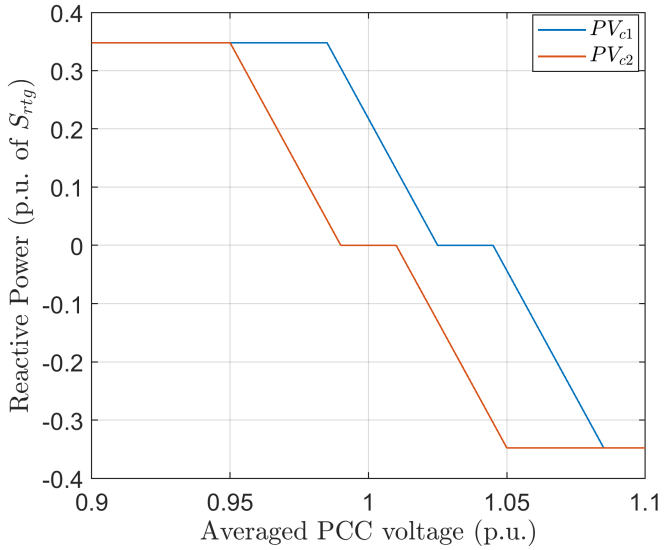


Figure 5.10: Input VV curves for centralized PV systems in feeder CO1. The deadband for PV_{c1} is between 1.025 p.u. and 1.045 p.u.

5.5.1 Simulation Results

Table 5.4 shows a comparison of the QSTS simulation results obtained by using brute-force method and the proposed fast QSTS algorithm. The RMS error in estimating the states of voltage regulators and capacitor banks is 0.88% and 4.56%. The error in estimating the total number of capacitor bank switch operations is slightly higher for Cap 2 and Cap 3. This is because of the small number of total actions recorded in the time series simulation (13.3% error corresponds to missing four capacitor bank switch operations for Cap 2). In addition, the errors in estimating the voltage extremities as well as duration of ANSI limit violations (Range A, 126/114 V on a 120 V_{base}) are well under the specified thresholds. Figure 5.11 shows the reactive power output (day 1) of the inverter interfaced with PV_{c2}. During the day time, the inverter absorbs reactive power to regulate its PCC voltage around the nominal value. At night time, the reactive power output drops to zero since the inverter shuts off. The fast QSTS algorithm is able to accurately estimate the reactive power output profile with high accuracy, as shown in the figure. The RMS error in estimating total reactive energy injected and absorbed by the inverters is 2% and 1%, respectively.

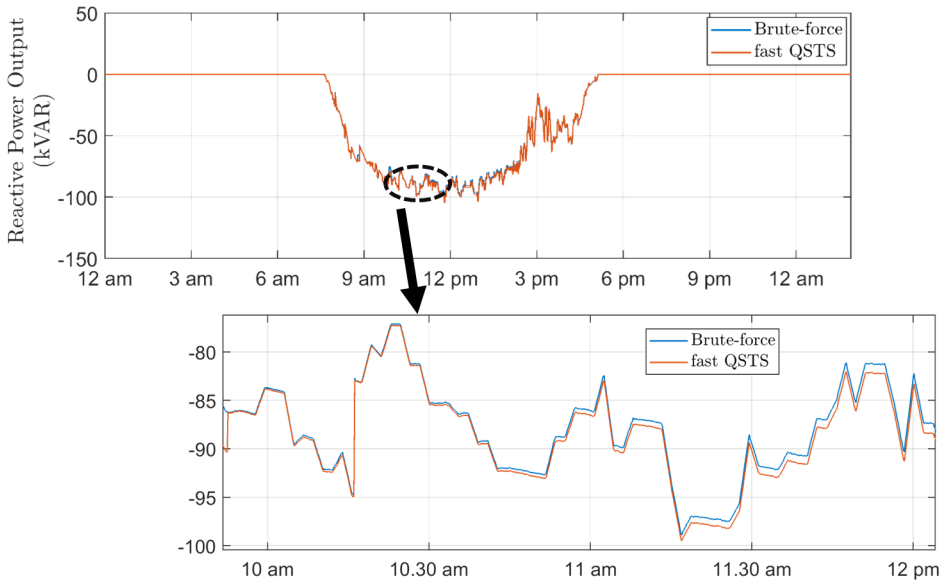


Figure 5.11: Reactive power output of the PV_{c2} inverter during the time series simulation (for day 1).

A timing comparison of the proposed algorithm with the brute-force QSTS is established in Table 5.2. The brute-force algorithm takes around three days to run. This is because of the complex iterative process required to accurately simulate smart inverter dynamic reactive power control [96]. On the other hand, the fast QSTS algorithm takes less than 30 minutes to compute all the voltage-related impact metrics. As the number of inverters in the circuit increase, the time taken by the brute-force solution rises exponentially. However, the proposed algorithm shows a linear increase in time due to the limited number of required power flow solutions.

Table 5.4: Accuracy comparison of the fast QSTS algorithm (CO1_VV)

QSTS Metric	**Brute-force**	**Fast QSTS (error)**
Regulator tap actions:		
Sub LTC (3-ϕ)	2701	+0.07%
VReg 1 (A-ϕ)	4976	+1.36%
VReg 2 (B-ϕ)	4822	-0.45%
VReg 3 (C-ϕ)	4704	+1.65%
Capacitor switches:		
Cap 1 (3-ϕ)	360	-0.55%
Cap 2 (3-ϕ)	30	-13.3%
Cap 3 (3-ϕ)	24	-8.33%
Cap 4 (A-ϕ)	526	-0.38%
Cap 5 (B-ϕ)	752	-0.26%
Feeder phase voltage:		
Highest	1.0613 p.u.	-0.0001 p.u.
Lowest	0.9067 p.u.	$<$0.0001 p.u.
Duration of ANSI violations:		
Over voltage	223.07 Hrs	+11.08 Hrs
Under voltage	129.39 Hrs	-3.56 Hrs
Total kVARh injected:		
PV_{c1} (3-ϕ)	1220.9	-2.69%
PV_{c2} (3-ϕ)	3898.8	-1.46%
Total kVARh absorbed:		
PV_{c1} (3-ϕ)	10.76	-1.46%
PV_{c2} (3-ϕ)	7.923×10^4	+0.58%
Per phase voltage (each bus):	total of 5469 nodes	
Highest	0.0005 p.u. (mean error)	
Lowest	0.0002 p.u. (mean error)	

Table 5.5: Timing comparison of the fast QSTS algorithm (CO1_VV)

	Brute-force	**Fast QSTS**	**% Reduction**
Total time taken	67.4 hours	29.8 minutes	99.26%
Power flow solutions	31.5 million	78,884	99.74%

CHAPTER 6

ESTIMATING CURRENT-RELATED PV IMPACTS USING FAST QSTS

6.1 Introduction

For reliable operation of the distribution system, an important consideration is to not exceed the ampacity ratings of the various circuit elements (transformers, overhead/underground lines, switches and protection devices). Exceeding the maximum ampacity rating for periods of time can cause overheating which can damage the conductor insulation, causing faults and even worse, total equipment failure. High penetrations of PV systems can easily overload the distribution system infrastructure in different ways [8]. Often coincident nature of peak PV output can result in excessive power injections back into the grid, which can potentially overload the circuit elements between such PV systems and load centers. In addition, distributed PV systems can have a *masking* effect on the native load of a given feeder. Consequently, the sudden loss of generation or disconnection of PV systems can cause excessive overloading if the proper analysis and upgrades are not performed beforehand. Another potential undesired outcome of high PV penetration is an increase in the overall system losses, which can have economic repercussions. These impacts are a direct consequence of the current injections by the PV systems and henceforth, are referred to as current-related PV impacts. An important aspect of running a QSTS analysis is identifying these impacts, and in particular, detecting potential thermal overloading of the distribution infrastructure that might arise due increased solar PV penetration. Thermal loading ρ_n of a conductor n is expressed as a percentage of the current magnitude I flowing through the conductor given its steady-state thermal rating I_r. The IEEE 738-2012 defines the steady state thermal rating as the constant electrical current that would yield the maximum allowable conductor temperature for specified weather conditions and conductor characteristics

under the assumption that the conductor is in thermal equilibrium [97]. A value of ρ_n greater than 100 indicates thermal overloading of the respective conductor.

In this chapter, we extend the linear sensitivity model to estimate the branch current magnitude using a technique referred to as decomposition analysis. A major challenge in estimating the current magnitude is its nonlinear nature, which is primarily caused due to the reverse power flow in the circuit. However, by decomposing the current magnitude into its constituent parts, the linear sensitivity model can be used to create an approximation of the highly nonlinear current-power manifold. Furthermore, the accuracy of the proposed decomposition-based method is evaluated on a variety of 3-phase, unbalanced test circuits using the fast QSTS algorithm. This chapter covers the work originally presented in [98].

6.2 Current Estimation using Linear Sensitivity Model

6.2.1 Impact of Power Injections on Branch Current

To better understand the correlation between current magnitude and the power injection profiles, we consider a simplified two bus circuit shown in Figure 6.1. The generator at bus j is a solar PV operating in Fixed Power Factor (FPF) mode. To simplify the analysis, we assume that the transmission line connecting bus i to j has minimal losses which implies,

$$\begin{aligned} P_i &= P_{Lj} - P_{Gj} \\ Q_i &= Q_{Lj} - Q_{Gj} \end{aligned} \tag{6.1}$$

where P_i and Q_i are the real and reactive power supplied by bus i. The magnitude of current flowing from bus i to j is then given by the expression,

$$I_{ij} = \frac{\sqrt{P_i^2 + Q_i^2}}{V_i} \tag{6.2}$$

where V_i is the voltage magnitude at bus i. For a constant load demand (P_{Lj}, Q_{Lj}), we can make the following observations regarding the current magnitude,

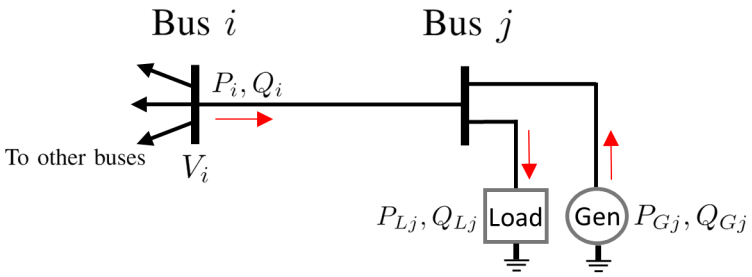


Figure 6.1: Simplified two bus circuit with a load and a PV connected to bus j.

- As the power injected by the PV (P_{Gj}, Q_{Gj}) increases, the apparent power through bus i decreases. (Eq. 6.1)
- This decrease in apparent power reduces the magnitude of current I_{ij}. (Eq. 6.2)
- The magnitude of current will become zero only when the real and reactive power demand is met locally by the PV system. This is rarely the case because PV systems are usually rated to meet the real load demand and generate reactive power only for voltage stability. In the case where $P_{Gj} = P_{Lj}$, the net reactive power demand will be met by Q_i, which implies $I_{ij} \neq 0$. (Eq. 6.2)
- If the PV system is over rated ($P_{Gj} > P_{Lj}$), after the real power demand is met, excess power is injected back into the bus i, which implies that the magnitude of current I_{ij} starts to increase again. (Eq. 6.2)

Based on these observations, it is evident that the magnitude of current flowing from bus i to j exhibits a highly non-linear, convex behavior. Furthermore, in the presence of system losses and mutual coupling between the lines, the overall behavior would be the same however, the minima will shift depending upon the circuit topology. We utilize the 3-phase, unbalanced, non-symmetrical IEEE 13-bus test circuit (discussed in section 3.3.1) to visually show this behavior in Figure 6.2. The x-axis represents the per unit value of the real power injected by the PV system, and the y-axis shows the phase A current magnitude in line 671.692[1]. The minimum value of current shifts upwards as the load connected to

[1]Line 671.692 refers to the phase conductors connecting bus 671 to bus 692.

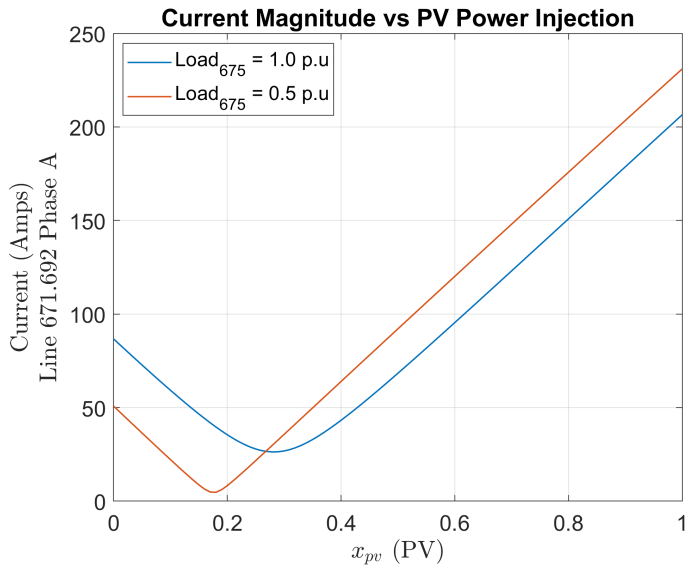


Figure 6.2: Impact of PV power injection on the current flowing through a line for the modified IEEE 13-bus test circuit. Notice how the minima shifts downwards as the value of load decreases however never reaches zero.

bus 675 increases because of the increased reactive power demand.

6.2.2 Impact of Capacitors and Regulators on Branch Current

Voltage regulators change their tap positions to regulate the voltage at the secondary winding of the transformer, thereby ensuring that the bus voltage remains within the specified range. On the other hand, capacitor banks change the reactive power demand in the circuit which changes the bus voltages. The discrete control actions of regulators and capacitor banks can cause jumps in the voltage-power manifold, as shown in earlier. In a similar manner, changing the tap position would also cause jumps in the *current-power* manifold because of the dependence of branch current on the voltage magnitude (Eq. 6.2). In case of a capacitor bank, depending upon its rating and location, this effect would be more pronounced as shown in Figure 6.3. The y-axis represents the per unit apparent power injection of all the loads connected to the circuit whereas the x-axis is the same as before. From Figure 6.3, it is evident that the impact of voltage regulators and capacitors cannot be ignored while estimating the current magnitude.

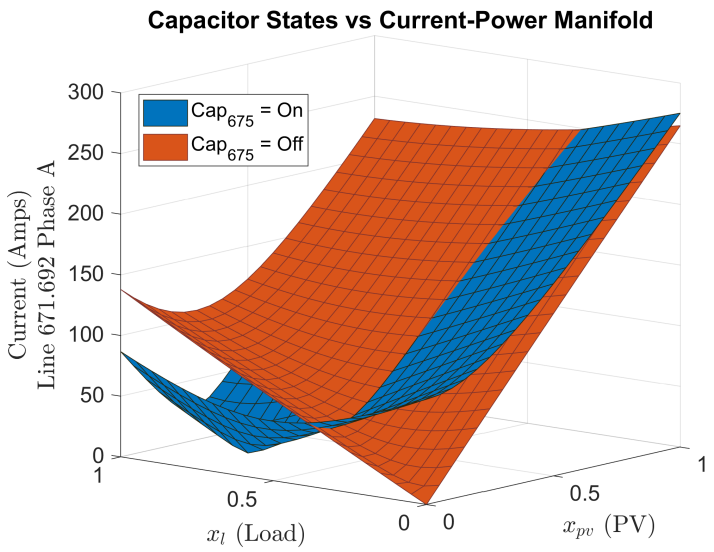


Figure 6.3: Impact of connecting (on) and disconnecting (off) a 3-phase, 600 kVAR capacitor on the current-power manifold for the IEEE 13-bus test case. Disconnecting the capacitor changes the net reactive power demand at bus 675, which causes the current magnitude to increase. The plot is obtained by disabling the capacitor controller and manually changing its state in OpenDSS.

6.2.3 Decomposition Analysis for Current Estimation

Unlike bus voltages, the current-power manifold exhibits a highly non-linear behavior; therefore, a linear correlation between current magnitude and power injections cannot be established. To efficiently utilize the linear sensitivity model, we propose decomposing the current magnitude into its constituent parts using equation (6.2). For a given system controller state, the real P_i and reactive Q_i powers supplied by bus i have a direct correlation with the power injection profiles (Eq. 6.1). As the apparent power of the loads increase, so does P_i and Q_i, however, the relationship is not strictly linear because of the system losses. Figure 6.4 shows the real and reactive power supplied by phase A of bus 671 as a function of the load and PV power injections. The real and reactive power manifolds (collectively referred to as PQ manifold) represent all the possible solutions of equation (3.12) within the valid solution space, $(x_l, x_{pv}) \in [0, 1]$. The negative sign indicates a change in the power flow direction i.e. power being absorbed by bus 671. We propose using the linear

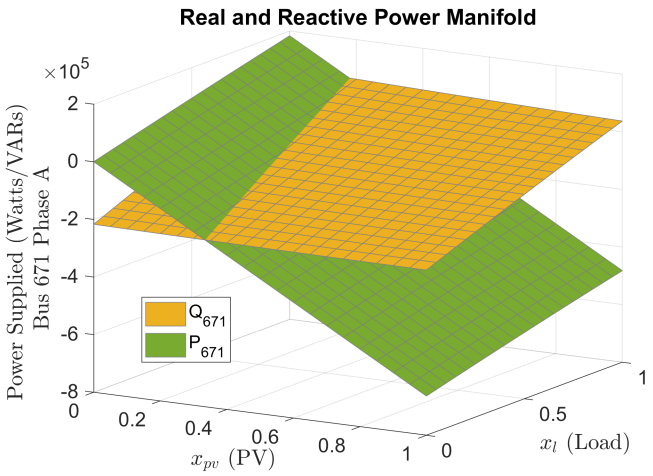


Figure 6.4: Real and reactive power supplied by bus 671 for the IEEE 13-bus test case, obtained by solving 441 discrete power flows. At zero load and PV power injection, the reactive power is negative because of the capacitor at bus 675, which is in on state.

sensitivity model to create a linearization of the PQ manifold, for every bus in the circuit. Let $p_\phi^{(j)}$ and $q_\phi^{(j)}$ denote the dependent variables, which represent the estimated real and reactive power injection of phase $\phi \in \{A, B, C\}$ at bus j. Without loss of generality, we drop the subscript ϕ to keep the formulation concise. For n power injection profiles, the relationship between $p^{(j)}, q^{(j)}$ and x_i is given by,

$$\left.\begin{aligned} p^{(j)} &= \lambda_0 + \textstyle\sum_{i=1}^{n} \lambda_i x_i, \\ q^{(j)} &= \psi_0 + \textstyle\sum_{i=1}^{n} \psi_i x_i, \end{aligned}\right\} \forall j \in \mathcal{N} \tag{6.3}$$

where λ_i and ψ_i are the power sensitivity factors that indicate an incremental change in real and reactive power transfer at a bus that occurs due to a per unit increase in load or PV power injections. Power sensitivity factors are similar to power-transfer distribution factors discussed in [99]. The magnitude of current flowing from bus j to k is given by,

$$i^{jk} = \frac{\sqrt{p^{(j)^2} + q^{(j)^2}}}{v^{(j)}} \tag{6.4}$$

The power sensitivity factors can be calculated using the framework of multiple linear regression. Let $\Lambda_{s_t}^{(j)} = [\lambda_0, \lambda_1, ..., \lambda_n]_{s_t}^{(j)}$ denote the vector of plane coefficients corresponding to the real power manifold for bus j. We propose using the SbML method to formulate the design matrix $\boldsymbol{X}$. The observed real power vector, $\boldsymbol{P}^{(j)} \in \mathbb{R}^{2n+1}$, is obtained by solving the nonlinear AC power flow equations corresponding to each query point in $\boldsymbol{X}$. Using the ordinary least squares estimator, the plane coefficients corresponding to a given system controller state s_t are then given by,

$$\Lambda_{s_t}^{(j)} = (\boldsymbol{X}^\top \boldsymbol{X})^{-1} \boldsymbol{X}^\top \boldsymbol{P}^{(j)} \tag{6.5}$$

Similarly, $\Psi_{s_t}^{(j)} = [\psi_0, \psi_1, ..., \psi_n]_{s_t}^{(j)}$ can be calculated by replacing $\boldsymbol{P}^{(j)}$ with $\boldsymbol{Q}^{(j)}$ (the vector of observed reactive power at bus j) in equation (6.5).

6.2.4 Error Performance of the Decomposition Method

To evaluate the error in estimating the current magnitude using the linear sensitivity model, we utilize the IEEE 13-bus test case (discussed in section 3.3.1), with VReg 1 (phase A LVR at substation) enabled. This allows us to show the impact of change in system controller state on the estimation error as well. Figure 6.5 shows the absolute error (in percent) between the estimated and actual value of phase A current flowing from bus 671 to 692. For ease of visualization, the PV power injection is fixed to a constant value ($x_{pv} = 0.5$) and the circuit loading is varied by changing x_l from 0 to 1. The orange lines indicate the estimation error due to the linear sensitivity model. The discontinuities are caused due to the LVR changing its tap position, which results in recomputation of the sensitivity coefficients for both power and voltage. The grey shaded region represents the permissible values of apparent power injections of all the loads for which the control voltage of the LVR remains within the deadband and no action is taken (feasible solution space). As shown, the error is well behaved and bounded within this region with a maximum value of 0.04%.

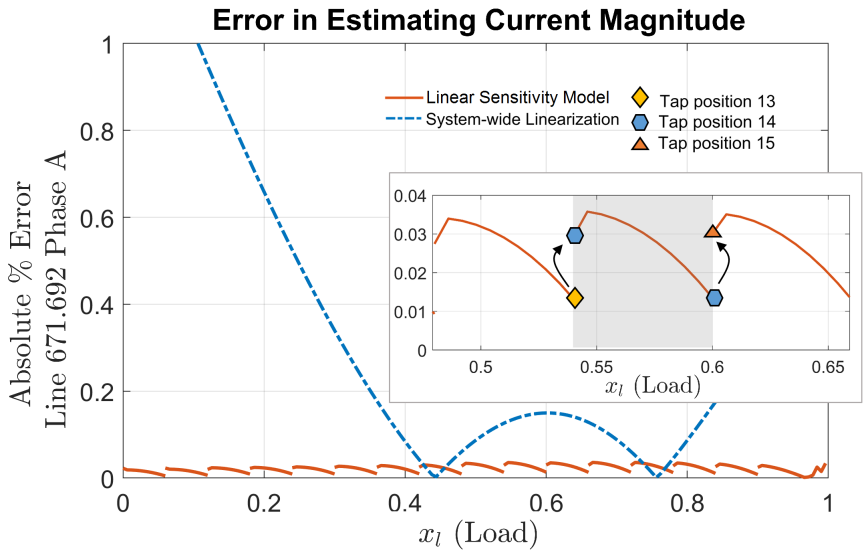


Figure 6.5: Error performance of the linear sensitivity model for estimating phase current magnitude. The grey shaded region represents the feasible solution space.

For comparison, we also plot the percentage error (dashed blue) while completely ignoring the state of the voltage regulator, which is referred to as *system-wide linearization*. In this case, the error performance is similar to Figure 3.3b, which is due to the nonlinear nature of voltage-power and PQ manifolds. As expected, the system-wide linearization produces significant estimation errors as the voltage deviation from the nominal increases (nominal voltage is obtained around $x_l = 0.6$).

6.2.5 Current-related QSTS Metrics

Table 6.1 shows the current-related QSTS metrics that are commonly used to evaluate the impacts of installing PV in a distribution feeder [8]. The acceptable error thresholds have been established in [18]. To calculate metrics 1-2, the per phase current profile flowing across each circuit element is required, which can be obtained by solving equation (6.4), at each time-step. However, similar to voltage profile, we propose using the nonuniform reconstruction method to determine the highest thermal loading along with the duration of thermal overload for each circuit element. Furthermore, since the power flows in and out of each bus are known (Eq. 6.3), the line losses can be calculated as a by-product. For

Table 6.1: Current-related PV impact metrics measured by QSTS

	QSTS Metrics	Error Threshold
1	Highest Thermal Loading (per component)	5%
2	Duration of Thermal Overload (per component)	24 Hrs
3	Total Feeder Line Losses	5%

example, for an arbitrary transmission line connected between bus i and j, the real power line loss for a given phase ϕ is simply $p_{\phi}^{(i)} - p_{\phi}^{(j)}$. The total feeder line loss is just the sum of real power losses observed across all the phase conductors in the circuit over a given simulation time horizon.

6.3 Simulation Case Studies

In this section, we evaluate the accuracy of the proposed algorithm in estimating the current-related QSTS metrics on five different test circuits, namely IEEE 13-bus, IEEE 123-bus, CO1, CO_VV and J1. The details pertinent to these test circuits have already been discussed in chapters 4 and 5. The baseline results are obtained using a 1-second resolution, yearlong brute-force QSTS simulation. Figure 6.6 shows the accuracy of the proposed method in estimating the maximum thermal loading for each of the test cases. For the IEEE 13-bus case, the accuracy comparison is shown for all of the 17 circuit elements (including transmission lines, LVRs and substation transformer). In case of IEEE 123-bus, CO1, CO1_VV and J1, the circuit elements that exhibited a maximum thermal loading greater than 50% are shown in the Figure 6.6. In addition, switches Sw 5 and Sw 7, used for feeder reconfiguration in the 123-bus circuit, are also shown. The branch current profiles are estimated using the nonuniform reconstruction method with a time-step of 1000 seconds. Table 6.2 shows a summary of the results for all five of the test circuits. The computational time taken by the fast QSTS includes estimating both the voltage and current-related impact metrics, listed in Table 3.1 and 6.1. Although the accuracy comparison for maximum thermal loading and overload duration is established against a small subset of circuit elements (those with

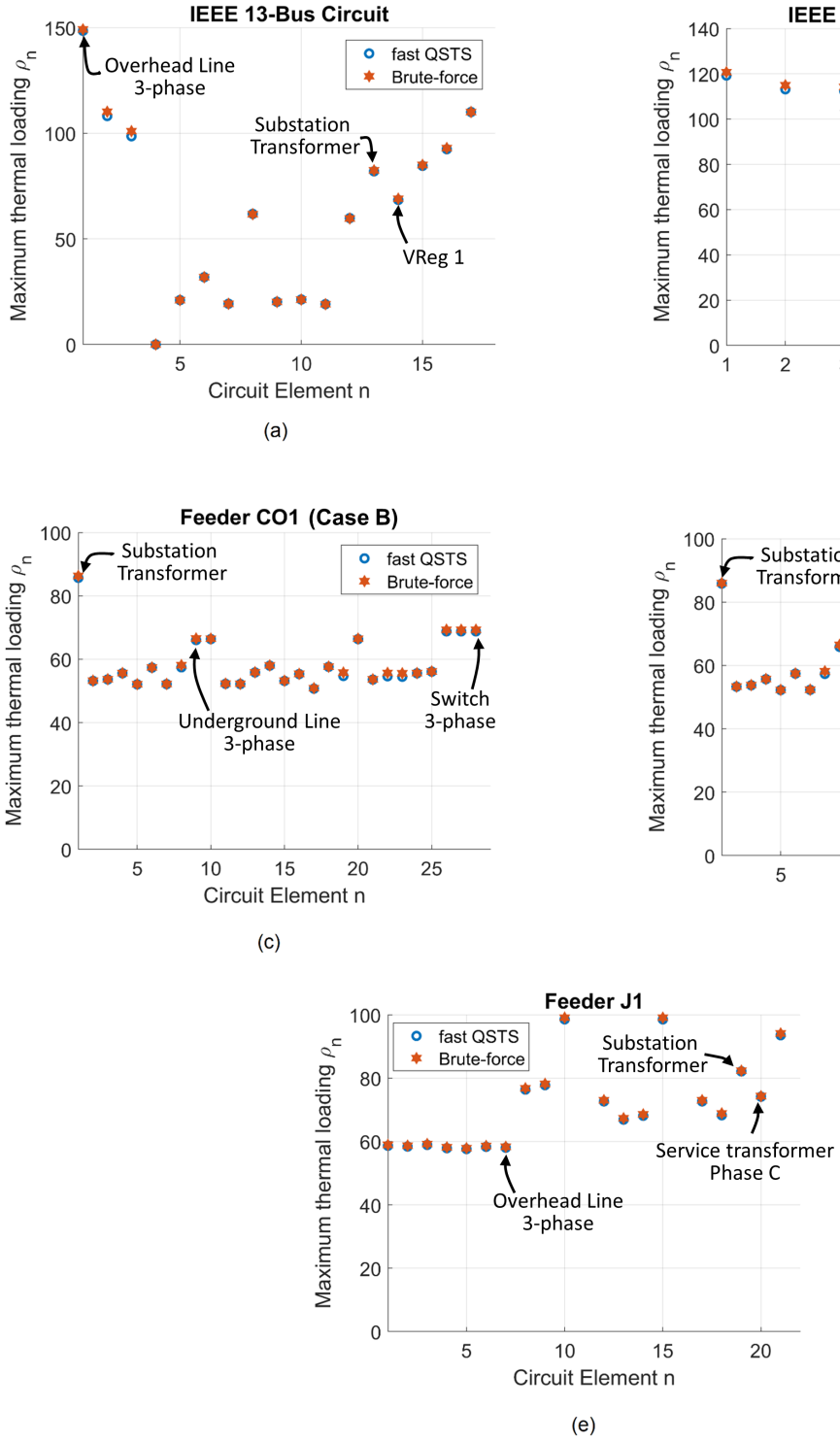


Figure 6.6: Accuracy comparison for maximum thermal loading of various circuit elements for five different test cases.

Table 6.2: Accuracy and timing comparison of the fast QSTS algorithm for various test cases

QSTS Metric	**Fast QSTS (RMS Error)**				
	13-bus	**123-bus (Case A)**	**CO1 (Case B)**	**CO1_VV**	**J1**
Regulator tap actions	0.36%	1.01%	0.71%	0.88%	0.36%
Capacitor bank switches	1.03%	N/A	1.28%	4.56%	1.11%
Per phase voltage:					
Highest	<0.0001 p.u.	0.0006 p.u.	0.0003 p.u.	0.0005 p.u.	<0.0001 p.u.
Lowest	0.0001 p.u.	0.0006 p.u.	0.0004 p.u.	0.0002 p.u.	0.0001 p.u.
Maximum thermal loading	0.44%	1.25%	0.28%	0.91 %	0.38%
Thermal overload duration	0.05 Hrs	1.56 Hrs	0.56 Hrs	0.48 Hrs	3.37 Hrs
Total line losses	-2.17%	+2.8%	+1.47%	+1.59%	+0.61%
(brute-force MWh)	(146.4)	(237.3)	(363.6)	(364.1)	(418.5)
Total time taken	10.9 secs	18.1 secs	10.5 mins	32.5 mins	19.1 mins
Speed gain (over brute-force QSTS)	78×	302×	165×	124×	76×

a maximum thermal loading greater than 50%), the computational time[2] does include the time taken to estimate these metrics for every element in the feeder. The total time taken by the proposed algorithm in Table 6.2 is slightly higher, as compared to the results presented earlier. This is due to the fact that the nonuniform reconstruction is done for both the voltage and the current profiles. Nonetheless, the fast QSTS algorithm shows an average speed improvement of around a 150 times, over the brute-force technique. Furthermore, the test cases listed in Table 6.2 represent both utility scale feeders (with low voltage secondary side) and standard IEEE test circuit, which shows the scalability and robustness of the method.

[2]The computation time does not include the communication overhead between MATLAB and OpenDSS (due to COM calls). OpenDSS requires one COM call per circuit element for obtaining the current flowing through it (in contrast to bus voltages that are returned as a vector and requires only a single COM call to read the voltages for all the buses). Therefore, for a fair comparison with the brute-force, the communication overhead is ignored.

CHAPTER 7
CONCLUSION AND FUTURE RESEARCH

7.1 Conclusion and Contributions

Understanding the impact of distributed solar photovoltaic (PV) resources on various elements of the distribution feeder is imperative for their cost effective integration. High resolution quasi-static time series (QSTS) simulations are an effective tool to identify and mitigate these impacts. However, the significant computational burden associated with running such simulations is a major challenge to their widespread adoption. The fast QSTS algorithm developed in this dissertation aims to overcome this challenge. It provides an average speed increase of around 150 times, compared to the traditional QSTS techniques, while maintaining low error thresholds.

The proposed algorithm leverages network sensitivities to estimate both the voltage and current-related solar PV impacts in distribution feeders with various voltage regulation (VR) devices, including load tap changing transformers, line voltage regulators and capacitor banks. The sensitivity coefficients for each node are estimated using a novel regression-based *perturb-and-observe* technique which is scalable to any number of input time series profiles and VR devices. These sensitivity coefficients represent a linearization of the nonlinear AC power flow manifold, and are only valid for a given state of the VR devices. If a corrective control action is performed by a VR device, the sensitivity coefficients are recomputed to account for the discontinuity caused in the AC power flow manifold by that action. Although computing these sensitivity coefficients does require solving a limited number of nonlinear AC power flow equations (perturb-and-observe), the computational time reduction comes from leveraging these sensitivities to estimate the nodal voltages and branch currents at each time-step, rather than solving the power flow problem.

The proposed algorithm can accurately estimate the states of VR devices, nodal voltage extremities, feeder duration outside ANSI C84.1 voltage limits, line losses, peak thermal loading and thermal overload duration of the circuit elements. An important feature of the algorithm is its ability to accurately simulate various smart inverter real and reactive power control functions including Volt-VAR and Volt-WATT. In addition, impact metrics related to these control functions, such as total reactive power output and total real power curtailed by the inverter, can be accurately estimated using the fast QSTS algorithm as well. This allows system planners and researchers a unique opportunity to quickly simulate a set of candidate smart inverter settings to ensure optimal performance of the PV system along with improving the reliability of the distribution grid.

To evaluate the scalability, accuracy and robustness of the algorithm, various test cases are discussed throughout this dissertation. These include both the standard IEEE test circuits and real utility-scale distribution feeders, with low voltage secondary side modeled. The algorithm provides a 98.6% reduction in computation time for a 4242 node distribution feeder with twelve VR devices, and ten 1-second resolution, yearlong input time series profiles. It produces a root mean square error of 0.55% in estimating the states of VR devices, 0.0001 p.u. in detecting the nodal voltage extremities and 0.61% in calculating the total line losses within this feeder. In comparison with other fast time series methods, the proposed algorithm shows a higher reduction in computational time and greater accuracy.

In the coming years, QSTS simulations will become an integral part of the distribution system analysis for solar PV impact studies. The significant computational time reduction means that electric utilities can more efficiently utilize QSTS simulation to evaluate PV interconnection requests. In addition, the ability to perform fast QSTS simulations like this has widespread applications to demand response control, conservation voltage reduction, locational hosting capacity and feeder reconfiguration strategies.

For a list of publications, please refer to Appendix C.

7.2 Recommended Future Work

The ideas presented in this dissertation aim at making QSTS simulation an attractive tool for evaluating solar PV impacts in distribution systems. However, research is a never ending endeavor and there is always room for advancement. The author recommends the following areas for future research work:

- The results from the fast QSTS simulations can be used to improve the hosting capacity (HC) estimates. Existing methods used by electric utilities to estimate the HC involves fixing the states of VR devices to their nominal positions (or in some cases extreme positions). Without any regulation, the amount of solar PV that can be installed at a particular node in a distribution feeder is usually limited by the over voltage constraint. As a result, the existing HC estimates are extremely conservative and unnecessarily limit the PV integration. On the other hand, the algorithm presented in this dissertation accurately tracks the states of VR devices through time. This output can be analysed further to determine the frequently occurring states of the VR devices. The upper and lower bounds of these frequently occurring states can be used to set the positions of the VR devices while determining the HC. This can lead to more realistic HC estimates that are specific to the feeder loading conditions.

- A more challenging avenue for research would be to formulate a probabilistic HC framework based on the QSTS results. The fast QSTS algorithm can be used to assign probabilities to the frequently occurring states, which could act as an input in determining the HC. Such a framework would allow distribution system planners to determine the maximum amount of PV that can be installed in a feeder with a given confidence level.

- The proposed perturb-and-observe method to estimate the sensitivity coefficients can be used to create models of various discrete-step VR devices such as voltage regulators and capacitor banks. These linear models can be used as constraints in solving

a wide variety of optimization problems including feeder reconfiguration, demand response control and conservation voltage reduction strategies.

- Lastly, the algorithm developed in this work can be used to determine the optimal smart inverter settings. Previous research done in this domain uses a very coarse resolution brute-force QSTS, mainly due to the computational time constraints [23]. However, the fast QSTS algorithm overcomes this limitation and allows for high fidelity time series simulations to be used for such an analysis.

Appendices

APPENDIX A

SUMMARY OF TEST CIRCUITS

A.1 Characteristics of the test circuits

Name	Buses, Nodes	Voltage (kV)	Peak Load (MW)	Length of Feeder	Regulating Devices	PV Penetration	Types of PV systems	Time series profiles
IEEE 13-bus	16, 41	4 .16	4.3	1.5 km	3 LVRs with LDC, 1 switching CAP bank	40%	1 centralized	2
IEEE 123-bus	132, 278	4.16	3.6	6.2 km	1 LTC and 6 LVRs with LDC	50%	1 centralized	5
Feeder CO1	2969, 5466	12.47	6.4	21.4 km	1 LTC and 3 LVRs, 5 switching CAP banks	62%	2 centralized, 142 distributed	6
Feeder J1	3433, 4242	12.47	6.3	18.1 km	1 LTC and 8 LVRs, 3 switching CAP banks	28%	2 centralized, 5 distributed	10

Additional Comments:

LVRs (or VREGs) are single phase line voltage regulators.

LTCs are 3-phase on-load tap changers installed at the substation transformer.

CAP stands for capacitor.

LVRs and LTCs have 33 taps (except for Feeder J1 where the LTC has 17 taps).

Each time series profile is 1-second, yearlong.

Centralized PV are 3-phase systems rated above 100 kW.

Distributed PV are single phase systems rated below 100 kW.

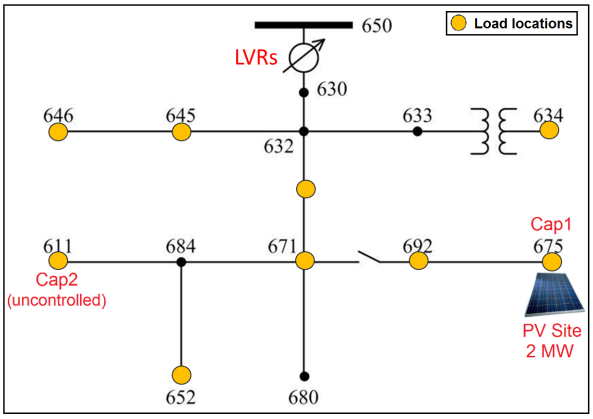
All regulating devices have delays and deadbands.

Time series data is synthesized from SCADA and on-field irradiance sensors.

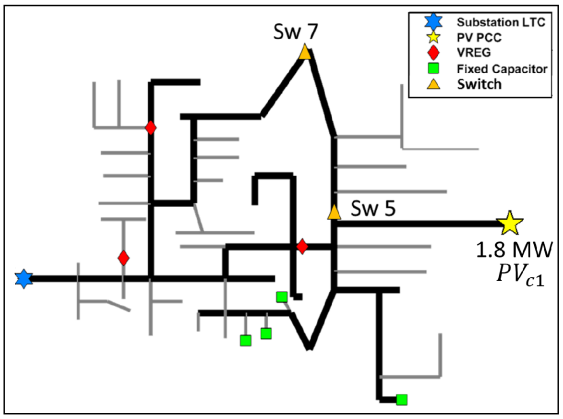
IEEE 123-bus reconfigures during the summer months using sectionalizing switches.

Feeder CO1 and J1 are actual utility feeders located in the U.S.

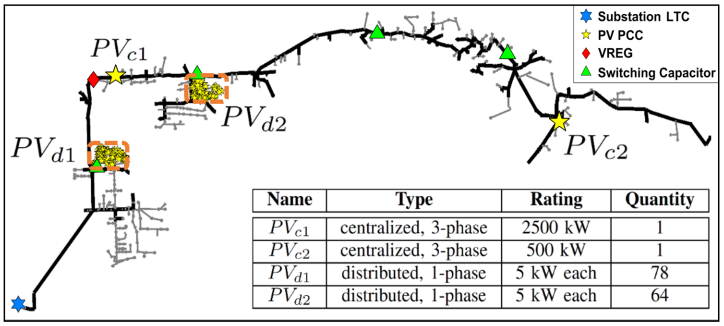
A.2 One line diagram of the test circuits



(a) IEEE 13-Bus

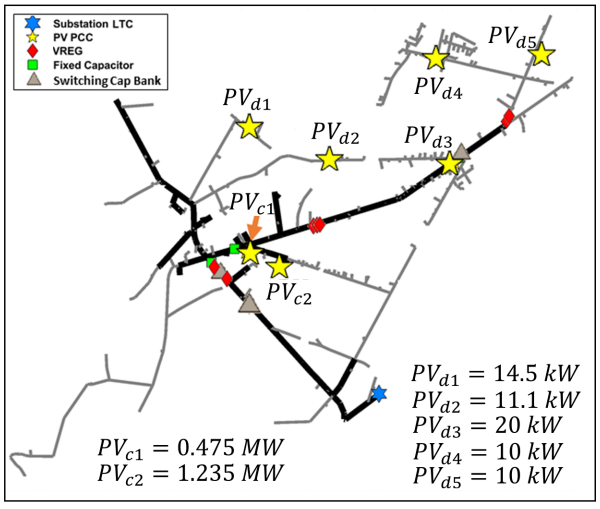


(b) IEEE 123-Bus



Name	Type	Rating	Quantity
PV_{c1}	centralized, 3-phase	2500 kW	1
PV_{c2}	centralized, 3-phase	500 kW	1
PV_{d1}	distributed, 1-phase	5 kW each	78
PV_{d2}	distributed, 1-phase	5 kW each	64

(c) Feeder CO1

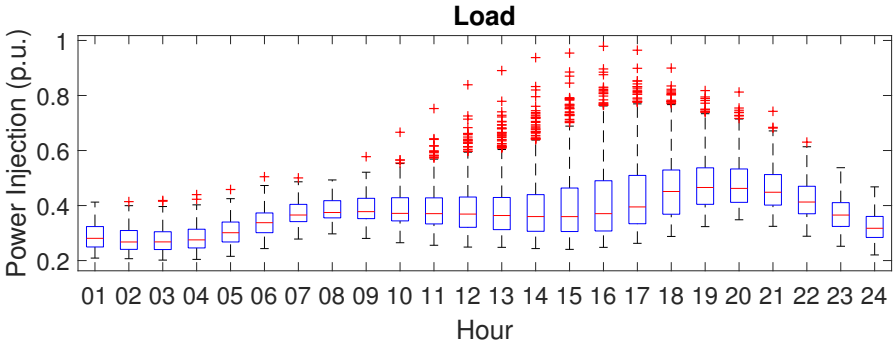


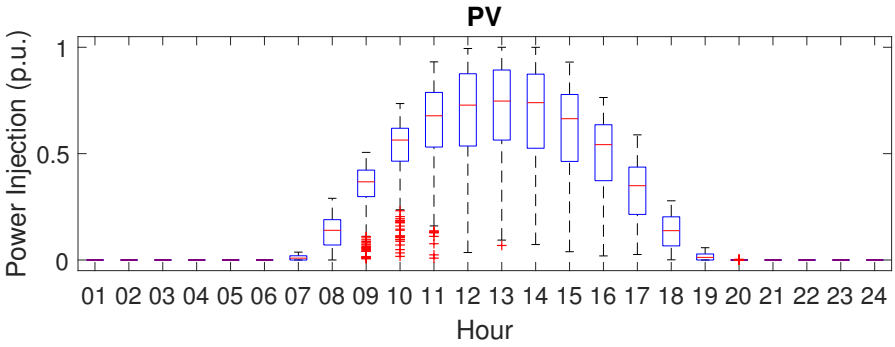
(d) Feeder J1

APPENDIX B

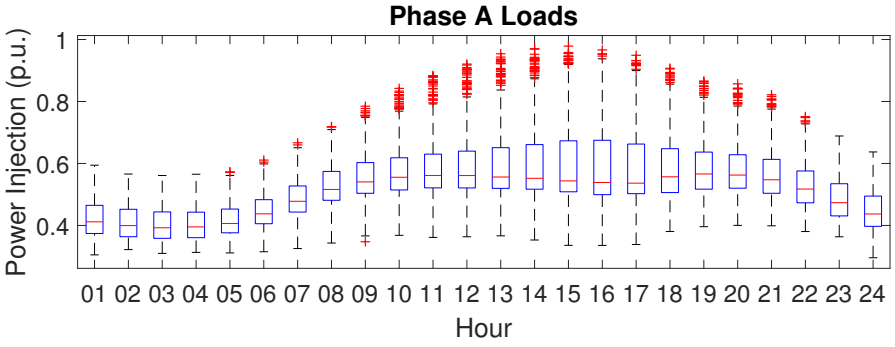
BOX PLOTS OF THE TIME SERIES PROFILES

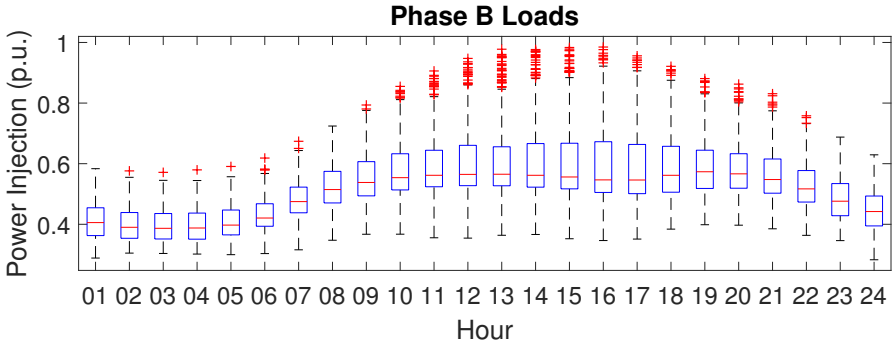
B.1 IEEE 13-bus

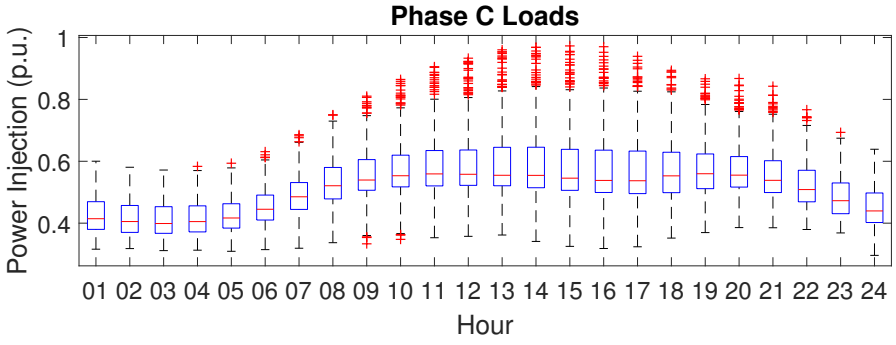


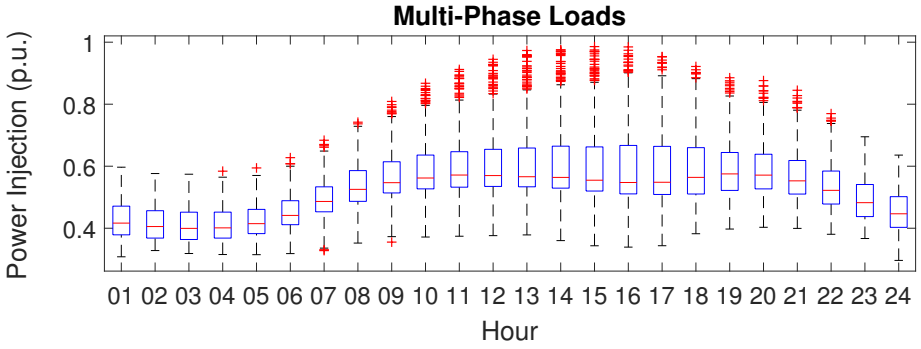


B.2 IEEE 123-bus

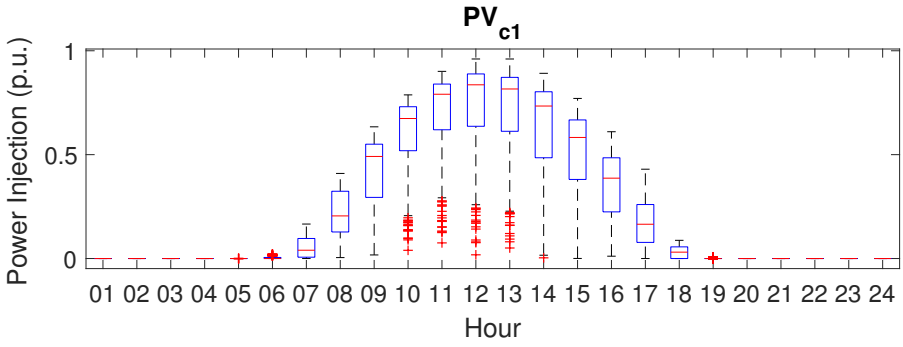


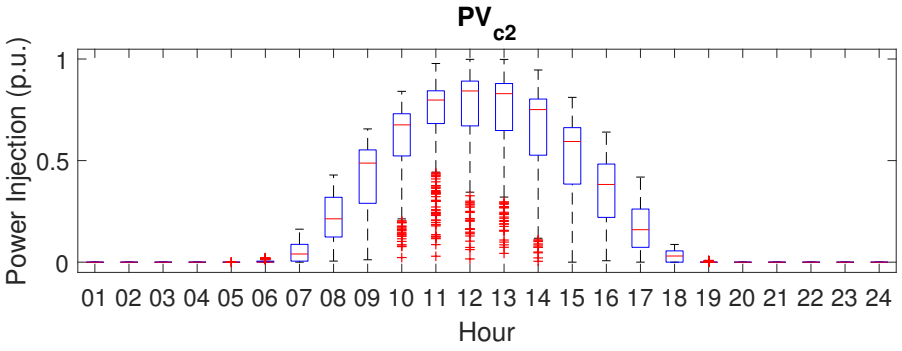


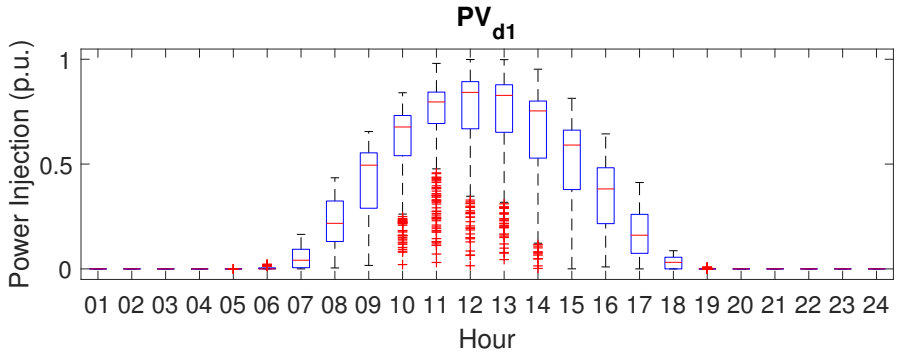


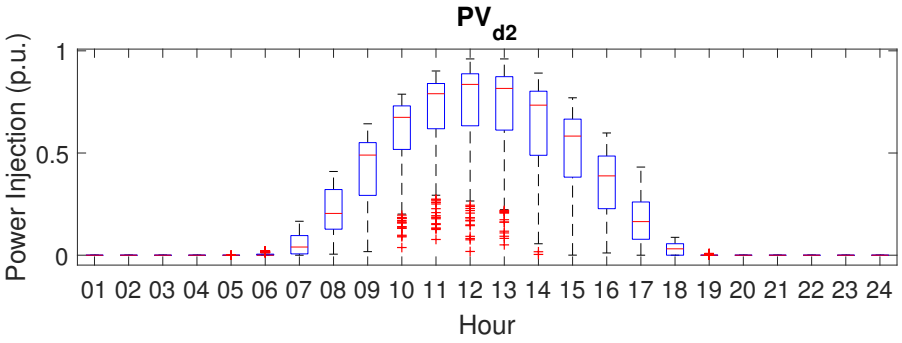


B.3 Utility Feeder CO1

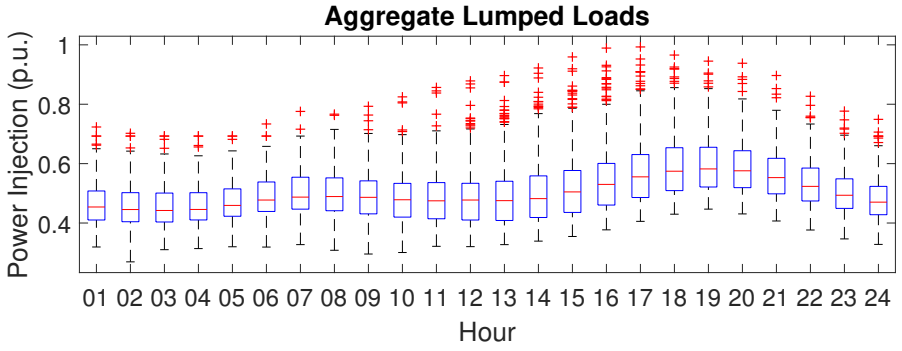


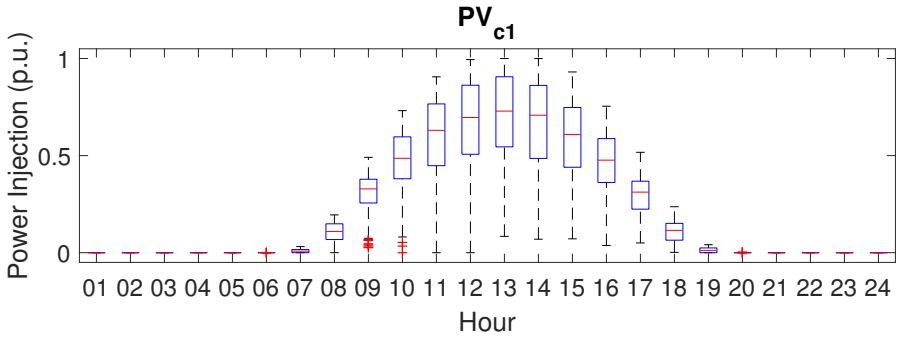


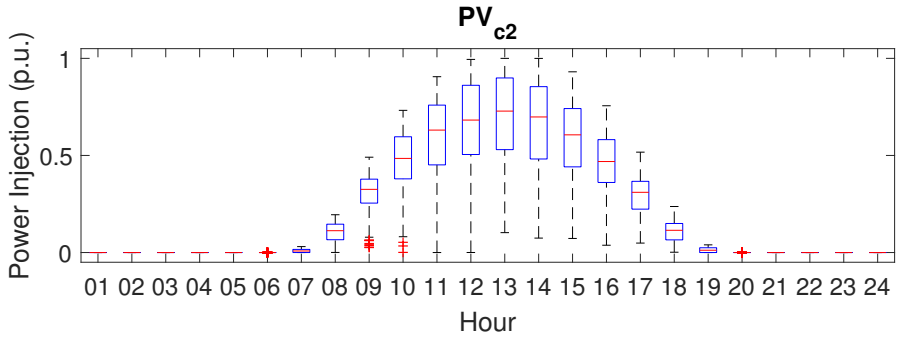




B.4 Utility Feeder J1




PV c1
Power Injection (p.u.)
0
0.5
1
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
Hour


PV c2
Power Injection (p.u.)
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0.5
1
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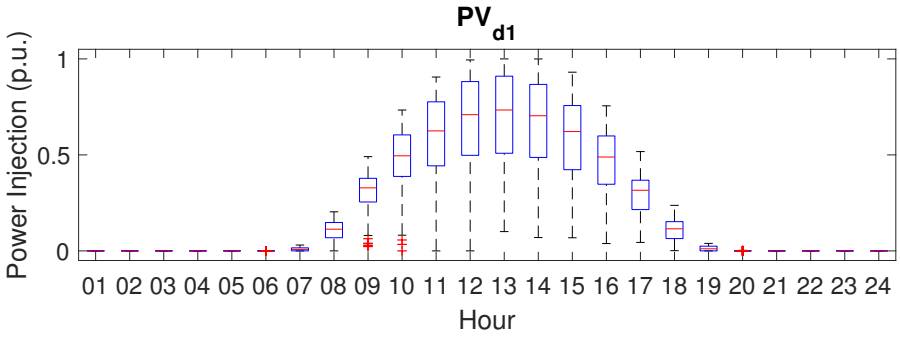
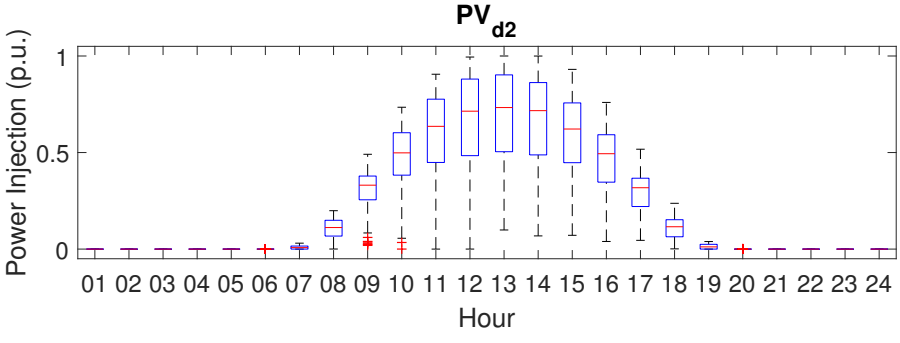
Hour


PV d1
Power Injection (p.u.)
0
0.5
1
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
Hour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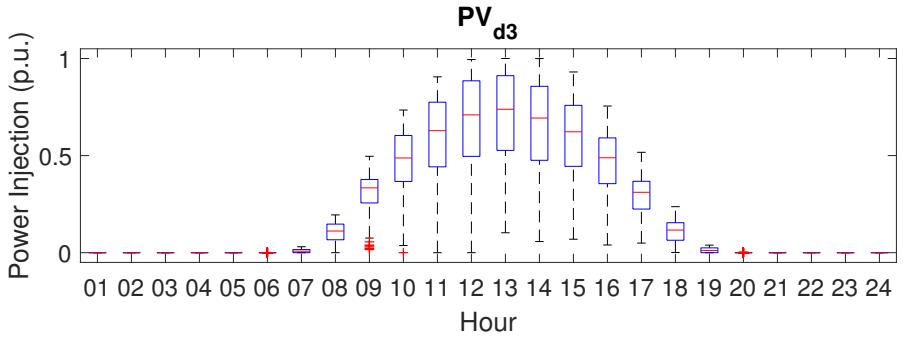
Hour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Power Injection (p.u.)
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0
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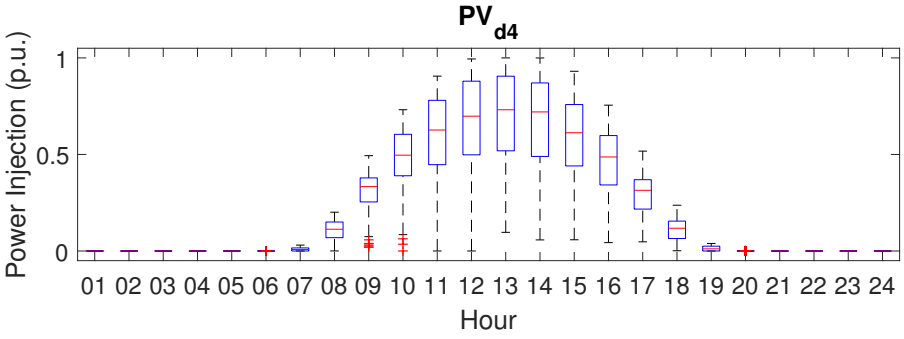
Hour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Power Injection (p.u.)
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0
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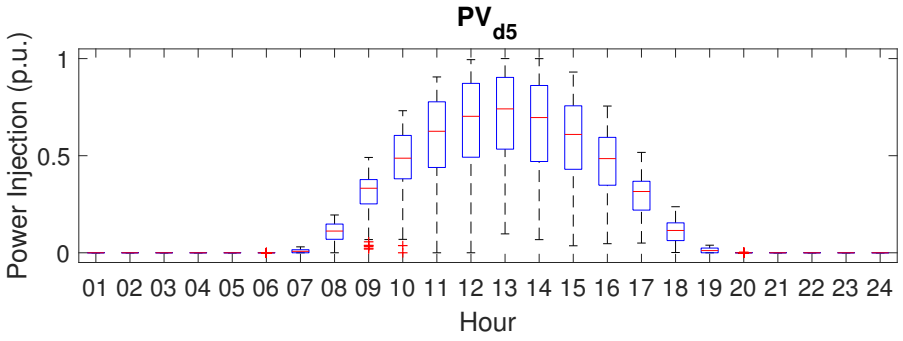
Hour


PV d5
Power Injection (p.u.)
1
0.5
0
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
Hour

APPENDIX C

PUBLICATIONS

The student has the following publications:

1. **M.U. Qureshi** et al., "A Fast Scalable Quasi-Static Time Series Analysis Method for PV Impact Studies using Linear Sensitivity Model", *IEEE Transactions on Sustainable Energy*, 2018.

2. **M.U. Qureshi**, S. Grijalva, "Enhanced Frequency Response based on Multi-Agent Distributed Power Agreement", *IEEE Transactions on Industry Applications*, 2018.

3. **M.U. Qureshi**, S. Grijalva and M.J. Reno, "A Rapid Quasi-Static Time Series Method for Evaluating Current-Related Distributed PV Impacts including Feeder Loading and Line Losses", *IEEE PES General Meeting*, 2019.

4. **M.U. Qureshi**, S. Grijalva and M.J. Reno, "A Fast Quasi-Static Time Series Simulation Method for PV Smart Inverters with VAR Control using Linear Sensitivity Model", *IEEE 45th Photovoltaic Specialist Conference (PVSC)*, 2018. (Nominated for Best Paper Award)

5. **M.U. Qureshi**, S. Grijalva, "Multi-Agent based Distributed Power Agreement for Enhanced Frequency Response of Transmission Systems", *IEEE 19th International Conference on Intelligent Systems Applications to Power (ISAP)*, 2017.

6. **M.U. Qureshi**, A. Girault, M. Mauger, S. Grijalva, "Implementation of Home Energy Management System with Optimal Load Scheduling based on Real-Time Electricity Pricing Models", *IEEE 7th International Conference on Consumer Electronics (ICCE-Berlin)*, 2017.

7. **M.U. Qureshi**, S. Grijalva, "Decentralized Power Agreement for Improved Frequency Response in Interconnected Power Systems", *IEEE 9th Green Technologies Conference (GreenTech)*, 2017.

8. R. Jamshad, **M.U. Qureshi**, S. Grijalva, "Geographic Information Systems (GIS) Image Analysis for Prioritizing Power System Restoration", *IEEE Clemenson University Power Systems Conference (PSC)*, 2018

9. Y. Wardi, M. Egerstedt, and **M.U. Qureshi**, "Hamiltonian-based algorithm for relaxed optimal control", *IEEE 55th Conference on Decision and Control (CDC)*, 2016.

10. M.T. Hale, Y. Wardi, H. Jaleel, M. Egerstedt, and **M.U. Qureshi**, "Hamiltonian-based algorithm for optimal control", (under revision) *Nonlinear Analysis: Hybrid Systems*, 2019.

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