Low-Temperature Electronics

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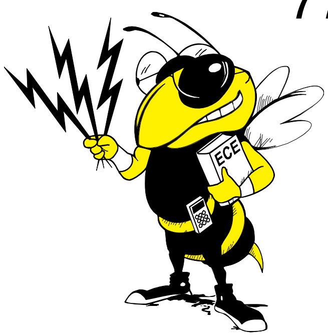

6th International Planetary Probe Workshop – Short Course, 6/21/08

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Outline

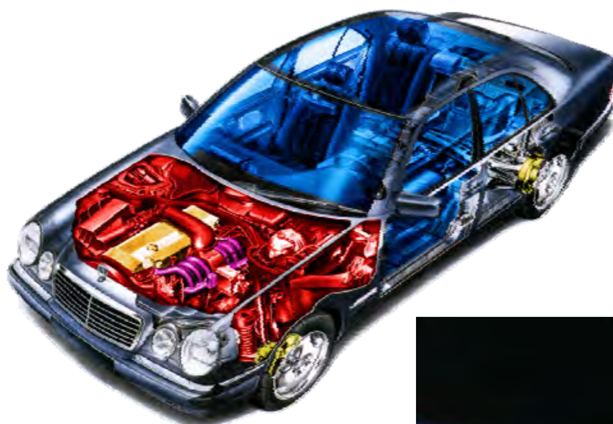
- Extreme Environment Electronics (EEE)
- Using Si CMOS at Low Temperatures
- Using SiGe HBTs at Low Temperatures
- Building the Infrastructure for EEE
- Summary

Extreme Environments

Defn: Operation Outside Commercial or Mil-Spec Conditions
- **temperature** (high-T, low-T, wide-T range)
- **radiation exposure** (TID, SEE)

- **Aerospace** (aircraft, satellites, etc.)
- **Space Exploration** (Moon, Mars, etc.)
- **Automotive** (on-engine electronics, etc.)
- **Drilling** (oil, etc.)

Drilling



Cars

Aerospace

Exploration

Cryogenic Electronics

- **Some Low-Temperature Electronics Applications**
  - deep-space probes and planetary missions (Moon, Europa, …)
  - satellite communications systems + space-based radar
  - ultra-high-speed / high sensitivity instrumentation systems
  - medical electronics (e.g., CT scanner)
  - superconductor-semiconductor hybrids (e.g., 20 Gb/sec ADC)
  - very low-noise receivers (radio astronomy)
  - cooled IR detector arrays

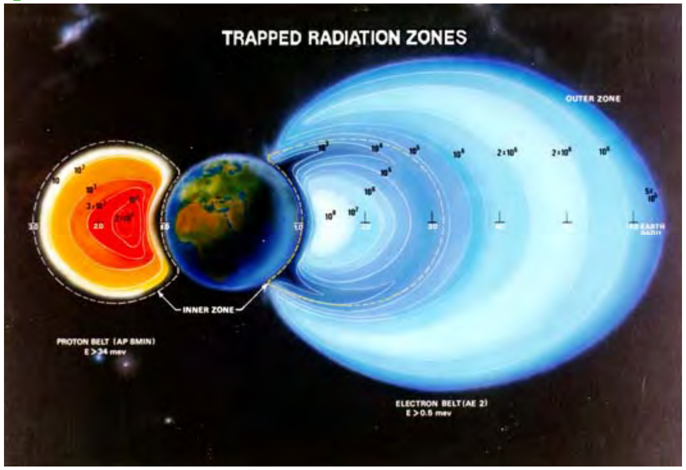
Landers / Rovers

James Webb Space Telescope

Space Radiation Effects

- **The Holy Grail of the Space Community**
  - IC technology space-qualified <u>without</u> additional hardening **(major cost adder)**
  - high integration levels to support SoC / SiP (low cost)

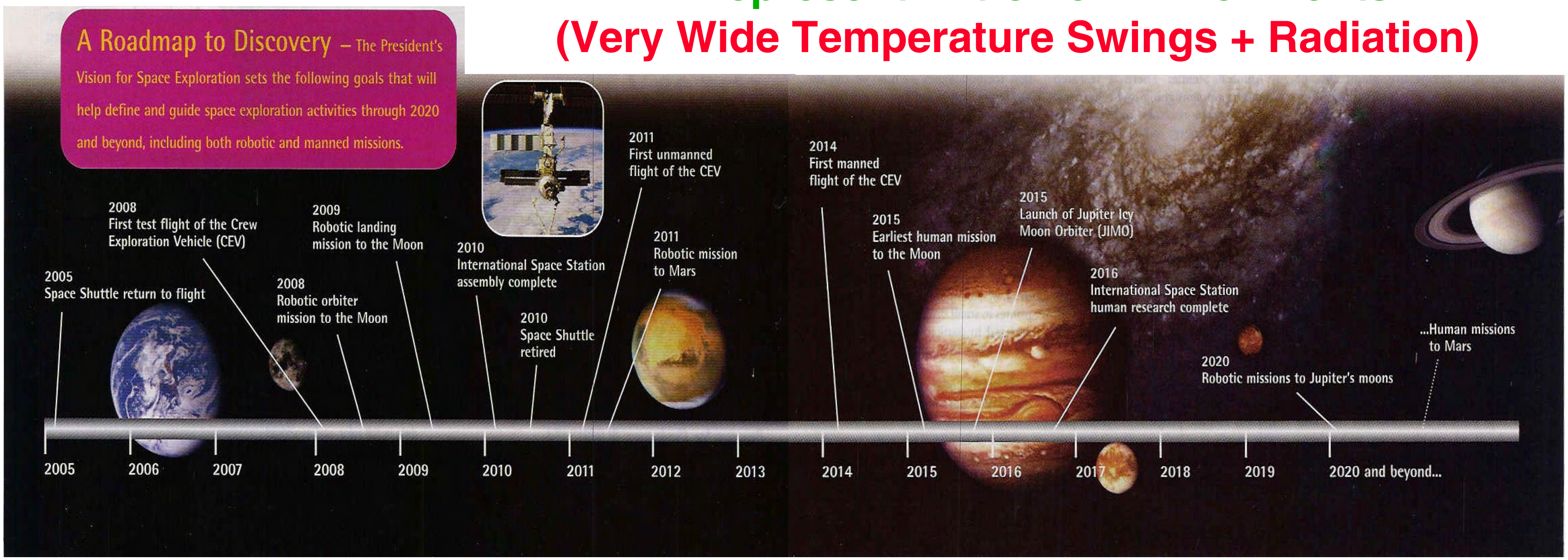
proton + electron belts



- **Total Ionizing Dose (TID) – ionizing radiation**
  - TID is measured in "rads" (1 rad = 100 ergs per gram of energy absorbed)
  - 100-1000 krad(Si) over 10 years for typical orbit *(300 rad(Si) is lethal to humans!)*
- **Single Event Effects (SEE) – high energy heavy ions**
  - SEU: measure data upset cross-section (σ) vs. Linear Energy Transfer (LET)
  - σ = # errors / particle fluence (ions/cm^2): LET = charge deposition (pC/μm)
  - **<u>Goals</u>:** low cross-section + high LET threshold

Space Exploration

All Represent Extreme Environments!
(Very Wide Temperature Swings + Radiation)



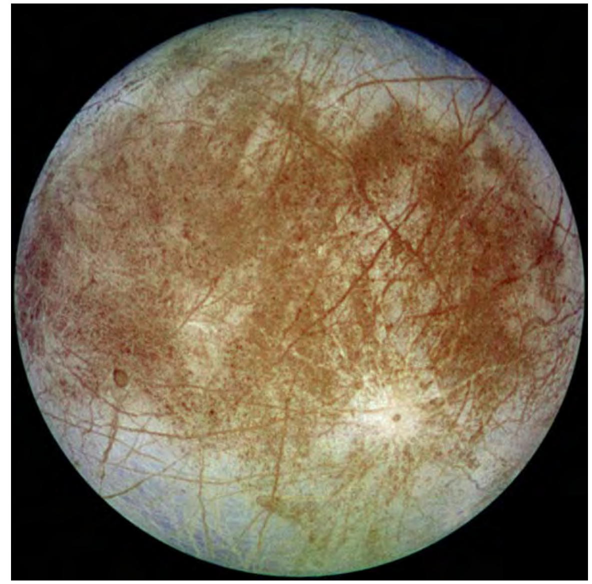
Moon

Mars

Outer Planets

Planet	$T_{surface}$ (K)	T_{sphere} (K)
Mercury	100-700	445
Venus	740	325
Earth	288-293	277
Mars	140-300	225
Jupiter	165	123
Saturn	134	90
Uranus	76	63
Neptune	72	50
~~Pluto~~	~~40~~	~~44~~

Upcoming Missions



The Moon

Temperature:

- +120°C to –180°C (93K)
- 28 day cycles
- -230°C in shadowed polar craters

Radiation:

- 100 krad total dose (modest)
- single event effects (solar storms)

Europa

Temperature:

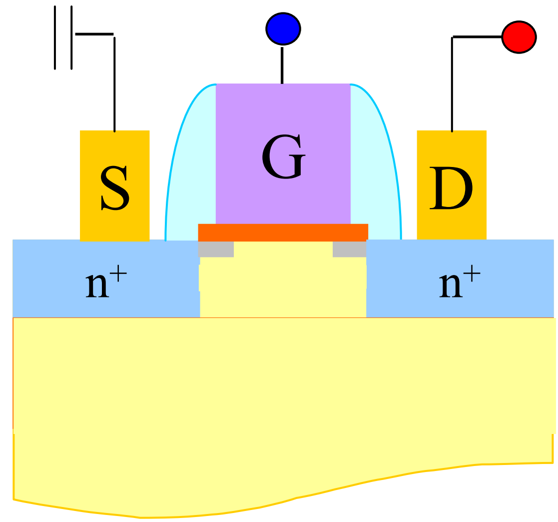
- -220°C at the poles
- -160°C at the equator

Radiation:

- 5 Mrad / 2 wks (extreme)
- single event effects

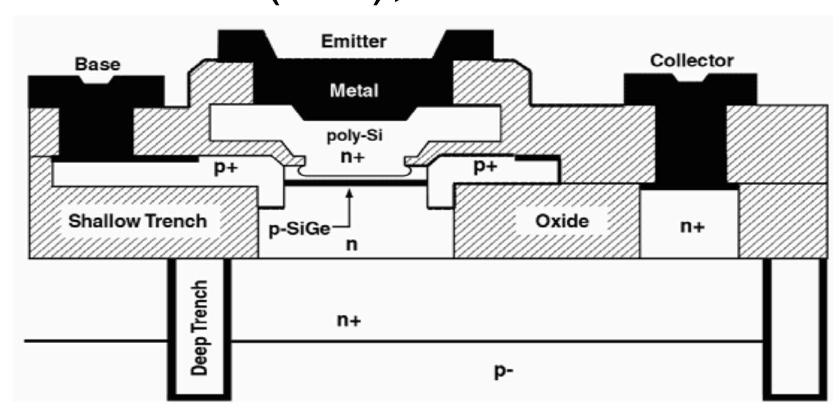
Technology Options

Commercial Technology Options for EEE:



- **Si CMOS** (bulk and SOI)
  - **cooling improves**: $I_{DS,sat}$, g_m, μ_{eff}, S, I_{off}
  - **cooling degrades**: V_T, hot carrier reliability
  - **radiation tolerance**: problem without RHBD

- **SiGe HBT** (bulk and SOI)
  - **cooling improves**: β, V_A, g_m, f_T, f_{max}, NF_{min}
  - **cooling degrades**: β at low currents
  - **radiation tolerance**: built-in to multi-Mrad (TID), RHBD for SEE



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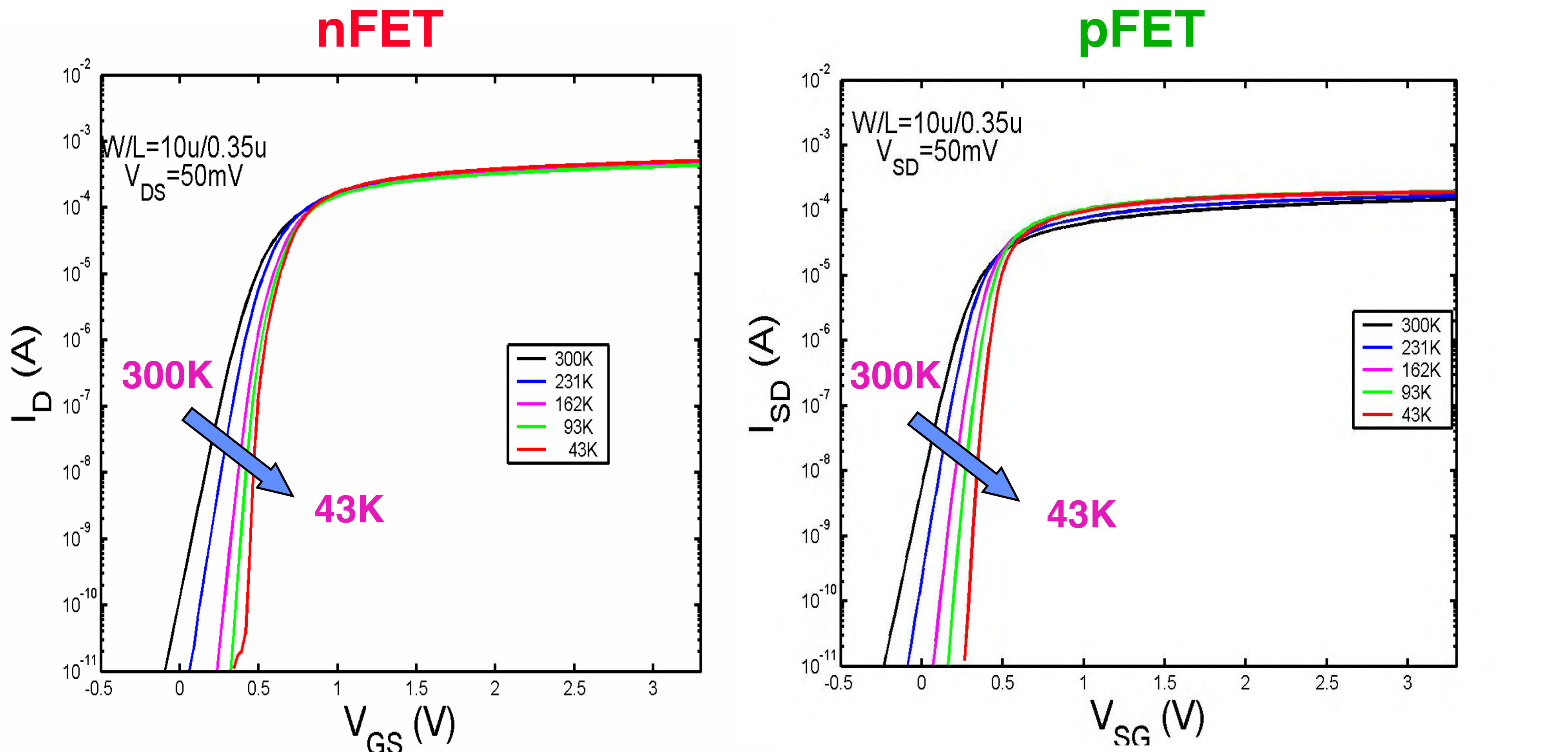
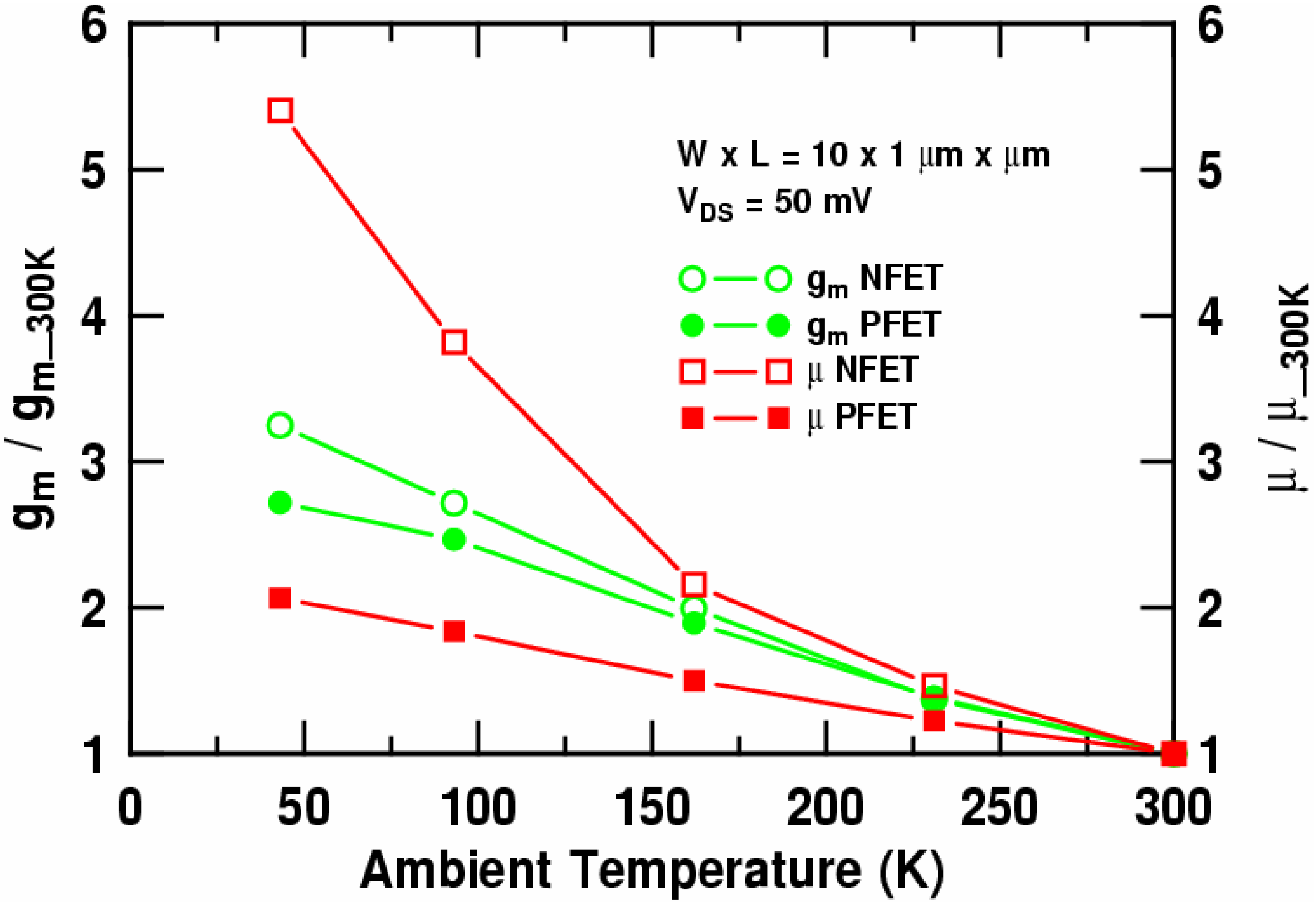
Cooling Bulk Si CMOS

- **Devices Function Well Down to 43 K** (and below)



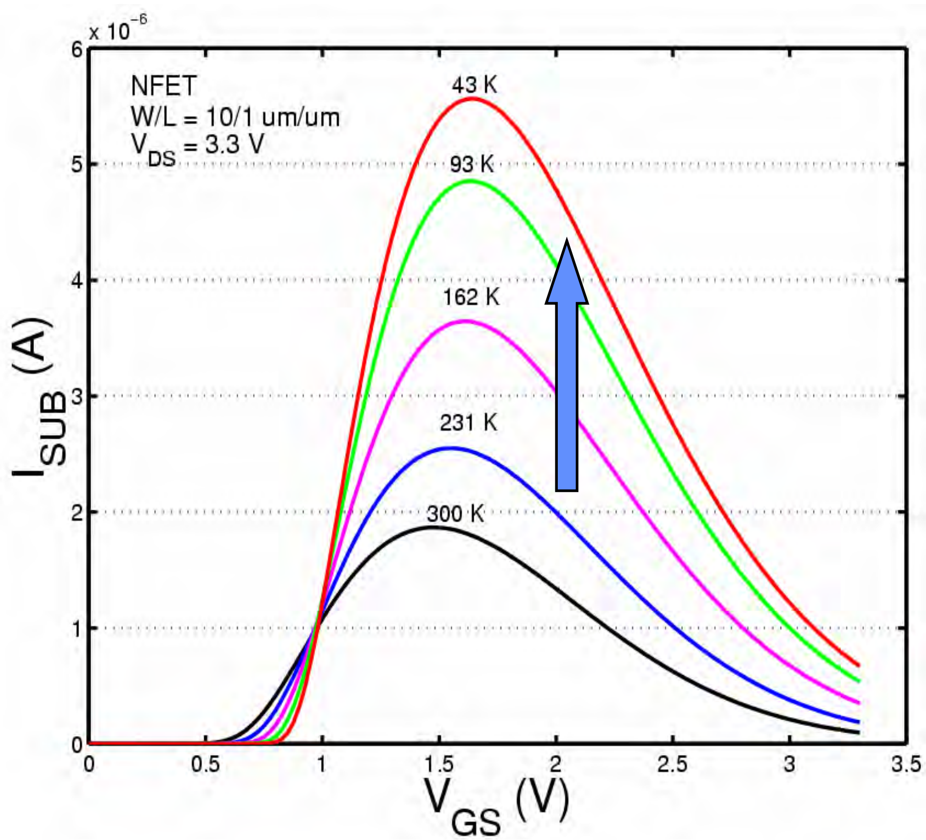
g_m / Mobility

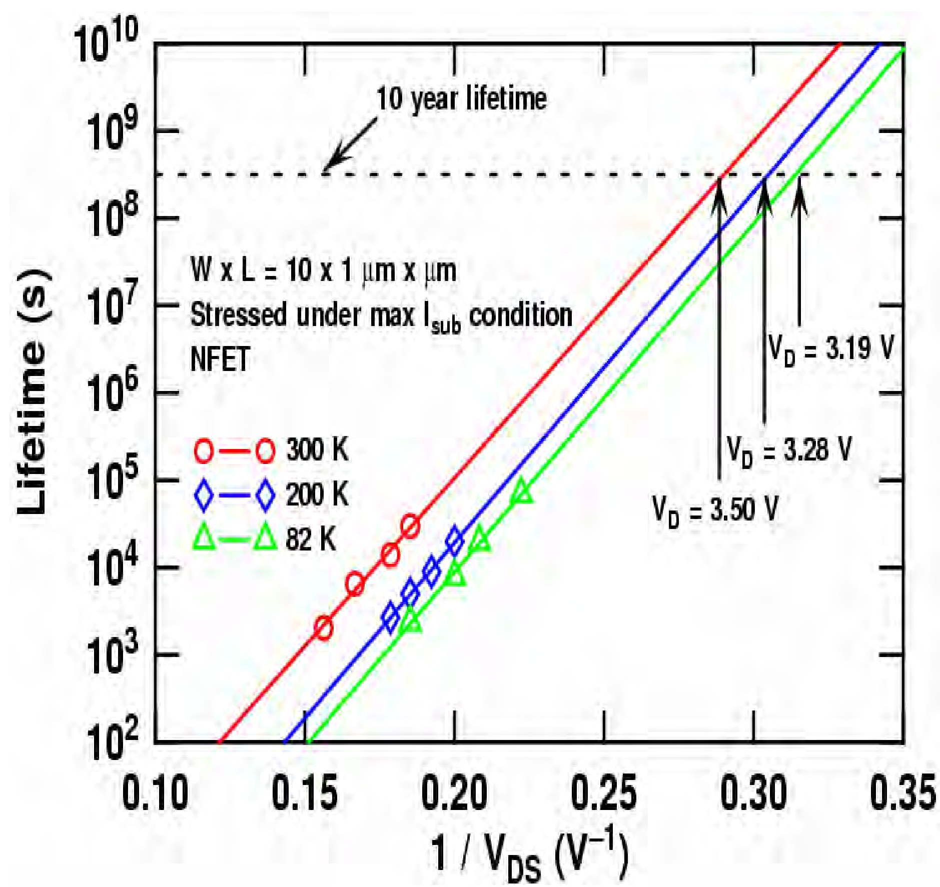
- **μ Increases as T Decreases** (reduction in scattering)
- **g_m Increases as T Decreases** (driven by mobility)



Reliability (Fixed L)

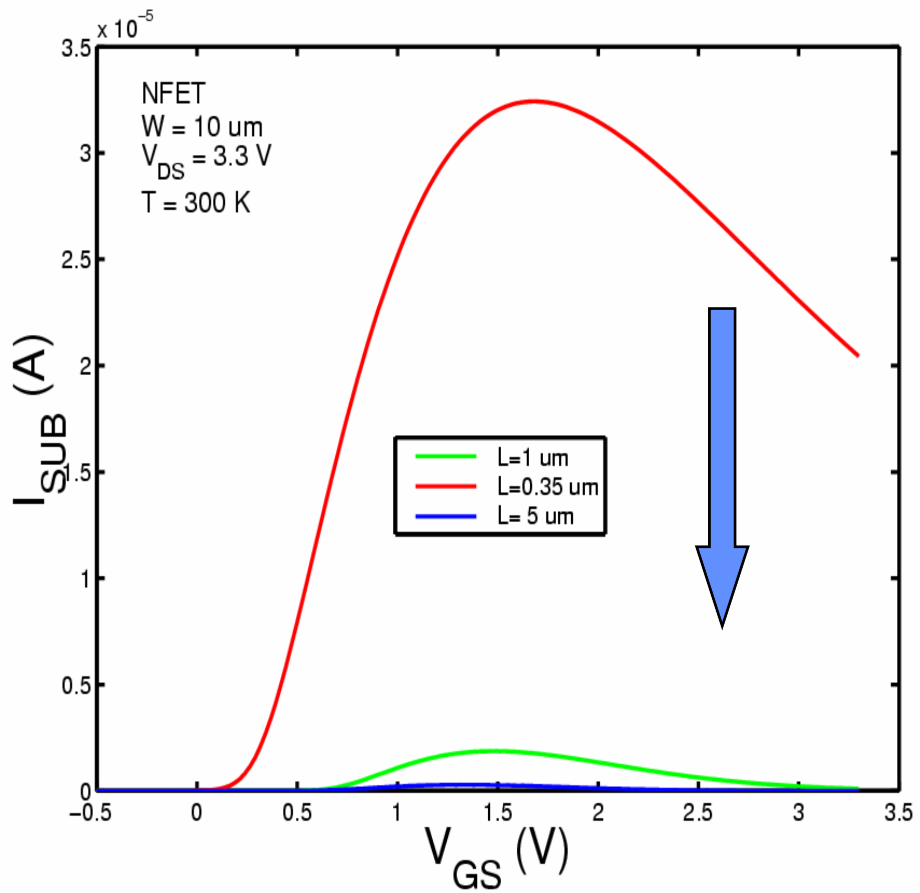
- **Max I_{SUB} Increases as T Decreases** (more impact ionization)
- **Lifetime Degrades as T Decreases** (more hot carrier damage)

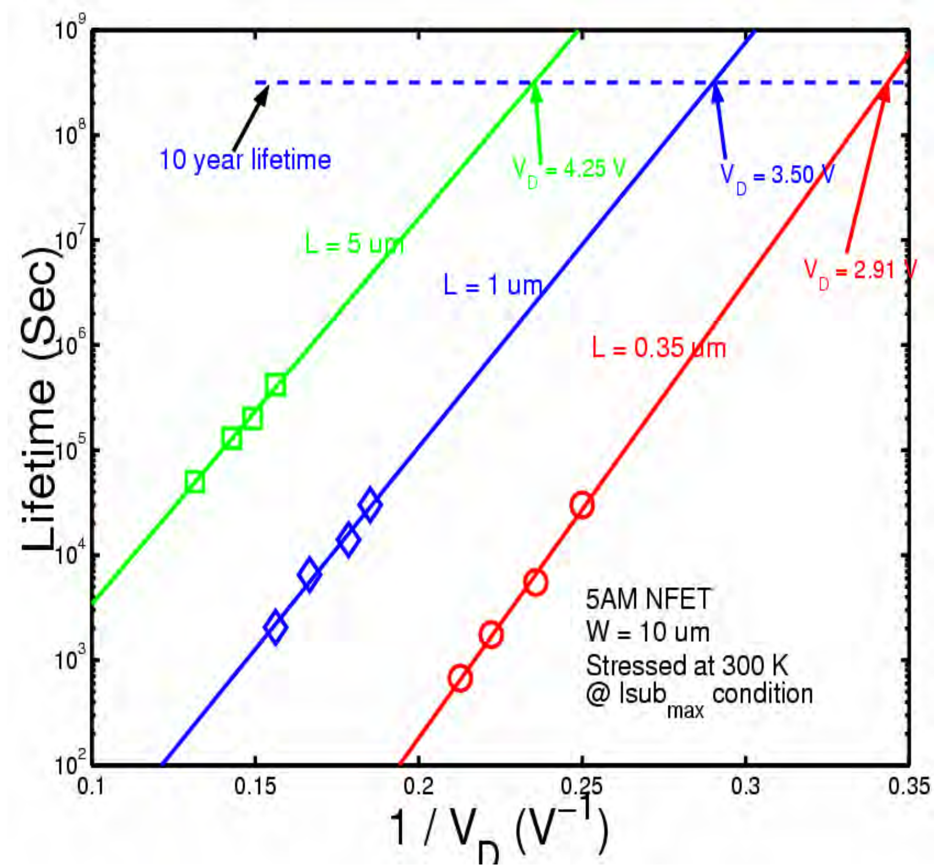




Reliability (Variable L)

- **Max I_{SUB} Increases as L Decreases** (decreased drain field)
- **Lifetime Degrades with Gate Length Scaling**

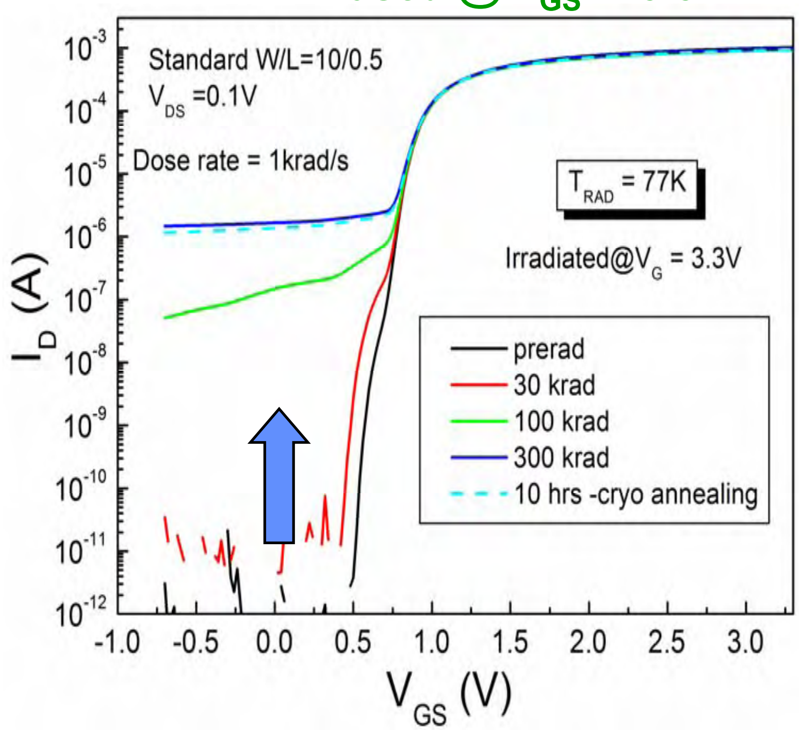




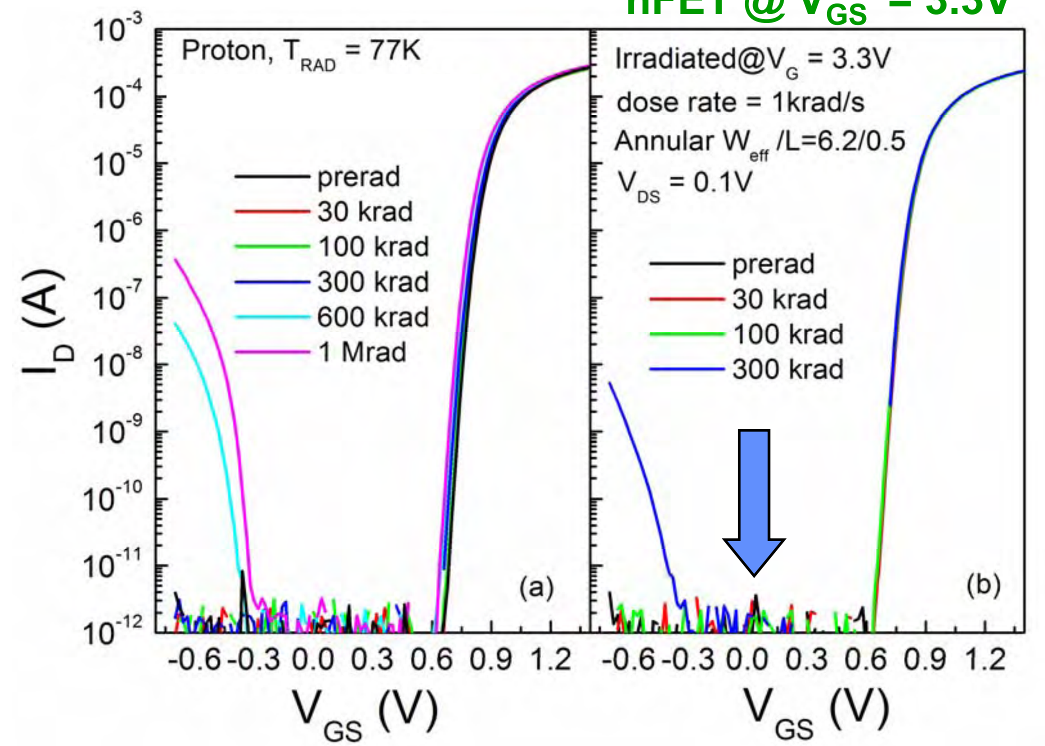
nFET 77K Irradiation

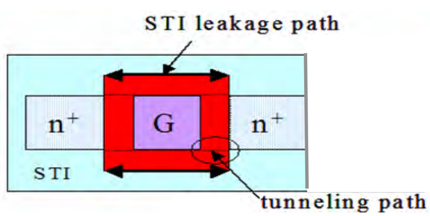
- STI Damage Causes Serious Off-State Leakage Issues
- Leakage Can Be Mitigated Using RHBD Techniques

nFET Biased @ V_{GS} = 3.3V

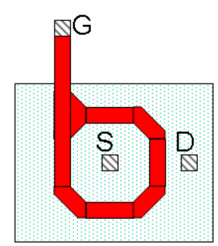


nFET @ V_{GS} = 3.3V



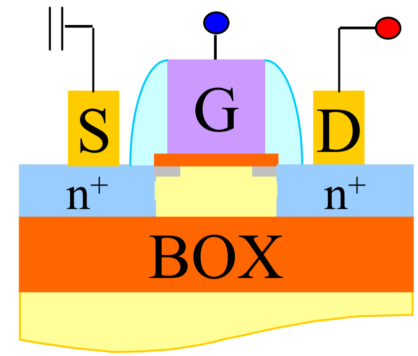


63 MeV protons

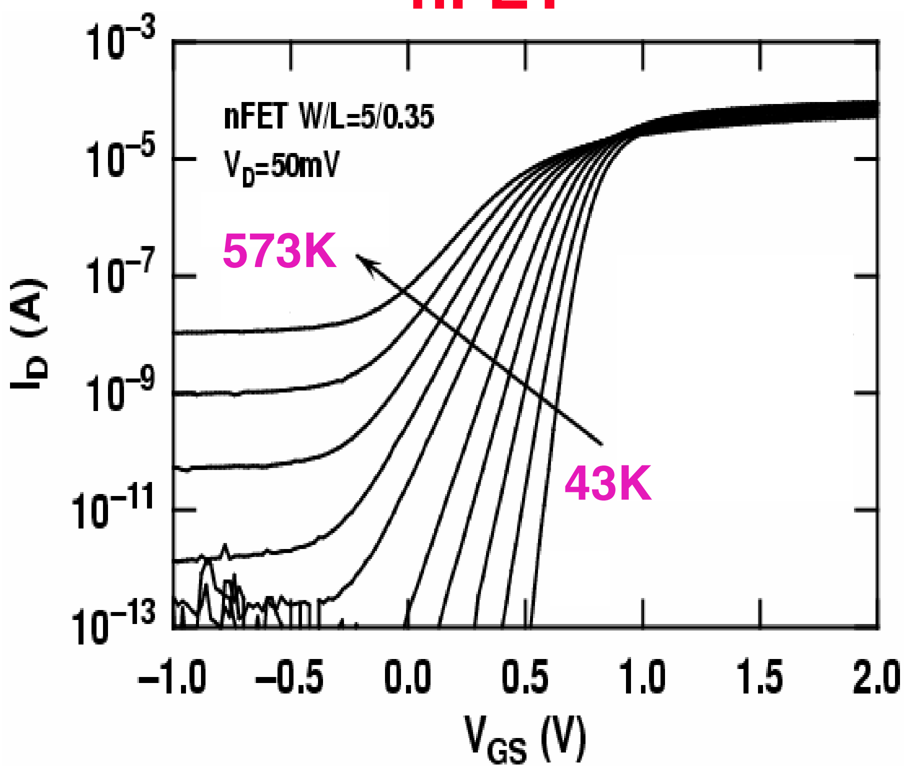


SOI CMOS

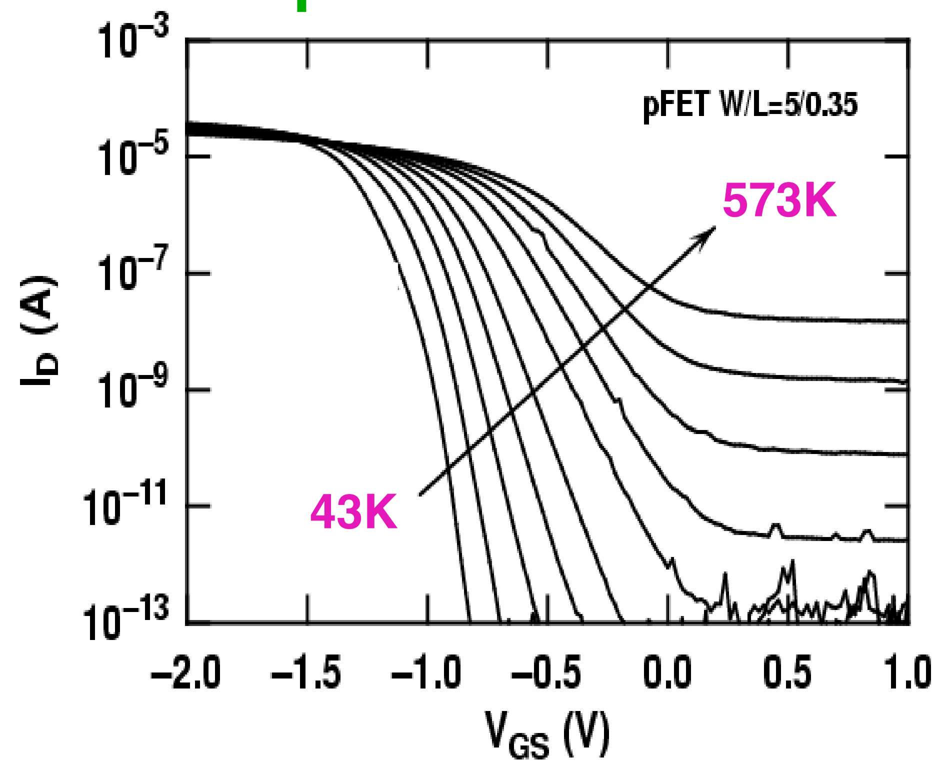
- **Similar Behavior at Cryo-T to Bulk CMOS**
- **Improved Radiation Response** (SEE)
- **Improved Operation at High-T** (leakage)



nFET



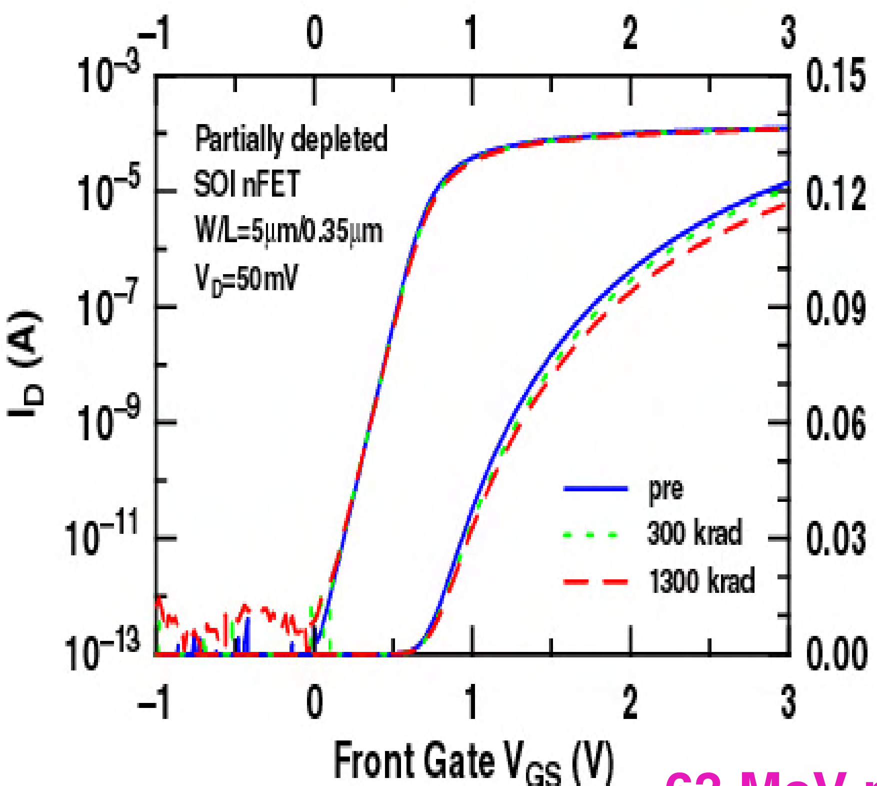
pFET



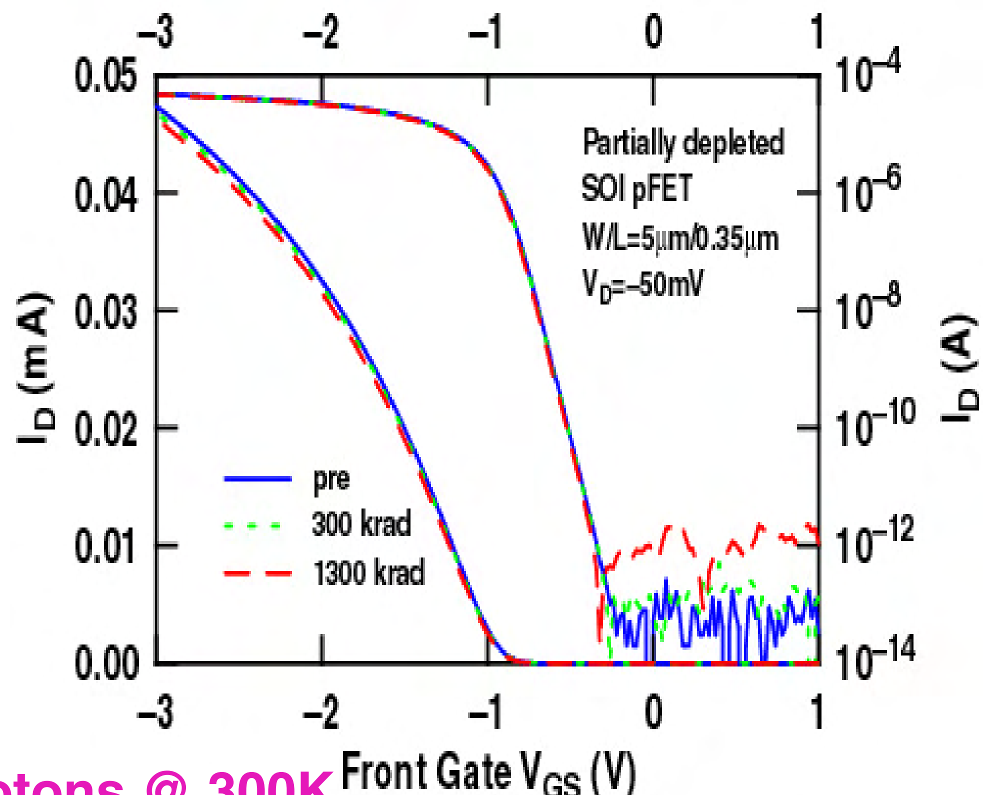
SOI Radiation Response

- **No Off-State Leakage (**edgeless H-gate device layout)
- **Some I_D Degradation in Strong Inversion**
  - mobility ↓, R_{SD} ↑, V_{th} ↑ with increasing total dose

nFET



pFET



63 MeV protons @ 300K

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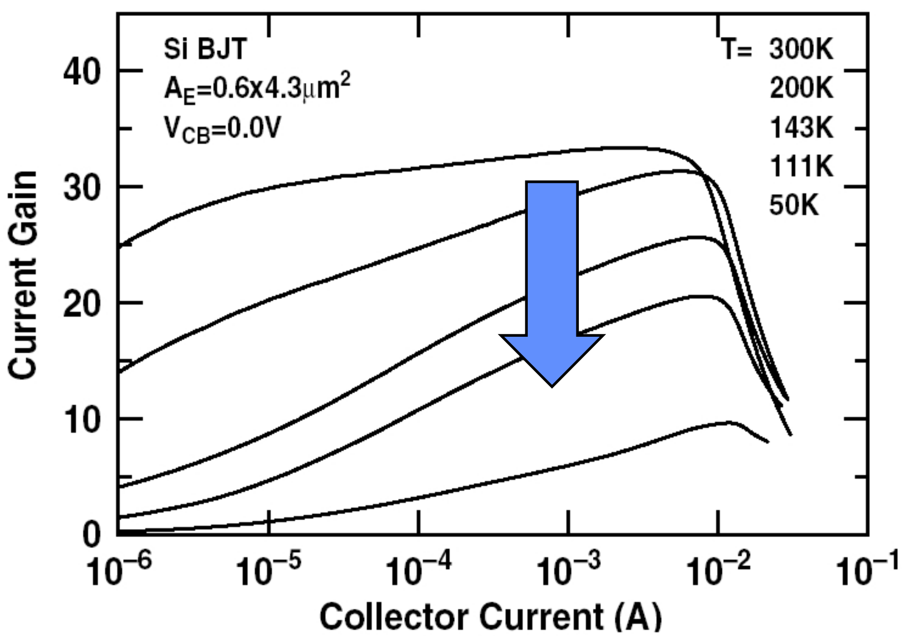
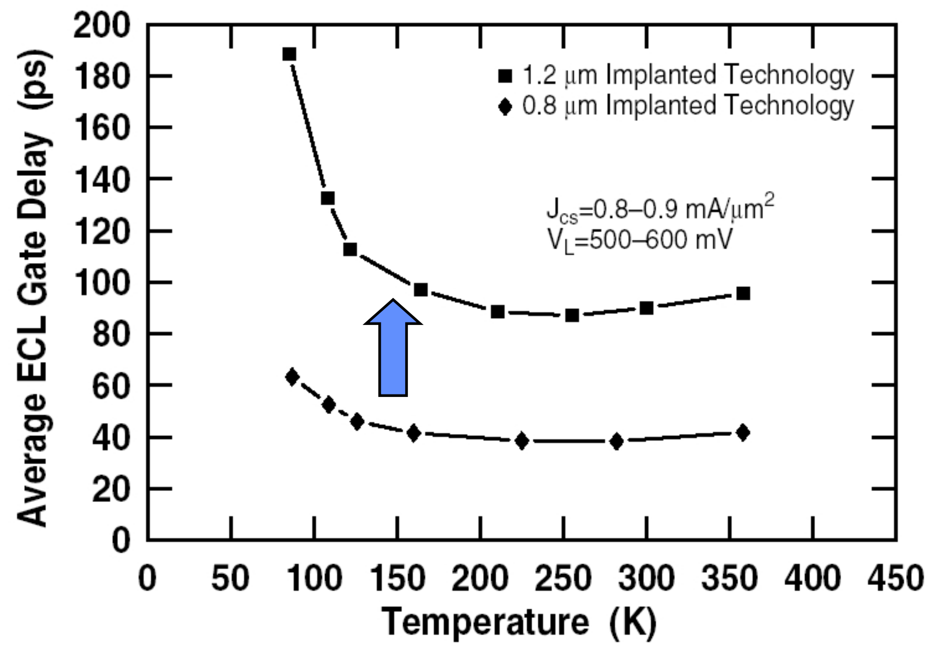
Si BJTs at Cryo-T

- **Degradation in Current Gain with Cooling (bad news)**
  - driven by emitter-to-base bandgap narrowing differences
- **Degradation in Speed with Cooling (bad news)**
  - driven by diffusivity decrease in base transit time and base freeze-out



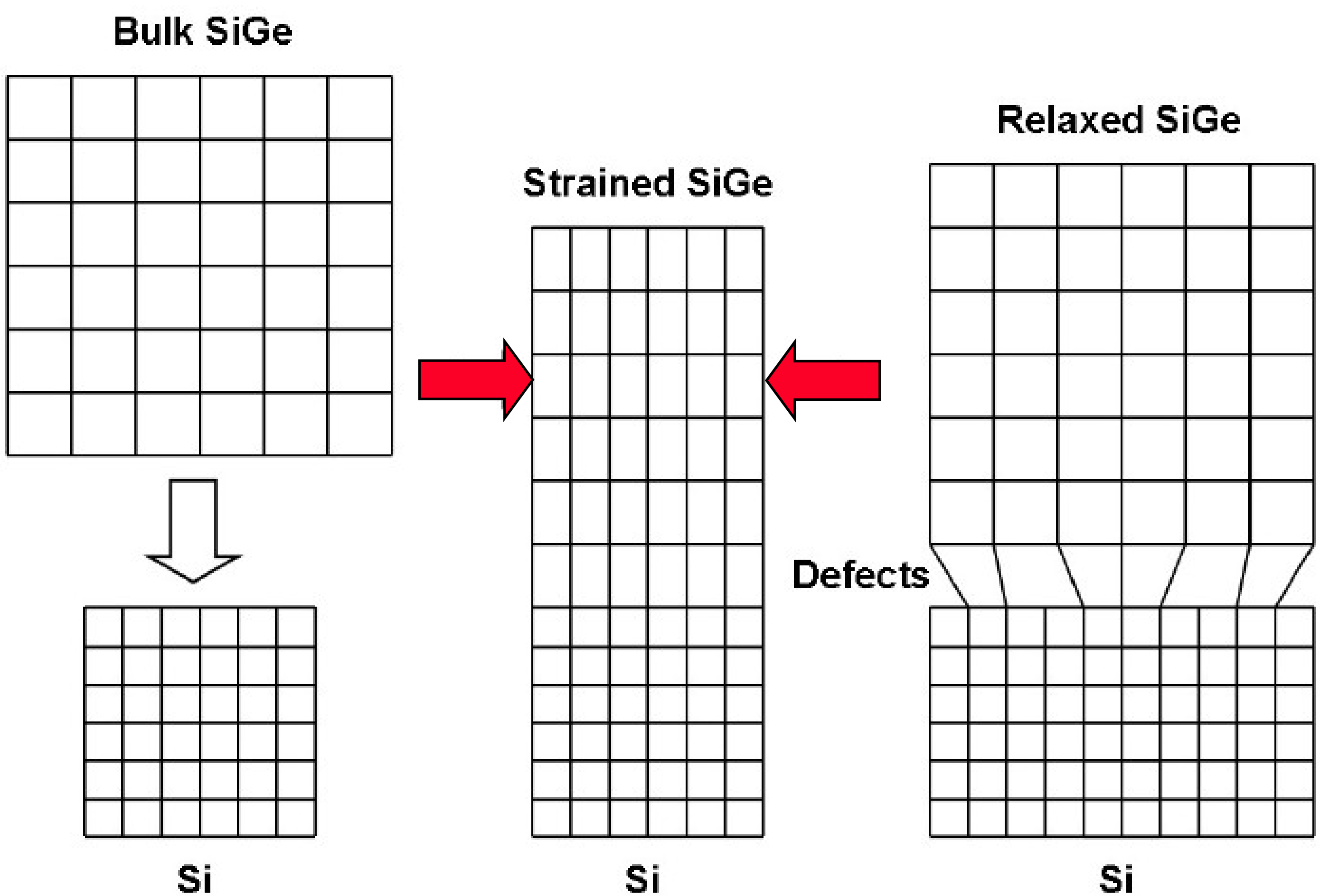


$$\beta_{ideal}(T) = \frac{q D_{nb}(T)\, L_{pe}(T)\, N_{de}^{+}(T)}{D_{pe}(T)\, W_b(T)\, N_{ab}^{-}(T)}\, e^{(\Delta E_{gb}^{app} - \Delta E_{ge}^{app})/kT}$$

$$\tau_{b,Si}(T) = \frac{W_b^2(T)}{2 D_{nb}(T)} = \frac{q W_b^2(T)}{2\, kT\, \mu_{nb}(T)}$$

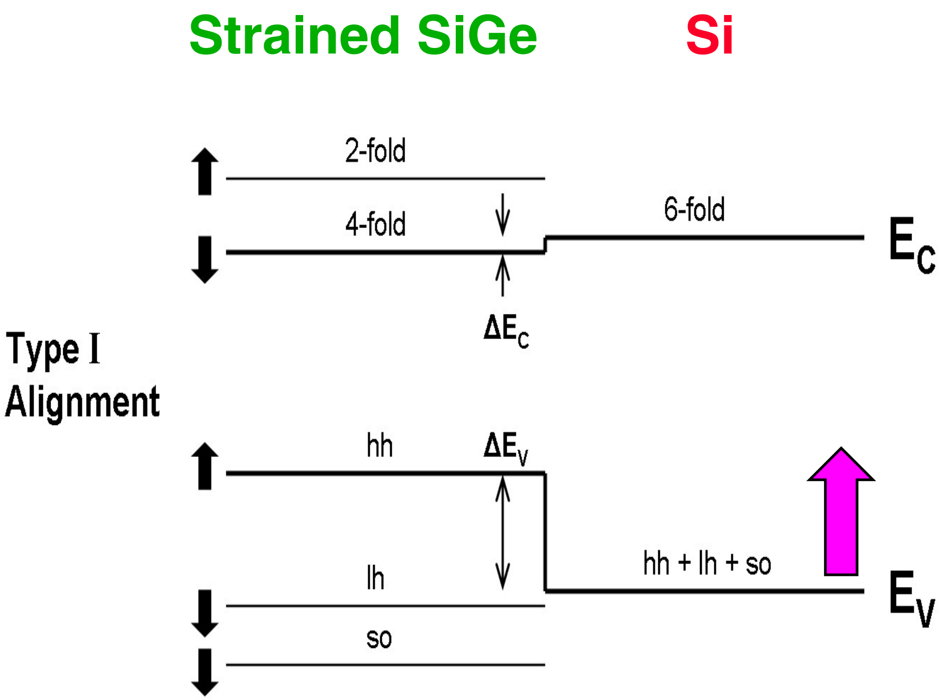
Putting SiGe on Si

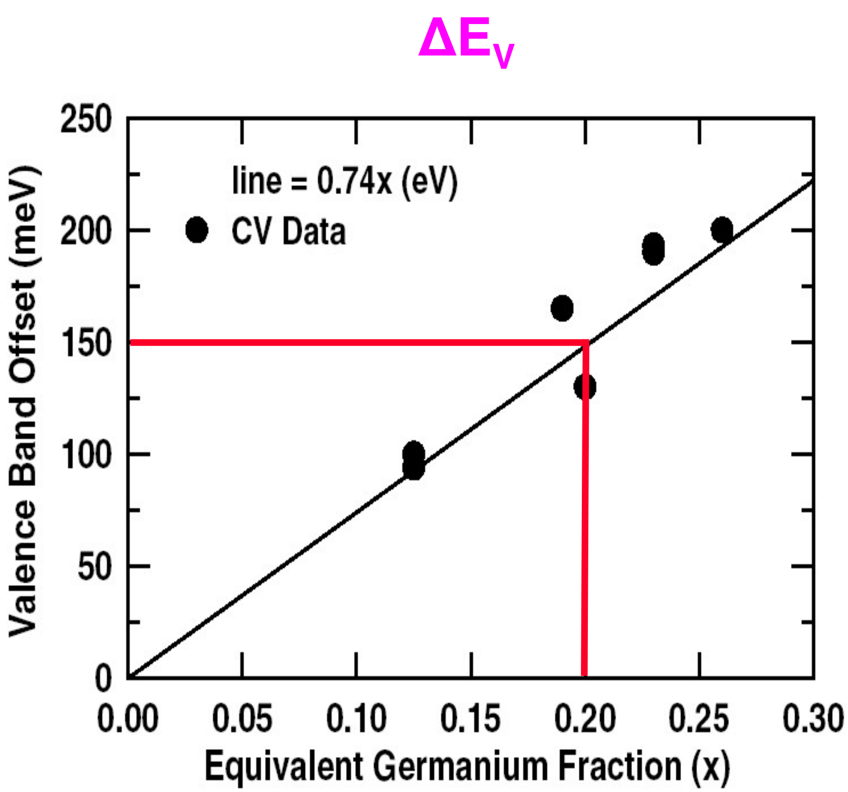
- **SiGe on Si ➡ Compressive Strain in the SiGe Layer**



Electrical Consequences

- **Type-I Band Alignment** (Valence Band Offset = 74 meV / 10% Ge)
- **Hole Mobility Enhancement** (good news)





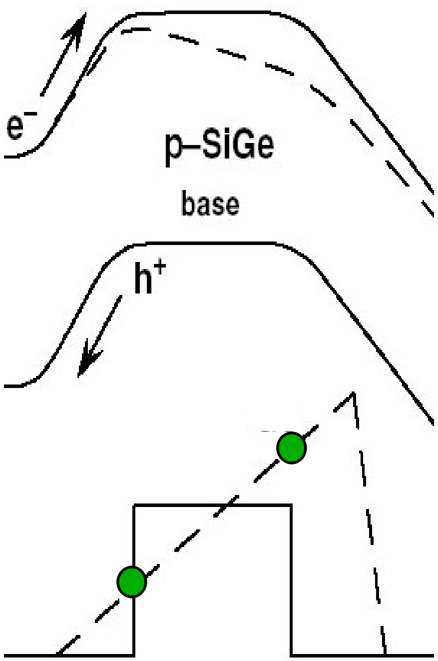
150 meV grading across 100 nm = 15 kV/cm electric field!

The SiGe HBT

The Idea: **Put Graded Ge Layer into the Base of a Si BJT**

Primary Consequences:

- smaller base bandgap increases electron injection (β⬆)
- field from graded base bandgap decreases base transit time (f_T⬆)
- base bandgap grading produces higher Early voltage (V_A⬆)
- decouples device performance metrics from base doping profile



$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{V_{BE}} \equiv \Xi = \left\{ \frac{\tilde{\gamma}\,\tilde{\eta}\,\Delta E_{g,Ge}(grade)/kT \; e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\}$$

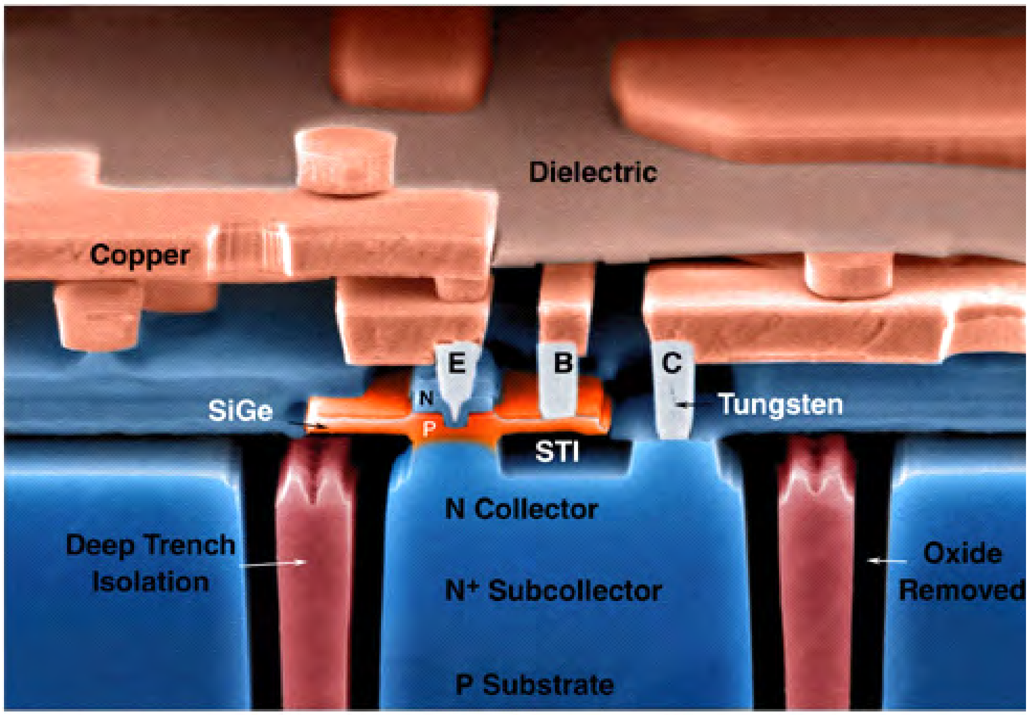
$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \left[1 - e^{-\Delta E_{g,Ge}(grade)/kT} \right] \right\}$$

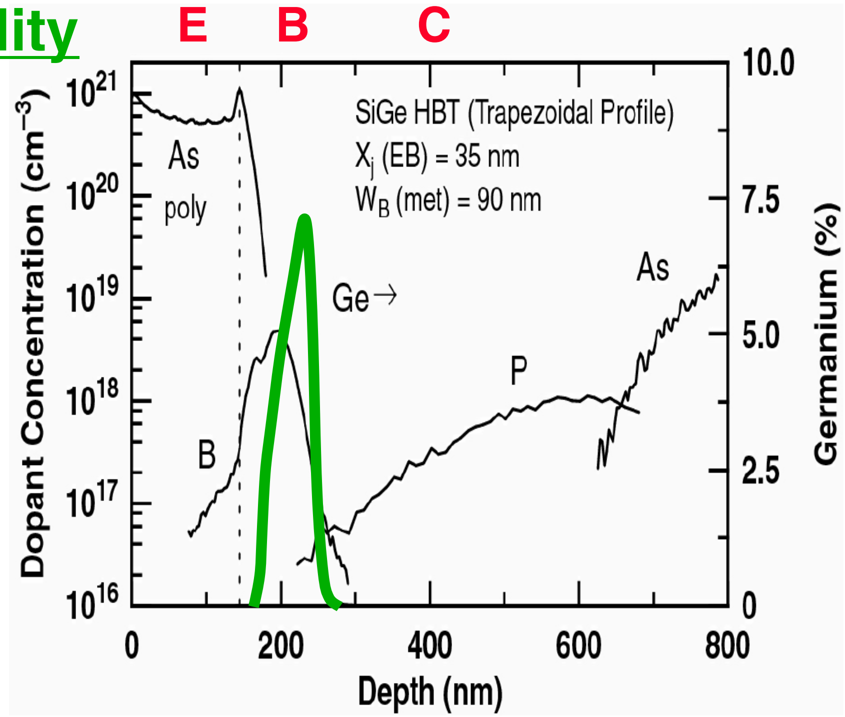
$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{V_{BE}} \equiv \Theta \simeq e^{\Delta E_{g,Ge}(grade)/kT} \left[\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right]$$

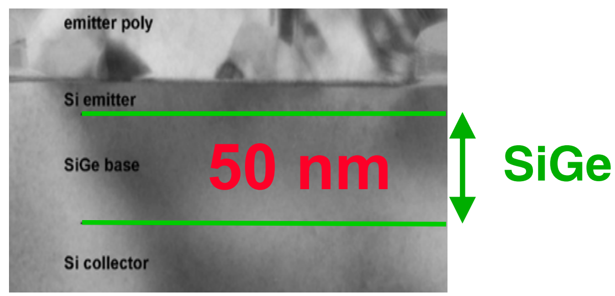
SiGe is a Natural Fit for Analog / RF Apps

The SiGe HBT

- Conventional Shallow and Deep Trench Isolation + CMOS BEOL
- Unconditionally Stable, UHV/CVD SiGe Epitaxial Base
- 100% Si Manufacturing Compatibility
- SiGe HBT + Si CMOS on wafer





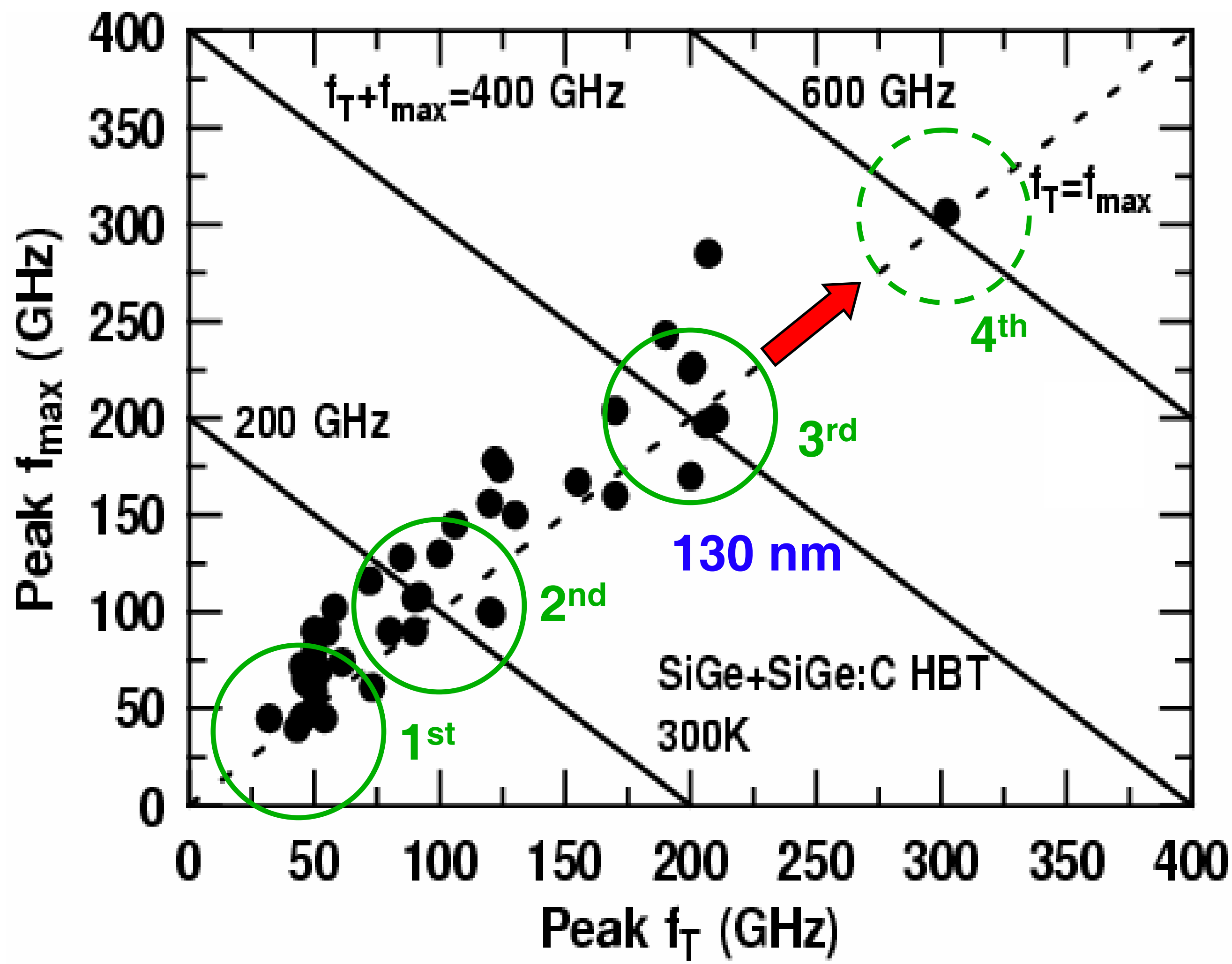


SiGe = III-V Speed + Si Manufacturing

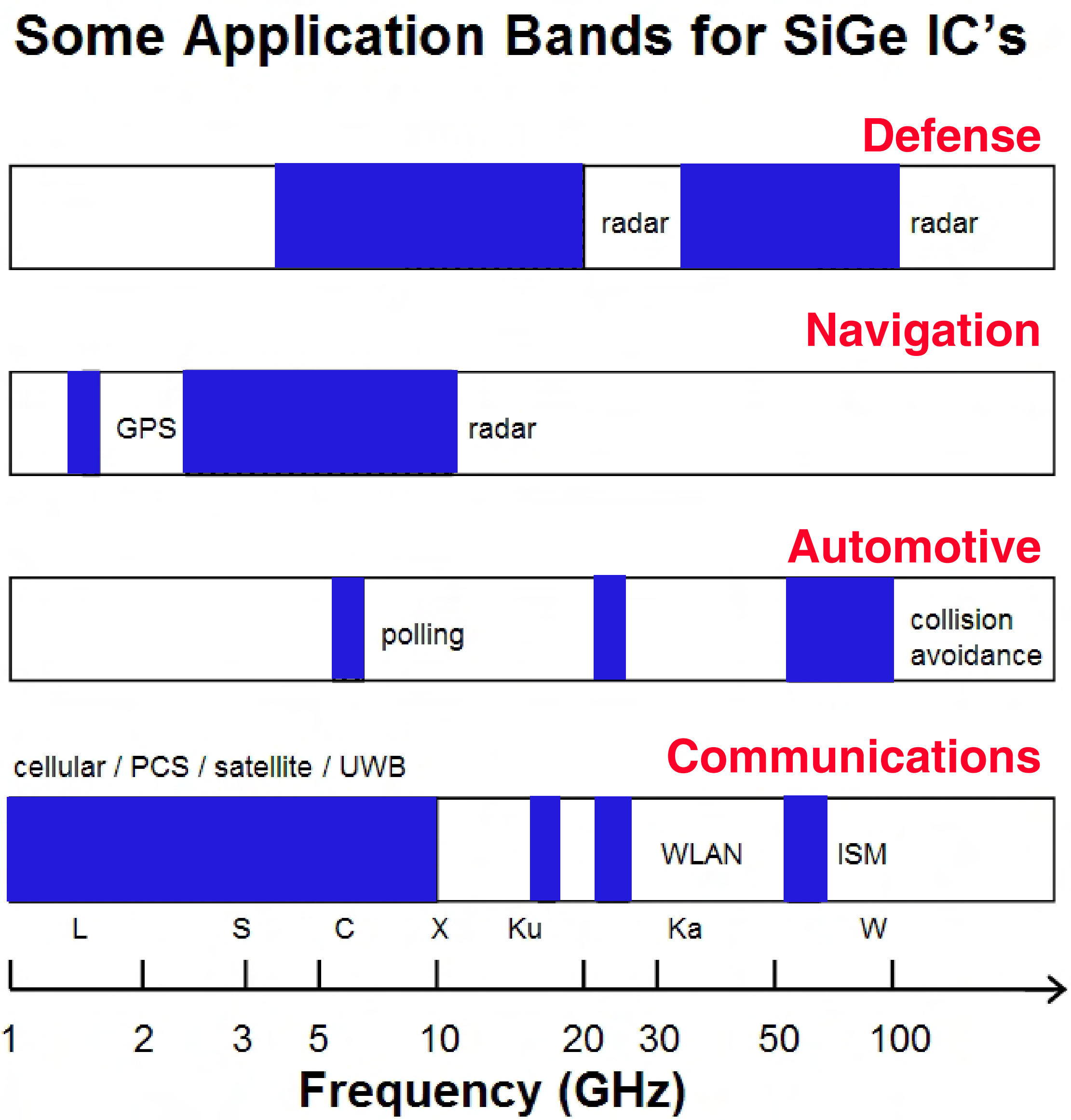
Win-Win!

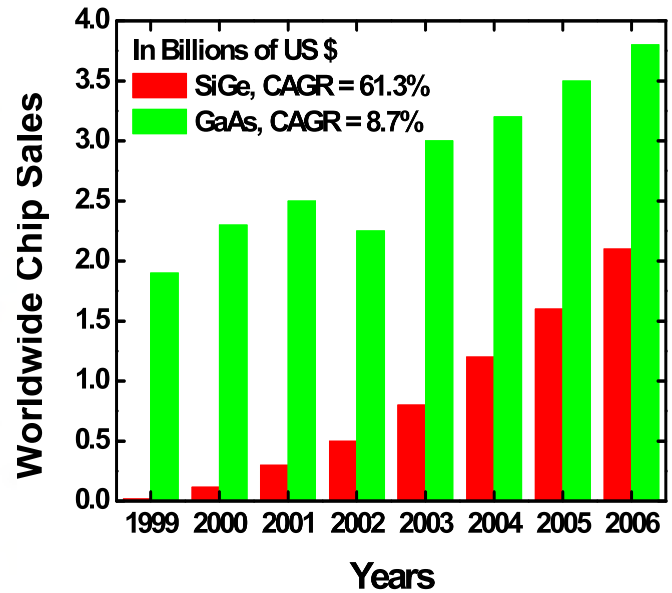
Performance Trends

- **SiGe HBTs Out-Perform RF-CMOS by 2 Generations**



SiGe Applications





SiGe Analog/RF ICs Are a Major Driver!

SiGe Performance Limits

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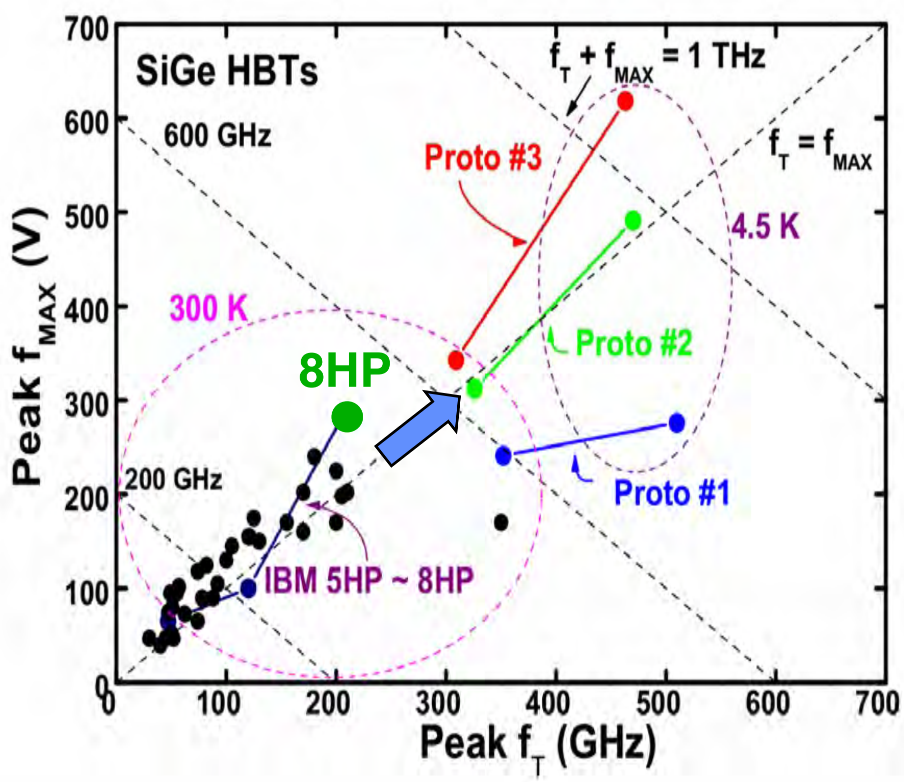
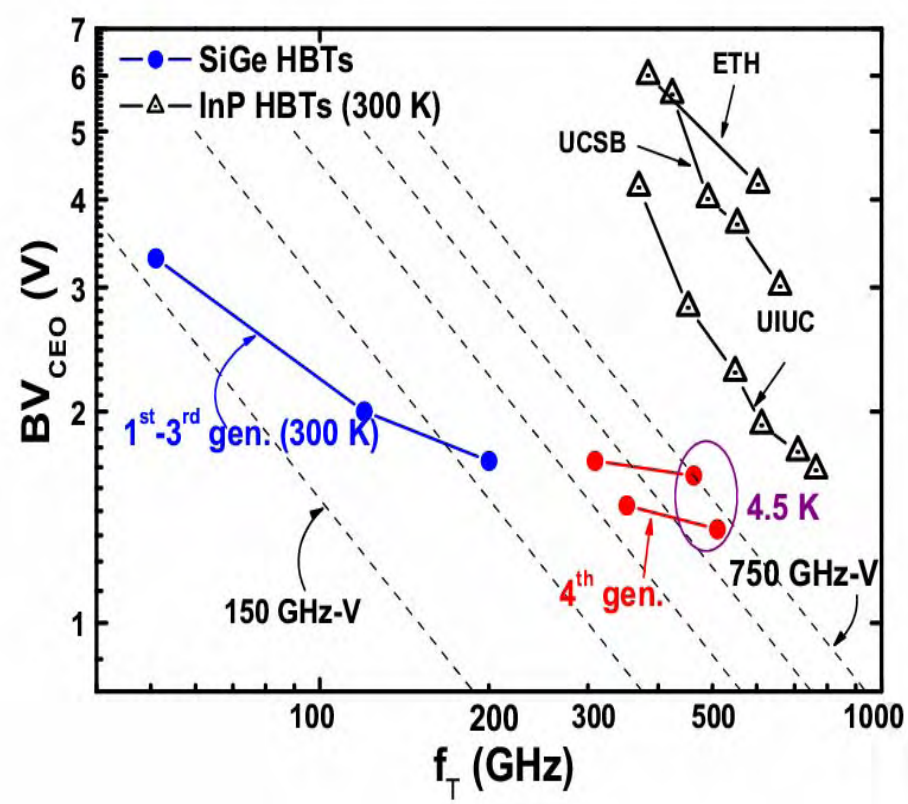
- Half-TeraHertz SiGe HBTs Are Clearly Possible (at modest lith)
- Both f_T and f_{max} above 500 GHz at Cryo-T (T = scaling knob)
- Goal: Useful BV @ 500 GHz (BV_{CEO} > 1.5 V + BV_{CBO} > 5.5 V)





200-500 GHz @ 130 nm Node!

New Opportunities

- **SiGe for Radar Systems**
  - **DoD phased arrays** (2-10 GHz and up) **+ automotive** (24, 77 GHz)
- **SiGe for Millimeter-wave Communications / THz Imaging**
  - **Gb/s wireless** (60, 94 GHz) **/ imaging systems** (100-300 GHz)
- **SiGe for Analog Applications**
  - **data conversion** (ADC limits) **+ the emerging role of C-SiGe** (npn + pnp)
- **SiGe for Extreme Environment Electronics**
  - **extreme temperatures** (4K to 300C)
  - **radiation** (e.g., space systems)
  - **explore performance limits of SiGe** (goal: 1 THz aggregate $f_T + f_{max}$)
- **SiGe for Enhanced Dynamic Range Systems**
  - **improved understanding of linearity / extreme wideband transceivers**

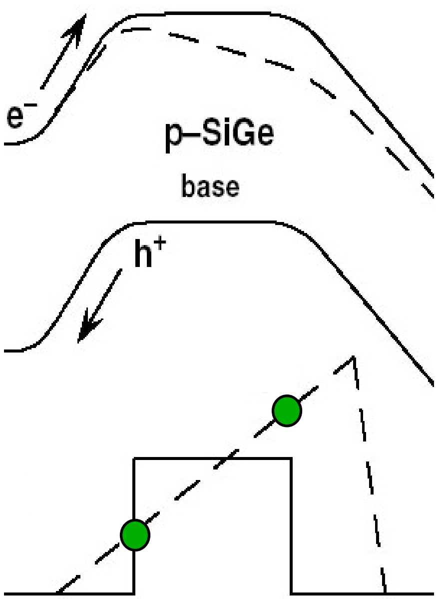
SiGe HBTs for Cryo-T

Georgia Institute of Technology

The Idea: **Put Graded Ge Layer into the Base of a Si BJT**

Primary Consequences:

- **smaller base bandgap increases electron injection** ($\beta\uparrow$)
- **field from graded base bandgap decreases base transit time** ($f_T\uparrow$)
- **base bandgap grading produces higher Early voltage** ($V_A\uparrow$)



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→ **All kT Factors Are Arranged to Help at Cryo-T!**

SiGe HBTs at Cryo-T

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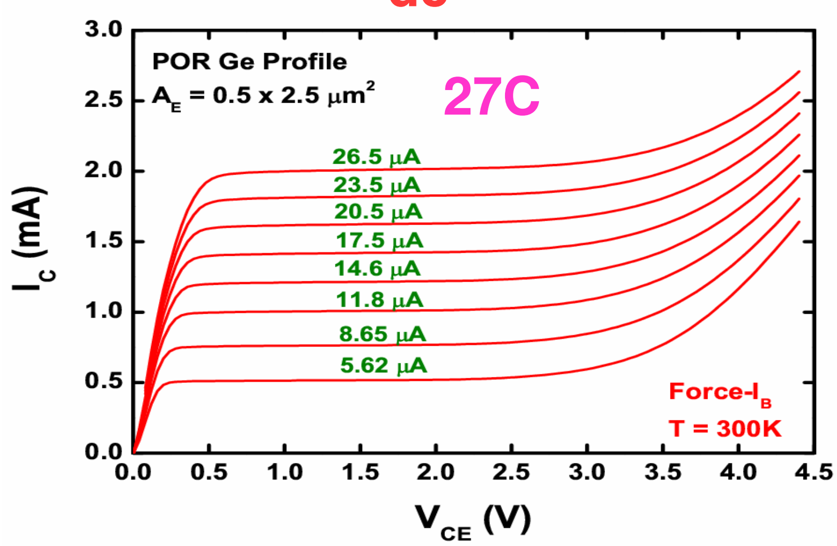

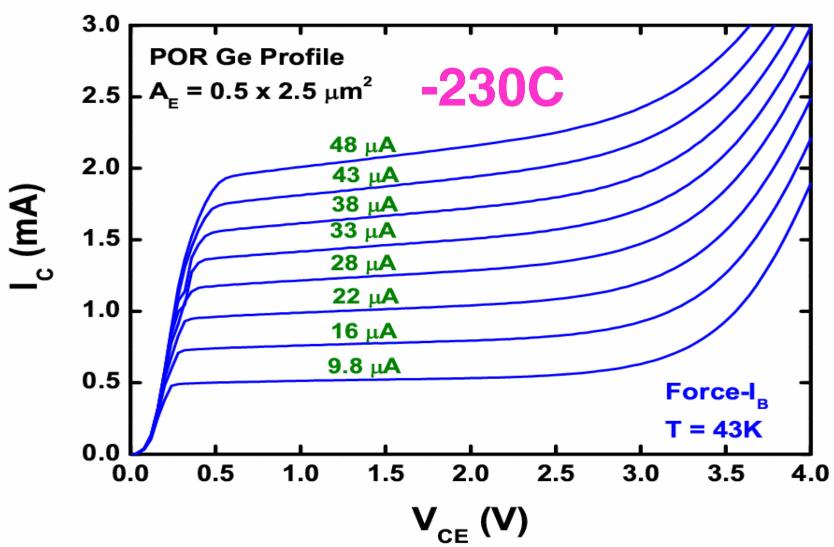

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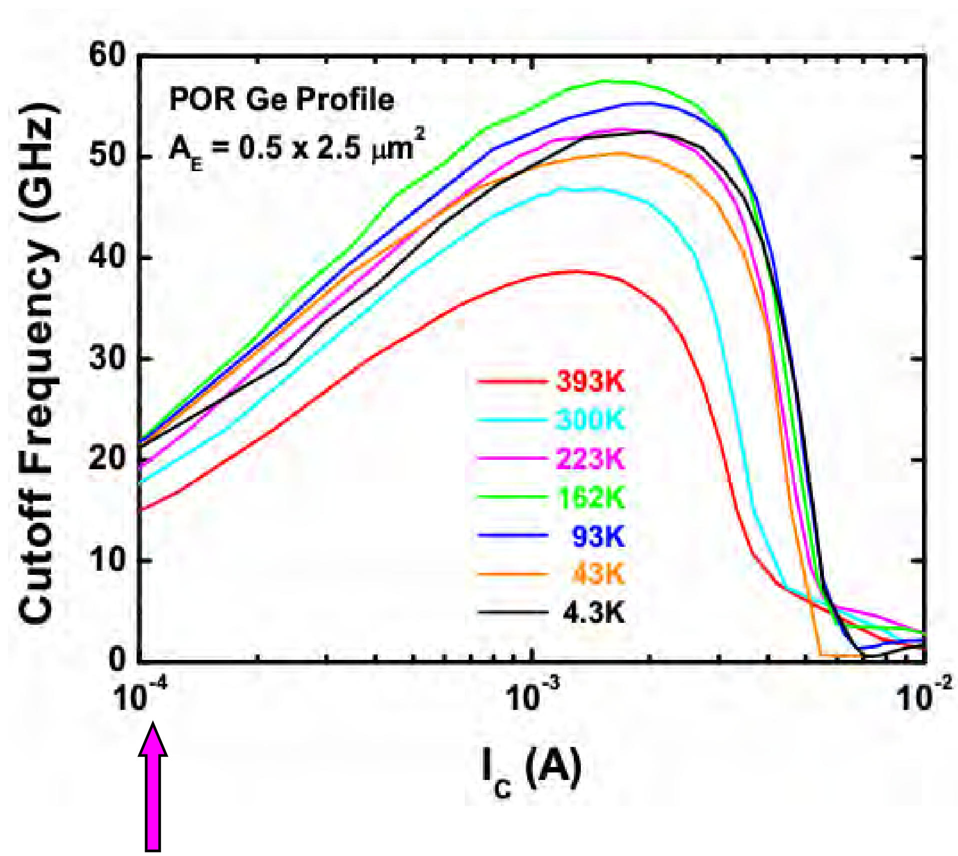
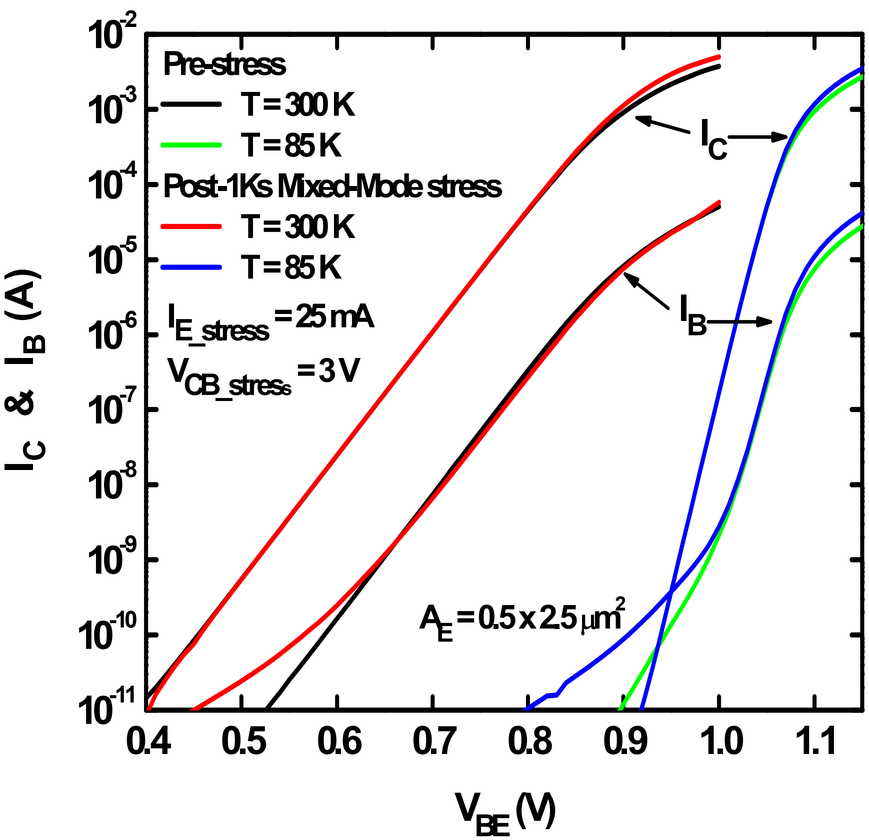


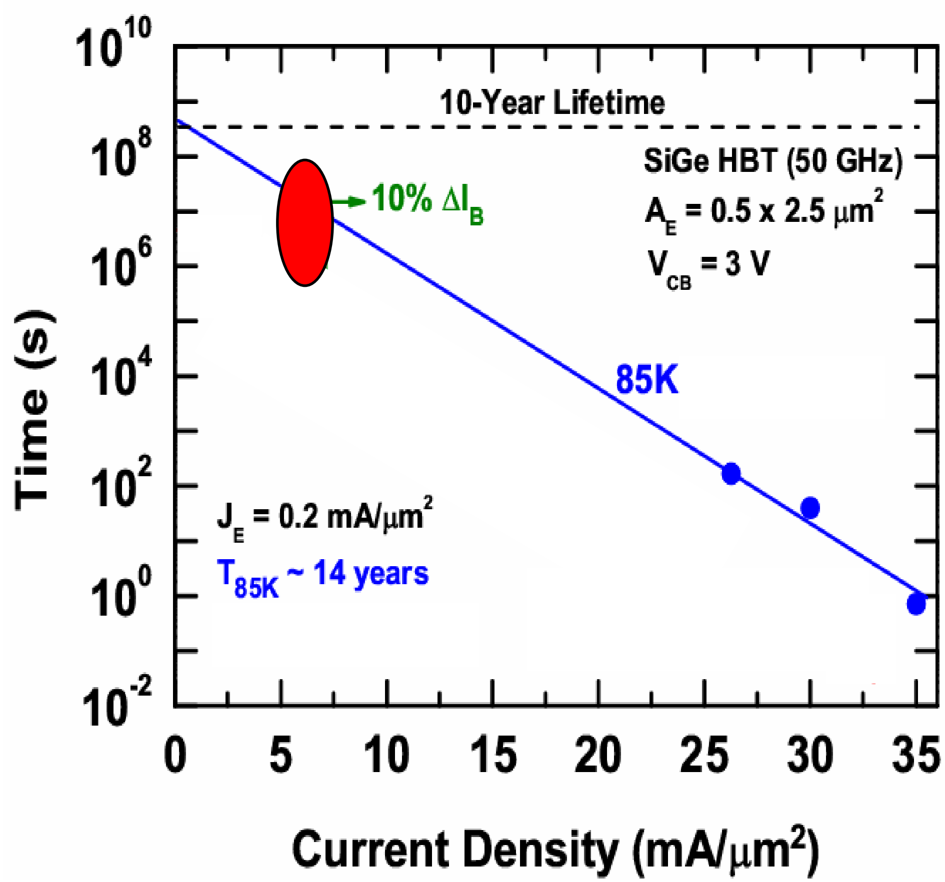
SiGe Exhibits Very High Speed at Very Low Power!

IBM SiGe 5AM

Reliability

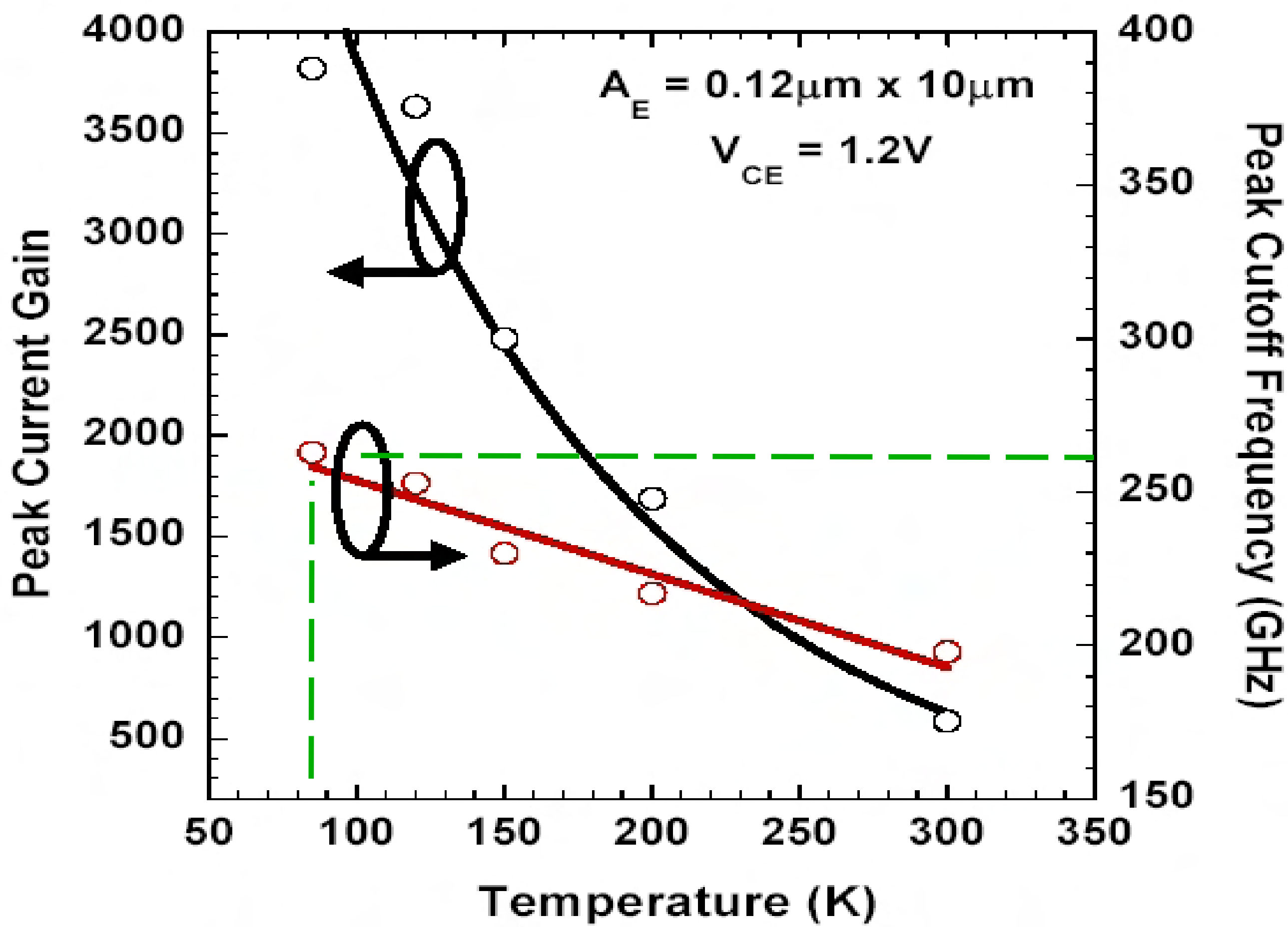
- **Extreme Mixed-Mode Stress Applied** (High J_C + High V_{CB})
- **SiGe HBTs Meets System Reliability Needs at Cryo-T**





Impact of Scaling

- 200 GHz SiGe HBTs (3rd Generation) Work VERY Well at 77K



Will Support Cryo-T mm-wave Circuits!

Cryogenic SiGe LNAs

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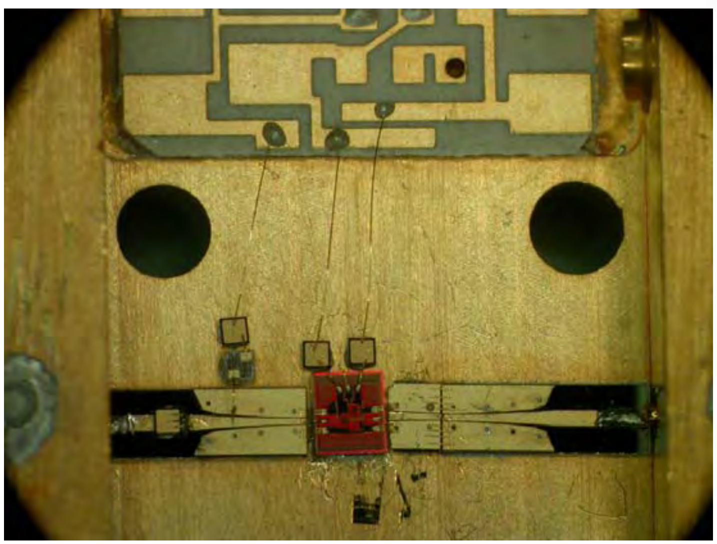
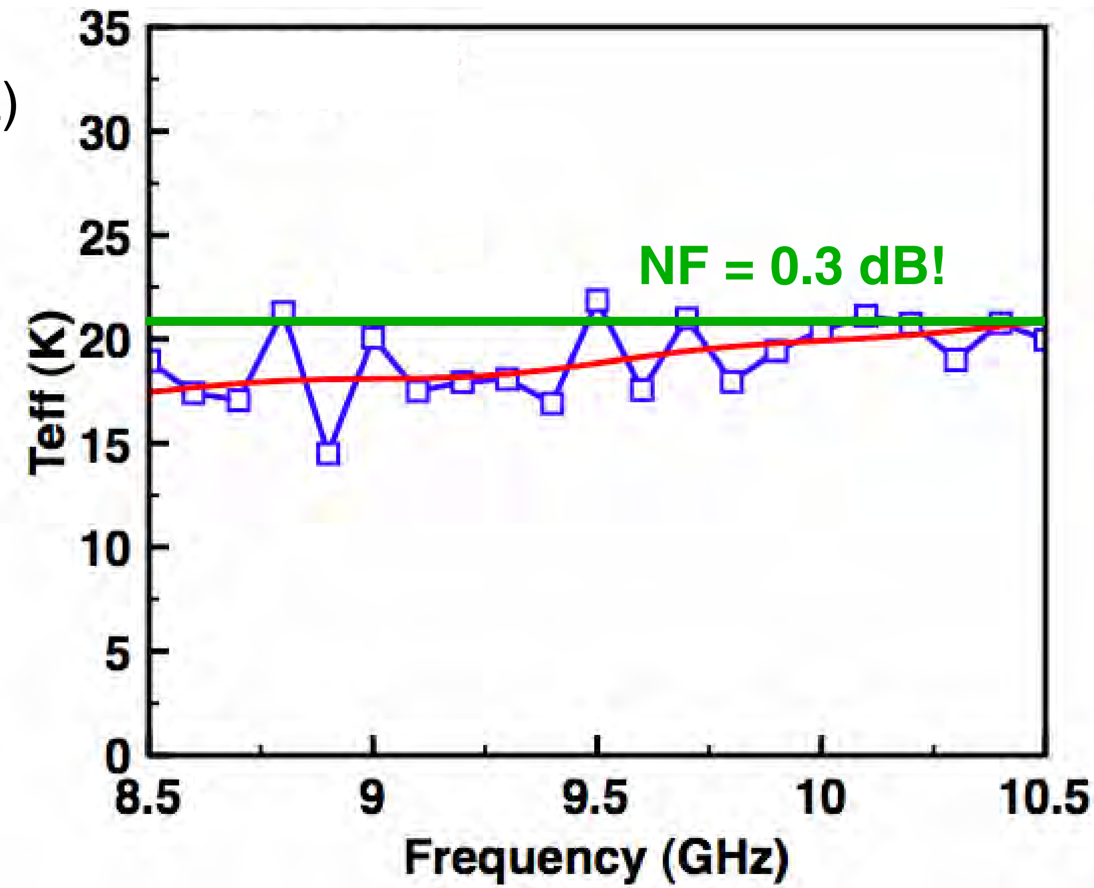
Record SiGe LNA Noise Figure at 15 K (Not Optimized!)

- **T_{eff} < 20 K** (noise T)
- **NF < 0.3 dB** (8.5-10.5 GHz)
- **Gain > 20 dB**
- ***dc* power < 2 mW**



Collaboration with
S. Weinreb & team, Cal Tech

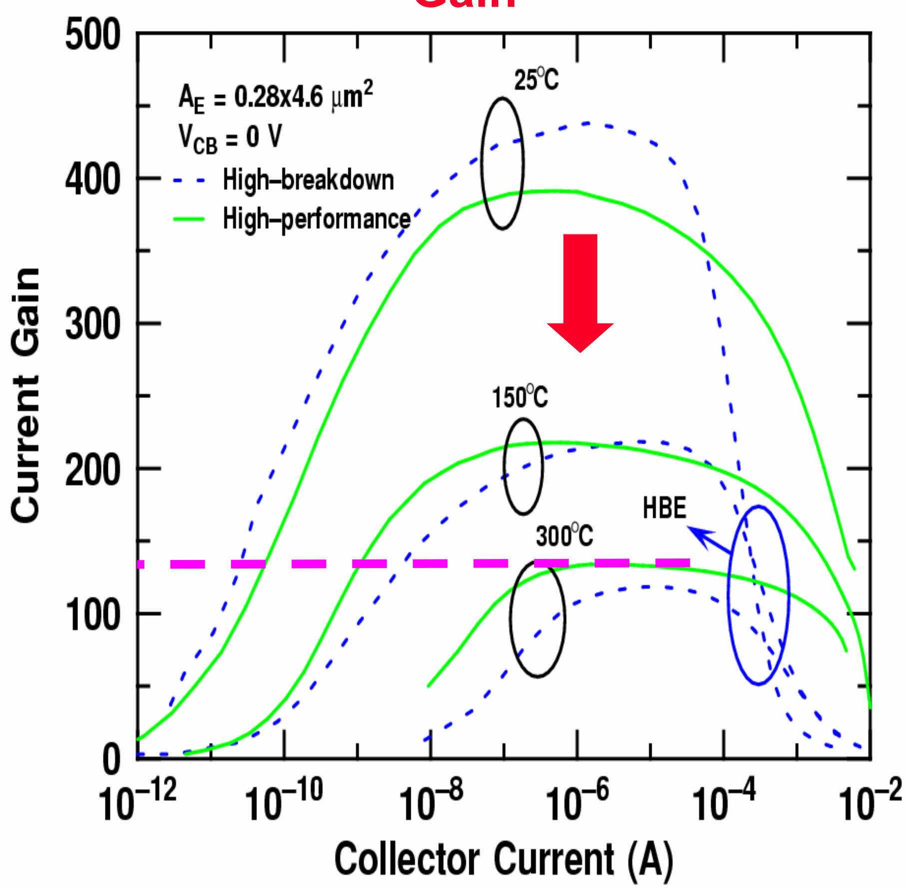


Getting Close to HEMT Noise Records!
… with 3rd Generation SiGe

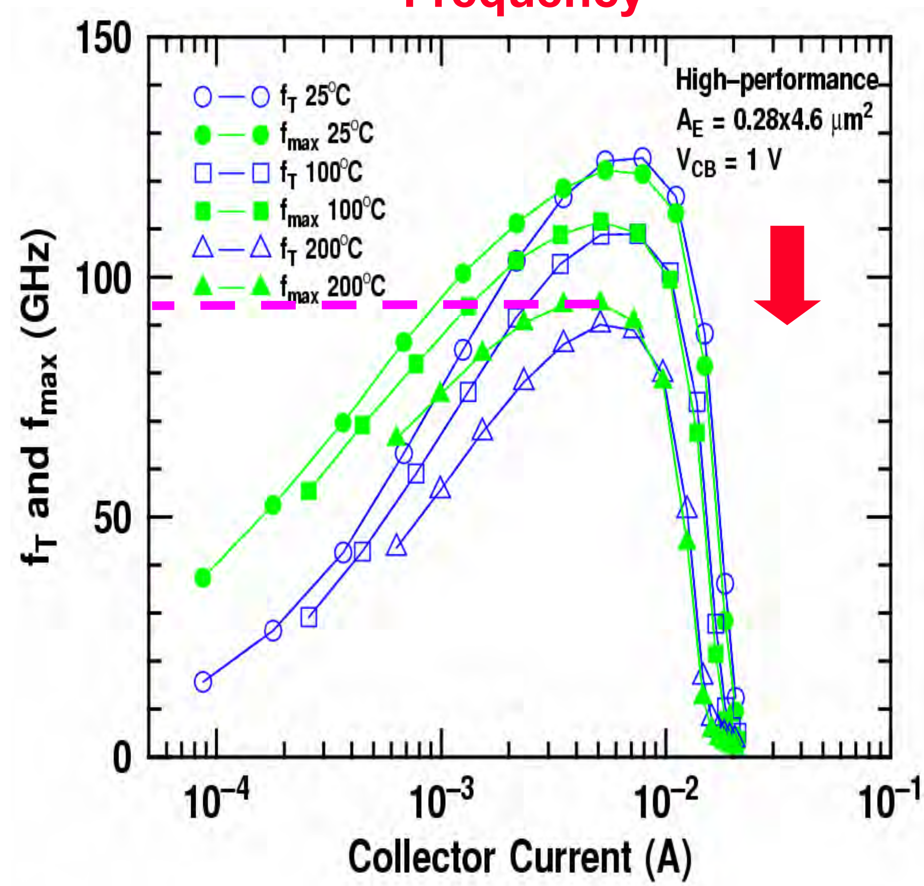
High-Temperatures

- How About SiGe for High-temperature (200-300C) Circuits?
- Degradation, But Plenty of Performance Left!
- Device-level Reliability Looks Good

Gain

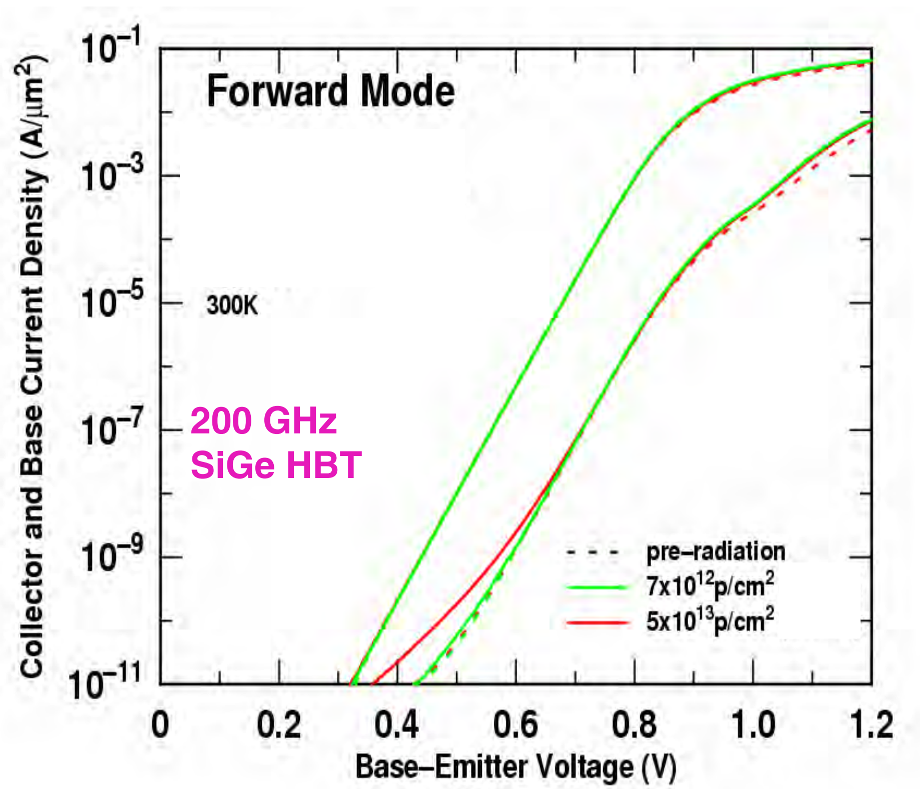


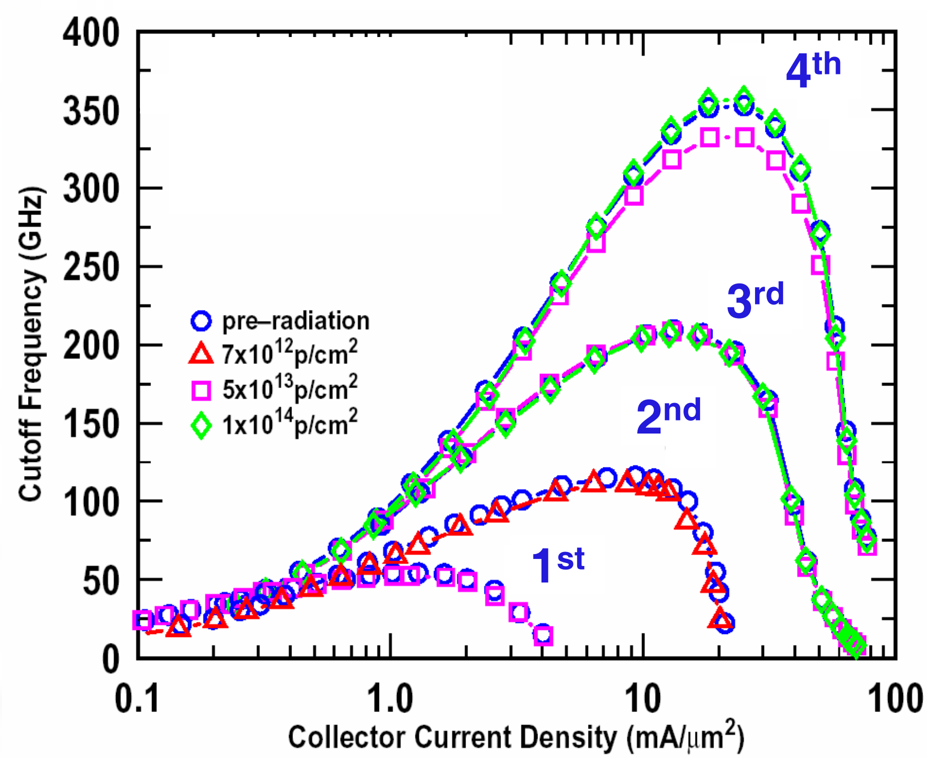
Frequency



Total-Dose Response

- **Multi-Mrad Total Dose Hardness (with no intentional hardening!)**
  - **- ionization + displacement damage very minimal over T; no ELDRS!**
- **Radiation Hardness Due to Epitaxial Base Structure (not Ge)**
  - thin emitter-base spacer + heavily doped extrinsic base + very thin base



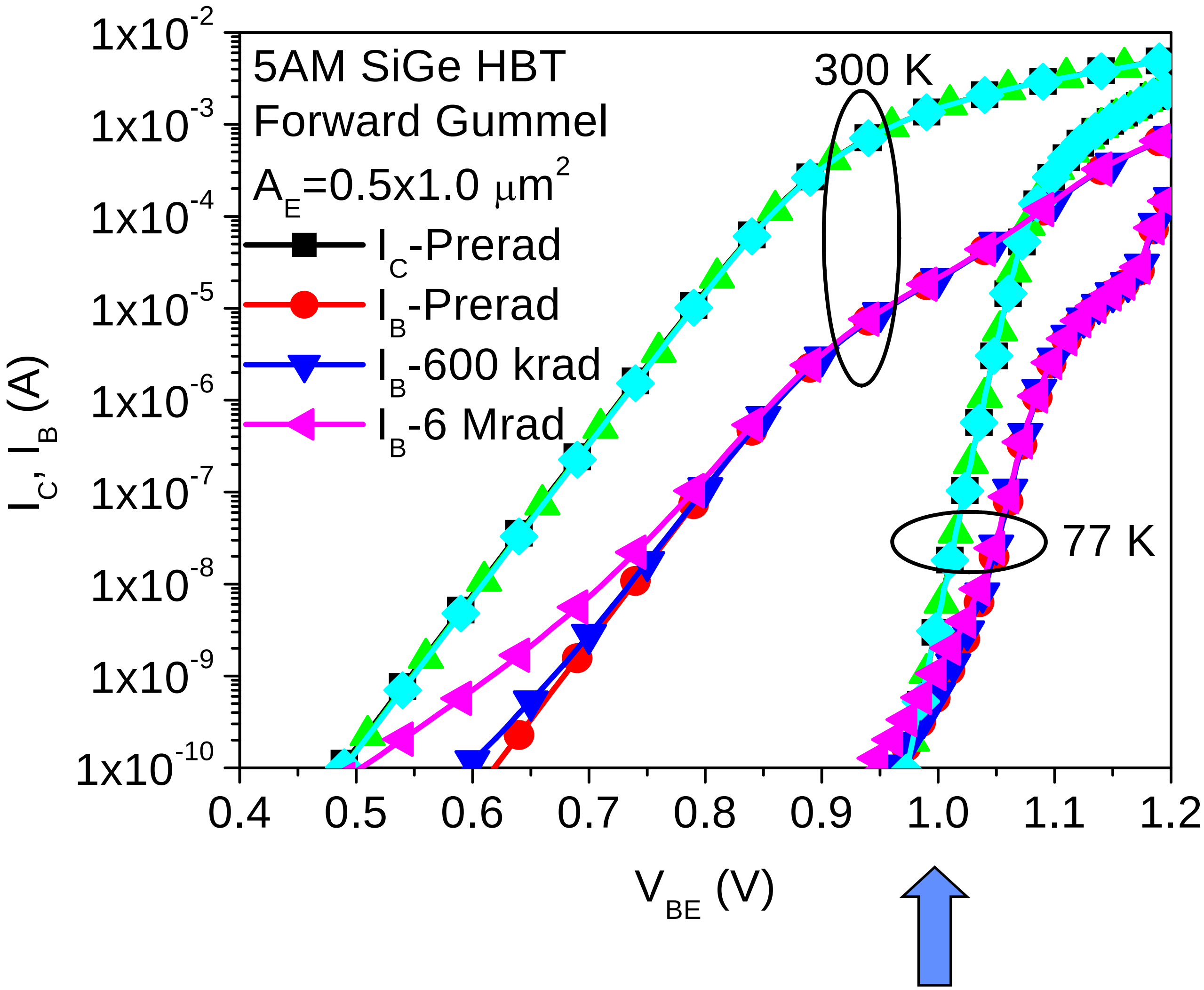


63 MeV protons @ $5x10^{13}$ p/cm^2 = 6.7 Mrad TID!

Cryo-T Irradiation

Georgia Institute of Technology

- **SiGe HBT Still Multi-Mrad Hard at 77K**

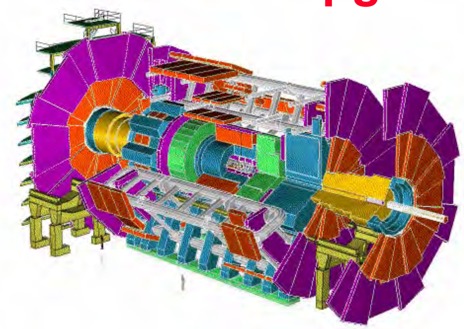


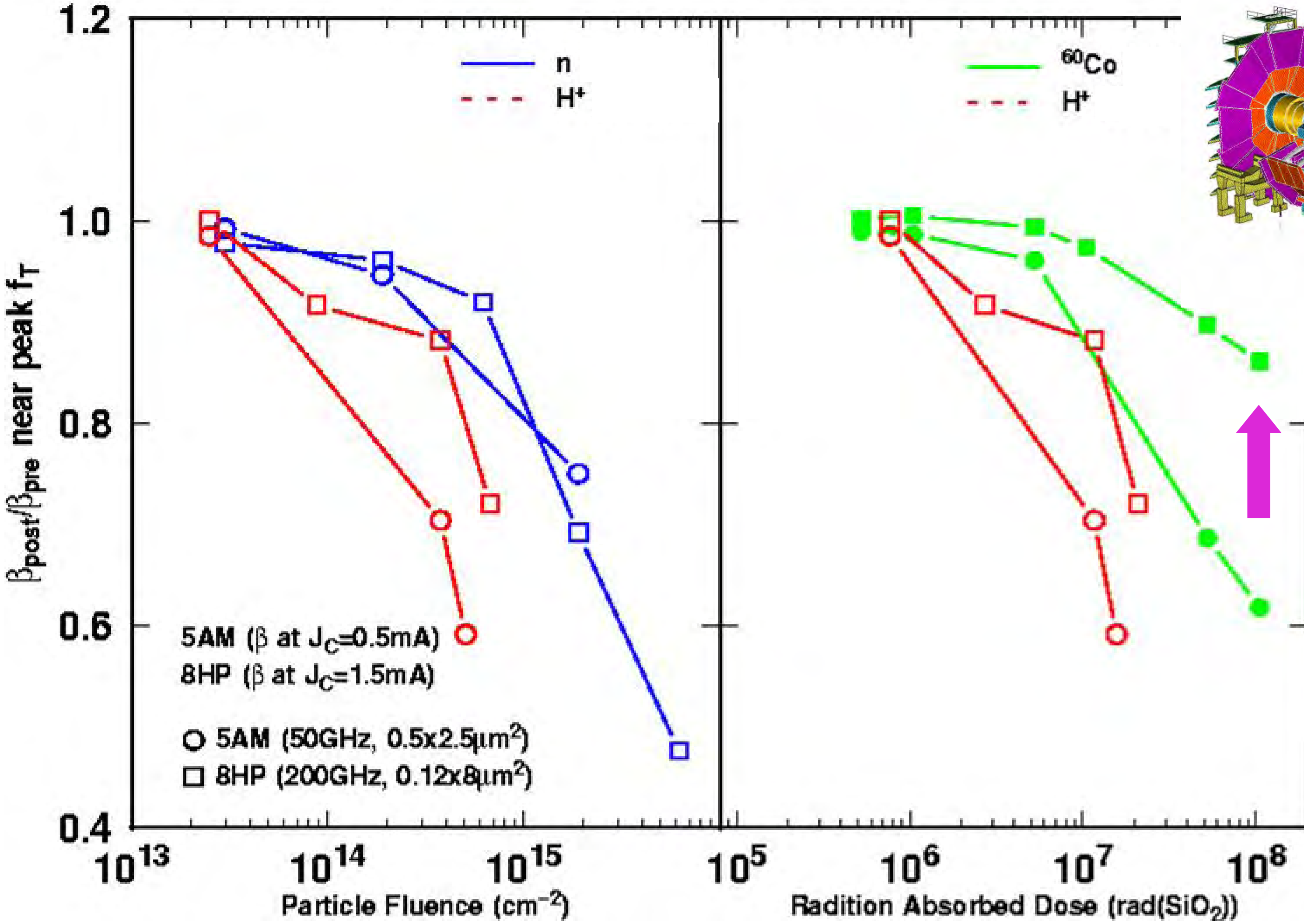
Extreme Dose / Fluence

Georgia Institute of Technology

- **Peak β > 50 after 1x10^{15} p/cm^2 / 100 Mrad**

CERN
ATLAS upgrade



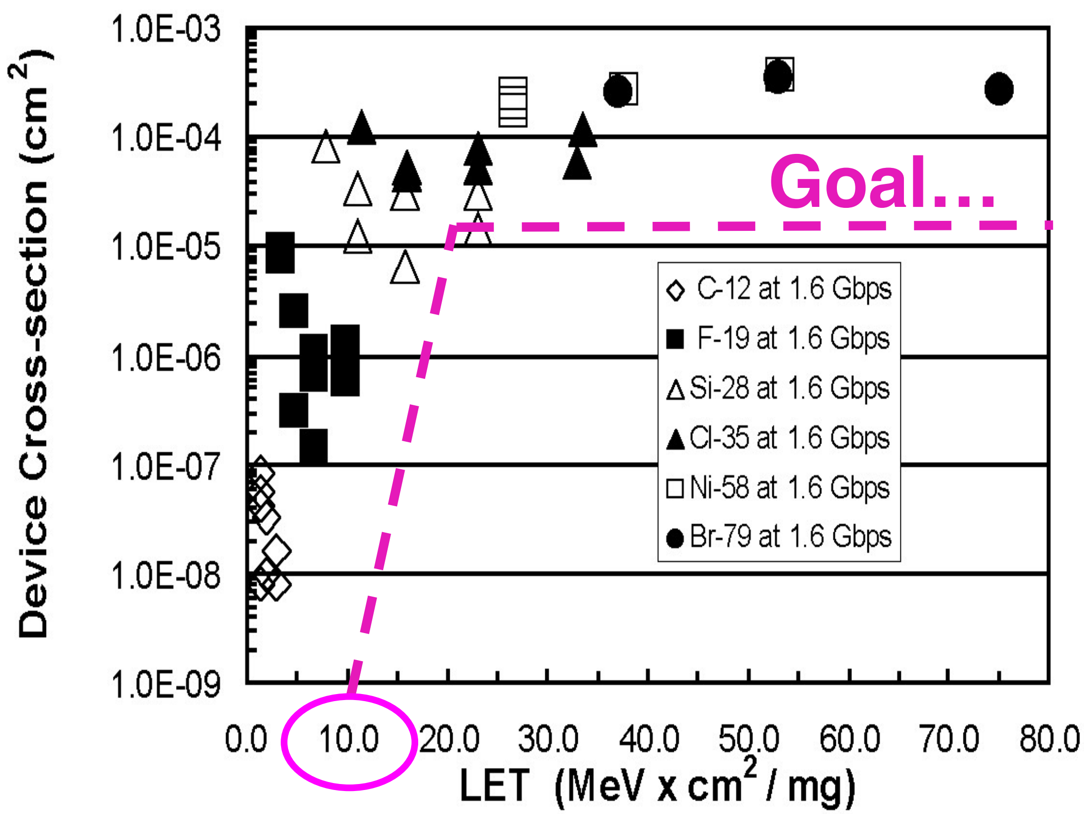


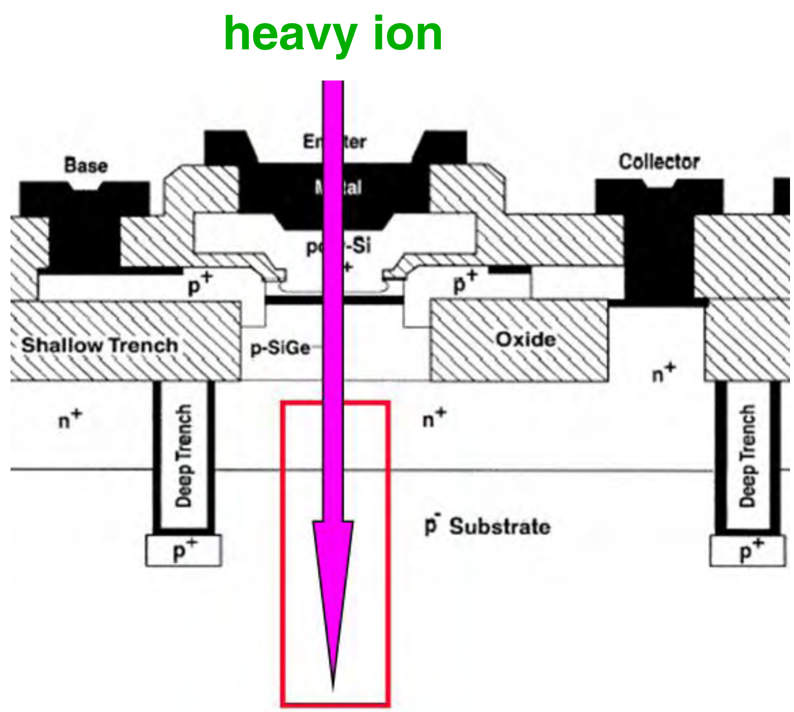
100 Mrad!

UC Santa Cruz
DOE Leverage

Single Event Effects

- **Observed SEU Sensitivity in SiGe HBT Shift Registers**
  - low LET threshold + high saturated cross-section **(bad news!)**

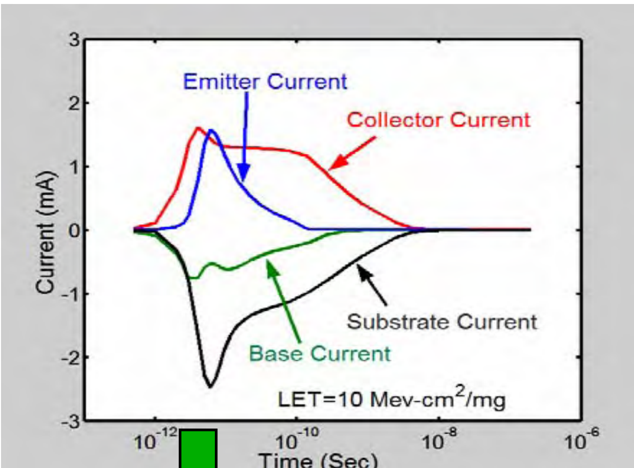


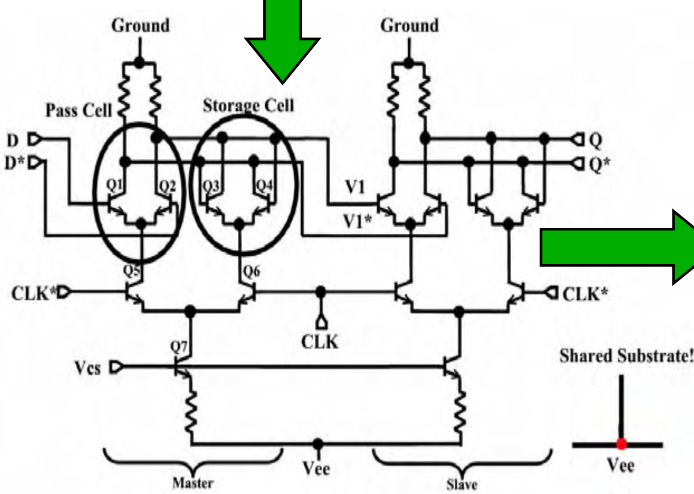


P. Marshall *et al.*, *IEEE TNS*, 47, p. 2669, 2000

SEU: TCAD to Circuits

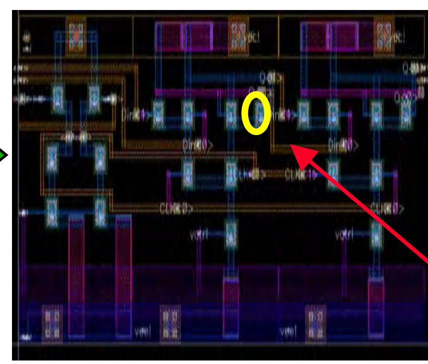
"TCAD Ion Strike"

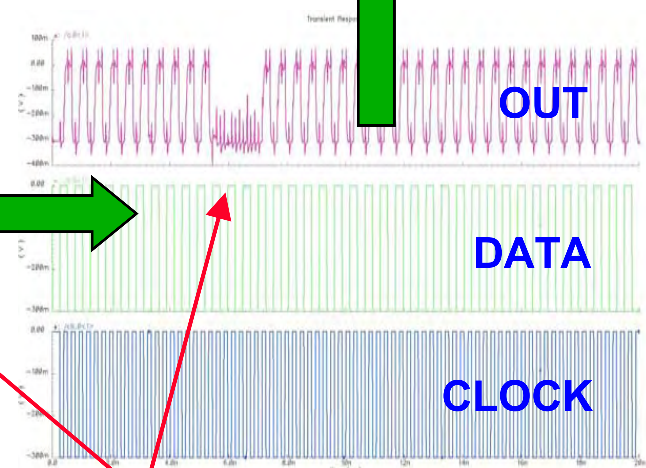




Standard Master Slave Latch

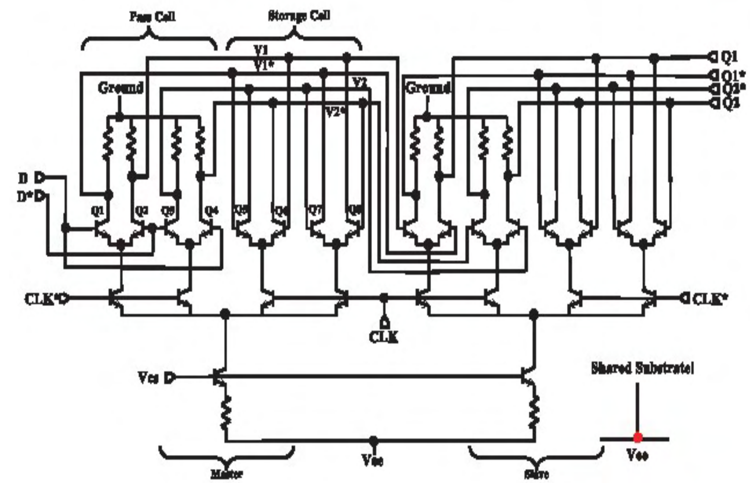
SEU "Soft"





UPSETS

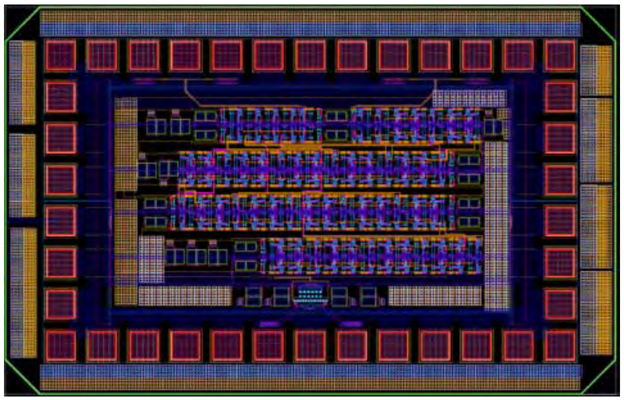
New RHBD SiGe Latch

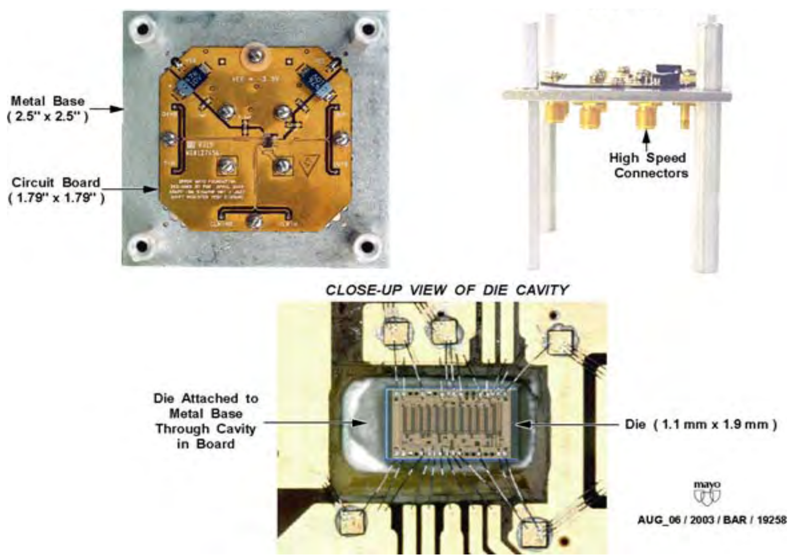


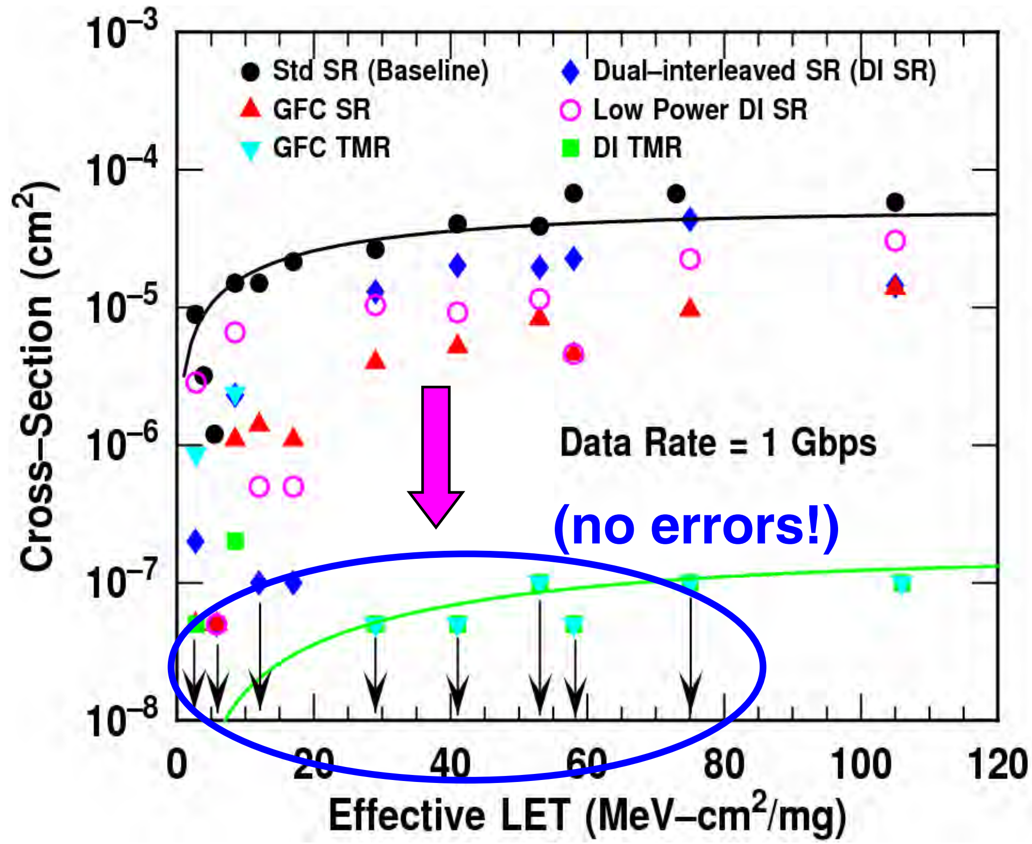
SEU RHBD Success!

Georgia Institute of Technology

- Reduce Tx-Tx Feedback Coupling Internal to the Latch
- Circuit Architecture Changes + Transistor Layout Changes







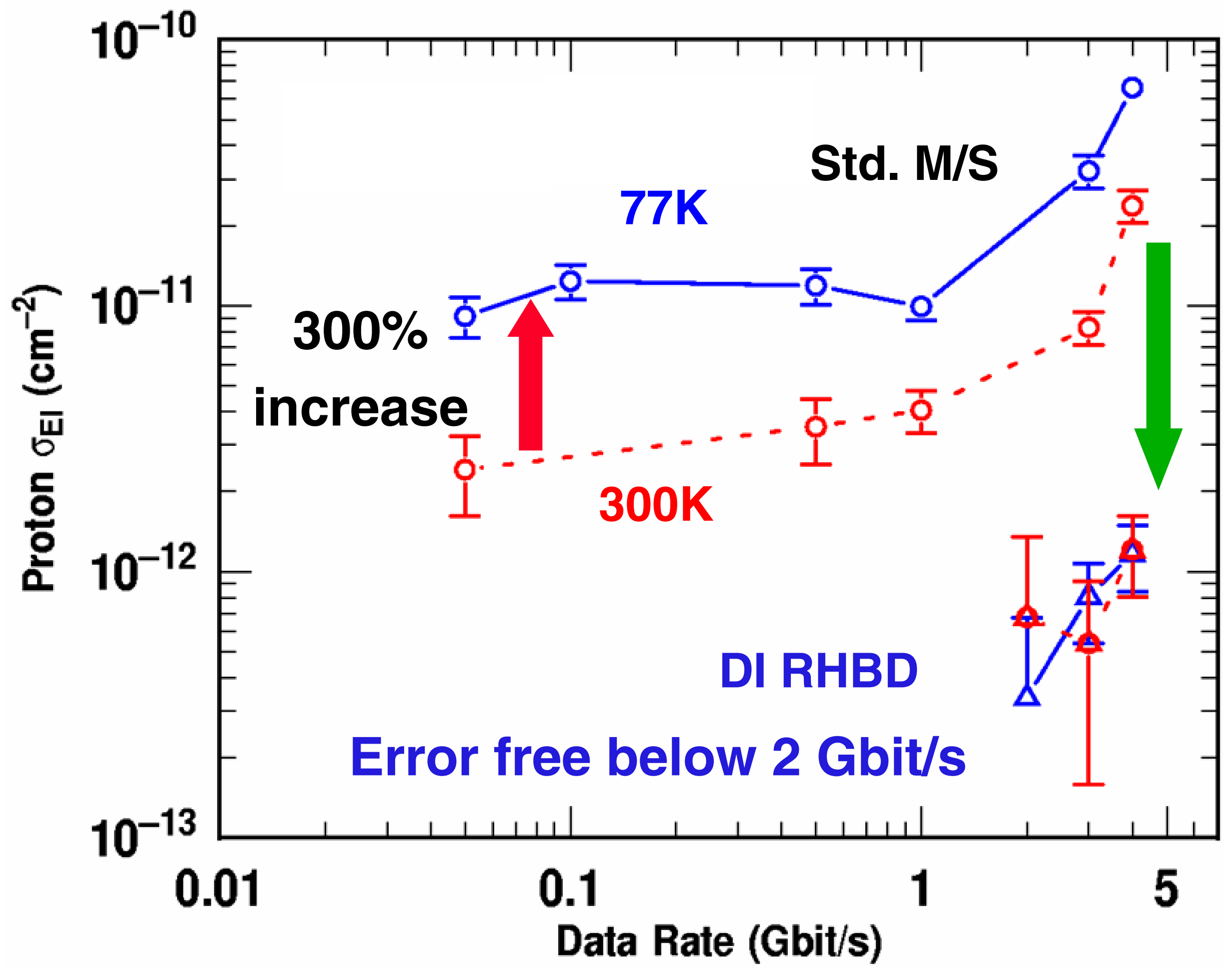
Future Path

- Eliminate TMR & Be Faster!
- Build a Rad-Hard System!

SEU at Cryo-T

Georgia Institute of Technology

- Proton σ_{EI} is 5 Orders of Magnitude Less Than Heavy Ion σ_{EI}
- 3X Increase in Proton Cross-section at 77K for Std. M/S … BUT
- DI RHBD is Error-free < 2 Gbit/s and Insensitive to Temperature



63 MeV protons

$$\sigma_{EI} = \frac{\text{Number of Error Intervals}}{\text{Fluence } (\Phi)}$$

Outline

- Extreme Environment Electronics (EEE)
- Using Si CMOS at Low Temperatures
- Using SiGe HBTs at Low Temperatures
- **Building the Infrastructure for EEE**
- Summary

NASA ETDP SiGe Project

Georgia Institute of Technology

"SiGe Integrated Electronics for Extreme Environments"

PM: A. Keys, NASA MSFC

Objectives:

Develop and Demonstrate Extreme Environment Electronic Components Required for Distributed Architecture Lunar / Martian Robotic / Vehicular Systems Using SiGe Technology

Extreme Environment Requirements: (e.g., Lunar)

- **+120C (day) to -180C (night) + cycling**
- **radiation** (TID + SEU tolerant)

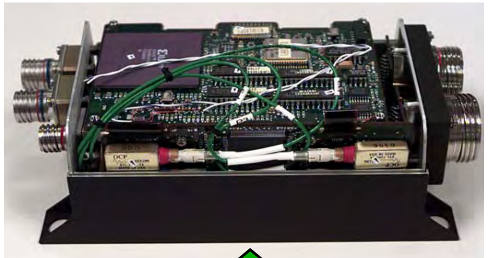
- **Major Project Goals / Approach:**
  - prove SiGe BiCMOS technology for +120C to -180C applications
  - develop mixed-signal electronics with proven extreme T + rad capability
  - develop best-practice extreme T range circuit design approaches
  - **deliver** compact modeling tools for circuit design **(design suite)**
  - **deliver** requisite mixed-signal circuit components **(component library)**
  - **deliver** robust packaging for these circuits **(integrated multi-chip module)**
  - **deliver** a functional SiGe REU prototype meeting lunar specs
  - validate device + circuit + package reliability
  - develop a robust maturation path for NASA mission insertion (TRL-6)

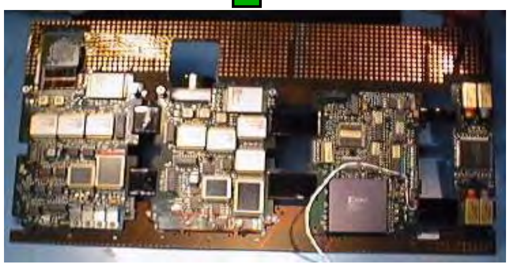
A World Class Team!

- **Georgia Tech** (Device Technology IPT lead)
  - John Cressler *et al.* (PI, devices, reliability, circuits)
  - Cliff Eckert (program management, reporting)
- **Auburn University** (Packaging IPT lead)
  - Wayne Johnson *et al.* (packaging); Foster Dai *et al.* (circuits); Guofu Niu *et al.* (devices)
- **University of Tennessee** (Circuits IPT lead)
  - Ben Blalock *et al.* (circuits)
- **University of Maryland** (Reliability IPT lead)
  - Patrick McCluskey *et al.* (reliability, package physics-of-failure modeling)
- **Vanderbilt University**
  - Mike Alles, Robert Reed *et al.* (radiation effects, TCAD modeling)
- **JPL** (Applications IPT lead)
  - Mohammad Mojarradi *et al.* (applications, reliability testing, circuits)
- **Boeing**
  - Leora Peltz *et al.* (applications, circuits)
- **University of Arkansas / Lynguent** (Modeling IPT lead)
  - Alan Mantooth / Jim Holmes *et al.* (modeling, circuits)
- **BAE Systems**
  - Richard Berger, Ray Garbos *et al.* (REU architecture, maturation, applications)
- **IBM**
  - Alvin Joseph *et al.* (SiGe technology, fabrication)

Remote Electronics Unit

Georgia Institute of Technology





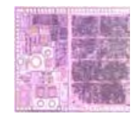
The X-33 Remote Health Unit, circa 1998

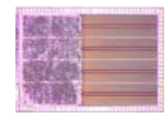
The NASA ETDP SiGe Remote Electronics Unit, circa 2009

REU in connector housing!

Analog front end die

Digital control die





Conceptual integrated REU system-on-chip SiGe BiCMOS die

Specifications

- 5” x 3” x 6.75” = 101 in^3
- 11 kg
- 17 Watts
- -55°C to +125°C

Goals

- 1.5” x 1.5” x 0.5” = 1.1 in^3 **(100x)**
- < 1 kg **(10x)**
- < 2 Watts **(10x)**
- **-180°C to +125°C, rad tolerant**

Supports Many Sensor Types:

Temperature, Strain, Pressure, Acceleration, Vibration, Heat Flux, Position, etc.

Use This SiGe REU as a Remote Vehicle Health Monitoring Node

Summary

- **Low-Temperature Electronics**
  - a key niche in the **extreme environment electronics** portfolio
  - a key need for envisioned planetary exploration
  - cryo-T is often needed in tandem with radiation exposure
- **Si CMOS**
  - many performance metrics improve with cooling
  - reliability issues can be a concern (address with longer L)
  - radiation exposure can be a concern (may need RHBD)
  - SOI can help on the radiation vulnerability
- **SiGe HBTs**
  - **all** performance metrics improve with cooling **(natural for EEE)**
  - major new lunar application for +120C to -180C **= infrastructure**
  - built-in multi-Mrad total dose hardness
  - use RHBD for SEE mitigation
  - SiGe Technology = SiGe HBT + Si CMOS (bulk + SOI)