DEVELOPMENT OF DUAL-FIBER ARRAY LASER ULTRASONIC SYSTEM FOR INSPECTING AND ASSESSING AREA-ARRAY MICROELECTRONIC PACKAGES

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To

My Mentor

Late Prof. Charles Ume

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LIST OF ABBREVIATIONS

AI	Artificial Intelligence
ALT	Accelerated Life Testing
AOI	Automated Optical Inspection
ATC	Accelerated Thermal Cycling
BGA	Ball Grid Array
BLR	Board Level Reliability
CSAM	C-mode Scanning Acoustic Microscopy
CSP	Chip-Scale Packages
CT	Computed Tomography
CTE	Coefficient of Thermal Expansion
DALUS	Dual-Fiber Array Laser Ultrasonic System
DCP	Data-Collection-Point
DIP	Dual In-line Package
DOE	Design of Experiments
DT	Drop Testing
DUI	Device Under Inspection
FC	Flip Chip
FCBGA	Flip Chip Ball Grid Array
FE	Finite-Element
FPBT	Four-Point Bend Testing
GRR	Gage Repeatability and Reproducibility
HIP	Head-In-Pillow

I/O	Input/Output
IC	Integrated Circuit
IMC	Inter-Metallic Compound
IoT	Internet of Things
IRM	Infrared Microscopy
IRT	Infrared Thermography
LCC	Leadless Chip Carrier
LSL	Lower Specification Limit
LSP	Local Search Pattern
LUI	Laser Ultrasonic Inspection
MCC	Modified Correlation Coefficient
MCI	Magnetic Current Imaging
MCI	Measurement Capability Index
MLCC	Multilayer Ceramic Capacitors
MVP	Minimum Viable Product
Nd:YAG	Neodymium-doped Yttrium Aluminum Garnet
NSMD	Non-Solder Mask Defined
P/T	Precision-to-Tolerance
PCB	Printed Circuit Board
PGA	Pin Grid Array
PoP	Package-on-Package
PZT	Piezoelectric Transducers
QFN	Quad-Flat No-leads
QFP	Quad Flat Package
SAC 305	96.5 Sn – 3% Ag – 0.5% Cu

SAM	Scanning Acoustic Microscopy
SCP	Single-Chip Package
SDK	Software Development Kit
SEM	Scanning Electron Microscopy
SiP	System-in-Package
SLUS	Single Laser Ultrasonic System
SMD	Surface Mount Devices
SMD	Solder Mask Defined
SMT	Surface Mount Technology
SNR	Signal-to-Noise Ratio
SOP	Small Outline Package
SPI	Solder Paste Inspection
TDR	Time Domain Reflectometry
TIM	Thermal Interface Material
TSAM	Through-Transmission Scanning Acoustic Microscopy
USL	Upper Specification Limit
WLCSP	Wafer Level Chip Scale Packages
WLP	Wafer Level Packages

SUMMARY

The microelectronic package design has been continuously evolving with complicated interconnections to keep up with the constant consumer demands of day to day electronic products that are miniature, fast, compact, high density, reliable, and low cost. Microelectronic technology made progress by leaps and bounds by transitioning from traditional through-hole technology to surface mount technology. Moreover, the utilization of surface mount devices, such as flip-chip packages, chip-scale packages, and ball grid array packages have helped to decrease the size of microelectronic packages using solder ball interconnections between devices and substrates and/or printed circuit boards.

The failures in solder ball interconnects makes a microelectronic packaging system inoperable. The failures often result from defects during assembly and/or due to damage accrued from thermo-mechanical and other loads during operation after the assembly. However, these interconnections in advanced microelectronic packages are difficult to evaluate because they are hidden underneath the package.

Currently, both destructive testing such as cross-sectioning along with microscopy, and dye-and-pry testing, as well as non-destructive testing such as daisy-chain electrical resistance measurement, X-ray and Scanning Acoustic Microscopy (SAM) are being used to detect solder interconnect failures. However, both destructive and non-destructive testing have significant limitations in detecting defects and failures. High-end electronics consumers like automotive, defense, etc. require near-flawless systems to prevent catastrophic failures. Therefore, there is an increased demand for a new reliable and robust inspection technique for the evaluation of solder ball interconnections, especially in the

area-array microelectronic packages. Laser Ultrasonic Inspection (LUI) has been regarded as a potential technique to meet this demand.

The objective of this research is to develop a fast, robust, low cost, non-contact, non-destructive, accurate, and highly sensitive Dual-Fiber Array Laser Ultrasonic System (DALUS) for inspecting and assessing area-array microelectronic packages. DALUS is a significant path forward of the previous Single Laser Ultrasonic System (SLUS) in the sense that this newly developed system has dual laser beams to excite at two spatially-distinct locations and thus allowing higher total energy to be delivered onto the microelectronic package under inspection. The higher laser energy produces higher strength ultrasound waves in the test sample, which will improve the sensitivity of the system as well as facilitate the inspection of large and multi-leveled packages. This report explains detailed improvements, safety features, and technical capabilities of the newly developed system.

This developed system is employed to detect failures in industrial microelectronic packages that were subjected to drop testing, thermal cycling test, and mechanical bend testing. The utility of the developed system is demonstrated in a holistic manner through these tests which produced different sizes and nature of cracks at various locations within the solder interconnects. The experimental results were validated with destructive testing results including Scanning Electron Microscopy (SEM) and dye-and-pry testing. In parallel to the experiments, finite-element simulations that account for the viscoplastic behavior of solder joints as well as the direction- and temperature-dependent properties of other materials in package assembly, are carried out. The damage predictions from the simulations and the experiments are correlated. Finally, the measurement capability of

DALUS is verified as per the industrial standards using gage repeatability and reproducibility analysis.

The successful completion of the research objectives has led to DALUS prototype with more user-friendliness, higher throughput, better repeatability/reproducibility, improved flexibility, and superior sensitivity. The application scope of the LUI technique is significantly expanded to evaluate solder ball interconnections in more complex and advanced microelectronic packages through the development of DALUS. These accomplishments have built strong credentials and laid a path to commercialization of the LUI technique.

CHAPTER 1. INTRODUCTION

Microelectronic packaging is an interface that combines Integrated Circuit (IC) chip and other components into a single, ready to use package that is used to form electronic products. This packaging provides the electrical pathways to connect IC to the outside world along with improved thermal and mechanical properties [1]. Since the advent of Surface Mount Technology (SMT) devices, the microelectronic industry has grown to touch almost every aspect of modern-day life. Miniaturization and high performance are the key trends in the current, rapidly growing microelectronic packaging technologies [2]. Electronic chip package design is evolving with complicated connections to the Printed Circuit Board (PCB) to keep up with electronics miniaturization trends. These connections in advanced electronic chip packages are hard to evaluate for defects and failures when assembled to the PCB as the connection points are underneath the package. Hence, the microelectronic packaging industry has an unfulfilled need for a reliable non-destructive technique for inspecting microelectronic packaging. Laser Ultrasonic Inspection (LUI) is providing a fast, low-cost, and noncontact electronic package inspection solution that allows accurate advanced chip connection evaluations.

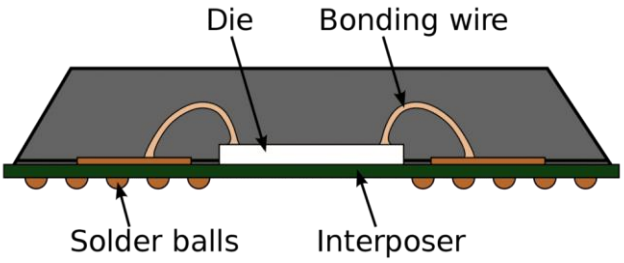
1.1 Overview of Microelectronic Packaging

1.1.1 Electronic System and Components

An Electronic System is a physical interconnection of components, or parts, that control a physical process or perform some type of mathematical operation on the signal. The electronic system gathers input signals from devices such as sensors, processes

the signal using ICs inside the microelectronic packages, and sends out an output signal(s) to do the desired function. Hence, electronic systems are essentially made of an assembly of ICs, microelectronic packages, and modules.

Microelectronic packages are the IC carriers that go onto system-level boards in electronic systems. An example of a Ball Grid Array (BGA) package with its components is shown in Figure 1. The primary function of microelectronic packaging is to enable the IC chip within the package to perform its designated function reliably through the intended design life of the system. Other roles of packaging are (i) to provide interconnections for signal and power, (ii) to provide mechanical support and robustness to the fragile IC, (iii) to provide environmental protection of the IC, and (iv) to provide heat dissipation.

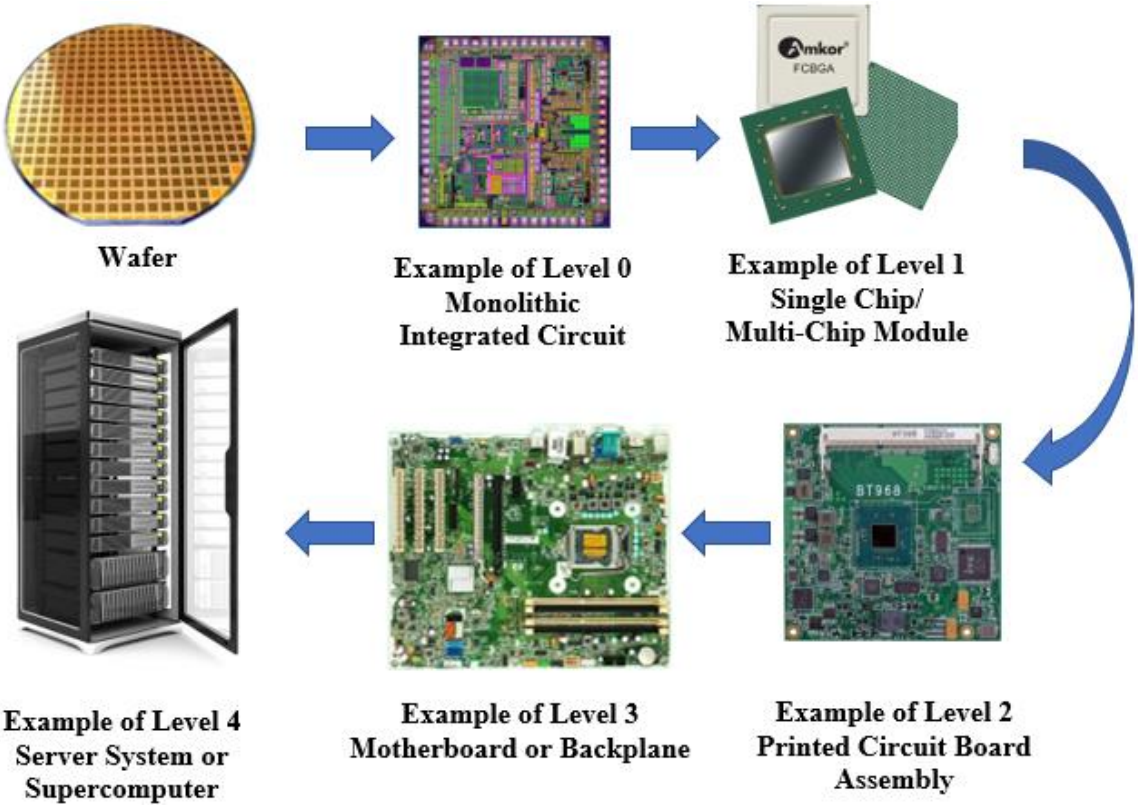


(Ref: NuWaves Engineering)

Figure 1 – Example of a Ball Grid Array (BGA) package

Different levels of packaging are needed to redistribute information from chip to human interface. Typically, electronic packaging is divided into five levels as shown in Figure 2. These levels are required to mitigate risk, if one subsystem fails, it can be replaced rather than the entire system. Level 0 is IC on a monolithic silicon die. Level 1 is an IC chip on the carrier (microelectronic package) where silicon die is assembled onto a package carrier (substrate or lead frame) with first-level interconnections. Level 2 is board-level packaging where one or more microelectronic packages are assembled onto the PCB or

another type of substrate. In level 3, multiple boards or packages are assembled to form a motherboard or back panel. Level 4 is a server-level system, where a rack or frame may hold several shelves of subassemblies that must be connected to make up a complete system, such as a server system or a supercomputer.



(Ref: Amkor, Intel, HP)

Figure 2 – Electronic packaging hierarchy

This dissertation work focuses on the development of the dual-fiber array laser ultrasonic system for the inspection of area-array microelectronic packages assembled on the PCB (Level 2 packaging in Figure 2).

1.1.2 Trends in Microelectronic Packaging

A schematic showing the evolution of microelectronic packaging is given in Figure 3. One of the first electronic packages that were invented is the Dual In-line Package (DIP) in 1964. The DIP consists of the active device (i.e. die) embedded in a plastic or epoxy compound and wired to a lead-frame that facilitated the external connections to the PCB, which is a typical through-hole packaging technology. In the 1970s, the Surface Mount Devices (SMDs) such as Quad Flat Package (QFP), and Small Outline Package (SOP) were developed to replace DIPs. These SMDs are easy to assemble when compared with DIP. They also help to improve the electrical performance of the devices and increased the density of packages per PCB which led to their widespread use [3]. However, the long signal pathways of these packages have limited the maximum signal speeds while a large amount of encapsulant impeded proper thermal management, thus making the form factor impractical for the emerging handheld electronics market. Leadless Chip Carrier (LCC) and Quad-Flat No-leads (QFN) packages were introduced to reduce the lead inductance and the size of the package.

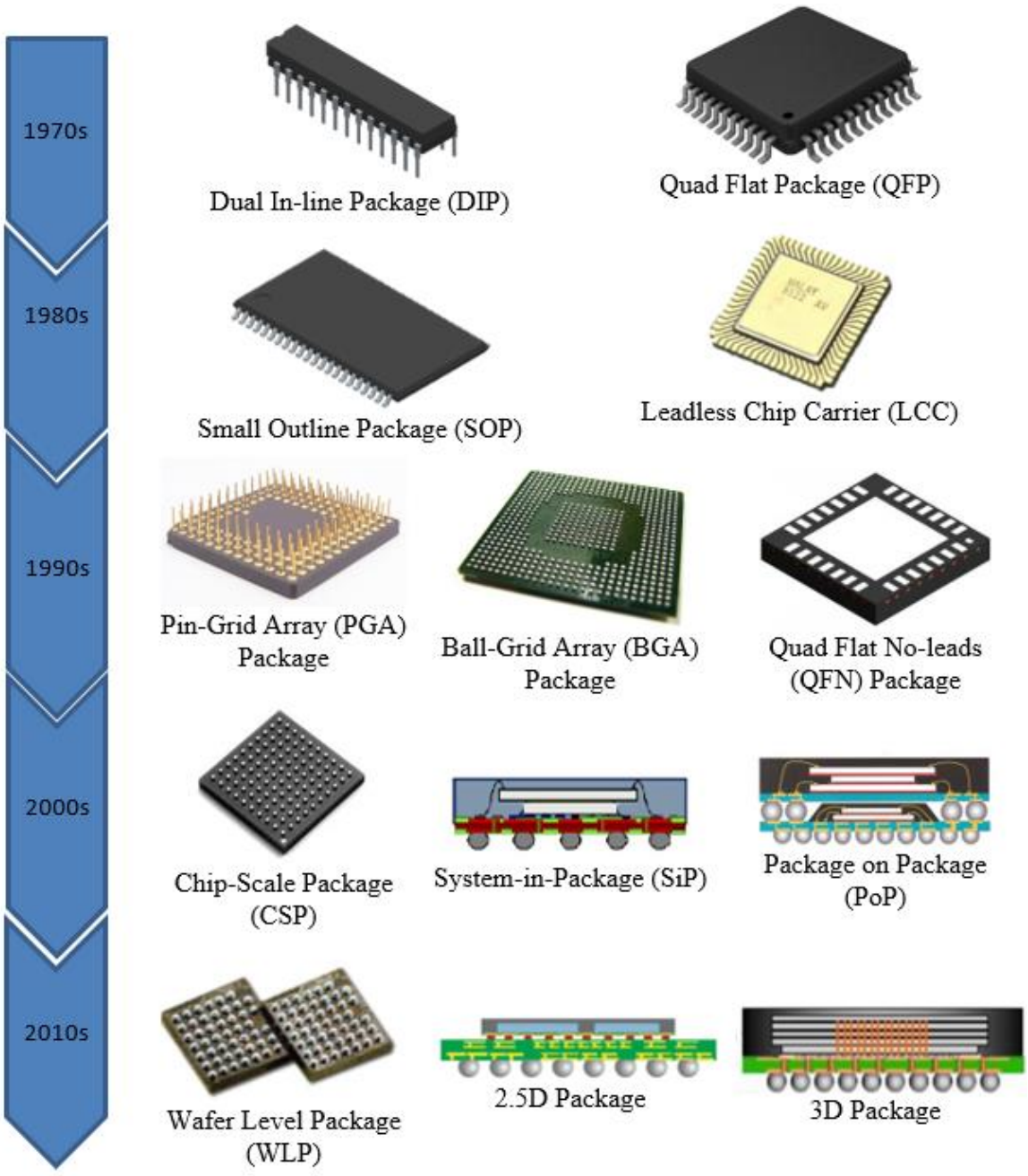


Figure 3 – Evolution of microelectronic packaging [4]

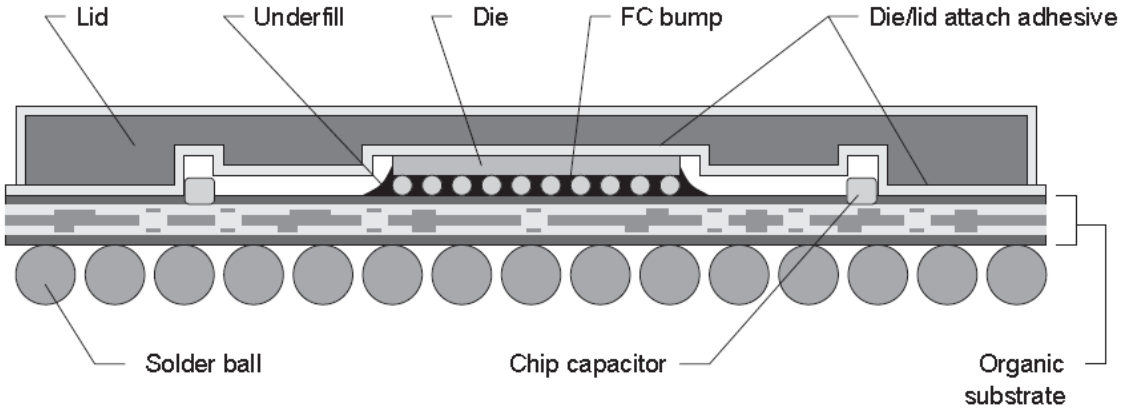
However, these advances were not enough for the demands of the modern world. Additionally, the use of device-to-board connections along only two sides of the chip, as for DIP packages, or along the four sides, as in QFP, QFN, or LCC packages, left large

amounts of space underneath the chip unutilized. Therefore, area-array type packages such as Pin Grid Array (PGA) and Ball Grid Array (BGA) packages were invented in the 1990s. PGAs are mounted on PCBs using the through-hole method or inserted into a socket. The BGA package is the most popular area-array package, where the connections are made with an array of solder balls on the underside of an interface layer called the substrate. In addition to a larger Input/Output (I/O) density, the solder balls also significantly reduce the electrical parasitics and resistance due to their shorter interconnect lengths. Even with BGA packages, the ratio of the die to package area was still inadequate so further advancements were desired. Thus, the Flip-Chip (FC) and Chip-Scale Packages (CSP) were evolved.

The package size of CSP is as small as 1.2 times that of the die itself [5]. Wafer Level Chip Scale Packages (WLCSP) or Wafer Level Packages (WLP) are true chip-scale packages, where the finished device is the same size as monolithic silicon die on the wafer [6]. One difference between WLPs and other CSPs is that WLPs are processed almost entirely before the wafers are diced. Flip-chip and WLP are so similar, in fact, sometimes the names are used interchangeably. The major difference is that FCs typically use greater solder ball pitches and larger solder balls to lessen the problems of excess stress and as such greatly reduce the need for underfill.

Even though solder balls started to emerge in BGA and CSP packages as the second-level interconnects, the wire-bond technique was still dominant in first-level packaging. With the advancement of flip-chip technology, the BGA and CSP packages have evolved into flip-chip packages where the solder balls served as the first-level interconnects. Flip-chip technology solder bumps are deposited on the die's I/O pads and the die is flipped over, active side down on either a carrier package or PCB directly as

shown in Figure 4 [7]. This reduces the number of levels in the packaging hierarchy to one, thereby increasing the signal speed significantly. The minimal package design of flip-chip technology cuts down the manufacturing costs and has many benefits such as high I/O density, excellent electrical characteristics, small size, and low weight.



Ref: Texas Instruments

Figure 4 – A Cross-sectional view of typical Flip-Chip BGA package

With the maturing of portable devices and the growth of the Internet of Things (IoT), manufactures are ever being pushed to create smaller, and more reliable packages. To meet these demands, the microelectronic packaging industry is moving towards developing more sophisticated and advanced packages such as System-in-Package (SiP), Package-on-Package (PoP), 2.5D packages, and 3D packages. Some of these advanced packages reduce real estate by stacking chips in the vertical direction. In 2.5D package technology, multiple dies are combined in the same package by stacking the dies on a substrate/interposer layer which interconnects the dies together and provides the pathways to the lowest level of the package with the connections to the board [8]. Three-dimensional package technology has taken this step further by stacking the silicon wafers themselves on top of each other, grinding off the excess silicon, and providing a means of

interconnection between them, such as silicon side-through, through-hole, and substrate [9]. Both 2.5D and 3D chip technologies offer many benefits over traditional packagings such as a dramatic increase in space efficiency and reduced power consumption [9]. As consumers continue to demand devices of ever-increasing power and functionality, 3D package technology will only continue to grow.

1.1.3 Levels of Interconnections in Area-Array Microelectronic Packages

Interconnections are connections that electrically and mechanically connect active silicon chip and dielectric substrate, and the substrate and PCB. The microelectronic packaging industry has described the hierarchical of interconnect structure by levels as illustrated in Figure 5. The work described in this dissertation, although concentrated on second-level interconnects, applies to all levels in which the solder ball structures are deployed.

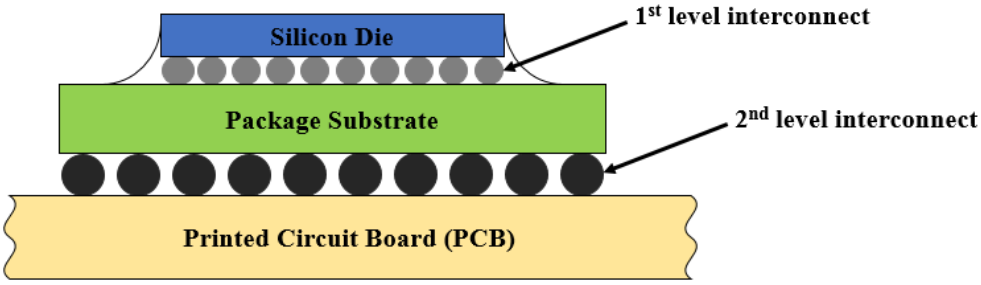
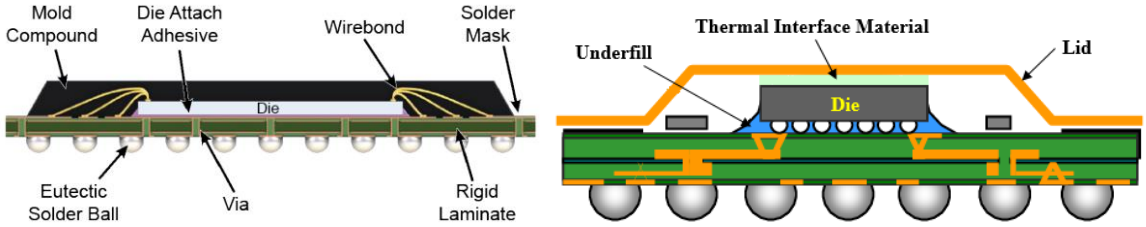


Figure 5 – Hierarchical interconnect level structure

First-level electrical routing from the silicon die is undertaken using either wire bond or flip-chip technology. The die being either "face-up" in case of wire bonding or "face-down or flip-chip" as illustrated in Figure 6 in order to make the attachment. For wire bonding, the back of the silicon die is bonded to the substrate using an epoxy resin. In the

case of flip-chip, epoxy adhesive underfill is applied at the first-level interconnection interface to improve the reliability performance of the solder bumps by distributing the strain. Also, the direct flip-chip-attachment to the substrate with the die "face down" can maintain smaller package outlines than the wire-bonding package as shown in Figure 6.



Ref: Amkor

Figure 6 – Second-level solder interconnects in wire-bond PBGA and FCBGA packages

Second-level interconnections at the substrate to the PCB interface comprises of either a solder ball or column. The difference between first-level and second-level interconnections is that, primarily, second-level solder balls have a higher diameter and placed at a higher pitch. In general, no underfill is present at the second-level to enable the repairability provision to remove/replace the package when necessary. The reliability of the first-level solder bump interconnect is influenced significantly by the uniformity of the solder ball and underfill distribution. The underfill between the silicon die and the package substrate increases the reliability of first-level solder bump interconnect tremendously in both thermal and vibration-induced cyclic forces. On the other hand, second-level solder ball interconnections experience higher levels of strain and they do not have underfill support. Hence, second-level interconnections are more susceptible to failures in thermal cycling dropping, bending, and warping. Therefore, there is a need for a non-destructive

inspection method especially for the evaluation of second-level solder ball interconnections.

1.2 Reliability of Microelectronic Packages

The adoption of flip-chip and BGA technologies has brought great success to the microelectronic industry. With these advances, however, there is a problem with the Coefficient of Thermal Expansion (CTE) mismatch. Because of the differences in materials used in the package assembly (die, substrate, PCB, etc.), and the high temperatures are needed to melt the solder, significant thermal strains are developed during the assembly. This can lead to crack initiation in the solder connections and eventually reduced device life. Besides, the increase in active component density leads to greater heating of the device during the field use and as a result, there is increased stress due to thermal loading. As IC technology advances, packages continue to shrink in size and as active component density increases, reliable solder connections become more difficult to achieve.

Reliability is usually defined as the ability of a product or a system to survive and to perform a required function, without failure or breakdown, for a specific envisaged period of time under the stated operation and maintenance conditions [10]. Consumers demand reliable, and long-lasting devices, and therefore the microelectronic packaging industry is following stringent reliability testing and failure analysis procedures. The industry aims to find failures and defects early in the manufacturing process so as to prevent premature device failures during usage.

Many prevalent processing defects and field failures (or service-induced failures) are related to the solder joint interconnections. Process-induced defects are referred to as

defects introduced during assembly. The common process-induced solder ball defects include cracked, head-in-pillow (HIP), open, poor-wetting, starved, misaligned, missing, and voids [1]. Oresjo conducted a fault-spectrum study of production data from 15 PCB assembly manufacturers with an inspection of over one billion solder joints [11]. Oresjo's fault spectrum of over one million defects is shown in Figure 7 [11]. The most dominant defects in this study are open solder joints (46% of all defects), followed by shorts (22%), and then insufficient solder joints (17%) [11].

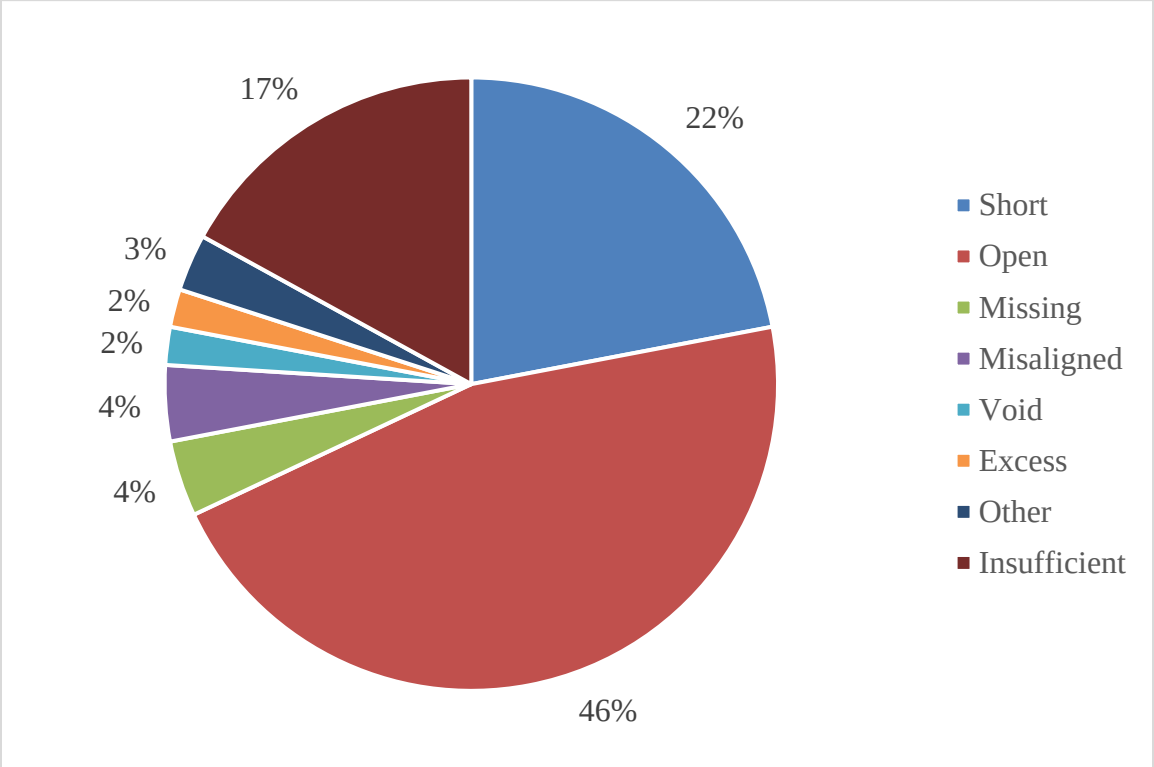


Figure 7 – Fault spectrum of over one million defects in solder joints [11]

An IC circuit generates heat during its operation. The fluctuations in the generated heat cause the microelectronic package to undergo high-temperature creep and thermal cycling fatigue etc. In addition, portable devices such as smartphones are subjected to

mechanical bend and drop conditions. These operating conditions are the main causes of service-induced failures or field failures in microelectronic packaging. The defects formed in the assembly process can act either as sources for catastrophic failures or as latent defects that can affect long term reliability of the microelectronic packaging. Tummala reported that thermal cycling and mechanical cycling fatigue of the microelectronic packaging, as the operating conditions result in 90% of all structural and electrical failures, especially in the solder interconnections [1]. The examples of service-induced failures include intermetallic cracking, solder cracking, pad cratering, laminate delamination, underfill delamination, etc.

Enterprises and researchers need to understand the life (time to failure), operating conditions to failure, and failure modes of the microelectronic packaging to improve the yield. However, in the real operating scenario, it takes a long time for the initiation and propagation of failure in the package. The industry cannot afford such a long time for the reliability testing between product design and release. Hence, the industry has adopted accelerated life testing, where the products are subjected to more severe use conditions to force them to fail more quickly. Accelerated Thermal Cycling (ATC) test is the most common thermal fatigue condition, and bend testing and drop testing are the most common mechanical conditions in Accelerated Life Testing (ALT). For the packages used in automotive or aerospace applications, vibration testing is another way to introduce failures.

1.2.1 Accelerated Thermal Cycling Testing

The integrity of the solder joint is very crucial to the reliability of the microelectronic packages during field-use conditions. During field-use conditions, the

microelectronic package is subjected to different temperature regimes either due to the heat generated from the functioning IC or due to exposed ambient temperature. As the microelectronic package is made of different materials having different CTE, exposure to different temperature regimes causes the solder joints connecting the package and the PCB board to undergo thermo-mechanical fatigue loading. The reliability of a solder joint under field-use for a solder joint is typically determined by subjecting the package to ATC testing characterized by increased ramp rates, dwell times, and temperature extremes. The life of the package, when subjected to ATC, can then be translated using an acceleration factor to the life of the package during field-use conditions.

In ATC, electronic packages are put into a thermal cycling chamber and subjected to thermal cycling. IPC9701A defined standards for temperature profiles for thermal cycling based on fields of applications [12]. According to IPC9701A, the preferred reference temperature profile is TC3 test condition: -40 °C ↔ +125 °C for the packages used in automobiles, aerospace, and computers [12]. The packages used in this dissertation, are subjected to TC3 test condition: -40 °C ↔ +125 °C with 15 minutes dwell at both high temperature and low temperature and 11°C/minute ramp rate.

However, ATC may not represent the realistic thermal distributions in microelectronic packaging. In ATC, the whole package along with PCB is almost at the uniform temperature with negligible thermal gradients within the package [13]. To address more realistic situations, a power cycling test is helpful. In the power cycling test, temperature distributions simulate the actual operational conditions by increasing and decreasing the temperature of the die by switching the power [13].

1.2.2 Mechanical Bend Testing

Mechanical bending is typically controlled by displacement. Three-point bending as shown in Figure 8 [14] and four-point bending as shown in Figure 9 are the common mechanical bend test setups. Controlled displacement is applied to the contacting head. During cyclic bending, solder balls are subject to cyclic strain and stress until the yielding point of the solder ball is reached. Then the solder ball crack initiates and propagates. Besides solder ball cracking, pad cratering is another typical failure mode during mechanical bending. Pad cratering refers to the initiation and propagation of fine cracks beneath the copper pads in the organic substrate materials or PCB laminates [15]. Resistance monitoring and strain monitoring are usually configured on the test boards to record the reliability data for failure analysis. In general, the four-point bend testing is preferred over the three-point bend testing because the constant moment is applied to the board in four-point bend testing.

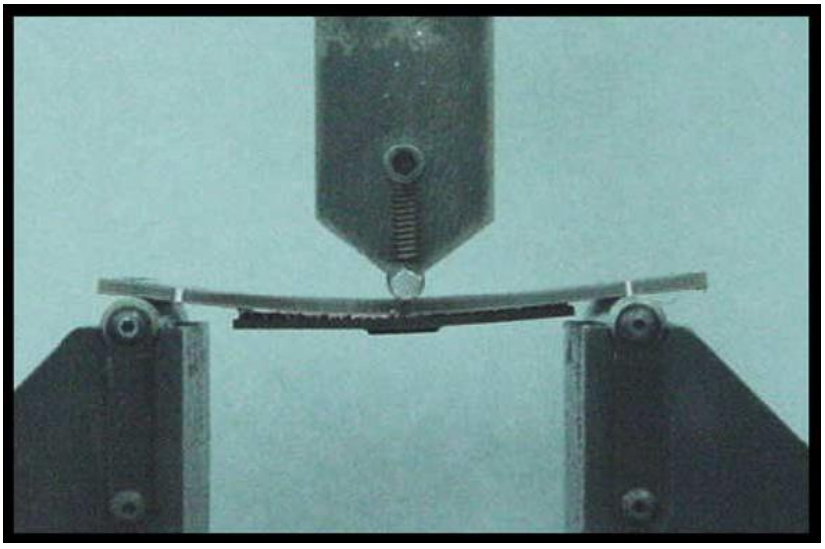
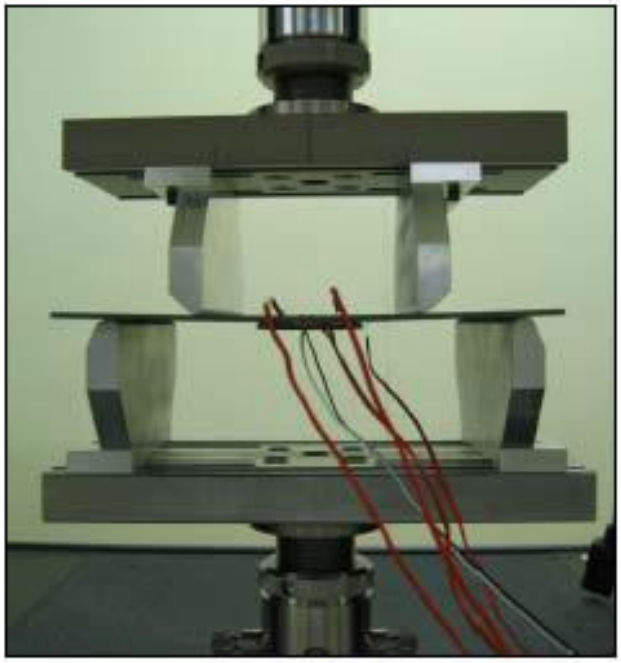


Figure 8 – Three-point bend testing setup [14]



Ref: Broadcom

Figure 9 – Four-point bend testing setup

1.2.3 Mechanical Drop Testing

Mechanical drop testing is typically controlled by acceleration. A schematic for the JEDEC board-level drop test along with the applied acceleration over time is shown in Figure 10. The test vehicle is mounted on the base plate with its corners fixed on the standoffs while the base plate is attached to the drop table. The drop table is released from a certain height to hit on the striking surface. An accelerometer is attached to the base plate to monitor the acceleration. In drop testing, solder ball failure is purely a brittle fracture. Whereas, in thermal cycling and mechanical bend cycling, the ductile fracture is the major phenomenon. There is almost no phase for crack propagation because of the transient shock in the drop testing. Drop testing plays a key role in product characterization of portable devices such as smartphones, laptops, etc.

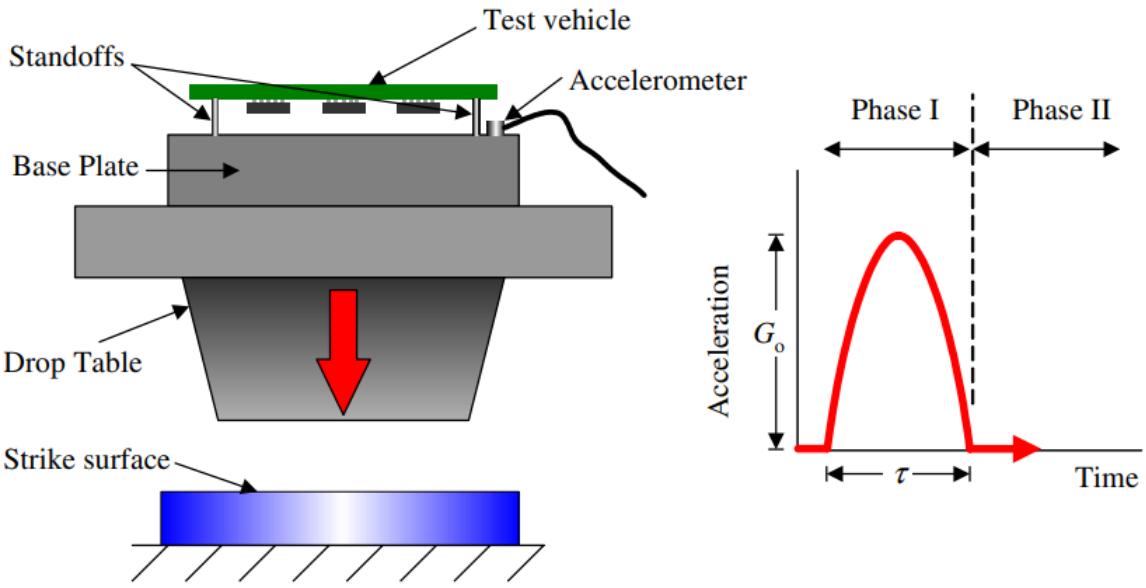


Figure 10 – Schematic for JEDEC board-level drop test [16]

1.2.4 Other Accelerated Life Testing

ALTs mainly help in understanding the physics of the expected or occurred failures in terms of failure modes and mechanisms [10]. Accelerated tests use elevated stress levels and/or higher stress-cycle frequency to hasten failures over a much shorter time frame. The stress does not necessarily have to be mechanical or thermo-mechanical, it can be electrical current or voltage, high (or low) temperature, high humidity, or any other factor responsible for the reliability of the device or the system [10]. For example, high humidity ALT is required for electronic packages with polymer encapsulation because of the susceptibility of the polymer material to water absorption. Moisture diffusing through the polymer can transport ions to the die surface and other interfaces, and trigger electrical current leakage, corrosion, and delamination [17].

Other common accelerated test conditions include high temperature (steady-state) soaking/storage/ baking/aging/ dwell, low-temperature storage, power cycling, thermal shock, thermal gradients, fatigue (crack initiation and propagation) tests, mechanical shock, sinusoidal vibration tests, random vibration tests, creep/stress-relaxation tests, voltage extremes, high humidity, and radiation [10]. In summary, ALTs play an important role in the evaluation, prediction, and assurance of the reliability of microelectronic packages.

1.3 Evaluation of Microelectronic Packages

The evaluation of microelectronic packages is performed in three stages, (i) during product and process development (pre-production) phase, (ii) during the production phase, and (iii) during the post-production phase or field use phase. The reliability testing explained in the previous section is part of the pre-production phase. The detailed failure analysis and root cause analysis are extremely important aspects in the pre-production phase and after the reliability testing of microelectronic packaging. The establishment of the causes of failures provides more information for improvements in design, materials, operating procedures, and the use of components. Therefore, at every stage of the pre-production phase, engineers adopt various destructive and non-destructive evaluation methods to inspect the quality of the product or the process. On the other hand, during production, manufacturers prefer non-destructive evaluations to ensure that the current process and the product are within the range of specified limits and that the evaluation is mostly based on pass/fail criteria. The evaluation in the post-production phase or the field is the product or issue-specific and it depends on the customer or manufacturer’s discretion.

The current trend in the electronic industry of making compact, miniature, high density, environment-friendly, and low-cost electronic devices, is driving the solder ball interconnection size and interconnections pitch to the lowest limits. As the ball size decreases, assembly defects are more likely to appear. Also, the smaller solder ball becomes less compliant, making it more susceptible to thermal and mechanical failures. Higher processing temperatures required for lead-free materials increase thermal stresses, which will increase the probability of solder balls to fail during manufacturing or in service and make the microelectronic package inoperable. The solder interconnections in advanced microelectronic packages are hard to evaluate for defects and failures when assembled to the PCB as they are hidden underneath the package. Consumers demand reliable, long-lived devices, and therefore device manufacturers have a great need for reliable inspection methods and tools to not only find solder joint faults as early in the manufacturing process as possible but also to detect defects to prevent premature device failure once the product has been sold. Hence, an inspection of solder ball interconnections has become a crucial process in the microelectronic packaging industry to ensure product quality and improve the yield. Currently, a combination of nondestructive testing and destructive testing is being used for the inspection of solder interconnect failures in microelectronic packages. Some of the major destructive and nondestructive inspection techniques are discussed in the following sections.

1.3.1 Destructive Inspection Techniques

Destructive techniques require modification of the specimen to reveal internal structures and analyze the failure site. Two destructive techniques, that are predominant across the microelectronic packaging industry, are (i) cross-sectioning and microscopy, and

(ii) dye-and-pry testing. Destructive techniques are still the foremost choice for failure analysis and root cause analysis because of the high-resolution visual image of the specimen of interest. However, destructive techniques are tedious, and there is a possibility of missing the correct section or region of interest in cross-sectioning or prying. Also, with destructive techniques, the study of failure evolution is not possible as the test sample can be used only once before its destruction.

1.3.1.1 Cross-sectioning and Microscopy

Cross-sectioning of a test sample involves physical cutting of the sample with an abrasive tool, encapsulating in an epoxy resin, and subjecting the encapsulated sample to a series of grinding steps from coarse to very fine, by targeting features of interest. Once the target location such as the center of the solder joint is reached, intermediate and final polishing steps are used to bring the surface to a sub-micron finish. Finally, chemical etching brings out the detail of the cross-section layer structure which is ready for inspection under the microscope. Optical microscopy and Scanning Electron Microscopy (SEM) are generally used to capture the high-resolution images of the cross-sectioned sample for the manual image analysis. The sample image from optical microscopy is shown in Figure 11 and the sample of high-resolution SEM image is shown in Figure 12.

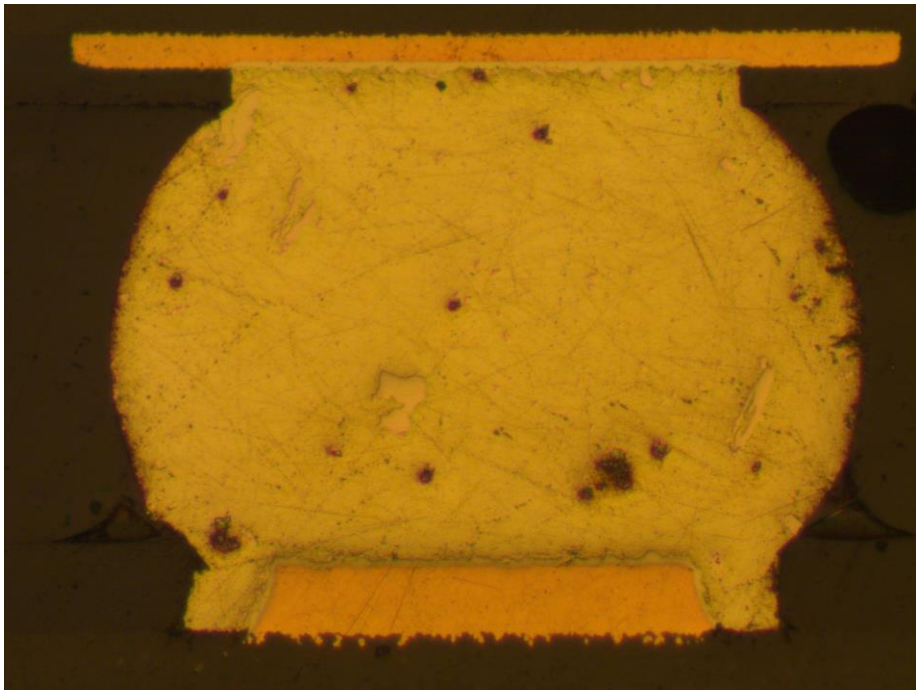


Figure 11 – Sample image of BGA solder ball from optical microscopy

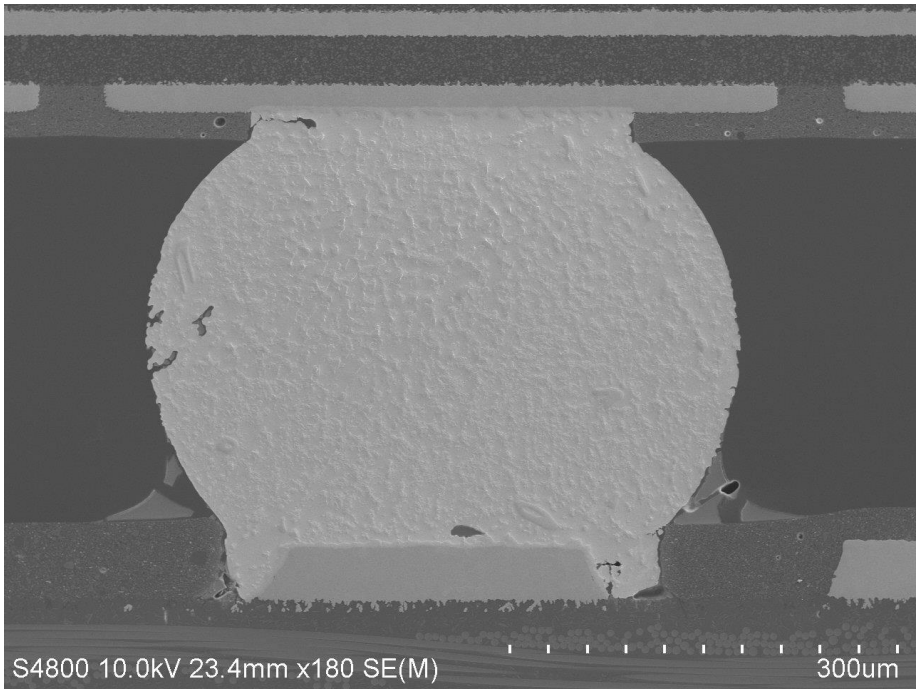


Figure 12 – Sample image of BGA solder ball from Scanning Electron Microscopy (SEM)

1.3.1.2 Dye-and-Pry Testing

Dye-and-pry testing is a destructive analysis technique used on SMT components to either perform failure analysis or inspect for solder joint integrity. It allows all solder joints in the array to be tested simultaneously. In the dye-and-pry testing, initially, the component of interest is submerged in a dye material, such as red steel dye, and placed under vacuum. This allows the dye to flow underneath the component and into any cracks or defects. The dye is then dried in an oven to prevent smearing during separation, which could lead to false results. The part of interest is mechanically separated from the PCB and inspected for the presence of dye. Any fracture surface or interface will have dye present, indicating the presence of cracks or open circuits as shown in Figure 13.

Figure 13 – Sample image from dye-and-pry testing

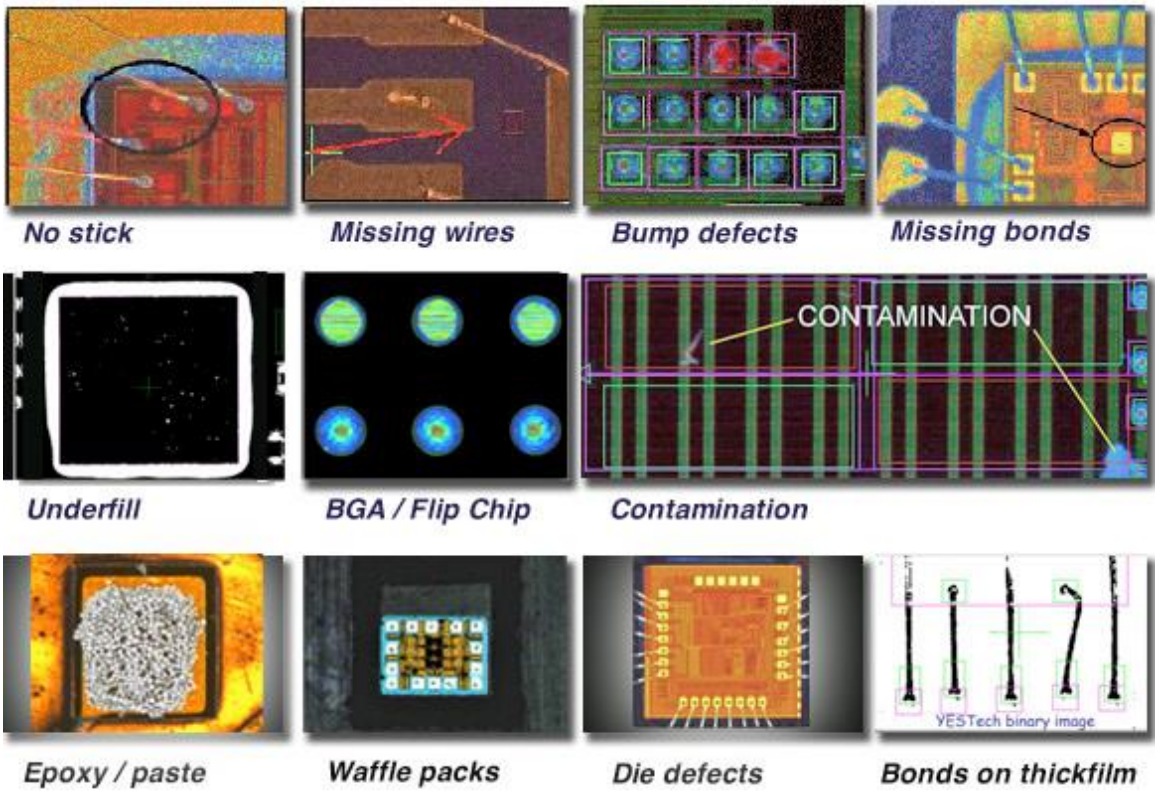
1.3.2 Non-destructive Inspection Techniques

Non-destructive inspection techniques are preferred for inspection and failure analysis of microelectronic packages as these techniques can preserve the test samples and reduce the overall effort from destructive techniques. Most used non-destructive techniques for identification of board-level defects or failures are, (i) optical inspection, (ii) electrical inspection, (iii) X-ray inspection, and (iv) acoustic inspection. While many of these techniques and systems are suitable for specific inspection tasks, they do not necessarily encompass all the capabilities required for evaluating the quality of the overall assembly.

1.3.2.1 Optical Inspection

A basic optical inspection system consists of an illumination source to light up the object, a camera to record the reflected light from the object, and an image processor that produces a recognizable image. Subsequently, the image can either be compared with a previously recorded good image to find the difference, or it can be interpreted using image processing and pattern recognition techniques. Automated Optical Inspection (AOI) is commonly used in the SMT manufacturing process at many stages including bare board inspection, Solder Paste Inspection (SPI), pre-reflow, and post-reflow, etc. AOI systems can inspect for most types of defects such as component placement, solder shorts, missing solder, etc. after solder reflow or "post-production. Typical defects that can be identified by an AOI system (Nordson YESTECH's M2) are shown in Figure 14. However, AOI is limited by the need to have a direct line of sight to the solder joint under examination and therefore cannot be used with flip-chip and BGA type packages. Industrial endoscopy is a

method that has been tried for inspecting solder joints in area-array microelectronic packages; however, this is only useful for peripheral solder balls. As such, optical inspection is of limited use in the inspection of flip-chip solder bumps and BGA solder balls.



Ref: Nordson YESTECH

Figure 14 – Defect classification identified by a typical AOI system

1.3.2.2 Electrical Inspection

Electrical resistance measurement is a widely used non-destructive technique in the industry to find electrical faults in the daisy-chain. At the basic level, electrical inspection involves electrically probing the test package and measuring the response. The response

for a particular stimulus is compared to the expected range of responses and any package with a response outside this range is deemed defective.

An electrical inspection can be classified into two major methods: functional testing and in-circuit testing. Functional testing is characterized by exercising the circuit to drive all possible functions performed under all possible environmental conditions, and finally, assess the circuit if it performed all the intended functions successfully [1]. The limitation of this form of testing is that normally the failure site and mode cannot be determined. Moreover, defects that can shorten the life of the device, but do not render it immediately inoperable (such as small cracks) cannot be detected by this method.

In-circuit testing or bed-of-nails testing evaluates the test package from a circuit perspective rather than an operational one. As shown in Figure 15, the test setup consists of a fixture with top and bottom plates that are equipped with test probes or bed-of-nails. These test probes make contact with conductive test pads on the substrate, which are electrically connected to different parts of the circuit. A stimulus is applied from the nails and the response measured, usually in the form of resistance or capacitance. This is compared to the expected range of values and a pass or fail assigned. The advantage of in-circuit testing is that the circuit of the test package can be broken down into smaller subdivisions which can be tested independently to isolate the region where the defect resides. The disadvantages of in-circuit testing are that the test pads can use a significant amount of board space, and that failure modes such as poor wetting and bridging cannot be detected. The electrical inspection is also incapable of recording failure evolution.

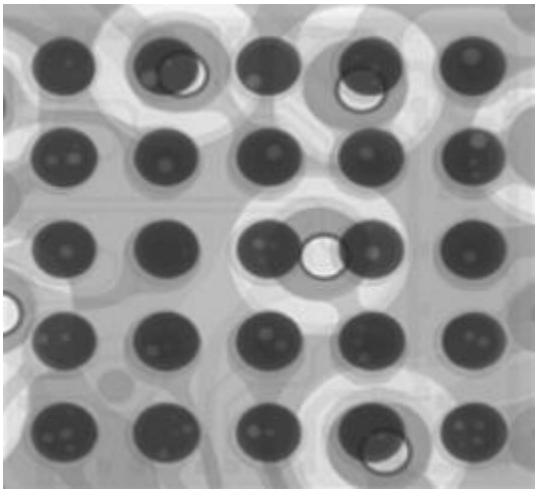
Ref: SPEA

Figure 15 – Bed-of-Nails tester

1.3.2.3 X-ray Inspection

X-rays have been used for non-invasive high-resolution imaging of industrial and biological specimens since their discovery in 1895. X-ray inspection is useful in industrial settings, in both the pre-production and production phase (in-line). X-rays are generated by accelerating electrons across a high voltage to collide with an anode composed of a high atomic number, and high melting point material such as tungsten. A typical X-ray inspection system usually has an X-ray source, an X-ray collector to receive the penetrated radiation, and a camera to convert the photons on the collector to a digital form and imaging interpretation software. The different materials in the sample under X-ray exposure absorb different amounts of X-rays. This leads to an image of the sample showing the absorption pattern being produced. X-ray inspection methods are divided into three modalities: 2D X-ray radiography, 2.5D (tiled view mode), and 3D mode (laminography, tomography, etc.).

Most commercially available 2D X-ray inspection systems use radiography. The sample under inspection is placed between stationary x-ray source and detector to produce a 2D grayscale absorption image for the sample as a whole without regard to spatial details along the source to detector axis. An example of a 2D X-ray image showing voids in a Micro BGA package is shown in Figure 16.

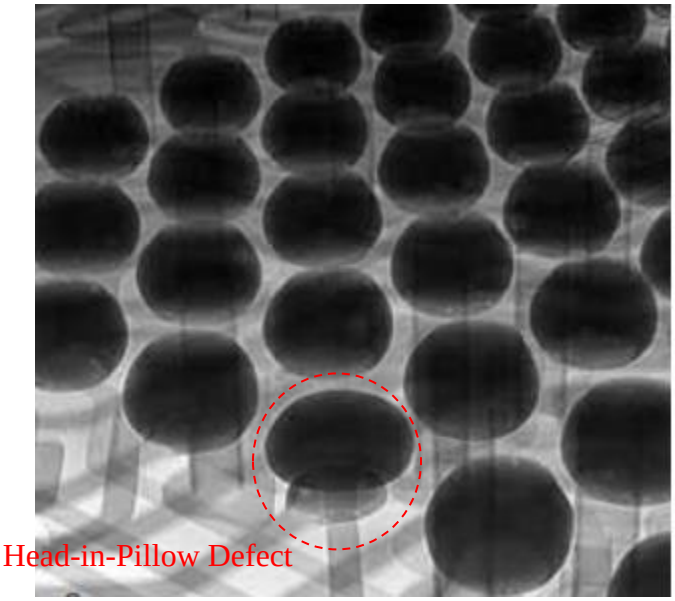


Ref: Nordson Dage

Figure 16 – 2D X-ray image of micro BGA package showing voids in the solder balls

2D X-ray radiography has been successfully used in detecting the presence of voids, solder bridges, missing solder balls, solder ball misalignment, and missing or broken internal connections. One of the main disadvantages of 2D X-ray radiography is that it's very difficult to interpret the images from multilayered or double-sided boards because other components on the board can absorb the X-rays thus casting a shadow over the point of interest. Also, depending on the orientation of cracks in the solder balls, the cracks can remain invisible to 2D radiography because the amount of material that is absorbing the x-rays does not change.

Most of the modern 2D X-ray inspection systems have additional features to tilt the X-ray head to capture tilted or angled views along with straight top-down views. This is called 2.5D mode inspection, which is a compromise between the 2D X-ray image and 3D X-ray image. Tilting can help to get a better view if components are obscuring the area of interest. The 2.5D image is especially useful to find major cracks and defects such as head-in-pillow without the need for complex and time-consuming Computed Tomography (CT) scans. An example of a 2.5D X-ray image showing head-in-pillow in a BGA package is shown in Figure 17.



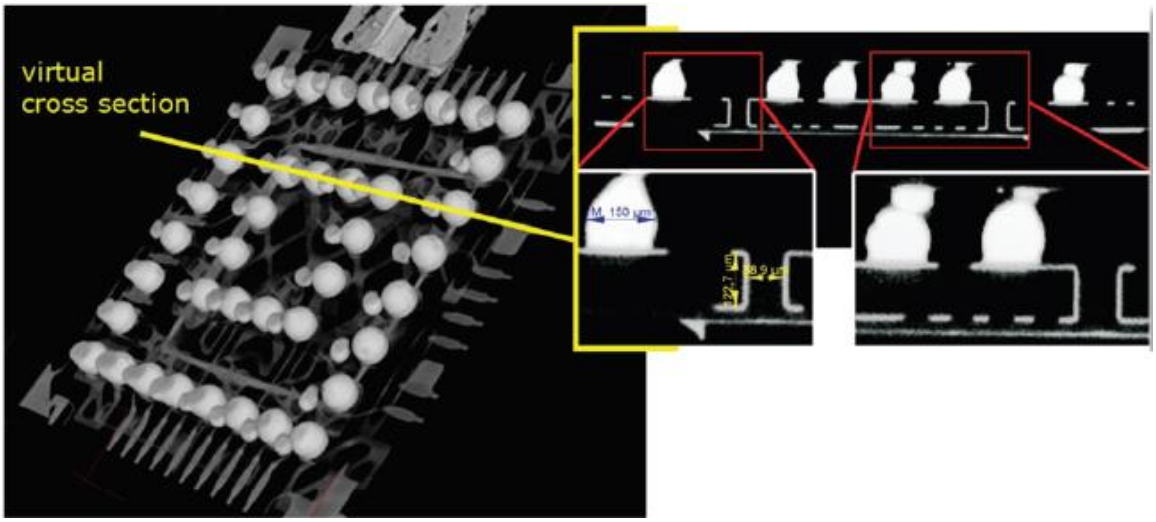
Ref: Yxlon

Figure 17 – 2.5D X-ray (titled view) image of BGA solder balls showing the head-in-pillow defect

X-ray laminography and X-ray tomography are popular 3D X-ray techniques. In X-ray laminography, the X-ray beam is focused on one plane at a time and slices the specimen horizontally. The X-ray source and the detector are moved synchronously in opposite directions. Due to that correlated motion, the vertical location of the focus plane

can also move within the sample, so it can create a 3D image. X-ray laminography is a natural extension of radiography that can give the depth as well as the X-Y position of defects/failures. However, its spatial resolution is limited because it requires high X-ray flux for rapid pass/fail solder ball inspection, and the equipment and operation costs of these systems are high [19]. It is also considered unsuitable for online applications because of its low throughput.

X-ray tomography generates a 3-D image by reconstruction from a sequence of images which are taken when the Device Under Inspection (DUI) rotates between the X-ray source and detector. The result is a 3D image that can be virtually cross-sectioned to reveal any defects/failures as shown in Figure 18 [20].



[20]

Figure 18 – 3D X-ray Computed Tomography (CT) image with virtual cross-section

X-ray tomography is a very powerful technique that is theoretically capable of inspecting all types of solder joint/solder bump defects/failures. Practically, sometimes it can be very difficult to interpret the images. Due to the necessity to rotate the sample during

the inspection process, it is difficult to inspect large and/or complex boards. Additionally, because of the time required for data acquisition and processing, it is considered unsuitable for online applications. Advances in computer processing power and image reconstruction techniques have been helping to alleviate these impediments to a degree. However, initial investment and operational costs for X-ray tomography systems remain prohibitive [19].

1.3.2.4 Acoustic Inspection

Acoustic techniques are widely used in the microelectronics industry for inspecting defects, such as voids, cracks, and interfacial delaminations in electronic packages in a non-invasive, fast, and reliable way. The acoustic imaging is generated based on ultrasound waves. A high-frequency ultrasonic pulse is generated by employing a piezoelectric transducer. As shown in Figure 19, the working principle of acoustic microscopy is that the propagation and reflection of the acoustic waves will be altered at the interface of two materials with different acoustic impedances (e.g. substrate to solder bump, solder bump to air, etc.). Depending on the operating mode, either the reflected or transmitted signal is detected by the same or another transducer. Then, the received signal information is converted into a grayscale image to delineate the internal structure of the DUI. Water acts as a couplant to propagate the acoustic energy from the transducer to the DUI.

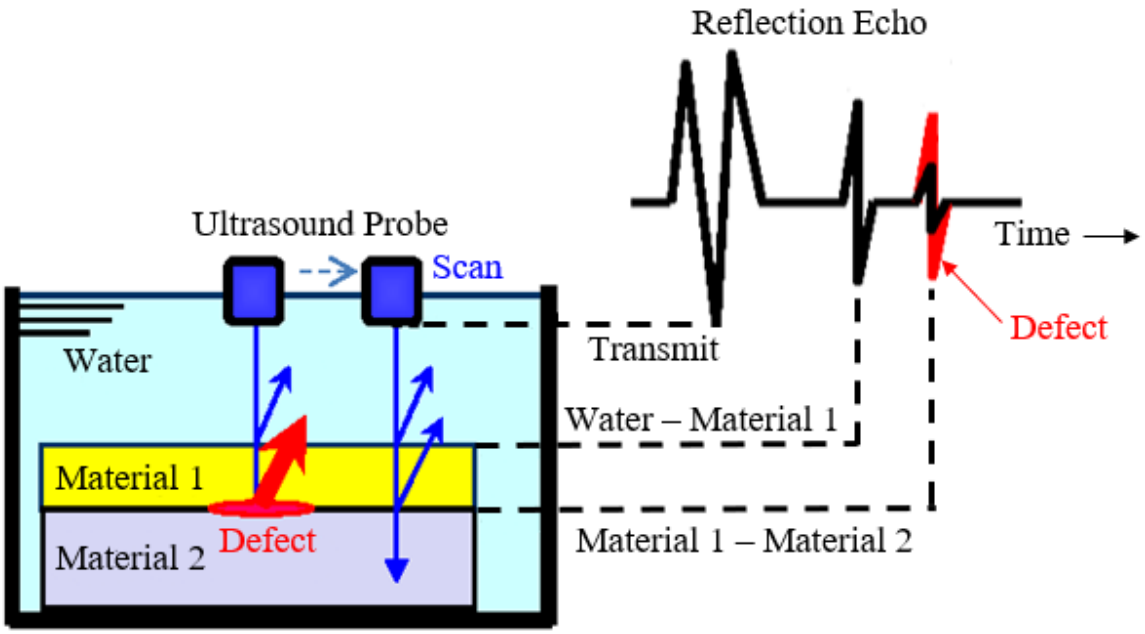


Figure 19 – Scanning acoustic microscopy principle of generating inspection image

C-mode Scanning Acoustic Microscopy (CSAM) with the pulse-echo method is commonly used acoustic technique in which the ultrasonic point source is moved across the surface of a sample while the reflected wave is captured at a specific depth region in the packages. When there is a flaw, it reflects a different echo whose amplitude is proportional to the difference in acoustic impedances between the flaws and surrounding medium. The typical reflection waveform in the time-domain is shown in Figure 19. The typical operating ultrasound frequencies range for CSAM is from 10 MHz to 2 GHz. The acoustic impedance of air increases with the frequency of the ultrasound; above ~10 MHz the acoustic impedance is such that the ultrasounds cannot propagate. Hence, acoustic microscopy is very sensitive to air pockets and it can detect cracks, voids, and interfacial delaminations effectively. An example of the CSAM image showing underfill delamination from the silicon die surface is shown in Figure 20 [21].

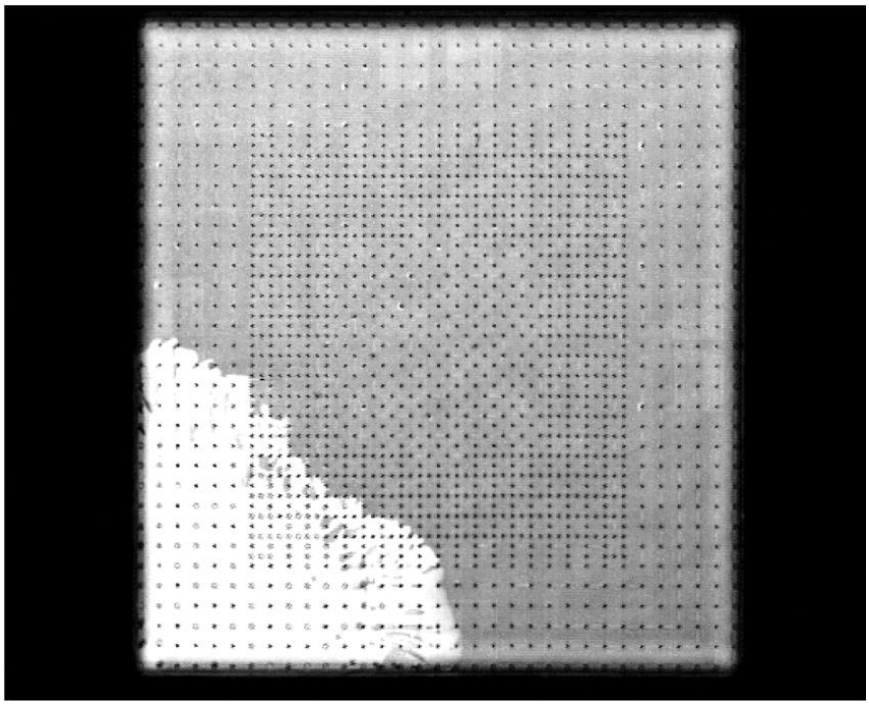


Figure 20 – CSAM image of a BGA package showing underfill delamination at the left-bottom corner (white spots) [21]

Another mode of acoustic microscopy is Through-Transmission Scanning Acoustic Microscopy (TSAM), in which, an ultrasound wave is transmitted through the entire package. A separate receiver at the other end of the package detects the transmitted ultrasound. Imaging is based on the absorption of ultrasound as it passes through the package. TSAM is relatively easy to set up, however it provides less spatial resolution than CSAM and it does not provide depth information about the defect. TSAM is normally used to verify CSAM results.

However, SAM has many limitations. The length of the pulse prevents focusing the beam on thin layers. A coupling medium (usually deionized water) is always required to propagate acoustic energy from a piezoelectric transducer to the specimen. Additionally,

effects such as frequency downshifting can significantly reduce the detection resolution [22]. SAM has limited use for the inspection of solder joints in thick packages. Higher frequency ultrasounds are attenuated more rapidly than lower frequency. This leads to a decrease in resolution as the signal propagates deep into the DUI. Consequently, the defects deep within the DUI might not be detected. Additionally, the orientation of the defect can impact its detectability. For example, a crack that runs perpendicular to the transducer axis might be able to be detected while the same size crack running parallel to the axis might be completely missed. As such, SAM of BGA packages is limited to detection of failures isolated in the upper regions of the package such as popcorn failures [24] and die interfacial delamination [25]. Edge effects also cause a decrease in measurement resolution along the edges.

In summary, although there are several techniques available for inspecting solder joints interconnections in microelectronic packages, they have their respective advantages and disadvantages. With new advanced package formats emerging, the microelectronic packaging industry demands more stringent requirements for a noncontact, nondestructive, high-speed, and low-cost technique for solder ball interconnections. Therefore, research continues aiming to develop new techniques to satisfy the inspection requirements of microelectronic packaging.

1.4 Motivation and Objectives

As discussed in previous sections, the microelectronic chip package design is continuing to evolve with the increased number of interconnections to the PCB to keep up with electronics miniaturization trends. These connections in advanced electronic chip

packages are hard to evaluate for defects and failures as the interconnections are underneath the package, especially for area-array configuration. While current non-destructive inspections such as electrical testing, X-ray, and acoustic microscopy are used to evaluate package connections, they have limitations on resolution and penetration depth, which make them difficult to identify defects or failures in interconnections, and also they have long processing times [19]. Destructive techniques result in the loss of the device, and such loss of devices is expensive for some of the defense and high-performance applications. As these inspections are used during product development to understand the failure modes and during production to control product quality, buyers and users gain limited confidence that potential defects and failures will be captured before products are shipped to customers.

The microelectronic packaging industry has an unfulfilled need for reliable non-destructive techniques for inspecting microelectronic package assemblies. As a disruptive innovation in the SMT chip packaging inspection industry, this dissertation serves as a building block to develop DALUS which will provide non-destructive, non-contact, fast, low-cost, highly sensitive, and offline, as well as inline inspection for advanced microelectronic chip package connections. By analyzing the microelectronic package vibration signature using an array of pulsed lasers, DALUS automatically identifies and precisely locates the defects and failures in various levels of solder interconnections. It identifies precise defect and failure locations as well as defect/failure severity within seconds.

The objectives of this dissertation are:

- To develop a non-contact, non-destructive, accurate, and high sensitivity Dual-Fiber Array Laser Ultrasonic System (DALUS) for inspecting and assessing area-array microelectronic packages in terms of defects and failures.
- To tune and calibrate the system to produce high strength ultrasound signals, and to attain a high signal-to-noise ratio for improved sensitivity to identify micro-sized defects and failures.
- To employ the system to evaluate different size industrial microelectronic packages subjected to mechanical bend testing, drop testing, and thermal cycling tests.
- To realize the commercial scope utility of the system to identify the defects and failures during assembly process development, reliability testing, and in-line quality evaluation in the microelectronic packaging industry.

1.5 Dissertation Outline

This dissertation is organized into 10 chapters as discussed below.

Chapter 1 presents an introduction to microelectronic packages, their evolution, and current trends. Different ALTs for the reliability assessment of microelectronic packages have been presented. Current destructive and nondestructive inspection methods for the evaluation of solder ball interconnections are reviewed along with their limitations. Afterward, the motivation and research objectives for this work are described.

Chapter 2 presents the background research and literature review relevant to this work, including the Laser Ultrasonic Inspection (LUI) principle, the methodology of LUI, fiber-array laser ultrasound, and Finite-Element (FE) analysis.

Chapter 3 examines the makeup of the basic LUI system as a whole and then describes each of the constituent parts in more detail. The limitations of Single Laser Ultrasonic System (SLUS) are also discussed.

Chapter 4 describes the development of the Dual-Fiber Array Laser Ultrasonic System (DALUS), related major system improvements, and additional safety features implemented on the system. The need for DALUS and the advantages of DALUS are also briefed in this chapter.

Chapter 5 discusses the technical and performance capabilities of DALUS to use for area-array microelectronic packages. The throughput and resolution of DALUS are defined based on experimental data.

In Chapter 6, experimental details and results using DALUS on large Flip-Chip Ball-Grid Array (FCBGA) packages subjected to mechanical testing (four-point bend testing and drop testing) are presented. Validation of DALUS results with cross-sectioning results and finite-element simulations are also discussed.

Chapter 7 explains the DALUS experimental results and validations using additional industrial FCBGA packages subjected to thermal cycling.

In Chapter 8, a correlation is established between DALUS results from the FCBGA packages subjected to thermal cycling and damage metrics (accumulated inelastic strain

per thermal cycle and accumulated inelastic work density per thermal cycle) from finite-element simulations. This correlation is important to predict the DALUS results in advance by performing finite-element simulations on a given package.

Chapter 9 is especially important to demonstrate the repeatability and reproducibility of the developed system and algorithm. In this chapter, the measurement capability of the DALUS as per industrial standards is explained using gage repeatability and reproducibility analysis.

Chapter 10 summarizes the work presented in this dissertation, lists the research contributions, and provides the scope for potential future research.

CHAPTER 2. BACKGROUND AND LITERATURE REVIEW

2.1 Innovative Inspection Techniques

Current nondestructive inspection techniques have significant limitations in identifying defects/failures in solder ball interconnections and meeting the industry demands. These limitations have led to an increased demand for reliable and robust inspection methods to meet the industry requirements. Several research studies have focused on developing non-destructive methods for testing and inspection of advanced microelectronic packaging. A detailed review of different non-destructive inspection techniques for microelectronic packages was presented by Aryan et al. [19]. Some of the innovative and competitive techniques are as follows.

X-ray Computed Tomography (CT) is gaining popularity at a rapid rate in the inspection of microelectronic packaging especially because of the recent advancements in machine learning methods based on artificial neural networks. Image processing based on Artificial Intelligence (AI) made it possible for accurate, high speed, automated X-ray inspection. Companies like Nordson, Nikon, Yxlon, etc. are investing heavily in developing high resolution and high-speed 3D X-ray CT. In a recent study on high-resolution X-ray CT, Oppermann et al. described that X-ray CT is not easy to use evaluation technology [20]. X-ray CT equipment is expensive, and it needs a lot of experience to get high-quality CTs [20]. Another major limitation with high powered 3D X-rays is that sensitive parts such as non-volatile memory parts that are also mounted on a board along with parts that need to be inspected are being failed because of unwanted X-ray exposure.

Research is underway for improved X-ray methods such as X-ray microlaminography and X-ray microscopy to meet industry demands for higher accuracy and resolution. Sassov et al. developed digital microlaminography, using digital algorithms to reconstruct individual layers from a set of microlaminography X-ray measurements [25]. It is possible to analyze distinct layers of flat objects with a specific depth resolution of micron using X-ray microlaminography and laminography [25].

Infrared Thermography (IRT) is used successfully to inspect flip-chips, solder joint defects, edge defects, misalignment of solder bumps, silicon crack, underfill void, delamination, and subsurface defects (up to 4 mm in depth) [19]. Both active and passive thermography methods are available for IRT inspection. The passive method relies on natural heat emitted from the structural components. On the other hand, in the active method, additional external heat is exerted to create thermal waves on the surface of the specimen. The active thermography methods have been adopted extensively to inspect the microelectronic packaging. Infrared detectors sense the thermal radiation for the analysis of the defects. Chai et al. demonstrated solder joint defect detection in the flip-chip package using active transient thermography at a wavelength range of 8 to 14 um [26].

The Magnetic Current Imaging (MCI) inspection method operates based on measurements of the magnetic field associated with a flowing current. In this method, hidden current-carrying components are mapped out by measuring the magnetic fields around them. The magnetic field images are converted into the current density images using Fourier transform inversion [27]. To locate the defect, the current density images are compared with defect-free samples. MCI method has been mostly successful for inspecting short circuit faults within electronic packaging [19].

Infrared Microscopy (IRM) is used for device images with a spatial resolution of 2–3 μm. IRM denotes microscopy achieved at infrared wavelengths of 2 μm to 14 μm. For flip-chip packages, the advantage of the IRM is that most silicon materials are transparent at wavelengths greater than 1 μm [19]. Hence, defects such as voids, delamination cracks, and corrosion can be investigated while the chip is mounted on the substrate [19]. Trigg published applications of IRM to IC and MEMS packaging [28]. However, this method is limited to samples with a thickness range of up to 10μm [28].

Time Domain Reflectometry (TDR) can successfully detect defects in solder interconnects and open failures in 3D packaging inspection [19]. The TDR inspection method operates by sending an electrical pulse and detecting reflections returning from impedance discontinuities along the controlled-impedance transmission path. TDR method has been used successfully by Cao et al., to detect cracks in flip-chips [29].

Our research explores the development and capabilities of a novel non-destructive testing method using laser ultrasonics. The overall objective of this research is to develop a non-contact, nondestructive, automated, accurate, high-sensitive, and low-cost DALUS for evaluating the quality of solder ball interconnections in area-array microelectronic packages. The non-destructive inspection system under this development aims to provide a solution that can overcome some of the limitations of current nondestructive inspection techniques. This system is expected to be used in-line during the assembly process (production phase) or off-line during process development and failure analysis (pre-production phase).

2.2 LUI Principle & Methodology

2.2.1 Laser Ultrasound Generation

In the LUI technique, ultrasound is generated inside the test sample by localized heating of sample surface with pulsed lasers. Unlike traditional contact piezoelectric transducers (PZTs), pulsed lasers do not require couplant. This makes laser ultrasound non-contact and suitable for automated inspection. Depending on the laser energy density, there are two regimes of laser-generated ultrasound: thermoelastic regime and ablation regime [30]. When the incident energy density on the incident area is relatively low and the local temperature is below the melting point of the material, ultrasound is generated through the thermoelastic mechanism. If the local temperature rises very rapidly and higher than the melting point of the incident surface materials, local vaporization and ejection of small particles occur. This phenomenon is called ablation, and it can be used for cutting and cleaning in industrial processes [30]. To avoid any surface damage to the microelectronic package components under inspection in the non-destructive laser ultrasound inspection system, the laser power is controlled within the thermoelastic regime.

A schematic of the ultrasound generation is shown in Figure 21. The localized heating produced by the pulsed laser generates thermal expansion and thermoelastic stresses in the sub-surface region of the sample. Thermoelastic stresses, in turn, generate ultrasonic elastic waves that propagate deep within the sample as bulk waves (longitudinal waves + shear waves + surface waves) [30]. Bulk ultrasound propagation and reflections from the interfaces within a package are dependent on the material properties and internal structure of the package, including defects, solder ball joints, etc. Therefore, the propagation of bulk ultrasound produces signature transient out-of-plane displacement (or vibrations) on the surface of the sample. A laser interferometer is used to measure these

transient out-of-plane displacements at different locations on the surface of the sample to record the signature signal at various locations.

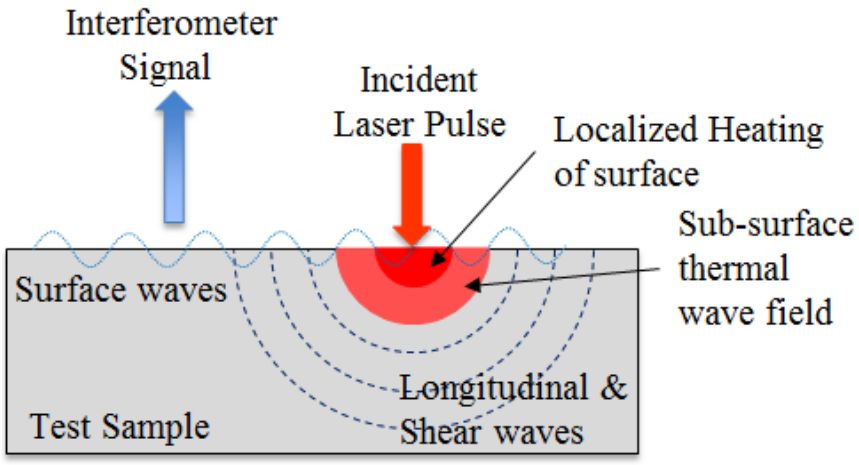


Figure 21 – Schematic diagram showing the principle of ultrasonic generation and signal acquisition

2.2.2 Signal Acquisition

The fiber-optic laser interferometer and doppler vibrometer are used to measure the out-of-plane surface displacement response at selected Data-Collection-Points (DCPs). Since the amplitude of the ultrasound generated in the thermoelastic regime will be in the nano-scale displacement range, the interferometric technique is preferred due to its high measurement resolution. Illustration of a heterodyne Michelson optic fiber interferometer for ultrasound detection is shown in Figure 22. The heterodyne interferometer is a two-beam interferometer with a reference arm and an object arm reflected from the object. The two beams to be mixed having slightly different optical frequencies. Typically, this is obtained by passing a laser beam through an acousto-optic modulator (Bragg cell). The frequency-shifted beam (of frequency $\Omega + \omega B$) will be refracted at a different angle and

will serve as the reference arm. The unaltered beam (of frequency Ω) will be the object beam. Both beams pass through a beam-splitter and are collected by the optical detector. The heterodyne interferometer has a broad detection bandwidth and good immunity to ambient vibrations. The optic fiber interferometer also adds flexibility in configuring the system [31][32].

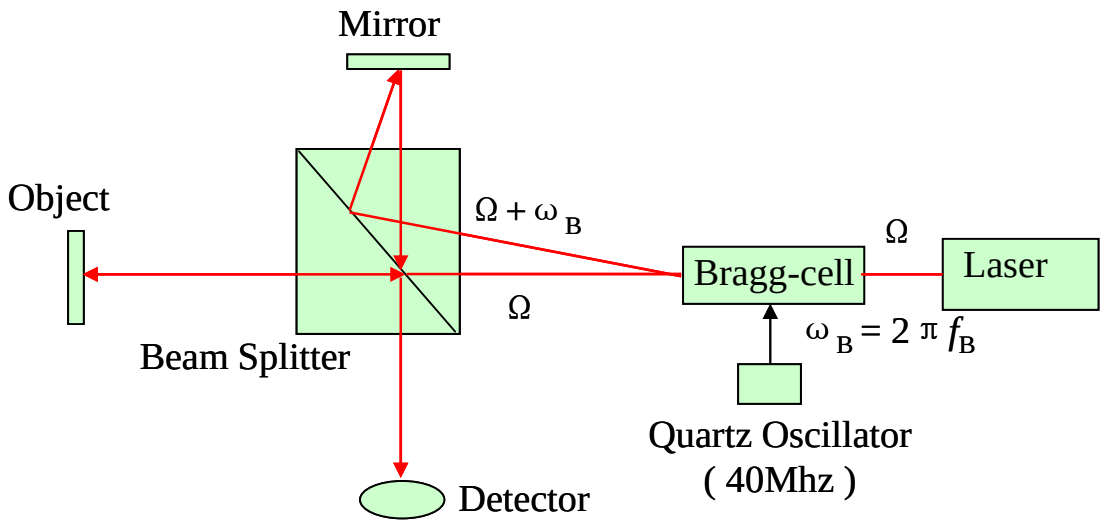


Figure 22 – Schematic of a heterodyne interferometer

The interferometer sensor head is positioned in an area perpendicular to the sample surface at 55 mm. The sensor head has a laser spot size of 3 μm. The vibrometer has a displacement measurement resolution of 0.1 nm and bandwidth from 25 kHz to 20 MHz. For a single DCP, multiple interferometer signal measurements are acquired at consecutive laser pulses and averaged to increase the signal to noise ratio. The analog output signal of the vibrometer is internally low-pass filtered with a cutoff frequency of 2 MHz and is sampled at 25 MHz. Vibration data is typically acquired for 160 seconds at each laser firing

with a sampling rate of 50 x 10^6 samples/second. The vibration of the package normally dies out completely by the end of each acquisition period.

2.2.3 Signal Analysis

The principle of detection of a defect in the LUI technique is to compare the transient out-of-plane displacement response of a known good reference package to that of the test package that is being inspected. Any anomaly in the vicinity of a DCP in the test package will produce a displacement response different from that of the response at the same DCP in the reference sample with no anomaly. Minor differences in the displacement response may arise from measurement instruments or environmental variations, although there are no considerable defects/failures in the sample. The reference board is considered as a gold standard sample (known good sample). If a known good sample is not available, a hybrid reference model [33] can be developed using a large sample set of 15 – 20 samples, where the assumption is made that the sample set contains several defect-free samples.

To quantify the differences in displacement responses and to estimate the defects/failures, a Modified Correlation Coefficient (MCC) was used to analyze the interferometer signals [34]. The MCC is given by Equation (1), as a correlation between the signals from the test sample and the reference sample at a DCP.

$$MCC = 1 - \left(\frac{\sum_n (R_n - \bar{R})(A_n - \bar{A})}{\sqrt{(\sum_n (R_n - \bar{R})^2)(\sum (A_n - \bar{A})^2)}} \right)^2 \quad (1)$$

$$where \begin{cases} R_n : Reference\ signal & \bar{R} : Mean\ of\ R_n \\ A_n : Test\ sample\ signal & \bar{A} : Mean\ of\ A_n \\ n : \#of\ sampling\ points\ of\ the\ signal \end{cases}$$

From Equation (1), MCC values range between 0 and 1. An MCC value of 0 indicates that the test signal and the reference signal match perfectly, indicating that there is no anomaly or defect. The closer the MCC value to zero (“0”), the more the correlation between the two signals. This means that the chip package being tested is good. Similarly, an MCC value above a certain threshold value indicates there is an anomaly at the DCP. An MCC value equal to 1 indicates that the signals are completely dissimilar. This means that the chip package being tested is grossly defective. The major cause of the difference in the signals is the presence of anomalies and abnormalities in the solder bumps/balls, vias, substrate or die. The reasons why the MCC values are never exactly zero even between two good chip packages are (i) variations in positioning the interferometer due to the finite accuracy of the positioning stages, (ii) minor fluctuations in the laser power, and (iii) most notably manufacturing variations inherent in all chip packages.

2.3 Background LUI Research Studies

LUI is a novel technique that has achieved great success in identifying solder interconnect defects/failures in chip-scale and ball-grid array packages. LUI system has seen plenty of improvements over the past decade. Several research articles have been published on the LUI technique. S. Liu et al., [35] and T. Howard et al., [36] developed initial laser ultrasound and laser interferometric system for the inspection of flip-chip solder bumps. S. Liu et al., [37][38] explained digital signal processing methods used in the LUI technique. Yang et al. developed a wavelet analysis and local temporal coherence analysis methods [39][40]. Wavelet analysis decomposes the time-domain signal into a series of wavelet components based on a specific frequency band and allows identification of local features from the scale of wavelets [39]. Local temporal coherence is a measure of

time-dependent shape differences between two signals and it emphasizes the short-time coherence between signals [40]. L. Zhang et al., [34][41] introduced the correlation coefficient as an effective measure to estimate LUI results. J. Yang et al., [42] and J. Gong et al., [43][44] demonstrated the use of LUI for evaluating solder joint quality in land grid array packages and ball grid array packages respectively. L. Yang et al., [45] studied the fundamentals of flip-chip and FCBGA's response under laser excitation in the LUI technique.

All these studies were conducted on prototype test vehicles that have simple physical configurations. To test modern electronic packaging, a fiber array laser ultrasonic system with two laser beams in place of a single laser beam system has been developed [46][47]. More recently, A. Mebane et al., [46] carried out feasibility studies of the new system successfully. V. Reddy et al., [47][48] demonstrated a dual laser ultrasonic system evaluating the quality of solder ball interconnections in a large 52.5 mm x 52.5 mm FCBGA package on board subjected to mechanical bending and drop tests to determine the pad cratering failures. V. Reddy et al., [49] demonstrated the system by evaluating BGA solder balls of more practical industrial samples in realistic failure setups.

The LUI technique is capable of evaluating both the first-level and second-level interconnections (shown in Figure 5). J. Yang [42] and J. Gong [43][44] used LUI technique to evaluate first-level interconnections in flip-chip packages and PBGA packages. The work described in this dissertation has concentrated on evaluating second-level solder interconnections in FCBGA packages. The first-level interconnections in the FCBGA packages under discussion are protected with underfill. From the history and manufacturing procedures of these samples, it is not expected to have any failures in the

first-level interconnections. To evaluate the first-level interconnections, it is recommended to conduct the LUI experiments on a package with only first-level interconnections, where die or substrate is attached to PCB using first-level solder interconnections. As the interferometer signal in the LUI technique is a result of defects and failures both in first-level and second-level interconnects, it is difficult to isolate which level contributed to the change in the signal. Thus, if one would like to determine the defects and failures in first-level interconnections, it is necessary to conduct the experiments using an unassembled package which will consist of a flip-chip, substrate, first-level interconnects, and possibly underfill. On the other hand, if one would like to determine defects and failures in second-level interconnects, then it is necessary to run the experiments on packages assembled on printed circuit boards, as presented in this work. In such a scenario, it is assumed that the first-level interconnects have already been examined and determined to have no defects, and the second-level interconnects are the focus of the test.

A comparison between different non-destructive solder joint/bump inspection techniques for the evaluation of microelectronic packaging is given in Table 1. With several revisions and improvements, the LUI technique shows the uniqueness and robustness among all other non-destructive inspection techniques. There is still scope for further improvements in the LUI system to increase the sensitivity and throughput of the system. However, with the current viable features, the LUI technology is ready to be introduced to the market. Building the industrial-scale prototype and Minimum Viable Product (MVP) are potential next steps.

Table 1 – Comparison of different non-destructive inspection techniques

Features			Electrical Test	X-Ray		Acoustic Inspection	Laser Ultrasonic Inspection Method
				2D X-Ray	3D X-Ray		
Contact/Non-contact			Contact via test pads	Non-contact	Non-contact	Contact (immersed in water)	Non-contact
Throughput			High	High	Low	Medium	High
Cost			Low	$150K - $250K	$200K - $1500K	$200K – $250K	$200K
Resolution/Sensitivity			Solder Joint (SJ) opening of size >50% of SJ width	~ 0.1µm feature detection	~ 10µm defect detection	~ 1µm spatial resolution	~ 2µm vertical separation
Capabilities	Silicon die defects		Yes	Yes	Yes	Yes	Yes
	Interlayer delamination		No	No	Yes	Yes	Yes
	Solder ball defects	Missing	Yes	Yes	Yes	Yes	Yes
		Misaligned	No	Yes	Yes	No	Yes
		Cracks	No	No	Yes	No	Yes
		Open	Yes	No	Yes	Yes	Yes
		Voids	No	Yes	Yes	No	Yes
	To Inspect various package types		Can be applied to any type of package but requires functional daisy chain	It is difficult to interpret images of multilayered or double-sided samples	Deep learning techniques are required to interpret the images	Incapable of inspecting packages with large thickness because of lack of penetration	Can potentially be applied to various package types

2.4 Fiber Array Laser Ultrasound

As the size of chip packages continues to grow, and/or the density of the solder balls interconnections increases, more laser energy is required to generate ultrasound with sufficient amplitude (strength) for reliable inspection using LUI technique. However, the laser power should not be above the thermoelastic regime threshold to avoid any damage to the package. One way to increase the laser power to the package is by increasing the laser power at the source and delivering through suitable higher core diameter fiber-optic cable.

It is common practice for the laser to be delivered to the DUI using a fiber-optic cable and a suitable end effector for focusing the laser beam. Fiber-optic cables have finite energy density capacities. If the laser energy is to be increased, the fiber must be sized to handle the laser energy without being damaged. However, the larger the diameter of the fiber, the larger the minimum bend radius. The fiber must not bend below the minimum bend radius (supplied by the manufacturer) to prevent breaking. Therefore, for the inspection systems that require high power pulses, the diameter of the fiber required could cause the footprint of the system to grow beyond optimal. Additionally, with this method, there is little control over the laser incident spot size. If the spot size is small enough, high laser energy density could cause the ablation.

Another effective way of increasing laser energy is by using multiple lasers via an array of optical fibers. Though overall laser energy is high, the laser energy in individual fibers can be low enough to carry safely in smaller core fibers. Small core diameter fibers will facilitate the compact size of the overall inspection system. Laser incident spots for

individual lasers can be separated to reduce laser energy density significantly and thus the total energy will always be in the thermoelastic regime.

A fiber array laser ultrasound has been used previously for material inspection. Cuiciang et al. used fiber-phased array laser ultrasound for cracks measurement [50]. The schematic of fiber-phased array laser ultrasonic system set-up developed by Cuixiang is shown in Figure 23 [50]. In the array method, the ultrasound signal amplitude is proportional to the number of elements in the array. Therefore, the performance fiber array laser ultrasound system can be improved by using more fiber segments with a higher power laser source. However, the increment of fibers will not only increase the cost of the system but also increases the optical complexity [50].

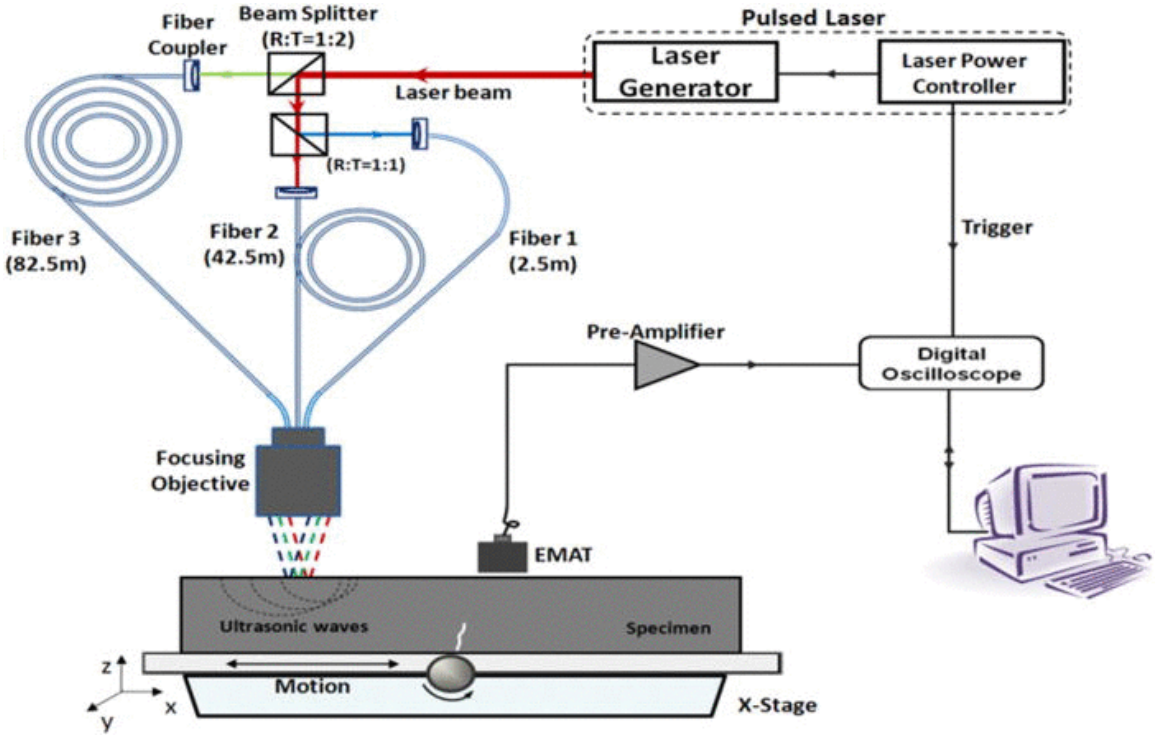


Figure 23 – Schematic of the fiber-phased array laser ultrasonic testing system for crack measurement [50]

Pavel et al. characterized the broadband and narrow fiberized laser ultrasonic sources for their effective application in nondestructive evaluations [51]. Yang J. et al. developed fiber phased array generation of ultrasound for non-destructive evaluation of materials [52][53], and Bao Mi implemented the same fiber phased array ultrasound generation system for weld penetration measurement [54].

2.5 Multi-mode Laser

There are two types of laser transmission modes through optical fibers, single-mode and multi-mode. The difference between single-mode and multi-mode lasers is shown graphically in Figure 24. Single-mode lasers are typically delivered via fiber with a core diameter of less than 25 μm, producing a narrow, high-intensity Gaussian beam that can be focused down to very small spot size. The high intensity and small spot size are ideally suited for fine laser marking, micromachining, or cutting applications. Multi-mode lasers use fibers with core diameters greater than 25 μm, resulting in lower and uniform intensity beam over a larger spot size as shown in Figure 24. In the LUI technique, the multi-mode laser was used to have a uniform and low-intensity laser over the incident spot to prevent any possible ablation of the sample surface. With a uniform intensity laser, it is possible to deliver high laser power with low laser energy density onto the test sample.

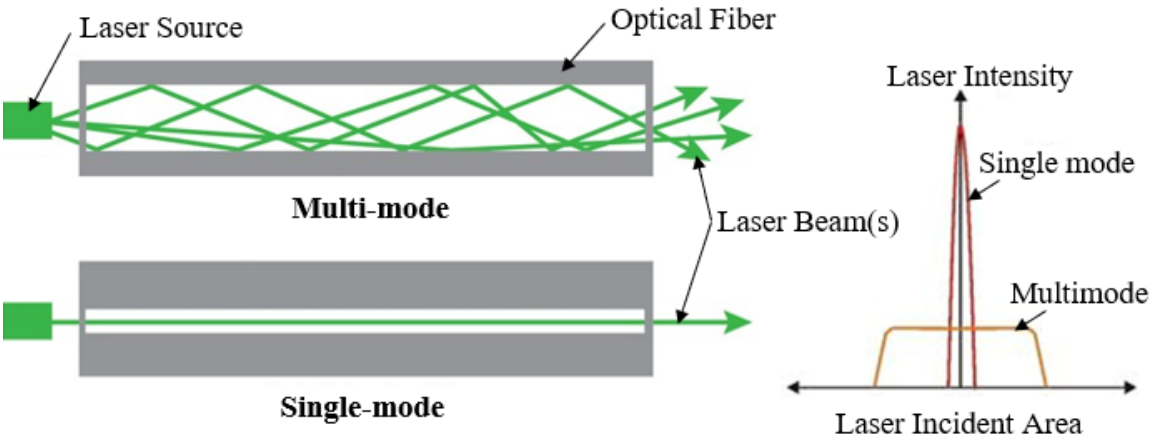


Figure 24 – Multi-mode and Single-mode laser propagation in optical fibers

2.6 Finite-Element Simulations

In this dissertation, finite-element simulations are used to validate and correlate the LUI results from the test samples subjected ALT such as four-point bending, drop testing, and ATC. Even though the ALT expedites the failure of the electronic products, however, they are still very expensive and time-consuming. A combination of ALT, LUI experiments, and finite-element simulations can reduce the effort significantly to predict the life of microelectronic packages under various operating conditions.

Finite-element simulations have been widely used to study the reliability of electronic products, especially solder joint reliability [55]. Predictive models such as the Coffin-Manson model [55] and the Darveaux model [56] are well established to predict the fatigue life of solder joints using damage metrics derived from finite-element simulations. Inelastic strain energy density (ΔW) and inelastic strain range ($\Delta\varepsilon$) are commonly used damage metrics in the Coffin-Manson predictive model [55]. Darveaux model is an energy-based model and uses accumulated inelastic energy density as a damage metric to find the

number of cycles to failure [56]. However, approximations are involved in choosing parameters for these models. Also, underlying assumptions, simplified geometry, and idealistic models such as Anand's viscoplastic model for solder joints, make finite-element simulations inconclusive without actual ALT results.

A good correlation equation between LUI results and damage metrics from the finite-element simulations can make fatigue prediction faster and accurate. However, the test vehicles should be subjected to a few hundreds of accelerated thermal cycles for better accuracy. A linear-quadratic equation was formulated between LUI results and accumulated inelastic strain per cycle (from finite-element simulations) in this dissertation.

CHAPTER 3. LASER ULTRASONIC INSPECTION SYSTEM

In this chapter, the original Single Laser Ultrasonic System (SLUS) which has been operational at the beginning of this dissertation research and its components/subsystems are discussed. The limitations of SLUS are also discussed. The schematic of the basic LUI system is shown in Figure 25. Original SLUS with most of its subsystems is shown in Figure 26. The system consists of (i) a Polaris II a Neodymium-doped Yttrium Aluminum Garnet (Nd:YAG) laser for generating pulsed laser beam, (ii) laser interferometer for measuring the transient out of plane displacement caused by the nano-amplitude vibrations, (iii) a laser doppler vibrometer controller for decoding the interferometer signal, (iv) band pass filter in low pass and amplifying mode to filter out unwanted high frequency noise as well as amplify the signal from the vibrometer controller, (v) autofocus system to adjust the stand-off height between interferometer head and the surface of the test vehicle to get optimal reflective interferometer laser strength, (vi) sample positioning stage for precise positioning of the test vehicle under the interferometer probe, (vii) vacuum fixture for easy, secure mounting of the test vehicle, (viii) end effector stage for positioning laser stage atop the sample positioning stage for fast, and repeatable positioning of the excitation laser, (ix) fiber-optic delivery system to transmit the laser beam from the laser generator to the test vehicle, (x) vision system for detecting device fiducials for package orientation and alignment, and (xi) a computer with a data acquisition controller for controlling the system and process, record and analyze the data.

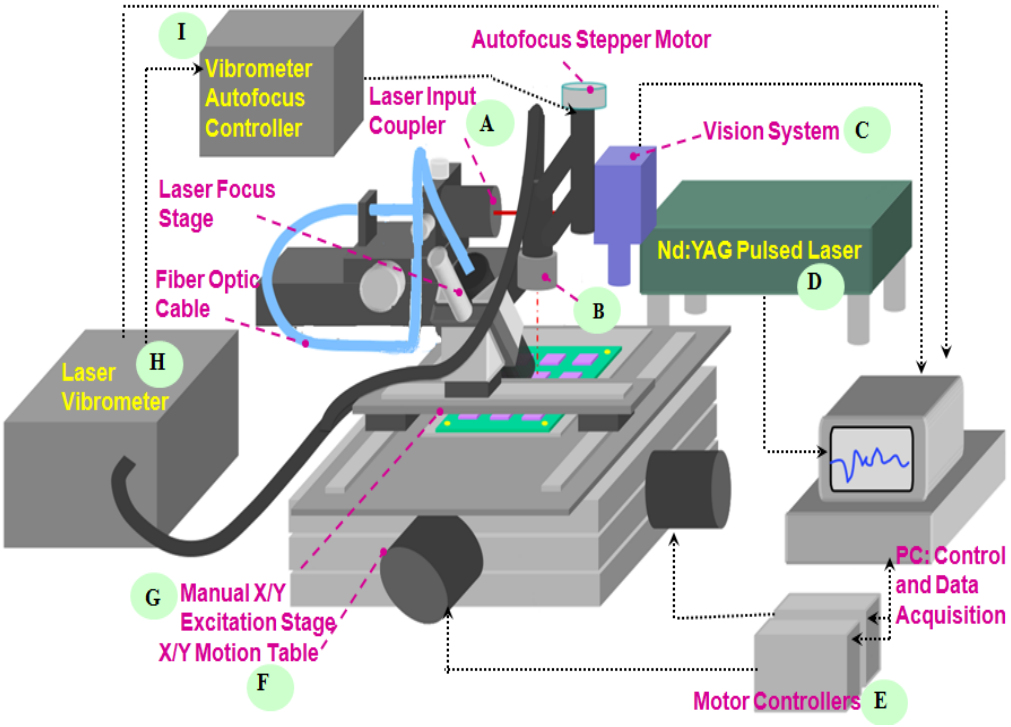


Figure 25 – Schematic of the laser ultrasonic inspection system

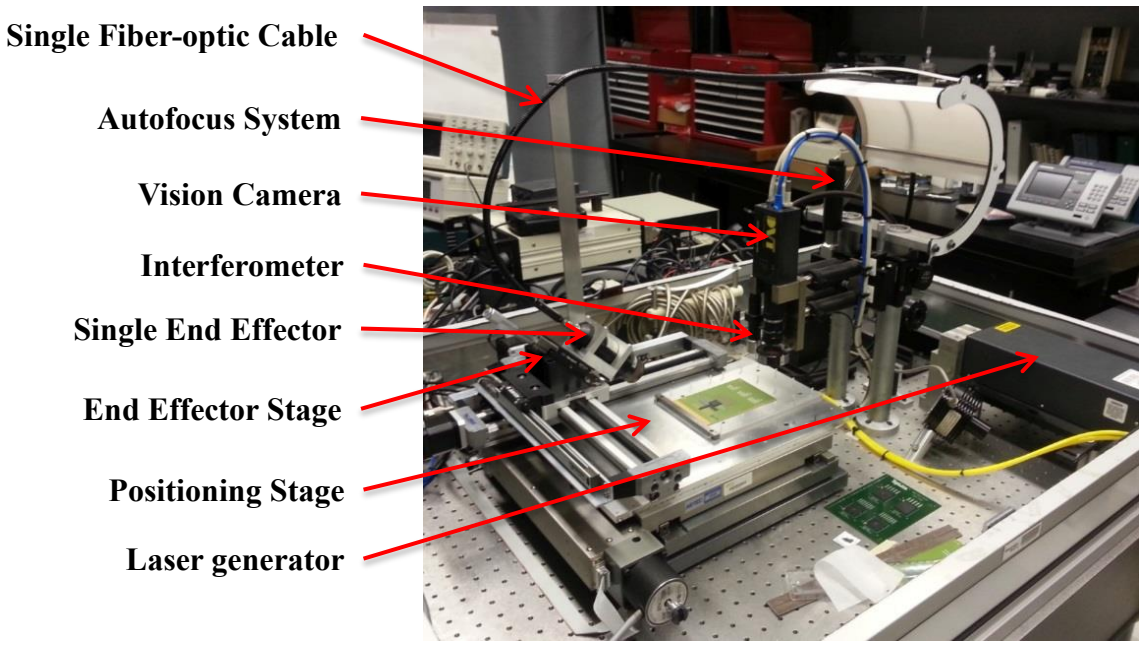


Figure 26 – Original Single Laser Ultrasonic System (SLUS)

3.1 System Hardware

3.1.1 Pulsed Nd:YAG Laser

A Polaris II Q-switched Nd:YAG laser system from New Wave Research, as shown in Figure 27, is used as the pulsed laser source. The pulsed Nd:YAG laser generates laser pulses with a duration of 4 to 5 ns at the wavelength of 1064 nm. The repetition rate of the laser pulse can be adjusted from 1 to 20 Hz. The output beam has a $1/e^2$ diameter of 3 mm. The $1/e^2$ diameter of a Gaussian laser beam is defined to be 2 times the radius from the beam axis at which the intensity has dropped to 13.5% of the maximum intensity. After the 30-minute warm-up, the output laser beam pulse to pulse energy stability is over 98% for 10,000 shots [35]. The maximum energy per pulse is 50 mJ. Though maximum energy per pulse is well beyond the damage threshold for most chip packages, the pulse energy is adjustable through a motorized optical attenuator, and it can be measured by a laser power meter. The laser power meter system used to calibrate the laser power for the particular test vehicle under inspection is shown in Figure 28. The proper laser energy level needs to be determined for different types of test vehicles. An excessive energy level will damage the chip surface, while an insufficient energy level cannot generate the ultrasonic response with enough strength.

Ref: New Wave Research

Figure 27 – NewWave Research Polaris II Nd:YAG laser system

Ref: Scientech

Figure 28 – Laser power meter

3.1.2 Laser Doppler Vibrometer

The system uses a laser Doppler vibrometer to capture the transient out-of-plane displacements in the nanometer scale induced by laser-generated ultrasound. The Doppler vibrometer is made up of a Polytec® OFV-511 fiber-optic heterodyne interferometer, shown in Figure 29, and a Polytec® OFV-2570 high-frequency vibrometer controller,

shown in Figure 30. The operating principle of the heterodyne interferometer is shown in Figure 22. The interferometer sensor head, as shown in Figure 31, is positioned perpendicular to the test sample surface, where it delivers the interferometer's laser beam with a wavelength of 650 nm. The laser spot size can be focused down to 3 µm to achieve a high spatial resolution. The vibrometer controller has an integrated 10 MHz bandwidth velocity decoder and a 24 MHz displacement decoder. As the out-of-plane vibration of the DUI is the variable of interest, only the displacement decoder is used. The maximum displacement measurable by the system is 75 nm with a measurement resolution of 0.3 nm. At each data collection point, multiple measurements were taken under a series of laser pulses and were then averaged to suppress noise. In addition to measuring the displacement, the vibrometer controller also measures the intensity of the reflected laser from the sample surface. The greater the amount of laser reflected back to the interferometer probe, the greater the Signal-to-Noise Ratio (SNR). In this system, the information concerning the intensity of reflected light is provided as feedback to the autofocus subsystem, which allows the automated adjustment of the distance between the sensor head and sample surface to maximize the collected light.

Figure 29 – Polytec OFV-511 heterodyne interferometer

Figure 30 – Polytec OFV-2570 vibrometer controller

Figure 31 – Interferometer sensor head

3.1.3 Bandpass Filter

A Krohn-Hite Corporation model 3945 high-pass/low-pass Butterworth/Bessel programmable filter, shown in Figure 32, is used in the low pass and amplifying mode to filter out unwanted high-frequency noise as well as to amplify the signal from the vibrometer controller. The programmable filter features 3 independent input channels, a frequency range from 3 Hz to 25.6 MHz, and a noise of less than 250 μV referred to the input. In this research, only the Butterworth low-pass channel is used with a cutoff frequency of 2 MHz and an input gain of 10 dB and an output gain of 6 dB.

Ref: Krohn-Hite Corporation

Figure 32 – Bandpass filter and amplifier

3.1.4 Autofocus System and Local Search Pattern

The surface finish of the test sample can greatly affect the amount of laser light from the interferometer that is reflected back into the interferometer head. The amount of light collected by the interferometer sensor (photodetector) greatly affects the SNR, with a decrease in the amount of laser corresponding to a low SNR and vice versa. If the sample

surface is smooth, a large amount of the incident laser beam can be reflected back into the interferometer head, which can produce a signal with good SNR. However, if the sample surface is rough, it leads to a scattered beam with speckle, and the amount of the reflected light received by the interferometer is greatly reduced. As a result, the accuracy of the measurement will be affected. Therefore, it is important to adjust the standoff distance between the interferometer sensor head and sample surface until the captured light is maximized. This is achieved by mounting the interferometer sensor head onto a motorized linear stage. The schematic of the autofocus system is shown in Figure 33 [57]. The motorized linear stage controls the standoff distance between the interferometer focusing head and the sample surface with a fixed focal length, which allows the spot size of the laser to be adjusted while searching for desirable signal strength. Before data is taken at a particular point, the system reads the intensity of the light collected by the sensor head and the result compared to a set threshold value. If the measured intensity is below the threshold the autofocus system will initialize a scan in which the height of the sensor head is adjusted until an intensity value above the threshold is found. Input shaping is implemented to control the motion of the linear stage for vibration reduction.

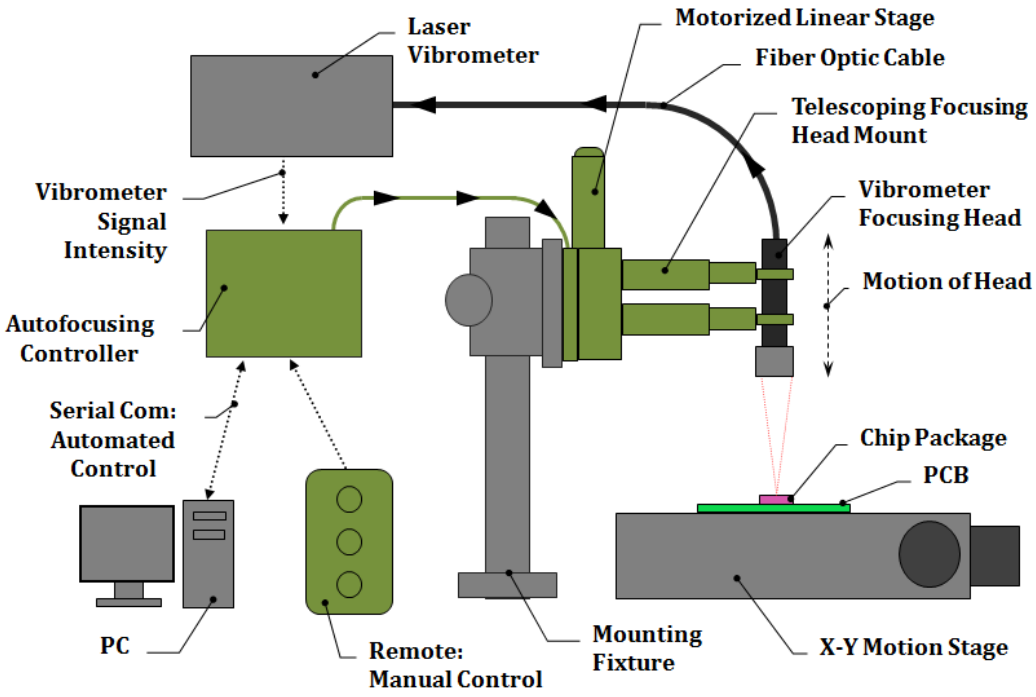


Figure 33 – Schematic of the autofocus system [57]

If the autofocus system still fails to focus properly; the system will initialize a Local Search Pattern (LSP) in which the target surface is moved in a rectangular spiral in increments of 1 micron at a time. An example of a 49-point local search pattern is shown in Figure 34. The center marker represents the initial inspection location, while the rest of the markers are the alternative data collection points. At each step in the process, the autofocus routine will search for an intensity value above the threshold. Once the interferometer signal intensity is above the threshold level at one of the alternative data collection points, the local searching will be terminated. If the intensity value above the threshold is not located after searching on all alternative data collection points, the interferometer data will be taken at the point where the highest intensity value is measured.

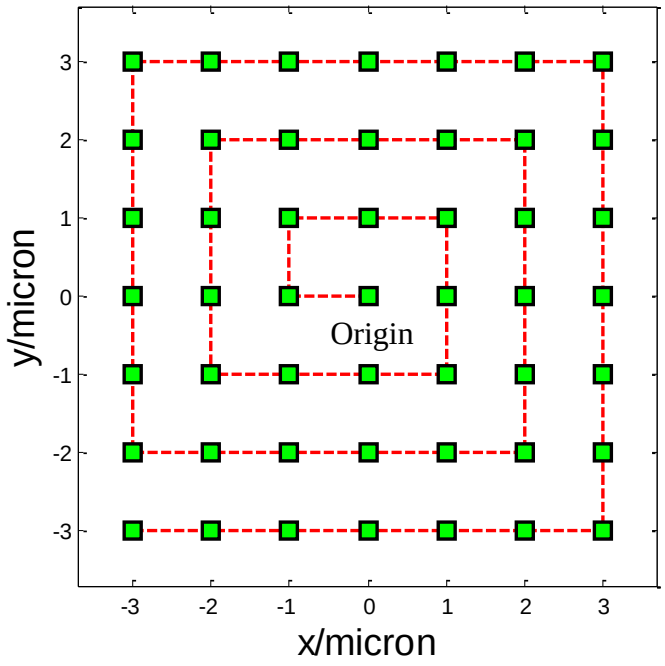
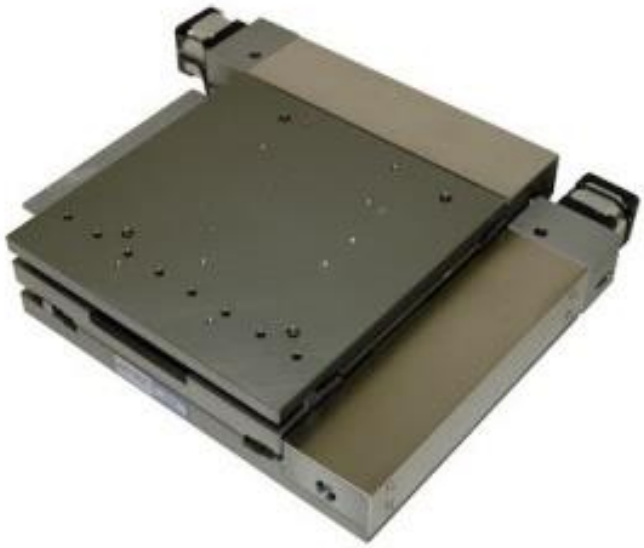


Figure 34 – A typical 49-point local search pattern

3.1.5 Sample Positioning Stage

The sample positioning stage, as shown in Figure 35, is a stepper motor-controlled X-Y table from Nutec Inc. This stage holds the test sample and is used for precise, automated positioning of the test sample. As per the manufacturer's specifications, the accuracy is 7.5 um per 100 mm of travel with bidirectional repeatability of ±1.0 µm, and an orthogonality error of fewer than 7.5 arc-seconds. This is accomplished using preloaded crossed-roller bearings which eliminate play. The precision-grade lead screw drive provides positioning accuracy and repeatability. The stage has a large 200 mm x 200 mm range of motion as well as a large mounting surface. Mounting surface is used for mounting the vacuum fixture and end effector stage.



Ref: Motioncontrol.com

Figure 35 – Sample positioning stage (XY Table)

3.1.6 Vacuum Fixture

The vacuum fixture, shown in Figure 36, is mounted on top of the sample positioning stage and is used to securely fix the test sample during the inspection process. The table consists of an anodized aluminum vacuum plate on which the test sample sits and an alignment fence for the sample to be butted up against for repeatable placement of the sample. The vacuum plate has two independent systems of channels machined into the back of it; these are connected to a total of 48 inlet ports. As seen in Figure 36, one system of channels and ports extends only over a small portion of the plate and is used for securing small samples while the other system extends over the entire plate and is used to secure larger samples. When a vacuum is drawn from one of the main vacuum ports, the air is sucked through the system channels and ports, which in turn will pull down the sample

positioned on the vacuum plate. This vacuum fixture can hold samples as large as 152.4 mm x 203.2 mm.

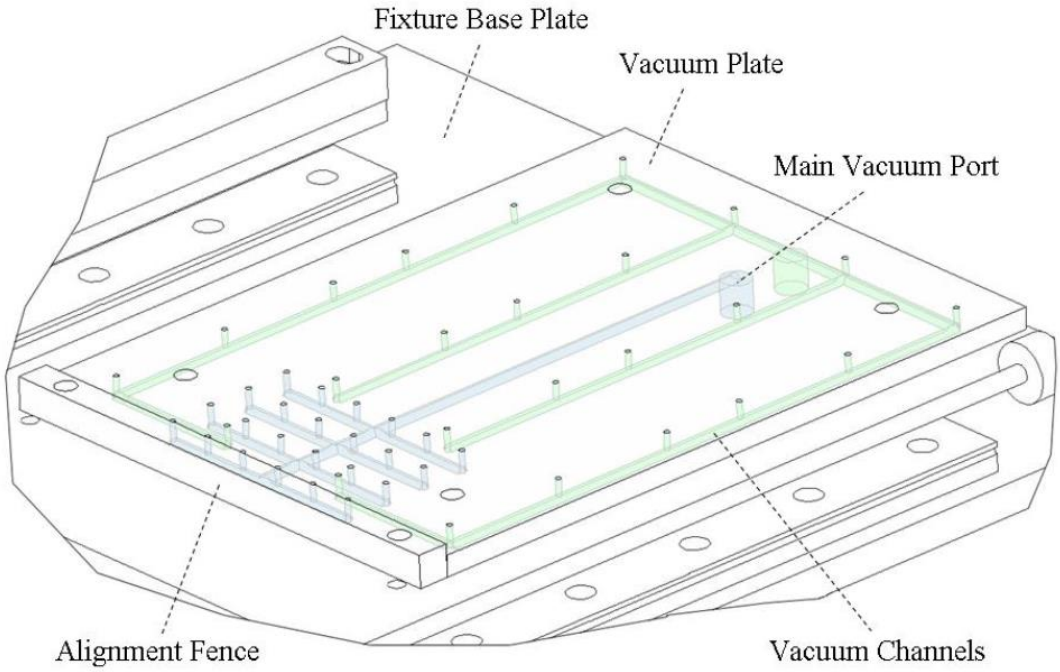


Figure 36 – Vacuum fixture for securing the samples during the inspection

3.1.7 End Effector Stage

The end effector stage is a custom-built motorized X-Y stage, holding laser end effector(s), for accurate, repeatable automated positioning of the laser excitation spot. The stage incorporates PBC 25 thread/in lead screws, 200 step/rev stepper motors, and an Arcus PMX-2ED-SA stepper motor controller, capable of micro-stepping and ±5% step accuracy. For accurate and repeatable positioning, feedback is provided by ACU-RITE MicoScale™ linear encoders. The encoder feedback allows 1 µm resolution for the positioning of the laser excitation spot with repeatability within one resolution count. The end effector stage with the Arcus system and the end effectors mounted on the top is shown in Figure 37. End

effector(s) are mounted on the X-Y stage at a 45° angle to allow the laser interferometer to perpendicularly measure the out-of-plane displacement. Thus, this setup also causes the excitation laser spot on a sample surface to be elliptical instead of circular, as shown in Figure 38.

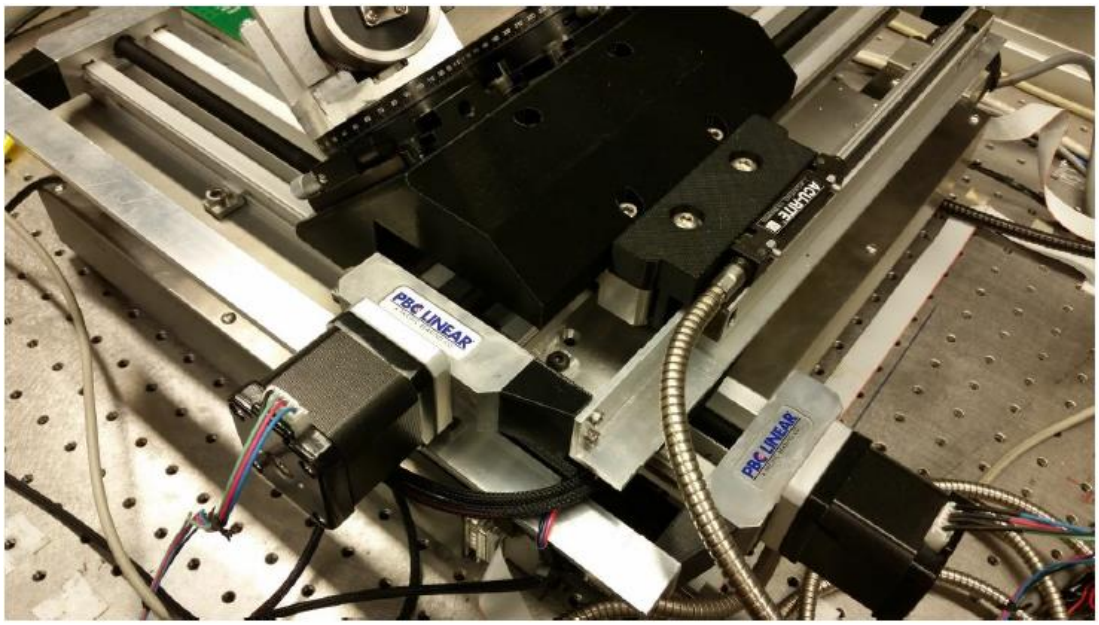


Figure 37 – End effector stage for positioning of the laser excitation spot

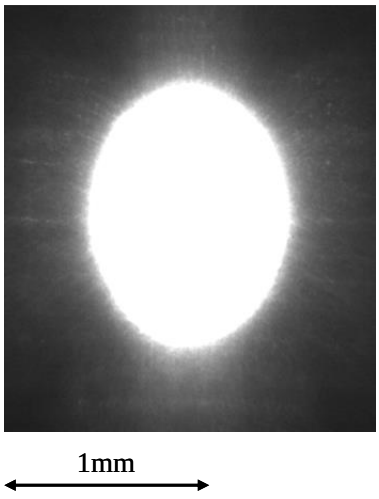


Figure 38 – The elliptical shape of the excitation laser spot

3.1.8 Fiber-Optic Delivery System

The goal of the fiber-optic delivery system is to deliver the required pulsed laser to the sample surface with minimal energy loss and maximal flexibility. The schematic of a fiber-optic delivery system is shown in Figure 39. The original fiber delivery system was composed of an input coupler, 600 µm core fiber-optic cable, and a non-adjustable end effector (collimator and focusing lens), all by U.S. Laser Corp. This system allows the excitation laser source to remain stationary while allowing the excitation spot on the sample surface to be positioned as needed. The fiber-optic cable features a PVC armored jacket that protects against mechanical shock and some resistance to over bending. LD-80 end connectors were used for secure, repeatable fiber attachment. The fused silica core was chosen for its high laser energy damage threshold and low loss characteristics, which allows the nanosecond scale laser pulses to be efficiently transmitted to the sample surface.

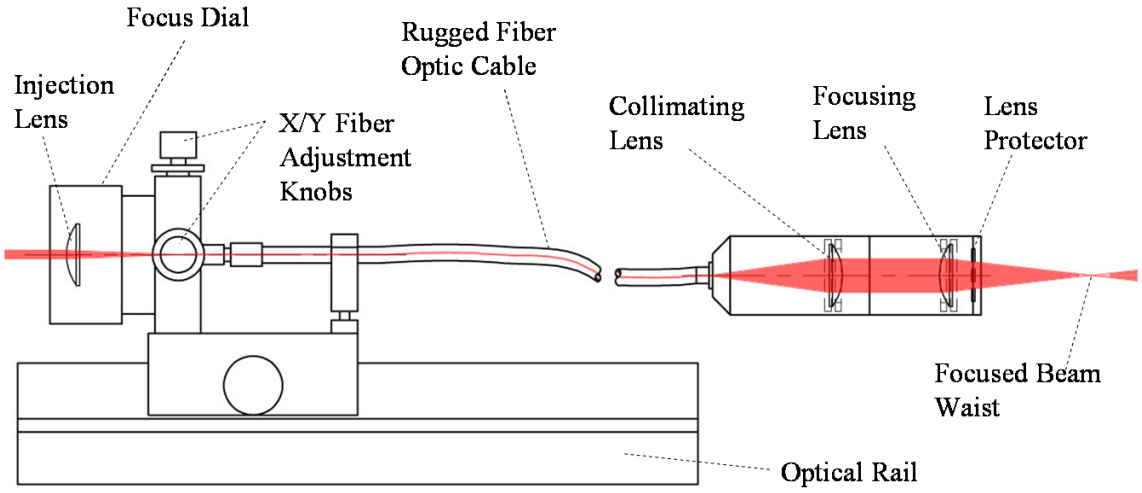


Figure 39 – Schematic of the fiber-optic laser beam delivery system

3.1.9 Vision System

The vision system is used to locate fiducial marks on the PCBs for calculating the coordinates (or relative positions) for the excitation laser spot and data collection points. Fiducial marks are usually circular, square, or cross-shaped solid pads on PCB. They serve as reference features for pick-and-place machines that use vision systems to accurately place microelectronic components on their corresponding bond pads during the assembly process. An example of a circular fiducial mark on a PCB is shown in Figure 40. In this research work, the fiducial marks are used by the vision system to detect the relative position of the PCB on the vacuum stage. Based on this information, the motor commands are used to move the end effector stage and sample positioning stage for precise positioning of the laser excitation spot and interferometer sensor head over the sample surface. The smart sensor DVT Series 600, shown in Figure 41, was used in this research. It uses a 3.6 x 4.8 mm CCD with a 480 x 640-pixel resolution. This sensor produces 8-bit grayscale images and incorporates FrameWork software for easy image processing.

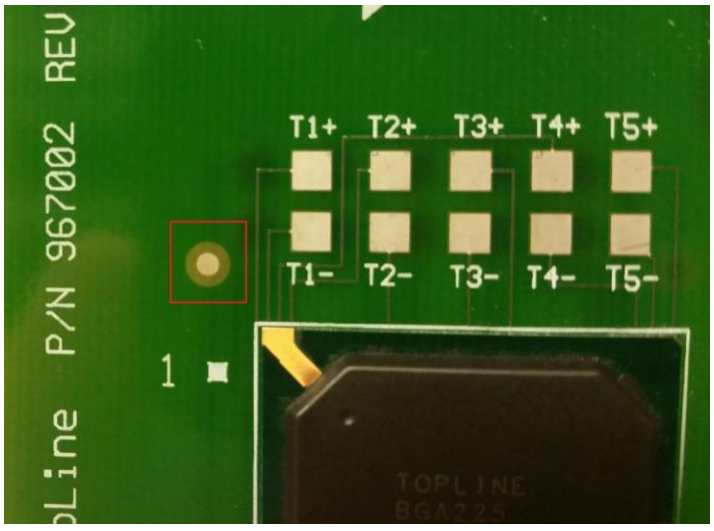


Figure 40 – Circular fiducial mark on a PCB

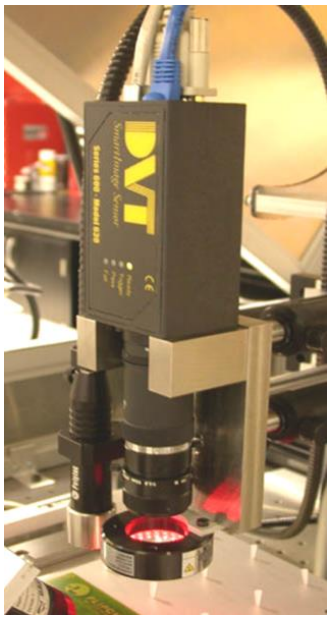
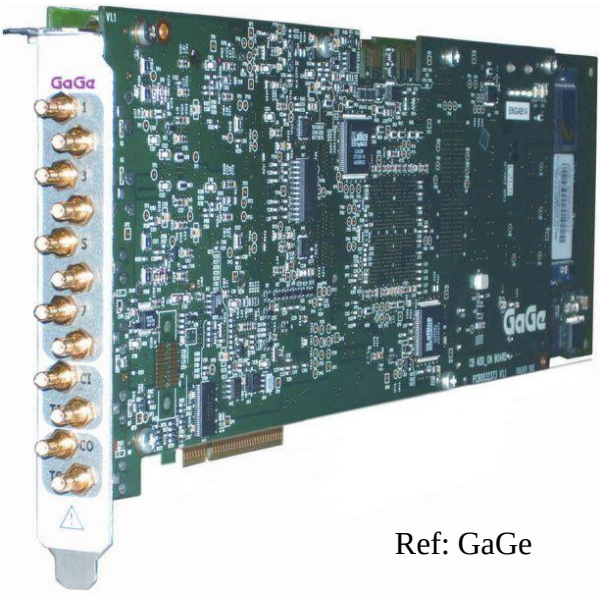


Figure 41 – DVT series 600 smart sensor camera for locating fiducial marks

3.1.10 Data Acquisition Board

In this research, a high-resolution and high-sampling rate data acquisition board, GaGe CompuScope 8327 PCI A/D card, as shown in Figure 42, was used to capture the ultrasound responses on a nanometer scale. This board has dual-channel, 14 bits resolution, and various sample rates ranging from 10 kHz to 125 MHz. Its input ranges, coupling, and impedances can also be easily adjusted. This board also provides a Software Development Kit (SDK) for MATLAB, which is ideal to develop a control interface to integrate all the subsystems explained above.



Ref: GaGe

Figure 42 – GaGe CompuScope 8349 PCI A/D card

3.2 System User Interface and Operation

All the components and sub-systems detailed in the previous section have been integrated to function as a complete system to enable and facilitate the laser ultrasonic inspection process. System integration and software control interface are developed using MATLAB. An overview of the operation flow chart is shown in Figure 43. Creating an inspection recipe from the original CAD file (or Gerber file) is the first step in the inspection process for a family of test samples. The next step is to teach the system about the orientation and alignment of the test sample on the vacuum fixture. The teaching is done using the vision system by locating fiducial marks on the test sample. Based on the fiducial locations and inspection recipe, the control interface will recalculate the positions of laser excitation spot and data collection points for the interferometer and saved in a text file. This text file will be used to send the motor commands to move the end effector stage

to the predetermined laser excitation spot and to move the sample positioning stage to the predetermined data collection points under the interferometer head.

MATLAB graphical user interface is used for experimental parameter setup and experiment control. LUI experiments can be controlled in both automatic mode and manual mode. Based on the mode, the sample positioning stage and end effector stage are driven automatically or manually to the desired positions, following the inspection recipe. In general, automatic mode is used for running experiments and manual mode is used for calibration and resetting of the system. After completing the inspection, signal analysis is also done using MATLAB to predict the failures in the test sample. Detailed system calibration procedure, operating procedure, and software instructions are available in the operation manual of laser ultrasound and interferometric inspection system [58].

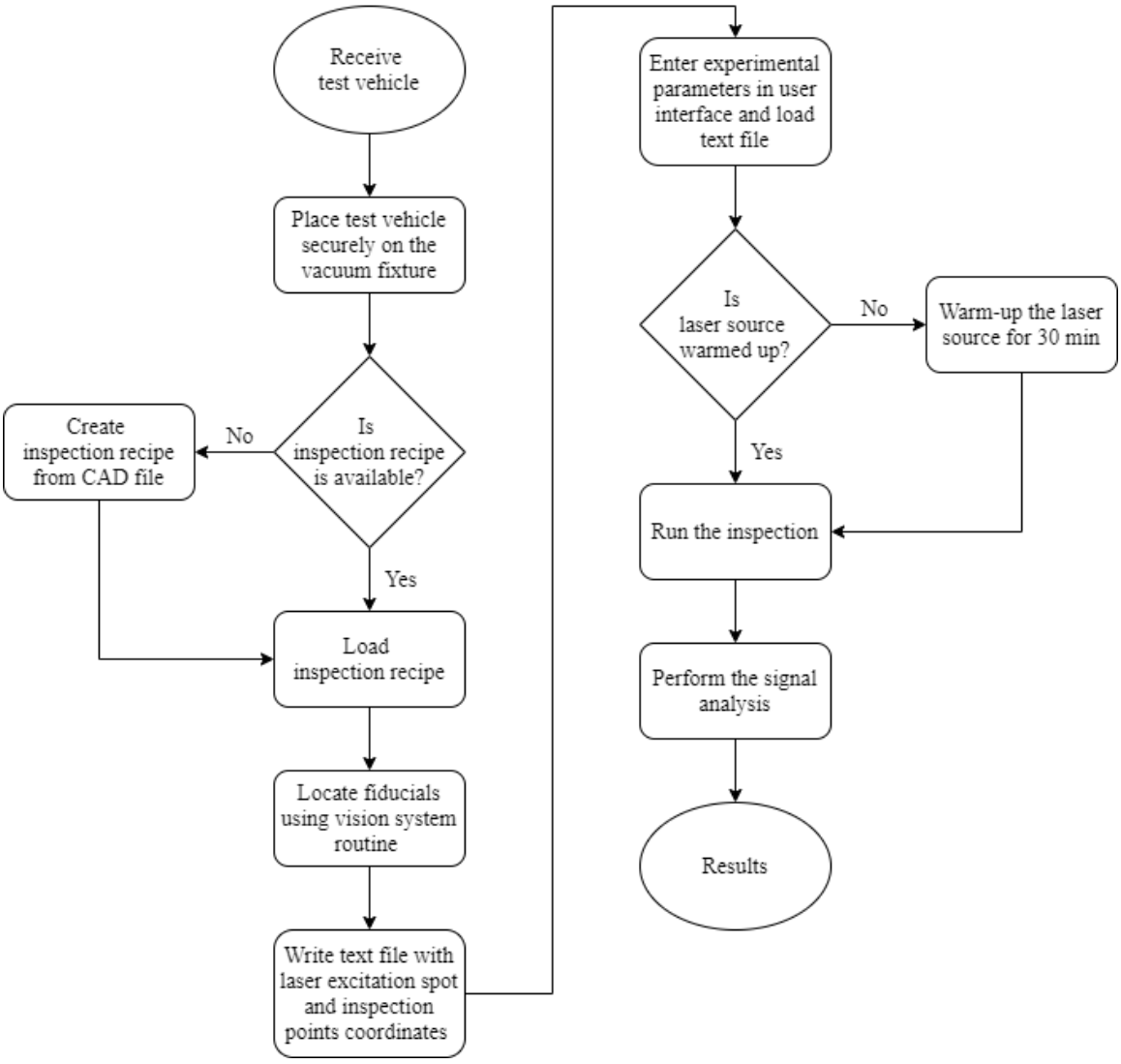


Figure 43 – Operation flow chart for laser ultrasonic inspection

3.3 Limitations of SLUS

SLUS has few major drawbacks with regards to laser power it can deliver to the test sample, accurate focusing of the laser beam onto the sample surface, and inadequate safety features, etc.

3.3.1 Limited Laser Power

The major limitation of SLUS is that the system cannot deliver high enough laser power without damaging the test sample and the fiber. SLUS has a single fiber-optic cable that can deliver the laser at one excitation spot. Fiber-optic cable limits the amount of energy that can be transmitted through it due to the intrinsic damage threshold of the fiber. On the other hand, the damage threshold of a test sample is concerned with the maximum laser energy density the sample surface can withstand before the material begins to be ablated. For a given fiber and incident spot size, this ablation damage threshold limits the energy that can be delivered for the ultrasonic generation. Hence, with the limited laser energy from a single fiber and single laser excitation spot, the strength of ultrasounds that can be produced from the maximum energy might not be strong enough to detect very small defects/failures or inspect large devices.

3.3.2 Non-adjustable End Effector

The end effector is composed of a collimating lens, to collimate the diverging beam exiting from the fiber-optic cable and a focusing lens for directing the collimated beam down to a small spot onto the test sample. The detailed collimating and focusing mechanisms are given in Figure 44. If the end of the fiber is at the focal point of the collimating lens (i.e. $D_1 = f_0$), the exiting beam will focus at the focal point of the focusing lens (i.e. $D_2 = f_h$). Similarly, if the end of the fiber is above the focal point of collimating lens (i.e. $D_1 < f_0$), the exiting beam will focus below the focal point of the focusing lens (i.e. $D_2 > f_h$) and vice versa (i.e. $D_1 > f_0 \rightarrow D_2 < f_h$).

SLUS has a non-adjustable end effector, as shown in Figure 45, which means, there is no provision to adjust the end position of the fiber with respect to the focal point of the collimating lens (i.e. distance D_1 is fixed). Because of this fixed D_1 distance, the focus of the exiting beam from the end effector is also fixed (i.e. distance D_2 is also fixed). These fixed foci of the beam will cause issues in laser excitation spot size on the sample surface. A simple illustration of how the incident laser spot size changes with the height of the test samples is shown in Figure 46. It is possible that the incident laser spot can be too small and laser energy density exceeds the damage threshold of the test sample or the spot size can be too large and laser energy density is too low to effectively generate ultrasound.

To address this impediment, an alternate way to move the entire end effector closer or farther from the sample surface is provided by mounting the end effector on a manual linear stage as shown in Figure 45. However, it is not an effective way to focus the laser spot on the sample surface. With this provision, the area of the incident spot could be varied from 0.6 mm^2 to approximately 8 mm^2 [59]. It has been envisaged to expand the range of possible incident spot sizes, so more investigations could be conducted on the effect of incident spot size on the inspection results.

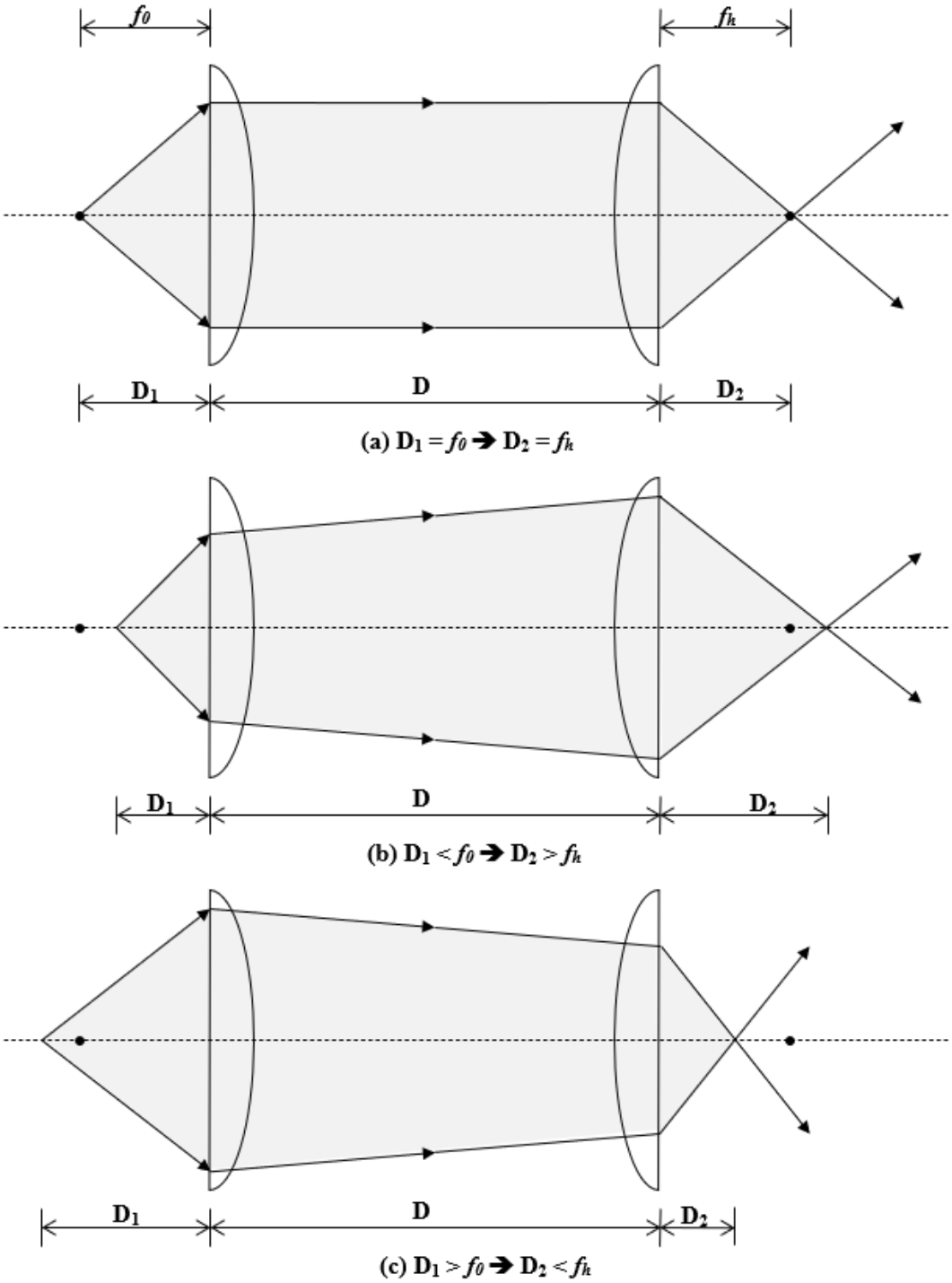


Figure 44 – Mechanisms of collimating and focusing of the beam in the end effector when the end of the fiber is (a) at the focus of the collimating lens (b) above the focus of the collimating lens and (c) below the focus of the collimating lens

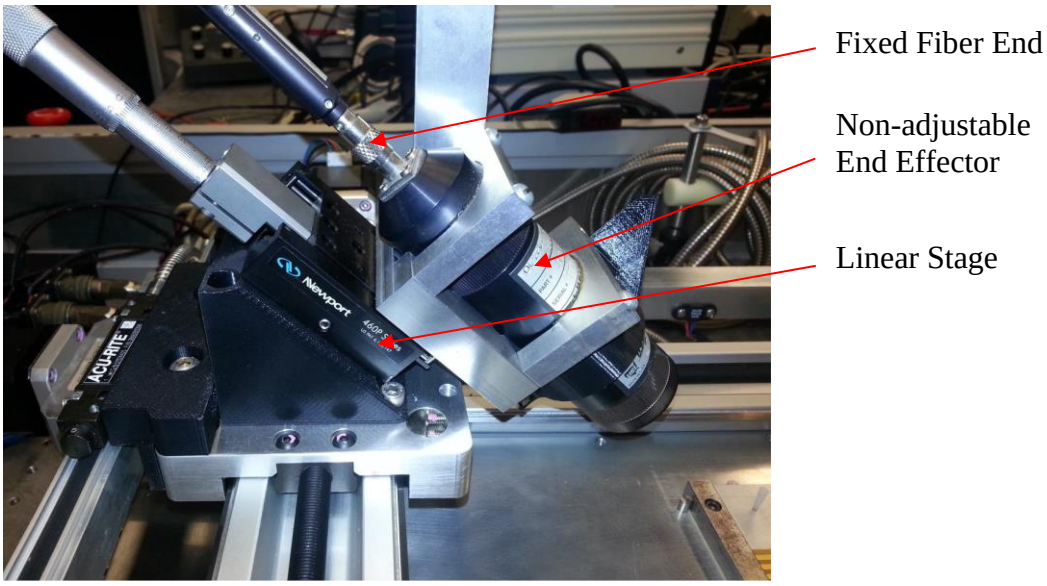


Figure 45 – The non-adjustable end effector of SLUS

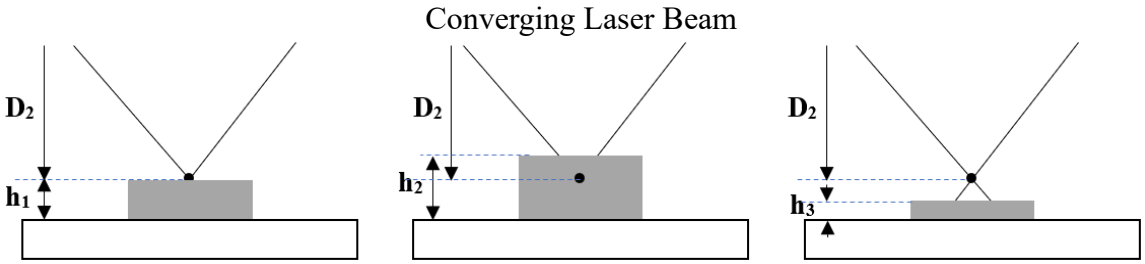


Figure 46 – Illustration for change of laser excitation spot with the variation of sample height ($h_2 > h_1 > h_3$)

3.3.3 Inadequate Safety Features

SLUS had inadequate safety features to protect against the collisions between the end effector and the interferometer head. Precise calibration of the locations of the laser excitation spot and the interferometer sensor head is required for accurate LUI measurements. Therefore, it is paramount that the interferometer head should not collide

with the end effector(s). In SLUS, a laser tripwire safety system was provided to cut the power to the end effector stage. However, the tripwire safety system will not stop sample positing stage from driving end effector to collide with interferometer head.

Additionally, the existing emergency stop switch in SLUS is not programmed to cut power to the whole system (especially to the sample positioning stage). If an impending collision was observed, it was difficult for the operator to stop the system in time either with the tripwire safety system or with the emergency stop. Multiple instances of collisions/near-collisions had occurred, leading to damaged components and many wasted hours on system downtime. Hence, there was a definite need to improve the safety features of SLUS.

CHAPTER 4. DEVELOPMENT OF A DUAL FIBER ARRAY LASER ULTRASONIC SYSTEM (DALUS)

Development of DALUS entails multidisciplinary expertise including microelectronic packaging, laser optics, laser ultrasound generation, and detection, mechatronics, digital signal processing, statistics, and finite-element analysis, etc. Only the successful integration of these various technologies can lead to the successful development of an inspection system that meets the overall research goal.

4.1 Need for DALUS

SLUS is very effective in evaluating the quality of first-level solder interconnections in small microelectronic packages. However, advanced packages are more complex and multi-leveled. Large packages like FCBGA need more laser energy to generate ultrasounds with sufficient amplitude. Additionally, to avoid damage to the test vehicle, the laser must operate in the thermoelastic regime. This limits the laser energy that can be delivered to the test vehicle surface. In the case of SLUS, the area of laser incidence spot with 600 μm core diameter of the fiber is 2.5 mm^2, and experiments have shown that 70 mW can cause damage to the silicon die by thermal ablation with an approximate energy density of 0.14 J/cm^2 [41]. The strength of ultrasound that can be produced from the maximum laser power of 70 mW using SLUS is not sufficient to achieve good SNR, especially in large packages and/or with micro-defects or failures. Therefore, there is a need to develop a robust system that can be used to evaluate the quality of first-level and second-level interconnections in all microelectronic package sizes.

4.2 Development of DALUS

DALUS is developed to deliver the laser at two incident spots. One of the major incentives to develop DALUS with a new laser array delivery system is the desire to deliver high laser power to the microelectronic package under inspection. The schematic of DALUS is shown in Figure 47 and the original image of the setup of DALUS is shown in Figure 48. Major modifications in DALUS are the introduction of a multiplexer, replacement of 600 µm optical fiber with two 1000 µm core/ 2 m length fibers along with two adjustable end effectors, and rotational stages.

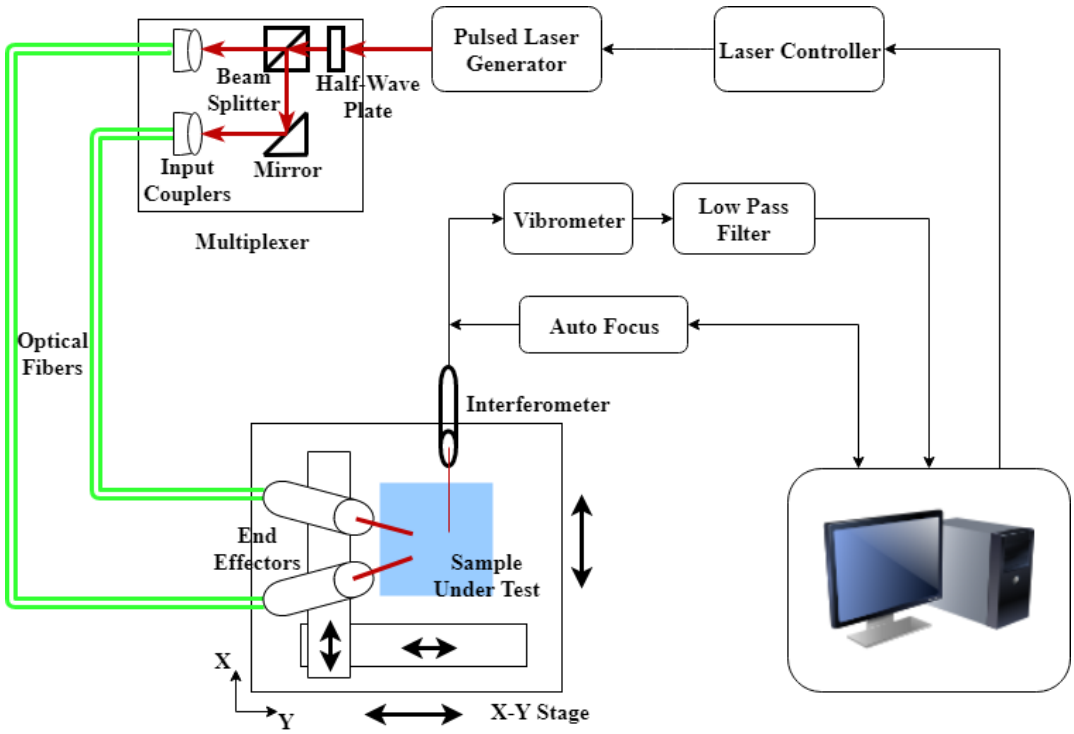


Figure 47 – Schematic of DALUS showing the multiplexer splitting the single laser beam into two beams

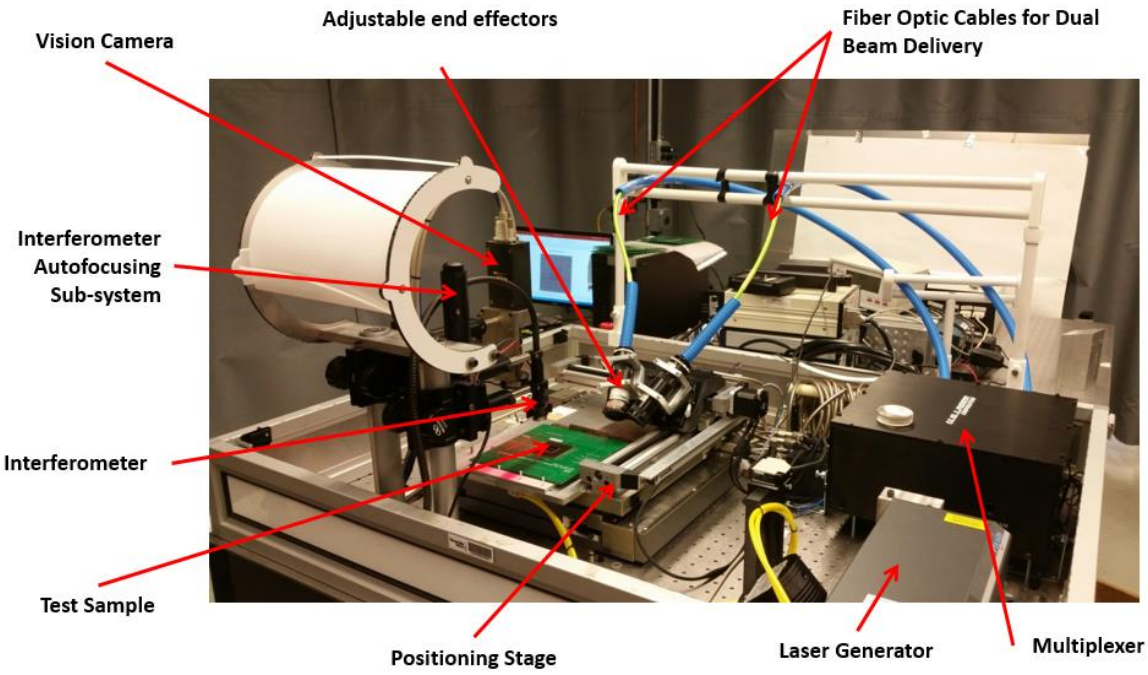


Figure 48 – Original image of DALUS setup

4.2.1 Multiplexer

The major upgrade in DALUS is multiplexer supplied by U.S. Laser Corp. The schematic and original image of multiplexer showing its internal components are shown in Figure 49. This device takes in a single laser beam from the source, splits into two beams, and launch the beams into two fiber-optic cables. Multiplexer consists of a half-wave plate to adjust the balance between the two beams, a beam splitter to split the beam into two beams of equal power at a 90° angle, a reflective mirror to direct the second beam into an input coupler, and two input couplers to fed the beams into fibers as shown in Figure 49.

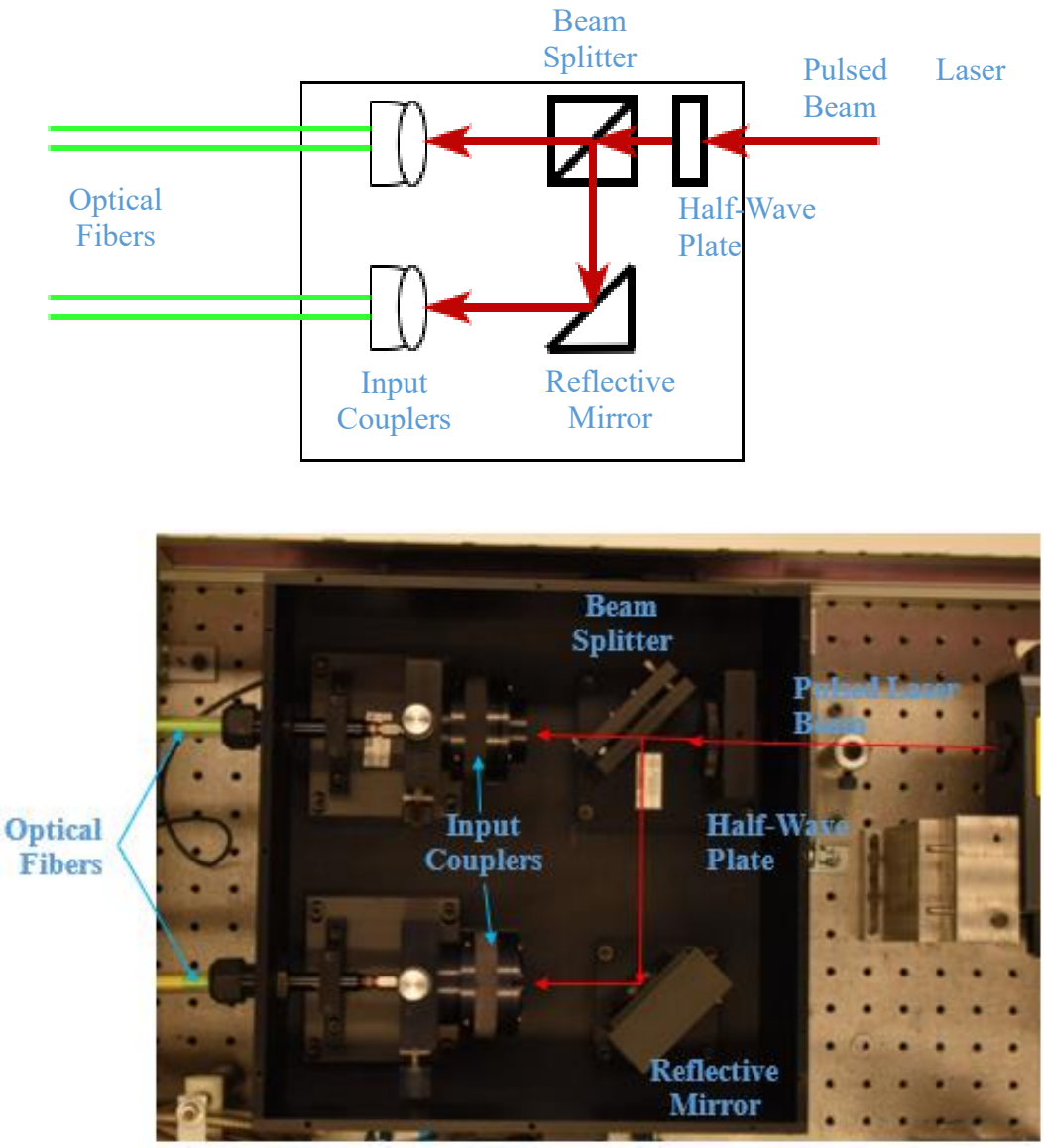


Figure 49 – Multiplexer with its internal components showing laser path

4.2.2 Fiber-optic Cables

As discussed earlier, fiber-optic cable limits the amount of energy at the experimenter's disposal due to the intrinsic damage threshold of the fiber. SLUS had one optical fiber of 600 µm core diameter. The maximum power carrying capacity of this 600 µm fiber is 100 mW according to the manufacturer's specifications. In order to increase

the maximum laser energy to be delivered to the sample, DALUS is equipped with two optical fibers of 1000 μm core diameter from FiberGuide Industries. The maximum power carrying capacity of each fiber is 200 mW (with 25% safety margin), which means, a total 400 mW laser power pulse can be delivered on the test sample. To exceed the recommended bend radius of the 1000 μm core fiber, which is 330 mm, 2 m length fibers are chosen. The complete system is reoriented to accommodate 2 m length fibers and multiplexer. The original image of DALUS with the multiplexer and optical fibers arrangement is shown in Figure 48.

4.2.3 Adjustable End Effectors

New adjustable end effectors from U.S. Laser Corp. are installed in DALUS. The schematic of the adjustable end effector is shown in Figure 50. The diverging beam from the end of the fiber is collimated through a collimating lens and the collimated beam is focused onto the sample surface using a focusing lens. As described in Figure 44, it is important to adjust the distance D_1 for the proper focus of the laser beam on the sample surface according to the sample height. The arrangement of the end effectors on rotational stages is shown in Figure 51. Adjustment of distance D_1 is achieved by rotating the threaded tube carrying the end of the fiber. A knurled ring is used to lock the threaded tube in place. Hence, it is convenient to adjust the distance D_2 and laser incident spot size using adjustable end effectors.

As shown in Figure 51, the end effector stage in DALUS consists of two adjustable end effectors mounted on top of the rotational stages via two machined aluminum clamps, and rotational stages are affixed onto a custom-designed stage that rides on Arcus

motorized X-Y stage. Adjustable end effectors are mounted at an angle of 45° to allow the laser interferometer to perpendicularly measure the out-of-plane displacement. The distance between the laser end effectors tip to the excitation spot on the vacuum fixture is around 75 mm.

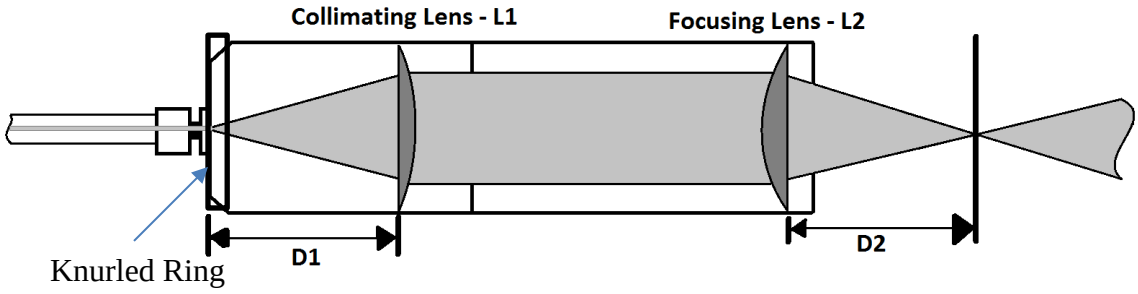


Figure 50 – Schematic of the adjustable end effector

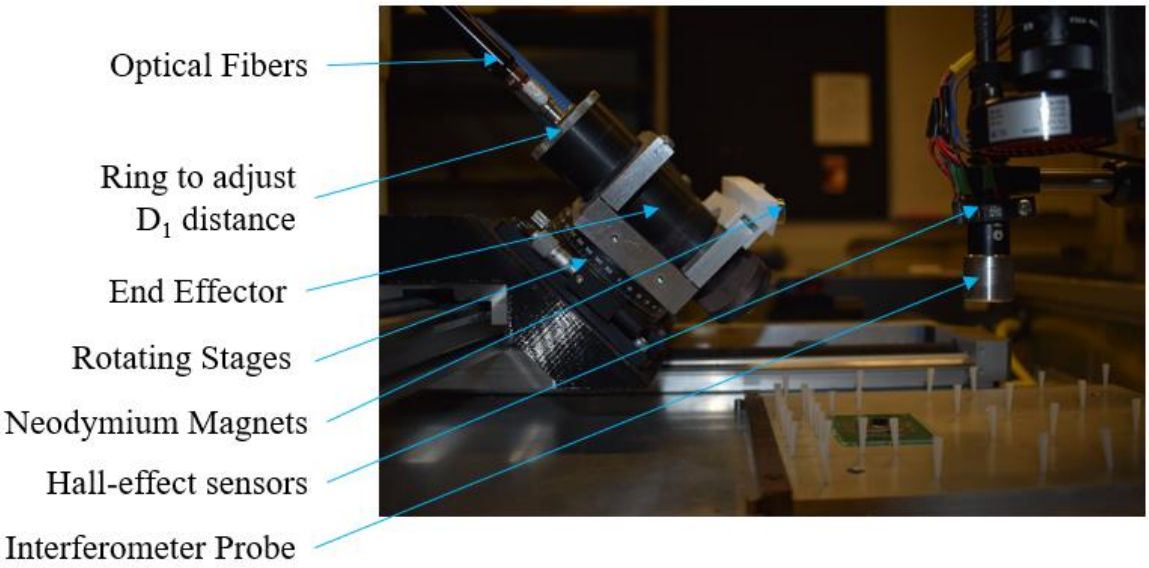


Figure 51 – Adjustable end effectors mounted on rotational stages on the end effector stage and hall effect safety system

4.2.4 Rotational Stages

Two ThorLabs PR01 rotational stages are installed for mounting of adjustable end effectors to set the required spacing between the two laser excitation spots. As seen in Figure 52, the rotational stage has a micrometer and Vernier scale for precise adjustment. The 5 arcmin gradations allow for adjustments of ±1 arcmin to be made. This correlates to repeatability in the spacing of about 0.5 mm. A MATLAB program was written to calculate angles for each rotational stage for a required spacing between the laser spots. This program is also customized for sample height.

Ref: ThorLabs

Figure 52 – ThorLabs rotational stage

4.2.5 Calibration and Alignment of the Laser Beam

After installation, DALUS has been calibrated as per the standard lab procedures for accurate and repeatable measurements. The first step in calibrating the system to align the laser beam to increase the coupling efficiency and minimize the power losses in the laser beam path. To achieve this, (i) multiplexer must be aligned properly to receive the input laser and split the beam with minimum losses, (ii) laser beams must be properly coupled into the optical fibers through input couplers, and (iii) end effectors must be

adjusted for the proper focus of the laser beam onto the test sample. Mechanical tools and mathematical calculations are enough for the alignment of the multiplexer and end effector. However, optical procedures are required to follow for coupling the laser beam into the optical fibers.

The fiber input coupler, as shown in Figure 53, is used for coupling the laser beam into the fiber. Input coupler consists of a focusing lens mounted in a movable housing that allows the lens to translate along the fiber's axis thereby focusing the beam onto the fiber's surface. Two screw knobs can adjust the XY alignment between the incoming beam and the end of the fiber.

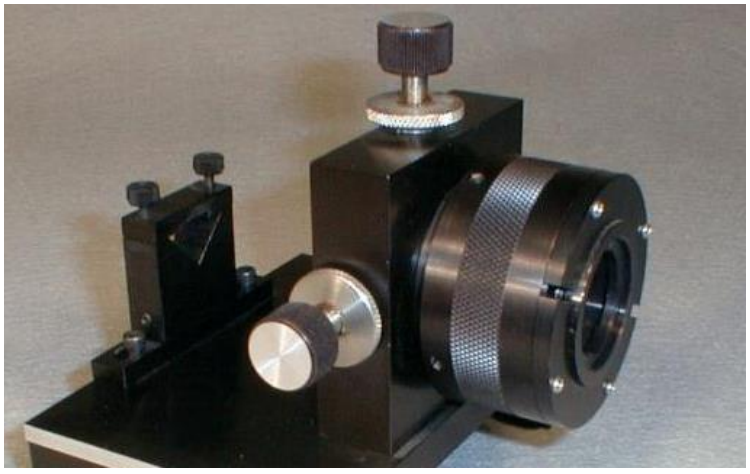


Figure 53 – Fiber input coupler mounted with a fiber holder on the left

To prevent damage to the fiber and/or power loss, the beam must not only be centered on the fiber's face but also focused correctly as shown in the schematic in Figure 54. It is important to make sure that only the diverging beam enters the fiber to prevent any damage to the fiber. Different possibilities for the alignment/focus of the laser beam into the fiber are shown in Figure 55 and Figure 55(e) shows the proper alignment and focus.

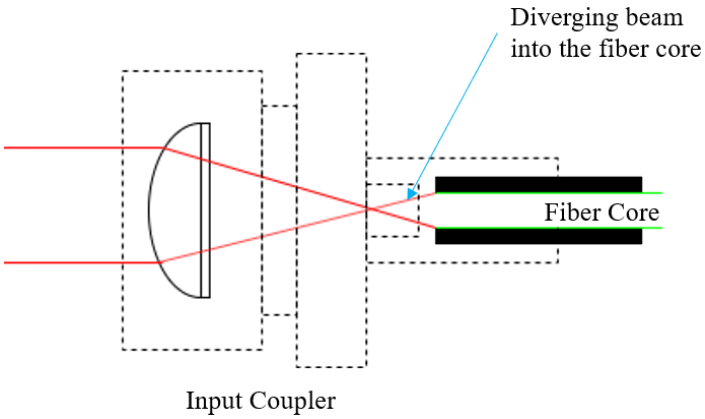


Figure 54 – Schematic of laser beam coupling into the fiber

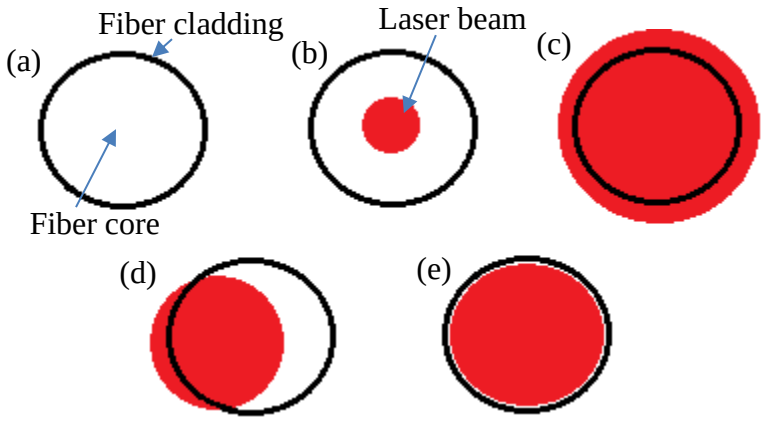


Figure 55 – Different possibilities in coupling the laser beam into the fiber

(a) No beam (b) Beam is aligned but focused too small (c) Beam is aligned but focused too large (d) Beam is misaligned (e) Proper alignment and focus

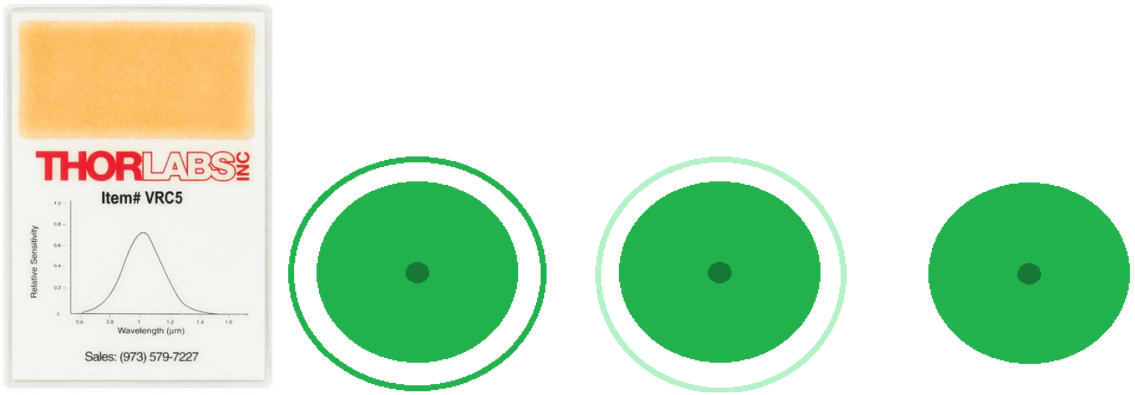
Alignment should be carried out on low laser power for the safety of equipment and the operator. Initial rough alignment can be achieved by placing a graphite coated paper over the output aperture of the input coupler. This makeshift viewing paper flashes green when irradiated with a laser which can be seen by the naked eye. The XY adjust knobs are adjusted to center the green spot as close as possible to the center of the output aperture.

Then, a copper aperture alignment tool, as shown in Figure 56, was screwed onto the input coupler's output, and the output laser power from the aperture is measured using the power meter. The adjustment knobs were varied, one axis at a time until the measured laser power is maximized. This assures that once the fiber was installed the laser would be centered on the fiber's face.

Figure 56 – A copper aperture alignment tool

After alignment is done, before setting the focus, the laser should be powered off, the copper aperture should be removed, the input coupler's focusing adjustment should be set all the way clockwise to the right end. To set the focus, the optical fiber cable is attached to the end of the input coupler, and the output of the fiber is directed into the power meter. The laser was set to low power and the focusing adjustment was then slowly turned counterclockwise until the measured power begins to decrease. The focusing adjustment is then reversed for a quarter turn. At this point, the power transmission was ~91% of the input power. Proper alignment and focusing can be confirmed by laser viewing card as shown in Figure 57. The output of the fiber is directed onto the laser viewing card.

Misaligned beam in the fiber will result in a bright visible ring around the laser spot as shown in Figure 57. A well-defined spot on the card means alignment and focusing were successful.



Ref: ThorLabs & U.S. Laser Corp.

Figure 57 – Laser viewing card and possible fiber alignment outputs

Other standard calibrations such as calibrating the position of the laser incident point with respect to the center of the camera's field of view and calibrating the relative position between the center of the camera's field of view and the center of the interferometer probe (within 5 µm accuracy) are performed according to the standard calibration procedure detailed in operation manual [58].

4.3 Safety Features

Precise positions of the laser incident spot and interferometer probe head are key features in a successful inspection of the test samples using the LUI system. Hence, it is paramount that the interferometer probe does not collide with the end effectors. Any collision would disrupt the alignment of the probe and possibly damage the internal lens

or other components of the system. A new safety system using Hall Effect sensors and neodymium magnets is devised to prevent any possible collision of interferometer head and end effectors as shown in Figure 51. Hall Effect sensors are arranged around the interferometer probe while the magnets are mounted over the end effectors. The Hall Effect sensors output an analog signal to a custom-designed microcontroller circuit. The closer the magnets are to the sensors the greater their output voltage. If that voltage surpasses a predetermined threshold, the microcontroller will shut off a relay controlling power to the system. This will stop the system in a fraction of a second to prevent the collision. An emergency stop button is installed to stop the system manually to the safety in case of any unusual occurrences observed by the operator.

4.4 Advantages of DALUS

The enhanced DALUS is a superior system over SLUS. The system can deliver high laser power with low laser energy density onto the test sample to produce high strength ultrasound. This system can be used for large test samples with high throughput. High signal strength also produces signals with better SNR. Because of multiple fibers with less bend radius, compact size is possible for the overall system. It has a high sensitivity to detect micro-level defects and failures. The advantages and performance of DALUS are discussed in the next chapter in detail.

CHAPTER 5. DALUS VERIFICATION AND TECHNICAL CAPABILITY STUDIES

To investigate the benefits of the dual fiber array LUI system, a series of tests were conducted using either one or two laser excitation points with different laser power levels. For the single beam tests, one of the fibers in DALUS was removed from its end effector and attached to a light absorbent container. Since the multiplexer splits the power coming from the laser, the output was doubled to compensate for the power, for single beam tests.

5.1 Damage Metrics for Silicon Die

This section is intended to show the calculations for the temperature and laser energy density on the sample surface, to demonstrate that the laser is not damaging the sample surface. The laser power needs to be set high enough to generate good strength ultrasound, and low enough to avoid causing damage to the incident surface. Scruby (Laser Ultrasonics) explained the calculations to plot a rise in temperature as a function of time, for a range of depths below the surface of the aluminum and mild steel, in response to a pulse of laser energy, calculated from Equation (2) [30]. DALUS typically uses a 5 ns laser pulse duration with a 20 Hz repetition rate. The maximum laser power carrying capacity of 1000 µm core optical fiber is 200 mW. The temperature profile T(t) as a function of time ‘t’, for a range of depths below the surface of the silicon die in response to an incident laser pulse of energy 200 mW and pulse duration 5 ns, is derived using Equation (2), and using parameters in Table 2.

When $t \leq t_0$

$$T(z,t) = \frac{2I_0(\kappa t)^{1/2}}{K} ierfc\left(\frac{z}{2(\kappa t)^{1/2}}\right)$$

And when $t > t_0$

$$T(z,t) = \frac{2I_0(\kappa t)^{1/2}}{K} ierfc\left(\frac{z}{2(\kappa t)^{1/2}}\right) - \frac{2I_0(\kappa (t-t_0))^{1/2}}{K} ierfc\left(\frac{z}{2(\kappa (t-t_0))^{1/2}}\right) \quad (2)$$

Integrated error function = $ierfc(\zeta) = \frac{1}{\sqrt{\pi}} e^{-\zeta^2} - \frac{2\zeta}{\sqrt{\pi}} \int_{\zeta}^{\infty} e^{-\xi^2} d\xi$

$$I_0 = \frac{E_0}{At_0} = \frac{Absorbed\ laser\ energy}{Laser\ Spot\ Area} = \frac{(1-R)E}{At_0}$$

Table 2 – Parameters in Equation (2) and values for silicon die

Symbol	Parameter	Value for Silicon die
z	Depth below the surface of Silicon Die	Varies
K	Thermal conductivity	80 W/m-K
ρ	Density	2330 kg/m^3
C	Specific thermal capacity	712 J/kg-K
κ	Thermal diffusivity = K/ρC	103 x 10^{-6} m^2/s
P	Pulse repetition rate	20 Hz
W	Average laser power	200 mW
E	Incident laser energy = W/P	10 mJ
R	Reflectivity	0.43
A	Laser excitation spot area	6.14 mm^2
t_0	Pulse duration	5 ns
I_0	Absorbed laser flux density	1.86 x 10^7 W/mm^2

The elliptical laser excitation spot area for 1000 µm core optical fiber at a 45° incident angle is ~6.14 mm^2. The reflectivity of photons at a wavelength of 1064 nm for silicon is 0.43 at the incidence angle of 45°. The temperature profile is plotted in Figure 58

for a range of depths below the surface of the silicon die, with a laser power of 200 mW. The maximum temperature attained on the surface of the sample is around 1149 K, and it quickly cools down to below 450 K in 50 ns and reaches room temperature in 0.1 ms. Considering the melting point of silicon as 1690 K, the temperature profile in Figure 58 is not supposed to cause any damage to the incident surface.

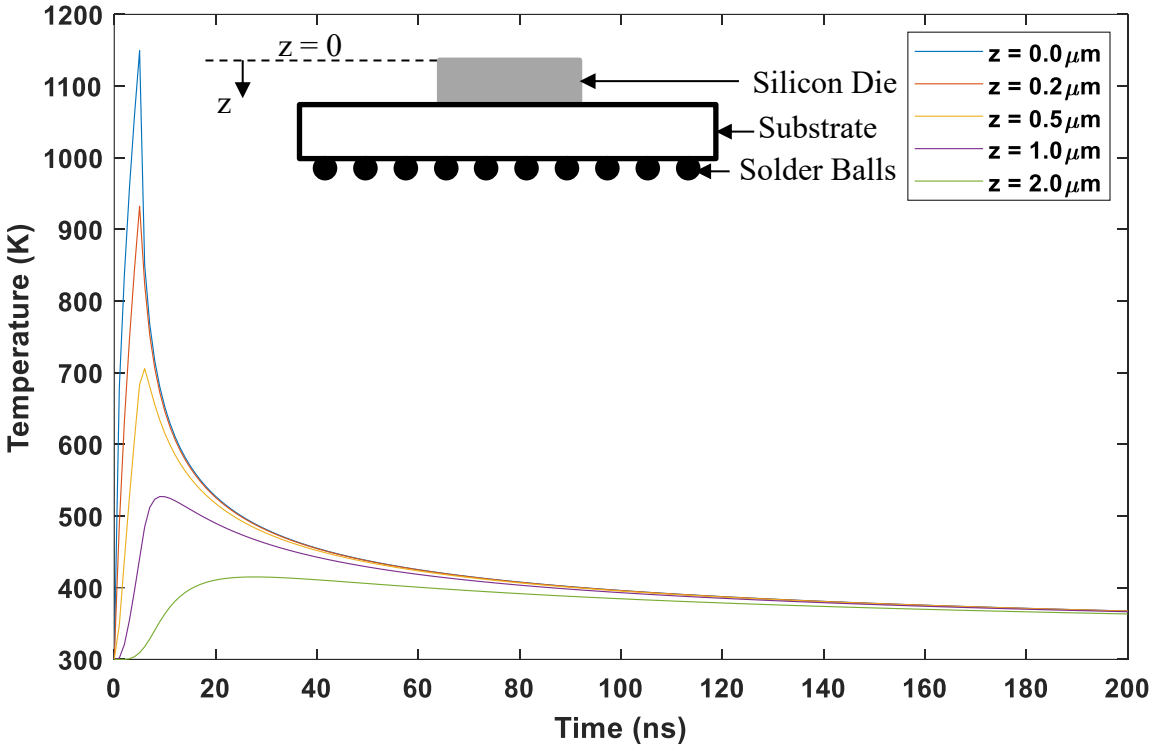


Figure 58 – Temperature profile for a range of depths below the surface of the silicon die in response to an incident laser pulse of energy 200 mW and pulse duration 5 ns

Dixon's study on ultrasound generation in single-crystal silicon reported that the transition from thermoelastic to ablation regime occurs above an energy density of 0.18–0.23 J/cm^2 [60]. In LUI system, with the elliptical laser excitation spot of about 6.14 mm^2 and average laser power of 200 mW, the approximate energy density is 0.16 J/cm^2.

Therefore, LUI system parameters guaranteed that only ultrasonic waves in the thermoelastic regime were generated.

Further, optical microscopy and SEM images are taken on the die surface after exposing the die surface to actual laser pulses for more than 40 hours. The optical microscopy image is shown in Figure 59 and the SEM image is shown in Figure 60. It may be noted that these images are stitched images of high magnification of scale (20X for optical microscopy and 35X for SEM). Both the optical microscopy image and SEM image have shown no signs of laser damage on the die surface. A typical LUI experiment takes a maximum of 3 hours of laser exposure. Hence, it is verified that the experimental laser settings generate ultrasonic waves in the thermoelastic regime.

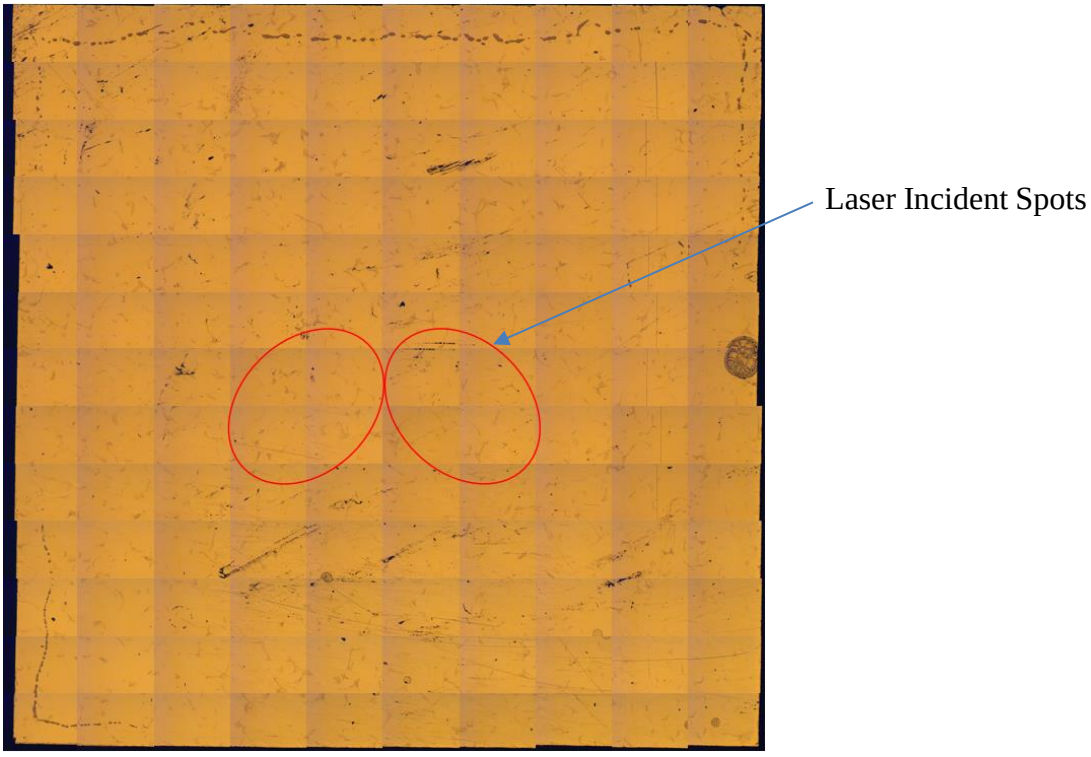


Figure 59 – Optical microscopy of die surface showing no signs of damage due to laser incidence

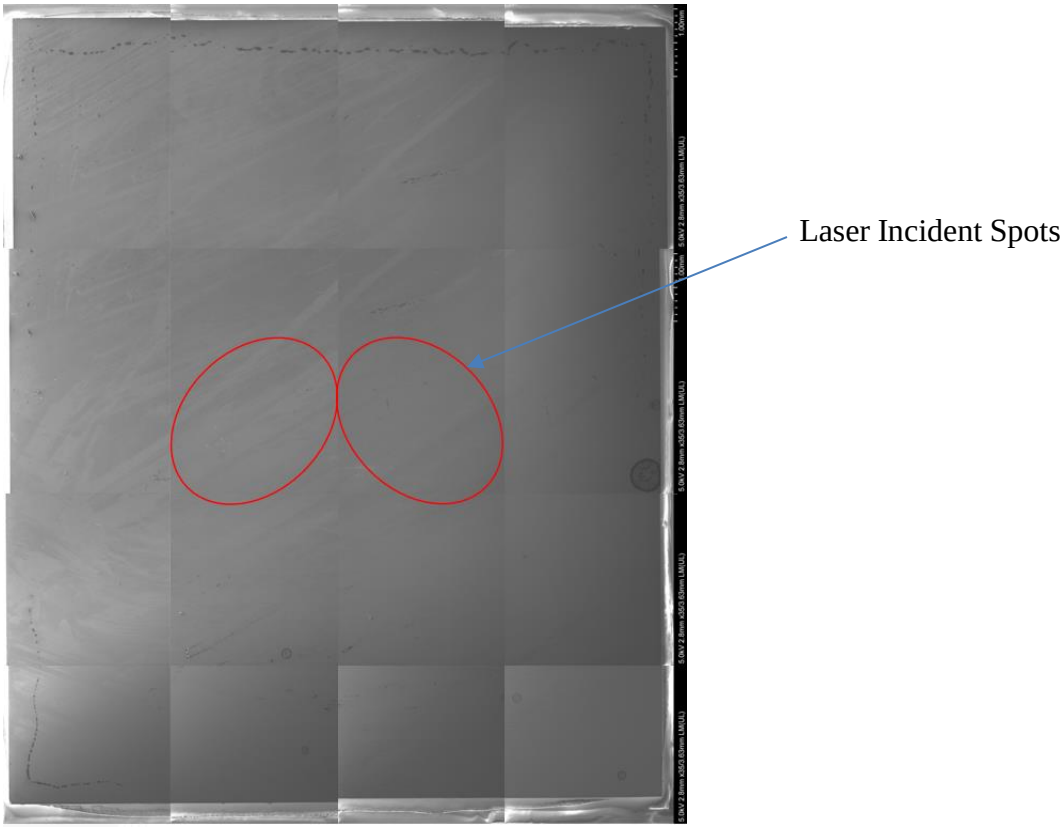


Figure 60 – SEM image of die surface showing no signs of damage due to laser incidence

5.2 Effect of Spacing between the Laser Excitation Spots

Preliminary experiments were carried out to check the effect of spacing between laser excitation spots. It is observed that MCC values at few locations are not the same with and without spacing between laser excitation spots and some of the known defects/failures are not being detected with spacing more than 2 mm between the laser spots. This is attributed to the inference fringe wave pattern that will be formed with the spacing of laser excitation spots. A schematic image showing an interference fringe pattern is shown in Figure 61. The white lines in Figure 61(a) is the destructive interference region. If a defect/failure exists in the destructive interference region, the interferometer may not

acquire any signature signal of the defect and the system may not identify the defect/failure. It is not expected to generate any interference pattern with a close distance between the laser excitation spots as shown in Figure 61(b). With the preliminary studies, it is observed that there is no special advantage with the spacing between the laser excitation spots. Therefore, it is decided to place the two laser excitation spots just touching each other as shown in Figure 61(c), to avoid the formation of any possible interference fringe pattern and to deliver as high laser power as possible within thermoelastic regime to produce high strength ultrasonic waves.

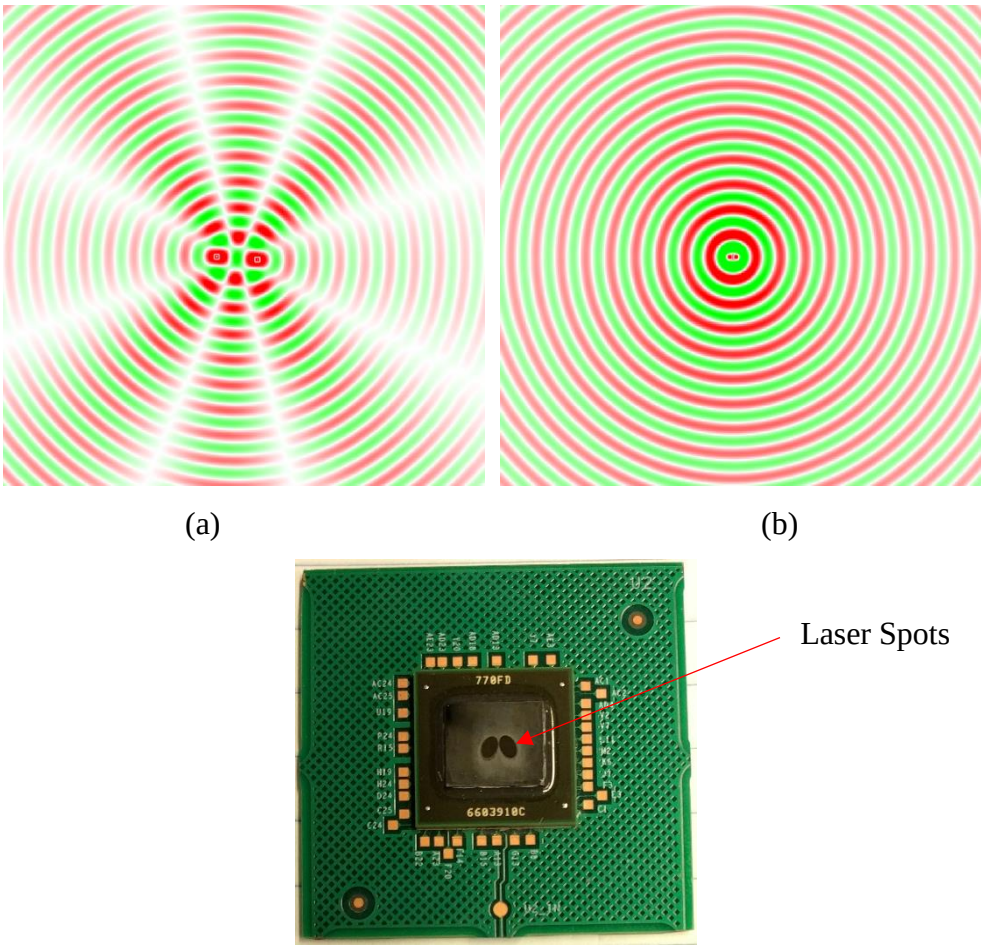


Figure 61 – Wave patterns with the spacing of laser excitation spots

(a) Interference fringe pattern formed with some significant spacing between laser excitation spots (b) No interference pattern will be formed with no/minimum spacing between laser excitation spots. (Ref: http://www.falstad.com/ripple/) (c) Laser spots on physical test sample covered with carbon coating

5.3 Performance Comparison between DALUS and SLUS

As discussed earlier, the laser power from the single beam laser system was not sufficient to vibrate the chip package with sufficient amplitude. In particular, if the multilayered package's footprint is large, the signal attenuates quickly within a short distance [30]. A comparison of major features between SLUS and DALUS are shown in Table 3 below.

5.3.1 Laser Power and Energy Density

SLUS is limited in terms of the fiber power carrying capacity and laser energy density on the chip package. In SLUS, the area of laser incidence spot with 600 µm core diameter of the fiber is 2.5 mm^2, giving an approximate energy density of 0.14 J/cm^2 [39]. Delivering high laser power results in high energy density, which can ablate the surface of the package. Experiments have shown that 70 mW can cause damage to the silicon die by thermal ablation with 2.5 mm^2 laser incident area. DALUS has fibers of 1000 µm core diameter and the area of laser incidence spot of 6.14 mm^2, which can deliver maximum power of 200 mW with an energy density of 0.16 J/cm^2.

Table 3 – Comparison of major features between DALUS and SLUS

Parameters	DALUS	SLUS
Fiber core diameter	1000 µm	600 µm
Number of Fibers	2	1
Coupling efficiency	Up to 86.5%	Up to 90%
Maximum power carrying capacity of fiber	200 mW	100 mW
Maximum total power delivered onto the surface of test vehicle without ablation	400 mW	70 mW
Maximum energy density	0.16 J/cm^2	0.14 J/cm^2

5.3.2 Signal Strength

A comparison of transient out of plane displacement signals at a data collection point on 52.5 x 52.5 FCBGA package (shown in Figure 65 in CHAPTER 6), from SLUS with laser power of 40 mW and DALUS with total laser power of 80 mW, is shown in Figure 62. It may be noted that SLUS here infers DALUS with only one laser beam. As shown in Figure 62 that DALUS is effective for generating very strong ultrasound signals. The peak to peak amplitude obtained with DALUS is three times that obtained by using a SLUS. Experiments have also shown that 200 mW laser power can produce good interferometer signal strength at a maximum distance of 35 mm from the laser incident point on the 52.5 x 52.5 FCBGA package.

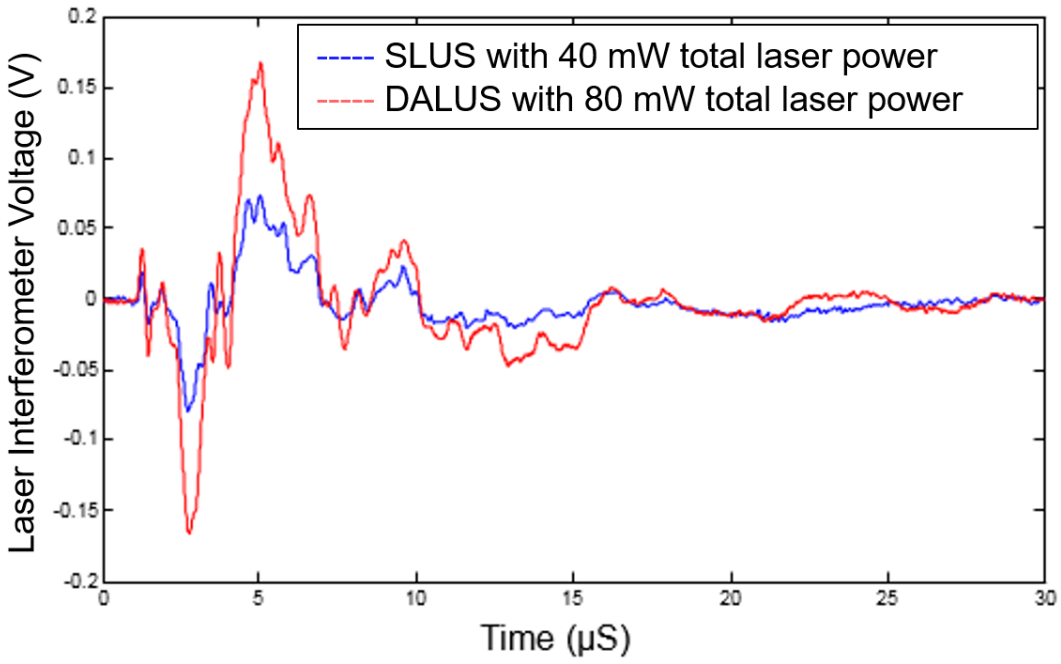
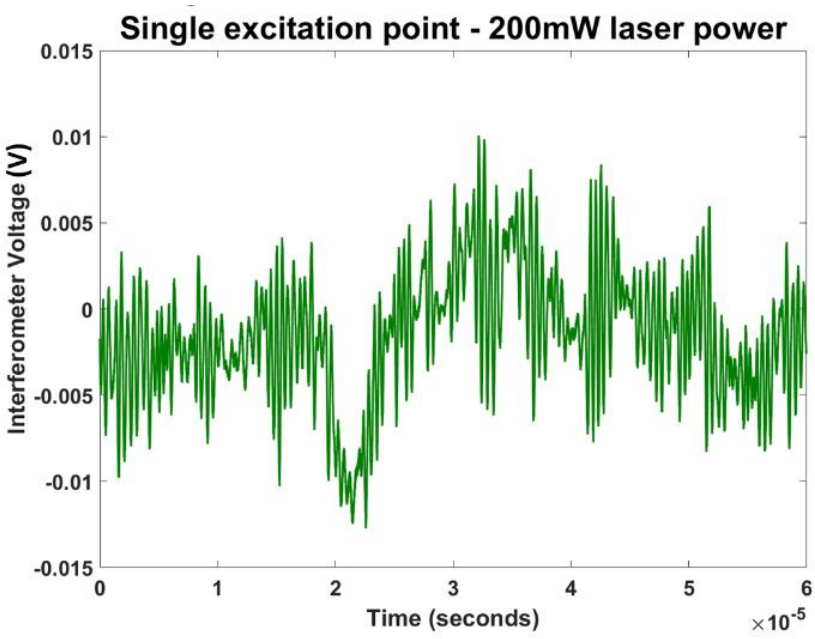


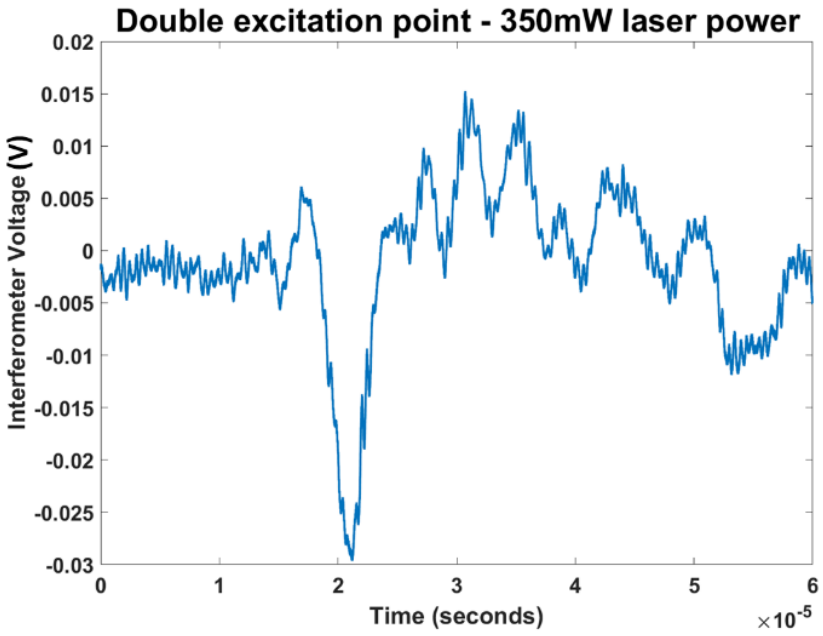
Figure 62 – Comparison of transient out of plane displacement signals from DALUS and SLUS

5.3.3 Signal-to-Noise Ratio (SNR)

A high amplitude signal can further yield better SNR, which is very important in detecting minor defects/failures such as intermetallic cracks, pad cratering, and partial delamination. The displacement signals acquired at one of the data collection points on 52.5 x 52.5 FCBGA package (shown in Figure 65 in CHAPTER 6) by exciting at the center of the die using SLUS (infers DALUS with only one laser beam) with 200 mW laser power and DALUS with total laser power of 350 mW, is shown in Figure 63.



(a)



(b)

Figure 63 – Vibrational response at a DCP on a 52.5 x 52.5 FCBGA package using (a) SLUS with 200 mW laser power, and (b) DALUS with 350 mW total laser power

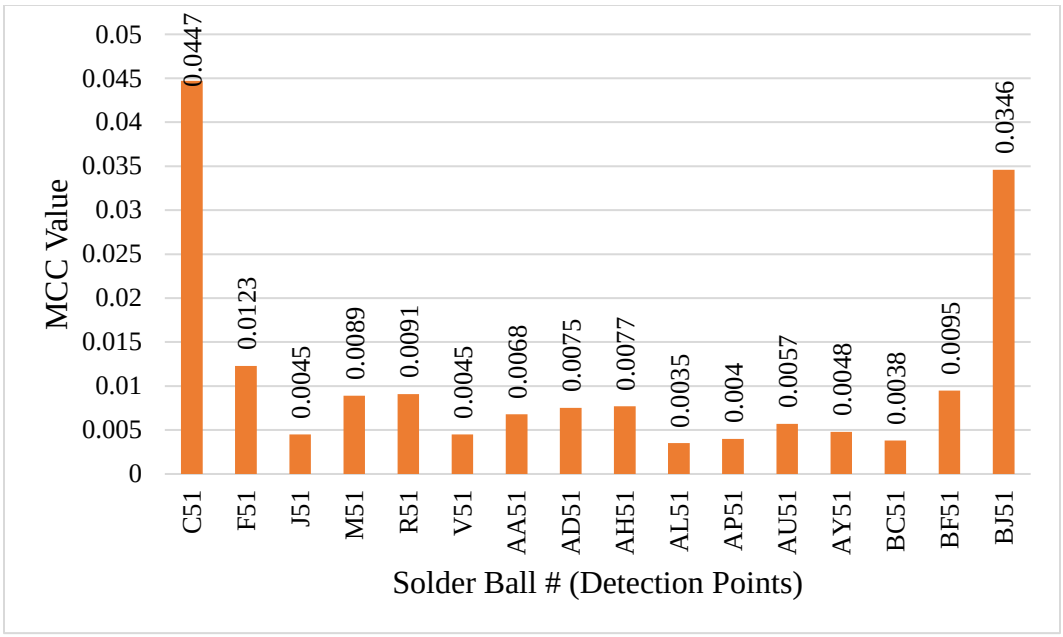
It is clearly seen that even though the laser was operating near the damage threshold, the interferometer voltages produced with SLUS are of insufficient amplitude to produce a clean signal. From Figure 63(a), SNR is estimated to be 1:1 with a peak to peak amplitude of both signal and noise at 0.01 V for single laser excitation. On the other hand, with the increased energy of DALUS, a well-defined signal was obtained as shown in Figure 63(b). An estimate of the SNR is as high as 8:1 with a peak to peak signal amplitude of 0.04 V and a peak to peak noise amplitude of 0.005 V. The eight-fold improvement in SNR would allow the inspection of larger and more complex chip packages using DALUS.

5.4 Throughput of DALUS

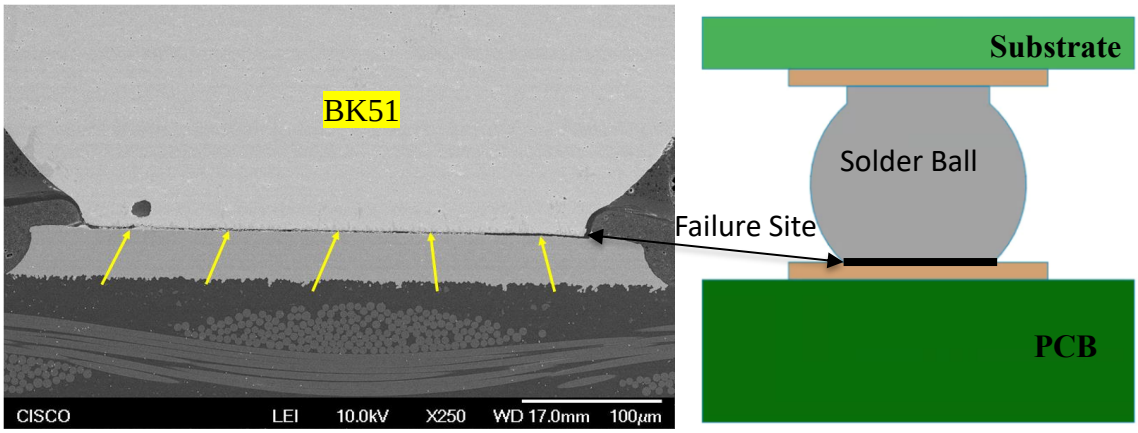
The overall throughput of DALUS depends on several parameters such as laser repetition rate, number of signals to average, alignment time, number of DCPs, speed of the stages, time for autofocusing/local searching, and speed of data acquisition and analysis. To test a family of a particular chip package, the initial setup time can take several minutes. But, once this initial setup is completed, testing other chips in the same family is very fast and can take less than 15 seconds per DCP, almost the same as with SLUS. However, in case of SLUS, larger packages need to be subdivided (subdivision of 52.5 x 52.5 FCBGA sample is shown in Figure 66 in in CHAPTER 6), to excite the individual package section to acquire sufficient strength interferometer signal with reasonable SNR. No such subdivision is required for DALUS; thus, it is expected to greatly increase the system's overall throughput for large and complex chip packages.

5.5 Resolution/Sensitivity

The system has the potential to detect defects/failures such as micro-cracks (Intermetallic crack or pad cratering) below 2 µm size with increased laser power and high spatial resolution. With the 52.5 x 52.5 FCBGA packages (shown in Figure 65 in CHAPTER 6) subjected to drop test, the system could detect pad cratering and Inter-Metallic Compound (IMC) cracks of vertical separation below 2 µm. The LUI results on a 52.5 x 52.5 FCBGA test vehicle on a column of solder balls are given in Figure 64(a), and Figure 64(b) shows SEM image of the corner solder ball in the same column (column 51). High MCC value of 0.0346 at the corner corresponding to IMC crack in the solder ball BK51 of vertical separation below 2 µm as shown in Figure 64. Horizontal separation of more than 20% of the solder ball width can be detected by DALUS. The detailed discussions about these results are presented in section 6.4. DALUS has not yet been tested to its limits to determine the system's resolution/sensitivity, because of the limitations in getting samples with very small defects/failures from our industrial partners. It is believed that the system can detect sub-micron level defects/failures. To determine the final sensitivity/resolution of the system, more samples with sub-micron level defects/failures shall be tested in the future.



(a)



(b)

Figure 64 – Demonstration for the sensitivity of DALUS

(a) Sample LUI results on a column of solder balls for 52.5 x 52.5 FCBGA package, and (b) SEM image of corner solder ball corresponding to MCC value of 0.0346 showing IMC crack with a vertical separation of about 2 µm size

CHAPTER 6. EVALUATION OF FCBGA SAMPLES SUBJECTED TO MECHANICAL RELIABILITY TESTS

SLUS was demonstrated successfully on flip-chip packages, CSPs, LGA packages, Multilayer Ceramic Capacitors (MLCCs), and PBGA packages. Modern packages such as FCBGAs have not been investigated as SLUS is not capable of inspecting those packages. The developed DALUS is employed to detect failures in advanced area-array microelectronic packages subjected to drop testing, thermal-cycling test, and mechanical bend testing. As these tests produce different sizes and nature of cracks at various locations within the solder interconnects, the utility of the developed DALUS is demonstrated. This chapter focuses on the evaluation of large FCBGA samples subjected to drop testing and four-point bend testing.

6.1 Test Vehicles

FCBGA test vehicles subjected to drop testing and four-point bend testing were supplied by Cisco. The image of the physical board along with the dimensions is shown in Figure 65. The test vehicle consists of an FCBGA package that was assembled on a high Glass Transition Temperature (Tg) FR4 PCB of size 180 mm x 180 mm. Lead free SAC 305 (96.5 Sn – 3% Ag – 0.5% Cu) solder balls are used as interconnections. The FCBGA package has a large footprint of size 52.5 mm x 52.5 mm and a thickness of 2.64 mm. The package also has a relatively large flip-chip die of size 18.5 mm x 20 mm with underfill between the flip-chip and BGA substrate. In total 2597 BGA solder balls of each 0.5/0.6 mm diameter at a pitch of 1 mm are arranged in 51 x 51 area-array. Such a robust package

is relatively difficult to evaluate with any of the present non-destructive techniques. Large packages tend to have significant warpage, which is another principal reason for the evaluation of the FCBGA package using acoustic microscopy is almost not possible.

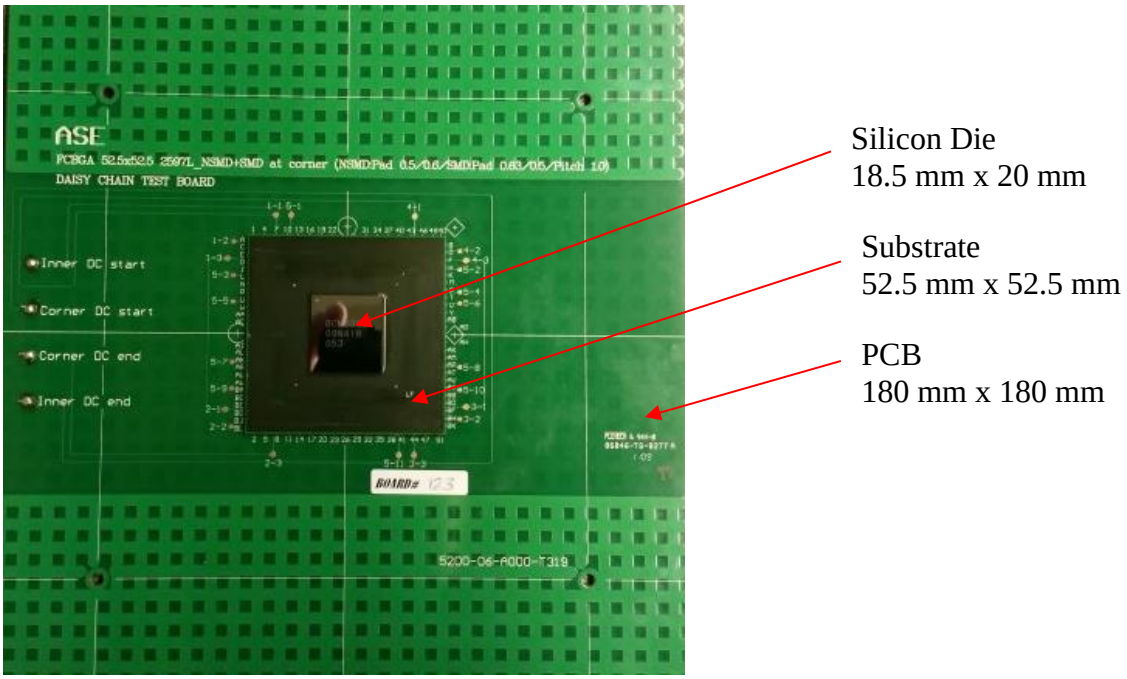


Figure 65 – Test vehicle with 52.5 x 52.5 FCBGA package

A total of 17 test vehicles, as listed in Table 4, were received from Cisco and evaluated using DALUS. Some of the test vehicles were thermally treated (thermal aging) to remove thermal history. For some of the test vehicles, Solder Mask Defined (SMD) pads on the corner solder balls are used as indicated in Table 4. Out of 17, four samples (#29, #62, #123, and #126) were time-zero samples which were not subjected to any reliability testing. Upon, preliminary MCC analysis among time-zero samples, boards #29, #62, and #126 have resulted in high MCC values, which indicates that there are some damage in these three packages. Hence, board #123 was considered as a reference specimen (a gold standard) for this research. The signals obtained at DCPs on its surface are used to compare

the signals obtained from the corresponding points on each of the test vehicles to measure MCC and identify the failures. Initially, the reference board #123 was assumed to have no defects/failures. After completing our experiments, board #123 was cross-sectioned to verify that board #123, in fact, has no significant defects/failures.

Table 4 – 52.5 x 52.5 FCBGA test vehicles and their pre-conditions

Board ID #	Type	Thermal aging	Reliability test	Reliability Test Condition	Electrical Testing Result
2	NSMD		FPBT	Not Available	Good
3	NSMD		FPBT	Not Available	Good
20	NSMD		FPBT	Not Available	Not Available
50	NSMD	150 °C / 500 hrs	FPBT	4 mm/sec, 6 mm max	Good
66	NSMD+SMD	100 °C / 500 hrs	FPBT	4 mm/sec, 5 mm max	Failed
80	NSMD+SMD	150 °C / 500 hrs	FPBT	Not Available	Not Available
113	NSMD+SMD		FPBT	4 mm/sec max 6 mm	Failed
9	NSMD		DT	200G; 3 +z and 3 –z drop cycles	Good
41	NSMD	100 °C / 500 hrs	DT	200G; 3 +z drop cycles	Failed
83	NSMD+SMD		DT	150G pass and then failed after 2 –z cycles of 200G	Failed
86	NSMD+SMD	75 °C / 500hrs	DT	100G 20 cycle start to fail	Partial Failure

Table 4 continued

107	NSMD+SMD		DT	200G; 3 +z drop cycles	Failed
117	NSMD+SMD		DT	100G 16 cycle	Failed
29	NSMD	Time-zero Sample			
62	NSMD	Time-zero Sample			
126	NSMD	Time-zero Sample			
123	NSMD	Time-zero Sample - Reference Board			

NSMD: Non-Solder Mask Defined

SMD: Solder Mask Defined

FPBT: Four-Point Bend Testing

DT: Drop Testing

6.2 Inspection Procedure

The system parameters used for the evaluation of 52.5 x 52.5 FCBGA packages using DALUS are listed in Table 5. High strength ultrasound and proximity of the DCP to the defect/failure are two key elements in detecting a defect/failure in the LUI method. Ultrasound signal intensity is maximum in the proximity of the laser incident point and attenuates with distance away from the incident point. Soft materials, multiple interfaces, and uneven geometry make the elastic waves attenuate faster and at shorter distances. The 52.5 x 52.5 FCBGA is a large package with soft underfill and has 11- layered substrate. In order to receive a good interferometer signal (high amplitude signal), two options are explored: i) using very high power laser and making it incident at the center of the package on top of the die, ii) dividing the package virtually into 9 sections, as shown in Figure 66, and making the low power laser to fire at the center of each section while collecting interferometer signal at DCPs in that section. The power of the laser that can be delivered

to the package is limited by the power-carrying capacity of the optical fiber and the thermoelastic temperature limit of the incident surface. Therefore, option 2 of dividing the package into 9 sections was selected in this research. Experiments were also conducted for a full package without dividing it into sub-sections by pulsing the laser on top of the flip-chip center [46]. To inspect a full package all at once, high laser powers, on the order of 400 mW, were used to have sufficient signal strength at each DCP.

Table 5 – System Parameters for the evaluation of 52.5 x 52.5 FCBGA test vehicles

Total average pulsed laser power	80 mW
Laser wavelength	1064 nm
Pulse duration	5 ns
Pulse frequency	20 Hz
Interferometer sampling rate	50 x 10^6 samples/s
# sample points considered for MCC	3000
Signals average per DCP	128

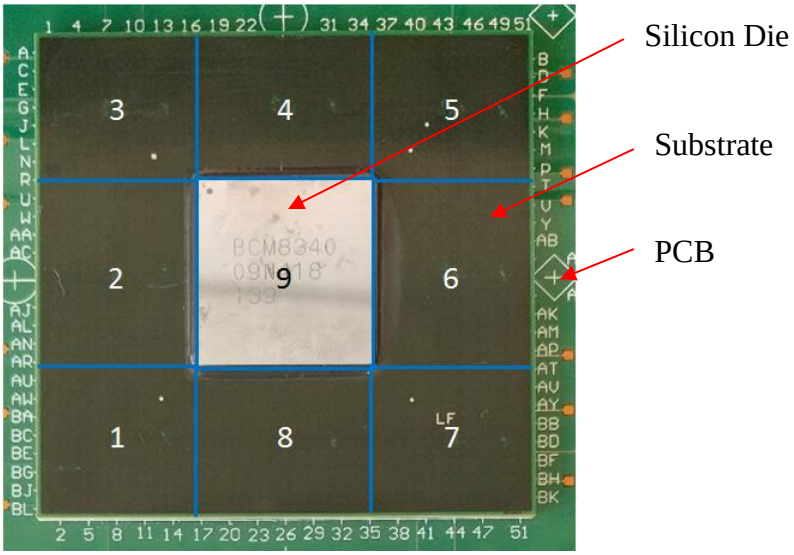


Figure 66 – Virtual sub-division of the FCBGA package into 9 sections (Section 9 is dedicated to the die)

The solder ball locations are usually chosen as the DCPs to collect the interferometer data/signal to determine the quality of that solder ball. However, the total inspection time depends on the number of DCPs. If the solder ball density (number of solder balls per unit area) is high, a certain number of solder balls can be grouped to have a representative DCP, preferably at the center of these grouped solder balls. In this way, the total number of DCPs can be reduced to reduce the overall time of the inspection. If required, further analysis can be performed by creating more DCPs within a group for the purpose of inspection.

The current FCBGA package has 2597 BGA solder balls in total. To reduce inspection time, a DCP was chosen for every 3 x 3 array of BGA solder balls, indicated as field-of-inspection. A defect or anomaly or failure at any solder ball in the 3 x 3 array (field-of-inspection) can affect the interferometer signal at that DCP. The X-ray image of the package showing 9 sections along with a zoomed image for the inspection pattern for section 5 superimposed on the X-ray image is shown in Figure 67. In Figure 67, black circular areas are BGA solder balls, green lines are section borders, dark blue squares are field-of-inspection (3 x 3 array of BGA solder balls that each DCP targeted), and light blue spots indicate DCPs. MCC values at each DCP portray the collective information of the surrounding 3 x 3 solder balls in the field-of-inspection. The laser incident or excitation spot is at the center of the section while collecting the interferometer data from DCPs in that section. It may be noted that for solder balls along the edges, one DCP was chosen for 3 solder balls as shown in Figure 67.

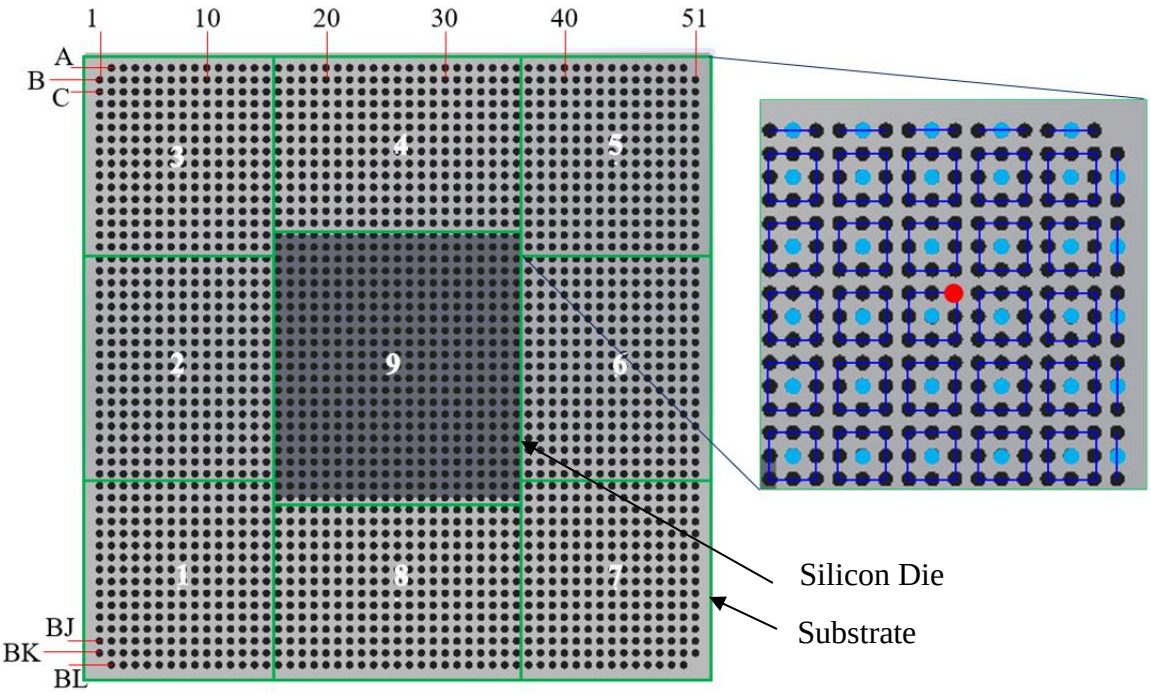
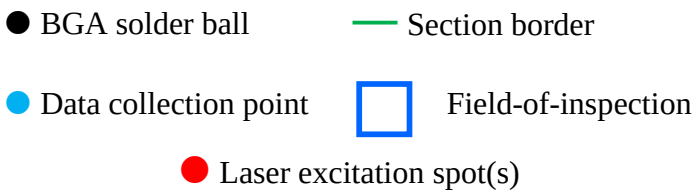


Figure 67 – Inspection pattern for section 5 overlaid on an X-ray image of the package



6.3 Evaluation of FCBGA samples subjected to Four-Point Bend Testing

6.3.1 Four Point Bend Test Setup

Bend testing is useful to predict the bounds of bending load conditions that the package can handle in a real-life scenario. Seven test vehicles listed in Table 4, underwent a four-point bend testing for reliability. The four-point bending load conditions and experimental schematic are shown in Figure 68. A support span of 140 mm length and a

load span of 85 mm length were used in this four-point bending test. The strain rate controlled by crosshead traveling speed was used as input loading. In-situ monitoring of the board strain was carried out using a strain gauge attached at the bottom of the PCB. From the available data, a crosshead traveling speed of 4 mm/sec was applied for maximum crosshead travel of 5 mm or 6 mm. Failure was detected by monitoring electrical continuity in the daisy chain while bending the board. A 20% increase in resistance value was considered a failure. A failure could be a partial or a complete solder joint crack or delamination. The electrical test results for each board are also presented in Table 4.

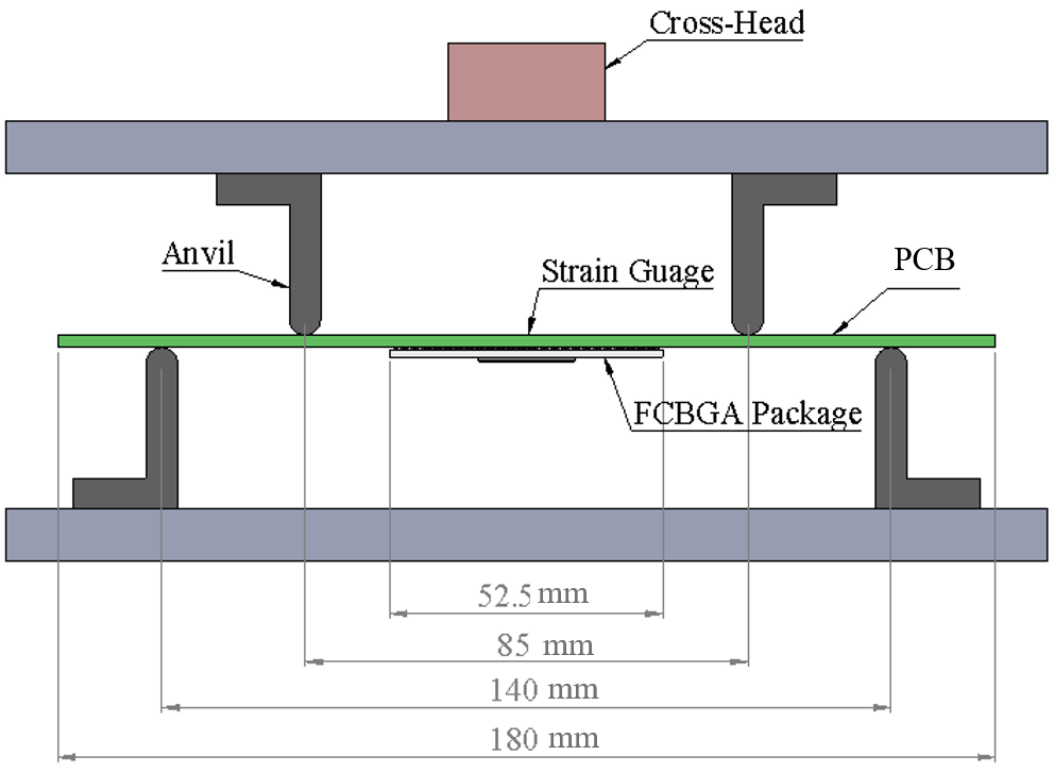


Figure 68 – Four-point bend testing set-up

6.3.2 Four-Point Bend Testing Finite-Element Simulations

Under the four-point bending test, the BGA solder balls (or second-level interconnections) in the FCBGA package are sensitive to the deflection of the PCB. Finite-element simulation can be used to effectively visualize the failure trends in BGA solder balls caused by these four-point bending test conditions [61]. ANSYS Workbench R18.1 was used for the finite-element simulations. A quarter model FCBGA package, as shown in Figure 69, was built with symmetric boundary conditions and loading parameters of 6 mm maximum deflection with 4 mm/sec traveling speed. The model consists of five layers: PCB, BGA solder balls, substrate, underfill, and die as shown in Figure 70. The PCB and substrate materials are modeled with orthotropic properties. Solder balls are modeled with Anand viscoplastic model to represent the inelastic deformation behavior. All the remaining materials are assumed to be isotropic. Cylinders of diameter 6 mm were used to simulate the traveling anvil and supporting anvil as shown in Figure 69 and Figure 70. According to the test conditions, i) the quarter model was constrained at both symmetric planes, ii) the bottom cylindrical anvil was fixed, and iii) the maximum displacement of 6 mm with 4 mm/sec slope was applied to the top anvil cylinder. The contact between cylindrical anvils and PCB is assumed to be frictionless.

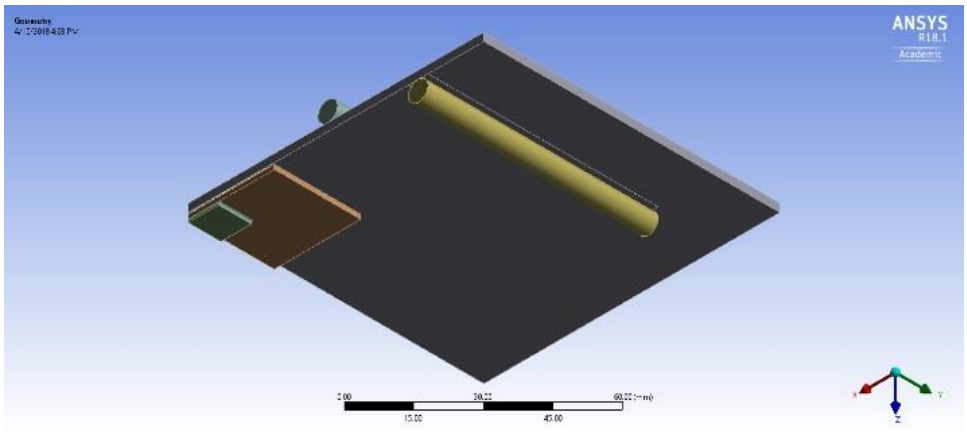


Figure 69 – A quarter model of FCBGA with cylindrical supports

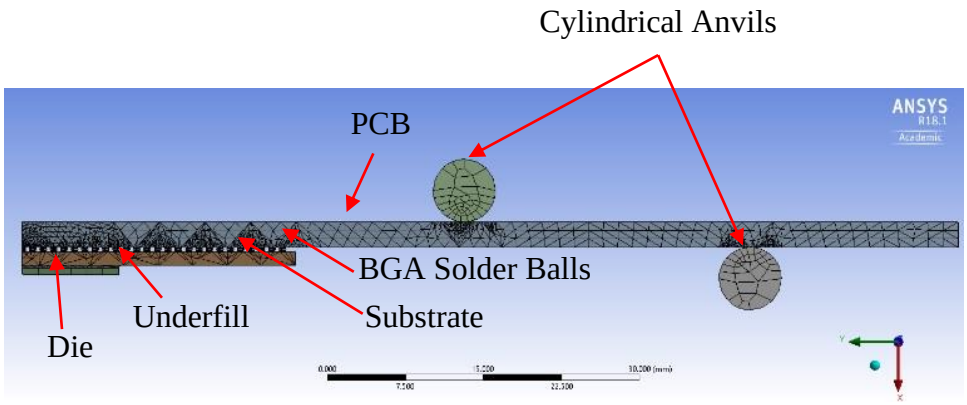


Figure 70 – Finite-element mesh model of the FCBGA package showing different components

Bending of the PCB will induce tensile loads on the solder joints, causing tensile failure of the joint. Thus, equivalent stress at the solder interface was considered for failure analysis. SAC305 solder ball joint tensile strength is reported as 41.1 MPa, and yield strength is reported as 34.2 MPa [62] [63]. When the stress at the interface between BGA solder ball and PCB or substrate is more than the tensile strength, the joint is expected to fail by producing intermetallic crack or pad cratering.

Finite-element analysis is mesh-sensitive for laminate structures [64]. In order to choose optimal mesh density (# elements per solder ball), mesh sensitivity studies have been carried out by varying mesh density in the solder balls and at interfaces in ANSYS Workbench. Hex20 element was used for solder ball mesh. As shown in Figure 71, the maximum equivalent stress in the corner solder ball increases with the mesh density. An increase from 108 elements per solder ball to 190 elements per solder ball yields only a 4.8% increase in stress. Therefore, mesh density with 108 elements per solder ball was considered as optimal for stress analysis.

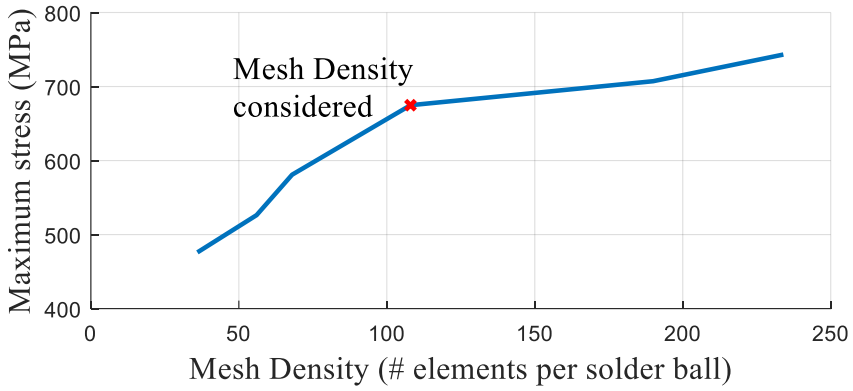


Figure 71 – Stress sensitivity to mesh density

The equivalent stress distribution on the solder balls at the interface between solder balls and PCB is shown in Figure 72. The dark blue color in Figure 72 represents stress at the interface below tensile strength and dark red represents the highest induced stress at the interface. Stress levels were correlated with the severity of crack at the interface. The solder balls in column 1 and column 2 would have separated from the laminate completely with maximum breach on the corner solder joints. The solder balls in the middle are always expected to be safe (dark blue region in Figure 72). It is also expected that the maximum number of solder balls in Row A are affected. In Row A, severe failures are predicted at

solder joints from A2 to A15, minor failures are predicted at solder joints from A16 to A18, and negligible failures or yielding is predicted at solder joints from A19 to A25. Similar stress trends have been observed in all other rows of solder balls. Further, it is also observed that the solder balls underneath the flip-chip experience very low stresses. Thus, the BGA solder balls underneath the flip-chip are not expected to fail in the four-point bend testing. These results were used for comparing LUI results, which are detailed in later sections.

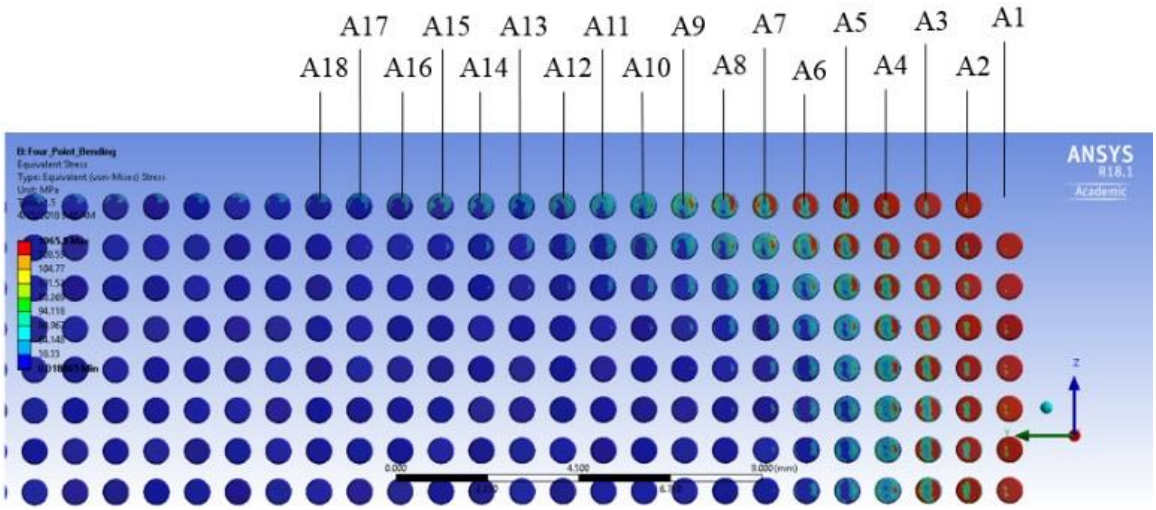


Figure 72 – Equivalent stress distribution in the solder balls at the interface between solder balls and PCB

6.3.3 LUI Results

All the test vehicles subjected to four-point bend testing listed in Table 4, were inspected using DALUS, and the results were consistent across all the boards. A similar trend of LUI results was obtained for board #2, board #3, board #20, and board #50. Board #80 and board #113 have similar LUI results trend. Hence, the LUI results on board #2, board #66, and board #113 are presented here for discussion. As discussed earlier, the LUI results are represented as MCC values by comparing the interferometer signals of test

samples against reference board #123. The MCC values at each detection point were calculated and plotted in the form of 3D histograms as shown in Figure 73 for board #2, Figure 74 for board #66, and Figure 75 for board #113.

For board #2, according to the LUI results shown in Figure 73, very high MCC values were recorded in sections 1, 2, 3, 5, 6, 7 and relatively low values were recorded in sections 4, 8, 9. This indicates severe failures in solder joints in sections 1, 2, 3, 5, 6, 7. These results are expected for a microelectronic package assembled onto a PCB and subjected to four-point bend testing.

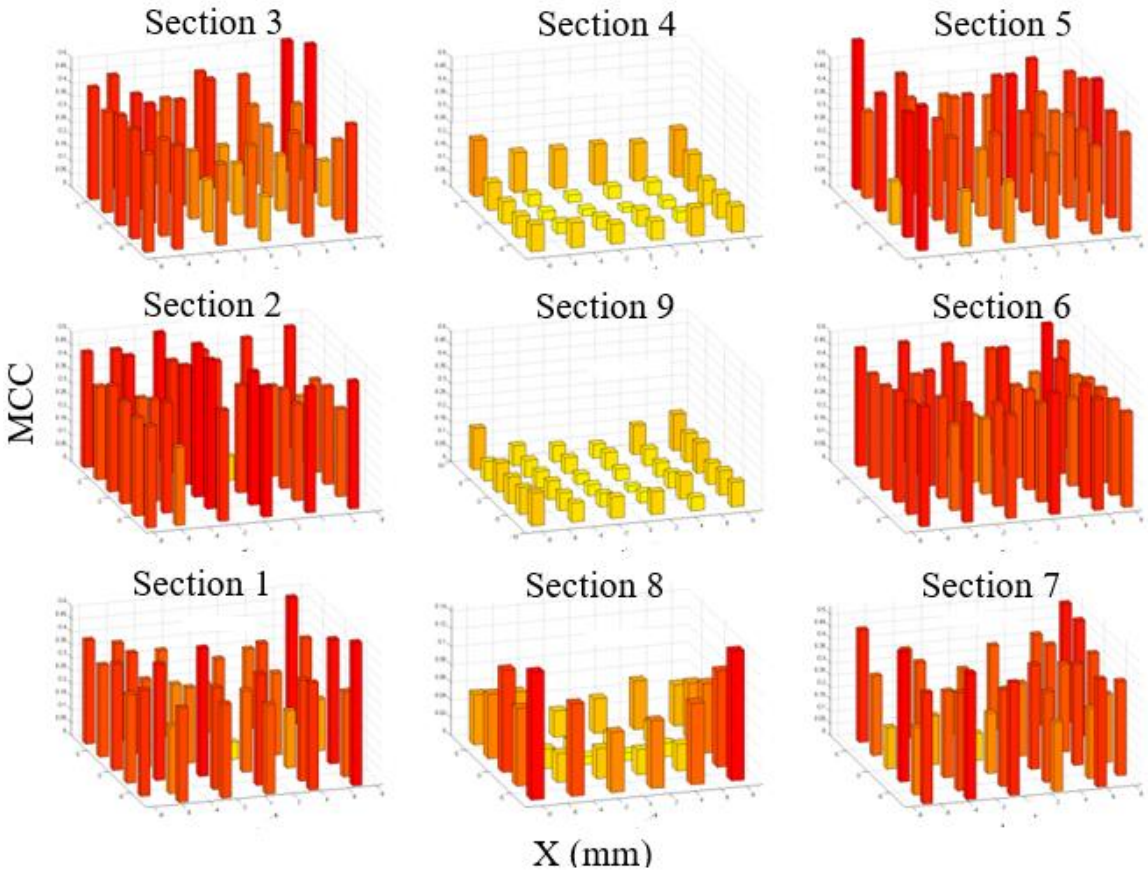


Figure 73 – LUI results (MCC values) at all DCPs for board #2 in 3D histogram format

For board #66, as shown in Figure 74, MCC values were very low across all the sections, indicating minor or no failures across all sections. However, the trend of MCC values at the outer edges of sections 1, 2, 3, and 5, 6, 7 were observed to be increasing towards the center (i.e., relatively high MCC values at the outer edges in section 2 and section 6). This clearly showed the effect of SMD pads at the corner solder balls. This indicates that SMD has more joint strength and can adhere to the laminate better, preventing separation of the solder pads from the laminate.

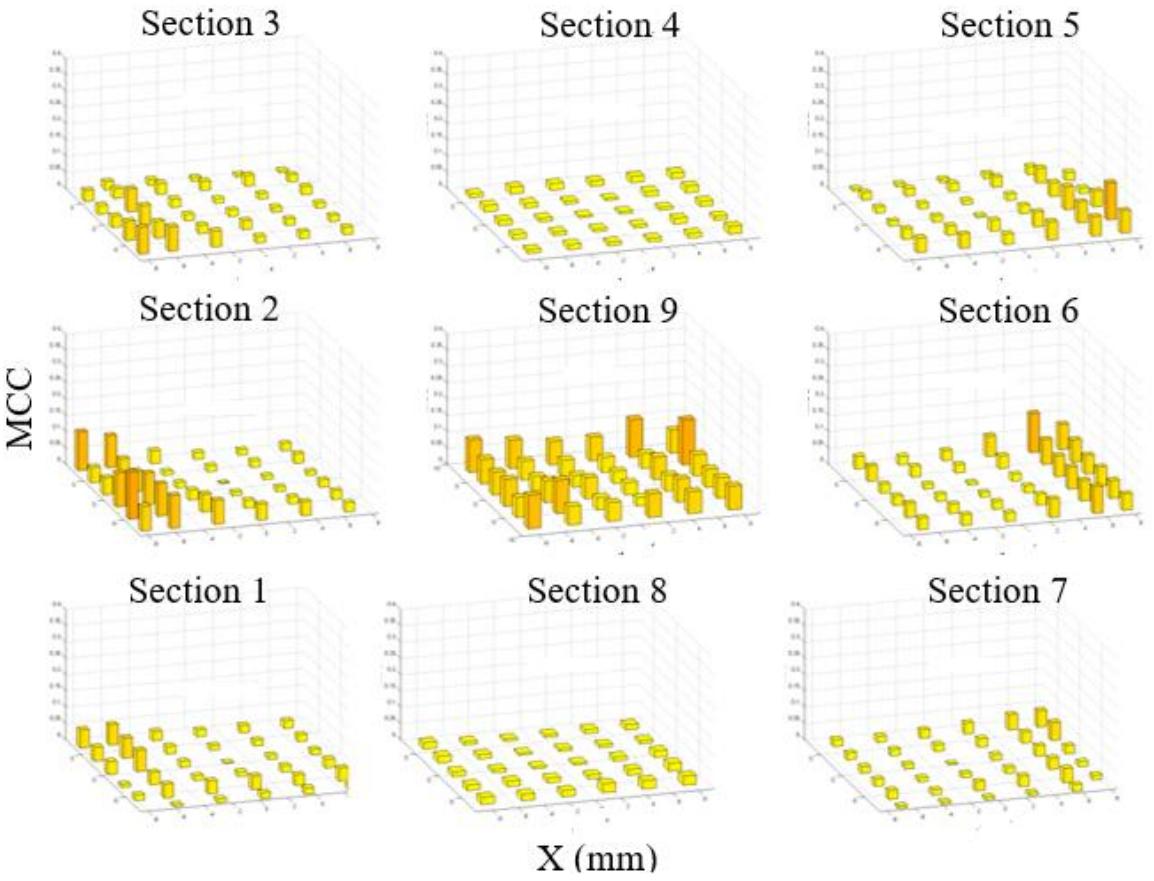


Figure 74 – LUI results (MCC values) at all DCPs for board #66 in 3D histogram format

The LUI results for board #80 and board #113 are similar as shown in Figure 75 for board #113. Unlike all the remaining boards, the LUI results for board #80 and board #113 are not symmetric with respect to anvils' neutral axis (along column 26 of solder balls). Sections 1, 2, 3, 4, 8 of the FCBGA package on board #113 have high MCC values, and sections 5, 6, 7 have relatively low MCC values. This implies severe failures are expected on left (1, 2, 3) and middle (4, 8, 9) sections, and no failures are expected in right sections 5, 6, 7. This asymmetry in the results could be due to the misalignment of the board during four-point bend testing.

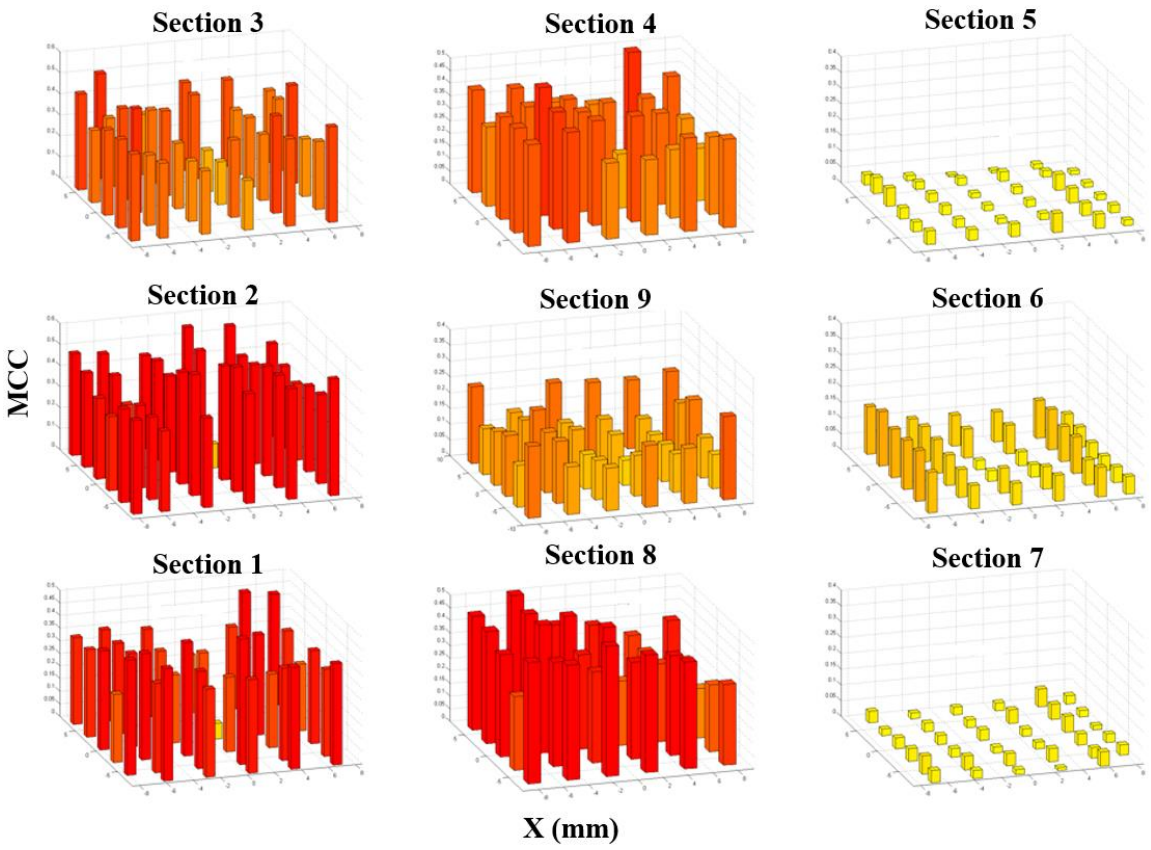


Figure 75 – LUI results (MCC values) at all DCPs for board #113 in 3D histogram format

6.3.4 Validation and Discussions

Validation of the LUI results is an important phase to justify the utility of DALUS in the microelectronic packaging industry. From the finite-element results, as shown in Figure 72, it is expected that the solder balls along the edges, parallel to the anvil (sections 1, 2, 3 and 5, 6, 7) would experience high bending stresses and probable failure of solder joints. For validation of LUI results, the packages were cross-sectioned and examined under the digital microscopy and SEM. Digital microscopy gave an initial insight into possible pad cratering of corner solder balls. SEM was carried out to further explore the cross-sectioned sample. For board # 2, and board #113, the cross-sectioning cut was made at section AA along the row of balls from ball A2 through A50 as shown in Figure 76. For board #66, two cross-sectioning cuts were made at section AA along the row of balls from ball A2 through A50 and at section VV along the row of balls from ball V1 through V51 as shown in Figure 76. It may be noted that cross-section AA doesn't contain corner solder balls A1 and A51. 2D histograms of MCC values along these cross-sections were extracted for detailed discussions and comparisons with SEM results.

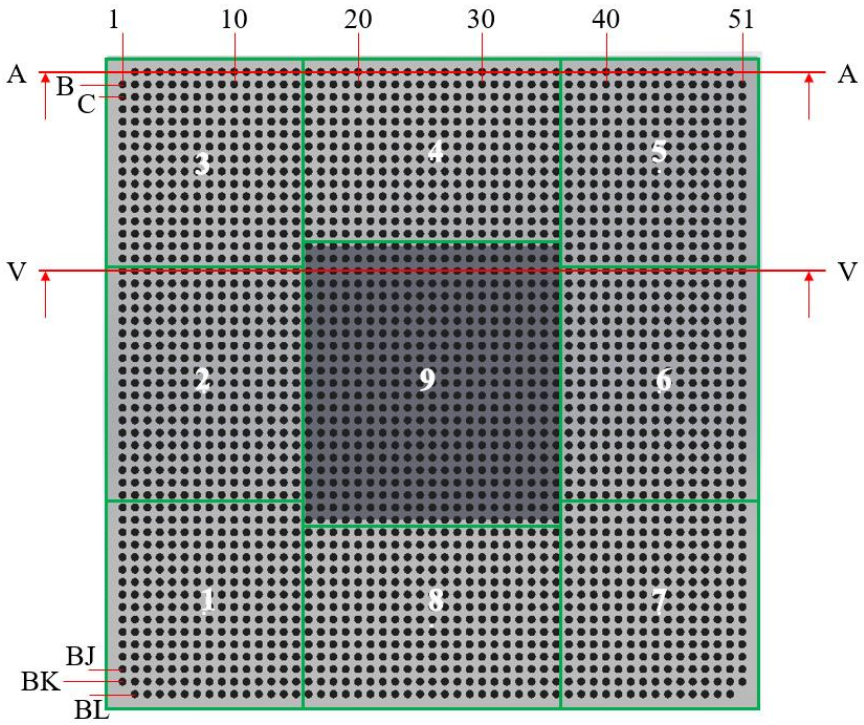


Figure 76 – X-ray image of the FCBGA package with BGA solder ball layout showing cross-section locations

A 2D histogram of the MCC values along the cross-section AA for board # 2 is shown in Figure 77. Very high MCC values are recorded on the DCPs representing A2 to A16, and A36 to A50 solder balls; high MCC values are recorded on the DCPs representing A17 to A21, and A30 to A35 solder balls; and low MCC values are recorded on the DCPs representing A22 to A29 solder balls. It may be noted that MCC values at a DCP represent the cumulative information about the failures in the field-of-inspection. For example, MCC value at DCP A3 in Figure 77, represents the cumulative information about damages in solder balls A2, A3, A4.

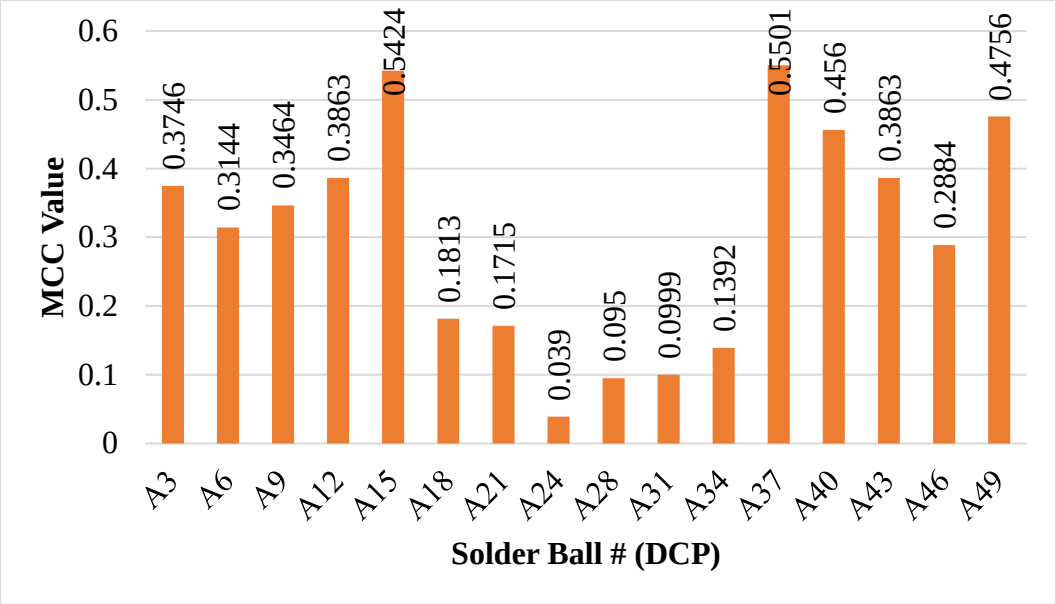


Figure 77 – 2D histogram of MCC values along the cross-section AA for board #2

The SEM images of selected solder balls along the cross-section AA for board #2 is shown in Figure 78. Separation of solder ball from the laminate (pad cratering) was the common failure observed across all the solder balls in section AA. From the SEM images, complete pad cratering was observed on solder balls from A2 to A18 and A32 to A37. Partial separation of solder balls from the laminate was observed on solder balls from A19 to A21 and A30 to A31. The severe separation was observed on solder balls from A38 to A50. No major failures were observed on solder balls through A22 to A29. Complete pad cratering on solder balls A2 and A3, partial pad cratering on solder balls A20 and A21, no failures on solder balls A24 and A25, and severe pad cratering on solder balls A49 and A50 are shown in Figure 78.

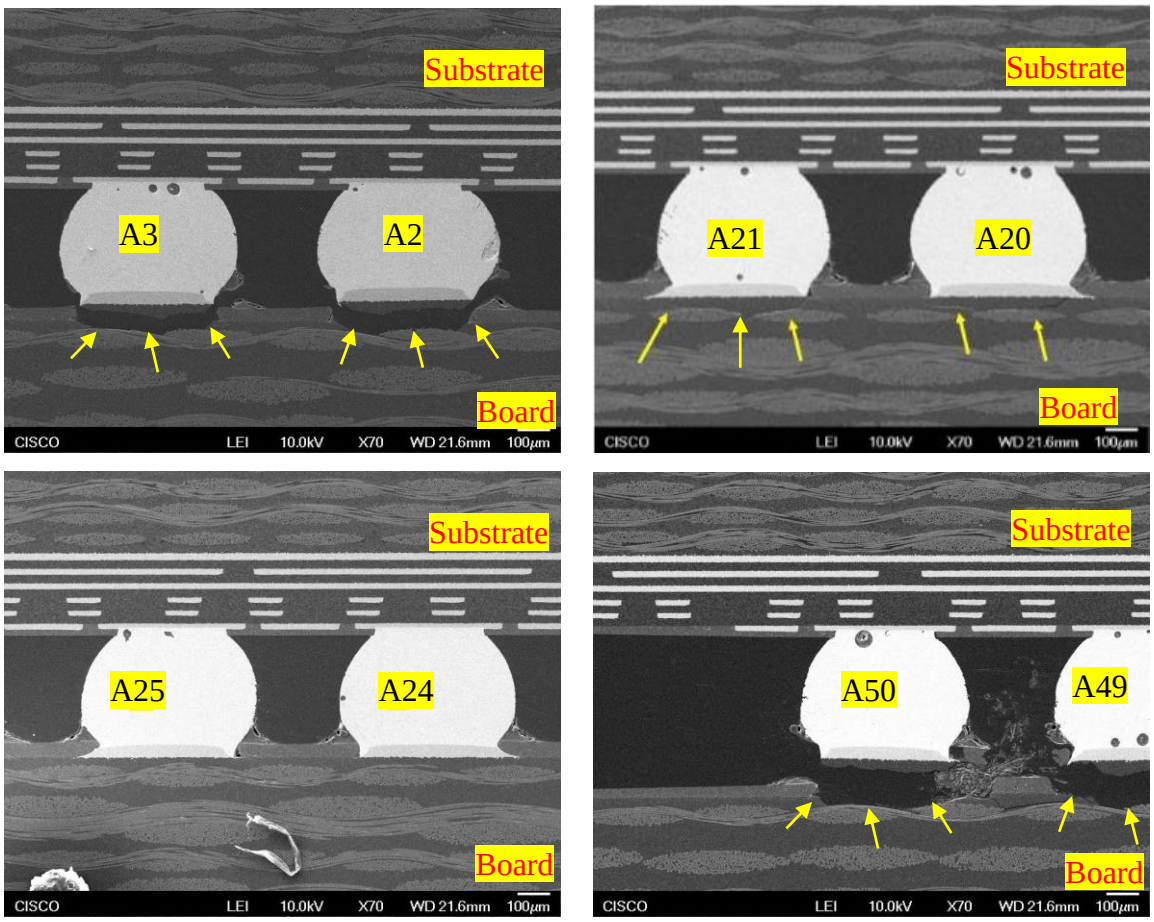


Figure 78 – SEM images of selected solder balls along the cross-section AA for board #2

The SEM results support the finite-element results shown in Figure 72 that the severity of pad cratering is highest at the edges and decreases towards the neutral plane. Also, the severity of pad cratering is approximately proportional to the MCC value. Complete pad cratering was observed at DCPs with MCC values more than 0.2, partial pad cratering was observed at DCPs with MCC values between 0.1 to 0.2, and no pad cratering was observed at detection points with MCC values below 0.1. A comparison of results from FE, LUI, and SEM, in terms of the severity of failures at section AA, is given in Table 6. It shows that there is a very good correlation between the results of the three different

methods. Solder balls with failures can be determined more precisely by increasing the number of detection points (i.e. increasing the resolution of inspection pattern), preferably a DCP over each solder ball. However, this will result in increased inspection time and energy consumption.

Table 6 – Comparison of severity of the failures from FE, LUI and SEM at section AA for board #2

	FE	LUI	SEM
Complete pad cratering	A2 to A15 & A36 to A50	A2 to A16 & A36 to A50	A2 to A18 & A32 to A50
Partial pad cratering	A16 to A18 & A34 to A36	A17 to A21 & A30 to A35	A19 to A21 & A30, A31
No pad cratering	A19 to A33	A22 to A29	A22 to A29

The MCC values are approximately symmetrical about the neutral plane. At the ends (detection points A3 & A49), MCC values were observed to be high; then they decreased initially in the inner rows (in detection points A6 & A46), and again increased to the highest values at the flip-chip edge (A15 & A37). Low MCC values were registered in the middle, with the lowest recorded at the neutral plane (A24). This trend didn't quite follow the finite-element and SEM results.

Upon further investigation, the finite-element analysis showed that there is a stress concentration zone in the substrate near the die boundary as shown in Figure 79. Four-point bend testing might have created discontinuities within the substrate layers near the die boundary of these high-stress zones. In LUI, out-of-plane displacements were measured from the top surface of the substrate. Any discontinuities within the substrate layer would increase the amplitude of the signals measured by the interferometer and would result in

high MCC values. Therefore, the high MCC values near the die boundary (at A15 & A37 in Figure 77) are attributed to the discontinuities in the substrate layers.

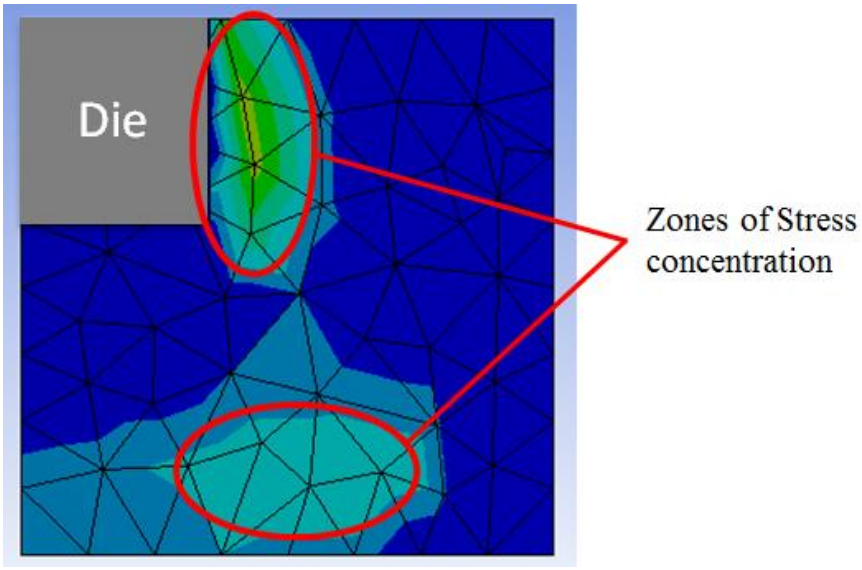


Figure 79 – Stress distribution in the substrate showing zones of stress concentration

For board #66, the pre-conditions and the loading conditions were different from those of board #2 as given in Table 2. Corner solder pads in board #66 were solder mask defined, and this board was also subjected to thermal aging at 100 °C for 500 hrs. The maximum displacement applied during the four-point bend testing was 5 mm. These conditions might have induced lower stresses and perhaps micro-cracks in the solder joints. A 2D histogram of MCC values along the cross-section AA for board #66 is shown in Figure 80. All MCC values were well below 0.05. It is expected that no failures would be found for these low MCC values. However, the SEM result showed that there was a very minor pad cratering at solder ball A2 as shown in Figure 81. DALUS with the current settings may not be sensitive to detect sub-micron failures. Further research shall be conducted with a high spatial resolution (placing DCP on a smaller cluster of solder balls)

and increasing the laser power. This is expected to increase the sensitivity of the system and make it possible to use it to detect such sub-micron failures.

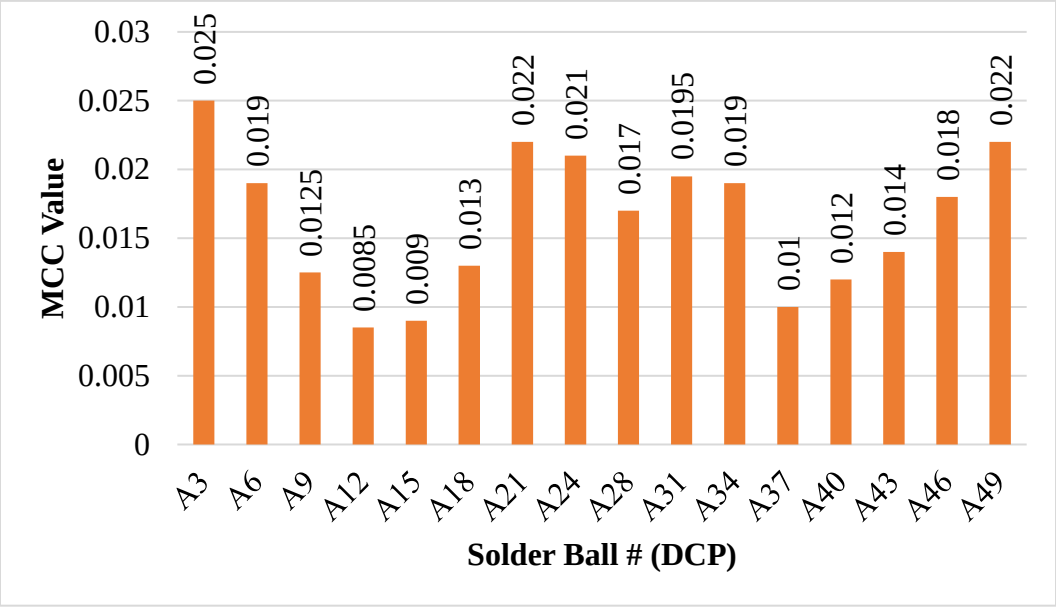


Figure 80 – 2D histogram of MCC values along the cross-section AA for board #66

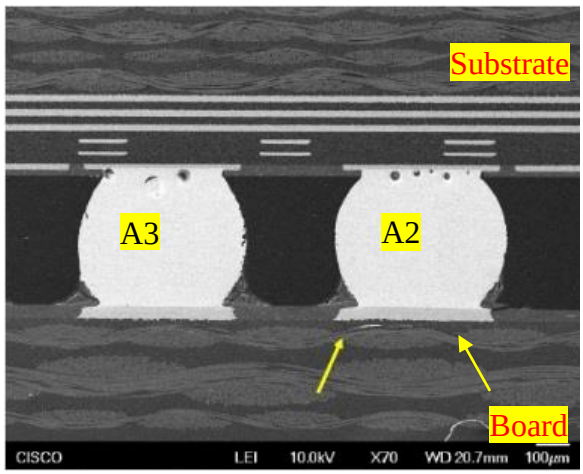


Figure 81 – SEM images of solder balls A2 and A3 for board #66

Apart from the cross-section AA on board #66, another cross-section, VV (which passes through the die) as shown in Figure 76 was evaluated to confirm the correlation

between MCC values and SEM results. The MCC values on top of the substrate (surface #1) at section VV are shown in Figure 82. MCC values from the top of the die (surface #2, which starts from solder ball V18 to V34) were not shown because the MCC values from the two different surfaces or geometries cannot be compared. The threshold values of MCC used to determine the presence of failures will vary depending on the geometry and the surface from which the interferometer probe is extracting the out-of-plane displacement data.

Along the cross-section VV, the MCC value recorded at detection point V1 was around 0.2 and the values recorded at the detection points V3 and V49 were around 0.1, as shown in Figure 82. From the SEM image results, as shown in Figure 83, pad cratering was observed at solder ball V1, and partial pad cratering was observed at solder balls V2, V4, V49, and V51. Again, the severity of pad cratering is proportional to the MCC value, confirming a strong correlation between MCC values and SEM results.

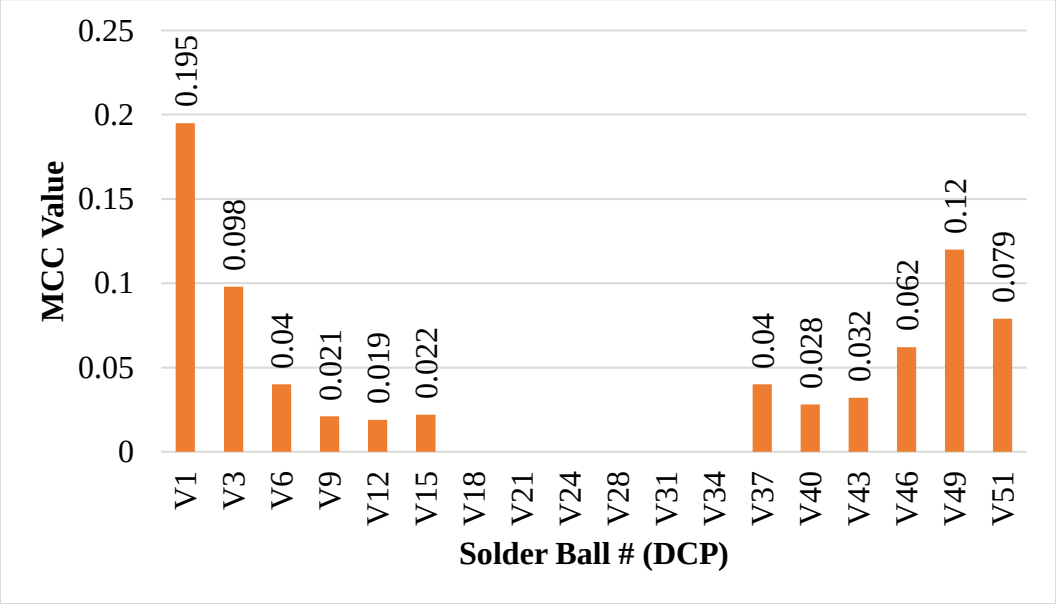


Figure 82 – 2D histogram of MCC values along cross-section VV for board #66

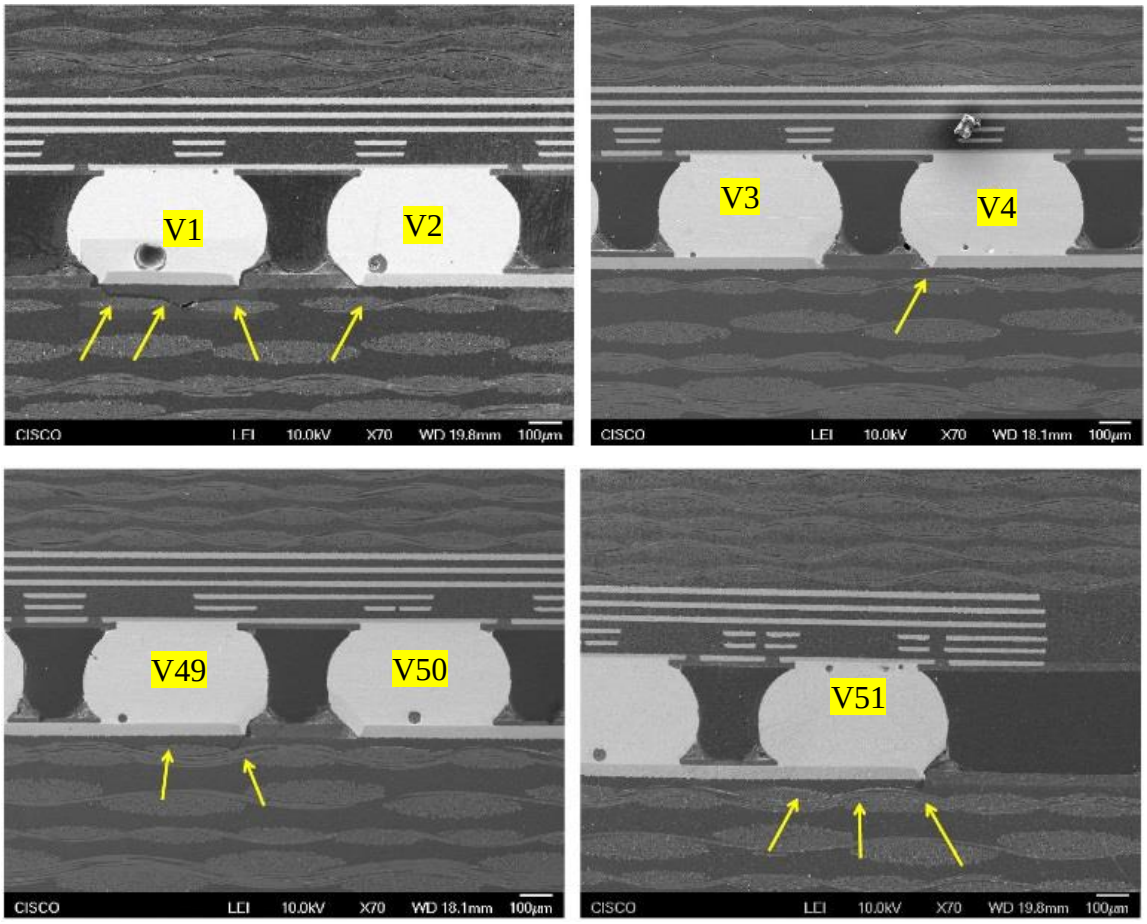


Figure 83 – SEM images of selected solder balls along the cross-section VV for board #66

For board #113, as discussed earlier, MCC values are not symmetric about the neutral axis. Not much information is available about these test samples. It is assumed that the asymmetry in the results could be due to the misalignment of the board during four-point bend testing. However, SEM was carried out along section AA on board #113 to validate the LUI results. 2D histogram of MCC values along the cross-section AA for board #113 is shown in Figure 84. High MCC values are recorded at the DCPs representing solder balls A2 to A36, and very low MCC values are recorded at the DCPs representing solder balls A37 to A50. From the SEM results, severe pad cratering failures were observed on

solder balls on A2 to A5, and A9 to A36. Solder interfacial fractures at the solder joint and the pads on the PCB were observed at solder balls at A6 to A8. Partial pad cratering was observed on solder balls A37 and A38. No major failure observed on solder balls A39 to A50.

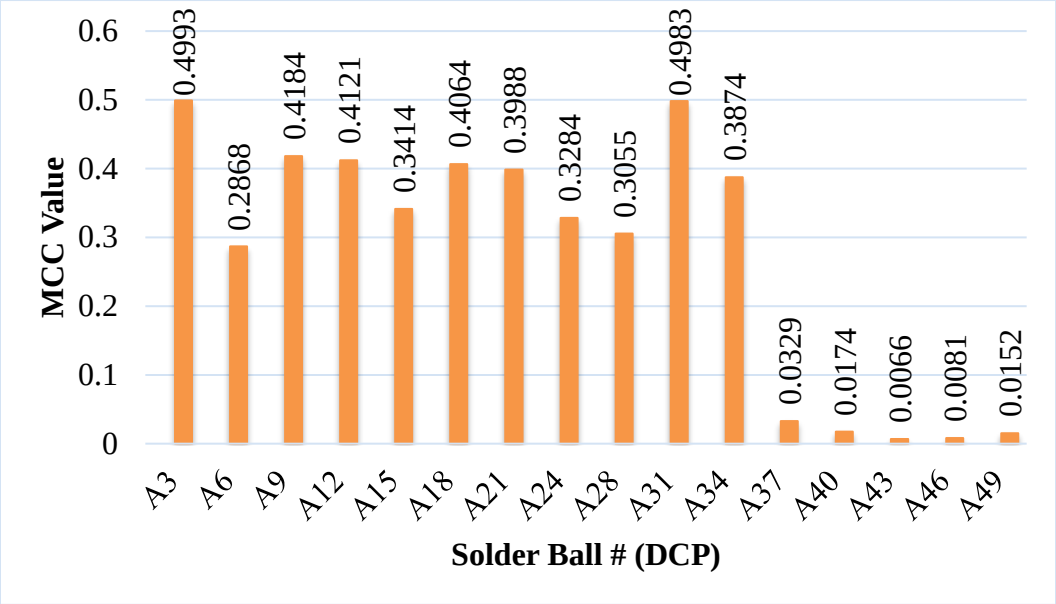


Figure 84 – 2D histogram of MCC values along the cross-section AA for board #113

Figure 85 shows the SEM images of solder balls A2 to A5 and A9 with very severe pad cratering, solder balls A6 to A8 with solder interfacial fracture, A37, and A38 with partial pad cratering, and A39, A40, and A47 to A50 with no major failures. MCC values of more than 0.2 matched well either with severe pad cratering failures or severe interfacial fractures. Again, DALUS with the current settings may not be sensitive to detect sub-micron failures on solder balls A37 and A38. It is also a possibility that minor failures below micron might have formed after DALUS experiments and during the cross-sectioning process. Overall, DALUS could successfully identify the failure locations and their severity accurately.

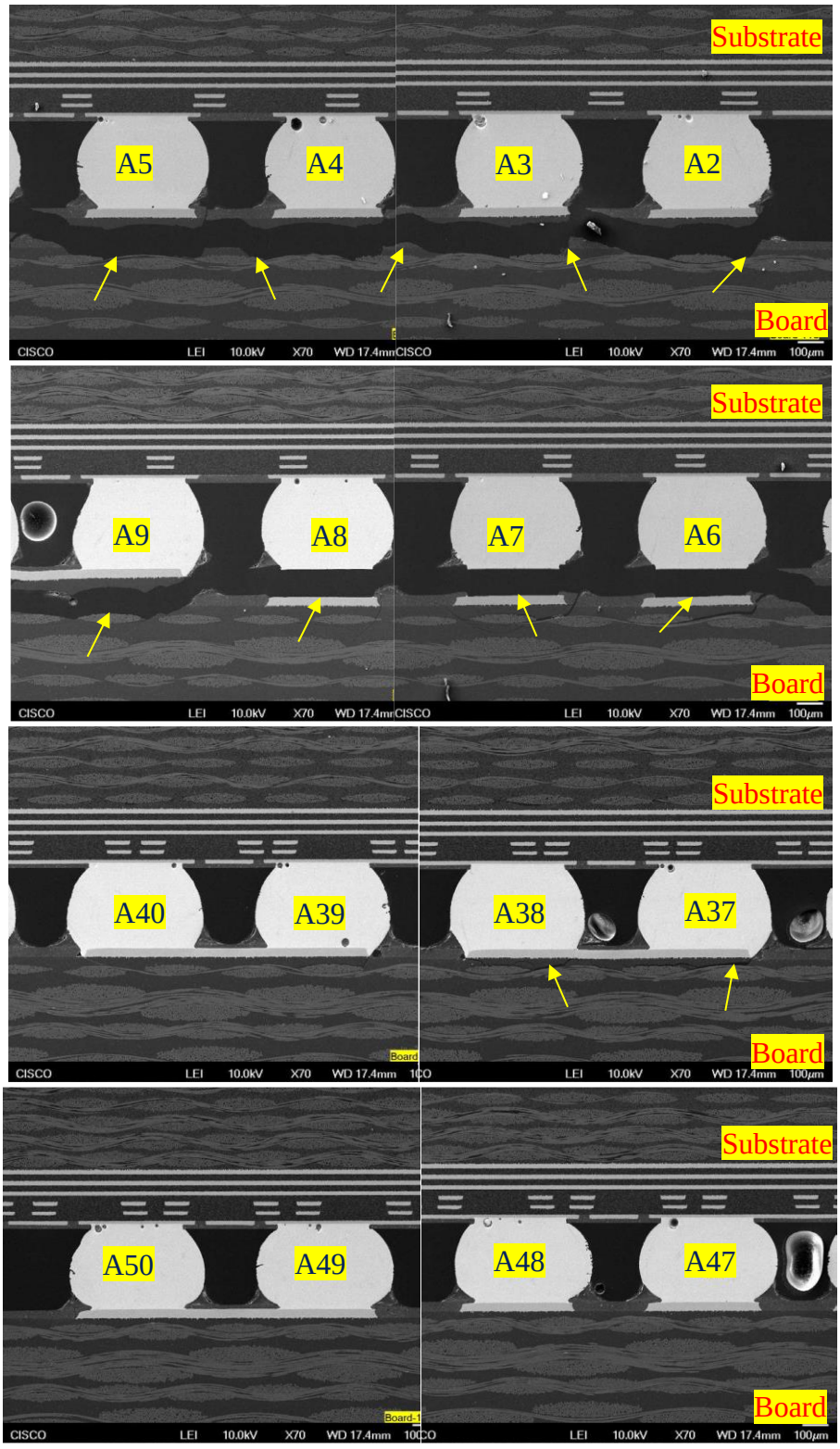


Figure 85 – SEM images of selected solder balls along the cross-section AA for board #113

6.4 Evaluation of FCBGA samples subjected to Drop Test

6.4.1 Drop Test Setup

The drop testing is another popular ALT for the design of impact-tolerant microelectronic packages. The world is entering a mobile era with all portable electronics, hence, drop testing plays an important role in product characterization. The test vehicles, board #9, #41, #83, #86, #107, #117 listed in Table 4 are subjected to a Board Level Reliability (BLR) drop test, which is a mechanical shock stressing of a package assembled onto the PCB. The JEDEC standard, JESD22-B111 methodology, with service condition D was adopted in performing the BLR drop test [65]. A schematic illustration of the drop test set-up is shown in Figure 86. Drop tests were conducted using a Lansmont M23 TTSII shock test system. The drop table is lifted and released from a certain height. When the drop table is released, it travels down on guide rods and strikes the striking surface, which is mounted over the rigid base. A base plate with standoffs is rigidly mounted on the drop table. The test vehicle assembly is mounted to the base plate standoffs using 4 shoulder screws at four corners. A stand-off distance of 10 mm is maintained between the PCB and the drop table in drop test experiments. The test vehicle is mounted on the base plate in two orientations as shown in Figure 86, +Z orientation is when the FCBGA package is facing upwards, and –Z orientation is when the FCBGA package is facing downwards. An accelerometer is mounted on the PCB to measure the acceleration when the drop table strikes the striking surface. A typical impact pulse of the drop test resembles a half-sine wave as shown in Figure 87. The impact pulse generated in the test board during the drop measured at the center of the PCB is also shown in Figure 87. Drop tests were repeated with +Z and –Z orientations as given in Table 4, until the failure of package occurred.

Failure is detected by monitoring electrical continuity in the daisy chain. A 20% increase in resistance value in the daisy chain is considered as a failure.

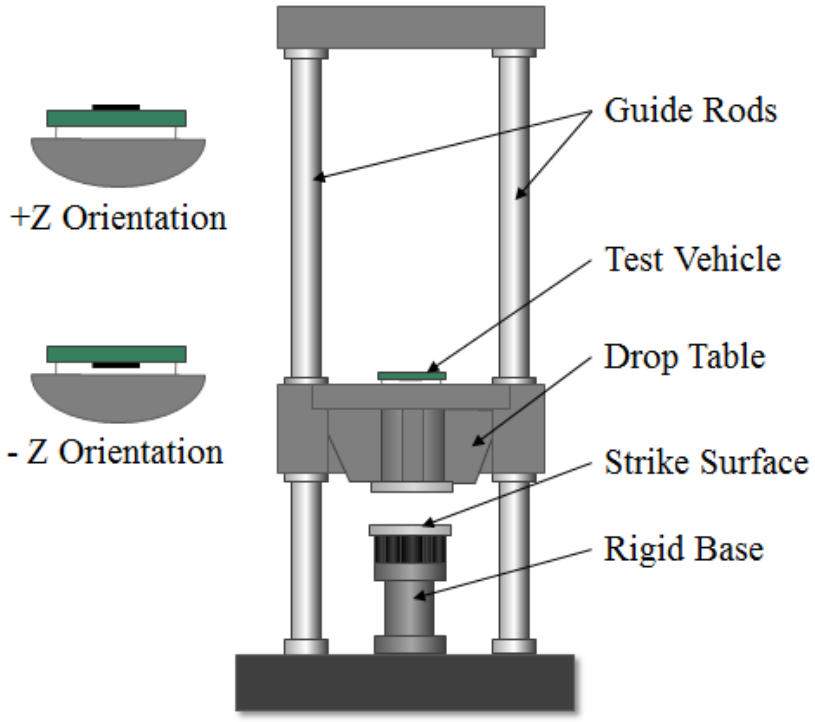


Figure 86 – Drop testing setup

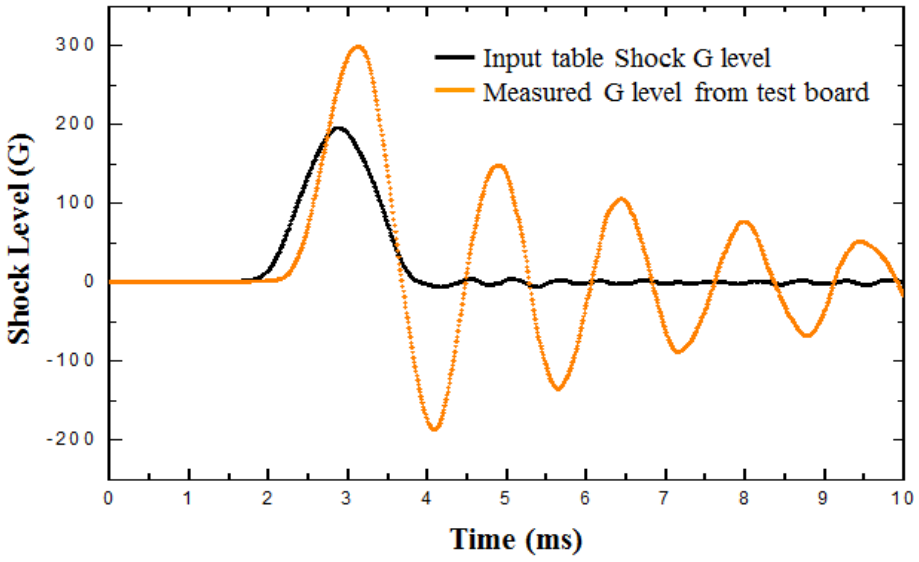


Figure 87 – Input and measured shock G level

6.4.2 Drop Testing Finite-Element Simulations

Similar to four-point bend testing finite-element simulations, a 3D quarter model FCBGA package, as shown in Figure 88, was created for drop testing simulations. Drop testing simulations helps in understanding the failure trends in BGA solder balls for drop scenario and to validate the LUI results. Like the four-point bend testing, the finite-element simulation model for drop testing consists of five components: silicon die, underfill, substrate, BGA solder balls, and PCB, as shown in Figure 89.

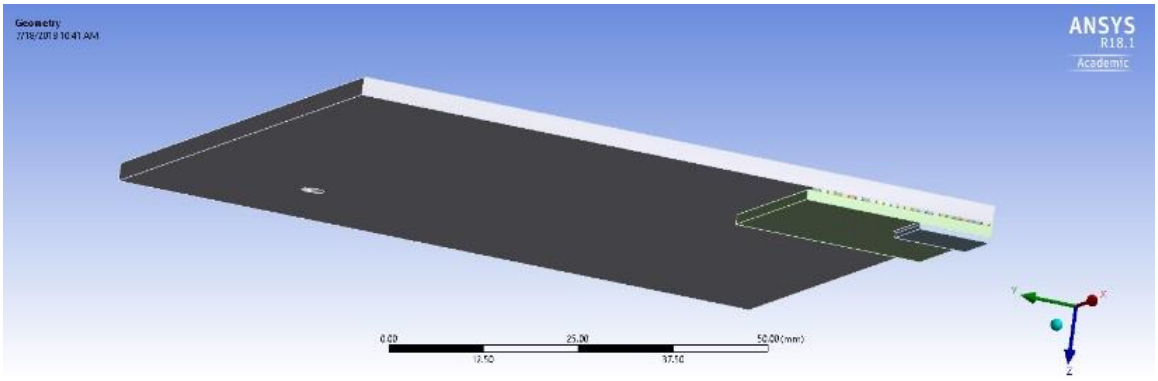


Figure 88 – A quarter model of FCBGA assembly for drop testing simulations

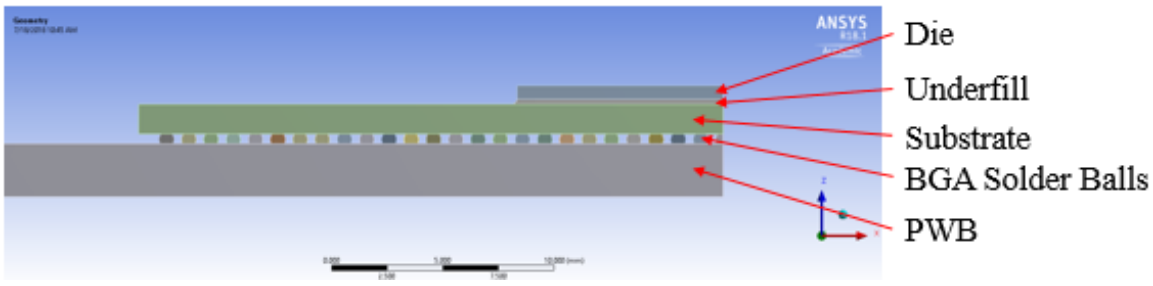


Figure 89 – Finite-element model of the FCBGA package showing different components

During the drop testing, the pulse generated on the drop table is transferred to the PCB through the four corner screws. So, the impact pulse measured in the experiment can be given as input directly to the finite-element model shown in Figure 88. In this way, all other drop test apparatus can be eliminated from the finite-element model. The input table shock G level and measured G level at the center of the test board are shown in Figure 87. From the experiments, and strain measurement, it is clear that the PCB has maximum deflection and maximum strain at the center for the given shock pulse. Hence, the measured G level has to be applied at the center of the board (on the opposite side of the package). However, ANSYS workbench does not support applying acceleration at a point in transient structural analysis. Therefore, harmonic acceleration is converted to displacement amplitude using Equation (3), and the displacement is applied at the center of the board while the board was fixed at the corner hole (representing that the board is screwed to the drop table), and symmetric boundary conditions were applied on symmetric sections.

$$d = -\frac{a}{\omega^2} = -\frac{a}{(2\pi f)^2} \tag{3}$$

Where d: displacement; a: acceleration; ω: angular frequency; f: frequency.

The equivalent stress distribution results obtained from the finite-element simulations are shown in Figure 90. It is observed that corner solder balls experience high stress. These corner solder balls are prone to failure on multiple drops or impact cycles. It may be noted that the LUI results also show high MCC values at the corner solder balls as shown in Figure 91 and Figure 92. Hence, FEM results helped in confirming high MCC values at the corner DCPs on the package, aligning with LUI results.

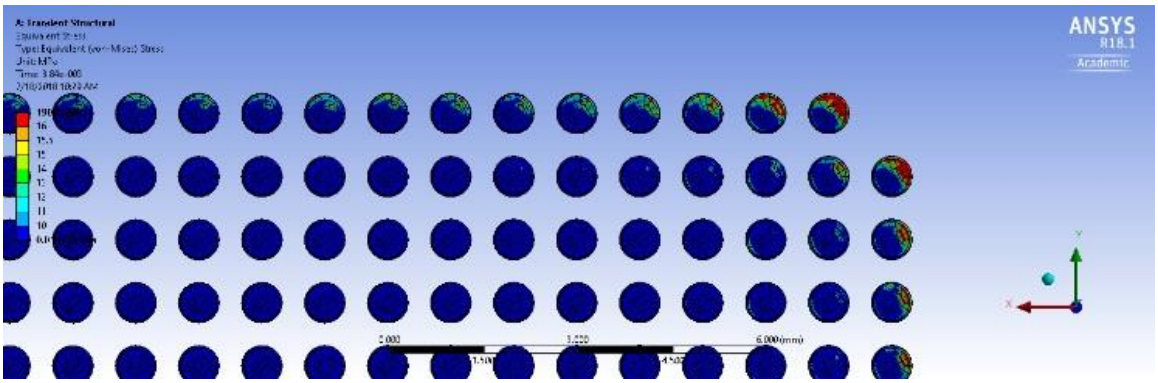


Figure 90 – Equivalent stress distribution in the solder balls at the interface between solder balls and PCB

6.4.3 LUI Results

Similar to the samples subjected to the four-point bend testing, all the test vehicles subjected to drop testing listed in Table 4 were inspected using DALUS. The LUI results on all boards subjected to drop testing are similar and results on board #83 and board #41 are presented here for discussion. Initially, interferometer transient out-of-plane displacement signals were collected on the reference board #123, and then on the test vehicles based on the inspection pattern described in the previous section 6.2. MCC values are calculated using Equation (1) at each DCP and plotted in the form of a 3D histogram as shown in Figure 91 for board #83, and Figure 92 for board #41.

The general observation is that MCC values are low at most of the DCPs. This indicates minor or no failures in the test packages. In both test packages, the corner MCC values are high, indicating failures at the corners. Even, from the finite-element simulations, corner solder balls are expected to fail in the drop test. Hence, it is predicted that the corner solder balls will have failures. Apart from the corners, there were observed

to be high MCC values in section 2 and section 6 for board #41. These high MCC values are attributed to noise in the interferometer signals because of the rough and uneven surface of the package in that specific area.

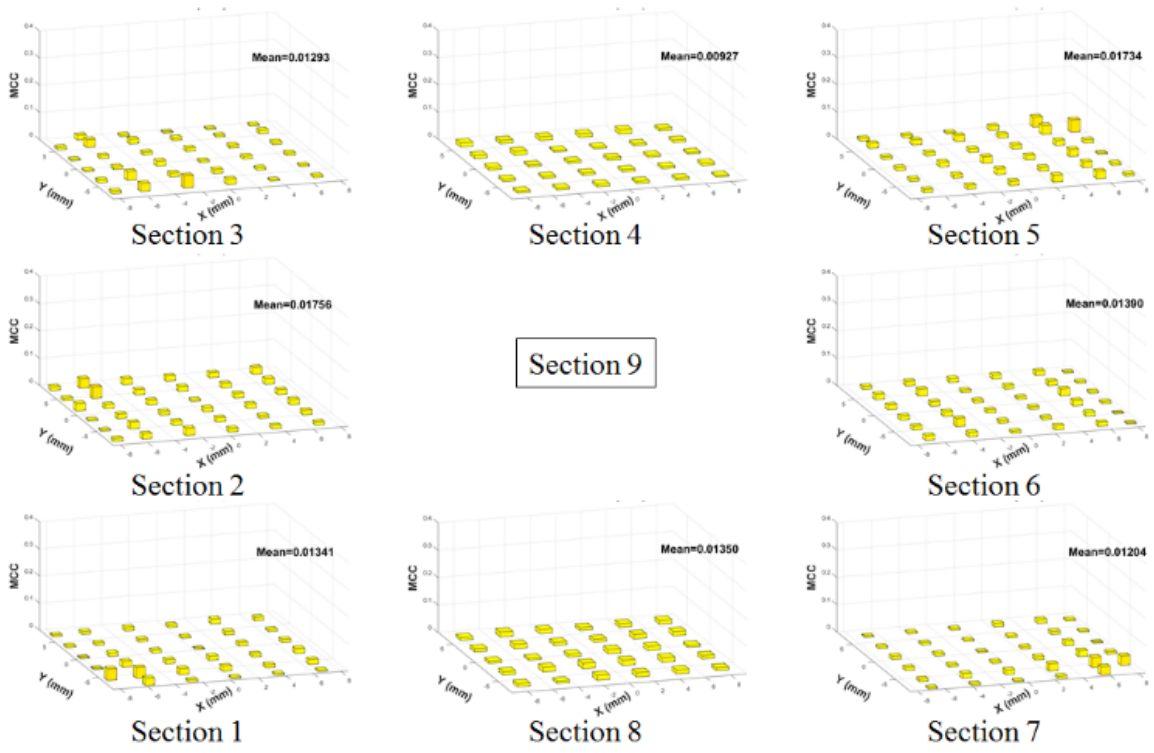


Figure 91 – LUI results (MCC values) at all DCPs for board #83 in 3D histogram format

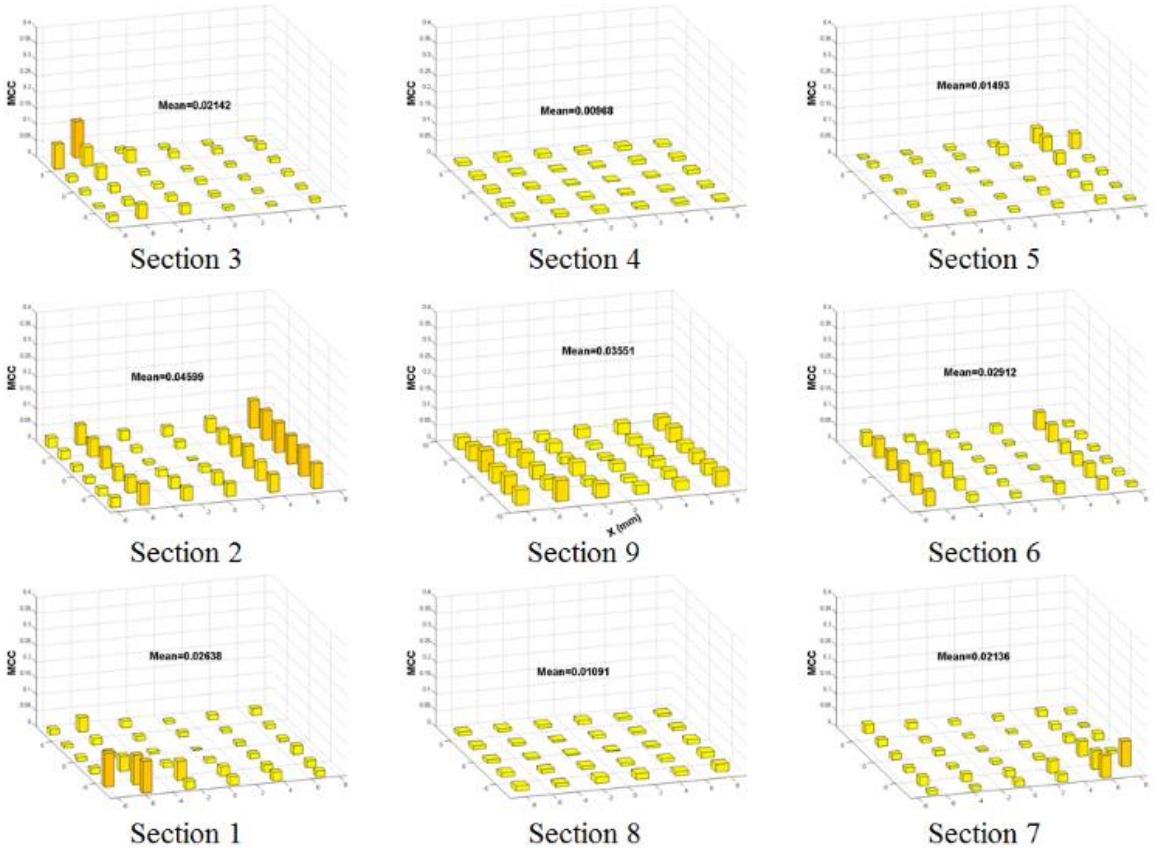


Figure 92 – LUI results (MCC values) at all DCPs for board #41 in 3D histogram format

6.4.4 Validation and Discussions

From the FEM results and LUI results, it is predicted that corner solder balls are failed. To validate the presence of failures, the test samples were cross-sectioned, polished, and observed via digital microscopy and SEM. Board #83 was cross-sectioned along column 51 of solder balls, and board #41 was cross-sectioned along column 1 of solder balls. Column 1 and column 51 can be visualized in Figure 76. 2D histogram of MCC values along column 51 of solder balls for board #83 is shown in Figure 93. 2D histogram of MCC values along column 1 of solder balls for board #41 is shown in Figure 94.

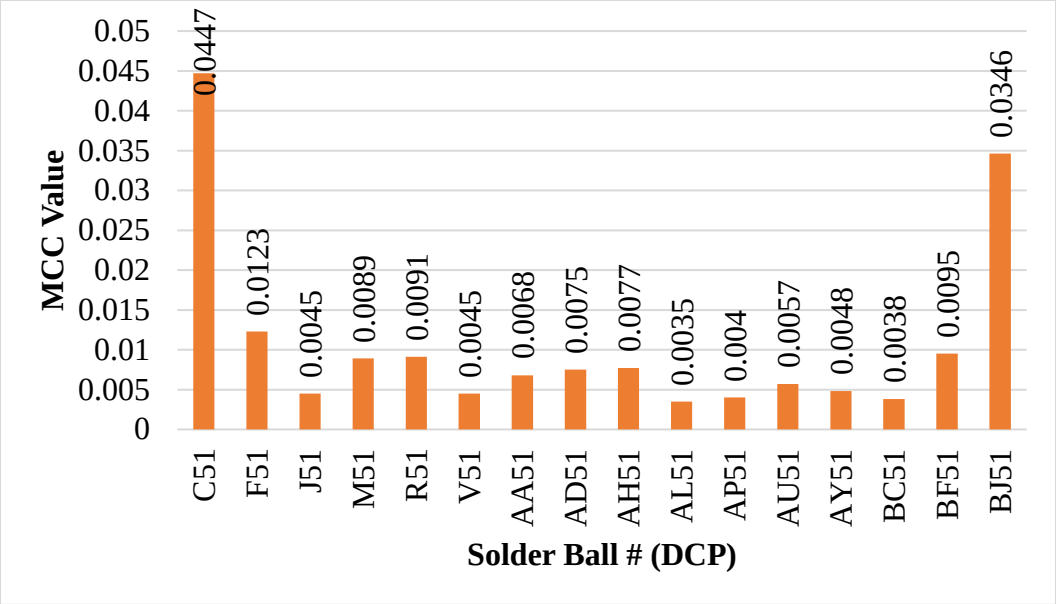


Figure 93 – 2D histogram of MCC values along the column 51 of solder balls for board #83

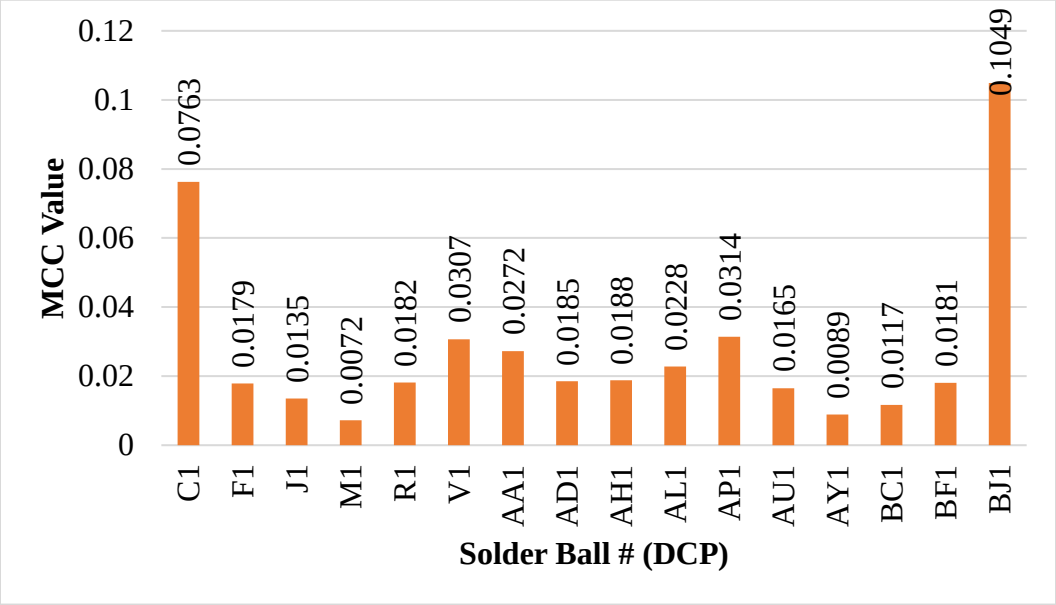


Figure 94 – 2D histogram of MCC values along column 1 of solder balls for board #41

The cross-sectional SEM images of corner solder balls on board #83 and board #41 are shown in Figure 95 and Figure 96 respectively. From the SEM results, corner solder balls in board #83 were observed to have IMC failures on the PCB side. The IMC failures in solder balls B51, C51, and BK51 in board #83 are shown in Figure 95. There were no noticeable failures in all remaining solder balls in column 51 of board #83. The MCC value at DCP on C51 corresponding to solder balls B51 and C51 is 0.0447, and the MCC value at DCP BJ51 corresponding to solder ball BK51 is 0.0346. These MCC values are clearly higher than the MCC values at other DCPs in the same column. Empirical data suggest that MCC values above 0.034 imply to failures in the field of view corresponding to that DCP for test vehicles subjected to drop testing. This confirms that high MCC values above 0.034 at the corners of the package for board #83 correspond to IMC cracks in the solder balls. Also, the IMC cracks in two solder balls B51 and C51 at one corner produced high MCC values when compared to the IMC crack on only solder ball BK51 at the other corner. Thus, the cumulative severity of the failures is correlated with the level of MCC value.

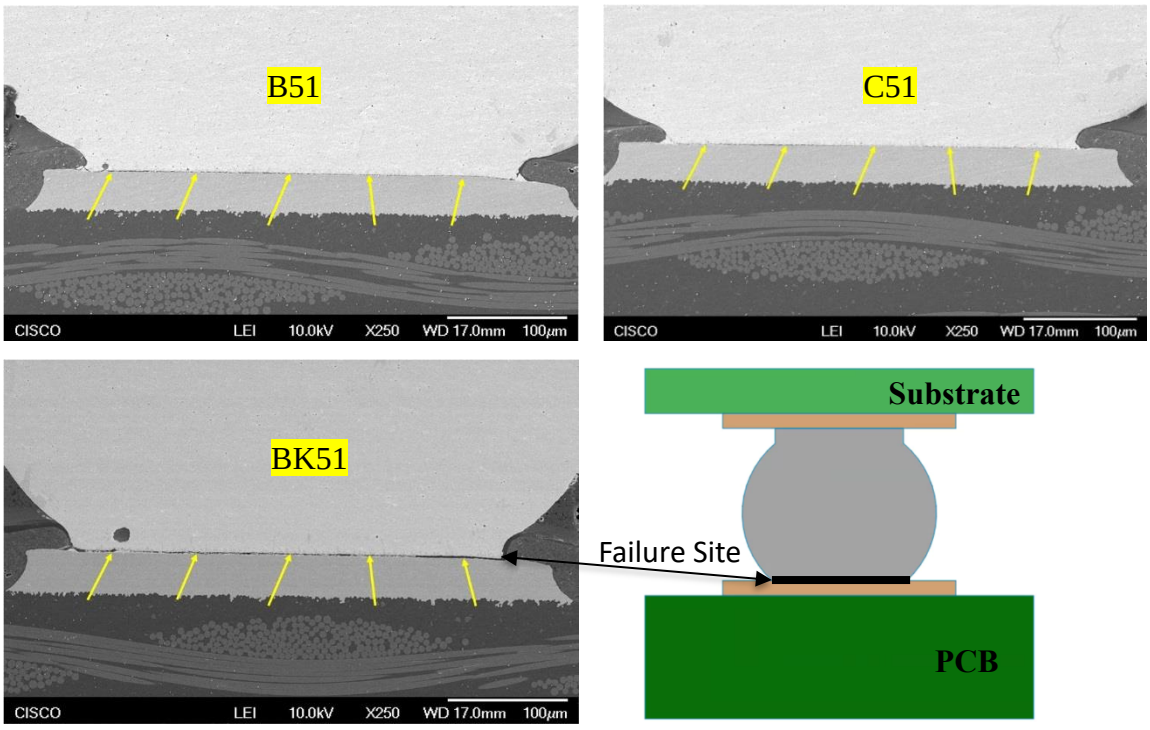


Figure 95 – SEM images of selected solder balls along the Column 51 for board #83

From the SEM images, board #41 was observed to have pad cratering failures in the PCB in corner solder balls. Partial pad cratering in solder balls B1, BH1, BJ1, and BK1 are shown in Figure 96. There were no noticeable failures in remaining solder balls in column 1 of board #41. The MCC value at DCP on C1 corresponding to solder ball B1 is 0.0763, and the MCC value at DCP on BJ1 corresponding to solder balls BH1, BJ1, and BK1 is 0.1049. Again, MCC value more than 0.034 related to failures in the solder balls in that corresponding field of view of the DCP. Cumulative failures in three solder balls (BH1, BJ1, and BK1) resulted in the highest MCC value, which confirms the proportionality relationship of the cumulative severity of the failures with the level of MCC value. High MCC values in board #41 correspond to a pad cratering failure unlike the IMC failures in board #83. The failure modes of the two packages are different because the corner solder

ball pads of board #83 are solder mask defined, whereas all pads on board #41 are non-solder mask defined.

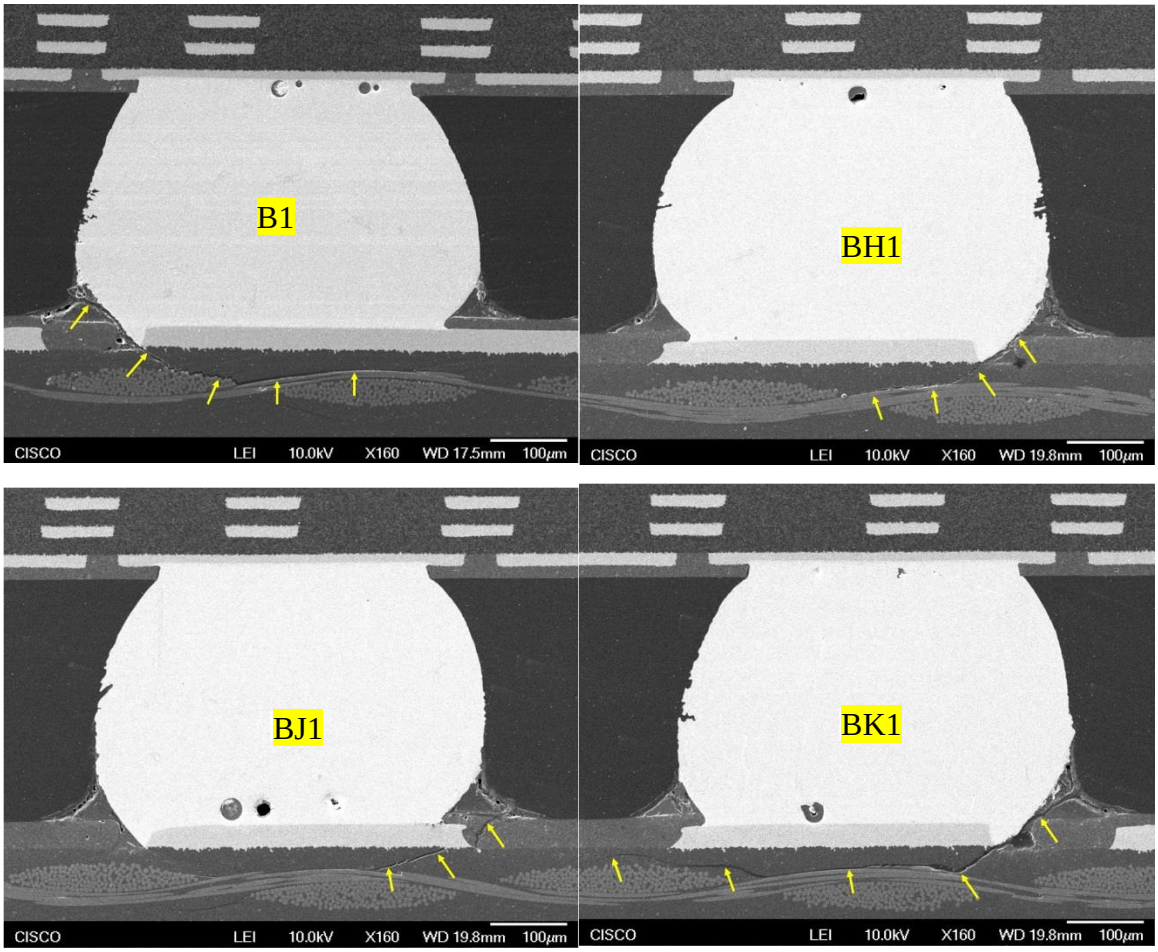


Figure 96 – SEM images of selected solder balls along Column 1 for board #41

In summary, LUI results show that the corner solder balls of the packages that were subjected to drop testing have high MCC values. SEM images revealed that the corner solder balls have failures, either IMC cracks and pad cratering. Hence, LUI results are validated. Though a high MCC value corresponds to some defect or failure, it is difficult to predict the kind of defect/failure with DALUS. A study of interferometer signals shall be carried out to develop a method to differentiate various mechanisms of defects/failures.

6.5 Evaluation of FCBGA samples by SAM and X-ray

The 52.5 x 52.5 FCBGA samples were also inspected using SAM and 2D X-ray. Sonoscan D9000 acoustical microscope was used for echo method SAM and the Nordson DAGE XD7600NT Diamond X-ray Inspection System was used for 2D X-ray. Both SAM and 2D X-ray could not detect the presence of failures in second-level interconnects. Sample results from an FCBGA package that was analyzed using Acoustic microscopy with 200MHz transducer are shown in Figure 97. Acoustic waves were able to penetrate up to only one layer of substrate out of 11 layers and only through holes between the top layer and the next layer have been identified as shown in Figure 97. Even with low-frequency ultrasound, it was highly difficult to detect failures like IMC cracks and pad cratering in solder balls.

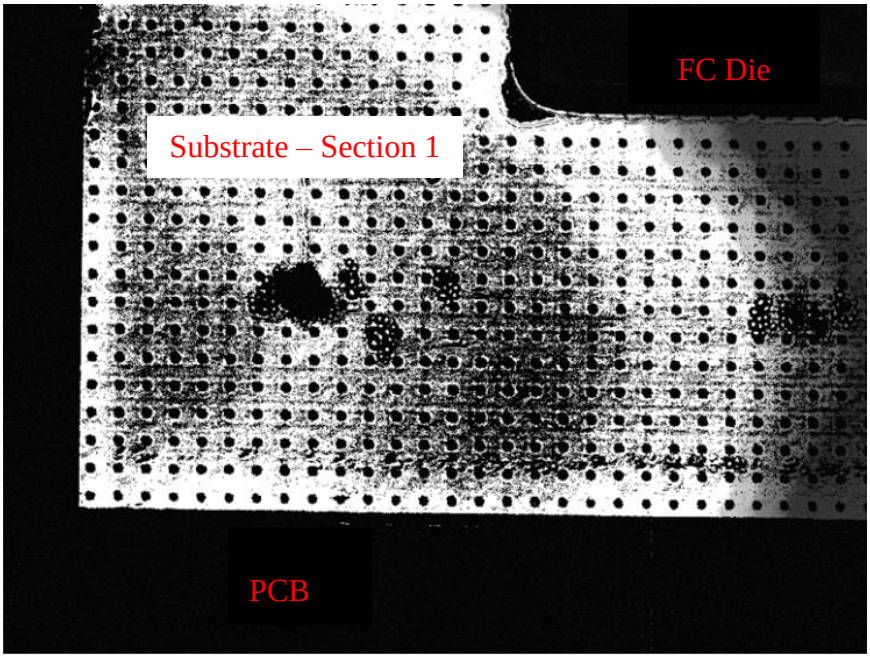


Figure 97 – Sample results from SAM with 200MHz transducer

Sample 2D X-ray result of an FCBGA package using a DAGE X-ray system is shown in Figure 98. This image is a 2D projection of the sample. The failures remain invisible to 2D X-ray because the amount of material that is absorbing the x-rays does not change. Sometimes, failures are hidden under voids and other structural constraints for X-rays in 2D projection. Hence, IMC and pad catering failures were not detected with the 2D X-ray technique. The 3D X-ray technique is gaining popularity in the modern era. However, high-resolution 2D images are required to produce high-quality 3D images and detect IMC and pad cratering failures with the 3D X-ray technique.

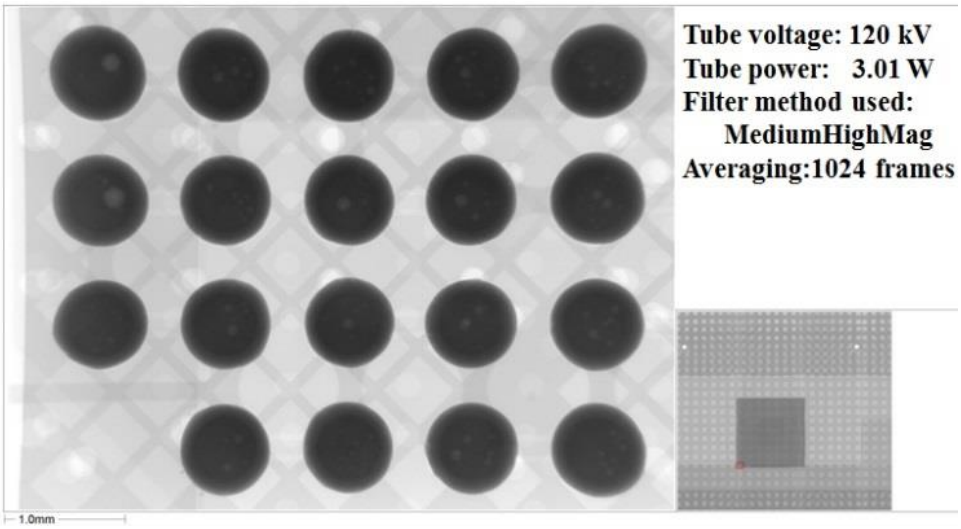


Figure 98 – Sample X-ray image of a corner of FCBGA package from DAGE X-ray inspection system

6.6 Summary

All the test vehicles listed in Table 4, have been inspected using DALUS. Board #123 has been used as a reference sample to calculate MCC on all the test vehicles based on the pre-programmed inspection pattern. Both the location and the severity of failures

are identified using DALUS. For validation and comparison of LUI results, finite-element simulations and SEM have been carried out. LUI results are aligned well with SEM results and FEM results. Also, MCC values are correlated with the cumulative severity of the failures.

Four-point bend testing resulted in mainly pad cratering, and complete solder interfacial fracture in the solder balls at the edge parallel to anvil axis. Drop testing resulted in IMC cracks and partial pad cratering at the corner solder balls. SAM with 200 MHz ultrasonic transducer and 2D X-ray could not detect these failures. Some of the test vehicles, which were assessed to be good in electrical tests, were actually found to have failures in both LUI and SEM results. This means electrical tests can give false-positive results (i.e., the test result indicates a good joint when the sample does have significant failures). Also, it is not possible to know the severity and exact location of a defect/failure by using electrical tests. DALUS has proven to be an accurate nondestructive technique for evaluating BGA solder balls in FCBGA packages. The sensitivity of DALUS and the accuracy of the results can further be improved by increasing the laser power and resolution of the inspection pattern.

CHAPTER 7. EVALUATION OF FCBGA SAMPLES SUBJECTED TO THERMAL CYCLING RELIABILITY TEST

In the previous chapter, evaluation of BAG solder balls in 52.5 x 52.5 FCBGA packages subjected to four-point bend testing and drop testing using DALUS is demonstrated. However, 52x52.5 FCBGA samples supplied by Cisco are still prototype test packages. The utility of DALUS in the industry can be better demonstrated if the practical advanced packages are evaluated using DALUS. This chapter is dedicated to the evaluation of such types of advanced FCBGA packages, which are being used in automobiles using DALUS. These samples experience temperature variations in their operation. Hence, they are subjected to thermal cycling accelerated life testing.

7.1 Test Vehicles

Two types of advanced industrial FCBGA packaging samples which are subjected to thermal cycling reliability testing were supplied by Texas Instruments to test DALUS capability to identify various chip to package interaction anomalies. Both types of samples are very similar except that the number of BGA solder balls and their footprint arrangement is different. The original image of the 17 x 17 FCBGA test vehicles is shown in Figure 99. The schematic of BGA solder ball locations (footprint) for Type-A test vehicle is shown in Figure 100. Type-B test vehicles have full area-array BGA solder balls. Type-A samples are used for evaluation of the quality of BGA solder balls using DALUS. Whereas Type-B samples are used for Gage Repeatability and Reproducibility (GRR) studies. In this chapter evaluation of Type-A samples is presented.

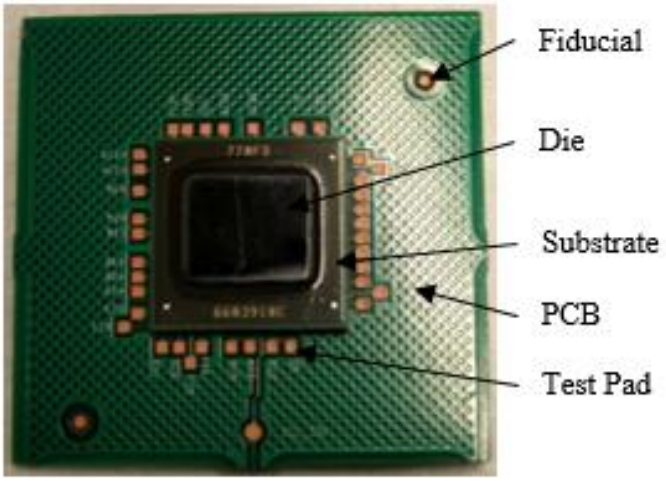


Figure 99 – Original image of TI 17 x 17 FCBGA test vehicle

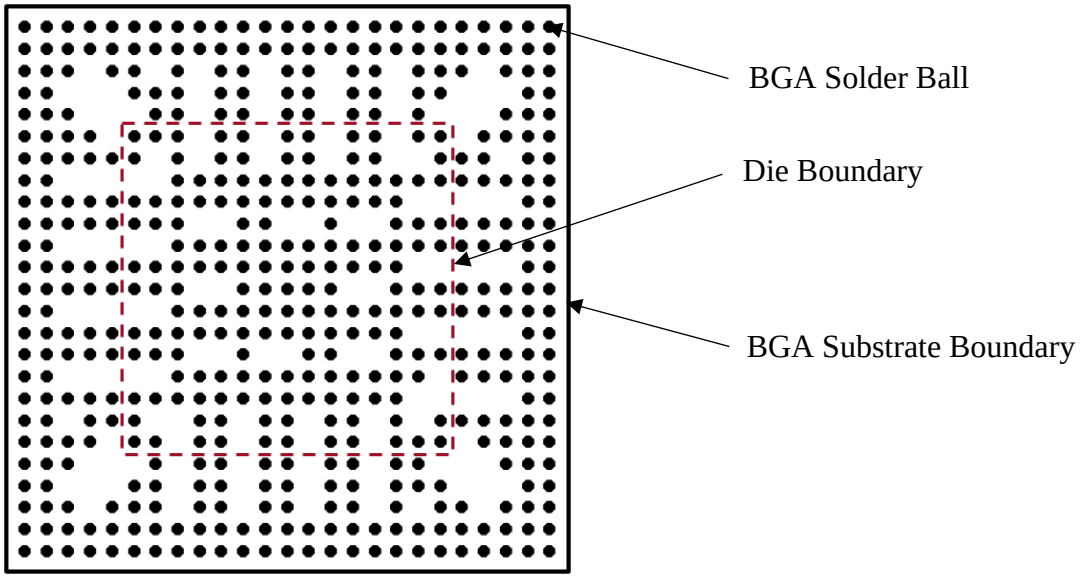


Figure 100 – BGA solder ball footprint of Type-A 17 x 17 FCBGA test vehicle

The Type-A test vehicle had a heat sink (metal plate) attached to the die using Thermal Interface Material (TIM) adhesive. The heat sink was removed for DALUS experiments because the adhesive between the heat sink and the die attenuates the ultrasound propagation into the package and makes it difficult to detect the

failures/anomalies. The packages have underfill between the die and the substrate, supporting first-level flip-chip solder bumps. Second-level BGA solder ball interconnections are not covered with any underfill. The FCBGA package has a footprint of size 17 x 17 mm (= BGA substrate size), the Silicon die of size 10.027 x 9.68 mm, and BGA solder balls of size 0.35 mm diameter with pitch 0.65 mm. BGA solder balls are made of Lead-free SAC 305 (96.5 Sn – 3% Ag – 0.5% Cu) material. As shown in Figure 100, the BGA solder ball layout is a 25 x 25 area-array but not a full area-array. 15 x 15 array of BGA solder balls at the center are under the die shadow, represented by a red dashed line in Figure 100.

In total eight Type – A test vehicles as listed in Table 7, were received from Texas Instruments. Four test vehicles, labeled as 9U1, 9U2, 9U3, and 9U4, are time-zero samples which were not subjected to the thermal cycling reliability test. According to the manufacturing standards and test procedures at Texas instruments, these time-zero samples are assumed to have no failures. The other four test vehicles, labeled as 5U1, 5U3, 6U1, and 6U2 are subjected to thermal cycling reliability test as per the Design of Experiments (DOEs) given in Table 7.

Table 7 – Details of Type – A 17 x 17 FCBGA test vehicles

Sample Description	Labeled as	Failed at (Cycles)	Pulled at (Cycles)	Failure sites
2535-9 U1	9U1	Time 0 Samples		No Failures
2535-9 U2	9U2			
2535-9 U3	9U3			
2535-9 U4	9U4			
2535-5 U1	5U1	2011	2036	M11 – Y7
2535-5 U3	5U3	2201	2929	Y20 – F20
2535-6 U1	6U1	2285	2929	A13 – K6; M11 – Y7; Y20 – F20
2535-6 U2	6U2	2291	2929	M11 – Y7; Y20 – F20

7.2 Thermal Cycling Reliability Test

As per industry standard specifications, IPC 9701 test condition TC3 with a temperature cycle range -40°C ↔ 125°C was adopted by Texas Instruments for thermal cycling reliability test to ensure reliable package performance under extreme operating temperature conditions [12]. ATC test condition TC3 involves the temperature range of -40 °C ↔ +125 °C with 15 minutes dwell at both high temperature and low temperature and 11 °C/minute ramp rate. Test vehicles 5U1, 5U3, 6U1, and 6U2 were highly stressed after end-of-life conditions and qualification release point per IPC 9701. The end of life was monitored by electrical testing. After every ~150 thermal cycles, the samples were pulled out of the thermal cycling test chamber and electrical resistance was measured on appropriate test pads for a net. The occurrence of the first event (first interruption for a period of at least 200 ns and an increase in resistance to at least 1,000 ohms) followed by nine additional events within 10% of the thermal cycles to the first event recorded is defined as a failed sample. Any abrupt increase in resistance between test pads based on

the aforementioned criteria indicates the failure in the net connecting two test pads. However, it is not possible to know the exact failure location or type in the failing net from the electrical test.

The details of test vehicles, corresponding number of thermal cycles where the test vehicle failed, thermal cycles after when they pulled out of the thermal chamber, and electrical failure sites (at failed cycles) are listed in Table 7. The electrical network connectivity diagram showing failed nets is given in Figure 101. Test vehicle 5U1 is failed at 2011 thermal cycles, and the failed net was in between M11 – Y7; 5U3 is failed at 2,201 thermal cycles, and failed net was in between Y20 – F20; 6U1 is failed at 2,285 thermal cycles, and failed nets were in between A13 – K6, M11 – Y7, and Y20 – F20; 6U2 is failed at 2291 cycles, and failed nets were in between M11 – Y7, and Y20 – F20. All the failed nets were at the edge under the die shadow. Corner solder balls under the die shadow might have failed. It may be noted that these failed nets are shown at thermal cycles listed as failed (cycles) in Table 7. However, test vehicles were placed again in the thermal chamber for further thermal cycles, and 5U1 was pulled out at 2036 thermal cycles, and the other three test vehicles (5U3, 6U1, and 6U2) were pulled out at 2929 thermal cycles. LUI experiments were conducted after the test vehicles are pulled out, which means the LUI results are expected to show more severe failures than predicted by electrical tests. Especially, failure samples 5U3, 6U2, and 6U3 were failed around 2,200 – 2,300 thermal cycles in the electrical test, whereas these samples were pulled out at 2,929 thermal cycles. Hence, electrical tests cannot be used for comparison with LUI results. Cross-sectioning along with SEM, and dye-and-pry destructive testing were carried out to verify the LUI results on failure samples.

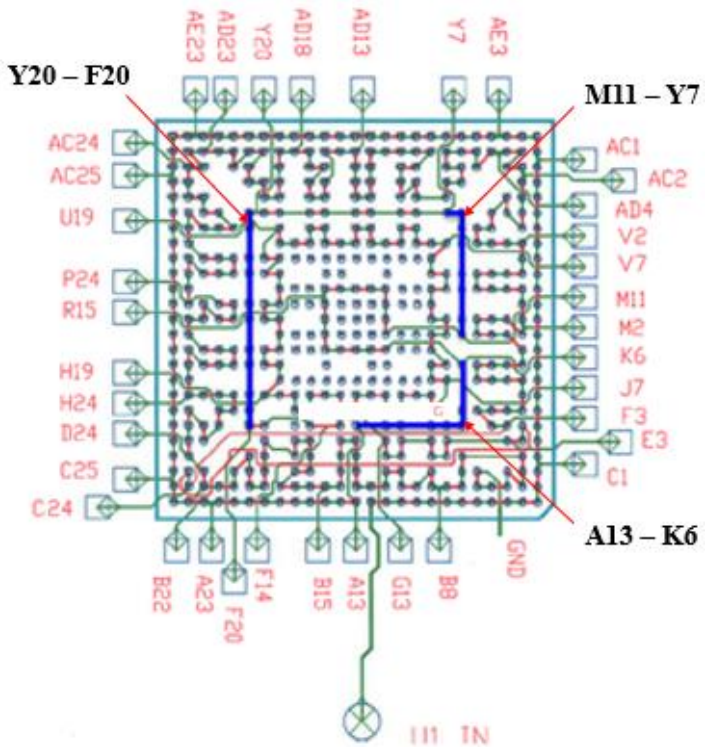


Figure 101 – Network connectivity diagram showing failed nets (blue lines) for the test vehicles 5U1, 5U3, 6U1, and 6U3

7.3 Inspection Procedure

The inspection pattern used for Type-A test vehicles along with the sequence number of DCPs was shown in Figure 102. MATLAB's view of the same inspection pattern is shown in Figure 103. As discussed earlier in section 6.2, it is preferred to collect interferometer displacement data at every BGA solder ball location for signal analysis and predicting the defects/failures at corresponding BGA solder ball. However, the total inspection time depends on the number of DCPs. To make the inspection simple and increase the throughput, DCPs are chosen at every alternative BGA solder ball location as shown in Figure 102. A small area around the die shadow boundary (red line in Figure 102) was not considered for inspection because of the underfill spread which is uneven/rough

surface. Rough surfaces make interferometer laser to scatter and produce high noise in the displacement data. In Figure 102, red spot represent laser excitation spot, black circles represent BGA solder balls, dark blue dots represent DCPs to acquire the signal information of BGA solder balls under the die shadow, and the light blue dots represent the peripheral DCPs to acquire the signal information of BGA solder ball under the substrate outside the die shadow.

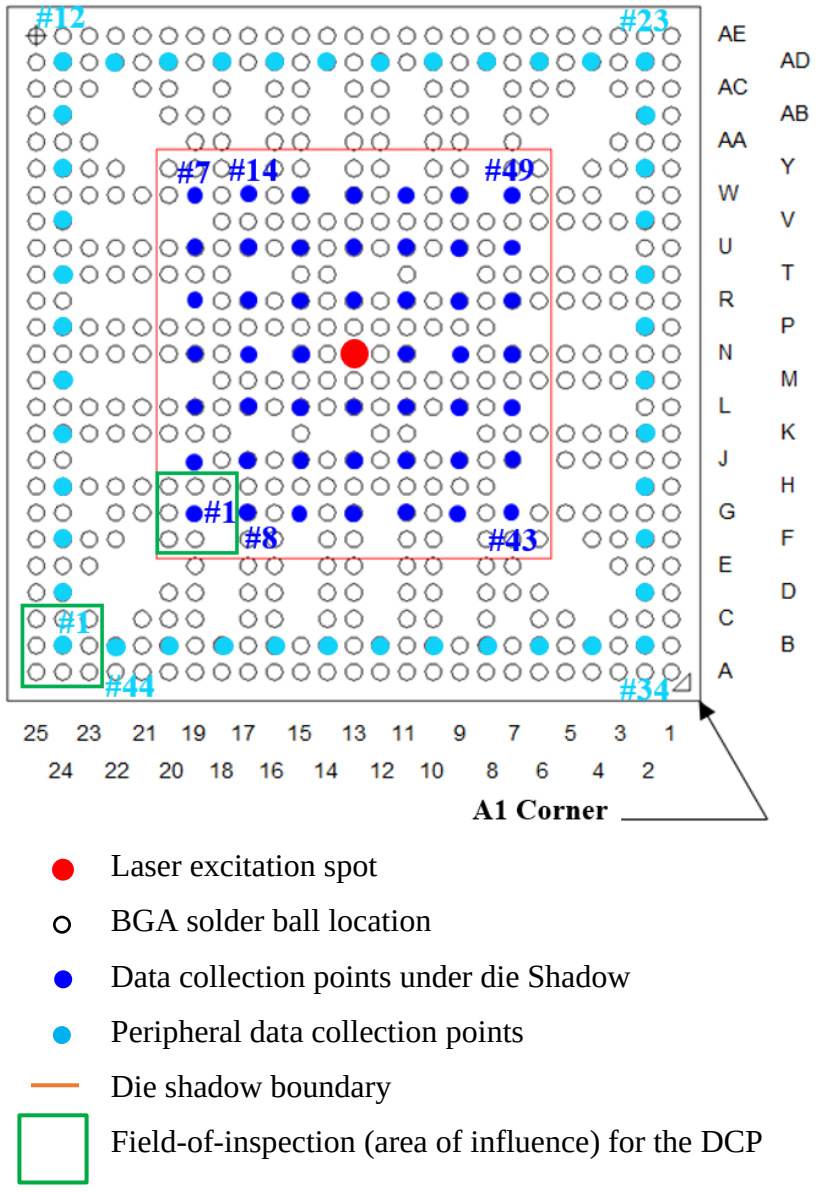


Figure 102 – Inspection pattern for Type – A 17 x 17 FCBGA package

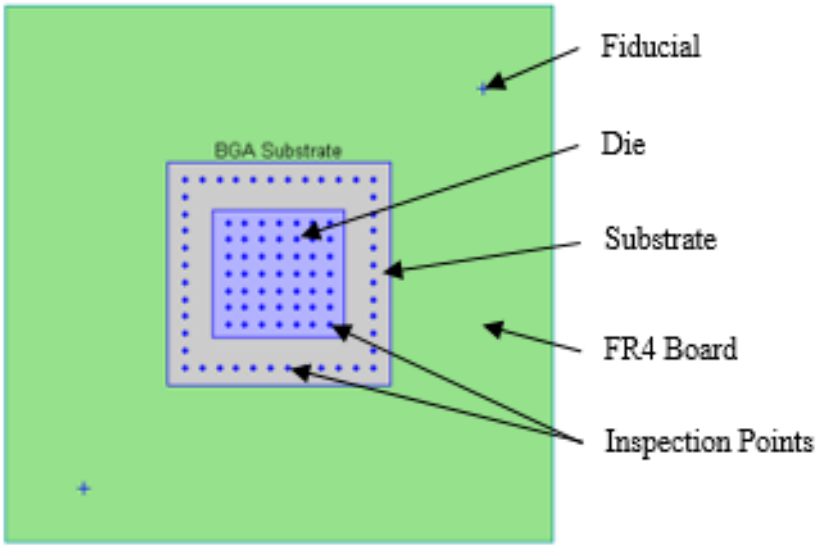


Figure 103 – MATLAB image showing the top view of the package with depicted inspection pattern on the top surface

The interferometer signal from a DCP represents the failure information from a 3 x 3 array of BGA solder balls around the DCP, indicated as field-of-inspection or area of influence. For example, the interferometer signal from DCP #1 at solder ball 19G under the die shadow represents the cumulative failure information from 3 x 3 solder balls in the green square (field-of-inspection) as shown in Figure 102. A significant defect or failure in any of the solder ball in the 3 x 3 array would affect the interferometer signal from the DCP in that field-of-inspection. Experiments (inspection runs) were carried out separately for collecting interferometer data from the top of the die and top of the substrate because the intensity of reflected interferometer laser is different from the die surface and the substrate surface as they have different material surface finish and z-height. The system parameters used for the evaluation of Type – A packages using DALUS are listed in Table 8.

Table 8 – System parameters for the evaluation of 17 x 17 FCBGA test vehicles

Total average pulsed laser power	400 mW
Laser wavelength	1064 nm
Pulse duration	5 ns
Pulse frequency	20 Hz
Interferometer sampling rate	50 x 10^6 samples/s
# sample points considered for MCC	1500
Signals average per DCP	128

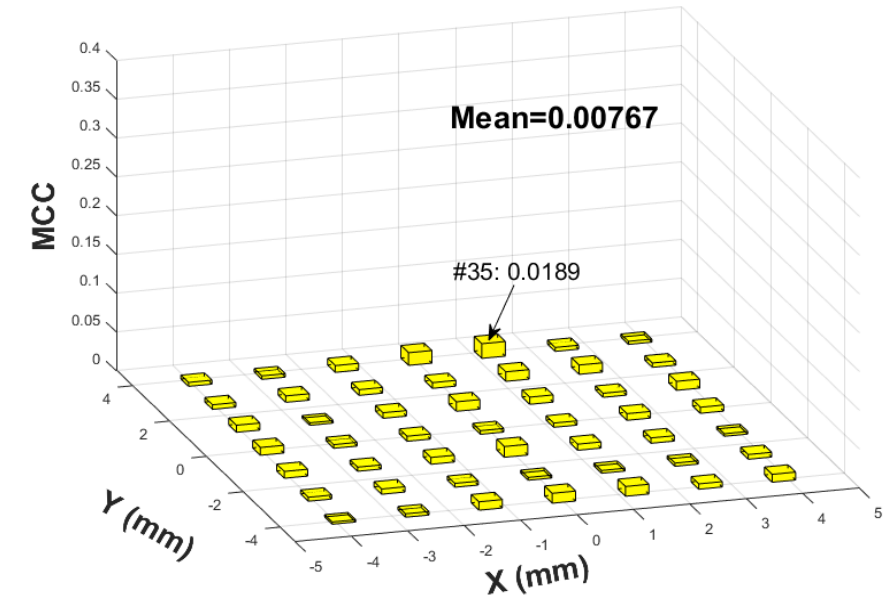
7.4 Results and Discussions

All the test vehicles in Table 7, were inspected using DALUS as per the inspection procedure described in the previous section. Signal analysis was carried out using Equation (1) to calculate MCC values at all DCPs. LUI results were plotted in the form of 3D histograms with MCC value on the z-axis and location of DCP on the XY plane. Separate plots were shown for LUI results on die shadow DCPs and peripheral DCPs. Initially, time-zero samples 9U1, 9U2, 9U3, and 9U4 were compared with each other. LUI results from MCC analysis among 9U1, 9U3, and 9U4 are very similar and they have very low MCC values, indicating that these three time-zero samples are good samples with no or negligible failures.

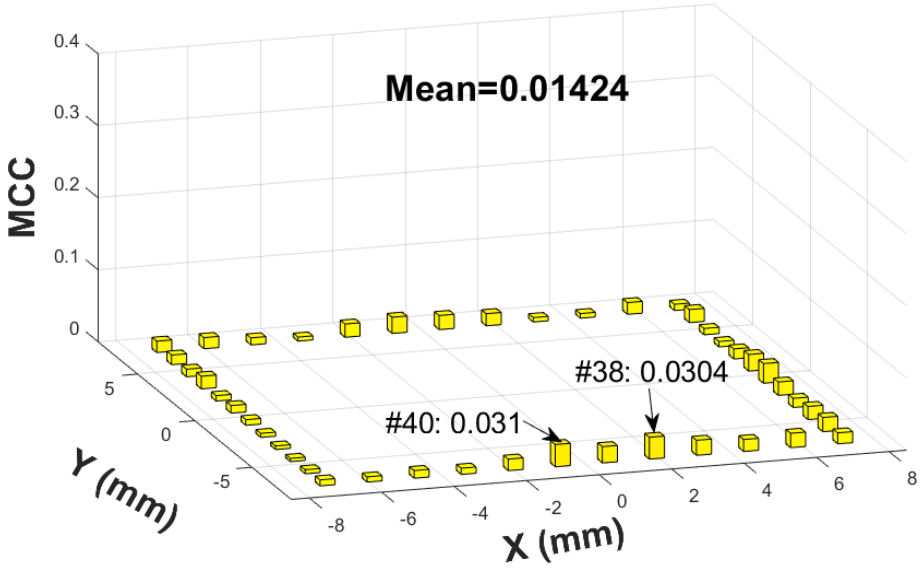
LUI results from MCC analysis between 9U1 and 9U3 is shown in Figure 104. All MCC values are below 0.02 for die shadow DCPs with a mean of 0.008 as shown in Figure 104(a), and below 0.031 for peripheral DCPs with a mean of 0.014 as shown in Figure 104(b). The LUI results from MCC analysis between 9U1 and 9U4 are shown in Figure 105, where all MCC values are below 0.025 for die shadow DCPs with a mean of 0.01, and below 0.04 for peripheral DCPs with mean of 0.018. The LUI results from MCC analysis

between 9U3 and 9U4 are shown in Figure 106, where all MCC values are below 0.004 for die shadow DCPs with a mean of 0.00125, and below 0.034 for peripheral DCPs with mean of 0.007. From these values, LUI evaluation predicts that these samples are good without any significant anomalies.

However, high MCC values are recorded on peripheral DCPs for time-zero sample 9U2 when analyzed with other 3 time-zero samples, 9U1, 9U3, and 9U4. LUI results from MCC analysis between 9U2 and 9U4 is shown in Figure 107. MCC values on die shadow DCPs are low, below 0.023 with a mean of 0.012 as shown in Figure 107(a). But, the MCC values on the right edge of peripheral DCPs are as high as 0.16 as shown in Figure 107(b). Upon scrutiny of the 9U2 sample, it was found that underfill spread (a rough surface) is extended on the BGA substrate which would have produced noise in the interferometer signal and resulted in high MCC values. To validate these LUI results, 9U2 and 9U3 were cross-sectioned and examined using SEM. From the SEM images, the samples were found good with no significant defects or failures.

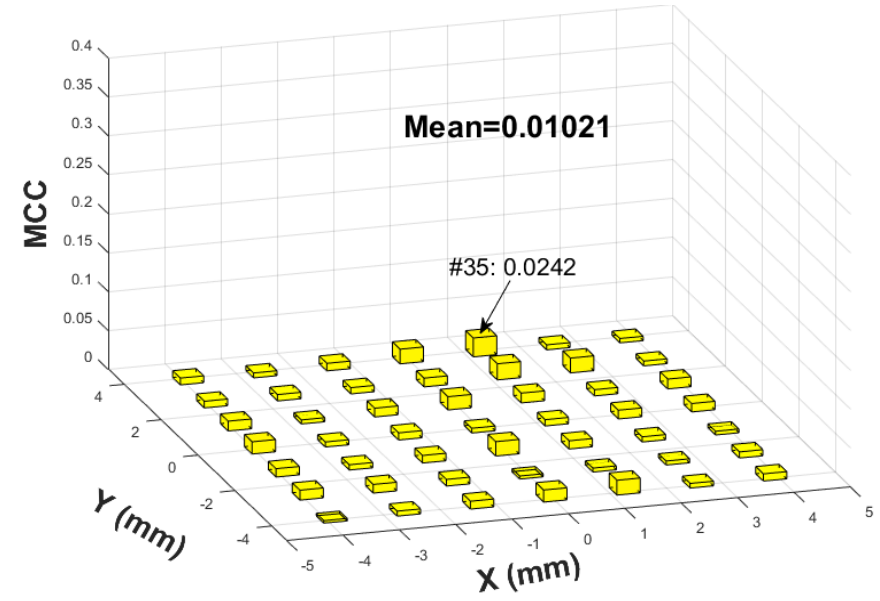


(a)

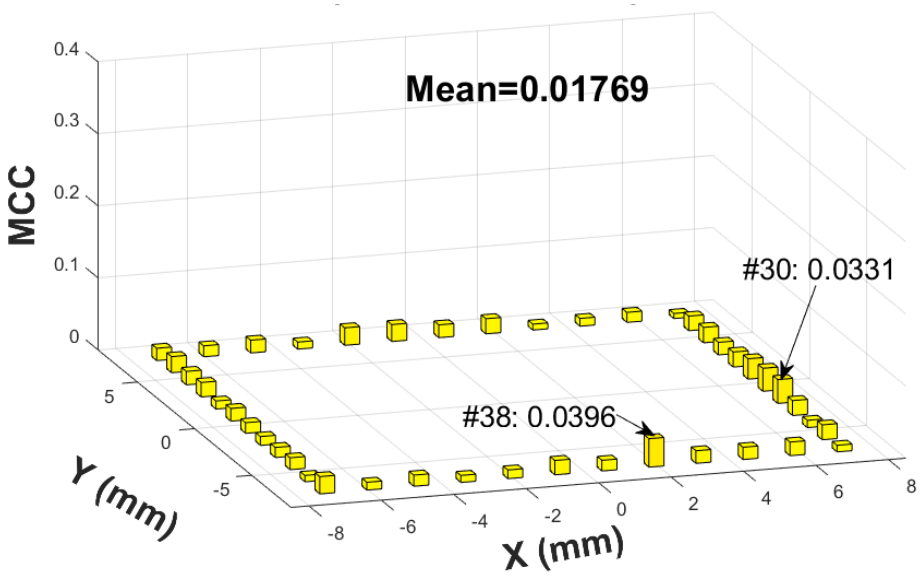


(b)

Figure 104 – LUI results from MCC analysis between 9U1 and 9U3 on (a) die shadow DCPs, and (b) peripheral DCPs

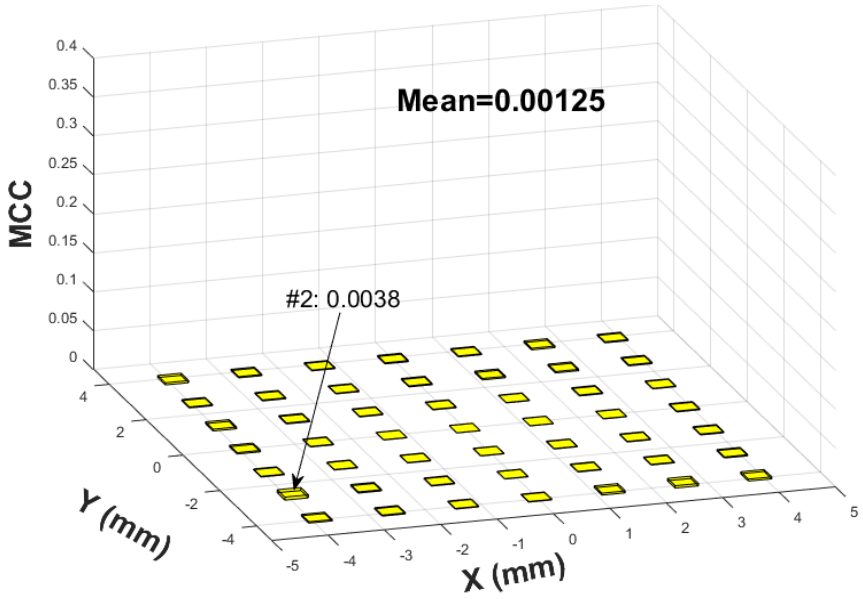


(a)

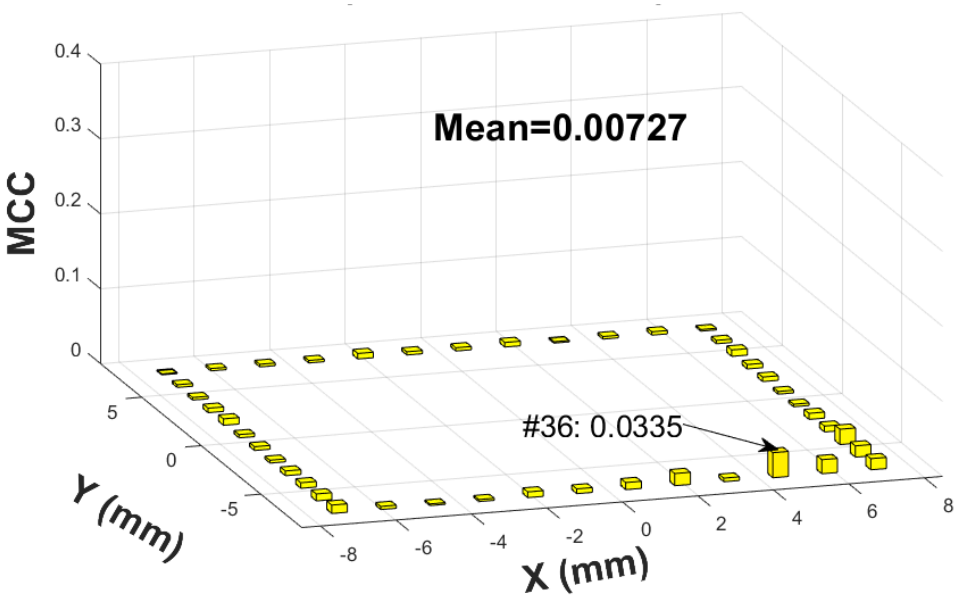


(b)

Figure 105 – LUI results from MCC analysis between 9U1 and 9U4 on (a) die shadow DCPs, and (b) peripheral DCPs

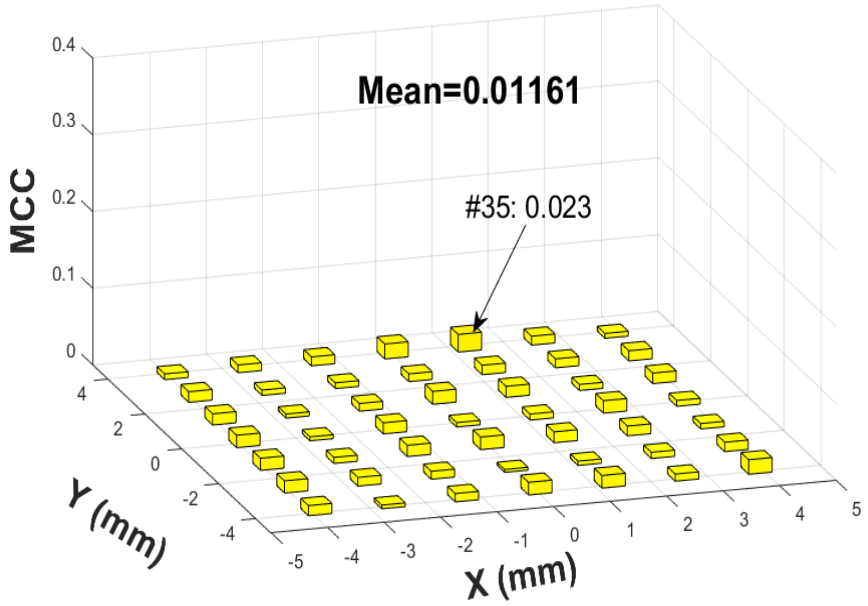


(a)

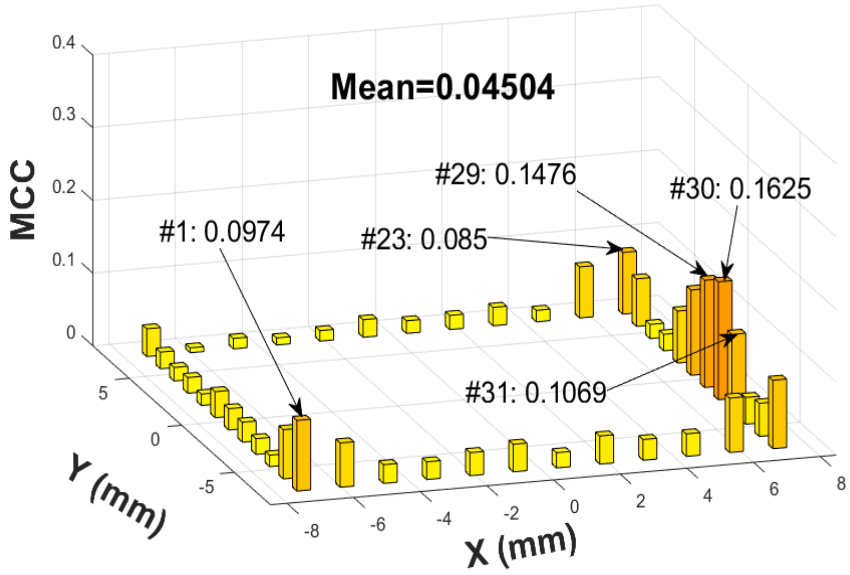


(b)

Figure 106 – LUI results from MCC analysis between 9U3 and 9U4 on (a) die shadow DCPs, and (b) peripheral DCPs



(a)

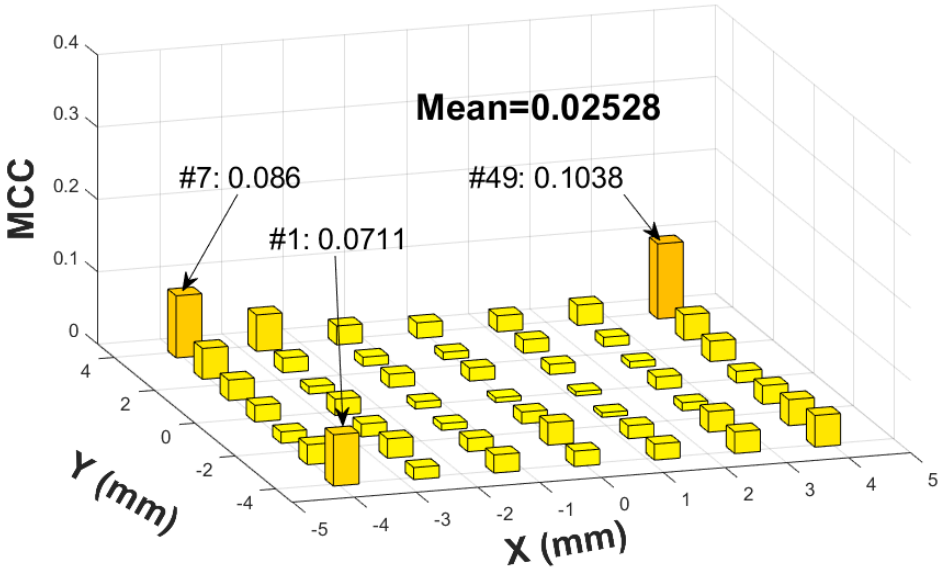


(b)

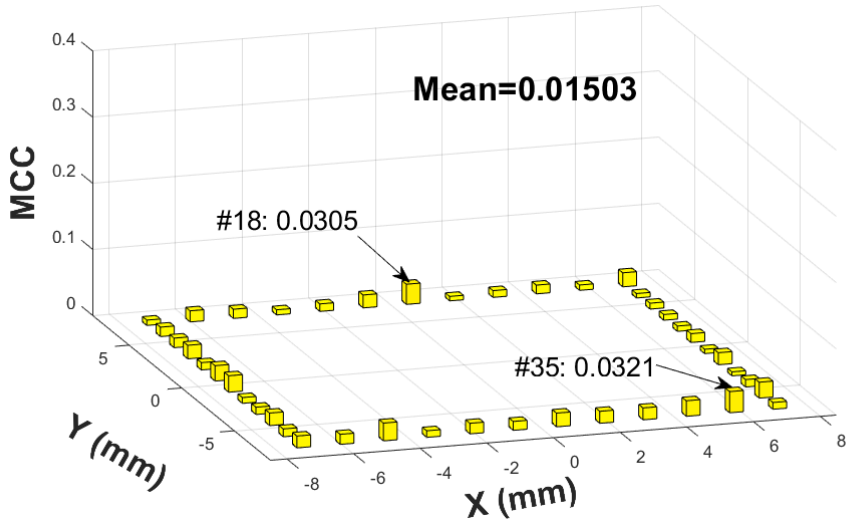
Figure 107 – LUI results from MCC analysis between 9U2 and 9U4 on (a) die shadow DCPs, and (b) peripheral DCPs

From the LUI analysis among the time-zero samples, three samples 9U1, 9U3, and 9U4 are found to be good, those can be used as reference samples for the MCC analysis of failure samples. LUI results for four failure samples (5U1, 5U3, 6U2, and 6U3) from the MCC analysis with any of the three time-zero samples (9U1, 9U3, and 9U4) are similar. Typically, corner BGA solder joints under the die shadow are going to fail first in thermal cycling reliability test due to CTE mismatch between die, substrate, and the board. Hence, high MCC values are expected at the corners under the die shadow. Empirical data suggests that the MCC value above 0.1 will have failures for thermal cycled samples.

The LUI results from MCC analysis between 5U1 and 9U1 are shown in Figure 108. Form Figure 108(a), though the mean of MCC values on die shadow DCPs is low about 0.025, MCC values are relatively high on the corners with highest value of 0.104 on DCP #49. For peripheral DCPs, all MCC values are below 0.032 with a mean of 0.015 as shown in Figure 108(b). Considering the threshold MCC value of 0.1, it is predicted that one or more BGA solder balls in 3 x 3 array at DCP #49 under the die shadow would have significant failures such as IMC cracks. Electric testing results for 5U1 sample from Figure 101, show that the failure net is M11 – Y7, which is at the top right corner under the die shadow. 5U1 sample is pulled out of the thermal chamber at 2,036 cycles, almost immediately after it failed in electrical test at 2,011 cycles. So, 5U1 is confirmed to have failures only in M11 – Y7 net. Hence, both LUI and electrical tests predicted the same location of failed BGA solder balls. This also confirms that the corner BGA solder joints under the die shadow are the first interconnections to fail in thermal cycling.



(a)



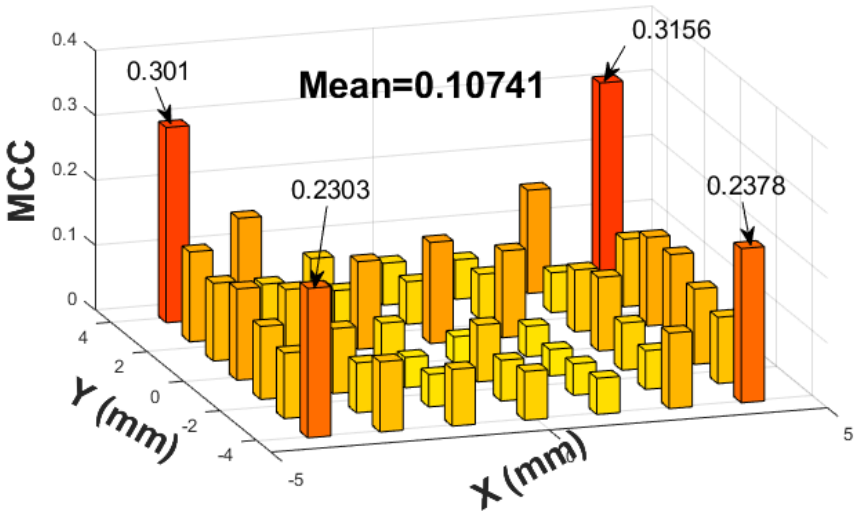
(b)

Figure 108 – LUI results from MCC analysis between 5U1 and 9U1 (Ref)

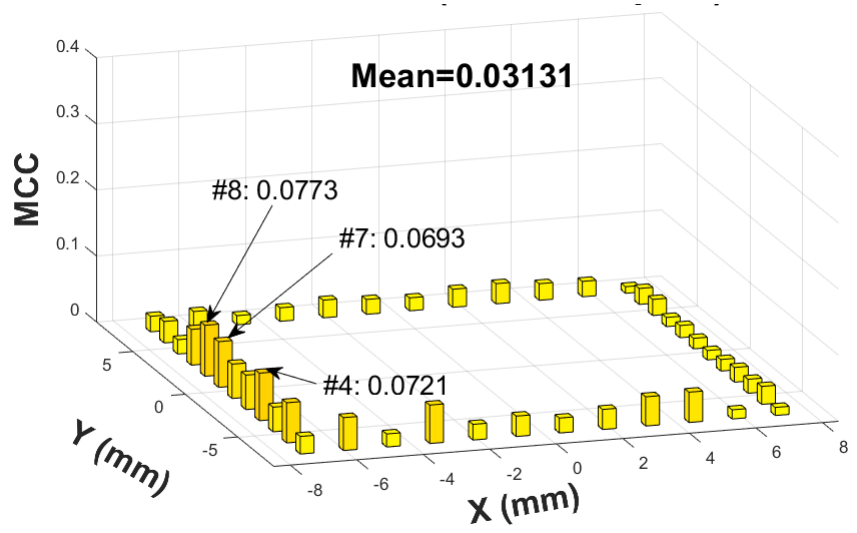
on (a) die shadow DCPs, and (b) peripheral DCPs

Figure 109 shows LUI results from MCC analysis between 5U3 and 9U1. From Figure 109(a), most of the MCC values on die shadow DCPs are high with a mean value of 0.11, which predicts that most of the BGA solder balls under the die shadow would

contain significant failures. From Figure 109(b), the MCC values on the left column peripheral DCPs (#2 to #9) are relatively high around 0.07 but below 0.1. Because most of the left column DCPs have high MCC values, it is predicted to have some level of failures in solder ball columns 19 to 25.



(a)



(b)

Figure 109 – LUI results from MCC analysis between 5U3 and 9U1 (Ref) on (a) die shadow DCPs, and (b) peripheral DCPs

To validate the LUI results, 5U3 sample was cross-sectioned, and columns from 25 to 16 were evaluated using SEM (column numbers and row numbers are shown in Figure 102). No significant failures were found in columns 25, 24, and 23. In columns 22 and 21, significant IMC cracks were found in the center from row ‘G’ to row ‘W’ as shown in Figure 110. As discussed earlier in section 7.3, there were no direct DCPs to acquire the information about columns 21 and 22 just outside the die boundary. The IMC failures in columns 22 and 21 would have influenced the signals acquired from peripheral DCPs from #2 to #9. This explains the relatively high MCC values but not above the threshold value of 0.1 at the center on the left column of peripheral DCPs.

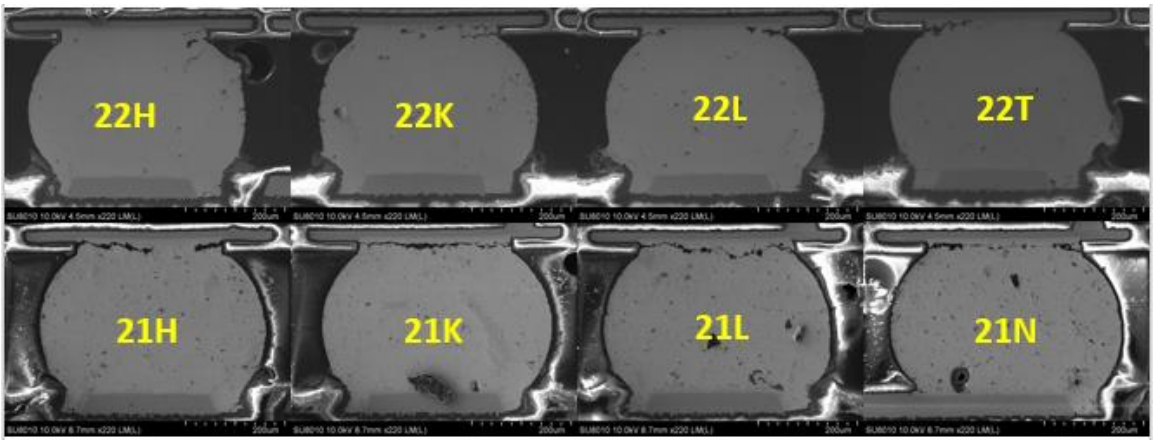


Figure 110 – SEM images of column 22 and 21 of failed sample 5U3, showing significant IMC cracks

Further cross-sectioning into columns 20 to 16, revealed IMC cracks in almost all solder balls under the die shadow and no significant failures outside the die shadow. SEM images of BGA solder balls in the 3 x 3 array of DCP #1 (at 19G solder ball location) under the die shadow is shown in Figure 111. It may be noted that there are no solder balls at 18F, 18G, and 19G locations. As shown in Figure 110, IMC cracks of size 10µm are found

in most of the solder balls under the die shadow. LUI results, as shown in Figure 109(a), also predicted the failures in entire die shadow. Hence, LUI results are validated.

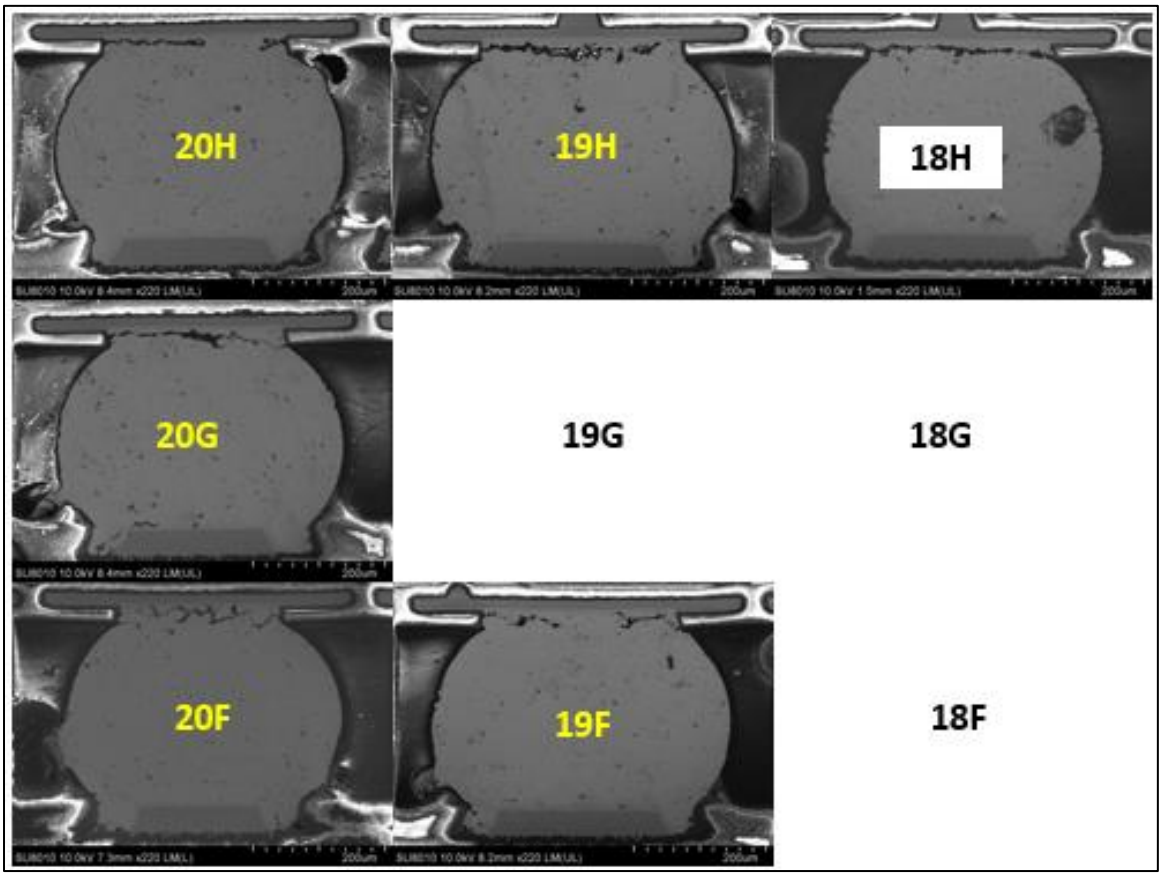
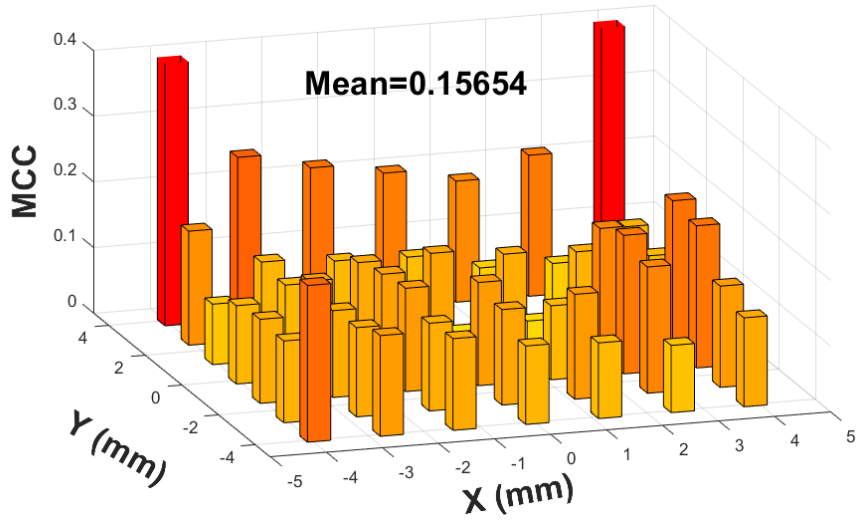


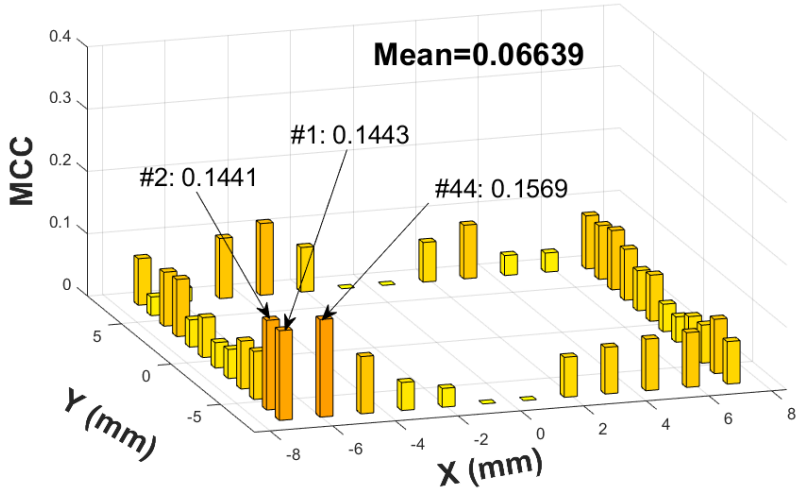
Figure 111 – SEM images of BGA solder balls in the field-of-inspection (3 x 3 array of solder balls) of DCP #1 at solder ball 19G location

Other failure samples 6U1 and 6U2 are also pulled out at 2,929 thermal cycles as 5U3. As expected, these three samples have similar LUI results' trend with high MCC values under the entire die shadow predicting BGA solder ball failures, and low MCC values on the peripheral DCPs, predicting failures in the BGA solder balls just outside the die shadow boundary. To further validate LUI results, the dye-and-pry test was carried out on 6U2 sample. The LUI results from MCC analysis between 6U2 vs 9U1 are shown in

Figure 112. Again, most of the MCC values on die shadow DCPs are high with a mean of 0.16 as shown in Figure 112(a), predicting failures in BGA solder balls under the entire die shadow. From Figure 112(b), apart from relatively high MCC values like in the sample 5U3, MCC values in the bottom left corner peripheral DCPs (#1, #2, and #44) are high about 0.15, predicting some significant failures at A25 corner of 6U2 sample.



(a)



(b)

Figure 112 – LUI results from MCC analysis between 6U2 and 9U1 (Ref) on (a) die shadow DCPs, and (b) peripheral DCPs

The dye-and-pry test results are shown in Figure 113. The presence of red dye indicates the extent of cracks in BGA solder joints. The red dye was present on most of the BGA solder joints under the die shadow and some of the BGA solder joints just outside the die shadow boundary. This means that there were partial to complete cracks in most of the BGA solder balls under the die shadow, which validates the LUI results shown in Figure 112(a).

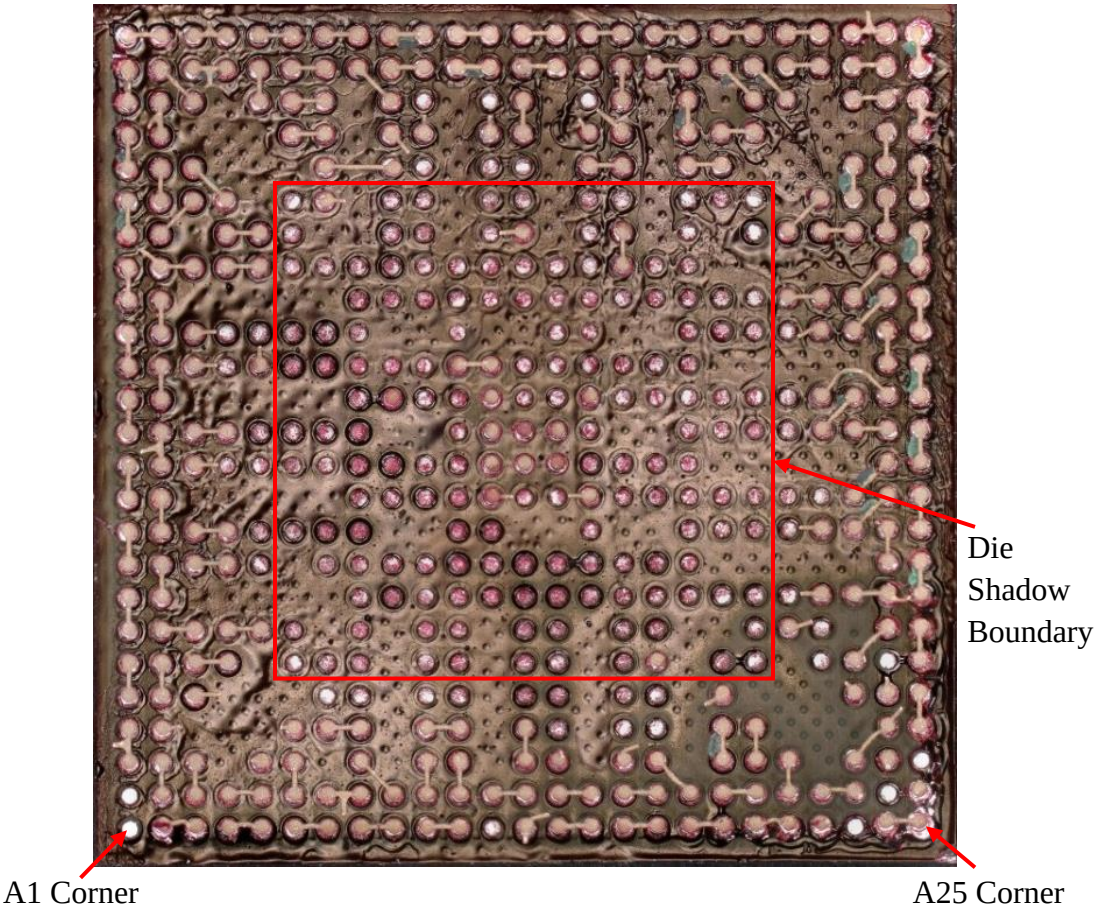


Figure 113 – Dye-and-pry test result on failure sample 6U2

From Figure 113, it is also observed that most of the solder joints outside the die shadow are intact, and red dye was present in some of the solder joints just outside the die shadow boundary. Relatively high MCC values in Figure 112(b) would have resulted

because of the cracks in BGA solder joints just outside the die shadow boundary. To validate the high MCC values at lower left corner (A25) peripheral DCPs (#1, #2, and #44), SEM image was captured at A25 corner as shown in Figure 114. From SEM image, A25 corner BGA solder balls are observed to have lower stand-off height with flattened solder balls as shown in Figure 114. Therefore, it is presumed that the lower stand-off height of the BGA solder balls at the A25 corner produced high MCC values at peripheral DCPs #1, #2, and #44.

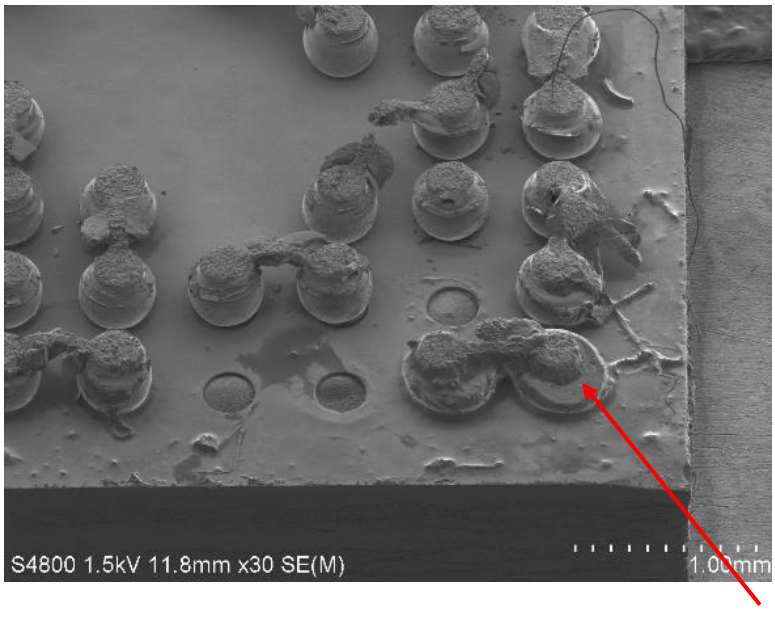


Figure 114 – SEM image of failure sample 6U2 at A25 corner after the dye-and-pry test

7.5 Summary

This study has demonstrated the utility of DALUS for evaluating BGA solder ball interconnection quality in industrial FCBGA packaging subjected to thermal cycling. All the test vehicles listed in Table 7, have been inspected using DALUS. The system could detect IMC cracks yielded from the thermal cycling test accurately. The LUI results are

validated with the results from electrical testing, SEM, and dye-and-pry. The achieved average throughput per part with 93 DCPs is about 15 minutes.

In this research, DALUS could evaluate the overall failures in the BGA solder balls in 17 x 17 FCBGA packages subjected to the thermal cycling reliability test. However, solder ball to solder ball correlation between LUI results (MCC values) and SEM results or dye-and-pry results could not be established. The FCBGA packages used in this research are highly stressed end-of-life failure samples which might contain defects and failures other than in BGA solder balls, inside the substrate, between the die and substrate, or inside the die itself. As the LUI technique is a cumulative defects and failures measurement technique, it is difficult to correlate the LUI results on these samples with SEM or dye-and-pry results. In the future, a progressive approach of performing LUI after every ~100 thermal cycles shall be planned to establish a better correlation between LUI results and the severity of BGA solder ball failures.

CHAPTER 8. CORRELATION STUDIES BETWEEN EXPERIMENTAL DATA AND FINITE-ELEMENT MODELING RESULTS

A thermal cycling reliability test is an effective life prediction model for a microelectronic package in the field. However, thermal cycling is a tedious and expensive process, and it should be accompanied by failure analysis tests like electrical tests and destructive tests for every 150 thermal cycles. With this complex procedure, the thermal cycling test, sometimes, might take several months to complete. Researchers have developed virtual reliability assessment models using finite-element simulations to predict fatigue life which will help in planning the thermal cycling tests [55].

Non-destructive LUI is a worthwhile method to use along with thermal cycling reliability testing. LUI method can replace other non-destructive and destructive failure analysis methods to check for the failures during the thermal cycling test. The life of a microelectronic package can be estimated accurately by measuring MCC values at a fewer number of thermal cycles. As explained in the previous chapters, LUI results (MCC values) and the severity of failure have a very good correlation.

In this chapter, LUI results (MCC values) on 17 x 17 FCBGA samples subjected to thermal cycling, as detailed in section 7.1, are correlated with finite-element results. Accumulated inelastic strain per cycle and/or accumulated inelastic work density per cycle in the solder joints are used as damage metrics from the finite-element model to build correlation with MCC values. From these correlation studies, MCC values can be predicted

from the number of thermal cycles or the accumulated inelastic strain per cycle and/or accumulated inelastic work density per cycle in finite-element simulations. Also, based on MCC values, the number of thermal cycles the sample underwent and accumulated inelastic strain per cycle and/or accumulated inelastic work density per cycle in the solder joints can be estimated. Additionally, the fatigue life of microelectronic packages can be predicted more accurately from LUI results. finite-element simulations are helpful to visualize the failure trends in BGA solder balls under thermal cycling loading conditions and to support experimental work presented in CHAPTER 7.

8.1 Finite-Element Model

The finite-element analysis procedure for the 17 x 17 FCBGA packages is outlined in this section. A 2D finite-element model with diagonal solder balls was developed using ANSYS Workbench 19.2®. In this section, the geometrical model, meshing, material models, and loading conditions used in the finite-element model are described first. This is followed by the results of the finite-element simulations. Then, the results from the finite-element simulations are combined with experimental results to develop correlation equations.

8.1.1 Geometrical Model

Two-dimensional half-symmetry model across the diagonal solder balls was constructed by taking advantage of the structural symmetry of the 17 x 17 FCBGA package as shown in Figure 115. Schematics of the geometric model, different components in the model and meshing is shown in Figure 115. The important geometrical dimensions of the package were obtained by Texas Instruments. Solder balls and copper pads dimensions

were measured from SEM images. Pitch of the solder balls is 0.65 mm. The model consists of a silicon die, underfill, top build-up layer, substrate core, bottom build-up layer, top copper pads, solder mask, SAC 305 BGA solder balls, bottom copper pads, and PCB as shown in Figure 115. Meshing was done with shared topology, mapped meshing, and refined meshing in the solder ball with 5µm element size at the top of solder ball interfacing with the top copper pad and with 10µm element size in the remaining part of the solder ball.

8.1.2 Material Models

A summary of the materials used for various parts of the PBGA package along with the material modeling method used is shown in Table 9. Underfill, build-up layer, substrate core, and solder mask were modeled as non-linear elastic and remaining materials are modeled as linear elastic. Temperature dependency was taken into consideration for all the applicable materials. The PCB is a fiber-reinforced epoxy which makes the properties differ in the out-of-plane direction. Orthotropic properties are therefore used for PCB. All the material properties were obtained from Texas Instruments as listed in Table 9, Table 10, and Table 11.

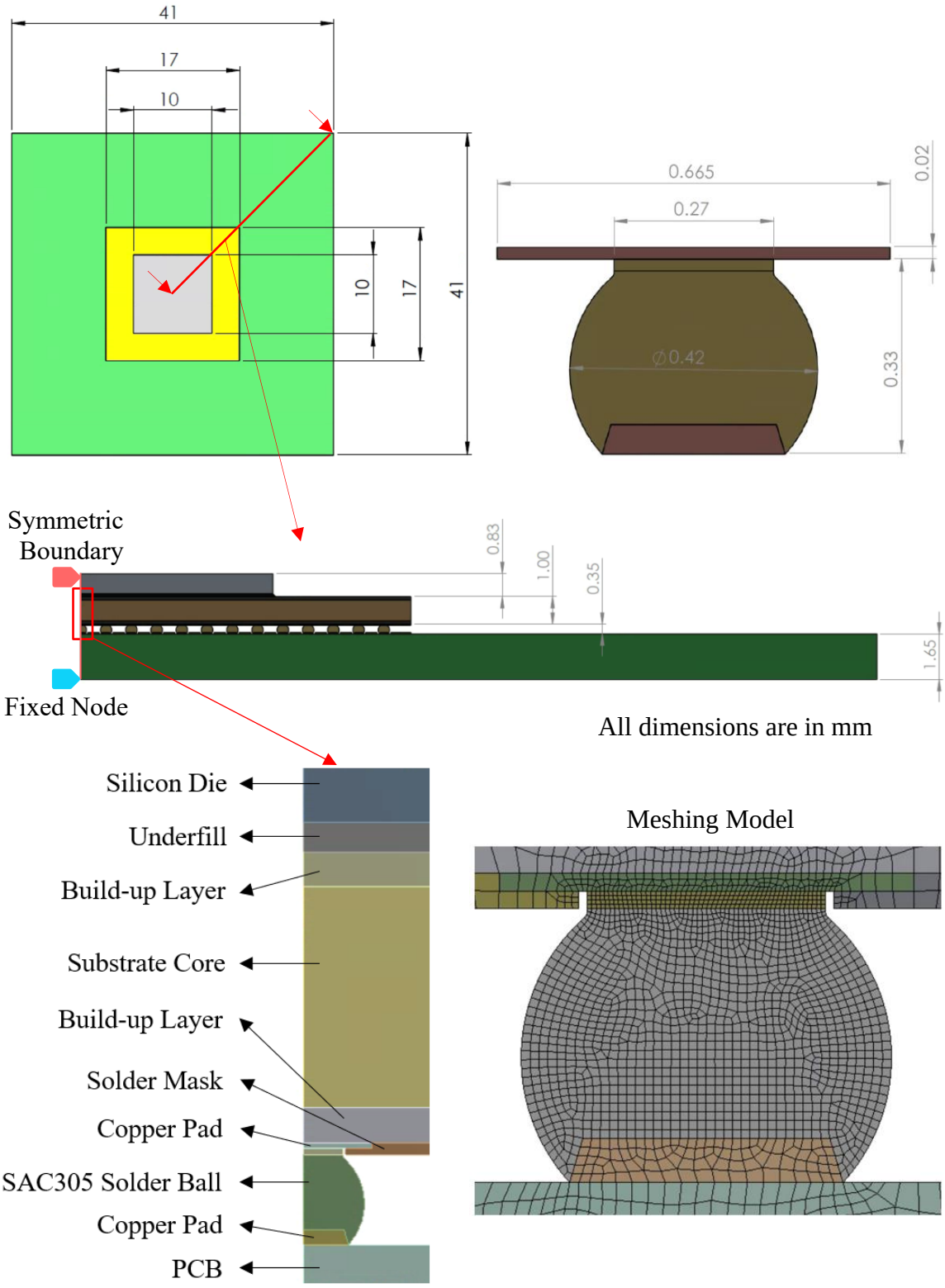


Figure 115 – Finite-element modeling of 17 x 17 FCBGA package

Table 9 – Material property details for the 17 x 17 FCBGA package

Name of Part	Material	Material Property	Temperature Dependency	Modulus E (GPa)	CTE (ppm/C)	Poisson Ratio
Die	Silicon	Elastic isotropic	No	131	2.61	0.278
Underfill	Underfill	Elastic isotropic	Yes	Table 10	Table 10	0.35
Build-up Layer	ABF	Elastic isotropic	Yes	Table 11	Below Tg (131°C): 46 Above Tg (131°C): 120	0.34
Substrate Core	Core Material	Elastic isotropic	Yes	Table 11	Below Tg (189°C): 11 Above Tg (189°C): 4	0.33
Solder Mask	Solder Mask	Elastic isotropic	Yes	Table 11	Below Tg (105°C): 55 Above Tg (105°C): 140	0.35
Copper Pad	Copper	Elastic isotropic	No	118	16.3	0.33
Solder Ball	SAC305	Elastic viscoplastic	Yes	47.51 – 0.194T	23.5	0.4
PCB	BLR Board	Elastic orthotropic	Yes	22.4 @ -40°C 18.7 @ 125°C	In-plane: 14.5 @ -40°C 18 @ 125°C Out-of-Plane: 65	0.255

Table 10 – Material properties for the underfill

Temperature (°C)	Modulus (MPa)
-55.2	12200
-40.2	11700
70	9130
88.1	8190
91.6	7910
115.3	780
121	190
125.2	110
149.9	60
260	150

Temperature (°C)	CTE (ppm/C)
-50	25
-40	25
80	41
90	50
110	93
120	101
130	102
150	101
170	100
260	72

Table 11 – Modulus for the build-up layer, substrate core, and solder mask

Temperature (°C)	Modulus (MPa)		
	Build-up Layer	Substrate core	Solder Mask
	7021 @ 17°C	20249 @ 31°C	4991 @ 28°C
25	6867		
50	6392	19946	4902
75	5916	19643	4422
100	5399	19232	3701
125	4084	18605	2286
150	3203	17741	916
175	629	16724	329
200	126	15384	214
225	126	13870	214
250	98	12595	267
275	98	11730	347
300		11557	391

The solder balls in the 17 x 17 FCBGA package is SAC305 alloy. The SAC305 solder balls are modeled with linear elastic combined with viscoplastic material property. The modulus of the solder joint is temperature-dependent and given as Equation (4). CTE of the solder balls is 23.5 ppm/C.

$$E(GPa) = 47.51 - 0.194T(℃) \quad (4)$$

The Anand's unified viscoplastic model [66] was employed to represent the inelastic deformation behavior for SAC305 solder alloys. ANSYS Workbench provides a simple way to directly implement this material model by providing the nine constants listed in Table 12. These properties have been provided by Texas Instruments and the same values have been determined experimentally by Mysore et al. [67].

Table 12 – Anand's model constants for SAC305 solder ball

Parameter	Value	Description
S_0 (MPa)	2.15	Initial value of deformation resistance
Q/R (K)	9970	Activation energy/Boltzmann's constant
A (1/sec)	17.994	Pre-exponential factor
ξ	0.35	Multiplier of stress
m	0.153	Strain rate sensitivity of stress
h_0(MPa)	1525.98	Hardening constant
$\hat{s}$ (MPa)	2.536	Coefficient for deformation resistance saturation value
n	0.028	Deformation resistance value
a	1.69	Strain rate sensitivity of hardening

8.1.3 Accelerated Thermal Cycling Loading Condition

Before subjecting the package to thermal loading conditions as seen in ATC, the stress-free temperatures of the various materials used in the package needs to be determined. The stress-free temperature of material corresponds to the temperature at which the material has either been cured or assembled. The silicon die was assembled to the package substrate using flip-chip solder bumps, then underfill was introduced between the die and substrate. This underfill was cured at 120°C. The stress-free temperature of the whole package, excluding the copper pad, was therefore assumed to be 120°C. The package with the BGA solder balls was then reflowed in an oven to mount it on a PCB. During reflow, the solder melts and its stress goes to zero. The stresses in the copper pads on the package and the board side and the stresses in the PCB are also zero at the melting temperature of the solder. As the assembly cools down, stresses build up in the copper pads, solder joints, and the PCB board. The stress-free temperature of copper pads, solder balls, and PCB was therefore assumed to be equal to the melting point of the solder, 217°C.

As discussed in section 7.2, IPC 9701 test condition TC3 was employed as a thermal reliability test condition for 17 x 17 FCBGA packages. To account for stress-free temperature effects, the package was simulated with a loading profile which involves cooling down from the melting temperature to room temperature in 15 minutes and then maintaining at room temperature for 15 minutes. The package was then simulated to be subjected to a loading profile as seen during ATC test condition TC3, which involves a temperature range of -40°C ↔ +125°C with 15 minutes dwell at both high temperature and low temperature and 11°C/minute ramp rate. Totally 10 thermal cycles (1 hour/cycle) were

considered for simulation to establish a stable stress-strain hysteresis loop. The simulated temperature profile is shown in Figure 116.

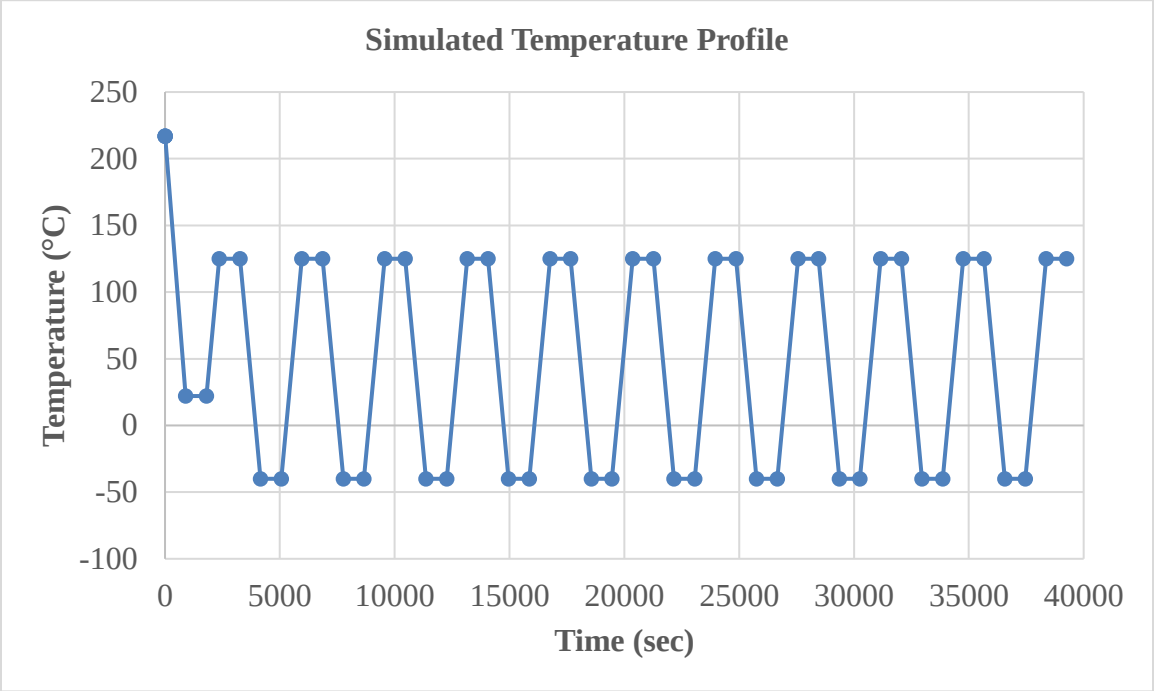
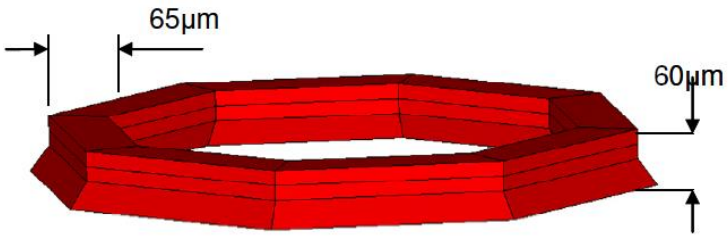


Figure 116 – The simulated temperature profile of ATC test for 17 x 17 FCBGA packages

8.2 Finite-Element Simulation Results

The objective of the finite-element simulation is to extract damage metrics for the relevant solder joints for one complete thermal cycle. The accumulated inelastic strain and accumulated inelastic work density are the two most commonly used damage metrics. To prevent any mesh dependency from affecting the results, the damage metrics were area-averaged. In 3D finite-element models, Darveaux [56] has used a solid thin layer of elements near the package-solder interface for volume averaging to derive the damage metrics. Tunga et al. [55] and Che et al. [68] have shown that an annular thin layer of

elements gives a better correlation with experimental results compared to a solid thin layer. Tunga et al. [55] used an annular region at the top of the solder ball as shown in Figure 117. The 2D model equivalent of the annular layer of elements in the 3D model is the elements in the annular cross-section area, as shown in Figure 118. It may be noted that the elements are distributed into two areas on both ends on top of the solder ball. This cross-section has an area of 20µm x 20µm on each side.



[55]

Figure 117 – An annular layer of elements for volume-averaging used by Tunga

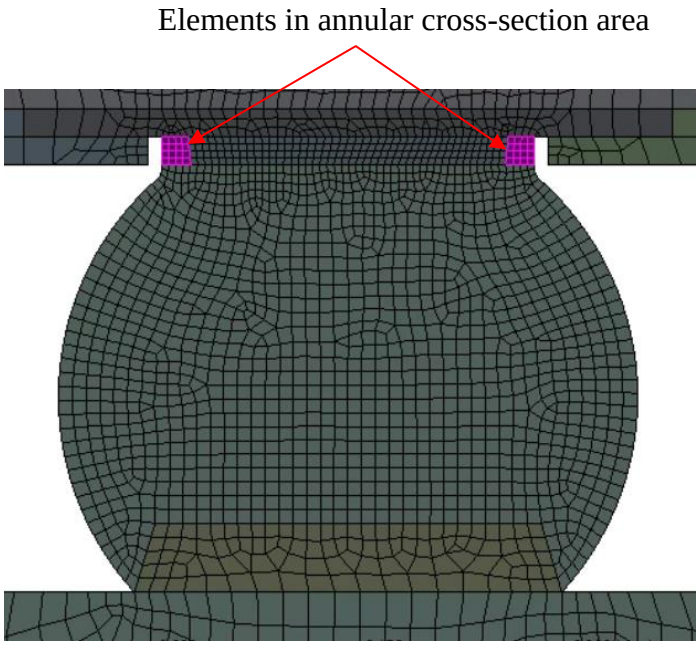


Figure 118 – The annular cross-section area of elements for area averaging for determining the damage metrics

The accumulated inelastic work density for one thermal cycle for a given element is given by Equation (5).

$$\Delta W_{acc} = \sum_{i=1}^{NINT} \sum_{j=1}^{NCS} \{\sigma\}^T \{\Delta \varepsilon^{in}\} A_i \quad (5)$$

Where NINT is the inelastic strain increment, NCS is the total number of converged substeps, σ is the current stress, $\Delta\varepsilon^{in}$ is the inelastic strain increment and A_i is the area of the element. This inelastic work density for an element can easily be extracted from ANSYS workbench APDL post-processing using the NLPLWK command. If N represents the number of load steps in one simulated ATC, the accumulated inelastic work density in one cycle for a given element is given by Equation (6).

$$\Delta W_{acc} = W_N - W_1 \quad (6)$$

Where W_N is the inelastic work density during the last load step of the cycle and W_1 is the inelastic work density during the first load step of the cycle. The area-averaged inelastic work density per thermal cycle is given by Equation (7).

$$\Delta W_{acc,avg} = \frac{\sum_{element} \Delta W_{acc} . A}{\sum_{element} A} \quad (7)$$

Where A is the area of a single element. APDL commands with NLPLWK were inserted in ANSYS Workbench according to Equation (6) and Equation (7) to obtain the accumulated inelastic work density/cycle in the annular cross-section area (shown in Figure 118) of every solder ball.

The accumulated inelastic strain for a given element is given by Equation (8),

$$\varepsilon_{acc}^{in} = \sum_{i=1}^{N-1} \frac{\sqrt{2}}{3} \sqrt{\left(\left(\Delta\varepsilon_{x,i,i+1}^{in} - \Delta\varepsilon_{y,i,i+1}^{in}\right)^2 + \left(\Delta\varepsilon_{x,i,i+1}^{in}\right)^2 + \left(\Delta\varepsilon_{y,i,i+1}^{in}\right)^2 + 6\left(\Delta\varepsilon_{xy,i,i+1}^{in}\right)^2\right)}$$

$$\Delta\varepsilon_{p,i,i+1}^{in} = \Delta\varepsilon_{p,i+1}^{in} - \Delta\varepsilon_{p,i}^{in} \tag{8}$$

Where, $\Delta\varepsilon_{p,i,i+1}^{in}$ is the difference of the p component of the inelastic strain between the $(i+1)^{th}$ and the i^{th} load step. This accumulated inelastic strain for an element can easily be extracted from ANSYS workbench APDL post-processing using the NLEPEQ command. the accumulated inelastic strain in one cycle for a given element is given by Equation (9).

$$\Delta\varepsilon_{acc}^{in} = \varepsilon_{acc_N}^{in} - \varepsilon_{acc_1}^{in} \tag{9}$$

Where, $\varepsilon_{acc_N}^{in}$ is the accumulated inelastic strain during the last load step of the cycle and $\varepsilon_{acc_1}^{in}$ is the inelastic strain during the first load step of the cycle. The area-averaged accumulated inelastic strain is given by Equation (10).

$$\Delta\varepsilon_{acc,avg}^{in} = \frac{\sum_{element} \Delta\varepsilon_{acc}^{in}.A}{\sum_{element} A} \tag{10}$$

Where A is the area of a single element. APDL commands with NLEPEQ were inserted in ANSYS Workbench according to Equation (9) and Equation (10) to obtain the accumulated inelastic strain/cycle in the annular cross-section area (shown in Figure 118) of every solder ball.

For ease of further discussion, solder balls are numbered, being center solder ball as #1 and last solder ball as #13 as shown in Figure 119. Solder ball #8 is the last solder ball under the die shadow.

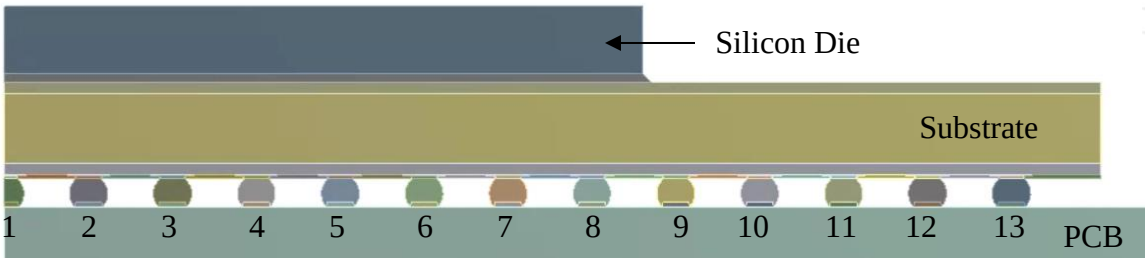


Figure 119 – Numbering of solder balls in finite-element simulations

The damage metrics per cycle are known to vary with the number of cycles and tend to stabilize after a few cycles. The results from the stabilized cycle should be used for further analysis. Ten thermal cycles were simulated as shown in Figure 116, to achieve the change in accumulated inelastic work density $\Delta W_{acc,avg}$ between consecutive cycles in the viscoplastic model below 0.05% and the change in accumulated inelastic strain $\Delta \varepsilon^{in}_{acc,avg}$ between consecutive cycles below 0.1%. A plot showing the variation of $\Delta W_{acc,avg}$ and $\Delta \varepsilon^{in}_{acc,avg}$ on solder ball #7 with the number of cycles is given in Figure 120. It can be seen from the plot that after seven cycles, both $\Delta W_{acc,avg}$ and $\Delta \varepsilon^{in}_{acc,avg}$ tends to stabilize. The results from the 10th cycle were therefore used for all subsequent analysis.

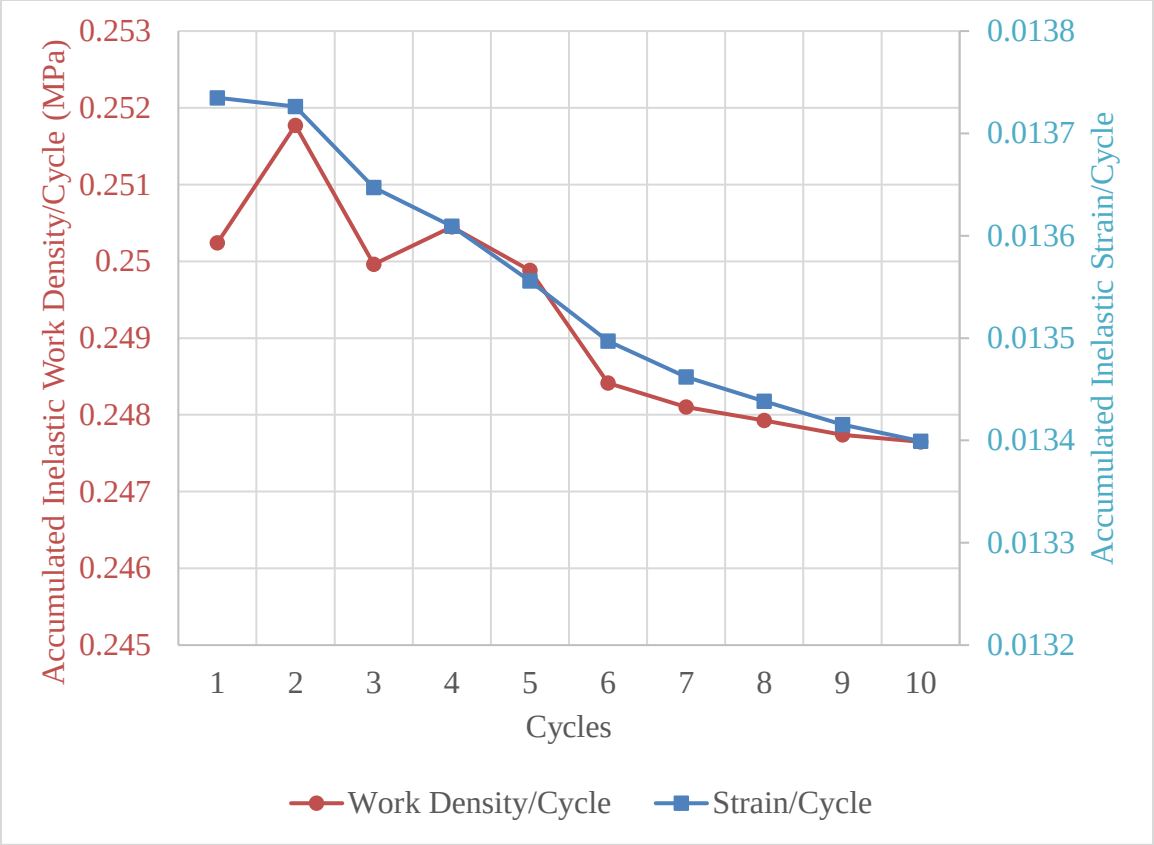


Figure 120 – Damage metrics per cycle vs Cycle count

A contour plot showing the variation of the accumulated inelastic work density and accumulated inelastic strain at the end of the 10th thermal cycle for solder ball #7, under the die shadow are given in Figure 121 and Figure 122 respectively. It can be seen from Figure 121 and Figure 122 that the maximum damage metrics (accumulated inelastic work density and accumulated inelastic strain) occurs on the top ends of the solder joint. Cracks due to thermal fatigue are therefore expected to occur and propagate along the intermetallic region on the top of the solder joint. Detailed failure modes of thermal cycling were presented in section 7.4.

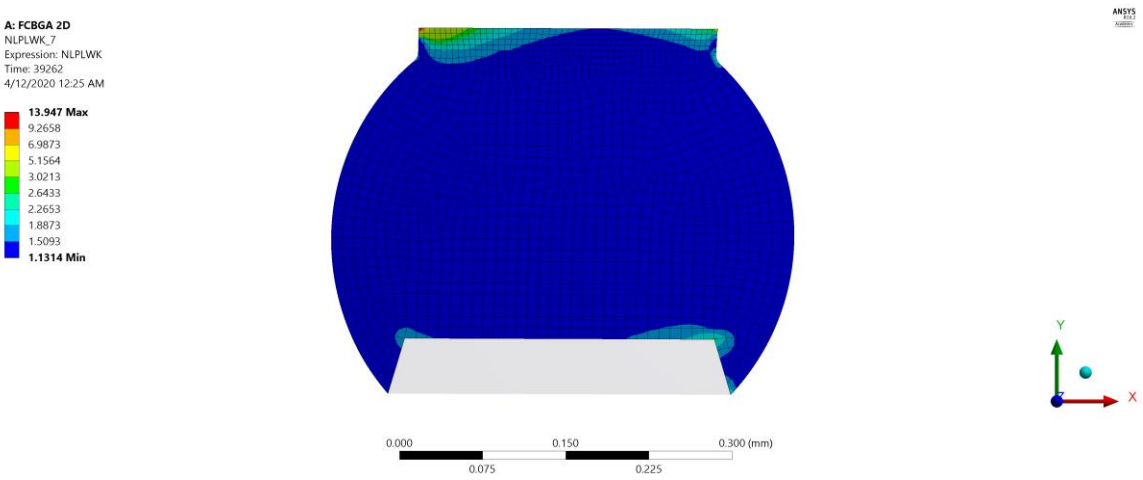


Figure 121 – Accumulated inelastic work density at the end 10th thermal cycle for solder ball #7

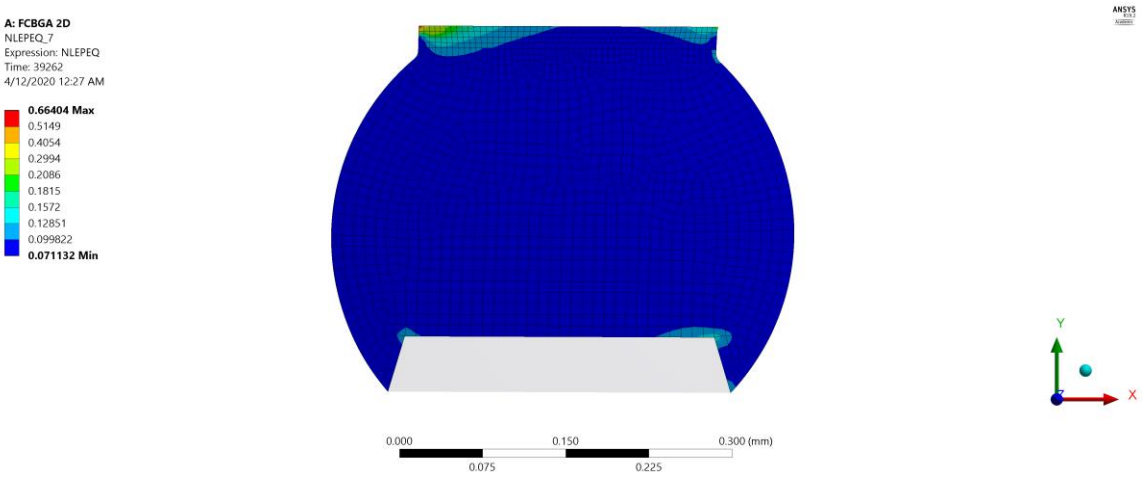


Figure 122 – Accumulated inelastic strain at the end 10th thermal cycle for solder ball #7

The area-averaged damage metrics for all the solder were determined and presented in Figure 123. The location of the die edge for the package is indicated by a vertical line on the plot. Both the damage metrics show similar variation along the solder balls. From the center solder ball (#1) of the package, the damage metrics in the solder balls increase

and reach a maximum on solder #7 located second from the die edge under the die shadow. Damage metrics then decreases across the die edge and increases gradually towards the package edge. Increased shear deformation due to CTE mismatch between the silicon chip and the package is the cause for the increasing variation from solder ball #1 to solder ball #7. There is very minimal difference between the CTEs of the package substrate and the PCB, hence, the decreasing variation across the die edge. The CTE difference between the silicon chip and the PCB, therefore, has more of an effect in determining this variation. Because of the similar variation, any of the two or both damage metrics can, therefore, be used for correlation studies.

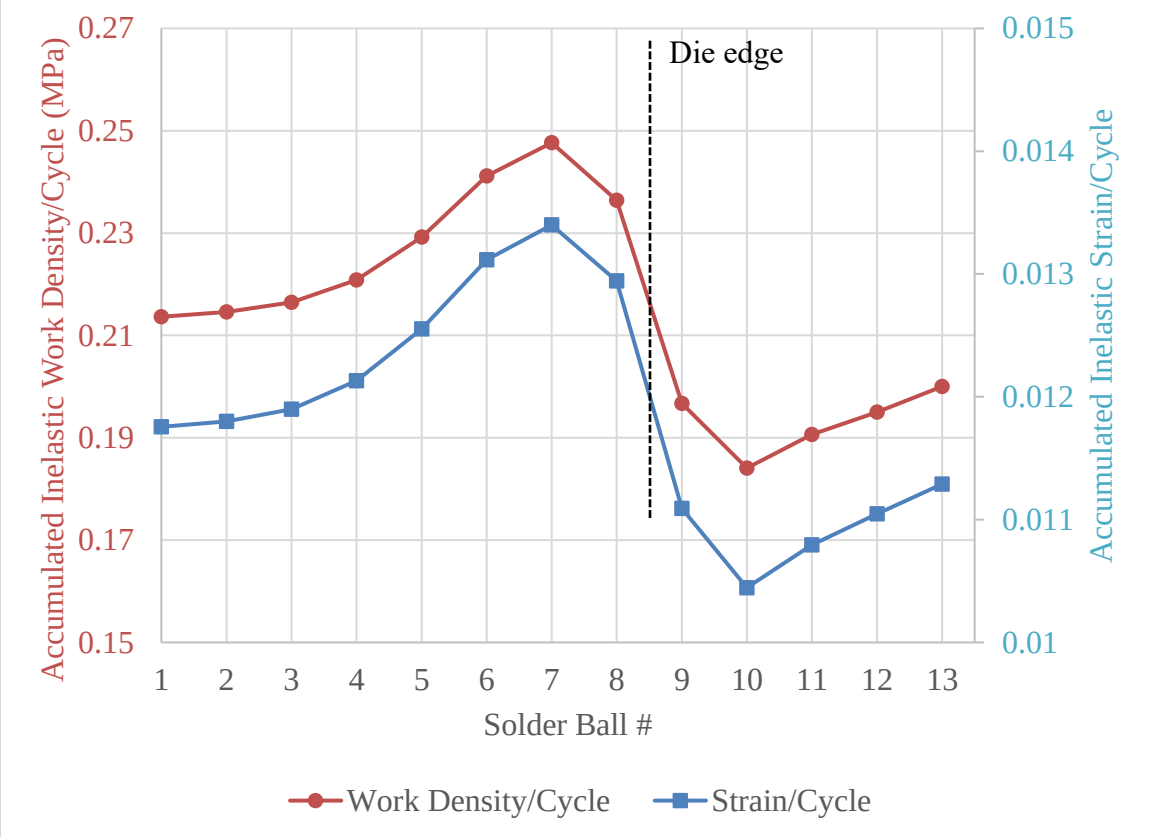


Figure 123 – Area averaged damage metrics per thermal cycle along the diagonal solder balls

8.3 LUI Results

As discussed before, 17 x 17 FCBGA samples subjected to thermal cycling were used for correlation studies. In total six 17 x 17 FCBGA samples were available which are subjected to thermal cycling as listed in Table 13. Detailed inspection procedure and results on Type – A samples were discussed in CHAPTER 7.

Table 13 – Details of 17 x 17 FCBGA samples used for correlation studies

Type of 17 x 17 FCBGA Package	Package Label	Number of thermal cycles (N)
Type – A	5U1	2036
	5U3	2929
	6U1	2929
	6U2	2929
Type – B	FU3	1293
	FU4	1293

Type – B test vehicle details and the inspection procedure are discussed in section 9.1. Both the test vehicles FU3 and FU4 were inspected using DALUS, and the LUI results in the form of 3D histograms with MCC value on the z-axis and location of DCP on XY plane are shown in Figure 124 and Figure 125. RU2 sample is used as a reference sample and more details about reference samples are presented in CHAPTER 9. As expected, corners have high MCC values, predicting high strain at the corner solder balls under the die shadow.

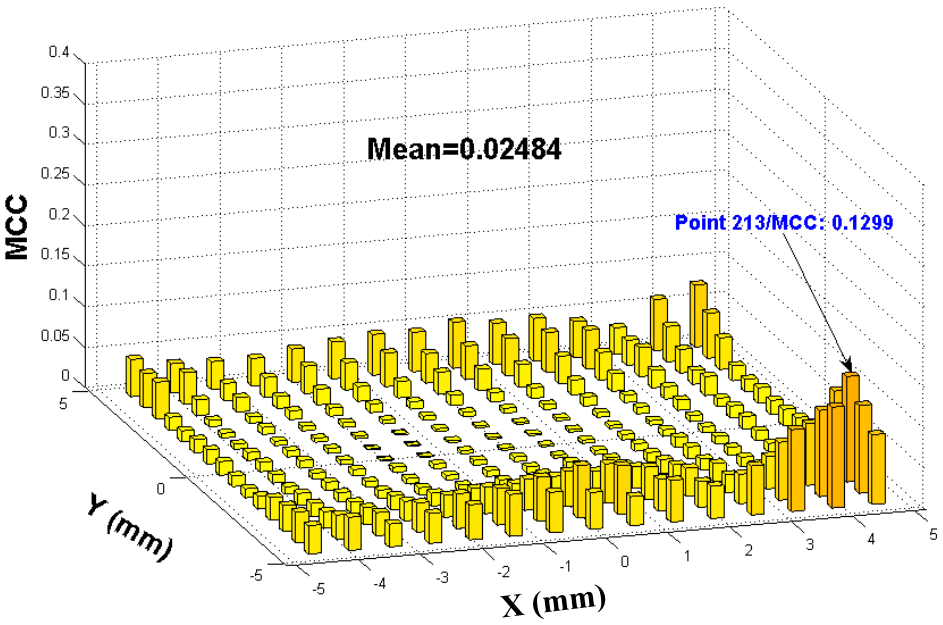


Figure 124 – LUI results from MCC analysis between FU3 and RU2 (Type – B samples) on die shadow DCPs

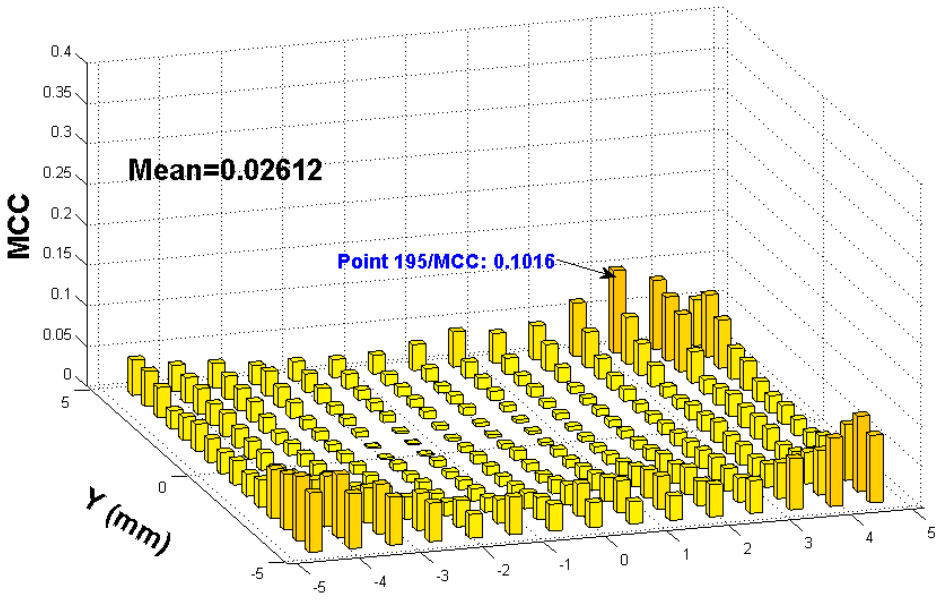


Figure 125 – LUI results from MCC analysis between FU4 and RU2 (Type – B samples) on die shadow DCPs

Damage metrics were determined along the half diagonal solder balls in FEM simulations. It may be noted that the diagonal line is shown in Figure 115 with a red line on top of view of the package. For correlation studies, it is important to extract the MCC value (LUI results) on these diagonal solder balls. However, there are four such diagonals in a package. The trend of MCC values along these four diagonals is similar but not perfectly same. Hence, MCC values on these four diagonals are averaged for correlation studies with the damage metrics from FEM simulations.

There are three Type – A samples that underwent 2929 thermal cycles, and two Type – B samples that underwent 1293 thermal cycles as listed in Table 13. As shown in Figure 109 and Figure 112, the three Type – A samples with 2929 thermal cycles have very similar LUI results. Similarly, the two Type – B samples with 1293 thermal cycles have very similar LUI results as shown in Figure 124 and Figure 125. Hence, averaged diagonal MCC values for each of these samples were averaged to obtain three sets of MCC values along the diagonal solder balls for 2036 thermal cycles, 2929 thermal cycles, and 1293 thermal cycles as shown in Figure 126. It may be noted that MCC values are not available on solder balls #8 and #13 for Type – A samples, and from solder balls #9 to #13 for Type – B samples as there are no DCPs at those locations for selected inspection patterns. These three curves are used to generate correlation equations with the damage metric curves in Figure 123.

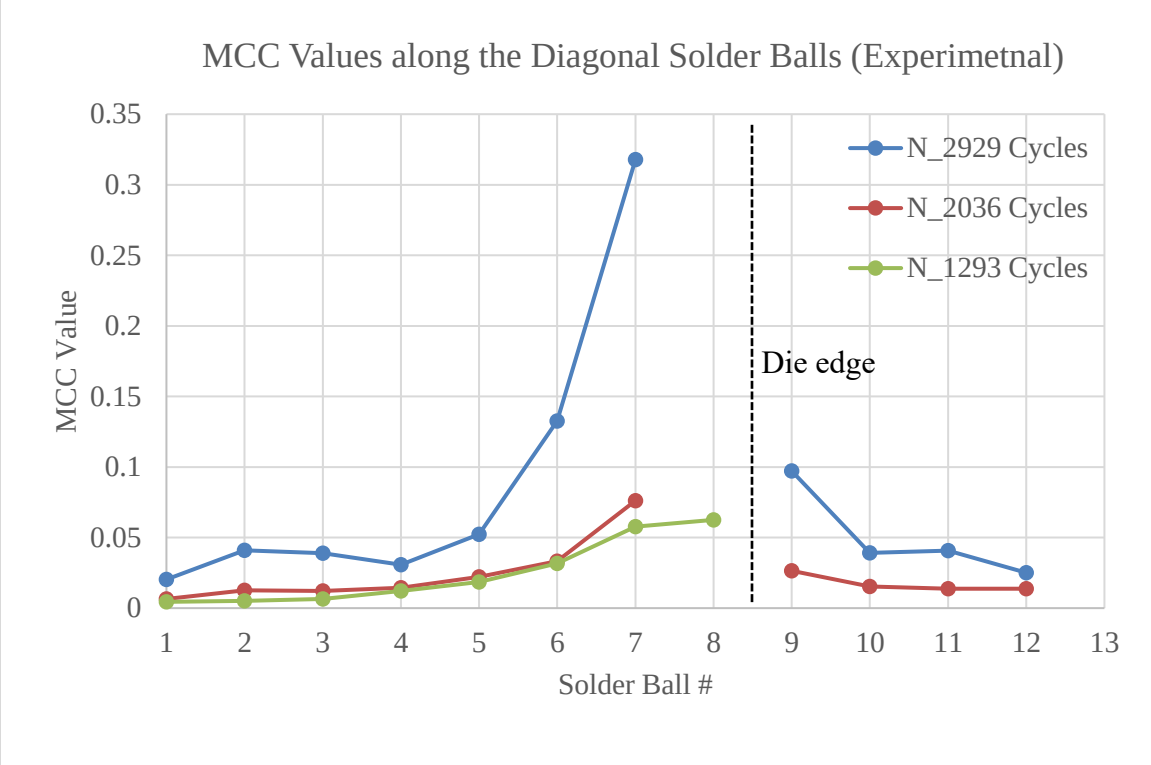


Figure 126 – Experimental LUI Results (MCC values) along the diagonal solder balls for different thermal cycles

8.4 Correlation Studies

Based on the experimental results in Figure 126 and finite-element simulation results in Figure 123, correlation equations are formulated to predict the MCC values based on damage metrics and vice-versa. Based on the trend of experimental results and finite-element simulation results, it is observed that MCC values have an exponential relationship with damage metrics and higher (power) order relationship with number of thermal cycles. For example, Figure 127 shows the variation of MCC values on solder ball #7 with number of thermal cycles, which indicates MCC values are some power of number of thermal cycles.

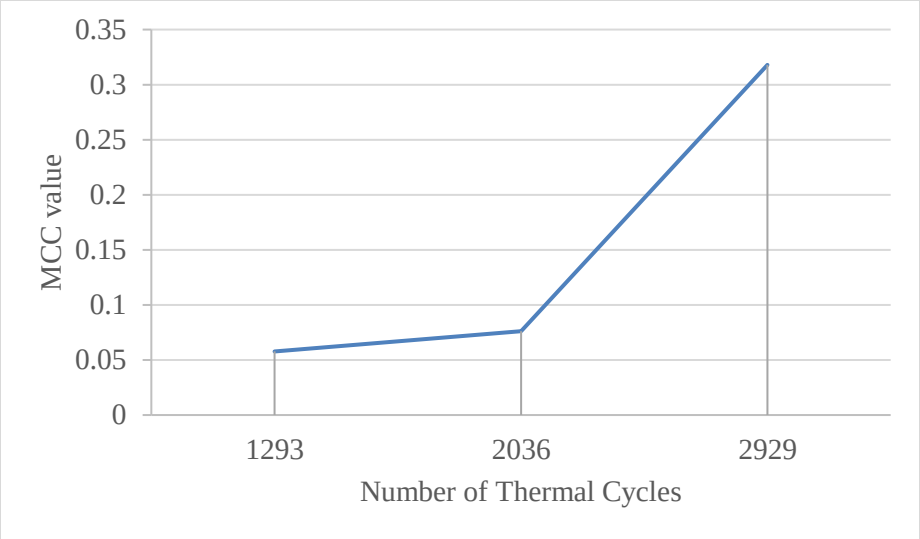


Figure 127 – Variation of MCC values on solder ball #7 with number of thermal cycles

JMP Pro 15® was used to generate a correlation equation for MCC values in terms of damage metrics and number of thermal cycles. Best fit equations are in the form given in Equation (11) for the relation between MCC and accumulated inelastic work density/cycle and Equation (12) for the relation between MCC and accumulated inelastic strain/cycle. Coefficients were calculated with JMP Pro with an R-squared variance of more than 85% and listed in Table 14. Finally, the predicted MCC values are plotted along with experimental MCC values in Figure 128 based on Equation (11) and Figure 129 based on Equation (12). Both equations predicted almost the same MCC values at each of the solder balls.

Correlation Equation with Accumulated Inelastic Work Density/Cycle:

$$MCC = a_0 \cdot N^{a_1} \cdot \exp\left(a_2 \Delta W_{acc}\right) \quad (11)$$

Correlation Equation with Accumulated Inelastic Strain/Cycle:

$$MCC = b_0 \cdot N^{b_1} \cdot \exp\left(b_2 \Delta \varepsilon_{acc}^{in}\right) \quad (12)$$

Table 14 – Coefficients in correlation equations

Coefficients in Equation (11)	Coefficients in Equation (12)
a_0 = 2E-19	b_0 = 2.284E-20
a_1 = 2.868	b_1 = 2.838
a_2 = 76.355	b_2 = 1589.608

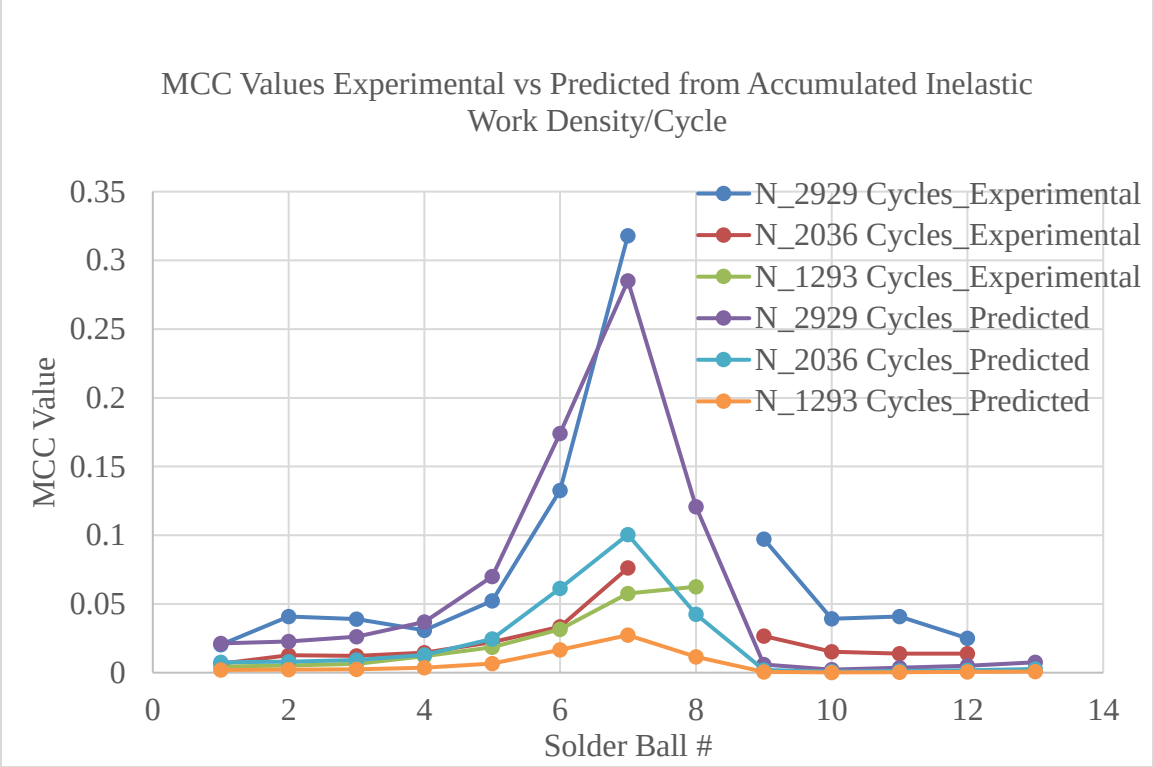


Figure 128 – Experimental and predicted MCC values from accumulated inelastic work density/cycle

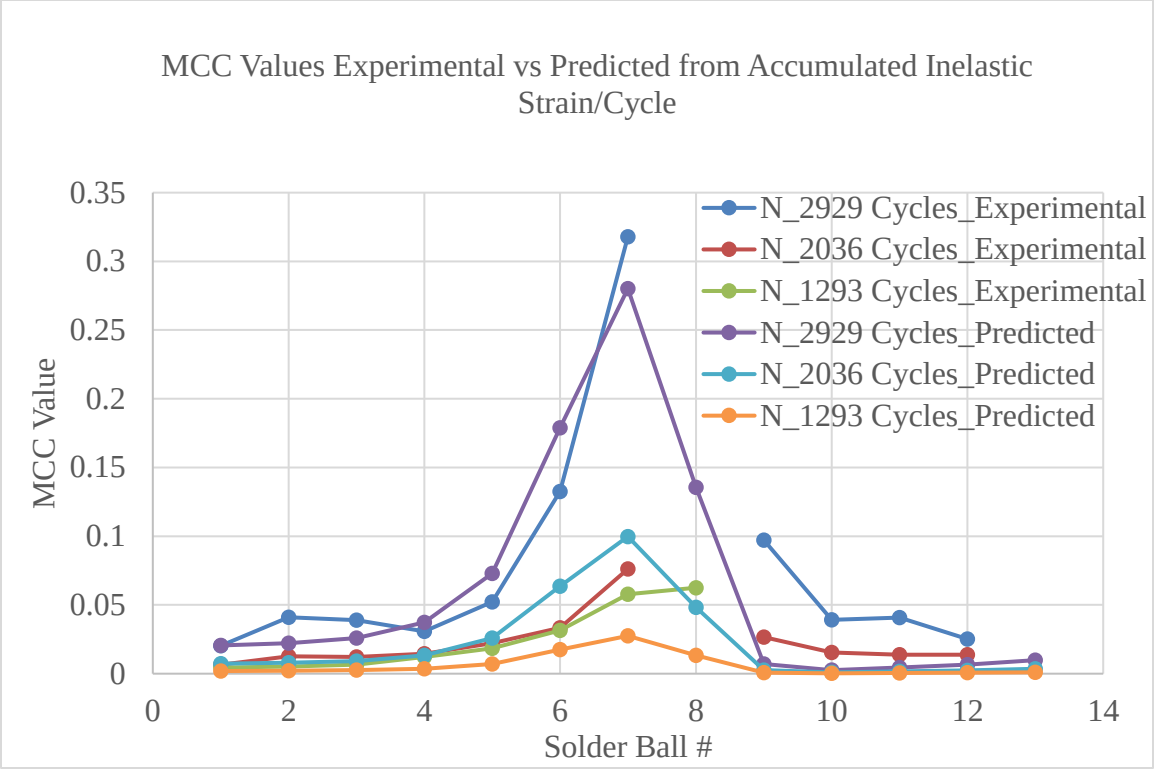


Figure 129 – Experimental and predicted MCC values from accumulated inelastic strain/cycle

8.5 Summary

This chapter mainly focused on establishing correlation equations for LUI results (MCC values) in terms of number of thermal cycles and damage metrics from finite-element simulations. Accumulated inelastic work density/cycle and accumulated inelastic strain/cycle were used as damage metrics in this study. The advantage of these correlation equations is that MCC values or number of thermal cycles the sample underwent can be predicted based on correlation equations. Further, the life of the packages can be predicted more accurately by measuring MCC values at a fewer number of thermal cycles. In the future, experimental studies shall be conducted to establish a strong correlation between

MCC values and severity of the failures at a given number of thermal cycles, instead of theoretical damage metrics from finite-element simulations.

These studies also help in supporting experimental results presented in CHAPTER 7. From finite-element simulations, inelastic work density and inelastic strain found to be maximum on the last two solder balls from the die edge under the die shadow. From experimental LUI results, MCC values also found to be maximum at the corner solder balls under the die shadow. This is the location of the largest CTE mismatch in the FCBGA assembly, hence, the results are validated.

CHAPTER 9. GAGE REPEATABILITY AND REPRODUCIBILITY ANALYSIS

The success of any metrology system depends upon precise and accurate data. DALUS data contains a certain percentage of variation and uncertainty due to manufacturing variations, sample surface conditions, signal noise, environmental variations, etc. It is important to determine the amount of acceptable variation to check the measurement capability of DALUS in the microelectronic packaging industry. Gage Repeatability and Reproducibility (GRR) is an effective tool to evaluate the amount of variation in the measurement data due to the measurement system and defining the capability of the measurement system [69]. Thus, the GRR study was conducted for evaluating the capability of DALUS. GRR studies will also help in choosing a reference sample for MCC analysis.

9.1 Test Vehicles and Inspection Procedure

Type – B 17 x 17 FCBGA samples supplied by Texas Instruments are used for GRR studies. As discussed in section 7.1, Type – B samples are very similar to Type – A samples except that Type – B samples have a full area-array BGA solder ball footprint as shown in Figure 130. In type – B samples, BGA solder ball layout is a 25 x 25 full area-array with 15 x 15 array of BGA solder balls at the center are under the die shadow (red dashed line in Figure 130). Like the Type – A samples, Type – B samples also have a heat sink (metal plate) which was removed for LUI experiments. Physical appearance and dimensions of Type – B samples are very similar to Type – A samples as shown in Figure 99. However,

in Type – B samples, underfill spread around the die extended almost till the edge of the BGA substrate. So, it is not possible to acquire a clean interferometer signal from the top of the BGA substrate. Hence, interferometer displacement data was taken from the top of die only. Unlike Type – A sample inspection pattern (describe in section 7.3), for Type – B samples, DCPs were chosen at every BGA solder ball location under the die shadow, totaling to 225 DCPs.

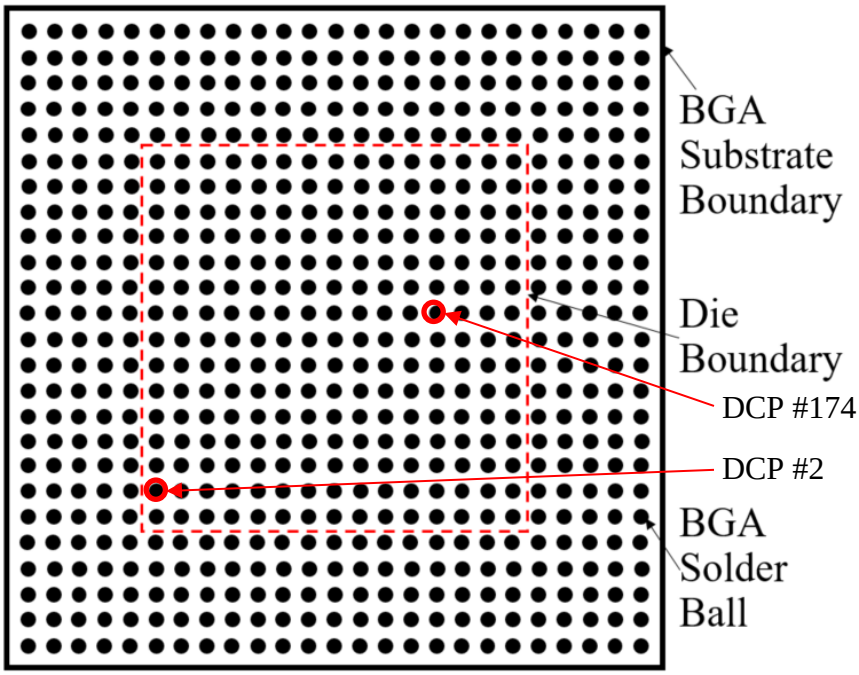


Figure 130 – BGA solder ball footprint of Type – B 17 x 17 FCBGA test vehicles

9.2 GRR Methodology

GRR studies assess repeatability and reproducibility of the measurements on a measuring system, in this case, DALUS. “Repeatability is the variation observed when an operator measures the same sample with the measurement system (with same system parameters) several times and reproducibility is the additional variation observed when

several operators use the same measurement system to measure the same sample" [69]. In this work, the same sample was taken out and re-positioned to make repeated measurements. However, for reproducibility analysis, the operator has no role to play in the measurements as DALUS is an automated system. Apart from the operator variation, it is common practice to consider the variation of measurements on different days, environmental variations, etc. Because LUI is a comparison technique, it is more appropriate to consider sample-to-sample variation for the reproducibility. Therefore, it was decided to analyze the variation when DALUS measures the same sample several times for repeatability analysis and to analyze the variation of measurement between different samples for reproducibility analysis.

JMP Pro 15® software, module Gauge R & R [70], was used for statistical evaluation for the measurement capability of DALUS. GRR or Precision of DALUS is defined as the overall standard deviation of the system (σ_t) which is square root of the sum of the repeatability variance (σ_{rpt}^2) and the reproducibility variance (σ_{rpd}^2) as given in Equation (13).

$$\sigma_t{}^2 = \sigma_{rpt}{}^2 + \sigma_{rpd}{}^2 \tag{13}$$

The measurement capability of a system can be represented by either Precision-to-Tolerance (P/T) ratio or process capability index (Cp). Process capability is defined by comparing the 6σ interval of a statistically stable process to the specification range or tolerance [69]. Cp is given by Equation (14). 6σ interval is selected because any measurement on microelectronic packages requires high precision. 6σ interval contains 99.7% of theoretical distribution.

$$C_p = \frac{USL - LSL}{6\sigma_t} \tag{14}$$

Where USL is Upper Specification Limit
LSL is Lower Specification Limit

Another Measurement Capability Index (MCI) is P/T ratio, given by Equation (15). The P/T ratio expresses the percentage of the specification window that is lost to the measurement error. P/T ratio is used as the MCI in this work.

$$P/T = \frac{6\sigma_t}{USL - LSL} = \frac{1}{C_p} \tag{15}$$

A smaller P/T ratio or higher C_p is desirable to specify a good measurement system. Cp in Equation (14) or P/T ratio in Equation (15) is defined based on an assumption that the distribution of measurements (or data set) is centered. Indices for not-centered data set are defined in Equation (16).

$$C_p = min\left\{\frac{USL - \mu}{3\sigma_t}, \frac{\mu - LSL}{3\sigma_t}\right\};\ P/T = max\left\{\frac{3\sigma_t}{USL - \mu}, \frac{3\sigma_t}{\mu - LSL}\right\} \tag{16}$$

Where μ is the mean of data set

DALUS measurements are characterized by MCC values. As explained in section 2.2.3, MCC values will be close to zero when LUI analysis is performed between similar samples or between the different runs on the same sample. Therefore, the distribution of MCC values is always right-skewed towards zero when the LUI analysis is performed between similar samples or between different runs on the same sample. Representative right-skewed distribution of MCC values on a DCP, among 7 runs on one of the Type – B

17 x 17 FCBGA samples is shown in Figure 131. It may be noted that comparison among 7 runs of LUI experiments on a given sample will give ${}^{7}C_{2}$ = 21 MCC values at each DCP.

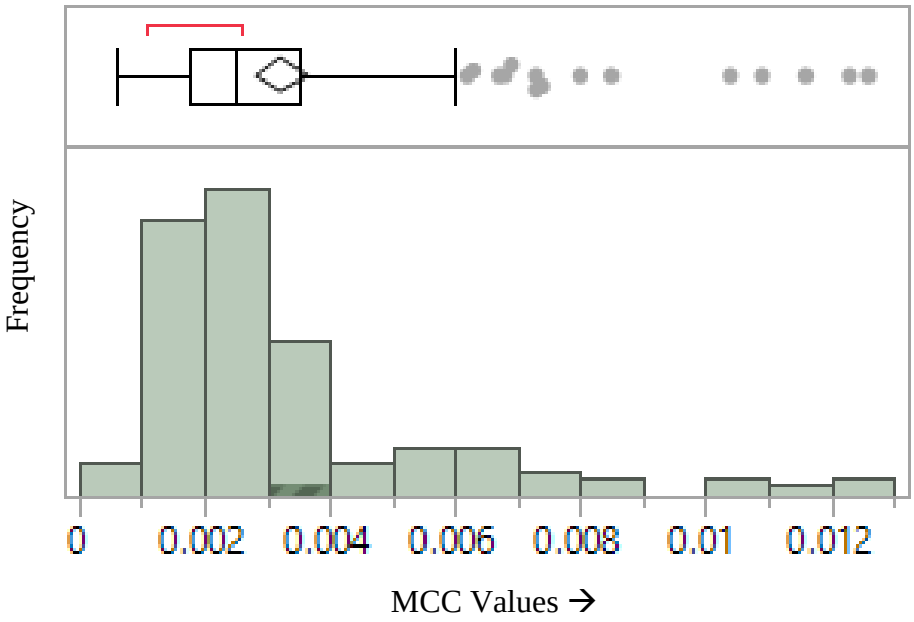


Figure 131 – Distribution of MCC values at a DCP among 7 runs on a Type – B 17 x 17 FCBGA sample

P/T ratio was used for the assessment of MCI in this research. For the right-skewed distribution of MCC values, P/T ratio is given by Equation (17).

$$P/T = \frac{3\sigma_t}{USL - \mu} \tag{17}$$

Where σ_t is the overall standard deviation of DALUS

μ is the mean of MCC values distribution

USL is Upper Specification Limit

9.3 Design of Experiments

Six time-zero pristine Type – B 17 x 17 FCBGA samples, labeled as RU2, RU3, RU4, RU5, RU7, and RU8, are selected for GRR studies. Seven runs of LUI experiments were carried out on each sample. MCC analysis was carried out among all seven runs to generate 21 MCC values at each DCP for each sample. Variation within these 21 MCC values for each of the 6 samples are used for repeatability analysis and to calculate repeatability standard deviation (σ_{rpt}). The variation between MCC values of one sample to the other sample is used for reproducibility analysis and to calculate reproducibility standard deviation (σ_{rpd}). From these, the overall standard deviation of the system (σ_t) from Equation (13) can be calculated.

From substantial LUI experiments performed on DALUS, the smallest defect or failure that can be identified by DALUS will have the lowest MCC value of 0.04. It may be noted the results of 52.5 x 52.5 FCBGA samples subjected to drop testing, with an MCC value of 0.04, DALUS could identify IMC cracks of 2µm vertical separation. Hence, empirical data suggest that no defect or failure is expected for MCC value below 0.04. As GRR studies were conducted on pristine time-zero samples, therefore, USL is considered as 0.04. Finally, P/T ratio can be calculated from Equation (17) to determine the measurement capability of DALUS. The guidelines for the measurement variation of a system, as suggested by Barrentine [69], are given in Table 15. As per microelectronic industry standards, any measurement system with measurement variation of $P/T \leq 30\%$ is acceptable.

Table 15 – Acceptance criteria for measurement variation of DALUS

P/T Ratio	Capability of the System
< 10%	Excellent
11% to 20%	Adequate
21% to 30%	Marginally acceptable
> 30%	Unacceptable

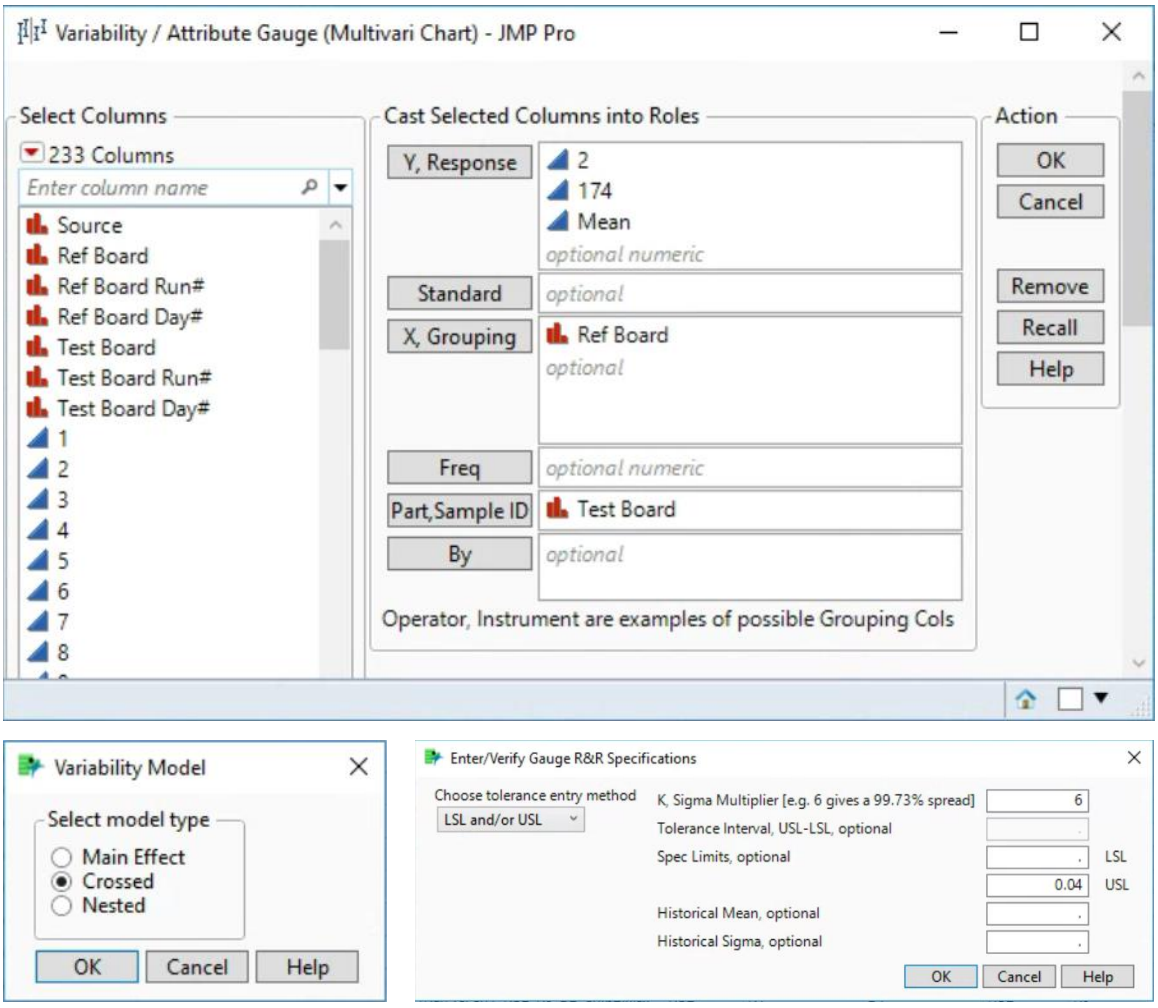


Figure 132 – JMP Pro screenshot showing the input parameters for GRR analysis of DALUS

Manual calculations for P/T ratio are tedious because of the large data. JMP Pro 15 has “Gauge R&R variability platform”, which is capable to do all the P/T ratio calculations according to Equation (17) and outputs detailed GRR report. The JMP screenshot for entering the input parameters to generate a GRR report is shown in Figure 132. In Figure 132, Y-Response is all MCC values at a DCP (With 7 runs each on 6 samples, total MCC values are 126 at one DCP). In this GRR methodology, X-Grouping and Part-Sample ID are interchangeable, which means the same result can be obtained by exchanging Ref Board and Test Board. The crossed variability model ensures repeatability analysis from seven runs on the same sample and reproducibility analysis form sample-to-sample variation. There is a provision to enter sigma multiplier (6σ) and LSL and/or USL individually for every Y-Response as shown in Figure 132.

9.4 Results and Discussions

Before performing GRR studies, LUI experiments were carried out on 6 samples for 7 runs on each. Signal analysis among the 7 runs (comparing signals between one run to other) was carried out using Equation (1) to calculate MCC values at all 225 DCPs. The representative LUI results from MCC analysis between Run1 and Run2 on the RU8 sample are plotted in the form of a 3D histogram, as shown in Figure 133, with MCC value on the z-axis and location of DCP on the XY plane. For this set of LUI results, the maximum MCC value is 0.0052 on DCP #179, and the mean of MCC values on all 225 DCPs is 0.00103 as shown in Figure 133.

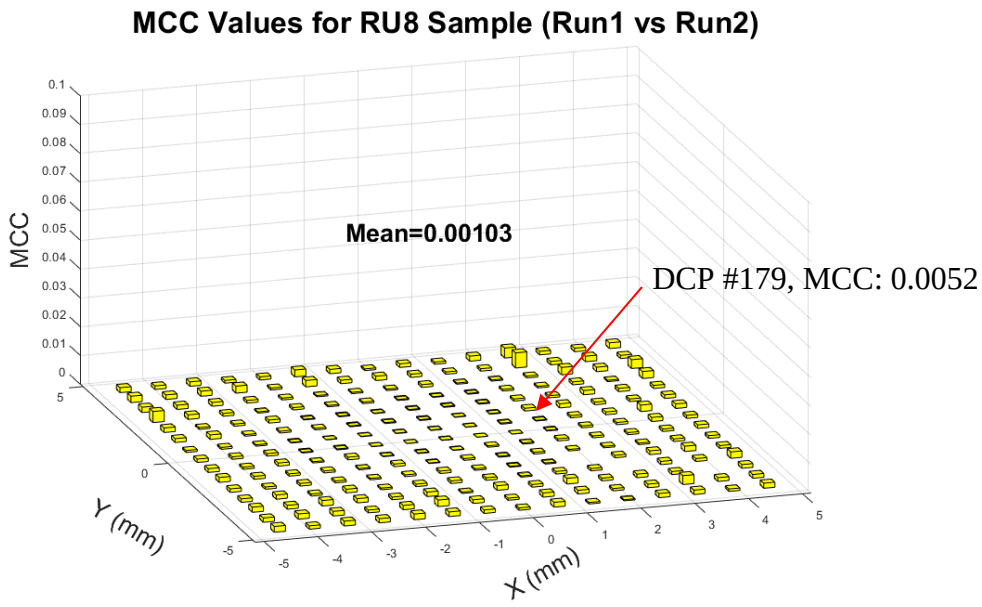
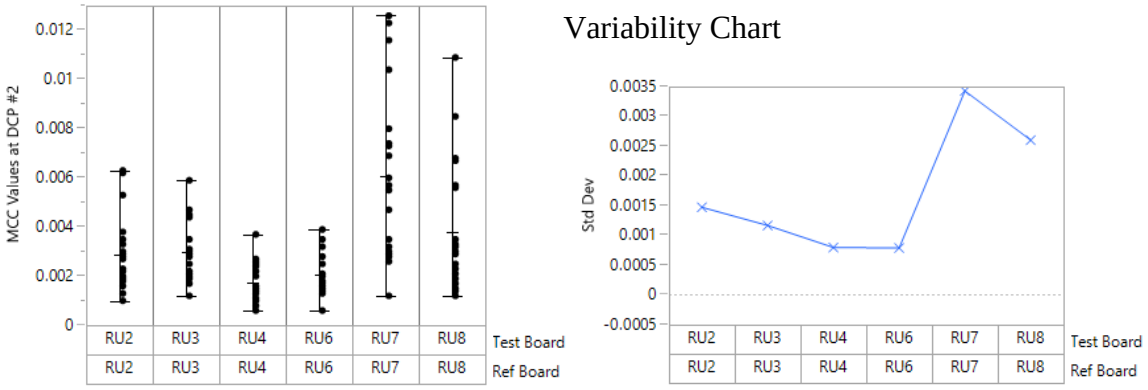


Figure 133 – Sample LUI results from MCC analysis between Run1 and Run2 on RU8 sample

GRR analysis was performed from the MCC values on all 225 DCPs individually and with the mean of these 225 MCC values. For example, one set of MCC values on 225 DCPs in the form of a 3D histogram and the mean of 225 MCC values (= 0.00103) are shown in Figure 133. GRR results on DCP #2, DCP #174, and with the mean of 225 MCC values are presented here for discussion. Locations of DCP #2 and DCP #174 are shown in Figure 130. DCP #2 is selected because it has the highest P/T ratio. P/T ratio on DCP #174 is on the lower side.

The GRR report, generated by JMP Pro, with MCC values on DCP# 2 is shown in Figure 134. From the variability chart, the maximum MCC value is about 0.012 on DCP #2 from the runs on the RU7 sample. Also, the maximum standard deviation of 0.0035 is from LUI experimental runs on RU7. Samples RU7 and RU8 have a relatively high variance when compared to other samples. However, this variance is well below acceptable

limits. P/T ratio (shown with the red arrow in Figure 134) on DCP #2 is 20.25%. It may be noted that DCP #2 has the highest P/T ratio among all DCPs. P/T ratio on DCP #2 is just above 20%, hence, the measurement variation is adequate according to Table 15.



Gauge R&R

Measurement Source		Variation (3*StdDev)	% of Tolerance		which is 3*sqrt of
Repeatability	(EV)	0.00591630	16.09	Equipment Variation	V(Within)
Reproducibility	(AV)	0.00451811	12.29	Appraiser Variation	V(Ref Board) + V(Ref Board*Test Board)
Ref Board		0.00451811	12.29		V(Ref Board)
Ref Board*Test Board		0.00000000	0.00		V(Ref Board*Test Board)
Gauge R&R	(RR)	0.00744419	20.25	Measurement Variation	V(Within) + V(Ref Board) + V(Ref Board*Test Board)
Part Variation	(PV)	0.00000000	0.00	Part Variation	V(Test Board)
Total Variation	(TV)	0.00744419	20.25	Total Variation	V(Within) + V(Ref Board) + V(Ref Board*Test Board) + V(Test Board)

3	k
100	% Gauge R&R = 100*(RR/TV)
0	Precision to Part Variation = RR/PV
0	Number of Distinct Categories = 1.41(PV/RR)
0.04	USL
0.00324	Grand Mean
0.03676	Tolerance = USL - Grand Mean
0.20251	Precision/Tolerance Ratio = RR/(Tolerance)

Using last column 'Test Board' for Part.

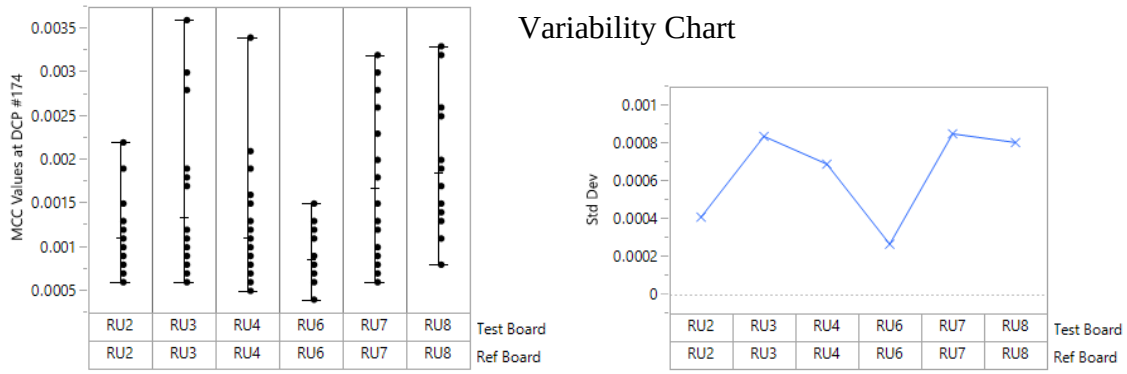
Variance Components for Gauge R&R

Component	Var Component	% of Total	20 40 60 80
Gauge R&R	6.15733e-6	100.0	
Repeatability	3.88918e-6	63.2	
Reproducibility	2.26815e-6	36.8	
Part-to-Part	0	0.0	

Figure 134 – JMP GRR Report with MCC values on DCP #2

The GRR report, generated by JMP Pro, with MCC values on DCP #174 is shown in Figure 135. From the variability chart, measurement variation is low. P/T ratio (shown

with the red arrow in Figure 135) on DCP #174 is 5.86%, which is below 10%. Hence, the measurement variation for DCP #174 is excellent according to Table 15.



Gauge R&R

Measurement Source		Variation (3*StdDev)	% of Tolerance		which is 3*sqrt of
Repeatability	(EV)	0.00202540	5.23	Equipment Variation	V(Within)
Reproducibility	(AV)	0.00102286	2.64	Appraiser Variation	V(Ref Board) + V(Ref Board*Test Board)
Ref Board		0.00102286	2.64		V(Ref Board)
Ref Board*Test Board		0.00000000	0.00		V(Ref Board*Test Board)
Gauge R&R	(RR)	0.00226903	5.86	Measurement Variation	V(Within) + V(Ref Board) + V(Ref Board*Test Board)
Part Variation	(PV)	0.00000000	0.00	Part Variation	V(Test Board)
Total Variation	(TV)	0.00226903	5.86	Total Variation	V(Within) + V(Ref Board) + V(Ref Board*Test Board) + V(Test Board)

3	k
100	% Gauge R&R = 100*(RR/TV)
0	Precision to Part Variation = RR/PV
0	Number of Distinct Categories = 1.41(PV/RR)
0.04	USL
0.00131	Grand Mean
0.0387	Tolerance = USL - Grand Mean
0.05864	Precision/Tolerance Ratio = RR/(Tolerance)

Using last column 'Test Board' for Part.

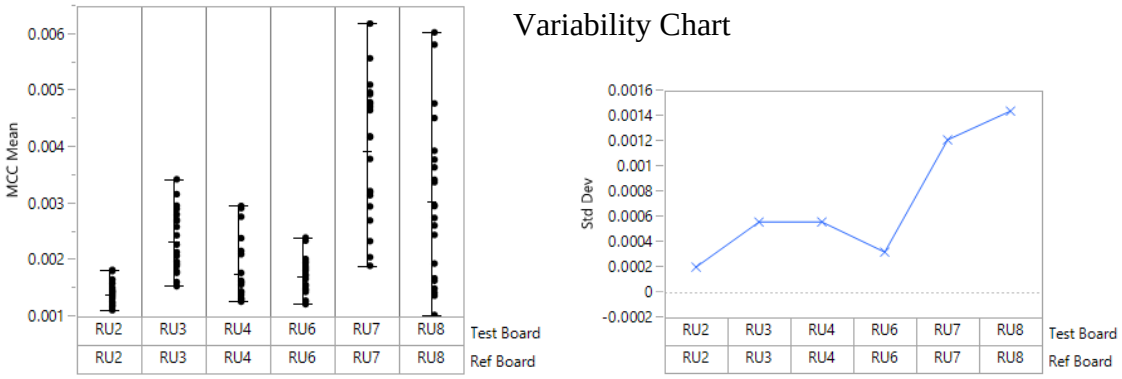
Variance Components for Gauge R&R

Component	Var Component	% of Total	20 40 60 80
Gauge R&R	5.72055e-7	100.0	
Repeatability	4.55806e-7	79.7	
Reproducibility	1.16248e-7	20.3	
Part-to-Part	0	0.0	

Figure 135 – JMP GRR Report with MCC values on DCP #174

The GRR report with mean MCC values from all 225 DCPs is shown in Figure 136. It may be noted that every MCC analysis between any two runs will have one mean value form 225 MCC values from all DCPs. The mean value is a good indicator to represent

measurement variation on all 225 DCPs. From the variability chart, measurement variation is relatively high in RU7 and RU8 samples when compared with other samples. But the variation is very low and within acceptable limits. P/T ratio (shown with the red arrow in Figure 136) is 10.09%, which is just above 10%. Hence, the measurement variation with mean MCC values is excellent. Overall, the highest P/T ratio on DCP #2 is about 20%, which shows that DALUS measurement variation is adequate.



Gauge R&R

Measurement Source		Variation (3*StdDev)	% of Tolerance		which is 3*sqrt of
Repeatability	(EV)	0.00254060	6.75	Equipment Variation	V(Within)
Reproducibility	(AV)	0.00282209	7.50	Appraiser Variation	V(Ref Board) + V(Ref Board*Test Board)
Ref Board		0.00282209	7.50		V(Ref Board)
Ref Board*Test Board		0.00000000	0.00		V(Ref Board*Test Board)
Gauge R&R	(RR)	0.00379721	10.09	Measurement Variation	V(Within) + V(Ref Board) + V(Ref Board*Test Board)
Part Variation	(PV)	0.00000000	0.00	Part Variation	V(Test Board)
Total Variation	(TV)	0.00379721	10.09	Total Variation	V(Within) + V(Ref Board) + V(Ref Board*Test Board) + V(Test Board)

3 k
100 % Gauge R&R = 100*(RR/TV)
0 Precision to Part Variation = RR/PV
0 Number of Distinct Categories = 1.41(PV/RR)
0.04 USL
0.00236 Grand Mean
0.03764 Tolerance = USL - Grand Mean
0.10088 Precision/Tolerance Ratio = RR/(Tolerance)

Using last column 'Test Board' for Part.

Variance Components for Gauge R&R

Component	Var Component	% of Total	20 40 60 80
Gauge R&R	1.60209e-6	100.0	
Repeatability	7.17181e-7	44.8	
Reproducibility	8.84909e-7	55.2	
Part-to-Part	0	0.0	

Figure 136 – JMP GRR Report with Mean of MCC values on 225 DCPs

9.5 Summary

GRR studies provide an opportunity to improve the process and reduce variation. GRR analysis was carried out on DALUS using six Type – B 17 x 17 FCBGA samples. Seven runs of LUI experiments were conducted on each sample and MCC was calculated by signal analysis between different runs of the same sample. JMP Pro crossed variability model was used for repeatability analysis from seven runs on the same sample and reproducibility analysis form sample-to-sample variation. P/T ratio was used as a measurement capability index in this research. P/T ratio was taken directly from JMP Pro reports for GRR analysis.

The maximum P/T ratio was observed to be 20.25% on DCP #2. P/T ratio with the mean of MCC values on 225 DCPs was 10.09%. With this P/T ratio of about 20%, the measurement variation is adequate. Also, DALUS is a lab-scale research prototype. It is possible to build a high precision DALUS in an industrial environment, in which measurement variation below 10% is possible. This establishes that DALUS is capable of repeatable and reproducible measurements and to identify the failures in microelectronic packages precisely. Additionally, RU7 and RU8 have relatively high variation when compared with other samples. Therefore, any of the four samples, RU2, RU3, RU4, and RU6, can safely be used as reference samples for MCC analysis of Type – B 17 x 17 FCBGA test samples.

CHAPTER 10. CONCLUSIONS, RESEARCH CONTRIBUTIONS AND FUTURE WORK

An enhanced Dual-Fiber Array Laser Ultrasonic System (DALUS) was developed to inspect a broad range of first-level and second-level solder joint defects and failures in a variety of microelectronic packages. The performance of this system has been improved through hardware upgrades and software improvements, making it a versatile, state-of-the-art non-destructive, automated, non-contact, accurate, fast, precise, cost-efficient, and high-resolution inspection equipment for advanced industrial microelectronic packages. DALUS hardware and software can be customized to meet the specific needs of the individual customer. The fully developed system can be used on-line as a go/no-go quality evaluation tool, and off-line for failure analysis or process development. With DALUS, microelectronic packaging manufacturers will benefit from reduced product development cycle time, optimized new product development, and improved results of sub-micron defect detection.

In this research, quality inspection and reliability study of second-level solder interconnections in two types of FCBGA packages have been successfully investigated using LUI technique, destructive techniques, and finite-element simulations. The experimental and simulation results have been validated and led to a better understanding of the underlying physics of the LUI technique applied to electronic packaging. DALUS, currently a lab-scale prototype, provided accurate information in defect locations and defect severity.

10.1 Conclusions

- A new Dual-Fiber Array Laser Ultrasonic System (DALUS) was developed by introducing a multiplexer to split the laser beam into two, replacing 600µm optical fiber with two 1000µm optical fibers along with two new adjustable end effectors, and rotational stages, to deliver laser beam at two incident spots. The complete system was assembled, re-positioned, and calibrated as per the standard lab procedures. Now, this new system can deliver high laser power to the microelectronic package to generate stronger ultrasonic vibrations, with low energy density to not to cause any damage to the package. Therefore, DALUS can now inspect large packages, packages with high solder density, and packages with sub-micron defects/failures, etc.
- Additional safety features were introduced to prevent the possible collision of end effectors and interferometer head. A safety system, using Hall Effect sensors to detect the proximity of magnets mounted on the end effectors, was developed and implemented. This additional safety system for collision prevention is of the utmost importance, as the impact from a collision results in damage to the expensive interferometer head, and disruption in system calibration and system settings. Any collision or near-collision will lead to multiple hours of system downtime while damage is assessed, and calibration is performed.
- The technical capabilities of the system were evaluated. First and foremost, high laser power from DALUS is verified to be not damaging the incident surface of the package. Hardware and software of DALUS have been fine-tuned to achieve a 4-fold increase in laser power, a 3-fold increase in ultrasound signal strength, and an

8-fold increase in SNR when compared with Single Laser Ultrasonic System (SLUS).

- DALUS and the system settings were optimized thoroughly to achieve the sensitivity to identify IMC failures of the size 2μm vertical separation and horizontal separation of more than 20% of the solder joint width. The throughput of DALUS was also improved. It will take about an average of 15sec to collect the data from a DCP and analyze the failure/defect result. Especially, DALUS overall throughput is high for large and complex microelectronic packages when compared with SLUS.
- DALUS was employed to evaluate the quality of solder interconnections in various FCBGA microelectronic packages subjected to drop testing, thermal-cycling test, and mechanical bend testing. As these tests produce different sizes and nature of cracks at various locations within the solder interconnects, the utility of DALUS for various types of failures/defects in advanced microelectronic packages was demonstrated successfully. The results from DALUS were validated using standard destructive tests (such as cross-sectioning along with microscopy, and dye-and-pry) and finite-element simulations.
- Many LUI experiments were conducted on various types of area-array microelectronic packages to determine the threshold MCC values based on the type of package and reliability test condition. The threshold MCC value is a value above which failures are seen in the BGA solder balls in FCBGA packages. Form the empirical data, threshold MCC value for four-point bend testing or thermal cycling

samples is 0.1, and for drop testing samples is 0.04. MCC values are proportional to the severity of the failures.

- Correlation equations, MCC in terms of the number of thermal cycles and damage metrics from finite-element simulations, have been developed. Accumulated inelastic strain per thermal cycle and accumulated inelastic work density per thermal cycle were used as damage metrics from finite-element simulations. To extract damage metrics, the finite-element model was developed to study thermal cycling reliability in FCBGA packages with the viscoplastic constitutive law. With these correlation equations, MCC values can be predicted from the number of thermal cycles in thermal cycling test and/or from the accumulated inelastic strain per cycle and/or from accumulated inelastic work density per cycle in finite-element simulations. Also, based on MCC values, the number of thermal cycles the sample underwent and accumulated inelastic strain per cycle and/or accumulated inelastic work density per cycle in the solder joints can be estimated. The finite-element simulations also reveal that corner solder ball under the die shadow are the most critical ones under thermal cycling loading and would fail first since they always experience the highest inelastic strain and inelastic strain energy density.
- To demonstrate DALUS measurement capability in the semiconductor manufacturing industry, GRR studies were conducted. GRR is an effective tool to evaluate the amount of variation in the measurement data due to the measurement system to define the precision and capability of the measurement system. From GRR studies, the maximum P/T ratio was observed to be 20.25%, which supports that DALUS is capable of repeatable and reproducible measurements to identify

the defects/failures in microelectronic packages. GRR studies were also useful to identify the reference sample to be used as a golden standard for signal analysis purposes. Based on the variation of MCC values on different time-zero samples, the reference sample(s) can be selected with the least variation in GRR studies.

10.2 Research Contributions

The research contributions from this work are as follows:

- A new DALUS, capable of identifying defects and failures in large and multilayer area-array microelectronic packages, was developed. It is a significant forward of previous SLUS, and it opened a path to improve the LUI technique to have high sensitivity by using more than one laser beam.
- This is the first time that the LUI technique was applied to identify defects/failures in real-world industrial FCBGA packages subjected to various accelerated life testing, thermal cycling, four-point bend testing, and drop testing.
- A proportionality correlation was established between the severity of the failures and MCC values. Now, the severity of the failures and defects can be assessed based on MCC values without destroying the samples.
- For the first time, LUI experimental data were correlated with finite-element modeling results. Correlation equations allowed predicting MCC values even before performing LUI experiments and predict the fatigue life of microelectronic packages more accurately.
- The viability of DALUS in the microelectronic manufacturing industry was demonstrated using gage repeatability and reproducibility studies. It is very

important for the microelectronic manufacturing industry that any inspection system should measure or identify the defects/failures with high precision and accuracy.

10.3 Future Work

The development of DALUS from this research opened many new avenues of investigation. Some potential areas for future research are presented in this section.

10.3.1 Multiple Fiber Array Laser Ultrasonic System

DALUS is a significant forward of the previous SLUS. DALUS allows higher total energy to be delivered onto the microelectronic package under inspection. The higher laser energy produces high-strength ultrasound waves in the sample, which will improve the sensitivity of the system as well as facilitate the inspection of large and multi-leveled packages. To improve the sensitivity further and to inspect the more complex packages such as 2.5D and 3D packages, more than two fiber array laser beams shall be developed. An illustration of the three-fiber array laser ultrasonic system is shown in Figure 137. So far, DALUS has not shown limitations in inspecting complex FCBGA packages to detect IMC cracks of 2µm vertical separation. If the intended sensitivity is to identify failures below 2µm vertical separations, it is worth developing multiple fiber array laser ultrasonic system.

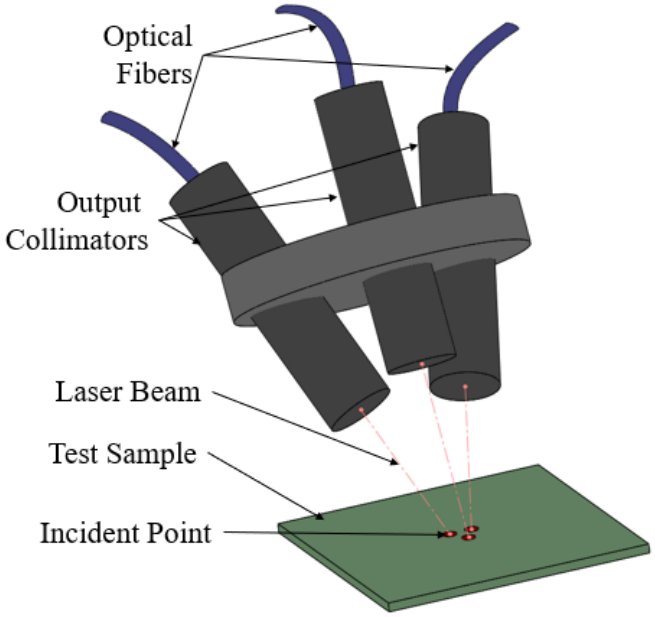


Figure 137 – Illustration of three-fiber array laser ultrasonic system

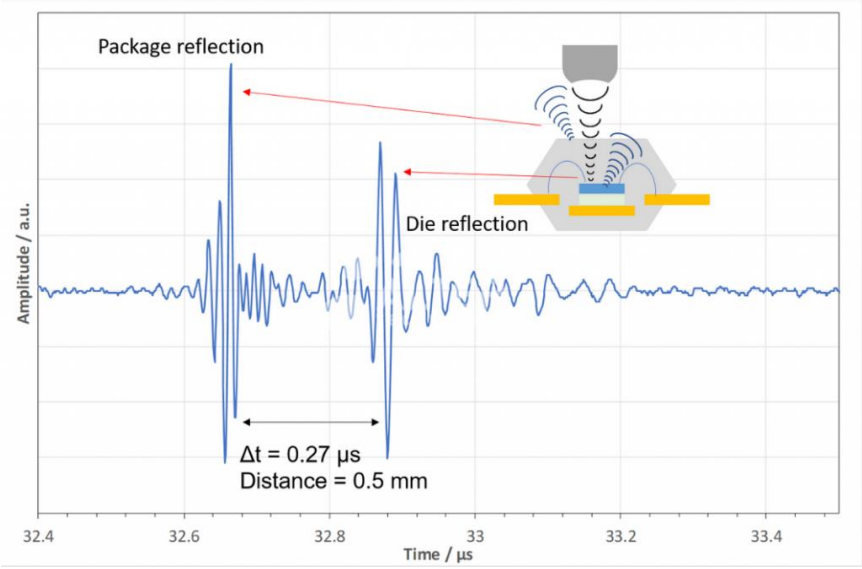
10.3.2 Signal Feature Extraction for Failure Mode Classification and Z-Location of the Failure

The main limitation of DALUS is that it cannot provide the failure mode information. The system can identify the failure XY location and the severity of the failure accurately. However, information related to the type of failure (IMC cracks, pad cratering, solder fracture, etc.) or type of defect (head-in-pillow, voids, open joints, etc.) and Z-location of the failure/defect is not available. Z-location is important in multi-level packages to distinguish the failures/defects from first-level interconnections and second-level interconnections.

Currently, signal processing mainly focusses on failure/defect detection and only a very limited set of signal features is exacted for this purpose. In MCC analysis, a linear

correlation of signals in frequency-domain is extracted. For failure mode classification, signal features in the frequency-domain shall be examined more closely. Previous researchers observed a decrease of certain natural frequencies caused by solder ball crack. However, a decrease of certain natural frequencies can also be related to other failure modes, such as pad cratering. Therefore, more signal features such as frequency shift, need to be extracted to classify the failure modes. In addition, machine learning techniques can be adopted to build a classification system when there is a large amount of data.

The MCC value at a DCP measures the cumulative failures/defects in the thickness direction at a given XY location. To estimate the exact Z-location of the failures, gate concept in the time-domain signals, like in the SAM technique, can be employed. An example of time-domain signals to locate the Z-height using a gate in the SAM technique is shown in Figure 138. A similar gate concept in interferometer signals either in the time-domain or frequency-domain might reveal the Z-location of failures/defects.



Ref: Alter Technology

Figure 138 – Sample time-domain signal to identify the Z-height in SAM technique

10.3.3 Expansion of Application Scope

So far, SLUS successfully demonstrated its capability to detect obvious failures in flip-chip packages, CSPs, LGA packages, MLCCs, and PBGA packages. In this research, DALUS was demonstrated to identify a variety of failures in second-level BGA solder interconnections of FCBGA packages. However, DALUS has not been tested to its potential. The application scope of DALUS can be expanded to other advanced packages such as SiP, PoP, 2.5D, and 3D. DALUS application shall be expanded to underfill delamination and void detection. Identification of defects/failures other than in solder ball interconnections such as cracks in Via (the inner connection between first-level interconnections and second-level interconnections) can be explored using DALUS.

One another possible application is crack detection in silicon wafers, and it is very attractive research and application area. Since silicon wafer (8 or 12 inches) is much larger than current small-size flip-chip packages, the wave propagation principle can be applied to interpret captured responses and detect cracks within wafers. The characterization and integrity evaluation of MEMS devices is another possible application of DALUS.

10.3.4 Correlation Studies between MCC and Number of Thermal Cycles

In this research, the correlation was established between MCC and damage metrics from finite-element simulations. A more practical correlation can be established between experimental MCC values and number of thermal cycles. For this, a large set of samples shall be selected, and batch-wise thermal cycling should be conducted. LUI experiments shall be carried out on all possible samples for every ~100 thermal cycles. Experimental damage metrics shall be extracted from a set of samples from the batches by destructive

techniques. Large data will help in establishing a better correlation. From these correlations, MCC values can be predicted beforehand based on the test condition applied to the test samples. Using these correlations, the life of the samples can be predicted more accurately by subjecting the samples few hundreds of thermal cycles and measuring MCC values. Hence, the time and effort required for thermal cycling reliability testing can be reduced to a great extent.

10.3.5 Multiphysics Simulation of Laser-Generated Ultrasound

The solder ball locations are normally considered to collect the interferometer data/signal to evaluate the quality of that solder ball. However, if the test package has hundreds of solder balls, it will take a lot of time to complete the inspection. A down-sampling inspection pattern is necessary for the interest of throughput. The choice of the down-sampling inspection pattern is closely related to the inspection sensitivity. Certain inspection patterns are superior to others. Currently, the down-sampling inspection pattern is determined empirically. Multiphysics simulation can be adopted to provide some guidance to optimize the inspection pattern. The simulation can be carried out by numerical methods using the finite-element analysis. COMSOL Multiphysics® is a better-known software tool for this kind of simulation. Multiphysics simulation can bring huge robustness to the inspection system. By taking advantage of this model, the transient out-of-plane displacement responses can be predicted even before running actual tests. It is possible to change many variables in the model, including the laser energy, the location of laser excitation, inspection location, and the chip package to study the effects. The effects of multiple laser excitations can also be evaluated using the model. The optimization of the

laser excitation locations and interferometer DCPs can be achieved using the model, which will provide great guidance to the actual tests.

10.3.6 Inline Laser Ultrasonic Inspection

In this research, LUI experiments were conducted offline. Samples were received from Cisco and Texas Instruments, after accelerated life testing. However, it is possible to use DALUS for inline inspection in the assembly line. To test the viability of the system for inline inspection, it is recommended to mount DALUS above a conveyor to receive the samples and simulate an industrial assembly line. In industrial settings, with few data collection points, DALUS would take just a few seconds to complete the inspection of the assembled sample without impeding the speed of the assembly line. If the inspection is based on pass/fail criteria, 5 to 10 data collection points should be sufficient for DALUS to accept or reject package assemblies as they come out of the reflow oven. Extensive additional studies are required, however, to evaluate the viability of the developed DALUS for in-line assembly inspection.

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