ORGANIC THIN-FILM TRANSISTORS AND THEIR APPLICATION IN LIGHT DETECTION

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ORGANIC THIN-FILM TRANSISTORS AND THEIR APPLICATION IN LIGHT DETECTION

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μ	Charge mobility
V_{TH}	Threshold voltage
Ψ	Wave function
$\widehat{H}$	Hamiltonian operator
E	Energy eigenvalue
E_g	Energy gap between HOMO manifold and LUMO manifold
E_F	Fermi level energy
E_C	Energy of conduction band
E_V	Energy of valence band
ϕ_m	Work function
ϕ_{bn}	Energy barrier height of electron injection
ϕ_{bp}	Energy barrier height of hole injection
k_{ET}	Charge-transfer rate
$\hbar$	The reduced Planck constant
k_B	Boltzmann constant
V_{ij}	Electronic coupling matrix element
ΔG^0	The variation of the Gibbs free energy
λ	Reorganization energy
$E^{(A1)}(A^+)$	The energy of the neutral acceptor A at the cation geometry
$E^{(A1)}(A)$	The energy of the neutral acceptor A at the ground-state geometry
$E^{(D2)}(D)$	The energy of the radical cation D^+ at the neutral geometry
$E^{(D2)}(D^+)$	The energy of the radical cation D^+ at the ground-state geometry
D	Diffusion coefficient
L_c	The mean length of a charge traveled
v	The average velocity
L	Channel length
W	Channel width

I_{DS}	Drain to source current
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
κ	Dielectric constant
q_{ind}	Total charge density induced in the semiconductor per area
C_{ox}	Capacitance density of dielectric layer
$V(x)$	Surface potential at a distance x from the source in the channel of an OTFT
$q_{int,ave}$	Average value of the induced charge density
σ	Conductivity
t	Thickness of the charged layer in the channel
I_{off}	Off current
I_{on}	On current
S	Subthreshold slope
R_C	Contact resistance
R_{on}	On-state resistance
R_{ch}	Channel resistance
R_{sh}	Sheet resistance
I-V	Current-voltage
φ_s	Work function of the sample
φ_t	Work function of the reference tip
e	Elementary charge
V_{CPD}	Contact potential difference
N_{tr}	Trapped charge density
ΔV_{TH}	Threshold voltage shift
N_f	Free carrier density
τ	Characteristic time constant
τ_1	Characteristic time constant
τ_2	Characteristic time constant
β	Dispersion parameter

β_1	Dispersion parameter
β_2	Dispersion parameter
J-E	Current density-electric field
J_{SC}	Short-circuit current density of an OPD
V_{OC}	Open-circuit voltage of an OPD
I_{SC}	Short-circuit current of an OPD
A	Device area of an OPD
n	Ideality factor of a diode
kT	Thermal energy
J_0	Revert saturation current density of an OPD
V_{TG}	Top-gate voltage of a DG-OTFT
V_{TB}	Bottom-gate voltage of a DG-OTFT
$V_{th,eff}$	Effective threshold voltage of a DG-OTFT
C_T	Capacitance densities of top-gate dielectric of a DG-OTFT
C_B	Capacitance densities of bottom-gate dielectric of a DG-OTFT
I_0	Reverse saturation current of a diode
I_{ph}	Photocurrent of an OPD
R_S	Series resistance of an OPD
R_{sh}	Shunt resistance of an OPD
P_{opt}	Incident optical power
$I_{DS,light}$	Channel current of the DG-OTFT when the OPD is under illumination
$I_{DS,dark}$	Channel current of the DG-OTFT when the OPD is in dark
R	Photoresponsivity of a photodetector
J_{ph}	Photocurrent density of an OPD
η	External quantum efficiency of an OPD
hc/λ	Incident photon energy
φ_1	Fitting parameters of an OTFT-based photodetector
φ_2	Fitting parameters of an OTFT-based photodetector
TFT	Thin-film transistor

FET	Field-effect transistor
LCD	Liquid crystal display
AMOLED	Active matrix organic light-emitting diode
RFID	Radio frequency identification tag
OTFT	Organic thin-film transistor
a-Si	Amorphous silicon
a-oxide	Amorphous oxide
μc-OTFT	Microcrystalline organic thin-film transistor
DG-OTFT	Dual-gate organic thin-film transistor
OPD	Organic photodiode
OPT	Organic phototransistor
MOSFET	Metal oxide semiconductor field-effect transistor
PECVD	Plasma-enhanced chemical vapor deposition
a-Si: H	Hydrogenated amorphous silicon
μc-Si	Microcrystalline silicon
LT *poly*-Si	Low-temperature polycrystalline silicon
a-IGZO	Amorphous indium gallium zinc oxide
PPI	Pixel per inch
OLED	Organic light-emitting diode
EPD	Electrophoretic displays
P3HT	Poly(3-hexylthiophene-2,5-diyl)
PTAA	Poly[bis(4-phenyl) (2,4,6-trimethylphenyl) amine]
TIPS-pentacene	6,13-Bis(triisopropylsilylethynyl)pentacene
diF-TES-ADT	2,8-Difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene
ALD	Atomic layer deposition
NL	Nanolaminate
PV	Photovoltaic
LED	Light-emitting diode
C_2H_4	Ethylene

LUMO	Lowest unoccupied molecular orbital
HOMO	Highest occupied molecular orbital
C_4H_6	Butadiene
C_8H_{10}	Octatetraene
IE	Ionization energy
EA	Electron affinity
HCl	Hydrochloric
HNO_3	Nitric acid
PVD	Physical vacuum deposition
MoO_3	Molybdenum oxide
SAM	Self-assembled monolayer
PFBT	2,3,4,5,6-Pentafluorothiophenol
tetralin	1,2,3,4-Tetrahydronaphthalene
PTFE	Polytetrafluoroethylene
PEIE	Polyethylenimine ethoxylated
ICBA	Indene-C_{60} bisadduct
CVD	Chemical vapor deposition
TMA	Trimethylaluminium
TEMAH	Tetrakis(ethylmethylamido)hafnium
CH_4	Methane
OH-	Hydroxyl group
CH_3-	Methyl group
PDMS	Poly(dimethylsiloxane)
CPD	Contact potential difference
HOPG	Pyrolytic graphite
SSE	Single-stretched exponential
sc-OTFT	Single-crystal OTFT
RH	Relative humidity
DSE	Double stretched-exponential

sc-PDIF-CN_2	Single-crystal PDIF-CN_2
DG-OTFT	Dual-gate organic thin-film transistor
EQE	External quantum efficiency
RADFET	Radiation field-effect transistor
AmBe	Americium-beryllium

SUMMARY

Thin-film transistors (TFTs) are widely used in backplane circuits in consumer electronics, especially in the display industry. In recent years, the demand for high performance and new features of electronics have continued to increase. Among these new features, flexible displays attract the most interest, although flexible electric technology is still in its infancy. As a member of TFTs, organic thin-film transistors (OTFTs) have some unique properties for flexible electronics development since they can be fabricated through cost-effective and solution-based processes at moderate temperatures on a wide range of flexible and deformable substrates, such as plastic films and paper substrates. In spite of these advantages, current OTFTs still have two issues that restrict their wide applications and mass production. One issue is their low charge mobility values, which limit their operating speed; the other one is their fast degradation when operating in air. At present, the charge mobility of state-of-the-art OTFTs in laboratories is superior to that of amorphous silicon (*a*-Si) and approaches that of amorphous metal oxide (*a*-oxide) TFTs in markets. However, the operational stability of OTFTs generally remains inferior and a point of concern for their commercial deployment. Therefore, this dissertation first focuses on improving the stability of OTFTs and then explores the application of these high-performance OTFTs in light detection.

The first part of this thesis work reports on the characterization of solution-processed microcrystalline OTFTs (μc-OTFTs), showing high environmental and operational stability. The μc-OTFTs yield charge carrier mobility values of up to 1.6 $cm^2 V^{-1} s^{-1}$, which is superior to that of *a*-Si TFTs. These μc-OTFT devices have an ultra-thin

bilayer gate dielectric that consists of an amorphous fluoropolymer CYTOP layer and an Al_2O_3: HfO_2 nanolaminate. We find that the bilayer geometry results in two distinct aging mechanisms that yield very small shifts in threshold voltage through a compensation effect. We model the aging mechanism with a double stretched-exponential equation, which predicts a threshold voltage shift in the range of 0.1 V to 0.25 V over a dc-bias stressing time of ten years even at 55 °C. These results suggest that the threshold voltage stability of the *μc*-OTFTs in this work is superior to that of *a*-Si TFT technologies. These *μc*-OTFTs exhibit excellent environmental stability even after prolonged immersion in water. Furthermore, in contrast to the TFTs that use single-layer gate dielectrics, our approach yields devices that exhibit threshold voltage shifts that appear less sensitive to temperature variations. This breakthrough brings *μc*-OTFTs on par with some other commercial TFTs technologies in terms of operational, environmental, and thermal stability.

Based on the highly stable OTFT structures, the second work reports on a new photodetector concept in which a dual-gate organic thin-film transistor (DG-OTFT) integrates with an organic photodiode (OPD) device. The OPD operates in a photovoltaic mode instead of the common photoconductive mode. This new photodetector yields photoresponsivity values above 10 A W^{-1} and video-rate compatible response times with low power consumption. Therefore, it shows significant advantages over OPDs (having low photoresponsivity below 1 A W^{-1}) or organic phototransistors (OPTs) (having long response time). Moreover, the modeling of the photodetector that has this novel device architecture suggests that the responsivity could increase to 10^4-10^6 A W^{-1} by scaling the channel dimension and modifying the charge mobility of the transistor. Furthermore, the proposed device geometry enables the design of imaging pixel arrays with a simple read-

out, making the platform of this novel photodetector concept a promising candidate for next-generation sensing systems.

CHAPTER 1. INTRODUCTION

1.1 Thin-Film Transistors

A thin-film transistor is a type of field-effect transistor (FET) that is usually used in backplanes in electronic systems, as shown in Figure 1, to realize functions of in-pixel switching, current driving, and signal processing [1]. The TFTs are one of the essential components in liquid crystal displays (LCDs) or active matrix organic light-emitting diode (AMOLED) displays in televisions, smartphones, video game systems, personal digital assistants, and other flat panel displays [2-4]. Besides their uses in displays, TFTs are also investigated for a wide range of sensing applications such as chemical sensing, biochemical sensing [5], X-ray detection [1], and radio frequency identification (RFID) [6], which require more device functionalities beyond pixel switching.

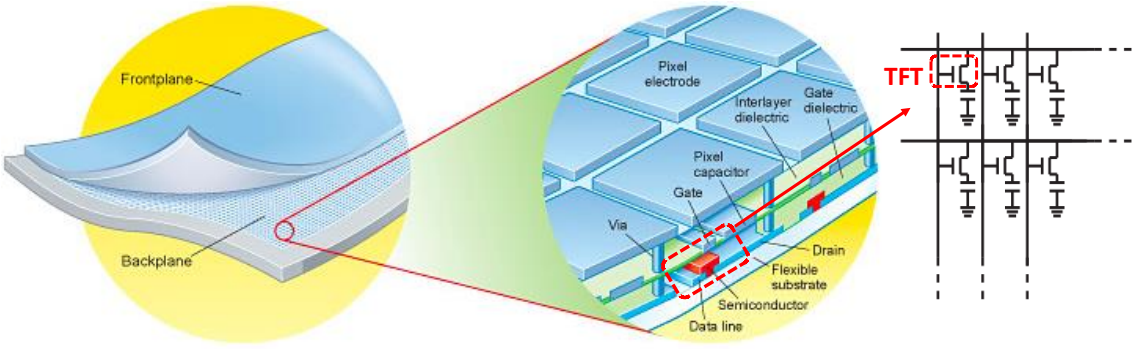


Figure 1. An illustration of a backplane structure (TFT array) with a front plane (sensor or display technology) [7].

1.1.1 Thin-Film Transistors and Metal Oxide Semiconductor Field-Effect Transistors

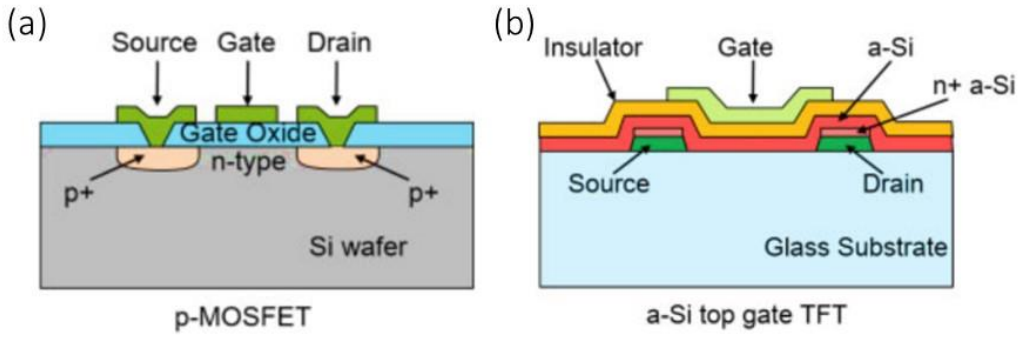


Figure 2. Schematic cross-section views of (a) a p-channel MOSFET and (b) an n-channel *a*-Si top-gate TFT [1].

As a type of FET, a TFT device consists of a semiconductor layer, a gate dielectric layer, and three electrodes (*i.e.*, gate, source, and drain). However, the structure of a TFT is different from that of a conventional metal oxide semiconductor field-effect transistor (MOSFET). Figure 2 shows device structures of a conventional p-channel MOSFET and an n-channel *a*-Si TFT.

The most apparent difference between TFTs and MOSFETs is their substrates and subsequent processing steps. For MOSFETs, layers are grown on silicon substrates, and thus, the fabrication techniques involve the deposition and ion implementation to form junctions around the source and drain electrodes. The process steps of MOSFETs are usually complicated, requiring many steps involving etching and photolithography. The process temperature of MOSFETs is typically higher than 600 °C. Also, the scalability of a MOSFET matrix is usually limited by the size of silicon wafers, whose diameters are less than 450 mm. In contrast, the process steps of TFT devices mainly involve thin-film deposition, which is usually through a plasma-enhanced chemical vapor deposition (PECVD) technique that is easily carried out on a variety of substrates at low temperatures and has high throughput with low costs. Thus, the primary advantage of TFTs over

MOSFETs is their simple processes and various options of substrates. TFTs can be fabricated on almost any kind of substrates, which could be very thin, transparent, flexible, and even stretchable. Also, there is almost no limitation on the dimensions of substrates. For example, the glass sheets and plastic films are widely used as substrates of TFT devices in both industry and laboratory research at present. With advantages in substrates and manufactory process, TFTs have been preferred as the main technology in large-area and flexible electronic systems, especially in the display industry.

1.1.2 Development of Thin-Film Transistor Technologies

The first widely used TFTs were made of CdS or CdSe, which charge carrier mobility (μ) values greater than 40 $cm^2\ V^{-1}\ s^{-1}$ [8, 9]. The mass production of these TFTs, however, was never fully realized. The main issues were poor uniformity and poor device reliability over large areas. In the 1980s, commercial adoption of TFT technologies was firstly realized by the use of hydrogenated amorphous silicon (*a*-Si: H), which is easily processable and shows much-improved stability at room temperature in an atmospheric environment [3]. Today, the *a*-Si: H TFT is still the most commonly used TFT technology. Figure 3 shows that the total shipment of *a*-Si: H TFTs displays used for smartphones reached 807 million units in 2018, which is the largest market share among all technologies [10].

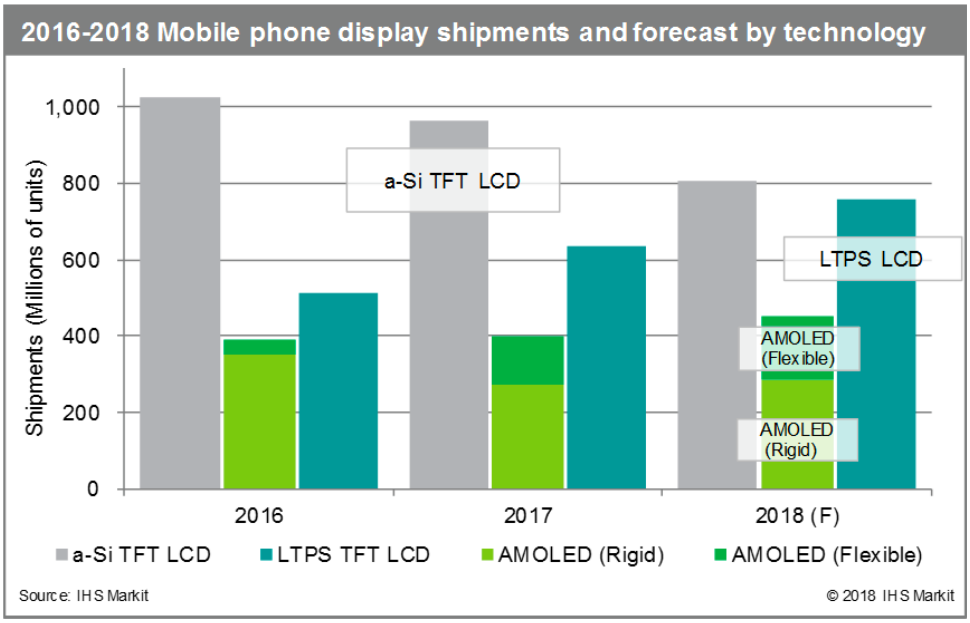


Figure 3. Shipments of mobile phone displays using different technologies [10].

However, we also observe that the shipment of *a*-Si: H TFT liquid crystal displays (LCDs) reduced from more than 1,000 million units in 2016 to 807 million units in 2018 in Figure 3. The shrinking market of *a*-Si: H TFTs is due to the limitation of *a*-Si: H TFTs in development and other emerging TFT technologies. Since the charge carrier mobility value of an *a*-Si: H TFT is limited in the range of 0.5 to 1 cm^2 V^{-1} s^{-1}, it hinders the development of fast switching circuits. Moreover, large threshold voltage (V_{TH}) instabilities of *a*-Si: H TFTs increase the complexity of backplane circuit designs [11, 12]. Especially, when the trend in consumer electronics demands higher performance, in terms of a higher display resolution and lower power consumption, as well as new features and functions, such as better flexibility, conventional *a*-Si: H TFTs reach bottlenecks in view of these challenges. To break through these limitations, there are tremendous research and development efforts focusing on the development of new TFT technologies using other semiconductor materials, such as microcrystalline silicon (μc-Si) [13], low temperature

polycrystalline silicon (LT *poly*-Si) [14], amorphous metal-oxide semiconductors (ex. amorphous indium gallium zinc oxide (*a*-IGZO)) [2], and organic semiconductors [15-18].

In recent years, the available types of TFTs, especially for the display market, are *a*-Si: H TFTs, LT *poly*-Si TFTs, metal-oxide TFTs, and organic TFTs. The development of these TFT technologies revolutionizes consumer electronic devices. At the same time, the increasing demand for consumer electronics is also a key factor driving growth in markets for TFTs development. As reported by the market research company, BBC Research, the global thin-film transistor market is estimated to reach $ 230.0 million by 2022 from $ 105.0 million in 2017 [19]. The growing market not only indicates an increase in the market size but also implies changes in the market proportions of different TFT technologies in the future.

1.1.3 Current Market for Thin-Film Transistors

The market proportion of each TFT technology usually depends on performance-based applications. Figure 4 shows the targeting display applications in consumer electronics of each TFT technology, in terms of device charge mobility and display resolution. The charge mobility is one of the most critical parameters of a TFT device in applications since it decides how fast a TFT could drive a pixel. It also determines the frame rate and the resolution of a display. Here, the frame rate of a display describes the frequency at which consecutive images (or frame) are displayed, and a standard value of a video display is 60 Hz due to temporal sensitivity of human vision sensitivity, so it would not vary a lot among different displays. However, display resolution describes the pixels

density of a display circuit and is usually calculated by pixel per inch (PPI). A higher resolution provides more details and a better definition of the image; thus, it is preferred by high-end and near-eye devices. The classification of displays by their resolution is also shown in Figure 4.

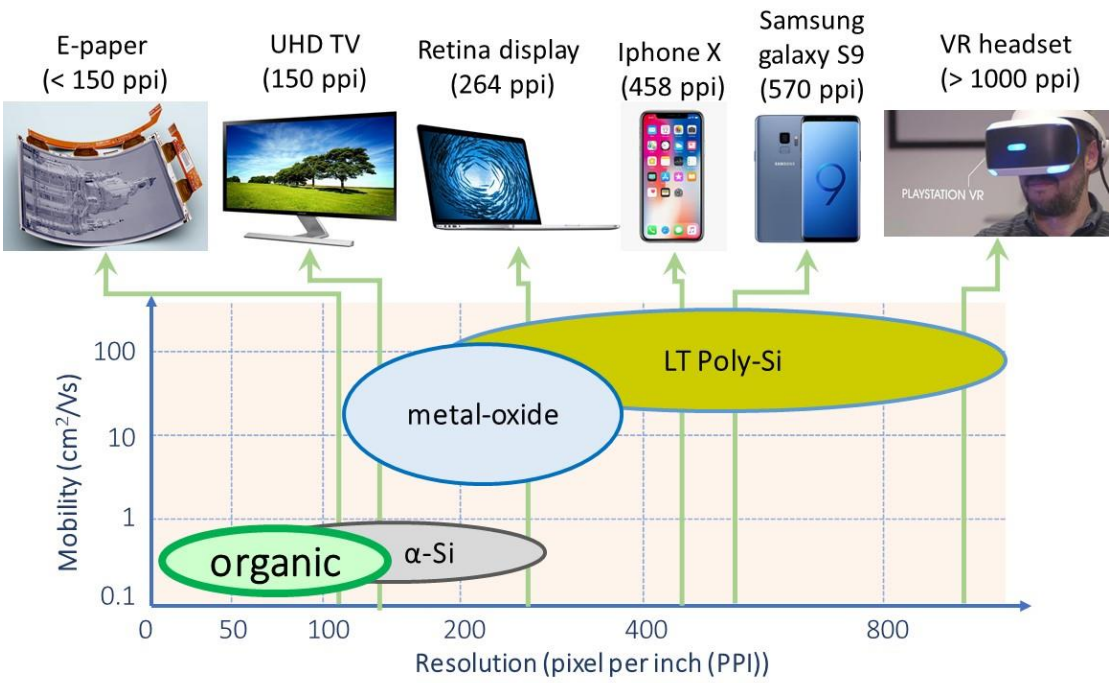


Figure 4. An illustration of TFT technologies in display market [20].

As discussed above, high-resolution displays are usually required in mobile and wearable devices, such as cell phones and smart glasses, of which the high resolution is realized by TFTs that use high charge mobility semiconductors. For example, LT *poly*-Si TFTs are preferred in displays with resolutions in the range of 200 to 1000 PPI, since their charge mobility values could be as high as 200 to 300 $cm^2\ V^{-1}\ s^{-1}$. However, the process temperature of LT *poly*-Si TFTs is usually above 400 °C, which requires the substrates having high resistance to heat. The metal-oxide TFTs are used in 150 to 300 PPI displays

with charge mobility values of around 10 to 100 cm^2 V^{-1} s^{-1}. Because metal-oxide TFTs have much lower process temperatures (typically between 200 °C to 350 °C) and better uniformity over large area comparing to LT *poly*-Si TFTs, they are typically used in larger portable devices, such as laptop computers, tablets, and high definition television displays. To drive television displays with relatively low resolution, *a*-Si: H TFTs are good candidates, due to their decent performance, low manufacturing costs, and well-established process systems for large-area display production. Despite the unique properties such as high flexibility and low process temperature, organic TFTs have currently limited commercial use, although they are being considered in niche markets such as electronic paper.

1.1.4 Potential of Organic Thin-Film Transistors

Figure 5 shows a forecast for the flexible display market in 2020. It is clear that the next-generation innovation of displays would be a paper-like display, which could be folded or rolled. Because of the intrinsic flexibility of organic semiconductors, organic light-emitting diode (OLED) technology is chosen to be used as the front panel of the flexible displays in today's market. For example, at CES 2018, the display company, LG, exhibited a massive curved 92-foot-long display, OLED Canyon, which was made up of more than 240 curved OLED displays. Also, Samsung demonstrated its first bendable cell phone at CES 2013 and released a foldable phone, Galaxy Fold, in 2019. At almost the same time, Huawei released its first foldable phone, Mate X. Figure 5 shows that bendable and foldable electronics will continue to gain market share and that stretchable electronics

will be launched as well. Since the OTFTs have the advantages of good flexibility as well as low process temperatures, they would have great potential for flexible electronics in the future.

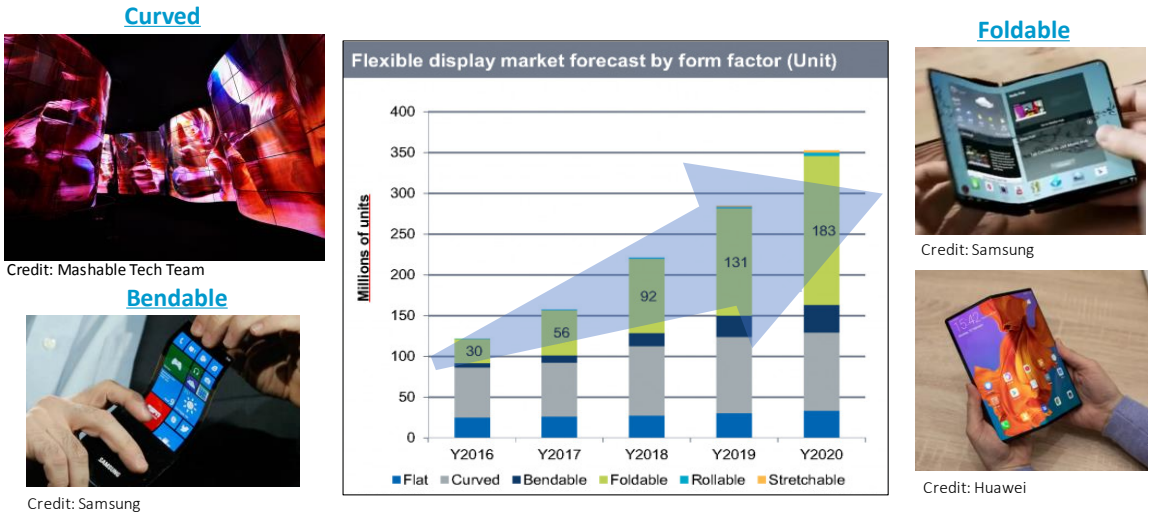


Figure 5. Flexible display market forecast to the year 2020 [21].

Even though the backplane of current OLED displays is still based on LT *poly*-Si TFTs and metal-oxide TFTs technologies, future backplanes for displays are likely to use OTFTs, due to the superior flexibility of organic semiconductor materials, if their charge mobility can be further increased. The high charge mobility of OTFT is especially critical for OLED devices where the luminance of a panel requires that a certain level of current be delivered to the OLEDs by the control OTFTs. Figure 6 shows some demonstrations of current applications of OTFTs in flexible electronics, ranging from flexible paper-thin computer screens and flexible plastic electrophoretic displays (EPD) to lightweight image scanners and flexible mechanical sensor skins. In addition, OTFTs have better compatibility with current OLED technology, resulting in a more natural integration. They could also share the same manufacturing techniques with OLEDs for mass production even

though most of the demonstrations are still at the laboratory research level. With the advantages and potentials discussed above, OTFTs will dramatically revolutionize the flexible electronic market once the technology gains further maturity. At present, there are still many issues existing in the OTFT technologies; they must be solved before mass production, which requires more efforts in OTFT's research.

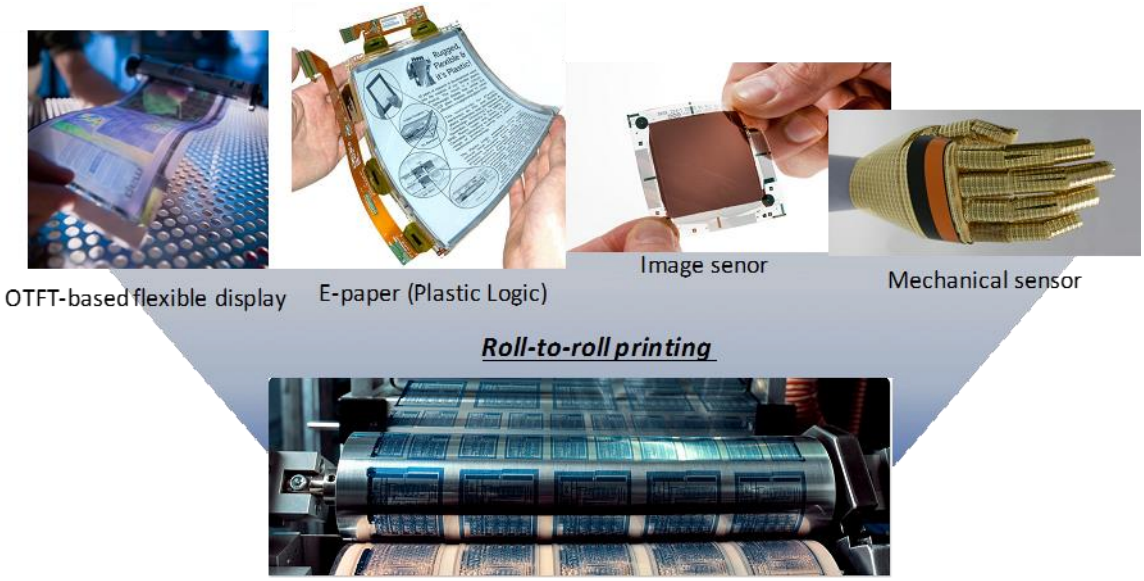


Figure 6. Examples of OTFT applications in flexible electronics [22-24].

1.1.5 Progress and Challenges for Organic Thin-Film Transistors

Next, we will discuss the progress of OTFTs achieved through research as well as remaining challenges. Since the first OTFT was demonstrated in the 1980s, they have attracted significant attention because of their capability to be processed at low temperature (typically below 100 °C) on flexible substrates (*e.g.*, metal foils and plastic sheets), with various low-cost printing and coating techniques (*e.g.*, roll-to-roll printing technique) [25].

With plenty of research on OTFTs in the areas of materials synthesis and device structures, the OTFT technology has been developed from a tool for organic semiconductor charge transport measurement to emerging technology for various applications [26-28]. Now, some prototypes using OTFTs have been realized and released in the market, even though there are still some remaining issues. Therefore, searching for the solutions to these issues is the most important work for realizing the mass production in more applications for OTFTs.

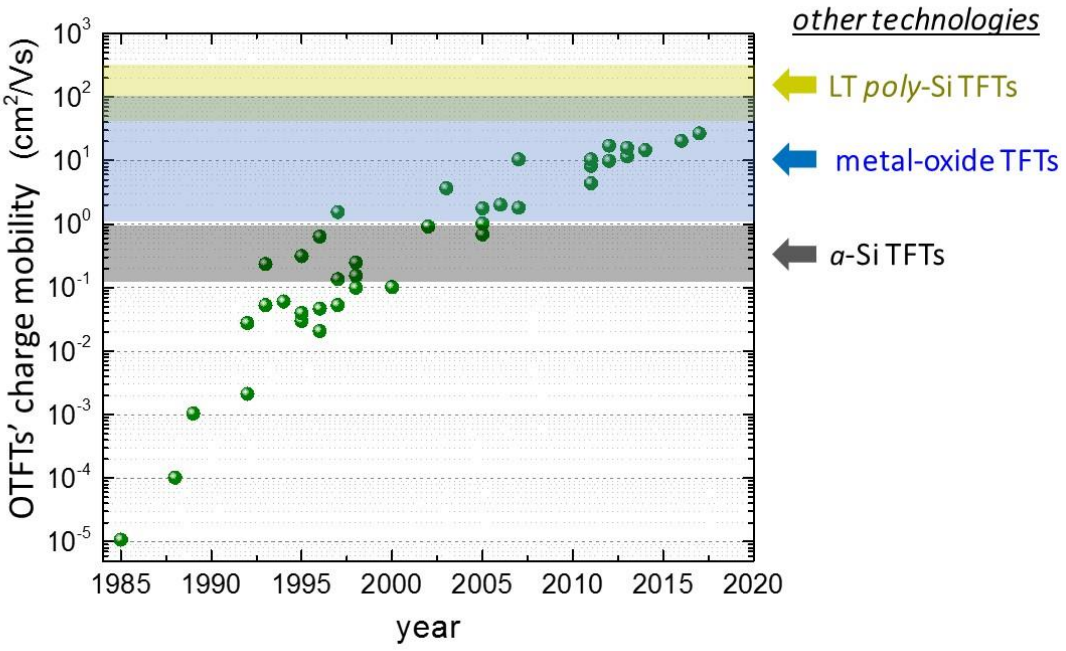


Figure 7. The progress of OTFTs' charge mobility in laboratory research [29, 30].

The first challenge for OTFTs is the low device charge mobility, which is below 1 $cm^2\ V^{-1}\ s^{-1}$ in today's market, as shown in Figure 4. Although this value is comparable to the charge mobility values of *a*-Si: H TFTs, it still limits the application scope of OTFTs. Therefore, one of the most popular study topics on OTFTs is increasing the device charge

mobility, which relies on fundamental charge transport physics of organic semiconductors. Figure 7 shows that, over the past decades, the values of charge mobility have increased from less than 10^{-3} cm^2 V^{-1} s^{-1} to over 30 cm^2 V^{-1} s^{-1} in laboratory research. These high charge mobility values of OTFTs have greatly exceeded those of benchmark *a*-Si: H TFTs and become comparable to those of metal-oxide TFTs that are used in mass products with relatively high resolution [31-33]. Although the charge mobility values of OTFTs are still lower than those of LT *poly*-Si TFTs, the current achieved values have already enabled a broad range of applications.

Besides the charge mobility issue, the high threshold voltage is another limitation for an OTFT as it influences power consumption during operation. In the early stage, operating voltages of OTFT devices were in the range of 100 - 150 V [34]. Such high operating voltages result in excessive power consumption, so it is not practical in most applications. This problem also has been studied in the past several years. Researchers have been working on improving the gate dielectric layer to reduce the threshold voltages [35]. In recent reports, by using high-κ materials as gate dielectric layers with small thicknesses, the threshold voltages were significantly reduced to around 1 V; this range of values is comparable to or even smaller than those of *poly*-Si TFTs [36, 37].

Another challenge for OTFTs is their performance in terms of stability during operation. Organic semiconductors, such as pentacene and poly(3-hexylthiophene-2,5-diyl) (P3HT), degrade fast when exposed to water or oxygen. In addition, for some applications, such as sensing, OTFTs must operate with high stability in an aqueous environment. Therefore, the stability of OTFTs has to be improved to enable reliable performance in applications. One effective method is to modify the device architecture, which must include

some environmental barriers to protect the semiconducting layer from reagents contained in air that can degrade the material.

1.2 Objectives

The primary objective of this dissertation is to develop a universal approach to improving the operational and environmental stabilities of OTFTs using low-cost fabrication methods. This research employs p-channel OTFTs with semiconducting layers consisting of blends of poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA) and 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) or 2,8-difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diF-TES-ADT). The gate dielectric layer of an OTFT comprises a thin amorphous fluoropolymer (CYTOP) layer and a metal-oxide layer grown by atomic layer deposition (ALD). This bilayer dielectric structure greatly reduces threshold voltages as well as operating voltages of OTFTs [16, 38]. Because it has been known that Al_2O_3 and HfO_2 nanolaminates (NL) grown by ALD could work as passivation layers that are good barriers for water and air [15, 39], Al_2O_3 - HfO_2 NL is used as the metal oxide layer in the bilayer gate dielectric structure to improve the device stability in high moisture and high oxygen environments.

Previous work had shown that the aging of an OTFT with a bilayer gate dielectric structure is very different from that of an OTFT with a single dielectric layer [38]. For OTFTs with bilayer gate dielectrics, the long-term operational stability of devices could be improved by engineering the thicknesses of two dielectric layers. To further investigate the stability of OTFTs with bilayer gate dielectrics, we use a model to simulate the aging

process of these OTFTs under different electrical operating conditions. The overall objective of our study is to compare the operational stability of OTFTs to that of inorganic TFTs, such as *a*-Si TFTs, metal-oxide TFTs, and even LT *poly*-Si TFTs.

The second objective of this research is to apply the OTFTs with high stability in the application of light detection. Two general architectures of organic photodetectors are organic photodiodes (OPDs) and organic phototransistors (OPTs). OPDs usually have fast responses to light signals, but have small photoresponsivity (< 1 A W^{-1}) without additional amplification mechanisms [40]. OPTs have high responsivity due to their fundamental property of signal amplification. However, their response time is much longer than that of OPDs. In this work, we investigate a new type of organic photodetector that consists of an OPD and a dual-gate organic thin-film transistor (DG-OTFT) to achieve high responsivity to weak light signals. In this device, a top-gate driven DG-OTFT is used to amplify the light signal which is detected by an OPD device. The response time is determined by the OPD, and it is around a millisecond level in this study. The structure of DG-OTFT is based on a single-gate OTFT with remarkable long-term operational and environmental stability. These DG-OTFTs also have small leakage currents and little noise, which defines the light detection resolution of the whole detection system.

1.3 Organization of the Dissertation

According to the motivations and objectives of this study, this dissertation is structured as follows. Chapter 1 introduces the necessary background of TFT technologies, including a comparison between TFTs and conventional MOSFETs, a comprehensive

discussion of inorganic and organic TFT technologies, and, especially, the potentials and challenges of organic TFTs in future development. Chapter 2 introduces a fundamental of organic semiconductors, semiconductor device physics, and operating principles of OTFTs. Chapter 3 covers the experimental methodologies of this work, including fabrication and characterization details of OTFTs and photodetectors. Chapter 4 discusses the stability of OTFTs, including the origin of device instability, the previous achievements to improve the stability of OTFTs, and results in this work. Systematical studies are discussed in this chapter with detailed analysis using mathematical models. Chapter 5 demonstrates the results of organic photodetectors with a new device structure, which consists of a DG-OTFT and an OPD. The device characteristics are also simulated with an analytical model. The impacts of device parameters on the performance of a photodetector are also discussed. Chapter 6 presents the conclusions of this work as well as some directions that can be further explored in the future.

CHAPTER 2. ORGANIC SEMICONDUCTORS AND DEVICE PHYSICS

2.1 Organic Semiconductors

Organic semiconductors are carbon-based materials that exhibit semiconducting properties. Organic compounds range in sizes from small molecules to macromolecules, or polymers. Their optoelectronic properties are easily tunable by modifying their chemical structures, which provide a considerable advantage over their inorganic counterparts. Moreover, some of these organic compounds can be soluble in organic solvents; therefore, they can form good films from a liquid state using low-cost conventional processing approaches, such as spin-coating and ink-jet printing. These advantages lead to remarkable design possibilities using organic semiconductors as active elements in optoelectronic devices, such as thin-film transistors, photovoltaic (PV) devices, and light-emitting diodes (LEDs). This work mainly focuses on OTFTs. Thus, the OTFT will be taken as an example to explain the principles of organic semiconductors.

2.1.1 Atomic Orbitals in the Carbon Atom

Carbon is a fundamental element in an organic molecule. Before discussing at a molecular level, this section introduces the atomic orbitals of a single carbon atom. In quantum mechanics, an atomic orbital is expressed by a mathematical function, which is a wave function (Ψ) that is a solution of the static Schrödinger equation, $\hat{H}\Psi = E\Psi$, where

$\widehat{H}$ is the Hamiltonian operator and E is an energy eigenvalue of a corresponding wave function (or eigenfunction). The wave function or atomic orbital describes the probability of finding an electron of an atom in any specific region. The plotted shape of an atomic orbital usually represents a physical space having a high probability of finding an electron.

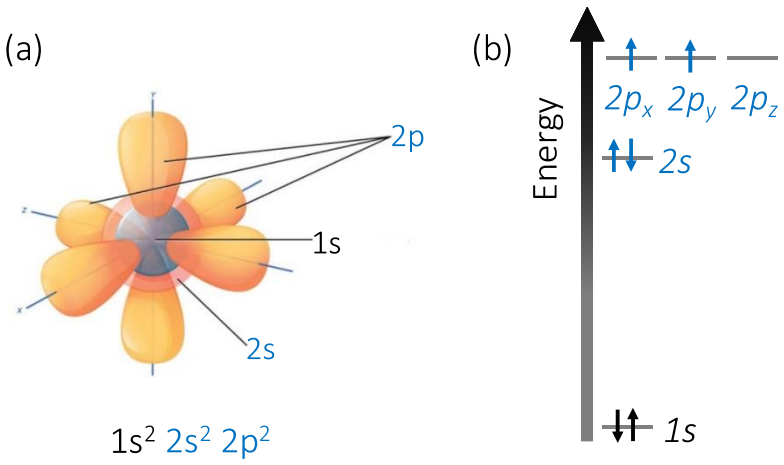


Figure 8. (a) An illustration of the atomic orbitals of an isolated carbon atom in its ground state [41]. (b) Energy levels (eigenvalues) of corresponding atomic orbitals of a carbon atom in its ground state. Each energy level is indicated by the name of its corresponding orbital.

Figure 8 (a) shows the atomic orbitals of an isolated carbon atom in its ground state and Figure 8 (b) shows the energy eigenvalues corresponding to these orbitals. A carbon atom has six electrons, and it has a $1s^2 2s^2 2p^2$ electronic configuration in its ground state. Two electrons having opposite spins occupy a spherical 1*s* orbital, with a higher probability density that is closest to the nucleus and a lower corresponding energy eigenvalue. The other four valence electrons occupy the outer shell orbitals: two in a spherical 2*s* orbital, one in a dumbbell-shaped $2p_x$ orbital, and one in a dumbbell-shaped $2p_y$ orbital.

2.1.2 Molecular Orbitals in Organic Materials

To start the description of molecular orbitals in organic semiconductor molecules, let us first take an ethylene molecule (C_2H_4) as an example. To form the molecular orbitals of a C_2H_4 molecule, the 2*s* orbital and two 2*p* orbitals of each carbon atom will combine to yield three $2sp^2$ hybrid orbitals, as shown in Figure 9. These three $2sp^2$ orbitals are equally distributed at 120° from each other in a plane, and the un-hybridized $2p_z$ orbital is perpendicular to the sp^2 orbital plane.

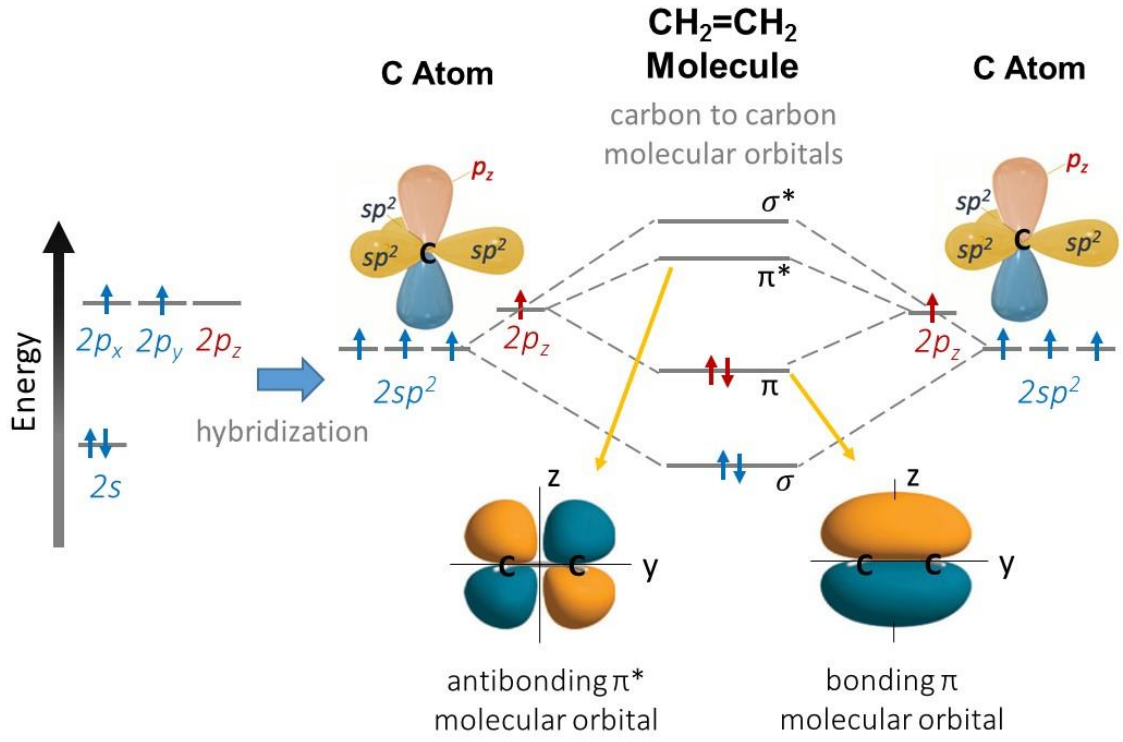


Figure 9. The energy values of sp^2 hybrid orbitals and un-hybridized p_z orbitals of carbon atoms that form an ethylene molecule, and the energy values of corresponding π and σ molecular orbitals formed between two carbon atoms in an ethylene molecule [42]. Each energy level is indicated by the name of its corresponding orbital.

In an ethylene molecule, two $2sp^2$ orbitals of each carbon atom linearly combine with the atomic orbitals of two hydrogen atoms and yield molecular orbitals that are known as σ molecular orbitals (their energy levels are not indicated in Figure 9). The remaining $2sp^2$ orbitals of two carbon atoms linearly combine and form another σ molecular orbital, of which corresponding energy levels are indicated in Figure 9. Electrons in σ molecular orbitals are localized between the nuclei of bonded atoms. Different from σ molecular orbitals, the orbitals formed by the combination of un-hybridized $2p_z$ orbitals of two carbon atoms is known as π molecular orbitals. Electrons in π molecular orbitals are referred to as π electrons, which are delocalized over the whole molecule.

A molecular orbital can be formed by the symmetric and antisymmetric linear combinations of two atomic orbitals; therefore, it has two possible wave functions with corresponding energy eigenvalues. For instance, in Figure 9, the π (or σ) molecular orbital has two possible wave functions with different energies, which are indicated with π and π* (or σ and σ*). The molecular orbital that has lower energy exhibits a high charge density in the region between two carbon atoms; therefore, it is referred to as a bonding π (or σ) molecular orbital. In contrast, the antisymmetric nature of the wave function corresponding to the higher energy molecular orbital results in a node in that region with zero charge density; therefore, it is referred to as an antibonding π* (or σ*) molecular orbital. In an isolated molecule at 0 K, two electrons occupy the bonding molecular orbital and have opposite spins due to the Pauli exclusion principle. In this case, the bonding π molecular orbital is the highest occupied molecular orbital (HOMO), and the antibonding π* molecular orbital is the lowest unoccupied molecular orbital (LUMO) in an ethylene molecule.

In general, organic semiconductor molecules, which contain π electrons, have carbon atoms that are connected through alternating double and single bonds, for instance, butadiene molecule (C_4H_6) and octatetraene molecule (C_8H_{10}) (see Figure 10). Such molecules are called conjugated molecules. In conjugated molecules with structures of extended chains (conjugated bridges) or rings (aromatic groups), π electrons are highly delocalized over the entire molecule. Also, when a conjugated molecule has more π molecular orbitals, the bonding π molecular orbital with the highest energy is the HOMO, and the antibonding π* orbital with the lowest energy is the LUMO. The HOMO and LOMO are usually referred to as frontier orbitals, as they generally decide the optical and electrical properties of an isolated molecule. This conclusion is based on an approximation that neglects the effect of electrons in σ orbitals and other π orbitals, considerably simplifying the description of electronic properties of an isolated conjugated molecule.

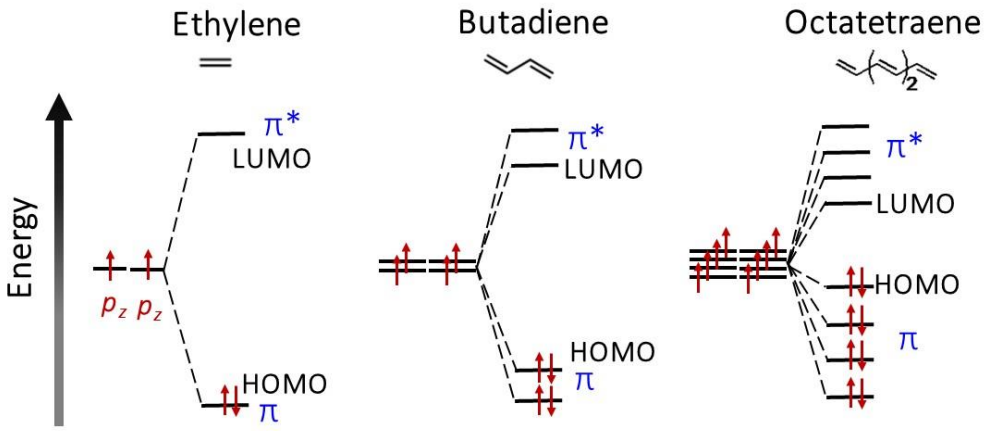


Figure 10. Energy levels of π molecular orbitals of ethylene, butadiene, and octatetraene molecules. Each energy level is indicated by the name of its corresponding orbital.

2.1.3 Energy Diagram in Solids

When considering a solid thin film that is made from conjugated molecules at finite temperature, one considers a large ensemble of molecules, typically in the range of 10^{21} molecules per cubic centimeter, and a correspondingly large number of π electrons. The energies of the frontier orbitals are no longer degenerate for each molecule of thin films in solid states, due to electronic interactions (*e.g.*, van der Waals forces) between the molecules in solid films and other effects such as positional and energetic disorder [43]. Therefore, a solid film can no longer be approximated by a two-level system with discrete energy levels of HOMO and LUMO. Instead, the electronic structure of a film is described in terms of HOMO and LUMO manifolds, as shown in Figure 11 (a).

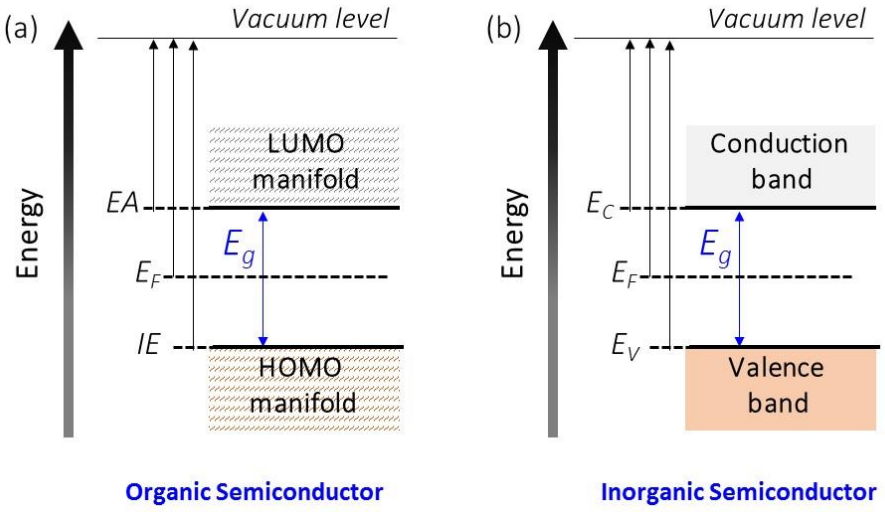


Figure 11. Energy diagrams of (a) organic and (b) inorganic semiconductors in solid films.

The difference in energy between the vacuum level and the highest energy of the HOMO manifold is called ionization energy (IE), while the difference in energy between the vacuum level and the lowest energy of the LUMO manifold is electron affinity (EA). The energies of HOMO and LUMO manifolds are separated by an energy gap (E_g), which induces the semiconducting properties of these materials. The Fermi level energy (E_F) of an intrinsic organic semiconductor is at the middle of the energy gap. The spatial overlap of frontier orbitals with nearly similar energy of neighboring molecules in a film provides the electronic coupling that is needed to enable π electrons to hop between molecules. These electron transfer reactions over many molecular building blocks at a macroscopic scale lead to electrical conduction.

By analogy with conventional inorganic semiconductors, the HOMO and LUMO manifolds of an organic semiconductor film can be associated with valance and conduction bands with an energy gap between them (see Figure 11 (b)). Thus, the IE and EA of an organic semiconductor correspond to the lowest energy of the conduction band (E_C) and the highest energy of the valence band (E_V) of an inorganic semiconductor film, respectively. Like in inorganic semiconductors, at finite temperature, due to the statistical thermodynamics, the probability of occupation of states at energies in the LUMO manifold is finite (Fermi-Dirac distribution function), leading to a finite density of electrons in the LUMO manifold and a finite density of holes in the HOMO manifold. These electrons and holes in LUMO and HOMO manifolds can contribute to the electrical conduction of organic semiconductor films. Within the free electron model and the effective mass approximation, electrical properties of an organic semiconductor can then be described in terms of electron and hole mobilities like in conventional materials. The optical properties

can be described in terms of transitions (*e.g.*, absorption and recombination) of particles between the HOMO and LUMO manifolds or one can also account for the excitonic effects (*i.e.*, effects of electron-hole interaction by the electrostatic Coulomb force).

2.1.4 Charge Transport

In conjugated organic semiconductor materials, charges are localized on different molecular sites; they can move through a succession of tunneling or transport by hopping between the nearest neighboring molecules through electronic couplings and electron-vibration interactions. The hopping process can be understood by an electron-transfer reaction between two neighboring molecules (*e.g.*, A_1 and A_2) and is represented by $A_1^- + A_2 \rightarrow A_1 + A_2^-$. Also, the similar reaction in hole transport between two neighbouring molecules (*e.g.*, D_1 and D_2) is given by $D_1 + D_2^+ \rightarrow D_1^+ + D_2$. Figure 12 (a) and (b) show the electron-transfer and hole-transfer reactions on energy level diagrams, respectively.

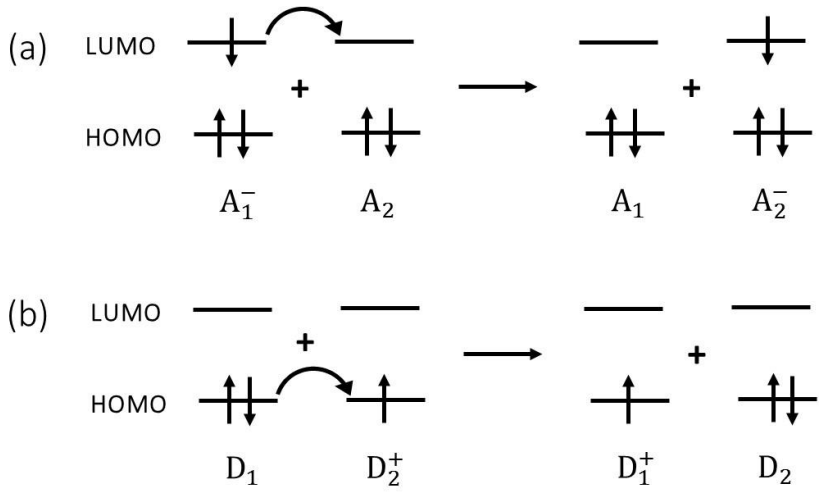


Figure 12. Illustrations of (a) electron-transfer reaction and (b) hole-transfer reaction.

To explain the energy changes during the charge transport process, let us take a donor-acceptor system as an example. The charge transfer reaction in a donor-acceptor (D-A) system could be represented by $D + A^+ \rightarrow D^+ + A$. The nuclear geometry in a natural state is different from that in a charged state. Figure 13 shows the potential energy surfaces corresponding to the donor and acceptor molecules in the neutral state (denoted by "1") and in the charged state (denoted by "2").

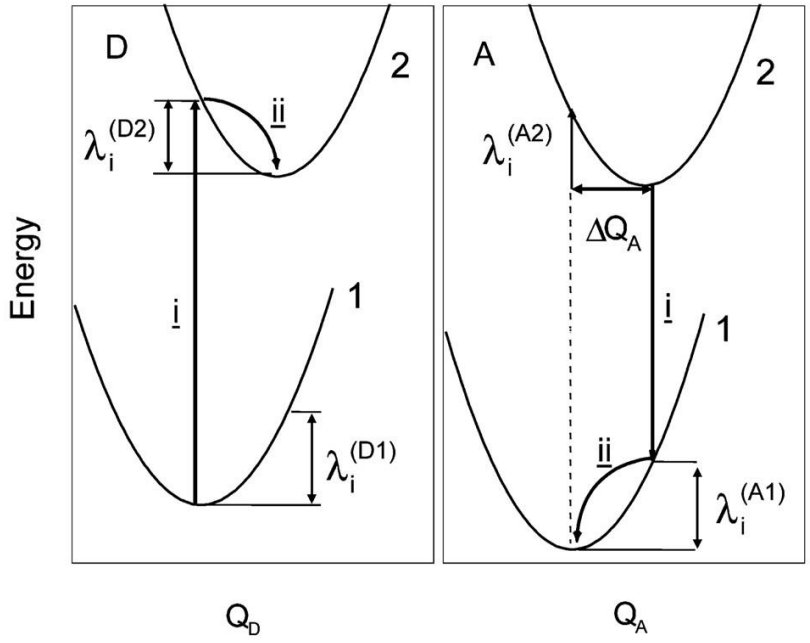


Figure 13. An illustration of the potential energy surfaces related to electron transfer [44, 45].

The electron transfer process includes two steps. Step i is the simultaneous oxidation of D (*i.e.* $D \rightarrow D^+$) and the reduction of A^+ (*i.e.*, $A^+ \rightarrow A$). Based on the Franck-Condon approximation, this step corresponds to a vertical transition from the minimum of the $D1$ surface to the $D2$ surface and a vertical transition from the minimum of the $A2$ surface to the $A1$ surface, as shown in Figure 13. Step ii corresponds to the relaxation of

the product nuclear geometries; the change of energy in this step is the reorganization energy. Therefore, the total reorganization energy λ in this reaction is given by [44, 45]:

$$\lambda = \lambda_i^{(A1)} + \lambda_i^{(D2)} \tag{1}$$

where $\lambda_i^{(A1)} = E^{(A1)}(A^+) - E^{(A1)}(A)$ and $\lambda_i^{(D2)} = E^{(D2)}(D) - E^{(D2)}(D^+)$. $E^{(A1)}(A^+)$ and $E^{(A1)}(A)$ are the energies of the neutral acceptor A at the cation geometry and the ground-state geometry, respectively; while $E^{(D2)}(D)$ and $E^{(D2)}(D^+)$ are the energies of the radical cation D^+ at the neutral geometry and the ground-state geometry, respectively.

The reorganization energy is one of the key factors that determine the charge-transfer rate. Based on Marcus theory, the rate (k_{ET}) of the charge-transfer process in a conjugated organic material is given by [44, 45]:

$$k_{ET} = \frac{2\pi}{\hbar}\left|V_{ij}\right|^2 \sqrt{\frac{1}{4\pi k_B T \lambda}} \exp[-\frac{(\Delta G^0 + \lambda)^2}{4\lambda k_B T}] \tag{2}$$

where $\hbar$ is the reduced Planck constant, k_B is the Boltzmann constant, T is the temperature, V_{ij} is the electronic coupling matrix element, and ΔG^0 is the variation of the Gibbs free energy during the reaction.

Given the charge-transfer rate, the charge mobility can be obtained by using the Einstein relation $\mu = \frac{eD}{k_B T}$, which describes the diffusion of the charges in the absence of applied electric fields. e is the elementary charge and D is the diffusion coefficient. In a one-dimension system, the diffusion coefficient is calculated as $D = L_c \times v$, where L_c is the mean length of a charge travelled, and v is the average velocity. Since $v = L_c \times k_{ET}$,

the diffusion coefficient is given by $D = L_c^2 \times k_{ET}$ [43]. Therefore, the charge mobility μ due to the hopping process can be expressed as:

$$\mu = \frac{eL_c^2}{k_B T}\frac{2\pi}{\hbar}\left|V_{ij}\right|^2\sqrt{\frac{1}{4\pi k_B T\lambda}}\exp[-\frac{(\Delta G^0+\lambda)^2}{4\lambda k_B T}] \quad (3)$$

When a charge hops from an ionized molecule to an adjacent neutral molecule and these two molecules have identical chemical natures, this hopping process can be described as a self-exchange electron-transfer reaction. In that context, $\Delta G^0 = 0$ in Equation (2) and (3). From Equation (3), we found that the value of charge mobility in organic semiconductors is related to two parameters: the electronic coupling V_{ij} and the reorganization energy λ. Thus, the charge mobility in organic materials can be improved by maximizing the electronic coupling between adjacent molecules or minimizing the reorganization energy.

2.1.5 Charge Injection into Organic Semiconductors from Electrode Contacts

When solid-state devices are fabricated from organic semiconducting films, besides electrical conduction of the films, one needs electrodes to either inject or collect charges that transport in the films. The capabilities of electrodes to inject or collect charges are relevant to the relative energy difference of IE or EA with the work function (ϕ_m) of the material used for the electrode. The relative energy difference between ϕ_m and EA is known as the energy barrier height of electron injection (ϕ_{bn}); while that between ϕ_m and IE is known as the energy barrier height of hole injection (ϕ_{bp}). Since most of the organic

semiconductors are intrinsic with the Fermi level energy at the middle of the energy gap, the type of an organic semiconductor device is generally determined by the energy barrier height of electrons or holes at metal-semiconductor interfaces.

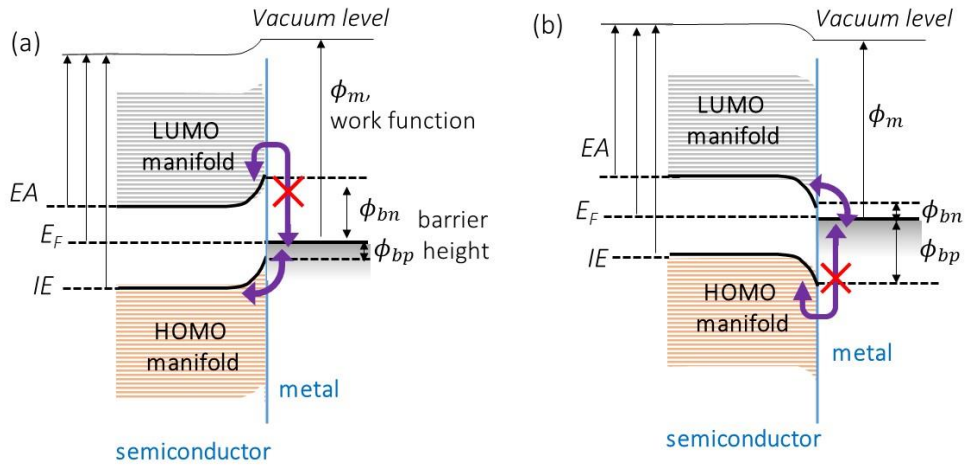


Figure 14. Energy diagrams of (a) a p-channel and (b) an n-channel organic semiconductor-metal interface.

Figure 14 (a) and (b) show the energy diagrams of a p-channel and an n-channel organic semiconductor-metal interface, respectively. The metal (or any conductive material) that has relatively high work function is often used in a p-channel organic semiconductor device. In this case, ϕ_{bp} is much smaller than ϕ_{bn}; thus, transport of holes between semiconductor and electrode is much easier than that of electrons. In contrast, the metal that has relatively low work function is chosen as the electrode for an n-channel organic semiconductor device. Since ϕ_{bp} is much larger than ϕ_{bn}, electrons can be injected to or collected from the semiconductor layer more easily than holes. These energy diagrams also explain the charge injection from source electrodes into semiconductor layers of OTFT devices. The injection barrier height will introduce the injection resistance (or contact resistance), which should be as small as possible for efficient injection.

Therefore, many studies focus on reducing the contact resistance to increase the field-injection current of a transistor effectively. The most common approach to reducing the contact resistance is to modify the work function of the electrodes [46-48].

2.2 Organic Thin-Film Transistors

Since we have discussed the semiconducting properties of organic materials and the principles of charge transport between organic semiconductor films and electrodes, this section will introduce basic device physics of organic thin-film transistors.

2.2.1 Device Structures

Figure 15 (a) and (b) show two typical OTFTs structures (the bottom-gate and the top-gate configurations) that are classified by the position of gate electrodes to the organic semiconductor layers. For both structures, an OTFT consists of a semiconductor layer, a gate dielectric layer, and three electrodes (gate, source, and drain). The current flows between the source and drain electrodes in the semiconductor layer, and the area between source and drain is defined as the channel of a transistor. The dimensions of the source and drain electrodes determine the channel length (L) and width (W), as shown in Figure 15 (c). In this work, the device length ranges from 60 μm to 200 μm and the width ranges from 2000 μm to 1 mm. The total thickness of the OTFT is around a few hundred nanometers. In operation, the voltage applied to the gate electrode (V_{GS}) controls the current that flows in the channel between the source and drain electrodes (I_{DS}), while the voltage across the drain and source electrodes (V_{DS}) determines the flow directions of channel carriers (*i.e.*, electrons or holes).

The geometries of OTFTs affect not only the feasibility of fabrication but also the device performance. The bottom-gate configuration has an advantage in research because of the commercially available highly doped Si wafer covered with SiO_2 with the fair quality for organic semiconductor deposition. However, the pre-treatment of the Si wafer is necessary, since organic semiconductor deposition is usually sensitive to the roughness and surface energies of substrates. In addition, passivation layers are needed on top of the semiconductor layer of an OTFT in the bottom-gate configuration, due to the instability of organic materials in the air. In contrast, the top-gate configuration shows the advantage over bottom-gate one since its insulator can work as passivation as well as gate dielectrics simultaneously so that greatly improves the stability of the device.

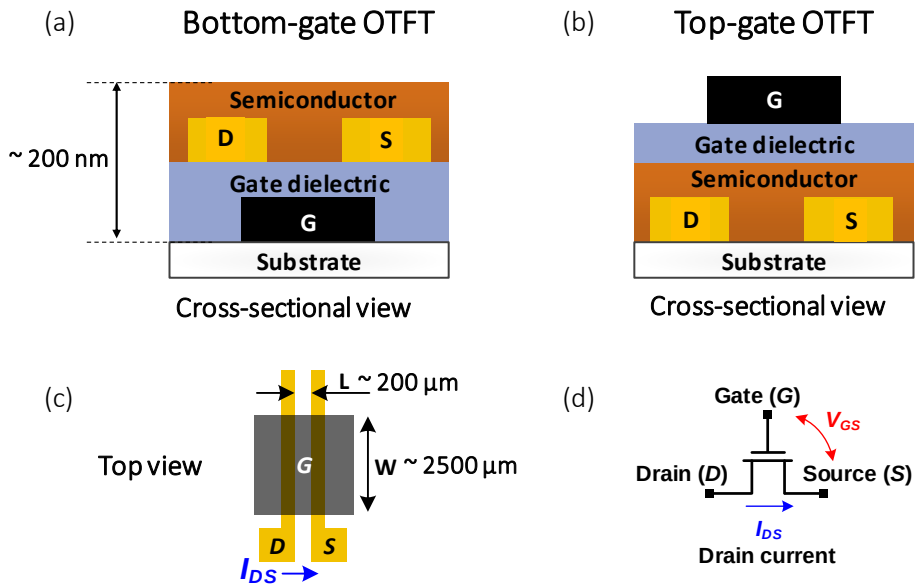


Figure 15. Cross-section views of (a) the bottom-gate and (b) the top-gate OTFT geometries. (c) A top view of an OTFT geometry. (d) Symbol of an OTFT.

2.2.2 Device Operation

The p-channel OTFT is chosen here as an example to discuss the device operation principles. The transporting carriers in a p-channel OTFT are holes, and their density depends on the gate voltage. In a real device, however, a large number of charge traps exist in the film, and they have to be filled before the gate-voltage induced charges can move. Moreover, the mismatch between the Fermi level energy of the gate material and the IE of the HOMO manifold will cause a band tilting in the organic semiconductor. Therefore, an additional voltage is necessary to be applied at the gate electrode to achieve the flat-band condition [49]. A minimum gate voltage that has to be applied to induce free carrier density in an OTFT is known as the threshold voltage (V_{TH}). Below this voltage, there is no mobile charges or current flow in the channel, and a transistor is at an "off" state.

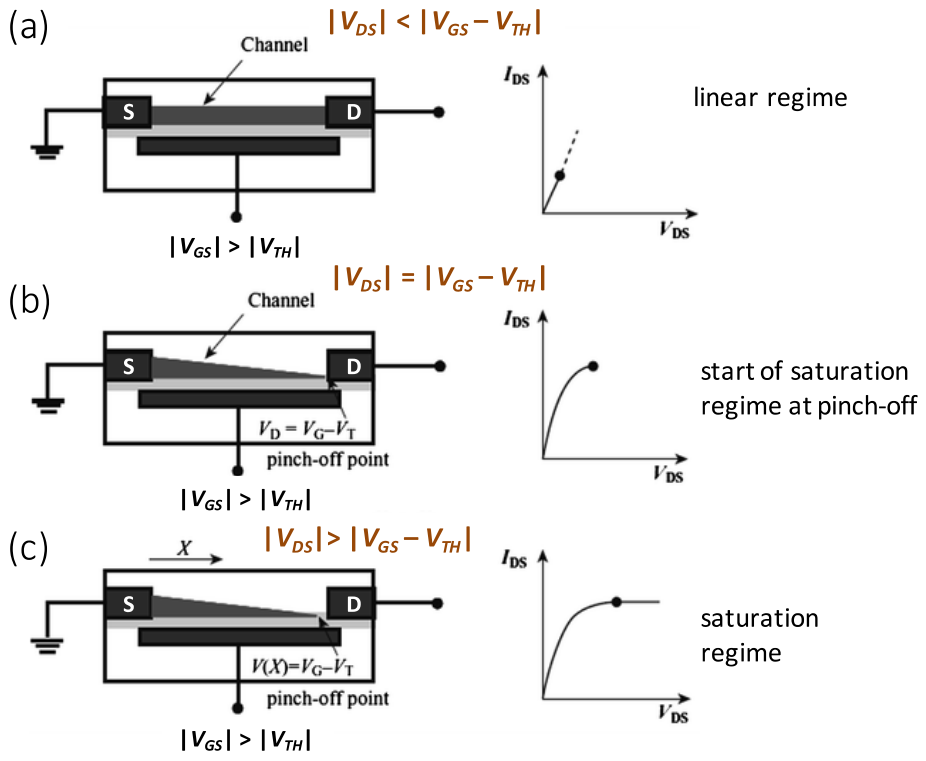


Figure 16. Carrier concentration profiles of an OTFT (a) in the linear regime, (b) when "pinch-off" occurs, and (c) in the saturation regime [50].

Figure 16 shows the carrier concentration profiles of an OTFT in different operation regimes. For a p-channel OTFT, when a negative voltage applied at the gate electrode and $|V_{GS} - V_{TH}| > 0$, positive charges will be induced at the interface between the insulator and the organic semiconductor. The total induced charge density in the semiconductor per area (q_{ind}) at a distance x from the source electrode is given by:

$$q_{ind}(x) = C_{ox}(V_{GS} - V_{TH} - V(x)) \tag{4}$$

where C_{ox} is the capacitance density of the gate dielectric layer, and $V(x)$ is the surface potential at x [51, 52]. Figure 16 (a) shows that when V_{DS} = 0 V, the charge density is uniform across the channel.

When $|V_{DS}|$ increases but remains below $|V_{GS} - V_{TH}|$, there is a linear gradient in the charge concentration at the channel, as shown in Figure 16 (b). In this case, the transistor works in the linear regime. The average value of the induced charge density ($q_{ind,ave}$) is $C_{ox}(V_{GS} - V_{TH} - \frac{V_{DS}}{2})$, which equals to the charge density at the middle point of the channel [51]. Based on Ohm's law, the current flow between the source and drain electrodes (I_{DS}) follows the equation:

$$I_{DS} = \frac{Wt}{L}\sigma V_{DS} \tag{5}$$

where σ is the channel conductivity, and t is the thickness of the charged layer in the channel. If we assume the charge mobility (μ) is constant, σ can be approximated by $\frac{\mu}{t}q_{ind,ave}$. Therefore, substituting σ into Equation (5), we obtain the current-voltage (*I-V*) equation of an OTFT in the linear regime:

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (6)$$

When $|V_{DS}| \ll |V_{GS} - V_{TH}|$, the term of $\frac{1}{2} V_{DS}^2$ in Equation (6) is negligible. In such conditions, Equation (6) can be further simplified to:

$$I_{DS} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} \quad (7)$$

Equation (7) shows that in this regime the channel current is linearly proportional to the drain to source voltage when $|V_{DS}| \ll |V_{GS} - V_{TH}|$.

Figure 16 (b) shows that when V_{DS} further increases to the point where a potential difference between the gate and the channel near the drain is zero ($|V_{DS}| = |V_{GS} - V_{TH}|$), a depleted area appears at the drain and the channel is said to be pinched off. Only a space-charge-limited saturation current can flow across this narrow depletion zone. Beyond this point, a further increase in V_{DS} pushes the pinch-off point further away from the drain, as shown in Figure 16 (c). As long as the depletion region is smaller than the channel length, the increase in V_{DS} will not increase the channel current. In other words, the channel current saturates, and this operating regime is known as the saturation regime. Therefore, when $|V_{GS}| > |V_{TH}|$ and $|V_{GS} - V_{TH}| \leq |V_{DS}|$, the OTFT operates in the saturation regime. By substituting $V_{DS} = V_{GS} - V_{TH}$ into Equation (6), we obtain and the *I-V* characteristics of an OTFT in the saturation regime:

$$I_{DS} = \mu C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2 \quad (8)$$

2.2.3 Characterization of Organic Thin-Film Transistors

Figure 17 (a) and (b) show two important types of *I-V* characteristics of a p-channel OTFT referred to as output and transfer characteristics. The output characteristic describes the I_{DS} as a function of V_{DS} at different V_{GS} values, and it clearly shows the linear regime and saturation regime of an OTFT in operation. The transfer characteristic describes I_{DS} as a function of V_{GS} at a specific value of V_{DS}. As discussed above, when V_{GS} is below the threshold voltage, there is no current flow in an ideal device between the source and drain electrodes, referred to as the "off-state" of an OTFT. However, in a real device, the measured current is nonzero, which mainly due to the leakage current of the gate dielectric. This current refers to as the off current (I_{off}). When V_{GS} is larger than V_{TH}, channel current I_{DS} will form, and the OTFT will be at the "on-state". The current at on-state refers to as on current (I_{on}). Figure 17 (b) shows the transfer curve that can be obtained by applying a constant large V_{DS} and sweeping the V_{GS} from the off-state ($|V_{GS}| < |V_{TH}|$) to the on-state ($|V_{GS}| > |V_{TH}|$) then from the on-state back to the off-state. From these results, we can observe if the OTFT has hysteresis, a feature that usually is not desired in the current-voltage behaviour of an OTFT.

The charge carrier mobility is one of the most important electrical parameters in the evaluation of the performance of an OTFT. If the value of C_{ox} is known, the value of saturation charge mobility μ can be extracted from the slope of a linear fit of the square root of drain current as a function of the gate voltage in the saturation regime, using Equation (8). Another important parameter, V_{TH}, often relates to the smallest power consumption to switch on an OTFT. In Figure 17 (b), the value of V_{TH} can be obtained

from the intercept of the gate voltage axis with the same linear fitting of the square root of drain current as a function of the gate voltage. The channel current on-off ratio is defined as the ratio of I_{DS} at the on-state and the off-state, and it can be calculated by I_{on}/I_{off}. Since I_{off} is the leakage current of an OTFT, a high-performance OTFT usually should have a large current on-off ratio.

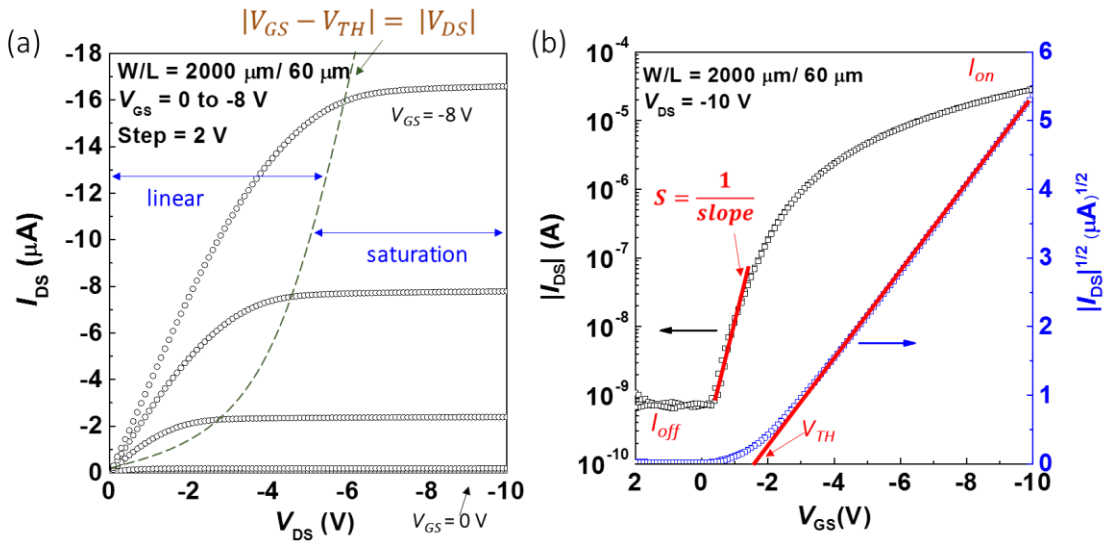


Figure 17. (a) The output characteristic and (b) the transfer characteristic of an OTFT.

Besides the primary electrical parameters of an OTFT, several other parameters are also usually considered when evaluating a real OTFT device. For example, the subthreshold swing (S) comes from the source-to-drain leakage current when the gate voltage is below but close to the threshold voltage. The value of *S* usually reflects the trap densities at the interface between the semiconductor and dielectric layers. Its value can be extracted from the transfer characteristic by fitting at the range close to the threshold voltage, and it follows the equation given by [53]:

$$S = \frac{dV_{GS}}{d(log(I_{DS}))} \tag{9}$$

In addition, contact resistance (R_C) is another parameter that might be not negligible in a real OTFT. In an ideal case, $\sqrt{I_{DS}}$ should linearly increase with V_{GS} in the saturation regime. However, Figure 17 (b) shows that $\sqrt{I_{DS}}$ is slightly curved when V_{GS} is close to the threshold voltage, due to the large contact resistance of the OTFT. As discussed previously, the contact resistance is caused by the energy difference between the work function of the metal contact and the corresponding IE (for p-channel) or EA (for n-channel) of the organic semiconductor, leading to energy barriers for the injection of carriers. The value of R_C should be as small as possible, and it could be reduced by modifying the work function of the metal electrode or changing the Fermi level energy of the semiconductor layer through doping.

The value of R_C can be calculated from the output curves. In Figure 17 (a), at a given drain-to-source voltage, the slope of each curve at a linear regime equals to the on-state resistance (R_{on}) of an OTFT. The relation between R_{on} and R_C is given by [54]:

$$R_{on} = R_{ch} + 2R_C = R_{sh}\frac{L}{W} + 2R_C \tag{10}$$

where R_{ch} is the channel resistance, and R_{sh} is the sheet resistance of the channel. Thus, the value of R_{on} linearly changes with the channel length at a fixed channel width. If we plot R_{on} versus L, the value of R_C could be extracted from the value of R_{on} when the channel length equals to zero.

CHAPTER 3. EXPERIMENTAL METHODS

This chapter will describe the fabrication and characterization setups of the devices employed in this dissertation, including OTFTs, capacitors, and photodetectors. The first part of this chapter focuses on the device fabrications. The process steps of OTFTs include the metal deposition of electrodes, the deposition of a self-assembled monolayer to reduce the contact resistance, the solution process of organic semiconductor layers and polymer gate dielectric layers, and the deposition of metal-oxide gate dielectric layers. The process steps of capacitors include the metal deposition of electrodes and the deposition of dielectrics, which are the same as the gate dielectric layers of OTFTs. Since the photodetector consists of an OTFT and an organic photodiode, besides the process of the OTFT, the organic photodiode is fabricated through the deposition of a hole collecting layer, a light absorption layer, and an electron collecting layer using solution processing and vacuum deposition techniques. The second part of this chapter describes general characterization methods that used in this work to measure the characteristics, such as the thicknesses of thin films, the work function of electrodes, the device current-voltage characteristics, the capacitances of dielectric layers, and the optical characteristics of photodetectors.

3.1 Device Fabrication

Organic semiconductor materials usually cannot survive in conventional semiconductor processes, which are minus processes, such as solvent cleaning, etching,

and photolithography. On the contrary, organic semiconductor devices are usually fabricated on bare substrates through additive processes, such as thermal evaporation, solution casting, and atomic layer deposition. In this section, we will introduce the specific fabrication techniques of the organic devices in this dissertation, from the preparation of substrates to the deposition of electrodes, self-assembled monolayers, semiconductor layers, and dielectric layers.

3.1.1 Substrates Preparation

An essential step of device fabrication is the preparation of the substrates, including substrates cutting, patterning, and cleaning. In this dissertation, the top-gate OTFT devices and the capacitors were fabricated on glass substrates (Corning® Eagle XG), and the organic photodetectors were fabricated on ITO-coated glass substrates, which have a sheet resistance of around 15 Ω/□ (Colorado Concept Coatings LLC).

For ITO substrates, pre-cutting and patterning were needed based on the geometries of devices. The as-purchased ITO sheet is 14” x 14” and the non-uniform part of the ITO-coated glass sheet was removed firstly. For the fabrication of the photodetector in this work, the ITO-coated glass sheet was cut down to 1.5” × 2” pieces. Then, the substrates were partially masked with Kapton® tapes, covering the place that would not be etched. For example, 1.5” x 1.5” of the ITO area was covered with Kapton® tapes on the substrates of photodetectors in this work. Next, the substrates were immersed in an etchant that consisted of a hydrochloric (HCl) and nitric acid (HNO_3) mixture solution in a 3:1 volume ratio for 8 minutes at a bath temperature of 60 °C. After the wet etching process, the

patterned slides were rinsed with distilled water immediately, followed by removing the Kapton® tapes. Next, the substrates were cleaned and scrubbed with detergent (Alconox Liquinox) to remove any remaining tape residue.

The preparation of glass substrates starts from solvent cleaning process without the patterning step. For solvent cleaning, the as-purchased glass substrates or patterned ITO substrates went through ultrasonic baths in deionized water, acetone, and 2-propanol in sequence. The ultrasonicator (Branson 5510) was used to create the ultrasonic baths and maintain the bath temperature at 45 °C for at least 20 min for each step. After the last bath step in 2-propanol, the samples were blown to dry by a stream of N_2 gas and placed in sample cases for the next process step.

3.1.2 Deposition of Metal Electrodes and Dopants

The device electrodes and dopants for contact doping were deposited by a computer-controlled physical vacuum deposition (PVD) system, which is a SPECTROS 200 system from Kurt J. Lesker Company and designed for the deposition of both organic and inorganic materials. Because most organic materials would degrade with oxygen and moisture in air, this deposition system was connected to a N_2-filled glovebox (MBRAUN) to avoid exposing samples to air during the process.

Instead of using conventional pattern techniques, such as photolithography, the organic devices in this work were patterned through shadow masks, which are metal sheets with some desired patterns for electrodes. These shadow masks were made of 0.12 mm-

thick molybdenum sheets (ASTM-B-386, Eagle Alloys Corp.). The patterns of masks were pre-designed through a computer-aided design software (Autodesk), and then the metal sheets were cut by an IR laser (Resoneticsm Corp.), which has a beam size of approximately 50 microns. The substrates of samples were attached with the desired shadow masks manually before loading in the chamber of the deposition system for metal deposition.

In the evaporator chamber, samples were fixed on a substrate holder, which rotated during the deposition to improve the uniformity of films. The films were deposited at a high vacuum condition with a base pressure below 10^{-7} Torr. The deposition rate was monitored by a standard quartz crystal. Since p-channel OTFTs were studied in this dissertation, the metal with a high work function was preferred for source and drain electrodes. In this work, Ag, with a work function around 4.7 eV, was usually chosen to be deposited as source and drain electrodes by the thermal deposition system. To further reduce the contact resistance between Ag electrodes and organic semiconductor layers, a p-type dopant material, molybdenum oxide (MoO_3), was also deposited by this system for contact doping in specific cases, such as at the source and drain electrodes of the p-channel OTFTs, and the electrodes close to the hole-collecting layers of the OPDs in this work.

3.1.3 Deposition of PFBT Self-Assembled Monolayers

Besides using dopant for the contact resistance reduction, depositing a self-assembled monolayer (SAM) on an electrode is another method to decrease the contact resistance, by modifying the work function of a metal electrode [55, 56]. In addition, this

monolayer could further improve the morphology of the semiconductor layer on its top. In this work, 2,3,4,5,6-pentafluorothiophenol (PFBT, Sigma Aldrich) was used to form a monolayer by chemisorption on source and drain electrodes of p-channel OTFTs, which need high work functions electrodes for hole injection. The chemical structure of PFBT is illustrated in Figure 18 (a).

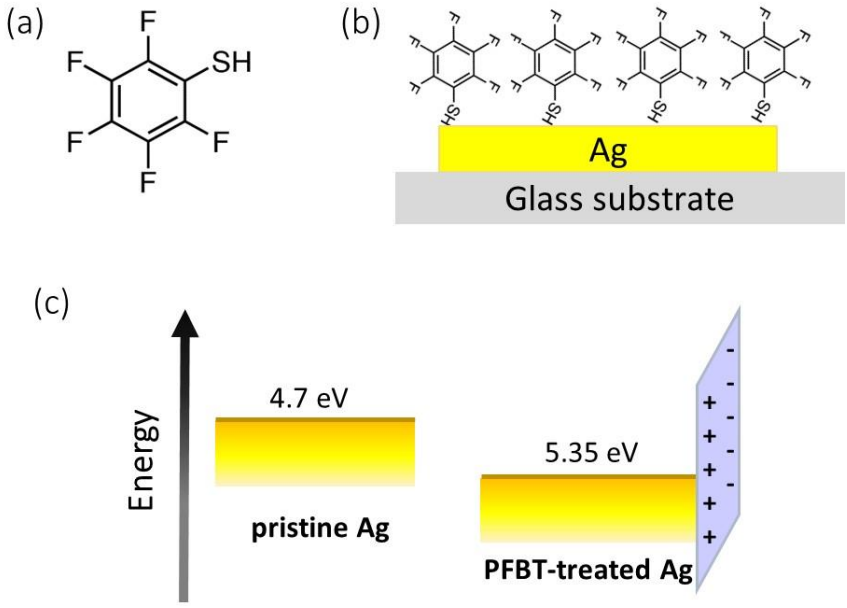


Figure 18. (a) The chemical structure of PFBT. (b) The formation of a PFBT self-assembled monolayer on a silver electrode. (c) The energy levels of a pristine silver electrode and a silver electrode that is modified by a PFBT monolayer.

For PFBT treatment, a 10 mM PFBT solution was prepared first by diluting with ethanol solvent. Before depositing semiconductor films, the substrates with electrodes were immersed in the PFBT solution for 15 min. In this way, a PFBT SAM was created on the surface of electrodes, which were made with Ag in this dissertation, as shown in Figure 18 (b). Then, the samples were rinsed in pure ethanol solvent for 1 min to remove any PFBT residue, followed by thermal annealing at 60 ºC on a hot plate for 5 min. Figure 18 (c) shows that the work function of Ag changed from 4.7 eV to 5.35 eV with the PFBT

treatment since the PFBT SAM created dipoles on the Ag surface and thus increased the work function of Ag. Therefore, the barrier height for hole carriers transporting between a Ag electrode and a p-channel semiconductor film was reduced. Moreover, this PFBT treatment process also improved the wetting properties of substrates, resulting in a better morphology of an organic semiconductor film with highly ordered packing of organic molecules [55].

3.1.4 Deposition of Organic Semiconductors

3.1.4.1 Organic Thin-Film Transistors

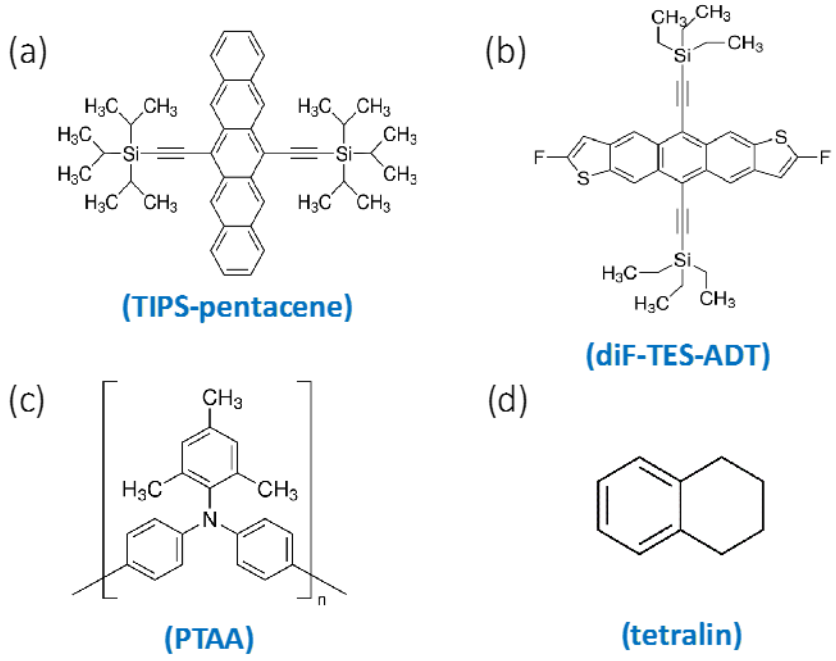


Figure 19. The chemical structures of (a) TIPS-pentacene, (b) diF-TES-ADT, (c) PTAA, and (d) tetralin.

This dissertation focuses on p-channel OTFTs, in which the semiconductor films were fabricated by solution processes with a blend of poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA, Sigma Aldrich) and 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene, Sigma Aldrich), or a blend of PTAA and 2,8-difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diF-TES-ADT, LumTec). To prepare the solution of organic semiconductor layers, a mixture of PTAA with TIPS-pentacene or diF-TES-ADT in a 1:1 weight ratio was dissolved in the 1,2,3,4-tetrahydronaphthalene (tetralin, anhydrous 99%, Sigma Aldrich) solvent for a solution concentration of 30 mg mL^{-1}. The chemical structures of these organic semiconductors and the solvent are shown in Figure 19. Solutions were placed on a magnetic stirrer to stir for more than 12 h in a N_2-filled glovebox before deposition. Then, the TIPS/PTAA or diF-TES-ADT/PTAA solution was filtered with a 0.2 μm polytetrafluoroethylene (PTFE) filter (VWR) and spin-coated at 500 rpm for 10 s with an acceleration of 500 rpm s^{-1} and at 2000 rpm for 20 s with an acceleration of 1000 rpm s^{-1} on substrates, which had PFBT-treated Ag source and drain electrodes, in a N_2-filled glovebox. Then, the samples were immediately moved on a hot plate at 100 ºC and annealed for 15 min. The final thicknesses of the semiconductor films are around 70 nm, which were measured by ellipsometry.

3.1.4.2 Organic Photodiodes

Since the organic photodiode is a part of the OTFT-based organic photodetector, we will discuss the materials that are used in the OPD. The OPD in this dissertation has an inverted structure, which is shown in Figure 20 (a). Figure 20 also shows the chemical

structures of those organic semiconductor materials and solvents that were used to fabricate the OPD devices.

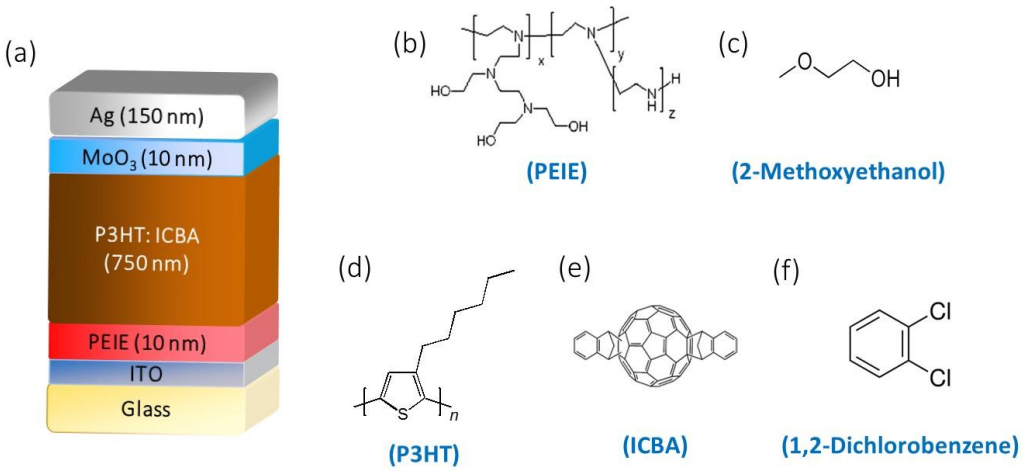


Figure 20. (a) The device structure of an OPD. The chemical structures of (b) PEIE, (c) 2-methoxyethanol, (d) P3HT, (e) ICBA, and (f) 1,2-dichlorobenzene.

A 0.4 wt.% polyethylenimine ethoxylated (PEIE, Sigma Aldrich) solution was prepared in 2-methoxyethanol (Sigma Aldrich) and spin-coated on the ITO substrates at 5000 rpm with an acceleration of 928 rpm s^{-1} for 60 s through a 0.2 μm PTFE filter, followed by thermal annealing at 100 °C for 10 min in air. Then, the PEIE-coated ITO substrates were transferred into a N_2-filled glovebox for the next process. A blend of poly(3-hexylthiophene-2,5-diyl) (P3HT, Rieke Metals) and indene-C_{60} bisadduct (ICBA, Luminescence Technology) in a weight ratio of 1:1 was dissolved in 1,2-dichlorobenzene (Sigma Aldrich) for a total concentration of 100 mg mL^{-1}. The solution was prepared on a hot plate at 70 °C with magnetically stirring at 500 rpm for 12 h inside a N_2-filled glovebox. Then, the P3HT: ICBA solution was spin-coated on top of the PEIE-coated substrates at 800 rpm with an acceleration of 10,000 rpm s^{-1} for 30 s through a 0.2 μm PTFE filter. Then,

the films were transferred in Petri-dishes for solvent annealing for 5 h, followed by thermal annealing on a hot plate at 150 °C for 10 min in a N_2-filled glovebox.

3.1.5 Deposition of Dielectrics

In this work, we fabricated the OTFTs with bilayer gate dielectric structures. Thus, the dielectric layer deposition is a very important step in device fabrication processes. The first dielectric layer was made with a fluoropolymer, which is solution processable, and the second dielectric layer was a metal oxide layer, which was fabricated by atomic layer deposition. Also, different types of metal oxide layers were investigated in this work. The capacitor devices were also fabricated with these dielectric layers to test the properties of dielectrics, such as capacitance densities and leakage currents.

3.1.5.1 Deposition of CYTOP Layers

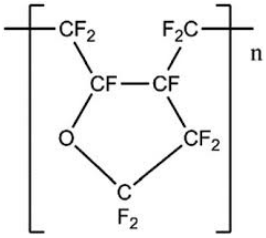


Figure 21. The chemical structure of CYTOP.

The amorphous fluoropolymer, CYTOP, is widely used in organic devices, because of its high transparency, high chemical stability, high hydrophobicity, and good dissolvability in fluorinated solvents that are orthogonal to most organic semiconductor

materials. It also has good mechanical properties [57]. The chemical structure of CYTOP is shown in Figure 21. In this dissertation, the as-purchased 9 wt.% CYTOP (ASAHI GLASS, CTL-890M) was diluted with a fluorine-based solvent (ASAHI GLASS, CT-SOLV180) in a volume ratio of 1:3.5 to have a 2 wt.% CYTOP solution. Then, the CYTOP solution was spin-coated on top of organic semiconductor layers at 3000 rpm for 60 s with an acceleration of 10000 rpm s^{-1}, followed by thermal annealing on a hot plate at 100 ºC for 10 min in a N_2-filled glovebox. The final thickness of the CYTOP film is 35 nm, which was measured by ellipsometry.

3.1.5.2 Atomic Layer Deposition

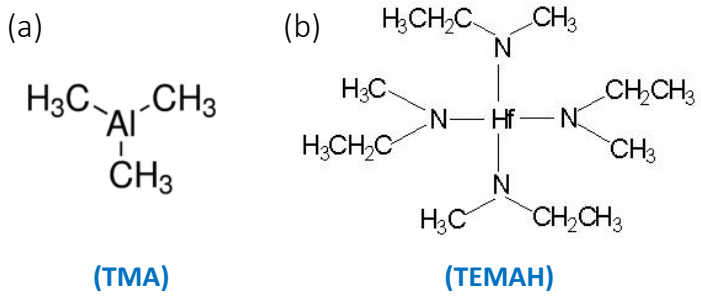
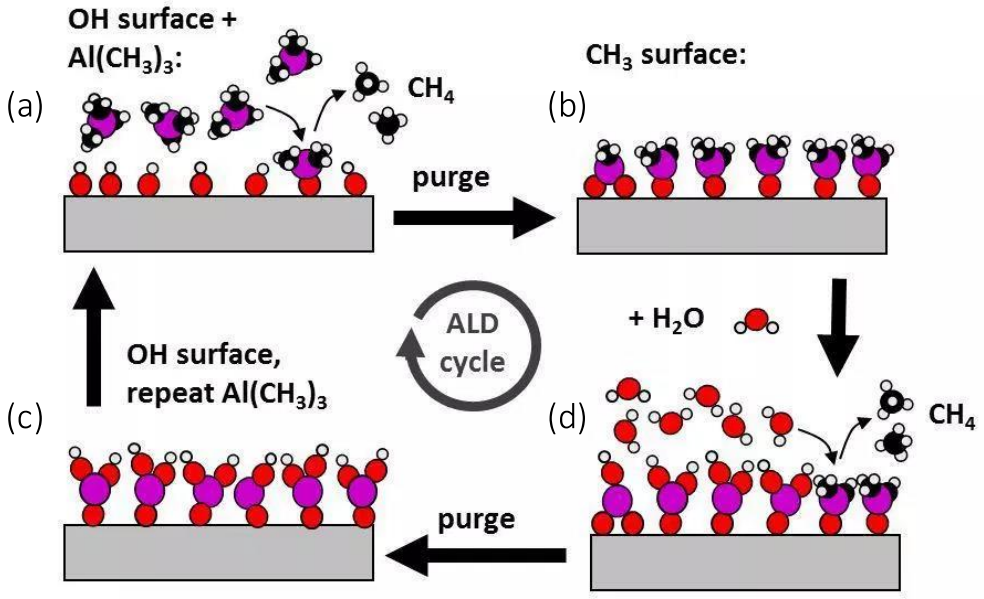


Figure 22. The chemical structures of (a) TMA and (b) TEMAH precursors.

The thin-film metal oxide layers (*i.e.*, Al_2O_3, HfO_2, and Al_2O_3-HfO_2 nanolaminate (NL)) in this work were fabricated in an atomic layer deposition (ALD) system, which is Savannah S200 ALD from Ultratech Inc. (Cambridge NanoTech Inc.). The principle of ALD is similar to that of chemical vapor deposition (CVD) except that the reaction of ALD breaks the CVD reaction into two reaction-steps, keeping the precursor materials separated

during the reaction. The process of ALD starts from a pulse of water vapor and then a pulse of a metal-organic precursor in this work. Figure 22 shows the chemical structures of the metal-organic precursors that are used in this work; they are trimethylaluminum ($Al(CH_3)_3$, TMA) for Al_2O_3 and tetrakis(ethylmethylamido)hafnium ($[(CH_3)(C_2H_5)N]_4Hf$, TEMAH) for HfO_2.



$$2\times Al(CH_3)_3 + 3\times H_2O \rightarrow Al_2O_3 + 6\times CH_4$$

Figure 23. An illustration of the atomic layer deposition of aluminum oxide via TMA and water.

Figure 23 shows an example of the ALD process for Al_2O_3 deposition, which is deposited by cycling pulses of TMA and water in the chamber. The chemical reaction during the deposition follows the formula shown in Figure 23. The process of one layer of Al_2O_3 deposition is described as follows. First, a pulse of water vapor flows in the chamber of the ALD system, and the water vapor is absorbed on the substrate surface and form hydroxyl groups. Then another pulse of the precursor, $Al(CH_3)_3$, flows in the chamber and

interacts with the hydroxyl groups (-OH) forming bondings between oxygen atoms of hydroxyl groups and aluminum atoms of $Al(CH_3)_3$ molecules. In the meanwhile, a methyl group ($-CH_3$) in an $Al(CH_3)_3$ molecule forms a bonding with a hydrogen atom from a hydroxyl group to yield a by-product, methane (CH_4) (see Figure 23 (a)). Then, the by-products are removed from the chamber by evacuating, leaving a layer of Al_2O_3 on the surface (see Figure 23 (b)). After forming a layer of Al_2O_3, another pulse of water vapor is introduced in the chamber. The water molecules are adsorbed on aluminum atoms. The oxygen atoms of water molecules bond with aluminum atoms by replacing all methyl groups that connect to aluminum atoms (see Figure 23 (c)). Then, the by-products are removed by evacuating again, and the surface is ready for the next cycle of deposition (see Figure 23 (d)). In this way, a metal oxide dielectric layer is formed through the repeated cycles as described above, and its thickness can be precisely controlled at a level of 0.1 nm (or atomic scale) by setting the number of cycles.

3.1.6 PDMS Masks Preparation

During the fabrication of the photodetector in a lateral structure, the OTFT area and the OPD area were covered by masks, respectively. These masks were made with poly(dimethylsiloxane) (PDMS). To fabricate the PDMS masks, the solution of base and agent (Gelest OE^{TM} 41) in a weight ratio of 1:1 was thoroughly mixed first. Next, the mixture was gently poured onto a flat glass mold without any trapped air bubbles and then cured at 80 °C for an hour under atmospheric pressure. The thickness of the PDMS film was around 0.1 cm. After cooling down, the PDMS film was formed and could be peeled

off. The peeled PDMS film was cut into the desired sizes of 1.5” x 1.3” and 1.5” x 0.7” for covering the OTFT area and OPD area, respectively, during the spin-coating process.

3.2 Characterization

3.2.1 Ellipsometry for Film Thickness Measurement

Ellipsometry is an optical technique for characterizing the properties of thin films by measuring the changes in polarization as light reflects or transmits from a material structure. It is primarily used to determine the thickness of a thin film (*i.e.*, dielectric and semiconductor films). The ellipsometry results usually depend on the optical properties of materials and the thicknesses of films. In this work, reflectance or transmittance data were measured by a spectroscopic ellipsometer (J.A. Woollam M-2000UI), and then acquired and modeled by the software CompleteEASE^{TM} (J.A. Woollam).

To measure the thickness of a thin film, the transmittance of the film is typically measured firstly. Since the sum of transmittance, reflectance, and absorption equals to one, we approximate that absorption of the film equals to one minus the transmittance of the film, assuming that the reflectance is negligible when measuring the transmittance of the film. For a material having little absorption at the range of the ellipsometer spectrum, a Cauchy model is used to fit the measured reflectance data and calculate the thickness of the film, such as metal oxide layers and CYTOP films. For a material having strong absorption at partial of the wavelength range, such as a P3HT semiconductor film, the

Cauchy model still can be used to fit the measured reflectance of the film at the non-absorption wavelength range.

3.2.2 Kelvin Probe

Kelvin probe is based on a vibrating capacitor and is usually used to measure the work functions of conducting materials, the Fermi level energies of organic semiconductor films or the surface potentials of the non-conductive films between a conducting specimen and a vibrating tip. Figure 24 shows the operating principle of a Kelvin probe, which measures the contact potential difference (CPD) between the work functions of a sample (φ_s) and a reference tip (φ_t).

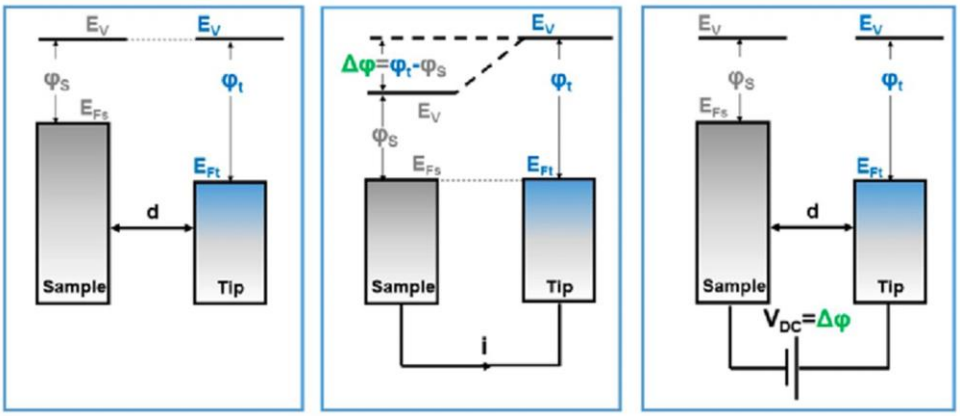


Figure 24. The operating principle of a Kelvin probe [58].

Figure 24 (a) shows that the tip and the sample are separated by a distance d with no electrical contact, creating a parallel plate capacitor. When the tip and the sample are in electrical contact, as shown in Figure 24 (b), the potential between these two surfaces is the contact potential difference ($V_{CPD} = \frac{\varphi_t - \varphi_s}{-e}$), where e is the elementary charge. If an

applied external bias (V_{DC}) has the same magnitude as V_{CPD} with the opposite direction, as shown in Figure 24 (c), the applied voltage eliminates the surface charge in the contact area. Thus, this V_{DC} is equal to the potential difference between the tip and the sample; the work function of the sample can be calculated when the work function of the tip is known. Before each measurement in this work, the Kelvin probe was calibrated with a freshly cleaved highly ordered pyrolytic graphite (HOPG) sample, which has a known work function of 4.6 eV.

3.2.3 Probe Stations for Devices Measurement

Two probe stations were used in the measurement setup in this work. For the characterization of most organic semiconductor devices, we used a Lucas-Signatone H100 series probe station, which consisted of a device stage with four inches of X-Y travel, three micromanipulators that control the positions of probes in three axes, and a microscope tower that provides a 3-dimensional image at a fixed position. The probe station placed on a portable air table to reduce the vibration in a N_2-filled glovebox (MBRAUN LabMaster 130), in which both O_2 and H_2O values were maintained below 0.1 ppm so that the performance of organic semiconductor devices would not be affected by oxygen and moisture. For device environmental stability study, we used another probe station (Rucker and Kolls model 260 probe station), which is designed and built for maximum mechanical stability and placed in air. This probe station also incorporated a device stage with X-Y positioning, micromanipulators, and a microscope tower.

3.2.3.1 Current Measurement

A two-channel source-monitor unit system (Agilent E5272A) was connected to one of the probe stations and used for multiple types of current-voltage characterization. Different LabView programs were designed to control the Agilent system to implement different tests and collect the data. In this study, the device characterizations that were measured by Agilent E5272A are:

- for OTFTs: transfer and output curves measurement, and dc-bias stress tests.
- for capacitors: leakage current measurement.
- for photodetectors: dark current and light current measurement.

3.2.3.2 Capacitance Measurement

For the characterization of capacitors, one of the probe stations was connected to a precision LCR meter (Agilent 4284A), which features a wide test frequency range from 20 Hz to 1 MHz with an adjustable dc bias. The capacitance densities of gate dielectrics were obtained by measuring and linear-fitting the capacitance values of the capacitors that had six different areas, ranging from 0.01 cm^2 to 0.38 cm^2.

Besides the leakage current of a capacitor, another two methods were used to evaluate the quality of a capacitor. The first method is to measure the capacitance of a capacitor as a function of applied dc voltages at a fixed frequency. In this case, the stability of the capacitance would be evaluated at a range of dc biases. The second method is to measure the capacitance as a function of frequencies at zero bias, and the quality of a

capacitor would be evaluated by the cut-off frequency since the capacitance is usually unstable at high frequency.

3.2.4 Optical Source for Photodetector Measurements

The light source for photodetector measurement was selected based on the light absorption range of a P3HT: ICBA organic semiconductor layer, which had strong absorption at the wavelength below 640 nm. In this work, a 635-nm laser (fiber-coupled Fabry-Perot benchtop laser, S1FC635) was used as the light source for the measurement of optical characteristics of a photodetector. The laser transmitted through an optical fiber and illumined on the device from the backside. The illumination area was confined in the active area of the photodetector. For the light response measurement, different optical powers were needed to study the optical responsivity of a photodetector at different light intensity. The output optical power of this laser is adjustable, and the maximum value is 2.5 mW. For an accurate characterization, the optical power of the laser was calibrated by a laser power and energy meter (OPHIR, Nova II).

CHAPTER 4. ORGANIC THIN-FILM TRANSISTORS WITH IMPROVED STABILITY

As discussed in Chapter 1, the charge mobility values of the state-of-the-art polycrystalline (small molecule) or nearly amorphous (conjugated polymer) OTFTs in academic research now have surpassed those found in *a*-Si: H TFTs and *a*-oxide TFTs [31, 33, 59]. However, the stability of OTFTs remains inferior to that of inorganic counterparts. The poor stability in long operating time and different environmental conditions (*i.e.*, oxygen, moisture, and high temperature) is a key point of concern towards the commercial deployment of OTFTs [15, 60]. This chapter describes the improvement of OTFT stability through the optimization of the OTFT structure, which has an ultra-thin bilayer gate-dielectric that consists of an amorphous fluoropolymer CYTOP layer and an Al_2O_3: HfO_2 nanolaminate (NL). This structure enables low operating voltages as well as high operational and environmental stability of polycrystalline OTFTs. This improved device operational stability shows that OTFTs could achieve the level of performance that is required for commercial applications.

4.1 Introduction

4.1.1 Origin of Instability of Organic Thin-Film Transistors

In most TFT systems, including organic or inorganic TFTs, the primary mechanism behind device instability arises from the trapped charge carriers or molecular species (such as oxygen or water) at either intrinsic structural defects or extrinsic impurities of devices.

These localized trapping sites could be pre-existing or stress-generated, and they might locate at microcrystalline boundaries of the semiconductor layer, nanometer-sized voids (due to porosity) of the semiconductor or dielectric layer, or at the semiconductor-dielectric interface [38, 61]. The total amount of charge carriers in a TFT is determined by the applied gate voltage. Once any of these charges are trapped, they will turn into fixed charges and cannot contribute to the channel current, but they are still part of the charges induced by the gate voltage. In addition, the trapped charges would build an electric field that has to be compensated by the gate voltage before the formation of the accumulation layer at the channel. As a result, when more charges are trapped, a higher gate voltage is needed to maintain the same mobile charge concentration and channel current.

Therefore, the instability of devices is usually described by the change of the source-to-drain current at specific voltages or the shift of the threshold voltage as a function of stressing time. These electrical characteristic changes would be observed when the device is stressed with a constant dc bias or an alternating voltage signal applied at the gate, source, and drain electrodes for a prolonged time. Also, these changes could be observed when the device operates at some severe environmental conditions, such as high temperature and high humidity. Especially, some organic semiconductors, such as pentacene and P3HT, exhibit fast degradation when they are exposed to certain atmospheric species (*i.e.*, oxygen and moisture) and light.

A common way to study the operational instability of TFTs with electrical bias tress is stressing the device with a constant voltage for a prolonged period. In order to observe the changes of transistor characteristics with stress, the stress is interrupted by the quick measurement of transfer curves at short time intervals. The shift of V_{TH} could be extracted

from these transfer curves. Since the shift of V_{TH} is dominated by charge trapping effect in operation, the shifting level depends on the number of trapped charges. If we assume that the trapped charge density is N_{tr}, the threshold voltage shift (ΔV_{TH}) is given by $\Delta V_{TH} = eN_{tr}/C_{ox}$, where e is the elementary charge and C_{ox} is the capacitance density of the gate dielectric layer. The charges trapping rate depends on the free carrier density (N_f). For an exponential distribution of trap states, the charge trapping rate is given by [62]:

$$\frac{dV_{TH}}{dt} \propto \frac{dN_{tr}}{dt} \propto N_f(t)\frac{t^{\beta-1}}{\tau^{\beta}} \tag{11}$$

where τ is a characteristic time constant and β is a dispersion parameter ($0 < \beta < 1$). By solving Equation (11) with the boundary condition that the value of V_{TH} at infinite stress time equals to the gate voltage, the stretched-exponential decay for the threshold voltage with time is given by [63]:

$$\Delta V_{TH,1}(t) = \Delta V_{TH,1\infty} \cdot \left\{1 - \exp\left[-\left(\frac{t}{\tau_1}\right)^{\beta_1}\right]\right\} \tag{12}$$

where $\Delta V_{TH,1\infty} = \left[V_{TH,1}(\infty) - V_{TH}(0)\right]$. The number "1" in the subscript of each parameter represents the parameter due to the charge trapping effect, which will be different from the other effect in the following discussion. In addition, we refer to this model as the single-stretched exponential (SSE) model in this work.

In a conventional OTFT with a single gate dielectric layer, the shift of V_{TH} due to the operating voltage bias stress follows the SSE model, as described by Equation (12). For example, Figure 25 (a) shows a typical device structure of a p-channel OTFT that has a single gate dielectric layer and a PTAA semiconductor layer. Figure 25 (b) shows the

device transfer curves measured before and after stressing the device with a constant gate bias voltage of –20 V for different stress periods. The transfer curve shifts to negative voltages with the bias stress. This bias stress effect is further quantified by ΔV_{TH} as a function of time, as shown in Figure 25 (c). The value of $|V_{TH}|$ increases continuously with the bias tress and the shifts of $|V_{TH}|$ exceed more than 17 V after a 100-h bias stress test. Moreover, the solid curve shows that the tendency of ΔV_{TH} with the stress time is well fitted with Equation (12). The fitting parameters are $\Delta V_{TH,1\infty}$= 19 V, τ_1 = 10^4 s, and β_1= 0.43.

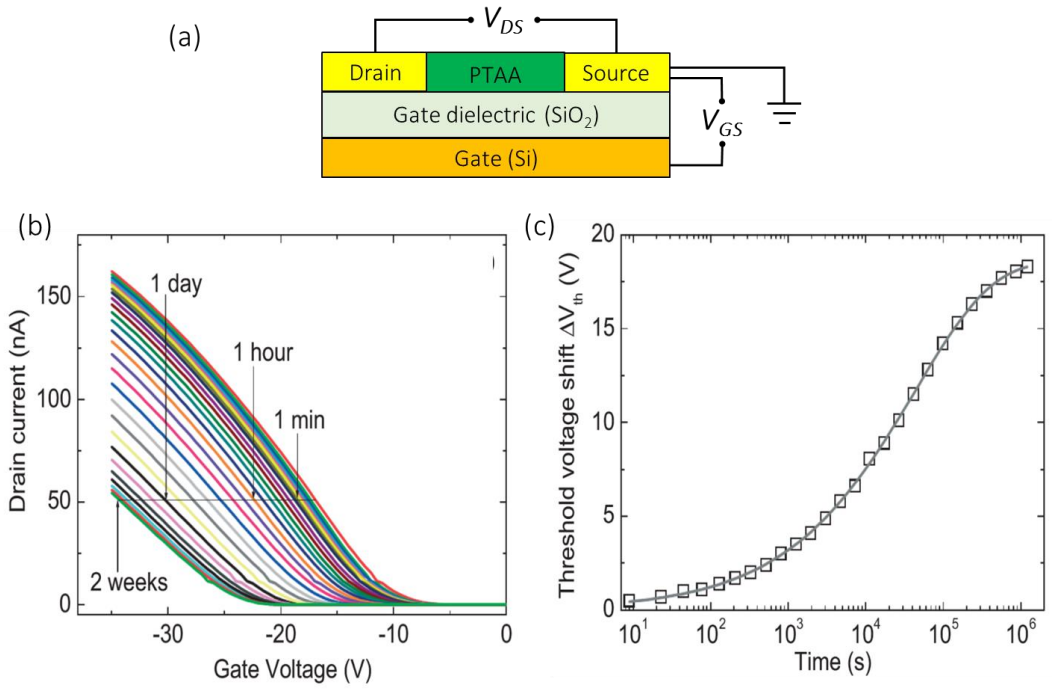


Figure 25. (a) The device structure of a bottom-gate p-channel OTFT with a single gate dielectric layer. (b) Transfer curves of OTFT as a function of stress time. (c) The ΔV_{TH} obtained from (b) presented as a function of stress time on a logarithmic scale (scatter symbols). The solid line shows a fit with Equation (12) [64].

4.1.2 Previous Progress

In recent years, many approaches to reduce or passivate the trap sites are developed, including the use of post-processing thermal annealing [65], molecular additives [60], and amorphous fluoropolymers (*e.g.*, CYTOP) as gate dielectric layers [66]. Despite progress, only in the absence of crystalline boundaries and porosity, such as in single-crystal OTFTs (*sc*-OTFTs), have OTFTs been shown able to exhibit superior V_{TH} stability than *a*-Si: H TFTs [17]. However, their V_{TH} stability remains inferior to that achieved by other commercial TFT technologies such as μc-Si, *a*-oxide TFTs, and *poly*-Si TFTs, which exhibit the most stable performance of all TFT technologies [67].

4.1.2.1 Bilayer Gate Dielectrics: CYTOP/Al_2O_3

In the past, our previous group members have shown that an alternative approach exists to significantly improve the environmental and operational stability of OTFTs [18, 38]. This approach consists of using a bilayer gate-dielectric (*e.g.*, CYTOP and metal-oxide) instead of the commonly used single-layer gate-dielectric (*e.g.*, CYTOP or metal-oxide). Figure 26 (a) shows the device structure of an OTFT using a bilayer gate dielectric that consists of a CYTOP layer and an Al_2O_3 layer deposited by ALD. Figure 26 (b) shows that the channel current changes of the OTFT with a bilayer gate dielectric are much smaller than those of the OTFT with a single CYTOP layer or a single Al_2O_3 layer of gate dielectric when the device is under continuous dc-bias stress for 1 h. In addition, in the bilayer gate-dielectric structure, the second dielectric layer is engineered to compensate for the shift of V_{TH} caused by the carriers trapping effect, since it introduces a second

mechanism that produces an opposite V_{TH} shift (*e.g.*, charge accumulation within the dielectric layer by slowly oriented dipoles). For example, Figure 26 (c) shows that the drain current changes during the bias stress test for 24 h on an OTFT with a bilayer gate dielectric that consists of a 40 nm CYTOP layer and a 50 nm Al_2O_3 layer. The OTFT shows good operational stability with less than 5% changes of channel current after 24 h stressing.

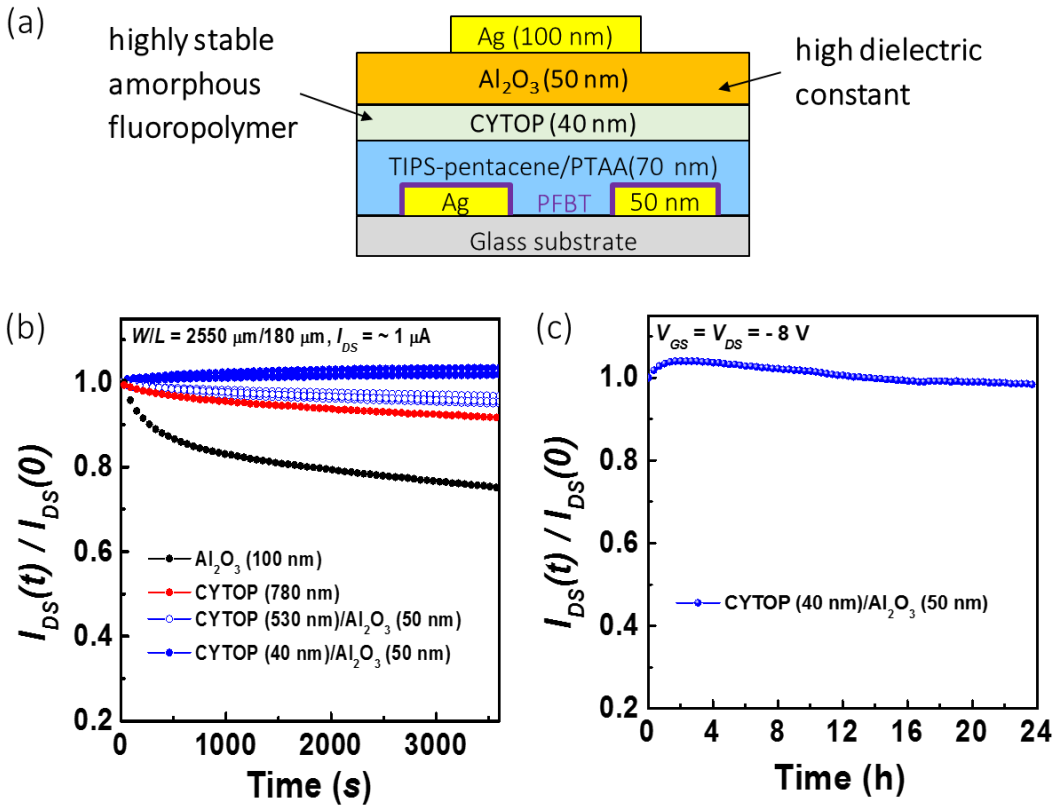


Figure 26. (a) The structure of top-gate TIPS-pentacene/PTAA OTFTs with gate dielectric layers of CYTOP/Al_2O_3. (b) The temporal evolutions of the normalized drain currents of OTFTs with different gate dielectric layers during the bias stress tests for 1 h. (c) The temporal evolution of the normalized drain current during the bias stress test for 24 h on an OTFT with a bilayer gate dielectric that consists of a 40 nm CYTOP layer and a 50 nm Al_2O_3 layer [38].

Specifically, the previous study has shown that when the second gate dielectric layer comprises a single metal-oxide layer processed by ALD (*e.g.*, Al_2O_3), *n*-channel and *p*-

channel OTFTs have good operational stability, and excellent environmental stability when operating at low voltages. For example, the devices remain functional after being subjected to oxygen plasma for several minutes and being immersed in water for several hours [16].

4.1.2.2 Bilayer Gate Dielectrics: CYTOP/Al_2O_3/NL

Furthermore, the previous group member, Cheng-Yin, found that when the second gate dielectric layer on the CYTOP layer consists of a first Al_2O_3 layer and a second nanolaminate layer comprising nanometer-thick alternating layers of Al_2O_3 and HfO_2 by ALD, as shown in Figure 27 (a), OTFTs can even sustain being immersed in water at 95 ^oC for tens of minutes [15]. Figure 27 (b) shows that all of the OTFTs having CYTOP/Al_2O_3 bilayer gate dielectric are completely damaged after immersing in water at 95 ^oC for 3 min. However, 50% of the OTFTs having Al_2O_3: HfO_2 NL in dielectric remain functional after being immersing in water at 95 ^oC for more than one hour. Therefore, the NL is a high-quality dielectric layer that effectively passivates the semiconductor layer in an OTFT.

In this work, we used the approach of the OTFTs with bilayer gate dielectrics that have been built in our group. We demonstrated that the OTFT with an optimized bilayer gate dielectric, which consisted of a first CYTOP layer and a second Al_2O_3: HfO_2 NL layer by ALD, exhibited not only improved environmental stability but also unprecedented operational stability. The V_{TH} shifts in these OTFTs over prolonged dc-bias stress time are comparable, or smaller than the ones reported in *a*-Si and *a*-oxide TFTs. Furthermore, the small V_{TH} shifts displayed by these OTFTs are weakly dependent on temperature variations

at least up to 50 °C above room temperature, thus highlighting the robustness of this approach [68].

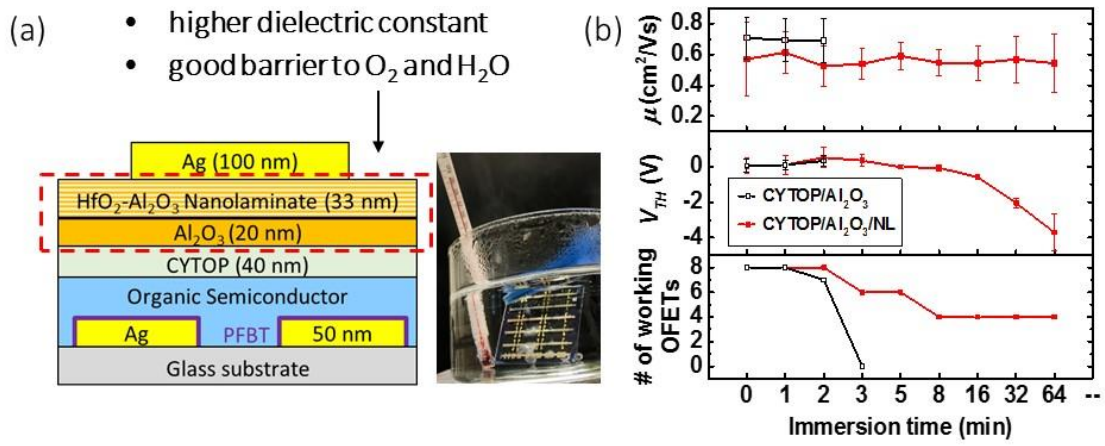


Figure 27. (a) The structure of top-gate TIPS-pentacene/PTAA OTFTs with gate dielectric layers of CYTOP/Al_2O_3/NL. (c) Charge mobilities, threshold voltages, and the number of working OTFTs with the immersion time in water at 95 °C. [15].

4.2 Device Fabrication

In this work, the TIPS-pentacene/PTAA OTFTs using two types of gate dielectric geometries were fabricated with different NL thicknesses, to investigate the influence of the NL thickness on the electrical properties and stability of the OTFTs. The device geometries are shown in Figure 28 (b) and (c). The samples with different dielectric layers were divided into two groups, which are referred to as group A (sample A_33, A_27, and A_22) and group B (sample B_44, B_22, and B_11). For group A, the gate dielectric layer consists of a CYTOP (35 nm) layer and an Al_2O_3: HfO_2 NL (varied thicknesses) by ALD. For group B, the gate dielectric layer of OTFTs consists of a CYTOP layer (35 nm) and

metal oxide layers, which are an Al_2O_3 layer (20 nm) and an Al_2O_3: HfO_2 NL (varied thicknesses) by ALD. Here, we name the devices with the letter "A" or "B", which indicates a specific device geometry, followed by "_#", which indicates the thickness of NL. The thicknesses of dielectric layers for each sample are described in Figure 28 (b) and (c).

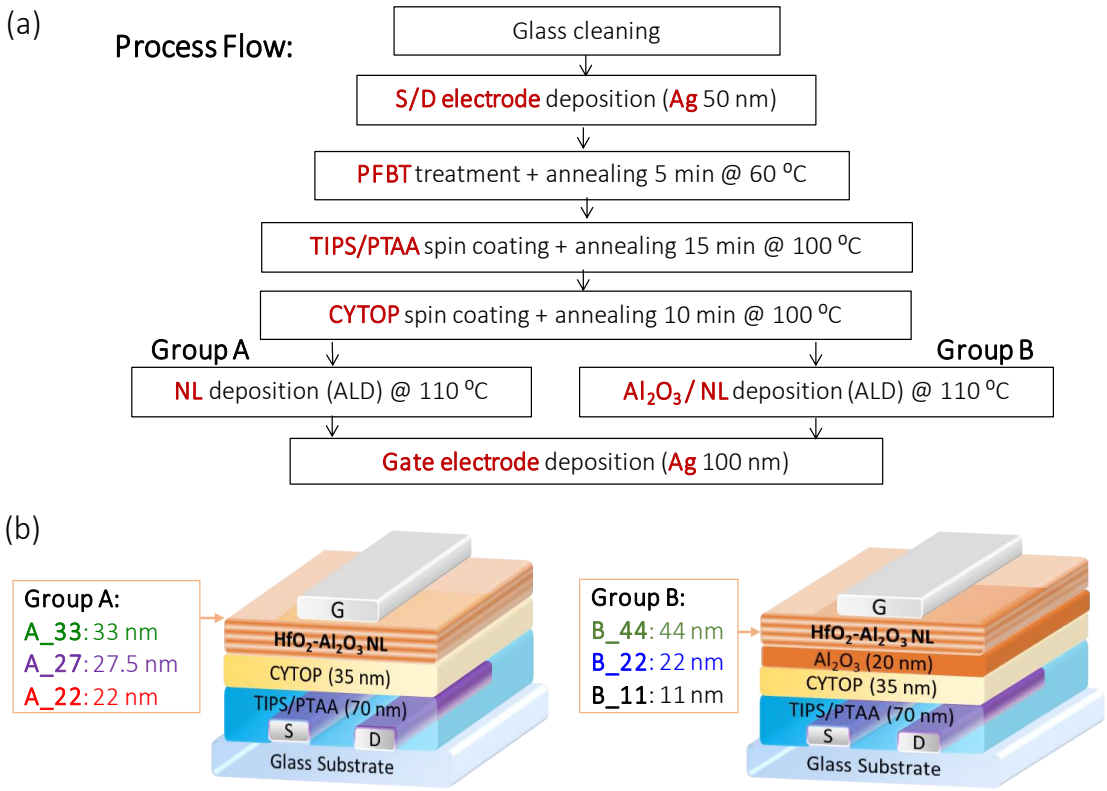


Figure 28. (a) Process steps of device fabrication. The structures of top-gate TIPS-pentacene/PTAA OTFTs with gate dielectric layers of (b) CYTOP/ALD Al_2O_3: HfO_2 NL (for group A), and (c) CYTOP/ALD Al_2O_3/ALD Al_2O_3: HfO_2 NL (for group B).

Figure 28 (a) shows the fabrication process flow of the OTFTs in group A and group B. All of the OTFTs with CYTOP/metal oxide as bilayer gate dielectrics are fabricated on glass substrates. After solvent cleaning step, the source and drain electrodes were deposited on the glass substrate by thermal evaporating a 50-nm thick Ag layer

through a shadow mask. Then the substrate with source and drain electrodes was treated with a PFBT solution to form a self-assembled monolayer of PFBT on the Ag electrodes. After the PFBT treatment, a 70-nm thick semiconductor layer of TIPS/PTAA was deposited by spin-coating on the substrate, followed by the deposition of a 35-nm thick CYTOP film. For each sample in group A, after CYTOP deposition, an Al_2O_3-HfO_2 NL was deposited in the ALD system by alternating 5-cycles of Al_2O_3 and 5-cycles of HfO_2 for 30 times (A_33), 25 times (A_27), and 20 times (A_22) at 110 ºC, producing films of 33 nm, 27.5 nm, and 22 nm, respectively. For each sample in group B, a 20-nm thick Al_2O_3 was deposited as a nucleation layer first; then an Al_2O_3-HfO_2 NL was deposited on top of the nucleation layer at 110 ºC in ALD chamber. The NL was deposited by alternating 5-cycles of Al_2O_3 and 5-cycles of HfO_2 for 40 times (B_44), 20 times (B_22), and 10 times (B_11), generating the films of 44 nm, 22 nm, and 11 nm, respectively. Finally, a 100-nm thick Ag layer was thermally evaporated through a shadow mask, forming the gate electrodes on the metal oxide layers.

4.3 Current-Voltage Characteristics

The pristine transfer characteristics of champion OTFTs (W/L = 2550 µm/180 µm) of samples in group A and group B are shown in Figure 29 (a) and (b), respectively. All devices were measured in an N_2-filled glovebox and exhibited hysteresis-free electrical characteristics. Table 1 shows a summary of the statistical values of the electrical parameters measured on the pristine OTFTs of all types. The charge mobility (μ), the threshold voltage (V_{TH}), and the absolute value of subthreshold swing ($|S|$) were extracted

from transfer curves. The maximum semiconductor-dielectric interfacial trap density was estimated using the values of $|S|$ [53]. All OTFTs in group A and group B have the similar maximum interfacial trap densities around 3.2×10^{12} cm^{-2}, which is consistent with the fact that CYTOP is coated on semiconductor layer as the first dielectric layer for all devices. The electrical parameters of OTFTs in group A and group B are comparable to those measured in other TIPS-pentacene/PTAA-based OTFTs having CYTOP/ALD-oxide gate dielectrics [15, 38].

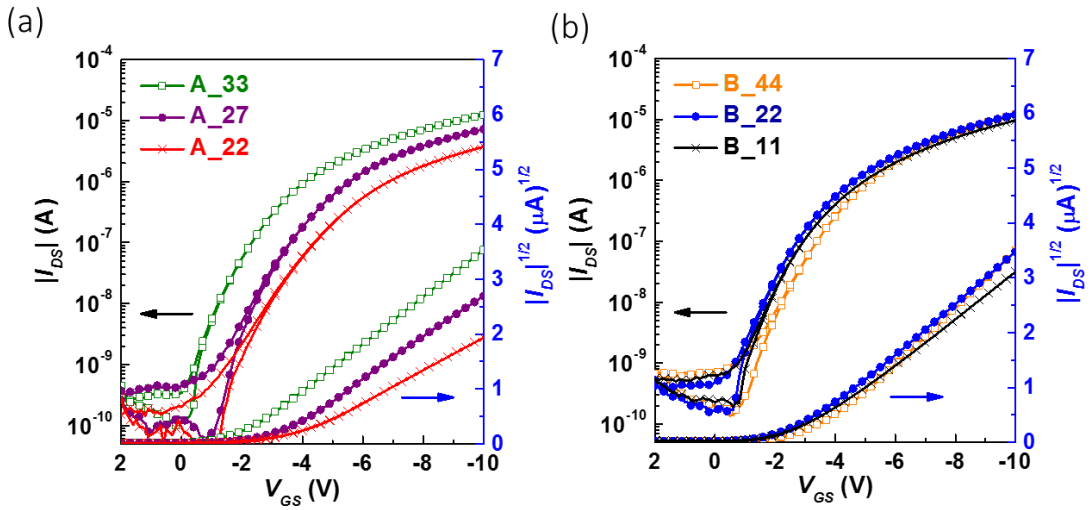


Figure 29. Pristine transfer characteristics of (a) group A devices and (b) group B devices.

Figure 30 shows the statistic values of μ and V_{TH}. The trends shown by μ and V_{TH} can be attributed to the differences in the gate-dielectric geometry and thickness; since the trap densities at the semiconductor-dielectric interfaces were the same. As the gate dielectric thickness is decreased, μ decreased from 0.8 cm^2 V^{-1} s^{-1} to 0.2 cm^2 V^{-1} s^{-1} for group A, and from 0.7 cm^2 V^{-1} s^{-1} to 0.5 cm^2 V^{-1} s^{-1} for group B. The thicker dielectric layers lead to the smaller leakage currents from channel to gate (see Figure 31), therefore,

the higher channel current between source and drain will be measured, resulting in higher calculated values of μ. By adjusting the thickness of the dielectric layer, we found that A_33 with 33 nm NL showed relatively small V_{TH} and high μ. This result also indicates that the layer-by-layer nanolaminate structure might have a denser configuration that leads to much lower leakage than a single Al_2O_3 layer for the same thickness.

Table 1 Summary of the device pristine electrical parameters.

Sample Name	C_{ox} (nF cm^{-2})	μ (cm^2 V^{-1} s^{-1})	V_{TH} (V)	$\lvert S \rvert$ (V decade^{-1})	Est. Max. Trap Density (cm^{-2})	# of Devices
A_33	40.8	0.8 ± 0.1	-1.9 ± 0.2	0.70 ± 0.04	2.7×10^{12}	23
A_27	42.5	0.4 ± 0.1	-2.6 ± 0.2	0.77 ± 0.03	3.2×10^{12}	17
A_22	43.1	0.2 ± 0.1	-3.0 ± 0.5	0.93 ± 0.03	3.9×10^{12}	11
B_44	36.2	0.7 ± 0.1	-3.0 ± 0.8	0.75 ± 0.03	2.6×10^{12}	9
B_22	40.7	0.6 ± 0.1	-2.7 ± 0.4	0.79 ± 0.02	3.1×10^{12}	12
B_11	42.2	0.5 ± 0.1	-2.8 ± 0.3	0.80 ± 0.02	3.3×10^{12}	5

To investigate this hypothesis, we measured the leakage current density against the electric field for each type of dielectric layer. As shown in Figure 31, the thicker dielectric layers lead to the smaller leakage current densities. The leakage current densities of A_33, which is lower than 5×10^{-8} A cm^{-2} at applied fields up to 3 MV cm^{-1}, are as low as those of B_44 and B_22.

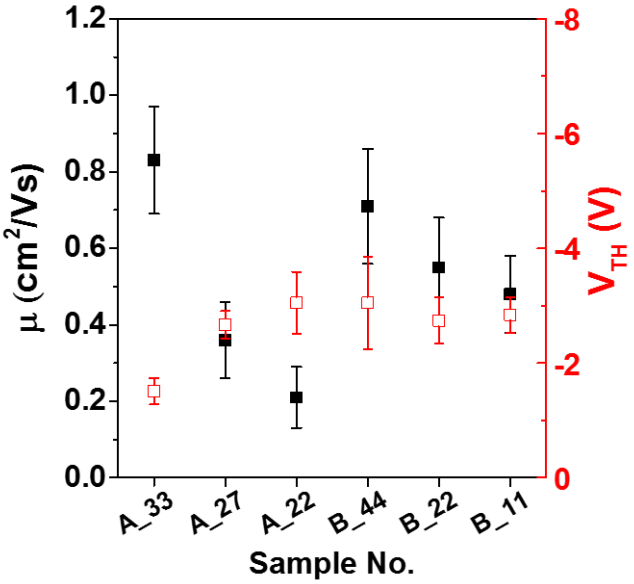


Figure 30. Statistic values of charge mobility and threshold voltages of OTFTs.

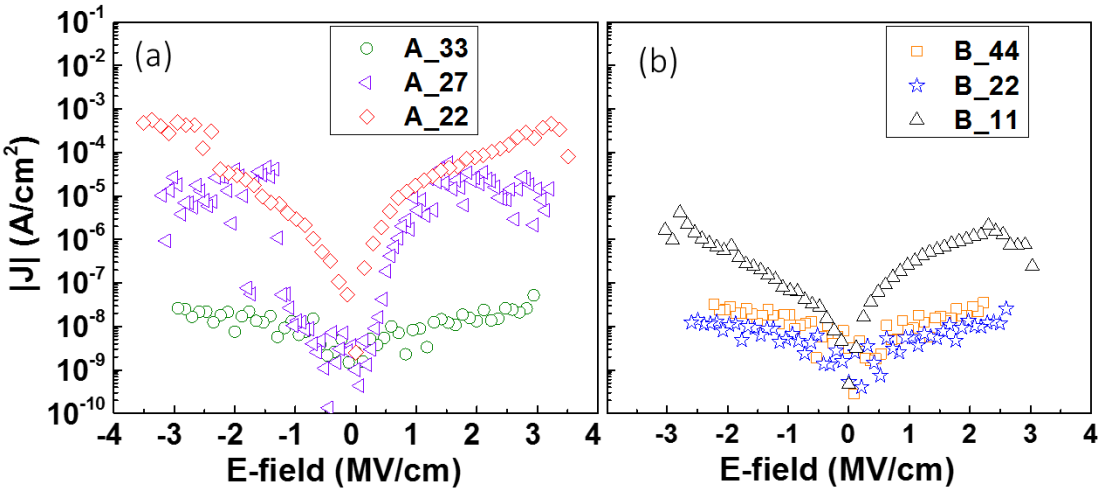


Figure 31. Current density-electric field (*J-E*) characteristics of dielectric layers of OTFTs in (a) group A and (b) group B.

4.4 Environmental Stability

In the past, we have shown that OTFTs with CYTOP/Al_2O_3/NL gate-dielectric layers (*i.e.*, B_44 OTFTs) exhibit superior environmental stability (when immersed in near-boiling water) than those with a CYTOP/Al_2O_3 gate dielectric [15]. Here we compare the environmental stability of A_33 and B_44 OTFTs, which showed the best characteristics in group A and B, respectively. We evaluated the temporal changes in the source-to-drain current during on-state gate bias stress experiments for one hour (*i.e.*, while OTFTs were subjected to constant bias stress in the saturation regime V_{DS} = V_{GS} = -10 V), after exposing all devices to the environmental conditions discussed below. First, the samples were kept in air at room temperature (RT, ca. 27 ºC) with a relative humidity (RH) of 35% for 24 h, and then they were transferred into a N_2-filled glovebox for bias stress testing. Second, the samples were immersed in distilled water for 16 h and subjected to another bias stress test. Last, the samples were vacuum annealed at 100 ºC for 16 h and subjected to a bias stress test again.

Figure 32 (b) and (c) show the temporal evolution of normalized I_{DS} (*i.e.*, $(I_{DS}(t)/I_{DS}(0))$ measured with A_33 and B_44 OTFT devices for all environmental conditions. After air exposure, the I_{DS} changes of less than 1% were observed in both A_33 and B_44 OTFTs. The prolonged immersion in water (16 h) resulted in larger changes of I_{DS} in both B_44 and A_33 OTFTs. Remarkably, after 1 h of bias stress, devices A_33 exhibited significantly smaller changes of I_{DS} (ca. 4%) than those observed on devices B_44 (ca. 20%). The performance of both types of devices recovered after the samples were annealed at 100 ºC for 16 h.

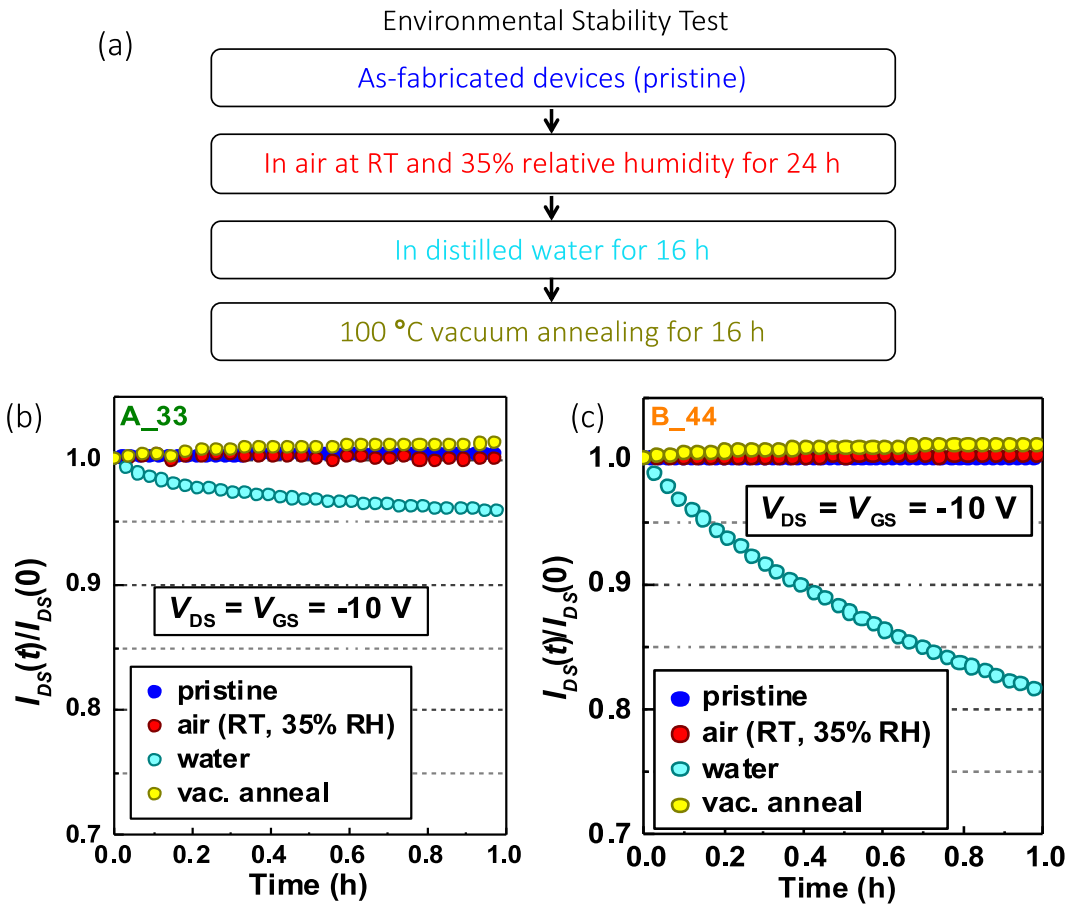


Figure 32. (a) The sequence of OTFTs exposure to different environmental conditions. The environmental stability of (b) A_33 devices and (c) B_44 devices under continuous dc-bias stress for OTFTs after exposing to different ambient conditions.

These general trends are fully consistent with our previous reports on the environmental stability of top-gate OTFTs, and in particular, on the detrimental effect that prolonged immersion in water produces on the I_{DS} stability. For instance, OTFTs having a CYTOP/ALD Al_2O_3 gate dielectric exhibited ΔI_{DS}(10 min) > 10% after immersion in water for 16 h [16], a significantly larger $\Delta I_{DS}(t)$ than those in A_33 and B_44 OTFTs in this work. Hence, while it is clear that water absorbed during prolonged exposure leads to the formation of traps and degradation of the device stability under continuous bias stress,

the presence of single ALD Al_2O_3 layers in the architecture of an OTFT (*e.g.*, B_44 OTFT) also correlates with an increased sensitivity to the presence of water in the environment. Therefore, the A_33 OTFT not only has a simpler device architecture compared with the B_44 OTFT but also has superior environmental stability.

In addition to the environmental tests above, a damp heat test was conducted to assess the stability performance of the A_33 and B_44 OTFTs when exposed to a high-temperature and high-humidity condition, which would accelerate the device degradation [69]. One of the typical damp heat test conditions is known as 85/85, meaning 85 °C and 85% of relative humidity [70]. The A_33 and B_44 OTFT devices that were used in this test were fabricated 18 months prior to the current testing, and they were stored in a N_2-filled glovebox. Although the OTFTs were stored in a N_2-filled glovebox, over a period of 18 months, they absorb small amount of moisture that is known to change the electrical properties of devices under constant bias stress. Hence, we did the vacuum thermal annealing on A_33 and B_44 OTFTs before exposing the devices to the 85/85 condition. All devices were subject to the following experimental conditions: first, the samples were vacuum annealed at 100 ºC for 16 h and subjected to bias stress test; then the samples were kept in air at 85 ºC and 85-90% of relative humidity for 24 h, and they were transferred into a N_2-filled glovebox for bias stress testing; then the samples were vacuum annealed at 100 ºC for 16 h and subjected to another bias stress test.

Figure 33 (b) and (c) show the temporal evolution of normalized I_{DS} (*i.e.*, $(I_{DS}(t)/I_{DS}(0))$ measured with A_33 and B_44 OTFT devices for the conditions discussed above. After initial vacuum thermal annealing, we conducted bias stress tests on samples A_33 and B_44 OTFTs and observed that the I_{DS} changed less than 0.5% in A_33 and

B_44 OTFTs. Then, the devices were exposed to an 85 ºC and 85-90% RH environment for 24 h. After exposure, we conducted bias stress tests on the devices in the glovebox. After one-hour bias stress tests, A_33 devices exhibited changes of I_{DS} of 2.5% to be compared with the 23% change observed on B_44 devices. These levels of changes in A_33 and B_44 OTFTs are similar to the changes after immersion in water, as shown in Figure 32 (b) and (c). Also, the performance of both types of OTFTs recovered after annealed at 100 ºC in vacuum for 16 h.

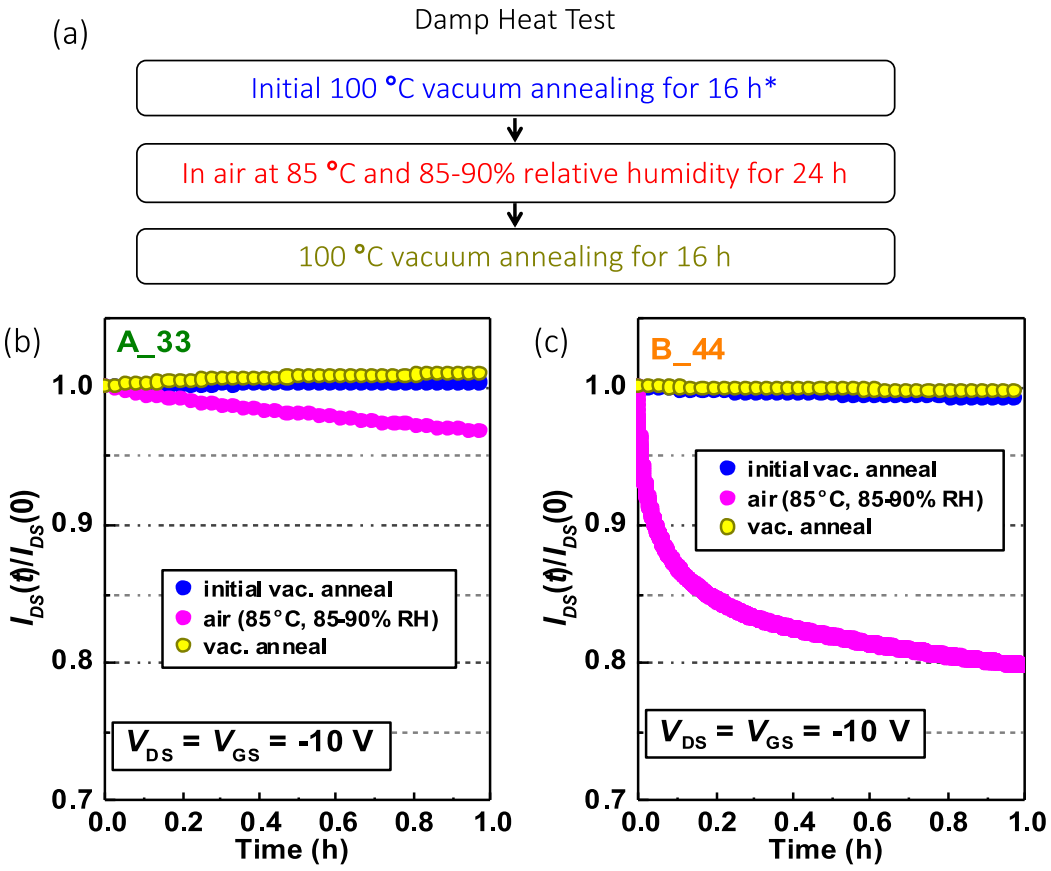


Figure 33. (a) The sequence of damp heat test on OTFTs. The stability of (b) A_33 devices and (c) B_44 devices under continuous dc-bias stress for OTFTs after exposing to different ambient conditions.

4.5 Operational Stability

4.5.1 One-Hour Operational Stability

Figure 34 shows the temporal evolution of the normalized $I_{DS}(t)$ measured during the dc-bias stress test for 1 h on group A and group B devices. The plotted data are from four devices for each of the A_33, B_44, B_22, and B_11 OTFTs, and two devices for each of the A_27 and A_22 OTFTs, respectively, since A_27 and A_22 showed a lower yield than the others. A_27 and A_22 also exhibited increased device-to-device variation, presumably due to the high leakage current of these two types of gate dielectrics.

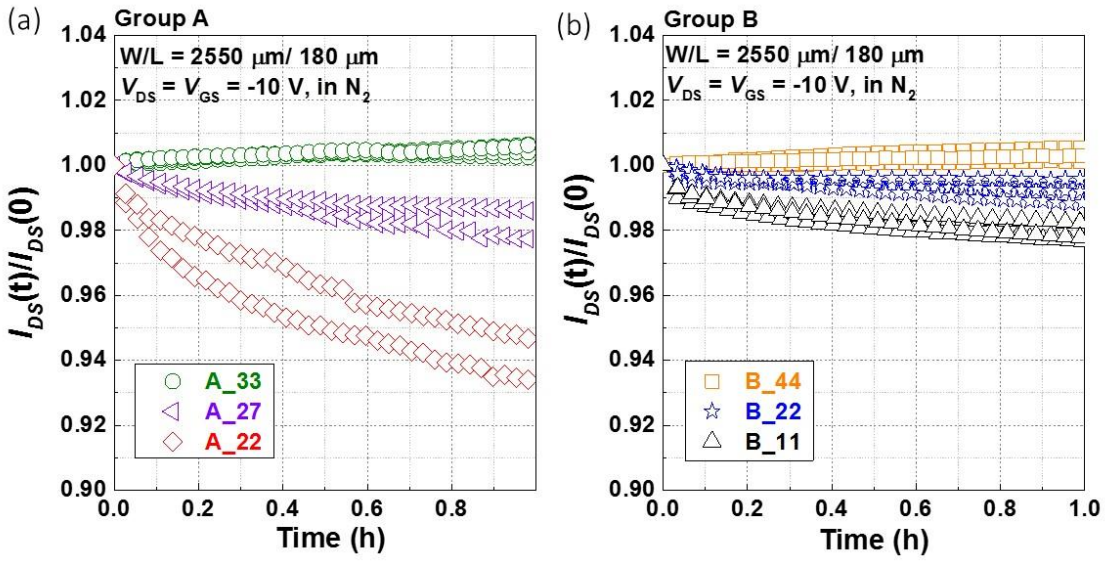


Figure 34. The operational stability of OTFTs in (a) group A and (b) group B during one-hour continuous dc-bias stress at V_{DS} = V_{GS} = -10 V in N_2.

After one hour of continuous dc-bias stress, the normalized I_{DS} of A_33 slightly increased to 1.008, while those of A_27 and A_22 dropped down to around 0.979 and 0.941, respectively. In group B, B_44 devices displayed normalized I_{DS} increases of ca. 1.002. During the same interval, the normalized I_{DS} dropped to 0.994 in B_22 and 0.981 in B_11

OTFTs. In addition, A_33 OTFTs exhibited higher operational stability than that of B_22 and B_11, which have similar or even thicker dielectric layers. These results demonstrate that the operational stability of an OTFT during bias stress tests can be controlled systematically by changing the thickness of the oxide gate dielectric layer [38].

4.5.2 Long-Term Operational Stability

Figure 35 shows the long-term temporal evolution of the normalized $I_{DS}(t)$ for TIPS/PTAA OTFTs in group A and group B. A_33 displayed remarkable I_{DS} stability after 40 h bias stress, within an overall change of I_{DS} smaller than 4%. On the contrary, A_27 and A_22 show poor long-term stability, presumably due to their high and unstable gate leakage current. On A_27 OTFTs, the normalized I_{DS} dropped to 0.92 before the device failed after 8 h of continuous bias-stress. On A_22 OTFTs, the normalized I_{DS} dropped below 0.8 in 4 h before failing. In contrast, Figure 35 (b) shows the changes of normalized I_{DS} after 24 h for group B devices (2.2%, -3.6%, and -5.9% for B_44, B_22, and B_11 OTFTs, respectively), which were not found to fail. In addition, A_33 OTFTs exhibited higher operational stability than that of B_22 and B_11, which had similar or even thicker dielectric layers compared to that of A_33. These results correlate to some extent with the quality of the dielectric layer as determined by leakage current measurements. Furthermore, they prove that the operational stability of these devices can be engineered by controlling the thicknesses of gate dielectric layers.

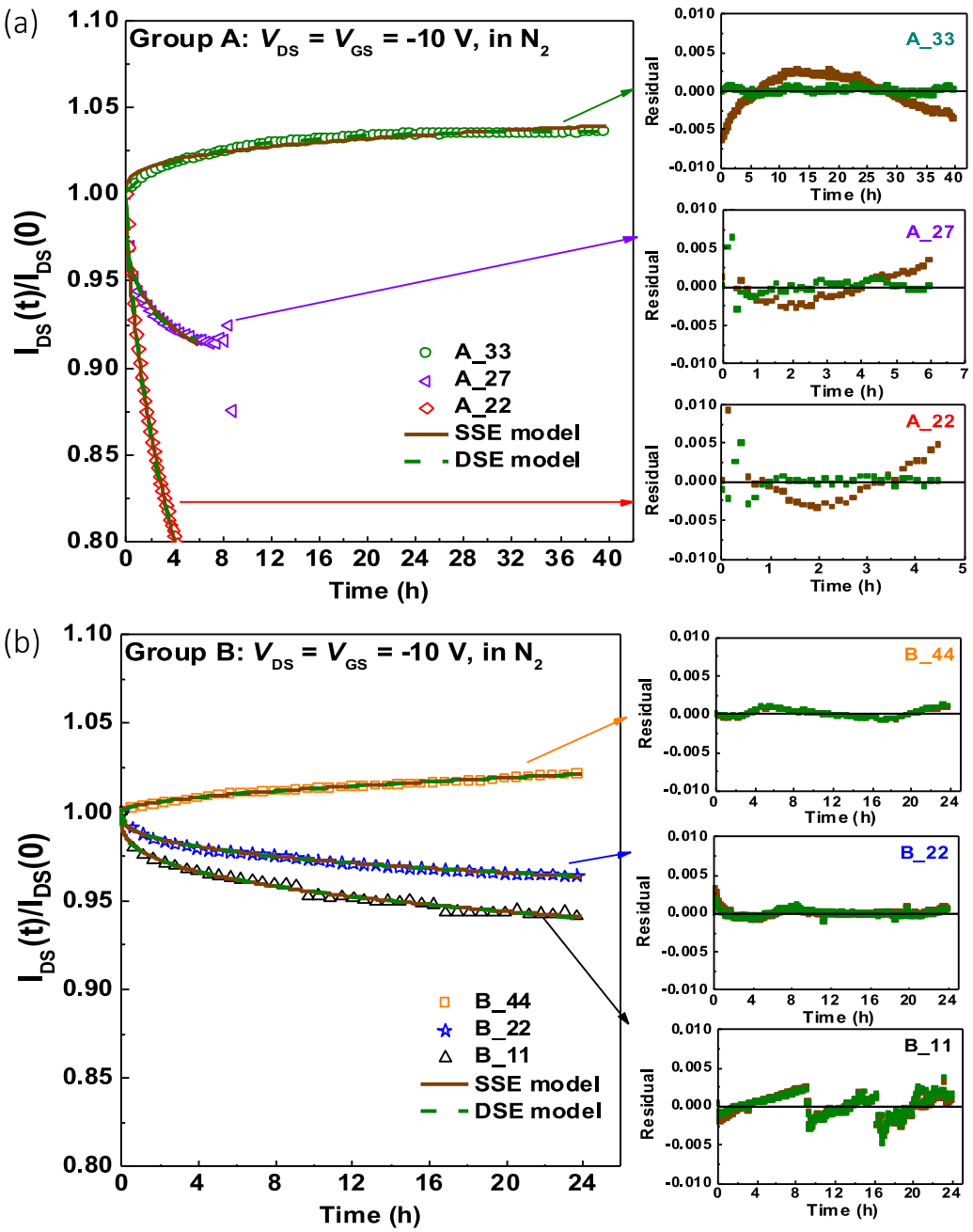


Figure 35. The long-term operational stability of OTFTs in (a) group A and (b) group B during dc-bias stress in N_2, with the fitted curves using the SSE model and DSE model. The fitting residuals are shown on the right to the main figures.

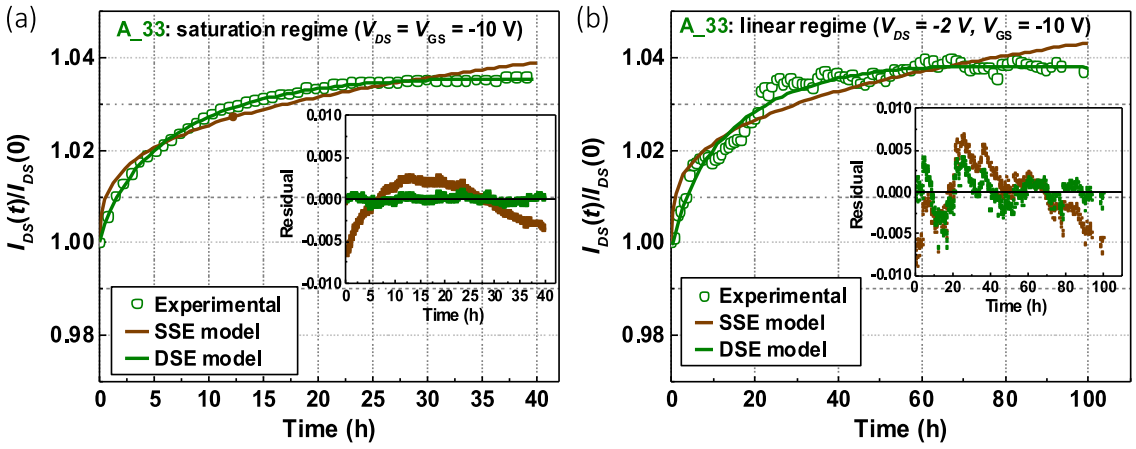


Figure 36. Temporal evolution of the normalized I_{DS} during dc-bias stress (a) at the saturation regime for 40 h with fitted curves, and (b) at the linear regime for 100 h with fitted curves. The insets show the fitting residuals of the SSE model (brown) and DSE model (green).

To study the stability of OTFTs when operating devices at different regimes, A_33 OTFTs were stressed at the saturation regime (V_{DS} = V_{GS} = -10 V) for 40 h and at the linear regime (V_{DS} = -2V, V_{GS} = -10 V) for 100 h, respectively. Figure 36 shows the temporal evolution of $I_{DS}(t)/I_{DS}(0)$ during the continuous on-state gate bias stress test at the saturation regime and the linear regime. At both regimes, A_33 OTFTs showed remarkable operational stabilities, with the changes of I_{DS} smaller than 4% after tens of hours of continuous operation.

4.5.3 Analytical Model of Operational Stability

To rationalize the temporal changes of $I_{DS}(t)$ and to extrapolate the long-term stability of these OTFTs, first, it is necessary to validate a model that describes these changes. In contrast to OTFTs with a single gate dielectric layer, the OTFTs with bilayer

gate dielectric structures show the contributions of two distinct aging mechanisms with opposite effects. The first one, more commonly reported, causes a decrease of I_{DS} during continuous dc-bias stress due to charge trapping at or around the semiconductor-dielectric interface. This contribution is described by assuming that $V_{TH}(t)$ follows a single stretched-exponential (SSE) model (Equation (12)). In OTFTs with bilayer gate dielectrics, a second effect causes $I_{DS}(t)$ to increase over time. Although the origin of this contribution is not fully understood, we believe that it is associated either with the orientation of dipoles at the gate dielectric or with the injection of carriers at the gate electrode. To account for this effect, we assume that $V_{TH}(t)$ changes due to this effect follows another single stretched-exponential model with the following expression [71, 72]:

$$\Delta V_{TH,2}(t) = \Delta V_{TH,2\infty} \cdot \left\{1 - \exp\left[-\left(\frac{t}{\tau_2}\right)^{\beta_2}\right]\right\} \tag{13}$$

where τ_2 is the characteristic decay time, β_2 is the dispersion parameter ($0<\beta_2<1$), and $\Delta V_{TH,2\infty} = \left[V_{TH,2}(\infty) - V_{TH}(0)\right]$.

Taken these two opposite bias stress effects into account, the overall bias stress effect of an OTFT with a bilayer gate dielectric results from the simultaneous occurrence of the charge trapping at dielectric-semiconductor interfaces and the reorientation of dipoles present in the gate dielectric layers or to the injection of charge carriers at the gate dielectric. Thus, the bias stress effects in OTFTs in this work could be modeled by the following equation:

$$\Delta V_{TH}(t) = \Delta V_{TH,1\infty} \cdot \left\{1 - \exp\left[-\left(\frac{t}{\tau_1}\right)^{\beta_1}\right]\right\} + \Delta V_{TH,2\infty} \cdot \left\{1 - \exp\left[-\left(\frac{t}{\tau_2}\right)^{\beta_2}\right]\right\} \quad (14)$$

This model will be referred to as the double stretched-exponential (DSE) model. The values of $\Delta V_{TH,1\infty}$ and $\Delta V_{TH,2\infty}$ cannot be unequivocally determined using this fitting procedure due to the practical constraints. Instead, we introduce a new fitting parameter $m = \Delta V_{TH,1\infty}/\Delta V_{TH,2\infty}$.

Assuming μ and C_{ox} are constant and using the standard transistor *I-V* Equation (7) and Equation (8), the I_{DS} changes of the SSE model and DSE model at the linear regime and the saturation regime could be derived from Equation (12) and Equation (14), respectively, using the following equations:

$$\frac{I_{DS}(t)}{I_{DS}(0)} = 1 - \frac{\Delta V_{TH}(t)}{V_{GS} - V_{TH}(0)}, linear\ regime \quad (15)$$

$$\frac{I_{DS}(t)}{I_{DS}(0)} = \left[1 - \frac{\Delta V_{TH}(t)}{V_{GS} - V_{TH}(0)}\right]^2, saturation\ regime \quad (16)$$

Next, the experimental data showing in Figure 35 and Figure 36 were fitted with Equation (12) and Equation (14) together with Equation (15) and Equation (16), to compare the SSE and DSE models. We note that for A_33 and B_44 OTFTs, which show an increasing tendency of I_{DS} over time, the data of A_33 and B_44 were fitted using Equation (12) but without the negative sign in the exponential function. The values of τ_1 and β_1 derived from the best fits of the SSE model to the experimental data are listed in Table 4 and compared with several typical transistors in literature. The parameters values of the

DSE model derived from these fits are shown in Table 5. Figure 36 (a) and (b) show a comparison of the best fits to the experimental data and the residuals (insets) using the SSE and DSE models. This comparison reveals that the DSE model better describes $I_{DS}(t)$ under dc-bias stress than the SSE model; particularly at the saturation regime and for a long stress time. Figure 36 (b) further confirms these observations also exist when devices are stressed at the linear regime for a long time.

4.5.4 Two Competing Effects

Since the devices in group A and group B have the same TIPS/PTAA-CYTOP interfaces with the TIPS/PTAA OTFTs with CYTOP single dielectric [38], the influence of charge trapping effect at the semiconductor-dielectric interface should be similar. Therefore, using DSE model, the A_33, A_27, B_44, B_22, and B_11 devices show similar values of $\tau_1$and β_1 (see Table 5), which are consistent with the values of $\tau_1$and β_1 fitted from experimental data of TIPS/PTAA OTFTs with CYTOP single gate dielectric using the SSE model (see Table 4). In Table 5, devices in group A and group B under bias stress in saturation regime also display comparable values of $\tau_2$and β_2. The values of τ_1, β_1, $\tau_2$and β_2 are less dependent on the NL thickness and are remarkably similar for both contributions to I_{DS}(t) changes, with values of β_1 and β_2 in the range of ca. 0.4 to 0.6. However, we found the ratio *m* to be dependent on the thickness of NL; devices with thicker NL in dielectric layers have larger values of *m*. This observation is applicable for both group A and group B devices; thus, it supports the hypothesis that thicker metal oxide

layers lead to the stronger influence of the second effects described by the second term in Equation (14).

For a more in-depth study of the dynamics of two opposite effects, we simulated ΔV_{TH} and the corresponding $\Delta V_{\mathrm{TH},1}$ and $\Delta V_{\mathrm{TH},2}$ using the DSE model and the lifetime parameters in Table 5 for A_33, A_27, and A_22 devices and B_44, B_22, and B_11 devices under on-state bias stress in the saturation regime. Figure 37 shows the contributions of the two opposite aging mechanisms, $\Delta V_{\mathrm{TH},1}$ (red curves) and $\Delta V_{\mathrm{TH},2}$ (blue curves), which show similar dynamics with opposite signs over the stress time. This similarity in the dynamics of both competing processes is unique if compared to other previous systems and allows the thickness of the NL to be used as a parameter to optimize the long-term stability of these OTFTs.

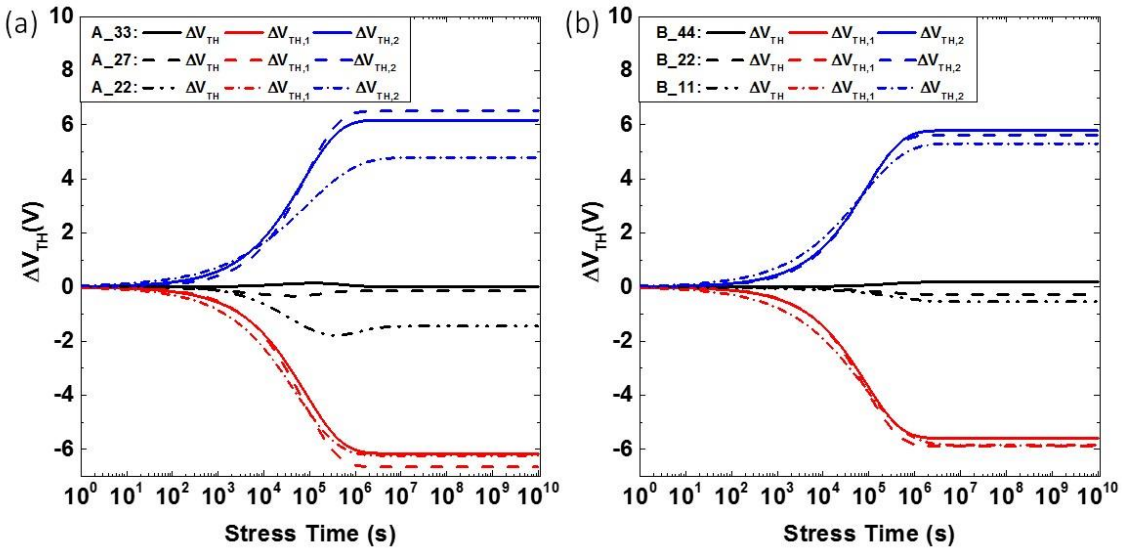


Figure 37. The simulation of ΔV_{TH} and the corresponding two opposite contributions ($\Delta V_{\mathrm{TH},1}$ and $\Delta V_{\mathrm{TH},2}$) of OTFTs during dc bias stress using the DSE model.

4.6 Temperature-Bias Stress Tests

Next, we focus our attention to V_{TH} changes occurring during positive and negative bias temperature stress tests; critical for assessing the operational stability of a TFT technology [11]. Here, to avoid confusion between biasing conditions for *n*-channel or *p*-channel TFTs, we refer to these tests as on-state and off-state temperature stress tests. The A_33 devices were stressed at on-state (V_{DS} = V_{GS} = -10 V) and off-state (V_{DS} = 0 V, V_{GS} = 10 V) for 1 h at the temperatures of 27 ºC, 55 ºC, and 75 ºC, respectively.

Figure 38 shows the transfer characteristics measured during these tests. All of the devices display high operational stability at elevated temperatures. At high temperature, the increase of the off current can be attributed to an increased gate dielectric leakage current, which is validated by the results shown in Figure 39. Figure 39 shows the leakage current density measured on the capacitor samples with CYTOP (35 nm)/NL (33 nm). When the temperature is higher than 55 °C, the leakage current density of the dielectrics increases from around 10^{-9} A cm^{-2} at room temperature to more than 10^{-7} A cm^{-2}.

From the transfer curves in Figure 38, the ΔV_{TH} of each condition are calculated and plotted in Figure 40. Although changes of V_{TH} are still observable, these changes are really small after 1 h dc-bias stress. $|\Delta V_{TH}(1h)|$ is less than 0.07 V during on-state temperature stress tests and smaller than 0.2 V during off-state temperature stress tests, even after the temperature is increased from room temperature to 75 °C. The measured $\Delta V_{TH}(t)$ values during on- and off-state temperature stress tests are also fitted using the DSE model and extrapolated to stress time of over 10 years, as shown in the insets of Figure 40 (a) and (b). Table 6 shows the values of the parameters used in these fits.

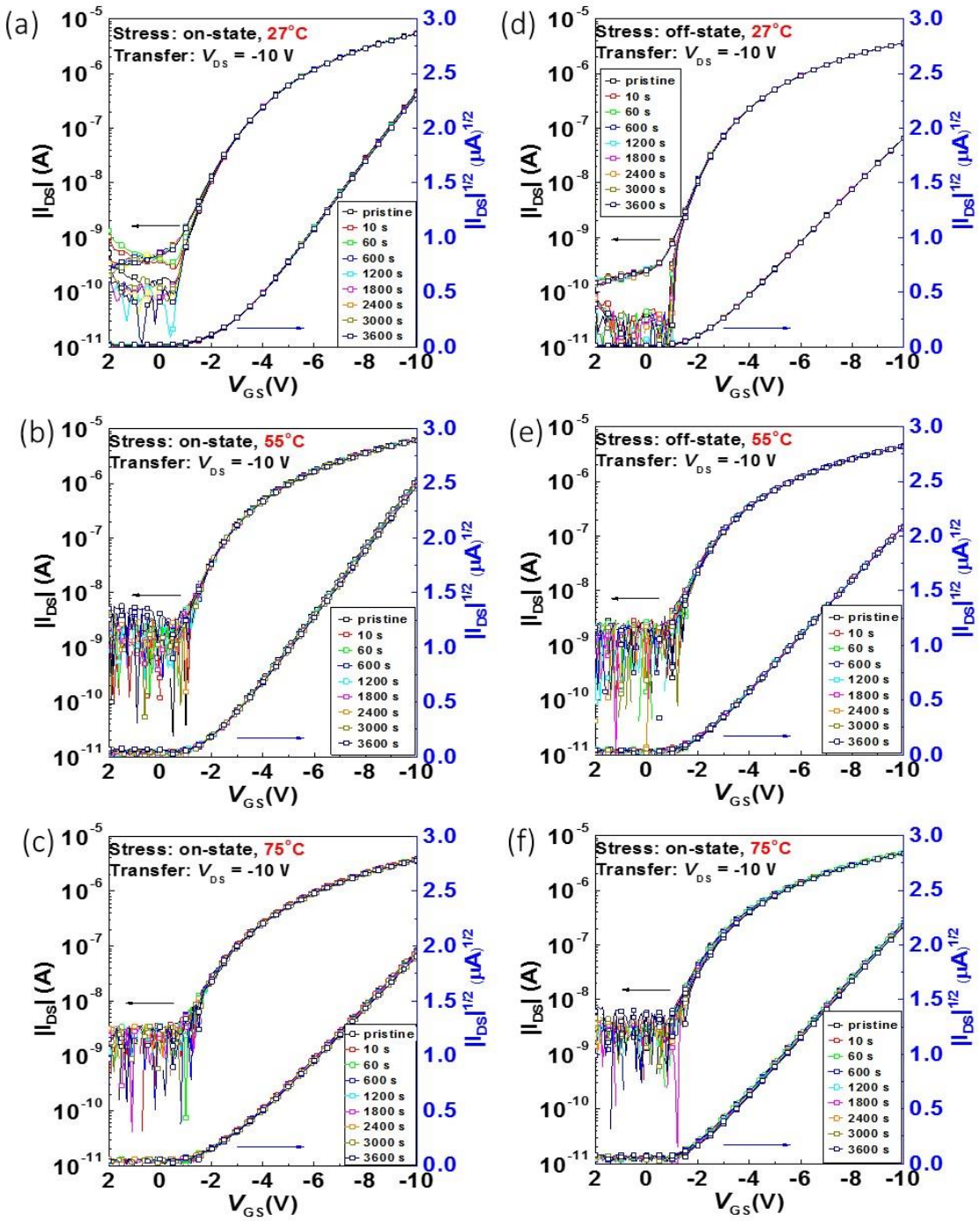


Figure 38. The transfer curves of as-fabricated A_33 devices after 1 h bias stress at on-state at (a) 27 ºC, (b) 55 ºC, and (c) 75 ºC, and off-state at (d) 27 ºC, (e) 55 ºC, and (f) 75 ºC.

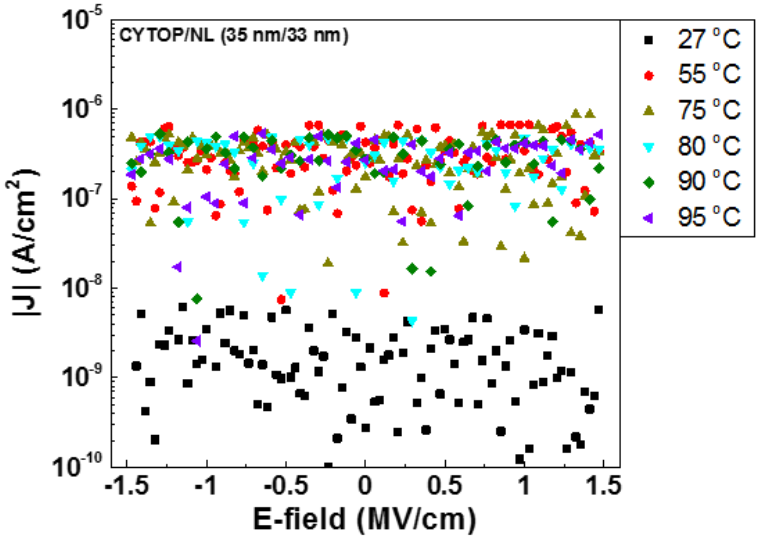


Figure 39. Current density-electric field (*J*-*E*) characteristics of the gate dielectric of A_33 devices at different temperatures.

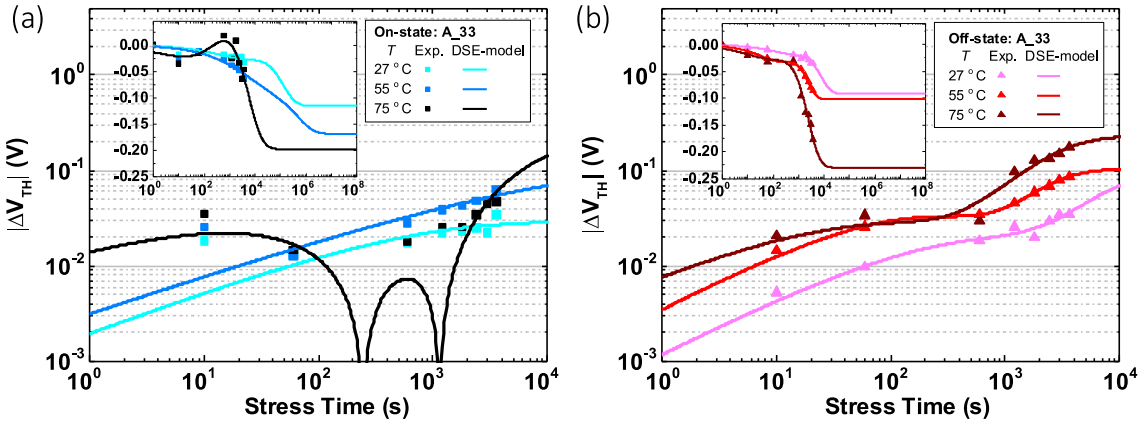


Figure 40. The $|\Delta V_{TH}|$ values after dc-bias stress of as-fabricated devices A_33 at (a) on-state and (b) off-state bias stress tests under different temperatures, with curves fitted from the corresponding ΔV_{TH} values using double stretched-exponential (DSE) model (see insets).

At 27 °C, values of parameters τ_i and m are slightly smaller than those found on previous I_{DS} bias stress effect studies. We attribute these differences to the different experimental procedures that are used to measure temporal I_{DS} changes, compared with that used to derive $\Delta V_{TH}(t)$ in bias stress tests. In one case by modeling I_{DS} changes during

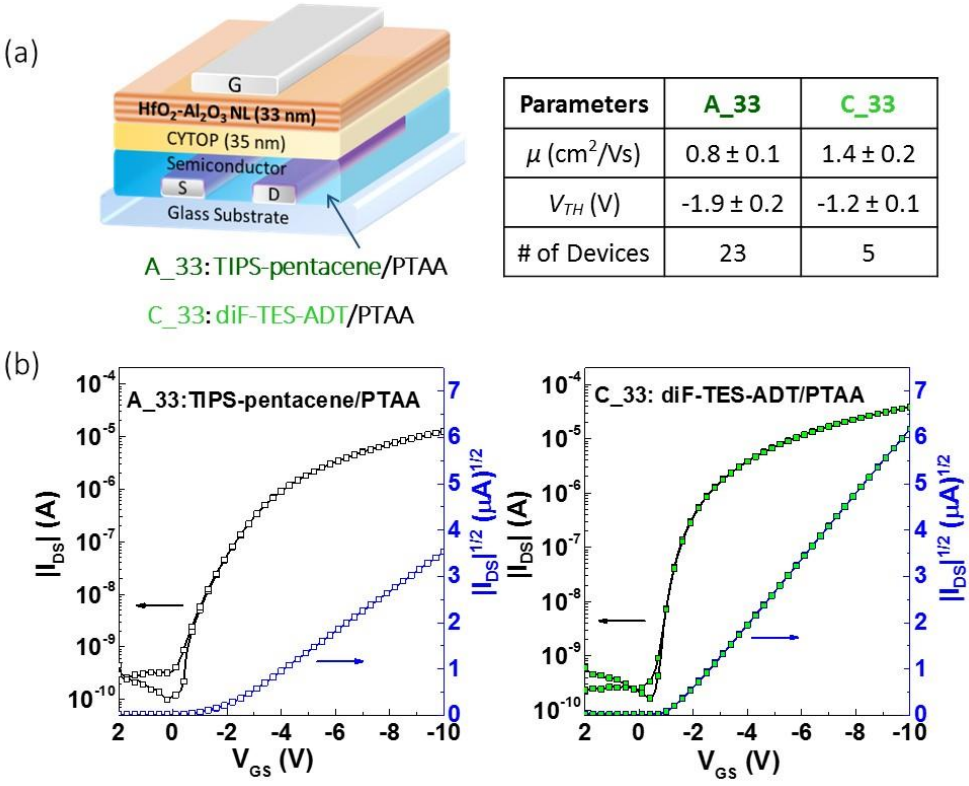
continuous bias stress; while in the other one, suspending the bias stress to measure changes in the transfer characteristics by sweeping the gate voltage from the positive to negative then back to positive voltages. With this in mind, while it is clear that at this point further systematic studies would be necessary to derive the physical insights that allow rationalizing the thermal dependence of $|\Delta V_{TH}|$. Also, it is clear that regardless of bias condition, $|\Delta V_{TH}|$ in all devices tested remains smaller than 0.2 V during on-state stress-tests for 1 h. Hence, $|\Delta V_{TH}|$ values during on-state stress tests measured in A_33 OTFTs are at least an order of magnitude smaller than those observed in *a*-Si TFTs (*e.g.*, $|\Delta V_{TH}|$ > 2 V during on-state stress tests at 70 °C for 1 h) [12] and around the same order of magnitude with the ones displayed by state-of-the-art *a*-oxide TFTs (*e.g.*, $|\Delta V_{TH}|$ > 0.01 V during on-state stress-tests at 70 °C for 1 h) [73].

4.7 Stability of OTFTs using Other Organic Semiconductors

In the previous discussion, the OTFT with a bilayer gate dielectric (CYTOP (35 nm)/NL (33 nm)) exhibited outstanding stability when using the blend of TIPS-pentacene and PTAA as the semiconductor layer. Next, we implement the same device structure on a different semiconductor system that uses a blend of diF-TES-ADT and PTAA as the semiconductor layer, which provides higher charge carrier mobility than that of the TIPS-pentacene /PTAA system. Figure 41 (a) shows the architecture of top-gate OTFTs with the gate dielectric layer in these devices comprises CYTOP (35 nm)/ALD Al_2O_3: HfO_2 NL (33 nm). The detailed fabrication process is described in the previous section and Chapter 2.

The semiconductor layer comprises a TIPS-pentacene/PTAA blend in a device of type A_33 and comprises a diF-TES-ADT/PTAA blend in a C_33 device.

The transfer characteristic of pristine champion A_33 and C_33 OTFT devices measured in an N_2-filled glovebox are shown in Figure 41 (b). All devices exhibited hysteresis-free electrical characteristics. The table summarizes the statistical values of the electrical parameters for pristine OTFTs of both types (W/L = 2550 µm/180 µm). C_33 OTFTs show similar performance parameters to previously reported diF-TES-ADT/PTAA-based OTFTs with a CYTOP/Al_2O_3 bilayer gate-dielectric [16].



Parameters	A_33	C_33
μ (cm^2/Vs)	0.8 ± 0.1	1.4 ± 0.2
V_{TH} (V)	-1.9 ± 0.2	-1.2 ± 0.1
# of Devices	23	5

Figure 41. (a) The structure of top-gate OTFTs with gate dielectric layers of CYTOP (35 nm)/NL (33 nm) and a semiconductor layer of TIPS-pentacene/PTAA (A_33) or diF-TES-ADT/PTAA (C_33). The table shows the pristine electrical parameters of OTFTs. (b) Transfer characteristics of as-fabricated OTFTs of A_33 (left) and C_33 (right).

Here, first, we conduct a direct comparison of the stability for A_33 and C_33 OTFTs after exposure to different environmental conditions as indicated in Figure 32. These environmental conditions are the same as those of the environmental stability tests in the previous section. Figure 42 shows that air exposure causes $|\Delta I_{DS}(t)|$ < 1% on both A_33 and C_33 OTFTs, while prolonged immersion in water (16 h) results in larger $|\Delta I_{DS}(1\ h)|$ values; with changes in A_33 (ca. 4%) devices found to be similar to those observed in C_33 (ca. 12%) devices. These changes are not permanent, and they are reversible after devices are vacuum annealed at 100 ºC for 16 h. These results are very consistent with those we discussed in previous the section, which proved that the devices with this gate dielectric geometry are also able to achieve high stability even with the high charge mobility semiconductor material.

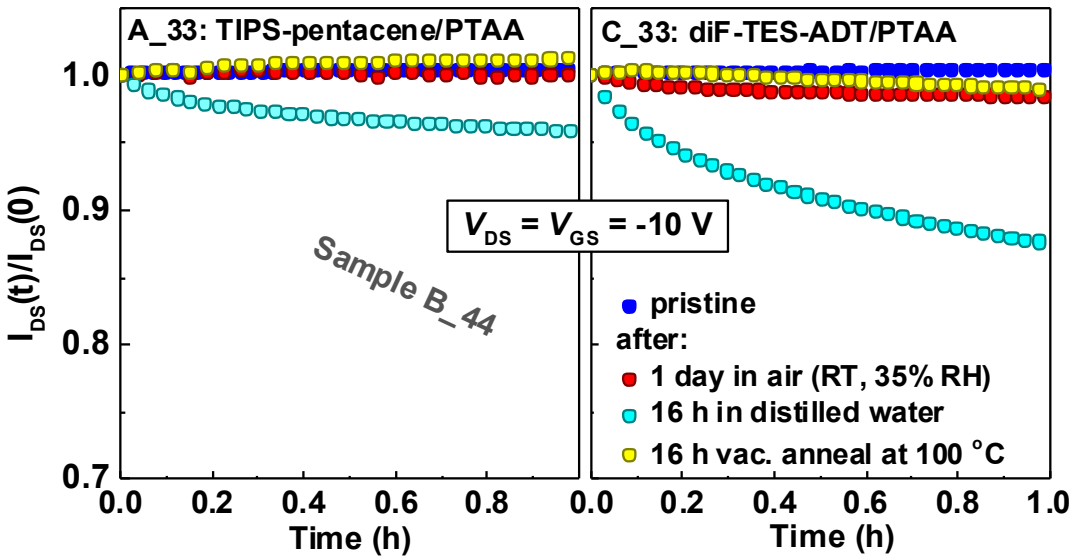


Figure 42. Environmental stability under continuous dc-bias stress for OTFTs in different ambient conditions.

Finally, we carried out independent long-term stress tests with V_{DS} = V_{GS} = -10 V at room temperature (RT, ca. 27 ºC) on pristine A_33 and C_33 μc-OTFTs for 163 h and

52 h, respectively. Figure 43 (a) and (b) show the transfer characteristics measured during these tests and reveal only very small changes. Table 2 provides a comparison of the electrical parameters (*i.e.*, μ, V_{TH}, $|S|$, and current on-off ratio) which are derived from these transfer characteristics before and after stress tests in Figure 43 (a) and (b). After stress, the values of μ, V_{TH}, and $|S|$ are changed by less than 3%. The current on-off ratios almost remain the same levels before and after the stress tests.

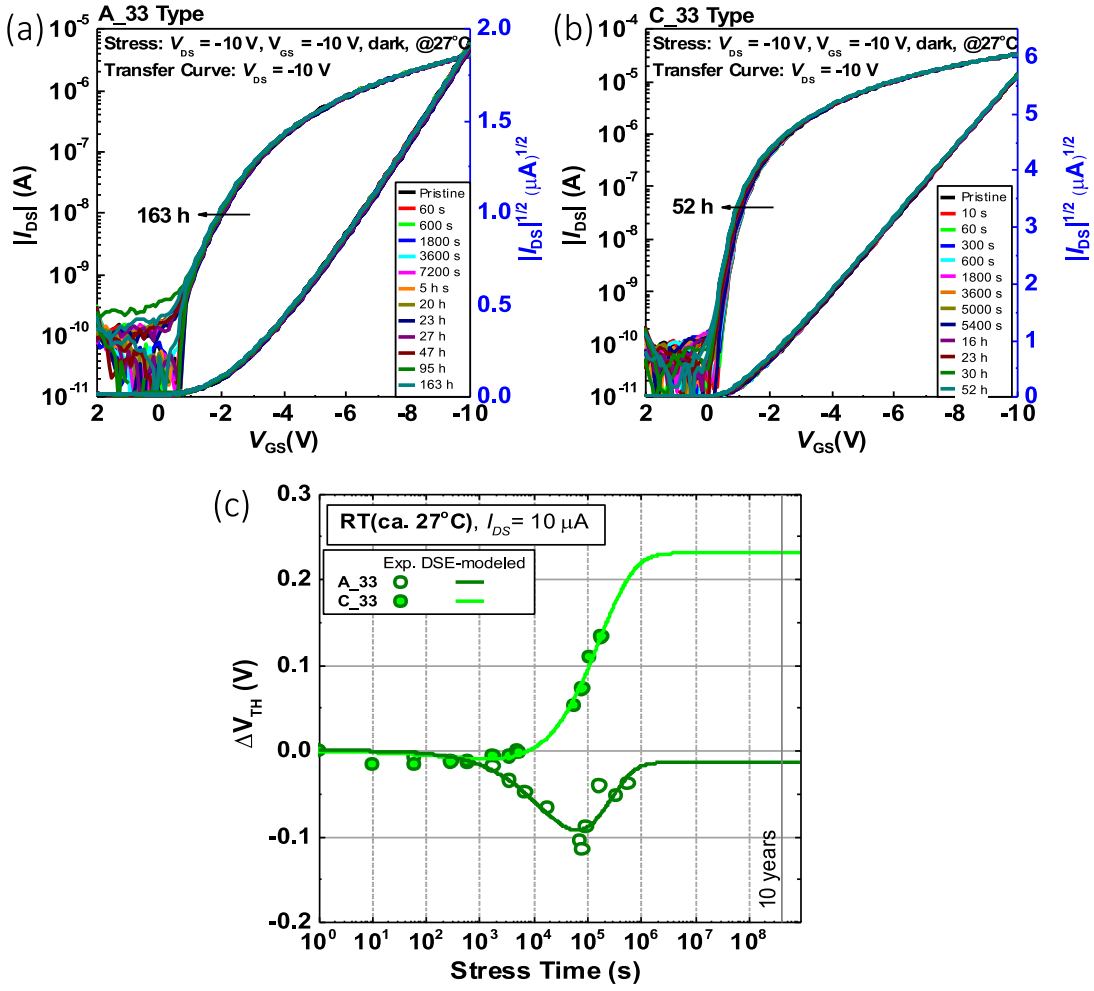


Figure 43. Transfer characteristics of (a) A_33 type OTFTs and (b) C_33 type OTFTs upon dc-bias stress. (c) Room-temperature measured ΔV_{TH} under the on-state bias stress test of A_33 and C_33 with fitted curves using a DSE model.

Figure 43 (c) shows the ΔV_{TH} values, which are calculated through the transfer curves of OTFTs shown in Figure 43 (a) and (b). The measurement results are also fitted with the DSE model. Also, the DSE-modeled values are extrapolated to a stress time of over 10 years. The values of the fitting parameters are shown in Table 7. Compared with the fitting parameters showing in Table 5, these results demonstrate that good consistency is obtained within one order-of-magnitude between the ΔV_{TH} values measured on different batches of devices and with different organic semiconductor layers.

Table 2 A summary of electrical parameters of OTFTs before and after stress tests.*

Sample No.	μ (cm^2 V^{-1} s^{-1})		V_{TH} (V)		$\|S\|$ (V decade^{-1})		Current on-off ratio	
	pristine	after stress**	pristine	after stress**	pristine	after stress**	pristine	after stress**
A_33	0.26	0.26	-2.69	-2.73	0.71	0.70	5.9×10^4	8.2×10^4
C_33	1.41	1.37	-1.12	-1.01	0.30	0.31	7.3×10^5	4.9×10^5

* The parameters are calculated from transfer curves in Figure 43 (b) and (c).
** The stress time is 163 h and 52 h for A_33 and C_33 OTFTs, respectively

4.8 Comparison with Other Technologies

Finally, we compare the extrapolated $|\Delta V_{TH}|$ estimated using the DSE model in the saturation regime ($I_{DS} \geq 10$ μA) with those extrapolated from SSE models derived for other TFT technologies, including organic single-crystal PDIF-CN_2 (*sc*-PDIF-CN_2) [17], the state-of-the-art OTFTs using IDTBT with F4TCNQ molecular additives [60], *a*-Si, μc-Si,

a-IGZO and LT *poly*-Si TFTs [74], as shown in Figure 44. The OTFTs fabricated in this work are μc-OTFTs, which are indicated as "μc-Organic" in Figure 44.

The left panel of Figure 44 shows the experimental $|\Delta V_{TH}|$ values of A_33 and C_33 μc-OTFTs in log-log scale with fitted curves from Figure 43 (c) and for comparison extrapolated SSE-modeled $|\Delta V_{TH}|$ derived for organic single-crystal PDIF-CN_2 (sc-PDIF-CN_2) TFTs [17] and the state-of-the-art OTFTs using IDTBT with F4TCNQ molecular additives [60]. These experiments in this work and literature were conducted at room temperature. Within device-to-device $|\Delta V_{TH}|$ values measured in all μc-OTFTs are at least an order of magnitude smaller than those expected from *sc*-OTFTs or the state-of-the-art OTFTs with molecular additives.

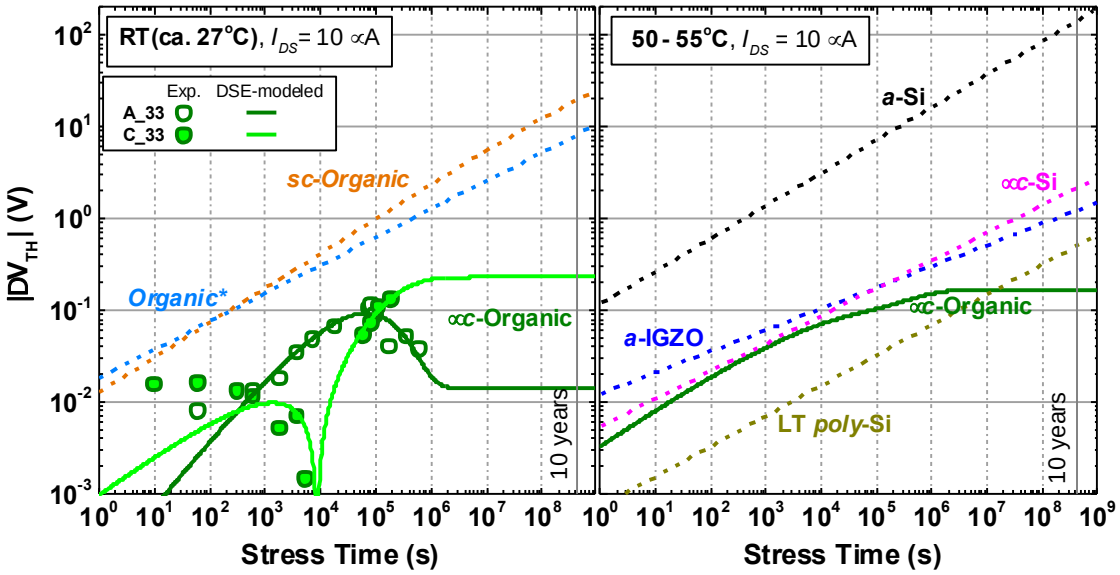


Figure 44. (Left panel) Room-temperature measured $|\Delta V_{TH}|$ under on-state bias stress test of A_33 and C_33 with fitted curves from Figure 43 (c). *The blue dashed data are from the state-of-the-art OTFT showing the highest stability by using IDTBT with F4TCNQ molecular additives. (Right panel) Comparison between DSE-modeled $|\Delta V_{TH}|$ at 55 °C for μc-OTFTs and SSE-modeled $|\Delta V_{TH}|$ at 50 °C for commercial TFTs technologies.

Furthermore, the right panel of Figure 44 shows a comparison of the DSE-modeled $|\Delta V_{TH}|$ values derived from fits to the experimental data at 55 ^{o}C displayed in Figure 40 (a) for our μc-OTFTs, with SSE-modeled $|\Delta V_{TH}|$ values for other commercial TFT technologies at 50 ^{o}C ($I_{DS} \geq$ 10 μA); for self-consistency taken from Ref. [74]. This comparison reveals that the extrapolated 10-year operating $|\Delta V_{TH}|$ in our μc-OTFTs (< 1.5 V) is nearly two orders of magnitude smaller than values expected in *a*-Si TFTs (> 100 V) [74], and comparable to or smaller than those found in μc-Si TFTs (ca. 2 V) and *a*-IGZO TFTs (ca. 1 V) [74].

4.9 Summary

In summary, we have demonstrated a practical approach of having an engineered bilayer gate dielectric comprising a CYTOP layer and a NL layer fabricated by ALD to realize stable top-gate μc-OTFTs from solution processing. These μc-OTFTs exhibited improved environmental stability (particular under aqueous environments) when compared to previously reported μc-OTFTs and an unprecedented level of operational stability. The stability of these μc-OTFTs is superior to that displayed by *a*-Si TFTs and comparable to state-of-the-art commercial TFT technologies. Although further studies will be necessary to improve our understanding of the physical mechanisms giving rise to the temporal and thermal dependence of the ΔV_{TH} observed, these results provided strong evidence that μc-OTFTs could achieve the level of performance of commercial inorganic semiconductor-based TFT technologies.

CHAPTER 5. OTFT-BASED PHOTODETECTORS

This chapter describes a new photodetector concept by integrating a dual-gate organic thin-film transistor with an organic photodiode device that operates in a photovoltaic mode instead of the common photoconductive mode. This new geometry with low power consumption yields a responsivity value above 10 A W^{-1} with video-rate compatible response time. Modeling of the operation of this photodetector with the novel device architecture suggests that the responsivity could increase to 10^4 - 10^6 A W^{-1} by scaling the channel dimension and charge mobility of the transistor.

5.1 Introduction

Rapid developments of sensing technologies with the fast responsivity, high sensitivity, and good flexibility are expected to support more design and application of artificial intelligence in consumer electronics and health monitoring systems [75-78]. With unique properties such as lightweight, mechanical flexibility, and transparency, organic materials become promising candidates in this field. Because of their low process temperature, organic devices can be fabricated by spin-coating and printing over arbitrary substrates with low fabrication cost, which further distinguishes them from conventional inorganic technologies [79-83]. Especially, the easily tuned optoelectronic properties of organic materials are appealing for light signal detection and attracting intense attention in recent years [84, 85].

Organic photodiodes (OPDs) and organic phototransistors (OPTs) are the two most widely adopted architectures of organic photodetectors [40]. In recent years, the broad spectral coverage, low dark current, high detectivity, and short response time of the state-of-the-art OPDs can compete with the performance of conventional inorganic counterparts [85, 86]. However, the external quantum efficiency (EQE) of a photodiode is smaller than 100% without additional amplification mechanisms. It is because an absorbed photon can generate at best one electron-hole pair. Therefore, the small EQE value limits the photoresponsivity of a photodiode. To improve the low photoresponsivity, the study on OPTs emerged, and it was inspired by combining the photoresponse properties of organic materials and the intrinsic signal amplification properties of transistors [87-89]. In general, with the signal amplification process, the EQE of an OPT is higher than 100% so that the responsivity of an OPT can reach more than 1,000 A W^{-1} even at weak light signal [87, 90, 91]. Different from the photoresponse mechanism of a photodiode, the build-up and decay of light-induced current of a phototransistor rely on the trap sites in the active layer. Since the speed of these processes are usually not fast, the light response time of an OPT is generally at ranges of a second to a hundred second, which is much longer than that of an OPD (at ranges of a nanosecond to a millisecond). Such slow signal responses of the OPT devices are not applicable in many situations [40]. To avoid the slow photoresponse process of the OPTs, it reported a three-component integrated organic photodetector that takes advantage of the fast drain-source current changes with gate-voltage of the transistor and obtains a fast signal response [92].

In this work, we demonstrate an organic photodetector, which is comprised of an OPD device and a dual-gate organic field-effect transistor (DG-OTFT) based on solution-

processed organic semiconductors. To achieve a high responsivity to a weak light signal, the top-gate driven DG-OTFT is used to amplify the light signal which is detected by the OPD. The response time of the OPD, in this work, is at the level of a millisecond. Also, the response time of the channel current with the gate voltage of the OTFT is less than the level of a millisecond. Therefore, the overall response time of the photodetector in this work is at the level of a millisecond. The structure of DG-OTFT is based on the single-gate OTFT, which shows remarkable operational and environmental stability. Also the OTFTs show very small leakage currents and little noise, which impact on the light detection resolution of the whole detection system. By calculating the photoresponsivity based on device parameters extracting from experimental data, we found that a high responsivity (> 1,000 A W^{-1}) could be easily achieved by merely adjusting the structure of DG-OTFT. These results make the novel photodetector a very promising device for future light detection applications.

5.2 Organic Photodiodes

Figure 45 (a) shows the organic photodiode in an inverted device structure that is used in this work, which has a similar vertical structure to the photovoltaic configuration. Light illuminates from the bottom side of the OPD since the ITO is a transparent electrode. The photoactive layer is made with a blend of P3HT and ICBA, and it is sandwiched between the hole-collecting interlayer (which has a high work function) and the electron-collecting interlayer (which has a low work function). The presence of interlayers,

especially the adoption of PEIE as the electron-collecting layer, effectively reduces the dark current of the device [46].

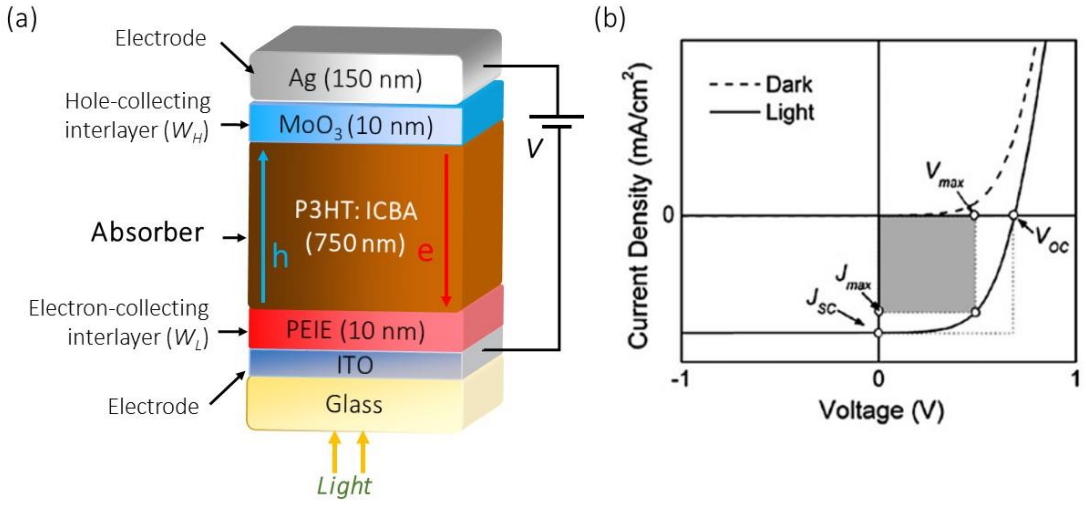


Figure 45. (a) The device structure of an OPD. (b) The *I-V* characteristics of an OPD [93].

Figure 45 (b) shows the current-voltage characteristics of an OPD in dark and under illumination. When an OPD is operated under illumination, the short-circuit current density, J_{SC}, is the maximum current density that the device generates at a particular irradiance when the applied voltage equals to zero (*i.e.*, the two terminals are shorted). The open-circuit voltage, V_{OC}, is the maximum voltage the device generates at the particular irradiance when the current is equal to zero (*i.e.*, the two terminals are open).

Figure 46 shows V_{OC} versus short-circuit current (I_{SC}) of an OPD at room temperature under variable irradiance, ranging from 10 nW to 1 mW. The device area (A) is 0.1 cm^2, which is a typical size of the OPD device in this work. The short-circuit current is plotted here for the comparison with the new OTFT-based photodetector in the next section, and it is equal to $A \times J_{SC}$.

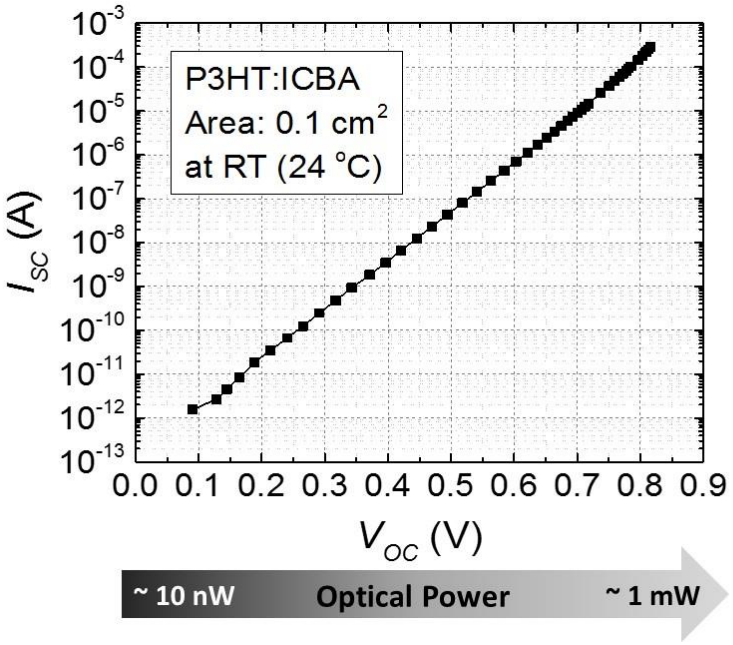


Figure 46. The short-circuit current plotted against the open-circuit voltage of an OPD (device area = 0.1 cm^2) on a semi-logarithmic scale as obtained via electrical characterization under variable irradiance.

As shown in Figure 46, the measurement data follows a straight line on the semi-logarithmic scale, which is consistent with the following equation that is derived from the equivalent circuit model of the OPD device [93]:

$$V_{OC} = \frac{nkT}{e} \ln(1 + \frac{J_{SC}}{J_0}) \tag{17}$$

where e is the elementary charge, kT is the thermal energy, n is the ideality factor of a diode, and J_0 is the revert saturation current density. As shown in Figure 46, when the optical power is very small, around 10 nW, the short-circuit current is around 1 pA. This level of current is too small to be measured by common equipment with a moderate detectivity. Since a transistor has an amplification mechanism and it could amplify the

voltage signal, we take advantages of the OTFT and the photovoltage generated by the OPD device and invent a new OTFT-based photodetector.

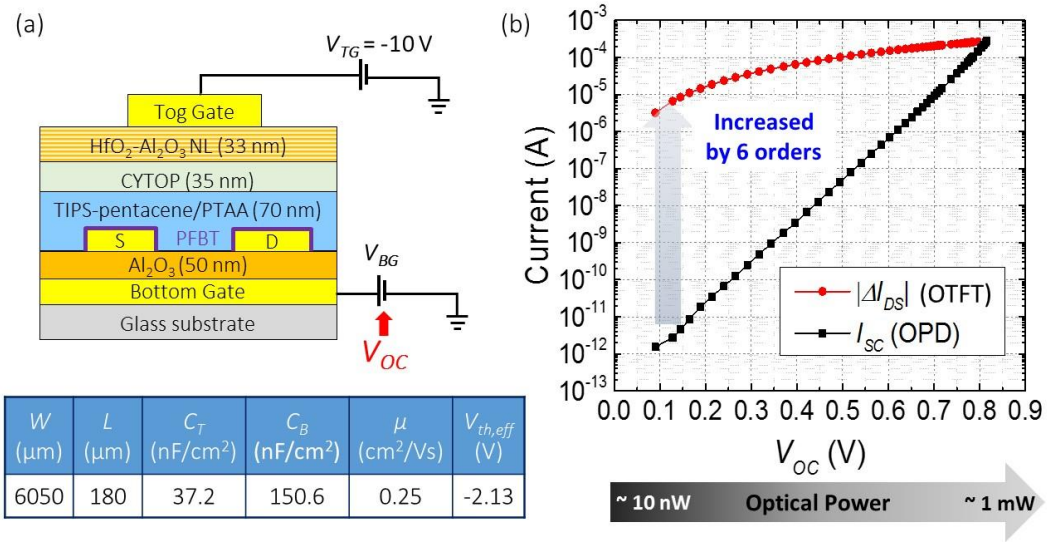
5.3 OTFT-based Photodetectors

The concept of new OTFT-based photodetector is based on an OPD that generates photovoltage (V_{OC}) and a DG-OTFT that amplifies the voltage signal. The device structure of a DG-OTFT is shown in Figure 47 (a). The DG-OTFT structure is used to avoid interferences since it has two independent gates that isolate the operating voltage and the signal voltage. For example, if the top-gate electrode is a control electrode that controls the transistor working at specific operating voltages, the bottom-gate electrode could work as a sense electrode to detect the V_{OC} signal from an OPD. Compared with the OTFT structure discussed in the previous chapter, the DG-OTFT device here has an extra bottom-gate dielectric layer (*i.e.*, a 50-nm thick Al_2O_3 layer) and a bottom-gate electrode, which could be made with any conductive material, such as Ag or ITO. The top and bottom structures share a semiconductor layer as well as source and drain electrodes.

When a DG-OTFT device is driven by a top-gate voltage V_{TG} with a constant bottom gate voltage V_{BG}, the device current-voltage characteristic in a saturation regime is described by [94]:

$$I_{DS} = \mu \frac{W}{2L} \frac{C_T^2}{C_T + C_B} \left(V_{TG} - V_{th,eff} + \frac{C_B}{C_T} V_{BG} \right)^2 \quad (18)$$

where μ is the intrinsic drift charge mobility of carriers, $V_{th,eff}$ is the effective threshold voltage, W is the channel width, L is the channel length, and C_T and C_B are the capacitance densities of the top- and bottom-gate dielectric, respectively. If we applied the V_{OC} of an OPD at the bottom-gate electrode of the DG-OTFT, the V_{BG} would be equal to the V_{OC}.



W (μm)	L (μm)	C_T (nF/cm²)	C_B (nF/cm²)	μ (cm²/Vs)	$V_{th,eff}$ (V)
6050	180	37.2	150.6	0.25	-2.13

Figure 47. (a) The device structure of a DG-OTFT. The table shows pristine device parameters of the DG-OTFT in this work. (b) The light-induced current plotted against the V_{OC} of an OPD (device area = 0.1 cm^2) on a semi-logarithmic scale.

The table in Figure 47 (a) is a summary of the pristine parameters of the DG-OTFT device with the structure shown above. Based on these parameters, we calculated the changed of I_{DS} ($|\Delta I_{DS}|$) with different V_{OC} values and a fixed top gate voltage (V_{TG} = -10 V), as shown in Figure 47 (b). As a result, at a very weak signal level close to 10 nW, the measurable changes of I_{DS} are around the level of a microampere, which is 6 orders of magnitude larger than the short circuit current of OPD. This improved measurable light-induced current shows great potential for weak light detection when using an OTFT in a photodetector.

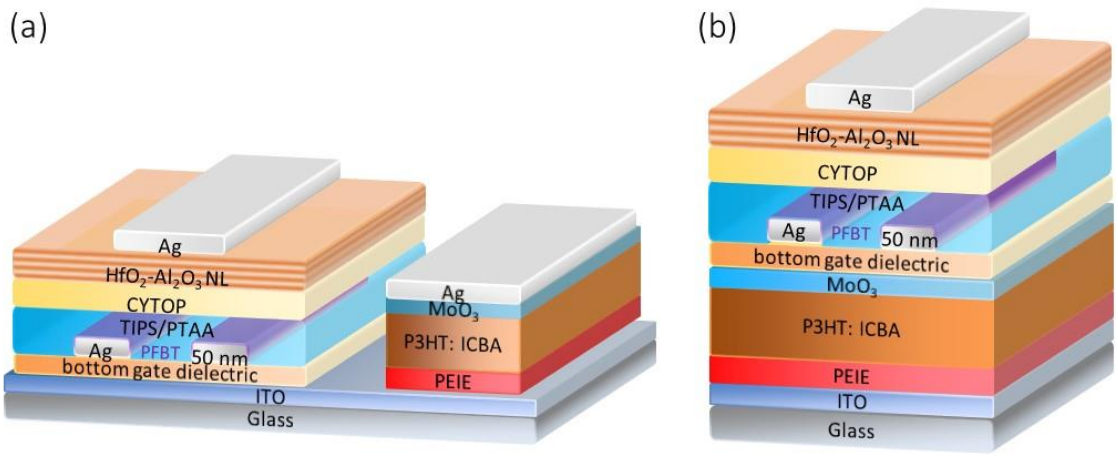


Figure 48. The OTFT-based photodetectors (a) in a lateral structure and (b) in a vertical structure.

For concept realization, two types of device structures are designed. In Figure 48 (a) and (b), an OTFT and an OPD are fabricated on the same ITO coated substrate in a lateral and a stacked structure, respectively. Therefore, the bottom gate of DG-OTFT and the bottom or top electrode of OPD are connected through the ITO. The bottom gate dielectric layer also has a high capacitance density as well as a small leakage. Thus, the OPD operates close to the open circuit condition. In operation, the top gate voltage and the drain to source voltage of the OTFT are fixed, then the change of I_{DS} is observed when the OPD is illuminated with different light intensity. Low electric power is consumed since no additional voltage is required on the OPD. The vertical structure has a smaller area, but the fabrication of this structure is more challenging than that of the lateral structure. Due to the fabrication limits, the lateral structure will be focused on for concept demonstration in the following sections.

5.4 Device Fabrication

The organic photodetector with a novel structure that is comprised of a DG-OTFT and an OPD in the lateral structure was fabricated on commercially available ITO-coated glass substrates, which were pre-cut into 1.5" x 2" pieces. The ITO of substrates was patterned by wet etching and cleaned by solvents. The final dimensions of the ITO and glass substrates are shown in Figure 49 (a). The PDMS masks were prepared in the size of 1.5" x 1.3" and 1.5" x 0.7" for covering the OTFT area and the OPD area, respectively.

During the fabrication of OPDs, the OTFT area was first covered with a PDMS mask. A 0.4 wt.% PEIE solution was spin-coated on the substrates, followed by thermal annealing at 100 °C for 10 minutes in air, generating a 10 nm thick PEIE layer (see Figure 49 (b)). The PEIE-coated ITO substrates were then transferred into a N_2-filled glovebox for the next process. The prepared P3HT: ICBA solution with a concentration of 100 mg mL^{-1} was spin-coated on top of PEIE-coated substrates, followed by solvent annealing for 5 h and then thermal annealing at 150 °C for 10 min in a N_2-filled glovebox (see Figure 49 (c)). Then a 10 nm thick MoO_3 layer and a 150 nm thick Ag layer as top electrodes of OPD were deposited on the P3HT: ICBA layer through a shadow mask in sequence by the thermal evaporator (see Figure 49 (d)). The top electrodes were extended with aluminum conductive tapes (3M™ 1170 tape), and the PDMS mask was removed from the OTFT area (see Figure 49 (e)).

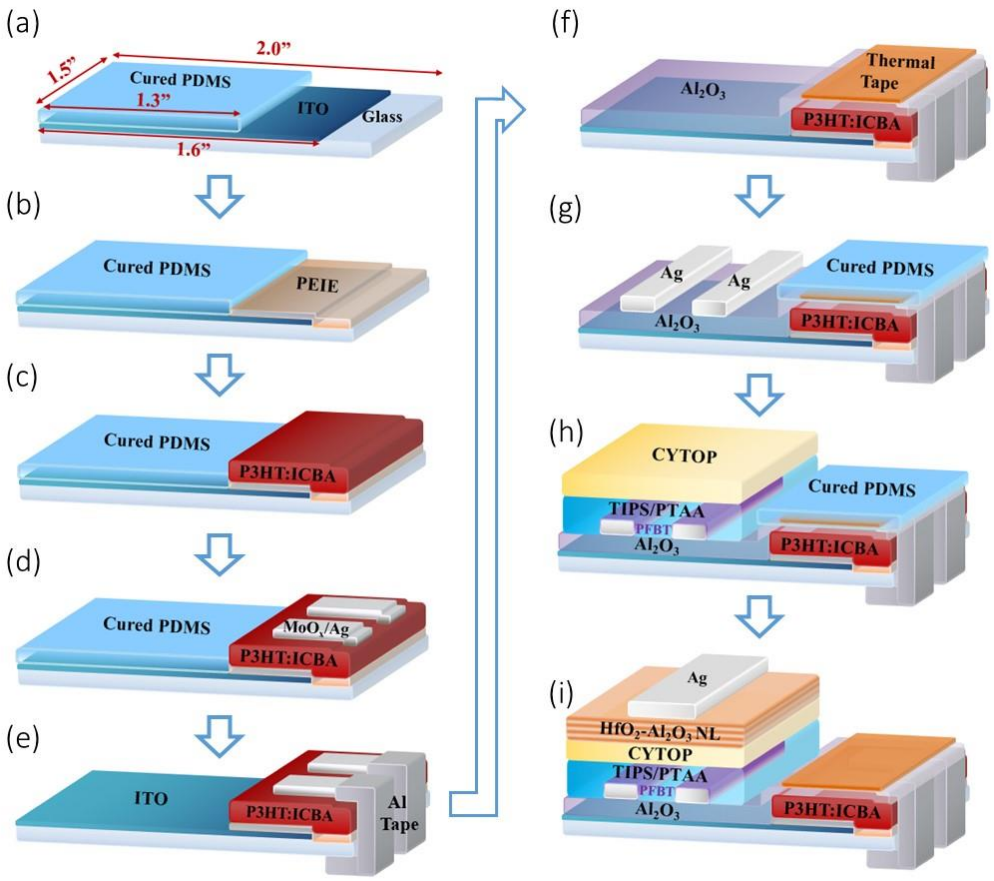


Figure 49. The fabrication processes of OTFT-based photodetector in the lateral structure: (a) ITO patterning and masked by PDMS; (b) PEIE deposition; (c) deposition of P3HT: ICBA thin film; (d) deposition of MoO_3 and Ag as OPD top electrodes; (e) OPD top electrodes extension with aluminum tape; (f) deposition of Al_2O_3 as bottom gate dielectric of OTFT; (g) deposition of Ag as OTFT source and drain electrodes; (h) deposition of PFBT mixed TIPS/PTAA and CYTOP on OTFT area; (i) deposition of HfO_2-Al_2O_3 NL as the second layer of OTFT top dielectric and Ag deposition OTFT top gate electrodes.

Then, a 50 nm thick Al_2O_3 layer was deposited by the ALD system at 110 °C on the substrate as the bottom gate dielectric layer of DG-OTFTs. Next, the OPD area was encapsulated with Kapton® tapes (see Figure 49 (f)), and the Ag source/drain electrodes (50 nm) were deposited through shadow masks by the thermal evaporator. Then, the OPD area was covered by the PDMS mask before spin coating the semiconductor layer of OTFT (see Figure 49 (g)). To form a self-assembled monolayer of PFBT on Ag electrodes, a 100

mM PFBT solution was prepared by dissolving in tetralin solvent. A 1:1 weight ratio of TIPS-pentacene and PTAA blend was dissolved in tetralin for a concentration of 30 mg mL^{-1}. Then, a 10 mM PFBT-mixed TIPS/PTAA solution was prepared by mixing the 100 mM PFBT solution in TIPS/PTAA solution in a volume ratio of 1:9. The PFBT-mixed TIPS/PTAA solution was spin-coated on the substrates, followed by annealing at 100 ºC on a hot plate for 15 min in a N_2-filled glovebox. Next, a 2 wt.% CYTOP solution was spin-coated on top of the semiconductor layer, followed by thermal annealing at 100 ºC for 10 min in a N_2-filled glovebox (see Figure 49 (h)). After removing the PDMS mask from OPD area, a 33 nm Al_2O_3-HfO_2 NL was deposited by ALD at 110 ºC. Finally, the Ag top-gate electrodes (100 nm) were deposited through a shadow mask by the thermal evaporator (see Figure 49 (i)).

5.5 Device Characterization

Figure 50 (a) shows the final device structure of the OTFT-based photodetector in this work. A picture of devices is shown in Figure 50 (b). Figure 50 (c) shows a circuit configuration of the photodetector consisting of a DG-OTFT and an OPD, in which the OPD is modeled by an approximated equivalent circuit that is comprised of a diode with a reverse saturation current I_0, a current source I_{ph}, a series resistance R_S, and a shunt resistance R_{sh} [93]. The I_{ph} corresponds to the photocurrent of an OPD under illumination. The source electrode of the DG-OTFT is grounded, while the top-gate voltage V_{TG} and drain-source voltage V_{DS} are applied on the electrodes of the transistor. The bottom electrode of the OPD is connected to the bottom-gate (BG) electrode of the DG-OTFT, and the top electrode is grounded. Thus, the load of OPD is a capacitor of the bottom-gate

dielectric layer of the transistor; it approximates to the open circuit condition. In this way, the open-circuit voltage V_{OC} of the OPD is reversely applied on the bottom-gate of the DG-OTFT as the bottom-gate voltage V_{BG}. Under specific V_{TG} and V_{DS} biases, the drain-source current I_{DS} is controlled by the value of V_{BG} (or V_{OC}); I_{DS} changes simultaneously with V_{OC} under different incident optical powers.

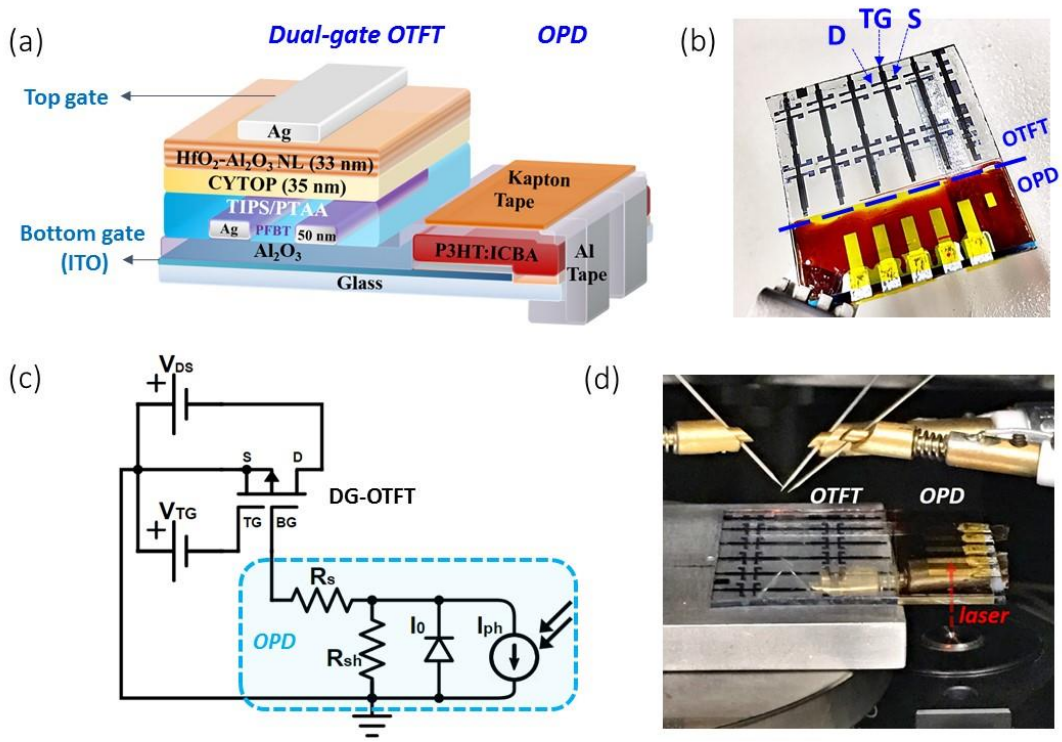


Figure 50. (a) The device structure of the organic photodetector which integrates a DG-OTFT with an OPD. (b) A photograph of fabricated devices. (c) The circuit configuration of the photodetector. (d) A photograph of the measurement setup.

5.5.1 Electrical Characterization

The electrical characteristics are first measured in dark condition, where V_{OC}= 0 V, meaning there is no bottom-gate controlled effect of the DG-OTFT. Figure 51 shows the

transfer and output characteristics of the DG-OTFT with only top-gate controlled properties. The transfer characteristics were measured by sweeping V_{TG} from 2 to -10 V and back to 2 V, in order to investigate hysteresis phenomena, which is negligible as observed. From Figure 51 (b), it clearly shows that the I_{DS} is weakly dependent upon the V_{DS} and is controlled primarily by the V_{TG} in the saturation region. In order to achieve the maximum gain with low power consumption, the bias voltages during light detection were determined as V_{TG} = -10 V and V_{DS} = -6 V in this work.

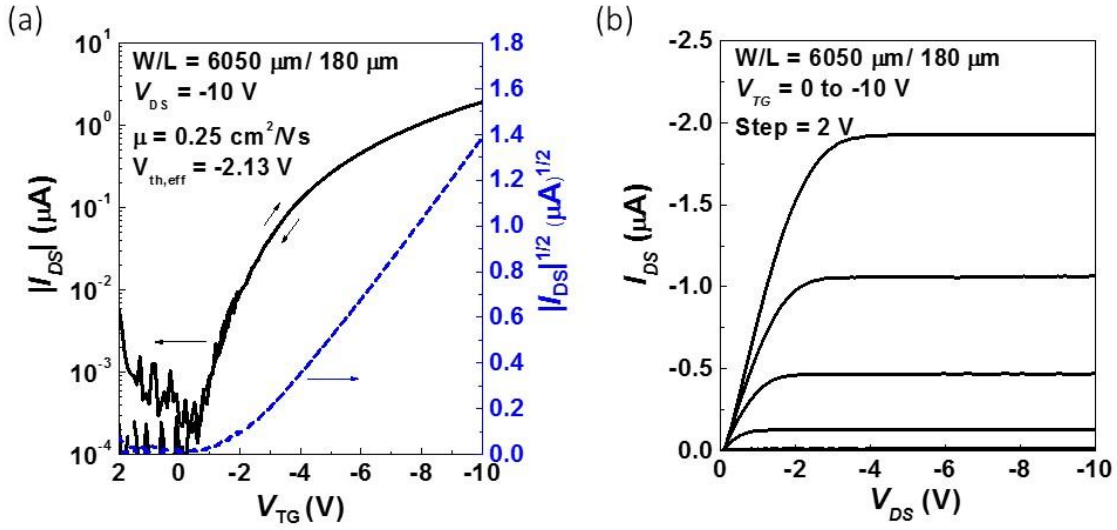


Figure 51. (a) The transfer characteristics and (b) output characteristics of the DG-OTFT, when the top electrode of the OPD is grounded.

5.5.2 Optical Characterization

Next, the optical characteristic of the devices was studied. Using the experimental setup shown in Figure 50 (d), a 635 nm laser source was used to illuminate from the backside of the OPD, while bias stress is also applied with V_{TG} = -10 V and V_{DS}= -6 V.

Figure 52 (a) compares the temporal $|I_{DS}|$ at the continuous bias-stress test in dark and under illumination with different incident optical powers P_{opt}. In all conditions, devices exhibited remarkable operational stability as well as little noise.

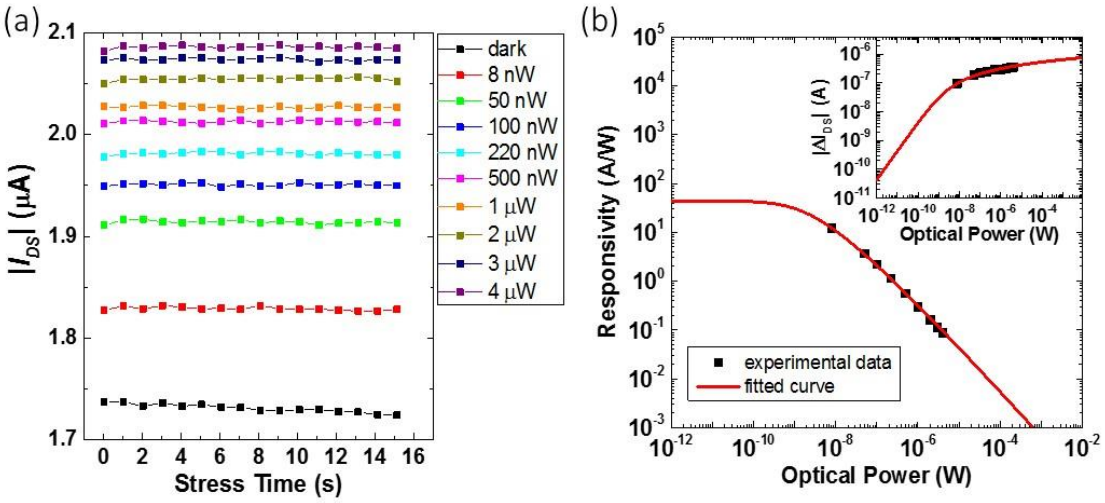


Figure 52. (a) Temporal evolution of $|I_{DS}|$ during bias-stress tests, when top electrodes of the OPDs were grounded. The tests were conducted in dark and under a 635 nm laser irradiation with different incident optical powers at the backside of the OPD. (b) The responsivity of photodetector versus incident optical power. The inset shows the I_{DS} changes due to illumination versus incident optical power.

The inset of Figure 52 (b) shows $|\Delta I_{DS}| = |I_{DS,light} - I_{DS,dark}|$ versus different optical powers, where $I_{DS,light}$ and $I_{DS,dark}$ are the experimental data of I_{DS} under illumination and in dark, respectively. The $|\Delta I_{DS}|$ is observed as a function of incident optical power P_{opt} and shows larger changes at weak illumination condition, which indicates a high sensitivity to the weak light signal. The measured values of $|\Delta I_{DS}|$ are generally above 10^{-7} A, which is around 1,000 times larger than the leakage current of OTFT, even when the P_{opt} is as low as 10^{-8} W. The light detection resolution, thus, can be as small as 10^{-8} W. Then we calculated the photoresponsivity (R) using the equation:

$$R = \frac{\left|I_{DS,light} - I_{DS,dark}\right|}{P_{opt}} \tag{19}$$

Using Equation (19), Figure 52 (b) presents the experimental data of R versus P_{opt}, and shows a significantly large photoresponsivity value that is as high as 12 A W^{-1} at a low optical power, *i.e.*, P_{opt} = 10^{-8} W.

5.6 Analytical Analysis

For a better understanding, the analytical expressions describing the conversion of the optical power to source-drain current I_{DS} changes are developed by solving for the equivalent circuit in Figure 50 (c). In Equation (18), which is the equation that describes the DG-OTFT current-voltage characteristic, V_{BG} = - V_{OC} = 0 V in dark condition, thus, the source-drain current in dark ($I_{DS,dark}$) could be expressed by Equation (18) without the term of V_{BG}. Therefore, the light-induced drain-source current change ($I_{DS,light} - I_{DS,dark}$) could be obtained as:

$$I_{DS,light} - I_{DS,dark} = k_1\left((k_2 V_{OC})^2 - 2k_2 V_{OC} V_{TG} + 2k_2 V_{OC} V_{th,eff}\right) \tag{20}$$

where $k_1 = \mu \frac{W}{2L} \frac{C_T^2}{C_T + C_B}$ and $k_2 = \frac{C_B}{C_T}$. The relation of the V_{OC} and the photocurrent density J_{ph} of an OPD is known as [93]:

$$V_{OC} = n \frac{kT}{e} \ln\left(1 + \frac{J_{ph}}{J_0}\right) \tag{21}$$

In addition, the J_{ph} is proportional to the P_{opt}, *i.e.*, $J_{ph} = \eta \frac{\lambda e}{hc} \frac{P_{opt}}{A}$, where η is the external quantum efficiency, $\frac{hc}{\lambda}$ is the incident photon energy, and A is the device active area. From Equations (20) and (21), the responsivity R could be derived:

$$R = \frac{\left|k_1\left((k_2 V_{OC})^2 - 2k_2 V_{OC} V_{TG} + 2k_2 V_{OC} V_{th,eff}\right)\right|}{P_{opt}} \tag{22}$$

with $V_{OC} = \varphi_1 \ln\left(1 + \varphi_2 P_{opt}\right)$. The fitting parameter φ_1 is proportional to $\frac{nkT}{e}$, which equals to 0.026 V with an ideality factor n = 1 at room temperature. The fitting parameter φ_2 is proportional to $\frac{\eta\lambda e}{hcAJ_0}$, which is in the range of 10^9 to 10^{10} W^{-1} in this work. The values of φ_1 and φ_2 can be obtained by fitting with the experimental data.

Table 3 A summary of device parameters obtained by fitting data shown in Figure 52 (b) with Equation (22).

Device Characteristics						**Bias Voltages**		**Fitting Parameters**	
W (μm)	L (μm)	μ ($cm^2 V^{-1} s^{-1}$)	C_T (nF cm^{-2})	C_B (nF cm^{-2})	$V_{th,eff}$ (V)	V_{TG} (V)	V_{DS} (V)	φ_1 (V)	φ_2 (W^{-1})
6050	180	0.25	37.2	150.6	-2.13	-10	-10	0.022	1.0×10^9

Hence, by fitting the experimental data with Equation (22), the values of φ_1 and φ_2 were obtained and are presented in Table 3. Table 3 also shows the other device parameters and bias voltages used in the analytical model. The same set of parameters was then used to simulate $|\Delta I_{DS}|$ versus P_{opt} using Equation (22), and the simulation results are in good agreement with the experimental data as shown in the inset of Figure 52 (b). These

simulations show that the photoresponsivity could reach values greater than 30 A W^{-1} with a weak light signal around 1 pW.

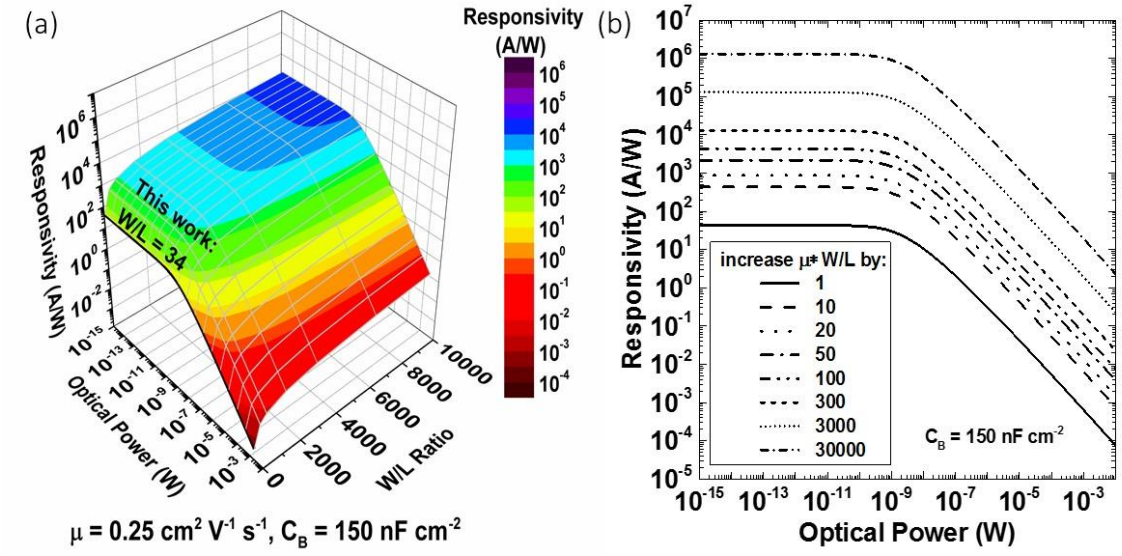


Figure 53. The simulation of the responsivity of the photodetector versus the incident optical power using Equation (22): (a) with varied W/L ratio and fixed charge mobility value presented in Table 3; (b) with increased values of μ*W/L (as presented in Table 3) by 1, 10, 20, 50, 100, 300, 3,000, and 30,000 times, while the other parameters are fixed with the values presented in Table 3.

In addition to the demonstration of the photodetector with high responsivity to weak light, we also provide a simple approach to improve the responsivity by engineering the DG-OTFT configuration. The Equation (22) clearly shows that the responsivity R is proportional to the value of φ_1 (or $\mu\frac{W}{L}$). Therefore, we first simulated the responsivity versus optical power with fixed charge mobility (μ = 0.25 cm^2 V^{-1} s^{-1}) and varied W/L ratios (ranging from 34 to 10,000) as shown in Figure 53 (a). All the other parameters were fixed with the values in Table 3. In this work, W/L = 6050 μm/180 μm = 34, and it could be easily increased by reducing the channel length or increasing the channel width by using

interdigitated electrode structures. As observed in Figure 53 (a), the responsivity could be increased to 10^5 A W^{-1} by only modifying the channel dimensions of the DG-OTFT.

On the other hand, the responsivity will be enhanced further by using high charge mobility semiconductor as an active layer instead of the one used here with the charge mobility of 0.25 cm^2 V^{-1} s^{-1}. Figure 53 (b) shows the simulation results of responsivity versus optical power with the value of $\mu \frac{W}{L}$ in this work multiplying by 1, 10, 20, 50, 100, 300, 3,000, and 30,000. This result shows the potential that the responsivity of this OTFT-based photodetector could reach up to the level of 10^8 A W^{-1}.

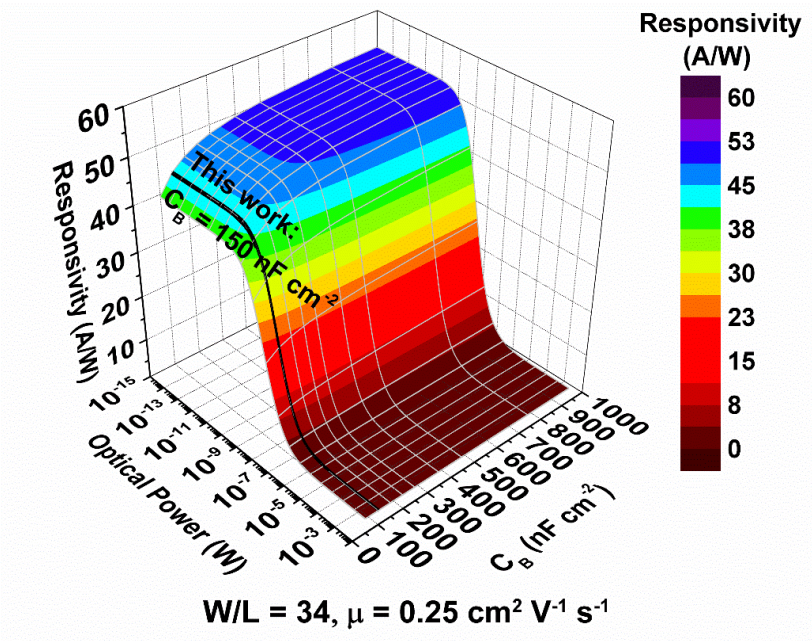


Figure 54. The simulation of the responsivity of the photodetector versus the incident optical power using Equation (22): with different bottom gate capacitance density when charge mobility value and W/L ratio are fixed as presented in Table 3.

From Equation (22), we observe other parameters, C_T and C_B, that relate to the responsivity. In general, the value of C_T is constant since the top gate dielectric origins from the previous study and shows good stability performance of OTFTs. Here, we studied

the impact of the capacitance density of the bottom gate dielectric, C_B, which could be changed by the dielectric constant of the material and thickness of the dielectric layer. In Figure 54, the responsivity versus optical power with varied C_B was simulated using Equation (22). All the other parameters were fixed with the values in Table 3. As a result, the responsivity slightly increased by around 1.2 times when C_B increased by 10 times; the C_B has much smaller impacts on the responsivity than the value of $\mu\frac{W}{L}$. Therefore, to achieve high responsivity, more efforts should be put on adjusting the W/L ratio and improving the charge mobility of a DG-OTFT.

5.7 Response Time

Next, we focus our attention on the response time of the photodetector. Figure 49 shows the normalized response of I_{DS} changes with an OPD under radiation of a surface mounted LED illumination at square waveform with on/off frequencies of 0.2 Hz, 1 Hz, and 5 Hz. The OTFT was continuously biased at V_{TG} = -10 V and V_{DS}= -6 V and the changes of channel current with the light signal from the LED was observed. The measurement data are acquired at every 15 ms, which is the smallest time interval of the equipment. The rise and fall time of the I_{DS} waveform is faster than the measurement resolution, in this case, indicating that the response frequency of photodetector is less than 100 Hz level which is comparable to the response frequency of the OPD and compatible with video rate requirements. The result of the fast response indicates a possibility for the photodetector to be widely used in applications; especially has a significant impact on the low radiance detection using low-cost and flexible optical organic materials.

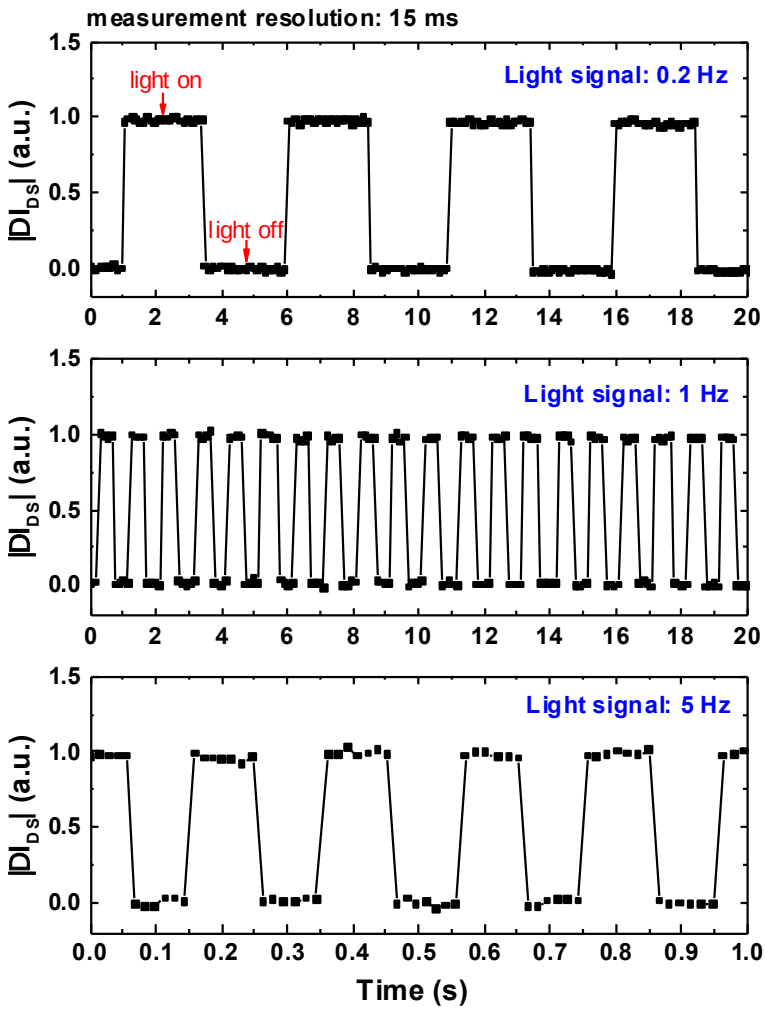


Figure 55. Response of I_{DS} changes under radiation of LED illumination at different on/off frequencies.

5.8 Summary

In summary, we demonstrated a high-sensitivity organic photodetector with a novel configuration that is comprised of a DG-OTFT and an OPD. The DG-OTFT exhibited not only low leakage current without hysteresis but also excellent operational stability. The OTFT-based photodetector in work showed a short response time (< 15 ms) as well as a

high photoresponsivity (around 10 A W^{-1}) to the weak light signal with an optical power around 10^{-8} W. In order to study the device working principle, we derived an analytic model which describes the electrical and optical operation of the OTFT-based photodetectors. With this model, we proposed a simple approach to improve the photoresponsivity, especially to the weak light signal with low optical power (around nanowatt level). The photoresponsivity could be easily improved by modifying the channel dimensions or the charge mobility of DG-OTFTs. Thus, this novel organic photodetector would have great potential for weak irradiance detection.

CHAPTER 6. CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusions

In this dissertation, an exhaustive study on the characterization of OTFTs with a bilayer gate dielectric has been reported in Chapter 4. In the past, our previous group members developed the bilayer gate dielectric structure of the OTFT to increase the device stability. They discovered that the bilayer gate dielectric could be engineered to balance the effects of two opposite mechanisms causing the shifts of V_{TH} in different directions. This compensation of two mechanisms led to OTFTs exhibiting improved operational stability. Moreover, when the second dielectric layer of an OTFT consists of an Al_2O_3 layer and an Al_2O_3 and HfO_2 nanolaminate grown by ALD, the OTFT device remained functional after being immersed in water at 95 ^oC for more than one hour. Based on these previous results, in this work, we further improved the environmental and operational stability of the OTFT by using a bilayer gate dielectric consisting of a CYTOP layer and an Al_2O_3 and HfO_2 nanolaminate, with optimized thicknesses. We achieved less than 4% changes in the channel current in one hour of bias stress after exposing to the environment with 85% humidity at 85 ^oC for 24 h or immersing in water for 16 h. These results showed an unprecedented level of environmental stability in these OTFTs. In addition, we achieved the maximum threshold voltage shifts that are smaller than 0.5 V after more than a hundred hours of bias stress at room temperature. These shifts were at least an order of magnitude smaller than those expected from the state-of-the-art OTFTs at that time. Although it is clear that further studies will be necessary to improve our understanding of the physical mechanisms giving rise to the temporal and thermal dependence of the V_{TH} shifts, we

proved that the metal oxide layer thickness can be effectively used to tailor the aging effects in OTFTs, and the temporal dynamics of V_{TH} can be modeled by two competing processes that appear to show similar dynamics and magnitude in bilayers of CYTOP and Al2O3: HfO2 NL. Using a double stretched exponential model, the extrapolated V_{TH} shifts at the temperature of 50 - 55 °C achieved values that were nearly two orders of magnitude smaller than those expected in commercial *a*-Si TFTs and comparable or superior to those found in *a*-IGZO TFTs and LT *poly*-Si TFTs. With this level of stability, we believe that these OTFT devices have great potential in applications, such as sensing systems.

Furthermore, we demonstrated a new type of organic photodetectors by integrating a DG-OTFT with an OPD, which has been discussed in Chapter 5. In this work, we developed the new device structure of the photodetector, in which the OPD device was used to generates a voltage signal under light illumination, and this voltage signal could be amplified by the DG-OTFT. Based on the structure of the highly stable OTFTs with bilayer gate dielectrics that was reported in Chapter 4, we demonstrated that these DG-OTFT devices exhibited low leakage current without hysteresis and showed excellent operational stability under bias stress tests. Compared to the traditional OPDs or OPTs, this whole photodetector achieved a great improvement in light detection performance, in terms of a high photoresponsivity (> 10 A W^{-1}) to a weak light signal (P_{opt} is around 10^{-8} W) and shorter response time (< 0.2 s). Also, we believe that this novel photodetector would have big potential for weaker light signal detection, which was confirmed by simulating with a theoretical model. Furthermore, we proposed a simple method to further improve the photoresponsivity by modifying the geometry and charge mobility of the DG-OTFT. These

results paved the road for developing the high-performance, low-cost, light-weight, flexible, and stable photodetector for the next generation of consumer electronics.

6.2 Recommendations for Future Work

The work presented in this dissertation can be extended in several directions for future study.

6.2.1 OTFT-based Photodetectors in a Vertical Structure

In Chapter 5, we demonstrated the OTFT-based photodetector in a lateral structure, as shown in Figure 48 (a). However, the device in a vertical structure, as shown in Figure 48 (b) was not able to be fabricated due to the process issue. The biggest problem was the dissolving of the semiconductor layer of the OPD when spin-coating the active layer of the OTFT. Hence, the interlayer between these two semiconductor layers is important since it serves as the bottom-gate dielectric layer of the OTFT as well as the passivation layer of the OPD to prevent the OPD structures from dissolving. The optimization of this interlayer could be further explored in future study.

In addition, from the simulation results shown in Figure 53, the responsivity of the photodetector can be easily increased by increasing the width-to-length ratio of the transistor. Therefore, the interdigitated electrodes could be used as the source and drain electrodes of the OTFTs. The proposed device structure is shown in Figure 56. The OPD

device is sandwiched between the conductive transparent substrate and the bottom-gate dielectric, such that it will generate the V_{OC} under the light illumination and apply the V_{OC} as the bottom-gate voltage on the DG-OTFT, which in turn modulates the channel current of the DG-OTFT. The interdigitated source and drain electrodes are used to enhance the photoresponsivity. Also, the high charge mobility materials can be explored and used as the semiconductor layer of the transistor, to improve the photoresponsivity further.

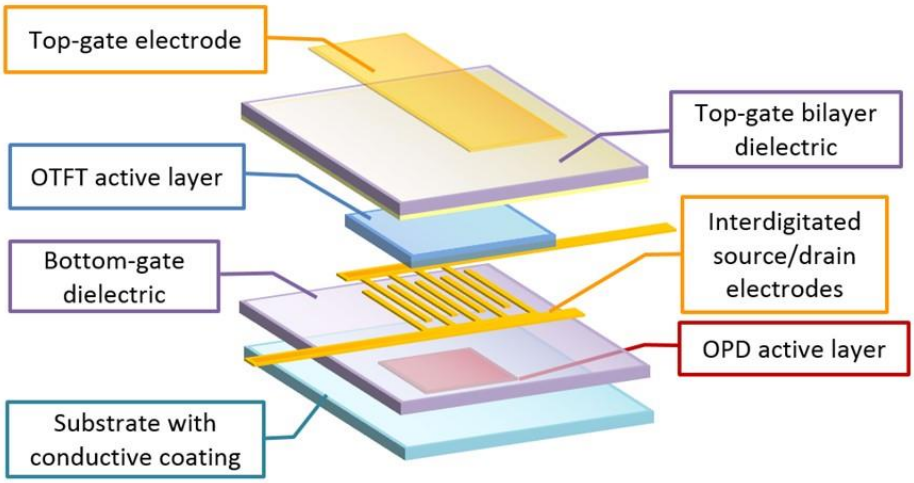


Figure 56. The vertical structure of the OTFT-based photodetectors with interdigitated source and drain electrodes.

6.2.2 Pixel Array Design

With the single photodetector device, the pixel array could be designed in the future, to realize more applications, such as imaging and movement detections. The device structure of one pixel is shown in Figure 56. Figure 57 (a) shows the schematic of the pixel array concept and Figure 57 (b) shows the associated circuit schematic. When a specific top-gate voltage applies on one pixel, the channel current flow changes will be readable.

Therefore, the pixel array is addressable by the top-gate electrode of the DG-OTFT in each column to control each pixel detector on and off. The signal could be read through the drain electrodes in each row. In this way, this pixel array could be easily scaled using current mass production techniques, such as roll-to-roll printing, which opens the possibility of low-cost, low-energy, high-performance, and large-area imaging sensors.

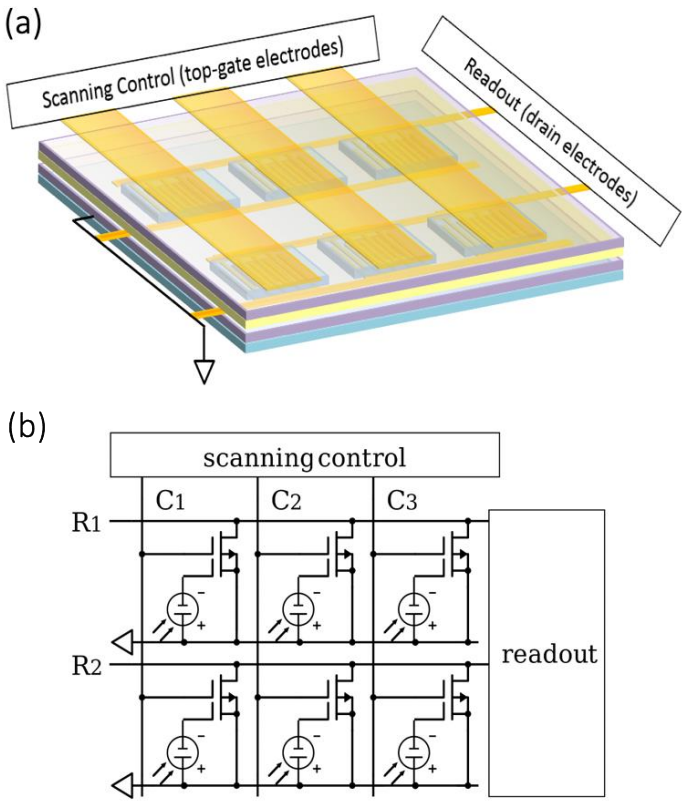


Figure 57. (a) The schematic view of the pixel array design using the concept of the novel photodetector geometry. (b) The associated circuit schematic of the pixel array design.

6.2.3 Other Detection Applications

The photodetector platform in Chapter 5 also could be used in other signal detection applications. One of the promising applications is the real-time high energy ionizing-radiation detection. For example, Figure 58 (a) shows the device structure of an organic radiation field-effect transistor (RADFET), which is designed based on a silicon RADFET [95]. The only difference from the OTFT-based photodetector is that the organic RADFET has a radiation interactive layer that replaces the OPD part below the OTFT. The radiation interactive layer can generate an electrical signal under ionizing radiation. This device is designed to capture and retain radiation-induced charges. In device design, except for the radiation interactive layer, the other components in the detector are required to be radiation-insensitive. Therefore, the shift of threshold voltages under radiation would reflect the radiation dose level, as shown in Figure 58 (b).

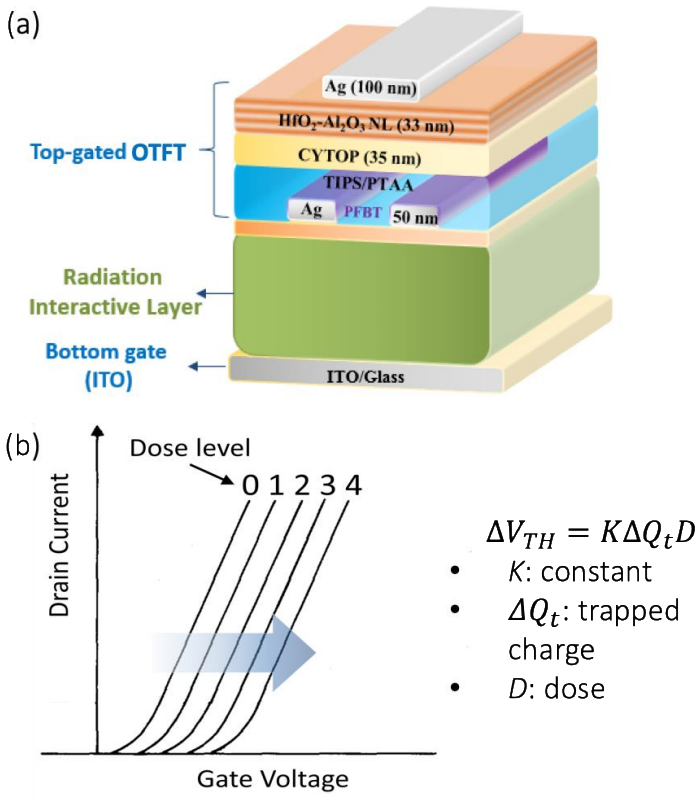


Figure 58. (a) The device structure of a proposed organic radiation field-effect transistor (RADFET). (b) The threshold voltage shifts with radiation dose levels.

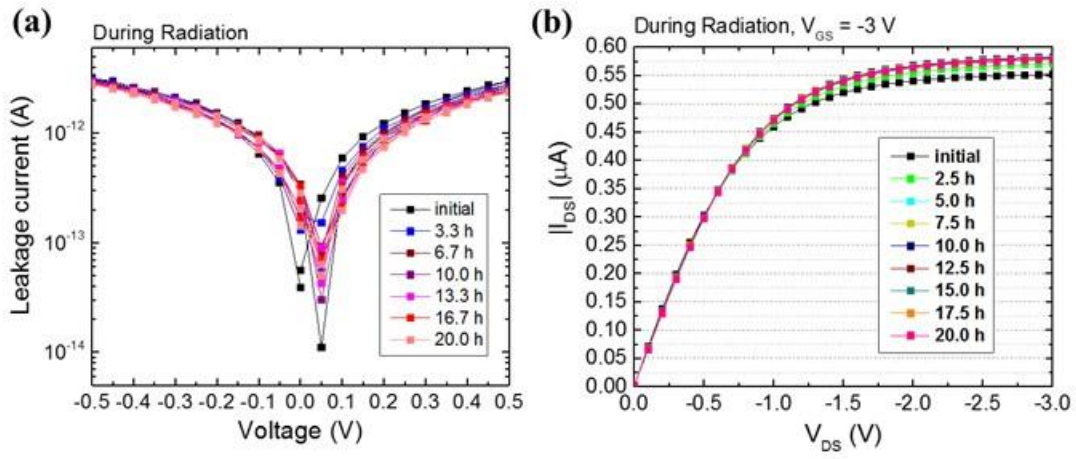


Figure 59. (a) The leakage current of a bilayer gate dielectric. (b) The *I-V* output curves measured during 20 h continuous exposure to an AmBe ionization source.

Organic TFTs are expected to be less sensitive to the radiation than Si electronics. The radiation hardness tests of the OTFTs with the device structure of A_33 in Figure 28 (b) were conducted with an americium-beryllium (AmBe) source, which emits gamma rays and neutrons at a rate of 1.19×10^8 neutrons s^{-1}. We observed the characteristics of the devices during 20 h radiation exposure to the AmBe ionization source. Figure 59 (a) shows the leakage current of a capacitor comprised of the CYTOP and Al_2O_3-HfO_2 NL bilayer dielectric with an active area of 0.1 cm^2. Figure 59 (b) shows the *I-V* output curves of an OTFT device at a fixed gate voltage of -3 V under radiation. The dielectric leakage current was monitored at every 3.3 h, and the *I-V* output curves were monitored at every 2.5 h during exposure to the AmBe source for 20 hours. We observed little changes in the electrical characteristics of the OTFT gate dielectric layer and the whole OTFT device after 20 h exposure, indicating that the OTFTs have good stability under high-energy radiation.

Therefore, the remaining work would be the investigation of the radiation interactive material that could generate an electrical signal in ionizing radiation.

6.3 Publications

[1] **X. Jia**, C. Fuentes-Hernandez, C.-Y. Wang, Y. Park, and B. Kippelen, "Stable organic thin-film transistors," *Science Advances,* vol. 4, no. 1, 2018.

[2] **X. Jia**, C. Fuentes-Hernandez, and B. Kippelen, "Stable Thin-Film Transistors," U.S. Patent Application No. 62/768,483, filed on November 16, 2018.

[3] K. Kim, **X. Jia**, C. Fuentes-Hernandez, B. Kippelen, S. Graham, and O. N. Pierron, "Optimizing Crack Onset Strain for Silicon Nitride / Fluoropolymer Nanolaminate Barrier Films," *ACS Applied Nano Materials*, 2019.

[4] C. Fuentes-Hernandez, W.-F. Chou, **X. Jia**, and B. Kippelen, "A Method to Produce High-Sensitivity Stable Sensors," U.S. Patent Application No. 62/803,360, filed on February 08, 2019.

[5] Y. Park, C. Fuentes-Hernandez, **X. Jia**, F. A. Larrain, J. Zhang, S. R. Marder, and B. Kippelen, "Measurements of the field-effect electron of the acceptor ITIC," *Organic Electronics,* vol. 58, pp. 290-293, 2018.

APPENDIX A.

Fitting Parameters with Bias Stress Effect Models

Table 4 A summary of lifetime parameters of OTFTs using the SSE model. The lifetime parameters of TFTs are obtained by fitting the measurement data in Figure 35 and Figure 36 with Equation (12), (15), and (16), and from the literature.

Semiconductor	Gate dielectric	Regime	$V_{GS} - V_{TH}(0)$ (V)	$\Delta V_{TH,1\infty}$ (V)	τ_1 (s)	β_1
TIPS/PTAA (this work)	A_33: CYTOP/NL (35/33 nm)	Saturation	-8.0	-11.84	2.50×10^{11}	0.302
		Linear	-8.0	-8.40	1.66×10^{10}	0.299
	A_27: CYTOP/NL (35/27.5 nm)	Saturation	-7.4	-3.92	7.76×10^{7}	0.296
	A_22: CYTOP/NL (35/22 nm)	Saturation	-7.0	-6.20	3.92×10^{5}	0.626
	B_44: CYTOP/Al_2O_3/NL (35/20/44 nm)	Saturation	-7.0	-2.24	4.62×10^{7}	0.548
	B_22: CYTOP/Al_2O_3/NL (35/20/22 nm)	Saturation	-7.2	-4.90	2.44×10^{9}	0.350
	B_11: CYTOP/Al_2O_3/NL (35/20/11 nm)	Saturation	-7.3	-7.52	4.77×10^{9}	0.322
TIPS/PTAA [38]	CYTOP	Saturation	-25	-5.25	6.07×10^{4}	0.527
PDIF-CN_2 (single-crystal) [17]	CYTOP/SiO_2	Linear	80	80	4.7×10^{9}	0.38
***a*-Si [11]**	SiN_x	Linear	30	30	3.2×10^{6}	0.39

Table 5 A summary of lifetime parameters of OTFTs using the DSE model. The lifetime parameters are obtained by fitting the measurement data in Figure 35 and Figure 36 with Equation (14), (15), and (16).

Sample No.	Regime	$V_{GS} - V_{TH}(0)$ (V)	$\Delta V_{TH,1\infty}$ (V)	τ_1 (s)	β_1	$\Delta V_{TH,2\infty}$ (V)	m	τ_2 (s)	β_2	Chi-Sqr.
A_33	Saturation	-8.0	-6.16	7.92×10^4	0.532	6.17	1.002	7.12×10^4	0.541	1.09×10^{-7}
	Linear	-8.0	-4.85	10.53×10^4	0.575	5.04	1.039	9.32×10^5	0.598	3.43×10^{-6}
A_27	Saturation	-7.4	-6.66	7.20×10^4	0.582	6.51	0.977	8.42×10^4	0.617	2.48×10^{-6}
A_22	Saturation	-7.0	-6.23	5.13×10^4	0.484	4.78	0.767	8.75×10^4	0.402	2.09×10^{-6}
B_44	Saturation	-7.0	-5.60	8.50×10^4	0.562	5.78	1.032	8.86×10^4	0.561	2.73×10^{-7}
B_22	Saturation	-7.2	-5.90	8.28×10^4	0.592	5.62	0.953	8.05×10^4	0.600	1.80×10^{-7}
B_11	Saturation	-7.3	-5.85	7.92×10^4	0.447	5.30	0.906	6.84×10^4	0.457	1.90×10^{-6}

Table 6 A summary of OTFTs lifetime parameters at different temperatures using the DSE model. The parameters are obtained by fitting the measurement data in Figure 40 for on-state and off-state temperature stress to Equation (14).

DC-bias	Temp.	$\Delta V_{TH,1\infty}$ (V)	τ_1 (s)	β_1	$\Delta V_{TH,2\infty}$ (V)	m	τ_2 (s)	β_2	Chi-Sqr.
On-state	27 °C	-6.50	1.98×10^4	0.537	6.38	0.982	1.92×10^4	0.543	5.96×10^{-5}
	55 °C	-6.50	6.43×10^4	0.463	6.33	0.974	6.38×10^4	0.469	1.57×10^{-4}
	75 °C	-7.95	7.53×10^2	0.496	7.75	0.975	6.87×10^2	0.507	7.30×10^{-4}
Off-state	27 °C	-6.27	1.99×10^3	0.718	6.18	0.986	1.95×10^3	0.723	1.63×10^{-5}
	55 °C	-6.46	5.78×10^2	0.751	6.35	0.983	5.69×10^2	0.761	9.19×10^{-6}
	75 °C	-6.28	5.37×10^2	0.619	6.05	0.963	5.00×10^2	0.630	3.21×10^{-4}

Table 7 A summary of lifetime parameters of OTFTs extracted from V_{TH} shifts using the DSE model. The lifetime parameters obtained by fitting data shown in Figure 43 (a) with Equation (14).

Sample No.	$\Delta V_{TH,1\infty}$ (V)	τ_1 (s)	β_1	$\Delta V_{TH,2\infty}$ (V)	m	τ_2 (s)	β_2	Chi-Sqr.
A_33	-6.51	4.71×10^4	0.582	6.50	0.998	5.00×10^4	0.579	3.03×10^{-4}
C_33	-6.06	5.50×10^4	0.513	6.29	1.038	5.92×10^4	0.517	9.56×10^{-5}

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